Journal of
Low Power Electronics and Applications

Special Issue Reprint

Ultra-Low-Power ICs for the Internet of Things (2nd Edition)

Edited by
Orazio Aiello

mdpi.com/journal/jlpea

MDPI

Ultra-Low-Power ICs for the Internet of Things (2nd Edition)

Ultra-Low-Power ICs for the Internet of Things (2nd Edition)

Guest Editor

Orazio Aiello

MDPI

Basel • Beijing • Wuhan • Barcelona • Belgrade • Novi Sad • Cluj • Manchester

Guest Editor
Orazio Aiello
Department of Electrical,
Electronic,
Telecommunications
Engineering and Naval
Architecture (DITEN)
University of Genoa
Genova
Italy

Editorial Office
MDPI AG
Grosspeteranlage 5
4052 Basel, Switzerland

This is a reprint of the Special Issue, published open access by the journal *Journal of Low Power Electronics and Applications* (ISSN 2079-9268), freely accessible at: https://www.mdpi.com/journal/jlpea/special_issues/919Q5756T0.

For citation purposes, cite each article independently as indicated on the article page online and as indicated below:

Lastname, A.A.; Lastname, B.B. Article Title. *Journal Name* **Year**, *Volume Number*, Page Range.

ISBN 978-3-7258-6734-9 (Hbk)
ISBN 978-3-7258-6735-6 (PDF)
https://doi.org/10.3390/books978-3-7258-6735-6

Contents

About the Editor

Orazio Aiello

Orazio Aiello received a B.Sc. and M.Sc. (cum laude) from the University of Catania, Italy, in 2005 and 2008, respectively; an M.Sc. (cum laude) from the Scuola Superiore di Catania, Italy, in 2009; and a Ph.D. from the Politecnico di Torino, Italy, in 2013. He gained his technical background in worldwide universities' R&D institutions, as well as through consultant activities and direct work experience in semiconductor companies. He is currently an Associate Professor at the University of Genoa, Italy. His main research interests include energy-efficient analog mixed-signal circuits and sensor interfaces.

Journal of
Low Power Electronics and Applications

MDPI

Editorial

Ultra-Low-Power ICs for the Internet of Things (2nd Edition)

Orazio Aiello

Department of Electrical, Electronics and Telecommunication Engineering and Naval Architecture (DITEN), University of Genoa, 16100 Genova, Italy; orazio.aiello@unige.it

After the success of the first edition [1], we are delighted to launch this second edition of our Special Issue focusing on Ultra-Low-Power (ULP) Integrated Circuits (ICs) operating within a tight power budget, which represent an essential element in building electronic devices that rely less and less on batteries. Our aim is, once again, to present novel IC design strategies to reduce the cost and power consumption of devices.

In this Special Issue, Tran et al., Pham et al., and Namdari et al. (Contributions 1–3) discuss IC solutions for biomedical applications. In particular, two capacitively coupled chopper instrumentation amplifiers (CCIAs) are presented as part of a 180 nm technology process for monitoring neural potentials. Tran et al. present a chopping ripple reduction to 0.36 mV, with an overall area of 0.123 mm^2 and a power consumption of 1.87 μW at a supply voltage of 1 V. Pham et al. show a programmable bandwidth from 0.2 to 10 kHz in an area of 0.083 mm^2 and an overall power consumption of 0.47 μW with two supply voltages at 0.2 V and 0.8 V.

A compact, universal, multi-mode Gm-C filter centered at 462 Hz using a 180 nn, with a supply voltage of 0.5 V, resulting in a power consumption of 32 nW, is reported in the work by Namdari et al. (Contribution 3). The work by Nicolini et al. (Contribution 4) presents a 16-channel in-pixel neural analog front end, enhancing both the system common-mode rejection ratio (SCMRR) and the common-mode interference (CMI) range with a power consumption of 3.77 μW per channel in 180 nm technology nodes.

This Special Issue then addresses general-purpose IC blocks (i.e., Contributions 5–8).

Wang et al. (Contribution 5) design a novel low-power MOS-only voltage reference, showing 21.7 ppm/°C of variation in a temperature range from −40 °C to 120 °C, consuming 23.2 nW with a supply voltage of 0.8 V in 55nm technology nodes.

Morell et al. (Contribution 6) propose a novel, stepwise charging driver circuit for four-phase adiabatic logic and validate it through an analysis in 15 nm FinFET technology nodes.

The work by Shah et al. (Contribution 7) describes a bulk-driven second-generation Current Conveyor (CCII) operating at 0.35 V, offering a linear current drive up to 2.5 μA, while consuming a total quiescent current of 2.86 μA.

Della Sala et al. (Contribution 8) report an approach to designing digital-based operational transconductance amplifiers (OTAs) by ensuring that the gates operate with a well-defined quiescent current and output voltage, meaning that they are resistant to PVT variations.

Regarding security applications, in their article, Zheng et al. (Contribution 9) propose an 8-Transistor (8T) power-gated Physically Unclonable Function (PUF) implemented in 65 nm technology, built to swiftly eliminate data remanence and maximize physical mismatch.

Among the faster and thus more power-hungry solutions, Naveed et al. (Contribution 10) present a multiplier and Siddiqui et al. (Contribution 11) present a VCO. Contribution 10 reports a delay-locked loop (DLL)-based frequency 8× multiplier with

a 22 nm FDSOI power consumption of 130 μW at 0.8 V supply with a new simple duty cycle correction circuit that is XOR logic-based for frequency multiplication. In Contribution 11, a tunable quadrature differential LC CMOS voltage-controlled oscillator (VCO) with a D flip-flop (DFF) frequency divider, consuming 2.02 mW with a tuning range of 4.4 to 5.7 GHz and showing a phase noise of −118.36 dBc/Hz at a 1 MHz offset frequency with a 1.2 V supply voltage, is designed through a 65 nm technology process.

Last, but not least, Baker et al. (Contribution 12) review advancements in wireless short-range communication (i.e., Bluetooth, RFID, and NFC), adding further value to this second Special Issue volume.

In summary, these research publications explore a wide array of prospects inspired by these innovative designing techniques, covering a broad range of areas in the ULP/ULV IC field.

Acknowledgments: As the Guest Editor of this Special Issue, "Ultra-Low-Power ICs for the Internet of Things (2nd Edition)", I would like to thank MDPI for the invitation to write this Editorial and introduce the 12 contributions. This Special Issue is freely available to read at https://www.mdpi.com/journal/jlpea/special_issues/919Q5756T0 (accessed on 16 September 2025). Moreover, based on the success of this Special Issue, a third edition has been launched at https://www.mdpi.com/journal/jlpea/special_issues/5X3201Q4L8 (accessed on 16 September 2025).

Conflicts of Interest: The author declares no conflicts of interest.

List of Contributions:

1. Tran, X.P.; Kieu, X.T.; Pham, X.T.; Pham, D.P.; Hoang, M.K. A 1.87 μW Capacitively Coupled Chopper Instrumentation Amplifier with a 0.36 mV Output Ripple and a 1.8 GΩ Input Impedance for Biomedical Recording. *J. Low Power Electron. Appl.* **2024**, *14*, 37. https://doi.org/10.3390/jlpea14030037.
2. Pham, X.T.; Kieu, X.T.; Hoang, M.K. Ultra-Low Power Programmable Bandwidth Capacitively-Coupled Chopper Instrumentation Amplifier Using 0.2 V Supply for Biomedical Applications. *J. Low Power Electron. Appl.* **2023**, *13*, 37. https://doi.org/10.3390/jlpea13020037.
3. Namdari, A.; Aiello, O.; Caviglia, D.D. A 0.5 V, 32 nW Compact Inverter-Based All-Filtering Response Modes Gm-C Filter for Bio-Signal Processing. *J. Low Power Electron. Appl.* **2024**, *14*, 40. https://doi.org/10.3390/jlpea14030040.
4. Nicolini, G.; Fava, A.; Centurelli, F.; Scotti, G. A 0.064 mm2 16-Channel In-Pixel Neural Front End with Improved System Common-Mode Rejection Exploiting a Current-Mode Summing Approach. *J. Low Power Electron. Appl***.** **2024**, *14*, 38. https://doi.org/10.3390/jlpea14030038.
5. Wang, S.; Lu, Z.; Xu, K.; Dai, H.; Wu, Z.; Yu, X. A Sub-1-V Nanopower MOS-Only Voltage Reference. *J. Low Power Electron. Appl.* **2024**, *14*, 13. https://doi.org/10.3390/jlpea14010013.
6. Morell, W.; Choi, J.-W. Design and Analysis of Self-Tanked Stepwise Charging Circuit for Four-Phase Adiabatic Logic. *J. Low Power Electron. Appl.* **2024**, *14*, 34. https://doi.org/10.3390/jlpea14030034.
7. Shah, M.O.; Caruso, M.; Pennisi, S. 0.35 V Subthreshold Bulk-Driven CMOS Second-Generation Current Conveyor. *J. Low Power Electron. Appl.* **2024**, *14*, 36. https://doi.org/10.3390/jlpea14030036.
8. Della Sala, R.; Centurelli, F.; Scotti, G. An Ultra-Low-Voltage Approach to Accurately Set the Quiescent Current of Digital Standard Cells Used for Analog Design and Its Application on an Inverter-Based Operational Transconductance Amplifier. *J. Low Power Electron. Appl.* **2024**, *14*, 39. https://doi.org/10.3390/jlpea14030039.
9. Zheng, Y.; Yakovlev, A.; Bystrov, A. A Power-Gated 8-Transistor Physically Unclonable Function Accelerates Evaluation Speeds. *J. Low Power Electron. Appl.* **2023**, *13*, 53. https://doi.org/10.3390/jlpea13040053.
10. Naveed; Dix, J. Design of a Low-Power Delay-Locked Loop-Based 8× Frequency Multiplier in 22 nm FDSOI. *J. Low Power Electron. Appl.* **2023**, *13*, 64. https://doi.org/10.3390/jlpea13040064.

11. Siddiqui, M.F.; Maheshwari, M.K.; Raza, M.; Masud, A.R. Design and Optimization of an Ultra-Low-Power Cross-Coupled LC VCO with a DFF Frequency Divider for 2.4 GHz RF Receivers Using 65 nm CMOS Technology. *J. Low Power Electron. Appl.* **2023**, *13*, 54. https://doi.org/10.3390/jlpea13040054.
12. Baker, B.; Woods, J.; Reed, M.J.; Afford, M. A Survey of Short-Range Wireless Communication for Ultra-Low-Power Embedded Systems. *J. Low Power Electron. Appl.* **2024**, *14*, 27. https://doi.org/10.3390/jlpea14020027.

Reference

1. Ultra-Low-Power ICs for the Internet of Things. Available online: https://www.mdpi.com/journal/jlpea/special_issues/low_power_iot (accessed on 16 September 2025).

Journal of
Low Power Electronics and Applications

MDPI

Article

A 1.87 μW Capacitively Coupled Chopper Instrumentation Amplifier with a 0.36 mV Output Ripple and a 1.8 GΩ Input Impedance for Biomedical Recording †

Xuan Phuong Tran [1], Xuan Thuc Kieu [1], Xuan Thanh Pham [1], Duy Phong Pham [2] and Manh Kha Hoang [1,*]

[1] Faculty of Electronics Engineering, Hanoi University of Industry, Hanoi 100000, Vietnam; phuongtx@haui.edu.vn (X.P.T.); thuckx@haui.edu.vn (X.T.K.); thanhpx@haui.edu.vn (X.T.P.)
[2] Faculty of Electronic and Telecommunication Engineering, Electric Power University, Hanoi 100000, Vietnam; phongphd@epu.edu.vn
* Correspondence: khahoang@haui.edu.vn; Tel.: +84-24-3765-5121
† This paper is an extended version of our paper published in 2023 International Conference on Advanced Technologies for Communications (ATC).

Abstract: Chopper and capacitively coupled techniques are employed in instrumentation amplifiers to create capacitively coupled chopper instrumentation amplifiers (CCIAs) that obtain a high noise power efficiency. However, the CCIA has some disadvantages due to the chopper technique, namely chopper ripple and a low input impedance. The amplifier can easily saturate due to the chopper ripple of the CCIA, especially in extremely low noise problems. Therefore, ripple attenuation is required when designing CCIAs. To record biomedical information, a CCIA with a low power consumption and a low noise, low output ripple, and high input impedance (Z_{in}) is presented in this paper. By introducing a ripple attenuation loop (RAL) including the chopping offset amplifier and a low pass filter, the chopping ripple can be reduced to 0.36 mV. To increase the Z_{in} of the CCIA up to 1.8 GΩ, an impedance boost loop (IBL) is added. By using 180 nm CMOS technology, the 0.123 mm^2 CCIA consumes 1.87 μW at a supply voltage of 1 V. According to the simulation results using Cadance, the proposed CCIA architecture achieves a noise floor of 136 $nV/\sqrt{Hz}$, an input-referred noise (IRN) of 2.16 μV_{rms}, a closed-loop gain of 40 dB, a power supply rejection ratio (PSRR) of 108.6 dB, and a common-mode rejection ratio (CMRR) of 118.7 dB. The proposed CCIA is a helpful method for monitoring neural potentials.

Keywords: low power; chopper amplifier; ripple attenuation; input impedance

1. Introduction

Wireless biomedical sensors (WBSs) are increasingly used to track our daily activities in order to detect cardiovascular diseases at an early stage [1–4]. Monitoring human biopotential requires the use of low-power sensors deployed in wearable or implantable systems. Researchers are currently developing brain–computer interfaces for numerous applications such as long-term monitoring, sports, rehabilitation, mobile monitoring, and improving the quality of life of patients [5,6]. WBSs typically use an instrumentation amplifier (IA) with low power consumption and low noise to connect with many types of biological sensors. The electrocardiograms (ECGs) of the heart and the electroencephalograms (EEGs) of the brain are examples of these biopotential signals. Neuroscience research and therapy can benefit from the use of biomarkers such as action potentials (APs) and local field potentials (LFPs) [7–9]. Biopotential signals often have an extremely small amplitude. For example, the amplitude range of an EEG is from 10 to 100 μV and that of an ECG is about 1 mV. The frequency range of the biopotential signals is 0.5–150 Hz [7,8]. The amplitude of the AP and LFP signals is about 100 μV to 1 mV, with a frequency range of 0.2 to 10 kHz for APs, and 1 to 200 Hz for LFPs [9]. Consequently, before signal processing is applied, these

neural signals need to be amplified. A wearable biomedical sensor, constructed as shown in Figure 1, provides these neurological signals.

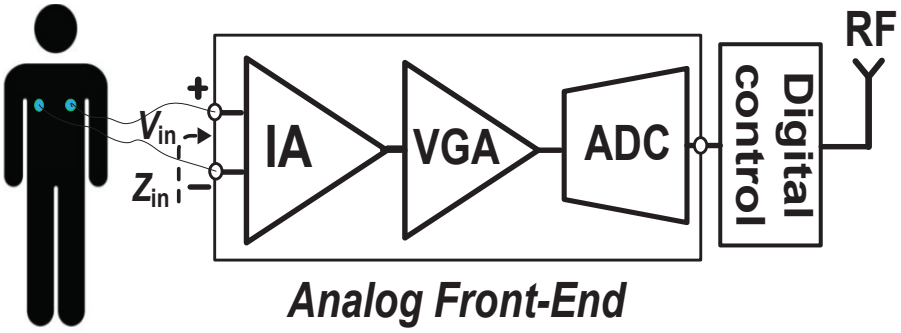


Figure 1. System architecture of a typical wireless sensor biomedical system.

The first stage measures the amplitude of the small bio signal with a dry or wet electrode. An analog front-end, consisting of an IA at the first stage, a variable gain amplifier (VGA) at the middle stage, and an analog-to-digital converter (ADC) at the last stage, processes the neural signal in the second stage before it is transmitted by RF. The preamplifier of the analog front-end must obtain a high input impedance (Z_{in}) to reduce the DC input current that could cause tissue damage [8]. The IA must likewise demonstrate a low power, low noise, high-power supply rejection ratio (PSRR), and common-mode rejection ratio (CMRR) to eliminate noise from the power line and environmental factor, which may be important in some cases.

The chopping technique is frequently used in IA [10–17] to create an IA with a high PSRR, CMRR, and noise efficiency. The input capacitance and the switches in the chopper block generate the switched capacitance resistor, which is inversely proportional to the chopper frequency. This leads to a limitation of the Z_{in} of the amplifier if there are no impedance boosting techniques [18]. The ripple appears as a triangular wave affecting the quality of the signal of interest caused by a modulated intrinsic offset [19–21]. Furthermore, for long-term battery life suitable for WBS applications, the power consumption of the IC must be as small as possible, and the noise must also be low so as not to affect the signal quality at the output of the IC. Although a number of biomedical amplifiers with low power consumption have been published, it has not yet been possible to improve the output ripple or Z_{in}. For example, in 2020, the chopper amplifier in [22] consumed 3.24 µW at a 1.8 voltage supply, the Z_{in} just reached 440 MΩ, while the ripple suppression technique used an AC coupling capacitor, which caused this design to be affected by the noise folding [19]. In 2021, the current-reuse instrumentation amplifier [23] dissipated 5.94 µW at a voltage supply of 1.8 V to achieve a Z_{in} of 2.6 GΩ without any ripple suppression approaches. In 2024, although the amplifier [24] consumed only 2.47 µW from a 1.5 V supply, the output ripple and Z_{in} were not improved.

This paper presents a CCIA for biomedical information recording that is characterized by low noise, high input impedance, low output ripple, and low power consumption. At 1 V, the 0.123 mm^2 CCIA, which was simulated using a 180 nm CMOS process, consumes 1.87 µW. According to simulation results, it is shown that the output ripple being reduced to 0.36 mV is achieved with an RAL being switched on, and the Z_{in} of the CCIA increases up to 1.8 GΩ when the impedance boost loop (IBL) is active. When both the RAL and IBL are activated, the proposed CCIA obtains a closed-loop gain of 40 dB, an input referred noise (IRN) of 1.81 μV_{rms}, a thermal noise of 136 $nV/\sqrt{Hz}$, a common mode rejection ratio (CMRR) of 118.7 dB, and a power supply rejection ratio (PSRR) of 108.6 dB. Achieving a noise efficiency factor (NEF) of 6.8 and 7.5 with both RAL and IBL turned off and on, respectively, demonstrates that the CCIA records biomedical information successfully.

2. Design

The proposed CCIA for biomedical monitoring applications with a low output ripple and a high Z_{in}, as shown in Figure 2, consists of the main channel and three auxiliary loops such as a negative feedback loop (FBL), a ripple attenuation loop (RAL), and an impedance boosting loop (IBL) in order to solve the main problems of biopotential amplifiers. The transconductance input stage (G_{m1}) of the main path is a dual-folded cascode amplifier (DFC) with a biased current of 1.2 µA. In order to attain a working stability and a high swing, the G_{m3} used a common source (CS) amplifier, combined with a Miller capacitor of 1.5 pF. A bias current of 1.8 µA is used for the channel and global common mode feedback (CMFB) from a V_{DD} of 1 V. The CCIA has a closed-loop gain of 40 dB, which is defined by the ratio of the input and negative feedback capacitors. In this design, the input capacitor $C_{in1,2}$ is set at 20 pF and the negative feedback capacitor $C_{fb1,2}$ is set at 0.2 pF. The PMOS pseudo-resistor $R_{b1,2}$ is used to bias DFC using the common mode voltage V_{CM} = 0.5 V. The capacitors ($C_{in1,2}$, $C_{fb1,2}$, $C_{m1,2}$, and $C_{LP1,2}$) are created using the MIM capacitor technique.

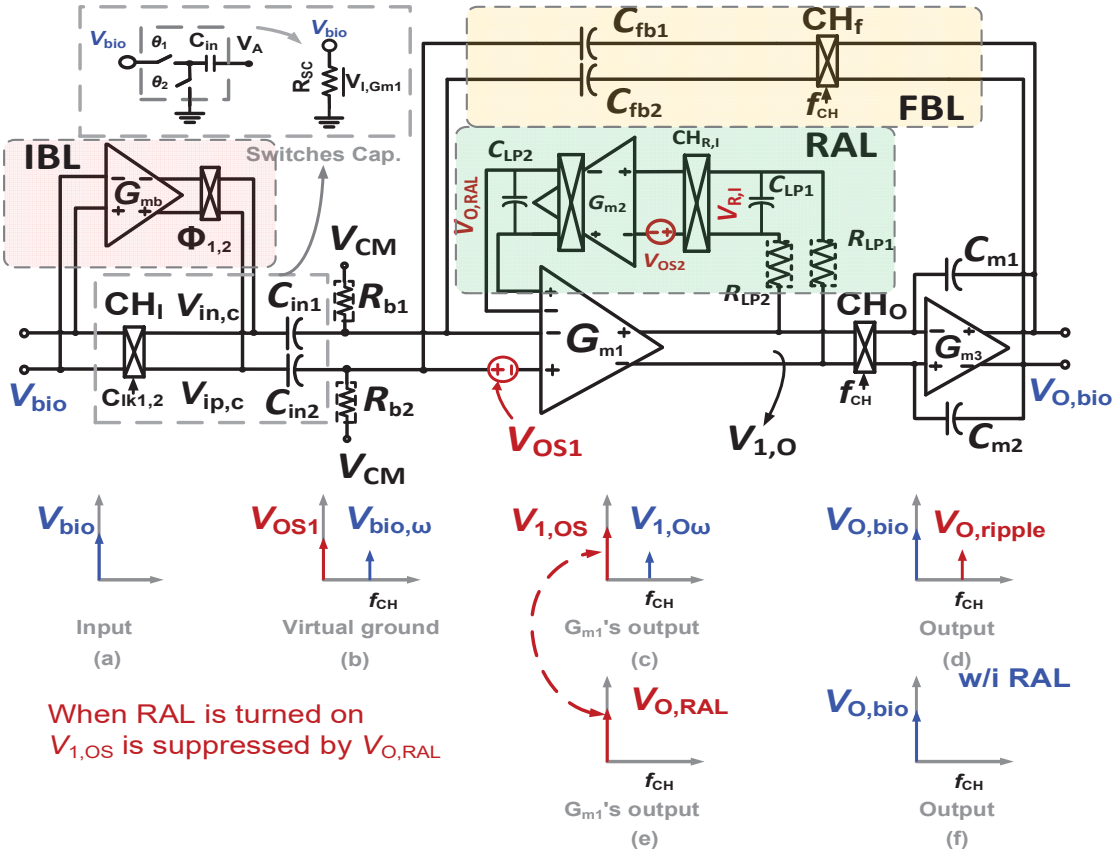


Figure 2. The schematic of the proposed CCIA with the spectrum of signal corresponding to each node.

As shown in Figure 2, the chopper CH_I is employed to modulate the bio signal input V_{bio} at low frequency (as shown in Figure 2a) up to a signal at f_{CH} = 10 kHz, before reducing it with a negative feedback loop at the virtual ground. When $V_{bio,\omega}$ is at virtual ground (as shown in Figure 2b), it can be written as $V_{bio,\omega} = V_{bio}/(1 + \beta A_V)$, where A_V is the open-loop gain voltage of the CCIA, and β is the factor of the negative feedback loop based on the ratio of C_{fb} to C_{in}. The chopper CH_O converts the $V_{bio,\omega}$ to the essential frequency band after G_{m1} has amplified it to produce $V_{1,O\omega}$. Finally, G_{m3} amplifies this signal to

generate a bio signal amplification $V_{O,bio}$ at the CCIA's output (as shown in Figure 2d). The transfer function of the proposed CCIA can be expressed as follows:

$$H(s) = -\left(g_{m1}C_{in1,2}\Big/(C_{in1,2}+C_{fb1,2})C_{m1,2}\right)\Big/\left(s+g_{m1}C_{fb1,2}\Big/(C_{in1,2}+C_{fb1,2})C_{m1,2}\right) \quad (1)$$

where g_{m1} is the transconductance of the first stage; and $C_{in1,2}$, $C_{fb1,2}$, and $C_{m1,2}$ are the input, negative, and Miller capacitors, respectively. Unfortunately, G_{m1} is attached to the offset voltage V_{OS1} resulting from the process variation (as shown in Figure 2b). After this is amplified by G_{m1} to create $V_{1,OS}$ at the output of DFC, the $V_{1,OS}$ is also chopped to the chopper frequency before being integrated by the Miller integrator. This results in a considerable ripple at the output (as shown in Figure 2d). The amplitude of the output ripple can be described as follows:

$$V_{O,Ripple} = \frac{V_{OS1}g_{m1}}{2f_{CH}C_{m1,2}} \quad (2)$$

where g_{m1} is the transconductance of the first stage; f_{CH} is the chopping frequency; and $C_{m1,2}$ are the phase margin compensation capacitors. For example, V_{OS1} = 10 mV, g_{m1} = 0.7 µS, f_{CH} = 10 kHz, $C_{m1,2}$ = 1.5 pF, and $V_{O,Ripple}$ = 233 mV.

The block diagram of an RAL is also shown in Figure 2. Instead of capturing the signal at the output, as in the usual approach, the RAL uses a low-pass filter (LPF) to obtain the signal at the output of the DFC ($V_{1,O} = V_{1,OS} + V_{1,O\omega}$) (as shown in Figure 2c) before the chopper output CH_O. This is because the $V_{1,OS}$ signal is continuously amplified, while the AC signal $V_{1,O\omega}$ is filtered out by the LPF in this case. To ensure that no AC signal is applied to G_{m1b}, which has the schemactic shown in next section, the capacitor C_{LP2} is added to the output of the RAL, although the LPF has a small low-pass corner controlled by $R_{LP1,2}$ and C_{LP1}. After amplifying $V_{1,OS}$, the signal $V_{O,RAL}$ is connected to G_{m1b}, creating a negative feedback loop to compensate for $V_{1,OS}$ (as shown in Figure 2e). This means that the ripple caused by V_{OS1} is reduced at the output of the CCIA (as shown in Figure 2f). To increase the loop gain (L_G) of the RAL and achieve a high ripple attenuation factor (RAF), G_{m2} is implemented using a two-stage operational amplifier for low noise and low power consumption. We assume that V_{OS2}, another inherent offset caused by process variations, is similarly associated with G_{m2}. The modulated offset V_{OS2} also generates the ripple at the CCIA's output and has the same effects as V_{OS1}, so it needs to be reduced. The ripple at the output of the CCIA is mitigated by a DC loop gain's factor $L_G(0)$ of the feedback loop RAL. The equation to determine L_G(s) in the technique proposed in this study is as follows:

$$L_G(s) \cong g_{m1b}R_{LP}A_{vGm2} = g_{m1b}R_{LP}\frac{A_{vGm2,DC}}{1+s/\omega_p} \quad (3)$$

$$L_G(0) \cong G_{m1}R_{LP}A_{vGm2,DC} \quad (4)$$

where G_{m1b} is the auxiliary transconductance of the first stage G_{m1}; and $A_{vGm2,DC}$ and f_p ($\omega_p = 2\pi f_p$) are the DC gain and cut-off frequency of the two-stage amplifier G_{m2}.

In the chopper biopotential amplifier, the input capacitor and the chopper are combined together, creating a switched capacitor resistor. At the completion of a cycle through the chopper clock f_{CH}, a charge of $Q = 2C_{in}V_{in}$ is delivered [7]. Therefore, Z_{in} can be determined as $Z_{in} = 1/(2C_{in}f_{CH})$. For example, Z_{in} is 2.5 MΩ for biomedical recording applications when the input capacitor C_{in} = 20 pF and f_{CH} = 10 kHz. An impedance boost loop (IBL) with a time diagram, as shown in Figure 3, is used to pre-charge Q to the C_{in}, as the Z_{in} must be improved by minimizing the charge Q from the input signal V_{in}. When the IBL is connected to C_{in}, the connection flowing from the input is interrupted and the V_{in} is copied by the buffer in IBL and is pre-charged to C_{in}. Assuming that the pre-charge current from the buffer is high enough, C_{in} will be fully charged from IBL; thus, when C_{in} is connected to the input after pre-charging, C_{in} does not require a charge from the

input signal V_{in}. This results in the fact that the Z_{in} can be set indefinitely. The Z_{in} can be represented following the analysis in [7], as follows:

$$Z_{in} = Z_0/(\alpha + \exp(-T/\tau)) \quad (5)$$

where Z_{in} is the input impedance, Z_0 is the input impedance without any boosting technique, α is the buffer gain error, T is the pre-charge time, and τ is the actual time constant.

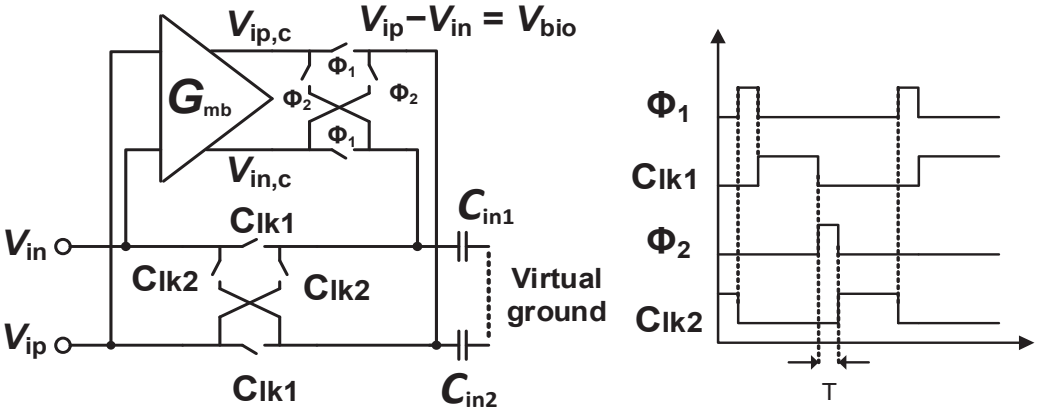


Figure 3. Schematics of the IBL and time diagram of the CCIA.

3. Circuit Implementation

Figure 4 shows the dual cascode amplifier (G_{m1}) combining with the RAL block. A feedback loop is set up comprising G_{m1b}, a two-stage chopper amplifier, and the RC-LPF in order to mitigate the output ripple. Figure 4 shows that the input stage consumes a power of 1.2 µW from a supply voltage of 1 V. The global common mode feedback circuit (CMFB) [25], which is used and consumed a biased current of 200 nA from 1 V, is employed to control the DC voltage at the output node of the CCIA. The gates of the transistors M_9 and M_{10} are adjusted using the CMFB circuit (V_{CMFB}) to control the output DC voltage followed to $V_{CM} = V_{DD}/2$. The power consumption of 1.4 µW of G_{m1} including CMFB is used.

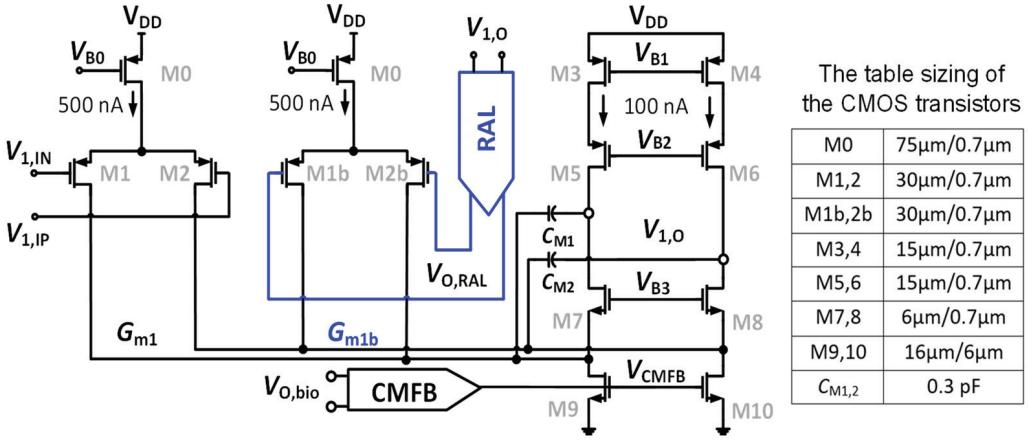
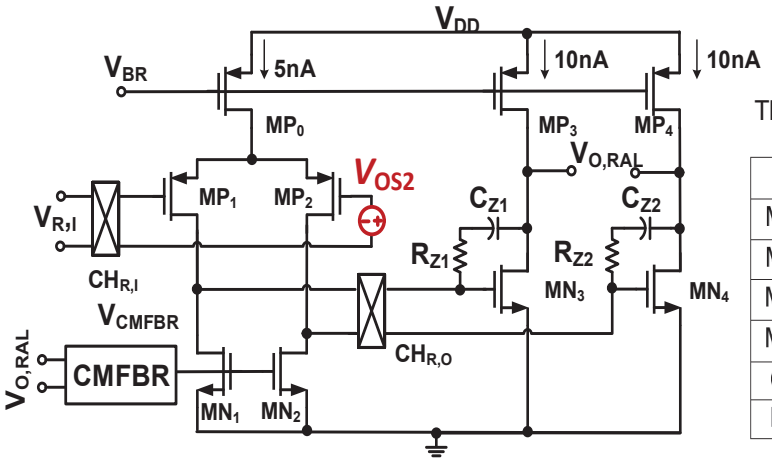


Figure 4. Schematic of the two-folded cascode opamp G_{m1} with table sizing of CMOS transistors.

Figure 5 shows the architecture of the chopper two-stage amplifier integrating with a common mode feedback circuit (CMFBR) [25] for G_{m2}. As already mentioned, the inherent offset V_{OS2} of G_{m2} has the same effect as V_{OS1}; the offset that is also upmodulated creates the ripple at the output of the CCIA. Consequently, it must be eliminated. In RAL, the chopper $CH_{R,I}$ is located at the output of the LPF, while the chopper $CH_{R,O}$ is put between the first and second stage of G_{m2}. This causes V_{OS2} to be modulated up to a high frequency

and then modulated down by the chopper CH_O, resulting in an offset voltage in the front of G_{m3}. Therefore, V_{OS2} is considered as an offset at the input of G_{m3}. Due to the high gain level of G_{m1} (about 80 dB), this offset is insignificant compared to the input. Therefore, its influence can be neglected. By using a 1 V supply, the first stage of G_{m2} consumes 5 nA, while the second stage of G_{m2} is biased to 20 nA for a better swing. The voltage V_{CMFBR} is generated by the CMFB circuit, which uses a bias current of 5 nA. Therefore, the total power of the RAL is only 30 nW.



The table sizing of the CMOS transistors

MP_0	30µm/0.7µm
$MP_{1,2}$	30µm/0.7µm
$MP_{3,4}$	60µm/0.7µm
$MN_{1,2}$	5µm/20µm
$MN_{3,4}$	0.7µm/0.7µm
$C_{Z1,2}$	3 pF
$R_{Z1,2}$	1.5 MΩ

Figure 5. Schematic of the chopper two-stage amplifier with table sizing of CMOS transistors.

The DC gain and the cut-off frequency of G_{m2} are decisive factors for determining the ripple attenuation factor and the bandwidth of the loop gain. The Monte Carlo simulation (MCS) method is used to study the fluctuation of these parameters across the chip and the mismatch of the device, including global variation and local mismatch. Figure 6a and Figure 6b show the value of the DC gain and cut-off frequency of G_{m2}, respectively. These distributions were derived from 300 samples of the MCS. The results show a mean value (MV) of the DC gain of G_{m2} of 90.9 dB, with a standard deviation (Std) of 0.167 dB. Furthermore, the MV of the cut-off frequency is 0.042 Hz with a Std of 0.0044 Hz.

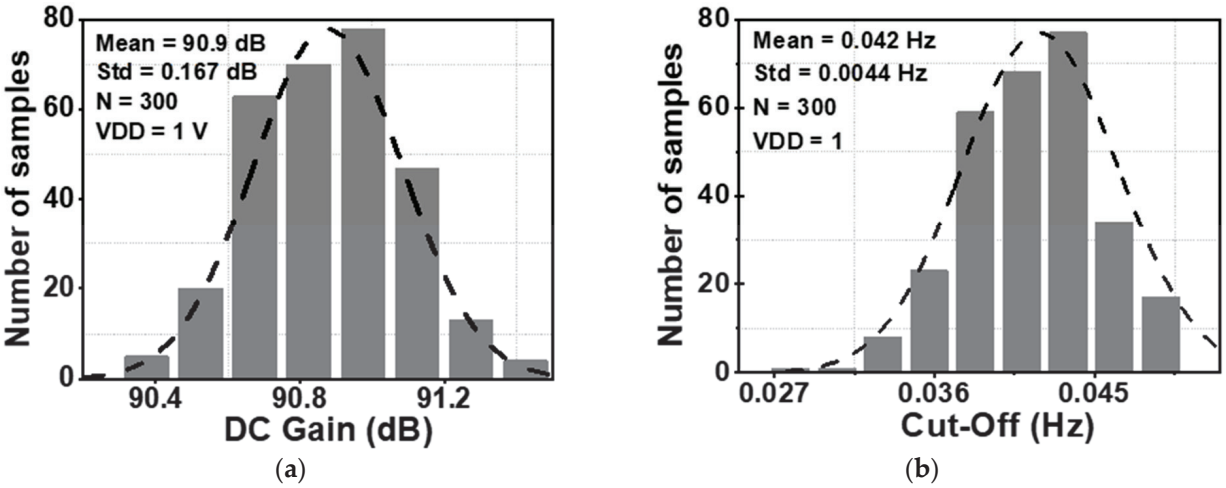
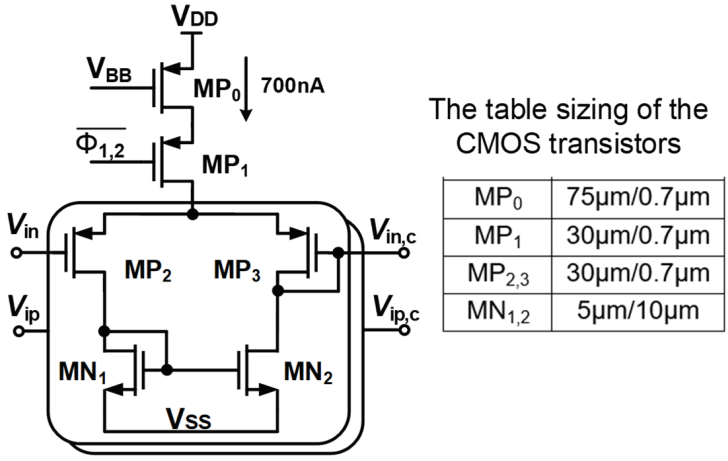


Figure 6. Monte Carlo simulation results for (**a**) DC gain, and (**b**) cut-off frequency of G_{m2}.

Figure 7 shows the schematic of the G_{mb} in the IBL. The MP0 and MP1 in G_{mb} are employed to bias and regulate the buffer with the purpose of reducing the impact of process variation on mismatch devices. The boosted input impedance in IBL can be affected by the pre-charge time T, the switches sizing of $\Phi_{1,2}$, and the buffer design. Figure 8 shows the clock generator for controlling the IBL. The pre-charge time T and $C_{lk1,2}$ are generated by

dividing the clock signal f_{CH}, which can be converted into a delayed signal by the use of several MOS capacitors and inverters. Although using a bias current of 700 nA, IBL is only enabled in 6 µs in each cycle of 100 µs (f_{CH} = 10 kHz); thus, IBL (G_{mb}) consumes only the current of 700 nA × 6/100 = 42 nA. The size and number of the MOS capacitor are shown in Figure 8. The sizing W/L of the switches $SW_{1,2}$ is set at about 0.5 µm/0.25 µm in order to minimize the inherent resistance. Furthermore, the pre-charge time T can be altered by using a two-switch $SW_{1,2}$ in order to mitigate the effect of process variability. This research examines the effect of the pre-charge time T and the size of the switches $\Phi_{1,2}$. Lengthening the pre-charge time T enhances the Z_{in} of the device, while simultaneously amplifying the noise of the device. The size of switches $\Phi_{1,2}$ in Figure 3 is another factor that affects the boost in Z_{in}. A small W/L size can result in a substantial voltage loss between these switches. Figure 9a and Figure 9b show the relationship between the Z_{in}, the input referred noise, the pre-charge time, and the switch sizing, respectively. As can be seen in Figure 9a, the Z_{in} improves from 2.5 MΩ to 0.7–1.8 GΩ when IBL is enabled with the pre-charge time T and is increased from 3 to 6 µs; however, the IRN increases sharply from 1.7 to 2.2 μV_{rms}. As shown in Figure 9b, when the switches sizing (Width-W) of $\Phi_{1,2}$ increases, the parasitic capacitors of these switches are also increased. When clock control for the pre-charge phase is applied to the gate of the CMOS transistor switches, the charge injection noise and clock feed-through increases [26,27], leading to an increase in the IRN. In this work, when the width of the switches sizing of $\Phi_{1,2}$ is changed from 1 to 5 µm, the IRN is increased from 1.8 to 2.1 μV_{rms}, while the noise increases from 2.5 to 3.2 μV_{rms} when W of $\Phi_{1,2}$ changes from 6 to 10 µm. According to the simulated results, as shown in Figure 9, in order to optimize Z_{in} and IRN, the pre-charge time T and the switches sizing $\Phi_{1,2}$ in this design are therefore set to 6 µs and W/L is set to 5 µm/0.5 µm.



The table sizing of the CMOS transistors

MP_0	75µm/0.7µm
MP_1	30µm/0.7µm
$MP_{2,3}$	30µm/0.7µm
$MN_{1,2}$	5µm/10µm

Figure 7. The schematic of the circuit in IBL with table sizing of the CMOS transistors.

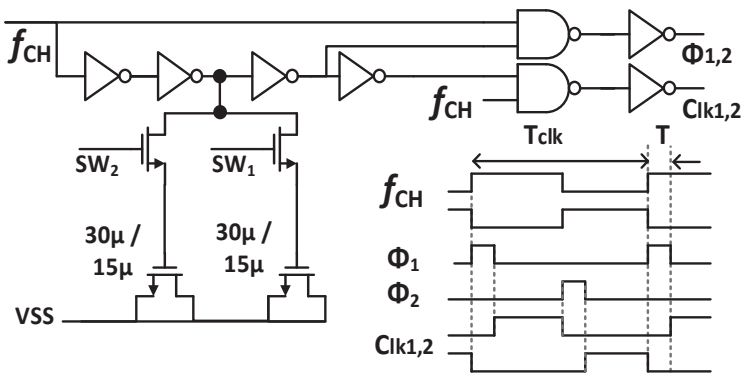


Figure 8. Schematic of a signal control generator for IBL.

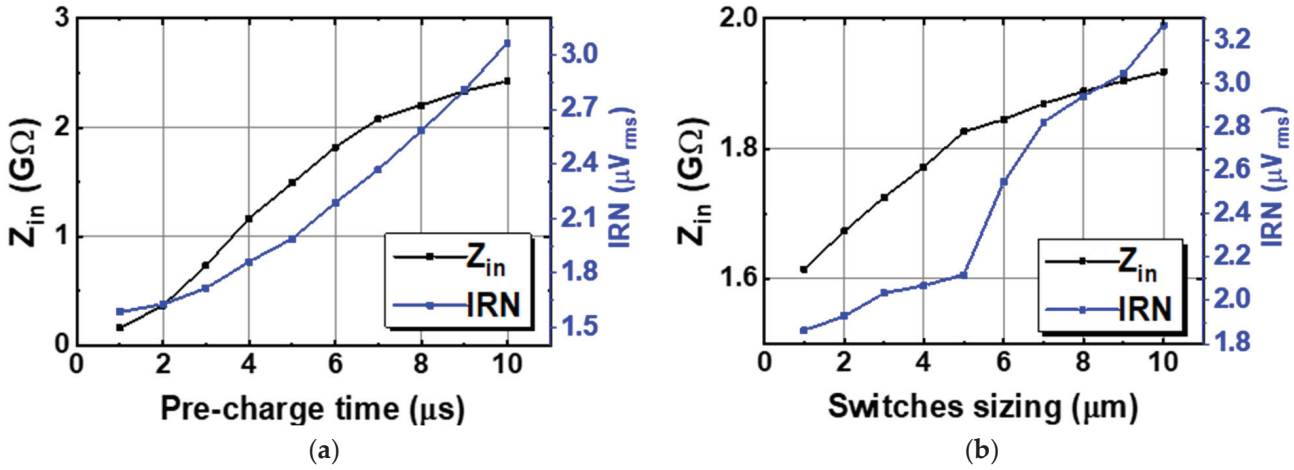


Figure 9. The relation between input impedance and noise to (**a**) the pre-charge time, and (**b**) the switches sizing.

4. Simulation Results

Figure 10 shows the layout of the proposed CCIA in the 180 nm CMOS process. The chip area of the CCIA configuration is 0.123 mm^2. Table 1 shows the power dissipation of each block in the CCIA. The total power consumption of the proposed CCIA is 1.87 μW from a V_{DD} of 1 V. G_{m1}, G_{m2}, G_{m3}, and G_{mb} consume 1400, 30, 400, and 40 nW, corresponding to 74.8%, 1.6%, 21.36%, and 2.24% of the total power consumption, respectively. According to the post-simulation results, it is shown that Figure 11 shows the simulated results of the CCIA's transfer function—(a) transient; (b) MCs. The CCIA's Av is 40 dB. The MCS results present that the MV of the closed-loop CCIA gain at 300 samples is 38.9 dB, with a Std of 0.28 dB. Figure 12 shows the MCS results for PSRR and CMRR after running 300 samples. At the 1 V supply, the MV of PSRR and CMRR are 108.6 and 118.7 dB with Stds of 23.7 and 24.4 dB, respectively.

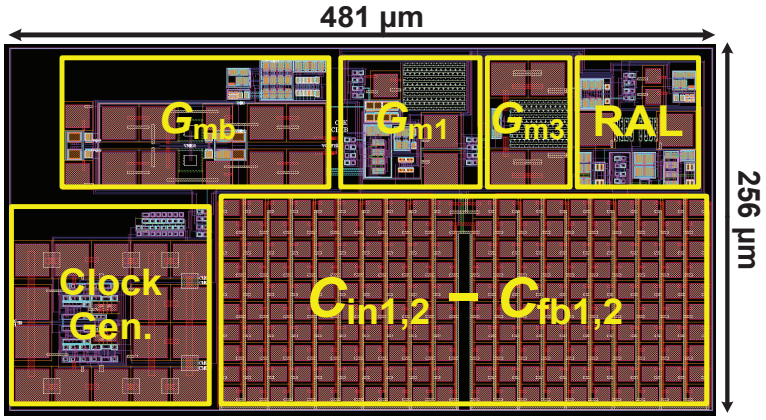


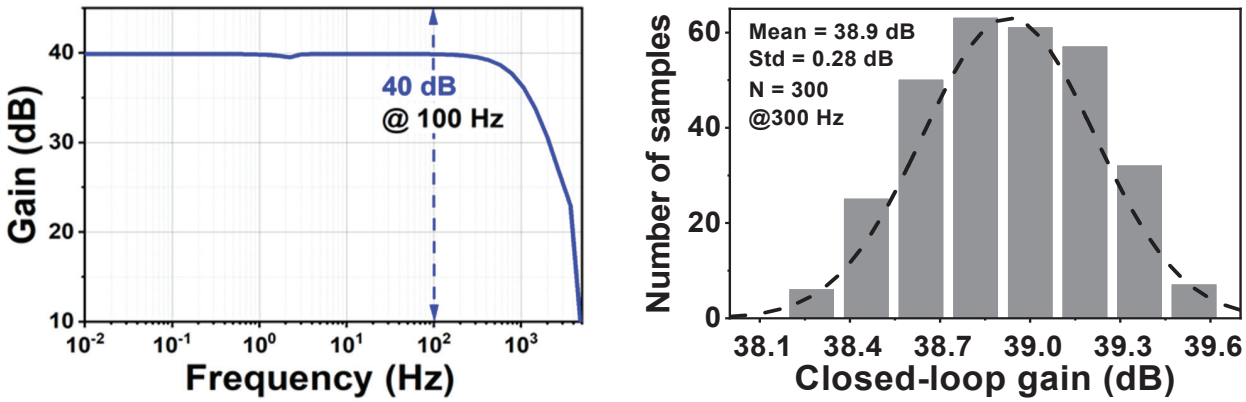
Figure 10. The layout of the proposed CCIA.

During the simulation, the input of the CCIA is configured so that it is short-circuited in order to test the output spectrum. Both V_{OS1} and V_{OS2} were set to a voltage of 5 mV. Figure 13 shows the simulated results of the voltage spectrum and the MCS of the output ripple. When the RAL is disabled, the amplitude of the output spectrum at the chopping frequency is about 82.2 mV, as shown in Figure 13a. The amplitude of the output ripple of the CCIA decreases to 0.36 mV when the RAL is enabled, as shown in Figure 13b. The output ripple is verified using an MCS that includes 300 samples and accounts for both local and global process variations. When the RAL level is changed from off to on, the MV of the output ripple decreases from 82.9 mV to 0.36 mV with a Std of 42.6 mV or 93 μV, as

shown in Figure 13c,d. The simulation results shown in Figure 14 therefore give an MV of 45.9 for the ripple attenuation, with a Std of 3.68 dB. The proposed feedback network effectively compensates for the offset voltage (V_{OS1}, V_{OS2}) caused by mismatches due to process, voltage, and temperature variations, resulting in a significant reduction in the output ripple voltage.

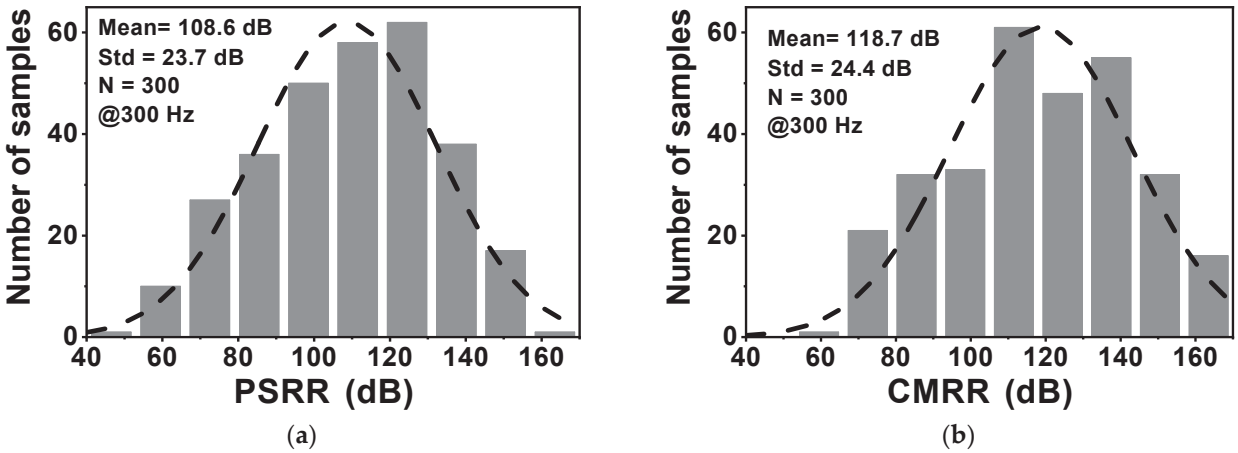
Table 1. The power dissipation of each block of the proposed CCIA.

Block	Circuit	Components	Power Dissipation (nW)
Dual_FC (G_{m1})	OPA-Dual FC	Differential Pair	500
		Differential Pair	500
		Cascode Branches	200
	CMFB		200
CS (G_{m3})	OPA-CS	Common source	400
RAL (G_{m2})	Stage-1	Differential Pair	5
	Stage-2	Common source	20
	CMFB2		5
IBL (G_{mb})	Buffer		42
	Total		1872



(**a**) (**b**)

Figure 11. (**a**) The transient of the proposed CCIA's transfer function; (**b**) MCS result of the proposed CCIA's transfer function.



(**a**) (**b**)

Figure 12. The MCS results of (**a**) PSRR; (**b**) CMRR.

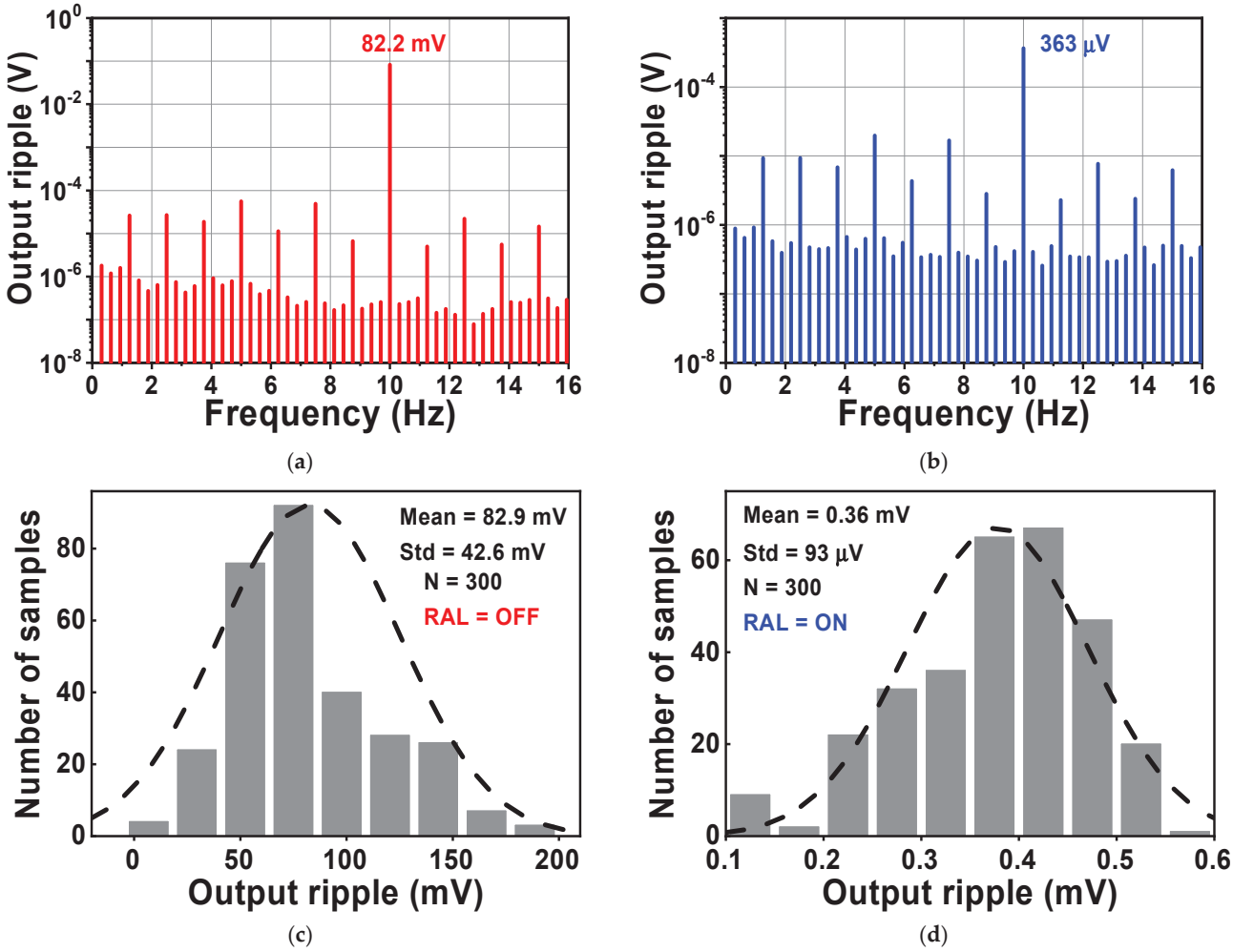


Figure 13. The simulated results of the voltage spectrum and MCS of the output ripple when RAL (**a**,**c**) is disabled, or (**b**,**d**) enabled.

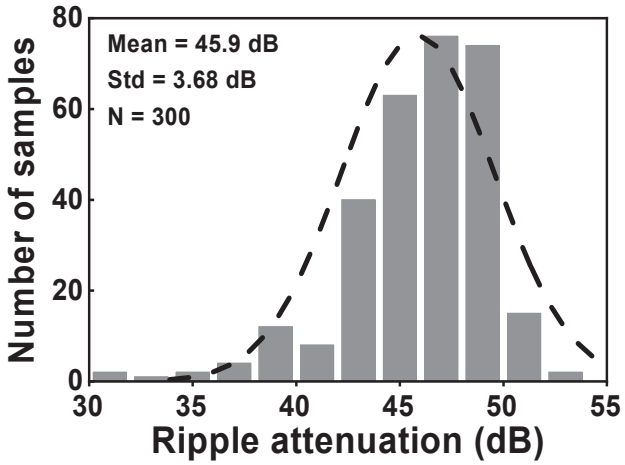


Figure 14. The MCS of the ripple attenuation result.

Figure 15 shows the effects of activating the impedance boost loop on the Z_{in} and the input-related noise. By setting the $SW_{1,2}$ parameter, it is possible to achieve different results for the input impedance. When $SW_{1,2}$ is set to 01 and 11, corresponding to a pre charge time of 3 and 6 µs, the Z_{in} in the low frequency range increases to about 0.7 and 1.8 GΩ, respectively, as shown in Figure 15a. Without the presence of IBL, the noise floor is

about 119 nV/$\sqrt{}$Hz, while the $1/f$ corner frequency is 10 Hz. When IBL is enabled, the noise floor increases to 136 nV/$\sqrt{}$Hz, resulting in an IRN over a bandwidth of 1 to 200 Hz of 2.16 μV_{rms}. This increase is observed for different values of $SW_{1,2}$, which determines the pulse width of the pre-charge time. Figure 16a shows the variation of IRN for the proposed amplifier across several process corners, ranging from 1.9 to 2.6 μV_{rms}. On the other hand, Figure 16b shows the MV of IRN, which is 2.16 μV_{rms}, with a Std of 97.9 nV_{rms}, verified using an MCS with 300 samples, considering both local and global process variations.

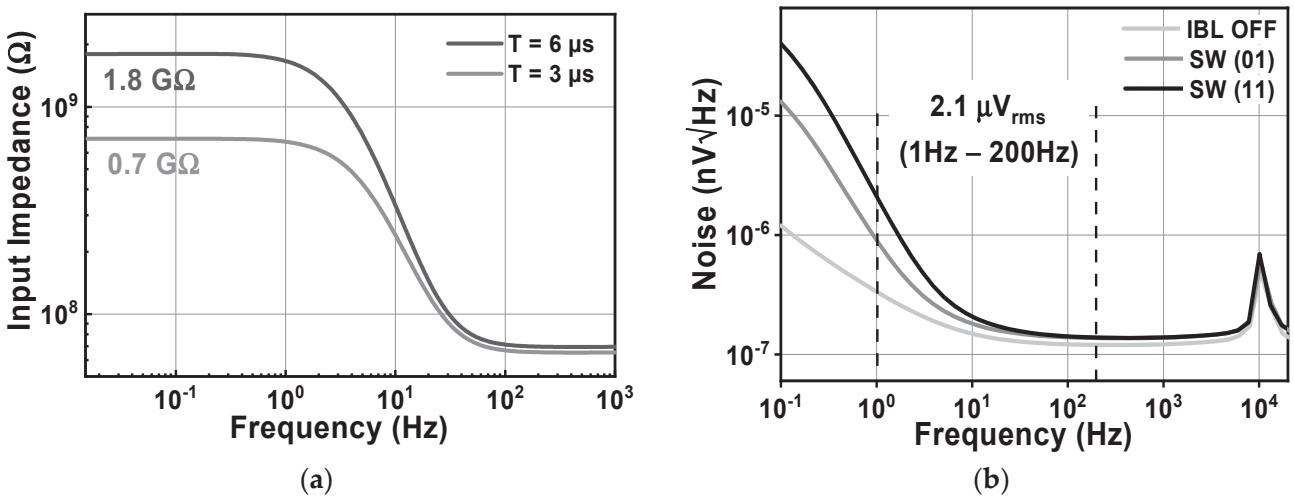


Figure 15. The simulated results of (**a**) the CCIA's input impedance; (**b**) the CCIA's noise.

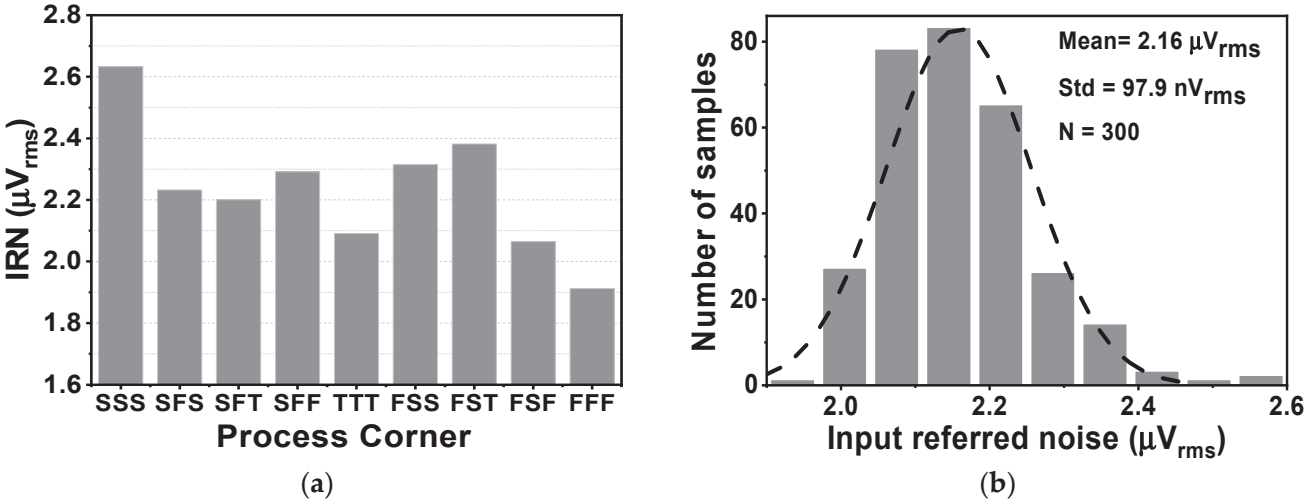


Figure 16. The simulated result of (**a**) the CCIA's noise across several the process corners and (**b**) the CCIA's noise.

Table 2 shows a brief summary of the primary design specifications, encompassing power consumption, output ripple's amplitude, Z_{in}, CMRR, PSRR, and NEF (noise efficient factor). There are several references that show simulation results, such as [24,28,29], in order to guarantee an equitable comparison. Table 2 is employed to evaluate the performance of the proposed design in comparison with the current state-of-the-art studies. The proposed CCIA obtains an NEF of about 7.5 by integrating RAL and IBL. Additionally, it exhibits a minimal output ripple of 363 µV and a significant Z_{in} of 1.8 GΩ. The CCIA's dissipation is 1.87 µW from a 1 V supply.

Table 2. Performance comparison.

Ref.	[18]	[23]	[24]	[28]	[29]	[30]	[31]	This Work
Year	2017	2021	2024	2022	2020	2021	2019	2024
Power (μW)	2	5.94	1.5	1.21	19.8	0.672	1.2	1.87
Supply (V)	1.2	1.8	2.47	1	1.8	2	5	1
Output ripple (mV)	0.012	NA	NA	0.061	NA	NA	NA	0.36
Ripple Attennuation (dB)	NA	NA	NA	>41	NA	NA	NA	45.9
Z_{in} (GΩ)	0.3	2.6	NA	NA	2.1	0.0575	400	1.8
Gain (dB)	25.7	40	59.7	40	46	40.6	20	40
PSRR (dB)	NA	85	>70	87	NA	84.2	N/A	108.6
CMRR (dB)	NA	93	>87	108	96	83.24	>70	118.7
IRN (μV_{rms})	9	1.4	1.18	1.8	1.9	2.01	3.7	2.16
NEF	7	NA	2.13	5.4	NA	2.63	NA	7.5
Tech. (nm)	40	180	130	180	180	350	180	180
Meas./Sim.	Meas.	Meas.	Sim.	Sim.	Sim.	Meas.	Meas.	Sim.

5. Conclusions

The paper presents a 1.87 μW capacitively coupled chopper instrumentation amplifier for biomedical recording. The output ripple is measured at 0.36 mV, and the input impedance is 1.8 GΩ. The CCIA chip occupies a chip area of only 0.123 mm^2 when implemented in a 0.18 μm CMOS technology. The ripple attenuation loop effectively decreases the output ripple of the proposed CCIA down to 0.36 mV. The CCIA is able to achieve a high input impedance of approximately 1.8 GΩ due to the impedance boosting loop. The low-power chopper amplifier has a power dissipation of 1.87 μW at a V_{DD} of 1 V. It also obtains a closed-loop gain of 40 dB, a PSRR of 108.6 dB, and a CMRR of 118.7 dB. The noise floor of the CCIA has a magnitude of 136 $nV/\sqrt{Hz}$, which leads to an IRN of 2.16 μV_{rms} across a bandwidth of 200 Hz. Thus, an NEF value of 7.5 is attained. This illustrates our ability to evaluate the performance of the proposed CCIA by comparing it to the most recent studies.

Author Contributions: Conceptualization, X.P.T., X.T.P., X.T.K. and M.K.H.; methodology, X.P.T., X.T.K., D.P.P. and M.K.H.; software, X.P.T. and X.T.P.; formal analysis, X.T.K., D.P.P. and M.K.H.; writing—original draft preparation, X.P.T.; writing—review and editing, X.T.K., D.P.P. and M.K.H.; visualization, X.T.P., D.P.P. and M.K.H.; supervision, X.T.K. and M.K.H.; project administration, X.P.T.; funding acquisition, X.P.T., X.T.P., X.T.K. and M.K.H. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: The data presented in this study are available in this article.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Tran, X.P.; Pham, X.T.; Kieu, X.T.; Nguyen, L.C.; Pham, D.P.; Hoang, M.K. A 1.8-GΩ Input Impedance 45-dB Ripple Reduction Factor Chopper Amplifier for Biomedical Recording. In Proceedings of the 2023 International Conference on Advanced Technologies for Communications (ATC), Da Nang, Vietnam, 19–21 October 2023.
2. Wang, S.; Koickal, T.J.; Hamilton, A.; Mastropaolo, E.; Cheung, R.; Abel, A.; Smith, L.S.; Wang, L. A Power-Efficient Capacitive Read-Out Circuit With Parasitic-Cancellation for MEMS Cochlea Sensors. *IEEE Trans. Biomed. Circuits Syst.* **2016**, *10*, 25–37. [CrossRef] [PubMed]

3. Jiang, X.; Bian, G.-B.; Tian, Z. Removal of artifacts from EEG signals: A review. *Sensors* **2019**, *19*, 987. [CrossRef] [PubMed]
4. Lin, C.T.; Ko, L.W.; Chang, M.H.; Duann, J.R.; Chen, J.Y.; Su, T.P.; Jung, T.P. Review of wireless and wearable electroencephalogram systems and brain-computer interfaces-a mini-review. *Gerontology* **2010**, *56*, 112–119. [CrossRef] [PubMed]
5. Fiedler, P.; Mühle, R.; Griebel, S.; Pedrosa, P.; Fonseca, C.; Vaz, F.; Zanow, F.; Haueisen, J. Contact Pressure and Flexibility of Multipin Dry EEG Electrodes. *IEEE Trans. Neural Syst. Rehabil. Eng.* **2018**, *26*, 750–757. [CrossRef] [PubMed]
6. Nguyen, V.-N.; Pham, X.T.; Lee, J.-W. Three-Step Cyclic Vernier TDC Using a Pulse-Shrinking Inverter-Assisted Residue Quantizer for Low-Complexity Resolution Enhancement. *IEEE Trans. Instrum. Meas.* **2021**, *70*, 1–12. [CrossRef]
7. Chandrakumar, H.; Marković, D. A high dynamic-range neural recording chopper amplifier for simultaneous neural recording and stimulation. *IEEE J. Solid-State Circuits* **2017**, *52*, 645–656. [CrossRef]
8. Pham, X.T.; Kieu, X.T.; Hoang, M.K. Ultra-Low Power Programmable Bandwidth Capacitively-Coupled Chopper Instrumentation Amplifier Using 0.2 V Supply for Biomedical Applications. *J. Low Power Electron. Appl.* **2023**, *13*, 37. [CrossRef]
9. Xu, J.; Lin, Q.; Ding, M.; Li, Y.; Van Hoof, C.; Serdijn, W.; Van Hellepute, N. A 0.6V 3.8μW ECG/bio-impedance monitoring IC for disposable health patch in 40nm CMOS. In Proceedings of the 2018 IEEE Custom Integrated Circuits Conference (CICC), San Diego, CA, USA, 8–11 April 2018.
10. Yaul, F.M.; Chandrakasan, A.P. A noise-efficient 36 nV/$\sqrt{\text{Hz}}$ chopper amplifier using an inverter-based 0.2-V supply input stage. *IEEE J. Solid-State Circuits* **2017**, *52*, 3032–3042. [CrossRef]
11. Huang, G.; Yin, T.; Wu, Q.; Zhu, Y.; Yang, H. A 1.3μW 0.7μVRMS chopper current-reuse instrumentation amplifier for EEG applications. In Proceedings of the 2015 IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, Portugal, 24–27 May 2015.
12. Wu, R.; Makinwa, K.A.A.; Huijsing, J.H. A Chopper Current-Feedback Instrumentation Amplifier With a 1 mHz 1/f Noise Corner and an AC-Coupled Ripple Reduction Loop. *IEEE J. Solid-State Circuits* **2009**, *44*, 3232–3243. [CrossRef]
13. Park, J.H.; Tang, T.; Zhang, L.; Ng, K.A.; Gammad, G.G.L.; Yen, S.C.; Yoo, J. A 15-Channel Orthogonal Code Chopping Instrumentation Amplifier for Area-Efficient, Low-Mismatch Bio-Signal Acquisition. *IEEE J. Solid-State Circuits* **2020**, *55*, 2771–2780. [CrossRef]
14. Nasseriana, M.; Peiravia, A.; Moradi, F. A fully-integrated 16-channel EEG readout front-end for neural recording applications. *AEU—Int. J. Electron. Commun.* **2018**, *94*, 109–121. [CrossRef]
15. Li, J.; Zhu, L.; Su, R.; Wang, W.; Zhou, Y.; Xie, S.; Mao, G.; Zhou, Z. A Capacitively Coupled Chopper Instrumentation Amplifier With Deadtime Offset Reduction Technique for Neural Signal Sensing. *IEEE Sens. Lett.* **2024**, *8*, 1–4. [CrossRef]
16. Zheng, J.; Ki, W.-H.; Hu, L.; Tsui, C.-Y. Chopper capacitively coupled instrumentation amplifier capable of handling large electrode offset for biopotential recordings. *IEEE Trans. Circuits Syst. II Express Briefs* **2017**, *64*, 1392–1396. [CrossRef]
17. Wu, J.; Law, M.K.; Mak, P.I.; Martins, R.P. A 2-μW 45-nV/$\sqrt{\text{Hz}}$ readout front end with multiple-chopping active-high-pass ripple reduction loop and pseudo feedback DC servo loop. *IEEE Trans. Circuits Syst. II Express Briefs* **2016**, *63*, 351–355.
18. Chandrakumar, H.; Marković, D. An 80-mVpp Linear-Input Range, 1.6- GΩ Input Impedance, Low-Power Chopper Amplifier for Closed-Loop Neural Recording That Is Tolerant to 650-mVpp Common-Mode Interference. *IEEE J. Solid-State Circuits* **2017**, *52*, 2811–2828. [CrossRef]
19. Zheng, J.; Ki, W.H.; Tsui, C.Y. Analysis and design of ripple reduction chopper bandpass amplifier. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2018**, *65*, 1185–1195. [CrossRef]
20. Chandrakumar, H.; Marković, D. A simple area-efficient ripple rejection technique for chopped biosignal amplifiers. *IEEE Trans. Circuits Syst. II Express Briefs* **2015**, *62*, 189–193. [CrossRef]
21. Fang, L.; Gui, P. A Low-Noise Low-Power Chopper Instrumentation Amplifier With Robust Technique for Mitigating Chopping Ripples. *IEEE J. Solid-State Circuits* **2022**, *57*, 1800–1811. [CrossRef]
22. Luo, D.; Zhang, M.; Wang, Z. A Low-Noise Chopper Amplifier Designed for Multi-Channel Neural Signal Acquisition. *IEEE J. Solid-State Circuits* **2019**, *54*, 2255–2265. [CrossRef]
23. Wenfei, C.; Yi, L.; Shubin, L.; Ling, W.; Rui, M.; Zhangming, Z. A 2.6 GΩ, 1.4 μVrms current-reuse instrumentation amplifier for wearable electrocardiogram monitoring. *Microelectron. J.* **2021**, *107*, 1049.
24. Chen, X.; Mo, T.; Wu, P.; Wu, B. A Capacitive-Feedback Amplifier with 0.1% THD and 1.18 μVrms Noise for ECG Recording. *Electronics* **2024**, *13*, 378. [CrossRef]
25. Baker, R.J. *CMOS Circuit Design, Layout, and Simulation*; Wiley: Hoboken, NJ, USA, 2010.
26. Xu, J.; Fan, Q.; Huijing, J.H.; Hoof, C.V.; Yazicioglu, R.F.; Makinwa, K.A.A. Measurement and Analysis of Current Noise in Chopper Amplifiers. *IEEE J. Solid-State Circuits* **2013**, *48*, 1575–1584.
27. Ha, H.; Hoof, C.V.; Helleputte, N.V. Measurement and Analysis of Input-Signal Dependent Flicker Noise Modulation in Chopper Stabilized Instrumentation Amplifier. *IEEE Solid-State Circuits Lett.* **2018**, *4*, 90–93. [CrossRef]
28. Pham, X.T.; Vu, T.K.; Nguyen, T.D.; Pham-Nguyen, L. A 1.2-μW 41-dB Ripple Attenuation Chopper Amplifier Using Auto-Zero Offset Cancelation Loop for Area-Efficient Biopotential Sensing. *Electronics* **2022**, *11*, 1149. [CrossRef]
29. Xu, W.; Wang, T.; Wei, X.; Yue, H.; Wei, B.; Duan, J.; Li, H. Low Noise, High Input Impedance Digital-Analog Hybrid Offset Suppression Amplifier for Wearable Dry Electrode ECG Monitoring. *Electronics* **2020**, *9*, 165. [CrossRef]

30. Sawigun, C.; Thanapitak, S. A Compact Sub-μW CMOS ECG Amplifier With 57.5-MΩ Zin, 2.02 NEF, 8.16 PEF and 83.24-dB CMRR. *IEEE Trans. Biomed. Circuits Syst.* **2021**, *15*, 549–558. [CrossRef]
31. Chen, M.; Chun, H.S.; Castro, I.D.; Torfs, T.; Lin, Q.; Van Hoof, C.; Wang, G.; Lian, Y.; Van Helleputte, N. A 400 GΩ Input-Impedance Active Electrode for Non-Contact Capacitively Coupled ECG Acquisition With Large Linear-Input-Range and High CM-Interference-Tolerance. *IEEE Trans. Biomed. Circuits Syst.* **2019**, *13*, 2. [CrossRef]

Journal of
Low Power Electronics and Applications

MDPI

Article

Ultra-Low Power Programmable Bandwidth Capacitively-Coupled Chopper Instrumentation Amplifier Using 0.2 V Supply for Biomedical Applications

Xuan Thanh Pham , Xuan Thuc Kieu and Manh Kha Hoang *

Faculty of Electronics Engineering, Hanoi University of Industry, Hanoi 10000, Vietnam; thanhpx@haui.edu.vn (X.T.P.); thuckx@haui.edu.vn (X.T.K.)
* Correspondence: khahoang@haui.edu.vn; Tel.: +84-243765-5121

Abstract: This paper presents a capacitively coupled chopper instrumentation amplifier (CCIA) with ultra-low power consumption and programmable bandwidth for biomedical applications. To achieve a flexible bandwidth from 0.2 to 10 kHz without additional power consumption, a programmable Miller compensation technique was proposed and used in the CCIA. By using a Squeezed inverter amplifier (SQI) that employs a 0.2-V supply, the proposed CCIA addresses the primary noise source in the first stage, resulting in high noise power efficiency. The proposed CCIA is designed using a 0.18 μm CMOS technology process and has a chip area of 0.083 mm^2. With a power consumption of 0.47 μW at 0.2 and 0.8 V supply, the proposed amplifier architecture achieves a thermal noise of 28 nV/$\sqrt{}$Hz, an input-related noise (IRN) of 0.9 μV_{rms}, a closed-loop gain (A_V) of 40 dB, a power supply rejection ratio (PSRR) of 87.6 dB, and a common-mode rejection ratio (CMRR) of 117.7 dB according to post-simulation data. The proposed CCIA achieves a noise efficiency factor (NEF) of 1.47 and a power efficiency factor (PEF) of 0.56, which allows comparison with the latest research results.

Keywords: ultra-low power; low noise; chopper amplifier; biomedical amplifier

1. Introduction

Wireless sensor biomedicine (WSB) is becoming increasingly popular to monitor our daily activities for early detection of cardiovascular diseases [1–3]. Due to its use in wearable or implantable devices, low-power sensors are required to monitor human biopotential signal. In addition to developing standard applications to improve patients' quality of life, long-term monitoring, mobile monitoring, sports and rehabilitation applications, and brain-computer interfaces will also be realized [4]. Typically, WSBs use a low-noise, low-power instrumentation amplifier (IA) to interface with many types of biomedical sensors. These biopotential signals include electrocardiograms (ECGs) and electroencephalograms (EEGs) from the heart and brain, respectively. Local field potentials (LFPs) and action potentials (APs) are biomarkers useful for both neuroscience research and treatment [5]. Biopotential signals, as shown in Figure 1, have a very low amplitude, ranging from 10 to 100 μV for EEG and about 1 mV for ECG. The biosignals range from 0.5 to 150 Hz [6]. LFP has a bandwidth of 1 to 200 Hz and a peak amplitude of about 1 mV, while APs have a peak amplitude of about 100 μV and occupy a frequency band of 200 Hz to 5 kHz [7]. Therefore, these neural signals must first be amplified before signal processing can be performed.

To improve the quality of neural signals, the readout system often includes an instrumentation amplifier (IA) implemented in CMOS technology. However, the IA has two important noise sources that must be taken into account, flicker noise ($1/f$) and thermal noise [8]. The chopper stabilization technique is commonly used on IA [9,10] to mitigate 1/f noise by up-modulating this noise at low frequencies beyond the spectrum of IA, while leaving thermal noise unresolved. For example, although the designs in [11,12] consume

only 2 μW and 1.89 μW, thermal noise remains a concern with values of 100 and 240 nV/Hz, respectively. In addition, the CCIAs in [13,14] only have a bandwidth of about 500 Hz. Therefore, CCIAs should have a variable bandwidth to allow better bandwidth selection, while biopotential signals are often bandlimited. This work is an extension of the work originally presented at ICCE'22 [15].

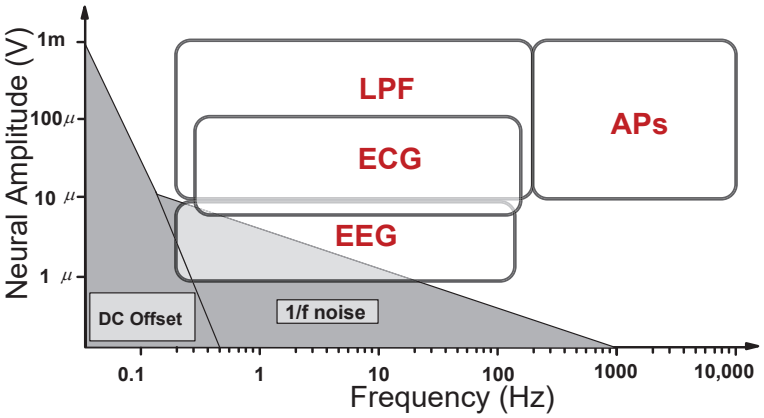


Figure 1. Amplitude and frequency ranges of the characteristics of neural signals.

This paper presents an ultra-low-power CCIA with programmable bandwidth for biomedical applications. To achieve high noise power efficiency, a squeezed inverter amplifier (SQI) operating with a 0.2-V supply is used in the CCIA. In addition, a programmable Miller compensation capacitor is used in the CCIA to obtain flexible bandwidth without additional power consumption. Simulated with a 0.18 μm CMOS technology process, the chip area of the proposed CCIA is only 0.083 mm^2. While the power consumption of 0.47 μW is achieved at the supply voltage of 0.2 and 0.8-V, the proposed amplifier architecture achieves a thermal noise of 28 $nV/\sqrt{Hz}$, an input-related noise (IRN) of 0.9 μV_{rms} over a bandwidth of 1 kHz, a closed-loop gain of 40 dB, a power supply rejection ratio (PSRR) of 87.6 dB, and a common-mode rejection ratio (CMRR) of 117.7 dB according to post-simulation data. The proposed CCIA compares well with the latest research results, with a noise efficiency factor (NEF) of 1.47 and a power efficiency factor (PEF) of 0.56.

2. Design

As we know, to reduce the thermal noise, there are two approaches: (1) The transistors of the amplifier are enlarger, resulting in an increase in chip area; (2) The DC current bias for the amplifier must be increased [8]. However, to achieve low power consumption, the supply voltage must be reduced to a minimum so that the transistor still works well. This is the biggest challenge in designing an amplifier. Therefore, the Squeeze inverter amplifier (SQI) with a supply voltage of 0.2 V is dropped in the proposed design. The multistage capacitively coupled chopper amplifier (CCIA) is shown schematically in Figure 2. Since the input stage (G_{m1}) causes most of the input noise, the low-power and low-noise SQI amplifier is implemented in the first stage to mitigate the noise. To achieve high transconductance, the CMOS transistors are operated at a comparatively high current of 800 nA in the subthreshold region. A low supply voltage $V_{DD,L}$ of 0.2-V is used to power the high-current input stage G_{m1}, which corresponds to two drain-source saturation voltages (V_{DSAT}) of both the PMOS and NMOS transistors in the SQI to reduce power consumption to only about 320 nW. The combination of the output stage of an amplifier with a common source (CS) is used to achieve a large output swing with the middle stage using a folded—cascode amplifier (FC) to achieve high gain. Since the output common mode voltage of the first stage is only 0.1 V, the FC stage must be used with PMOS transistor input pairs. To handle the low-frequency flicker noise ($1/f$), the chopper CH_I is connected before the input capacitor to modulate the input signal V_{in} to the chopper frequency f_{CH} = 10 kHz, which is then modulated down to the baseband by the chopper CH_O. The proposed multistage CCIA

creates multiple poles, which reduce the stabilization of the circuit. To ensure stability while maintaining bandwidth, Miller compensation capacitors $C_{C1,2}$ and resistors $R_{Z1,2}$ are added to the last stage feedback loop.

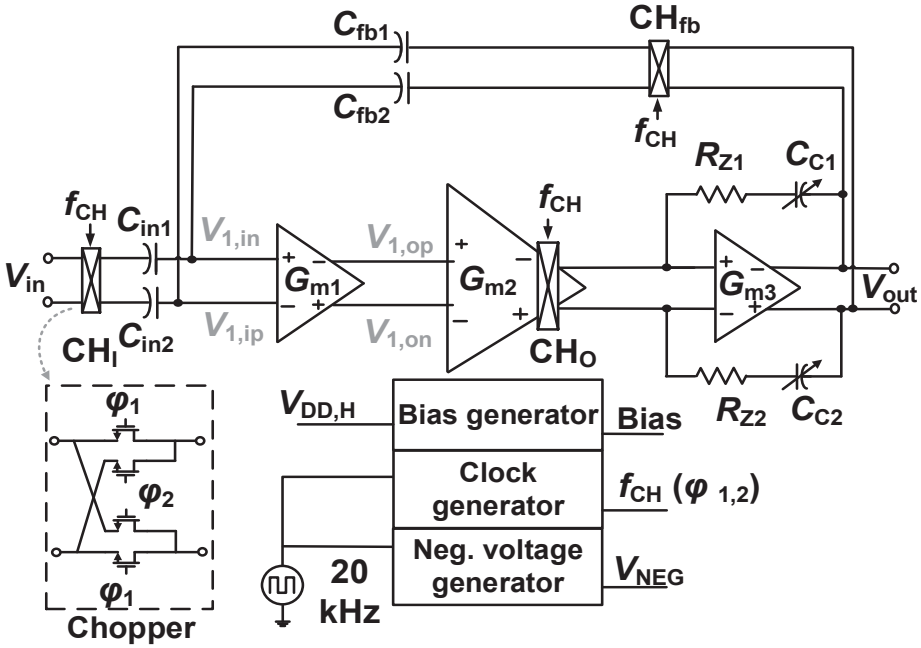


Figure 2. Schematic of the proposed CCIA with $C_{in1,2}$ = 4 pF, $C_{fb1,2}$ = 40 fF, $R_{Z1,2}$ = 0.9 MΩ, $C_{C1,2}$ = 0.62/6.2/30 pF.

As we know, the amplifier is stable when the phase at the loop gain crossover is higher than −180 degrees when the loop gain is 0 dB. By moving either the loop gain crossover or the phase crossover point, i.e., the point where the phase reaches −180 degrees, away from the origin, you can increase the stability. Thus, decreasing $C_{C1,2}$ causes the loop gain crossover of CCIA to move away from the origin, increasing the bandwidth of CCIA. Moreover, the serial nulling resistors $R_{Z1,2}$ are used to reduce the null in the right half plane (RHP) caused by the feedforward using the compensation capacitors. The multi-stage CCIA proposed in this work has a flexible bandwidth from 0.2 to 10 kHz thanks to the programmable Miller compensation capacitors $C_{C1,2}$. In contrast, previous designs [16,17], which also use a multi-stage circuit in the main path, use fixed values of the Miller compensation components so that the bandwidth of these designs is 0.67 and 0.8 kHz, respectively. The midband gain of the CCIA is determined by the ratio of the input capacitances $C_{in1,2}$ and the feedback capacitances $C_{fb1,2}$. In this work, $C_{in1,2}$ = 4 pF, $C_{fb1,2}$ = 40 fF are realized by the metal-insulator-metal (MIM) capacitor technique to reduce the active chip area so that the midband gain of the CCIA reaches 40 dB.

3. Circuit Implementation

3.1. Squeezed-Inverter Amplifier

As shown in Figure 3, the first stage uses the scheme of SQI with a common mode feedback circuit (CMFB) sharing to increase the CMRR. By using an ultra-low voltage supply $V_{DD,L}$ = 0.2-V, the CMOS transistors in the SQI operate in the subthreshold region. The IRN of the first stage can be calculated as follows:

$$\overline{V_{n,in,Gm1}^2} = \frac{8kT}{g_{m,n} + g_{m,p}} \cong \frac{4kTnV_T}{I_{BIAS}} \quad (1)$$

where $g_{m,n}$ and $g_{m,p}$ are the transconductance of the NMOS NM and PMOS PM transistors, respectively, the bias current I_{BIAS} is 0.8 μA, thermal voltage V_T = 26 mV, and the subthreshold factor [18] n = 1.5. The SQI stage operates with low noise by increasing the

bias current. Moreover, due to using an ultra-low-voltage supply of 0.2 V, SQI archives high noise power efficiency.

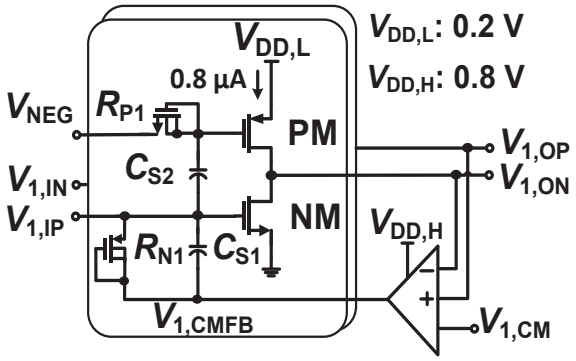


Figure 3. Schematic of SQI C_{S1} = 1 pF, C_{S2} = 4 pF.

The input stage G_{m1} is the main source of noise in the design and requires a large bias current to limit the output noise with $1/f$ noise and thermal noise [15]. The chopping approach can be used to remove the flicker noise while the thermal noise is not compatible with the bias current. Therefore, an acceptable bias current of 0.8 µA was chosen to compensate for an extremely low supply voltage of 0.2 V to reduce noise floor while keeping power dissipation low. To operate at the 0.2 V supply voltage, the negative bias voltages of the input PM and NM transistors in SQI are regulated by a negative bias generator and a CMFB loop. A negative voltage V_{NEG} generated by the negative bias generator (see Figure 3) is used to bias the PM input transistor via a pseudo-resistor $R_{P1,2}$. The gate voltage of the transistor NM is controlled by a common CMFB loop [10] driven by a high voltage source $V_{DD,H}$ = 0.8-V to maintain the common output voltage of SQI at $V_{DD,L}/2$. Capacitors $C_{S1,2}$ are used for AC coupling. Since the subthreshold transistors operate without a tail current source, it is challenging to balance the bias current for the input pairs using the CM voltage. Therefore, a common CMFB circuit, as shown in Figure 4, is required for the SQI differential branches to solve this problem. By using a voltage of $V_{1,CM}$ = 0.1-V as a reference, a negative feedback loop is created to monitor and adjust the output common mode voltage of the SQI. The output of the CMFB, $V_{1,CMFB}$, is used to control the gate voltage of the transistor NM in each SQI branch through a pair of pseudo-resistors $R_{N1,2}$. This approach provides balanced bias currents for the SQI stage since any change in $V_{1,CMFB}$ affects the input pair by the same amount.

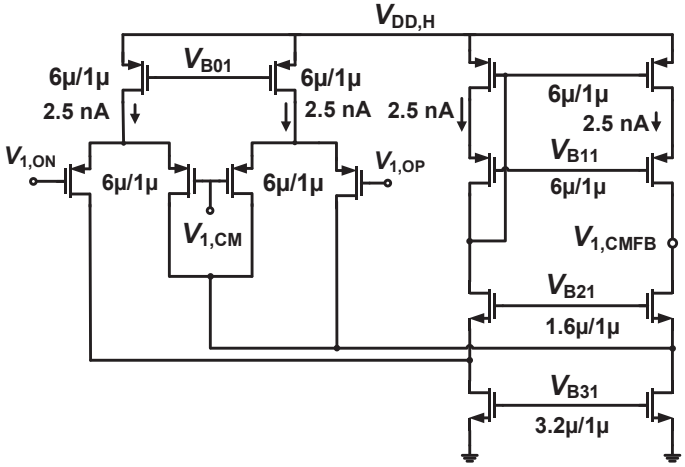


Figure 4. Schematic of CMFB circuit of the SQI.

3.2. Bias Circuit for Squeezed-Inverter Amplifier

As we know, CMOS transistors must be biased in SQI, but the extremely low supply voltage $V_{DD,L}$ = 0.2-V makes this difficult. While PM transistors need a negative bias voltage lower than ground, the voltage drives the gate of the NM transistors using a CMFB through the high voltage supply $V_{DD,H}$ = 0.8-V. In the conventional negative voltage generator [16], a switched capacitor loop (SC) is used, in which a 1/10 scaled replica M_{PB} of the PMOS input transistor is used to generate the negative voltage to regulate the bias current of the SQI. M_{PB} and the FC work together to provide a negative feedback loop that continuously regulates V_G during the time that the drain voltage is held at $V_{DD,L}/2$. An SC network is also used by the feedback loop to hold V_G below ground. A low-noise copy of V_G is created using a low-pass filter replica (V_{NEG}). To prevent switching spikes from affecting the desired signals, a frequency of 20 kHz is used by this SC. To turn off the switches completely, a negative level shifter is driven by V_G or V_{NEG}. However, after each switching period, the level shifter supplies its "ground" rail, increasing the voltage differences between V_G and V_{NEG} during startup. The negative feedback loop has V_G fixed, so inaccurate replication of V_{NEG} will result in an unexpected bias current. V_{NEG} will be higher than V_G, when the level shifter uses V_{NEG}. As a result, the bias current of SQI will be reduced, which will increase the input noise. On the other hand, the bias current will be lower than predicted when this level shifter is driven by V_G, which drastically increases the power consumption. Therefore, an auxiliary path is needed to generate a voltage V_B, a replica of the voltage V_G to supplement the negative voltage generator circuit. The proposed negative bias voltage generator is shown in Figure 5. The V_B-fed negative voltage for the level shifter does not affect V_G and V_{NEG}. Therefore, the bias current of SQI is set to the appropriate value, and V_{NEG} is an exact duplicate of V_G. According to the simulation results shown in Figure 6, the expected level of V_{NEG} is about −150 mV after V_G or V_{NEG} is used by the level shifter but is changed to about −100 mV or −210 mV accordingly after the start time. Since only V_B is supplied by the dynamic current of the level shifter, V_G and V_{NEG} are controlled by an equal voltage of −150 mV when V_B is injected. The improved negative bias generator in the SQI circuit achieves a bias current of 1.56 μA or an almost theoretical value of 1.6 μA.

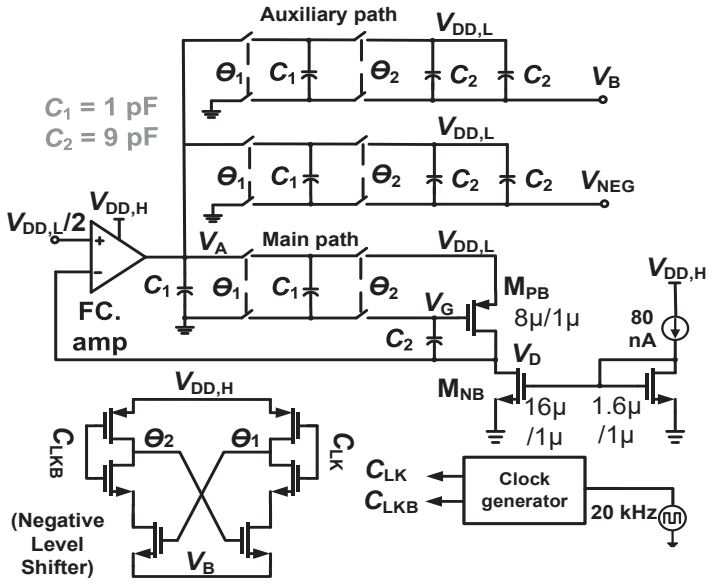


Figure 5. Schematic of negative voltage bias generator circuit.

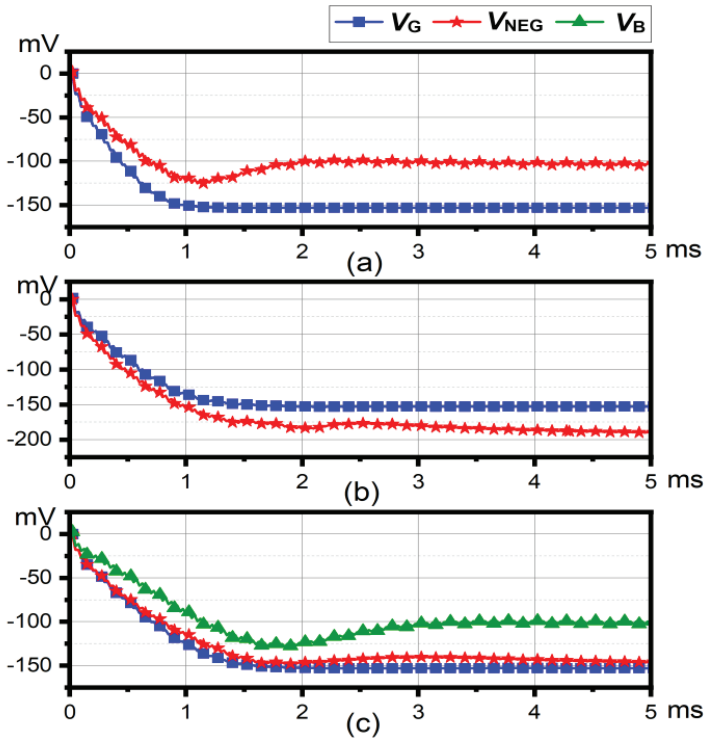


Figure 6. Simulated results of the negative voltage generator when the level shifter is powered by (**a**) V_{NEG}, (**b**) V_G, (**c**) V_B.

Monte Carlo simulation results of the negative voltage V_{NEG} and bias current of SQI (one branch) are shown in Figure 7, where both random process variations and mismatches were considered. The results of the Monte Carlo simulation with 200 samples show that the average value of V_{NEG} is −147.6 mV and the bias current of SQI is 785.6 nA with a standard deviation of 14.9 mV and 15.2 nA, respectively. The effect of temperature and variable $V_{DD,L}$ on the open-loop gain of SQI is shown in Figure 8. The temperature and variable $V_{DD,L}$ are examined from −15 to 70 degrees Celsius and 0.1 to 0.3-V, respectively. At a temperature of 27 degrees Celsius and a $V_{DD,L}$ of 0.2-V, the open-loop gain of the SQI reaches about 30 dB.

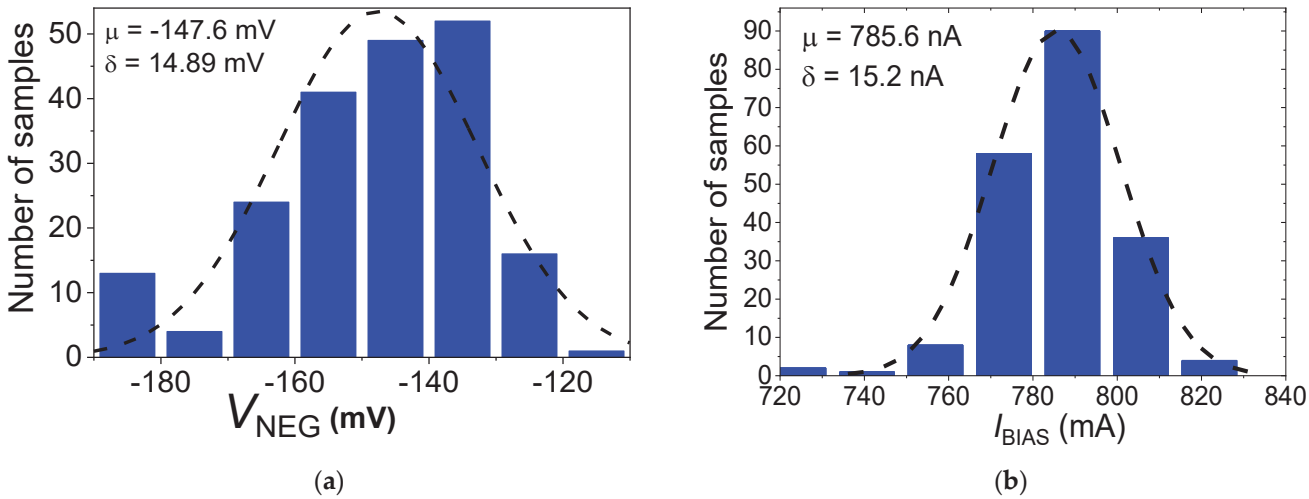


Figure 7. The result of Monte Carlo simulation of (**a**) negative voltage V_{NEG} (**b**) the bias current of SQI.

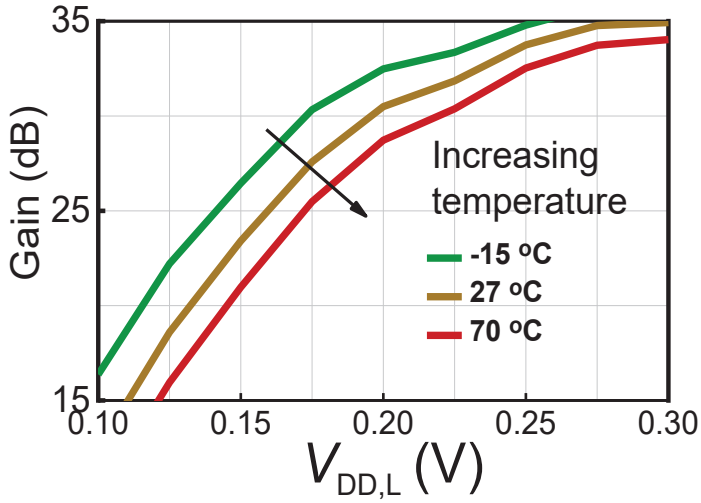


Figure 8. Simulated gain of the SQI stage depending on $V_{DD,L}$ and temperature.

3.3. Middle and Output Stage

To obtain high gain and output swing, the middle and last stage of CCIA employs the FC and the CS amplifiers, respectively. The schematic of FC is shown in Figure 9, while the schematic of CS with the phase margin compensation circuit is shown in Figure 10. Using a supply voltage $V_{DD,H}$ of 0.8-V, the FC is biased a DC current of 40 nA while CS draws a DC current of 80 nA. Although the current consumption is much lower than SQI's current drawing, the effect that the noise of the G_{m2} and G_{m3} have on the input is very small because it is divided into the gain of G_{m1} (normally 30 dB). The FC input pair must use PMOS transistors interfacing to SQI's low output voltage of around 0.1-V. The G_{m3} that employs CS with a passive CMFB circuit built by the pseudo resistors in parallel with MIM capacitors is also shown in Figure 10a. The network compensation capacitor $C_{C1,2}$ is shown in Figure 10b. $C_{C1,2}$ is built from three parallel capacitors (0.62 pF, 5.58 pF, and 23.8 pF); therefore, the value of $C_{C1,2}$ can be changed from 0.62 pF to 30 pF by the controlling switches $SW_{1,2,3}$.

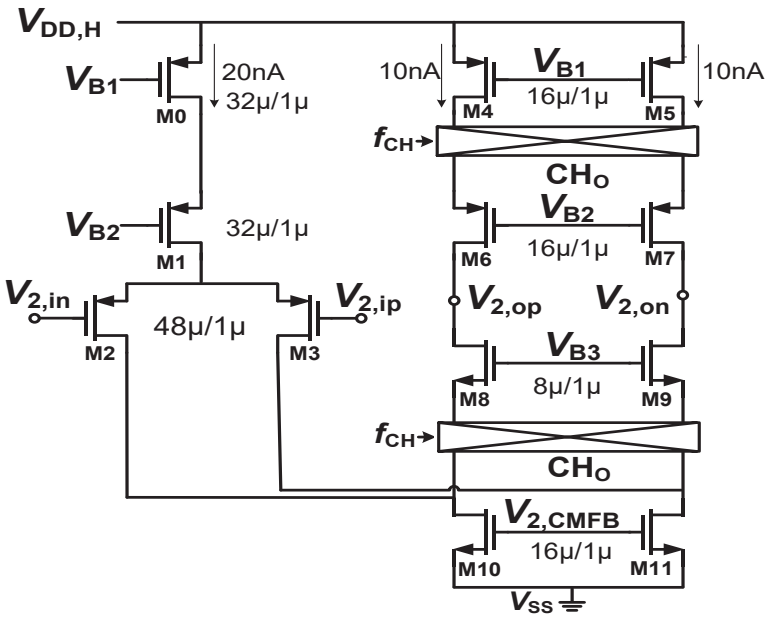
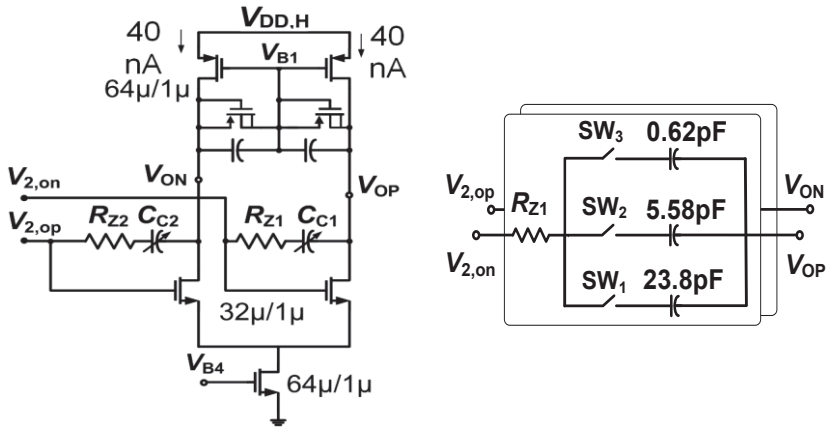


Figure 9. The schematic of the FC amp circuit.



(**a**) (**b**)

Figure 10. (**a**) The schematic of CS amp circuit, (**b**) the schematic of phase margin compensation circuit.

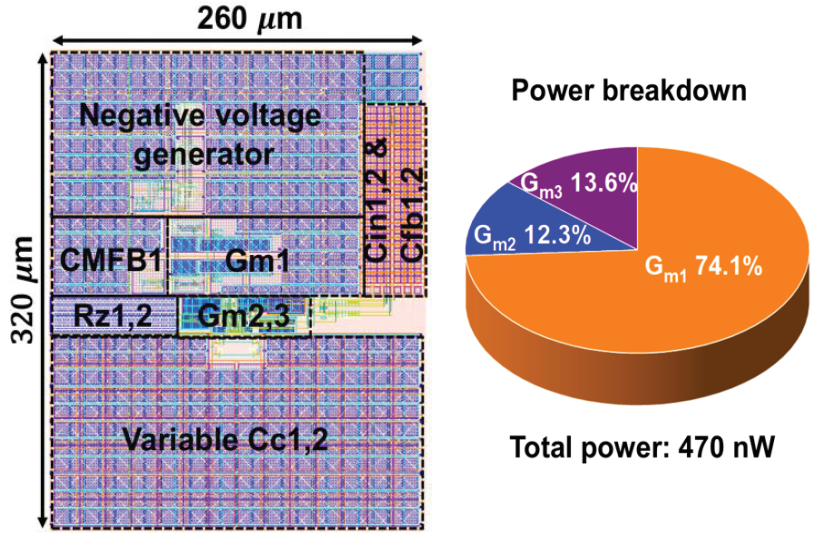
The IRN of the proposed CCIA, $\overline{V_{n,in}^2}$ can be calculated as

$$\begin{aligned}\overline{V_{n,in}^2} &= \left(\frac{C_{tot}}{C_{in1,2}}\right)^2\left(\overline{V_{n,in,Gm1}^2} + \frac{\overline{V_{n,in,Gm2}^2}}{A_{V1}}\right)\\ &= \left(\frac{C_{tot}}{C_{in1,2}}\right)^2\left[\frac{4kTnV_{th}}{I_{BIAS}} + \frac{8kTn}{A_{V1}g_{m1,2}}\left(1+\frac{g_{m3,4}+g_{m9,10}}{g_{m1,2}}\right)\right]\end{aligned} \tag{2}$$

where $C_{tot} = C_{in1,2} + C_{fb1,2} + C_p$, C_p is the parasitic capacitance of the first stage, $\overline{V_{n,in,Gm1}^2}$ and $\overline{V_{n,in,Gm2}^2}$ are the IRN of G_{m1} and G_{m2}, respectively.

4. Simulation Results

In the 0.18 μm CMOS technology, Figure 11 shows the microphotography of the layout and the power decay of the CCIA. The chip area of the CCIA layout occupies only 0.083 mm^2. With a $V_{DD,L}$ of 0.2-V and a $V_{DD,H}$ of 0.8-V, the simulated total power dissipation of the CCIA is 470 nW. G_{m1}, G_{m2}, and G_{m3} consume 74.1%, 12.3%, and 13.6% of the power, respectively.



(**a**) (**b**)

Figure 11. (**a**) Microphotograph and (**b**) the power breakdown of the fabricated CCIA.

The amplitude–frequency response and Monte Carlo simulation of the midband gain of the proposed CCIA are shown in Figure 12. The closed-loop gain reaches 40 dB while passing 200 samples, the Monte Carlo simulation results of the midband gain show that the closed-loop mean value of the CCIA gain is 39.4 dB with a standard deviation of 24.8 mdB. Since the capacitance value of $C_{C1,2}$ is programmable, the bandwidth of the CCIA can be successfully adjusted from 0.2 to 10 kHz. This design is suitable for recording biomedical signals with variable frequency bands. The Monte Carlo simulation results of the power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR) are shown in Figure 13 after a run of 200 samples. Figure 13 shows the average value of PSRR of 87.6 dB at a supply voltage of 0.2-V and CMRR of 117.7 dB with standard deviations of 24.4 and 32.3 dB, respectively.

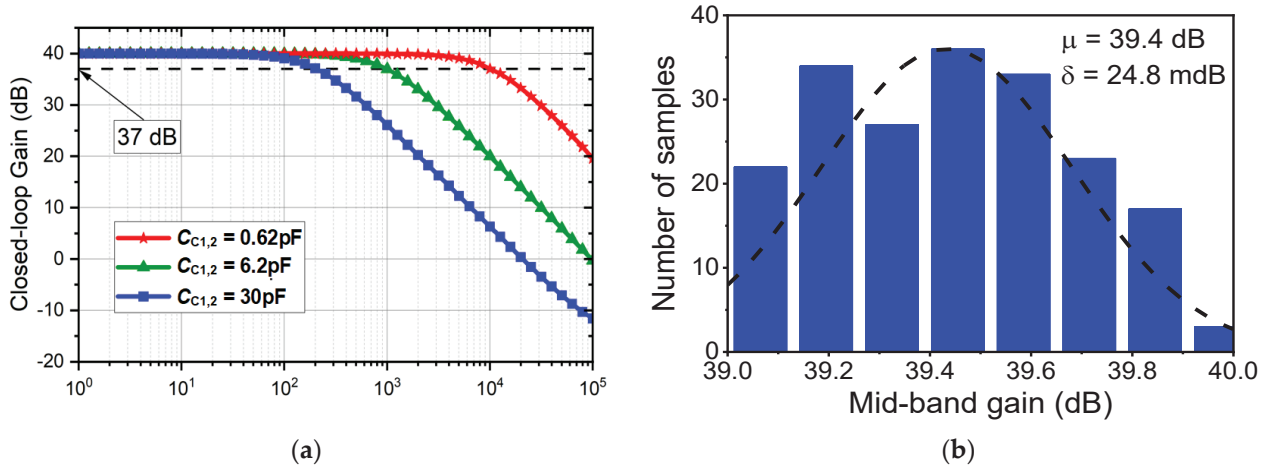


Figure 12. (**a**) The CCIA's variable bandwidth of the transfer function, (**b**) CCIA's the Monte Carlo Simulation of the middle-band gain.

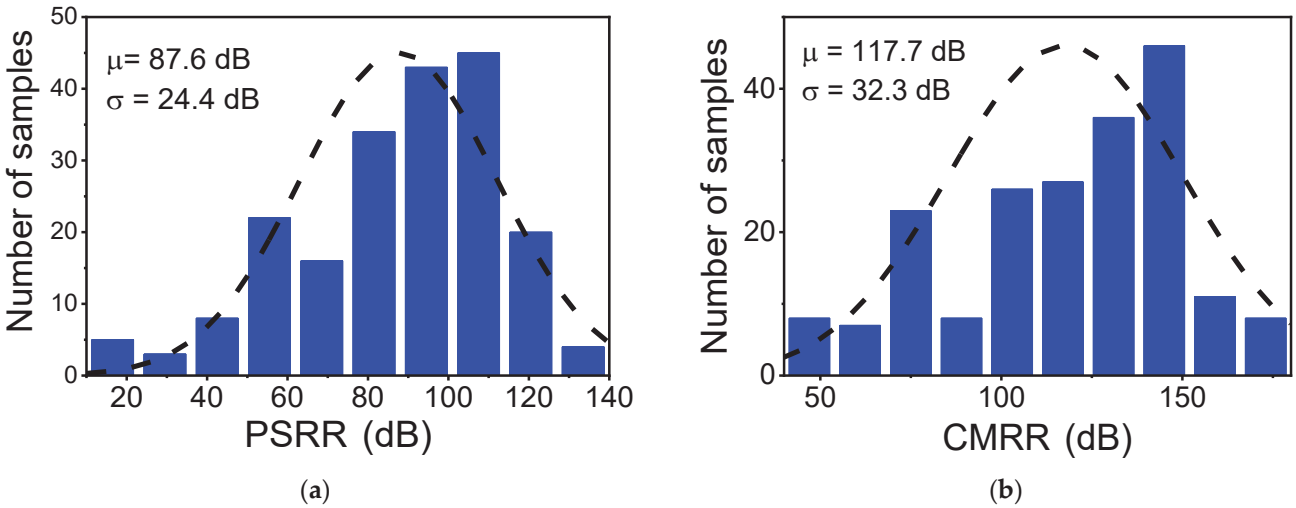


Figure 13. The Monte Carlo simulation result of (**a**) the CCIA's PSRR, (**b**) the CCIA's CMRR.

Figure 14 shows the input noise of the proposed CCIA. At a bandwidth of 1 kHz, the IRN of the CCIA is 0.9 μV_{rms} with a thermal noise of 28 nV/$\sqrt{Hz}$ and a $1/f$ corner of 4 Hz. To investigate the effect of process corners on noise, Monte Carlo simulations were performed with random mismatches of the devices with 200 samples. Figure 15a shows how the IRN of the proposed amplifier changes from 0.894 to 0.963 μV_{rms} over several process corners, while Figure 15b shows the average IRN, which is 0.916 μV_{rms}, with a standard deviation of 62.2 nV_{rms}. The performances of the proposed CCIA operating in different bandwidth modes are summarized in Table 1. The IRN of the proposed CCIA

over the bandwidths of 0.2/1/10 kHz is 0.4/0.9/2.8 μV_{rms}. NEF and PEF show practically comparable values of 1.49 and 0.56, respectively, when the bandwidth changes as the IRN scales with the integrated bandwidths.

$$^{\dagger}\text{NEF} = V_{\text{ni,rms}} \times \sqrt{\frac{I_{\text{DC}}}{\pi V_T 4kT \times BW}}; \; ^{\dagger\dagger}\text{PEF} = V_{\text{ni, rms}}^2 \frac{2P_{\text{DC}}}{\pi V_T 4kT \times BW} = \text{NEF}^2 \times V_{\text{DD}} \quad (3)$$

where I_{DC} is the total current consumption, V_{T} is the thermal voltage, k is the Boltzmann constant, BW is the bandwidth of the proposed CCIA over which the noise is integrated, and V_{DD} is the voltage supply.

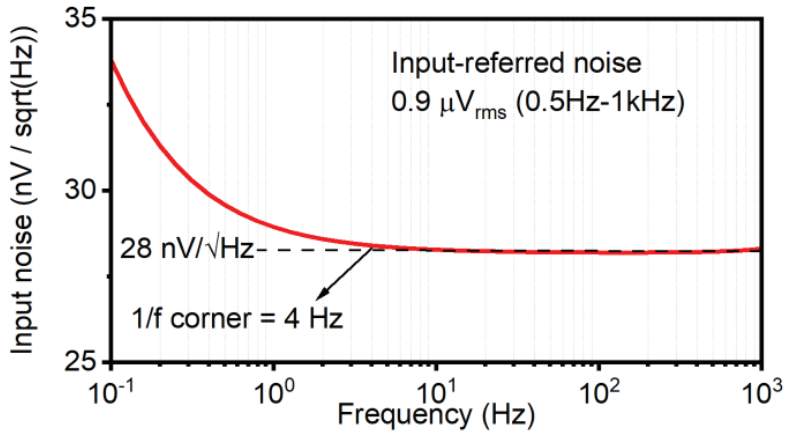
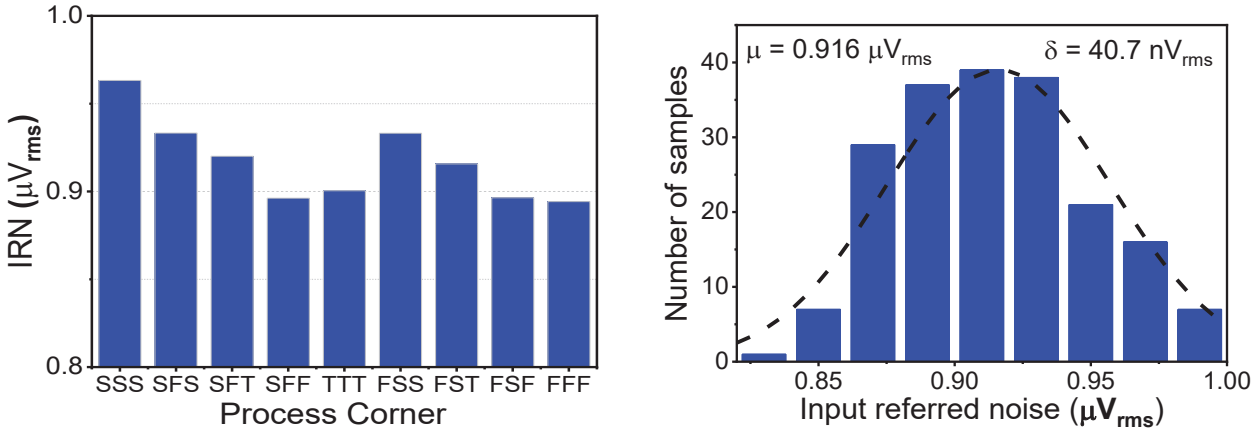


Figure 14. The simulation result of the CCIA's input-referred noise.



(**a**) (**b**)

Figure 15. The simulation result of (**a**) the CCIA's IRN depending on the process corners and (**b**) the CCIA's input-referred noise.

Table 1. Performance analysis with varying bandwidth.

Miller Compensate Capacitors $C_{C1,2}$ (pF)	**30**	**6.2**	**0.62**
Bandwidth—BW (kHz)	0.2	1	10
Thermal noise (nV/$\sqrt{}$H z)	28	28	28
Input-referred noise—$V_{\text{ni,rms}}$ (μV_{rms})	0.4	0.9	2.8
Noise Efficiency Factor (†NEF)	1.49	1.49	1.47
Power Efficiency Factor (††PEF)	0.56	0.56	0.55

Table 2 contains several references with simulation results, including [6,19–21] for a fair comparison. The key design specifications such as power consumption, bandwidth, thermal noise, CMRR, PSRR, NEF, and PEF are summarized in this table to compare the achieved performance of the proposed design with the state-of-the-art designs. By choosing different bandwidths, the proposed CCIA achieves a competitive PEF of about 0.56 with a low input noise of 28 nV/$\sqrt{}$Hz and a noise corner of up to 4 Hz with a power consumption of 0.47 μW.

Table 2. Performance comparison of the proposed CCIA.

Ref.	**[6]**	**[16]**	**[17]**	**[19]**	**[20]**	**[21]**	**[22]**	**[23]**	**This Work**
Year	2022	2017	2021	2020	2020	2018	2022	2018	2023
Supply (V)	1	0.2/0.8	0.2/0.8	1.8	1.2	1	0.5/1.8	1.5/3.3	0.2/0.8
Power (μW)	1.21	0.79	0.52	3.96	1.9	0.96	4.5	330	0.47
Gain (dB)	40	57.8	39.6	31.7	58.4	62	60	1/12/20/40	40
Bandwidth (kHz)	0.8	0.67	0.8	9	8.7	0.23	300	1250	0.2/1/10
Flexible Bandwidth	N	N	N	N	Y	N	N	N	Y
Thermal noise (nV/$\sqrt{}$Hz)	121	36	32	49.5	N/A	N/A	13	60	28
CMRR (dB)	108	85	104	85	110	88	84	90	117.7
PSRR (dB)	87	80	82	87	87	101	88	100	87.6
†NEF	5.4	2.1	1.7	2.08	1.47	3.34	1.3	29	1.49
††PEF	29.7	1.6	0.7	7.78	2.59	9.06	1.1	N/A	0.56
Tech. (nm)	180	180	180	180	130	180	180	180	180
Sim./Meas.	Sim.	Meas.	Meas.	Sim.	Sim.	Sim.	Meas.	Meas.	Sim.

5. Conclusions

This paper describes the design and simulation of an ultra-low-power, programmable bandwidth, capacitively coupled instrumentation amplifier operating on a 0.2 V supply for biomedical applications. By implementing it in a standard 0.18 μm CMOS technology, the chip area of the CCIA occupies only 0.083 mm^2. By using programmable Miler compensation capacitors, the bandwidth of the CCIA can be changed from 200 Hz to 10 kHz. Thanks to the SQI in the first stage and the chopping technique, the CCIA can achieve high power efficiency and low noise. With a power consumption of only 470 nW at $V_{DD,L}$ of 0.2-V and $V_{DD,H}$ of 0.8-V, the prototype ultra-low-power amplifier IC achieves a closed-loop gain of 40 dB, a CMRR of 117.7 dB and a PSRR of 87.6 dB. The CCIA thermal noise is 28 nV/$\sqrt{}$Hz, resulting in an IRN of 0.9 μV_{rms} over a bandwidth of 1 kHz. Therefore, NEF of 1.49 and PEF of 0.56 are achieved. This shows that the performance of the proposed CCIA can be compared with the latest studies.

Author Contributions: Conceptualization, X.T.P., X.T.K. and M.K.H.; methodology, X.T.P., X.T.K. and M.K.H.; software, X.T.P.; formal analysis, X.T.K. and M.K.H.; writing—original draft preparation, X.T.P.; writing—review and editing, X.T.K. and M.K.H.; visualization, X.T.P. and M.K.H.; supervision, X.T.K.; project administration, X.T.P.; funding acquisition, X.T.P., X.T.K. and M.K.H. All authors have read and agreed to the published version of the manuscript.

Funding: The research was funded by Hanoi University of Industry Research Fund under grant number 19-2022-RD/HD-DHCN.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Wang, S.; Koickal, T.J.; Hamilton, A.; Mastropaolo, E.; Cheung, R.; Abel, A.; Smith, L.S.; Wang, L. A Power-Efficient Capacitive Read-Out Circuit with Parasitic-Cancellation for MEMS Cochlea Sensors. *IEEE Trans. Biomed. Circuits Syst.* **2016**, *10*, 25–37. [CrossRef] [PubMed]
2. Casson, A.J.; Yates, D.C.; Smith, S.J.M.; Duncan, J.S.; Rodriguez-Villegas, E. Wearable Electroencephalography. *IEEE Eng. Med. Biol. Mag.* **2010**, *29*, 44–56. [CrossRef] [PubMed]
3. Lin, C.T.; Ko, L.W.; Chang, M.H.; Duann, J.R.; Chen, J.Y.; Su, T.P.; Jung, T.P. Review of wireless and wearable electroencephalogram systems and brain-computer interfaces—A mini-review. *Gerontology* **2010**, *56*, 112–119. [CrossRef] [PubMed]
4. Fiedler, P.; Mühle, R.; Griebel, S.; Pedrosa, P.; Fonseca, C.; Vaz, F.; Zanow, F.; Haueisen, J. Contact Pressure and Flexibility of Multipin Dry EEG Electrodes. *IEEE Trans. Neural Syst. Rehabil. Eng.* **2018**, *26*, 750–757. [CrossRef] [PubMed]
5. Chandrakumar, H.; Marković, D. A high dynamic-range neural recording chopper amplifier for simultaneous neural recording and stimulation. *IEEE J. Solid-State Circuits* **2017**, *52*, 2811–2828. [CrossRef]
6. Pham, X.T.; Vu, T.K.; Nguyen, T.D.; Pham, N.L. A 1.2-μW 41-dB Ripple Attenuation Chopper Amplifier Using Auto-Zero Offset Cancelation Loop for Area-Efficient Biopotential Sensing. *Electronics* **2022**, *11*, 1149. [CrossRef]
7. Muller, R.; Gambini, S.; Rabaey, J.M. A 0.013 mm^2, 5 μW, DC-Coupled Neural Signal Acquisition IC with 0.5 V Supply. *IEEE J. Solid-State Circuits* **2012**, *47*, 232–243. [CrossRef]
8. Razavi, B. *Design of Analog CMOS Integrated Circuits*, International ed.; Mc Graw Hill: New York, NY, USA, 2003.
9. Ha, H.; Hoof, C.V.; Helleputte, N.V. Measurement and Analysis of Input-Signal Dependent Flicker Noise Modulation in Chopper Stabilized Instrumentation Amplifier. *IEEE Solid-State Circuits Lett.* **2018**, *4*, 90–93. [CrossRef]
10. Pham, X.T.; Nguyen, N.T.; Nguyen, V.T.; Lee, J.-W. A 0.6-μW chopper amplifier using a noise-efficient DC servo loop and squeezed-inverter stage for power-efficient biopotential sensing. *Sensors* **2020**, *20*, 2059. [CrossRef] [PubMed]
11. Chandrakumar, H.; Marković, D. An 80-mVpp Linear-Input Range, 1.6-GΩ Input Impedance, Low-Power Chopper Amplifier for Closed-Loop Neural Recording That Is Tolerant to 650-mVpp Common-Mode Interference. *IEEE J. Solid-State Circuits* **2017**, *52*, 2811–2828. [CrossRef]
12. Xu, J.; Lin, Q.; Ding, M.; Li, Y.; Van Hoof, C.; Serdijn, W.; Van Helleputte, N. A 0.6 V 3.8 μW ECG/bio-impedance monitoring IC for disposable health patch in 40 nm CMOS. In Proceedings of the 2018 IEEE Custom Integrated Circuits Conference (CICC), San Diego, CA, USA, 8–11 April 2018.
13. Muller, R.; Le, H.P.; Li, W.; Ledochowitsch, P.; Gambini, S.; Bjorninen, T.; Koralek, A.; Carmena, J.M.; Maharbiz, M.M.; Alon, E.; et al. A Minimally Invasive 64-Channel Wireless μECoG Implant. *IEEE J. Solid-State Circuits* **2015**, *50*, 344–359. [CrossRef]
14. Park, J.H.; Tang, T.; Zhang, L.; Ng, K.A.; Gammad, G.G.L.; Yen, S.C.; Yoo, J. A 15-Channel Orthogonal Code Chopping Instrumentation Amplifier for Area-Efficient, Low-Mismatch Bio-Signal Acquisition. *IEEE J. Solid-State Circuits* **2020**, *55*, 2771–2780. [CrossRef]
15. Nguyen, T.V.; Han, H.-D.; Pham, N.L.; Pham, X.T.; Hoang, M.K. A 0.47-μW Multi-stage Low Noise Amplifier Employing 0.2-V-supply OTA. In Proceedings of the 2022 IEEE Ninth International Conference on Communications and Electronics (ICCE), Nha Trang, Vietnam, 27–29 July 2022.
16. Yaul, F.M.; Chandrakasan, A.P. A noise-efficient 36 nV/$\sqrt{\text{Hz}}$ chopper amplifier using an inverter-based 0.2-V supply input stage. *IEEE J. Solid-State Circuits* **2017**, *52*, 3032–3042. [CrossRef]
17. Pham, X.T.; Nguyen, V.-N.; Kim, J.-S.; Lee, J.-W. A 0.52 μW, 38 nV/$\sqrt{\text{Hz}}$ chopper amplifier with a low-noise DC servo loop, an embedded ripple reduction loop, and a squeezed inverter stage. *IEEE Trans Circuits Syst. II Express Briefs* **2021**, *68*, 1793–1797. [CrossRef]
18. Huang, G.; Yin, T.; Wu, Q.; Zhu, Y.; Yang, H. A 1.3 μW 0.7 μV_{RMS} chopper current-reuse instrumentation amplifier for EEG applications. In Proceedings of the 2015 IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, Portugal, 24–27 May 2015.
19. Liu, Y.; Zhou, Z.; Zhou, Y.; Li, W.; Wang, Z. A Low-Noise Chopper Amplifier with Offset and Low-Frequency Noise Compensation DC Servo Loop. *Electronics* **2020**, *9*, 1797. [CrossRef]
20. Omidvar, A.; Shaterian, M. A low-power digitally programmable neural recording amplifier with selectable multiunit activity (MUA) and local field potential (LFP) recording modes. *Microelectron. J.* **2020**, *95*, 104654. [CrossRef]
21. Nasseriana, M.; Peiravia, A.; Moradi, F. A fully-integrated 16-channel EEG readout front-end for neural recording applications. *AEU—Int. J. Electron. Commun.* **2018**, *94*, 109–121.
22. Fang, L.; Gui, P. A Low-Noise Low-Power Chopper Instrumentation Amplifier with Robust Technique for Mitigating Chopping Ripples. *IEEE J. Solid-State Circuits* **2022**, *57*, 1800–1811. [CrossRef]
23. Del Cesta, S.; Ria, A.; Piotto, M.; Simmarano, R.; Bruschi, P. A compact current-mode instrumentation amplifier for general-purpose sensor interfaces. *AEU—Int. J. Electron. Commun.* **2018**, *92*, 8–14.

Journal of
Low Power Electronics and Applications

MDPI

Article

A 0.5 V, 32 nW Compact Inverter-Based All-Filtering Response Modes Gm-C Filter for Bio-Signal Processing

Ali Namdari *, Orazio Aiello and Daniele D. Caviglia

Department of Electrical, Electronic, Telecommunications Engineering and Naval Architecture (DITEN), University of Genova, Via Opera Pia 11a, I-16145 Genoa, Italy; orazio.aiello@unige.it (O.A.)
* Correspondence: ali.namdari@edu.unige.it

Abstract: A low-power, low-voltage universal multi-mode Gm-C filter using a 180 nm TSMC technology node is presented in this paper. The proposed filter employs only three transconductance operational amplifiers (OTAs) operating in the sub-threshold region with a supply voltage of 0.5 V, resulting in a power consumption of 32 nW. Moreover, without additional active elements, the proposed circuit can operate various functional modes, such as voltage, current, transconductance, and trans-resistance. The filter's frequency, centered at 462 Hz, and a compact and low-power solution showing only 93.5 μVrms input-referred noise make the proposed filter highly suitable for bio-signal processing.

Keywords: low-power; low-voltage; Gm-C; universal filter; CMOS

1. Introduction

Nowadays, low-power techniques in integrated circuits (ICs) design have gained a critical role in low-power application systems. Several advanced approaches have been employed to reduce power consumption, including lowering the supply voltage, bulk-driven techniques, floating gates, and biasing transistors in the subthreshold region [1–3]. Among these, reducing the supply voltage directly reduces energy consumption, extending operation within a given power budget [3–8]. In any case, the most extreme care ought to be given to not jeopardize the proper operation of the circuit, characterized at the application level. This is particularly important for low-power bio-signal sensing devices in biomedical applications that are frequently combined with devices that gather and store energy [9–11]. However, if a high supply voltage is required, the system should be equipped with DC/DC or AC/DC converters, depending on the energy available source type [12,13]. When the converters are used in energy harvester systems, the conversion efficiency can be estimated in the range between 40% and 80%, leading to power waste [14]. As a consequence, to improve the performance and efficiency of an energy-harvested system, the use of low-power techniques will be fundamental [15–17].

From the perspective of making sensory devices, integrated filter blocks exhibit advantageous features, such as signal conditioning capabilities, and the elimination of interference and noise. One of the common filter topologies is Active-RC, which is usually used in communication systems [18]. Despite its good accuracy and low distortion, it cannot be used in applications that require low power. In analog integrated circuits, Gm-C filters are among the main building blocks, and their use has led to excellent performance, both in terms of chip size and power consumption [19–22]. An additional way to further reduce the power consumption of Gm-C filters is to implement their operational transconductance amplifiers (OTAs) by using inverter-based topologies. In fact, inverter-based OTAs offer supply voltage scalability, and thus are very effective at reducing power consumption. A range of ultra-low power analog filters with inverter-based topologies has been described in [23–25], which feature a high-frequency response and low power consumption. For different applications, analog filters with different frequency responses are required, including

low-pass (LP), high-pass (HP), band-reject (BR), all-pass (AP), and band-pass (BP). Therefore, the design of a universal filter capable of generating all possible filtering responses is often required [26,27]. There are several modes of operation for multi-mode analog filters, such as voltage mode (VM), current mode (CM), trans-resistance mode (TRM), and transconductance mode (TCM). This paper describes a low-power integrated Gm-C filter capable of generating all filtering responses under the respective operation modes.

This paper is structured as follows: Section 2 outlines the proposed filter design, while Section 3 presents the simulation results. Section 4 details the noise analysis, and Section 5 covers the sensitivity analysis. Section 6 compares the proposed filter with the state of the art. Finally, conclusions are drawn in Section 7.

2. The Proposed Filter Design

Figure 1 depicts the proposed ultra-low-power universal Gm-C filter, capable of operating in various filtering modes. i_{in1}, i_{in2}, and i_{in3} represent current inputs, while v_{in1}, v_{in2}, and v_{in3} correspond to voltage inputs. v_{OUT} denotes the output voltage, and i_{OUT} represents the output current.

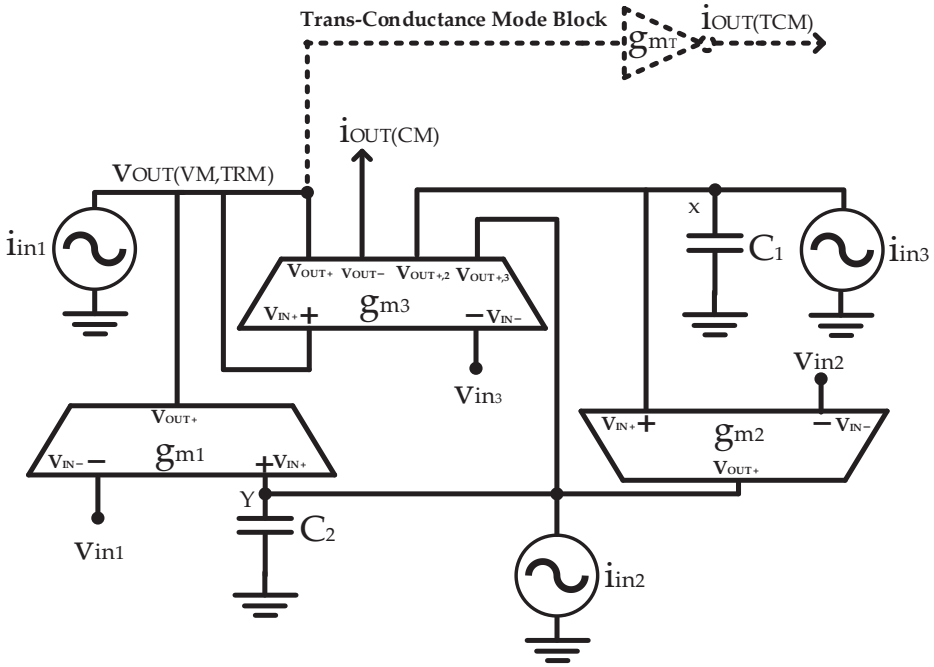


Figure 1. The proposed universal multi-mode Gm-C filter.

The proposed filter can operate in voltage, current, trans-resistance, and transconductance modes. It is composed of three gm blocks; g_{m1}, g_{m2}, and g_{m3} in Figure 1, respectively. When a transconductance mode is required, a dedicated transconductance mode block g_{mT} is added to the basic filter (dashed line in Figure 1). Furthermore, to further investigate the transfer function, Figure 2 reports the signal flow graph (SFG) of the proposed circuit. Defining D(s) a polynomial function as:

$$D(s) = s^2 + \frac{g_{m1}}{C_2}s + \frac{g_{m2}g_{m1}}{C_2C_1} \tag{1}$$

The transfer functions that describe the behavior of the universal multi-mode Gm-C filter in the different operating modes are as follows:

$$v_{OUT(VM)} = \frac{D(s)v_{in3} + \frac{g_{m2}g_{m1}}{g_{m3}C_2}sv_{in2} + \frac{g_{m1}}{g_{m3}}s^2v_{in1}}{D(s)} \tag{2}$$

$$i_{OUT(TCM)} = \frac{g_{mT}\left[D(s)v_{in3} + s\frac{g_{m2}g_{m1}}{g_{m3}C_2}v_{in2} + \frac{g_{m1}}{g_{m3}}s^2 v_{in1}\right]}{D(s)} \quad (3)$$

$$i_{OUT(CM)} = \frac{s^2 i_{in1} + s\frac{g_{m1}}{C_2}i_{in2} + \frac{g_{m2}g_{m1}}{C_2C_1}i_{in3}}{D(s)} \quad (4)$$

$$v_{OUT(TRM)} = \frac{s^2 i_{in1} + s\frac{g_{m1}}{C_2}i_{in2} + \frac{g_{m2}g_{m1}}{C_2C_1}i_{in3}}{g_{m3}D(s)} \quad (5)$$

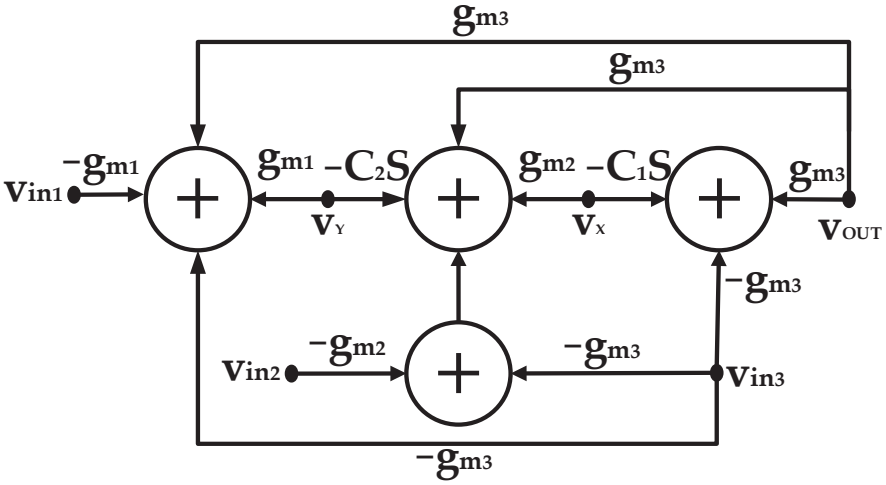


Figure 2. The signal flow graph of the Gm-C proposed filter.

2.1. Current and Trans-Resistance Modes

When $v_{in1} = v_{in2} = v_{in3} = 0$, the filter operates in the current mode, and its filtering responses are obtained as:

Low-Pass (LP): if $i_{in} = i_{in3}$; $i_{in1} = i_{in2} = 0$

$$\frac{i_{OUT(LP)}}{i_{in}} = \frac{\frac{g_{m2}g_{m1}}{C_2C_1}}{D(s)}; \quad \frac{v_{OUT(LP)}}{i_{in}} = -\frac{\frac{g_{m2}g_{m1}}{C_2C_1}}{g_{m3}D(s)} \quad (6)$$

High-Pass (HP): if $i_{in} = i_{in1}$; $i_{in2} = i_{in3} = 0$

$$\frac{i_{OUT(HP)}}{i_{in}} = \frac{s^2}{D(s)}; \quad \frac{v_{OUT(HP)}}{i_{in}} = -\frac{s^2}{g_{m3}D(s)} \quad (7)$$

Band-Pass (BP): if $i_{in} = i_{in2}$; $i_{in1} = i_{in3} = 0$

$$\frac{i_{OUT(BP)}}{i_{in}} = \frac{\frac{g_{m1}}{C_2}s}{D(s)}; \quad \frac{v_{OUT(BP)}}{i_{in}} = -\frac{\frac{g_{m1}}{C_2}s}{g_{m3}D(s)} \quad (8)$$

Band-Reject (BR): if $i_{in} = i_{in1} = i_{in3}$; $i_{in2} = 0$

$$\frac{i_{OUT(BR)}}{i_{in}} = \frac{s^2 + \frac{g_{m2}g_{m1}}{C_2C_1}}{D(s)}; \quad \frac{v_{OUT(BR)}}{i_{in}} = -\frac{s^2 + \frac{g_{m2}g_{m1}}{C_2C_1}}{g_{m3}D(s)} \quad (9)$$

All-Pass (AP): if $i_{in} = i_{in1} = i_{in2} = i_{in3}$

$$\frac{i_{OUT(AP)}}{i_{in}} = \frac{s^2 + \frac{g_{m1}}{C_2}s + \frac{g_{m2}g_{m1}}{C_2C_1}}{D(s)}; \quad \frac{v_{OUT(AP)}}{i_{in}} = -\frac{s^2 + \frac{g_{m1}}{C_2}s + \frac{g_{m2}g_{m1}}{C_2C_1}}{g_{m3}D(s)} \quad (10)$$

2.2. Voltage and Transconductance Modes

When $i_{in1} = i_{in2} = i_{in3} = 0$, the voltage mode filtering responses are obtained as:
Low-Pass (LP): if $v_{in} = -v_{in1} = -v_{in2} = v_{in3}$

$$\frac{v_{OUT(LP)}}{v_{in}} = \frac{\frac{g_{m2}g_{m1}}{C_2C_1}}{D(s)}; \quad \frac{i_{OUT(LP)}}{v_{in}} = -g_{mT}\frac{\frac{g_{m2}g_{m1}}{C_2C_1}}{D(s)} \tag{11}$$

High-Pass (HP): if $v_{in} = v_{in1}; v_{in2} = v_{in3} = 0$

$$\frac{v_{OUT(HP)}}{v_{in}} = \frac{\frac{g_{m1}}{g_{m3}}s^2}{D(s)}; \quad \frac{i_{OUT(HP)}}{v_{in}} = -g_{mT}\frac{\frac{g_{m1}}{g_{m3}}s^2}{D(s)} \tag{12}$$

Band-Pass (BP): if $v_{in} = v_{in2}; v_{in1} = v_{in3} = 0$

$$\frac{v_{OUT(BP)}}{v_{in}} = \frac{\frac{g_{m2}g_{m1}}{g_{m3}C_2}s}{D(s)}; \quad \frac{i_{OUT(BP)}}{v_{in}} = -g_{mT}\frac{\frac{g_{m2}g_{m1}}{g_{m3}C_2}s}{D(s)} \tag{13}$$

Band-Reject (BR): if $v_{in} = -v_{in2} = v_{in3}; v_{in1} = 0$

$$\frac{v_{OUT(BR)}}{v_{in}} = \frac{s^2 + \frac{g_{m2}g_{m1}}{C_2C_1}}{D(s)}; \quad \frac{i_{OUT(BR)}}{v_{in}} = -g_{mT}\frac{s^2 + \frac{g_{m2}g_{m1}}{C_2C_1}}{D(s)} \tag{14}$$

All-Pass (AP): if $v_{in} = v_{in3}; v_{in1} = v_{in2} = 0$

$$\frac{v_{OUT(AP)}}{v_{in}} = \frac{s^2 + \frac{g_{m1}}{C_2}s + \frac{g_{m2}g_{m1}}{C_2C_1}}{D(s)}; \quad \frac{i_{OUT(AP)}}{v_{in}} = -g_{mT}\frac{s^2 + \frac{g_{m1}}{C_2}s + \frac{g_{m2}g_{m1}}{C_2C_1}}{D(s)} \tag{15}$$

Furthermore, the filter performance parameters such as the center frequency ω_0 and the quality factor Q can be calculated as:

$$\omega_0 = \sqrt{\frac{g_{m2}g_{m1}}{C_2C_1}} \tag{16}$$

$$Q = \sqrt{\frac{g_{m2}C_2}{g_{m1}C_1}} \tag{17}$$

Table 1 summarizes how different filtering functions come from a different setup of the inputs universal Gm-C filter.

Table 1. The filtering functions of the proposed universal multi-mode Gm-C filter.

Filtering Function	Input for Current and Trans-Resistance Modes	Input for Voltage and Transconductance Modes
LP	i_{in3}	$-v_{in1} = -v_{in2} = v_{in3}$
HP	i_{in1}	v_{in1}
BP	i_{in2}	v_{in2}
BR	$i_{in1} = i_{in3}$	$-v_{in2} = v_{in3}$
AP	$i_{in1} = i_{in2} = i_{in3}$	v_{in3}

3. Simulation Results

3.1. Proposed OTA and Gm-C Structures

The filter's performance has been verified using the 180 nm TSMC technology process. The operational transconductance amplifier (OTA), which is the building block of the proposed filter, as well as the g_{mT} block required for the transconductance mode, are depicted in Figure 3a and Figure 3b, respectively. The body terminals of the NMOS transistors are tied to the ground, while the body terminals of the PMOS are usually tied to

the supply voltage V_{DD}, whether differently specified or not. In fact, the body terminals of the PMOS transistors highlighted in red in Figure 3 are connected together, and available for proper biasing. This voltage allows the center frequency of the Gm-C filter to be adjusted whenever process, supply voltage, and temperature (PVT) variations occur. The inverter-based topology can provide a transconductance gain while the circuit minimizes its power consumption. In particular, the gain of the proposed OTA is:

$$A_V = \frac{\left(g_{m18,21} + g_{m17,22}\right) \cdot \left(g_{m2,11} + g_{m3,12} + g_{m6,9} + g_{m7,10}\right)}{g_{m13,14}} \cdot \left(r_{d18,21} \parallel r_{d16,19}\right) \quad (18)$$

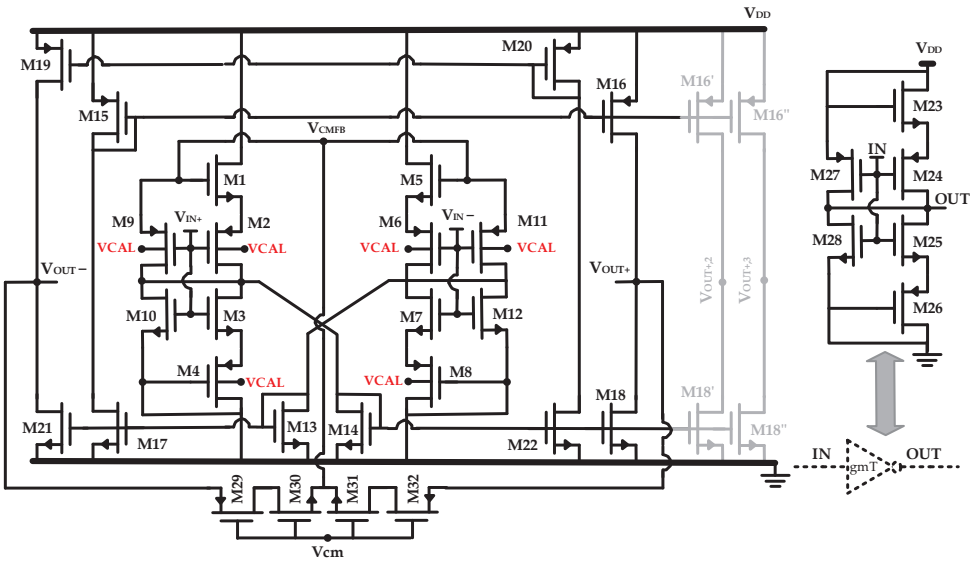


Figure 3. The circuits used in the proposed Gm-C filter (**a**) The proposed OTA (gray branches refer to g_{m3} block only and in red, the terminal for the calibration. (**b**) Transconductance mode g_{mT} block.

Table 2 summarizes the transistor aspect ratios, while Table 3 lists the features of the proposed OTA structure (Figure 3) employed in the Gm-C filter, such as DC gain, gain-bandwidth product (GBW), phase margin, CMRR, and PSRR, referring to a capacitance load value (C_L) of 1 pF. Then, the AC simulation results for the gain and phase of the proposed OTA are shown in Figure 4. Notice that two output replicas (shown in gray in Figure 3) provide additional voltages ($V_{OUT+,2}$ and $V_{OUT+,3}$) as outputs of the transconductance g_{m3} only in the proposed filter (see Figure 1). A still-inverter-based Common-mode Feedback (CMFB) circuit is made by the transistor M29-M30 and M31-M32 with a common mode voltage value of V_{CM} = 0.3 V (see Figure 3). The circuit exhibits an input common mode dynamic range from 0.1 V to 0.4 V.

Table 2. The aspect ratio of the OTA transistors employed in the proposed filter.

Aspect Ratio of OTA	
Transistor	**W/L [μm/μm]**
M1, M3, M5, M7, M10, M12	1/0.3 = 3.33
M2, M4, M6, M8, M9, M11	4/0.3 = 13.33
M13, M14	3/0.3 = 10
M15–M22	3/1 = 3
M29–M32	1/0.18 = 5.56
Aspect ratio of transconductance mode g_{mT} block	
Transistor	W/L [μm/μm]
M23, M25, M28	1/0.18 = 5.56
M24, M26, M27	4/0.18 = 22.22

Table 3. Characteristics of the proposed OTA used in the proposed filter.

Specification	Value
Supply voltage	0.5V
DC gain	46.6 dB
Phase margin	86°
GBW	17.5 kHz
CMRR	48 dB
PSRR	44 dB
Input-referred noise	503 n$\frac{V}{\sqrt{Hz}}$
Power consumption	6.3 nW
C_L	1 pF

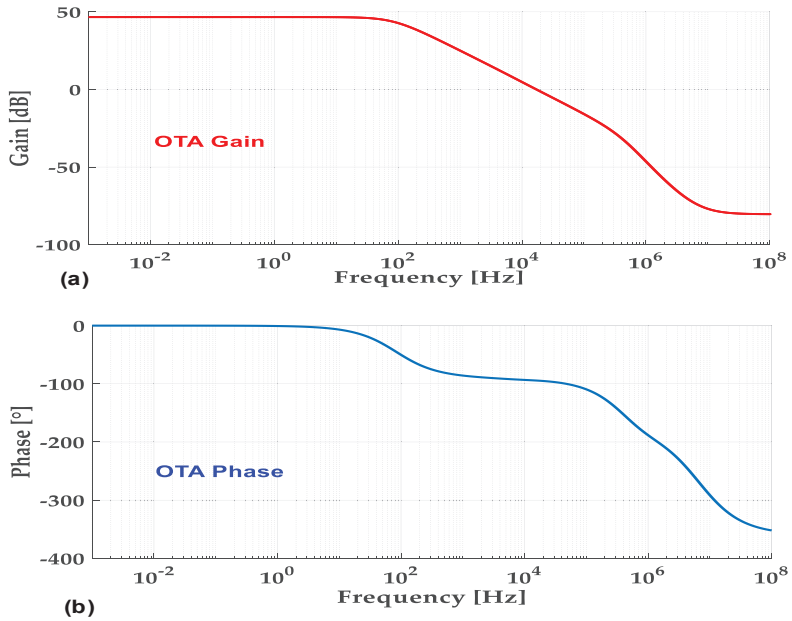


Figure 4. The OTA AC responses: (**a**) gain response; (**b**) phase response.

3.2. Gm-C Structures

Figure 5 illustrates the simulation results for the general proposed multi-mode Gm-C filter, while the transconductance (g_m) and capacitance ($C_1 = C_2$) values are 58 nS and 20 pF.

3.3. PVT Analysis

A Monte-Carlo analysis is performed to find out how process and mismatch variations affect the center frequency of the proposed Gm-C filter. Figure 6 shows the band-pass frequency response for 1000 iterations. Moreover, a complete PVT variation analysis has been performed. In particular, the center frequency of the Gm-C filter is investigated under different corner processes in Table 4. Table 5 refers to the variation in the supply voltage (−/+10%), while Table 6 considers the temperature variation in a temperature range from 0 °C to 40 °C. From these tables, a significant variation in the center frequency of the proposed filter is shown. This can also be highlighted in Figures 7–9. Figure 7 depicts the band-pass frequency responses for the Gm-C filter proposed in various corners. Figures 8 and 9 illustrate the effects of supply voltage variations from 0.45 V to 0.55 V and temperature variations from 0 °C to 40 °C on the band-pass and low-pass filters, respectively.

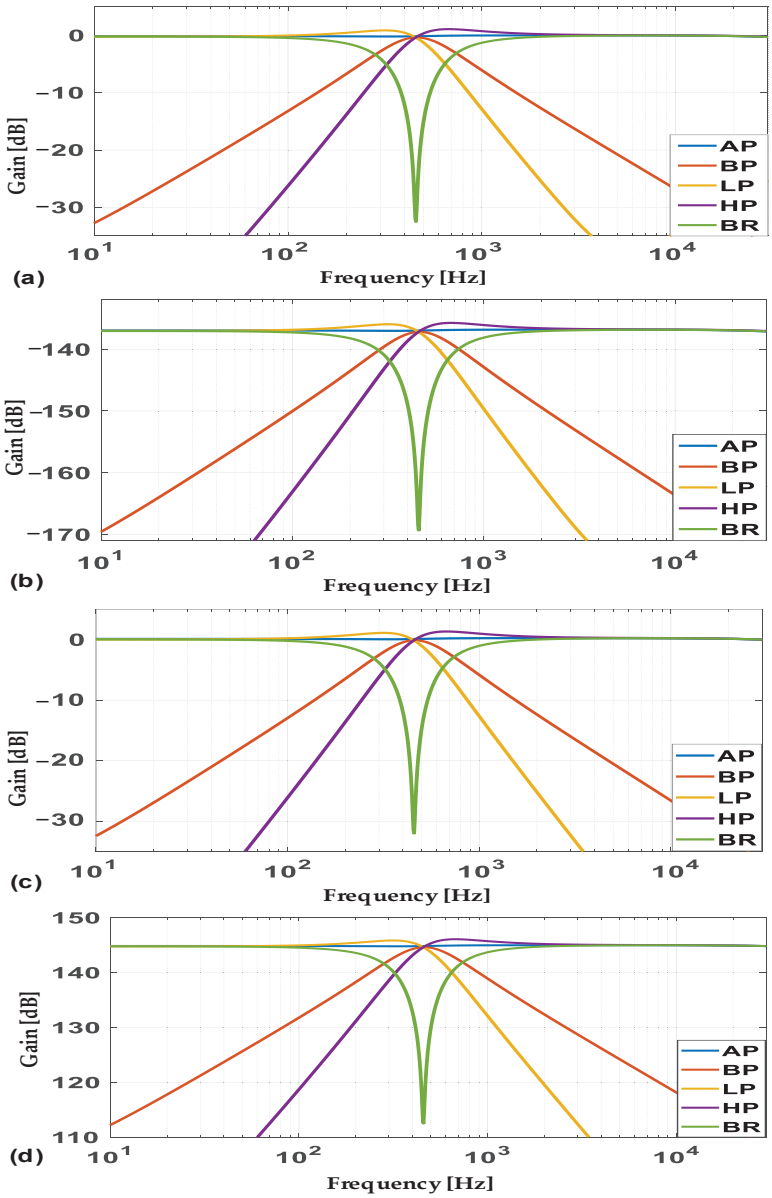


Figure 5. The frequency responses of the proposed Gm-C filter in the various modes: (**a**) voltage mode; (**b**) transconductance mode; (**c**) current mode; (**d**) trans-resistance mode.

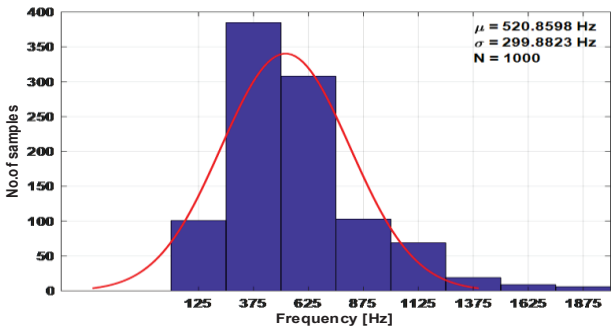


Figure 6. Monte-Carlo simulation results for the center frequency of the band-pass filter.

Table 4. The corner variations of the proposed Gm-C design.

	SS	SF	TT	FS	FF
Power consumption	8.3 nW	94.5 nW	32 nW	10 nW	118 nW
Center frequency	132 Hz	1.34 kHz	462 Hz	129 Hz	1.43 kHz

Table 5. The supply voltage variations (−/+10%) of the proposed Gm-C design.

	0.45 V	0.5 V	0.55 V
Power consumption	42 nW	32 nW	32.7 nW
Center frequency	693.4 Hz	462 Hz	305.5 Hz

Table 6. The temperature variations of the proposed Gm-C design.

	0 °C	10 °C	27 °C	40 °C
Power consumption	10 nW	16 nW	32 nW	41.5 nW
Center frequency	164.5 Hz	247 Hz	462 Hz	760 Hz

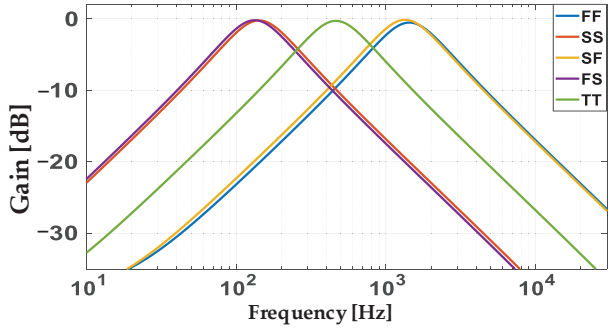


Figure 7. Variations in corner technology for the band-pass frequency response.

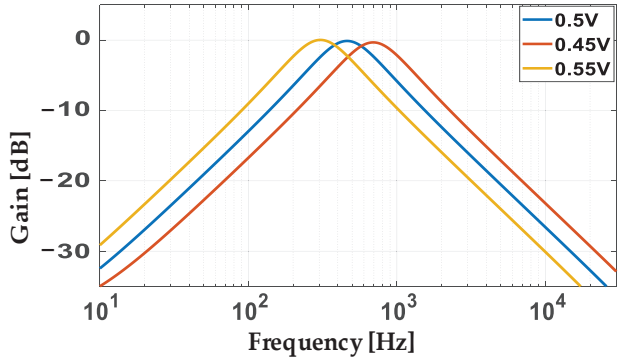


Figure 8. Variations in supply voltage for the band-pass frequency response.

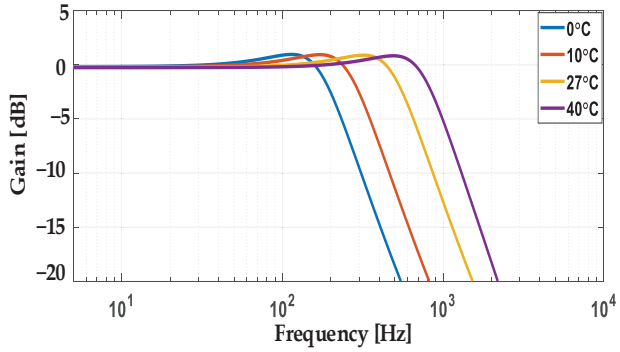


Figure 9. Variations in temperature for the low-pass frequency response.

3.4. Bulk-Biasing Technique

To compensate for the shift of the center frequency of the proposed Gm-C filter due to the PVT variations, calibration by fine-tuning the body bias of the PMOS transistors of the transconductance blocks (see V_{CAL} terminals in Figure 3) is considered. From this perspective, Table 7 shows the values of V_{CAL} to compensate for the variation in the center frequency across the five-corner process. Notice that the center frequency is affected in the corner process SS and FS and SF and FF in 132 mV and 100 mV of drift from the supply voltage allows for the re-centering of the filter on the frequency of 462 Hz. Table 8 shows how a variation of $+/-$ 10% on the supply voltage can be compensated with only 2 mV changes of V_{CAL}. Table 9 reports how the lower temperature affected the center frequency of the filter. Thus, the circuit is suitable for integrated systems for indoor applications.

Table 7. Proposed filter's center frequency regulation using the body-bias tuning V_{CAL} across the corner process.

	SS	**SF**	**TT**	**FS**	**FF**
Body bias of M2, M4, M6, M8, M9, M11	0.368 V	0. 4 V	0.5 V	0.368 V	0.4 V
Power consumption	28.4 nW	31 nW	32 nW	32.2 nW	38 nW
Center frequency	462 Hz	462 Hz	462 Hz	462 Hz	462 Hz

Table 8. Proposed filter's center frequency regulation using the body-bias tuning V_{CAL} for supply voltage changing $+/-$ 10%.

	0.45 V	**0.5 V**	**0.55 V**
Body bias of M2, M4, M6, M8, M9, M11	0.498 V	0.5 V	0.498 V
Power consumption	27.8 nW	32 nW	43.4 nW
Center frequency	462 Hz	462 Hz	462 Hz

Table 9. Proposed filter's center frequency regulation using the body-bias tuning V_{CAL} at different temperatures.

	0 °C	**10 °C**	**27 °C**	**40 °C**
Body bias of M2, M4, M6, M8, M9, M11	0.39 V	0.43 V	0.5 V	0.45 V
Power consumption	28 nW	29.3 nW	32 nW	33 nW
Center frequency	462 Hz	462 Hz	462 Hz	462 Hz

Figure 10 shows a match between the theoretical (given by a math calculation) and simulation results for the proposed Gm-C filter. In particular, the simulation finds a frequency value of 422 Hz, while the theoretical one is $f_0 = \frac{1}{2\pi}\sqrt{\frac{g_{m2}g_{m1}}{C_2C_1}} = 426$ Hz.

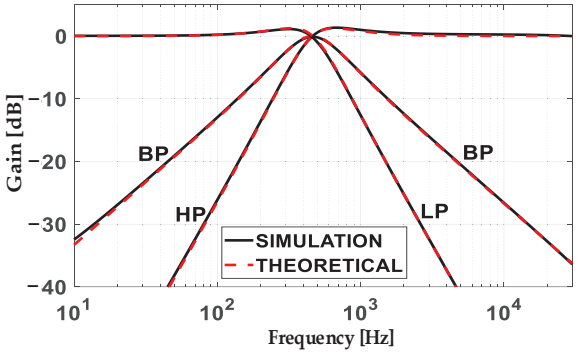


Figure 10. Comparison between simulation and theoretical results for the proposed Gm-C filter.

3.5. Group Delay of the Band-Pass Filter

The general transfer function for the band-pass filter is:

$$H(s) = \frac{\left[\frac{\omega_0}{Q}\right]s}{s^2 + \left[\frac{\omega_0}{Q}\right]s + {\omega_0}^2} \tag{19}$$

where ω_0 is the center pulsation and Q is the quality factor of the filter. The group delay for the band-pass filter is:

$$D(\omega) = \frac{\left[\frac{\omega_0}{Q}\right]\left[{\omega_0}^2 + \omega^2\right]}{\left[{\omega_0}^2 - \omega^2\right]^2 + \left[\frac{\omega_0}{Q}\right]^2\omega^2} \tag{20}$$

Thus, the maximum value of the group delay for the band-pass filter is:

$$D(\omega) = \frac{2}{\left[\frac{\omega_0}{Q}\right]} = \frac{2C_2}{g_{m1}} \tag{21}$$

The group delay is shown in Figure 11: 690 µs is the group delay at the filter's center frequency.

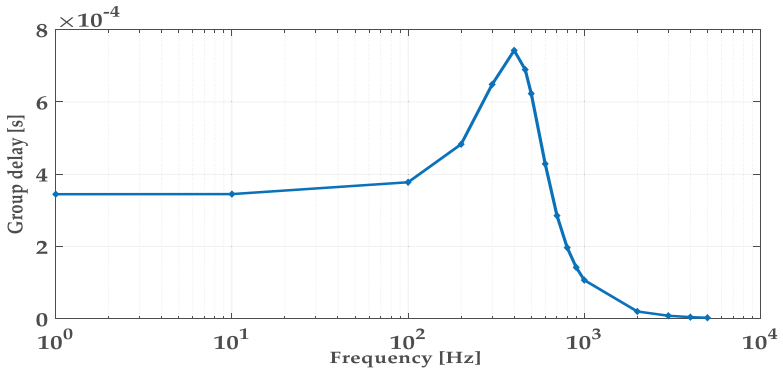


Figure 11. Group delay for the proposed band-pass filter.

3.6. The Linearity Performance of the Proposed Filter

The proposed filter's linearity performance is investigated by applying a 40 mVPP sinusoidal input at 10 Hz. Figure 12 shows the input and output transient simulation results for different responses. Furthermore, as the input signal frequency of 10 Hz is outside the pass band of the band-pass and high-pass filters, their output signals are significantly weakened in comparison to those of the filtering responses, which are approximately the same amplitude as the input signals. Also, the input signal frequency of 462 Hz (center frequency) has been applied, as shown in Figure 13. Figure 14 highlights how the total harmonic distortion (THD) of the proposed Gm-C filter varies due to the input voltage amplitude changes between 40 mVpp and 120 mVpp. The THD values for the proposed filter for different signal amplitudes and across the five corner processes are summarized in Tables 10 and 11, respectively.

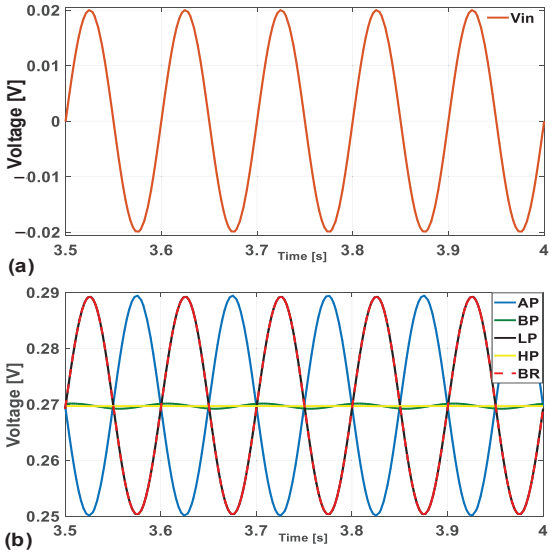


Figure 12. Transient simulation results for the proposed filter: (**a**) input (10 Hz); (**b**) output.

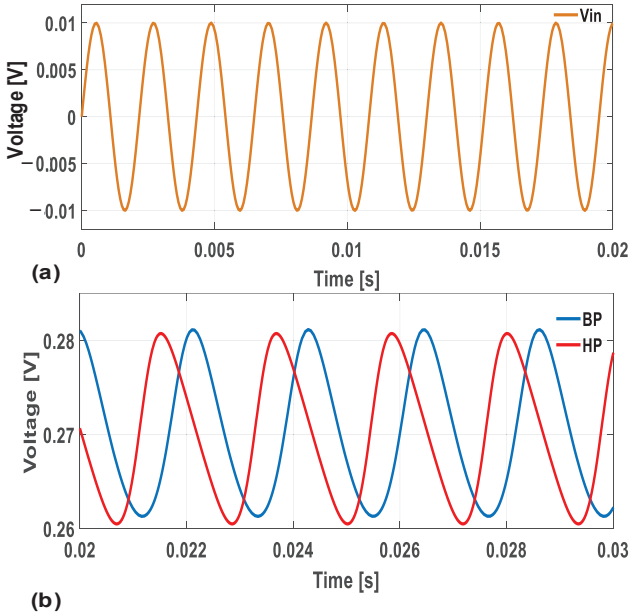


Figure 13. Transient simulation results for the proposed band-pass and high-pass filters at the center frequency (462 Hz): (**a**) input; (**b**) output.

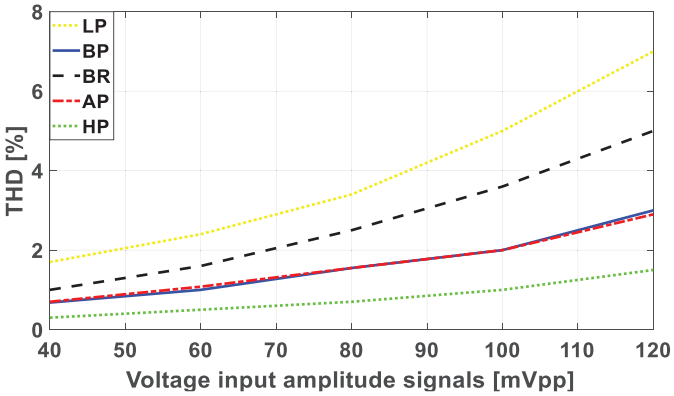


Figure 14. THD versus voltage input amplitudes.

Table 10. THD performance of the proposed filter for different signal amplitudes.

Input Voltage Amplitude (mV_{PP})	THD% at 10 Hz				
	LP	**BP**	**BR**	**AP**	**HP**
40	0.68	1	0.7	0.3	1.7
60	1	1.6	1.08	0.5	2.4
80	1.55	2.5	1.55	0.7	3.4
100	2	3.6	2	1	5
120	3	5	2.9	1.5	7

Table 11. THD performance of the proposed filter for various corner parameters.

Corner Process	THD% at 10 Hz				
	LP	**BP**	**BR**	**AP**	**HP**
SS	2.3	3.7	2.4	0.2	2.8
SF	4.8	6.6	4.8	4.7	8
FS	2	3.3	2.2	0.17	2
FF	0.5	0.3	0.48	0.47	0.94
TT	0.68	1	0.7	0.3	1.7

4. Noise Analysis

Given the low level of the input signal, the noise performance analysis is critical. To understand qualitatively how design parameters affect the overall input-referred noise, the following equations refer to the saturation region model, assumed as the worst-case scenario. In any case, the subthreshold real values are expected to be lower [28–30]. Assuming g_{mINV}, the transconductance at the OTA input terminals is as follows:

$$g_{mINV} = \left[g_{m2} + g_{m3} + g_{m9} + g_{m10}\right] \tag{22}$$

The input-referred thermal and flicker noise values for the OTA used in the proposed Gm-C filter are:

$$\overline{V^2_{n,Thermal}} = 8KT\gamma\left[\frac{g_{m14} + g_{mINV}}{g^2_{mINV}} + 2\frac{g^2_{m14}(g_{m16} + g_{m18})}{g^2_{mINV}\, g^2_{m18}}\right] \tag{23}$$

$$\begin{aligned}\overline{V^2_{n,Flicker}} = {} & \frac{2K_P}{C_{oxf}}\left[\frac{1}{(W{\cdot}L)_2} + \frac{1}{(W{\cdot}L)_9}\right] + \frac{2K_N}{C_{oxf}}\left[\frac{1}{(W{\cdot}L)_3} + \frac{1}{(W{\cdot}L)_{10}} + \frac{{g_{m14}}^2}{{g_{mINV}}^2(W{\cdot}L)_{14}}\right] + \\ & + \frac{4}{C_{oxf}}\frac{{g_{m14}}^2}{{g_{mINV}}^2}\left\{\left[\frac{K_P}{(W{\cdot}L)_{16}} + \frac{K_N}{(W{\cdot}L)_{18}}\right]\left(1 + \frac{{g_{m16}}^2}{{g_{m18}}^2}\right)\right\}\end{aligned} \tag{24}$$

where K is the Boltzmann constant, T is the temperature, γ is the noise factor, K_P and K_N are the flicker noise coefficients of the PMOS and NMOS transistors, C_{OX} is the gate-oxide capacitance, W is the width and L is the length of the transistors. These equations offer design guidelines for noise minimization. The overall noise is:

$$\overline{V^2_{n,in,OTA}} = \overline{V^2_{n,Thermal}} + \overline{V^2_{n,Flicker}} \tag{25}$$

Notice that g_{mINV} is roughly 4× higher than the transconductance of other transistors in the OTA topology in Figure 3. This results in the minimized input-referred noise of the overall Gm-C filter.

Considering ($|H_{N1,2,3}(s)|$) as the transfer function for each OTA input-referred noise and ($|H_B(s)|$), the band-pass filter's transfer function is as follows:

$$|H_{N1}(s)| = \left|\frac{V_{n,OUT1}}{V_{n,in1}}\right| = \left|\frac{\frac{g_{m1}}{g_{m3}}S^2}{D(s)}\right| \tag{26}$$

$$|H_{N2}(s)| = |H_B(s)| = \left|\frac{V_{n,OUT2}}{V_{n,in2}}\right| = \left|\frac{\frac{g_{m2}g_{m1}}{g_{m3}C_2}S}{D(s)}\right| \quad (27)$$

$$|H_{N3}(s)| = \left|\frac{V_{n,OUT3}}{V_{n,in3}}\right| = \left|\frac{s^2 + \frac{g_{m1}}{C_2}s + \frac{g_{m2}g_{m1}}{C_2C_1}}{D(s)}\right| \quad (28)$$

The input-referred noise of the three transconductance blocks for the band-pass filter ($V_{n,in,in1}$, $V_{n,in,in1}$, $V_{n,in,in3}$ in Figure 15) can be expressed by:

$$\overline{V^2_{n,in,in1}} = \left|\frac{V_{n,OUT1}}{H_B(s)}\right|^2 = \overline{V^2_{n,in1}}\left|\frac{H_{N1}(s)}{H_B(s)}\right|^2 = \overline{V^2_{n,in1}}\left[\frac{C_2 s}{g_{m2}}\right]^2 \quad (29)$$

$$\overline{V^2_{n,in,in2}} = \left|\frac{V_{n,OUT2}}{H_B(s)}\right|^2 = \overline{V^2_{n,in2}}\left|\frac{H_{N2}(s)}{H_B(s)}\right|^2 = \overline{V^2_{n,in2}} \quad (30)$$

$$\overline{V^2_{n,in,in3}} = \left|\frac{V_{n,OUT3}}{H_B(s)}\right|^2 = \overline{V^2_{n,in3}}\left|\frac{H_{N3}(s)}{H_B(s)}\right|^2 = \overline{V^2_{n,in3}}\left[\frac{g_{m3}C_2D(s)}{g_{m2}g_{m1}s}\right]^2 \quad (31)$$

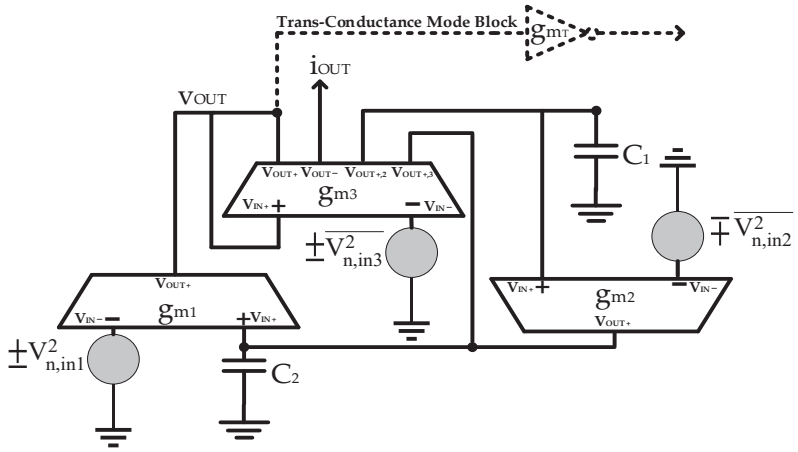


Figure 15. Modeling of the noise equivalent circuit for the proposed universal filter.

Thus, the overall equivalent input-referred noise for the band-pass filter $\overline{V^2_{n,in,BP}}$ is:

$$\overline{V^2_{n,in,BP}} = \overline{V^2_{n,in,in1}} + \overline{V^2_{n,in,in2}} + \overline{V^2_{n,in,in3}} \quad (32)$$

5. Sensitivity Analysis

Naming Š the sensitivity of the K circuit characteristic with respect to the L parameter, is defined as:

$$\check{S}^K_L = \frac{\partial K}{\partial L}\cdot\frac{L}{K} \quad (33)$$

For instance, the sensitivity of the g_{m2} for the current-mode low-pass filter is calculated in (34), which is similar to the sensitivity analysis for g_{m2} in (35).

$$\check{S}^{LPi}_{g_{m2}} = \frac{\partial LP_i}{\partial g_{m2}}\cdot\frac{g_{m2}}{LP} = \frac{g_{m1}C_2C_1D(s) - g_{m2}{g_{m1}}^2}{D(s)^2}\cdot\frac{g_{m2}C_2C_1D(s)}{g_{m2}g_{m1}} = \frac{S^2 + \frac{g_{m1}}{C_2}S}{D_{(s)}} \quad (34)$$

5.1. The Sensitivity Analysis of the Current-Mode Filter

The sensitivity of the universal filter responses in the current mode to the capacitance and transconductance values are as follows:

$$\breve{S}^{LP_i}_{g_{m2}} = -\breve{S}^{LP_i}_{C_1} = \frac{s^2 + \frac{g_{m1}}{C_2}s}{D(s)} \tag{35}$$

$$\breve{S}^{BP_i}_{C_1} = -\breve{S}^{BP_i}_{g_{m2}} = \frac{\frac{g_{m2}g_{m1}}{C_2C_1}}{D(s)} \tag{36}$$

$$\breve{S}^{LP_i}_{g_{m1}} = -\breve{S}^{LP_i}_{C_2} = \breve{S}^{BP_i}_{g_{m1}} = -\breve{S}^{BP_i}_{C_2} = \frac{s^2}{D(s)} \tag{37}$$

$$\breve{S}^{HP_i}_{C_1} = -\breve{S}^{HP_i}_{g_{m2}} = \frac{\frac{g_{m2}g_{m1}}{C_2C_1}}{D(s)} \tag{38}$$

$$\breve{S}^{HP_i}_{C_2} = -\breve{S}^{HP_i}_{g_{m1}} = \frac{\frac{g_{m1}}{C_2}s + \frac{g_{m2}g_{m1}}{C_2C_1}}{D(s)} \tag{39}$$

$$\breve{S}^{BP_i}_{C_1} = \breve{S}^{LP_i}_{C_1} + \breve{S}^{HP_i}_{C1} \tag{40}$$

$$\breve{S}^{BR_i}_{C_2} = \breve{S}^{LP_i}_{C_2} + \breve{S}^{HP_i}_{C_2} \tag{41}$$

$$\breve{S}^{BR_i}_{gm_1} = \breve{S}^{LP_i}_{gm_1} + \breve{S}^{HP_i}_{gm_1} \tag{42}$$

$$\breve{S}^{BR_i}_{gm_2} = \breve{S}^{LP_i}_{gm_2} + \breve{S}^{HP_i}_{gm_2} \tag{43}$$

Notice that the sum of the sensitivity values to the all-filtering responses in the current mode is zero, as reported in the following:

$$\begin{aligned}&\breve{S}^{LP_i}_{g_{m1}} + \breve{S}^{LP_i}_{C_1} + \breve{S}^{LP_i}_{g_{m2}} + \breve{S}^{LP_i}_{C_2} + \breve{S}^{BP_i}_{g_{m1}} + \breve{S}^{BP_i}_{C_1} + \breve{S}^{BP_i}_{g_{m2}} + \breve{S}^{BP_i}_{C_2} + \\ &+\breve{S}^{HP_i}_{g_{m1}} + \breve{S}^{HP_i}_{C_1} + \breve{S}^{HP_i}_{g_{m2}} + \breve{S}^{HP_i}_{C_2} + \breve{S}^{BR_i}_{g_{m1}} + \breve{S}^{BR_i}_{C_1} + \breve{S}^{BR_i}_{g_{m2}} + \breve{S}^{BR_i}_{C_2} = 0\end{aligned} \tag{44}$$

5.2. The Sensitivity Analysis in Voltage-Mode Filter

The sensitivity of the universal filter responses in the voltage mode to the capacitance and transconductance values are as follows:

$$\breve{S}^{LP_v}_{g_{m1}} = -\breve{S}^{LP_v}_{C_2} = \breve{S}^{BP_v}_{g_{m1}} = -\breve{S}^{BP_v}_{C_2} = \breve{S}^{HP_v}_{g_{m1}} = \frac{s^2}{D(s)} \tag{45}$$

$$\breve{S}^{LP_v}_{g_{m2}} = -\breve{S}^{LP_v}_{C_1} = \breve{S}^{BP_v}_{g_{m2}} = \frac{s^2 + \frac{g_{m1}}{C_2}s}{D(s)} \tag{46}$$

$$\breve{S}^{BP_v}_{C_1} = \breve{S}^{HP_v}_{C_1} = -\breve{S}^{HP_v}_{g_{m2}} \frac{\frac{g_{m2}g_{m1}}{C_2C_1}}{D(s)} \tag{47}$$

$$\breve{S}^{HP_v}_{C_2} = \frac{\frac{g_{m1}}{C_2}s + \frac{g_{m2}g_{m1}}{C_2C_1}}{D(s)} \tag{48}$$

$$-\breve{S}^{BP_v}_{g_{m3}} = -\breve{S}^{HP_v}_{g_{m3}} = 1 \tag{49}$$

$$\breve{S}^{BR_v}_{C_1} = \breve{S}^{LP_v}_{C_1} + \breve{S}^{HP_v}_{C1} \tag{50}$$

$$\breve{S}^{BR_v}_{C_2} = \breve{S}^{LP_v}_{C_2} + \breve{S}^{HP_v}_{C_2} \tag{51}$$

$$\breve{S}^{BR_v}_{gm_1} = \breve{S}^{LP_v}_{gm_1} + \breve{S}^{HP_v}_{gm_1} \tag{52}$$

$$\check{S}^{BR_v}_{gm_2} = \check{S}^{LP_v}_{gm_2} + \check{S}^{HP_v}_{gm_2} \tag{53}$$

Again, the sum of the sensitivity values to the all-filtering responses, also in the voltage mode, is zero:

$$\begin{aligned}&\check{S}^{LP_v}_{g_{m1}} + \check{S}^{LP_v}_{C_1} + \check{S}^{LP_v}_{g_{m2}} + \check{S}^{LP_v}_{C_2} + \check{S}^{BP_v}_{g_{m1}} + \check{S}^{BP_v}_{C_1} + \check{S}^{BP_v}_{g_{m2}} + \check{S}^{BP_v}_{C_2} + \\ &\check{S}^{HP_v}_{g_{m1}} + \check{S}^{HP_v}_{C_1} + \check{S}^{HP_v}_{g_{m2}} + \check{S}^{HP_v}_{C_2} + \check{S}^{BR_v}_{g_{m1}} + \check{S}^{BR_v}_{C_1} + \check{S}^{BR_v}_{g_{m2}} + \check{S}^{BR_v}_{C_2} + \check{S}^{BP_v}_{g_{m3}} + \check{S}^{HP_v}_{g_{m3}} = 0\end{aligned} \tag{54}$$

6. Comparison with the State of the Art

Table 12 compares the proposed Gm-C circuit with the state of the art. The proposed filter shows a lower rms input-referred noise than [31–36]. Additionally, the proposed circuit consumes less power and even the figure-of-merit (FOM) for the filter. It is defined as:

$$\text{FOM} = \frac{P}{f \cdot N \cdot DR} \tag{55}$$

where P is the power consumption, f is the center frequency of the Gm-C filter, N is its order, and DR is the dynamic range.

Table 12. Gm-C filter's state-of-the-art comparison referring to their band-pass' central frequency.

	[31]	[32]	[33]	[34]	[35]	[36]	[37]	This Work
Supply voltage [V]	0.6	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Universal	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multi-mode	Yes	Voltage	Yes	Yes	Yes	Voltage	Voltage	Yes
Filter order	2	2	2	2	2	2	2	2
Center frequency [Hz]	5000	254	211	323	114	153	10	462
Dynamic range [dB]	53.2	49.7	58.23	53.2	53.2	50	63	43.59
Rms input-refer. noise [μVrms]	155	116	130	108	208	220	45	93.5
Power consumption [μW]	5.77	0.616	0.281	0.646	0.058	0.037	0.053	0.032
FOM $[10^{-12}$ W $\cdot$Hz$^{-1}\cdot$dB$^{-1}]$	1.26	3.96	0.816	2.187	0.556	2.41	1.88	0.229

7. Conclusions

An ultra-low-power, low-voltage Gm-C filter capable of producing various filtering responses (LP, HP, AP, BP, BR) in four-mode filtering operations has been designed in a 180 nm TSMC technology node. The Gm-C filter performance at a center frequency of 462 Hz has been shown in this paper. Body-bias-driven compensations for all the frequency responses under the PVT variations have also been reported. Also, the THD, the overall input-referred noise, and the sensitivity have been considered. The proposed filter operates at 0.5 V supply voltage with the minimum number of gm blocks, with its building transistors operating in the subthreshold region, showing an overall power consumption of 32 nW.

Author Contributions: Conceptualization, A.N.; methodology, A.N.; validation, A.N.; formal analysis, A.N.; investigation, A.N., O.A, and D.D.C.; resources, O.A. and D.D.C.; data curation, A.N., O.A., and D.D.C.; writing—original draft preparation, A.N.; writing—review and editing, O.A. and D.D.C.; visualization, A.N.; supervision, O.A. and D.D.C.; project administration, O.A., and D.D.C.; funding acquisition, O.A., and D.D.C. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: Data is contained within the article.

Acknowledgments: The authors would like to thank Europractice and TSMC for PDK access.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

TSMC	Taiwan Semiconductor Manufacturing Company
OTA	Transconductance Operational Amplifiers
VM	Voltage Mode
CM	Current Mode
TCM	Transconductance-Mode
TRM	Trans-resistance Mode
LP	Low-Pass
HP	High-Pass
BP	Band-Pass
BR	Band-Reject
AP	All-Pass

References

1. Silva, R.-S.; Rodovalho, L.-H.; Aiello, O.; Rodrigues, C.-R. A 1.9 nW, Sub-1 V, 542 pA/V linear Bulk-Driven OTA with 154 dB CMRR for Bio-Sensing Applications. *J. Low Power Electron. Appl.* **2021**, *11*, 40. [CrossRef]
2. Lopez-Martin, A.; Garde, M.-P.; Algueta-Miguel, J.-M.; Beloso-Legarra, J.; Carvajal, R.-G.; Ramirez-Angulo, J. Energy-Efficient Amplifiers Based on Quasi-Floating Gate Techniques. *Appl. Sci.* **2021**, *11*, 3271. [CrossRef]
3. Rodovalho, L.H.; Aiello, O.; Rodrigues, C.R. Ultra-low-voltage inverter-based Operational Transconductance Amplifiers with Voltage Gain Enhancement by Improved Composite Transistors. *Electronics* **2022**, *9*, 1410. [CrossRef]
4. Garcia, J.-C.; Montiel-Nelson, J.A.; Nooshabadi, S. High Performance CMOS Level up Conversion for Systems with Low-Voltage Power Supply. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, 26–29 May 2019; pp. 1–5.
5. Rodovalho, L.-H.; Rodrigues, C.-R.; Aiello, O. Self-Biased and Supply-Voltage Scalable Inverter-Based Operational Transconductance Amplifier with Improved Composite Transistors. *Electronics* **2021**, *10*, 935. [CrossRef]
6. Namdari, A.; Aiello, O.; Caviglia, D.-D. 0.5V 32nW Inverter-Based Gm-C Filter for Bio-Signal Processing. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Singapore, 19–22 May 2024; pp. 1–5. [CrossRef]
7. Rodovalho, L.-H.; Aiello, O. Inverter-Based Amplifier with Active Frequency Compensation and Adaptive Voltage Scaling. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Singapore, 19–22 May 2024; pp. 1–5. [CrossRef]
8. Lee, S.-Y.; Cheng, C.-J. Systematic Design and Modeling of an OTA-C Filter for Portable ECG Detection. *IEEE Trans. Biomed. Circuits Syst.* **2009**, *3*, 53–64. [CrossRef] [PubMed]
9. Chen, Z.; Law, M.-K.; Mak, P.-I.; Martins, R.P. A single-chip solar energy harvesting IC using integrated photodiodes for biomedical implant applications. *IEEE Trans. Biomed. Circuits Syst.* **2017**, *11*, 44–53. [CrossRef]
10. Roy, A.; Calhoun, B.H. A 71% efficient energy harvesting and power management unit for sub-μW power biomedical applications. In Proceedings of the IEEE Biomedical Circuits and Systems Conference (BioCAS), Turin, Italy, 19–21 October 2017; pp. 1–4.
11. Yi, H.; Yu, W.-H.; Mak, P.-I.; Yin, J.; Martins, R.P. A 0.18-V 382-μW Bluetooth low-energy receiver front-end with 1.33-nW sleep power for energy-harvesting applications in 28-nm CMOS. *IEEE J. Solid-State Circuits* **2018**, *53*, 1618–1627. [CrossRef]
12. Della Sala, R.; Centurelli, F.; Scotti, G.; Palumbo, G. Rail to Rail ICMR and High Performance ULV Standard-Cell-Based Comparator for Biomedical and IoT Applications. *IEEE Access* **2024**, *12*, 4642–4659. [CrossRef]
13. Boragno, C.; Aiello, O.; Caviglia, D.D. Monitoring the Air Quality in an HVAC System via an Energy Harvesting Device. *Sensors* **2023**, *23*, 6381. [CrossRef]
14. Sinha, A.K.; Radin, R.L.; Caviglia, D.D.; Montoro, C.G.; Schneider, M.C. An Energy Harvesting Chip designed to Extract Maximum Power from a TEG. In Proceedings of the IEEE Circuits & Systems Conference (LASCAS), Florianopolis, Brazil, 28 February–2 March 2016; pp. 1–4.
15. Della Sala, R.; Centurelli, F.; Monsurrò, P.; Scotti, G.; Trifiletti, A. A 0.3V Rail-to-Rail Three-Stage OTA With High DC Gain and Improved Robustness to PVT Variations. *IEEE Access* **2023**, *11*, 19635–19644. [CrossRef]
16. Toledo, P.; Aiello, O.; Crovetti, P.S. A 300mV-Supply Standard-Cell-Based OTA with Digital PWM Offset Calibration. In Proceedings of the 2019 IEEE Nordic Circuits and Systems Conference (NORCAS), Helsinki, Finland, 29–30 October 2019; pp. 1–5. [CrossRef]
17. Della Sala, R.; Centurelli, F.; Scotti, G.; Tommasino, P.; Trifiletti, A. A Differential-to-Single-Ended Converter Based on Enhanced Body-Driven Current Mirrors Targeting Ultra-Low-Voltage OTAs. *Electronics* **2022**, *11*, 3838. [CrossRef]
18. Ye, L.; Shi, C.; Liao, H.; Huang, R.; Wang, Y. Highly power-efficient active-RC filters with wide bandwidth-range using low-gain push-pull opamps. *IEEE Trans. Circuits Syst. I* **2013**, *60*, 95–107. [CrossRef]
19. Sun, C.-Y.; Lee, S.-Y. A Fifth-Order Butterworth OTA-C LPF with Multiple-Output Differential-Input OTA for ECG Applications. *IEEE Trans. Circuits Syst. II* **2018**, *65*, 421–425. [CrossRef]
20. Carrillo, J.M.; Cruz-Blas, C.A. 0.6-V 1.65-μW Second-Order Gm-C Bandpass Filter for Multi-Frequency Bioimpedance Analysis Based on a Bootstrapped Bulk-Driven Voltage Buffer. *J. Low Power Electron. Appl.* **2022**, *12*, 62. [CrossRef]

21. Sala, R.-D.; Monsurrò, P.; Scotti, G.; Trifiletti, A. Area-Efficient Low-Power Bandpass Gm-C Filter for Epileptic Seizure Detection in 130nm CMOS. In Proceedings of the IEEE Int. Electronics, Circuits and Systems Conference (ICECS), Genoa, Italy, 27–29 November 2019; pp. 1–4.
22. Della Sala, R.; Centurelli, F.; Scotti, G. A Novel High Performance Standard-Cell Based ULV OTA Exploiting an Improved Basic Amplifier. *IEEE Access* **2024**, *12*, 17513–17521. [CrossRef]
23. Ramesh, N.; Gaggatur, J.-S. A 0.6 V, 2nd order low-pass Gm-C filter using CMOS inverter-based tunable OTA with 1.114 GHz cut-off frequency in 90 nm CMOS technology. In Proceedings of the 2021 34th International Conference on VLSI Design and 2021 20th International Conference on Embedded Systems (VLSID), Guwahati, India, 20–24 February 2021; pp. 305–309.
24. Deng, J.; Fu, Z.; Wang, Z.; Chen, D.; Tang, X.; Guo, J. Improved Nauta Transconductor for Wideband Intermediate-Frequency gm-C Filter. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, MD, USA, 28–31 May 2017; pp. 1–4.
25. Kweon, S.-J.; Shin, S.-H.; Jo, S.-H.; Yoo, H.-J. Reconfigurable High-Order Moving-Average Filter Using Inverter-Based Variable Transconductance Amplifiers. *IEEE Trans. Circuits Syst. II* **2014**, *61*, 942–946. [CrossRef]
26. Jaikla, W.; Khateb, F.; Kulej, T.; Pitaksuttayaprot, K. Universal Filter Based on Compact CMOS Structure of VDDDA. *Sensors* **2021**, *21*, 1683. [CrossRef] [PubMed]
27. Kumngern, M.; Khateb, F.; Kulej, T.; Psychalions, C. Multiple-Input Universal Filter and Quadrature Oscillator Using Multiple-Input Operational Transconductance Amplifiers. *IEEE Access* **2021**, *9*, 56253–56263. [CrossRef]
28. Binkley, D.M. *Tradeoffs and Optimization in Analog CMOS Design*; John Wiley & Sons: Hoboken, NJ, USA, 2008. [CrossRef]
29. Chang, J.; Abidi, A.A.; Viswanathan, C.R. Flicker noise in CMOS transistors from subthreshold to strong inversion at various temperatures. *IEEE Trans. Electron Devices* **1994**, *41*, 1965–1971. [CrossRef]
30. Allogo, Y.A.; Marin, M.; de Murcia, M.; Llinares, P.; Cottin, D. 1/f noise in 0.18 μm technology n-MOSFETs from subthreshold to saturation. *Solid-State Electron.* **2002**, *46*, 977–983. [CrossRef]
31. Namdari, A.; Dolatshahi, M. Design of a low-voltage and low-power, reconfigurable universal OTA-C filter. *Analog. Integr. Circuits Signal Process.* **2022**, *111*, 169–188. [CrossRef]
32. Khateb, F.; Kumngern, M.; Kulej, T.; Biolek, D. 0.5 V Differential Difference Transconductance Amplifier and Its Application in Voltage-Mode Universal Filter. *IEEE Access* **2022**, *10*, 43209–43220. [CrossRef]
33. Khateb, F.; Kumngern, M.; Kulej, T. 0.5-V 281-nW Versatile Mixed-Mode Filter Using Multiple-Input/Output Differential Difference Transconductance Amplifiers. *Sensors* **2023**, *24*, 32. [CrossRef] [PubMed]
34. Kulej, T.; Kumngern, M.; Khateb, F.; Arbet, D. 0.5 V Versatile Voltage- and Transconductance-Mode Analog Filter Using Differential Difference Transconductance Amplifier. *Sensors* **2023**, *23*, 688. [CrossRef] [PubMed]
35. Khateb, F.; Kumngern, M.; Kulej, T. 58-nW 0.5-V mixed-mode universal filter using multiple-input multiple-output OTAs. *IEEE Access* **2023**, *11*, 130345–130357. [CrossRef]
36. Khateb, F.; Kumngern, M.; Kulej, T.; Akbari, M.; Stopjakova, V. 0.5 V, nW-Range Universal Filter Based on Multiple-Input Transconductor for Biosignals Processing. *Sensors* **2022**, *22*, 8619. [CrossRef]
37. Jaikla, W.; Khateb, F.; Kumngern, M.; Kulej, T.; Ranjan, R.-K.; Suwanjan, P. 0.5 V Fully Differential Universal Filter Based on Multiple Input OTAs. *IEEE Access* **2020**, *8*, 187832–187839. [CrossRef]

Journal of
Low Power Electronics and Applications

MDPI

Article

A 0.064 mm^2 16-Channel In-Pixel Neural Front End with Improved System Common-Mode Rejection Exploiting a Current-Mode Summing Approach

Giovanni Nicolini, Alessandro Fava , Francesco Centurelli and Giuseppe Scotti *

Dipartimento di Ingegneria dell'Informazione, Elettronica e Telecomunicazioni (DIET), Università di Roma La Sapienza, 00184 Roma, Italy; giovanni.nicolini@uniroma1.it (G.N.); alessandro.fava@uniroma1.it (A.F.); francesco.centurelli@uniroma1.it (F.C.)
* Correspondence: giuseppe.scotti@uniroma1.it

Abstract: In this work, we introduce the design of a 16-channel in-pixel neural analog front end that employs a current-based summing approach to establish a common-mode feedback loop. The primary aim of this novel structure is to enhance both the system common-mode rejection ratio (SCMRR) and the common-mode interference (CMI) range. Compared to more conventional designs, the proposed front end utilizes DC-coupled inverter-based main amplifiers, which significantly reduce the occupied on-chip area. Additionally, the current-based implementation of the CMFB loop obviates the need for voltage buffers, replacing them with simple common-gate transistors, which, in turn, decreases both area occupancy and power consumption. The proposed architecture is further examined from an analytical standpoint, providing a comprehensive evaluation through design equations of its performance in terms of gain, common-mode rejection, and noise power. A 50 μm × 65 μm compact layout of the pixel amplifiers that make up the recording channels of the front end was designed using a 180 nm CMOS process. Simulations conducted in Cadence Virtuoso reveal an SCMRR of 80.5 dB and a PSRR of 72.58 dB, with a differential gain of 44 dB and a bandwidth that fully encompasses the frequency range of the bio-signals that can be theoretically captured by the neural probe. The noise integrated in the range between 1 Hz and 7.5 kHz results in an input-referred noise (IRN) of 4.04 μV_{rms}. Power consumption is also tested, with a measured value of 3.77 μW per channel, corresponding to an overall consumption of about 60 μW. To test its robustness with respect to PVT and mismatch variations, the front end is evaluated through extensive parametric simulations and Monte Carlo simulations, revealing favorable results.

Keywords: front end; neural recording; system common-mode rejection ratio

1. Introduction

Understanding the intricate correlation between individual neuron activities is pivotal for advancing the development of numerous applications within the realm of neuroscience [1,2]. Among these, a notable area of research focuses on investigating the mechanisms underlying the effects of neurodegenerative diseases such as Parkinson's or Alzheimer's, in light of their increasing global spread and the corresponding rise in treatment costs [3–6]. Additionally, ongoing research endeavors center around the development of efficient brain–machine interfaces (BMIs) for diagnostic and neuro-prosthetic purposes [7–9].

However, to achieve breakthroughs in these and other areas of neuroscientific research, reliance solely on non-invasive methods of neural recording (i.e., EEG or fMRI) has proven to be insufficient. Although affordable and safe to perform, such techniques are hampered by limited spatial and temporal resolutions and exhibit a low signal-to-noise ratio (SNR) due to the filtering effect of the intermediate layers between the scalp and the source of the bio-signals [10,11]. Invasive neural recording through implantable neural probes,

on the other hand, allows for the isolation of spike events from single neurons with sub-millisecond time precision by recording the neuronal activity directly from the extracellular space of the membrane [12].

Multi-channel neural probes can be fabricated using a variety of techniques and materials. Most notably, silicon is widely favored on account of its cost-effectiveness, compatibility with standard fabrication processes, and the ability to integrate CMOS circuits on the same substrate [13,14]. Taking advantage of this aspect, recently introduced active neural probes have been a key factor in contributing to the gradual increase in the density of recording channels that can be implemented in a single probe's shank. In turn, the number of individual neurons that can be simultaneously recorded has also experienced a steady rise [15]. At the forefront of neural recording, devices such as Neuropixels 2.0, Neuroseeker, and SiNAPS have produced groundbreaking results when applied to small mammals and non-human primates [16–20].

Designing CMOS neural probes presents a multifaceted challenge, involving various disciplines such as electronics, material science, and biology [21–23]. While implanted micro-electrodes provide superior access to fine-grained neural activity, they inherently cover a smaller volume of brain tissue compared to standard non-invasive methods. Thus, future advancements must prioritize increasing the density and number of integrated recording sites to achieve large-scale brain coverage. Moreover, reducing the area occupied by neural probes can significantly decrease their invasiveness, which, in turn, decreases the risk of tissue damage during the probe's insertion and reduces the chances of inflammatory response under chronic recording conditions [24–26]. It is worth noting that down-scaling the technology to achieve a smaller area introduces short-channel effects of the MOS transistors, resulting in a reduction in transconductance and an increase in gate leakage current, flicker, and thermal noise power [27].

Furthermore, optimizing power consumption in neural recording devices, and thus managing potential heat generation through dissipation, is a critical parameter [28,29]. Recent studies have shown that power consumption exceeding 40 mW leads to a temperature increase of over 2 °C, which, in turn, triggers neural cell death within a few days [30].

Another important aspect to consider when designing neural probes is the ability of the circuit to effectively reject interferences, that is, the common-mode rejection ratio (CMRR) and the power supply rejection ratio (PSRR). To preserve the integrity of the acquired bio-signals and maintain a high SNR, both the common-mode signals, typically fed through the micro-electrodes, and the power supply noise, such as wall-mounted 50/60 Hz interference, should be rejected accordingly [31]. Although various methods have been employed to ensure a high CMRR for the amplifiers employed in multi-channel neural probes, few studies have centered on the system CMRR in analog front ends [32–34]. Typically, the system common-mode rejection ratio (SCMRR) in systems with a high channel count N decreases as N itself increases and is also dependent on the mismatch between the impedance of the reference electrode and the impedance of the signal-acquiring electrode.

In this regard, the novel approach introduced in [34] aims to raise the SCMRR and the common-mode interference (CMI) range of a DC-coupled neural recording front end through the implementation of a shared voltage-averaging circuit (VAC) and a floating-rail common-mode feedback loop (CMFB). The latter employs an error amplifier with an open-loop gain of 45 dB that accepts as input the mean of the voltage outputs of the multiple input amplifiers and, in turn, produces a feedback voltage, used to retroactively cancel out any common-mode interference.

Similarly, in this work, we introduce the architecture of a DC-coupled analog front end designed for high-channel-count in-pixel neural recording systems. The described structure features 15 recording channels alongside a single reference channel. It incorporates a CMFB loop, which operates on the sum of individual channel currents to enhance both the SCMRR and the CMI range. In addition, the proposed design focuses on minimizing the on-chip area footprint of the front end, aligning with the demand for compact and efficient neural recording devices set by the state of the art.

The remainder of this paper is organized as follows. Section 2 delves into the architecture of the front end, highlighting its innovative features. The topologies of the various components that make up the front end are presented in detail in Section 3, while Section 4 concerns the analytical aspects of the circuit's performance. The results obtained through simulations are subsequently presented in Section 5, along with a final table to compare the results with current state-of-the-art devices. The conclusions are drawn in Section 6.

2. System Architecture

In order to effectively contextualize the novel contributions brought forth by the analog front end proposed in this document, it is necessary to first provide a characterization of the fundamental workings of the circuit outlined in [34], thereby establishing a baseline for comparison. In this regard, the circuit depicted in Figure 1 comprises 16 recording channels, 15 of which serve as input channels, while the remaining one acts as a reference channel. For local conditioning of the acquired bio-signals, each front-end channel integrates an in-pixel low-noise neural amplifier with a bandwidth of 7.5 kHz, ensuring coverage of both the action potentials and local field potentials recorded in the extracellular space. In a conventional IC multi-channel recording system, the total common-mode rejection ratio is dependent on the intrinsic CMRR of the input amplifiers, as well as the number of employed channels, as demonstrated in [33]:

$$SCMRR = \left(\frac{1}{ICMRR} + \left(\frac{1 + 2\left(\left| \frac{Z_{IN}}{Z_E} \right| + N\epsilon \right)}{2(N\epsilon - 1)} \right)^{-1} \right)^{-1} \tag{1}$$

Here, Z_{IN} represents the input impedance of the low-noise amplifier, while Z_E denotes the impedance of the recording electrode. The term ϵ is used to quantify the difference in impedance between the reference electrode and the signal electrode, with a value of one indicating a condition of a perfect match. With the goal of improving the SCMRR and, therefore, increasing the CMI range in high-channel-count systems, the solution presented in [34] employs a common-mode feedback loop based on the average sum of the output voltages of the input amplifiers.

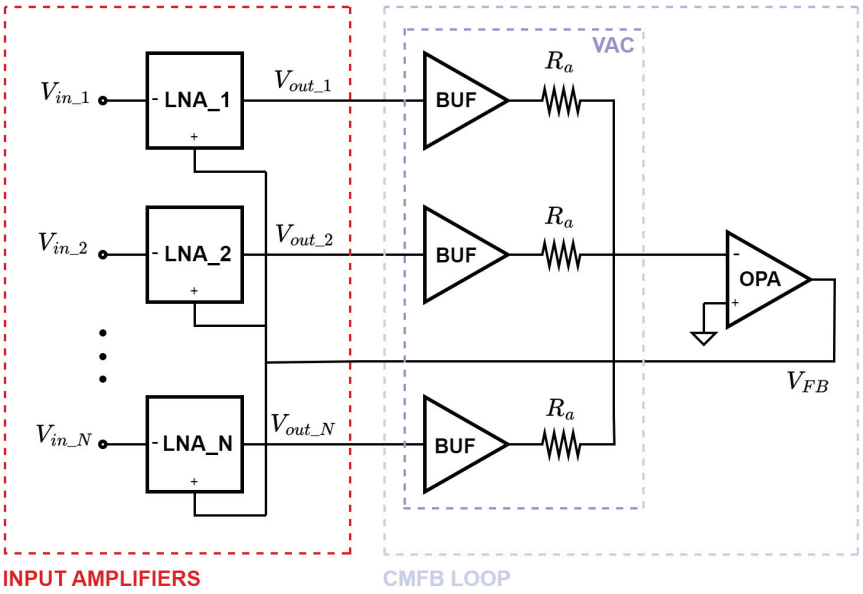


Figure 1. Block diagram of DC-coupled front end with voltage-based CMFB loop.

The CMFB consists of a voltage-averaging circuit and an error amplifier. In relation to the single recording channel, the former is composed of a voltage buffer, necessary to eliminate the loading effect to the main amplifier, and a resistor R_a. Assuming the same

value for all 16 resistors, the voltage fed to the inverting input of the error amplifier can be expressed as follows:

$$V_{in\_i} = \frac{\frac{V_{out\_1}}{R_a} + \frac{V_{out\_2}}{R_a} + \ldots + \frac{V_{out\_N}}{R_a}}{\frac{N}{R_a}} = \frac{1}{N}\sum_{i=1}^{N} V_{out,i}. \quad (2)$$

To complete the CMFB loop, the output of the error amplifier, denoted as V_{FB}, is fed back to the pixel amplifiers. As previously mentioned, the implementation of this kind of common-mode feedback loop enhances the SCMRR. However, it is important to acknowledge that including a voltage buffer for each recording channel results in a substantial increase in the on-chip area occupation, which is a critical aspect to consider in the context of neural recording devices.

To address this limitation, we devised a variation of the aforementioned front end, designed with the aim of significantly reducing its area occupation without compromising the system's performance. As depicted in the block diagram in Figure 2, this modified version of the front end maintains the same number of recording channels. Its distinctive feature lies in the operation mode of the CMFB loop: in place of the mean calculation of the output voltages, a sum of the output currents is conducted instead.

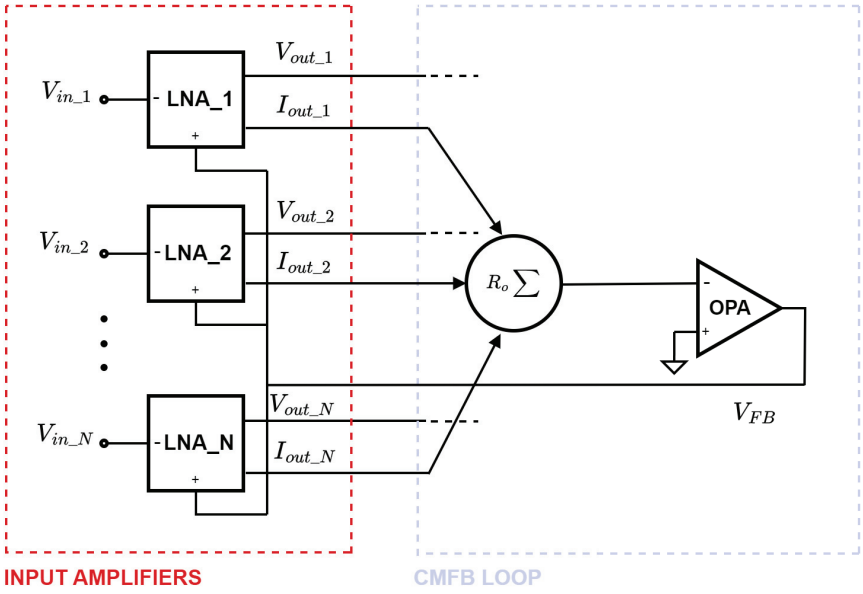


Figure 2. Block diagram of DC-coupled front end with current-based CMFB loop.

Summing the output signals as currents eliminates the need for voltage buffers and resistors, resulting in a significant reduction in the on-chip area occupation per recording channel. In particular, for each input amplifier, the voltage-averaging circuit is replaced with two much smaller transistors, while the current sum is made possible by implementing two common-gate transistors. In doing so, the voltage buffers and the resistors depicted in Figure 1 are no longer required. As a result, the on-chip area occupation is significantly reduced.

3. Circuit Design

The following section of the paper delves deeper into the topologies of the various stages that comprise the proposed multi-channel neural recording front end, providing insight into the mechanisms underlying the amplifying stage and the CMFB loop.

3.1. Pixel DC-Coupled Amplifiers

The schematic of the primary low-noise amplifier utilized in each recording channel is depicted in Figure 3. Following the topology proposed in [34], transistors *M*1 and *M*2

form the DC-coupled inverter-based amplifier of the system. In contrast to commonly used configurations employing differential amplifiers, the utilization of single-ended amplifiers offers notable benefits, such as reduced area occupancy and power dissipation, albeit at the cost of a decreased system rejection to interfering common-mode signals and power supply variations.

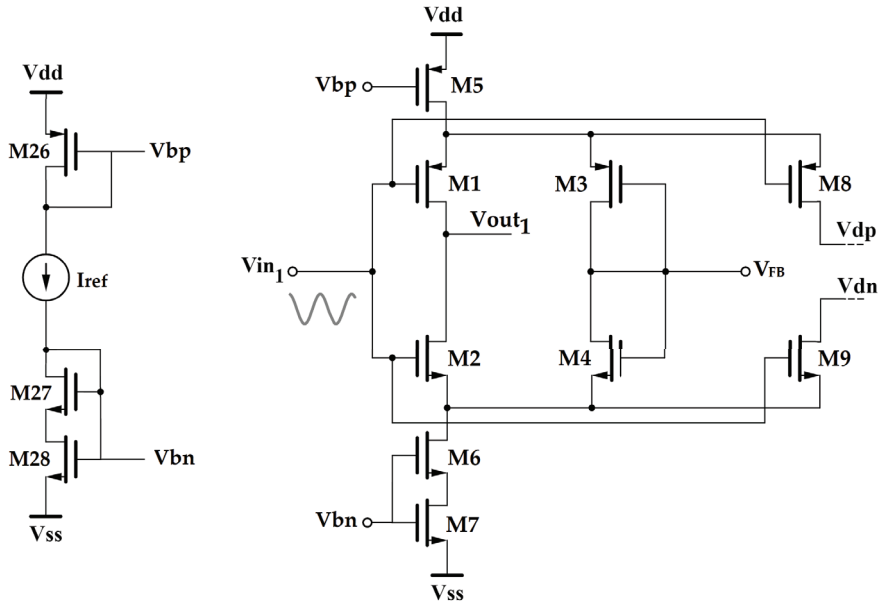


Figure 3. Schematic of the input pixel amplifier employed in the multi-channel analog front end.

For the *i*-th channel, the output current produced by the main inverter-based amplifier is duplicated by utilizing the replicating transistors *M*8 and *M*9, which share the same source and gate nodes as the transistors comprising the inverter itself. The magnitude of the duplicated current is determined by the transconductance of *M*8 and *M*9. As such, by adjusting the aspect ratios of *M*8 and *M*9 to a fraction of the ratios of transistors *M*1 and *M*2, it is possible to replicate a scaled current with precision. This is done to ensure a more efficient occupation of the on-chip area and a reduction in power consumption.

With reference to the schematic in Figure 3, transistors *M*3 and *M*4 provide a way to set the voltages of the floating rails of the input pixel amplifier. Acting as the terminal of the CMFB loop of the system, these transistors are diode-connected to avoid strong variations in the output high-impedance node, which would otherwise require Miller compensation. Additionally, the pairs *M*3–*M*4 and *M*1–*M*2 must be sized equally in order to effectively reject common-mode interference and also to prevent an increase in the IRN caused by the eventual mismatch.

Biasing of the amplifier is achieved through the voltages V_{bp} and V_{bn} applied to the gates of transistors *M*5 and *M*6–*M*7, which, respectively, act as a current source and a current sink for the inverter. Concerning the pair *M*6–*M*7 in particular, connecting the gate nodes and the body nodes of the two transistors allows us to virtually obtain a transistor with a channel length capable of exceeding the upper limit set by the specific adopted technology [35].

3.2. Common-Mode Feedback Stage

The topology of the CMFB stage in the front end is structured around two common-gate transistors, namely *M*11 and *M*12, which are used to establish a low-impedance node for summing the scaled duplicated currents. Referring to the schematic presented in Figure 4, node A serves as the summing node for the currents duplicated by the 16 NMOS replicating transistors, while node B provides the same function for the currents duplicated by the PMOS replicating transistors connected to the main amplifiers.

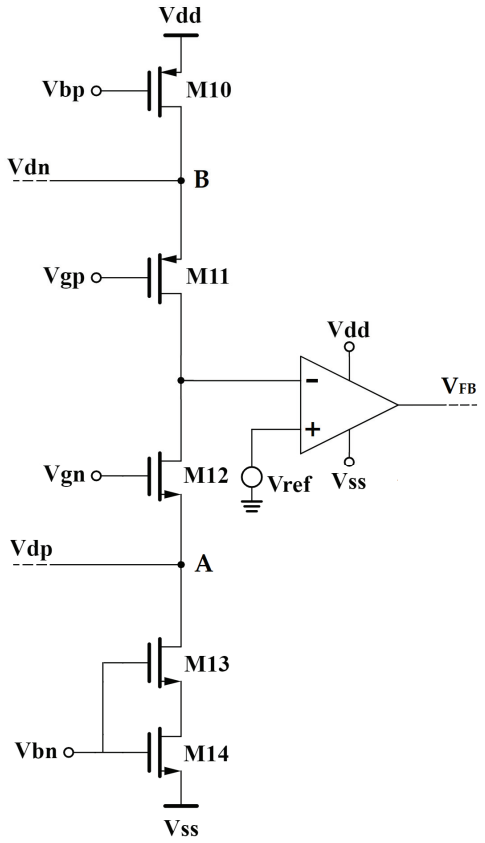


Figure 4. Schematic of the current-summing stage of the CMFB loop.

Transistors *M*11 and *M*12 effectively form two folded cascode structures, with the total scaled output current being converted into the input voltage of the error amplifier through the output resistance at their shared drain node. This voltage is subsequently amplified and fed back to the gate of the feedback amplifiers introduced in Section 3.1.

In terms of biasing, transistors *M*10 and *M*13–*M*14 act as current sources and are employed to set the bias current for the branch of the CMFB stage. It must be noted that the pair *M*13–*M*14 is designed following the same principle as the pair *M*6–*M*7 that makes up one of the two current generators used to bias the inverter-based amplifier.

3.3. Error Amplifier

The topology of the error amplifier utilized to implement the CMFB loop is illustrated in Figure 5. Designed to operate in weak inversion mode, the amplifier comprises three stages; transistors *M*15, *M*16, *M*17, *M*18, *M*19, and *M*20 form a differential active-load amplifying stage, with the signal coming from the inverting input. Note that a reference voltage is applied to the non-inverting input instead. Transistors *M*19 and *M*20 ensure the correct biasing of the stage and are driven by a voltage V_{bn} applied to the shared gate node.

The second stage of the amplifier is made up of a common-source transistor, *M*21, biased through the composite transistors *M*22–*M*23. A compensation feedback capacitor C_C is connected between the drain and the gate of *M*21 to ensure the stability of the amplifier, as well as to provide a sufficient gain bandwidth product according to the following formula [36]:

$$C_C = \frac{g_{m1}}{2\pi \cdot GBW}. \tag{3}$$

The final class AB stage implemented through *M*24–*M*25 guarantees a rail-to-rail output swing, which, in turn, allows for the overall front end to achieve a high CMI value.

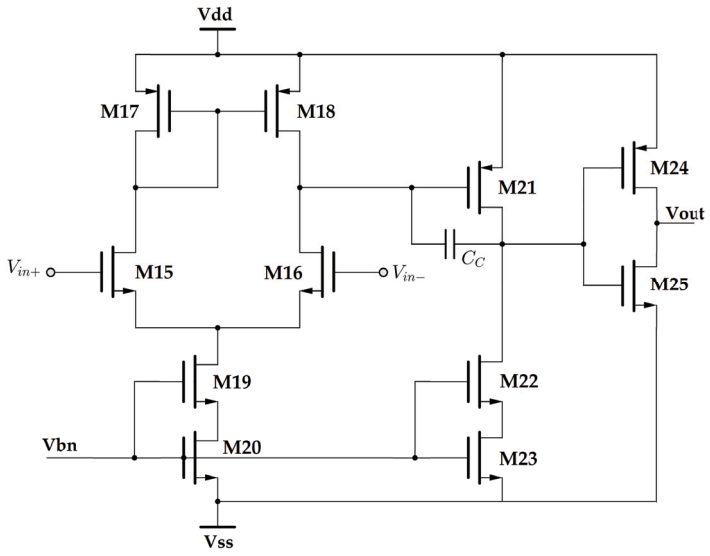


Figure 5. Schematic of error amplifier.

4. Circuit Analysis

The following section aims to provide an analytical overview of the circuit's small-signal performance. The proposed design equations mainly focus on parameters such as the differential gain, common-mode gain, and SCMRR. Additionally, the circuit's noise performance is evaluated.

4.1. Gain and SCMRR

Despite being classified as a single-ended amplifier, the pixel amplifier effectively operates with an inverting input for the acquired signal and a non-inverting input for the feedback voltage due to the diode-connected pair of transistors that closes the CMFB loop. For the *k*-th recording channel, the gain of the former is A_L, while the gain of the latter is defined as A_R. Therefore, the output voltage of the amplifier can be expressed as

$$V_o = -A_L V_i + A_R V_{FB} \simeq -A_1 (V_i - V_{FB}), \tag{4}$$

where A_R and A_L are assumed to be approximately equal to each other. Referring to the small-signal model of the pixel amplifier (Figure 6), the gain A_1 can be computed as

$$A_1 \simeq A_0 \frac{g_{mF}}{g_{mF} + g_{mR}} \frac{1 + s/\omega_{TF}}{1 + s/\omega_1}, \tag{5}$$

where A_0 corresponds to

$$A_0 = \frac{g_m}{g_0}, \tag{6}$$

and ω_{TF} and ω_1 are defined as

$$\omega_{TF} = \frac{g_{mF}}{C_{gsF}}; \tag{7}$$

$$\omega_1 = \frac{g_{mR} + g_{mF}}{C_{gs} + C_{gsR} + C_{gsF}} < \omega_{TF}. \tag{8}$$

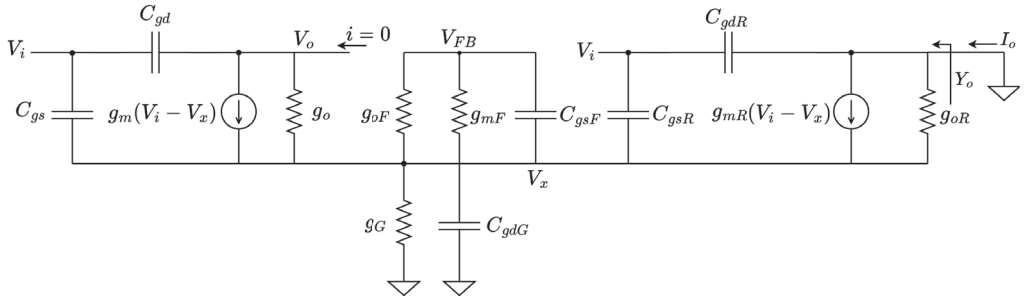


Figure 6. Small-signal model of the *k*-th pixel amplifier stage of the front end.

It is important to note that the expressions presented here are based on several approximations. Firstly, to simplify the calculations, the parameters of the NMOS and PMOS transistors are assumed to be identical to each other. As such, the small-signal parameters g_* and C_* are equivalent to $g_{*n} + g_{*p}$ and $C_{*n} + C_{*p}$, respectively. Furthermore, the computation of V_o assumes the output of the system to be an open circuit, while the capacitance C_{gd} has been disregarded in the node equations of the first stage. By applying Norton's theorem, the output current of the equivalent circuit is found to be equal to

$$I_o \simeq -\frac{g_{mR}}{A_0} V_o, \tag{9}$$

with the equivalent Norton's admittance being denoted as

$$Y_o = \frac{g_{mF}}{g_{mF} + g_{oR}} g_{oR} \frac{1 + s/\omega_2}{1 + s/\omega_1}, \tag{10}$$

where

$$\omega_2 = \frac{g_{mF}}{C_{gs} + C_{gsF} + C_{gsR}} \tag{11}$$

is smaller than ω_1. The small-signal model of the current summing stage of the circuit is presented in Figure 7. The output voltage V_{o2} can be derived as

$$V_{o2} = -A_2(V_{ic} - V_{FB}) \tag{12}$$

with $V_{ic} = (1/N)\sum_{j=1}^{N} V_i$.

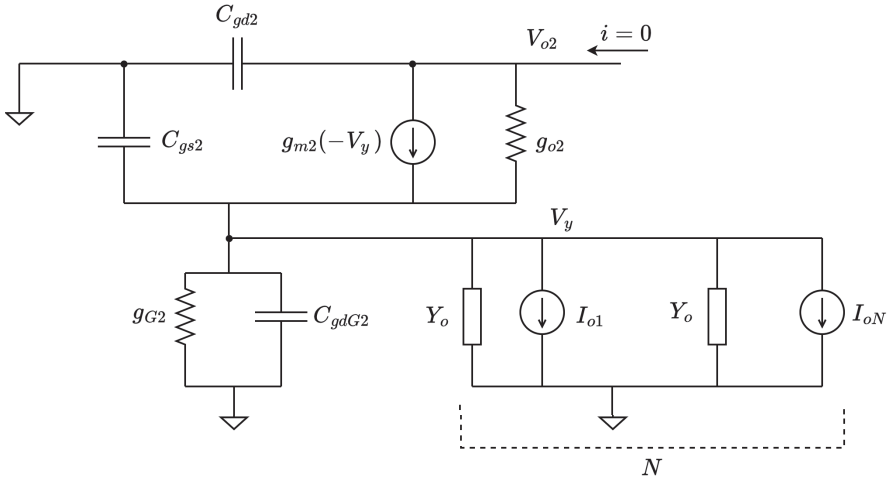


Figure 7. Small-signal model of the CMFB stage of the front end.

The gain A_2 is computed as follows:

$$A_2 = \frac{g_{m2} + g_{o2}}{g_{o2}} \frac{g_{mR} g_{mF} (1 + s/\omega_{TF})}{d_0 + d_1 s + d_2 s^2} N. \tag{13}$$

In this case, N indicates the number of recording channels that make up the front end. Coefficients d_0, d_1, and d_2 can be expressed as (see Appendix A):

$$\begin{gathered} d_0 = N g_{mF} g_{oR} + g_{mF} g_{G2} + g_{mR} g_{G2} \\ d_1 = N(C_{gsF} + C_{gs} + C_{gsR}) g_{oR} + g_{G2}(C_{gsF} + C_{gs} + C_{gsR}) + C_{gs2}(g_{mF} + g_{mR}) \\ d_2 = C_{gs2}(C_{gs} + C_{gsR} + C_{gsF}) \end{gathered} \tag{14}$$

Voltage V_{o2} is subsequently fed to the inverting input of the error amplifier. We may assume $V_{REF} = 0$ for the small-signal analysis. The resulting feedback voltage is equal to

$$V_{FB} = -A_E V_{o2}. \tag{15}$$

The single-pole error amplifier is characterized by a gain A_E that can be denoted by the following expression:

$$A_E = \frac{A_{E0}}{1 + s\tau_E}. \tag{16}$$

By replacing V_{o2} in (15) with the expression defined in (12), the feedback voltage can be rewritten as

$$V_{FB} = \frac{A_2 A_E}{1 + A_2 A_E} V_{ic} = \frac{LG}{1 + LG} V_{ic}.$$

Particularly, the loop gain $LG = A_2 A_E$ is equivalent to

$$LG = \frac{g_{m2} + g_{o2}}{g_{o2}} \frac{g_{mR}}{g_{oR}} \frac{(1 + s/\omega_{TF})}{1 + \frac{d_1}{d_0} s + \frac{d_2}{d_0} s^2} \frac{A_{E0}}{1 + s\tau_E} \tag{17}$$

Under the hypothesis that the pole $1/\tau_E$ is dominant and that $1/\tau_E << \omega_{TF}$, the expression for the loop gain can be further simplified. As a result, LG can be expressed as

$$LG \simeq \frac{A_{E0}}{1 + s\tau_E} A_{02} A_{0R}, \tag{18}$$

where $A_{02} = g_{m2}/g_{o2}$ and $A_{0R} = g_{mR}/g_{oR}$. Considering an input voltage $V_i = V_{ic} + \hat{V}_i$, the output voltage, as defined in (4), becomes

$$V_o = -A_1 \left(V_{ic} + \hat{V}_i - \frac{LG}{1 + LG} V_{ic} \right) = -A_1 \left(\hat{V}_i + \frac{V_{ic}}{1 + LG} \right). \tag{19}$$

By setting $\hat{V}_i = 0$, the common-mode gain of the system can be evaluated accordingly. From (19), it is found that A_{cm} can be computed as

$$A_{cm} = \left. \frac{V_o}{V_{ic}} \right|_{\hat{V}_i = 0} = -\frac{A_1}{1 + LG}. \tag{20}$$

It is evident from Equation (20) that the common-mode gain presents a zero in $1/\tau_E$, which is set by the error amplifier employed in the CMFB loop. In order to compute the SCMRR of the front end, the expression for the single-channel gain must be derived as well. By imposing $V_{ic} = 0$ in (4), we obtain the following:

$$A_{ch} = \left. \frac{V_o}{\hat{V}_i} \right|_{V_{ic} = 0} = -A_1. \tag{21}$$

Therefore, the $SCMRR$ can be derived from (20) and (21) as

$$SCMRR = A_{ch}/A_{cm} = 1 + LG. \tag{22}$$

According to (22), the SCMRR's behavior in frequency is dependent on the error amplifier, with a pole in $1/\tau_E$.

4.2. Noise Analysis

For the purpose of noise analysis, each transistor has been modeled by a single noise current source that encompasses both thermal and flicker noise. With reference to the model presented in Figure 8, $g_F = g_{mF} + g_{oF} \simeq g_{mF}$. Concerning the CMFB stage of the front end, the noise current generator I_y represents the noise of g_{G2}, as well as the noise of the other channels.

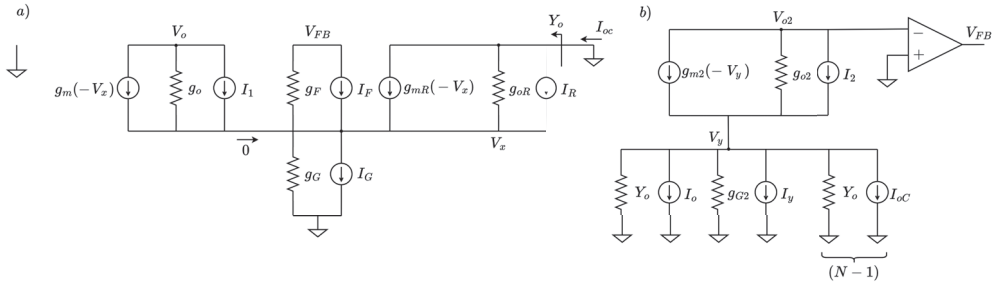


Figure 8. (**a**) Noise model of the first stage. (**b**) Noise model of the current-summing stage.

The equilibrium equation at V_x results in

$$G_D V_x = g_F V_{FB} + g_{oR} V_y + I_F - I_G + I_R, \tag{23}$$

with $G_D = g_F + g_{mR} + g_{oR} + g_G \simeq g_{mF} + g_{mR}$. Hence, the output admittance Y_o and the output current I_o can be expressed as

$$Y_o \simeq g_{oR} \frac{g_F}{G_D}; \tag{24}$$

$$I_o = I_{onoise} + I_{oc}. \tag{25}$$

Regarding the expression in (25), the output current's terms are defined as follows:

$$I_{onoise} = \frac{g_F I_R - g_{mR}(I_F - I_G)}{G_D}; \tag{26}$$

$$I_{oc} = -G_C V_{FB}, \tag{27}$$

where $G_C \simeq \frac{g_{mR} g_F}{G_D}$. Noise sources make it so that $V_y \neq 0$, which, in turn, causes $V_{FB} \neq 0$. This affects the channel under consideration and the other recording channels, whose I_{oc} affects V_y. The analysis of the second stage provides

$$V_{o2} \simeq A_{02} V_y - \frac{I_2}{g_{o2}}. \tag{28}$$

Considering that $V_{FB} = -A_E V_{o2}$ and, therefore, $I_{oc} = G_C A_E V_{FB}$, voltage V_y can be derived as

$$V_y \simeq \frac{I_2}{g_{m2}} - \frac{I_y + I_{onoise}}{N A_E A_{02} G_C}, \tag{29}$$

where $I_y = I_{G2} + (N-1)I_{onoise}$. By substituting V_y in Equation (23) and considering $V_o = A_o V_x - I_1/g_o$, the output noise voltage is computed as

$$V_{onoise} \simeq \frac{A_o}{G_D}\left[-\frac{G_D}{g_m}I_1 + \frac{N-1}{N}(I_F - I_G) + \left(1 + \frac{g_F}{Ng_{mR}}\right)I_R + \frac{g_{oR}}{g_{m2}}I_2 + \frac{G_D}{Ng_{mR}}I_y\right]. \quad (30)$$

The input noise can be calculated by dividing the expression in (30) by the gain A_1, as defined in (5), as follows:

$$V_{inoise} \simeq \frac{1}{g_F}\left[-\frac{G_D}{g_m}I_1 + \frac{N-1}{N}(I_F - I_G) + \left(1 + \frac{g_F}{Ng_{mR}}\right)I_R + \frac{g_{oR}}{g_{m2}}I_2 + \frac{G_D}{Ng_{mR}}I_y\right], \quad (31)$$

By looking at Equation (31), it is apparent that the contribution of I_2 to the IRN is negligible, as its coefficient is much lower than one. Additionally, it can be noticed that I_F, I_G, and I_R contribute to the overall input noise due to the presence of the CMFB loop. Other recording channels affect V_{inoise} through the term I_y.

5. Simulation Results

The proposed analog front end was designed and simulated following the 180 nm CMOS process from TSMC. This section delves into the layout design aspects of the DC-coupled pixel input amplifiers and provides sizing information concerning the various components. Additionally, it showcases the results obtained through extensive simulations.

5.1. Layout and Transistor Sizing

The layout of the analog front end is depicted in Figure 9, showing the 16-pixel amplifiers, each with an area footprint of 50 µm × 65 µm, placed along two rows. Utilizing six metal layers, this compact layout encompasses all the transistors described in detail in Section 3. Notably, the smaller transistors (*M*8–*M*9 in Figure 3), responsible for replicating the scaled currents, are surrounded by the transistors of the main inverter and the feedback transistors to mitigate potential mismatch between the devices. Overall, the area occupation per channel is lower than 0.004 mm^2.

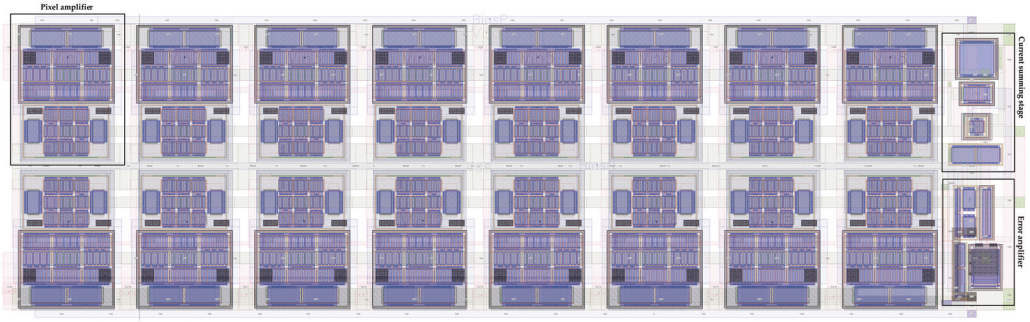


Figure 9. Layout of the 16-channel neural front end.

With reference to Figures 3 and 4, Table 1 summarizes the size parameters of the MOS transistors used in both the pixel amplifier and the CMFB stage that make up the closed loop. As stated previously, the transistors that make up the inverter and the feedback transistors are sized equally by design. In order to accurately scale the currents of the main amplifiers, feedback transistors *M*8 and *M*9 are sized with a width scaled by a factor of 4. Transistors *M*5 and *M*6–*M*7 are sized with the intent of producing a bias current of 2.5 µA for the main amplifying branch. Regarding the common-gate transistors implemented in the current-summing branch of the front end, the sizes are chosen to be equal to the replicating transistors to minimize area occupation. For biasing purposes, the *W* and *L* parameters of transistors *M*10 and *M*13–*M*14 are chosen to generate a current at least equal to the sum of the scaled, replicated currents.

Table 1. Transistor sizes for the pixel amplifier and the CMFB stage.

MOSFET	Width	Length
*M*1–*M*3	175 µm	1 µm
*M*2–*M*4	40 µm	1 µm
*M*8–*M*11	43.75 µm	1 µm
*M*9–*M*12	20 µm	1 µm
*M*5	12.70 µm	15 µm
*M*6–*M*7	5 µm	10 µm
*M*10	15 µm	14.1 µm
*M*13–*M*14	10 µm	6.91 µm

Table 2 displays the sizing choices made with respect to the error amplifier. In this case, the parameters of the transistors are set with the aim of obtaining a high open-loop gain for the amplifier of at least 80 dB, with a phase margin of 60°.

Table 2. Transistor sizes for the error amplifier.

MOSFET	Width	Length
*M*15–*M*16	8 µm	5 µm
*M*17–*M*18	20 µm	1 µm
*M*19–*M*20	1 µm	10 µm
*M*21	150 µm	500 nm
*M*22–*M*23	3 µm	10 µm
*M*24	10 µm	180 nm
*M*25	3 µm	180 nm

5.2. Circuit Simulations

The proposed front end's nominal behavior was simulated within the Cadence Virtuoso environment. To achieve results that closely resemble the actual implementation of the neural recording system, simulations were conducted using the post-layout netlist with extracted parasitics. The circuit was biased with a dual voltage supply ($Vdd = -Vss = 0.5$ V), while the total current used to bias a single channel was set at 3.5 µA.

Figure 10 shows that the inverter-based pixel amplifiers integrated into each recording channel boasted a differential gain of 44.16 dB, alongside a high cutoff frequency exceeding 100 kHz. These metrics highlight the amplifiers' ability to capture and amplify neural signals across the entire frequency spectrum, encompassing both local field potentials and action potentials as measured from the extracellular space.

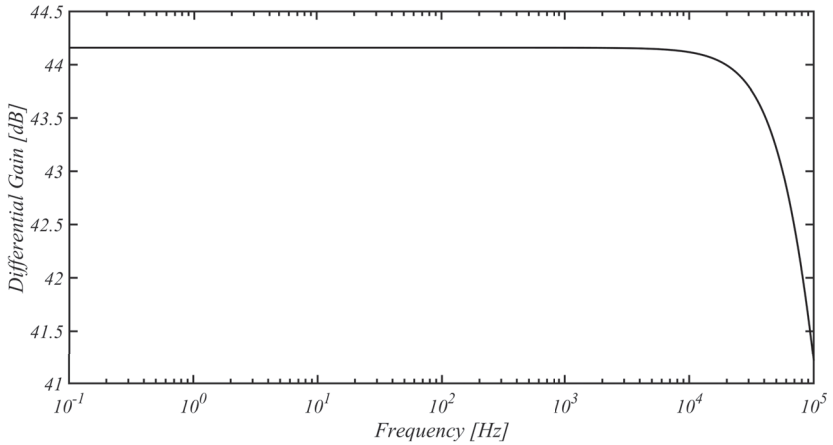


Figure 10. Differential gain of the main amplifier within the proposed front end.

As shown in Figure 11, further simulations revealed a favorable SCMRR of 80.5 dB at low frequencies. Particularly noteworthy was the performance of the front end within the range between 0.1 Hz and 100 Hz, where the SCMRR maintained a value of at least 80 dB. A moderately high level of rejection was maintained at higher frequencies, with the SCMRR exceeding 60 dB up to a frequency of 2 kHz.

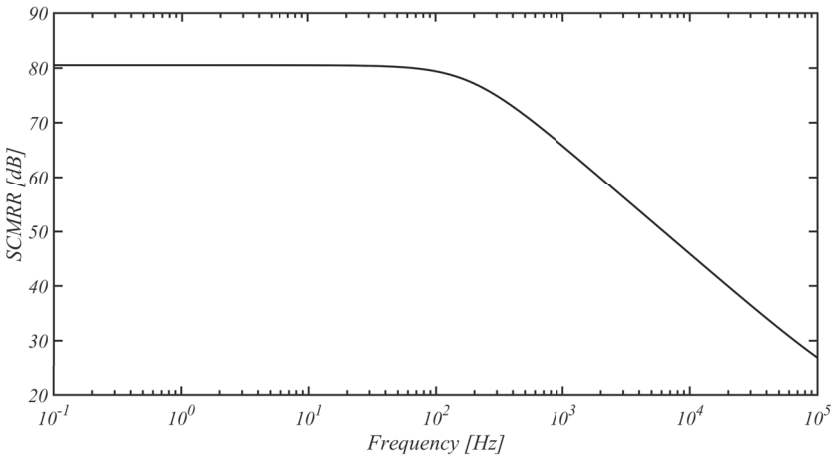


Figure 11. *SCMRR* of the proposed front end.

The PSRR of the front end, as indicated in Figure 12, exhibited a value of 72.55 dB at frequencies in the range spanning from 0.1 Hz to 100 Hz. For higher frequencies, the measured PSRR exhibited a similar behavior to the SCMRR, maintaining a level above 60 dB up until 2 kHz.

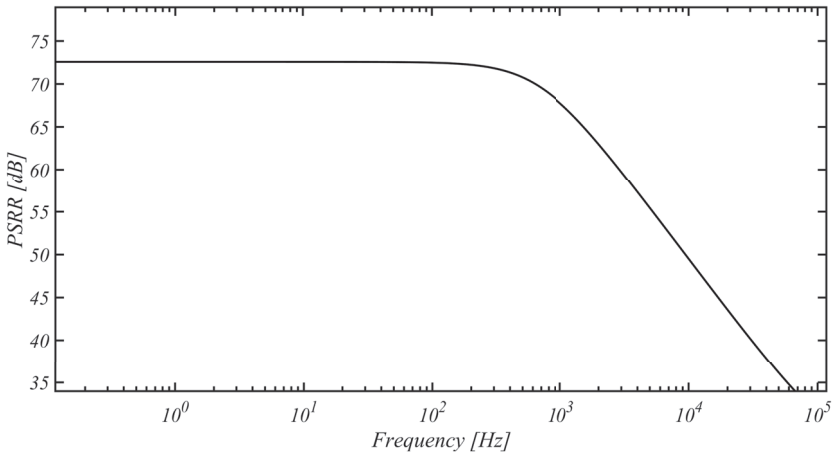


Figure 12. PSRR of the proposed front end.

The input-referred noise spectrum of the input amplifier is presented in Figure 13, showing a noise level of 100 nV/$\sqrt{\text{Hz}}$ at 100 Hz and a value of 50 nV/$\sqrt{\text{Hz}}$ at 1 kHz. By integrating the noise spectrum across various frequency intervals, the noise performance of the amplifier was evaluated in terms of the IRN. Specifically, the considered frequency bands are those associated with the LFP signals (1 Hz–300 Hz), the action potentials (300 Hz–7.5 kHz), and the overall spectrum that characterizes the bio-signals recorded from the extracellular space (1 Hz–7.5 kHz). The resulting measurements, acquired by varying the number of channels, are reported in Table 3.

As seen in the results reported in Table 3, the IRN exhibited an increasing trend as the number of recording channels decreased. This is consistent with Equation (31), highlighting the significance of the contribution of I_R, the noise source associated with the smaller replicating transistors, which became negligible when using at least eight channels.

Table 3. IRN values measured in different frequency intervals.

N° of Ch.	IRN_{LFP} (μV_{rms})	IRN_{AP} (μV_{rms})	IRN_{TOT} (μV_{rms})
2	6.44	8.72	10.83
4	3.57	4.90	6.059
8	2.71	3.77	4.64
16	2.36	3.30	4.04

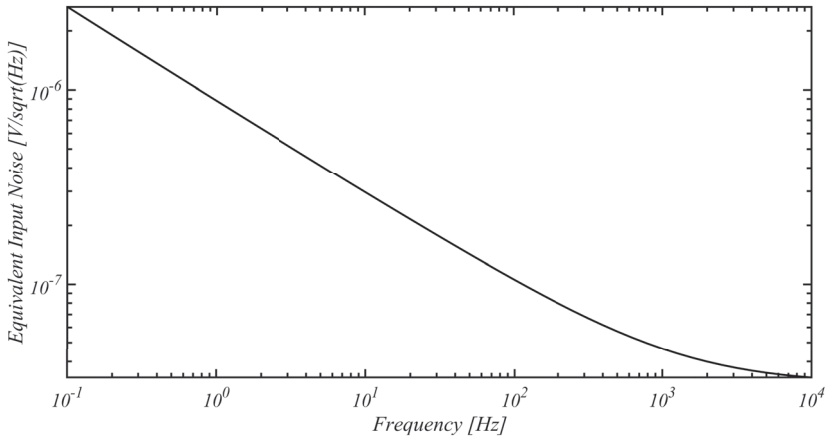


Figure 13. Equivalent input noise of the *i*-th recording channel.

A widely used figure of merit that allows us to relate the noise performance of the circuit with its power consumption and bandwidth is the noise efficiency factor (NEF) [37], expressed as follows:

$$NEF = IRN \cdot \sqrt{\frac{2 \cdot I_{TOT}}{\pi \cdot V_T \cdot 4k_bT \cdot BW}}, \tag{32}$$

where V_T is the thermal voltage, I_{TOT} is the total supply current of the amplifier, and BW is the amplifier's bandwidth in Hz. By substituting the values of the total current required to bias the individual recording channel, the IRN, and the bandwidth into (32), we obtain

$$NEF = 3.32.$$

In addition, the power efficiency factor (PEF) can be computed as

$$PEF = NEF^2 \cdot (Vdd - Vss) = 11.02. \tag{33}$$

5.3. Process and Mismatch Simulations

To assess the robustness of the front end against PVT (Process, Voltage, and Temperature) and mismatch variations, the system underwent comprehensive testing via multiple simulations. Specifically, a Monte Carlo simulation comprising 200 iterations was conducted. The outcomes of these simulations are outlined in Table 4.

Table 4. Performance under mismatch variations.

Parameter	Min	Max	Mean	Std. Dev.
G_D (dB)	44.05	44.24	44.16	0.04
G_{CM} (dB)	−41.06	−34.00	−36.38	1.42
$SCMRR$ (dB)	78.07	85.33	80.53	1.45
$PSRR$ (dB)	64.89	94.52	74.11	6.27
V_{out_DC} (mV)	−24.52	30.54	1.99	11.38

It must be noted that both the differential gain and the common-mode gain of the front end demonstrated standard deviations within a 2 dB interval, consequently maintain-

ing a similarly constrained SCMRR. Particularly, the differential gain exhibited minimal fluctuations around its mean value of 44.16 dB. Although the PSRR (power supply rejection ratio) variance was marginally higher, it remained moderately limited, with a mean of 74.11 dB and a variance of 6.30 dB. In both instances, the tested performance metrics yielded favorable results, with both figures of merits exceeding 70 dB on average.

Concerning the SCMRR and PSRR, histograms related to the distribution of results over the 200 Monte Carlo iterations are presented in Figures 14 and 15.

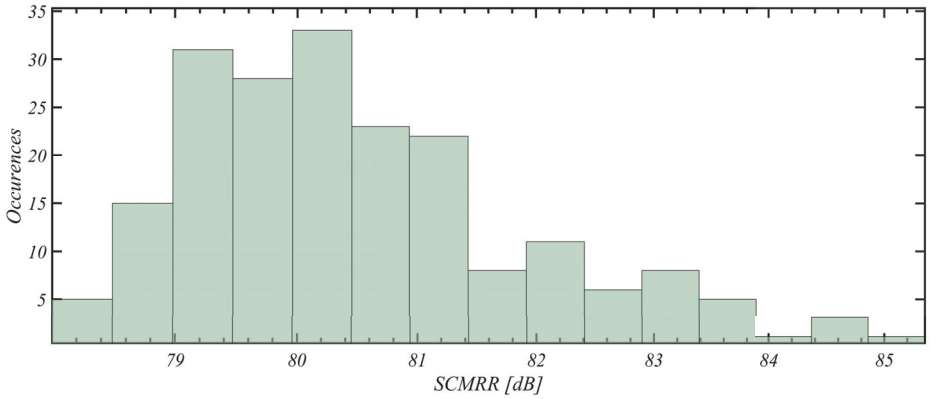


Figure 14. Histogram of the SCMRR of the proposed front end for 200 Monte Carlo mismatch iterations.

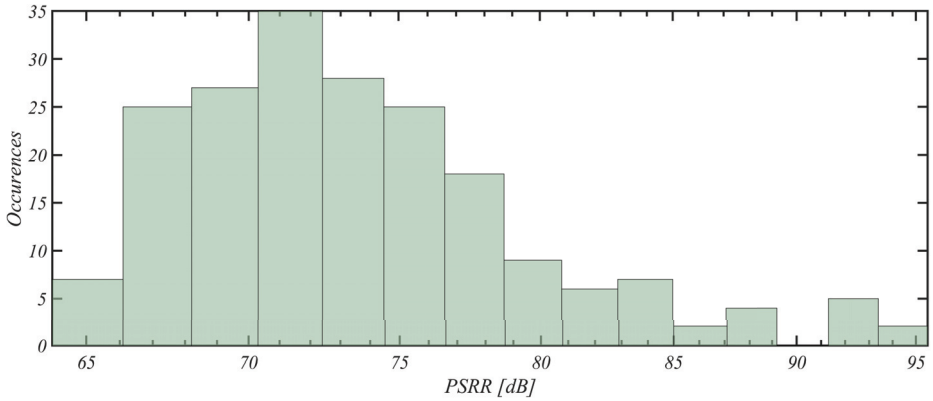


Figure 15. Histogram of the PSMRR of the proposed front end for 200 Monte Carlo mismatch iterations.

To further test the robustness of the proposed front end, a parametric simulation focusing on temperature variations was conducted. By gradually varying the operating temperature within the range [0 °C–50 °C], the front end's gain and noise parameters, along with the rejection parameters, were evaluated accordingly (Table 5).

Table 5. Performance under temperature variations.

Temp. (°C)	0.00	10.50	21.00	31.60	42.10	50.00
G_D (dB)	44.64	44.45	44.30	44.07	43.38	43.73
G_{CM} (dB)	−29.89	−32.20	−34.60	−37.33	−40.37	−43.99
$SCMRR$ (dB)	74.53	76.65	78.90	81.40	84.25	86.72
$PSRR$ (dB)	90.46	79.17	74.37	71.28	68.92	67.42
V_{out_DC} (mV)	1.64	1.86	1.95	1.95	1.90	1.84
IRN_{LFP} (μV_{rms})	2.27	2.30	2.34	2.38	2.41	2.44
IRN_{AP} (μV_{rms})	3.14	3.20	3.27	3.33	3.40	3.45
IRN_{TOT} (μV_{rms})	3.87	3.95	4.02	4.10	4.17	4.23

Regarding the differential gain of the input amplifiers, minimal fluctuations were observed; however, the common-mode gain of the system exhibited a gradual decrease

in value as the test temperature rose. Consequently, the SCMRR displayed an increasing trend with rising temperatures, reaching a maximum value of 86.72 dB at 50 °C. Conversely, the PSRR of the system tended to decrease in value with rising temperatures. In the range corresponding to the physiological conditions of the brain [38 °C–41 °C], both the PSRR and SCMRR were characterized by relatively minor variations, maintaining values of around 70 dB and 80 dB, respectively. When examining the noise performance of the front end amidst temperature variations, it was expected that the IRN of the system would experience a gradual rise. Nevertheless, at 4.23 μV_{rms}, considering the total bandwidth [1 Hz–7.5 kHz], IRN_{TOT} barely exceeded its nominal value measured at 27 °C.

Continuing with the evaluation of the front end, the following batch of simulations was conducted by varying the power supply voltage ±10% of its nominal value. By consulting the results displayed in Table 6, it can be seen that variations in the differential gain were once again minimal. In a similar manner, the common-mode gain of the system varied between a minimum of -39.21 dB for $(Vdd - Vss)$ = 1.1 V and a maximum of -32.36 for $(Vdd - Vss)$ = 0.9 V. Integrating the input noise spectrum across the bandwidths of interest revealed a minor increasing trend in the band related to the local field potentials [1 Hz–300 Hz] and a minor decreasing trend in the band related to the action potentials [300 Hz–7.5 kHz]. Overall, the IRN measured across the total frequency band exhibited a negligible decrease.

Table 6. Performance under supply voltage variations.

$Vdd - Vss$ (V)	0.90	0.94	0.97	1.02	1.07	1.10
G_D (dB)	44.18	44.17	44.16	44.15	44.15	44.15
G_{CM} (dB)	−32.36	−33.93	−35.54	−37.03	−38.34	−39.21
$SCMRR$ (dB)	76.54	78.10	79.70	81.18	82.49	83.36
$PSRR$ (dB)	59.78	65.66	70.81	74.96	77.80	79.01
V_{out_DC} (mV)	1.25	0.99	1.65	2.63	3.66	4.39
IRN_{LFP} (μV_{rms})	2.32	2.34	2.36	2.37	2.39	2.41
IRN_{AP} (μV_{rms})	3.45	3.38	3.32	3.28	3.25	3.23
IRN_{TOT} (μV_{rms})	4.16	4.11	4.07	4.05	4.03	4.03

To conclude with the PVT analysis, the results of the simulations under corner variations are compiled in Table 7. Generally, it can be observed that the front end's robustness is quite favorable.

Table 7. Performance under process variations.

Temp. (°C)	TT	FF	SS	SF	FS
G_D (dB)	44.16	43.59	44.73	44.09	44.17
G_{CM} (dB)	−36.04	−40.47	−32.38	−35.56	−24.97
$SCMRR$ (dB)	80.20	84.06	77.11	79.65	69.14
$PSRR$ (dB)	72.55	72.38	71.58	68.75	91.49

Table 8 shows a comparison between the front end proposed in this work and various analog front ends introduced in recent years. In terms of noise, SCMRR, PSRR, and power consumption per channel (P/Ch), the simulation results presented in this section are comparable with modern state-of-the-art findings. Of particular importance is the area occupation per recording channel (A/Ch), which, for our devised front end, was reduced by a factor of 3 with respect to the front end introduced in [34], and was approximately one-tenth of the area occupied by the work presented in [33]. Additionally, thanks to the implemented closed CMFB loop, the CMI range of the front end described here was significantly higher than those measured for other devices.

Table 8. Performance comparison against state-of-the-art front ends.

	[33] *	[38] *	[39] **	B	This Work **
Year	2016	2018	2019	2022	**2024**
Process	65 nm	180 nm	180 nm	180 nm	**180 nm**
N° Channels	16	4	4	15	**15**
Supply (V)	1	1.8	±1.2	±0.5	**±0.5**
P/Ch (μW)	3.28	4.50	7.68	1.20	**3.77**
A/Ch (mm^2)	0.042	0.072	0.0214	0.012	**0.004**
NEF/PEF	3.19/10.2	1.94/6.77	2.65/8.43	2.65/7.02	**3.32/11.04**
SCMRR (dB)	90	76	>50	75	**80.50**
PSRR (dB)	78	80	>53	74	**72.55**
CMI (mV_{pp})	220	–	–	300	**400**
IRN (μV_{rms})	4.13	3.20	3.87	5.30	**4.04**
THD (%(@ mV_{pp}))	1(0.7)	–	–	1.6 (2)	**1 (1.2)**

*: Results obtained by testing a physical chip. **: Results obtained through post-layout simulations.

6. Conclusions

In this work, we have presented a 16-channel in-pixel neural front-end architecture utilizing a common-mode feedback loop to enhance the SCMRR and the CMI range. The closed loop was achieved by scaling and summing the input currents of DC-coupled inverter-based amplifiers on low-impedance nodes provided by common-gate transistors. Designed using a 180 nm CMOS process from TSMC, post-layout simulations demonstrated a DC gain of 44.16 dB, with nominal values for the SCMRR and PSRR measured at 80.50 dB and 72.55 dB, respectively. The front end was shown to consume 3.77 μW per recording channel, totaling about 60 μW. Noise analysis indicated an IRN of 4.06 μV_{rms} in the frequency range [1 Hz–7.5 kHz]. Further simulations confirmed the system's robustness against PVT and mismatch variations. Overall, the front end exhibited comparable results with other state-of-the-art devices in terms of rejection, noise, and power consumption. Thanks to the implementation of DC-coupled amplifiers and a current-based CMFB loop, the occupied area per channel was minimized to 0.004 mm^2.

Author Contributions: Conceptualization, G.S., A.F. and G.N.; methodology, G.N. and A.F.; software, G.N.; validation, G.N. and A.F.; formal analysis, F.C.; investigation, G.N. and F.C.; resources, G.S.; data curation, G.N.; writing—original draft preparation, G.N., A.F. and F.C.; writing—review and editing, G.S., F.C. and G.N.; visualization, G.N.; supervision, G.S.; project administration, G.S. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding author.

Conflicts of Interest: The authors declare no conflicts of interest.

Appendix A

Derivation of Equation (15)

From the small-signal model in Figure 7, equilibrium equations allow us to obtain the following system:

$$\begin{cases} g_{m2}(-V_y) + g_{o2}(V_{o2} - V_y) = 0 \\ 0 = sC_{gs2}V_y + g_{G2}V_y + \sum_{i=1}^{N} Y_o V_Y + \sum_{i=1}^{N} I_i = (g_{G2} + NY_o + sC_{gs2})V_y + \sum_{i=1}^{N} I_{oi} \end{cases} \quad \text{(A1)}$$

With respect to (A1), the output voltage of the current-summing stage can be calculated as

$$V_{o2} = \frac{g_{m2} + g_{o2}}{g_{o2}} V_y = \frac{g_{m2} + g_{o2}}{g_{o2}} \left(- \frac{\sum_{i=1}^{N} I_{oi}}{g_{G2} + NY_o + sC_{gs2}} \right). \quad \text{(A2)}$$

In particular, I_{oi} and Y_o can be obtained by applying Norton's theorem to the circuit presented in Figure 6. The equivalent output current for the i-th recording channel is, therefore, defined as

$$I_{oi} = g_{mR}(V_i - V_x) - g_{oR}V_x. \tag{A3}$$

From the equilibrium equations applied to the first stage of the front end, V_x can be computed as

$$V_x = \frac{Y_F V_{FB} + XV_i}{D}, \tag{A4}$$

where $Y_F = g_{mF} + g_{oF} + sC_{gsF}$, $D = g_{mR} + Y_F + g_{oF} + g_G + s(C_{gs} + C_{gsF})$, and $X = g_{mR} + sC_{gs} + sC_{gsR}$. By replacing V_x's expression in (A3) with the one calculated in (A4), the former becomes

$$I_{oi} = \frac{g_{mR}Y_F + g_{mR}g_G - g_{oR}s(C_{gs} + C_{gsR})}{D}V_i - (g_{mR} + g_{oR})\frac{Y_F}{D}V_{FB} \simeq$$
$$\simeq g_{mR}\frac{Y_F}{D}(V_i - V_{FB}). \tag{A5}$$

The expression of Y_o is computed by applying a test voltage V_T and imposing $V_i = V_{FB} = 0$:

$$Y_o = \frac{1}{Z_o} = \frac{I_{oi}}{V_T} = g_{oR}\frac{H}{D}, \tag{A6}$$

where $H = D - g_{mR} - g_{oR} = Y_F + g_G + s(C_{gs} + C_{gsR})$. By substituting (A5) and (A6) into (A2), the following expression is obtained:

$$V_{o2} = -\frac{g_{m2} + g_{m2}}{g_{o2}}\frac{g_{mR}Y_F N}{NHg_{oR} + D(g_{G2} + sC_{gs2})}\left(\frac{1}{N}\sum_{i=1}^{N}V_i - V_{FB}\right).$$

Let $NHg_{oR} + D(g_{G2} + sC_{gs2}) = \Delta$; through basic approximations, it is possible to derive the values of d_0, d_1, and d_2

$$\Delta \simeq N(g_{mF} + sC_{gsF} + sC_{gs} + sC_{gsR})g_{oR} +$$
$$(g_{mF} + g_{mR} + sC_{gs} + sC_{gsF} + sC_{gsR})(g_{G2} + sC_{gs2}) \tag{A7}$$

From (A7), the target values can be calculated as

$$d_0 = Ng_{mF}g_{oR} + g_{mF}g_{G2} + g_{mR}g_{G2}$$
$$d_1 = N(C_{gsF} + C_{gs} + C_{gsR})g_{oR} + g_{G2}(C_{gsF} + C_{gs} + C_{gsR}) + C_{gs2}(g_{mF} + g_{mR})$$
$$d_2 = C_{gs2}(C_{gs} + C_{gsR} + C_{gsF}). \tag{A8}$$

References

1. Stevenson, I.H.; Kording, K.P. How advances in neural recording affect data analysis. *Nat. Neurosci.* **2011**, *14*, 139–142. [CrossRef] [PubMed]
2. Lopez, C.M. Unraveling the Brain with High-Density CMOS Neural Probes: Tackling the Challenges of Neural Interfacing. *IEEE Solid-State Circuits Mag.* **2019**, *11*, 43–50. [CrossRef]
3. Duraivel, S.; Rahimpour, S.; Chiang, C.H.; Trumpis, M.; Wang, C.; Barth, K.; Harward, S.C.; Lad, S.P.; Friedman, A.H.; Southwell, D.G.; et al. High-resolution neural recordings improve the accuracy of speech decoding. *Nat. Commun.* **2023**, *14*, 6938. [CrossRef]
4. Wang, D.D.; de Hemptinne, C.; Miocinovic, S.; Qasim, S.E.; Miller, A.M.; Ostrem, J.L.; Galifianakis, N.B.; Luciano, M.S.; Starr, P.A. Subthalamic local field potentials in Parkinson's disease and isolated dystonia: An evaluation of potential biomarkers. *Neurobiol. Dis.* **2016**, *213*, 22–89. [CrossRef] [PubMed]
5. Benabid, A.L.; Chabardes, S.; Mitrofanis, J.; Pollak, P. Deep brain stimulation of the subthalamic nucleus for the treatment of Parkinson's disease. *Lancet Neurol.* **2009**, *1*, 67–81. [CrossRef] [PubMed]
6. Ning, S.; Jorfi, M.; Patel, S.R.; Kim, D.Y.; Tanzi, R.E. Neurotechnological Approaches to the Diagnosis and Treatment of Alzheimer's Disease. *Front. Neurosci.* **2022**, *16*, 854992. [CrossRef] [PubMed]

7. Hochberg, L.R.; Bacher, D.; Jarosiewicz, B.; Masse, N.Y.; Simeral, J.D.; Vogel, J.; Haddadin, S.; Liu, J.; Cash, S.S.; Smagt, P.V.; et al. Reach and grasp by people with tetraplegia using a neurally controlled robotic arm. *Nature* **2012**, *485*, 372–375. [CrossRef]
8. Fetz, E.E. Restoring motor function with bidirectional neural interfaces. *Prog. Brain Res.* **2015**, *52*, 218–241.
9. Choi, J.R.; Kim, S.M.; Ryu, R.H.; Kim, S.P.; Sohn, J.W. Implantable Neural Probes for Brain-Machine Interfaces—Current Developments and Future Prospects. *Exp. Neurobiol.* **2018**, *27*, 453–471. [CrossRef]
10. Zhang, M.; Tang, Z.; Liu, X.; Van der Spiegel, J. Electronic neural interfaces. *Nat. Electron.* **2020**, *3*, 191–200. [CrossRef]
11. Pesaran, B.; Vinck, M.; Einevoll, G.T.; Sirota, A.; Fries, P.; Siegel, M.; Truccolo, W.; Schroeder, C.E.; Srinivasan, R. Investigating large-scale brain dynamics using field potential recordings: Analysis and interpretation. *Nat. Neurosci.* **2018**, *21*, 903–919. [CrossRef] [PubMed]
12. Buzsáki, G.; Anastassiou, C.A.; Koch, C. The origin of extracellular fields and currents–EEG, ECoG, LFP and spikes. *Nat. Rev. Neurosci.* **2012**, *13*, 407–420. [CrossRef] [PubMed]
13. Wang, S.; Garakoui, S.K.; Chun, H.; Gomez Salinas, D.; Sijbers, W.; Putzeys, J. A compact quad-shank CMOS neural probe with 5120 addressable recording sites and 384 fully differential parallel channels. *IEEE Trans. Biomed. Circuits Syst.* **2019**, *13*, 1625–1634. [CrossRef] [PubMed]
14. Lopez, C.M.; Andrei, A.; Mitra, S.; Welkenhuysen, M.; Eberle, W.; Bartic, C.; Puers, R.; Yazicioglu, R.F.; Gielen, G.G.E. An implantable 455-active-electrode 52-channel CMOS neural probe. *IEEE J. Solid-State Circuits* **2014**, *49*, 248–261. [CrossRef]
15. Urai, A.E.; Doiron, B.; Leifer, A.M.; Churchland, A.K. Large-scale neural recordings call for new insights to link brain and behavior. *Nat. Neurosci.* **2022**, *25*, 11–19. [CrossRef] [PubMed]
16. Raducanu, B.C.; Yazicioglu, R.F.; Lopez, C.M.; Ballini, M.; Putzeys, J.; Wang, S.; Andrei, A.; Rochus, V.; Welkenhuysen, M.; Helleputte, N.v.; et al. Time Multiplexed Active Neural Probe with 1356 Parallel Recording Sites. *Sensors* **2017**, *17*, 2388. [CrossRef] [PubMed]
17. Steinmetz, N.A.; Aydin, C.; Lebedeva, A.; Okun, M.; Pachitariu, M.; Bauza, M.; Beau, M.; Bhagat, J.; Böhm, C.; Broux, M.; et al. Neuropixels 2.0: A miniaturized high-density probe for stable, long-term brain recordings. *Science* **2021**, *372*, eabf4588. [CrossRef] [PubMed]
18. Trautmann, E.M.; Hesse, J.K.; Stine, G.M.; Xia, R.; Zhu, S.; O'Shea, D.J.; Karsh, B.; Colonell, J.; Lanfranchi, P.F.; Vyas, P.; et al. Large-scale high-density brain-wide neural recording in nonhuman primates. *bioRxiv* **2023**. [CrossRef]
19. Angotzi, G.N.; Boi, F.; Lecomte, A.; Miele, E.; Malerba, M.; Casile, A.; Berdondini, L. SiNAPS: An implantable active pixel sensor CMOS-probe for simultaneous large-scale neural recordings. *Biosens. Bioelectron.* **2019**, *126*, 355–364. [CrossRef]
20. Boi, F.; Perentos, N.; Lecomte, A.; Schwesig, G.; Zordan, S.; Sirota, A. Multi-shanks SiNAPS Active Pixel Sensor CMOSprobe: 1024 simultaneously recording channels for highdensity intracortical brain mapping. *bioRxiv* **2020**, 749911. [CrossRef]
21. Marblestone, A.H.; Zamft, B.M.; Maguire, Y.G.; Shapiro, M.G.; Cybulski, T.R.; Glaser, J.I.; Amodei, D.; Stranges, P.; Kalhor, R.; Dalrymple, D.A.; et al. Physical principles for scalable neural recording. *Front. Comput. Neurosci.* **2013**, *7*, 137. [CrossRef]
22. Yang, W.; Gong, Y.; Li, W. A Review: Electrode and Packaging Materials for Neurophysiology Recording Implants. *Front. Bioeng. Biotechnol.* **2021**, *8*, 622923. [CrossRef] [PubMed]
23. Fattahi, P.; Yang, G.; Kim, G.; Abidian, M.R. A review of organic and inorganic biomaterials for neural interfaces. *Adv. Mater.* **2014**, *26*, 1846–1885. [CrossRef]
24. Perna, A.; Angotzi, G.N.; Berdondini, L.; Ribeiro, J.F. Advancing the interfacing performances of chronically implantable neural probes in the era of CMOS neuroelectronics. *Front. Neurosci.* **2023**, *17*, 1275908. [CrossRef]
25. Kook, G.; Lee, S.W.; Lee, H.C.; Cho, I.J.; Lee, H.J. Neural Probes for Chronic Applications. *Micromachines* **2016**, *7*, 179. [CrossRef] [PubMed]
26. Polikov, V.S.; Tresco, P.A.; Reichert, W.M. Response of brain tissue to chronically implanted neural electrodes. *J. Neurosci. Methods* **2005**. *148*, 1–18. [CrossRef]
27. Hashemi Noshahr, F.; Nabavi, M.; Sawan, M. Multi-Channel Neural Recording Implants: A Review. *Sensors* **2020**, *20*, 904. [CrossRef] [PubMed]
28. Kim, S.; Tathireddy, P.; Normann, R.A.; Solzbacher, F. Thermal impact of an active 3-D microelectrode array implanted in the brain. *IEEE Trans.-Neural Syst. Rehabil. Eng.* **2007**, *15*, 493–501. [CrossRef] [PubMed]
29. De Dorigo, D.; Moranz, C.; Graf, H.; Marx, M.; Wendler, D.; Shui, B.; Herbawi, A.S.; Kuhl, M.; Ruther, P.; Paul, O.; et al. Fully immersible subcortical neural probes with modular architecture and a deltasigma ADC integrated under each electrode for parallel readout of 144 recording sites. *IEEE J. Solid-State Circ.* **2018**, *53*, 3111–3125. [CrossRef]
30. Lopez, C.M.; Putzeys, J.; Raducanu, B.C.; Ballini, M.; Wang, S.; Andrei, A.; Rochus, V.; Vandebriel, R.; Severi, S.; Hoof, C.V.; et al. A neural probe with up to 966 electrodes and up to 384 configurable channels in 0.13 µm SOI CMOS. *IEEE Trans. Biomed. Circ. Syst.* **2017**, *11*, 510–522. [CrossRef]
31. Lee, H.S.; Eom, K.; Park, M.; Ku, S.B.; Lee, K.; Lee, H.M. High-density neural recording system design. *Biomed. Eng. Lett.* **2022**, *12*, 251–261. [CrossRef] [PubMed]
32. Tang, T.; Goh, W.L.; Yao, L.; Cheong, J.H.; Gao, Y. An integrated multichannel neural recording analog front-end ASIC with area-efficient driven right leg circuit. In Proceedings of the 39th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), Jeju, Republic of Korea, 11–15 July 2017; pp. 217–220.
33. Ng, K.A.; Xu, Y.P. A Low-Power, High CMRR Neural Amplifier System Employing CMOS Inverter-Based OTAs with CMFB through Supply Rails. *IEEE J. Solid-State Circuits* **2016**, *51*, 724–737.

34. Wang, Q.; You, C.; Xue, N.; Zhang, X.; Feng, C.; Zhao, Z.; Yao, L.; Li, T. A DC-coupled 1.2 µW 0.012 mm^2 per channel neural amplifiers array with 75 dB system common mode rejection ratio and 300 mV common mode interference. *Elettron. Lett.* **2022**, *58*, 876–878. [CrossRef]
35. Rodovalho, L.H.; Orazio, A.; Ramos Rodrigues, C. Ultra-Low-Voltage Inverter-Based Operational Transconductance Amplifiers with Voltage Gain Enhancement by Improved Composite Transistors. *Electronics* **2020**, *9*, 1410. [CrossRef]
36. Magnelli, L.; Amoroso, F.A.; Crupi, F.; Cappuccino, G.; Iannaccone, G. Design of a 75-nW, 0.5-V subthreshold complementary metal–oxide–semiconductor operational amplifier. *Int. J. Circuit Theory Appl.* **2013**, *42*, 967–977. [CrossRef]
37. Steyaert, M.S.; Sansen, W.M. A micropower low-noise monolithic instrumentation amplifier for medical purposes. *IEEE J. Solid-State Circuits* **1987**, *22*, 1163–1168. [CrossRef]
38. Rezaei, M.; Maghsoudloo, E.; Bories, C.; De Koninck, Y.; Gosselin, B. A Low-Power Current-Reuse Analog Front-End for High-Density Neural Recording Implants. *IEEE Trans. Biomed. Circuits Syst.* **2018**, *12*, 271–280. [CrossRef]
39. Jomehei, M.G.; Sheikhaei, S. A low-power low-noise CMOS bio-potential amplifier for multi-channel neural recording with active DC-rejection and current sharing. *Microelectron. J.* **2019**, *83*, 197–211. [CrossRef]

Journal of
Low Power Electronics and Applications

MDPI

Article

A Sub-1-V Nanopower MOS-Only Voltage Reference

Siqi Wang [1], Zhenghao Lu [2,*], Kunpeng Xu [3], Hongguang Dai [3], Zhanxia Wu [3] and Xiaopeng Yu [1]

[1] Institute of VLSI Design, Zhejiang University, Hangzhou 310027, China; skiwong@zju.edu.cn (S.W.); yuxiaopeng@zju.edu.cn (X.Y.)
[2] School of Electronics and Information, Soochow University, Suzhou 215123, China
[3] Beijing Smartchip Microelectronics Technology Co., Ltd., Beijing 102200, China; xukunpeng@sgchip.sgcc.com.cn (K.X.); daihongguang@sgchip.sgcc.com.cn (H.D.); wuzhanxia@sgchip.sgcc.com.cn (Z.W.)
* Correspondence: luzhh@suda.edu.cn; Tel.: +86-188-6257-7999

Abstract: A novel low-power MOS-only voltage reference is presented. The Enz–Krummenacher–Vittoz (EKV) model is adopted to provide a new perspective on the operating principle. The normalized charge density, introduced as a new variable, serves as an indicator when trimming the output temperature coefficient. The proposed voltage reference consists of a specific current generator and a 5-bit trimmable load. Thanks to the good match between the current source stage and the output stage, the nonlinear temperature dependence of carrier mobility is automatically canceled out. The circuit is designed using 55 nm COMS technology. The operating temperature ranges from −40 °C to 120 °C. The average temperature coefficient of the output voltage can be reduced to 21.7 ppm/°C by trimming. The power consumption is only 23.2 nW with a supply voltage of 0.8 V. The line sensitivity and the power supply rejection ratio at 100 Hz are 0.011 %/V and −89 dB, respectively.

Keywords: voltage reference; MOS-only; low power; low voltage; sub-threshold

1. Introduction

The low-power voltage reference is an essential circuit block in power-limited applications, such as the Internet of Things (IoT), portable devices, and biological interfaces [1–5]. As a constant reference quantity for the circuit system, the robustness and insensitivity of its output have crucial impacts on the performance of the system. The voltage reference in such applications aims to keep a stable and constant output in any process, voltage, and temperature (PVT) with minimal power.

Currently, voltage reference sources can be roughly sorted into three categories: bipolar (BJT) references, CMOS references, and hybrid references. The traditional bipolar bandgap references (BGRs) generate an output voltage of about 1.2 V (V_{BG}), which is relatively consistent among different process technologies. Despite that BGR has little process variation, it requires a supply voltage higher than 1 V [6–8]. This is not suitable for most low-power applications and is not available in some advanced technology nodes. Furthermore, the temperature coefficient (TC) of the conventional first-order BGR is relatively large. Meanwhile, high-order compensation technology inevitably makes the circuit topology more complex.

To realize a voltage reference operating with a sub-1 V supply, the latter two references have been developed [9–14]. The CMOS references are generally based on the temperature characteristics of the threshold voltage (V_T). The V_T-based references (VTR) utilize the exponential relationship of MOS transistors biased in the subthreshold region to take the place of BJTs. The output voltage of VTRs is usually equal to the extrapolated value of the threshold voltage, thus allowing the lower supply voltage. Unfortunately, the process variation of its output voltage is larger compared to that of BGR. Some VTRs also need resistors to generate a controllable voltage proportional to the absolute temperature (PTAT) [15–17].

Because the current is limited to very small, it can be seen that the resistor not only costs more mask layers in manufacturing but also occupies more chip area. In addition, some designs associate the different types of transistors [1,18,19], generating an output proportional to the difference of two threshold values ($V_{T1} - V_{T2}$). Although this technique can significantly reduce the supply voltage, it also requires the use of more masks and increases the process variations.

Recently, some works combined the principles of VTR and BGR, creating a hybrid voltage reference [20–22]. The hybrid reference generates a nominal value of $V_{BG} - V_T$ with process dependence compensated by a dimension-induced side-effect. However, reducing the minimum supply voltage of the hybrid reference is challenging because of the fixed voltage drop between the base and emitter.

Based on the analyses above, we present a new VTR that only consists of one type of MOS transistor. A novel current source is proposed and discussed by a new approach. A simple trimming method is also adopted to further reduce the TC. The paper is organized as follows. Section 2 reviews the basic EKV model, and introduces it into the explanation of the principle of V_T-based voltage reference. Section 3 presents the design of the proposed circuit and shows the detailed design considerations of each part. Section 4 gives the simulated results and the comparison with other works that have been reported in recent years. Section 5 concludes the paper.

2. Principle of MOS-Only Voltage Reference

2.1. EKV Model

Before we look into the Enz–Krummenacher–Vittoz (EKV) model, it is admirable to revisit the conventional square-law model, which is widely adopted in textbooks. For saturation region and triode region, the drain current equation I_D of the square-law model can be expressed as follows:

$$I_{\mathrm{D}} = \mu C_{\mathrm{ox}} \frac{W}{L} \left[(V_{\mathrm{GS}} - V_{\mathrm{TH}}) V_{\mathrm{DS}} - \frac{1}{2} V_{\mathrm{DS}}^2 \right], \tag{1}$$

where μ is the carrier mobility, C_{ox} is the gate oxide capacitance of unit area, W is the width of the MOS transistor, L is the length of the MOS transistor, and V_{GS} and V_{DS} are, respectively, the gate and drain voltage referred to the source terminal. It is important to note that, to distinguish it from V_T, V_{TH} is the threshold voltage with respect to the source. It can be seen from Equation (1) that the thermal voltage U_T is not taken into account, which leads to the poor coherence between the equation and simulation in temperature-dependent performance. As a circuit module that is highly concerned with temperature characteristics, when designing and analyzing the voltage reference, the model should include a comprehensive representation of temperature characteristics. Thus, we introduce the Enz–Krummenacher–Vittoz (EKV) model to explain and optimize the proposed voltage reference circuit.

The EKV model is a charge-based compact model proposed by Enz, Krummenacher, and Vittoz in Switzerland in 1995 [23]. The starting point of this model was to establish a single equation that could adapt to all inversion regions [24–27]. The drain current I_D of the EKV model is expressed through the normalized drain current i [28,29]:

$$i = \frac{I_D}{I_S}, \tag{2}$$

where I_S is the specific current, defined as

$$I_S = 2n{U_T}^2 \mu C_{ox} \frac{W}{L} = 2n{U_T}^2 \mu C_{ox} K. \tag{3}$$

Here, n is the subthreshold slope factor of the MOS transistor, which varies between 1.3 and 2, depending on the process technology. K is called the aspect ratio. It can be seen that

the temperature dependence of I_S depends on the carrier mobility and thermal voltage. The temperature dependence of the mobility can be expressed as $\mu = \mu(T_R) \cdot (T/T_R)^{-m}$, where the range of m is 1.5 to 2 [30]. Hence, the specific current is a nonlinear increasing function of temperature, approximately proportional to T^{2-m}.

The basic EKV model introduces a new variable q_x, called normalized mobile charge density, to value the amount of charge density at the location x along the channel. The normalized mobile charge density can be calculated from the nonequilibrium voltage V_x along the channel as follows:

$$V_P - V_x = U_T[2(q_x - 1) + \ln(q_x)], \tag{4}$$

$$V_P = \frac{V_G - V_T}{n}, \tag{5}$$

where V_T and V_G are the bulk-referenced threshold voltage and gate voltage, respectively, and V_P is defined as the pinch-off voltage. Equation (4) represents the relationship between the V_x and q_x at the location x. We can replace the subscript of x with S or D to obtain the charge density at the source or drain terminal. When we obtain the q_S and q_D based on the source and drain voltage, the normalized drain current of the transistor i can be derived as follows:

$$i = (q_S^2 + q_S) - (q_D^2 + q_D). \tag{6}$$

On the right side of Equation (6), the square term q^2 represents drift current, which is proportional to the surface potential strength. The linear term q represents diffusion current, which is proportional to the mobile charge density gradient. The part inside the first bracket is called forward current, and the part inside the second bracket is called reverse current. Equation (6) is applicable to both saturated and nonsaturated transistors. However, for saturated transistors, where the V_D is greater than the pinch-off voltage V_P, the current contributed by the second bracket can be neglected.

Above are the basic equations of the EKV model. For the origin of Equations (4)–(6), we provide a detailed derivation in Appendix A. It is admirable that the EKV model provides predictions of MOSFET behavior across all operating regions, including weak inversion, moderate inversion, and strong inversion. In addition, q not only represents the normalized charge density but also can serve as an index of channel inversion level. When $q \ll 1$, that is, $q > q^2$, the diffusion current is dominant. At this point, the channel is in weak inversion (WI). Similarly, when $q \gg 1$, the channel is in strong inversion (SI). When $q = 1$, the drift current is equal to the diffusion current, and the channel is in moderate inversion (MI).

2.2. MOS-Only Voltage Reference Operation Principle

The basic principle of V_T-based voltage reference is to bias a diode-connected MOSFET with a definite current that varies with temperature. The conceptual diagram is shown in Figure 1a, and the following text details the analysis of how to determine the magnitude and the temperature dependence of this current.

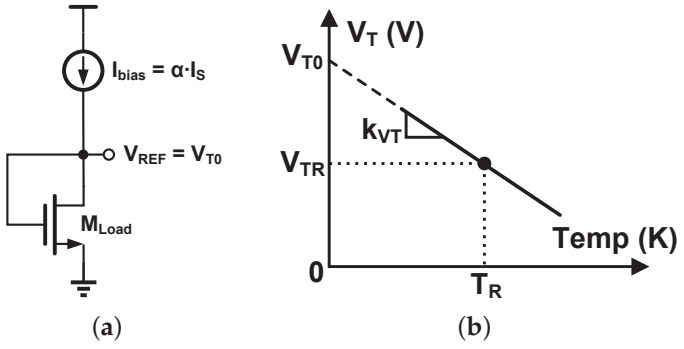


Figure 1. (**a**) The conceptual diagram of V_T-based voltage reference; (**b**) the temperature characteristic of V_T.

As shown in Figure 1b, the threshold voltage V_T is complementary to the absolute temperature (CTAT) with good linearity. Thus its temperature dependence can be represented by a linear function:

$$V_T = V_{T0} - k_{VT}T, \tag{7}$$

where k_{VT} is the temperature coefficient (positive value), and V_{T0} is the intersection when the line is extrapolated to absolute zero temperature.

According to Equations (4) and (5), the gate voltage for a source-grounded MOSFET can be expressed as follows:

$$V_G = nU_T[2(q_S - 1) + \ln(q_S)] + V_T. \tag{8}$$

The first term of Equation (8) is PTAT, and the second term is CTAT. In other words, to make the gate voltage a temperature-independent quantity V_{REF}, the temperature coefficients of the two terms must complement each other.

$$\frac{nk_b}{e_0}[2(q_S - 1) + \ln(q_S)] = k_{VT}, \tag{9}$$

where k_b is the Boltzmann constant, e_0 is the elementary charge. Unfortunately, Equation (9) does not have an analytical solution, but we can use the function $\omega(x)$ to represent the solution of the equation $y + \ln(y) = x$. $\omega(x)$ can be found in the Symbolic Math Toolbox of MATLAB R2018a or newer versions as a mathematical function *wrightOmega*. Therefore, q_S can be expressed as follows:

$$q_S = \frac{1}{2}\omega(\frac{k_{VT}}{k_b/e_0} + 2 + \ln 2). \tag{10}$$

Assuming the transistor is saturated, we eliminate the reverse current by combining Equations (2), (6) and (10), and it can be determined that the required bias current I_{bias} is

$$I_{bias} = I_S \cdot \frac{1}{4}\omega^2(\frac{k_{VT}}{k_b/e_0} + 2 + \ln 2) = \alpha I_S, \tag{11}$$

where α is a positive dimensionless constant. As shown in Equation (11), the quantity in the parentheses is temperature-independent, i.e., α is temperature-independent. Therefore, the temperature characteristic of the required bias current is consistent with the temperature characteristic of I_S. At this bias current, the gate voltage of the diode-connected transistor M_{Load} is equal to V_{T0}. It should be noted that the drain voltage of M_{Load} is also V_{T0}; thus, the assumption of saturation holds.

Through the analysis above, we can see that the key of V_T-based voltage reference is to generate a current exactly proportional to the specific current I_S of the load transistor. It is worth noting that when q_S deviates from our expected value, the right side of Equation (8) introduces a temperature-dependent term. In other words, the target bias current biases the load transistor to a constant inversion level. Interestingly, the temperature characteristic of carrier mobility does not appear in the analysis above. This is because as long as the bias current is proportional to the specific current, the nonlinear temperature dependence of μ is automatically canceled out.

3. Circuit Design

3.1. Proposed Specific Current Source

Just as we concluded in Section 2.2, the key of the V_T-based voltage reference is to design a specific current source. The core circuit of the proposed specific current source is shown in Figure 2. The devices in the circuit determining the current are $M_1 - M_4$. To ensure that the current generated matches the load transistor M_{Load}, the unit size of $M_1 - M_4$ is equal to the size of M_{Load}. In other words, to avoid V_T mismatch caused by inconsistent channel lengths, all NMOS transistors have identical unit sizes to eliminate the

impact of second-order effects. In addition, the bulk terminals of all NMOS are connected to VSS.

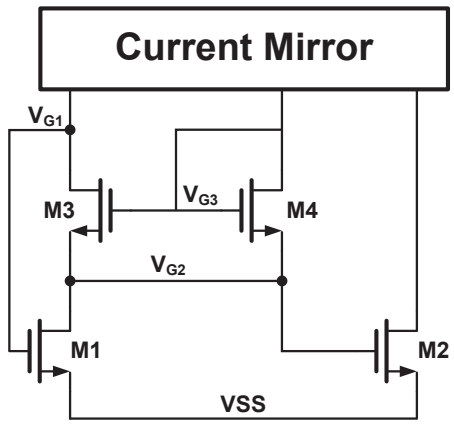


Figure 2. Core circuit of the proposed specific current source.

The current mirror in the upper part of Figure 2 could be replaced by either a simple PMOS current mirror or a cascoded one. For ease of explaining its operating principle, we assume that the current ratios of these three branches are equal. Thus, the drain currents of $M_1 - M_4$ can be expressed as follows:

$$\frac{1}{2} i_1 I_{S1} = i_2 I_{S2} = i_3 I_{S3} = i_4 I_{S4} = I_R. \tag{12}$$

For each transistor, we can use Equations (4) and (6) to sequentially derive out the following relationships:

$$M_1 : \begin{cases} V_{P1} = U_T[-2 + \ln(q_{S1})] = \frac{V_{G1} - V_T}{n} \\ i_1 = q_{S1} = \frac{2I_R}{I_{S1}} \end{cases} ; \tag{13}$$

$$M_2 : \begin{cases} V_{P2} = U_T[-2 + \ln(q_{S2})] = \frac{V_{G2} - V_T}{n} \\ i_2 = q_{S2} = \frac{I_R}{I_{S2}} \end{cases} ; \tag{14}$$

$$M_3 : \begin{cases} V_{P3} - V_{G2} = U_T[2(q_{S3} - 1)] \\ V_{P3} - V_{G1} = U_T[2(q_{D3} - 1)] \\ i_3 = q_{S3}^2 - q_{D3}^2 = \frac{I_R}{I_{S3}} \end{cases} ; \tag{15}$$

$$M_4 : \begin{cases} V_{P4} - V_{G2} = U_T[2(q_{S4} - 1)] \\ i_4 = q_{S4}^2 = \frac{I_R}{I_{S4}} \end{cases} . \tag{16}$$

The equations listed above were simplified based on the proper assumptions as follows: (i) The sizes of M_1 and M_2 are set large enough, thus, the $q_{1,2} = I_{D1,2}/I_{S1,2} \ll 1$. (ii) The sizes of M_3 and M_4 are set small enough, thus, the $q_{3,4} = I_{D3,4}/I_{S3,4} \gg 1$. Simply speaking, $M_{1,2}$ are in weak inversion level, and $M_{3,4}$ are in strong inversion level. If we set the sizes of the M_1 and M_2 to be similar, the difference between V_{G1} and V_{G2} can be controlled at a lower level. In other words, M_3 is in the deep triode region, while $M_{1,2,4}$ is in saturation. In Equations (13), (14) and (16), therefore, we neglected the contribution of $q_{D1,2,4}$ to the normalized drain current.

By combining Equations (13) and (14), we have the following:

$$V_{G1} - V_{G2} = nU_T \ln(\frac{2I_{S2}}{I_{S1}}). \tag{17}$$

Since V_{P3} is equal to V_{P4}, we can easily determine that q_{S3} and q_{S4} are equal. When we take the difference of the first two rows of Equation (15), we can obtain another relationship of V_{G1} and V_{G2}:

$$V_{G1} - V_{G2} = 2U_T(q_{S3} - q_{D3}). \tag{18}$$

The third row of Equation (15) can also be written as follows:

$$q_{S3}{}^2 - q_{D3}{}^2 = \frac{I_R}{I_{S3}} = \frac{q_{S4}^2 \cdot I_{S4}}{I_{S3}} = \frac{q_{S3}^2 \cdot I_{S4}}{I_{S3}}. \tag{19}$$

By substituting Equation (17) into Equation (18), we will have a quadratic equation of q_{S3}:

$$q_{S3}^2 - (q_{S3} - c_1)^2 = q_{S3}^2 \cdot c_2, \tag{20}$$

where $c_1 = \frac{1}{2} n \ln(2I_{S2}/I_{S1})$, and $c_2 = I_{S4}/I_{S3}$. Finally, we can obtain the solution of Equation (20), and the produced current can be expressed as follows:

$$q_{S3} = \frac{c_1}{c_2}(1 + \sqrt{1 - c_2}) = q_{S4}, \tag{21}$$

$$I_R = q_{S4}^2 \cdot I_{S4} = \frac{c_1^2}{c_2^2}(1 + \sqrt{1 - c_2})^2 \cdot I_{S4}. \tag{22}$$

The other root of Equation (20) is discarded, as it does not comply with the assumption made before, that $q_{S3,D3} \gg 1$. If we substitute c_1 and c_2 with the aspect ratios of $M_1 - M_4$, Equation (22) can be rewritten as follows:

$$I_R = \frac{1}{2}\mu U_T^2 C_{ox} n^3 \ln^2\left(\frac{2K_2}{K_1}\right) \cdot \frac{K_3^2}{K_4}\left(1 + \sqrt{1 - \frac{K_4}{K_3}}\right)^2. \tag{23}$$

Therefore, the current of each branch is proportional to the specific current. The temperature characteristic of I_R also follows the characteristic of the unit transistor.

The complete schematic of the proposed voltage reference is given in Figure 3. As annotated in the figure, the overall circuit is composed of four parts: a specific current source, an operational transconductance amplifier (OTA), a start-up circuit, and a trimmable output stage. A cascode transistor M_5 is added to mitigate the difference in drain voltage between M_1 and M_2. The OTA is used to decrease the voltage difference of V_{D7} and V_{D8}, thus, improving the accuracy of the current mirror and reducing the line sensitivity. The role of the start-up circuit is to help the circuit to reach the desired stable state after power-up. Finally, the output stage copies the I_R and generates the reference voltage V_{REF}. In the following subsection, we will give detailed explanations of the operating principles of the remaining part.

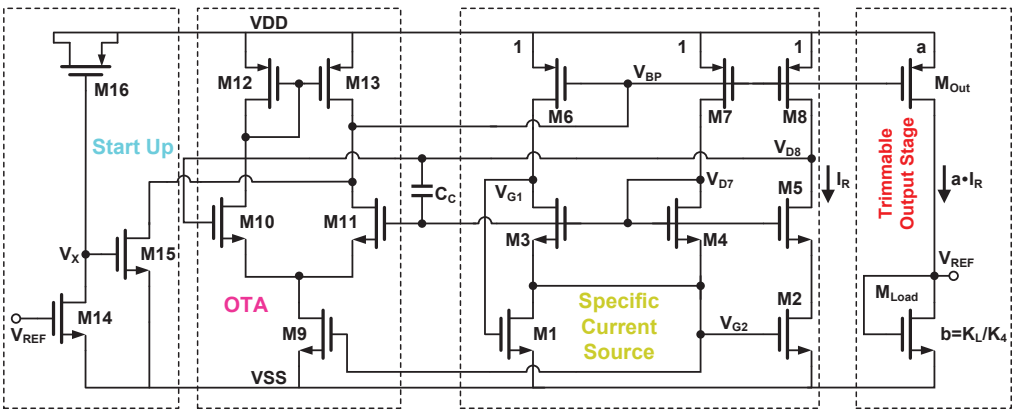


Figure 3. Schematic of the proposed V_T-based voltage reference source.

3.2. Loop Stability

While the amplifier enhances the loop gain, at the same time, the stability of the loop needs to be carefully analyzed. Thus, to prevent the parasitic oscillation of the circuit, a compensation capacitor C_C is added.

The proposed specific current source contains three branches, and both positive feedback and negative feedback exist in the loop. Thus, the expression of the total loop gain is quite complex. Based on reasonable simplifications and comparison with simulation, the frequency response of the loop gain can be expressed as follows:

$$LG(s) = \frac{K(s - w_z)}{(s - w_{p1})(s - w_{p2})(s - w_{p3})}, \tag{24}$$

where

$$\begin{aligned} w_z &= -\tfrac{g_{m1}}{C_{gs2}}; \\ w_{p1} &= w_{ota} = -\tfrac{g_{ota}}{C_{ota}}; \\ w_{p2} &= -\frac{g_{dsp}}{C_c\left(1+\frac{g_{m2}}{g_{m1}}+\frac{g_{m2}g_{m3}}{g_{m4}g_{ds3}}\right)}; \\ w_{p3} &= -\tfrac{g_{m2}}{C_{gs2}} \cdot (1 + \tfrac{g_{m1}}{g_{m2}} + \tfrac{g_{m1}}{g_{ds3}}); \\ LG(0) &= -\tfrac{g_{mp}}{g_{dsp}} \cdot \tfrac{g_{m2}}{g_{ds3}} \cdot (1 - \tfrac{g_{m3}}{g_{m_4}}) \cdot \tfrac{g_{mota}}{g_{ota}}. \end{aligned} \tag{25}$$

$LG(0)$ is the DC gain of the loop. g_{ota} and C_{ota} denote the conductance and capacitance at the output node of the amplifier. The loop gain contains one negative zero and three negative poles. w_{p1} and w_{p2} are much smaller than w_{p3}, contributing a phase shift of $-180°$. Given that the current in M_1 is twice that of M_2, g_{m1}/g_{m2} is approximately equal to 2. Hence, w_{p3} is larger than the zero w_z, causing the phase to increase by 90° and then decrease by 90°. The distribution of the loop's poles and zero is shown in Figure 4. As the compensating capacitance C_C increases, w_{p2} moves towards the origin. By carefully locating two poles, w_{p1-2}, it is possible to retain enough phase margin. The detailed stability results will be presented in the section on simulation results.

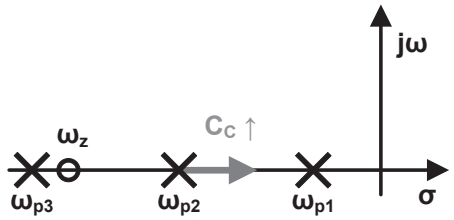


Figure 4. Pole-zero plot of loop gain and the effect of compensating capacitor.

3.3. Output Stage

After generating the required current I_R, we can copy it into the load transistor with a certain proportion and obtain a reference voltage approximately equal to V_{T0}. Due to the variation of V_T and its temperature coefficient during the actual manufacturing, it is necessary to perform trimming in the output branch. As follows, two methods of trimming will be presented: (i) trimming the multiplier of M_{Load}; (ii) trimming the copy ratio of the current mirror.

If we suppose the copy ratio of the PMOS current mirror is $1 : a$, and the aspect ratio of the load transistor is K_L, then

$$q_{SL} = \sqrt{\frac{aK_4}{K_L}} \cdot q_{s4} = \frac{c_1}{c_2}(1 + \sqrt{1 - c_2}) \cdot \sqrt{\frac{a}{b}}, \tag{26}$$

where $b = K_L/K_4$. According to Equation (10), the trimming range determined by the variables a and b must cover the variations in k_{VT} caused by the process corner. The effects of a and b on the normalized charge density of M_{Load} are shown in Figure 5. If we increase the output stage current, i.e., a, the normalized charge density of the load q_{SL} will rise.

When it reaches the value calculated from Equation (10), the temperature coefficient of the V_{REF} approximates zero. Similarly, adjusting the size of the load transistor, i.e., b, can achieve the same goal.

The dashed line represents the target charge density, where the temperature coefficient should be zero. $q^*_{SL}(k_{VT,max})$ corresponds to the case of a relatively large k_{VT}, and, similarly, the $q^*_{SL}(k_{VT,min})$ does, too. Hence, the intersection points of two dashed lines and $q_{SL}(a)$, or $q_{SL}(b)$, indicate the minimum trimming range.

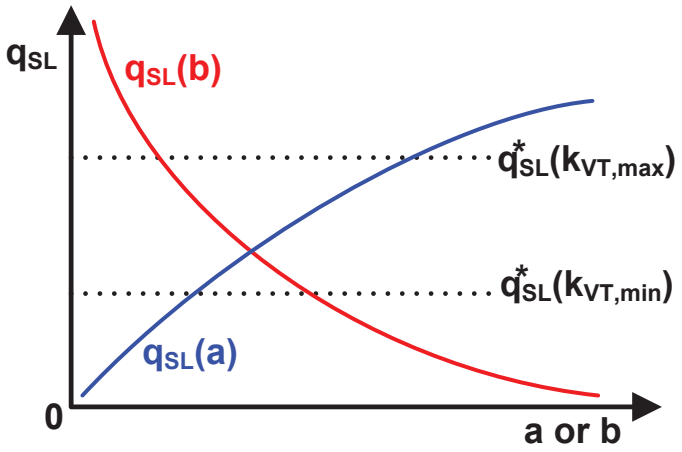


Figure 5. The impact of a (current mirror copy ratio) and b (size ratio K_L/K_4) on the normalized charge density of M_{Load}.

3.4. Start-Up Circuit

When the power supply voltage is applied, all branches in the voltage reference may remain zero. Thus, a start-up circuit formed by $M_{14} - M_{16}$ is adopted to assist the circuit escape from the zero-current state [31].

In the initial start-up stage, due to V_{REF} being zero, M_{14} is turned off. Therefore, the ramp-up of VDD is coupled to node V_{ST} through the MOS capacitor M_{16}. Once the voltage of V_{ST} exceeds the threshold voltage of M_{15}, the node V_{BP} will be pulled down, hence the branch current rising. Meanwhile, V_{REF} will also rise until it reaches the final steady state. When V_{REF} becomes the desired value, approximately V_{T0}, M_{14} is turned on, discharging the node V_{ST} to ground. Finally, M_{15} is turned off, disconnecting the start-up circuit from the core circuit.

4. Simulation Results

In the early stage of circuit design, we use the EKV model to investigate the behavior of the circuit and roughly determine the size of the transistor. The parameters of the EKV model can be extracted through simulation using a MATLAB script which is available on the website provided in [29]. To ensure the simulation accuracy, the final results are still obtained through the Spectre simulator with the BSIM4 model. Table 1 gives the sizes of each transistor in Figure 3.

Table 1. Sizes of the transistors in Figure 3.

Transistor	Size	Transistor	Size
M_u	0.12/20 (µm/µm)	$M_{10,11}$	$4M_u$
M_1	$64M_u$	$M_{12,13}$	5/20 (µm/µm)
M_2	$52M_u$	M_{14}	$2M_u$
M_3	$3M_u$	M_{15}	$2M_u$
$M_{4,5}$	$1M_u$	M_{16}	5/20 (µm/µm)
M_{6-8}	5/20 (µm/µm)	M_{Out}	3×5/20 (µm/µm)
M_9	$104M_u$	M_{Load}	$(\frac{1}{4}\sim\frac{47}{64})M_u$

4.1. Temperature Dependence before Trimming

As explained in Section 3.3, we can trim the temperature coefficient by adjusting the size of the load transistor or the current mirror ratio. It is preferred to take the method of trimming load, thus the consumption of the circuit can be constant. The total current consumption of the proposed voltage reference is proportional to the specific current of the unit NMOS transistor. According to Equation (3), the power of the circuit is approximately a PTAT quantity. At room temperature, the generated specific current I_R is 3.6 nA. As we set the output current ratio a equal to 3, the total current is approximately 8 times that of I_R, i.e., 29.0 nA. Across the entire temperature range, the total current increases from 19.3 nA at -40 °C to 41.2 nA at 120 °C.

In order to determine the trimming range of the circuit, it is necessary to evaluate the temperature dependence before trimming. A Monte Carlo simulation of 500 samples is performed, sweeping the temperature from -40 °C to 120 °C. Both mismatch and corner variation are included in the model to ensure the performance after layout. To avoid making the figure too cluttered, only 100 V_{REF} curves are shown in Figure 6. Thanks to the fact that the specific current of M_{Load} is well matched to the current generated, curves before trimming are relatively flat. The average value of V_{REF} varies from 421 mV to 522 mV. Figure 7 shows the TC histogram of 500 samples. The mean of TC is about 41.8 ppm/°C, and the standard deviation is about 37.0 ppm/°C. The statistical distribution indicates that the temperature coefficient of the vast majority of samples is less than 100 ppm/°C, which can be easily reduced through trimming.

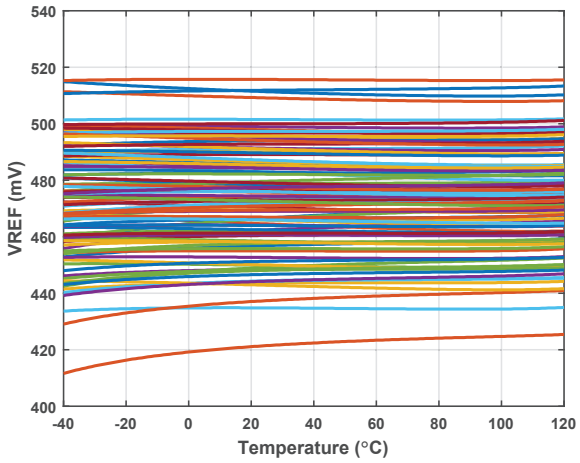


Figure 6. Monte Carlo simulation results before trimming: temperature dependence of V_{REF}.

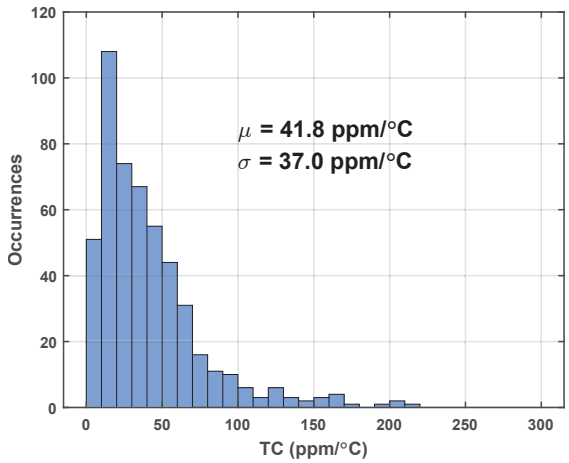


Figure 7. Monte Carlo simulation results before trimming: histogram of temperature coefficient.

4.2. Temperature Dependence after Trimming

The process variation range of V_{T0} is relatively wide, as Figure 6 confirms. Therefore, we cannot use the one-point trimming methodology as BJT-based voltage reference does. The trimming method we adopted can be described as follows: (1) Sweep the trim bits at one ambient temperature, e.g., 20 °C, to obtain the voltage of V_{REF}. (2) Sweep the trim bits at another ambient temperature, e.g., 60 °C, to obtain another set of output values. (3) Take the absolute difference between two sets of data. The trim bits corresponding to the minimum difference are the final bits we need.

A single NMOS switch is used to connect or disconnect the variable load transistors to the output. The size of the variable load follows a binary order, specifically, 1, 1/2, 1/4, 1/16, and 1/32, with respect to the size of M_{Load}. Similarly, we performed a Monte Carlo simulation of 500 samples with the above trimming procedure. Figure 8 presents the trimmed output voltage after subtracting its mean value. The curves intersect at the two temperature points where we performed the trimming. The histogram in Figure 9 shows that the mean of TC is reduced to 21.7 ppm/°C and the standard deviation to 10.6 ppm/°C. A total of 84.2 percent of the samples have a temperature coefficient below 30 ppm/°C, and 95.4 percent of the samples have a temperature coefficient below 40 ppm/°C.

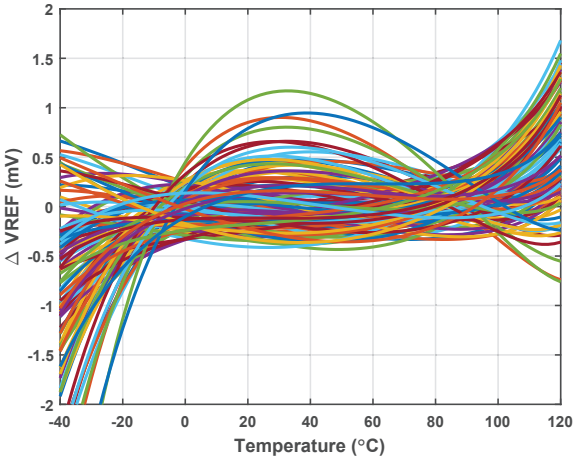


Figure 8. Monte Carlo simulation results after trimming: temperature dependence of ΔV_{REF}.

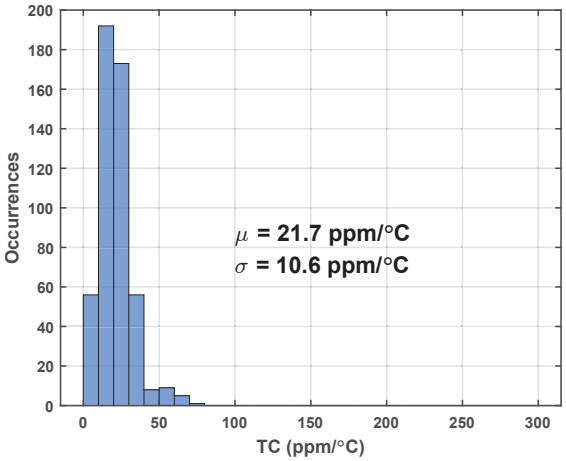


Figure 9. Monte Carlo simulation results after trimming: histogram of temperature coefficient.

After calibration, the distribution of average output voltage and the final determined trimming bits are shown in Figures 10 and 11. The mean value of the V_{REF} is 474.4 mV, roughly similar to the output under the typical process corner. As we adopted the global Monte Carlo model during simulation, the variation coefficient σ/μ is 5.8%, which is larger compared to the coefficient of BGR. V_{REF} is relatively higher under the fast corner and

lower under the slow corner; therefore, the proposed voltage reference can also serve as an indicator of the NMOS corner. Figure 11 implies that the selection of a 5-bit trimming range can meet the needs of the vast majority of samples. The bits number varies from 9 to 23, and its mean value is around the half of 2^5.

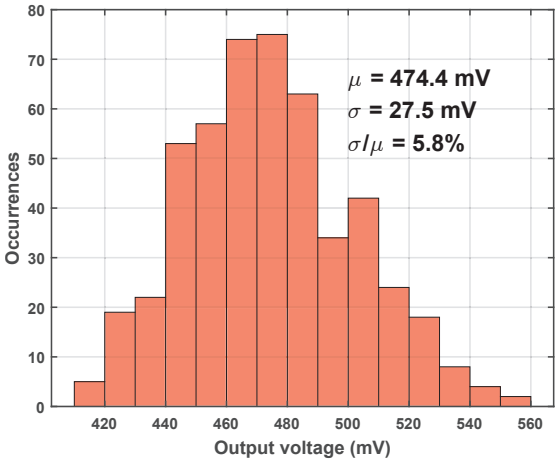


Figure 10. Histogram of average output voltage after trimming.

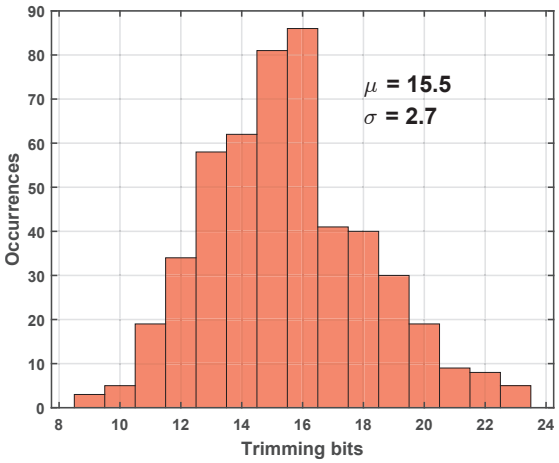


Figure 11. Histogram of determined trimming bits number.

4.3. Frequency Compensation

Figure 12 illustrates the frequency response of the loop gain with or without C_C. The red circles in the figure denote the unit gain frequency and the corresponding phase margin. As explained in Section 3.2, the increasing of C_C compresses the unity gain bandwidth of the loop. When the unity gain bandwidth decreases, the frequency point corresponding to the phase margin first approaches w_{p3} and then moves closer to w_z. In a figurative sense, the corresponding point will first climb a hill and then descend into a valley. The simulation result of phase margin versus C_C is shown in Figure 13. The capacitance value of the C_C is finally determined to be 400 fF, while the phase margin of the loop is 38.7°.

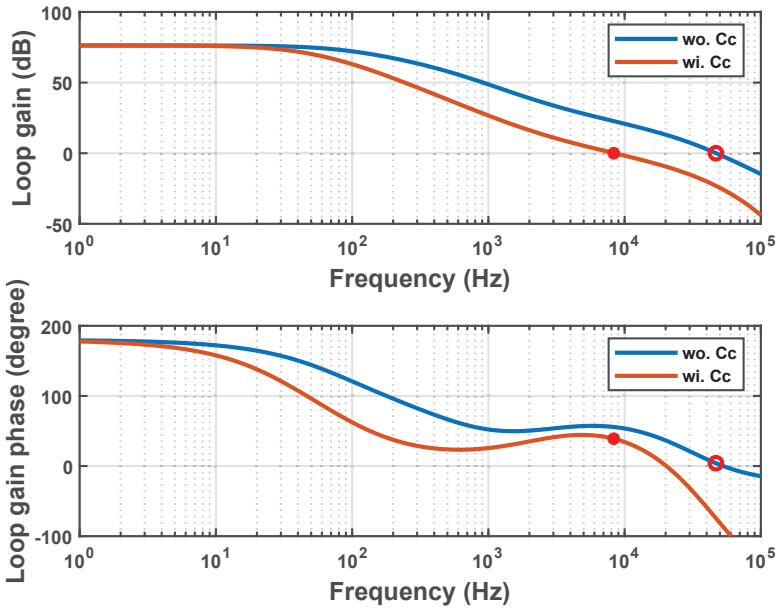


Figure 12. Frequency response of loop gain without or with C_C.

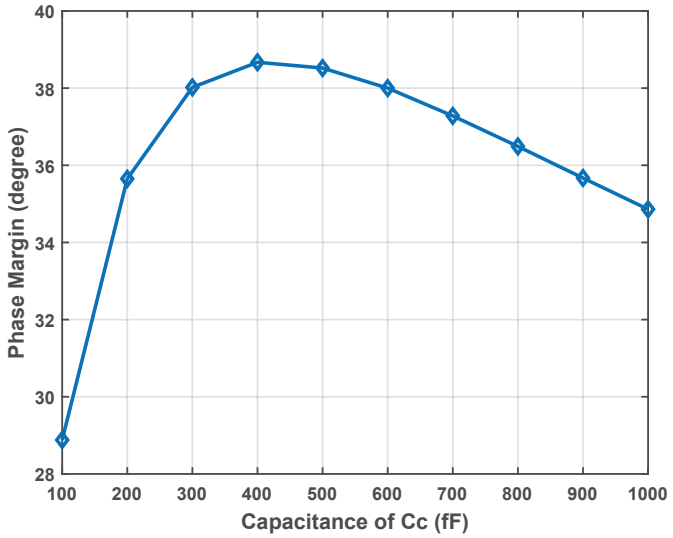


Figure 13. Phase margin as a function of C_C.

4.4. Supply Dependence

The supply dependence of the proposed voltage reference was simulated at room temperature. Figure 14 shows the output voltage and the input difference of the amplifier as functions of VDD. The minimum supply voltage could be as low as 0.8 V, and the line sensitivity (LS) is 0.011%, ranging from 0.8 V to 1.5 V. The maximum supply voltage is mainly limited by the breakdown voltage of V_{DS}. The results also indicate that a lower supply voltage leads to inaccuracy in the specific current generator. The acceptable supply voltage depends not only on the voltage headroom of the PMOS current mirror but also on the allowable amplifier input residue, because the larger the residue, the worse the temperature coefficient of V_{REF}. Figure 15 shows the power supply rejection ratio (PSRR) with a load capacitance of 10 pF at room temperature. Thanks to the additional amplifier, the PSRR is −89 dB at 100 Hz.

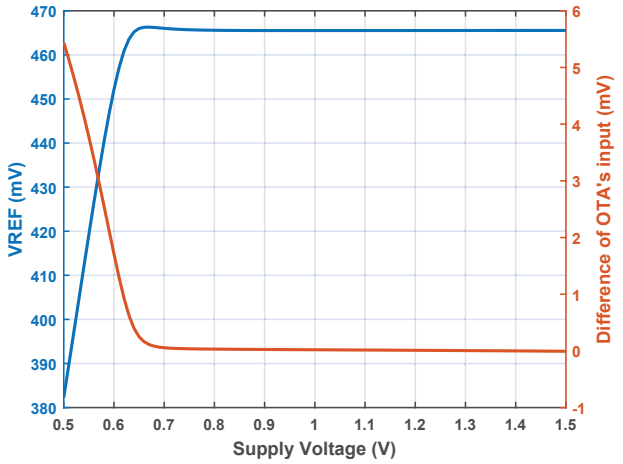


Figure 14. V_{REF} and difference of OTA's input voltage versus supply voltage.

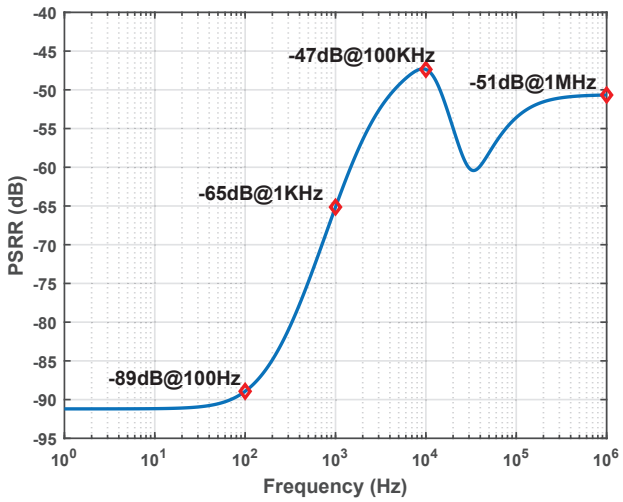


Figure 15. PSRR with a C_L of 10 pF.

Figure 16 shows the layout of the proposed voltage reference. Each part of the circuit is annotated, including the compensation capacitor C_C. The overall area of the core circuit is only 90 µm × 100 µm. Since the size of all NMOS is determined based on the unit cell M_u, the layout of the circuit is highly compact. C_C is composed of a metal–insulator–metal (MIM) capacitor using top metal; thus, it can be stacked on the active device to save area. Dummy transistors are added on both sides of the layout to mitigate the layout-dependent effect (LDE).

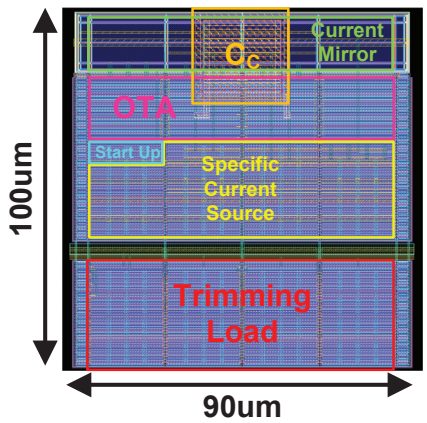


Figure 16. Layout.

Table 2 compares the performance of the proposed V_T-based voltage reference with other reported works. It can be seen that the proposed reference is very competitive in many aspects. We balanced the circuit's power and TC, adding an amplifier to improve LS with an acceptable current consumption. Thus, our design shows excellent supply and temperature independence. Meanwhile, our design only adopts one type of MOSFET, which makes it more efficient in terms of mask layer numbers and process portability. Compared with [32], which also contains one MOSFET type, our design achieves a lower supply voltage and less power consumption. In addition, our design enables the majority of chips to achieve a small TC through a 5-bit trimming, which improves the yield in practical system applications.

Table 2. Comparison of the proposed voltage reference with previous works.

Parameter	This Work	TCASII'23 [1]	TCASII'23 [15]	TCASII'21 [32]	SBCCI'20 [14]	JLPEA'18 [18]
Process (nm)	55	180	65	180	130	350
Temp. Range (°C)	−40–120	−10–100	−20–80	−40–85	−40–125	−70–85
TC (ppm/°C)	21.7	90	79.4	60.86	28.8	42
V_{REF} (mV)	474.4	288	107.2	985	575.2	1520
σ/μ (%)	5.8	0.574	2.4	2.6	4.32	2
Supply (V)	0.8–1.5	0.5–2	0.4–0.8	1.5–6	1–1.8	1.7–3.3
LS (%/V)	0.011	0.23	0.54	0.003	0.071	10
Consumption (nW)	23.2	0.5	56.7	63	36.4	1110
PSRR (dB)	−89 (@100 Hz)	−45 (@100 Hz)	−66.5 (@10 Hz)	−93.3 (@10 Hz)	−54.4 (@100 Hz)	−35 (@100 Hz)
Area (mm^2)	0.009	0.0029	0.0084	0.015	0.0078	0.06
Components	1 Type MOS	3 Types MOS	MOS + Res	2 Types MOS	1 Type MOS	2 Types MOS + Res

5. Conclusions

This paper presents a 55 nm low-power V_T-based voltage reference. The reference proposed only requires MOS transistors, and no BJTs or resistors are needed. A detailed explanation of the operating principle and design of the circuit was given with the EKV model. The reference consists of a novel specific current generator, a simple amplifier, a start-up circuit, and a trimmable output stage.

The simulation results showed that a balanced trade-off between TC and power was achieved. The proposed voltage reference has an average TC of 21.7 ppm/°C with a power consumption of 23.2 nW. The circuit also has excellent supply independence. Its line sensitivity is only 0.011 %/V, and PSRR is −89 dB at 100 Hz. The core area of the circuit is 0.009 mm^2. Therefore, the proposed circuit is a suitable voltage reference module for low-power applications.

Author Contributions: Conceptualization, S.W.; methodology, S.W.; validation, S.W.; writing—original draft, S.W.; writing—review and editing, Z.L. and X.Y.; supervision, K.X.; project administration, H.D. and Z.W. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the National Key Research and Development Program of China under Grant SQ2022YFB3200085.

Data Availability Statement: All data are available from the authors upon request.

Conflicts of Interest: Authors Kunpeng Xu, Hongguang Dai and Zhanxia Wu were employed by the company Beijing Smartchip Microelectronics Technology Co., Ltd. The remaining authors declare that the research was conducted in the absence of any commercial or finacial relationships that could be construed as a potential conflict of interest.

Appendix A

In this appendix, the origins of basic EKV equations are derived. Firstly, there are two transport mechanisms in the composition of the MOS transistor: drift current and diffusion current. The total drain current I_D can be expressed as follows:

$$I_D = \mu W\left(-Q_i\frac{d\psi_S}{dx} + U_T\frac{dQ_i}{dx}\right), \tag{A1}$$

where Q_i is the mobile charge density, and ψ_S is the surface potential at the position x along the channel. The diffusion factor varies little across the WI, MI, and SI. Therefore, for diffusion current, the relationship between Q_i and surface potential can be approximated as follows:

$$d\left(-\frac{Q_i}{C_{ox}}\right) = -\left(1+\frac{\gamma}{2\sqrt{\psi_S}}\right)d\psi_S = -nd\psi_S, \tag{A2}$$

where γ is known as the back gate parameter. We normalize the Q_i as follows:

$$q = -\frac{Q_i}{2nU_TC_{ox}}, \tag{A3}$$

Thus, Equation (A2) can be expressed as follows:

$$d\psi_S = -2U_Tdq. \tag{A4}$$

Therefore, we rewrite the differential equation of the drain current:

$$\int_S^D I_Ddx = \int_S^D -2nU_T^2C_{ox}(2q+q)dq. \tag{A5}$$

Finally, we perform the integration from the source terminal to the drain terminal and obtain

$$I_D = 2nU_T^2\mu C_{ox}\frac{W}{L}\cdot\left[\left(q_S^2+q_S\right)-\left(q_D^2+q_D\right)\right]. \tag{A6}$$

Another fundamental physical equation of the EKV model relates the nonequilibrium voltage V and q:

$$Q_i \propto \exp\left(\frac{\psi_S-\phi_F-V}{U_T}\right), \tag{A7}$$

hence,

$$\frac{dQ_i}{Q_i} = \frac{dq}{q} = \frac{d\psi_S-dV}{U_T}. \tag{A8}$$

Substituting Equation (A4) into Equation (A8), we obtain

$$\int_{q_x}^{q_P}\left(2+\frac{1}{q}\right)dq = \int_{V_x}^{V_P}-\frac{1}{U_T}dV. \tag{A9}$$

where q_P denotes the normalized charge density at the pinch-off point and equals one. Thus, we connect the V and q after integration and have Equation (4).

The physical interpretation of the linear relationship between V_P and V_G is relatively complex, and due to text space constraints, the detailed derivation is not provided here. Readers can find a detailed explanation of Equation (5) in reference [23,28].

References

1. Wang, J.; Sun, X.; Cheng, L. A Picowatt CMOS Voltage Reference Operating at 0.5-V Power Supply with Process and Temperature Compensation for Low-Power IoT Systems. *IEEE Trans. Circuits Syst. II Express Briefs* **2023**, *70*, 1336–1340. [CrossRef]
2. Parisi, A.; Finocchiaro, A.; Papotto, G.; Palmisano, G. Nano-Power CMOS Voltage Reference for RF-Powered Systems. *IEEE Trans. Circuits Syst. II Express Briefs* **2018**, *65*, 1425–1429. [CrossRef]

3. Zhu, Z.; Hu, J.; Wang, Y. A 0.45 V, Nano-Watt 0.033% Line Sensitivity MOSFET-Only Sub-Threshold Voltage Reference with No Amplifiers. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2016**, *63*, 1370–1380. [CrossRef]
4. Yan, W.; Li, W.; Liu, R. Nanopower CMOS Sub-Bandgap Reference with 11 ppm/°C Temperature Coefficient. *Electron. Lett.* **2009**, *45*, 627. [CrossRef]
5. Zhang, H.; Liu, X.; Zhang, J.; Zhang, H.; Li, J.; Zhang, R.; Chen, S.; Carusone, A.C. A Nano-Watt MOS-Only Voltage Reference with High-Slope PTAT Voltage Generators. *IEEE Trans. Circuits Syst. II Express Briefs* **2018**, *65*, 1–5. [CrossRef]
6. Kim, M.; Cho, S. A Single BJT Bandgap Reference with Frequency Compensation Exploiting Mirror Pole. *IEEE J. Solid-State Circuits* **2021**, *56*, 2902–2912. [CrossRef]
7. Zhang, Z.; Zhan, C.; Wang, L.; Law, M.K. A −40 °C–125 °C 0.4-µA Low-Noise Bandgap Voltage Reference with 0.8-mA Load Driving Capability Using Shared Feedback Resistors. *IEEE Trans. Circuits Syst. II Express Briefs* **2022**, *69*, 4033–4037.
8. Huang, W.; Liu, L.; Zhu, Z. A Sub-200nW All-in-One Bandgap Voltage and Current Reference without Amplifiers. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *68*, 121–125. [CrossRef]
9. Vita, G.D.; Iannaccone, G. A Sub-1 V, 10 ppm/°C, Nanopower Voltage Reference Generator. In Proceedings of the 2006—32nd European Solid-State Circuits Conference, Montreaux, Switzerland, 19–21 September 2006; pp. 307–310.
10. Ueno, K.; Hirose, T.; Asai, T.; Amemiya, Y. A 300 nW, 15 ppm/°C, 20 ppm/V CMOS Voltage Reference Circuit Consisting of Subthreshold MOSFETs. *IEEE J. Solid-State Circuits* **2009**, *44*, 2047–2054. [CrossRef]
11. Qiao, H.; Zhan, C.; Chen, Y. A −40 °C to 140 °C Picowatt CMOS Voltage Reference with 0.25-V Power Supply. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *68*, 3118–3122. [CrossRef]
12. Aminzadeh, H. All–MOS Self-Powered Subthreshold Voltage Reference with Enhanced Line Regulation. *AEU Int. J. Electron. Commun.* **2020**, *122*, 153245. [CrossRef]
13. Luong, P.; Christoffersen, C.; Rossi-Aicardi, C.; Dualibe, C. Nanopower, Sub-1 V, CMOS Voltage References with Digitally-Trimmable Temperature Coefficients. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2017**, *64*, 787–798. [CrossRef]
14. De Lima, V.F.; Klimach, H. A 37 nW MOSFET-Only Voltage Reference in 0.13 µm CMOS. In Proceedings of the 2020 33rd Symposium on Integrated Circuits and Systems Design (SBCCI), Campinas, Brazil, 24–28 August 2020; pp. 1–6.
15. Che, C.; Lei, K.M.; Martins, R.P.; Mak, P.I. A 0.4-V 8400-µm^2 Voltage Reference in 65-nm CMOS Exploiting Well-Proximity Effect. *IEEE Trans. Circuits Syst. II Express Briefs* **2023**, *70*, 3822–3826.
16. Parisi, A.; Finocchiaro, A.; Palmisano, G. An accurate 1-V threshold voltage reference for ultra-low power applications. *Microelectron. J.* **2017**, *63*, 155–159. [CrossRef]
17. Fan, H.; Fang, Z.; Li, Y.; Qian, Q.; Kang, X.; Chen, M.; Sun, W. A 3.38-ppm/°C Voltage Reference for Harsh Environment Applications Empowered by the In-Loop Resistance Trimming Technique. *IEEE Trans. Circuits Syst. II Express Briefs* 2023, *early access.* [CrossRef]
18. Navidi, M.M.; Graham, D.W. A Low-Power Voltage Reference Cell with a 1.5 V Output. *J. Low Power Electron. Appl.* **2018**, *8*, 19. [CrossRef]
19. Seok, M.; Kim, G.; Blaauw, D.; Sylvester, D. A Portable 2-Transistor Picowatt Temperature-Compensated Voltage Reference Operating at 0.5 V. *IEEE J. Solid-State Circuits* **2012**, *47*, 2534–2545. [CrossRef]
20. Ji, Y.; Lee, J.; Kim, B.; Park, H.J.; Sim, J.Y. 18.8 A 192pW Hybrid Bandgap-Vth Reference with Process Dependence Compensated by a Dimension-Induced Side-Effect. In Proceedings of the 2019 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 17–21 February 2019; pp. 308–310.
21. Liu, X.; Liang, S.; Liu, W.; Sun, P. A 2.5 ppm/°C Voltage Reference Combining Traditional BGR and ZTC MOSFET High-Order Curvature Compensation. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *68*, 1093–1097. [CrossRef]
22. Chowdary, G.; Kota, K.; Chatterjee, S. A 1-nW 95-ppm/°C 260-mV Startup-Less Bandgap-Based Voltage Reference. In Proceedings of the 2020 IEEE International Symposium on Circuits and Systems (ISCAS), Seville, Spain, 12–14 October 2020; pp. 1–4.
23. Enz, C.C.; Krummenacher, F.; Vittoz, E.A. An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications. *Analog Integr. Circuits Signal Process.* **1995**, *8*, 83–114. [CrossRef]
24. Enz, C.; Chicco, F.; Pezzotta, A. Nanoscale MOSFET Modeling: Part 1: The Simplified EKV Model for the Design of Low-Power Analog Circuits. *IEEE Solid-State Circuits Mag.* **2017**, *9*, 26–35. [CrossRef]
25. Enz, C.; Chicco, F.; Pezzotta, A. Nanoscale MOSFET Modeling: Part 2: Using the Inversion Coefficient as the Primary Design Parameter. *IEEE Solid-State Circuits Mag.* **2017**, *9*, 73–81. [CrossRef]
26. Enz, C.; Chalkiadaki, M.A.; Mangla, A. Low-power analog/RF circuit design based on the inversion coefficient. In Proceedings of the ESSCIRC Conference 2015—41st European Solid-State Circuits Conference (ESSCIRC), Graz, Austria, 14–18 September 2015; IEEE: New York, NY, USA, 2015; pp. 202–208.
27. Enz, C.; Pezzotta, A. Nanoscale MOSFET modeling for the design of low-power analog and RF circuits. In Proceedings of the 2016 MIXDES—23rd International Conference Mixed Design of Integrated Circuits and Systems, Lodz, Poland, 23–25 June 2016; IEEE: New York, NY, USA, 2016; pp. 21–26.
28. Jespers, P. *The gm/ID Methodology, a Sizing Tool for Low-Voltage Analog CMOS Circuits: The Semi-Empirical and Compact Model Approaches*; Springer Science & Business Media: New York, NY, USA, 2009.
29. Jespers, P.G.A.; Murmann, B. *Systematic Design of Analog CMOS Circuits: Using Pre-Computed Lookup Tables*; Cambridge University Press: Cambridge, UK, 2017.
30. Filanovsky, I.; Allam, A. Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits. *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.* **2001**, *48*, 876–884. [CrossRef]

31. Alhasssan, N.; Zhou, Z.; Sánchez Sinencio, E. An All-MOSFET Sub-1-V Voltage Reference with a—51-dB PSR up to 60 MHz. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2017**, *25*, 919–928. [CrossRef]
32. Chen, Y.; Guo, J. A 42nA I_Q, 1.5–6V V_{IN}, Self-Regulated CMOS Voltage Reference with −93dB PSR at 10 Hz for Energy Harvesting Systems. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *68*, 2357–2361. [CrossRef]

Journal of
Low Power Electronics and Applications

MDPI

Article

Design and Analysis of Self-Tanked Stepwise Charging Circuit for Four-Phase Adiabatic Logic

William Morell [1,*] and Jin-Woo Choi [2]

[1] School of Electrical Engineering and Computer Science, Louisiana State University, Baton Rouge, LA 70803, USA
[2] Department of Electrical and Computer Engineering, Michigan Technological University, Houghton, MI 49931, USA; choijw@mtu.edu
* Correspondence: wmorel3@lsu.edu

Abstract: Adiabatic logic has been proposed as a method for drastically reducing power consumption in specialized low-power circuits. They often require specialized clock drivers that also function as the main power supply, in contrast to standard CMOS logic, and these power clocks are often a point of difficulty in the design process. A novel, stepwise charging driver circuit for four-phase adiabatic logic is proposed and validated through a simulation study. The proposed circuit consists of two identical driver circuits each driving two opposite adiabatic logic phases. Its performance relative to ideal step-charging and a standard CMOS across mismatched phase loads is analyzed, and new best practices are established. It is compared to a reference circuit consisting of one driver circuit for each phase along with a paired on-chip tank capacitor. The proposed driver uses opposite logic phases to act as the tank capacitor for each other in a "self-tanked" fashion. Each circuit was simulated in 15 nm FinFET across a variety of frequencies for an arbitrary logic operation. Both circuits showed comparable power consumption at all frequencies tested, yet the proposed driver uses fewer transistors and control signals and eliminates the explicit tank capacitors entirely, vastly reducing circuit area, complexity, and development time.

Keywords: adiabatic logic; stepwise charging; tank capacitor; FinFET

1. Introduction

Adiabatic logic, a novel approach in low-power digital circuit design, has been proposed as a method to increase the energy efficiency of digital circuits, especially in energy constrained applications such as IoT devices and other embedded systems. By employing adiabatic logic, these energy-constrained applications can achieve notable improvements in energy efficiency, allowing for prolonged battery life, reduced power consumption, and enhanced overall performance. The main principle by which an adiabatic logic circuit differs from a typical CMOS logic circuit lies in the differing methods of charging or discharging a load capacitance in the system through careful control of the power supply [1]. By smoothly ramping between different target voltages (i.e., a logic high or a logic low), losses caused by charging the load capacitance of each logic gate can be reduced. Often, this can require complex resonant circuits adding to design time and reducing manufacturability [2–5]. Alternatively, stepwise charging can be used to find a middle ground between typical CMOS logic power consumption and ideal adiabatic logic operation [6–10]. Instead of smoothly transitioning between targets as in ideal adiabatic logic or sharply jumping between a logic high and a logic low, step-charging transitions between multiple intermediate voltage levels. Step-charging energy consumption approaches that of ideal adiabatic charging as the number of steps increases. These step-charging circuits can require multiple supply voltage levels or large on-chip tank capacitors in their design. This work aims to reduce design time and chip area by use of a redesigned step-charging driver circuit that eliminates the need for tank capacitors.

2. Adiabatic Logic

Consider a typical CMOS inverter with a load capacitance C as shown in Figure 1. During a charging event, an amount of charge $Q = CV_{DD}$ travels from the power supply to the load capacitance through the pull-up PFET. Now, the voltage across the load is equal to the supply voltage V_{DD} and the capacitor stores an amount of energy $E_{stored} = \frac{1}{2}CV_{DD}^2$, but an amount of energy equal to $E_{total} = QV_{DD} = CV_{DD}^2$ leaves the power supply. The difference is lost in the upper transistor (PFET). Similarly, it can be easily seen that during a discharging event, all the charge stored in the capacitor is dumped to ground through the lower transistor (NFET), and all the stored energy is lost in the NFET. Charging and discharging events both consume an amount of energy, $E_{lost} = \frac{1}{2}CV_{DD}^2$, regardless of any properties of the NFETs or PFETs that comprise the logic gates.

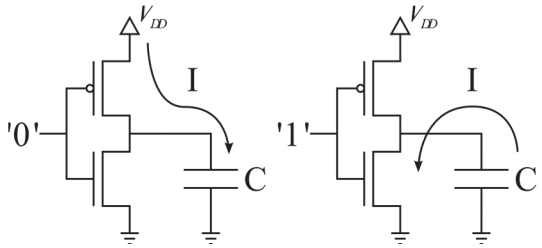


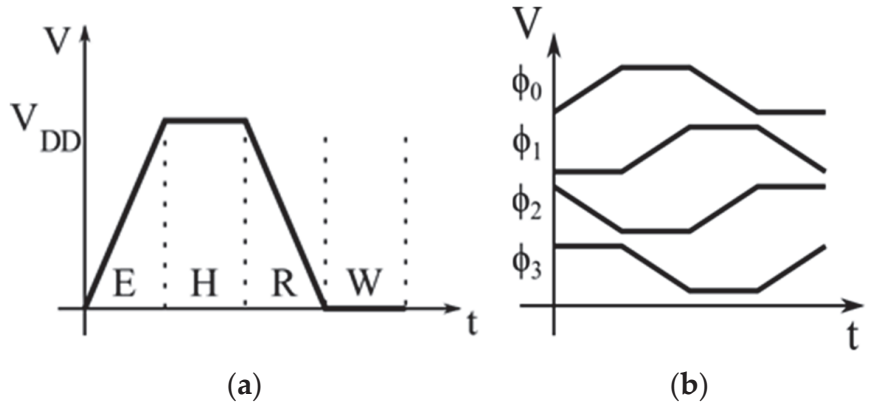
Figure 1. CMOS inverter circuit showing the current path during both a charging and discharging event. The capacitor C represents the load created by attaching further logic gates to the inverter.

By contrast, during adiabatic charging of the same system, the supply voltage, v_S, is not static but slowly ramps from 0 V to V_{DD} over a time T. In doing so, the voltage across the load capacitance can be modeled as approximately following the supply voltage, that is, $v_C \approx v_S = \frac{V_{DD}}{T}t$. In doing so, the overall energy dissipated in charging the capacitor over this time period can be found:

$$E_{lost} = \frac{RC}{T}CV_{DD}^2 \tag{1}$$

where R is the on-resistance of the PFET PMOS channel during charging. Through this method, less than $\frac{1}{2}CV_{DD}^2$ energy can be lost during a charging event through careful control of device parameters and charging time.

There is a variety of circuit architectures that implement this adiabatic charging method, with a common application being in different four-phase adiabatic logic families such as "efficient charge recovery logic" (ECRL) [11] and "positive feedback adiabatic logic" (PFAL) [12]. In both families, the ideal power supply consists of a trapezoidal power clock, as illustrated in Figure 2a. Four separate phases occur in the power clock: evaluate, hold, recover, and wait. During the evaluate phase, the supply voltage follows the ramp illustrated earlier and allows for the logic gate to perform its computation. The hold phase holds the output logic values for any successor logic to evaluate its own operation. Recover allows for the charge in the load capacitance to return to the power supply and the wait phase provides symmetry for smooth operation. Four different power clocks are required to implement an ECRL or PFAL system, staggered as shown in Figure 2b, with the evaluate phase being in line with its predecessor's hold phase. Logic is thus chained together as in Figure 3, with each gate passing data along in a pipeline.



(**a**) (**b**)

Figure 2. Ideal trapezoidal power clocks for adiabatic logic. (**a**) Power clock showing relative voltage levels during each phase of operation: evaluate, hold, recover, and wait; (**b**) four staggered power clocks used in four-phase adiabatic logic, each offset 90 degrees such that the evaluate phase of one clock is during the hold phase of its predecessor.

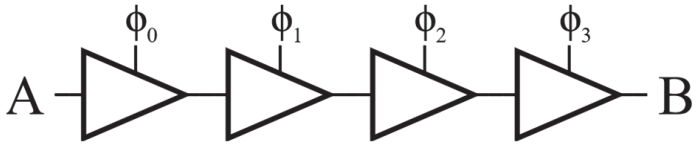


Figure 3. Four successive buffers implemented in four-phase adiabatic logic, buffering a logical value from point A to B, each taking a different power clock in sequence.

3. Stepwise Charging

As mentioned previously, for PFAL and ECRL, generation of the ideal trapezoidal waveform is quite difficult and can require carefully tuned resonant circuits. To this end, alternative methods consisting of multiple steps to intermediate voltages in the charging process to mimic the smooth ramp up have been investigated [6–10]. The simplest of these is the two-step charging case illustrated in Figure 4. A switch brings the load capacitance to half the supply voltage during the evaluation phase, dissipating $\frac{1}{8}C_L V_{DD}^2$, followed by a second switch to V_{DD} and dissipating another $\frac{1}{8}C_L V_{DD}^2$. While nowhere near as efficient as the ideal trapezoidal behavior in (1), the two-step case results in only $\frac{1}{4}C_L V_{DD}^2$ being lost in each charge or discharge cycle, half that of conventional CMOS.

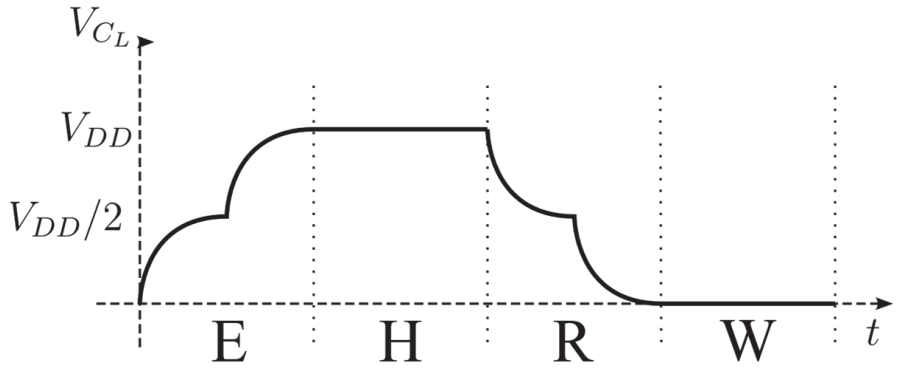


Figure 4. Stepwise charging of a load capacitance using two steps, each contributing half the charge needed to reach supply voltage. The four phases used in this clock match those of the trapezoidal clock of Figure 2a. The exponential behavior of charging and discharging the load capacitance is exaggerated for illustration.

To implement step-charging, specific driver circuits are used, as demonstrated in [7] and shown in Figure 5a. These consist of a large tank capacitance C_T and pass-transistors for moving the required charge around. This driver circuit is controlled by a finite state machine of conventional CMOS logic with an operating frequency higher than that of the driven adiabatic logic (with the goal that the power saved by using adiabatic logic is not outweighed by the power consumed by the driver circuit and control logic). During the beginning of the evaluate and recover phases of the power clock the transmission gate controlled by S_1 levels the voltage between C_L and C_T, ideally bringing both their voltages to $\frac{V_{DD}}{2}$. During the latter half of these phases, either S_0 or S_2 drives C_L to the supply voltage or ground, respectively. The control signal timing for the step driver can be seen in Figure 5b.

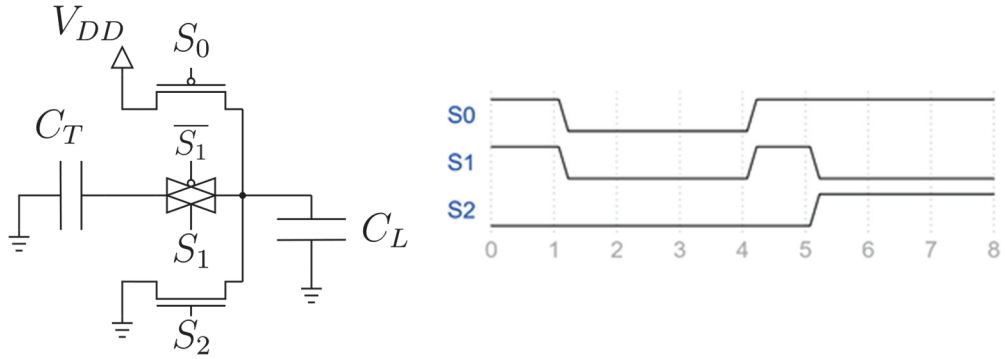


Figure 5. Traditional stepwise charging driver circuit. (**a**) The driver circuit; different pass transistors control the flow of charge to the power clock node represented by capacitor C_L. The tank capacitor C_T sources or sinks charge during the middle of evaluate and recover phases, respectively. (**b**) Control signal timing for each of the pass transistors.

One of these driver circuits and companion FSM is required for each power clock and the tank capacitance must be tuned to match the load carried by that specific clock's logic, with a larger tank capacitance allowing the step voltage to be closer to half the supply, improving efficiency, though with more area overhead. In [7], it was found that a tank capacitance equal to ten times the load capacitance was a good rule of thumb for proper logical operation and circuit efficiency before hitting diminishing returns. In practice, this requires careful investigation of the load represented by each phase of logic and an additional area overhead needed to implement the large tank capacitance. A total of 4 tank capacitances, 12 switching devices, and 12 different control signals are thus required to implement this system for any four-phase adiabatic logic.

4. Improved Step-Charging Circuit

An improved step-charging circuit can be implemented using the circuit shown in Figure 6a. In contrast to the reference work, only two of these circuits are needed, one for each pair of opposite logic phases. Thus, only 10 switching devices and control signals are required, and importantly, no explicit tank capacitors are required. It achieves this by using the load capacitance, C_n, of phase ϕ_n as the tank capacitor for its opposite phase ϕ_{n+2} and vice versa in a "self-tanked" fashion.

When one phase is dropping in its first step down from V_{DD}, this charge is used to step up the opposite phase from ground. If the load capacitances for each phase are equal, then any charge will be distributed equally, the step voltage will be equal to $\frac{V_{DD}}{2}$, and the energy consumed remains at half of that of a conventional CMOS. If the load capacitances are not equal (a more likely scenario), then the load capacitances for each phase can be defined as such: C_L is the nominal CMOS load and will correspond to the phase with the lower load and C_H will correspond to the phase with the higher load. $C_H = \alpha C_L$ and

$\alpha \geq 1$, α representing the factor by which one phase's load is larger than the other. Note that the order of these two loads does not matter, as a full cycle of their power clocks will be considered. Due to charge conservation between the mismatched capacitances, two different step voltages occur at different points in the power clock:

$$V_{step-A} = \frac{1}{\alpha+1} V_{DD} \qquad and \qquad V_{step-B} = \frac{\alpha}{\alpha+1} V_{DD} \tag{2}$$

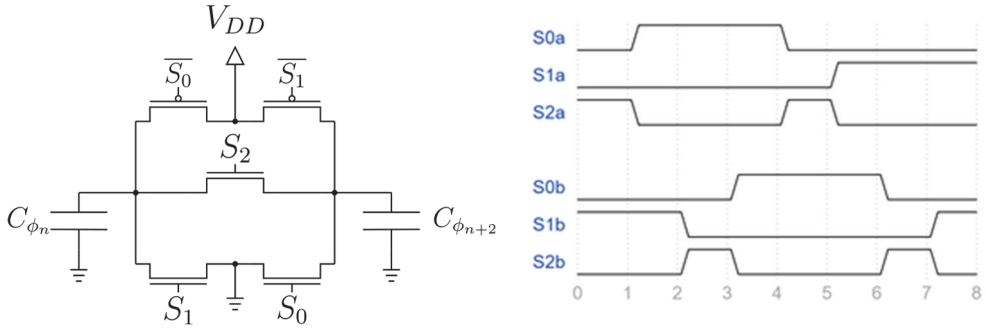


Figure 6. Improved stepwise charging driver circuit. (**a**) The driver circuit; different pass transistors control the flow of charge between to opposite phases of the adiabatic logic, represented here by their loads and relative offset from each other: C_{ϕ_n} and $C_{\phi_{n+2}}$; (**b**) Control signal timing for each of the pass transistors, separated into 'a' control signals for ϕ_0 and ϕ_2, and 'b' signals for ϕ_1 and ϕ_3.

ϕ_L, the clock corresponding to the lower load, will attain $\frac{\alpha}{\alpha+1} V_{DD}$ on its way to charging to V_{DD}, while lowering to $\frac{1}{\alpha+1} V_{DD}$ on its descent to 0 V. ϕ_H will do just the opposite on its way up and down. Now, a charging event and the energy lost for ϕ_L can be decomposed into its two steps:

$$E_{L,charging} = \frac{1}{2} C_L \left(\frac{\alpha}{\alpha+1} V_{DD} \right)^2 + \frac{1}{2} C_L \left(V_{DD} - \frac{\alpha}{\alpha+1} V_{DD} \right)^2 \tag{3}$$

$$E_{L,charging} = \frac{1}{2} C_L V_{DD}^2 \left[1 - 2\frac{\alpha}{\alpha+1} + 2\left(\frac{\alpha}{\alpha+1} \right)^2 \right]. \tag{4}$$

A discharge event and its energy can be decomposed in the same way:

$$E_{L,discharging} = \frac{1}{2} C_L V_{DD}^2 \left[1 - 2\frac{1}{\alpha+1} + 2\left(\frac{1}{\alpha+1} \right)^2 \right]. \tag{5}$$

Combined, the overall energy lost during a complete cycle of ϕ_L can be shown as follows:

$$E_L = \frac{1}{2} C_L V_{DD}^2 \cdot 2\frac{\alpha^2+1}{(\alpha+1)^2}. \tag{6}$$

It is at this moment that two interesting observations can be made. Setting $\alpha = 1$, results in the case with no mismatch and an overall energy loss of $\frac{1}{2} C_L V_{DD}^2$ for both a single charge and discharge, congruent with the results stated in the goals of stepwise charging (note that $E_{CMOS} = C_L V_{DD}^2$ when combining a single charge and discharge). Additionally, taking the limit as $\alpha \to \infty$ results in $E_L = C_L V_{DD}^2$, again, the standard CMOS result. This factor can be thought of as corresponding to a higher load capacitance whose voltage cannot be changed no matter how much charge is taken out of it, a $V_{step-A} = 0\ V$, and a $V_{step-B} = V_{DD}$. Thus, the higher capacitance acts as a static voltage source, just like a CMOS power supply.

The same process of finding energy loss can be performed for C_H as well, remembering to factor in α for the load capacitance being a higher value, resulting in the following:

$$E_H = \frac{1}{2} C_L V_{DD}^2 \cdot 2\alpha \frac{\alpha^2 + 1}{(\alpha + 1)^2}. \tag{7}$$

Again, this can be checked for congruence to the no mismatch case by setting $\alpha = 1$, and indeed does result in half the energy of standard CMOS charging. Combining both (6) and (7), a combined energy loss for the two mismatched phases can be determined:

$$E_H + E_L = C_L V_{DD}^2 \cdot \left[\alpha \frac{\alpha^2 + 1}{(\alpha + 1)^2} + \frac{\alpha^2 + 1}{(\alpha + 1)^2} \right] = C_L V_{DD}^2 \left[\frac{\alpha^2 + 1}{\alpha + 1} \right]. \tag{8}$$

Similarly, the energy for a standard CMOS circuit going through both a charge and discharge cycle with two different loads can also be determined:

$$E_{CMOS} = E_{H,CMOS} + E_{L,CMOS} = \alpha C_L V_{DD}^2 + C_L V_{DD}^2 = (\alpha + 1) C_L V_{DD}^2. \tag{9}$$

An energy savings factor can then be defined as the ratio between (8) and (9):

$$ESF\% = \frac{E_H + E_L}{E_{H,CMOS} + E_{L,CMOS}} = \frac{\alpha^2 + 1}{(\alpha + 1)^2}. \tag{10}$$

For the matched $\alpha = 1$ case, this again shows that the step-charging circuit will use half the energy of a standard CMOS circuit. Even if the higher load in a phase is twice that of the lower, this still results in an energy consumption 55% that of standard CMOS.

It may seem prudent at this point to add additional compensation capacitance to the lower load phase to force $C_H = C_L$ and $\alpha = 1$. However, doing so changes the combined energy of the step-charging phases to the following:

$$E_{H,compensated} + E_{L,compensated} = \alpha C_L V_{DD}^2. \tag{11}$$

This can be compared to the unadjusted energy in (8) to determine how much compensation adjusts the energy used:

$$Compensation\ \%\ Change = \frac{E_{H,compensated} + E_{L,compensated}}{E_H + E_L} = \frac{\alpha^2 + \alpha}{\alpha^2 + 1}. \tag{12}$$

For $\alpha > 1$, this always results in more energy being used in the compensated case vs. the uncompensated case in (10). Therefore, there is no benefit to adding capacitance to the lower load to account for a mismatch between phases.

5. Implementation and Simulation

A test circuit was designed using the FreePDK15 15 nm FinFET PDK provided by North Carolina State University [13].

This circuit consisted of two of the step-charging driver circuits depicted in Figure 6a as well as an example test logic circuit (Figure 7) implemented in ECRL using the methods laid out in [11]. Buffers were interspersed to add additional load to the example circuit as well as to keep signals properly in-phase as they are pipelined through the circuit in accordance with ECRL design principles. Control signals for the step-driver circuits were defined using idealized voltage sources and follow the timing of Figure 6b.

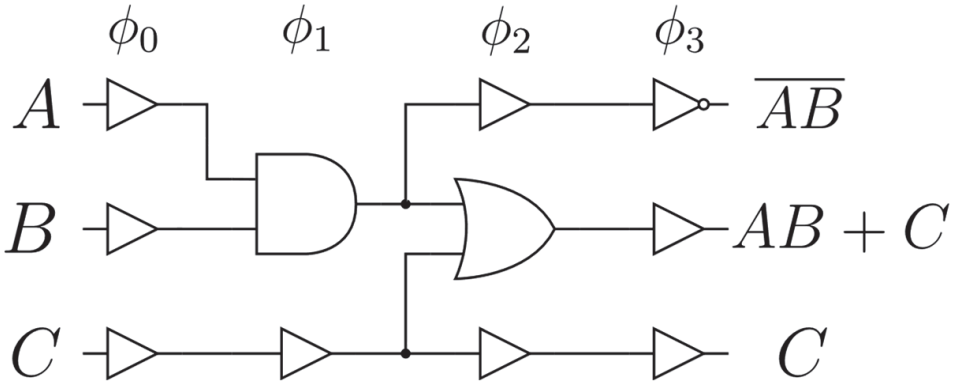


Figure 7. Logic circuit used to test the power consumption of the stepwise charging driver circuits. Each combination of logic signals A, B, and C were tested. Each gate was implemented in ECRL, and buffers were included to ensure proper timing of signal propagation through the circuit. Each logic gate used minimized FinFETs as allowed for by the PDK with two fins per device.

All FinFETs used in the simulation were of minimum sizing, as detailed in the PDK with two fins used per device. V_{DD} was set to 0.8 V.

The A, B, and C data signals depicted in Figure 7 merely count up from a binary 0 with A being the least significant bit and C being the most significant, allowing for all logical results to be evaluated for the average power consumption. All results are available after one ECRL period after being applied due to the inherent pipelining of ECRL.

The proposed system was compared to the reference driver circuit in Figure 5. First an implementation of the reference driver circuit was designed using minimum sized FinFET parameters and two fins per device. Control signals were also created using ideal voltage sources. This is to keep consistency with the proposed driver implementation. Then, a sweep of the tank capacitor for each driver was performed to confirm the findings laid out in [7], each of the four drivers receiving identical capacitance values. The reference drivers were attached to each clock phase for the test logic circuit and driven to result in an adiabatic logic frequency of 250 MHz. Average power consumption was then computed for these simulations. These results can be seen in Figure 8. After a tank capacitance of 20 fF, savings in power suffers from significant diminishing returns. Therefore, 20 fF was chosen as the baseline for tank capacitor in the reference driver circuit, with 100 fF being used as an extreme to compare efficiency with the proposed driver circuit. In all reference driver simulations, tank capacitors were pre-charged to 0.4 V in order to model the circuit having reach its steady state of operation, with the goal being to mimic the "few cycles to settle" requirement laid out in [7]. Simulations for each circuit were then performed at a range of adiabatic system frequencies (100 MHz to 1 GHz), and power consumption for each system (proposed, reference at 20 fF, and reference at 100 fF) was calculated.

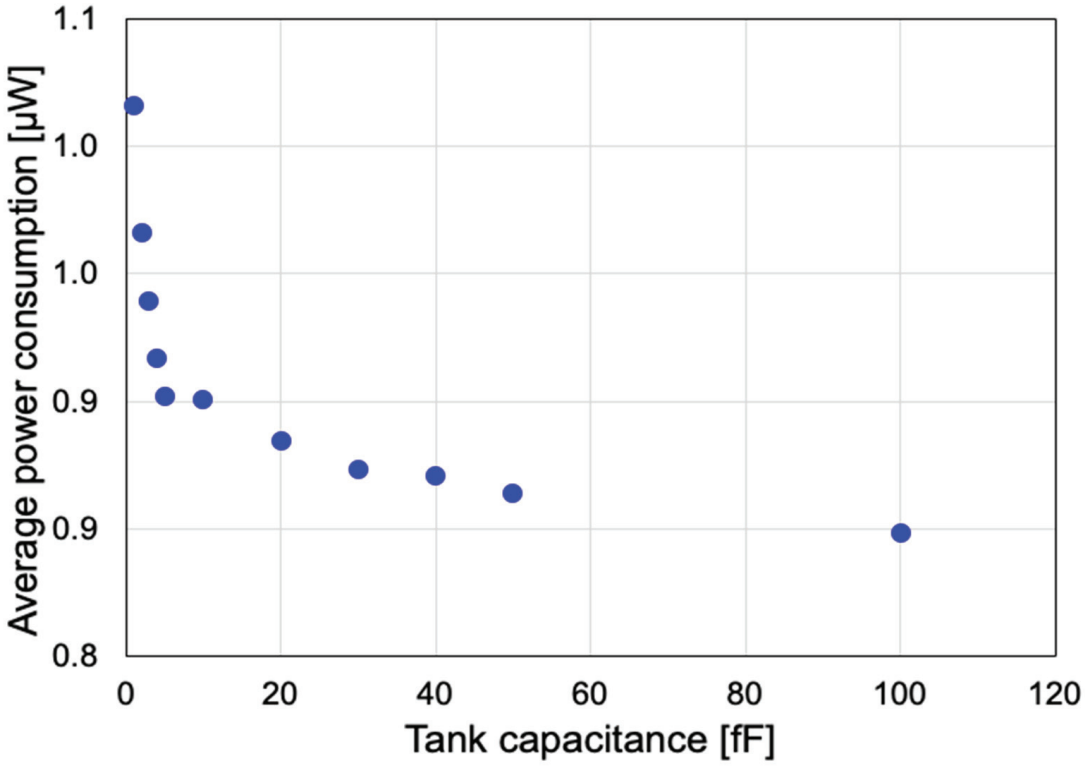


Figure 8. Tank capacitor sweep at 250 MHz operation of the reference driver and test logic circuit. After about 20 fF of tank capacitance on each phase, the circuit hits diminishing returns in regard to power savings.

6. Analysis

All test logic circuits adequately performed the logical operations required under their respective drivers, confirming that both methods are sufficient for proper logical operation. Power consumption across the frequency range for each driver is shown in Figure 9. As can be seen, across the majority of the frequency range, both the 20 fF reference driver, the 100 fF reference driver, and the proposed driver perform within 1% of each other with regard to power consumption. Lower frequencies slightly deviate from each other as these ranges are more dominated by leakage power rather than the dynamic switching power. Additionally, when observing the waveforms of the clocks in Figure 10 for the proposed driver, the mismatch in load between the phases can be seen. ϕ_0 and ϕ_2 are relatively well balanced, and their step voltages do not deviate far from $\frac{V_{DD}}{2}$ during either charging or discharging. This can be explained by the relatively even load for each phase based on the logic used in Figure 7. ϕ_1 and ϕ_3, however, show a deviation to about 480 mV at the worst in a given charge or discharge cycle. Again, by looking at Figure 7, it is easy to see that the load seen by ϕ_3 is the lowest in the circuit, as the outputs of logic gates driven by ϕ_3 do not drive any other gates, only their self-loading is present. Adding dummy load to clock 3 in the form of capacitor connected NFETs allowed for the step voltage to reach closer to the ideal of $\frac{V_{DD}}{2}$, in agreement with (2) and the reduction in α to be closer to 1, but overall increased the power consumed by the circuit in agreement with the findings in (11) and (12).

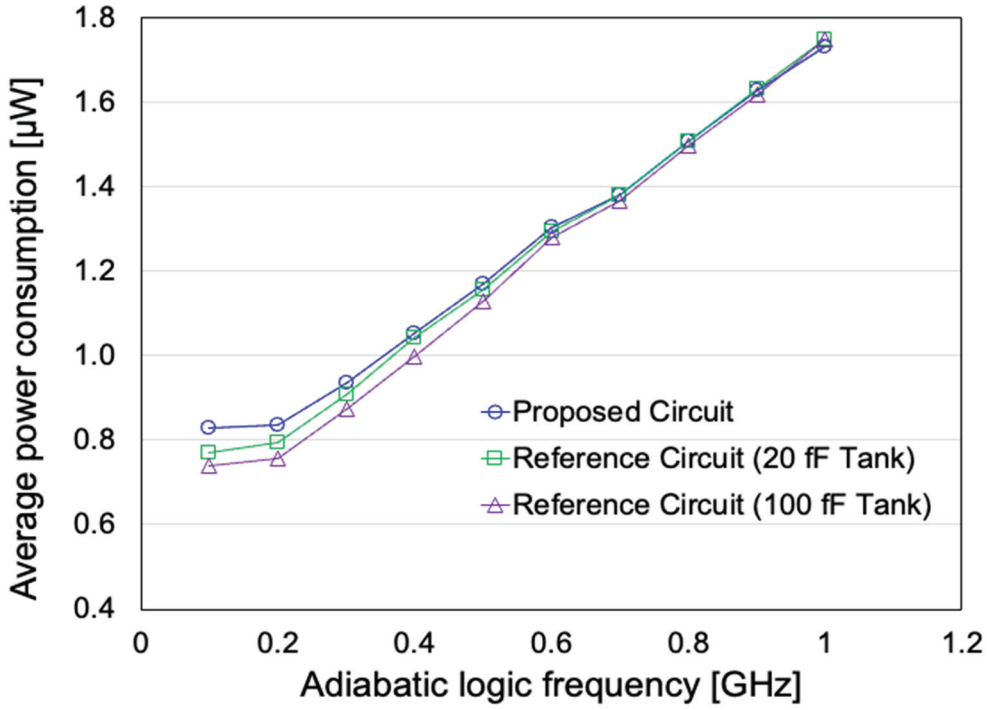


Figure 9. Comparison of power consumption for each circuit under test at different adiabatic logic frequencies. The proposed stepwise charging driver circuit is compared to the reference work at with both 20 fF and 100 fF tank capacitors. During low-frequency operation, power is largely dominated by leakage current and little change in power consumption occurs with a change in frequency. As frequency increases, power scales linearly. Higher frequencies show power consumptions within 1% of each other for each circuit under test.

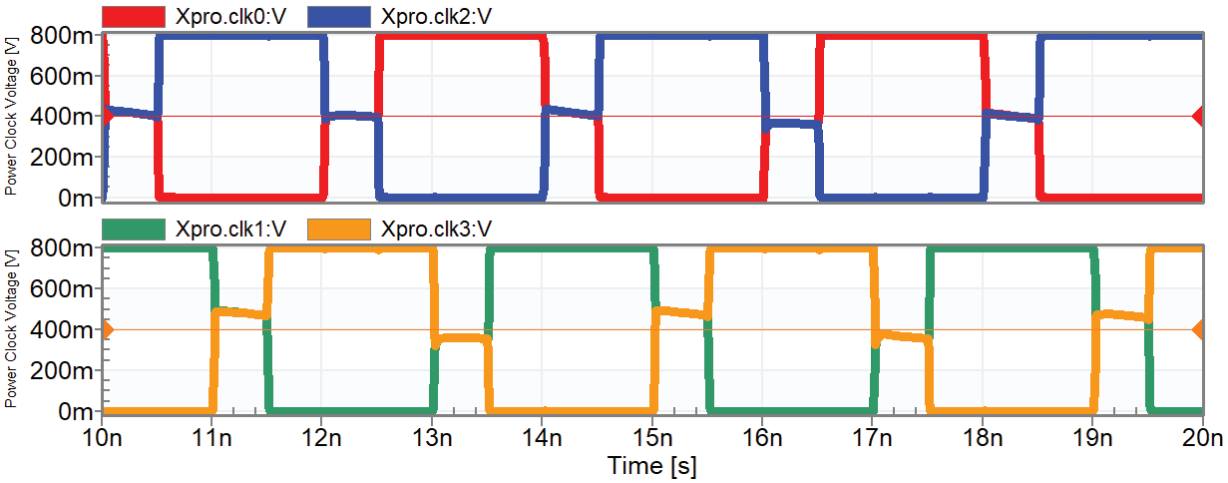


Figure 10. Power clock waveforms for the proposed stepwise charging driver circuit at 500 MHz adiabatic logic operation. **Upper plot:** ϕ_0 (red) and ϕ_2 (blue) can be seen to have relatively equal load as both their step voltages follow closely to half the supply voltage. **Lower plot:** ϕ_1 (green) and ϕ_3 (orange) show mismatched load as their step voltages deviate from half the supply. An analysis of the unloaded outputs of ϕ_3 in Figure 7 show this to be the case, with only the self-loading of the logic gates present for that power clock.

7. Conclusions

A novel stepwise charging driver circuit for four-phase adiabatic logic was designed and analyzed for power consumption compared to a standard CMOS and to a reference

step driver design. A series of simulations was performed using the FreePDK15 15 nm FinFET process comparing the two driver circuits. The proposed and reference drivers were both tasked with driving the same arbitrary logic function and both logical accuracy and power consumption were analyzed. These simulations were performed across a logical frequency range of 100 MHz to 1 GHz. Both drivers were able to drive the logic circuits for correct logical operation for each frequency tested. For the majority of the frequency range observed, both proposed and reference driver circuits operated within 1% power consumption of each other for the performance of adiabatic logic operations. However, the proposed driver circuit eliminates six transistors, six control signals, and four on-chip tank capacitors, leading to reduced circuit area requirements for the same circuit operation and efficiency.

Author Contributions: Conceptualization, W.M.; methodology, W.M.; software, W.M.; validation, W.M. and J.-W.C.; formal analysis, W.M.; investigation, W.M.; resources, W.M.; data curation, W.M. and J.-W.C.; writing—original draft preparation, W.M.; writing—review and editing, W.M. and J.-W.C.; visualization, W.M. and J.-W.C.; supervision, J.-W.C.; project administration, W.M. and J.-W.C.; funding acquisition, J.-W.C. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: Dataset available on request from the authors.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Athas, W.; Svensson, L.; Koller, J. Low-Power Digital Systems Based on Adiabatic-Switching Principles. *IEEE Trans. Very Large Scale Integr. Syst.* **1994**, *2*, 398–407. [CrossRef]
2. Kuttappa, R.; Filippini, L.; Sica, N.; Taskin, B. Scalable Resonant power Clock Generation for Adiabatic Logic Design. In Proceedings of the IEEE Computer Society Annual Symposium on VLSI, Tampa, FL, USA, 7–9 July 2021.
3. Kuttappa, R.; Khoa, S.; Filippini, L.; Pano, V.; Taskin, B. Comprehensive Low Power Adiabatic Circuit Design with Resonant Power Clocking. In Proceedings of the 2020 IEEE International Symposium on Circuits and Systems, Seville, Spain, 12–14 October 2020.
4. Frank, M.; Brocato, R.; Conte, T.; Hsia, A.; Jain, A.; Missert, N.; Shukla, K.; Tierney, B. Special Session: Exploring the Ultimate Limits of Adiabatic Circuits. In Proceedings of the IEEE 38th International Conference on Computer Design, Hartford, CT, USA, 18–21 October 2020.
5. Jeanniot, N.; Pillonnet, G.; Nouet, P.; Azemard, N.; Todri-Sanial, A. Synchronised 4-Phase Resonant Power Clock Supply for Energy Efficient Adiabatic Logic. In Proceedings of the 2017 IEEE International Conference on Rebotting Computing, Washington, DC, USA, 8–9 November 2017.
6. Koller, J.G.; Svensson, L. Driving a capacitive load without dissipating fCV2. In Proceedings of the IEEE Symposium on Low Power Electronics, San Diego, CA, USA, 10–12 October 1994.
7. Raghav, H.S.; Bartlett, V.A.; Kale, I. Energy efficiency of 2-step charging power-clock for adiabatic logic. In Proceedings of the 2016 26th International Workshop on Power and Timing Modeling, Optimization and Simulation, Bremen, Germany, 21–23 September 2016.
8. Chernichenko, D.; Kushnerov, A.; Ben-Yaakov, S. Adiabatic charging of capacitors by Switched Capacitor Converters with multiple target voltages. In Proceedings of the 2012 IEEE 27th Convention of Electrical and Electronics Engineers in Israel, Eilat, Israel, 14–17 November 2012.
9. Khorami, A.; Saeidi, R.; Sharifkhani, M. An Analysis of Stepwise Adiabatic Circuits. In Proceedings of the 28th Iranian Conference on Electrical Engineering, Tabriz, Iran, 4–6 August 2020.
10. Raghav, H.S.; Bartlett, V.; Kale, I. Investigation of stepwise charging circuits for power-clock generation in Adiabatic Logic. In Proceedings of the 2016 12th Conference on Ph.D. Research in Microelectronics and Electronics, Lisbon, Portugal, 27–30 June 2016.
11. Moon, Y.; Jeong, D.-K. An efficient charge recovery logic. *IEEE J. Solid-State Circuits* **1996**, *31*, 514–522. [CrossRef]
12. Vetuli, A.; Pascoli, S.; Reyneri, L. Positive feedback in adiabatic logic. *Electron Lett.* **1996**, *32*, 1867–1869. [CrossRef]
13. FreePDK15. Available online: https://eda.ncsu.edu/freepdk15/ (accessed on 10 January 2024).

Journal of
Low Power Electronics and Applications

MDPI

Article

0.35 V Subthreshold Bulk-Driven CMOS Second-Generation Current Conveyor

Muhammad Omer Shah, Manfredi Caruso and Salvatore Pennisi *

DIEEI (Dipartimento di Ingegneria Elettrica Elettronica e Informatica), University of Catania, 95125 Catania, Italy; muhammad.shah@phd.unict.it (M.O.S.); manfredicaruso1@gmail.com (M.C.)
* Correspondence: salvatore.pennisi@unict.it; Tel.: +39-095-7382318

Abstract: This study describes a high-performance second-generation Current Conveyor (CCII) operating at 0.35 V and achieving rail-to-rail operation at the Y terminal and class AB current drive at the X and Z terminals. The solution utilizes a low-voltage subthreshold bulk-driven CMOS OTA that was experimentally developed earlier, making systematic use of body terminals to improve small-signal and large-signal performance. The circuit has a high open-loop voltage gain and uses cascoded current mirror topologies, resulting in precise voltage and current transfer with bandwidths of 1.33 MHz and 2.13 MHz, respectively. The CCII offers a linear current drive up to 2.5 μA while consuming a total quiescent current of 2.86 μA (758 nA in the output branches), displaying one the highest figures of merit in terms of current utilization for sub 1 V solutions.

Keywords: bulk-driven; CMOS analog integrated circuits; low-voltage; operational transconductance amplifier

1. Introduction

Bulk-driven (BD) techniques have gained significant attention among circuit designers in recent years [1–5] because they eliminate the threshold voltage limitation when driving MOS field-effect transistor (MOSFET) devices via their bulk (body) terminals. The effectiveness of the BD approach has been particularly evident in implementing Operational Transconductance Amplifiers (OTAs) that function with supply voltages from 400 mV down to 250 mV [6–19]. This approach allows for the widest common-mode input range, nearly providing rail-to-rail limits. Furthermore, it often results in quiescent current consumption of only a few microamperes or less, which is achieved by properly biasing MOSFETs in their sub-threshold region. The above properties meet the rising demand for ultra-low-voltage, ultra-low-power integrated circuits (ICs) in portable, wearable, and implantable electronics [20–23] but also in the Internet of Things and in the automotive field, which require the development of new circuit topologies and design methodologies aimed at preserving the performance characteristics of established CMOS solutions while enhancing input/output voltage swing and reducing the necessary supply voltage, particularly in the analog domain.

In this framework, the second-generation Current Conveyor, CCII, is a versatile three-terminal (namely, Y, X, and Z terminals) block that provides distinctive performance as it brings together voltage-mode processing characteristics (the voltage follower action between the Y and X terminals) with current-mode ones (the current follower action between X and Z terminals). CCIIs have indeed been used for active filter implementation and are found to be building blocks of transimpedance and current feedback operational amplifiers, voltage, and current operational amplifiers [24–27].

A comprehensive review of the recent literature reveals that numerous publications explore novel CCII implementations with low-voltage and low-power capabilities that also exploit body-driven and subthreshold techniques to attain rail-to-rail performance [28–33]. In this paper, we present an alternative high-accuracy body-driven CCII solution supplied

from 0.35 V and with a 2.86 μA total quiescent current (758 nA in the two output branches). Among the most relevant performances, thanks to the high open-loop gain and exploitation of cascoded current mirror topologies, the circuit provides accurate voltage (Y to X) and current (X to Z) transfers with a −3 dB frequency of 1.33 MHz and 2.13 MHz, respectively, and with an efficient current drive capability of around 2.5 μA.

Compared to other sub-1V solutions, the proposed design achieves superior current drive efficiency. This metric, defined as the ratio of maximum output current to total quiescent current, is particularly important in targeted battery-operated or even battery-less applications.

The rest of the paper is organized as follows. The presented solution is described in Section 2, where particular focus is directed towards elucidating the primary novel design solutions and fundamental design equations. Section 3 delves into the simulations conducted to assess the proposed solution, while in Section 4 the paper concludes with the authors presenting their findings and drawing conclusions.

2. The Proposed Solution

The proposed solution is depicted in Figure 1 and was derived from the OTA configuration presented by one of the authors in a recently published work that employs MOSFETs in the subthreshold region and strategically leverages the body terminals to enhance small-signal and large-signal performance [19].

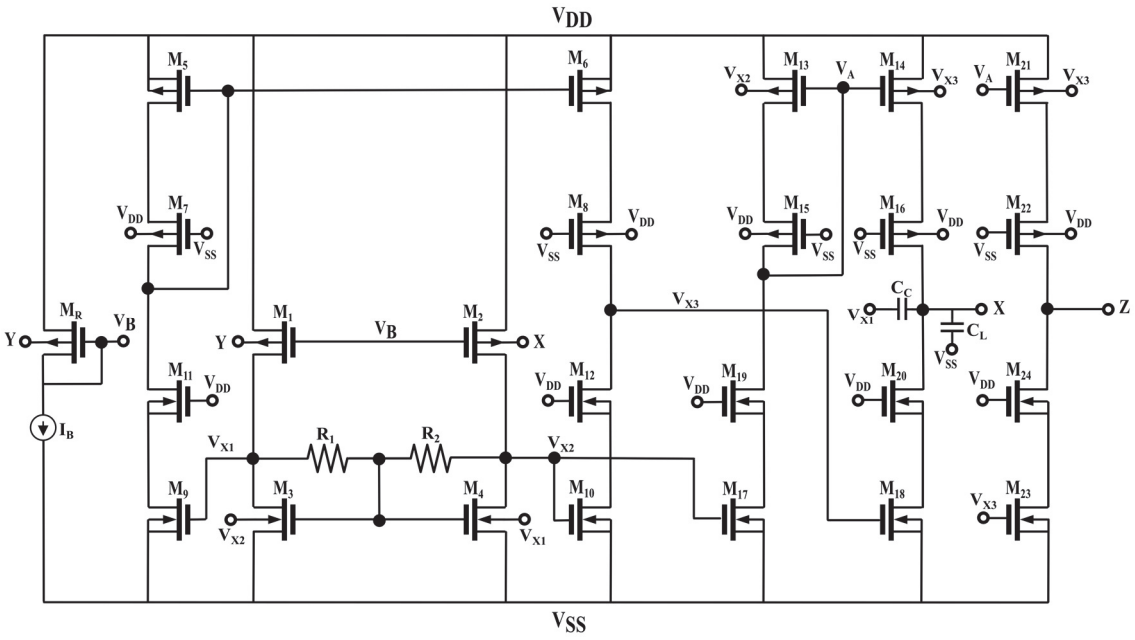


Figure 1. Schematic diagram of the proposed BD CCII.

Our proposed current-conveyor circuit introduces several key modifications compared to the design presented in [19]. Firstly, we introduce a current branch replicating current at terminal X in terminal Z. Secondly, we remove the Slew-Rate Enhancer section of [19] to eliminate nonlinearities inherent to this highly nonlinear circuit. Finally, we employ extensive transistor cascoding to achieve superior DC and AC matching, while also optimizing loop gain and the equivalent resistance at terminal Z. Moreover, while reference [19] focuses on off-chip, high-drive applications, our CCII is specifically designed for on-chip, low-load capacitance applications. This necessitates a distinct design approach to optimize for these contrasting use cases.

The solution is based on local positive feedback for improved input transconductance which is achieved through the bodies of M_3–M_4, and dynamic threshold voltage control to boost the current drive capability is implemented with the bodies of M_{13}–M_{14}. It is to be

noted that a trade-off among simplicity, current transfer accuracy, linearity, high impedance, and voltage compliance is achieved through supply-biased cascode structures. In other words, all the n-channel (p-channel) cascode transistors have their gates connected to V_{DD} (V_{SS}).

Specifically, the solution is made up of four sections: the BD rail-to-rail input stage (M_1–M_4, R_1–R_2), the second gain stage with a differential-to-single-ended function (M_5–M_{12}) the third noninverting gain stage (M_{13}–M_{20}), and a replica of the output branch (M_{21}–M_{24}) which, working in class AB, mirrors the current from terminal X into terminal Z.

The input stage utilizes transistors M_1 and M_2, forming a minimum-supply tail-less body-driven pair without a dedicated current source transistor. A constant current (I_B) establishes the quiescent current through this pair via the diode-connected transistor M_R (with the body connected to terminal Y). The actual current flowing through M1 and M2 is determined by the mirror ratio $(W/L)_{1,2}/(W/L)_R$, where W and L represent the width and length of the transistors. Due to the virtual short at the input of the OTA ($V_X = V_Y$), these transistors share the same body voltage at DC, resulting in the same threshold voltage.

The active load for the input stage comprises transistors M_3 and M_4, with negative feedback resistors R_1 and R_2 playing a crucial role in amplifying differential signals. This load configuration allows the inherently pseudo-differential pair (M_1 and M_2) to effectively handle differential inputs. Local positive feedback is implemented by connecting the body of M_3 to the drain of M_4 and vice versa, enhancing the overall transconductance of the input stage.

The second stage, designed for high output impedance and for converting differential to single-ended output, consists of transistors M_5–M_{12}. The quiescent current in this stage mirrors the current in the first stage through M_9 and M_{10} because M_3 and M_4 act as diode-connected devices at DC, ensuring no current flows through R_1 and R_2 at DC.

Given that $V_{BS3,4} = V_{GS3,4}$ while $V_{BS9,10} = 0$, the current mirror gain is reduced compared to a conventional current mirror, where this factor equals 1 [19].

The third gain stage, consisting of common-source transistor M_{17} with cascode M_{19} and active loads M_{13}–M_{16} and M_{18}, M_{20}, regulates the X branch's quiescent current through the current mirror gains of $M_{3,4}$ to M_{17}, and of M_{13} to M_{14}. Notably, the pull-down i_X current from M_{18} can exceed the quiescent value, like the pull-up i_X current from M_{14}, although to a lesser extent. In fact, both M_{14} and M_{18} operate in class AB but the positive-going output step responds slower than the negative-going step due to the limited variation of the gate voltage of M_{17} compared to the gate voltage of M_{18}. To address this asymmetry, the gain in the current mirror formed by transistors M_{13}–M_{14} is dynamically adjusted based on the required current level. This is achieved by connecting the body of M_{13} to the drain of M_4 and the body of M_{14} to the drain of M_8 (M_{12}), as shown in Figure 1. This configuration leverages the dependence of the threshold voltage of M_{13} and M_{14} on variations in V_{X2} and V_{X3}, boosting the current mirror gain when the output stage supplies current, as explained in [19].

The output of this stage is tied to the inverting input of the input pair M_1–M_2 providing unity gain configuration through high-gain negative feedback and hence ensuring virtual short between voltages at nodes Y and X.

The current flowing in terminal X through M_{14} and M_{18} is mirrored to terminal Z thanks to the class-AB current mirror made up of transistors M_{21}–M_{24} replicating the branch formed by M_{14}, M_{16}, M_{18}, and M_{20}.

Capacitor C_c provides frequency compensation. Transistor dimensions and other design parameters are summarized in Tables 1 and 2.

Table 1. Transistor dimensions of circuit in Figure 1.

Device	W/L (μm/μm)
M_R, M_1, M_2	34/0.5
M_3, M_4	8/1
M_5, M_6	160/1
M_7, M_8	9/0.5
M_{11}, M_{12}	2/0.5
M_9, M_{10}	32/1
M_{13}	50/0.5
M_{15}	5/0.5
M_{17}	16/1
M_{18}	1.5/0.5
M_{14}, M_{21}	200/0.5
M_{16}, M_{22}	20/0.5
M_{18}, M_{23}	60/2
M_{20}, M_{24}	6/1

Table 2. Other design parameters of circuit in Figure 1.

Param	Value
V_{DD}–V_{SS}	0.35 V
I_B	200 nA
R_1, R_2	250 kΩ
C_C	200 fF
C_L	1 pF

Small-Signal Analysis and Noise

Owing to the negative feedback, the CCII voltage transfer from terminal Y to X is as follows:

$$\frac{V_X}{V_Y} = \frac{1}{1+\frac{1}{T(s)}} \approx \frac{1}{1+\frac{1}{T(0)}} \frac{1}{1+\frac{s}{\omega_{GBW}}} \tag{1}$$

where $T(0)$ is the loop gain $G_{mEQ} r_{oX3} g_{m17} r_{oX}$, in which r_{oX3} and r_{oX} are equivalent resistances at the drain of M_8, M_{12} and M_{16}, M_{20}, respectively, and G_{mEQ} is given by $g_{mb1,2}/(1 - g_{mb3,4} r_{X1,2})$, due to the local positive feedback operated by the bodies of M_3 and M_4, and as detailed in [19]. As usual, ω_{GBW} is given by G_{mEQ}/C_c.

It is seen that the DC value of (1) tends to be 1 for high values of $T(0)$.

The equivalent (closed loop) small signal resistance at terminal X is approximately given by the following equation:

$$r_X \approx \frac{r_{oX}}{T(0)} = \frac{g_{m20} r_{o18} r_{o20} \,//\, g_{m16} r_{o14} r_{016}}{T(0)} \tag{2}$$

and the small signal equivalent resistance at terminal Z is simply as follows:

$$r_Z = g_{m24} r_{o23} r_{024} \,//\, g_{m22} r_{o21} r_{022} \tag{3}$$

The CCII noise performance can be modeled by considering the equivalent input noise voltage of the voltage buffer (v_{nY}, in series to terminal Y) and the equivalent input noise current of the current buffer (i_{nX}, in parallel to terminal X), as shown in Figure 2 [34].

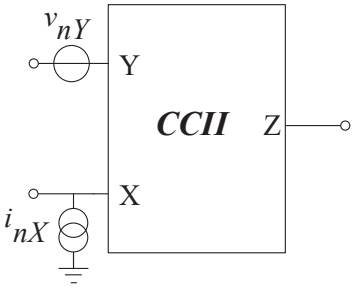


Figure 2. CCII with noise sources.

The equivalent input-referred noise voltage spectral density of the CCII, $\overline{v_{nY}^2}$, accounts for the contribution of transistors M_1 and M_2, that of transistors M_3 and M_4, and of resistors $R_{1,2}$. It can be approximated as in Equation (4), considering only white noise for simplicity [9].

$$\begin{aligned}\overline{v_{nY}^2} &\approx 2\overline{v_{n1,2}^2}\left(\frac{g_{m1,2}}{g_{mb1,2}}\right)^2 + 2\overline{v_{n3,4}^2}\left(\frac{g_{m3,4}}{g_{mb1,2}}\right)^2 + \overline{v_{nR1,2_Y}^2} \\ &= 2\tfrac{2}{3}4kT\frac{1}{g_{mb1,2}}\left(\frac{g_{m1,2}}{g_{mb1,2}} + \frac{g_{m3,4}}{g_{mb1,2}}\right)\Delta f \\ &+4kTR_{1,2}\left(\frac{1}{g_{mb1,2}r_{o1}}\right)^2\left[1+\left(1+\frac{2r_{o1}}{R_{1,2}}\right)^2\right]\Delta f\end{aligned} \tag{4}$$

where $\overline{v_{ni}^2}$ is the gate-referred noise voltage spectral density of the i-th transistor, $\overline{v_{nR1,2Y}^2}$ is the input-referred noise contribution of the resistors R_1 and R_2, r_{o1} is the output resistance of $M_{1,}$ and k and T are the Boltzmann's constant and the absolute temperature.

In the above expression, noise from M_R is neglected since it is seen as a common-mode signal and is rejected. Additionally, the noise from the $R_{1,2}$ results is considered to be negligible by the following equation:

$$(g_{m1,2}+g_{m3,4})r_{o1} \gg \frac{3}{4}\frac{R}{r_{o1}}\left[1+\left(1+\frac{2r_{o1}}{R}\right)^2\right] \tag{5}$$

Unfortunately, (5) is not fulfilled in our design.

The noise current generator, i_{nX}, is equal to the output noise at terminal Z when terminal X is floating. The mean-square value can easily be calculated as follows:

$$\overline{i_{nX}^2} \approx g_{m14}^2\overline{v_{n14}^2} + g_{m21}^2\overline{v_{n21}^2} + g_{m18}^2\overline{v_{n18}^2} + g_{m23}^2\overline{v_{n23}^2} \tag{6}$$

3. Simulation Results

The circuit was designed and simulated using a standard 65 nm CMOS technology supplied by TSMC and accessed through EUROPRACTICE. The supply voltage is 350 mV and the total current consumption is 2.86 µA, with the current in the X and Z output branches equal to 758 nA each.

Figure 3a,b shows the Bode plots, magnitude, and phase, of the open loop gain from the body of M_2 and the drain of M_{16} and M_{20}, with a load capacitance of 1 pF. The DC gain is around 70 dB and the unity gain bandwidth is 600 kHz, with more than 70° phase margin.

The Bode plots of the (closed-loop) voltage transfer (from Y to X) are shown in Figure 4a,b. The low-frequency gain is −4.096 mdB. Montecarlo simulations on 1000 iterations show 68 mdB of standard deviation. The −3 dB frequency is 1.33 MHz.

Additional simulations indicate little changes in the low-frequency gain with different DC levels of the voltage at the Y terminal in the range [20 mV–350 mV]. The same marginal variations are found for different operating temperatures in the range [−40 °C–120 °C].

The Bode plots of the current transfer (from X to Z) are shown in Figure 5a,b. The low-frequency gain is −2.087 mdB. Montecarlo simulations on 1000 iterations show 72.5 mdB of standard deviation. The −3 dB frequency is 2.13 MHz. A 14.1 dB peak is observed at 1.38 MHz.

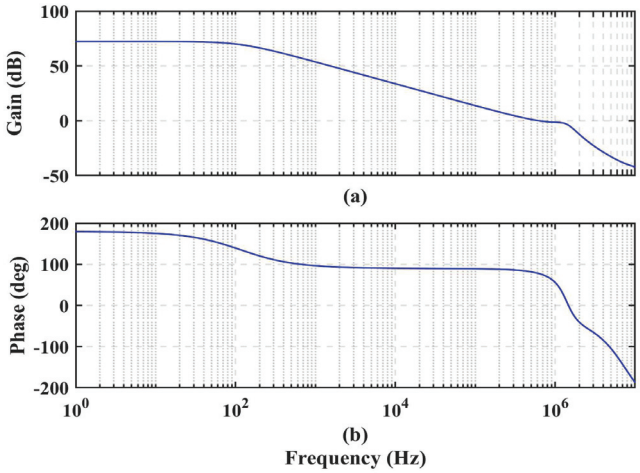


Figure 3. Gain (**a**) and phase (**b**) of open loop Y to X voltage transfer.

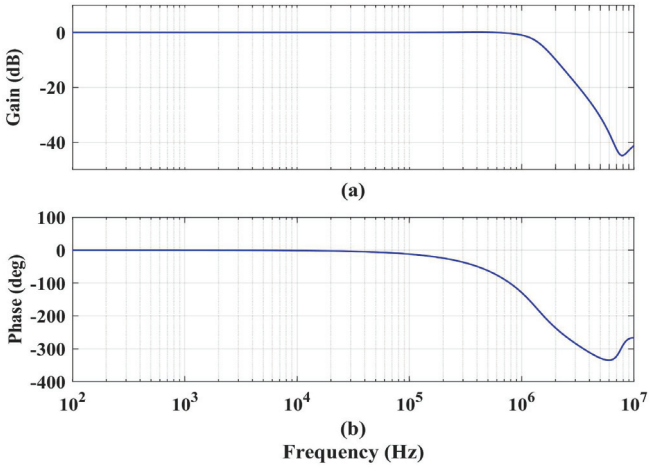


Figure 4. Magnitude (**a**) and phase (**b**) of voltage transfer (Y to X) versus frequency.

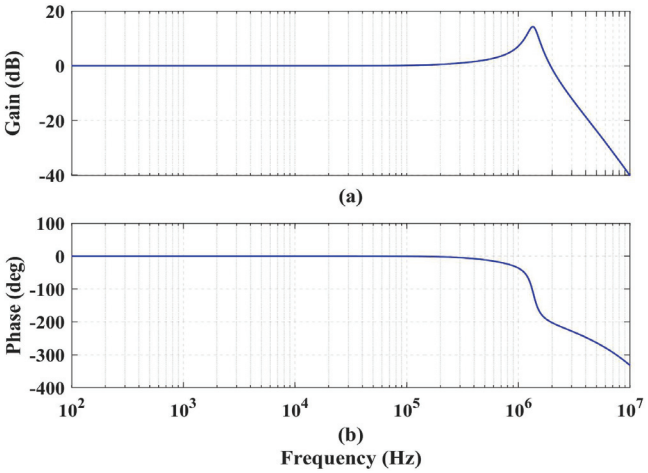


Figure 5. Magnitude (**a**) and phase (**b**) of current transfer (X to Z) versus frequency.

The magnitude of the impedance at terminal Y versus the frequency is shown in Figure 6. It decreases with the frequency while maintaining a substantial high value. For example, it is 118 GΩ at 10 Hz, 150 MΩ at 10 kHz, and 1.6 MΩ at 1 MHz. The parasitic capacitance at this terminal is evaluated to be 96.5 fF.

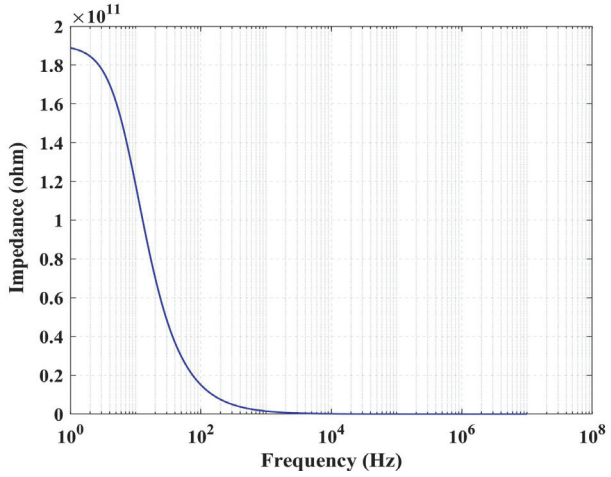


Figure 6. Magnitude of impedance at node Y versus frequency.

Figure 7 shows the input current at terminal Y as a function of V_Y. Under a 175 mV V_Y, the input current is 378.9 fA (with 189 fA flowing into each bulk of M_R and M_1). The maximum input current, for V_Y equal to 0, is 26 pA.

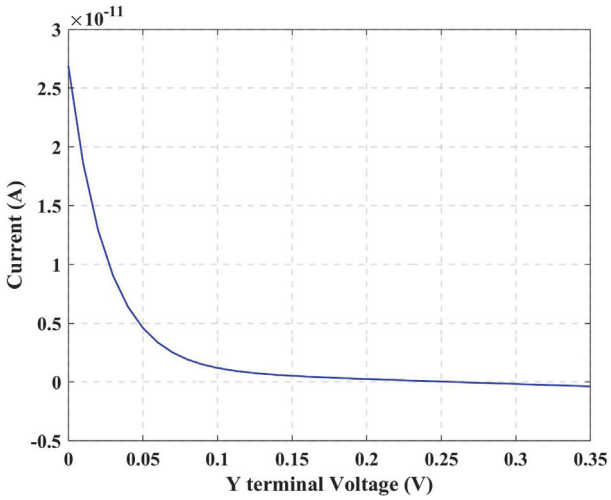


Figure 7. Leakage current at terminal Y versus V_Y.

The magnitude of the impedance at terminal X versus frequency is shown in Figure 8. The low-frequency impedance is 1.8 kΩ. The inductive behavior is apparent because of the peaking of around 520 kΩ at around 1.5 MHz. The magnitude of the impedance at terminal Z versus frequency is shown in Figure 9, and the low-frequency value is 7.46 MΩ.

The DC transfer characteristic of the voltage transfer V_X versus V_Y and of the current transfer I_Z versus I_X are illustrated in Figures 10 and 11, respectively. The rail-to-rail input (Y) and output (X) voltage ranges are apparent from Figure 10. Figure 11 shows that the linear current range is around ±2.5 μA (the quiescent current in the two branches with nodes X and Z is around 758 nA each). The systematic offset current at terminal Z is 1.1 pA.

The Total Harmonic Distortion (THD) of the voltage at terminal X for different input sinusoidal amplitudes and frequencies is shown in Figure 12. It shows that the THD at 1 kHz and 10 kHz equals 1% at about 340 mV_{p-p} and 305 mV_{p-p} input, respectively. The THD of the current at terminal Z (tied to a voltage equal to $V_{DD}/2$) for different input sinusoidal amplitudes and frequencies is shown in Figure 13. It shows that the THD at 1 kHz and 10 kHz equals 1% at about 2.8 μA and 2.7 μA input, respectively.

As discussed in the previous section, two equivalent noise sources are necessary to characterize a CCII. The equivalent noise voltage generator (at terminal Y) and the

equivalent noise current generator (at terminal X) spectral densities are plotted in Figure 14a and Figure 14b, respectively. White noise levels are, respectively, 849 $\frac{nV}{\sqrt{Hz}}$ and 943 $\frac{fA}{\sqrt{Hz}}$. In agreement with (5) and (7), the noise voltage main contributions are due to $R_{1,2}$ (44%), $M_{1,2}$ (27%), and $M_{3,4}$ (16%). The noise current main contributions are due to M_{14}, M_{21}, M_{18}, and M_{23}, giving more than 50% of the total.

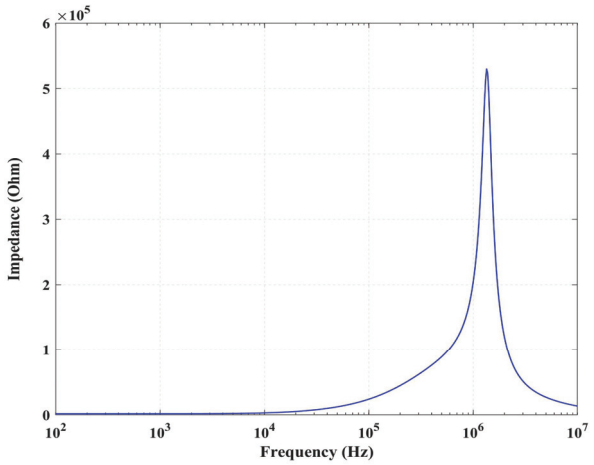


Figure 8. Magnitude of impedance at node X versus frequency.

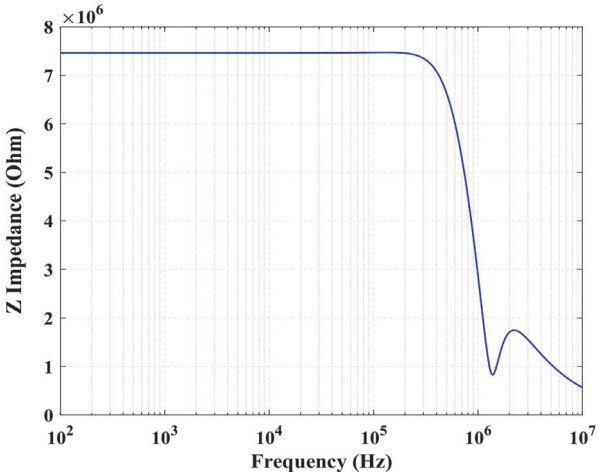


Figure 9. Magnitude of impedance at node Z versus frequency.

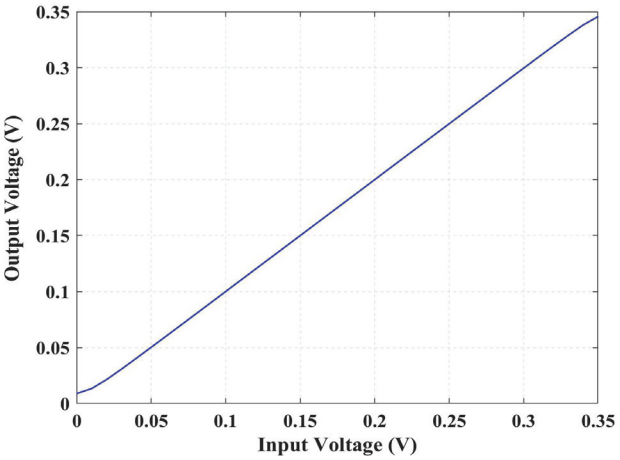


Figure 10. DC voltage transfer characteristic, V_X versus V_Y.

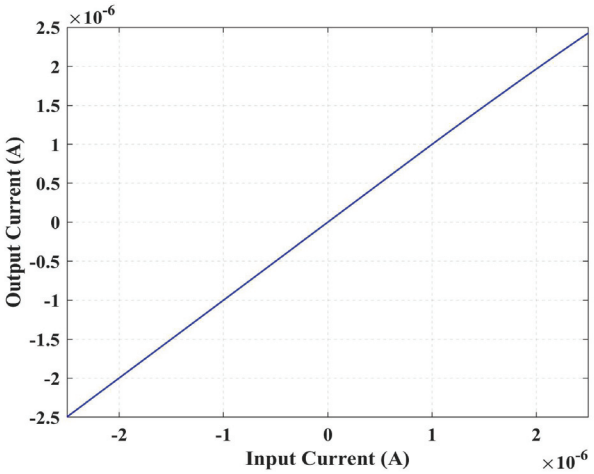


Figure 11. DC current transfer characteristic, I_Z versus I_X.

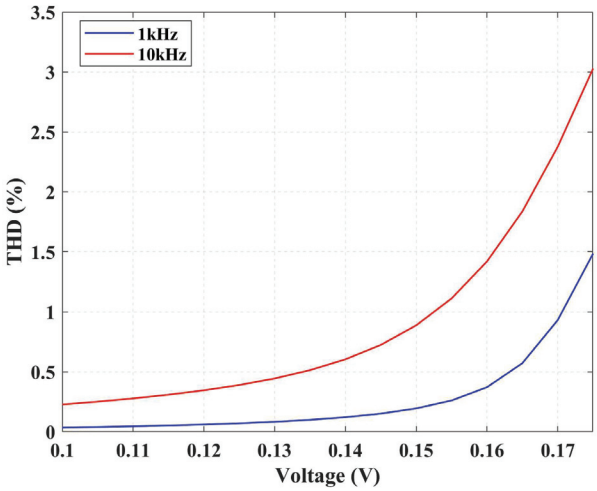


Figure 12. THD of voltage at terminal X versus magnitude of applied input voltage at Y.

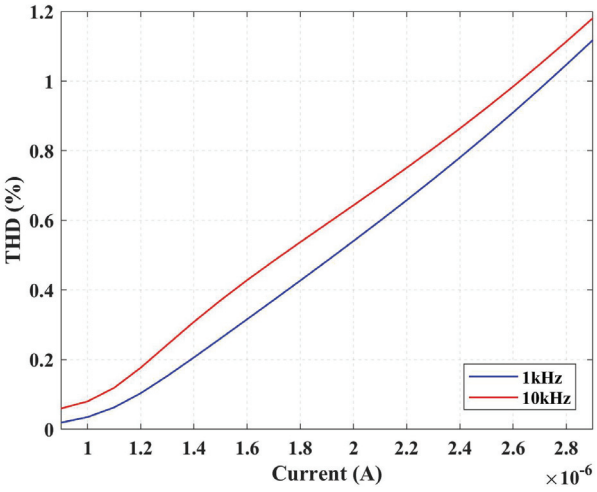


Figure 13. THD of current flowing from terminal Z versus magnitude of applied input current at X.

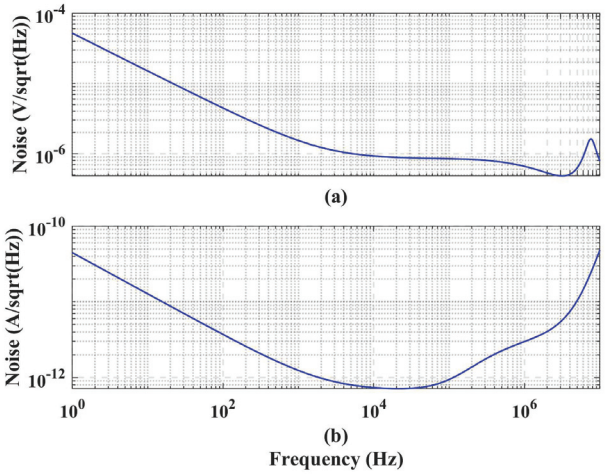


Figure 14. Input noise spectral density: (**a**) noise voltage at terminal Y (**a**) and (**b**) noise current at terminal X.

Table 3 summarizes the performance of the proposed CCII (last column) compared to recent low-voltage, low-power CCII implementations [28–33]. Notably, reference [33] is the only fully fabricated and measured design in the table. While both designs utilize a class AB configuration, reference [33] operates at a supply voltage exceeding 1 V. It can be observed that the trend favors reduced supply voltage and lower DC power consumption. However, maintaining acceptable values of equivalent resistance R_X, −3 dB frequencies for voltage and current transfer, and input current range at node X (which corresponds to the current drive capability at node Z) necessitates a trade-off between these parameters and current consumption. The proposed solution demonstrates good current utilization efficiency which can be defined as the ratio between the maximum input/output linear current ($I_{Xmax,Zmax}$) and the total quiescent current (I_Q). This efficiency metric highlights the proposed CCII's ability to achieve high performance while maintaining low power consumption. Moreover, the −3 dB frequency of the voltage transfer is also good in comparison to the low I_Q utilized.

Table 3. Performance comparison of low voltage CCIIs.

Ref.	[33] *	[28]	[29]	[30]	[31]	[32]		Proposed
Year	2003	2011	2012	2012	2017	2019		2024
Tech. (nm)	350	180	180	180	90	180		65
V_{DD} (V)	1.5	0.8	1	0.5	0.4	0.3	0.5	0.35
I_Q (µA)	173	80	10	60	4.5	63.3×10^{-3}	1.01	2.86
DC Power (µW)	2595	64	10	30	1.8	0.019	0.509	1
Y-Input voltage range (%VDD)	73	95	100	80	n.a.	100	100	97
X-Input current range (µA)	±900	±7	±3	±15	n.a.	±0.024	±0.4	2.5
$I_{Xmax,Zmax}/I_Q$	5.2	8.75×10^{-2}	0.3	0.25	n.a.	0.379	0.396	0.87
R_Y (MΩ)	∞	∞	∞	∞	n.a.	703	664	150 @10 kHz
R_X (Ω)	150	27	42	260	106	56×10^3	3×10^3	1.8×10^3
R_Z (MΩ)	0.3	0.89	53	0.113	n.a.	94.7	8	7.46
Voltage gain V_X/V_Y (mdB)	−20	0	0	−17.4	34.7	−11.3	−8.69*	−4.1
Current gain I_Z/I_X (dB)	−40	0	0	−34.8	0	−8.69	−8.69	−2.1
−3 dB BW V_X/V_Y (MHz)	2.4 @C_L = 10 pF	14	4.8	11	1	4.1×10^{-3} *	56.4×10^{-3} * @C_L = 30 pF	1.33 @C_L = 1 pF
−3 dB BW I_Z/I_X (MHz)	1.2	13	8.2	10	1.25	39.2×10^{-3}	578×10^{-3}	2.13

* Measured results.

As a final remark in the conclusion of this section, being the solution based on the topology in [19] that was experimentally characterized and found in reasonable agreement with the simulations, we are confident that also the simulations of this CCII, implemented in the same CMOS technology, provide meaningful and quite accurate results, even under MOSFETs' subthreshold regime.

4. Conclusions

This work demonstrated a 0.35 V high-performance CCII achieving rail-to-rail voltage operation at the Y terminal and class AB current operation at the Z terminal. The design leverages a previously developed low-voltage subthreshold bulk-driven CMOS OTA which strategically utilizes body terminals for enhanced small-signal and large-signal performance. The resulting circuit boasts high open-loop gain and cascoded current mirror topologies, leading to accurate voltage and current transfer with bandwidths of 1.33 MHz and 2.13 MHz, respectively. Under a total quiescent current consumption of 2.86 μA, the CCII provides a linear current drive of up to 2.5 μA, with one of the best figures of merit concerning current utilization.

This work contributes to the growing body of research on CCII implementations suitable for portable and implantable electronics and for emerging applications requiring high performance and sub-1V, low-power consumption.

Author Contributions: Conceptualization, S.P.; methodology, M.O.S. and M.C.; validation, M.O.S. and M.C.; writing—original draft preparation, S.P.; writing—review and editing, M.O.S. and M.C. All authors have read and agreed to the published version of the manuscript.

Funding: This work was developed under project SAMOTHRACE (ECS00000022) and funded by the European Union (NextGeneration EU), through the MUR-PNRR.

Data Availability Statement: The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding author.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Chatterjee, S.; Tsividis, Y.; Kinget, P. 0.5-V Analog Circuit Techniques and their Application in OTA and Filter Design. *IEEE J. Solid-State Circuits* **2005**, *40*, 2373–2387. [CrossRef]
2. Monsurrò, P.; Pennisi, S.; Scotti, G.; Trifiletti, A. Biasing technique via bulk terminal for minimum supply CMOS amplifiers. *Electron. Lett.* **2005**, *41*, 779–780. [CrossRef]
3. Monsurró, P.; Pennisi, S.; Scotti, G.; Trifiletti, A. Exploiting the Body of MOS Devices for High Performance Analog Design. *IEEE Circuits Syst. Mag.* **2011**, *11*, 8–23. [CrossRef]
4. Khateb, F.; Dabbous, S.B.A.; Vlassis, S. A Survey of Nonconventional Techniques for Low-voltage Low-power Analog Circuit Design. *Radioengineering* **2013**, *22*, 415–427.
5. Moghaddam, A.K.; Chuah, J.H.; Ramiah, H.; Ahmadian, J.; Mak, P.-I.; Martins, R.P. A 73.9%-Efficiency CMOS Rectifier Using a Lower DC Feeding (LDCF) Self-Body-Biasing Technique for Far-Field RF Energy-Harvesting Systems. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2017**, *64*, 992–1002. [CrossRef]
6. Blalock, B.; Allen, P.; Rincon-Mora, G. Designing 1-V Op Amps Using Standard Digital CMOS Technology. *IEEE Trans. Circuits Syst. II Analog. Digit. Signal Process.* **1998**, *45*, 769–780. [CrossRef]
7. Ferreira, L.H.C.; Sonkusale, S.R. A 60-dB Gain OTA Operating at 0.25-V Power Supply in 130-nm Digital CMOS Process. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2014**, *61*, 1609–1617. [CrossRef]
8. Abdelfattah, O.; Roberts, G.W.; Shih, I.; Shih, Y.-C. An Ultra-Low-Voltage CMOS Process-Insensitive Self-Biased OTA With Rail-to-Rail Input Range. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2015**, *62*, 2380–2390. [CrossRef]
9. Cabrera-Bernal, E.; Pennisi, S.; Grasso, A.D.; Torralba, A.; Carvajal, R.G. 0.7-V Three-Stage Class-AB CMOS Operational Transconductance Amplifier. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2016**, *63*, 1807–1815. [CrossRef]
10. Kulej, T.; Khateb, F. Design and Implementation of Sub 0.5-V OTAs in 0.18-μm CMOS. *Int. J. Circuits Theor. Appl.* **2018**, *46*, 1129–1143. [CrossRef]
11. Khateb, F.; Kulej, T. Design and Implementation of a 0.3-V Differential Difference Amplifier. *IEEE Trans. Circuits Syst. I Regul. Papers* **2019**, *66*, 513–523. [CrossRef]
12. Kulej, T.; Khateb, F. A 0.3-V 98-dB Rail-to-Rail OTA in 0.18 mm CMOS. *IEEE Access* **2020**, *8*, 27459–27467. [CrossRef]
13. Woo, K.-C.; Yang, B.-D. A 0.25-V Rail-to-Rail Three-Stage OTA with an Enhanced DC Gain. *IEEE Trans. Circuits Syst. II Express Briefs* **2020**, *67*, 1179–1183. [CrossRef]

14. Ballo, A.; Grasso, A.D.; Pennisi, S. 0.4-V, 81.3-nA Bulk-Driven Single-Stage CMOS OTA with Enhanced Transconductance. *Electronics* **2022**, *11*, 2704. [CrossRef]
15. Centurelli, F.; Della Sala, R.; Monsurró, P.; Tommasino, P.; Trifiletti, A. An Ultra-Low-Voltage class-AB OTA exploiting local CMFB and Body-to-Gate interface. *AEU-Int. J. Electr. Comm.* **2022**, *145*, 154081. [CrossRef]
16. Akbari, M.; Hussein, S.M.; Hashim, Y.; Tang, K.-T. 0.4-V Tail-Less Quasi-Two-Stage OTA Using a Novel Self-Biasing Transconductance Cell. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2022**, *69*, 2805–2818. [CrossRef]
17. Kulej, T.; Khateb, F.; Arbet, D.; Stopjakova, V. A 0.3-V High Linear Rail-to-Rail Bulk-Driven OTA in 0.13 μm CMOS. *IEEE Trans. Circuits Syst. II Express Briefs* **2022**, *69*, 2046–2050. [CrossRef]
18. Ballo, A.; Grasso, A.D.; Pennisi, S.; Susinni, G. A 0.3-V 8.5-μ a Bulk-Driven OTA. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2023**, *31*, 1444–1448. [CrossRef]
19. Ballo, A.; Carvajal, R.G.; Grasso, A.D.; Luján-Martínez, C.I.; Pennisi, S.; Venezia, C. 0.35-V SR-Enhanced Bulk-Driven OTA for Loads up to 10 nF. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2024**. *in print*. [CrossRef]
20. He, T.; Lee, C. Evolving Flexible Sensors, Wearable and Implantable Technologies Towards BodyNET for Advanced Healthcare and Reinforced Life Quality. *IEEE Open J. Circuits Syst.* **2021**, *2*, 702–720. [CrossRef]
21. Das, R.; Moradi, F.; Heidari, H. Biointegrated and Wirelessly Powered Implantable Brain Devices: A Review. *IEEE Trans. Biomed. Circuits Syst.* **2020**, *14*, 343–358. [CrossRef] [PubMed]
22. Shi, Q.; Dong, B.; He, T.; Sun, Z.; Zhu, J.; Zhang, Z.; Lee, C. Progress in Wearable Electronics/photonics—Moving toward the Era of Artificial Intelligence and Internet of Things. *InfoMat* **2020**, *2*, 1131–1162. [CrossRef]
23. Toledo, P.; Crovetti, P.; Aiello, O.; Alioto, M. Design of Digital OTAs with Operation Down to 0.3 V and nW Power for Direct Harvesting. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2021**, *68*, 3693–3706. [CrossRef]
24. Ferri, G.; Guerrini, N. *Low-Voltage Low-Power CMOS Current Conveyors*; Springer: Berlin/Heidelberg, Germany, 2003.
25. Colucci, P.; D'amico, A.; De Marcellis, A.; Falconi, C.; Ferri, G.; Giovannelli, F.; Parente, F.R.; Stornelli, V. CCII-based voltage amplifier optimization for reduced relative gain error. *Circuits Syst. Signal Process.* **2018**, *37*, 1315–1326. [CrossRef]
26. Stornelli, V.; Ferri, G.; Pantoli, L.; Barile, G.; Pennisi, S. A rail-to-rail constant-gm CCII for instrumentation amplifier applications. *AEU-Int. J. Electron. Commun.* **2018**, *91*, 103–109. [CrossRef]
27. De Marcellis, A.; Ferri, G.; Mantenuto, P. A CCII-based non-inverting Schmitt trigger and its application as astable multivibrator for capacitive sensor interfacing. *Int. J. Circuit Theory Appl.* **2017**, *45*, 1060–1076. [CrossRef]
28. Khateb, F.; Khatib, N.; Kubánek, D. Novel low-voltage low-power high-precision CCII± based on bulk-driven folded cascode OTA. *Microelectron. J.* **2011**, *42*, 622–631. [CrossRef]
29. Khateb, F.; Khatib, N.; Kubánek, D. Novel ultra-low-power class AB CCII+ based on floating-gate folded cascode OTA. *Circuits Syst. Signal Process.* **2012**, *31*, 447–464. [CrossRef]
30. Raikos, G.; Vlassis, S.; Psychalinos, C. 0.5V bulk-driven analog building blocks. *AEU-Int. J. Electron. Commun.* **2012**, *66*, 920–927. [CrossRef]
31. Eldeeb, M.A.; Ghallab, Y.H.; Ismail, Y.; Elghitani, H. Low-voltage subthreshold CMOS current mode circuits: Design and applications. *AEU-Int. J. Electron.* **2017**, *82*, 251–264. [CrossRef]
32. Khateb, F.; Kulej, T.; Kumngern, M. 0.3V Bulk-Driven Current Conveyor. *IEEE Access* **2019**, *7*, 65122–65128. [CrossRef]
33. Mita, R.; Palumbo, G.; Pennisi, S. 1.5-V CMOS CCII+ with high current-driving capability. *IEEE Trans. Circuits Syst. II Analog. Digit. Signal Process.* **2003**, *50*, 187–190. [CrossRef]
34. Arbel, A. Comparison between the Noise Performances of Current-Mode and Voltage-Mode Amplifiers. *Int. J. Analog. Integr. Circuits Signal Process.* **1995**, *7*, 221–242. [CrossRef]

Journal of
Low Power Electronics and Applications

MDPI

Article

An Ultra-Low-Voltage Approach to Accurately Set the Quiescent Current of Digital Standard Cells Used for Analog Design and Its Application on an Inverter-Based Operational Transconductance Amplifier

Riccardo Della Sala *, Francesco Centurelli and Giuseppe Scotti

Department of Information Electronic and Telecommunication (DIET), Sapienza University of Rome, Via Eudossiana 18, 00184 Rome, Italy; francesco.centurelli@uniroma1.it (F.C.); giuseppe.scotti@uniroma1.it (G.S.)
* Correspondence: riccardo.dellasala@uniroma1.it

Abstract: An approach to design analog building blocks based on digital standard cells is presented in this work. By ensuring that every CMOS inverter from a standard-cell library operates with a well-defined quiescent current and output voltage, the suggested method makes it possible to construct analog circuits that are resistant against PVT variations. The method uses the local supply voltages connected to the source terminals of the p-channel and n-channel MOS transistors of the standard-cell inverters as control inputs. It is based on adaptive supply voltage generator (ASVG) reusable blocks, which are comparable to those used in digital applications to handle process variations. All of the standard-cell inverters used for analog functions receive the local supply voltages produced by the ASVGs, which enable setting each cell's quiescent current to a multiple of a reference current and each cell's static output voltage to an appropriate reference voltage. Both the complete custom design of the ASVG blocks and a theoretical study of the feedback loop of the ASVG are presented. An application example through the design of a fully synthesizable two-stage operational transconductance amplifier (OTA) is also provided. The TSMC 180 nm CMOS technology has been used to implement both the OTA and the ASV generators. Simulation results have demonstrated that the proposed approach allows to accurately set the quiescent current of standard-cell inverters, dramatically reducing the effect of PVT variations on the pmain performance parameters of the standard-cell-based two-stage OTA.

Keywords: ultra-low voltage; ultra-low power; IoT; OTA; body driven; replica bias; CMFF

1. Introduction

The evolution of technology has made electronics more and more pervasive [1–3]. Modern electronic systems are essentially digital systems [4] with analog interfaces, enabling them to interact with the real world [5–7]. However, even if the analog part often constitutes just a small fraction of the overall system, its design typically requires the most effort since it is a custom, trial-and-error process, compared to the fully automated design and layout of the digital part [8–15]. For this reason, research is ongoing to automate the design of analog blocks, or at least use automatic place and route tools for the layout phase, to speed up the marketing time and improve the portability of designs across different technologies [16]. In this context, an interesting research field concerns the use of digital standard cells to design analog blocks that are compatible with the automatic place and route tools of the digital design flow [17–21].

Two approaches are possible to design standard-cell-based analog blocks: the analog functions can be rethought from basic principles to implement them in the digital domain (e.g., DIGOTA [13,14,20,22], dyadic pulse DAC [23–26]). On the other hand, standard cells can be exploited to mimic the basic analog building blocks and reproduce analog circuit

topologies [9,18,19,27,28]. The latter approach allows a better control of the circuits' analog performance and is more familiar to the analog designer; however, it requires the designer to cope with the variations of process parameters, temperature, and supply voltage (PVT).

A typical field of application for such circuits is that of ultra-low-voltage (ULV) and ultra-low-power (ULP) systems [29] for biomedical and Internet of Things (IoT) systems [30–36] that include a large digital part, with a low supply voltage (0.3–0.5 V) limiting the use of standard analog approaches such as differential pairs and cascode [37–40]. To implement analog functions such as amplifiers and filters [41–44], body driving and inverter-based stages are the most common options [37,45–56]. For blocks at the edge of the analog and digital worlds, such as comparators, the use of standard cells allows an efficient implementation of low-voltage latches [57–61].

In absence of the tail current generator, which is not compatible with the ULV environment, controlling the bias point of gain stages and hence the performance of the amplifiers (gain, gain–bandwidth product)—with respect to variations in PVT and input common-mode voltage—is extremely difficult [19,27]. Body biasing is a solution that is often adopted in inverter-based stages [45,62], but it is compatible only with standard-cell families where body voltage rails are explicitly accessible.

An approach to center the input–output transfer characteristic of standard-cell inverters to keep the DC output voltage constant has been recently proposed in [27]. This allows us to design robust amplifiers, such as a cascade of inverter stages, keeping them optimally biased [18,28]; however, this also provides no control of the inverters' quiescent current and hence on their transconductance (and consequently on the gain–bandwidth product of amplifiers based on such inverters). The quiescent current is in fact affected by PVT variations of the threshold voltage of devices [51], and this causes huge variations of the transconductance, especially in standard-cell inverters biased in the sub-threshold region [9,45].

Adaptive supply voltage scaling (ASV) is often utilized by digital designers to cope with PVT variations and to reduce the spread of the maximum operating frequency and power consumption of digital circuits [63–65]. In these approaches, specific adaptive supply voltage generators (ASVGs) are exploited to provide local supply voltage for optimizing the speed/power consumption trade-off [66]. These blocks are typically designed following a full-custom approach, similarly to the standard cells in the digital libraries of a given technology. Once all the needed files are available, ASVGs can be used in a semi-custom design flow, where the layout step is performed by an automatic place and route tool.

In this work, we propose a novel approach in which suitable ASVGs are exploited to keep the bias current of digital standard cells used for analog design constant by generating suitable values of local supply voltages $V_{DD_{ctrl}}$ and $V_{SS_{ctrl}}$ in order to counteract the effects of PVT variations on the quiescent current. The proposed approach is applied to the design of a simple two-stage inverter-based OTA implemented with standard-cell inverters. Simulation results referring to the standard-cell library of a 180 nm CMOS technology highlight the capability of the proposed methodology to dramatically reduce the spread of main OTA performance parameters with respect to the conventional design. In Section 2, we present both a theoretical study and simulation results of the conventional standard-cell-based two-stage OTA operating in sub-threshold to highlight the strong impact of PVT variations on the main OTA parameters. The proposed approach to set the quiescent current of standard-cell inverters and its application to a standard-cell-based two-stage OTA are discussed in Section 3, the results of parametric and Monte Carlo simulations are presented in Section 4, and some conclusion are drawn in Section 5.

2. Two-Stage Standard-Cell-Based OTA Operating in Sub-Threshold

To explain the proposed approach in detail, we refer, as a case study, to the conventional two-stage inverter-based OTA implemented with standard-cell inverters. The topology of the two-stage inverter-based OTA is depicted in Figure 1. The first stage is composed using $I_{1–4}$, which implement a standard-cell-based differential to a single-ended

converter [19], whereas the second stage is composed using I_5, implementing the inverting output stage. Although it is simple, this architecture is very effective for highlighting the main limitations that come from the adoption of a standard-cell approach to analog design, in which analog blocks are directly connected to the supply voltages V_{DD} and V_{SS}, without any control of the bias current of standard-cell inverters.

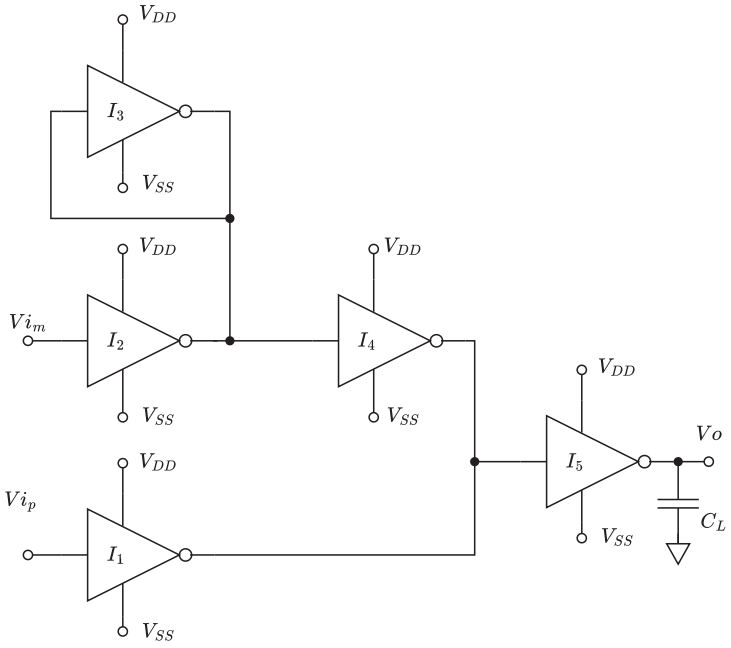


Figure 1. Conventional two-stage standard-cell-based OTA.

2.1. Characterization of the CMOS Inverter Operating in Sub-Threshold and Transfer Matrix

For the following analysis, we denote the input capacitance of the generic i-th inverter with C_{gs_i}, which is given by the sum of the gate-source capacitances $C_{gs_{n,p_i}}$ of the NMOS and PMOS transistors of the inverter, with C_{gd_i} being the sum of the gate-drain capacitances $C_{gd_{n,p_i}}$, gm_i being the sum of the transconductances gm_{n,p_i} of the NMOS and PMOS transistors of the inverter, and with gds_i being the sum of output conductances gds_{n,p_i} of the NMOS and PMOS transistors of the inverter. By using this notation, the inverter's transfer matrix input voltage, output voltage, and currents can be written as follows:

$$\begin{bmatrix} V_{In} \\ I_{In} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \times \begin{bmatrix} V_{Out} \\ -I_{Out} \end{bmatrix} \tag{1}$$

where

$$A = \frac{gds_i}{gm_i}\left(1 + s\, C_{gd_i}/gds_i\right) \tag{2}$$

$$B = \frac{s \cdot \left(Cgs_i + gm_i/gds_i \cdot Cgd_i\right) \cdot gds_i}{gm_i} \cdot \left(1 + s\, C_{gd_i}/gds_i\right) \tag{3}$$

$$C = 1/gm_i \tag{4}$$

and, finally,

$$D = \frac{s \cdot \left(Cgs_i + gm_i/gds_i \cdot Cgd_i\right)}{gm_i} \tag{5}$$

As it can be observed, the coefficients of the inverter's transfer matrix depend on terms gm_i and gds_i. These terms rely on the quiescent current of the NMOS and PMOS transistors

of the inverter which, due to the operation in the sub-threshold region, can be expressed as follows:

$$\begin{cases} I_{d_n} = I_{d_{0n}} e^{\frac{Vgs_n - Vth_n}{n\ Ut}} \left(1 - e^{-\frac{Vds_n}{Ut}}\right) & \text{NMOS} \\ I_{d_p} = I_{d_{0p}} e^{\frac{Vsg_p + Vth_p}{n\ Ut}} \left(1 - e^{-\frac{Vsd_p}{Ut}}\right) & \text{PMOS} \end{cases} \tag{6}$$

where usual notation is adopted for gate-source, drain-source, and threshold voltages of NMOS and PMOS transistors; Ut denotes the thermal voltage; and $n = 1 + C_{depl}/C_{ox}$ and I_{d_0} can be written as follows:

$$I_{d_{0n,p}} = \mu_{n,p}(n-1)C_{ox}\frac{W_{n,p}}{L_{n,p}}U_t^2 \tag{7}$$

where $\mu_{n,p}$ and C_{ox} are the mobility and oxide capacitance per unit area, whereas $W_{n,p}$ and $L_{n,p}$ are the gate width and gate length of NMOS and PMOS devices, respectively.

It is evident from the above equations that the quiescent current of MOS devices, and therefore the small signal parameters of the inverter, are strongly dependent on PVT variations. This has a strong impact on the performance parameters of the conventional two-stage standard-cell-based OTA, as it will be better pointed out in the next subsections.

2.2. Analytical Characterization of the Standard-Cell-Based Two-Stage OTA

The most important performance parameters of an OTA are the gain–bandwidth product (GBW), the phase margin ($m\varphi$), the differential voltage gain (Av_D), the power consumption (P_d), and the average slew rate (SR_{avg}). Referring to the OTA in Figure 1, using the notation introduced in Section 2.1, and denoting the load capacitance of the OTA with C_L, the main performance parameters of the OTA can be easily expressed as follows:

$$Av_D = \frac{1}{2}\left(1 + \frac{gm_2}{gm_3}\right) \cdot \frac{gm_1}{gds_4 + gds_1} \cdot \frac{gm_5}{gds_5} \cdot \frac{1}{1 + sC_L/gds_5} \tag{8}$$

$$GBW = \frac{1}{2}\left(1 + \frac{gm_2}{gm_3}\right) \cdot \frac{gm_1}{gds_4 + gds_1} \cdot \frac{gm_5}{C_L} \tag{9}$$

$$m\varphi = 180 - arctan\left\{GBW \cdot \frac{gds_4 + gds_1}{C_{gs_5}}\right\} - arctan\left\{GBW \cdot \frac{gds_5}{C_L}\right\} \tag{10}$$

$$SR_{avg} = \frac{Id_0\ e^{\frac{V_{DD} - Vth_n}{n\ Ut}} + Id_0\ e^{\frac{V_{DD} - Vth_p}{n\ Ut}}}{2} \tag{11}$$

As it can be observed, all the terms in the above equations depend on gm_i and gds_i of the inverters, which, as discussed in Section 2.1, are strongly dependent on the supply voltages, which set the value of gate-source and drain-source voltages, the temperature (due to the temperature dependence of parameters such as Ut or $I_{d_{0n,p}}$), and process variations (due to the dependence of V_{th} on process steps).

All these considerations allow us to conclude that the conventional standard-cell-based two-stage OTA exhibits performance parameters that strongly dependent on PVT variations. This point will be further assessed in the next section through transistor-level simulations.

2.3. Simulation Results on the Conventional Standard-Cell-Based Two-Stage OTA Operating in Sub-Threshold without Quiescent Current Control

The two-stage standard-cell-based OTA reported in Figure 1 was designed in reference to the standard-cell library of the TSMC 180 nm CMOS technology with a nominal supply voltage $V_{DD} - V_{SS}$ of 0.35 V. Transistor-level simulations were carried out within the Cadence Virtuoso environment. To quantify the dependence of performance parameters on PVT variations, parametric and corner simulations were executed. The results are summarized in Table 1, where V_{off} denotes the error with respect to the ideal DC output

voltage of the OTA in a unity–gain feedback configuration and where Itot is the total current drawn by the OTA. The first five columns in the table (from Typ to FS) refer to the five process corners of the technology, the sixth and seventh column refer to supply voltage variations, and the last two columns refer to temperature variations.

Table 1. Performance parameters of the conventional standard-cell-based OTA under PVT variations.

	Typ	**FF**	**SS**	**SF**	**FS**	**90% V_{DD}**	**110% V_{DD}**	**0°**	**80°**
V_{off} [mV]	2.2	2	2.3	−0.5	7.1	7.6	2.9	2.2	2.2
Pd [nW]	1.688	6.958	0.371	1.599	3.338	1.013	1.505	0.536	9.713
Itot [nA]	4.221	17.39	0.927	3.998	8.345	3.217	3.909	1.341	24.28
Av_d [dB]	52.12	49.53	56.41	51.95	51.18	48.71	51.78	52.9	50.55
GBW [kHz]	53.56	217.8	12.12	66.63	39.58	13.32	42.22	18.05	265.8
$m\varphi$ [deg]	60.41	63.03	56.38	53.67	71.71	72.89	63.92	60.9	60.46
SR_{avg} [V/ms]	144.5	546.2	34.17	149.5	394.1	21.59	101.1	90.86	368.1

The results of process-only and mismatch-only Monte Carlo simulations are reported in Table 2 and Table 3, respectively. The histograms of GBW, Pd, and $m\varphi$ under process-only and mismatch-only Monte Carlo simulations are reported in Figure 2 and Figure 3, respectively.

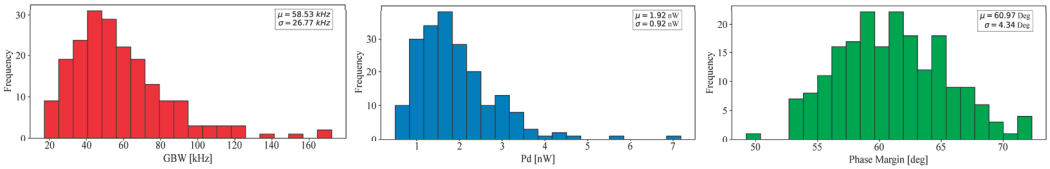
Table 2. Performance parameters of the conventional standard-cell-based OTA under process-only Monte Carlo simulations.

	Mean	**Std Dev**
V_{off} [mV]	2.3	0.99
Pd [nW]	1.92	0.92
Itot [nA]	4.379	2.319
Av_d [dB]	51.12	0.90
$m\varphi$ [deg]	60.97	4.34
GBW [kHz]	58.53	26.77
SR_{avg} [V/ms]	147.5	80.44

Table 3. Performance parameters of the conventional standard-cell-based OTA under mismatch-only Monte Carlo simulations.

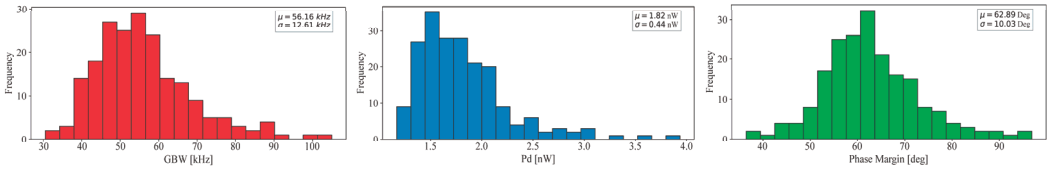
	Mean	**Std Dev**
V_{off} [mV]	3.1	18.11
Pd [nW]	1.82	0.44
Itot [nA]	4.314	1.106
Av_d [dB]	49.11	10.11
$m\varphi$ [deg]	62.89	10.03
GBW [kHz]	56.16	12.61
SR_{avg} [V/ms]	146	30.52

As it can be observed in all the above tables and figures, the quiescent current of the standard-cell inverters operating in a sub-threshold exhibits huge variations, resulting in large variations in the GBW and $m\varphi$ of the OTA. Due to this behavior, the applicability of this OTA to signal processing systems presents many difficulties and drawbacks, and its usage is not justified. In order to make this standard-cell-based OTA usable in real applications, the quiescent current of the inverters should be controlled to at least reduce variations with respect to temperature and process variations.



(**a**) (**b**) (**c**)

Figure 2. Gain–bandwidth product (**a**), power consumption (**b**), and phase margin (**c**) of the conventional standard-cell-based OTA under process-only Monte Carlo simulations.



(**a**) (**b**) (**c**)

Figure 3. Gain–bandwidth product (**a**), power consumption (**b**), and phase margin (**c**) of the conventional standard-cell-based OTA under mismatch-only Monte Carlo simulations.

3. Proposed Approach to Set the Quiescent Current of Standard-Cell Inverters and Application to a Standard-Cell-Based OTA

In the conventional approach, standard-cell inverters are directly supplied with two constant voltages V_{DD} and V_{SS}. However, standard-cell inverters with constant supply voltages V_{DD} and V_{SS} exhibit huge variations in their transconductance, especially if operating in a sub-threshold. This, as demonstrated in the previous section, results in large variations in the main OTA parameters, such as the gain–bandwidth product, the power dissipation, and the phase margin.

In order to properly set the quiescent current of standard-cell inverters, the approach proposed here takes advantage of two locally generated supply voltages, $V_{DD_{ctrl}}$ and $V_{SS_{ctrl}}$, whose main role is to accurately set the DC current of all the standard-cell inverters used for analog design through a replica-bias approach, thus strongly reducing the variability of the transconductance and output conductance gm_i and gds_i of the standard-cell inverters operating in a sub-threshold. The simplified schematic of the proposed approach to set the quiescent current of standard-cell inverter is reported in Figure 4. The two circuits in the upper and lower right corner of the figure act as ASV generators to produce the $V_{DD_{ctrl}}$ and $V_{SS_{ctrl}}$, respectively. These voltages are then routed as local supply voltages to all the standard-cell inverters used for analog purposes (i.e., the inverters implementing the two-stage OTA in this example). Referring to Figure 4, transistors Mn_3 and Mp_3 implement a replica of the NMOS and PMOS device of the minimum area standard-cell inverter, respectively, whereas Mn_1–Mn_2 and Mp_1–Mp_2 implement conventional current mirrors that force a reference current I_{bias} in Mn_3 and Mp_3. The gate voltage of the replica devices Mn_3 and Mp_3 is set to a reference voltage V_{ref} (usually set at the midpoint between V_{DD} and V_{SS}), and their drain voltage is compared with the same reference voltage V_{ref} through the two error amplifiers EA_1 and EA_2. The task of amplifiers EA_1 and EA_2 is to generate the two control voltages, $V_{DD_{ctrl}}$ and $V_{SS_{ctrl}}$, which close the loops at the source nodes of Mp_3 and Mn_3, respectively. In this way, the two control voltages $V_{DD_{ctrl}}$ and $V_{SS_{ctrl}}$ are changed by the feedback loops in order to set the bias current of Mn_3 and Mp_3 to I_{bias} and the drain voltages of Mn_3 and Mp_3 to V_{ref} despite PVT variations, as will be better assessed in the next sections.

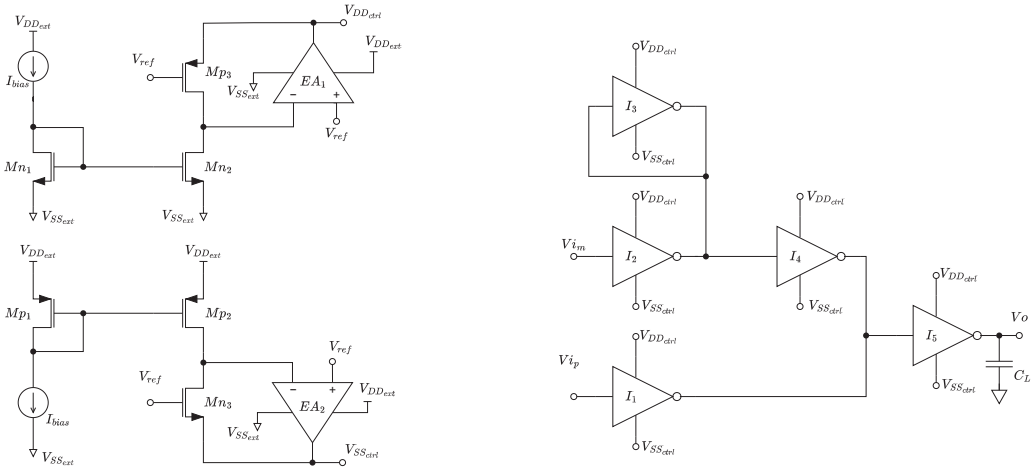


Figure 4. Proposed approach to set the quiescent current of standard-cell inverters and application to the standard-cell-based two-stage OTA.

3.1. Analysis of the Feedback Loop in the ASV Generators

In the following section, we derive a simplified model of the feedback loop implementing the ASV generator for the $V_{DD_{ctrl}}$ (see the upper right corner of Figure 4). A similar model can be developed for the ASV generator for the $V_{SS_{ctrl}}$. The block scheme derived for the feedback loop in the upper right corner of Figure 4 is depicted in Figure 5: Id_{p_3} is the current that flows in Mp_3 when the supply voltage $V_{DD_{ctrl}}$ has its nominal value, and Vx is the variation of $V_{DD_{ctrl}}$ with respect to such value. I_{bias} is the reference current, mirrored through $Mn_{1,2}$.

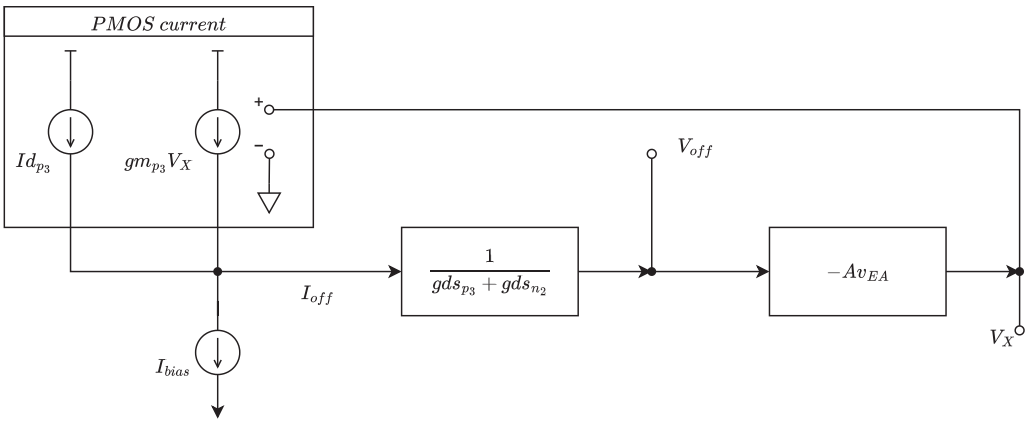


Figure 5. Block scheme derived for the feedback loop of the $V_{DD_{ctrl}}$ ASV generator.

The comparison between the drain current of Mp_3 and I_{bias} generates an offset current I_{off} which, flowing through the output conductance $gds_{p3} + gds_{n2}$, turns into an offset voltage (V_{off} in Figure 5 is the difference between the DC output voltage and V_{ref}). The error amplifier EA_1, with gain Av_{EA}, closes the loop, modifying the supply voltage $V_{DD_{ctrl}}$, hence the current in Mp_3, to cancel the offset. Due to the finite loop gain, the residual offset current is

$$I_{off} = \frac{Id_{p_3} - Id_{bias}}{1 + \frac{gm_{p3}Av_{EA}}{gds_{p3}+gds_{n2}}} \tag{12}$$

By performing the same analysis on the feedback loop in the ASV generator for the $V_{SS_{ctrl}}$, the offset current in Mn_3 can be expressed as follows:

$$I_{off} = \frac{Id_{n_3} - Id_{bias}}{1 + \frac{gm_{n3}Av_{EA}}{gds_{n3}+gds_{p2}}} \tag{13}$$

Equations (12) and (13) show that the proposed feedback loops suppress the offset current by a factor given by the gain of the auxiliary amplifier times the gain of the replica stage. This means that the feedback loops allow us to set the quiescent current of Mp_3 and of Mn_3 to I_{bias}, strongly reducing the effect of PVT variations (which give rise to the component I_{off}). It has to be pointed out that, since Mp_3 and of Mn_3 are a replica of the transistors of the standard-cell inverter, the quiescent current of all the standard-cell inverters using $V_{DD_{ctrl}}$ and $V_{SS_{ctrl}}$ as local supply voltages will also be set approximately equal to I_{bias} despite PVT variations.

3.2. Implementation of the Error Amplifier

The error amplifier was implemented according to Figure 6. It is a two-stage OTA with a Miller compensation. The transistors' sizes are reported in Table 4. Since V_{ref} = 0.2 V, V_{DD} = 0.5 V, and Mp_3 and Mp_4 are biased in a sub-threshold, the current source Mp_2 is properly biased in saturation. The compensation capacitance C_{comp} is 10 pF, whereas Co_{EA} is the parasitic capacitance seen at the output of the error amplifier, which is in the order of hundreds fF (it depends on the C_{gs} and C_{gd} seen at the source terminals of transistors).

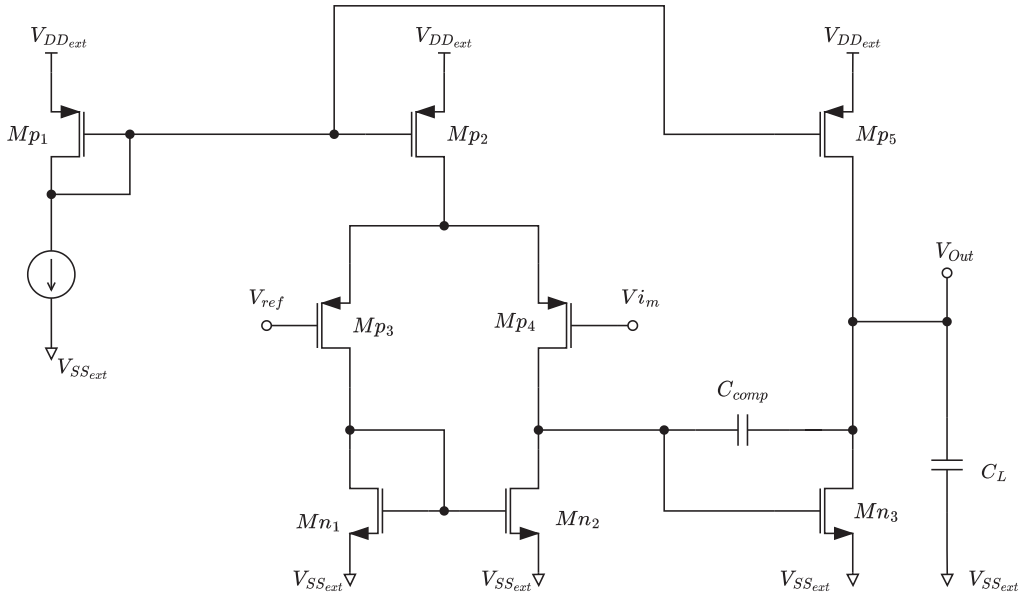


Figure 6. Schematic of the error amplifier.

Table 4. Transistor sizing of the error amplifier.

	$Mp_1 = Mp_2$	$Mp_3 = Mp_4$	$Mn_1 = Mn_2$	Mn_3	Mp_5
W [m]	1 µ	1 µ	440 n	3.52 µ	4 µ
L [m]	500 n	500 n	1 µ	220 n	500 n

To effectively bias multiple stages, it is crucial to properly size the error amplifier's output stage, which has to supply a current to all the standard cells. In the design phase, by estimating the overall system requirements, the error amplifier can be appropriately sized to bias all cells simultaneously, eliminating the need for additional stages.

3.3. Impact of the $V_{DD_{ctrl}}$ and $V_{SS_{ctrl}}$ ASV Generators on the PSRR

By using the proposed approach to stabilize the bias current of standard-cell-based analog blocks, the supply voltage to such blocks is provided by the ASV generators. This affects the power supply rejection ratio (PSRR) of the analog block, since disturbances from the overall supply voltages are filtered by the ASVGs: the overall gain from the global positive supply voltage to the output of the analog block can be written as

$$A_{dd,tot} = A_{ASV1,dd}A_{dd} + A_{ASV2,dd}A_{ss} \tag{14}$$

and

$$A_{ss,tot} = A_{ASV1,ss}A_{dd} + A_{ASV2,ss}A_{ss} \tag{15}$$

where A_{dd} and A_{ss} are the gains from positive and negative supply voltages to the output of the analog block (e.g., an OTA), and $A_{ASV1,dd}(A_{ASV1,ss})$ and $A_{ASV2,dd}(A_{ASV2,ss})$ are the gains from the positive (negative) supply voltage to the outputs of the positive and negative (positive) ASVGs, respectively. An analog expression can be written for the negative supply voltage.

The analysis of the ASVG circuit in Figure 4 shows that the gains $A_{ASV1,dd}$ and $A_{ASV2,ss}$ are approximately inversely proportional to the intrinsic gain A_0 of MOS devices, thus resulting in an improvement of the order of A_0 in the PSRR. If we define the positive and negative PSRRs of the analog block as $PSRRd$ and $PSRRs$, the overall positive and negative PSRRs are approximately given by

$$PSRRd_{tot} = \frac{A_0}{\frac{1}{PSRRd} - \frac{1}{PSRRs}\left(1 + \frac{gm_p}{gm_n}\right)} \tag{16}$$

$$PSRRs_{tot} = \frac{A_0}{\frac{1}{PSRRs} - \frac{1}{PSRRd}\left(1 + \frac{gm_n}{gm_p}\right)} \tag{17}$$

where the generic transconductance gain of MOS devices is denoted with gm_p and gm_n.

In Figure 7, the gain $A_{ASV1,dd}$ is reported in a blue color, gain $A_{ASV2,dd}$ is reported in a green color, gain $A_{ASV1,ss}$ is reported in a red color, and gain $A_{ASV2,ss}$ is reported in a purple color.

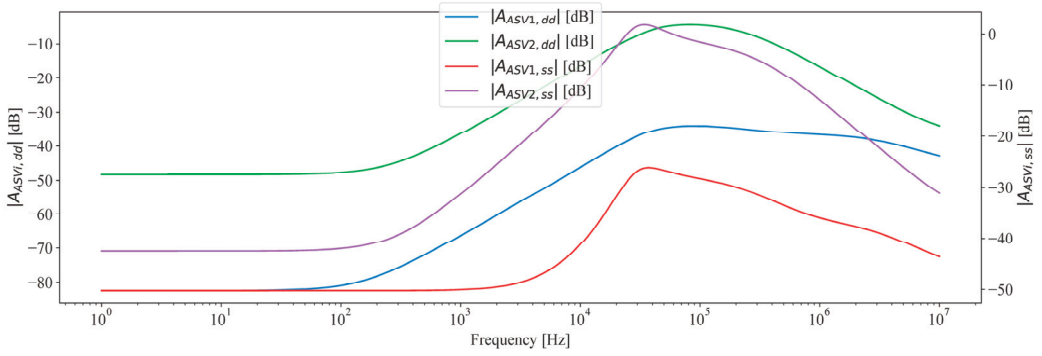


Figure 7. Gain $A_{ASV1,dd}$ is reported in a blue color, gain $A_{ASV2,dd}$ is reported in a green color, gain $A_{ASV1,ss}$ is reported in a red color, and gain $A_{ASV2,ss}$ is reported in a purple color.

4. Simulation Results on the Standard-Cell-Based Two-Stage OTA Operating in Sub-Threshold with the Proposed Quiescent Current Control

The two-stage standard-cell-based OTA with the proposed quiescent current control scheme reported in Figure 4 was also designed in reference to the TSMC 180 nm CMOS technology, with a global supply voltage $V_{DD} - V_{SS}$ of 0.5 V for the ASV generators and a nominal local supply voltage $V_{DD_{ctrl}} - V_{SS_{ctrl}}$ of 0.35 V for the standard-cell invert-

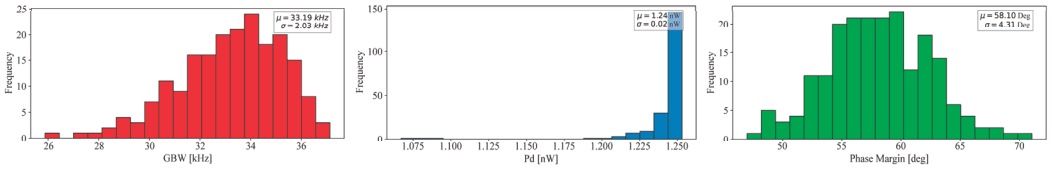
ers used in the OTA. Transistor-level simulations were carried out within the Cadence Virtuoso environment.

To highlight the effectiveness of the proposed approach in strongly reducing the effects of PVT variations, the same parametric and corner simulations executed for the OTA without the quiescent current control were also carried out on the OTA, exploiting the proposed current control approach. Results of these simulations are summarized in Table 5, where Itot is the total current drawn by the OTA. The first five columns in the table refer to the five process corners of the technology, the sixth and seventh columns refer to global supply voltage variations, and the last two columns refer to temperature variations. As it can be observed, with respect to the conventional OTA without quiescent current control, both current dissipation and the GBW are much more stable. To further improve the robustness of the proposed circuit to temperature variations, the reference current I_{bias} was assumed to be generated by a proportional to absolute temperature (PTAT) current source, which set a bias DC in the standard-cell inverter to approximately 500 pA in typical conditions. The usage of the PTAT current source is evident from the the last two columns of Table 5, in which Itot results varied from 1.945 nA to 3.56 nA in order to keep the GBW almost constant in the specified temperature range from 0° to 80°.

Table 5. Performance parameters of the standard-cell-based OTA with the proposed quiescent current control scheme under PVT variations.

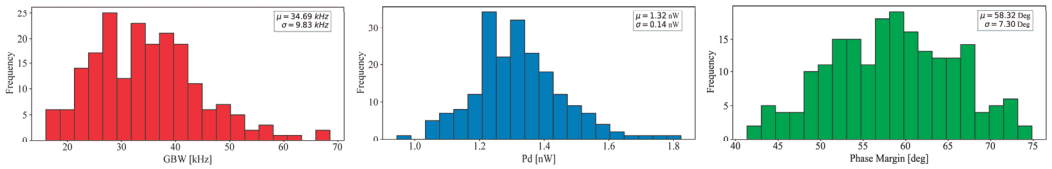
	Typ	**FF**	**SS**	**SF**	**FS**	**90% V_{DD}**	**110% V_{DD}**	**0**	**80**
V_{off} [mV]	0.01	0.04	0.2	−0.1	0.023	0.02	0.13	0.04	0.03
Itot [nA]	2.497	2.505	2.167	2.399	2.499	2.477	2.499	1.945	3.56
Pd [nW]	1.249	1.253	1.084	1.199	1.249	1.239	1.25	0.972	1.78
Av_d [dB]	51.29	45.72	58.65	51.19	50.72	51.27	51.29	53.59	45.41
$m\varphi$ [deg]	57.8	69.8	40.79	58	59.12	57.83	57.82	52.75	69.71
GBW [kHz]	33.67	27.42	36.04	31.91	33.48	33.42	33.68	31.25	31.42
SR_{avg} [V/ms]	30.1	12.27	114.6	19.27	55.41	33.83	29.32	70.82	7.218

In addition, the results of process-only and mismatch-only Monte Carlo simulations are reported in Table 6 and Table 7, respectively. The histograms of GBW, Pd, and $m\varphi$ under process-only and mismatch-only Monte Carlo simulations are also reported in Figure 8 and Figure 9, respectively. As it can be observed, the power dissipated. Moreover, the current consumption and the GBW were characterized by an extremely small standard deviation, especially if compared with the same topology characterized without a control loop, confirming the extreme robustness achieved by the standard-cell-based OTA exploiting the proposed ASV-based quiescent current control approach.



(**a**) (**b**) (**c**)

Figure 8. Gain–bandwidth product (**a**), power consumption (**b**), and phase margin (**c**) of the standard-cell-based OTA with the proposed quiescent current control scheme under process-only Monte Carlo simulations.



(**a**) (**b**) (**c**)

Figure 9. Gain–bandwidth product (**a**), power consumption (**b**), and phase margin (**c**) of the standard-cell-based OTA with the proposed quiescent current control scheme under mismatch-only Monte Carlo simulations.

Table 6. Performance parameters of the standard-cell-based OTA with the proposed quiescent current control scheme under process-only Monte Carlo simulations.

	Mean	**Std Dev**
V_{off} [mV]	0.03	0.022
Pd [nW]	1.248	0.022
Itot [nA]	2.497	0.044
Av_d [dB]	51.22	1.90
$m\varphi$ [deg]	58.18	4.31
GBW [kHz]	33.41	2.03
SR_{avg} [V/ms]	31.49	10.48

Table 7. Performance parameters of the standard-cell-based OTA with the proposed quiescent current control scheme under mismatch-only Monte Carlo simulations.

	Mean	**Std Dev**
V_{off} [mV]	−0.9	15.82
Pd [nW]	1.32	0.14
Itot [nA]	2.62	0.27
Av_d [dB]	51.32	2.54
$m\varphi$ [deg]	58.32	7.30
GBW [kHz]	34.69	9.83
SR_{avg} [V/ms]	31.88	10.48

5. Conclusions

In most cases, the existing ways to implement analog building blocks from digital standard-cell libraries do not provide enough control over the quiescent operating point. This makes the same solutions vulnerable to significant fluctuations in performance when PVT conditions are changed. This research offered a technique for biasing through the development of ASV generators, which appears to be a workable way to create analog circuits based on standard cells that have output voltages and quiescent currents that are well defined. A fully synthesizable two-stage OTA was designed in a 180 nm CMOS process to illustrate the application of the proposed approach. Excellent stability of the GBW, power consumption, and phase margin of the OTA exploiting the proposed quiescent current control strategy were demonstrated by the simulation results. More specifically, the ratio between the mean value and the standard deviation ($\frac{\sigma}{\mu}$) of the GBW (Pd) obtained from process-only Monte Carlo simulations for the OTA designed with the proposed approach was about 0.06 (0.017). These values, when compared with the $\frac{\sigma}{\mu}$ values of the GBW (Pd) obtained from the conventional standard-cell-based OTA without ASVGs, which were 0.5 (0.53), confirm the dramatic reduction in the $\frac{\sigma}{\mu}$ of main performance parameters under process variations that was allowed by the proposed approach.

Author Contributions: Conceptualization, R.D.S., G.S. and F.C.; methodology, R.D.S., G.S. and F.C.; software, R.D.S.; validation, R.D.S. and G.S.; formal analysis, R.D.S.; investigation, R.D.S. and G.S.; resources, G.S.; data curation, R.D.S.; writing—original draft preparation, R.D.S.; writing—review and editing, R.D.S., G.S. and F.C.; visualization, R.D.S., G.S. and F.C.; supervision, G.S.; project administration, G.S.; funding acquisition, G.S. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: No new data were created or analyzed in this study. Data sharing is not applicable to this article.

Conflicts of Interest: The authors declare no conflicts of interest.

Abbreviations

The following abbreviations are used in this manuscript:

ASV	Adaptive Supply Voltage
ASVG	Adaptive Supply Voltage Generator
DAC	Digital-to-Analog Converter
DIGOTA	Digital Operational Transconductance Amplifier
GBW	Gain–Bandwidth Product
IoT	Internet of Things
OTA	Operational Transconductance Amplifier
PSRR	Power Supply Rejection Ratio
PVT	Process, Supply Voltage, and Temperature
ULP	Ultra-Low Power
ULV	Ultra-Low Voltage

References

1. Buzzin, A.; Asquini, R.; Caputo, D.; de Cesare, G. Sensitive and Compact Evanescent-Waveguide Optical Detector for Sugar Sensing in Commercial Beverages. *Sensors* **2023**, *23*, 8184. [CrossRef] [PubMed]
2. Gupta, B.B.; Quamara, M. An overview of Internet of Things (IoT): Architectural aspects, challenges, and protocols. *Concurr. Comput. Pract. Exper.* **2020**, *32*, e4946. [CrossRef]
3. Kadhim, K.T.; Alsahlany, A.M.; Wadi, S.M.; Kadhum, H.T. An Overview of Patient's Health Status Monitoring System Based on Internet of Things (IoT). *Wirel. Pers. Commun.* **2020**, *114*, 2235–2262. [CrossRef]
4. Barbirotta, M.; Cheikh, A.; Mastrandrea, A.; Menichelli, F.; Vigli, F.; Olivieri, M. A Fault Tolerant soft-core obtained from an Interleaved-Multi- Threading RISC- V microprocessor design. In Proceedings of the 2021 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), Athens, Greece, 6–8 October 2021; pp. 6–8. [CrossRef]
5. Chuah, J.W. The Internet of Things: An overview and new perspectives in systems design. In Proceedings of the 2014 International Symposium on Integrated Circuits (ISIC), Singapore, 10–12 December 2014; pp. 10–12. [CrossRef]
6. Aiello, O.; Crovetti, P.; Alioto, M. Fully Synthesizable Low-Area Analogue-to-Digital Converters with Minimal Design Effort Based on the Dyadic Digital Pulse Modulation. *IEEE Access* **2020**, *8*, 70890–70899. [CrossRef]
7. Di Patrizio Stanchieri, G.; Aiello, O.; De Marcellis, A. A 0.4 V 180 nm CMOS Sub-μW Ultra-Compact and Low-Effort Design PWM-Based ADC. In Proceedings of the 2024 IEEE International Symposium on Circuits and Systems (ISCAS), New Delhi, India, 18–19 October 2024; pp. 19–22. [CrossRef]
8. Toledo, P.; Aiello, O.; Crovetti, P.S. A 300mV-Supply Standard-Cell-Based OTA with Digital PWM Offset Calibration. In Proceedings of the 2019 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC), Helsinki, Finland, 29–30 October 2019; pp. 29–30. [CrossRef]
9. Centurelli, F.; Della Sala, R.; Scotti, G. A Standard-Cell-Based CMFB for Fully Synthesizable OTAs. *J. Low Power Electron. Appl.* **2022**, *12*, 27. [CrossRef]
10. Barbirotta, M.; Menichelli, F.; Cheikh, A.; Mastrandrea, A.; Angioli, M.; Olivieri, M. Dynamic Triple Modular Redundancy in Interleaved Hardware Threads: An Alternative Solution to Lockstep Multi-Cores for Fault-Tolerant Systems. *IEEE Access* **2024**, *12*, 95720–95735. [CrossRef]
11. Sood, L.; Agarwal, A. A CMOS standard-cell based fully-synthesizable low-dropout regulator for ultra-low power applications. *AEU Int. J. Electron. Commun.* **2021**, *141*, 153958. [CrossRef]
12. Xu, Z.; Ojima, N.; Li, S.; Iizuka, T. An All-Standard-Cell-Based Synthesizable SAR ADC With Nonlinearity-Compensated RDAC. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **2021**, *29*, 2153–2162. [CrossRef]
13. Toledo, P.; Crovetti, P.; Aiello, O.; Alioto, M. Design of Digital OTAs With Operation Down to 0.3 V and nW Power for Direct Harvesting. *IEEE Trans. Circuits Syst. I* **2021**, *68*, 3693–3706. [CrossRef]

14. Toledo, P.; Crovetti, P.; Aiello, O.; Alioto, M. Fully Digital Rail-to-Rail OTA With Sub-1000-μm^2 Area, 250-mV Minimum Supply, and nW Power at 150-pF Load in 180 nm. *IEEE Solid-State Circuits Lett.* **2020**, *3*, 474–477. [CrossRef]
15. Aiello, O.; Crovetti, P.; Sharma, A.; Alioto, M. Fully-Synthesizable Current-Input ADCs for Ultra-Low Area and Minimal Design Effort. In Proceedings of the 2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Genoa, Italy, 27–29 November 2019; pp. 27–29. [CrossRef]
16. Liu, J.; Park, B.; Guzman, M.; Fahmy, A.; Kim, T.; Maghari, N. A Fully Synthesized 77-dB SFDR Reprogrammable SRMC Filter Using Digital Standard Cells. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **2018**, *26*, 1126–1138. [CrossRef]
17. Toledo, P.; Klimach, H.; Bampi, S.; Crovetti, P. A 300 mV-Supply, 144 nW-Power, 0.03 mm^2-Area, 0.2-PEF Digital-Based Biomedical Signal Amplifier in 180 nm CMOS. In Proceedings of the 2021 IEEE International Symposium on Medical Measurements and Applications (MeMeA), Lausanne, Switzerland, 23–25 June 2021; pp. 23–25. [CrossRef]
18. Della Sala, R.; Centurelli, F.; Scotti, G. A High Performance 0.3 V Standard-Cell-Based OTA Suitable for Automatic Layout Flow. *Appl. Sci.* **2023**, *13*, 5517. [CrossRef]
19. Sala, R.D.; Centurelli, F.; Scotti, G. A Novel Differential to Single-Ended Converter for Ultra-Low-Voltage Inverter-Based OTAs. *IEEE Access* **2022**, *10*, 98179–98190. [CrossRef]
20. Toledo, P.; Crovetti, P.; Klimach, H.; Bampi, S.; Aiello, O.; Alioto, M. A 300mV-Supply, Sub-nW-Power Digital-Based Operational Transconductance Amplifier. *IEEE Trans. Circuits Syst. II* **2021**, *68*, 3073–3077. [CrossRef]
21. Angioli, M.; Barbirotta, M.; Cheikh, A.; Mastrandrea, A.; Menichelli, F.; Jamili, S.; Olivieri, M. Design, Implementation and Evaluation of a New Variable Latency Integer Division Scheme. *IEEE Trans. Comput.* **2024**, *73*, 1767–1779. [CrossRef]
22. Privitera, M.; Crovetti, P.; Grasso, A.D. A Novel Digital OTA Topology With 66-dB DC Gain and 12.3-kHz Bandwidth. *IEEE Trans. Circuits Syst. II* **2023**, *70*, 3988–3992. [CrossRef]
23. Crovetti, P.S. All-Digital High Resolution D/A Conversion by Dyadic Digital Pulse Modulation. *IEEE Trans. Circ. Syst. I* **2016**, *64*, 573–584. [CrossRef]
24. Aiello, O.; Crovetti, P.; Alioto, M. Standard Cell-Based Ultra-Compact DACs in 40-nm CMOS. *IEEE Access* **2019**, *7*, 126479–126488. [CrossRef]
25. Aiello, O.; Crovetti, P.S.; Alioto, M. Fully Synthesizable Low-Area Digital-to-Analog Converter With Graceful Degradation and Dynamic Power-Resolution Scaling. *IEEE Trans. Circ. Syst. I* **2019**, *66*, 2865–2875. [CrossRef]
26. Rubino, R.; Crovetti, P.S.; Aiello, O. Design of Relaxation Digital-to-Analog Converters for Internet of Things Applications in 40nm CMOS. In Proceedings of the 2019 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Bangkok, Thailand, 11–14 November 2019; pp. 11–14. [CrossRef]
27. Sala, R.D.; Centurelli, F.; Scotti, G. Enabling ULV Fully Synthesizable Analog Circuits: The BA Cell, a Standard-Cell-Based Building Block for Analog Design. *IEEE Trans. Circuits Syst. II* **2022**, *69*, 4689–4693. [CrossRef]
28. Sala, R.D.; Centurelli, F.; Scotti, G. A Novel High Performance Standard-Cell Based ULV OTA Exploiting an Improved Basic Amplifier. *IEEE Access* **2024**, *12*, 17513–17521. [CrossRef]
29. Aiello, O.; Crovetti, P.; Alioto, M. Ultra-Low Power and Minimal Design Effort Interfaces for the Internet of Things: Invited paper. In Proceedings of the 2019 IEEE International Circuits and Systems Symposium (ICSyS), Kuantan, Malaysia, 18–19 September 2019; pp. 18–19. [CrossRef]
30. Buzzin, A.; Cupo, S.; Giovine, E.; de Cesare, G.; Belfiore, N.P. Compliant Nano-Pliers as a Biomedical Tool at the Nanoscale: Design, Simulation and Fabrication. *Micromachines* **2020**, *11*, 1087. [CrossRef] [PubMed]
31. Namdari, A.; Aiello, O.; Caviglia, D.D. 0.5V 32nW Inverter-Based Gm-C Filter for Bio-Signal Processing. In Proceedings of the 2024 IEEE International Symposium on Circuits and Systems (ISCAS), New Delhi, India, 18–19 October 2024; pp. 19–22. [CrossRef]
32. Sanchotene Silva, R.; Rodovalho, L.H.; Aiello, O.; Ramos Rodrigues, C. A 1.9 nW, Sub-1 V, 542 pA/V Linear Bulk-Driven OTA with 154 dB CMRR for Bio-Sensing Applications. *J. Low Power Electron. Appl.* **2021**, *11*, 40. [CrossRef]
33. Aiello, O.; Crovetti, P.; Lin, L.; Alioto, M. A pW-Power Hz-Range Oscillator Operating With a 0.3–1.8-V Unregulated Supply. *IEEE J. Solid-State Circuits* **2019**, *54*, 1487–1496. [CrossRef]
34. Buzzin, A.; Asquini, R.; Caputo, D.; de Cesare, G. Evanescent waveguide lab-on-chip for optical biosensing in food quality control. *Photonics Res.* **2022**, *10*, 1453–1461. [CrossRef]
35. Aiello, O. Electromagnetic Susceptibility of Battery Management Systems' ICs for Electric Vehicles: Experimental Study. *Electronics* **2020**, *9*, 510. [CrossRef]
36. Aiello, O.; Crovetti, P.; Alioto, M. 5.2 Capacitance-to-Digital Converter for Operation Under Uncertain Harvested Voltage down to 0.3V with No Trimming, Reference and Voltage Regulation. In Proceedings of the 2021 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 13–22 February 2021; pp. 13–22. [CrossRef]
37. Rodovalho, L.H.; Aiello, O.; Rodrigues, C.R. Ultra-Low-Voltage Inverter-Based Operational Transconductance Amplifiers with Voltage Gain Enhancement by Improved Composite Transistors. *Electronics* **2020**, *9*, 1410. [CrossRef]
38. Ballo, A.; Grasso, A.D.D.; Pennisi, S.; Susinni, G. A 0.3-V 8.5-µ a Bulk-Driven OTA. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **2023**, *31*, 1444–1448. [CrossRef]
39. Ballo, A.; Carvajal, R.G.; Grasso, A.D.; Luján-Martínez, C.I.; Pennisi, S.; Venezia, C. 0.35-V SR-Enhanced Bulk-Driven OTA for Loads up to 10 nF. *IEEE Trans. Circ. Syst. I* **2024**, 1–9. [CrossRef]

40. Della Sala, R.; Centurelli, F.; Monsurró, P.; Scotti, G. On the Feasibility of Cascode and Regulated Cascode Amplifier Stages in ULV Circuits Exploiting MOS Transistors in Deep Subthreshold Operation. *IEEE Access* **2024**, *12*, 73292–73303. [CrossRef]
41. Kumngern, M.; Aupithak, N.; Khateb, F.; Kulej, T. 0.5 V Fifth-Order Butterworth Low-Pass Filter Using Multiple-Input OTA for ECG Applications. *Sensors* **2020**, *20*, 7343. [CrossRef] [PubMed]
42. Khateb, F.; Kulej, T.; Vlassis, S. Extremely Low-Voltage Bulk-Driven Tunable Transconductor. *Circuits Syst. Signal Process.* **2017**, *36*, 511–524. [CrossRef]
43. Kulej, T.; Khateb, F.; Arbet, D.; Stopjakova, V. A 0.3-V High Linear Rail-to-Rail Bulk-Driven OTA in 0.13 μm CMOS. *IEEE Trans. Circuits Syst. II* **2022**, *69*, 2046–2050. [CrossRef]
44. Jaikla, W.; Khateb, F.; Kumngern, M.; Kulej, T.; Ranjan, R.K.; Suwanjan, P. 0.5 V Fully Differential Universal Filter Based on Multiple Input OTAs. *IEEE Access* **2020**, *8*, 187832–187839. [CrossRef]
45. Rodovalho, L.H.; Ramos Rodrigues, C.; Aiello, O. Self-Biased and Supply-Voltage Scalable Inverter-Based Operational Transconductance Amplifier with Improved Composite Transistors. *Electronics* **2021**, *10*, 935. [CrossRef]
46. Kulej, T. 0.5-V bulk-driven CMOS operational amplifier. *IET Circuits Devices Syst.* **2013**, *7*, 352–360. [CrossRef]
47. Kulej, T.; Khateb, F. Design and implementation of sub 0.5-V OTAs in 0.18-μm CMOS. *Int. J. Circuit Theory Appl.* **2018**, *46*, 1129–1143. [CrossRef]
48. Kulej, T.; Khateb, F. A Compact 0.3-V Class AB Bulk-Driven OTA. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **2019**, *28*, 224–232. [CrossRef]
49. Kulej, T.; Khateb, F. A 0.3-V 98-dB rail-to-rail OTA in 0.18 μm CMOS. *IEEE Access* **2020**, *8*, 27459–27467. [CrossRef]
50. Khateb, F.; Kulej, T. Design and Implementation of a 0.3-V Differential Difference Amplifier. *IEEE Trans. Circ. Syst. I* **2018**, *66*, 513–523. [CrossRef]
51. Della Sala, R.; Centurelli, F.; Monsurrò, P.; Scotti, G.; Trifiletti, A. A 0.3V rail-to-rail three-stage OTA with high DC gain and improved robustness to PVT variations. *IEEE Access* **2023**, *11*, 19635–19644. [CrossRef]
52. Kulej, T.; Khateb, F. 0.4-V bulk-driven differential-difference amplifier. *Microelectron. J.* **2015**, *46*, 362–369. [CrossRef]
53. Kulej, T. 0.4-V bulk-driven operational amplifier with improved input stage. *Circuits Syst. Signal Process.* **2015**, *34*, 1167–1185. [CrossRef]
54. Kulej, T. 0.5-V bulk-driven OTA and its applications. *Int. J. Circuit Theory Appl.* **2015**, *43*, 187–204. [CrossRef]
55. Khateb, F.; Kulej, T.; Akbari, M.; Steffan, P. 0.3-V bulk-driven nanopower OTA-C integrator in 0.18 μm CMOS. *Circuits Syst. Signal Process.* **2019**, *38*, 1333–1341. [CrossRef]
56. Centurelli, F.; Della Sala, R.; Monsurró, P.; Scotti, G.; Trifiletti, A. A novel OTA architecture exploiting current gain stages to boost bandwidth and slew-rate. *Electronics* **2021**, *10*, 1638. [CrossRef]
57. Della Sala, R.; Spinogatti, V.; Bocciarelli, C.; Centurelli, F.; Trifiletti, A. A 0.15-to-0.5 V Body-Driven Dynamic Comparator with Rail-to-Rail ICMR. *J. Low Power Electron. Appl.* **2023**, *13*, 35. [CrossRef]
58. Aiello, O.; Crovetti, P.; Toledo, P.; Alioto, M. Rail-to-Rail Dynamic Voltage Comparator Scalable Down to pW-Range Power and 0.15-V Supply. *IEEE Trans. Circuits Syst. II* **2021**, *68*, 2675–2679. [CrossRef]
59. Sala, R.D.; Centurelli, F.; Scotti, G.; Palumbo, G. Rail to Rail ICMR and High Performance ULV Standard-Cell-Based Comparator for Biomedical and IoT Applications. *IEEE Access* **2024**, *12*, 4642–4659. [CrossRef]
60. Sala, R.D.; Bocciarelli, C.; Centurelli, F.; Spinogatti, V.; Trifiletti, A. A Novel Ultra-Low Voltage Fully Synthesizable Comparator exploiting NAND Gates. In Proceedings of the 2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), Valencia, Spain, 18–21 June 2023; pp. 18–21. [CrossRef]
61. Aiello, O.; Crovetti, P.; Alioto, M. Fully Synthesizable, Rail-to-Rail Dynamic Voltage Comparator for Operation down to 0.3 V. In Proceedings of the 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 27–30 May 2018; pp. 27–30. [CrossRef]
62. Ballo, A.; Pennisi, S.; Scotti, G. 0.5 V CMOS Inverter-Based Transconductance Amplifier with Quiescent Current Control. *J. Low Power Electron. Appl.* **2021**, *11*, 37. [CrossRef]
63. Chen, T.; Naffziger, S. Comparison of adaptive body bias (ABB) and adaptive supply voltage (ASV) for improving delay and leakage under the presence of process variation. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **2003**, *11*, 888–899. [CrossRef]
64. Eireiner, M.; Henzler, S.; Georgakos, G.; Berthold, J.; Schmitt-Landsiedel, D. Local Supply Voltage Adjustment for Low Power Parametric Yield Increase. In Proceedings of the 2006 32nd European Solid-State Circuits Conference, Montreux, Switzerland, 19–21 September 2006; pp. 98–101. [CrossRef]
65. Cha, S.; Milor, L. Adaptive supply voltage and duty cycle controller for yield-power optimization of ICs. In Proceedings of the 2017 7th IEEE International Workshop on Advances in Sensors and Interfaces (IWASI), Vieste, Italy, 15–16 June 2017; pp. 133–138. [CrossRef]
66. Nielsen, L.S.; Niessen, C.; Sparso, J.; van Berkel, K. Low-power operation using self-timed circuits and adaptive scaling of the supply voltage. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **1994**, *2*, 391–397. [CrossRef]

Journal of
Low Power Electronics and Applications

MDPI

Article

A Power-Gated 8-Transistor Physically Unclonable Function Accelerates Evaluation Speeds

Yujin Zheng *, Alex Yakovlev and Alex Bystrov

Microsystems Group, School of Engineering, Newcastle University, Newcastle upon Tyne NE1 7RU, UK; alex.yakovlev@newcastle.ac.uk (A.Y.); a.bystrov@newcastle.ac.uk (A.B.)
* Correspondence: y.zheng26@newcastle.ac.uk

Abstract: The proposed 8-Transistor (8T) Physically Unclonable Function (PUF), in conjunction with the power gating technique, can significantly accelerate a single evaluation cycle more than 100,000 times faster than a 6-Transistor (6T) Static Random-Access Memory (SRAM) PUF. The 8T PUF is built to swiftly eliminate data remanence and maximise physical mismatch. Moreover, a two-phase power gating module is devised to provide controllable power on/off cycles for the chosen PUF clusters in order to facilitate fast statistical measurements and curb the in-rush current. The architecture and hardware implementation of the power-gated PUF are developed to accommodate fast multiple evaluations of PUF *Responses*. The fast speed enables a new data processing method, which coordinates Dark-bit masking and Multiple Temporal Majority Voting (TMV) in different Process, Voltage and Temperature (PVT) corners or during field usage, hence greatly reducing the Bit Error Rate (BER) and the hardware penalty for error correction. The designs are based on the UMC 65 nm technology and aim to tape out an Application-Specific Integrated Circuit (ASIC) chip. Post-layout Monte Carlo (MC) simulations are performed with Cadence, and the extracted PUF *Responses* are processed with Matlab to evaluate the 8T PUF performance and statistical metrics for subsequent inclusion in PUF *Responses*, which comprise the novelty of this approach.

Keywords: physically unclonable function; PUF; power gating; SRAM; dark bit; metastability; data remanence; data retention; reset

1. Introduction

1.1. Background

The Internet of Things (IoT) market is growing fast in annual revenue. However, this globally interconnected world poses a much more severe challenge to security. Due to the extremely resource-constrained nature of many IoT devices, e.g., wearables, lightweight security schemes and enhanced energy efficiency are consequently in great demand. To build a strong physical cyber-defence capability from the very start of the Integrated Circuit (IC) design [1], PUFs are promising hardware security primitives because they are easy to evaluate and physically hard to duplicate [2]. PUFs are functions that map *Challenges* to *Responses* through physically unclonable devices [2,3], and each PUF device is unique. Their uniqueness comes from the uncontrollable physical parameter mismatch generated in semiconductor fabrication. The proposed 8T PUF is derived from conventional 6T-SRAM. SRAM is an indispensable part of mainstream embedded designs because of its symmetric structure and mass entropy. The SRAM PUF was first proposed by Guajardo et al. [4] and Holcomb et al. [5], who discovered the intrinsically random start-up values of SRAM cells. Accordingly, these repeatable start-up values are the raw data for creating the *Response* of the PUF, and the address used to read them is the *Challenge*, as shown in Figure 2.

However, in a small number of SRAM cells, random logical states inevitably appear after every power-up due to negligible physical mismatch. They cause unreliable PUF readings, which cannot be tolerated for authentication. Moreover, some stable cells become

unstable with the change in environmental conditions, such as temperature or supply voltage, because the physical mismatch in cells is affected, e.g., the threshold voltages of transistors.

One PUF application is extracting and regenerating *Secret Keys*. The raw data read from the PUF cells are the source for creating *Secret Keys*. The keys are normally extracted during manufacturing in a stable nominal temperature and voltage condition and regenerated in the field with various environmental conditions. Since no error can be tolerated for *Secret Key* application, there are some requisite techniques for identifying unstable PUF cells during manufacturing, such as Multiple Evaluation [6], TMV [6–9], Dark-bit masking [7–10], etc. Then, the stable cells can be used to derive the *Secret Key* for authentication. Whilst the keys are regenerated in the field, SRAM PUF is sensitive to environmental changes and ambient noise, which both cause bit errors. However, time is too limited to execute any aforementioned techniques to reduce errors. Thus, bit error correction techniques are vital, such as BCH codes [11], Hamming codes [12], etc. For error correction and its required PUF entropy, the hardware overheads increase exponentially with the growth in error numbers [13]. This is unsuitable for lightweight IoT applications.

1.2. Main Contributions

Two fundamental circuits are built in this work: one is the custom 8T PUF in Figure 1a; the other is the two-phase power gating cell in Figure 1b. A single-phase power gating cell is also implemented for comparison, as shown in Figure 1c. Based on these circuits, a power-gated 8-Transistor (8T) PUF architecture presented in Figure 2 is developed to alleviate some of the aforementioned issues. This power gating structure can also be utilised with the other bistable PUFs to improve PUF performance. The main contributions are listed below:

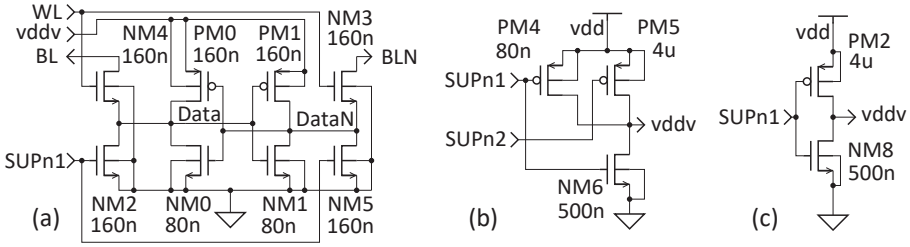


Figure 1. Schematics of (**a**) 8T PUF cell, (**b**) two-phase power gating cell and (**c**) single-phase power gating cell.

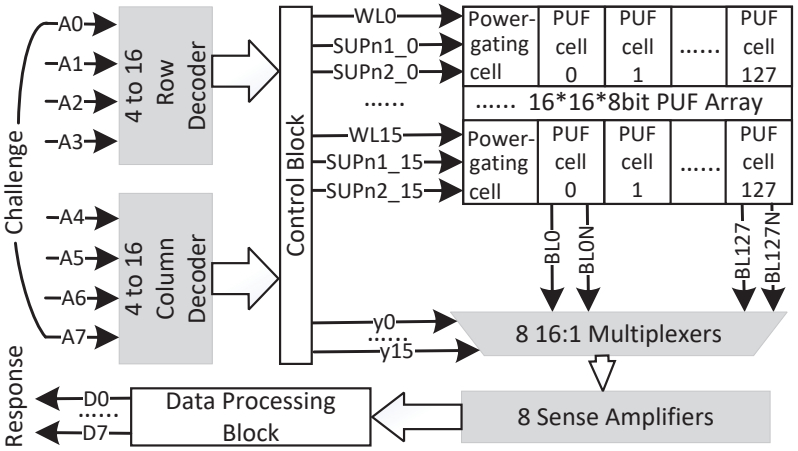


Figure 2. A two kilo-bit power-gated PUF architecture.

- **The custom 8T PUF facilitates fast statistical measurements and improves security:** The 8T PUF maximises physical mismatch and eliminates data retention swiftly for

high-speed evaluations and countering security attacks [14–18]. It does not require a special process for high-density SRAM manufacturing and can be fabricated in the same process as microcontrollers (MCUs). Fast statistical measurements can be performed on this platform to extract raw PUF bits. These raw bits are then processed and marked onto a bitmap to identify the PUF cell instability. These unstable bits, which are discarded in the references, can be used for *True Random Number* generation or as part of the PUF *Response* [19–22].

- **Two-phase power gating improves PUF performance and security whilst saving energy and delaying ageing:** This newly developed power-switching process includes three stages:
  1. Reset stage: The reset stage drops the virtual power supply (vddv), quickly drains the remaining current and eliminates retained data.
  2. Phase I power-up stage: Phase I slowly powers up the chosen PUFs to prolong the metastability-resolving process in the hope of reducing EMI and crosstalk amongst PUF cells [23].
  3. Phase II power-up stage: Finally, phase II speeds up the voltage ramp-up process.

  In addition, different combinations of power gating parameters can curb the in-rush current, thus shielding it from side channel attacks, e.g., Differential Power Analysis (DPA) [14,15]. Moreover, the 8T PUF cells are partitioned into rows, and only the chosen rows will be powered up during the reading process. Besides saving energy proportionally, PUF cells without a power supply cannot be read out and are protected from security attacks. Furthermore, power gating can delay the transistor ageing effect.
- **A new data processing method marks out most errors:** The high-speed measurements not only reduce the time needed for the enrolment phase in manufacturing but also enable multiple evaluations in the key regeneration phase. Since the positions of the unstable PUF cells drift away in different voltage or temperature corners, and extreme corners cause more unstable PUF cells, TMV plus Dark-bit masking in nominal conditions [7–9] is insufficient. We propose a new data processing method here. First, during manufacturing, Multiple TMV under nominal conditions and extreme corners are used to mark out unstable readings and flipped readings as Dark bits onto a bitmap. Then, during field usage, the Dark bits are discarded first and followed by the regeneration of Secret Keys using fast TMV. Finally, with a significantly reduced number of error bits remaining, an error correction technique with a lower hardware penalty will be applied. When the BER drop close to 0%, the hardware penalty for error correction can be reduced significantly. The stability levels of PUFs are also recorded on the bitmap. These unstable readings can be used further for True Random Number generation or as part of the PUF *Response*.

1.3. State of the Art and Related PUF Works

Before starting a new silicon-based PUF design, the implementation method needs to be considered first. The silicon-based PUFs can be implemented in an ASIC or a Field-Programmable Gate Array (FPGA). Since FPGAs have ready-to-use resources and can be purchased off-the-shelf, many early PUF works are based on FPGAs [2–4]. However, ASIC-based PUFs can offer far more energy and have a cost-efficient design, which is crucial for lightweight IoT devices [8,9,24–34]. However, FPGA-based PUFs [35–41] are indispensable parts for applications which are not area or energy sensitive but time sensitive instead. In addition, FPGA is a feasible platform for assessing PUF design methods and performance. There are several novel FPGA-based bistable PUF works [36–41], which we intend to implement in our test chip with the power gating method to compare the metastable behaviour and PUF performance.

There are several PUF applications [42–45] that previously applied the power gating method, but their purposes and implementations are different to this approach. Maes et al. [42] implemented power-gated PUF blocks for further investigation. Xu et al. [43] utilised the random duration of multiple power gating to replace voltage control so as

to induce failure patterns to determine the Data Retention Voltage (DRV). In comparison, our design diminishes data retention swiftly for high-speed evaluation. Although with a different purpose, this research and its predecessor [46] have clarified that "a strong DRV fingerprint is correlated with power-up tendency". This substantiates that the stability or instability degrees of PUF cells come from their innate physical mismatch. However, it can be seen that 40 μs is not enough to eliminate retention data at 25 °C. In 2020, a 2D power gating scheme to relieve an enhancement–enhancement (EE) SRAM PUF from short-circuit currents and also to protect PUF data from attacks was presented by Liu et al. [44]. However, there was no consideration of the major power gating parameters, such as the *SLEEP* transistor design [47], power distribution network [48], etc. This scheme also has a half-selected cell problem, which requires additional peripheral circuits to lower the extra energy consumption.

1.4. Paper Structure

The remainder of this paper is organised as follows. Section 2 describes the power-gated PUF architecture, the 8T PUF design, the two-phase power gating implementation and a new data processing method combining Multiple TMV and Dark-bit masking. Section 3 firstly analyses the power gating parameters, then compares the power-gated 8T PUF behaviour with the 6T PUF, and lastly discusses the importance of a thorough reset for PUF applications. Section 4 measures the processed data for a PUF property comparison. Finally, Section 5 concludes the main contributions and outlines the ongoing work and future plan.

2. Power-Gated PUF Architecture and Design Methods

An example architecture of a power-gated PUF array is illustrated in Figure 2. This architecture consists of some general SRAM function blocks in grey, a 2 kilo-bit power-gated PUF array and two functional blocks, i.e., a Control block and a Data Processing block. The two function blocks will be implemented and evaluated in due course.

- **Challenge–Response pair (CRP):** The 8-bit address inputs are the PUF *Challenges*, and the 8-bit corresponding data outputs are the PUF *Responses*. Together, they form a Challenge–Response pair (CRP).
- **PUF array:** In the PUF array, there are 128 PUFs in a row gated by a power gating cell. Since the main purpose of power gating is facilitating fast evaluations by switching the power supply, the general term *SLEEP* for normal power gating is replaced by *SUPPLY* in this work.
- **Control block:** The switching activity is controlled by the Control block. Apart from passing the decoded higher 4-bit address to choose an 8-bit word from 16:1 multiplexers, it generates *SUPn1*, *SUPn2* and *WL* (Word Line) signals from the decoded lower 4-bit address. Once a PUF row is chosen by the lower 4-bit address, the *SUPn1* signal is discharged to '0' to switch on the power supply. After *Data* are settled down, the *SUPn2* will be discharged to '0', and *WL* will be asserted to '1' in sequence for a reading process. Then, in the Reset stage, both *SUPn1* and *SUPn2* signals are asserted to '1'. There will be no power supply to the PUF cells, and the data will be discharged to '0'. The protocol of the two-phase power gating method is shown in Figure 3.

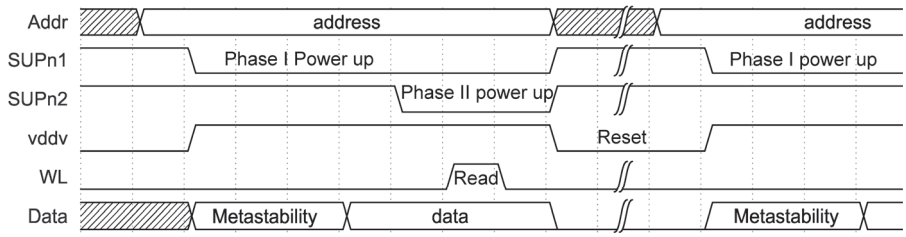


Figure 3. Protocol of two-phase power gating.

- **Data Processing block:** The Data Processing block is there to evaluate the raw read-out bits and marking out different stability levels of each PUF cell. Using TMV under nominal or various voltage and temperature conditions is to sift the unstable or flipped bits to achieve a lower Bit Error Rate (BER).

The input vectors and the output vectors of multiple PUF arrays can be concatenated to match the PUF entropy requirement. The parameters of this architecture, e.g., the type of PUF cell, the number of rows or columns, word width, etc., can be altered for various purposes or implemented in different fabrication techniques. It is worth noting that with larger PUF array dimensions, the sizes of *SUPPLY* transistors need to be evaluated. The driven ability of *SUPn1* and *SUPn2* signals needs to be improved.

The design is implemented with UMC 65 nm technology. The layout of one test circuit is partly illustrated in Figure 4. It includes rows of two-phase power-gated 8T PUFs on the left-hand side and rows of single-phase power-gated 6T-SRAM PUFs on the right-hand side for comparison. Each row has 128 PUF cells.

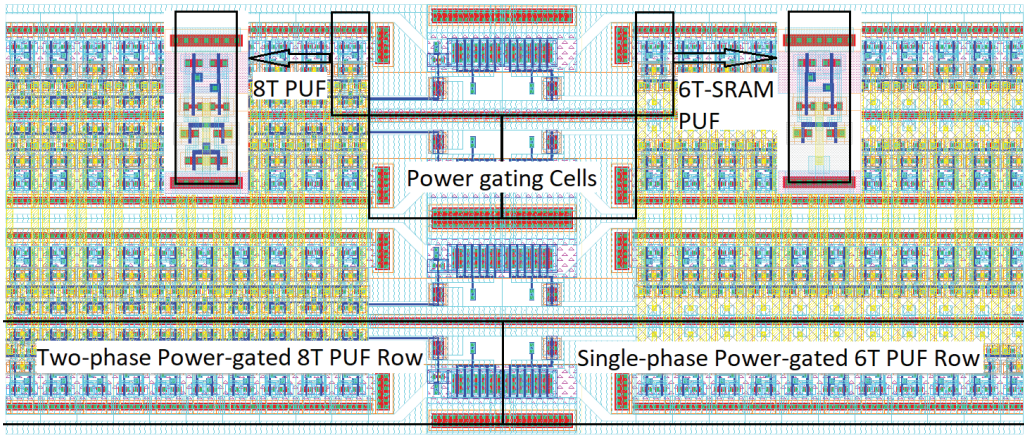


Figure 4. Part of the power-gated PUF test circuit layout.

2.1. 8-Transistor PUF Design

A distinctive feature of the 8T PUF is preparing a clean status for the next power-on cycle with a high reset speed. This clean status means attackers cannot read out any retention data. Unlike some 8T SRAM designs [49,50] concentrating on improving the write margin and dealing with the opposite requirements for read stability and write ability, this 8T PUF abandons the write function and keeps only the SRAM read ability. The physical parameter mismatch, which affects SRAM stability, is actually a vital feature of PUFs. Since mismatch amongst transistors increases with the scaling down the physical size, the 8T PUF uses the smallest transistor to maximise the mismatch. An 8T PUF can be fabricated by the same process as MCUs, so a special process for high-density SRAM is not needed.

The 8T PUF cell shown in Figure 1a stems from conventional 6T-SRAM [51]. Four transistors, namely *PM0*, *PM1*, *NM0* and *NM1*, make up two cross-coupled inverters for storing data. The unique PUF readings predominantly come from the threshold voltage mismatch among these transistors. After powering up, the mutual input and output nodes, i.e., *Data* and *DataN*, both reach a metastable state [52], at which time the outputs of two cross-coupled inverters are lingering between logical '0' and '1', then cross it and settle in one of these stable states. *NM4* and *NM3* are access transistors. They connect the internal nodes *Data* and *DataN* to bit lines *BL* and *BLN*. In addition, two NMOS transistors *NM2* and *NM5* are designed to rapidly discharge the *Data* and *DataN* nodes during the reset stage with both *SUPn1* and *SUPn2* signals asserting. As a result, the reset time can be shortened by 5 orders of magnitude, i.e., from 120 microseconds to 1 nanosecond, hence facilitating high-rate PUF evaluation. Furthermore, no data remanence can be exploited by attackers [53,54]. The PUF layouts were implemented symmetrically. During the evaluations, it is shown that a tiny bias of layout influences the proportion of the ones and

zeros of the PUF readings. With two additional transistors, the area cost of the 8T PUF is 13.2% more than its 6T-SRAM PUF counterpart, which was implemented for comparison as shown in Figure 4.

2.2. Two-Phase Power Gating Method and Design

Originally, the power gating technique was introduced to reduce leakage, which is independent of the transistor switching activity and thus lessens power dissipation. This design eliminates the leakage current from unchosen PUF rows, so the energy consumption is roughly proportional to the chosen PUF percentage. In the two-phase power gating method, the power gating cells switch the chosen rows of PUF cells on and off in three stages: a reset stage, phase I power-up and phase II power-up. First and foremost, this enables fast statistical evaluations, which improve PUF performance. Secondly, this method facilitates different combinations of power gating parameters in hardware implementation, so that the in-rush current can be curbed by adjusting these parameters. The flattened currents provide a method against side channel attacks. Moreover, PUF rows without power supply cannot be read out and are protected from security attacks.

Conventional power gating is conducted via a *SLEEP* transistor to enable a power or ground connection [47]. Figure 1b shows the single-phase power gating cell is operated via a PMOS transistor *PM2* as a *SUPPLY* transistor to switch power on/off and an NMOS transistor *NM8* for fast resetting. As illustrated in Figure 1c, the two-phase power gating cell employs two PMOS transistors as *SUPPLY* transistors for two-stage power switching and an NMOS transistor *NM6* for resetting. In the test circuits, each power gating cell controls the power supply of a row of 128 PUF cells. The reset transistor *NM6* quickly drains the remaining current and drops *vddv* to 0 V. Since a smaller transistor curbs the drain current and the *vddv* output, the two-phase power gating exploits this to generate a gentle voltage incline with a smaller *SUPPLY* transistor *PM4* in phase I and create a steep slope of *vddv* using a larger *SUPPLY* transistor *PM5* in phase II. Consequently, the metastability resolving time in phase I is lengthened in the hope of minimum mutual disturbance amongst PUF cells. Meanwhile, if all PUF cells start metastability in a very short period of time, the in-rush current will be significant due to all the cross-coupled transistors in 8T PUF cells being in saturation mode. The prolonged phase I is able to flatten the current peak as well. Afterwards, phase II takes control and increases *vddv* swiftly. The sizes of two *SUPPLY* transistors and the time duration of the two phases need to be evaluated to obtain the best trade-off. This will be discussed in the evaluation part in Section 3.1.

2.3. Multiple TMV and Dark-Bit Masking

In some previous methods combining TMV with Dark-bit masking [7–9], TMV cannot eliminate the unstable bits in different environmental conditions, and the Dark-bit mismatch increases bit errors more than 10-fold during field usage. This is because the physical mismatch, e.g., the threshold voltages, vary under different voltages or temperatures. Hence, some stable cells become unstable and vice versa. However, there are some cells that even change their bias tendency and flip their readings. PUF cells with flipped readings cannot be distinguished by TMV under nominal condition.

We introduce a Multiple TMV method with additional TMV thanks to the high-speed evaluation enabled by the proposed design and architecture. During manufacturing, the golden reading is extracted using TMV in the nominal condition first. Then, by comparing the TMV results at all worst corners with the golden reading, any flipped bits and unstable bits are marked as Dark bits. Afterwards, while the *Secret Key* regenerates in the field, the marked-out Dark bits will be eliminated from the raw data first. Then TMV will be executed next, and the unstable bits at this moment are the error bits. Then, these error bits will be corrected with the error correction technique with a lower hardware penalty. The simulation results show that the BER can drop to 0%, which is presented in Section 4.

3. Evaluations and Results Analyses

Due to the sensitivity of bistable PUFs, e.g., the 8T PUF and the SRAM PUF, many aspects of parameter mismatch count for the PUF stability. Although the layouts were implemented symmetrically to avoid human-made bias, the physical parameters still exhibit variations. For this reason, post-layout simulation is a much more accurate way to evaluate the sizes of *SUPPLY* transistors and measure PUF performance, such as uniqueness, robustness and randomness. For various evaluation purposes, different simulation methods were executed with corresponding test circuits.

3.1. Power Gating Parameter Evaluation

A DC sweep and post-layout transient simulations were performed to evaluate the size of *SUPPLY* transistors for a cluster of 128 PUF cells and the corresponding behaviour of the PUF cells.

For two-phase power gating, the phase one *SUPPLY* transistor *PM4* must be small enough to prolong the metastability process. Meanwhile, the phase two *SUPPLY* transistor *PM5* should be large enough to supply power to 128 PUF cells quickly. As presented in Figure 5, there is a roughly linear relationship between the *SUPPLY* transistor width and the approximate value of the *vddv* plateau while metastability resolves. There is also a nearly quadratic dependence between the *SUPPLY* transistor width and the time duration for *vddv* to reach 1.2 V or the metastability resolving time duration. Hence, by varying the size of the *SUPPLY* transistor, the metastability resolving time can be manipulated.

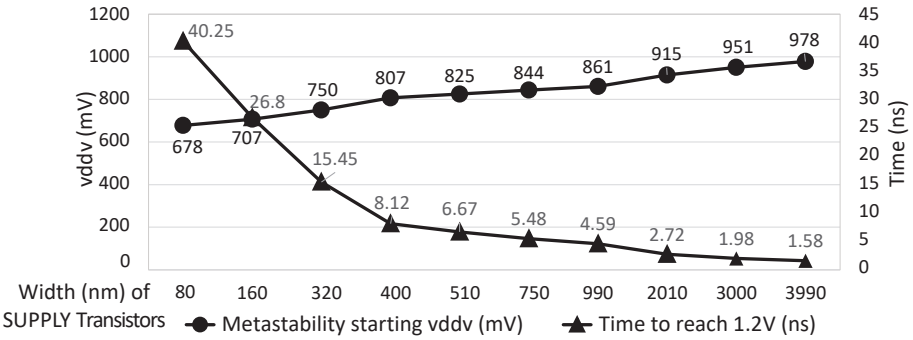


Figure 5. *SUPPLY* transistor sizes vs. metastability starting vddv and time to reach 1.2 V.

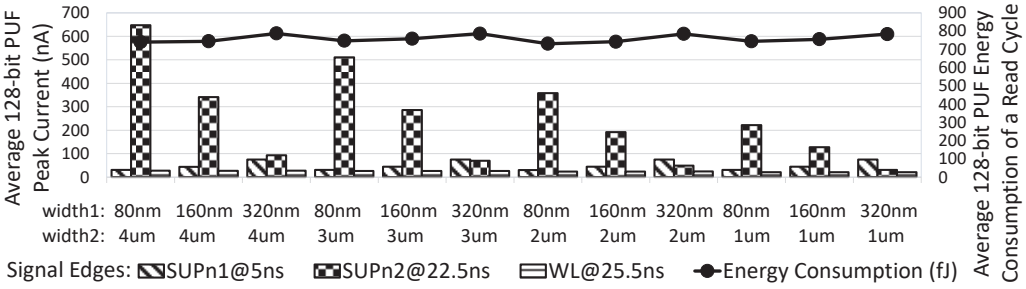


Figure 6. *SUPPLY* transistor sizes vs. currents and energy consumption.

Phase I *SUPPLY* transistor widths of 80 nm to 320 nm and phase II *SUPPLY* transistor widths of 1 µm to 4 µm were picked to evaluate various combinations of two-phase power gating. Figure 6 illustrates the comparison of the current peaks of different signal edges in different combinations of *SUPPLY* transistors whilst power gating a 128-bit PUF. It can be seen that a higher power-up current corresponds to a larger *SUPPLY* transistor. The phase II current also relates to the *vddv* value at the start point of phase II. The energy consumption of a PUF cell for each reading cycle exhibits minimal variation, i.e., from 5.7 fJ to 6.2 fJ. These adjustable power-up currents can limit the in-rush current and be exploited further as a candidate against side channel attacks. In our design, the SUPPLY

transistor combination of 80 nm for PM4 and 4 µm for PM5 is implemented to emphasise the prolonged PUF metastability-resolving process and the rapid reset process.

The power consumption of a power-gated PUF array is proportional to the chosen PUF percentage, in addition to the power consumption of the power-gating cells. The post-layout simulation results show that the power consumption is about 36.5% when only a quarter of PUF rows are enabled. For example, a row of 128 8T PUFs consumes 954 fJ in an array of four PUF rows, which consume 2.613 pJ under the same conditions. The dynamic power of one two-phase power gating cell is about 812.5 aJ.

3.2. Power-Gated PUF Behaviour

To examine the PUF behaviour of 8T PUFs, post-layout Monte Carlo simulations with a Gaussian distribution of transistor threshold voltages were carried out under nominal conditions, i.e., a supply voltage of 1.2 V, an ambient temperature of 27 °C and a *Typical–Typical (TT)* process corner. The test circuit includes a row of 128 two-phase power-gated 8T PUFs and a row of 128 single-phase power-gated 6T-SRAM PUFs on the right-hand side for comparison.

The 128-run Monte Carlo simulation results illustrate the different power-up and reset behaviours of PUF cells, as shown in Figure 7. In Figure 7a, with a 4 µm width *SUPPLY* transistor, the *vddv* of single-phase power gating reaches 1.2 V in roughly 1 ns, whilst quickly resolving the metastability of inside node pairs, i.e., *Data* and *DataN*. In contrast, Figure 7b illustrates that *vddv* reaches around 0.7 V in 5 ns and lingers for about 4 ns, then gradually climbs up towards 1.2 V at phase I power-up with the *SUPPLY* transistor width of 80 nm. Following this, with a 4 µm width *SUPPLY* transistor, phase II starts from 22.5 ns and swiftly increases *vddv* to 1.2 V in around 1 ns with the help of the 80 nm *SUPPLY* transistor. It can be seen that the low start-up voltages in phase I lengthen the metastability resolving time of 8T PUFs. Simultaneously, *Data* and *DataN* start wrestling while *vddv* is ramping up slowly, then escape out of metastability and tend to their distinct logical status in various resolving times due to their intrinsically varied physical parameters. These opposite tendencies of *Data* and *DataN* resemble the random PUF behaviour in real circuits.

After powering up, the *WL* signal asserts at 25 ns for data reading. Finally, in the reset stage, PUF cells are powered down. The remaining currents are drained away quickly from the 8T PUF cells within 1 ns. However, the traditional 6T-SRAM PUFs still have data retention, which not only affects the initial states of *Data* and *DataN* pairs in the following cycles but also can be targeted by attackers. It is worth noting that with the technology scaling down from 90 nm to 65 nm, the reset period for the same 6T-SRAM design lengthens from 5 µs to 120 µs, as listed in Table 1.

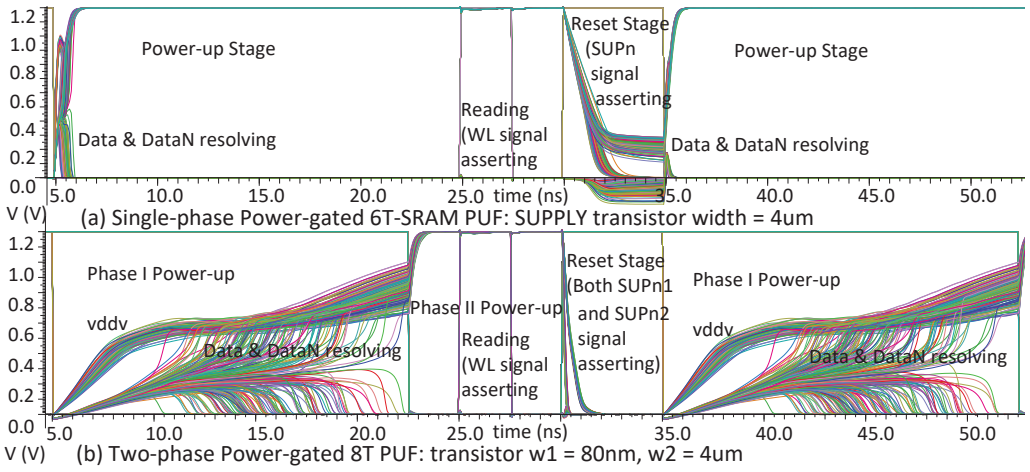


Figure 7. Waveforms of a 128-run post-layout Monte Carlo simulation.

Table 1. Reset periods in comparison.

	HOST 2012 [6]	DFT 2012 [55]	ESSCIRC 2014 [10]	DFT 2016 [20]	DATE 2023 [56]	This Work	This Work
Design	6T-SRAM	6T-SRAM	Hybrid	DFF	6T-SRAM	6T-SRAM	8T PUF
Technology	65 nm	45 nm	22 nm	45 nm	90 nm	65 nm	65 nm
Reset Time	1 ms	1 s	1 s	50 µs	5 µs	120 µs	1 ns

3.3. Reset Period and Effect

Without resetting thoroughly, the assessment of the PUF characteristics can be misguiding. One piece of evidence is that with the data remanence, the under-reset 6T-SRAM PUF readings do not change in more than 200,000 runs of a Monte Carlo simulation compared to the 8T PUF. This creates a deceptive deduction that the 6T-SRAM PUF cells are 100% stable in nominal conditions [57]. However, if the reset time duration is prolonged to 120 µs with 65 nm technology, the simulation results show that the stability of the thoroughly reset 6T-SRAM PUF will be affected in the same way as the 8T PUF, as illustrated in Figure 8. Long duration transient simulations were conducted with intensified noise. In these simulations, the 8T PUF cell, with the help of two discharging NMOS transistors, can reset two internal data nodes to the absolute values below 10 mV within 1 ns, while the 6T-SRAM PUF can barely achieve the same reset level even in 100 µs.

This reset issue has been overlooked because most research does not switch power at such high frequencies, as listed in Table 1. Consequently, the longer power-off periods result in a better reset quality under the same conditions.

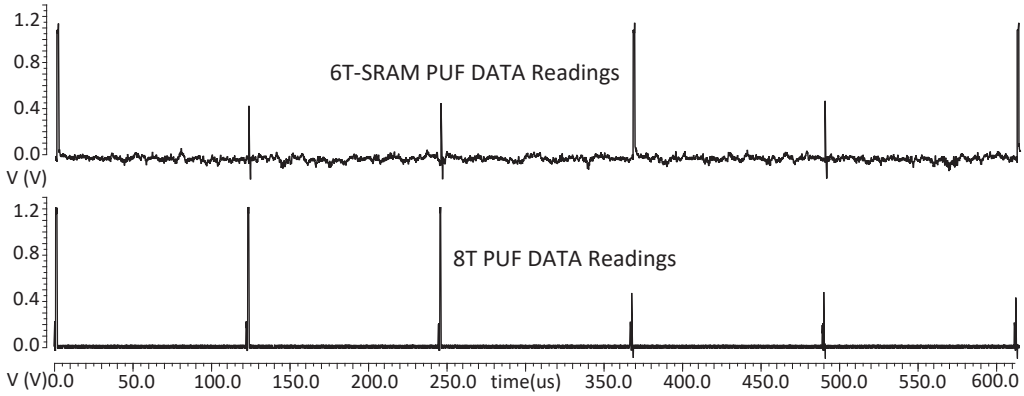


Figure 8. Transient noise simulation with a 120 µs reset period.

4. 8-Transistor PUF Performance Measurements

To assess the PUF performance, 5G transient noise, including thermal noise, flicker noise, shot noise, etc., was added to the post-layout Monte Carlo simulations because all 8T PUF cells and 6T-SRAM PUF cells were stable in nominal conditions without any external noise. For the two-phase power gating *SUPPLY* transistors, an 80 nm width was chosen for phase I, and 4 µm was chosen for phase II. Meanwhile, the 6T-SRAM PUF was examined under the same conditions for comparison. In addition to nominal conditions, the design was evaluated under different PVT corners, i.e., temperatures from −40 °C to 85 °C and supply voltages from 0.8 V to 1.6 V, and the process corners included *Slow–Slow (SS)*, *Fast–Fast (FF)* etc. For quantitative evaluation, clusters of 2048 PUF cells were read out for 100 power on–off cycles of 60 ns. This resembles 100 times the same *Challenge*. The 100 2048-bit read-out strings are the PUF *Responses*. Furthermore, the PUF clusters imitate different PUF devices. With a thorough reset, these PUF characteristics are able to be assessed with post-layout simulations. The intensive multiple simulations here aim to examine the PUF properties to prepare for prototype chip fabrication, so the extracted data were then processed with Matlab to acquire PUF robustness, uniqueness, randomness, etc.

The results were compared with some prior work in Table 2. It is worth noting that the works [8,9,25,58–61] are ASIC-based measurements, and only [62] and this work include simulation-based evaluations. In fact, post-layout simulations are very resource and time consuming, so only a few works, e.g., [62], can extract data from schematic-based simulations.

Table 2. PUF performance comparison.

Measurement			**CMOS**	**Chip-Based**				**Simulation-Based**	
	ISSCC 2014 [8]	**ISSCC 2015 [58]**	**ISSCC 2016 [59]**	**JSSC 2017 [9]**	**JSSC 2020 [44]**	**JSSC 2022 [60]**	**Electronics 2023 [61]**	**IJCTA 2017 [62]**	**This Work**
Technology	22 nm	65 nm	45 nm	14 nm	130 nm	180 nm	130 nm	65 nm	65 nm
Bitcell Area (μm^2)	4.66	25.35	5.3	1.84	6.3	223	72.03	-	4.19
Bitcell Area (F^2)	9632	6000	2613	9388	373	7222	4262.13	-	992
Unstable Bits	30%	1.73%	-	26.37%	2.14%	0.61%	0.586%	0.32% $^{\Delta}$	7.71%
Native BER	-	-	0.1%	5.76%	0.21%	0.13%	0.49%	-	1.17%
Worst BER	6%	4.56% *	2.84%	6.78%	0.34%	1.1%	3.125%	-	12.21%
Stabilised BER	0.97%	1.73%	0.21%	1.46%	0%	0.13%	-	-	0%
Intra-distance	2.58%	0.92%	-	3.4%	0.3%	0.16%	0.491%	2.25% $^{\Delta}$	1.45%
Inter-distance	49%	50.14%	49.8%	48.6%	49.23%	49.3%	50.12%	-	50.67%
Mask Ratio	11%	-	18.5%	20%	31.2–75%	0.61%	0%	-	21.78%
ACF @95% c.l †	0.01	0.0363	0.017	-	0.0228	0.0472	0.025	-	0.0315
Energy/bit (fJ)	13	15	-	4	128	-	5.36	-	6.15

* The worst unstable bit rate. † Auto-correlation Function at 95% confidence level. $^{\Delta}$ M_{VOUT} = 1 mV.

By comparing this work with state-of-the-art designs, it is shown to satisfy the basic PUF requirements and can be evaluated as a PUF. From Table 2, it can be seen that some of the latest designs [44,59–61] improve the native stability of PUFs and achieve the native BER very close to 0%. Ref. [44] realises a 0% stabilised BER with relatively high mask ratios and energy consumption per bit, while [59–61] utilises a novel circuit implementation. This work tries to reach the same level of performance with high-frequency evaluations enabled by the power-gated 8T PUF structure. Since the post-layout simulation is extremely time and resource consuming, there are only a few previous works that attain the same level of results by simulation, e.g., the results of [62] are extracted from schematic-based simulations. The main achievement of the proposed design and structure is the speed, which saves time and hence conserves the total power consumption, etc.

4.1. Uniformity

For PUF uniformity, the proportion of ones and zeros of the 8T PUF readings should be evenly distributed. Our results of stable zeroes are 46.22% and stable ones are 46.06%.

4.2. Robustness: Intra-Distance and BER

For an ideal PUF cell, the *Responses* to the same *Challenge* should always be the same. However, the existence of unstable cells makes this impossible. Thus, the intra-distance, which is the Hamming distance between bit strings of the *Responses* from repeated measurements of the same PUF, is used to evaluate the PUF robustness. To minimise the area overheads for error correction in the key regeneration phase, the intra-distance is expected to be close to zero. By comparing every pair of two *Response* bit strings and adding up the total numbers of different bits, the intra-distances are calculated. The average intra-distance of all the simulated 8T PUF groups is 1.45%.

Under nominal conditions, the average percentage of total unstable bits in 20 groups of 2048 8T PUF cells is 7.71%; the raw BER is 1.17%. The corresponding BER of the worst corner is 12.21%. Most of the unstable readings can be fixed by the Data Processing block using TMV, which can be visualised in the golden bitmap generated in the key enrolment phase. For example, in the golden bitmap shown in Figure 9, squares with different colours represent the statistical results of the PUF stability, i.e., white indicates stable '0', black squares show stable '1' and different grey shades present the degree of bias of the cells. Most impressively, the worst corner BER can be decreased to 0% with Dark-bit

masking coordinated with TMV in the worst voltage and temperature corners and in the field. The mask ratio is 21.78%. As a result, the hardware penalty for error correction is minimised.

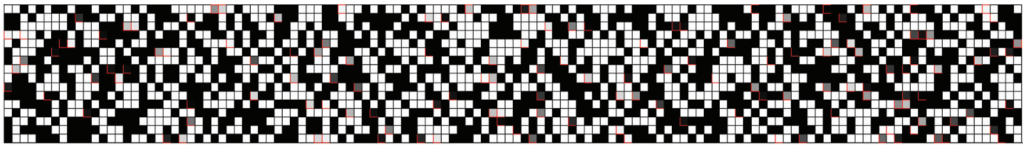


Figure 9. Golden bitmap of 2048 8T PUFs.

4.3. Uniqueness: Inter-Distance

Since PUFs are the hardware sources for identifying individual devices or generating *Secret Keys*, the extracted information from each PUF should be unique. The fractional Hamming distance was computed between different PUF devices. In order to successfully identify each PUF device, this value should be close to 50%. In the experiments, the *Response* bit strings of different PUF clusters were compared to calculate the inter-distance. The average inter-distance of the 20 8T PUF clusters is 50.67%.

4.4. Randomness

Firstly, the Applied Auto-correlation Function (ACF) was used to analyse the spatial correlations among 64 groups of 2048 8T PUFs. The result is 0.0315, which is close to zero, within the 95% confidence bound. This indicates a low spatial correlation of the 8T PUFs based on the physical extraction from the layout design. Then, the randomness of 64 groups of 2048 8T PUFs was assessed with the NIST SP 800-22 [63] statistical test suite. The NIST results are listed in Table 3. The simulation results passed most of the tests. However, the randomness generated by the simulator has limitations, especially for the large amount of data which is required by both the ACF and NIST test suite. Moreover, this practical simulation method is time and resource consuming. A test chip for facilitating on-chip statistical experiments is under development to improve the evaluation efficiency and verify the PUF behaviour in the real world.

Table 3. NIST analysis for 64 PUF groups.

	String Length	*p*-Value	Proportion
Frequency	2048	0.73856	64/64
Block Frequency	2048	0.91013	64/64
Cumulative Sums	2048	0.87698	64/64
Runs	2048	0.0204	11/64
Longest Run	2048	0.005	14/64
Rank	2048	0.44962	64/64
FFT	2048	0.18139	52/64
Approx. Entropy	2048	0.009	28/64
Serial	2048	0.18290	40/64
Linear Complexity	2048	0.63316	61/64

5. Conclusions and Future Work

In this paper, the design, architecture and evaluation of a rapid reset 8T PUF utilising the power gating technique are presented. Its purpose is to enhance PUF stability and minimise the hardware penalty for error corrections. The design can apply on–off power cycles repeatedly to PUF clusters to facilitate fast multiple evaluations for extracting the bias probability of PUF cells. The ultra-fast speed enables TMV in different voltage and temperature corners or in the field. Dark-bit masking based on these extracted data can reduce the BER to close to zero in experiments. In the design, an SRAM-based 8T PUF cell with the ability to eliminate data retention is built, and a two-phase power gating method is devised and evaluated. Besides switching the power supply swiftly and

saving power, the power-up process can be manipulated via varying the power gating method and parameters so as to decrease the interference between sensitive PUF cells and limit the in-rush current during power-up. Consequently, PUF stability and security are enhanced. In addition, the clean and fast reset makes it possible for swift and accurate PUF measurements either in simulation or in a fabricated silicon chip. The 8T PUF characteristics, including robustness, uniqueness and randomness, are thus qualitatively confirmed.

Future work will include quantitative evaluations of the 8T PUF performance on various PVT corners and assessments of different power gating settings. The extracted unstable degrees of PUF cells will be post-processed and added to the PUF *Response* to increase its entropy. In addition to this, a test chip is currently being fabricated. Afterwards, the fabricated test chip will enable on-chip statistical experiments, which serve as a platform to extract analogue secrets. Finally, the differences in the power-gated 8T PUF's entropy compared to its 6T-SRAM PUF counterpart will be assessed, measured and reported.

Author Contributions: Conceptualisation, A.B.; methodology, Y.Z. and A.B.; circuit design, Y.Z.; circuit simulation, Y.Z.; validation, Y.Z.; software, Y.Z.; formal analysis, Y.Z. and A.B.; resources, A.Y.; data curation, Y.Z.; writing—original draft preparation, Y.Z.; writing—review and editing, A.B and A.Y.; visualisation, Y.Z.; supervision, A.B. and A.Y. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

8T	8-Transistor
PUF	Physically Unclonable Function
6T	6-Transistor
SRAM	Static Random-Access Memory
TMV	Temporal Majority Voting
PVT	Process, Voltage and Temperature
BER	Bit Error Rate
ASIC	Application Specific Integrated Circuit
IoT	Internet of Things
IC	Integrated Circuit
MCU	Microcontroller
vddv	virtual power supply
DPA	Differential Power Analysis
FPGA	Field-Programmable Gate Array
CRP	Challenge–Response Pair
DRV	Data Retention Voltage
WL	Word Line
TT	Typical–Typical
SS	Slow–Slow
FF	Fast–Fast
CMOS	Complementary Metal Oxide Semiconductor
ACF	Applied Autocorrelation Function

References

1. Verbauwhede, I. Security Adds an Extra Dimension to IC Design: Future IC Design Must Focus on Security in Addition to Low Power and Energy. *IEEE Solid-State Circuits Mag.* **2017**, *9*, 41–45. [CrossRef]
2. Gassend, B.; Clarke, D.; Van Dijk, M.; Devadas, S. Silicon physical random functions. In Proceedings of the 9th ACM Conference on Computer and Communications Security, Washington, DC, USA, 18–22 November 2002; pp. 148–160.
3. Gassend, B.; Clarke, D.; Van Dijk, M.; Devadas, S. Controlled physical random functions. In Proceedings of the 18th Annual Computer Security Applications Conference, Las Vegas, NV, USA, 9–13 December 2002; pp. 149–160.
4. Guajardo, J.; Kumar, S.S.; Schrijen, G.J.; Tuyls, P. FPGA intrinsic PUFs and their use for IP protection. In *Cryptographic Hardware and Embedded Systems-CHES 2007: 9th International Workshop, Vienna, Austria, September 10–13*; Springer: Berlin/Heidelberg, Germany, 2007; Proceedings 9, pp. 63–80.
5. Holcomb, D.E.; Burleson, W.P.; Fu, K. Initial SRAM state as a fingerprint and source of true random numbers for RFID tags. In Proceedings of the Conference on RFID Security, Malaga, Spain, 10–13 April 2007; Volume 7, No. 2, p. 1.
6. Bhargava, M.; Cakir, C.; Mai, K. Reliability enhancement of bi-stable PUFs in 65nm bulk CMOS. In Proceedings of the 2012 IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), San Francisco, CA, USA, 3–4 June 2012; pp. 25–30.
7. Armknecht, F.; Maes, R.; Sadeghi, A.R.; Sunar, B.; Tuyls, P. Memory leakage-resilient encryption based on physically unclonable functions. In *Towards Hardware-Intrinsic Security: Foundations and Practice*; Springer: Berlin/Heidelberg, Germany, 2010; pp. 135–164.
8. Mathew, S.K.; Satpathy, S.K.; Anders, M.A.; Kaul, H.; Hsu, S.K.; Agarwal, A.; Chen, G.K.; Parker, R.J.; Krishnamurthy, R.K.; De, V. 16.2 A 0.19 pJ/b PVT-variation-tolerant hybrid physically unclonable function circuit for 100% stable secure key generation in 22 nm CMOS. In Proceedings of the 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, CA, USA, 9–13 February 2014; pp. 278–279.
9. Satpathy, S.K.; Mathew, S.K.; Suresh, V.; Anders, M.A.; Kaul, H.; Agarwal, A.; Hsu, S.K.; Chen, G.K.; Krishnamurthy, R.K.; De, V.K. A 4-fJ/b delay-hardened physically unclonable function circuit with selective bit destabilization in 14-nm trigate CMOS. *IEEE J. -Solid-State Circuits* **2017**, *52*, 940–949. [CrossRef]
10. Satpathy, S.K.; Mathew, S.K.; Li, J.; Koeberl, P.; Anders, M.A.; Kaul, H.; Chen, G.K.; Agarwal, A.; Hsu, S.K.; Krishnamurthy, R.K. 13fJ/bit probing-resilient 250K PUF array with soft darkbit masking for 1.94% bit-error in 22nm tri-gate CMOS. In Proceedings of the ESSCIRC 2014-40th European Solid State Circuits Conference (ESSCIRC), Venice, Italy, 22–26 September 2014; pp. 239–242.
11. Bose, R.C.; Ray-Chaudhuri, D.K. On a class of error correcting binary group codes. *Inf. Control* **1960**, *3*, 68–79. [CrossRef]
12. Hamming, R.W. Error detecting and error correcting codes. *Bell Syst. Tech. J.* **1950**, *29*, 147–160. [CrossRef]
13. Bösch, C.; Guajardo, J.; Sadeghi, A.R.; Shokrollahi, J.; Tuyls, P. Efficient helper data key extractor on FPGAs. In Proceedings of the Cryptographic Hardware and Embedded Systems–CHES 2008: 10th International Workshop, Washington, DC, USA, 10–13 August 2008; Springer: Berlin/Heidelberg, Germany, 2008; Proceedings 10, pp. 181–197.
14. Kocher, P.; Jaffe, J.; Jun, B. Differential power analysis.In Proceedings of the Advances in Cryptology—CRYPTO'99: 19th Annual International Cryptology Conference Santa Barbara, California, USA, 15–19 August 1999; Springer: Berlin/Heidelberg, Germany, 1999; Proceedings 19, pp. 388–397.
15. Rührmair, U.; Xu, X.; Sölter, J.; Mahmoud, A.; Koushanfar, F.; Burleson, W. Power and timing side channels for PUFs and their efficient exploitation. *Cryptol. Eprint Arch.* **2013**, 476–492.
16. Rührmair, U.; Sölter, J.; Sehnke, F.; Xu, X.; Mahmoud, A.; Stoyanova, V.; Dror, G.; Schmidhuber, J.; Burleson, W.; Devadas, S. PUF modeling attacks on simulated and silicon data. *IEEE Trans. Inf. Forensics Secur.* **2013**, *8*, 1876–1891. [CrossRef]
17. Halderman, J.A.; Schoen, S.D.; Heninger, N.; Clarkson, W.; Paul, W.; Calandrino, J.A.; Feldman, A.J.; Appelbaum, J.; Felten, E.W. Lest we remember: Cold-boot attacks on encryption keys. *Commun. ACM* **2009**, *52*, 91–98. [CrossRef]
18. Anagnostopoulos, N.A.; Arul, T.; Rosenstihl, M.; Schaller, A.; Gabmeyer, S.; Katzenbeisser, S. Attacking SRAM PUFs using very-low-temperature data remanence. *Microprocess. Microsyst.* **2019**, *71*, 102864. [CrossRef]
19. Wang, Y.; Liang, H.; Wang, Y.; Yao, L.; Yi, M.; Huang, Z.; Lu, Y. A reconfigurable PUF structure with dual working modes based on entropy separation model. *Microelectron. J.* **2022**, *124*, 105445. [CrossRef]
20. Della Sala, R.; Scotti, G. Exploiting the DD-Cell as an Ultra-Compact Entropy Source for an FPGA-based Re-Configurable PUF-TRNG Architecture. *IEEE Access* **2023**, *11*, 86178–86195. [CrossRef]
21. Maiti, A.; Nagesh, R.; Reddy, A.; Schaumont, P. Physical unclonable function and true random number generator: A compact and scalable implementation. In Proceedings of the 19th ACM Great Lakes symposium on VLSI, Boston Area, MA, USA, 10–12 May 2009; pp. 425–428.
22. Baturone, I.; Román, R.; Corbacho, Á. A Unified Multibit PUF and TRNG based on Ring Oscillators for Secure IoT Devices. *IEEE Internet Things J.* **2022**, *10*, 6182–6192. [CrossRef]
23. Halak, B. *Physically Unclonable Functions*; Springer International Publishing: Berlin, Germany, 2018; pp. 60–61.
24. Halak, B.; Zwolinski, M.; Mispan, M.S. Overview of PUF-based hardware security solutions for the Internet of Things. In Proceedings of the 2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS), Abu Dhabi, United Arab Emirates, 16–19 October 2016; pp. 1–4.
25. Jeon, D.; Baek, J.H.; Kim, Y.D.; Lee, J.; Kim, D.K.; Choi, B.D. A Physical Unclonable Function With Bit Error Rate $< 2.3 \times 10^{-8}$ Based on Contact Formation Probability Without Error Correction Code. *IEEE J. Solid-State Circuits* **2019**, *55*, 805–816.

26. Jeon, D.; Lee, D.; Kim, D.K.; Choi, B.D. A 325F^2 Physical Unclonable Function Based on Contact Failure Probability With Bit Error Rate < 0.43 ppm After Preselection With 0.0177% Discard Ratio. *IEEE J. Solid-State Circuits* **2022**, *58*, 1185–1196.
27. Lee, J.W.; Lim, D.; Gassend, B.; Suh, G.E.; Van Dijk, M.; Devadas, S. A technique to build a secret key in integrated circuits for identification and authentication applications. In Proceedings of the 2004 Symposium on VLSI Circuits. Digest of Technical Papers (IEEE Cat. No. 04CH37525), Honolulu, HI, USA, 17–19 June 2004; pp. 176–179.
28. Sahoo, D.P.; Mukhopadhyay, D.; Chakraborty, R.S.; Nguyen, P.H. A multiplexer-based arbiter PUF composition with enhanced reliability and security. *IEEE Trans. Comput.* **2017**, *67*, 403–417. [CrossRef]
29. Zhou, C.; Parhi, K.K.; Kim, C.H. Secure and reliable XOR arbiter PUF design: An experimental study based on 1 trillion challenge response pair measurements. In Proceedings of the 54th Annual Design Automation Conference, Austin, TX, USA, 18–22 June 2017; pp. 1–6.
30. Majzoobi, M.; Koushanfar, F.; Devadas, S. FPGA PUF using programmable delay lines. In Proceedings of the 2010 IEEE International Workshop on Information Forensics and Security, Seattle, WA, USA, 12–15 December 2010; pp. 1–6.
31. Zhao, X.; Gan, P.; Zhao, Q.; Liang, D.; Cao, Y.; Pan, X.; Bermak, A. A 124 fJ/bit cascode current mirror array based PUF with 1.50% native unstable bit ratio. *IEEE Trans. Circuits Syst. Regul. Pap.* **2019**, *66*, 3494–3503. [CrossRef]
32. Yang, K.; Dong, Q.; Blaauw, D.; Sylvester, D. 8.3 A 553F^2 2-transistor amplifier-based Physically Unclonable Function (PUF) with 1.67% native instability. In Proceedings of the 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 5–9 February 2017; pp. 146–147.
33. Taneja, S.; Alvarez, A.B.; Alioto, M. Fully synthesizable PUF featuring hysteresis and temperature compensation for 3.2% native BER and 1.02 fJ/b in 40 nm. *IEEE J. Solid-State Circuits* **2018**, *53*, 2828–2839. [CrossRef]
34. Alvarez, A.B.; Zhao, W.; Alioto, M. Static physically unclonable functions for secure chip identification with 1.9–5.8% native bit instability at 0.6–1 V and 15 fJ/bit in 65 nm. *IEEE J. Solid-State Circuits* **2016**, *51*, 763–775.
35. Liu, J.; Zhao, Y.; Zhu, Y.; Chan, C.H.; Martins, R.P. A Weak PUF-Assisted Strong PUF With Inherent Immunity to Modeling Attacks and Ultra-Low BER. *IEEE Trans. Circuits Syst. Regul. Pap.* **2022**, *69*, 4898–4907. [CrossRef]
36. Yamamoto, D.; Sakiyama, K.; Iwamoto, M.; Ohta, K.; Takenaka, M.; Itoh, K. Variety enhancement of PUF responses using the locations of random outputting RS latches. *J. Cryptogr. Eng.* **2013**, *3*, 197–211. [CrossRef]
37. Serrano, R.; Duran, C.; Sarmiento, M.; Dang, T.K.; Hoang, T.T.; Pham, C.K. A Unified PUF and Crypto Core Exploiting the Metastability in Latches. *Future Internet* **2022**, *14*, 298. [CrossRef]
38. Habib, B.; Kaps, J.P.; Gaj, K. Efficient sr-latch PUF. In Proceedings of the Applied Reconfigurable Computing: 11th International Symposium, ARC 2015, Bochum, Germany, 13–17 April 2015; Springer International Publishing: Berlin, Germany, 2015; Proceedings 11, pp. 205–216.
39. Yamamoto, D.; Sakiyama, K.; Iwamoto, M.; Ohta, K.; Ochiai, T.; Takenaka, M.; Itoh, K. Uniqueness enhancement of PUF responses based on the locations of random outputting RS latches. In Proceedings of the Cryptographic Hardware and Embedded Systems–CHES 2011: 13th International Workshop, Nara, Japan, 28 September–1 October 2011; Springer: Berlin/Heidelberg, Germany, 2011; Proceedings 13, pp. 390–406.
40. Della Sala, R.; Scotti, G. A Novel FPGA Implementation of the NAND-PUF with Minimal Resource Usage and High Reliability. *Cryptography*, **2023**, *7*, 18. [CrossRef]
41. Bossuet, L.; Ngo, X.T.; Cherif, Z.; Fischer, V. A PUF based on a transient effect ring oscillator and insensitive to locking phenomenon. *IEEE Trans. Emerg. Top. Comput.* **2013**, *2*, 30–36. [CrossRef]
42. Maes, R.; Rozic, V.; Verbauwhede, I.; Koeberl, P.; Van der Sluis, E.; Van der Leest, V. Experimental evaluation of physically unclonable functions in 65 nm CMOS. In Proceedings of the European Solid-State Circuits Conference (ESSCIRC), Bordeaux, France, 17–21 September 2012; pp. 486–489.
43. Xu, X.; Holcomb, D.E. Reliable PUF design using failure patterns from time-controlled power gating. In Proceedings of the 2016 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), Storrs, CT, USA, 19–20 September 2016; pp. 135–140.
44. Liu, K.; Min, Y.; Yang, X.; Sun, H.; Shinohara, H. A 373-F^2 0.21%-Native-BER EE SRAM Physically Unclonable Function With 2-D Power-Gated Bit Cells and V_{ss} Bias-Based Dark-Bit Detection. *IEEE J. Solid-State Circuits* **2020**, *55*, 1719–1732. [CrossRef]
45. Li, G.; Wang, P.; Ma, X.; Shi, Y.; Chen, B.; Zhang, Y. A multimode configurable physically unclonable function with bit-instability-screening and power-gating strategies. *IEEE Trans. Very Large Scale Integr. (Vlsi) Syst.* **2020**, *29*, 100–111. [CrossRef]
46. Holcomb, D.E.; Rahmati, A.; Salajegheh, M.; Burleson, W.P.; Fu, K. DRV-fingerprinting: Using data retention voltage of SRAM cells for chip identification. In Proceedings of theRadio Frequency Identification. Security and Privacy Issues: 8th International Workshop, RFIDSec 2012, Nijmegen, The Netherlands, 2–3 July 2012; Springer: Berlin/Heidelberg, Germany, 2013; Revised Selected Papers 8, pp. 165–179.
47. M. Keating; Flynn, D.; Aitken, R.; Gibbons, A.; Shi, K. Sleep Transistor Design. In *Low Power Methodology Manual: For System-on-Chip Design*; Springer Science & Business Media: Berlin/Heidelberg, Germany, 2007; pp. 249–265.
48. M. Keating; Flynn, D.; Aitken, R.; Gibbons, A.; Shi, K. Design of the Power Switching Network. In *Low Power Methodology Manual: For System-on-Chip Design*; Springer Science & Business Media: Berlin/Heidelberg, Germany, 2007; pp. 225–247.
49. Chang, L.; Montoye, R.K.; Nakamura, Y.; Batson, K.A.; Eickemeyer, R.J.; Dennard, R.H.; Haensch, W.; Jamsek, D. An 8T-SRAM for variability tolerance and low-voltage operation in high-performance caches. *IEEE J. Solid-State Circuits* **2008**, *43*, 956–963. [CrossRef]

50. Morita, Y.; Fujiwara, H.; Noguchi, H.; Iguchi, Y.; Nii, K.; Kawaguchi, H.; Yoshimoto, M. An area-conscious low-voltage-oriented 8T-SRAM design under DVS environment. In Proceedings of the 2007 IEEE Symposium on VLSI Circuits, Kyoto, Japan, 14–16 June 2007; pp. 256–257.
51. List, F.J. The static noise margin of SRAM cells. In Proceedings of the ESSCIRC'86: Twelfth European Solid-State Circuits Conference, Finlandia Hall, Helsinki, 16–18 September 1986; pp. 16–18.
52. Kleeman, L.; Cantoni, A. Metastable behavior in digital systems. *IEEE Des. Test Comput.* **1987**, *4*, 4–19. [CrossRef]
53. Skorobogatov, S. *Low Temperature Data Remanence in Static RAM*; No. UCAM-CL-TR-536; University of Cambridge, Computer Laboratory: Cambridge, MA, USA, 2002.
54. Cakir, C.; Bhargava, M.; Mai, K. 6T SRAM and 3T DRAM data retention and remanence characterization in 65nm bulk CMOS. In Proceedings of the IEEE 2012 Custom Integrated Circuits Conference, San Jose, CA, USA, 9–12 September 2012; pp. 1–4.
55. Cortez, M.; Dargar, A.; Hamdioui, S.; Schrijen, G.J. Modeling SRAM start-up behavior for physical unclonable functions. In Proceedings of the 2012 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), Austin, TX, USA, 2–4 October 2012; pp. 1–6.
56. Zheng, Y.; Bystrov, A.; Yakovlev, A. A Rapid Reset 8-Transistor Physically Unclonable Function Utilising Power Gating. In Proceedings of the 2023 Design, Automation & Test in Europe Conference & Exhibition (DATE), Antwerp, Belgium, 17–19 April 2023; pp. 1–2.
57. Takahashi, Y.; Koyasu, H.; Kumar, S.D.; Thapliyal, H. Quasi-Adiabatic SRAM Based Silicon Physical Unclonable Function. *SN Comput. Sci.* **2020**, *1*, 237. [CrossRef]
58. Alvarez, A.; Zhao, W.; Alioto, M. 14.3 15fJ/b static physically unclonable functions for secure chip identification with< 2% native bit instability and 140× Inter/Intra PUF hamming distance separation in 65 nm. In Proceedings of the 2015 IEEE International Solid-State Circuits Conference-(ISSCC) Digest of Technical Papers, San Francisco, CA, USA, 22–26 February 2015; pp. 1–3.
59. Karpinskyy, B.; Lee, Y.; Choi, Y.; Kim, Y.; Noh, M.; Lee, S. 8.7 Physically unclonable function for secure key generation with a key error rate of 2E-38 in 45nm smart-card chips. In Proceedings of the 2016 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 5–9 February 2016; pp. 158–160.
60. Vatalaro, M.; De Rose, R.; Lanuzza, M.; Crupi, F. Static CMOS physically unclonable function based on 4T voltage divider with 0.6%–1.5% bit instability at 0.4–1.8 V operation in 180 nm. *IEEE J. Solid-State Circuits* **2022**, *57*, 2509–2520. [CrossRef]
61. Della Sala, R.; Bellizia, D.; Centurelli, F.; Scotti, G. A Monostable Physically Unclonable Function Based on Improved RCCMs with 0–1.56% Native Bit Instability at 0.6–1.2 V and 0–75 °C. *Electronics* **2023**, *12*, 755. [CrossRef]
62. De Rose, R.; Crupi, F.; Lanuzza, M.; Albano, D. A physical unclonable function based on a 2-transistor subthreshold voltage divider. *Int. J. Circuit Theory Appl.* **2017**, *45*, 260–273. [CrossRef]
63. Rukhin, A.; Soto, J.; Nechvatal, J.; Smid, M.; Barker, E. *A Statistical Test Suite for Random and Pseudorandom Number Generators for Cryptographic Applications*; Booz-Allen and Hamilton Inc. Mclean Va: McLean, VA, USA, 2001.

Journal of
Low Power Electronics and Applications

MDPI

Communication

Design of a Low-Power Delay-Locked Loop-Based 8× Frequency Multiplier in 22 nm FDSOI

Naveed * and Jeff Dix

Department of Electrical Engineering and Computer Science, University of Arkansas, Fayetteville, AR 72701, USA
* Correspondence: naveed@uark.edu

Abstract: A low-power delay-locked loop (DLL)-based frequency multiplier is presented. The multiplier is designed in 22 nm FDSOI and achieves 8× multiplication. The proposed DLL uses a new simple duty cycle correction circuit and is XOR logic-based for frequency multiplication. Current starved delay cells are used to make the circuit power efficient. The circuit uses three 2× stages instead of an edge combiner to achieve 8× multiplication, thus requiring far less power and chip area as compared to conventional phase-locked loop (PLL) circuits. The proposed 8× multiplier occupies an active area of 0.09 mm^2. The measurement result shows ultra-low power consumption of 130 μW at 0.8 V supply. The post-layout simulation shows a timing jitter of 24 ps (pk-pk) at 2.44 GHz.

Keywords: WSN; frequency multiplier; XOR; FDSOI 22 nm

1. Introduction

The development of wireless sensor networks (WSNs) has seen an increased demand in the last decade. The interest can be attributed to their cost-effective and easy implementation in a wide range of fields such as agriculture, environment monitoring, surveillance, etc. [1]. Designing a sensor node requires several critical design considerations such as form factor, network size, operating conditions, power consumption, maintenance, etc. For WSNs, when designing a battery-less sensor node, minimizing the power consumption is a challenging task. Among the several functional blocks of a sensor node, most of the available power is used for carrier signal generation for data transmission. Using a local oscillator for carrier generation not only necessitates a significant amount of power consumption, but it is also quite difficult to achieve sufficient accuracy over process–voltage–temperature (PVT) variations [2]. Thus, it is challenging to implement a low-power wireless communication architecture in low-cost WSNs without the availability of a stable reference frequency.

Backscattering the incoming signal to eliminate the need for carrier signal generation has been a popular and uncomplicated solution [3]. However, backscattering can make the system prone to self-jamming [4]. The phase-locked loop (PLL) architecture is another dominant choice for carrier frequency synthesis. Ref. [5] shows the implementation of a transceiver that uses the received 915 MHz signal as input of a PLL to realize a 2.4-GHz RF carrier for wireless data transmission. However, due to the need for a VCO, a phase detector, and a frequency divider, a PLL is physically large and consumes a significant amount of power [6]. The PLL also suffers from phase noise accumulation in the voltage-controlled oscillator (VCO) [7].

In the last decade, the delay-locked loop (DLL)-based frequency synthesis has been under exploration [8–13] due to its low power, low complexity, and area-efficient performance. Ref. [8] presents a DLL based on a voltage-controlled delay line (VCDL) and an edge combiner. This approach may suffer from duty cycle distortion due to the possible mismatches in the VCDL and because the frequency multiplier triggers on both the rising and the falling edge. Another DLL uses VCDL, which can be configured as a resettable VCO [9].

However, this approach may have a high in-lock error due to the process of injecting back the frequency into the VCDL. Since the DLL operation does not require any inductors and for the most part consists of digital logic circuits, its implementation is area efficient. This paper presents the design of a low-power XOR logic-based DLL. The proposed DLL is designed as a part of a battery-less wireless sensor node. To conserve power, the sensor node extracts the carrier of an ISM band signal and divides the received frequency. The DLL then applies 8× multiplication to the input signal to generate a 2.44 GHz signal in the output. Therefore, it is critical for the DLL to be energy efficient for its application. The design uses current-starved voltage-controlled delay cells (VCDLs) to minimize power consumption. A series of three 2× multiplication stages are used to achieve 8× frequency multiplication. A new charge pump (CP)-based duty cycle control loop (DCCL) is implemented in each multiplication stage to achieve low duty cycle distortion over PVT variation.

This paper is organized as follows: Section 2 describes the implemented DLL architecture. The circuit implementation is discussed in Section 3. Section 4 presents the experimental results, and a conclusion ends the paper.

2. DLL Architecture and Operation

The block diagram of the proposed frequency multiplier is shown in Figure 1.

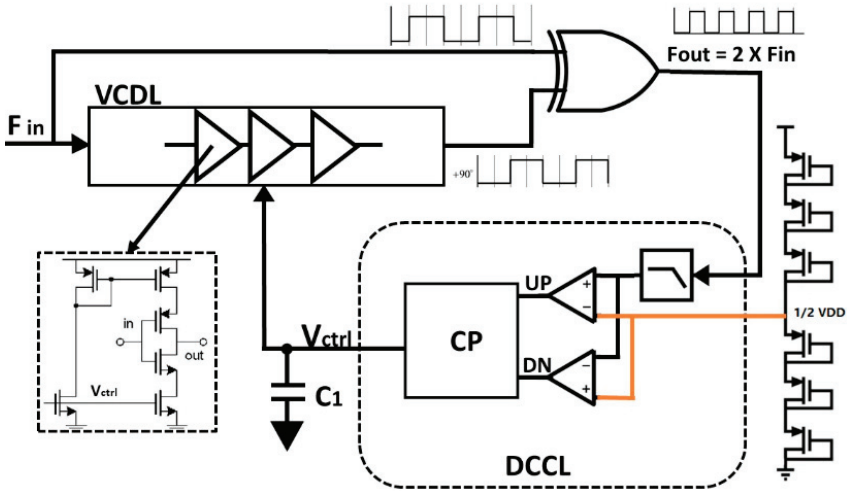


Figure 1. Proposed DLL architecture showing the full operation of 2× multiplication.

Each 2× multiplication comprises a VCDL, an XOR gate, and a duty cycle control loop (DCCL). A series of three 2× multipliers is used to achieve 8× frequency multiplication. VCDL is then followed by a low-power XOR gate. Given that frequency locking is not an issue, an XOR gate is preferred as the phase detector in our approach. The XOR gate takes in both the original signal and the delayed signal to output a 2× frequency, as shown in Figure 2.

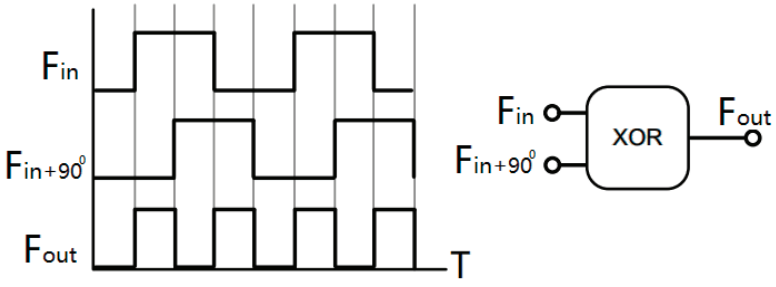


Figure 2. XOR logic-based frequency multiplication technique.

Initially, the delay introduced by the VCDL may not be exactly 90°. The duty cycle may be less than or greater than 50%. The duty cycle correction circuit uses a passive integrator to generate an average DC voltage proportional to the duty cycle. The output of the integrator is compared with a voltage level equal to half of the supply voltage (VDD) using comparators. After comparison, the DCCL circuit signals the charge pump (CP) circuit to generate feedback control voltages. The feedback coming from CP then varies Vctrl to correct the delay to 90°, achieving a 50% duty cycle. It is to be noted that in the case of a single 2× multiplication stage for an input frequency of 305 MHz, the whole circuit except the output of the XOR gate is switching at 610 MHz, i.e., twice the input frequency.

3. Circuit Implementation

3.1. Current-Starved Delay Cell

Current-starved full-swing inverter cells are used in the VCDL to generate the 90° delay. The implemented delay cell is optimized for low power consumption and is shown in Figure 3. The current in the delay cell is controlled by the gate voltage of MN2 and MP2. The inverter is sized to produce only a fraction of the total delay. Too many or too few delay cells in VCDL can impact the process corner variation. Therefore, the number of delay cells in each VCDL is optimized to achieve better performance across process corners. Careful consideration in layout design is taken to minimize mismatches.

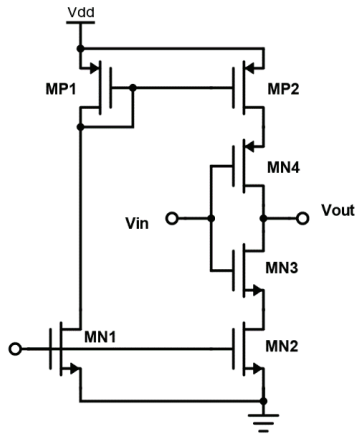


Figure 3. Current-starved delay cell.

3.2. XOR Logic

Conventional XOR gates are used for frequency multiplication. The use of an edge combiner is avoided in this implementation to reduce the number of XOR gates. The current implementation uses only three XOR gates in total to achieve 8× frequency multiplication. Comparatively, an edge combiner will require seven XOR gates for 8× multiplication. The schematic of the implemented XOR gate topology is shown in Figure 4. Since each multiplication stage has a different input frequency, each of the XOR gates is optimized for power consumption and frequency.

3.3. Duty Cycle Correction Loop

The DCCL ensures a 50% duty cycle of the output on all PVT corners. It controls the delay of VCDL using the signal Vctrl. The feedback forces the average (i.e., DC component) of the 2× signal to be equal to half of the VDD to achieve a 50% duty cycle. To save power and area, diode-connected stacked PMOS devices are used. The stacked MOS diodes generate a VREF equal to half of VDD. A passive RC integrator extracts the DC of the 2× signal and compares it with VREF using OTAs, as shown in Figure 5. The OTAs are biased in the subthreshold region to achieve ultra-low-power operation. The UP and DN signals coming from the OTAs are fed into the charge pump circuit to generate Vctrl.

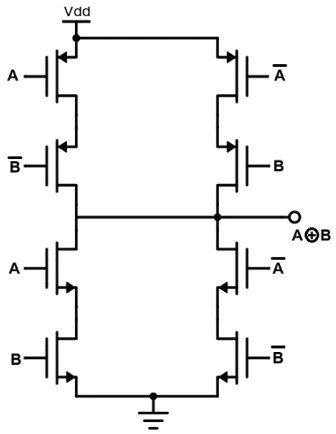


Figure 4. Implemented XOR gate.

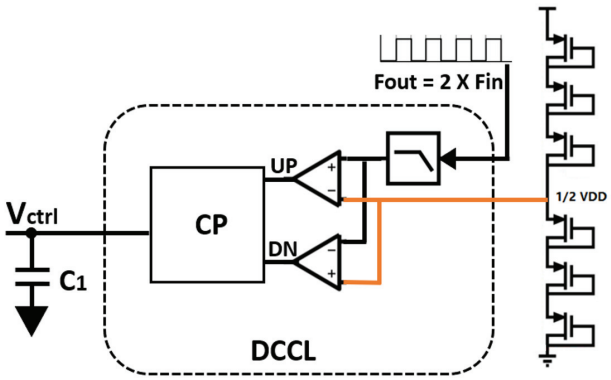


Figure 5. Proposed duty cycle correction loop.

The implemented charge pump (CP) circuit is shown in Figure 6. The CP is biased in the subthreshold region for low current consumption. Self-cascoded transistors are used in the current mirrors to boost the output resistance allowing a high output voltage swing. When the duty cycle is >50%, the UP signal is High, and the DN signal is Low so that C1 charges and Vctrl increases. This increase in Vctrl decreases the delay in the VCDL until the duty cycle becomes 50%. When the duty cycle is <50%, the UP signal is Low and the DN signal is High, thus correcting the duty cycle by decreasing Vctrl. This feedback loop ensures a 50% duty cycle across all PVT corners.

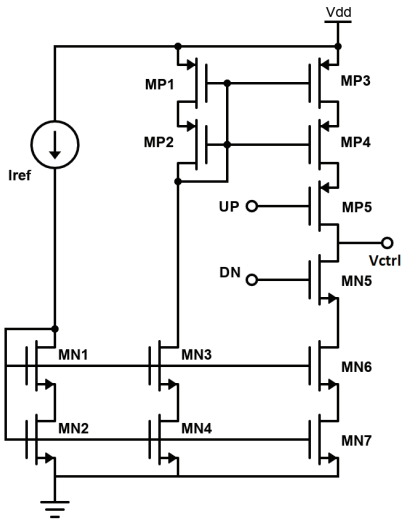


Figure 6. Charge pump circuit implementation.

3.4. Simulation Results of a Single 2× Multiplication Stage

Figure 7 illustrates a transient simulation of a single stage of 2× frequency multiplication. The input frequency provided to the 2× multiplier is 305 MHz, yielding a 605 MHz signal at the output. Due to the action of the duty cycle correction loop, the circuit achieves a 50% duty cycle across all simulated process corners. The simulated power consumption of the 2× multiplier is approximately 40 µW at a 0.8 V supply.

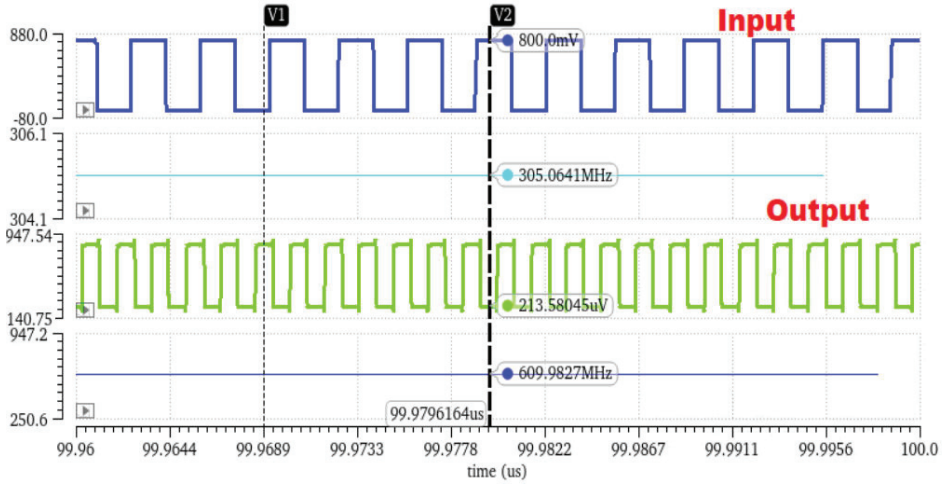


Figure 7. Simulation results of the input vs. output frequency of the 2× multiplication stage.

For the implementation of DLL in this work, 22 nm FD-SOI (Fully Depleted Silicon-On-Insulator) process technology is used. FD-SOI transistor technology offers superior electrical performance due to its reduced parasitic capacitance, energy efficiency, and improved isolation as compared to the transistor fabricated over bulk silicon [14], leading to enhanced signal integrity and lower power consumption. Additionally, the improved short-channel effects in FD-SOI contribute to better device scaling, allowing for the integration of more compact and efficient DLL components. Overall, the utilization of the FD-SOI process in DLL implementation promises superior performance, reduced power consumption, and increased design flexibility compared to traditional CMOS processes.

4. Experimental Results

The circuit is implemented in 22 nm FD-SOI technology and is designed in Cadence Virtuoso. The block schematic of the 2× multiplier is shown in Figure 8 which highlights all the sub-blocks of the circuit. The proposed 8× multiplication circuit occupies an active area of 0.09 mm^2. The layout and micrograph of the circuit is shown in Figure 9.

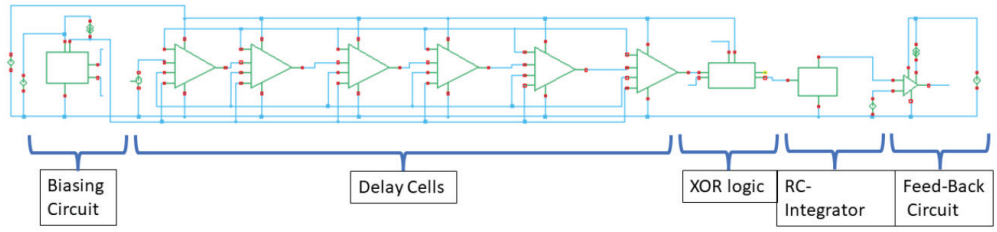


Figure 8. Block schematic of the 2× multiplier in 22 nm FD-SOI.

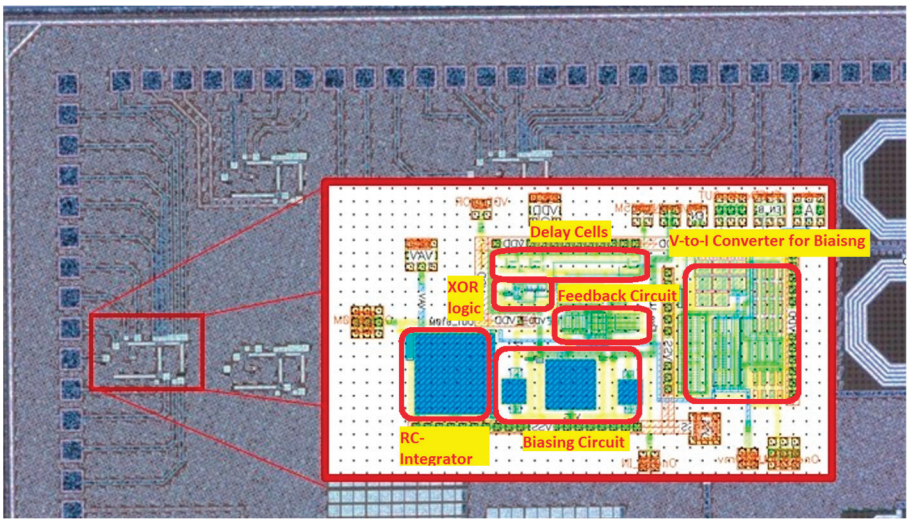


Figure 9. Micrograph and layout of the proposed circuit.

Figure 10 shows the post-layout performance of the 8× frequency multiplier. Here, 305 MHz is given as input frequency to the multiplier, which generates an output frequency of 2.44 GHz. Figure 11 shows the action of the control loop to correct the duty cycle of the output signal. It takes about 40 µs to achieve a 50% duty cycle. The measured power consumption of the 8× multiplier is about 130 µW at 0.8 V.

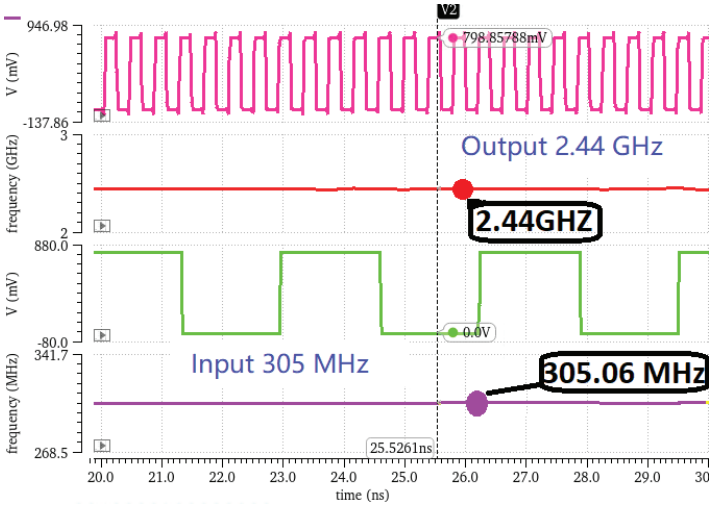


Figure 10. Post−layout simulation of the input vs. output frequency of the proposed circuit showing 8× multiplication.

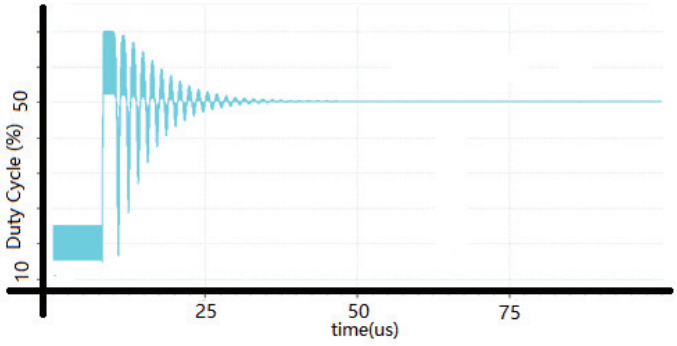


Figure 11. Post layout simulated response of the duty cycle correction loop. The circuit takes 40 µs to achieve a 50% duty cycle.

The circuit passed all the post-layout process corner simulations for a temperature range of −20 to 110 °C while the supply voltage was kept constant at 0.8 V.

The DC offset of the OTAs for error corrections changes across process corners and appears as a static duty cycle error. This error can be seen as spurious tones in the output frequency spectrum. For all process and temperature corners, the duty cycle error remains in an acceptable range of −5% to 3%. For all the process and temperature corners, the number of delay stages is chosen such that the duty cycle error before correction is always positive. The observation shows that the feedback loop can correct a max duty cycle error of 30% before saturating.

Figure 12 shows the measured frequency spectrum of the output. The sideband harmonics power level is seen at least 25 dB lower than the carrier. The simulation shows a timing jitter of 24 ps (pk-pk).

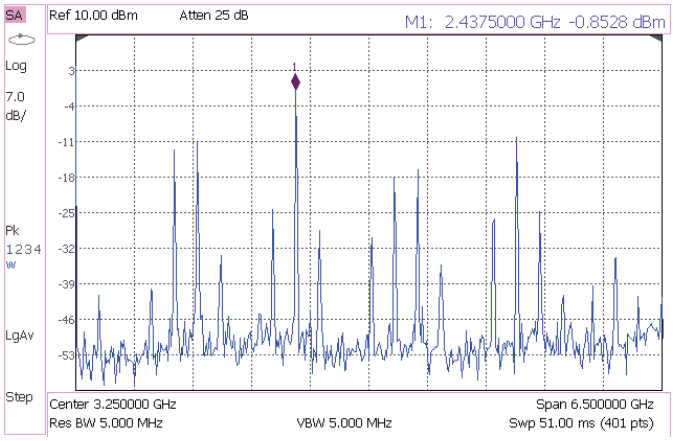


Figure 12. Measured frequency spectrum of the output.

A FOM (figure of merit) is derived from [15] to make a performance comparison with the state of the art. Equation (1) calculates the FOM using multiplication factor (N), Power Consumption (Pdc), Process minimum length (L_{min}), operating bandwidth (BW in %), and Area (A). The comparison of performance is summarized in Table 1. The proposed multiplier achieves the best FOM due to lower power consumption, wider operating bandwidth, and better multiplication factor/area ratio. Note that a lower FOM is an indication of better performance.

$$\text{FOM} = 10\log\frac{\text{Pdc}}{\text{N}} + 10\log\frac{\text{A}}{\text{L}_{\text{min}}} - 10\log(\text{BW}), \quad (1)$$

Table 1. Summary of performance comparison.

	This Work	**[11]**	**[12]**	**[13]**
Supply Voltage (V)	0.8	0.6–1.2	1	N/A
Multiplication Factor	8×	32×	3×	3×
Input/Output Frequency (GHz)	0.305/2.44	0.017/0.574	20/60	3.5/10.5
Timing jitter (Simulated) (ps)	24 ps @ 2.44 GHz (pk-pk)	97 ps @ 0.574 GHz (pk-pk)	N/A	N/A
Normalized periodic jitter (jitter/period)	0.0586	0.055	N/A	N/A
Power consumption (mW)	0.13	2.71	50	5.5
Active area (mm^2)	0.09	0.014	0.4	0.075
Technology	22 nm FD-SOI	28-nm FD-SOI	45 nm SOI CMOS	22 nm FD-SOI
FOM	74.01	91.76	111.85	114.53

5. Conclusions

An XOR logic-based, low-power DLL frequency multiplier is presented. The circuit achieves 8× multiplication in three 2× stages. The design eliminates the need for edge combining, effectively minimizing the power consumption to 130 μW at 0.8 V supply. The circuit utilizes a new simpler duty cycle correction loop offering multiplication of a wide frequency. The duty cycle correction loop also ensures minimal duty cycle distortion across all PVT corners. A timing jitter of 24 ps (pk-pk) is observed at 2.44 GHz output comparable to the state-of-the-art options. The proposed design is a suitable low-power frequency multiplier for battery-less wireless sensor nodes.

Author Contributions: Conceptualization, N. and J.D.; methodology, N. and J.D.; software, N.; validation, N.; formal analysis, N.; investigation, N.; resources, J.D.; data curation, N.; writing—original draft preparation, N.; writing—review and editing, N. and J.D.; visualization, N. and J.D.; supervision, J.D.; project administration, J.D.; funding acquisition, J.D. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: Data are contained within the article.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Sansoy, M.; Buttar, A.S.; Goyal, R. Empowering Wireless Sensor Networks with RF Energy Harvesting. In Proceedings of the 2020 IEEE 7th International Conference on Signal Processing and Integrated Networks (SPIN), Noida, India, 27–28 February 2020; pp. 273–277.
2. Hou, B.; Chen, H.; Wang, Z.; Mo, J.; Chen, J.; Yu, F.; Wang, W. A 11 mW 2.4 GHz 0.18 μm CMOS Transceivers for Wireless Sensor Networks. *Sensors* **2017**, *17*, 223. [CrossRef] [PubMed]
3. Vauche, R.; Bergeret, E.; Gaubert, J.; Bourdel, S.; Fourquin, O.; Dehaese, N. A remotely UHF-powered UWB transmitter for high precision localization of RFID tag. In Proceedings of the 2011 IEEE International Conference on Ultra-Wideband (ICUWB), Bologna, Italy, 14–16 September 2011; pp. 494–498.
4. Finkenzeller, K. *RFID Handbook: Fundamentals and Applications in Contactless Smart Cards and Identification*, 2nd ed.; Wiley: West Sussex, UK, 2003; pp. 134–136.
5. Papotto, G.; Carrara, F.; Finocchiaro, A.; Palmisano, G. A 90-nm CMOS 5-Mbps crystal-less RF-powered transceiver for wireless sensor network nodes. *IEEE J. Solid-State Circuits* **2014**, *40*, 335–346. [CrossRef]
6. Saavedra, C.E.; Zhang, Y. A clock frequency doubler using a passive integrator and emitter-coupled comparator circuit. In Proceedings of the 2004 IEEE Canadian Conference on Electrical and Computer Engineering, Niagara Falls, ON, Canada, 2–5 May 2004; Volume 1, pp. 137–140.
7. Du, Q.; Zhuang, J.; Kwasniewski, T. A Low-Phase Noise, Anti-Harmonic Programmable DLL Frequency Multiplier with Period Error Compensation for Spur Reduction. *IEEE Trans. Circuits Syst. II Expr. Briefs* **2006**, *53*, 1205–1209. [CrossRef]
8. Foley, D.J. CMOS DLL-Based 2-V 3.2-ps Jitter 1-GHz Clock Synthesizer and Temperature-Compensated Tunable Oscillator. *IEEE J. Solid-State Circuits* **2001**, *36*, 417–423. [CrossRef]
9. Wei, G.-Y.; Stonick, J.T.; Weinlader, D.; Sonntag, J.; Searles, S. A 500MHz MP/DLL clock generator for a 5Gb/s backplane transceiver in 0.25 μm CMOS. In Proceedings of the 2003 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 3 February 2003; Volume 1, pp. 464–465.
10. Farjad-Rad, R.; Dally, W.; Ng, H.T.; Senthinathan, R.; Lee, M.J.; Rathi, R.; Poulton, J. A Low-Power Multiplying DLL for Low-Jitter Multi-gigahertz Clock Generation. *IEEE J. Solid-State Circuits* **2002**, *37*, 1804–1811. [CrossRef]
11. Cochet, M.; Clerc, S.; Naceur, M.; Schamberger, P.; Croain, D.; Autran, J.L.; Roche, P. A 28 nm FD-SOI standard cell 0.6–1.2 V open-loop frequency multiplier for low power SoC clocking. In Proceedings of the 2016 IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, QC, Canada, 22–25 May 2016; pp. 1206–1209.
12. Lee, W.; Dinc, T.; Valdes-Garcia, A. Reconfigurable 60-GHz Radar Transmitter SoC with Broadband Frequency Tripler in 45-nm SOI CMOS. In Proceedings of the 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Boston, MA, USA, 2–4 June 2019; pp. 43–46.
13. Balasubramaniyan, A.; Bellaouar, A. Digital Frequency Multiplier for LO Generation using 22-nm FDSOI. In Proceedings of the 2018 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), Burlingame, CA, USA, 15 October 2018; pp. 1–2.

14. Celis, J.-P.; Prakash, B. Chapter 4—Surface Modification of Materials by Plasma Immersion Ion Implantation. In *European Materials Research Society Series, Materials Surface Processing by Directed Energy Techniques*; Pauleau, Y., Ed.; Elsevier: Amsterdam, The Netherlands, 2006; pp. 111–149.
15. Nam, K.-H.; Hong, N.-P.; Park, J.-S. A 16-Times Frequency Multiplier for 5G Synthesizer. *IEEE Trans. Microw. Theory Tech.* **2021**, *69*, 4961–4976. [CrossRef]

Journal of
Low Power Electronics and Applications

MDPI

Article

Design and Optimization of an Ultra-Low-Power Cross-Coupled LC VCO with a DFF Frequency Divider for 2.4 GHz RF Receivers Using 65 nm CMOS Technology

Muhammad Faisal Siddiqui *, Mukesh Kumar Maheshwari *, Muhammad Raza and Aurangzeb Rashid Masud

Department of Electrical Engineering, Bahria University, Karachi 75260, Pakistan;
mraza.bukc@bahria.edu.pk (M.R.); aurangzebrashid.bukc@bahria.edu.pk (A.R.M.)
* Correspondence: faisalsiddiqui.bukc@bahria.edu.pk (M.F.S.); mukeshkumar.bukc@bahria.edu.pk (M.K.M.);
Tel.: +92-3219202022 (M.F.S.)

Abstract: This article presents the design and optimization of a tunable quadrature differential LC CMOS voltage-controlled oscillator (VCO) with a D flip-flop (DFF) frequency divider. The VCO is designed for the low-power and low-phase-noise applications of 2.4 GHz IoT/BLE receivers and wireless sensor devices. The proposed design comprises the proper stacking of an LC VCO and a DFF frequency divider and is simulated using a TSMC 65 nm CMOS technology, and it has a tuning range of 4.4 to 5.7 GHz. The voltage headroom is preserved using a high-impedance on-chip passive inductor at the tail for filtering and enabling true differential operation. The VCO and frequency divider consume as low as 2.02 mW altogether, with the VCO section consuming only 0.47 mW. The active area of the chip including the pads is only 0.47 mm^2. The designed VCO achieved a much better phase noise of −118.36 dBc/Hz at a 1 MHz offset frequency with 1.2 V supply voltages. The design produced a much better FoM of −196.44 dBc/Hz compared to other related research.

Keywords: CMOS; quadrature; differential; DFF frequency divider; phase noise; quality factor; varactor; Inductor Capacitor voltage-controlled oscillator (LC-VCO); layout

1. Introduction

The proliferation of mobile phones and the establishment of cellular networks revolutionized personal communication. The 21st century witnessed the emergence of 3G, 4G, and 5G wireless networks, enabling faster data transfer and the growth of the mobile internet. Wireless communication has continued to evolve, with innovations in areas like Wi-Fi, Bluetooth, and IoT (Internet of Things) communication. These technologies have become integral to daily life and various industries. The advent of Wi-Fi, Bluetooth low energy (BLE), and the subsequent growth of IoT (Internet of Things) devices has had a significant impact on the way we live, work, and interact with technology. The number of Internet of Things (IoT) devices and connected objects has grown significantly in recent years. Examples include automation systems for homes, smart appliances, smart agriculture systems, smart healthcare systems, wireless sensors, wearable technology, etc. The transportation, logistics, healthcare, life, and digital industries are all being improved with the emergence of intelligent, wirelessly interconnected objects. It is anticipated that billions of devices with sensor will be linked to the Internet through diverse access networks. Cisco's IoT Connections Count Forecast estimated that there would be over 36 billion connected IoT devices by 2025. The future of wireless communication holds the promise of even faster and more reliable networks, expanded IoT applications, and the integration of wireless technology into areas like autonomous vehicles and smart cities.

The proliferation of IoT devices, many of which rely on 2.4 GHz devices like Wi-Fi and Bluetooth low energy (BLE) for connectivity, has been revolutionary. These devices are embedded in our homes, industries, transportation systems, and cities. They collect

data, automate tasks, and enhance efficiency and convenience. Implementing economical, low-power, and adaptable systems is a significant necessity for these devices. The IoT sensor node needs to be mobile, battery-operated, and perhaps able to retain energy for several years. It is a crucial element of IoT systems, and it mostly influences the system's performance. Therefore, the transceiver RF must adhere to strict power limitations. The most important part of every RF transceiver is the voltage-controlled oscillator (VCO).

A substantial amount of the power budget is used by the VCO. The key challenge in this endeavor is reducing the power consumption.

The leading idea of this article is to produce a design that has low phase noise, low power consumption, accurate quadrature oscillation, and a better frequency tuning range with a reduced chip size. In this regard, we adopted the best technique of a VCO and frequency divider and integrated them at their optimal level. It has been used to satisfy the requirements of IoT applications: autonomy, stability, and frequency agility.

Wireless communication has become a ubiquitous part of our daily lives, and the demand for low-power, cost-effective, and secure RF transceivers has increased dramatically with the emergence of the Internet of Things (IoT) and other wireless applications.

The use of advanced techniques by RFIC designers has resulted in improved efficiency for RF transceivers. These techniques have allowed for the integration of more functionality onto a single chip, resulting in more efficient, reliable, and cost-effective wireless communication systems. The complete system-on-chip (SoC) design approach enables the integration of numerous components, including RF transceivers, onto a single chip, resulting in decreased power consumption and cost.

In this article, the LC tank complementary cross-coupled differential voltage-controlled oscillator (VCO) technique is used to achieve perfect symmetry between the quadrature outputs of an oscillator. This technique addresses the intrinsic asymmetry issue in current reusing and ensures an accurate quadrature phase relationship, leading to improved performance in RF transceivers.

In article [1], comparative analyses were conducted on various LC oscillator topologies, including Colpitts, Hartley, and common-source cross-coupled differential pairs, in the frequency range of 1 to 100 GHz. The circuits were implemented in 28 nm bulk CMOS technology to operate at different frequencies while maintaining equal power consumption, quality factor, and transistor sizes for a fair comparison. The impulse sensitivity function was accurately evaluated with all the necessary steps and settings discussed in detail. Additionally, PN performances were assessed through periodic steady-state simulations in the Spectre RF-Cadence environment.

The quadrature differential cross-coupled LC oscillator and the VCO Ring Oscillator are the two most prevalent kinds of integrated oscillators. Both types have their advantages and disadvantages, which make them more suitable for specific applications. Ring oscillators are so widely used because of their low power consumption and small size, which make them ideal for many applications where these factors are critical. The ring oscillator's phase noise performance is inferior to that of quadrature differential cross-coupled LC oscillators in applications where phase noise is an important characteristic. On the other hand, quadrature differential cross-coupled LC oscillators are preferred for systems that require high data rates and low bit error rates. They perform better in terms of phase noise than ring oscillators in RF applications demanding high-quality signals. However, they may require more area and consume more power compared to ring oscillators.

Due to their low power usage, improved phase noise performance, and straightforward implementation, LC tank VCO techniques and quadrature differential cross-coupled LC oscillator techniques are frequently used in high-performance RF and wireless communication systems. Their unique topologies and careful selection of components make them ideal for a wide range of applications. Those require high-speed data transfer rates, low bit error rates, and low power consumption [2]. When compared to a quadrature VCO, the approach of operating the VCO at twice the LO frequency and then $\frac{1}{2}$ division is often used to cover less chip space [3].

A power-efficient method for reusing current is the LC VCO followed by a 1/2 frequency divider circuit. When oscillation amplitude is decreased, the voltage headroom for each MOS is likewise decreased, which results in more phase noise than a separated VCO and divider. To minimize the trade-off between voltage headroom and power usage, VCO and frequency divider circuits must be carefully designed together [4].

1.1. Quadrature Generation VCO

Direct conversion transceivers are commonly used in modern radio systems. They offer a simpler architecture compared to other types of transceivers, such as super heterodyne transceivers, which require multiple stages of frequency conversion and filtering. Quadrature down-conversion is necessary for recent modern radio systems to reject the image signals in direct conversion and low-IF receivers. Both the Colpitts and LC oscillators can produce quadrature signals; however, the Colpitts oscillator performs worse concerning phase noise as compared to the LC oscillator [5,6].

To generate quadrature signals, the VCO usually employs a coupling network, such as a quadrature LC tank or a pair of coupled resonators, which provides the necessary phase shift between the two outputs. However, this coupling network can introduce additional phase noise, which can degrade the overall phase noise performance of the VCO. This demonstrates that a traditional parallel-coupled QVCO outperforms a single-phase VCO in terms of phase noise due to the coupling transistors being connected in parallel with the switching pairs, which causes a non-zero resonator phase shift and reduces the phase noise of the QVCO. A trade-off between phase noise and phase accuracy led to this coupling approach. [7]. Secondly, the QVCO design acquires more chip area as compared to a single VCO [4,8–10].

The most precise quadrature LO signals across a broad frequency range are produced using a double-frequency VCO using a 1/2 frequency divider technique. Increased power consumption was a result of this technique of high operating frequency for the VCO and frequency divider. However, the master–slave flip-flops, which have to be designed for the doubled frequency, consume much power. If the primary design concern is low cost or small area, then this solution clearly must be preferred, as the VCO designed at double frequency features a smaller coil, and the area of the master–slave flip-flops in sub-μm CMOS is negligible. Also, in ZERO-IF receivers, this solution should be preferred because it avoids direct parasitic coupling between the VCO and receiver input. There is a tradeoff between power consumption and phase noise and this technique will provide better phase noise [2].

The leading idea of this article is to produce a design that provides better phase noise, low power consumption, accurate quad oscillation, and a better frequency tuning range with a reduced chip size. In this regard, we adopted the best technique of the VCO and frequency divider and integrated them at their optimal level. The proposed VCO technique naturally provides an output CM level about equal to VDD/2. The technique can be viewed as complementary cross-coupled CMOS (NMOS and PMOS pair) sharing the same bias current. Instead of using a CMOS current source at the tail of the structure, we used a high-impedance passive inductor to save the voltage headroom and reduce the noise factor. To maximize the tuning range, we carefully selected the CMOS dimensions as mentioned in the article's design methodology in Section 3.1. More than fifty iterations were carried out during the design, integration, and simulation process by using TSMC 65 nm with a 1 poly and 9 metals (1P9M) CMOS process in the Cadence Virtues CAD environment. This article's results show that we achieved better phase noise, ultra-low power consumption, and better quad oscillation with the reduced chip area as compared to other related work.

1.2. The Contribution

The main objective of our work is to further reduce the phase noise and power consumption along with a reduced chip size. The proposed technique achieves phase noise as low as −118.36 dBc/Hz at a 1 MHz offset frequency with 1.2 V supply voltages and

consumes only 0.47 mW of power. The proposed technique consumed 76% less power as compared to the latest related work published in [11]. The active area of the chip including the pads is only 0.47 mm^2; furthermore, in the proposed design, we used a DFF master–slave $\frac{1}{2}$ frequency divider to obtain the accurate quadrature oscillation.

In this article, we used TSMC 65 nm with 1 poly and 9 metals (1P9M) CMOS technology in a Cadence Virtues CAD environment for the VCO schematic design, simulations, layout, and post-layout simulations. This article is structured in four sections. Section 2 of the paper discusses the LC-VCO and frequency divider designs. Section 3 presents the results of the post-layout simulation employing 0.65 m CMOS technology and its comparisons. Section 4 of the paper describes a brief conclusion.

2. Literature Review

Commonly Used Techniques in Traditional Low-Voltage LC-VCO

To reduce phase noise in cross-coupled oscillators, many research efforts have been carried out in recent years, each of which has distinct advantages and disadvantages. In an earlier study, by improving the resonator's design, the researchers also attempted to reduce phase noise as discussed in [12–14]. In [10], an active resonator with a high Q factor was used to minimize phase noise. In [13,14], the study's findings were that the oscillator's phase noise efficiency can be enhanced by increasing the inductance energy factor (IEF). In [15], the tail current shaping technique was used to manage tail current and improve phase disturbance.

One of the most popular types of oscillators is the quadrature differential cross-coupled LC tank oscillator, as they have advantages including better phase noise performance, less power consumption, and simple and straightforward designs, as reported in [7,16–18]. However, the researchers faced significant design challenges while trying to obtain lower phase noise in these oscillators. The analysis and prediction of phase noise or timing jitter in oscillators is a particularly difficult problem, since oscillators are independent non-linear circuits and their non-linearity is essential to their operation and evaluation of their noise performance. Along with LC tank loss, the MOSFET switching pairs and tail biasing MOSFET also produced some noise in this kind of oscillator.

Traditionally, PMOS or NMOS devices, or both together, could be utilized to produce a quadrature differential cross-coupled pair (CMOS). The quadrature differential cross-coupled MOS oscillator consumes less power, but the phase noise is increased because of noise from the extra cross-coupled block as compared to a single MOSFET. However, the power consumption of the CMOS circuit is almost half that of single pair topologies [6,15].

The complementary quadrature differential cross-coupled is the widely used technique of the LC–VCO presented in [2,12]. The circuit employs two MOSFETs to provide negative transconductance ($-gm$), which compensates for LC tank losses. It lessens the $1/f$ noise and has a symmetric and straightforward structure. However, due to the tail current source's limited voltage headroom, this configuration is inappropriate for low-supply voltage operation. A different method employed in [16] is effective for low-power applications. In a typical quadrature differential cross-coupled VCO, cross-connected PMOS and NMOS transistors produce the same negative conductance because of half-power dissipation. Since there is no tail current circuit, this architecture will not impact the headroom. Furthermore, because of its low power supply voltage and lack of a tail MOS current source in its design, this VCO is more sensitive to PVT changes. It has been reported in [19] that the VCO's performance would be improved by increasing its tolerance to PVT fluctuations by adopting an adaptive body-biasing approach.

The capacitive source degeneration (CSD) technique is used to improve the phase noise performance of an LC oscillator. In the CSD technique, a capacitor is placed in series with the input signal source of the LC tank, which provides a negative feedback path that reduces the amplitude of the oscillation signal. This reduces the non-linearity of the oscillator and improves its phase noise performance, as reported in [15,20,21]. Due to the improper selection of degeneration capacitors, the primary downside to this approach

is that it lowers the resonator's effective quality factor and hurts phase noise. The noise source is increased by placing an active MOS device in the tail. This technique lowers the thermal noise of the tail current by filtering several tail current harmonics through the source capacitor.

The researcher completed a lot of work to reduce the phase noise, like a traditional current source, which utilizes RC for noise filtering, tail filtering using LC, and sinusoidal noise shaping. All these techniques have some trade-offs. For example, by employing the notch filter feature of the LC circuitry, the second harmonic of the tail current noise can be eliminated. To prevent an increase in both the noise injected into the tank and the tank loss, sinusoidal noise shaping requires an external bias voltage and, respectively, larger resistors, as reported in [15,22].

This work aims to address some of the limitations that are associated with LC-VCO design, including the effect of the LC tank, a tail-active MOS device for the current source, large resistance at the tail, or the unsuitable selection of a degeneration capacitor. These limitations may negatively impact the performance of the LC-VCO. The LC-VCO is discussed in the next section, which may involve various techniques or strategies to address the identified limitations and describe the circuit diagram, components, parameters, or equations used in the design process. Additionally, we compare the suggested LC-VCO's performance to other methods that are already in use or gauge its main characteristics, such as frequency stability, phase noise, power consumption, or tuning range [6,23].

3. Design Methodology

3.1. The Proposed Circuit Design

In this article, a differential quadrature differential cross-coupled PMOS and NMOS LC-VCO with a tail inductor D flip-flop (DFF) frequency divider is proposed. In the design, the quadrature differential cross-coupled CMOS architecture is used to provide high linearity and low phase noise performance.

The cross-coupled architecture ensures that the output signals have a 180-degree phase difference between the complementary outputs, which improves the circuit's linearity. The differential architecture also provides a high common-mode rejection ratio (CMRR), which reduces the impact of common-mode noise on the output signals. The DFF frequency divider is used to divide the frequency of the output signals by a factor of two. The output of the VCO is connected to the clock input of the DFF, and the divided output signals are obtained from the Q and Q' outputs of the DFF. The use of a frequency divider allows the circuit to generate two signals with a 90-degree phase difference at a frequency that is half the frequency of the VCO output.

Here are some key design aspects to consider when implementing this VCO:

Differential cross-coupling: The VCO employs two pairs of PMOS and NMOS transistors that are cross-coupled differentially to create a positive feedback loop. Cross-coupling topology is designed to provide sufficient feedback to achieve the desired oscillation frequency and phase noise performance.

LC tank design: The resonant frequency and Q factor of the LC tank are critical parameters that determine the output frequency and phase noise performance of the oscillator. The tank should be designed with an appropriate inductance and capacitance to achieve the desired resonant frequency and Q factor.

Tail inductor design: The tail inductor is an additional inductor that is connected to the common source node of the differential transistors. It provides additional negative feedback to improve the oscillator's phase noise performance. The tail inductor is designed with an appropriate inductance value and quality factor to achieve optimal performance.

Transistor sizing and biasing: The PMOS and NMOS transistor sizes are appropriately chosen to achieve the desired oscillation frequency and phase noise performance. The biasing conditions of the transistors are chosen carefully to ensure optimal power consumption and linearity.

Parasitic elements: Parasitic elements, such as resistance and capacitance, can have a significant impact on the oscillator's performance. These elements can contribute to power consumption, noise, and frequency stability. It is important to carefully account for these parasitic elements in the design and layout of the oscillator.

3.2. A Quadrature Differential Cross-Coupled LC VCO Is Proposed

In this structure, a VCO design is intended for use in 2.4 GHz IoT/BLE devices such as direct conversion, low IF receivers, or WSN sensors. The design replaces the tail MOS transistor with a high-quality factor inductor to reduce tail noise effects and improve the effective quality factor of the LC tank. The VCO operates at twice the needed LO frequency and is followed by a frequency divider's bias current. The design is aimed at achieving accurate quadrature signal generation while consuming low power.

Figure 1 depicts the proposed VCO, which features the high-quality factor inductor in place of the tail transistor. This modification results in a reduction in the tail noise current and an increase in the effective quality factor of the LC tank, thereby improving the overall performance of the oscillator. The VCO is designed to operate at 2.4 GHz, making it suitable for use in IoT/BLE devices. Its power-efficient design and accurate quadrature signal generation make it well-suited for low-power wireless applications.

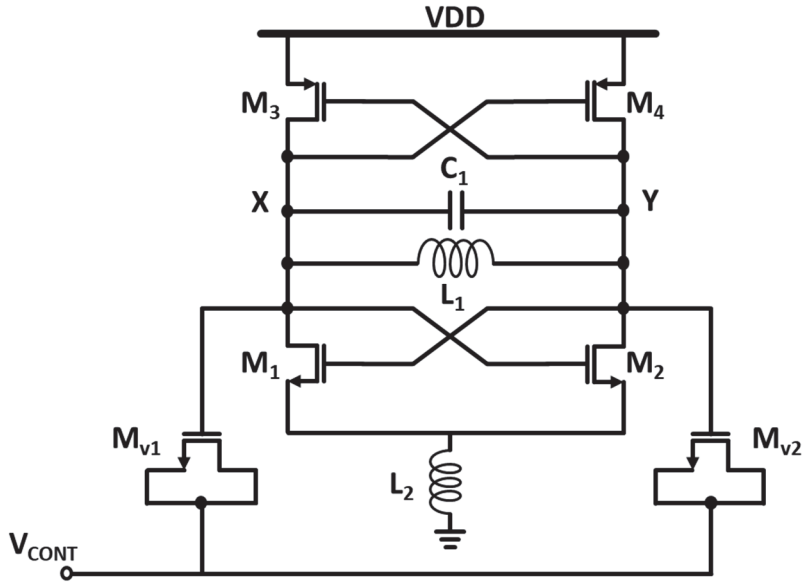


Figure 1. The schematic of the proposed differentially quadrature differential cross-coupled PMOS and NMOS LC-VCO with a tail inductor.

The proposed technique is based on two back-to-back quadrature differential cross-coupled inverting CMOSs along with a high impedance inductor at the tail for biasing, and provides truly differential operation. The bias current is reused by the PMOS devices, which provide high transconductance, and the quadrature differential cross-coupled NMOS and PMOS pair shares the same current. However, it offers double the voltage swing, which places points X and Y at VDD/2 at the CM level. The capacitive varactors are used to adjust the resonance frequency; the LC tank is employed to reach the desired frequency. The on-chip high Q integrated inductor is used to reduce losses in the LC tank.

In the proposed design technique, the PMOS transistors utilize the bias current to increase transconductance. However, a more significant benefit of other LC topologies, such as traditional two LC tanks with just NMOS quadrature differential cross-coupled VCOs and top-biased LC tank quadrature differential cross-coupled VCOs, is that they provide double the voltage swing for a given bias current and inductor design. To comprehend this issue, we suppose that L1 and L2 in a traditional two-tank circuit correspond to LXY in

the complementary architecture. Consequently, LXY displays an equal parallel resistance of 2Rp.

The design of the proposed VCO consists of a pair of PMOS and NMOS transistors coupled back-to-back to form differential complementary CMOS architecture. The PMOS transistors staked at top of the circuit provide a high transconductance. This approach anticipates an output common-mode (CM) level equal to VDD/2. The suggested technique yields double the voltage swing for a given bias current as compared to typically only NMOS, PMOS, or LC CMOS pairs. The nodes LXY present an equivalent parallel resistance of 2Rp. In the design, a high-impedance inductor is introduced at the tail of the VCO for biasing instead of the conventional MOS current source. This induction of the inductor is used to block the 1/f noise to enhance spectral purity. This technique will save the voltage headroom of the supply voltage. Furthermore, due to no 1/f noise, the phase noise was also reduced, as reflected in the results.

The paragraph describes the role of the passive high-impedance tail inductor in the performance of the VCO. The high-impedance inductor is placed at the tail for filtering purposes and to preserve voltage headroom while ignoring frequency modulation. Traditionally, the output common-mode (CM) level is modulated by the capacitances of the varactors, which are cross-coupled with a MOSFET current source at the tail for biasing. This can result in poor phase noise due to the modulation of the CM level. However, the article addresses this issue by replacing the MOS current source with a high-quality factor inductor at the tail. This modification reduces the phase noise and improves the performance of the VCO.

The MOS varactor is occupied as a PN junction, with Mvar1 and Mvar2 appearing parallel to the tanks. The two factors that determine a varactor's performance are (a) the capacitance range, or the ratio between the maximum and minimum capacitances it can deliver as the applied voltage varies, and (b) the quality factor, which is constrained by the series resistance within the varactor structure [22]. As a consequence of the high impedance inductor at the tail, the design saves the voltage headroom, lowers phase noise, and ignores frequency modulation. Because the complementary structure has quadrature differential cross-coupled pairs of PMOS and NMOS transistors, which are useful in deep submicron CMOS technologies, it exhibits resilience to process changes. The capacitance of M_{V1} and M_{V2} reduces when V*cont* increases from zero to VDD because their gates are operating at an average level equal to VDD, maintaining a positive gate-source voltage. This behavior persists even when there are significant voltage fluctuations across M_{V1} and M_{V2} and at X and Y. The control voltage (V*cont*) across each varactor varies from zero to VDD. There is a monotonic decrease in the varactor's capacitances which is observed as the control voltages increase. Hence, the oscillation frequency may be written as,

$$\omega_{osc} = \frac{1}{\sqrt{L1(C1 + Cvar)}} \quad (1)$$

Cvar is the average capacitance of each varactor.

In the case of the proposed LC-VCOs, the RF circuit sizing tool was used to optimize the circuit performance by exploring various design parameters such as the sizes of the transistors, capacitors, and inductors, and their respective placements in the circuit. The goal was to achieve the desired performance specifications, such as frequency stability, phase noise, and power consumption while minimizing the impact of noise and other sources of interference. There are boundaries for design variables (transistor width, length, bias current, inductor value, Q factor (size), and varactor (control voltages and capacitance value)).

The design methodology described here involves optimizing the components of a voltage-controlled oscillator (VCO), including the inductor, varactor, and active circuit. The focus of the optimization process is to improve the power consumption and phase noise performance of the VCO.

The merit of paper is to design an ultra-low-power VCO. The design methodology emphasizes the importance of optimizing each component of the VCO to meet the required performance parameters. By optimizing the inductor, varactor, and active circuit, it is possible to enhance the VCO's phase noise and power consumption efficiency overall. The design flow is to be considering a part of optimizing the overall design of the VCO. To improve the design, three key considerations have been taken into account, as is shown below in Figure 2. To reduce the resistive loss (gL) and increase the quality factor, the inductor must first be tuned, after which the varactor needs to be optimized, and then the active circuit needs to be optimized.

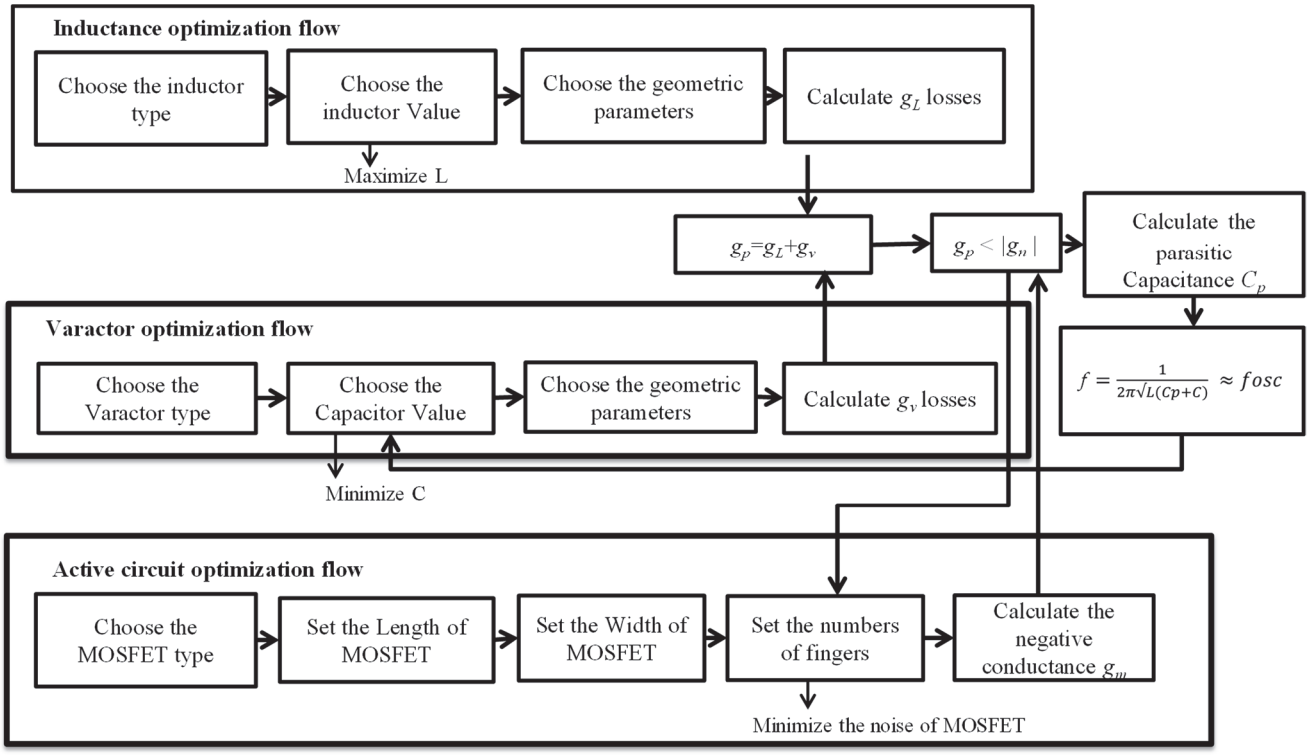


Figure 2. Design flow of ULP LC-VCO.

Inductance optimization:

When considering the design of a ULP VCO, the inductor optimization process requires an abundance of focus. A suitable inductance value and quality factor are used in the design of the tail inductor to ensure optimum performance. The initial phase is to select the type of inductor based on the desired boundaries.

In the proposed design, we selected a high-impedance passive inductor (spiral_std_mu_z) from the tsmcN65 library. In comparison with the other types of inductors, this type of inductor presented a good compromise between quality factor (QL), resistive loss (gL), occupation area, and self-resonant frequency (SRF). The following phases involve selecting the proper inductance size (width and length), as well as geometrical variables such spacing, count of turns, inner radius, and guard ring distance. By choosing a high inductor value with minimal series resistance and maximum quality factor, both power consumption and power factor can be reduced. It is important to note that increasing L's value is limited by its SRF, which should be greater than the oscillation frequency. The inductor track width (W) and the number of turns (N) have been adjusted. The minimum number of turns (Nmin) is needed to reduce the resistive loss (gL). As a result, Nmin must be increased to increase the inductance value. In addition, SRF, QL, and gL are significantly impacted by the inductor's track width. Increasing track width typically enables a reduction in gL followed by an increase in QL. However, it has several downsides, like increased substrate

coupling. The frequency of self-resonance may decrease as a result. For the inductive action to continue, this SRF should be greater than the operational frequency. Therefore, we had used the minimum track width (Wmin) on occasion to boost the SRF.

Varactor optimization:

The phase noise and power dissipation capabilities of the LC resonator are greatly influenced by the varactor's quality factor, making it a crucial component of the device. In order to evaluate the performance of the VCO, the varactor must be optimized. The initial phase of the optimization technique is to select the appropriate varactor type based on the application-specific constraints. In particular, MOS varactors have been proposed as their tuning range is highly constrained. The diode varactor, on the other hand, offers a good compromise between linearity, quality factor (Qv), and effective parallel equivalent conductance, making it desirable for applications with high limits on consumption. In order to attain the wide tuning range for this design, a MOS varactor has been adopted. In order to mitigate PN and power consumption, the value of C should be lowered. The frequency tuning range will, however, be restricted as a result. Subsequently, it is necessary for adjusting the varactor's physical settings. In terms of tuning range and PN, these properties have an impact on the oscillator's performance.

Active circuit optimization:

A key element of the VCO employed to compensate for tank loss is the active circuit. It also reaffirms parasitic components, though, which may manipulate the oscillation frequency and compromise the phase noise of the VCO. The switching speed and power consumption of this circuit can be improved by employing low-leakage transistors with modest channel lengths. In order to provide the lowest transconductance, transistor width is determined next. The performance of the VCO in terms of noise and power consumption is further improved by using the maximum number of fingers (NF), which lowers the gate resistance.

Furthermore, in this article, we used TSMC 65 nm with I poly and 9 metal (1P9M) CMOS technology in a Cadence Virtues CAD environment for the VCO schematic design, simulations, analysis of the simulation results, layout, and post-layout simulation. Optimizing a VCO is a complex and iterative process. In this research, the optimizing process took several iterations to obtain the best results. The following steps have been taken to design and optimize the proposed VCO.

VCO specifications: The leading idea of this article is to produce a design that provides better phase noise, low power consumption, accurate quad oscillation, and a better frequency tuning range with reduced chip size. In this regard, we adopted the best technique of the VCO and frequency divider.

VCO schematic: Using Cadence Virtuoso, create the VCO schematic that meets the specifications of cross-coupled LC VCO. Choose an appropriate MOS sizing as the transistor size is crucial in optimizing the VCO.

Simulate the VCO: Simulate the VCO using Cadence Spectre in TSMC 65 nm. The simulation should include frequency response and phase noise. Completing the proper biasing can ensure stable oscillation and minimize phase noise. Adjust the voltage levels and current source of the VCO to be properly biased.

Analyze the simulation results: Analyze the simulation results to identify areas that require improvement. To reduce the phase noise, use different transistor sizes and adjust the biasing.

Modify the VCO schematic: Based on the analysis of the simulation results, modify the VCO schematic to improve its performance. This may include changing the transistor sizes, adding or removing components, and adjusting the biasing.

Simulate and analyze the modified VCO: Simulate the modified VCO and analyze the simulation results to determine if the performance has been improved. If necessary, repeat steps 5 and 6 until the desired performance is achieved.

Lay out the VCO: Once the VCO schematic has been optimized, lay out the VCO using the Cadence Virtuoso layout editor. Ensure that the layout adheres to the SMC 65 nm with 1P9M CMOS technology rules and guidelines.

Verify the layout: Verify the layout using the Cadence Virtuoso verification tools to ensure that it meets the design rules and guidelines, and is free from any errors.

Simulate the post-layout VCO: Simulate the post-layout VCO using the Cadence Spectre simulation tools to verify its performance.

Analyze the simulation results and perform optimization: Analyze the simulation results of the post-layout VCO and perform any necessary optimization to further improve its performance.

All these steps were carried out to produce the best results. This article's results show that we achieved lower phase noise, ultra-low power consumption, and better quad oscillation with the reduced chip area as compared to other related work.

Overall, this design methodology emphasizes the importance of optimizing each component of the VCO to meet the required performance parameters. By following this methodology and optimizing the inductor, varactor, and active circuit, it is possible to enhance the VCO's phase noise and power consumption efficiency. Furthermore, the article proposes an optimized approach for addressing the trade-off between phase noise and power consumption in VCO design by using a high-quality factor inductor at the tail to minimize phase noise. This modification improves the performance of the VCO and makes it suitable for use in low-power wireless applications. A high-impedance passive inductor (spiral_std_mu_z) is used from the tsmcN65 library at the tail for filtering, which preserves voltage headroom and ignores frequency modulation. The tail inductor provides additional negative feedback to improve the oscillator's phase noise performance as well. The induction of the tail inductor instead of the conventional MOSFET current source results in a reduction in the tail noise current and an increase in the effective quality factor of the LC tank, thereby improving the overall performance of the oscillator.

3.3. Frequency Divider Design

An effective frequency divider is an essential component in many electronic circuits and systems, particularly in wireless communication applications. The primary function of a frequency divider is to divide the input frequency by a fixed integer value to generate a lower-frequency output signal. However, an effective frequency divider must not only divide frequencies correctly across the entire band of interest, but also add very little noise to the system.

There are different topologies of frequency dividers. In general, the injection-locked dividers have the simplest structure and the narrowest locking range, which results in the greatest operation frequency. Only for low frequencies do static dividers show a reasonably wide range of operation. Miller dividers, also referred to as regenerative dividers, serve as a common way between the two. Among them, the static dividers for relatively low frequencies would be a better choice for this research perspective as they cater for 2.4 GHz applications. The static divider has some different techniques like the LC tank, Current Mode Logic CML ring, and CML DFF. The D flip-flops 1/2 frequency divider utilized current mode logic (CML) with negative feedback, whereas the LC tank and CML ring frequency dividers employ injection locking. The DFF frequency divider is used by most researchers in VCOs and PLL circuits, as reported in [24–26].

Static frequency dividers have been extensively used in synthesizer design because of their ease of implementation and robustness. MOS current mode logic (CML) is commonly used for D-latch applications in a static frequency divider. CML logic can handle high operation frequencies due to its small voltage swing, which reduces rise and fall times. In addition, the CML logic's inherent differential configuration would reduce switching and supply noise. A power-efficient method for reusing current is the LC VCO followed by a 1/2 frequency divider circuit. When oscillation amplitude is decreased, the voltage

headroom for each MOS is likewise decreased, which results in more phase noise than a separated VCO and divider. This technique produces an accurate quadrature signal.

The proposed VCO is followed by a 1/2 frequency divider with two D-type flip-flop latches for quadrature waveform at the desired frequency, as shown in Figure 3. Two D latches constitute the frequency divider's adopted circuit based on the master–slave formation, i.e., the inverted output of the slave latch (MD2, ML1) connect to the input of the master latch (MD1, ML1), which is also reported in [6,26].

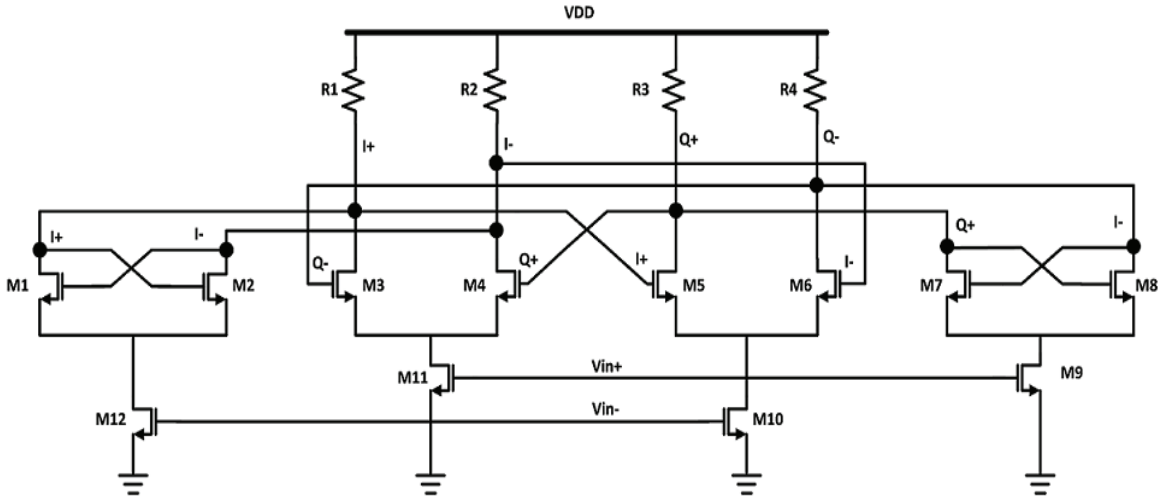


Figure 3. The schematic of the proposed CML D flip-flop 1/2 frequency divider.

The master–slave DFF latch formation is a popular technique for implementing high-speed digital circuits. To create the differential and quadrature phases in the latch formation, the output of the master DFF is delayed by half an input clock cycle, while the output of the slave DFF is delayed by a quarter of an output clock cycle. This delay creates a phase difference between the two outputs, which can be used to drive downstream circuitry. The sizing of the MOS transistors in the divider circuit can have a significant impact on the overall performance of the oscillator, including its frequency stability, phase noise, and power consumption. By optimizing the transistor sizes and other parameters in the divider circuit, it is possible to improve the overall performance of the oscillator and achieve self-oscillation at minimum power dissipation. The W_L/W_D widths ratio has a critical effect on increasing the operating frequency of the divider. The master and slave MOS latches width ratio determines the operating frequency range of the divider. The simulation results show that, with a small W_L/W_D width ratio, the divider is capable of dividing much higher frequencies but with a higher input frequency range such that (4.4–5.8 GHz @ W_L/W_D = 0.1) compared to a large W_L/W_D ratio, where the lower input frequency range such that (1.8–2.2 GHz @ W_L/W_D = 1), as depicted in Figure 4.

As discussed in [24], a necessary condition of the divider for self-oscillation is

$$gm_L R_{LD} > 1 \quad (2)$$

where gm_L is the transconductance of the latch M_L and R_{LD} is the load resistor of the divider. It is observed that the width of the latch transistor decreases and the transconductance also decreases. To self-oscillate the divider, the load resistance should be increased accordingly, affecting the increase in the output voltage swing. Furthermore, the width of the divider transistor W_D is decreased, causing a further increase in the maximum frequency of the divider. The maximum division frequency and W_L have a monotonic relationship is observed. To ensure that the divider's minimum input division frequency is within the specified frequency range of 2.2 GHz, a low W_L/W_D ratio of 0.6 was selected. This range also gives better amplitude as compared to other W_L/W_D width ratios.

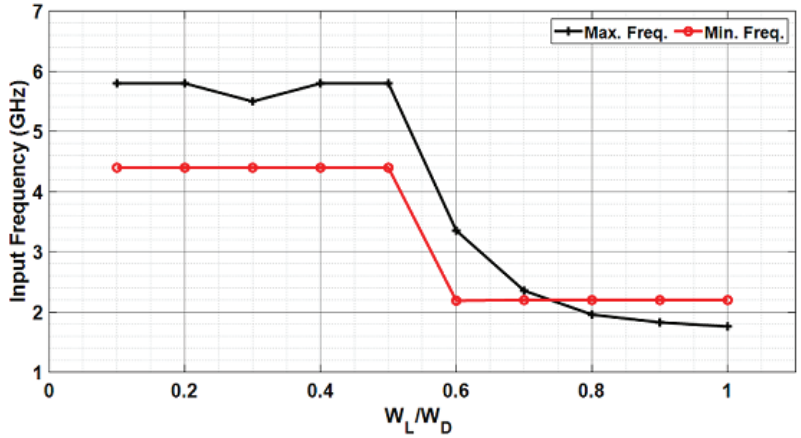


Figure 4. The latch-to-driver width ratio (W_L/W_D) concerning the input frequency range response.

Figure 5 shows the transistor's clock width (W_{CLK}) response concerning the divider's input frequency range. At high frequencies, it is critical to optimize the energy linked to the common source node for a certain externally injected signal. The transistor's clock size and biasing have an important role. For a particular size of the clock transistor, a specific common-mode value produces the maximum self-oscillating frequency [25]. A constant W_L/W_D ratio is used to simulate the response, and it is evident that the divider works at high input frequencies for small-size M_{CLK} transistors such that (4.4–5.8 GHz @ 1 μm). Comparatively, as the M_{CLK} transistor size increased, the input frequency range became narrower such that (1.9–2.2 GHz @ 10 μm).

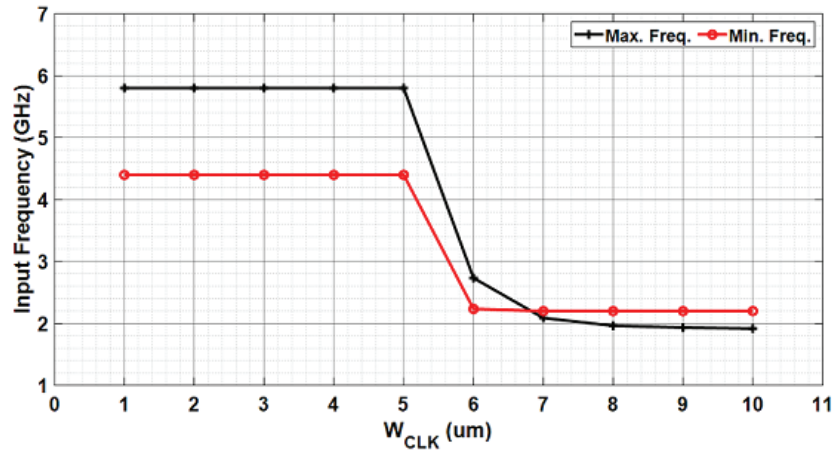


Figure 5. The input frequency ranges as a function of W_{CLK}.

For similar reasons as those cited above for choosing the W_L/W_D ratio, a width of WCLK = 6 μm was chosen for the divider in this work.

4. Post-Layout Simulation Results Using the TSMC 65 nm CMOS Process

This section describes the performance evaluation of the VCO designed with the inclusion of a high-impedance inductor at the tail of two quadrature differential cross-coupled MOSs instead of a conventional MOS current source. The simulation results focus on three performance metrics: phase noise, power consumption, and chip size. Phase noise is an essential parameter in the performance evaluation of a VCO as it determines the amount of jitter or frequency instability in the output signal. Minimizing power consumption is critical in the design of low-power wireless communication systems. By using low-power components, power management techniques, and optimizing the design of individual components, it is possible to extend the battery life of the system. Finally, a

key factor in the design of integrated circuits is the chip size because smaller chips result in lower manufacturing costs and greater integration densities.

The post layout simulations were performed using TSMC 65 nm with 1 poly and 9 metals (1P9M) CMOS technology in a Cadence Virtues CAD environment. Based on the simulation results of the design of the VCO, the performance matrices of the VCO are analyzed. The results are compared with those of a conventional VCO that uses an MOS current source at the tail. The inclusion of the high-impedance inductor is expected to improve the phase noise performance of the VCO while reducing power consumption. Additionally, the design should allow for a smaller chip size.

The proposed work is focused on a quadrature differential cross-coupled CMOS VCO followed by a 1/2 CML DFF frequency divider using a 1.2 V supply voltage which produced low phase noise and consumed low power. The designed VCO using a 2.4 GHz carrier frequency and a 1.2 V supply voltage consumed only 0.47 mW of ultra-low power and has −118.36 dBc/Hz of phase noise at 1 MHz offset with the control voltages (V*cont*) of 1.2 V. The proposed VCO combined with a frequency divider consumed only 2.02 mW power. A small active chip area of 0.19 mm^2 is covered by the proposed VCO with a frequency divider.

Several articles analyzing the performance of the LC VCO have reported a widely acknowledged figure of merit, as indicated below and described in [26]:

$$\mathbf{FoM} = \mathbf{L}(\Delta\mathbf{f}) + \mathbf{10log}\left(\frac{\mathbf{P_{dc}}}{[\mathbf{mW}]}\right) - \mathbf{20log}\left(\frac{\mathbf{f_o}}{\mathbf{F_{offset}}}\right) \quad (3)$$

where L{Δf} is the phase noise measured at a 1 MHz offset frequency, the power consumption (P_{dc}) is measured in mW, and the oscillation frequency is (f_0).

This article establishes a new figure of merit (FoM) expression. The FoM is an important metric in integrated circuit (IC) design that considers multiple factors such as phase noise, power consumption, and chip area. The newly proposed FoM expression includes all these factors and extends Equation (3) which includes the chip area as shown in the below expression.

$$\mathbf{FoM} = \mathbf{L}(\Delta\mathbf{f}) + \mathbf{10log}\left(\frac{\mathbf{P_{dc}}}{[\mathbf{mW}]}\right) - \mathbf{20log}\left(\frac{\mathbf{f_o}}{\mathbf{F_{offset}}}\right) - \mathbf{10log}(\mathbf{chip\ area}) \quad (4)$$

The FoM expression includes a tradeoff between the various factors considered, and the goal is to optimize the FoM value for a given application. By including the chip area in the FoM expression, the new expression allows for a more comprehensive assessment of the IC design, as chip area is an important consideration in IC manufacturing cost and integration density. The new FoM expression provides a valuable tool for IC designers to optimize their designs based on a comprehensive set of performance metrics.

4.1. Phase Noise

This section discusses the phase noise achieved after the simulation. In the presented work, we successfully achieved the required phase noise characteristics at low offset frequencies. The flicker noise is a dominant source of noise at low frequencies, and the VCO design aims to minimize this noise contribution to achieve low phase noise.

As depicted in Figure 6, the phase noise efficiency improved when the control voltages of the VCO were increased from 0 V to 1.2 V.

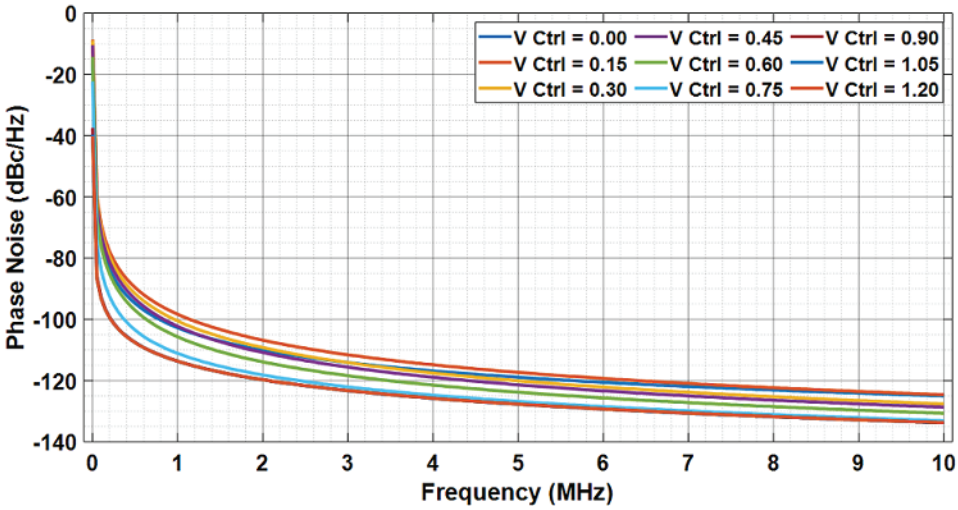


Figure 6. Phase noise v/s frequency at different control voltages.

The lowest phase noise of −118.36 dBc/Hz at 1 MHz offset is achieved at the carrier frequency of 2.4 GHz and a control voltage of 1.2 V, as depicted in Figure 7. The proposed VCO design achieves low phase noise performance by minimizing the effects of flicker noise and optimizing the control voltages. The results show that the VCO design is effective in achieving the required phase noise characteristics, rendering it appropriate for use in a variety of applications, including low IF receivers, wireless sensor networks, and direct conversion receivers.

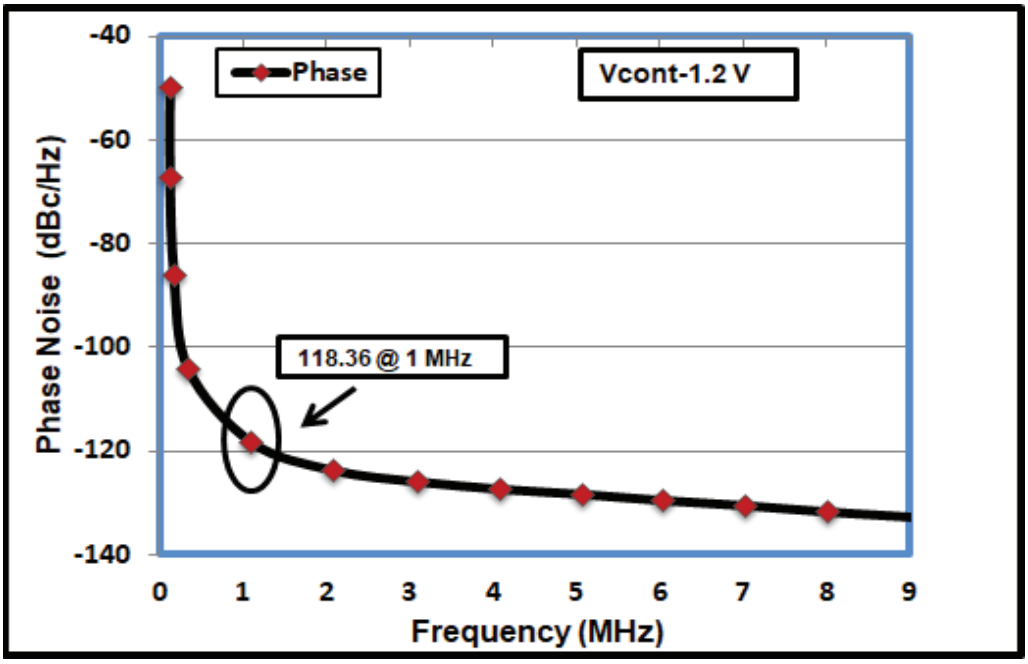


Figure 7. Phase noise −118.36 @ 1 MHz offset frequency.

The quadrature differential cross-coupled VCO and divide-by-two frequency divider's output frequencies may be adjusted between 4.4 GHz and 5.7 GHz, as depicted in Figure 8, where, at minimum control voltages, the frequency is low, i.e., 4.4 GHz, and as the voltages increase, the VCO exhibits a high frequency, i.e., 5.7 GHz. These characteristics of the VCO make it tunable. By changing the variable capacitor's control voltage, the frequency of oscillation may be tuned. The VCO takes around 29 ns to attain a steady amplitude. The time domain output of the designed LC-VCO is present in Figure 9.

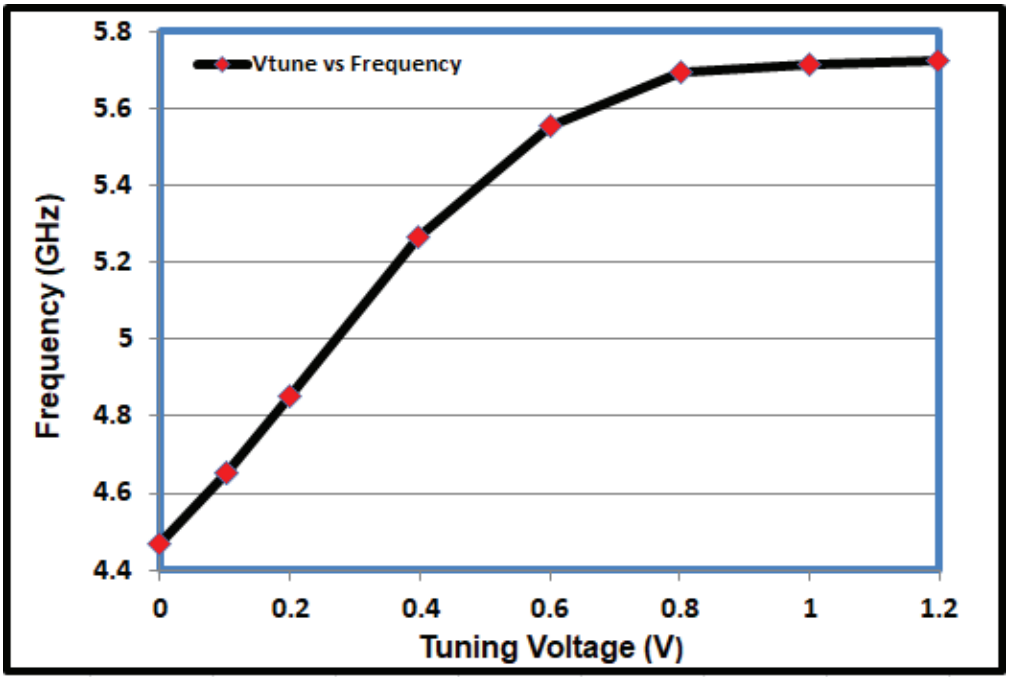


Figure 8. Frequency v/s control voltages.

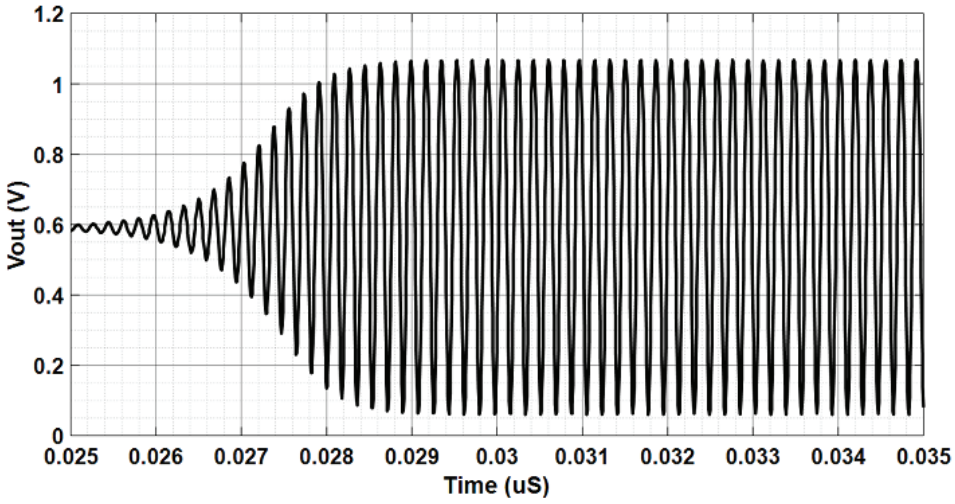


Figure 9. The proposed VCO's time domain output waveform.

In this article, a differential VCO technique has been adopted that consists of an LC tank complementary cross-coupled MOS pair (NMOS and PMOS) operating at double the required LO frequency reuses the bias current of a divide-by-two frequency divider and capacitor varactor for voltage control. The technique provides high phase accuracy and acquires low power and accurate quadrature local oscillator (LO) signal generation. The master–slave flip-flop in series makes it possible to generate two output signals that are 90 degrees out of phase with each other and this constitutes the divide-by-two frequency divider which generates the accurate quadrature LO signals.

The fact that the complementary cross-coupled pair only requires half the current than the cross-coupled structure allows for the more efficient utilization of current resources, leading to lower power consumption. Furthermore, the reduced current requirement in the complementary pair allows for the possibility of increasing the tail current without significant concerns for power consumption. By increasing the tail current, the gain of the VCO can be improved, resulting in better overall performance. The current is reused in

the PMOS and NMOS pair leading to an increase in the transconductance gm. It would double the transconductance *gm* for the same current. The symmetry provided by the complementary topology can help lower phase noise. Phase noise refers to the random fluctuations in the output signal's phase, which can degrade the performance of an oscillator. The balanced structure of the complementary topology can reduce phase noise, which is the unpredictable variation in the phase of the output signal. These fluctuations can negatively impact the oscillator's performance. However, the symmetry of the complementary pair can minimize specific sources of phase noise, resulting in better spectral purity and improved performance.

Furthermore, the most precise quadrature LO signals across a broad frequency range are produced using a double-frequency VCO using a 1/2 frequency divider technique. In this article, a LC tank complementary cross-coupled differential voltage-controlled oscillator (VCO) with master-slave D flip-flops is used to achieve perfect symmetry between the quadrature outputs of an oscillator. This technique addresses the intrinsic asymmetry issue in current reusing and ensures an accurate quadrature phase relationship, leading to improved performance in RF transceivers. To design ZERO-IF receivers, this solution should be preferred because it avoids direct parasitic coupling between the VCO and receiver input. Figure 10 exhibits the quadrature output waveform in the time domain of the proposed VCO with a frequency divider in post-layout simulation.

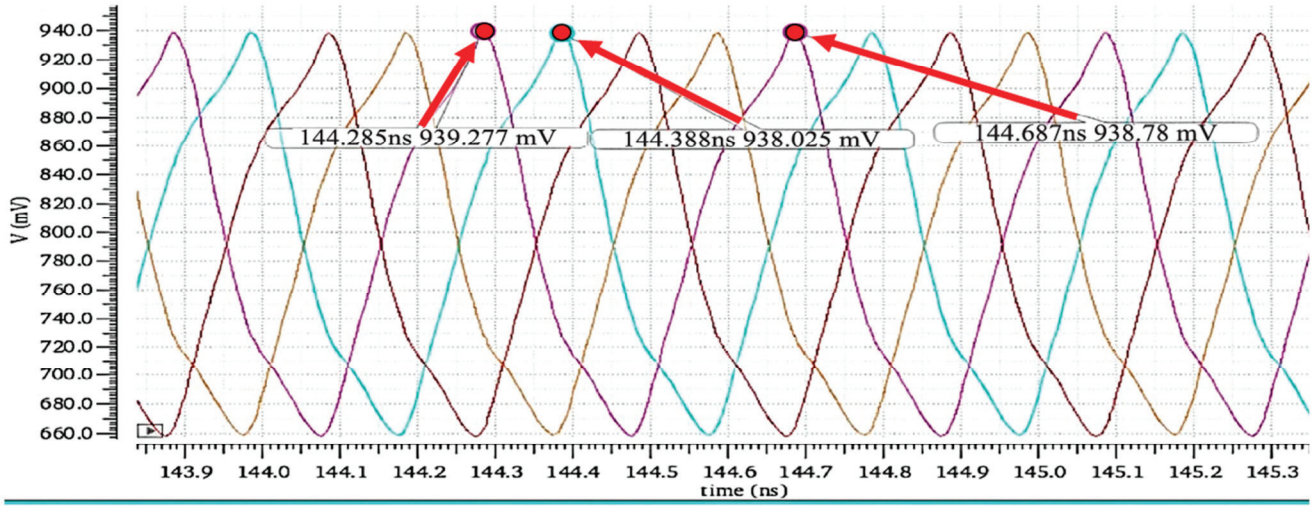


Figure 10. The quadrature time domain output waveform of the proposed VCO with a frequency divider.

The proposed VCO technique naturally provides an output CM level around equal to VDD/2. The technique can be viewed as two back-to-back CMOS inverters or as cross-coupled NMOS and PMOS pairs sharing the same bias current. Instead of using CMOS current source at the tail of the structure, we used a high-impedance passive inductor to save the voltage headroom and reduced the noise factor. To maximize the tuning range, we carefully selected the CMOS dimensions as mentioned in the article.

4.2. Design Layout

The layout area of the presented CMOS VCO and frequency divider architecture in this article occupied a small active area of 0.19 mm^2 of the chip without a pad and 0.47 mm^2 with pads. Figure 11 shows a chip photograph of the proposed LC-VCO. The design presented in this article is simulated with the TSMC 65 nm CMOS technology with 1 poly and 9 metals.

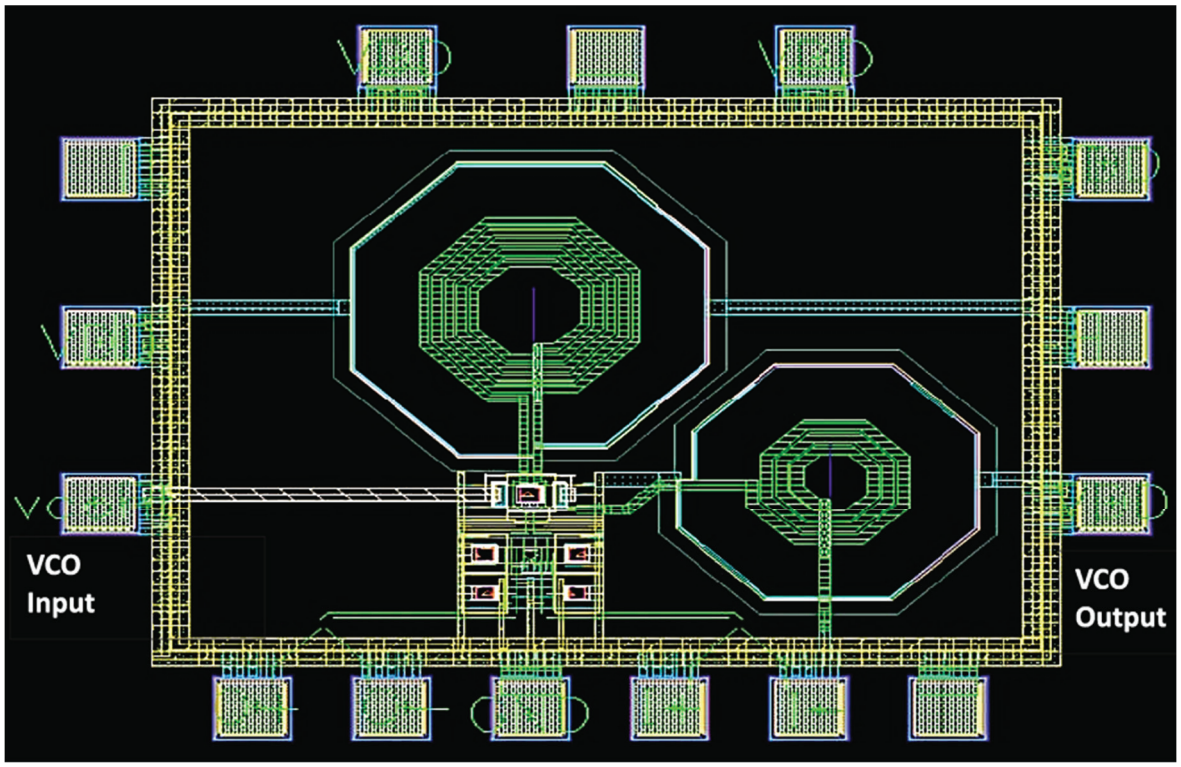


Figure 11. Layout of proposed ULP-VCO using 65 nm CMOS technology.

As highlighted, the simulation results may differ during the manufacturing process. These would be manufacturing deviations, temperature variations, supply voltage variations, or environmental noise sources. These variations would impact design results if not properly simulated considering these factors. To mitigate the impact of manufacturing deviations and environmental influences, designers employ techniques such as process calibration, temperature compensation, voltage regulation, shielding, and isolation to improve the performance and reliability of the complementary structure of cross-coupled VCOs. Furthermore, proper layout techniques, the use of well-matched components, and the careful consideration of environmental factors during the design process can help minimize the effects of these influences.

To mitigate the impact of manufacturing deviations and environmental influences and to maintain the desired performance, we adopted the following:

Layout techniques: Proper layout techniques can minimize the impact of environmental influences. Careful placement of critical components, proper grounding, and separation of sensitive RF circuitry from noise sources reduced the effects of noise and interference.

Simulation and modeling: Advanced simulation tools and accurate models enabled us to predict the impact of environmental influences during the design phase. By simulating the behavior of RF circuits under different environmental conditions, it optimized circuit performance, selected the appropriate compensation techniques, and ensured robustness against environmental variations.

These techniques collectively help mitigate the influence of environmental factors on RF circuits, maintain consistent performance, and ensure reliable operation across different operating conditions and environments.

We used TSMC 65 nm with 1 poly and 9 metals (1P9M) CMOS technology in Cadence Virtues CAD environment for the VCO schematic design, simulations, analysis of the simulation results, layout, and post-layout simulation. To cater to the manufacturing deviations and environmental influences and maintain the desired performance, Cadence has tools to account for real-world effects in the development of a VCO. We adopted multiple steps, and some are as follows:

Circuit Simulation: After the selection of the appropriate components and schematic design, we used Cadence's circuit simulation tool SpectreRF 65 nm to perform various simulations. These simulations help analyze the circuit's behavior under different operating conditions, including manufacturing variations and environmental influences.

Layout Design: Once the circuit behavior was validated through simulations, we went through the layout design phase. We used Virtuoso Layout Suite to create the physical layout of the VCO circuit, considering design rules, parasitic effects, and the manufacturing process.

Design Rule Checking (DRC) and Layout Versus Schematic (LVS) Checks: Before proceeding further, we used Cadence's DRC and LVS tools to ensure that the layout adhered to the design rules and matched the schematic connectivity accurately.

Post-layout Simulation: Once the layout was verified, we performed post-layout simulations to evaluate the circuit's performance under real-world conditions. This step considered parasitic effects, such as parasitic capacitance and inductance, which can significantly affect the VCO's behavior.

Due to some limitations, we would not go for the fabrication of the chip to further prototype testing and validation after. Unfortunately, up until now, this research received no specific grant from any funding agency in the public or commercial sectors. If we found any potential collaborator in near future, we would definitely go for the chip fabrication through TSMC Taiwan.

4.3. Comparison with Previous Work

The proposed LC cross-coupled VCO with a high impedance passive tail inductor followed by a frequency divider in this paper has exhibited better phase noise, less chip area, i.e., 0.19 mm^2, and consumed only 0.47 mW of power. The leading idea of the article is to produce a design that provides better phase noise, low power consumption, accurate quad oscillation, and a better frequency tuning range with reduced chip size. The citations cover a wide range of topics related to oscillator design, including low-phase noise design, low-power operation, frequency dividers, and various techniques for improving VCO performance. There are some recent works but with different CMOS process, techniques, and carrier frequency are cited in [27–31].

To fairly compare of our work with other VCO techniques, we only cater to the frequency range of 2.4 GHz. We have adopted the conventional state-of-the-art FoM equations as well, and compared the VCO results with other similar works. To better understand and elaborate on our results, we compare the results of our proposed VCO with the conventional FoM equation and with the FoM equation including chip size as well, as described in Tables 1 and 2. To compare this work with other related works, we used conventional FoM equations.

$$\mathbf{FoM} = \mathbf{L}(\Delta\mathbf{f}) + \mathbf{10log}\left(\frac{\mathbf{P_{dc}}}{[\mathbf{mW}]}\right) - \mathbf{20log}\left(\frac{\mathbf{f_o}}{\mathbf{F_{offset}}}\right) \tag{5}$$

$$\mathbf{FoM} = \mathbf{L}(\Delta\mathbf{f}) + \mathbf{10log}\left(\frac{\mathbf{P_{dc}}}{[\mathbf{mW}]}\right) - \mathbf{20log}\left(\frac{\mathbf{f_o}}{\mathbf{F_{offset}}}\right) - \mathbf{10log}(\mathbf{chip\ area}) \tag{6}$$

The proposed VCO has produced -196.44 dBc/Hz of FoM. Overall, this research exhibits a better figure of merit than other related works.

Table 1. Performance comparison of LC-VCO with other similar VCO designs.

Simulated/ Measured	FoM (dBc/Hz)	Chip Area (mm^2 (Active))	Power Consumption (mW)	Phase Noise @ 1 MHz (dBc/Hz)	Supply Voltage (V)	Carrier Frequency (GHz)	CMOS Process (nm)	Reference
S	−184.47	0.63	8.22	−125	1.5	2.7	180	[4]
M	−179.7	0.72	4.32	−121.5	1.8	1.58	180	[10]
S	−192.22	0.48	2.4	−130	1.2	2	130	[23]
M	−187	1.44	2.92	−117.4	1	5.13	180	[32]
S	−186.91	0.837	2.04	−122.4	1.2	2.4	130	[11]
S	−189.24	0.19	0.47	−118.36	1.2	2.4	65	This Work

Table 2. Performance comparison of LC-VCO with other similar VCO designs including chip area.

Simulated/ Measured	FoM (dBc/Hz)	Chip Area (mm^2 (Active))	Power Consumption (mW)	Phase Noise @ 1 MHz (dBc/Hz)	Supply Voltage (V)	Carrier Frequency (GHz)	CMOS Process (nm)	Reference
S	−186.47	0.63	8.22	−125	1.5	2.7	180	[4]
M	−177.7	0.72	4.32	−121.5	1.8	1.58	180	[10]
S	−189.04	0.48	2.4	−130	1.2	2	130	[23]
M	−188.53	1.44	2.92	−117.4	1	5.13	180	[32]
S	−187.68	0.837	2.04	−122.4	1.2	2.4	130	[11]
S	−196.44	0.19	0.47	−118.36	1.2	2.4	65	This Work

5. Conclusions

This article presents a tunable quadrature differential cross-coupled CMOS LC-VCO followed by a 1/2 DFF frequency divider for low-power, low-phase IoT/BLE receivers and wireless sensors. An ultra-low-power VCO with a tuning range of 4.4 to 5.8 GHz was designed using TSMC 65-nm CMOS technology. The technique is constructed on two back-to-back quadrature differential cross-coupled inverting CMOSs through a high-impedance on-chip passive inductor at the tail and allows for truly differential operation followed by a $\frac{1}{2}$ DFF frequency divider producing accurate quadrature outputs. In the design, a high-impedance inductor is used at the tail for filtering, and this preserves voltage headroom and ignores frequency modulation.

The designed VCO operates at 2.4 GHz carrier frequency and 1.2 V supply voltage consuming only 0.47 mW of ultra-low power and has −118.36 dBc/Hz of phase noise at 1 MHz offset with the control voltages (V*cont*) of 1.2 V. The proposed VCO combined with a frequency divider consumed only 2.02 mW power. The active area of the chip is 476 × 416 m^2 without pads and 783 × 638 m^2 with pads. A figure of merit (FoM) of −196.44 dBc/Hz was produced by the proposed VCO. In comparison to other related research, this work exhibits a higher figure of merit (FoM).

Future Enhancement:

The fabrication and testing of the simulated ULP VCO design are important steps towards validating the design and demonstrating its potential impact in the field of wireless communication. The use of a well-developed IC design tool library for 65 nm CMOS technology from TSMC made the design process more efficient and cost-effective.

Once the ULP VCO design is fabricated and tested, it can be evaluated for its performance in terms of frequency stability, phase noise, phase error, and power consumption. This will provide valuable data that can be used to further optimize the design and evaluate its suitability for specific applications. The potential applications for IoT/BLE receivers and WSN devices make this design highly impactful in the field of wireless communication. Its successful fabrication and testing can lead to the development of more efficient and

reliable IoT/BLE receivers and WSN devices, which can have a positive impact on various industries, such as healthcare, industrial automation, and smart cities.

Author Contributions: Conceptualization, M.F.S. and M.K.M.; methodology, M.F.S. and M.R.; investigation, M.F.S. and M.R.; supervision, M.K.M. and A.R.M.; writing—original draft, M.F.S. and M.K.M.; review and editing, M.F.S., M.K.M. and A.R.M. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: All the materials used in the study are mentioned within the article.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Chlis, I.; Pepe, D.; Zito, D. Comparative analyses of phase noise in 28 nm CMOS LC oscillator circuit topologies: Hartley, colpitts, and common-source cross-coupled differential pair. *Sci. World J.* **2014**, *2014*, 421321. [CrossRef] [PubMed]
2. Park, K.-G.; Jeong, C.-Y.; Park, J.-W.; Lee, J.-W.; Jo, J.-G.; Yoo, C. Current Reusing VCO and Divide-by-Two Frequency Divider for Quadrature LO Generation. *IEEE Microw. Wirel. Compon. Lett.* **2008**, *18*, 413–415. [CrossRef]
3. Ji, X.; Wu, J.; Shi, L. Current reused Colpitts VCO and frequency divider for quadrature generation. In Proceedings of the 2011 International Conference on Electric Information and Control Engineering, ICEICE 2011—Proceedings, Wuhan, China, 15–17 April 2011; pp. 256–259. [CrossRef]
4. Yu, F.; Tang, Q.; Wang, W.; Wu, H. A 2.7 GHz Low-Phase-Noise LC-QVCO Using the Gate-Modulated Coupling Technique. *Wirel. Pers. Commun.* **2015**, *86*, 671–681. [CrossRef]
5. Lee, K.K.; Bryant, C.; Törmänen, M.; Sjöland, H. A 65-nm CMOS ultra-low-power LC quadrature VCO. In Proceedings of the 2009 NORCHIP, Trondheim, Norway, 16–17 November 2009; pp. 1–4. [CrossRef]
6. Razavi, B. *RF Microelectronics*, 2nd ed.; Prentice Hall Communications Engineering and Emerging Technologies Series; Prentice Hall Press: Hoboken, NJ, USA, 2011.
7. Liu, P.; Sah, S.P.; Jung, J.; Upadhyaya, P.; Heo, D. Load independent bulk-coupled low power quadrature LC VCO. In Proceedings of the 2012 IEEE/MTT-S International Microwave Symposium Digest, Montreal, QC, Canada, 17–22 June 2012; pp. 1–3.
8. Peng, Y.; Liu, H.; Kong, S.; Yu, Y.; Zhao, C.; Wu, Y.; Kang, K. A Low Noise VCO with Common-Tail Inductor in 180 nm CMOS Technology. In Proceedings of the 2019 IEEE Asia-Pacific Microwave Conference (APMC), Singapore, 10–13 December 2019; pp. 1658–1660. [CrossRef]
9. Hong, J.-P.; Yun, S.-J.; Oh, N.-J.; Lee, S.-G. A 2.2-mW Backgate Coupled LC Quadrature VCO With Current Reused Structure. *IEEE Microw. Wirel. Compon. Lett.* **2007**, *17*, 298–300. [CrossRef]
10. Cheng, K.-W.; Allstot, D.J. A gate-modulated CMOS LC quadrature VCO. In Proceedings of the 2009 IEEE Radio Frequency Integrated Circuits Symposium, Boston, MA, USA, 7–9 June 2009; pp. 267–270. [CrossRef]
11. Marzuki, A.; Lee, C.H.; Noh, N.M.; Mohamed, M.F.P. Design of 0.13-μm CMOS Voltage-Controlled Oscillator (VCO) for 2.45 GHz IoT Application. In Proceedings of the 2022 3rd International Conference for Emerging Technology (INCET), Belgaum, India, 27–29 May 2022; pp. 31–34. [CrossRef]
12. Stornelli, V.; Pantoli, L.; Leuzzi, G. Active resonator for low-phase- noise tunable oscillators. *Microw. Opt.* **2006**, *48*, 2611–2615. [CrossRef]
13. Moezzi, M.; Bakhtiar, M.S. Design of LC Resonator for Low Phase Noise Oscillators. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2016**, *63*, 169–180. [CrossRef]
14. Sheikhahmadi, S.; Moezzi, M.; Ghafoorifard, H. A Low Phase Noise Class-C Oscillator with Improved Resonator and Robust Start-Up. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *68*, 92–96. [CrossRef]
15. Soltanian, B.; Kinget, P.R. Tail current-shaping to improve phase noise in LC voltage-controlled oscillators. *IEEE J. Solid-State Circuits* **2006**, *41*, 1792–1802. [CrossRef]
16. Kebria, S.; Ghonoodi, H. Increasing power efficiency in the design of a low power and low phase noise CMOS LC oscillator. *Int. J. Circuit Theory Appl.* **2020**, *49*, 18–30. [CrossRef]
17. Yun, S.J.; Shin, S.B.; Choi, H.C.; Lee, S.G. A 1mW current-reuse CMOS differential LC-VCO with low phase noise. In Proceedings of the 2005 IEEE International Digest of Technical Papers, Solid-State Circuits Conference, San Francisco, CA, USA, 10 February 2005; Volume 48, pp. 450–451. [CrossRef]
18. Azadmousavi, T.; Aghdam, E. A Low Power Current-Reuse LC-VCO with an Adaptive Body-Biasing Technique. *AEU-Int. J. Electron. Commun.* **2018**, *89*, 56–61. [CrossRef]
19. Park, D.; Cho, S. An Adaptive Body-Biased VCO with Voltage-Boosted Switched Tuning in 0.5-V Supply. In Proceedings of the 2006 Proceedings of the 32nd European Solid-State Circuits Conference, Montreaux, Switzerland, 19–21 September 2006; pp. 444–447. [CrossRef]

20. Wei, M.-D.; Negra, R.; Chang, S.-F.; Chen, C.-S. Wideband complementary CMOS VCO with capacitive-source-degeneration technique. In Proceedings of the IEEE EUROCON 2017—17th International Conference on Smart Technologies, Ohrid, Macedonia, 6–8 July 2017; pp. 287–291. [CrossRef]
21. Ataei, F.; Yavari, M. A 2.2GHz high-swing class-C VCO with wide tuning range. In Proceedings of the 2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS), Seoul, Republic of Korea, 7–10 August 2011; pp. 1–4. [CrossRef]
22. Afacan, E.; Dundar, G. A comprehensive analysis on differential cross-coupled CMOS LC oscillators via multi-objective optimization. *Integration* **2019**, *67*, 162–169. [CrossRef]
23. Jafari, B.; Sheikhaei, S. Phase noise reduction in a CMOS LC cross coupled oscillator using a novel tail current noise second harmonic filtering technique. *Microelectron. J.* **2017**, *65*, 21–30. [CrossRef]
24. Gui, X.; Chen, Z.; Green, M. Analysis of Nonlinearities in Injection-Locked Frequency Dividers. *IEEE Trans. Microw. Theory Tech.* **2015**, *63*, 945–953. [CrossRef]
25. Lei, X.; Wang, Z.; Wang, K.; Li, W. A novel wideband low phase noise 2: 1 frequency divider. *J. Semicond.* **2010**, *31*, 065005. [CrossRef]
26. Amin, N.M.; Wang, Z.; Li, Z.; Li, Q.; Liu, Y. A low power, low noise figure quadrature demodulator for a 60 GHz receiver in 65-nm CMOS technology. *J. Semicond.* **2015**, *36*, 045005. [CrossRef]
27. Zhu, M.; Ding, T.; Liao, X.; Ye, S.; Jiang, D.; Zhao, D. A Low-Noise VCO and a Low-Power Frequency Divider in 40-nm CMOS. In Proceedings of the 2020 IEEE MTT-S International Wireless Symposium (IWS), Shanghai, China, 20–23 September 2020. [CrossRef]
28. Sun, K.; Wang, J.; Wang, X.; Gu, J.; Li, L.; Fan, X. A Low Phase Noise 11.8–15.3 GHz CMOS LC-VCO with High-Q Inductor. In Proceedings of the 2021 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), Hualien, Taiwan, 25–27 August 2021. [CrossRef]
29. Wan, C.; Xu, T.; Yi, X.; Xue, Q. A VCO with Extra Cross-Coupling Path. *IEEE Microw. Wirel. Compon. Lett.* **2021**, *31*, 1130–1133. [CrossRef]
30. Pakasiri, C.; You, J.H.; Wang, S. A low-phase-noise and low-power CMOS colpitts VCO using Gm boosting and capacitance switching techniques. *Microw. Opt. Technol. Lett.* **2021**, *63*, 46–50. [CrossRef]
31. Singh, U.; Green, M. Dynamics of high-frequency CMOS dividers. In Proceedings of the 2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353), Phoenix-Scottsdale, AZ, USA, 26–29 May 2002; Volume 5. [CrossRef]
32. Sachan, D.; Kumar, H.; Goswami, M.; Misra, P.K. A 2.4 GHz Low Power Low Phase-Noise Enhanced FOM VCO for RF Applications Using 180 nm CMOS Technology. *Wirel. Pers. Commun.* **2018**, *101*, 391–403. [CrossRef]

Journal of
Low Power Electronics and Applications

MDPI

Review

A Survey of Short-Range Wireless Communication for Ultra-Low-Power Embedded Systems

Billy Baker [1,*], John Woods [1], Martin J. Reed [1] and Martin Afford [2]

[1] School of Computer Science and Electronic Engineering, University of Essex, Colchester CO4 3SQ, UK; woodjt@essex.ac.uk (J.W.); mjreed@essex.ac.uk (M.J.R.)
[2] Emergency Lighting Products, Billingshurst RH14 9EZ, UK; mafford@jordan-elp.com
* Correspondence: bb18655@essex.ac.uk

Abstract: Wireless short-range communication has become widespread in the modern era, partly due to the advancement of the Internet of Things (IoT) and smart technology. This technology is now utilized in various sectors, including lighting, medical, and industrial applications. This article aims to examine the historical, present, and forthcoming advancements in wireless short-range communication. Additionally, the review will analyze the modifications made to communication protocols, such as Bluetooth, RFID and NFC, in order to better accommodate modern applications. Batteryless technology, particularly batteryless NFC, is an emerging development in short-range wireless communication that combines power and data transmission into a single carrier. This modification will significantly influence the trajectory of short-range communication and its applications. The foundation of most low-power, short-range communication applications relies on an ultra-low-power microcontroller. Therefore, this study will encompass an analysis of ultra-low-power microcontrollers and an investigation into the potential limitations they might encounter in the future. In addition to offering a thorough examination of current Wireless short-range communication, this article will also attempt to forecast future patterns and identify possible obstacles that future research may address.

Keywords: NFC (near field communication); RFID; ultra-low-power microcontroller; batteryless; Bluetooth; Wi-Fi; short-range communication; wireless communication

1. Introduction

Short-range wireless technology is a vital part of modern life, with its reach continuing to grow [1]. It is used in most sectors, from wireless payments in shops and door access in schools [2] to TV remotes at home. Its continued growth has been powered by the widespread use of smartphones, which are ubiquitous in the modern era, reaching above 80% ownership in Germany, the UK and the USA [3] and 4.6 billion smartphone users worldwide in 2023 [4], bringing short-range wireless technology to the forefront of applications.

This review paper will cover a brief history of short-range wireless technology, an in-depth review of modern low-power applications using short-range wireless technology, as well as predictions of the future of short-range wireless technology and the research that is needed to improve or adjust short-range wireless technology for future applications. Short-range wireless communication is an extensive term that can be split into two parts: *wireless* can be defined as a gap between the transmitter and receiver that is not connected by wires, while *short range* changes depending on the use case and protocol—in this article, short range will be any protocol with a typical range below 100 meters; communication means data are at least transmitted from one system to another system. This defines the minimum requirements for a protocol to consist of short-range wireless communication in this article.

Understanding whether a short-range wireless system is passive or active is crucial in grasping its use cases and applications. Active refers to a state where both sides of the

overall system are simultaneously powered, whereas passive indicates a condition where only one side is powered i.e., the opposite side receives power through the transmission. An example of an active system is a TV remote. The TV remote operates using a battery, while the TV itself is powered by the mains supply, ensuring that both the transmitter and receiver are supplied with power. An instance of a passive system would be wireless payments, such as credit cards. In this instance, the credit card receives power via inductive coupling from the RFID reader, indicating that it is a passive system, as one side is not powered by an internal power supply.

Table 1 displayed above shows the most prevalent short-range wireless technologies, with the range indicating the highest rated distance of their typical application. A non-line of sight protocol refers to a situation where the signal has the ability to pass through the outer covering of an electromagnetically permeable case, e.g., plastic. This is essential for embedded systems where direct visibility between the transmitter and receiver is usually unattainable. A Broadcast technology allows the transmitter to natively communicate with multiple devices at the same time. Each short-range technology serves different purposes but can generally be categorized into two primary applications, identification and data transfer, with specific technologies capable of performing both functions. Identification methods include UWB, barcode, UHF RFID, VHF RFID, and HF RFID. Data transfer can be achieved through various means, including infra-red communication, Wi-Fi, Bluetooth, and NFC.

Table 1. Table comparing short-range technology.

Name	Passive/Active	Range in Meters (m)	Non-Line of Sight	Broadcast	Identification/Data Transfer
Optical communications [5]	Active	7 m	NO	NO	Data transfer
VHF and HF RFID [6]	Passive	0.1 m	YES	YES	Identification
UHF RFID [7]	Passive/Active	1 m/100 m	YES	YES	Identification
NFC [8]	Passive/Active	0.1 m	YES	NO	Data transfer
Barcode [9]	Passive	0.1 m	NO	NO	Identification
Wi-Fi [10]	Active	$\geq$10 m	YES	YES	Data transfer
Bluetooth [11]	Active	5 m	YES	NO	Data transfer
UWB [12]	Active	15 m	YES	YES	Data transfer
MST * [13]	Passive	0.1 m	YES	NO	Identification

* Magnetic Secure Transmission.

Various constraints exist for each of the short-range technologies, encompassing factors such as costs, availability, and power consumption. The method of communication varies depending on the specific application or circumstance. Nevertheless, there are instances where certain short-range technologies are becoming obsolete and surpassed in particular functions due to overlaps, such as infra-red communication being substituted by Bluetooth and Wi-Fi and Magnetic Secure Transmission being replaced by NFC. However, certain technologies persist in usage despite the availability of alternative options that excel in specific domains, such as substituting barcodes with RFID tags. The implementation of this latter technology is generally limited to industrial applications rather than retail applications, primarily due to its higher cost.

Short-range wireless technologies such as Wi-Fi (IEEE 802.11 Wi-Fi standards) and NFC are constantly evolving, with new revisions being released on a regular basis. For instance [14], Wi-Fi 6 (802.11ax) was released in 2019, and RFID ISO/IEC was revised in 2020. The reason behind these constant revisions is the evolution of parallel technology and its applications. For instance, NFC technology is now a standard feature in most modern smartphones. However, it was introduced in 2004 and was developed in anticipation of

the growing popularity of mobile phones [15]. Similarly, low-power embedded systems currently use Bluetooth mesh and dynamic NFC technology. However, they may evolve to adapt to ultra-low-power or batteryless applications in the future. It is evident that NFC, UHF, HF, and VHF RFID are interlinked. NFC, also known as Near Field Communication, can be regarded as a derivative of RFID technology. This communication protocol operates at a frequency of 13.56 MHz and shares protocols with HF RFID (ISO14443 [16] and ISO15963 [17]). However, NFC has distinct features and use cases compared to RFID. One notable difference is that some NFC devices can switch between tag and reader modes, enabling two-way data transfer. Additionally, NFC is limited to Peer-to-Peer communication, whereas RFID may transmit in broadcast mode. There are multiple different frequencies used for RFID technology: 125 KHz (VHF), 13.56 MHz (HF), 433 MHz (Active UHF), and 865–915 MHz (Passive UHF). Each frequency serves a specific purpose. The 125 kHz (VHF) and 13.56 MHz (HF) frequencies operate through inductive coupling. The 433 MHz (Active UHF) and 2.45 GHz (Active Microwave) frequencies are used for active tags, which means they require a battery but have an enhanced transmission range. On the other hand, the 865–915 MHz (Passive UHF) frequency utilizes backscatter to transmit data.

While identification is the basis for many protocols and applications, data transfer can also achieve identification while also having unique communication applications. Data transfer is typically dynamic, while identification is static. Dynamic means that both sides of the system are active, and so for data transfer to occur, both sides must communicate with each other. While communication is the normal focus of short-range wireless technology, there is another area, short-range energy harvesting technology, which transmits power between devices instead of data. An example is wireless power transfer [16], which can be included in wearable devices or electric vehicles. Wireless power transfer typically uses inductive coupling to transmit power between devices.

Another crucial area is the network type of the protocol [17]. A Personal Area Network (PAN) is used for connecting devices within a small area, typically within a range of less than 10 meters. A local area network (LAN), on the other hand, is used to connect devices within a wider location such as a building, office or home. A LAN is normally less than 100 meters. Lastly, a wide area network WAN is used to connect devices over a larger area, including a metropolitan area and international connections. PAN examples include the majority of short-range wireless protocols such as Bluetooth and infra-red connections. However, Wi-Fi is an example of a LAN network. WAN technologies are not typically used in short-range networks.

The rest of this paper is organized as follows: Section 2 will review a brief history of short-range technology and give a timeline of major developments. Section 3 will cover four of the most used short-range protocols: Bluetooth, Wi-Fi, UWB, and RFID. Section 4 will go into detail about the developing technology of batteryless communication, which, as introduced before, combines both communication and power transmission. Section 5 covers an overview of the power consumption of short-range wireless communication applications. As will be discussed in Section 5, a critical factor of the majority of low-power embedded applications is the microprocessor, so Section 6 will review current ultra-low-power microcontrollers and their future limits, as ultra-low-power microcontrollers are the key limiting factor to making ultra-low-power applications feasible. Section 7 discusses the future of short-range wireless protocols and applications before concluding in Section 8.

2. Brief History of the Evolution of Wireless Short-Range Technology

Short-range wireless communication did started gaining traction after 1945. Before 1945, there were some short-range wireless technologies; however, their use cases were minimal, and wired communication was used for most purposes. That changed in a unique case of international espionage: the “Great Seal Bug” [18] in 1945 was one of the first passive short-range communication devices to be used in a real-world application. The device was powered externally by a transmitter and covertly transmitted audio. “The Great Seal Bug” [18] is the precursor to modern RFID. The espionage device shows the possibility of

transferring data passively, and the possibilities of the technology have become apparent in the modern era with the invention of standard RFID.

Before 1980, the widespread use of short-range wireless technology was limited. In the 1960s and 1970s, research into short-range communication was ongoing and with real-world technology bringing more commercial products such as TVs into households, wireless communication between two devices became a necessity. The first TV remote invented in the 1940–1950s used light to send signals; however, in the 1960s, ultrasonic TV remotes were introduced. While infra-red TV remotes were developed in 1970, they were not used in commercial products until the 1980s. The introduction and innovation of new technology were due to the increase in real-world applications in the case discussed due to the proliferation of the TV; however, this revolution also happened in many sectors and products.

The decades between 1980 and 2000 saw the rapid advancement of RFID. Both passive and active RFID became commercially available, with one of the active main uses being animal tracking with the introduction of ISO 11784 in 1994, while passive RFID became a mainstay in libraries and shops. This has become possible because of low-voltage, low-power CMOS logic circuits. The technology of low-voltage, low-power CMOS logic circuits made passive RFID possible, causing a surge in use. In 1985, an RFID tag circuit would cover 1/4 of a credit card [6], while by 1999, an RFID circuit could be built into a single IC, significantly reducing the size. The massive reduction in cost and size between 1980 and 2000 has led to the modern adoption of RFID. What can be gathered from the development of RFID is that hardware improvements influence the applications of the protocol, so while there is no direct change in the protocol, ongoing research and development will cause changes in the applications and use cases.

Bluetooth first standard was released in 1999 [19]; however, since then, there has been substantial modification to the Bluetooth protocol, which was made for computer peripherals. The modifications have led to a standard that works specifically with battery and IoT devices; this can be seen in Bluetooth version 4, which lowered energy consumption (Bluetooth low energy (BLE)), making the protocol more efficient for IoT applications.

In [20], published in 2007, it states, "RFID finds relatively limited applications these days and must overcome many technical hurdles for wide acceptance. However, none of these hurdles seems to pose a fundamental barrier, and it is evident RFID will soon be pervasive in our daily life". While UHF RFID has not replaced bar-codes in low-cost environments, it has increased use in smart factory concepts [21]; it has also been looked at as a batteryless solution with ideas such as WISP and UHF RFID sensors. HF RFID (ISO14443 and ISO15963) has been used as a standard for NFC.

The increase in low-power battery devices in the mid/late 2000s influenced the creation of the NFC forum and publication of ISO 18000-3 [22] in 2004; the development of BLE in 2010; and the publishing of Zigbee (802.15.4) in 2003 [23]. The adoption of new or adapted protocols started around 2005, with the main use case being low-power, battery-powered embedded systems. The shift to battery-powered, wireless connected devices has enabled greater convenience, mobility, and connectivity in various aspects of the modern era, from smartphones and wearables to smart homes and the Internet of Things (IoT) [24].

If the timeline is to be defined, the development of data transfer short-range protocols spans two different eras: the current battery-powered era, and the era before battery-powered devices became dominant, which was the mains-powered era. The battery era heavily influenced short-range communication protocols which were modified and created to focus on low-power battery-powered systems. This came with different specifications to the prior era of short-range communication, which was made for either mains-powered to mains-powered communication or mains-to-battery systems. The main difference between the two eras is that low-power communication was a necessity in battery-powered devices, which has caused a shift in short-range wireless communication protocols. This shift has caused the development and modification of protocols to fit the low-power application, protocols such as Bluetooth low power (BLE) and Zigbee.

3. Overview of Modern Day Short-Range Wireless Communication Protocol

3.1. Comparing Modern-Era Short-Range Wireless Protocols

The volume of research related to each communication protocol is hard to measure; however, Table 2 shows the number of journal entries based on the keyword between the years 2018 and 2024. These data show that the most researched protocol is RFID, followed by Bluetooth and Wi-Fi; however, this only gives a brief overview of the influence of certain protocols in the research. Figure 1 displays the grouping of different frequency bands; a protocol's frequency is a critical factor. The most popular band is the 2.45 GHz band with Bluetooth, Wi-Fi, and Zigbee; it contains two of the dominant protocols as seen in Table 2. Ultra-wideband differs from the others in both the frequency range and its application, which is mostly for localization rather than data transmission.

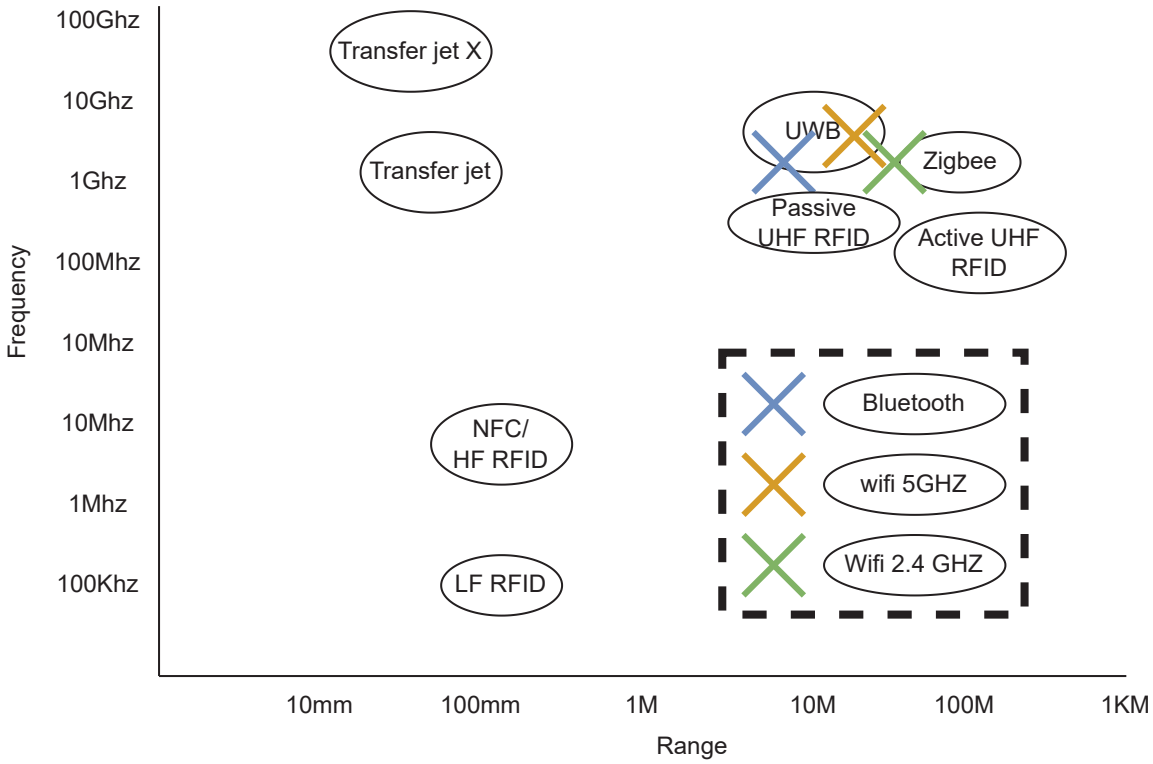


Figure 1. Graph of short-range protocols.

Table 2. Table of IEEE journal entries for keyword 2018–2024.

Keyword	Search Results
RFID	2627
BLUETOOTH	1723
Wi-Fi	1328
UWB	1152
QR	794
UHF RFID	402
NFC	130
BARCODE	98

3.2. RFID

RFID Types

RFID is split into a range of different frequencies; however, there are two main components to every RFID system: readers and tags. All RFID readers transmit data that is modulated by an RFID tag. There are two main methods of communication through RFID depending on the frequency used as seen in Table 3 *near field inductive coupling* or

backscatter coupling. Near field coupling is used by LF and HF RFID due to the longer wavelength [25].

Table 3. Table comparing RFID technology.

Name	Low-Frequency RFID	High-Frequency RFID	Active UHF RFID	Passive UHF RFID	Microwave RFID
Frequency	125/134 KHz	13.56 MHz	433 MHz	860–928 Mhz	2.45 GHz/5.8 GHz
Typical Type	Passive	Passive/Active	Active	Passive	Passive/Active
Read range	0.3 m	1 m	100 m	6 m	10 m
Dipole Antenna size	1141.2 m	10.52 m	329.45 mm	155.9 mm	58.22 mm
Communication method	Near field inductive coupling	Near field inductive coupling	Transmitter Backscatter coupling	Backscatter coupling	Backscatter coupling

A system is said to be in near field at a distance of $C/2\pi f$ where C is the speed of electromagnetic radiation and f is frequency. Thus, using the relevant frequencies, we can define this for the relevant bands as:

$$\text{LF RFID:} \quad 3 \times 10^8 / (2\pi \times 125 \times 10^3) = 382 \text{ m}$$

$$\text{HF RFID:} \quad 3 \times 10^8 / (2\pi \times 13.56 \times 10^6) = 3.52 \text{ m}$$

$$\text{UHF RFID:} \quad 3 \times 10^8 / (2\pi \times 860 \times 10^6) = 0.055 \text{ m}$$

As can be seen, the near field region will only work with LF and HF RFID tags as the near field region drops below 10 cm at UHF, so UHF and microwave RFID use Far Field coupling. At these higher frequencies, a technique called backscatter [20] is used to reflect the electromagnetic wave.

RFID was developed for identification and detection. Detection that an RFID tag is in the range of the RFID reader is a main feature of RFID. This is the type of system used in many retail outlets for device detection. While the retail outlet scenario is interesting, most do not have a smart system, so it only detects when a tag is in the range of the sensor and not the specific tag. This is where the libraries use case [26] is unique; they use both parts of RFID identification and detection in one system. This system means a book can be tracked around the library in the same way RFID is used in logistics and can be sorted using its ID and then placed either by hand or by conveyor to the correct location. It was also used to know when a nook had left the library. This can be performed by an allowlist to only let certain IDs through the RFID reader.

Some RFID detection systems are used to track people. For example, an RFID tag is applied to clothing such as boots [22]. This smart system can detect how often the RFID tag is moved through the reader. Alternative methods use wristbands, which can be seen at major attractions; this uses a handheld reader to scan the RFID tag.

RFID has many applications, with identification being the most prominent use case. It is widely used in industries such as retail, logistics, healthcare, and asset tracking. While RFID is used in regular identification systems, such as logistics and asset tracking, there is another use case where RFID is used as a sensor. This significantly changes the use cases of RFID and has the potential to use RFID as the communication protocol to obtain a low-power passive sensor, which, in some research, is a batteryless system. Unlike the typical RFID use for identification and detection, where RFID tags are detected by RFID readers, RFID as a communication protocol for low-power passive sensors involves using RFID technology to transmit data from the sensor to a reader. This means that the RFID tag itself acts as a sensor, collecting and transmitting data such as temperature, humidity, or pressure [27]. This opens up new possibilities for applications where battery-powered or wired sensors are not feasible or practical. However, there are many different methods

for RFID sensors. The three main categories of sensors are battery-assisted RFID sensors, hybrid RFID sensors, and batteryless RFID sensors. There are two main methods for RFID sensors: chipless and chip-based.

Chip vs. chipless systems: As stated, these are the two main design methods. One is centered around using a solution-on-chip to perform communication. While chipless systems [28] use many different types of communication techniques, some examples are On–Off Keying (OOK), Pulse Position Modulation, Phase Modulation and Backscattered-Based Tags. On–Off Keying tags transmit using 1 or 0, so one way to perform this technique is to use a capacitor [29] to detect when the transmission should be reflected back to the reader. This is a simple way to obtain a binary sensor. Pulse Position Modulation uses the same binary signals with 1 and 0; however, it changes the signal based on a timing window if, with a 0 and 1 reflection timing transmitting a 0 or 1 [30], Phase Modulation uses a number of [31] delay lines to effect the phase of the signal with the number of delay lines being proportional to the number of bits. Backscattered-Based Tags [32], instead of using the time domain, use the frequency domain and so the tag can change its resonance frequency and so can be different from other tags with the same use case as barcodes, a cheap solution to identify products.

Battery-assisted RFID sensors, as the name implies, use a battery and, therefore, an active tag; however, for RFID sensors, most research uses the passive range for these sensors. This is due to the different use cases for UHF active RFID at 433 MHz, which is most commonly used for long-range identification or tracking. At the same time, RFID sensors do not have a range at the forefront of their application; the battery's main purpose is to collect data and then use passive RFID to transmit data, saving power and conserving lifespan. This idea also has the difference that, in some scenarios, the battery can be charged through RF energy harvesting, meaning a smaller battery or supercapacitor can be used, and the tag can be smaller and be embedded for years and could theoretically have an indefinite lifespan if powered periodically [33].

Batteryless RFID sensors have no battery, which significantly changes the dynamics of the tag, as it is a passive tag with active features. It uses a low-power sensor to gather data and uses backscatter to send the signal. The WISP Wireless Identification and Sensing Platform [34] is one of the design ideas for a batteryless RFID. This specifies the use of an ultra-low-power microcontroller, which makes it flexible enough to be used with many different sensors, and this would lead to many applications, such as temperature sensing. There are many different types of batteryless RFID designs, and [35] Chipless, Antenna Resonance, Multi-Port Architecture, and Digitally Integrated are four different types of batteryless RFID sensor methods.

Hybrid RFID systems can be either batteryless or battery-assisted RFID sensors; however, they are normally associated with battery-assisted RFID. This can be split into a communication or power hybrid system. A communication-hybrid system uses another short-range communication technology to transfer data; Bluetooth [36] can be paired with either RFID or Zigbee [37], RFID can be used for location-based sensing while Zigbee can communicate at extended distances, making a system that can be used for message-based detection when an object reaches a selected location. Energy harvesting and RFID are the main use cases of hybrid RFID. This type of RFID uses extremely low power transmission with an alternate energy source, which can be RF, solar, or piezoelectric energy harvesting.

RFID is a growing sector of research [38], with the increase starting around 2010 with the advent of the Internet of Things (IoT) and the adoption of other short-range communication, such as Bluetooth BLE, making wireless handheld portable systems inexpensive. RFID is also the most common protocol term since 2018 in the keyword search shown in Table 2, which shows that research into RFID development is continuing in the modern era.

3.3. Bluetooth Low Power Applications

Bluetooth has been in development since 1999 when Bluetooth version 1 was introduced; however, a major development occurred in 2010 when Bluetooth 4 was introduced,

bringing Bluetooth low energy (BLE). This created a shift in the Bluetooth protocol and its applications, with Bluetooth inclusion in a growing number of devices. There were 2.7 billion device shipments that included Bluetooth in 2014; in 2023, it was estimated that there would be 5.4 billion [39], with the growth of Bluetooth devices continuing into the future [19]. As mentioned, BLE is a subset of Bluetooth and is specifically made for low-power battery-powered devices and IoT. Its main difference from Bluetooth is its work cycle, while Classic Bluetooth is always paired. BLE can go into sleep mode and has a protocol stack specifically built for low power, which drastically reduces power consumption while also being built to be connected to unlimited devices. Classic Bluetooth only has a limit of eight simultaneous devices.

Due to its work cycle nature, BLE has unique applications in sensor networks and IoT, which include fields such as logistics, retail, and medical. The sleep cycle of the BLE device is a critical factor; ref. [40] shows that a round trip with a connection interval of 375 ms has an estimated lifespan of 2 years, while a connection interval of 4000 ms has a lifespan of 12 years using a CC2540 (SoC) for Bluetooth low-energy applications [40]. The power consumption ranges from 10 mA at 7.5 ms intervals to less than 100 μA at 375 ms. This does not take into account the sensing power and the ultra-low-power microcontroller work cycle, which shows the possibility of BLE low-power sensors and applications [41].

BLE has many applications in the medical field; for example, [42] describes a sensor for blood pressure monitoring using a CC2541F256 SoC. It combines the BLE RF transceiver and an 8051 MCU, with the reader of the sensor being a smartphone with a custom app. This is a typical BLE sensor design with the sensor being powered by a battery. The work by Lin et al. shows a complete platform for BLE in the medical use case [43]; in this IoT solution, the sensor is connected to the cloud as shown in Figure 2. This means data can be collected from a sensor network and accumulated in an online database. These applications can be used to monitor people consistently and without the need for an on-site visit in some circumstances. The issue with this system is that it needs two protocols, BLE and Wi-Fi, to be compatible, and so it has three points of failure: a sensor, a smartphone, and Wi-Fi.

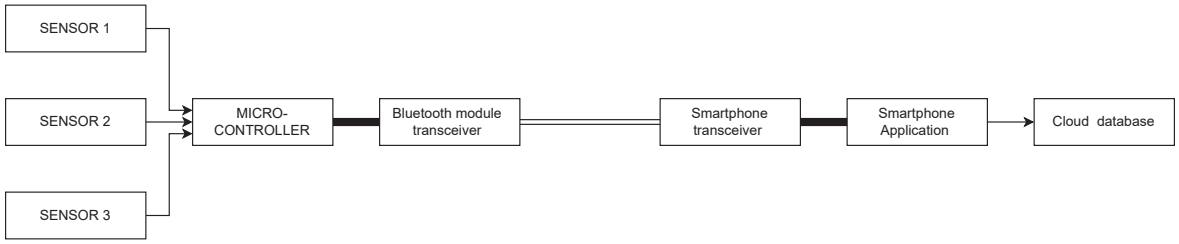


Figure 2. Bluetooth sensor network block diagram.

BLE has a major advantage in hybrid systems, as its work cycling transmission means it has low power, compared to an alternative such as Wi-Fi; extended range, compared to NFC; and compatibility with smartphones, compared to UHF RFID. A hybrid system has distinct advantages [44]. For example, combining BLE and Wi-Fi makes a distinct hybrid system, with BLE low-power sensors data can be collected and then through Wi-Fi they can be stored in the cloud. However, this also means updates can be sent as well to multiple sensors. This hybrid functionality can also be included into a single SoC such as the ESP32 and ESP8266 devices, which have both BLE and Wi-Fi capabilities. An indoor localizing system can be the combination of Wi-Fi and Bluetooth [45], showing that combining the two technologies in parallel is also an alternative, giving more reading and better reliability.

The other hybrid BLE design combines BLE and energy harvesting. This can be performed with different energy-harvesting methods; however, due to the higher power consumption of BLE compared with RFID, the most viable option for energy harvesting is solar [46]. There are a number of commercial BLE hybrid systems available, such as Cyalkit-E02 BLE beacon and Gimbal BLE beacon. These show the viability of BLE and solar hybrid technology with a power consumption of 0.17 mW and 0.28 mW, respectively,

with a range of 0.59 m and 0.31 m. They are low-power, low-range technologies that can be powered by a solar cell measuring 15 mm × 15 mm [47].

3.4. Wi-Fi Low Power Applications

Wi-Fi has many versions and is defined in IEEE 802.11 [48]. The 802.11b (2.4 GHz signaling) is the original 1999 standard, and 802.11g was released in 2003; both are 2.4 GHz Wi-Fi versions. Ultra-low-power Wi-Fi suggests a similar idea to BLE, which changes the work cycle from a 100% work to a sleep/wake-up cycle doing the same; this means performing bursts of work and then sleeping until the next transmission. An example of limiting Wi-Fi to reduce power consumption is limiting packets per second. The transmission of 10 packets per second with a battery of 7500 mAH would last approximately 40 months, while increasing the packets per second to 100 packets per second would make the battery life decrease to 20 months and another increase to 330 packets would only last 10 months, respectively [49].

Wi-Fi [50] is used in IoT to link PAN and LAN networks to a database; this is a critical infrastructure in IoT applications. Some IoT applications that contain Wi-Fi have the prospect to be used in a smart grid, intelligent environment protection, and precision agriculture [51]. An ESP8266 is a module with Wi-Fi standard IEEE 802.11 b/g/n, and with a 1000 mAh battery can last 40–60 h in light sleep [52], depending on the transmission interval. Wi-Fi also has a use case in tracking and identification, while this is not its main use case [53]. Research into Wi-Fi-based localization has been performed and is viable. This brings up the comparison to RFID. While Wi-Fi transmitters are cheaper and have a longer range than RFID transmitters, RFID transmitters have significantly lower power due to backscatter as well as having significantly reduced cost per device.

Another interesting use case of Wi-Fi is in energy harvesting; compared to RFID or BLE, where the energy harvesting is received, Wi-Fi could act as a transmitter for RF energy harvesting, which could power an ultra-low-power sensor in an indoor environment. There has been research on Wi-Fi energy harvesting [54]; however, the issue is the efficiency of energy harvesting with multiple antennas having an efficiency below 20% and a maximum output of 2V at 1mA output. Another area of research is hybrid Wi-Fi systems; this could be with another LAN protocol such as LIFI [55] or a PAN protocol [56] such as Bluetooth.

3.5. Ultra Wide Band (UWB) Short-Range Applications

Ultra-WideBand (UWB) is defined in IEEE 802.15.4, and the primary use case is location-based sensing, specifically, the time of flight sensing. The first standard was released in 2007 (IEEE 802.15.4a) [12]. UWB spans from 3.1 to 10.6 GHz. However, different global regions have varying UWB-allocated frequencies.

One of the main differentiation factors between UWB and other wireless short-range communication methods is the frequency band as indicated in the name. There are 16 predefined channels, with channels 1–16 ranging from a center frequency of 3494.4 MHz and channel 16 having a center frequency of 9484.8 MHz [12]. Compared to other protocols, UWB has less traffic at its designated frequency as seen by Figure 1, and UWB signals employ a significantly wider bandwidth than other technologies such as Wi-Fi and Zigbee. This wider bandwidth means a shorter pulse is needed for communication.

One of the applications for Hybrid UWB entails integrating UWB with alternative short-range wireless communication protocols, including Bluetooth low energy (BLE) [57], Wi-Fi [58], or UHF RFID [59]. By means of this integration, UWB hybrid systems are able to exploit precise positioning and high data transfer rates while benefiting from low power consumption compared to BLE and Wi-Fi due to their shorter duty cycle.

An instance of this can be seen in a hybrid UWB and BLE system, where UWB is employed to facilitate precise indoor positioning and proximity detection; this hybrid technology can also be combined with Wi-Fi for a flexible system [60], and BLE serves as a low-power conduit for transmitting data over greater distances or establishing connections with devices lacking UWB support. Short-range precision tracking accuracy and long-

range data transfer are essential for applications such as asset tracking, indoor navigation, and smart home automation; hybrid UWB can be a feasible solution.

Overall, UWB communication offers high data transfer rates, precise positioning capabilities, resistance to interference, and ultra-low average power consumption, making it well suited for a wide range of applications across industries and applications that require identification and tracing capabilities.

4. In-Depth Discussion of Batteryless Near Field Communication (NFC)

NFC is based on RFID protocols ISO 14443 and ISO 15963 [61] and has five tag types. Type 1–4 use ISO 14443 and have a range of 100 mm, while type 5 NFC tags use ISO 15963 and have a range of 1 m. NFC has three operating modes specified in the standard: Read/Write, Peer-to-Peer, and Card Emulation. Read/Write mode is the typical mode used in NFC where you have a dedicated tag and reader; the tag is a passive tag, while the reader can be mains or battery powered. Peer-to-Peer is performed between two NFC devices, which switch between reader and tag modes. This NFC method is either mains-to-battery or battery-to-battery. Card Emulation is the simplest mode, where an NFC device emulates a smart card. The NFC device is normally battery powered.

Three significant forces are pushing towards a future where batteryless Near Field Communication (NFC) applications become a standard. These forces include improvements in ultra-low-power microcontrollers, the rise of affordable NFC energy harvesting integrated circuits (ICs), and the widespread integration of NFC readers in most smartphones. These dynamics fit together to create a standard of wireless communication that does not rely on conventional power sources, opening up possibilities across various industries, daily life, and new applications.

The reason for the focus on batteryless NFC is the combination of data and energy transfer in a single communication protocol. This differs from the hybrid approach, which uses a combination of two differing protocols. An example of a hybrid system can be seen by combining [62] solar cells with Bluetooth BLE or Wi-Fi energy harvesting and infra-red. Batteryless NFC uses one protocol, which means simplicity over the hybrid approach. As batteryless NFC does not include a type of significant energy storage, such as a battery or supercapacitor, this leads to the system being powered by an external source in the batteryless NFC tag. This is achieved through an NFC reader through near-field coupling.

Another term associated with the batteryless NFC concept is passive–active NFC. Passive–active NFC is a subset of passive NFC communication, where an NFC tag can be powered externally from an NFC reader and does work. The work that is performed can be data transfer or sensor reading. The difference between passive and passive–active is that tasks outside the NFC protocol can be achieved [63], which means external memory checking where the data are transferred or confirmed by a microcontroller or temperature sensing where sensor data are sent over NFC. Batteryless NFC can be included in the passive–active NFC concept; however, the difference between passive and passive–active NFC is that passive–active NFC can have a battery or be connected to the mains but can also switch states while including the batteryless mode. This gives flexibility, as the system is not confined to one mode of NFC but can switch between modes.

A batteryless NFC tag contains three main parts: the transmission system, which contains the antenna and matching circuit; the NFC protocol, which is contained on a dynamic NFC IC; and the work part, which contains sensors and a microcontroller IC. The transmission system is a loop antenna matched to 13.56 Mhz with a corresponding matching circuit if necessary. The size of the antenna can vary significantly depending on the use case, size and range of the device. With the majority of NFC antennas being loop antennas [64], a typical NFC antenna size is 30 mm $\times$ 40 mm; however, the overall size can be reduced significantly [65]. One type of NFC antenna is the PCB loop antenna. This type of antenna can be as small as 2.4 by 2.4 mm by having a dual-layer PCB loop antenna; however, this will affect the range of energy that is achievable. In designing this type of antenna, a design choice is energy harvesting range vs. antenna size.

There are a range of dynamic NFC tags used for batteryless NFC such as the M24LR, ST25DV16K, NT3H211, and RF430FRL152H. This range of ICs has been achieved by the development of batteryless NFC and passive–active NFC; these ICs are a range of NFC type NT3H211, which is a type 2 NFC tag using ISO 14443, while M24LR and ST25DV16K are type 5 NFC tags using ISO 15963. The most unique is the RF430FRL152H, which also uses ISO 15693. However, it is a combination of a dynamic NFC IC tag and a microcontroller in a single IC, whose stated use is as a sensor transponder [66]. These ICs have opened the door to easy access to batteryless NFC; there has been a switch from chipless batteryless design in the 2010s to use commercial dynamic NFC ICs in the 2020s.

However, as mentioned in the discussion of RFID, the factor range of an NFC tag system varies significantly depending on a range of factors. The range of a system is critical in batteryless NFC, as this determines the working distance using smartphones. The range of batteryless NFC is limited to 8–45 mm, with the typical batteryless NFC application having a range of 20 mm. ISO 14443 is limited to a range of around 10 cm; however, type 5 NFC tags, which are designed for industrial applications, can have a stated range of 100 cm. However, this means an industrial NFC reader can be used to power the system to increase the range of the system. A system is shown with increased range using an industrial NFC reader and increased power transfer by using wireless power transfer and a wireless power transfer antenna [67].

As seen in Table 4, there is a range of researched applications for batteryless NFC with a varied combination of both NFC ICs and microcontrollers. The applications range from industrial, agricultural and medical use cases for batteryless NFC. The range of the batteryless applications displayed in Table 4 only uses smartphone NFC readers for range measurements compared to industrial NFC readers, and as such, the range is below 45 mm for all applications. The NFC Bicycle Tyre Pressure Sensor [68] only has a range of 8 mm. This is due to the small antenna size of 14 × 48 mm; however, with an alternative reader, this range could be extended.

Table 4. Table comparing NFC applications.

Application Name	Year	Range	NFC IC	Microcontroller
Batteryless soil moisture measurement system [69]	2018	20 mm	M24LR	ATTINY85
Batteryless NFC Sensor for pH Monitoring [70]	2019	18 mm	M24LR	ATTINY85
Batteryless NFC Bicycle Tire Pressure Sensor [68]	2021	8 mm	NT3H211	ATTINY85
Smart Bandage With Wireless Strain and Temperature Sensors [71]	2020	43 mm	RF430FRL152H	RF430FRL152H
Smartphone-Based NFC Potentiostat for Wireless Electrochemical Sensing [72]	2021	20 mm	SIC4341	N/A
Concertina-Shaped Vibration Energy Harvester-Assisted NFC Sensor [73]	2022	45 mm	ST25DV16K	STM32L031
glucose monitoring via smartphone [74]	2023	N/A	SIC4341	N/A
Total Minerals in Drinking Water via Smartphone [66]	2021	30 mm	M24LR16E	MSP430FR2433
Dosimeter tag for ionizing radiation [75]	2023	N/A	M24LR64E	PIC16LF1703

The range of batteryless NFC applications shows how batteryless NFC is versatile and can be used to solve many tasks. The reason for this is that NFC is a widespread protocol with use cases in payment systems, which has led to the integration of NFC readers in smartphones while also being a wireless protocol used for identification, which competes with QR codes. One of the main applications of batteryless NFC is in the medical field, where its use could be widespread to include sense internal or external sensor measurements. Another example system shows a smartbandage that uses an

RF430FRL152H [71]. It uses a combination of strain and temperature sensors to collect data; however, it performs no data analysis internally and stores the data in ROM for transmission over ISO 15963. This system is a typical sensor system, which is the most common use case for batteryless NFC sensor-based systems, which typically uses a microcontroller to input and convert sensor readings into a dynamic IC memory storage in the case of the RF430FRL152H. This is performed inside a single IC compared to other examples which have a dedicated NFC IC. Another researched use case is glucose monitoring [74]. This was performed using a SIC4341 device, which is a dynamic NFC IC; this system received data from the glucose sensor and transmitted them through NFC. Both systems described above use a smartphone as the NFC reader and display the data in a smartphone app. The advantage of this is that any user with a smartphone with NFC capabilities can use this system.

Batteryless NFC sensors are the primary focus of batteryless NFC research. In [69], an example is given of a soil moisture measurement system that uses an M24LR NFC IC while using an ATTINY85 as the MCU. This system, during work, uses approximately 1 mA of power, which is performed using a SIC4341, a dynamic NFC IC. This system receives data from the glucose sensor and transmits the data through NFC. The supply voltage varies from 2.7 to 3.3 volts, and the system includes three sensors which measure humidity, temperature, and soil water content. This system shows a typical application and the responding power levels [76]. The maximum claimed NFC power is 10 mA at 3.3 V. This comes from the SIC43XX series; however, it uses ISO14443, so the range is limited. M24LR-E-R has a claimed maximum 6 mA at 3 V. The soil moisture measurement system has a range of 20 mm. This is mostly due to its antenna size and antenna design and is limited by the reader's choice of smartphone. This range would increase if an industrial reader were used, which is viable with ISO 15963,

One of the main developments that could use batteryless NFC is smart factories or smart devices to perform batteryless over-the-air (OTA) programming or transmission. This can be performed in a batteryless way in passive–active systems either in the field or in a controlled environment such as a factory. This could be a batteryless wireless in-application programming into an embedded system, possibly without the need to power the system or to a system with no other communication protocol. This could be used to embed sensors without the need for energy storage and be able to communicate [77]. OTA programming also has a range of benefits, as programming can be performed quickly and wirelessly, so there is no need to remove packaging while also having a way to internally read the device data as an advanced label. Where this becomes specific for batteryless NFC is the advantage of confirming that the communication was successful, as well as being able to add security features and conduct testing.

5. Power Consumption of Short-Range Wireless Communication Applications

Short-range wireless communication covers various standards and protocols with varying power consumption based on application. RFID and UWB, which focus on identification and location, respectively, are low-power protocols with low amounts of static data transfer. This is comparable to BLE and batteryless NFC, which involve more dynamic data transfer, while Wi-Fi is focused on data transfer compared to power consumption. The type of system, whether it is batteryless, battery powered, or mains powered, plays a significant role in determining the power requirements. This factor is crucial in selecting the most suitable wireless communication protocol, as each system type has different power consumption needs.

Dedicated ICs vs. system on a chip differ between protocols; BLE has a range of different chipsets. The power consumption of different chipsets varies massively with operation and hardware power consumption; however, an estimation of processing power vs. communication power can be achieved with the Intel A-101 having an average current of 0.089 mA and a 21.338% processing vs. communication ratio, Cypress CY8CKIT-042-BLE having an average current of 0.018 mA and a 23.02% ratio, and the NXP FRDM-

KW41Z having an average current of 0.036 mA and a 28.07 ratio [41]. SOCs with a single microcontroller are naturally more efficient than dedicated ICs due to the need for two simultaneous processors to be active. This can be seen in the batteryless NFC operation in [69]. The M24LR dynamic NFC IC power consumption is 0.4 mA. The ATtiny85 power consumption is 0.3 mA, and the ratio is 47% when the timer is taken into account.

While communication transmission power consumption takes up a significant proportion of the overall power consumption during active operation, there is a limit to reducing the power consumption unless we want to reduce the range or communication duty cycle of the system. Microprocessors are the main power drain during the non-active operation of the system, and reducing the power consumption of the microprocessor either during active or non-active operation can make a batteryless system viable or increase the battery life of battery power systems.

Comparing the power consumption of different short-range wireless communication applications is challenging due to the varying factors between systems and applications, such as duty cycle, the range required, the microprocessor used, and the varying number of sensors used in data-gathering devices. To avoid this problem, the minimum system requirements must be the focus. These limits determine the feasibility and limits of short-range wireless communication, which must be considered.

The transmit power consumption is based on different protocols, Bluetooth 102.6 mW, Wi-fi 722.7 mW, Zigbee 73.5, UWB 749.1 mW [78], and RFID reader 180 mW [79]. However these values only show the peak power required. These power requirements set a limit on pure batteryless-based solutions, as energy storage is required for high-power short duty cycle transmission compared to a battery-based system, where the average power consumption is the important distinction.

Ultra-low-power microcontrollers are a critical part of dynamic short-range wireless communication systems, as they limit the power consumptionin dynamic applications such as BLE, Zigbee, and batteryless NFC.

6. Review of Ultra-Low-Power Microcontrollers

Historically, ultra-low-power microcontrollers were distinguished from standard microcontrollers by their unique characteristics. In 2000, ultra-low-power microcontrollers [80] had unique features compared to standard microcontrollers. One of the main differences was the supply voltage, with some ultra-low-power microcontrollers having a supply voltage of 1.8 V, whereas standard microcontrollers had a supply of 3.3 V. The other factor was the inclusion of multiple low-power modes compared to the standard, which included just a sleep mode. In 2024, ultra-low-power microcontrollers are more difficult to distinguish from their standard series counterparts. This is evident in the STM32 series of microcontrollers, where the STM32L0 series has a supply voltage range of 1.65–3.6 volts, and the STM32H723 high-performance microcontroller has a supply voltage range of 1.62–3.6 volts, in addition to a number of low-power modes and a 32 kHz internal clock. Regular microcontrollers incorporate ultra-low-power microcontroller features. However, the primary distinction between standard and ultra-low-power microcontrollers lies in their respective purposes. An ultra-low-power microcontroller aims to control and reduce power consumption. This is typically accomplished in two distinct ways. In work/run mode, the objective is to complete as much work as possible while consuming the least amount of energy possible. In sleep mode, the sole objective is to consume as little energy as possible.

Many factors affect ULP microcontrollers, but the most critical is power consumption. The goal of ULP microcontrollers is to have the lowest possible power consumption while getting the most work done, compared to regular microcontrollers, where getting work done fast and efficiently is the most important factor. Power consumption is affected by both hardware and software factors; the main hardware factors are supply voltage, transistor size, and the number of cores. The software factors include low power modes, efficiency of work, and length of work.

The divergence between regular and ULP microcontrollers occurred in the early 2000s. ULP microcontrollers have the goal of the lowest power consumption, which enhances battery life, as the battery capacity is not growing as fast as other associated technologies. Decreasing power consumption is one way to increase lifespan without affecting the size of the battery; this is crucial in areas such as spacecraft, medical implants, and IoT devices. ULP microcontrollers have also led the way in energy harvesting and, in the future, batteryless technology. Another divergence occurred in 2000. The transistor size in both CISC and RISC products were significantly closer than in the modern era, with the size of the transistor being 250 nm for a workstation, 350 nm for an embedded system, and 500 nm in the year 2000, while today, typically a CISC core is 7 nm [81], while the RISC typical core size is 65 nm [82].

The supply voltage of both the internal transistors and the minimum supply voltage of a microcontroller are vital for ULP microcontrollers and have a significant impact on low-power performance. The reduction in the supply voltage of transistors dropped by around 40% from 2003 to 2020 as shown in Figure 3. The drop from 1.2 V to 0.7 V means it is possible to reduce the power consumption of ULP microcontrollers; the issue is that the standard for ULP microcontrollers is still 1.8 V and has not shifted since the mid-2000s. Some series of microcontrollers have reduced the supply voltage such as the STM32L, which has a minimum supply voltage of 1.65 V; however, the reduction is minimal, and no mainstream chipset has reduced their supply voltage significantly. The problem is that the supply voltage is only reduced when a new series comes out, and this is normally less than two times the transistor voltage. This can be seen in STM32, which released in 2014. The 2013 supply voltage was $0.86 \times 2 = 1.72$. A mainstream series of 1.4 V might be possible by 2025. The supply voltage will stall due to expected technological barriers. This will cause major issues, as reducing the supply voltage is one of the two ways to reduce power consumption without affecting performance.

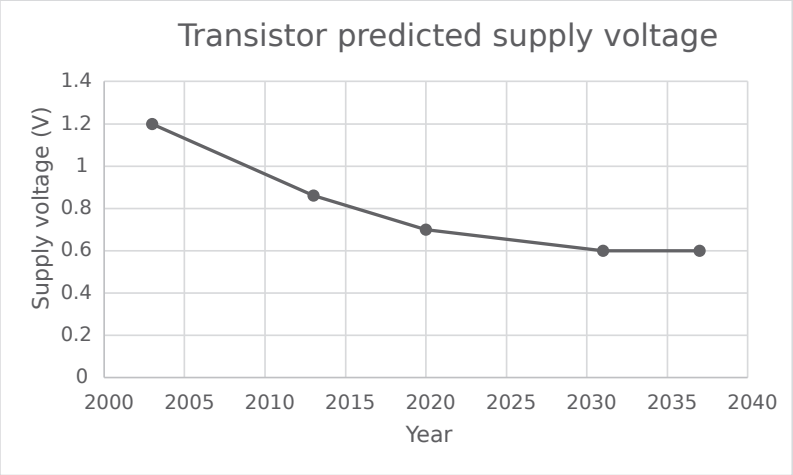


Figure 3. Figure microcontroller predicted supply voltage [81] .

The selection of the microcontroller for low-power short-range communication is crucial; with different protocols having differing requirements, the challenge is selecting a microcontroller for an application, with Table 4 showing that there is a range of microcontroller options for a single application. What is known is that the slowing of power consumption optimization [83] is making generational change smaller and causing the older microcontrollers to still have relevance.

7. Future Discussion

The current state of short-range communication protocols is heavily influenced by the prevalence of battery-powered devices. The shift happened around 2005 when protocols were specifically modified, such as in the case of BLE, or created, such as NFC. The change

occurred due to a combination of factors, including the [84] development and improvement of battery technology, as well as the development of ultra-low-power microcontrollers, hardware improvements, and the addition of software and power consumption optimization. The shift to low-power embedded systems and battery power devices has led to a range of use cases, which has led to the development of BLE, NFC, and low-power Wi-Fi. One of the questions concerning the development of wireless communication protocols is: does the protocol develop first, or does the use case? One real-world example of the modification of an existing protocol is Bluetooth, as the protocol was already developed but was modified to fit low-powered devices, while NFC was built specifically for the use of contactless payments [85]. However, there is continued research into future use cases of current protocols such as Bluetooth localization and passive RFID sensors such as WISP.

What is happening to batteryless technology is that existing protocols such as NFC are being used without modification while standalone platforms such as NFC-WISP [86] are in development. Batteryless technology is used in RFID and NFC; however, without modification, they do not perform any work and are static devices. However, passive–active NFC changes this, making a use case where either a sensor or over-the-air programming is viable without an additional component added to the system. This is comparable to a hybrid communication-energy-having system, which, while having advantages, is less desirable than a single protocol to perform both energy and data transfer.

There are many challenges ahead to continue the evolution of ultra-low-power systems; for example, microcontroller development is coming to a physical limit Figure 4 in the size of transistors and supply voltage. The current trend of improvements to hardware power consumption optimization might lead to the development of more software-based power consumption techniques. The development of batteryless and hybrid systems that rely on external power sources are currently being researched as seeming viable to be included in embedded systems [54]. Wi-Fi energy harvesting is an example where direct inclusion into low-power applications that are currently in use, such as TV remotes, clocks, and smoke alarms, will lead to the inclusion of hybrid technology. The adoption of batteryless systems using RFID and NFC technology would lead to the optimization and maybe integration of batteryless NFC systems into one platform. This could lead to internal sensors, and the application for internal battery sensors includes areas from construction to medical use. The use of tiny internal batteryless sensors could lead to an increase in health monitoring [87], and implants could help with patient monitoring. Another use is in long-life sensors such as inside concrete [67] or insulation, which would be used to monitor temperature.

Figure 4. Figure of microcontroller predicted transistor size [81].

8. Conclusions

The main conclusion from comparing different short-range wireless communications is that protocols can evolve to conform to different application scenarios, for example, the

change from Bluetooth to BLE or NFC to batteryless NFC. Additionally, protocol optimizations such as those seen in Wi-Fi are critical to keeping protocols prevalent. Research is continuing to advance the current protocols to improve operational parameters such as power consumption, range, data rates or to add new, more advanced, features.

Factors influencing IoT and embedded systems contribute to the growing interest in short-range wireless communication. The analysis in this paper encompasses the customary short-range communication protocols and technologies currently used. The current era is focused on battery-powered, low-power communication, and this will be the focus for the majority for many years; however, physical limitations in ultra-low-power microcontrollers and battery technology will seem to lead to an end to hardware power consumption growth. This can be seen by the slowing of microcontroller size and supply voltage reductions [88]. This has led to the development of multi-core microprocessors, and the industry believes in the innovation of core stacking. This, however, conflicts with the ultra-low-power microcontroller goal of low power consumption, as this does not help with lowering power consumption, as transistor size and supply voltage are crucial for lowering power consumption. For a microcontroller, this will lead to a stagnation in hardware power consumption.

Another increasing factor in modern-day IoT and embedded systems is the increasing number of devices, as well as the goal of being able to make smart devices with smaller size and longer life. This has led to an increase in IoT device research; however, some tasks are impractical with current research and technology. The aim is to overcome physical hardware hurdles for smaller devices with energy-harvesting solutions and software solutions.

Short-range wireless communication has many solutions, depending on the application and use case. It connects at least two systems together in a range of different ways; with the protocols in this review, only the most widespread protocols were discussed, but as seen, Bluetooth, Wi-Fi, and optical communication are still being developed and modified with adjustments, and new versions are still in development. While RFID has not had any major changes or updates, it is still being updated, with ISO 15963 having a specification in 2020. There is also new long-range communication, such as ZigBee or Sigfox, which can be used to connect short-range devices to low-power networks. What can be seen is the evident evolution in short-range wireless communication, even though existing protocols seem to have become dominant in some application scenarios.

Batteryless and hybrid energy systems are rapidly evolving and have numerous advantages over traditional systems as highlighted in this review. Although not yet mainstream, the applications and use cases for this technology are immense. One of the most significant advantages of hybrid systems is their lifespan, which can last for a few years in the right conditions. In contrast, a batteryless system could theoretically last for an indefinite period. To incorporate these systems into an IoT or smart system, a low-power communication protocol that can be combined with energy harvesting is essential.

Author Contributions: Conceptualization, literature review, analysis, conclusions and original draft, B.B.; writing, reviewing, editing and supervision, J.W., M.J.R. and M.A. All authors have read and agreed to the published version of the manuscript.

Funding: Knowledge Transfer Partnerships UK (KTP 13449): Innovate UK and Emergency Lighting Products Ltd.

Data Availability Statement: Data is contained within the article or cited items.

Acknowledgments: CSEE Department at University of Essex.

Conflicts of Interest: As author Martin Afford was employed by the company Emergency Lighting Products Ltd. All authors declare no conflicts of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data or in the decision to publish the results.

References

1. Basic, F.; Gaertner, M.; Steger, C. Secure and Trustworthy NFC-based Sensor Readout for Battery Packs in Battery Management Systems. *IEEE J. Radio Freq. Identif.* **2022**, *6*, 637–648. [CrossRef]
2. Xiao, X.; Fu, Y.; Yang, Y.; Nikitina, M.A.; Zhang, X. Battery-free wireless moisture sensor system for fruit monitoring. *Results Eng.* **2022**, *14*, 100420. [CrossRef]
3. Olson, J.A.; Sandra, D.A.; Colucci, É.S.; Al Bikaii, A.; Chmoulevitch, D.; Nahas, J.; Raz, A.; Veissière, S.P. Smartphone addiction is increasing across the world: A meta-analysis of 24 countries. *Comput. Hum. Behav.* **2022**, *129*, 107138. [CrossRef]
4. Shanahan, M.; Bahia, K. *The State of Mobile Internet Connectivity 2023*; GSMA: London, UK, 2023.
5. Warmerdam, K.; Pandharipande, A.; Caicedo, D. Connectivity in IoT indoor lighting systems with visible light communications. In Proceedings of the 2015 IEEE Online Conference on Green Communications, Piscataway, NJ, USA, 10–12 November 2015; pp. 47–52.
6. Landt, J. The history of RFID. *IEEE Potentials* **2005**, *24*, 8–11. [CrossRef]
7. Zhang, J.; Periaswamy, S.C.; Mao, S.; Patton, J. Standards for passive UHF RFID. *GetMobile Mob. Comput. Commun.* **2020**, *23*, 10–15. [CrossRef]
8. Cappelli, I.; Fort, A.; Mugnaini, M.; Panzardi, E.; Pozzebon, A.; Tani, M.; Vignoli, V. Battery-Less HF RFID Sensor Tag for Soil Moisture Measurements. *IEEE Trans. Instrum. Meas.* **2021**, *70*, 1–13. [CrossRef]
9. Sangkharat, T.; La-or, J. Application of Smart Phone for Industrial Barcode Scanner. In Proceedings of the 2021 7th International Conference on Engineering, Applied Sciences and Technology (ICEAST), Pattaya, Thailand, 1–3 April 2021; pp. 9–12.
10. Deng, C.; Fang, X.; Han, X.; Wang, X.; Yan, L.; He, R.; Long, Y.; Guo, Y. IEEE 802.11 be Wi-Fi 7: New challenges and opportunities. *IEEE Commun. Surv. Tutorials* **2020**, *22*, 2136–2166. [CrossRef]
11. Liu, C.; Zhang, Y.; Zhou, H. A comprehensive study of bluetooth low energy. In Proceedings of the Journal of Physics: Conference Series, Zhuhai, China, 24–26 September 2021; IOP Publishing: Bristol, UK, 2021; Volume 2093, p. 012021.
12. Coppens, D.; Shahid, A.; Lemey, S.; Van Herbruggen, B.; Marshall, C.; De Poorter, E. An overview of UWB standards and organizations (IEEE 802.15. 4, FiRa, Apple): Interoperability aspects and future research directions. *IEEE Access* **2022**, *10*, 70219–70241. [CrossRef]
13. Choi, D.; Lee, Y. Eavesdropping of magnetic secure transmission signals and its security implications for a mobile payment protocol. *IEEE Access* **2018**, *6*, 42687–42701. [CrossRef]
14. Mozaffariahrar, E.; Theoleyre, F.; Menth, M. A survey of Wi-Fi 6: Technologies, advances, and challenges. *Future Internet* **2022**, *14*, 293. [CrossRef]
15. Shen, W.; Remédios, D.; Sousa, L.; Barata, M.; Osório, L. NFC technologies in mobile phones and emerging applications. In Proceedings of the Information Technology For Balanced Manufacturing Systems: IFIP TC5, WG 5.5 Seventh International Conference on lnformation Technology for Balanced Automation Systems in Manufacturing and Services, Niagara Falls, ON, Canada, 4–6 September 2006; Springer: Boston, MA, USA, 2006; pp. 425–434.
16. Zhang, Z.; Pang, H.; Georgiadis, A.; Cecati, C. Wireless power transfer—An overview. *IEEE Trans. Ind. Electron.* **2018**, *66*, 1044–1058. [CrossRef]
17. Bahashwan, A.A.; Anbar, M.; Abdullah, N.; Al-Hadhrami, T.; Hanshi, S.M. Review on common IoT communication technologies for both long-range network (LPWAN) and short-range network. In *Advances on Smart and Soft Computing: Proceedings of ICACIn 2020*; Springer: Singapore, 2021; pp. 341–353.
18. Brooker, G.; Gomez, J. Lev Termen's Great Seal bug analyzed. *IEEE Aerosp. Electron. Syst. Mag.* **2013**, *28*, 4–11. [CrossRef]
19. Zeadally, S.; Siddiqui, F.; Baig, Z. 25 years of bluetooth technology. *Future Internet* **2019**, *11*, 194. [CrossRef]
20. Chawla, V.; Ha, D.S. An overview of passive RFID. *IEEE Commun. Mag.* **2007**, *45*, 11–17. [CrossRef]
21. Feng, J.; Li, F.; Xu, C.; Zhong, R.Y. Data-Driven Analysis for RFID-Enabled Smart Factory: A Case Study. *IEEE Trans. Syst. Man Cybern. Syst.* **2020**, *50*, 81–88. [CrossRef]
22. Michel, A.; Lisi, F.; Manara, G.; Nepa, P. Design Considerations on a UHF RFID Smart Gate Antenna for the Detection of Tags Embedded into Boots. In Proceedings of the 2022 IEEE 12th International Conference on RFID Technology and Applications (RFID-TA), Cagliari, Italy, 12–14 September 2022; pp. 98–100.
23. *IEEE Std 802.15.4-2003*; IEEE Standard for Telecommunications and Information Exchange Between Systems—LAN/MAN Specific Requirements—Part 15: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low Rate Wireless Personal Area Networks (WPAN). IEEE: Philadelphia, PA, USA, 2003; pp. 1–680.
24. Cano, J.C.; Berrios, V.; Garcia, B.; Toh, C.K. Evolution of IoT: An industry perspective. *IEEE Internet Things Mag.* **2018**, *1*, 12–17. [CrossRef]
25. Indra, W.A.; Khang, A.W.Y.; Tung, Y.; Alsayaydeh, J. Radio frequency identification (RFID) item finder using radio frequency energy harvesting. *ARPN J. Eng. Appl. Sci.* **2019**, *14*, 3554–3560.
26. Zhang, J.F.; Wen, C.J. The university library management system based on radio frequency identification. In Proceedings of the 2017 10th International Congress on Image and Signal Processing, BioMedical Engineering and Informatics (CISP-BMEI), Shanghai, China, 14–16 October 2017; pp. 1–6.
27. Tan, J.; Sathyamurthy, M.; Rolapp, A.; Gamez, J.; Hennig, E.; Schäfer, E.; Sommer, R. A Fully Passive RFID Temperature Sensor SoC With an Accuracy of ±0.4 °C (3σ) From 0 °C to 125 °C. *IEEE J. Radio Freq. Identif.* **2019**, *3*, 35–45. [CrossRef]

28. Herrojo, C.; Paredes, F.; Mata-Contreras, J.; Martín, F. Chipless-RFID: A Review and Recent Developments. *Sensors* **2019**, *19*, 3385. [CrossRef]
29. Shao, B.; Chen, Q.; Amin, Y.; David, S.M.; Liu, R.; Zheng, L.R. An ultra-low-cost RFID tag with 1.67 Gbps data rate by ink-jet printing on paper substrate. In Proceedings of the 2010 IEEE Asian Solid-State Circuits Conference, Beijing, China, 8–10 November 2010; pp. 1–4.
30. Forouzandeh, M.; Karmakar, N.C. Chipless RFID tags and sensors: A review on time-domain techniques. *Wirel. Power Transf.* **2015**, *2*, 62–77. [CrossRef]
31. Schüßler, M.; Mandel, C.; Maasch, M.; Giere, A.; Jakoby, R. Phase modulation scheme for chipless RFID-and wireless sensor tags. In Proceedings of the 2009 Asia Pacific Microwave Conference, Singapore, 7–10 December 2009; pp. 229–232.
32. Jalaly, I.; Robertson, I. Capacitively-tuned split microstrip resonators for RFID barcodes. In Proceedings of the 2005 European Microwave Conference, Paris, France, 4–6 October 2005; Volume 2.
33. Walton, M.; Woods, J. Intelligent control of micro power–Immortal machine. *Nano Energy* **2020**, *72*, 104699. [CrossRef]
34. Sample, A.P.; Yeager, D.J.; Powledge, P.S.; Smith, J.R. Design of a passively-powered, programmable sensing platform for UHF RFID systems. In Proceedings of the 2007 IEEE international Conference on RFID, Grapevine, TX, USA, 26–28 March 2007; pp. 149–156.
35. Khalid, N.; Mirzavand, R.; Iyer, A.K. A survey on battery-less RFID-based wireless sensors. *Micromachines* **2021**, *12*, 819. [CrossRef]
36. Shaikh, A.; Merilampi, S.; Leino, M.; Jabari, S.; Buruk, O.; Hamari, J.; Virkki, J. Textile-Based Game Controller Platform Through Combination of Bluetooth and Passive UHF RFID. In Proceedings of the 2023 8th International Conference on Smart and Sustainable Technologies (SpliTech), Split, Croatia, 20–23 June 2023; pp. 1–5.
37. Yang, H.; Yang, L.; Yang, S.H. Hybrid Zigbee RFID sensor network for humanitarian logistics centre management. *J. Netw. Comput. Appl.* **2011**, *34*, 938–948. [CrossRef]
38. Casella, G.; Bigliardi, B.; Bottani, E. The evolution of RFID technology in the logistics field: A review. *Procedia Comput. Sci.* **2022**, *200*, 1582–1592. [CrossRef]
39. ABI, R. 2023 Market Update. 2023. Available online: https://www.bluetooth.com/2023-market-update/ (accessed on 8 May 2024).
40. Gomez, C.; Oller, J.; Paradells, J. Overview and evaluation of bluetooth low energy: An emerging low-power wireless technology. *Sensors* **2012**, *12*, 11734–11753. [CrossRef]
41. Garcia-Espinosa, E.; Longoria-Gandara, O.; Pegueros-Lepe, I.; Veloz-Guerrero, A. Power consumption analysis of Bluetooth low energy commercial products and their implications for IoT applications. *Electronics* **2018**, *7*, 386. [CrossRef]
42. Lin, Z.M.; Chang, C.H.; Chou, N.K.; Lin, Y.H. Bluetooth Low Energy (BLE) based blood pressure monitoring system. In Proceedings of the 2014 International Conference on Intelligent Green Building and Smart Grid (IGBSG), Taipei, Taiwan, 23–25 April 2014; pp. 1–4.
43. Sayeed, T.M.S.; Rayhan, M.T.; Chowdhury, S. Bluetooth Low Energy (BLE) based portable medical sensor kit platform with cloud connectivity. In Proceedings of the 2018 International Conference on Computer, Communication, Chemical, Material and Electronic Engineering (IC4ME2), Rajshahi, Bangladesh, 8–9 February 2018; pp. 1–4.
44. Khanchuea, K.; Siripokarpirom, R. A multi-protocol IoT gateway and WiFi/BLE sensor nodes for smart home and building automation: Design and implementation. In Proceedings of the 2019 10th International Conference of Information and Communication Technology for Embedded Systems (IC-ICTES), Chonburi, Thailand, 7–9 May 2017; IEEE: Philadelphia, PA, USA, 2019; pp. 1–6.
45. Antevski, K.; Redondi, A.E.; Pitic, R. A hybrid BLE and Wi-Fi localization system for the creation of study groups in smart libraries. In Proceedings of the 2016 9th IFIP wireless and mobile networking conference (WMNC), Colmar, France, 11–13 July 2016; IEEE: Philadelphia, PA, USA, 2016; pp. 41–48.
46. Kano, K.; Yoshida, T.; Hayashida, N.; Asai, Y.; Matsuyama, H.; Katayama, S.; Urano, K.; Yonezawa, T.; Kawaguchi, N. Smartphone Localization with Solar-Powered BLE Beacons in Warehouse. In Proceedings of the International Conference on Human-Computer Interaction, Virtual Event, 26 June –1 July 2022; Springer: Cham, Switzerland, 2022; pp. 291–310.
47. Spachos, P.; Mackey, A. Energy efficiency and accuracy of solar powered BLE beacons. *Comput. Commun.* **2018**, *119*, 94–100. [CrossRef]
48. *IEEE Std 802.11-2020 (Revision of IEEE Std 802.11-2016)*; IEEE Standard for Information Technology–Telecommunications and Information Exchange between Systems–Local and Metropolitan Area Networks–Specific Requirements—Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications. IEEE: Philadelphia, PA, USA, 2021; pp. 1–4379.
49. Varghese, A.; Tandur, D.; Ray, A. Suitability of WiFi based communication devices in low power industrial applications. In Proceedings of the 2017 IEEE International Conference on Industrial Technology (ICIT), Toronto, ON, Canada, 22–25 March 2017; IEEE: Philadelphia, PA, USA, 2017; pp. 1307–1312.
50. Sheth, J.; Dezfouli, B. Enhancing the energy-efficiency and timeliness of IoT communication in WiFi networks. *IEEE Internet Things J.* **2019**, *6*, 9085–9097. [CrossRef]
51. Li, L.; Xiaoguang, H.; Ke, C.; Ketai, H. The applications of wifi-based wireless sensor network in internet of things and smart grid. In Proceedings of the 2011 6th IEEE Conference on Industrial Electronics and Applications, Beijing, China, 21–23 June 2011; IEEE: Philadelphia, PA, USA, 2011; pp. 789–793.

52. Mesquita, J.; Guimarães, D.; Pereira, C.; Santos, F.; Almeida, L. Assessing the ESP8266 WiFi module for the Internet of Things. In Proceedings of the 2018 IEEE 23rd International Conference on Emerging Technologies and Factory Automation (ETFA), Torino, Italy, 4–7 September 2018; Volume 1, pp. 784–791.
53. Soltanaghaei, E.; Dongare, A.; Prabhakara, A.; Kumar, S.; Rowe, A.; Whitehouse, K. Tagfi: Locating ultra-low power wifi tags using unmodified wifi infrastructure. *Proc. Acm Interact. Mobile Wearable Ubiquitous Technol.* **2021**, *5*, 1–29. [CrossRef]
54. Kadir, E.A.; Hu, A.P.; Biglari-Abhari, M.; Aw, K.C. Indoor WiFi energy harvester with multiple antenna for low-power wireless applications. In Proceedings of the 2014 IEEE 23rd International Symposium on Industrial Electronics (ISIE), Helsinki, Finland, 19–21 June 2023; IEEE: Philadelphia, PA, USA, 2014; pp. 526–530.
55. Wu, X.; Soltani, M.D.; Zhou, L.; Safari, M.; Haas, H. Hybrid LiFi and WiFi networks: A survey. *IEEE Commun. Surv. Tutorials* **2021**, *23*, 1398–1420. [CrossRef]
56. Subedi, S.; Hwang, S.S.; Pyun, J.Y. Hybrid wireless indoor positioning system combining BLE beacons and Wi-Fi APs. In Proceedings of the 2020 International Conference on Information and Communication Technology Convergence (ICTC), Jeju Island, Republic of Korea, 11–13 October 2023; IEEE: Philadelphia, PA, USA, 2020, pp. 36–41.
57. Minoli, D.; Occhiogrosso, B. Ultrawideband (UWB) technology for smart cities IoT applications. In Proceedings of the 2018 IEEE international smart cities conference (ISC2), Kansas City, MO, USA, 16–19 September 2018; IEEE: Philadelphia, PA, USA, 2018; pp. 1–8.
58. Monica, S.; Bergenti, F. Hybrid indoor localization using WiFi and UWB technologies. *Electronics* **2019**, *8*, 334. [CrossRef]
59. Lee, Y.; Kim, J.; Lee, H.; Moon, K. IoT-based data transmitting system using a UWB and RFID system in smart warehouse. In Proceedings of the 2017 Ninth International Conference on Ubiquitous and Future Networks (ICUFN), Milan, Italy, 4–7 July 2017; IEEE: Philadelphia, PA, USA, 2017; pp. 545–547.
60. Kolakowski, J.; Djaja-Josko, V.; Kolakowski, M.; Broczek, K. UWB/BLE tracking system for elderly people monitoring. *Sensors* **2020**, *20*, 1574. [CrossRef]
61. Shobha, N.S.S.; Aruna, K.S.P.; Bhagyashree, M.D.P.; Sarita, K.S.J. NFC and NFC payments: A review. In Proceedings of the 2016 International Conference on ICT in Business Industry & Government (ICTBIG), Indore, India, 18–19 November 2016; IEEE: Philadelphia, PA, USA, 2016; pp. 1–7.
62. Wu, T.; Arefin, M.S.; Redouté, J.M.; Yuce, M.R. A solar energy harvester with an improved MPPT circuit for wearable IoT applications. In Proceedings of the 11th EAI International Conference on Body Area Networks, Turin, Italy, 5–16 December 2016; pp. 166–170.
63. Cho, J.H.; Cole, P.H.; Kim, S. An NFC transceiver using an inductive powered receiver for passive, active, RW and RFID modes. In Proceedings of the 2009 International SoC Design Conference (ISOCC), Busan, Republic of Korea, 22–24 November 2009; IEEE: Philadelphia, PA, USA, 2009; pp. 456–459.
64. Zhao, A.; Chen, H. Small size NFC antenna with high performance. In Proceedings of the 2016 IEEE International Symposium on Antennas and Propagation (APSURSI), Fajardo, Puerto Rico, 26 June–1 July 2016; pp. 1469–1470.
65. Kordzadeh, A.; Holzmann, D.; Binder, A.; Moldaschl, T.; Sturm, J.; Roshanghias, A. Miniaturized On-Chip NFC Antenna versus Screen-Printed Antenna for the Flexible Disposable Sensor Strips. *IoT* **2020**, *1*, 309–319. [CrossRef]
66. Qian, X.; Li, Z.; Meng, Z.; Gao, N.; Zhang, Z. Flexible RFID tag for sensing the total minerals in drinking water via smartphone tapping. *IEEE Sens. J.* **2021**, *21*, 24749–24758. [CrossRef]
67. Bigler, T.; Kovács, G.; Treytl, A.; Windl, R. NFC for Powering Sensors in concrete. In Proceedings of the 2020 25th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA), Vienna, Austria, 8–11 September 2020; IEEE: Philadelphia, PA, USA, 2020; Volume 1, pp. 1355–1358.
68. Boada, M.; Lazaro, A.; Villarino, R.; Gil-Dolcet, E.; Girbau, D. Battery-less NFC bicycle tire pressure sensor based on a force-sensing resistor. *IEEE Access* **2021**, *9*, 103975–103987. [CrossRef]
69. Boada, M.; Lázaro, A.; Villarino, R.; Girbau, D. Battery-Less Soil Moisture Measurement System Based on a NFC Device With Energy Harvesting Capability. *IEEE Sens. J.* **2018**, *18*, 5541–5549. [CrossRef]
70. Boada, M.; Lazaro, A.; Villarino, R.; Girbau, D. Battery-less NFC sensor for pH monitoring. *IEEE Access* **2019**, *7*, 33226–33239. [CrossRef]
71. Escobedo, P.; Bhattacharjee, M.; Nikbakhtnasrabadi, F.; Dahiya, R. Smart bandage with wireless strain and temperature sensors and batteryless NFC tag. *IEEE Internet Things J.* **2020**, *8*, 5093–5100. [CrossRef]
72. Krorakai, K.; Klangphukhiew, S.; Kulchat, S.; Patramanon, R. Smartphone-based NFC potentiostat for wireless electrochemical sensing. *Appl. Sci.* **2021**, *11*, 392. [CrossRef]
73. Paul, K.; Gawade, D.R.; Simorangkir, R.B.; O'Flynn, B.; Buckley, J.L.; Amann, A.; Roy, S. A concertina-shaped vibration energy harvester-assisted NFC sensor with improved wireless communication range. *IEEE Internet Things J.* **2022**, *9*, 25474–25486. [CrossRef]
74. Promsuwan, K.; Soleh, A.; Samoson, K.; Saisahas, K.; Wangchuk, S.; Saichanapan, J.; Kanatharana, P.; Thavarungkul, P.; Limbut, W. Novel biosensor platform for glucose monitoring via smartphone based on battery-less NFC potentiostat. *Talanta* **2023**, *256*, 124266. [CrossRef] [PubMed]
75. Pousibet-Garrido, A.; Escobedo, P.; Guirado, D.; Ristic, G.S.; Palma, A.; Carvajal, M. Batteryless NFC dosimeter tag for ionizing radiation based on commercial MOSFET. *Sens. Actuators A Phys.* **2023**, *354*, 114295. [CrossRef]

76. Lazaro, A.; Villarino, R.; Girbau, D. A survey of NFC sensors based on energy harvesting for IoT applications. *Sensors* **2018**, *18*, 3746. [CrossRef] [PubMed]
77. Ulz, T.; Pieber, T.; Steger, C.; Lesjak, C.; Bock, H.; Matischek, R. SECURECONFIG: NFC and QR-code based hybrid approach for smart sensor configuration. In Proceedings of the 2017 IEEE International Conference on RFID (RFID), Warsaw, Poland, 20–22 September 2017; pp. 41–46.
78. Lee, J.S.; Su, Y.W.; Shen, C.C. A comparative study of wireless protocols: Bluetooth, UWB, ZigBee, and Wi-Fi. In Proceedings of the IECON 2007-33rd Annual Conference of the IEEE Industrial Electronics Society, Taipei, Taiwan, 5–8 November 2007; IEEE: Philadelphia, PA, USA, 2007; pp. 46–51.
79. Golsorkhtabaramiri, M.; Issazadehkojidi, N.; Pouresfehani, N.; Mohammadialamoti, M.; Hosseinzadehsadati, S.M. Comparison of energy consumption for reader anti-collision protocols in dense RFID networks. *Wirel. Netw.* **2019**, *25*, 2393–2406. [CrossRef]
80. Sugai, M.; Nishimura, K.; Takamatsu, K.; Fujinaga, T. Low power consumption microcontrollers and their applications. *Hitachi Rev.* **1999**, *48*, 313.
81. IEEE. International Roadmap for Devices and Systems (IRDS), 2022. Available online: https://irds.ieee.org/editions/2022/more-moore (accessed on 8 May 2024).
82. Blutman, K.; Kapoor, A.; Majumdar, A.; Martinez, J.G.; Echeverri, J.; Sevat, L.; van der Wel, A.P.; Fatemi, H.; Makinwa, K.A.; de Gyvez, J.P. A low-power microcontroller in a 40-nm cmos using charge recycling. *IEEE J. Solid-State Circuits* **2017**, *52*, 950–960. [CrossRef]
83. Danowitz, A.; Kelley, K.; Mao, J.; Stevenson, J.P.; Horowitz, M. CPU DB: Recording Microprocessor History: With this open database, you can mine microprocessor trends over the past 40 years. *Queue* **2012**, *10*, 10–27. [CrossRef]
84. Reddy, M.V.; Mauger, A.; Julien, C.M.; Paolella, A.; Zaghib, K. Brief History of Early Lithium-Battery Development. *Materials* **2020**, *13*, 1884. [CrossRef]
85. Madlmayr, G.; Langer, J.; Kantner, C.; Scharinger, J. NFC Devices: Security and Privacy. In Proceedings of the 2008 Third International Conference on Availability, Reliability and Security, Barcelona, Spain, 4–7 March 2008; pp. 642–647.
86. Zhao, Y.; Smith, J.R.; Sample, A. NFC-WISP: A sensing and computationally enhanced near-field RFID platform. In Proceedings of the 2015 IEEE International Conference on RFID (RFID), San Diego, CA, USA, 15–17 April 2015; IEEE: Philadelphia, PA, USA, 2015; pp. 174–181.
87. Lazaro, A.; Boada, M.; Villarino, R.; Girbau, D. Study on the reading of energy-harvested implanted NFC tags using mobile phones. *IEEE Access* **2019**, *8*, 2200–2221. [CrossRef]
88. Theis, T.N.; Wong, H.S.P. The End of Moore's Law: A New Beginning for Information Technology. *Comput. Sci. Eng.* **2017**, *19*, 41–50. [CrossRef]

MDPI AG
Grosspeteranlage 5
4052 Basel
Switzerland
Tel.: +41 61 683 77 34

Journal of Low Power Electronics and Applications Editorial Office
E-mail: jlpea@mdpi.com
www.mdpi.com/journal/jlpea

Academic Open
Access Publishing

mdpi.com

ISBN 978-3-7258-6735-6