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SiC Based Miniaturized Devices, 3rd Edition

Edited by
Stephen Edward Saddow, Brenda L. VanMil and Benoit Hamelin

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Contents

Preface

Silicon carbide (SiC) devices are found in many of today's advanced systems that demand high-power switching in harsh, high-temperature environments such as those found in base station power supplies, solar power inverters, and electric vehicles (EVs), where they are the enabling technology driving efficiency and thereby extending battery life and range. Radiation-hard sensors and the harsh-environment operation of micro-electrical–mechanical systems (MEMS) are increasingly looking to SiC to satisfy performance requirements in ways that traditional silicon cannot. The plethora of applications on the commercial market speaks for itself, especially for the highly precise manufacturing of silicon-based MEMS and NEMS. While this is a tremendous achievement, silicon as a material comes with some drawbacks, mainly in terms of mechanical fatigue and its thermal properties. Silicon carbide (SiC) is a well-known wide-bandgap semiconductor, and its adoption in commercial products is experiencing exponential growth, especially in the power electronics arena. While SiC power electronics and MEMS have been around for decades, in this Reprint, we seek to present both an overview of the devices that have been demonstrated to date and to bring new technologies and developments in the SiC processing field to the forefront. SiC continues to find new applications in consumer electronics, optical communications, industry, medicine, agriculture, space, and defense.

Stephen Edward Saddow, Brenda L. VanMil, and Benoit Hamelin
Guest Editors

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Editorial

Editorial for the Special Issue on SiC Based Miniaturized Devices, 3rd Edition

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Silicon Carbide: Enabling Next-Generation Power Electronics and High-Performance Computing.

The past two years have shown that Silicon Carbide is no longer an emerging technology: it is a fully ascendant force shaping the future of electrification, high-power computing, and advanced manufacturing. With global megafabs coming online, substrate and defect-control breakthroughs accelerating, and SiC penetrating deeper into automotive, industrial, and energy infrastructures, the material has reached a defining moment. For the first time, the world is preparing to manufacture it at the scale necessary to power the next generation of energy and computing systems.

Major Accomplishments (2024–2026)

- Global transition to 200 mm SiC wafers, led by major multibillion-dollar fab expansions in the U.S., Europe, and Asia [1].
- Unprecedented investment momentum, driven by national semiconductor initiatives and accelerating electrification [2–4].
- Market growth trajectory exceeding $10 billion by 2030, underpinned by EVs, renewable energy, and high-density data centers [5].
- Breakthrough substrate technologies, including SmartSiC engineered substrates and advanced composite wafer designs that reduce stress, cost, and defectivity [6,7].
- Strengthened global supply chain, with new crystal-growth facilities, vertically integrated EV module development, and high-volume SiC power-module packaging capabilities [8].
- Expansion beyond power electronics, with new activity in quantum sensing, advanced materials engineering, eco-friendly SiC synthesis, and multifunctional composite applications [9–14].

This volume, drawn from the Special Issue "SiC Based Miniaturized Devices, 3rd Edition" of *Micromachines*, and edited by Prof. Dr. Stephen E. Saddow, Dr. Brenda L. VanMil, and Dr. Benoit Hamelin, offers a comprehensive snapshot of the rapid progress and expanding scope of Silicon Carbide (SiC) technologies. The contributions assembled here reflect a vibrant and multidisciplinary research landscape, encompassing material growth, device physics, advanced modeling, and device reliability in extreme environments. Collectively, these works reaffirm SiC's position as a critical enabling material for next-generation miniaturized devices and high-performance systems.

The opening paper, "Model of Quality Factor for (111) 3C-SiC Double-Clamped Beams" (contribution 1), provides a rigorous investigation into the performance limits of SiC-based MEMS resonators. By combining experimental datasets with both analytical and numerical models, the authors elucidate the role of crystallographic defects at the 3C-SiC/Si interface in determining the quality factor. The identification of a minimum thickness threshold for optimal device performance offers a clear and actionable design guideline, bridging material science and MEMS engineering.

Expanding into high-voltage device innovation, "A 3.3 kV SiC Semi-Superjunction MOSFET with Trench Sidewall Implantations" (contribution 2) introduces a practical semi-superjunction architecture that balances enhanced electrical performance with fabrication feasibility. Through detailed TCAD simulations, the authors demonstrate meaningful improvements in breakdown voltage and on-state resistance, particularly in trench-based configurations. This contribution highlights the importance of manufacturable design strategies in advancing SiC power electronics.

The third paper, "Analyzing the Impact of Gate Oxide Screening on Interface Trap Density in SiC Power MOSFETs Using a Novel Temperature-Triggered Method" (contribution 3), addresses a long-standing challenge in device characterization. The proposed temperature-triggered threshold voltage shift (T3VS) method offers a streamlined approach to extracting interface trap density without requiring extensive prior knowledge of device structure. The findings emphasize the superior interface quality of trench devices while also cautioning against aggressive screening techniques that may inadvertently introduce defects, thereby underscoring the delicate balance between performance optimization and reliability.

In "A High-Density 4H-SiC MOSFET Based on a Buried Field Limiting Ring with Low Qgd and Ron" (contribution 4), the authors present a novel structural design that significantly enhances device efficiency. By incorporating a grounded P+ shield within a split trench architecture, the proposed MOSFET effectively mitigates electric field concentrations at the gate oxide. The resulting improvements in switching charge and figure of merit demonstrate how thoughtful structural innovation can overcome traditional trade-offs in device design.

Complementing these developments, "Simulation Study on 6.5 kV SiC Trench Gate p-Channel Superjunction Insulated Gate Bipolar Transistor" (contribution 5) explores the application of superjunction concepts to p-channel IGBTs. The work reveals substantial gains in forward conduction and switching behavior, while also analyzing temperature-dependent effects and performance trade-offs. These insights are particularly valuable for the development of ultra-high-voltage devices intended for demanding operational environments.

The importance of accurate modeling is further emphasized in "Numerical Simulations of 3C-SiC High-Sensitivity Strain Meters" (contribution 6), where the authors introduce anisotropic damping formulations to better capture energy dissipation in dynamic systems. By moving beyond conventional isotropic assumptions, this work enhances the predictive power of simulations and improves alignment with experimental observations, particularly in complex and directionally dependent materials.

Reliability under extreme conditions is a defining strength of SiC technologies, as demonstrated in "SPICE Model for SiC Bipolar Transistor and TTL Inverter Degradation Due to Gamma Radiation" (contribution 7). This study presents a calibrated SPICE model that connects radiation-induced material degradation to circuit-level performance. The demonstrated resilience of SiC devices under high radiation exposure, along with predictive

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lifetime modeling, underscores their suitability for space, nuclear, and other radiation-intensive applications.

Finally, "Optimization and Simulation on Gas Flow and Temperature Fields on the Homoepitaxial Growth of N-Doped 4H-SiC Wafers" (contribution 8) addresses the foundational challenge of material uniformity. By systematically analyzing chemical vapor deposition parameters and their influence on nitrogen doping profiles, the authors identify the conditions necessary for achieving homogeneous epitaxial layers. This work provides essential guidance for scaling SiC wafer production while maintaining the material quality required for advanced device applications.

Across all contributions, a unifying theme emerges: the critical interplay between material quality, device architecture, and modeling accuracy. Progress in SiC technology is shown to depend not on isolated advances, but on the integration of insights across these domains. From the control of defects at the atomic scale to the optimization of device performance and reliability at the system level, each paper contributes to a deeper and more cohesive understanding of the field. As SiC continues to transition from a specialized material to a mainstream platform for miniaturized and high-power devices, the importance of such integrated research efforts cannot be overstated. Future developments will likely build upon the methodologies and innovations presented here, further enhancing performance, scalability, and robustness.

In conclusion, this Special Issue captures both the current state and the future trajectory of SiC-based miniaturized devices. The editors were delighted to assemble a collection that not only advances the field but also inspires continued exploration and collaboration across disciplines. The work presented in this volume will undoubtedly serve as a valuable reference for researchers and engineers striving to push the boundaries of what SiC technology can achieve.

Conflicts of Interest: Author Benoit Hamelin was employed by the company EngeniusMicro. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

List of Contributions

1. Garofalo, A.; Muoio, A.; Sapienza, S.; Ferri, M.; Belsito, L.; Roncaglia, A.; La Via, F. Model of Quality Factor for (111) 3C-SiC Double-Clamped Beams. *Micromachines* **2025**, *16*, 148. https://doi.org/10.3390/mi16020148.
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Article

Model of Quality Factor for (111) 3C-SiC Double-Clamped Beams

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Abstract: Silicon carbide (SiC) is an interesting semiconductor for MEMS devices. The high-value Young's modulus of silicon carbide facilitates high frequencies and quality (Q) factors in resonant devices built with double-clamped beams. The aim of this work is to achieve the determination and modeling of the Q-Factor for samples of micromachined 3C-SiC film on <111> silicon substrates. This study demonstrates that the experimental datasets created by Romero, integrated with the thicker samples reported in this work, fit the theoretical model presented in the paper. Furthermore, the influence of the crystallographic defects present at the 3C-SiC/Si interface on the Q-factor can be observed both in the analytical model of Romero and in the numerical model present in COMSOL. 3C-SiC layers with thickness greater than 600 nm are needed to achieve an ideal performance from double-clamped beams.

Keywords: silicon carbide; MEMS; quality factor; 3C-SiC; resonance frequency

1. Introduction

The term MEMSs refers to micro-electromechanical systems, and it is used to describe a device or an array of devices than can range in size from a few microns to a few millimeters. This type of system constitutes a collection of microsensors which can detect and control environmental changes from the micro scale to respond on the macro scale, and obtain information about materials' properties, geometry, and mechanical or electromagnetic effects [1]. Currently, MEMSs are everywhere; they can be found in thermal sensors, pressure sensors, resonators, mass and temperature sensors, pumps, motors, optical sensors and transmission systems [2–8]; in microsurgery, medical and biomedical devices [9]; and even in earthquake- [10–12] and volcanic eruption-monitoring sensors [13–15]. Given the notable success of MEMSs as sensors in the most disparate applications, it is possible to think about their eventual use in a so-called harsh environment. Thus, they must be able to operate and provide realistic results even when exposed to this type of environment for long time and should be suitable for use in a wide range of applications without sustaining damage or breakages. A harsh environment is defined as one that includes exposure to strong mechanical vibrations or sudden variations, elevated temperatures—potentially for long periods of time—highly corrosive and erosive conditions, and an intense to high level of radiation [16]. Semiconductors are materials that respond perfectly to these requests, and we have the potential to be able to exploit their properties. Silicon is the principal material

in semiconductors-based MEMSs due to its good electronic and mechanical properties. The fact that silicon is the prevailing semiconductor in the industry gives it several advantages, like low-cost fabrication and is potential to be combined with other materials in the same system, compared to all others. However, silicon has limitations in application fields where performances are limited by its material properties [1]. Silicon-based systems are not the right choice for applications in harsh environments. Silicon electronics cannot operate for long periods of time at temperatures beyond 150 °C; indeed, a Si-based system is limited to electronic device efficiency below 250 °C for bulk silicon substrate devices and close to 300 °C for silicon-on-insulator (SOI) substrate devices [17,18]. Therefore, research has moved towards other alternative wide-bandgap semiconductors with good mechanical, thermal and chemical properties. Silicon carbide (SiC) is a valid alternative to replace silicon in MEMSs devices. Among SiC's properties, its mechanical properties have been studied and analyzed so that they can be exploited for use in various applications. Such properties include its high-value Young's modulus, which permits it to achieve higher resonance frequencies than other materials, and the quality factor (also called the Q-factor) which describes the energy loss of the system, determining the noise level in resonant sensors, which is closely related to the sensor resolution. Achieving a high-resonator-quality factor is important for applications like precision mass sensing, and, to enhance the resonator's performance, the product of the frequency and the quality factor must reach a maximum value. The resonant frequency for micro-beam geometry depends on the residual stress of the material and the elastic properties, dimensions and geometry of the system. Varying the length and width of the resonator, it is possible to study the quality factor and resonance frequency variations. A reduction in width and an increase in length determine an increase in the quality factor due to clamping loss. Comparing several samples with different dimensions, the resonance frequency increases by 20% as the silicon carbide stress doubles, and the quality factor grows. Then, in this way, the product fxQ achieves a four-fold increase. The best value for Q is 3.41×10^6 with a product fxQ of 9.49×10^{11} Hz for an epitaxial SiC(111) on silicon substrate [19].

In this paper, we study and measure the Q-factor on double-clamped (DC) beam resonators, which is realized by micromachining of 3C-SiC films grown on (111) silicon substrates, and its maximum value as a function of the film thickness, using the analytical model described in a paper by Romero et al. [20] as a function of (111) 3C-SiC film thickness, extending the range of film thicknesses. This behavior has also been simulated numerically using COMSOL Multiphysics® and a different model, and the final results are in good agreement with the analytical model.

2. Materials and Methods

2.1. Origin of Defects and Stress in 3C-SiC

Silicon carbide and silicon have similar cubic crystal structures: Si has a diamond structure with a lattice parameter equal to 0.543 nm, whereas 3C-SiC has a lattice parameter equal to 0.436 nm and has a zinc-blende crystal structure; the resulting lattice mismatch between 3C-SiC and Si is approximately 20% and contributes to the generation of compressive intrinsic stress.

The growth of epitaxial 3C-SiC layer on silicon substrate is also affected by the difference between the thermal expansion coefficients (about 8%), providing a tensile stress contribution during the final cooling step of the growth process. The lattice and thermal mismatches are the main reasons for defects in the system, typically at the interface film/substrate. The linear defects are, typically, dislocations; the planar defects are called stacking faults, while the volume defects are micro-twins (MTs), anti-phase boundaries

(APBs) and protrusions. Misfit dislocation and stacking faults are the main types of detectable defects, and they are generated at the 3C-SiC/Si interface and can propagate up to the surface of the film, influencing and modifying the mechanical and electrical properties of the material. Previous works have demonstrated how the best matching at the SiC/Si interface was achieved by 5 crystalline cells of 3C-SiC, with 4 crystalline cells of Si resulting in a generation of array of misfit dislocation spaced approximately 1.6 nm from one another [21–24]. Both defects are thickness dependent. It has been observed that the density can be reduced by increasing the film thickness. The most difficult defects to remove are the stacking faults which start at the 3C-SiC/Si interface and propagate into the film. The crystal quality increases when lower growth rates are used [25]. In a recent publication by Calabretta et al. [13], it was observed that (111) 3C-SiC is extremely interesting because there is a mechanism, which is not present in (100) 3C-SiC, that produces a faster decrease in the SFs density and can have a strong effect on the performance of the MEMS devices created using this material. This later study explains the better quality of (111) 3C-SiC layers and their higher stress level that produces a resonator with higher resonance frequency and a higher Q-factor. Then, in this work, several resonators are created using this material, which is extremely promising for future MEMSs devices.

2.2. Sample Preparation

The 3C-SiC film growth on silicon substrates was made in a horizontal, resistively heated hot wall and low-pressure Chemical Vapor Deposition (LPCVD) system with a rotating sample holder. The heteroepitaxial growth consists of two different growth steps: first, carbonization and second, a growth ramp, with purified hydrogen (H_2) and argon (Ar) as a gas carrier, silane (SiH_4) as a silicon precursor and Propane (C_3H_8) as a carbon precursor.

During the growth, in the reactor chamber, N_2 and tri-methyl-aluminum diluted in H_2(TMA) are introduced as N-type (N) and P-type (Al), respectively. Aluminum incorporation is realized and controlled by adding HCl to the process. The substrates are on-axis (111) bare Si with 1000 μm of thickness. All the samples are prepared with different bulk and film thicknesses, doping types (n, p), and doping levels (from NID (Non-Intentionally Doped) < 10^{16} cm^{-3}, to $\sim 5 \times 10^{19}$ cm^{-3}). The fabrication process of the micromachined structures on bulk wafer is a type of front-side bulk micromachining in which part of the bulk substrate is removed by RIE etching and isotropic and anisotropic wet etching to create channels, grooves or pits in the substrate with the advantage of creating a free-standing 3C-SiC thin-film membrane, or double-clamped beams [26]. The micromachining flow is based on the following steps: by LPCVD, a 3C-SiC film is grown on silicon substrate, and a mask made of two piled layers of SiO_2 (with 1.5 μm thickness) and polycrystalline silicon (with 300 nm of thickness) are used. The next step involve lithography and self-aligned RIE etching (Reactive Ion Etching). The mask composed of polysilicon and SiO_2 is patterned and then the pattern is transferred to the 3C-SiC layer by another RIE etching step on the silicon surface. The polysilicon is eliminated, while some residual traces of SiO_2 can be found on the surface; these protect the SiC layer during the next step, when isotropic silicon plasma etching is realized. All the residual SiO_2 on the surface is removed by wet silicon oxide etching. The last step foresees additional TMAH silicon etching to increase the under-etching of the microstructures without damaging the SiC. In this way, several beams with widths of 16 μm and different lengths ranging from 200 μm to 1 mm have been realized, as reported in Figure 1. More details about the fabrication process of the resonators and the effect of the different doping methods on the Young's modulus of the layer can be found in [27].

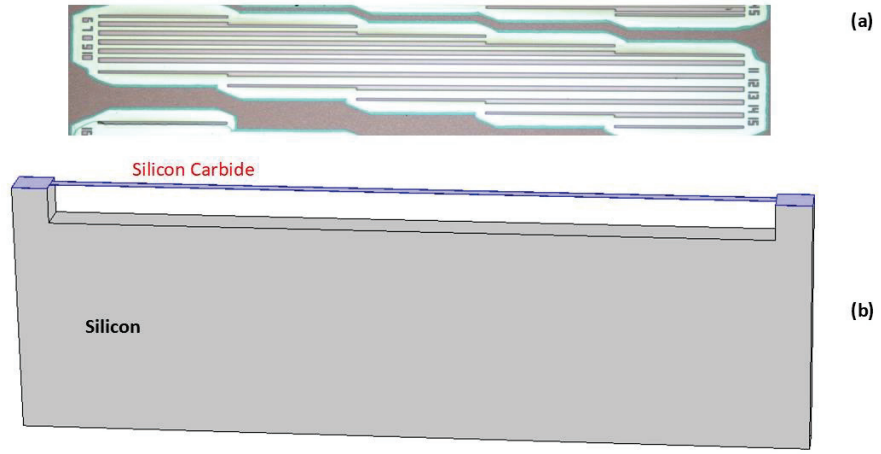

Figure 1. (**a**) Double-clamped beam arrays, viewed from the top, with variable length and width; (**b**) from the scheme, the two materials SiC and Si can be distinguished.

2.3. Characterization

The measurements of the mechanical resonance frequency were performed with an optical setup based on the Doppler interferometer, in which the actuation of the resonator at different frequencies was realized using a L515A1 Thorlabs laser diode, operating at a wavelength of 515 nm in the power range 0–10 mW, connected to the output signal of an Anritsu MS2036C Network Analyzer (NA). The sensing of the induced beam vibration was carried out by connecting the output of the laser Doppler focused on the vibrating resonator to the input of the network analyzer for open-loop measurements. The measured samples were placed inside a vacuum chamber to avoid an air damping effect and the peak amplitude at the resonance frequency of beams was measured for quality factor evaluation. The Q-factor was calculated with the formula $Q = \frac{f_0}{\Delta f}$, where f_0 is the resonance frequency and Δf is the Full-Width Half-Maximum (FWHM) that can be achieved with Lorentz fit (see Figure 2). The vacuum chamber was made of brass to avoid leakage and degassing and fitted with a transparent glass window to align the laser with the aid of a video camera with $10\times$ magnification. The high vacuum in the chamber was achieved by a turbo pumping station from Pfeiffer Vacuum, below 10^{-3} mbar. Based on the resonance frequency, it was also possible to calculate the residual stress of the beams, which confirmed the previously results obtained in [27] with a different setup based on piezo-electric actuation.

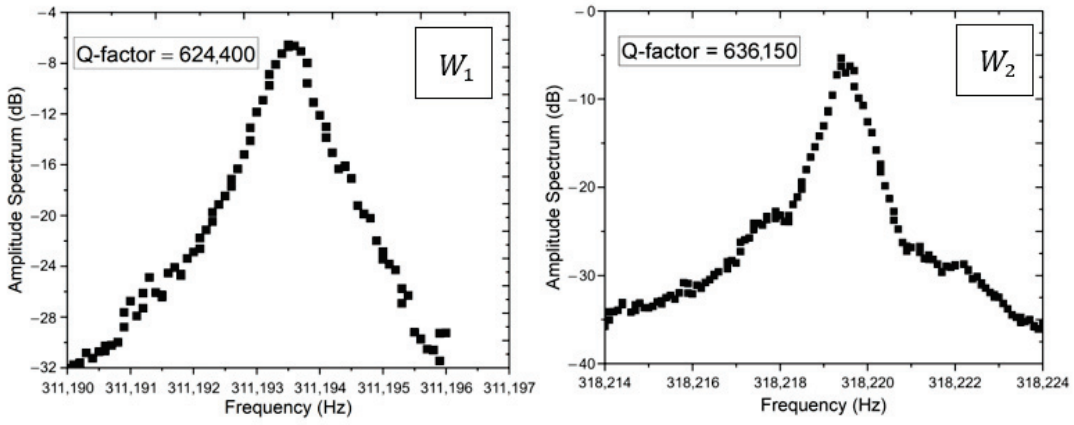

Figure 2. Amplitude spectrum of 1000 µm beam of W1 (**left**) and W2 (**right**). The legend shows the corresponding Q-factor value.

After the first round of measurements, several results were considered inaccurate due to the frequency resolution of the NA (1 Hz) being lower than the FWHM of the peak amplitude at resonance frequency. Thus, a new setup was adopted to perform additional measurements on the same devices. In the new setup, instead of the NA, a custom electronic readout (Figure 3) was developed to produce the actuation signal controlling the green laser and to analyze the output of the Doppler vibrometer, calculating the phase and amplitude spectrum. The frequency resolution achieved with this new setup was better than the first, with a minimum frequency variation of 0.07 Hz, and the output current signal could be varied up to 46 mA for the DC value and 6 mA for the AC value.

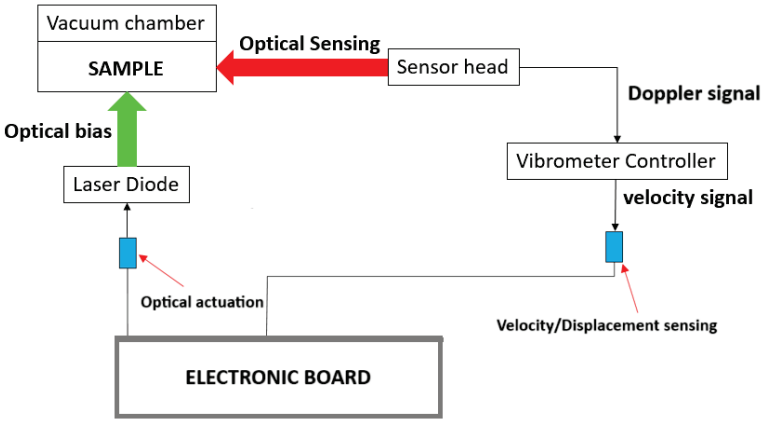

Figure 3. Setup for the characterization of the beam resonators.

Beam arrays with a fixed width 16 μm and length of 1000 μm, the same dimensions as the Romero samples, were measured as reported in Table 1:

Table 1. Overview of Q-factor, residual stress and resonance frequency measurements on 3C-SiC samples.

Wafer Id	Si Type	Doping	Thickness (μm)	Res. Stress (MPa)	Res. Frequency (kHz)	Q-Factor
W1	<111>	NID	0.89	1010	312.20	624,400
W2	<111>	NID	0.73	982	318.07	636,150

Q-factor values refer to 1000 μm beam length.

3. Theoretical Model of Losses at the 3C-SiC/Si Interface

Some devices require a very high degree of frequency stability with respect to changes in the environment. In this application, it is important to study the sensitivity of a device's eigenfrequencies with respect to the variation in different physical quantities, e.g., length, thickness. Simulations of the system under consideration were created below with COMSOL Multiphysics® (version 6.1), a finite element analyzer, solver, and simulation software package with various applications, which is especially relevant to coupled phenomena and multiphysics. When a structure vibrates in a more complex normal mode, there are some regions of compression and some of extension, and it is associated with energy loss from the vibrational mode and corresponding damping for the resonant mode. Thermoelastic damping is particularly important in smaller MEMSs structures, in which regions of compression and expansion are in close proximity. Eigenfrequencies or natural frequencies are certain discrete frequencies at which a system is prone to vibrate. When vibrating at a certain eigenfrequency, a structure deforms into a corresponding shape: the eigenmode.

An eigenfrequency analysis can only provide the shape of the mode, not the amplitude of any physical vibration.

There are several ways by which damping can be described from a mathematical point of view. The following is the equation of motion for a system with a single degree of freedom (DOF) with viscous damping and no external loads:

$$m\ddot{u} + c\dot{u} + ku = 0. \tag{1}$$

After division with the mass, m, we get a normalized form, usually written as:

$$\ddot{u} + 2\zeta\omega_0\dot{u} + \omega_0 2u = 0 \tag{2}$$

Here, ω_0 is the undamped natural frequency and ζ is called the damping ratio. For the motion to be periodic, the damping ratio must be limited to the range $0 < \zeta < 1$. The amplitude of the free vibration in this system will decay with the factor:

$$e^{-\zeta\omega_0 t} = e^{-\frac{2\pi\zeta t}{T_0}} \tag{3}$$

where T_0 is the period of the undamped vibration. The relation between the logarithmic decrement and the damping ratio is:

$$\delta = \frac{2\pi\zeta}{\sqrt{1-\zeta^2}} \approx 2\pi\zeta \tag{4}$$

When a structure is subjected to a harmonic excitation at a frequency that is close to a natural frequency exactly at resonance, the vibration amplitude tends to reach infinity, unless there is some damping in the system. The actual amplitude at resonance is controlled solely by the amount of damping. In some systems, like resonators, the aim is to achieve as much amplification as possible. This leads to another popular damping measure: the quality factor or Q factor. It is defined as the amplification at resonance. The Q factor is related to the damping ratio by:

$$Q = \frac{1}{2\zeta\sqrt{1-\zeta^2}} \approx \frac{1}{2\zeta} \tag{5}$$

Another starting point for the damping description is to assume that there is a certain phase shift between stress and strain. Talking about phase shifts is only meaningful for a steady-state harmonic vibration.

Given the Q factor and residual stress values, the aim of this work was to verify if the experimental data, combined with the experimental results in the literature on 3C-SiC (111) follow the model of quality factor described by Romero et al. [20]. The generic model for the total quality consists of five different energy-dissipation mechanisms grouped in two main categories: intrinsic and external. The external energy dissipation is due to two mechanisms: gas damping Q_{gas}^{-1} and clamping loss Q_{clamp}^{-1}. The intrinsic dissipation consists of surface losses Q_{surf}^{-1}, intrinsic friction in the volume of the material Q_{vol}^{-1} and thermoelastic losses Q_{TED}. The contribution of the thermoelastic losses has already been calculated [20] in highly stressed trampoline resonators ($Q_{TED} \sim 10^9$) and it is assumed to be neglected in this study due to their small contribution to thin resonators. The total quality factor is then given by:

$$Q^{-1} = D^{-1}Q_{int}^{-1} + Q_{clamp}^{-1} \tag{6}$$

With the dilution factor D(h) depending on the dimensions (thickness h and length L), the 3C-SiC Young's modulus E and the mean stress of the beam. Please refer to Appendix A for a thorough explanation of the Q-factor model.

One method for estimating the mean stress is to measure the resonance frequency of the released double-clamped beam. Because of the high residual stress in the structures, the resonance frequency can be simplified, depending only on the length of the beam, the mean stress and the density of the material ($\rho = 3210 \frac{kg}{m^3}$ for SiC). For the mean stress σ as a function of the thickness of the beam, an approximated model for resonators has been developed by the following analytic expression:

$$\sigma(h) = \sigma_{\max}\left(1 - e^{-[c_1(h-h_0)]^{c_2}}\right) \tag{7}$$

where the mean stress depends only on the thickness. In the analytic expression, h_0 is the transition thickness at which the mean stress transitions from compressive to tensile ($\sigma(h_0) = 0$), c_1 is the exponential growth constant and c_2 is the kinetic order. The maximum value for the mean stress is σ_{max}.

Clamping losses are caused by phonon tunneling from the beam to the substrate through the clamping points in the form of acoustic radiation. The analytical results obtained for the contribute Q_{clamp} for the double-clamped beams are reported in the Appendix A.

The intrinsic dissipation Q_{int}^{-1} in microresonators originates from two mechanisms: surface losses Q_{surf}^{-1} and volume losses Q_{vol}^{-1}. The main contribution to the surface losses occurs on the top and the bottom surface of the device, as they have a larger area than the lateral surface. The volume losses are caused by the defect motion in the volume of the resonator.

When the vertical density of the defects is not uniform, as is the case for heteroepitaxial-grown 3C-SiC on Si substrate, the dissipation profile is vertically nonuniform. So, for this nonuniform vertical density of the defects, a simple model is considered for the intrinsic dissipation contribution to the quality factor. In this model, SiC film is considered as a bilayer system: the first layer is a layer with a high density of defects, with thickness h_0, near the 3C-SiC/Si interface; the second layer, with thickness $(h - h_0)$, is a high-quality crystal layer above the rich-defect layer, and a reduction in the defect density is expected, but total elimination is not anticipated. The contribution of the surface and volume losses to the Q-factor and all the parameters involved in the calculation are detailed in the Appendix A. The parameters derived by the fitting of the experimental Q-factor data in [20] were as follows: $\beta_{hq} = (12 \pm 5) \times 10^{10}$ m^{-1}, $\beta_{def} = (10 \pm 4) \times 10^{10}$ m^{-1} $Q_{def}^{vol} = (0.75 \pm 0.15) \times 10^3$ and $Q_{hq}^{vol} = (8.0 \pm 1.8) \times 10^3$. The last two parameters are related to the volumetric dissipation due to crystal dislocations, stacking faults or defects in the bulk SiC.

4. Comparison of Experimental Data

Given Q-factor and residual stress values, the aim of this work was to verify if our experimental data, combined with the results in the literature relating to thinner materials, are in agreement with the model of quality factor described in Romero et al.'s paper [20].

Given the residual stress values of the beam, it was necessary to verify the trend of mean stress σ as function of the thickness h of the beam, using the analytic expression given in Equation (7). Among all the wafers used for the measurement, only two samples were acceptable for our purposes, because both the NID (Non-Intentionally Doped) and 3C-SiC film were grown on (111) silicon substrate. Therefore, combining the residual stress of our samples (red circles) with the results present in the literature for 3C-SiC films with thicknesses ranging between 75 and 340 nm (black squares) on silicon substrates [20], the total residual stress as function of the thickness of 3C-SiC films is represented in Figure 4:

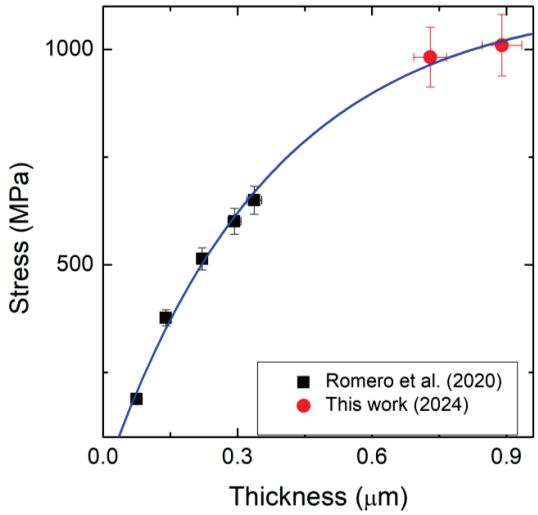

Figure 4. Mean stress σ(h) as a function of the thickness of the 3C-SiC film for the resonators. Black squares refer to Romero et al.'s data [20]; red circles refer to our samples.

According to the fit of the data using the analytical model given in Equation (3), the following calculations are achieved: maximum residual stress σ_{max} = 1063 MPa; the transition thickness is $h_0 = 0.011$ μm, at which the mean stress transitions from compressive to tensile ($\sigma(h_0 = 0) = 0$), while the exponential growth constant $c_1 = 0.02$ nm^{-1} and the kinetic order $c_2 = 0.62$. For the stress fit [20], the σ_{max} = 740 MPa, h_0 = 0.068 μm and the exponential growth constant $c_1 = 0.0015$ nm^{-1} and the kinetic order $c_2 = 0.54$; the different results are mainly due to the higher thickness values added in this work, which improved the precision of the fitting.

The experimental D(h) values determined by combining the measurements of the stress σ(h) and the analytical model of the thickness-dependent dilution factor for a beam of length L are represented in Figure 5.

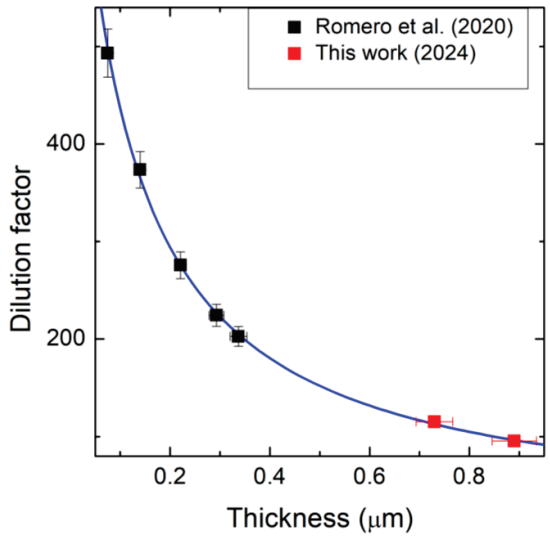

Figure 5. Dilution factor D(h) as function of the thickness of the 3C-SiC film for the resonators. Black squares refer to Romero et al.'s [20] data; red squares refer to our samples.

After the determination of dilution factor D(h) values, the residual stress σ(h) and the quality factor, the intrinsic and external contributions to the total quality factor were

studied by combining the data for our 3C-SiC on (111) Silicon substrates and the results in the literature [20].

The experimentally determined values of Q_{int}, as shown in Figure 6, are deduced from Equation (1) with the analytic model for Q_{clamp} and $D(h)$, while the theoretical fit is obtained using equation given by the Q-factor model maintaining β_{hq} and β_{def} values [20]. For 3C-SiC films, the bilayer system is used, which involves the intrinsic parameter Q_{def} of the defect-rich layer (green curve) and Q_{hq} of the high-quality layer (red curve). Each layer is limited by its respective volume loss $Q_{hq}^{vol} = 1.42 \times 10^4$ and $Q_{def}^{vol} = 132$, represented by a dashed red line and a dashed green line, respectively. This result of a Q_{hq}^{vol} that is more than an order of magnitude of Q_{def}^{vol} confirms how the rich-defect layer determines the reduction in the quality factor due to the defect at the interface. The total surface loss in the bilayer system (dashed purple line) represents the surface dissipation in both layers (high-quality and rich-defect layers).

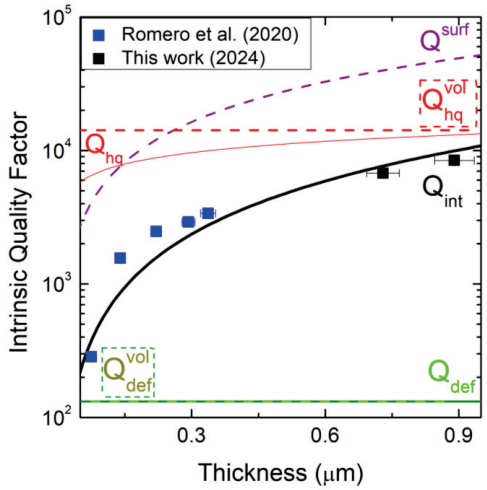

Figure 6. Thickness-dependent fitting intrinsic Q-factor parameters for the bilayer system. Blue squares refer to the intrinsic Q-factor values of Romero's samples [20]; black squares refer to ours, while the black curve represents the theoretical fit. The dashed purple curve is the total surface loss curve in the bilayer system; the green curve and red curve represent the intrinsic parameter of the defect-rich and high-quality layer, respectively. Each red and green curve is limited by a dashed line, referring to the respective volume loss factor.

In the intrinsic quality factor graph, as a function of the thickness of the SiC films, a result consistent with the literature was found. The same trend was expected for every intrinsic Q-factor parameter. The first difference is related to the value of $Q_{def}^{vol} = 132$ and $Q_{hq}^{vol} = 1.42 \times 10^5$, in our case, and $Q_{def}^{vol} = 750$ and $Q_{hq}^{vol} = 8 \times 10^3$ in the literature. The main reason for this may be due to the thickness of our samples, which is greater than the thickness in the literature, influencing the overall trends. When the thickness of the films is increased, both Q_{def} and Q_{hq} tend toward to the respective Q_{def}^{vol} and Q_{hq}^{vol} because the intrinsic dissipation in the bilayer system does not occur through surface losses at the top and bottom surface of the devices but by the defect motion in the volume. The highest value of Q_{int}, increasing film thickness, was found near 1 μm, but for the total quality-factor curve, the external clamping loss must be calculated to observe the eventual deviations. The last step of this work is related to the study of the total quality factor, considering several trends.

In Figure 7, the black squares and red circles indicate the experimental values of the quality factor Q(h) determined during the first step of measurements, calculating the resonance frequency and FWHM ratio, with error bands found by error propagation. The blue line indicates the theoretical fit given by Equation (A1). The dashed red and green lines represent the DxQ_{hq} and DxQ_{def}, respectively; the limit for the Q-factor when only the high-quality

(or rich-defect) layer of the resonator is considered explains the huge difference (two orders of magnitude) between the two curves. The dashed purple curve is Q_{clamp} calculated using the analytical expression (A4) in Appendix A for a beam resonator with mean stress σ(h). Neglecting the Q_{clamp} curve, the DxQ_{hq} curve is about two orders of magnitude greater than the total quality factor, and it is related to the possibility of fabricating beams in which only a high-quality film can be considered. In the literature, this result has been achieved for back-side-etched resonators. The lower DxQ_{def} curve refers to the quality factor of a resonator in which the rich-defect layer has a thickness greater than that of the high-quality layer, so in this case, a worsening of the intrinsic dissipation occurs, and the quality factor decreases with the thickness. The dashed black line DxQ_{int} shows how the contribution of clamping losses cannot be neglected in Equation (A1). Despite this, when it comes to highly stressed resonators, clamping loss is often neglected; the main contribution comes from the intrinsic dissipation. In this case, DxQ_{int} is used, but from the graph in Figure 5, it is easy to observe the deviation of Q from DxQ_{int}, so the external clamping loss must be considered. Therefore, when the 3C-SiC film thickness increases, the highest quality factor is about 6.3×10^5 at around 1 μm of thickness, and to achieve this, all the contributions must be considered—intrinsic and external. The energy-dissipation mechanisms at this thickness result from the intrinsic dissipation, considering mainly the volumic contributions for both high-quality and rich-defect layers in the bilayer system, and the external clamping losses related to the phonon tunneling from the beam to the substrate through the clamping points in the form of acoustic radiation. Even in the total Q-factor trend, there is a high congruence between our data and the results in the literature. Therefore, this model for quality factor developed by Romero et al. [20], which considers the two main energy-dissipation mechanisms (intrinsic and external), and the bilayer system model for the intrinsic contributions, can be used to determine the quality factor and the material properties of (111) 3C-SiC-undoped film on silicon substrate. Achieving this high-value quality factor, at 1 μm thickness, is a key result for application fields in which high resolution and sensitivity are fundamental. The experimental results obtained in this section have been used as a reference for the numerical modeling in the following section.

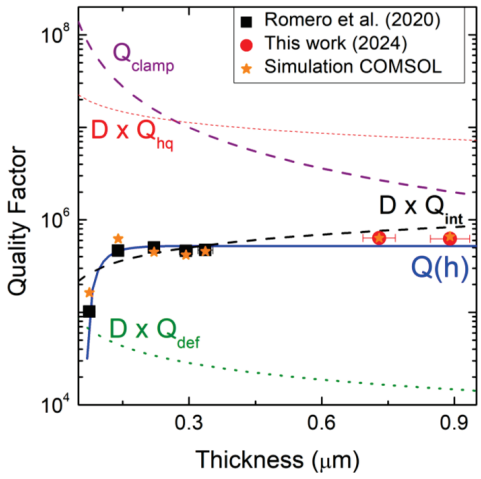

Figure 7. Mean values of the measured Q-factor with different thicknesses. Black squares refer to the total Q-factor of Romero et al.'s data [20]; red circles refer to our samples, while the dashed blue curve is the theoretical fit of the total quality factor. The dashed red and green curves are, respectively, the limit for the Q-factor when only the high-quality (or rich-defect) layer is considered in the resonator. The dashed purple curve is the external energy dissipation resulting from clamping loss. The dashed black curve is obtained when, for the total Q-factor, it is possible to neglect external energy dissipation via clamping loss, considering only intrinsic energy loss. The orange stars represent data simulated with COMSOL Multiphysics®.

5. Numerical Simulation of Damping and Resonant Frequency Analysis

Damping defined by an isotropic loss factor is proportional to the displacement amplitude. Usually, the conversion between the damping ratio and loss factor damping is considered at resonant frequency, and then $\eta \approx 2\zeta$ where η is inversely proportional to the Q-factor:

$$Q = \frac{1}{\eta} \tag{8}$$

One of the most obvious manifestations of damping is the amplitude decay during free vibrations. In a structural dynamics analysis, modeling the damping is important. The main reason to include damping in an eigenfrequency analysis is to estimate how much different resonances will be dampened. When using COMSOL Multiphysics, it is possible to include loss factor damping through the Damping subnode via a material model. The Damping node adds Rayleigh damping by default and the damping parameter ξ is expressed in terms of the mass m and the stiffness k as shown below.

$$\xi = \alpha_{dM} m + \beta_{dK} k \tag{9}$$

Rayleigh damping is proportional to a linear combination of the stiffness and mass. In the following equation, loss information appears as a multiplier for the elastic constitutive matrix D^c

$$D^c = (1 + j\eta_s)D \tag{10}$$

The use of loss factor damping traditionally refers to a scalar-valued loss factor η_s; it is a value deduced from true complex-valued material data. Comparing the experimental resonance frequency and the simulated data, we can identify some limitations of the current damping models, especially with respect to a double-clamped configuration. The simulated resonance frequency points are always greater than the experimental ones, and their difference is not constant. In Figure 8, we plot the difference between the values of the experimental and simulated resonance frequencies as a function of the thicknesses; there is a linear correlation (R = 0.998) between resonance frequency and thickness (t). The graphical points show an evident linear proportionality.

$$\Delta F = kt + c \tag{11}$$

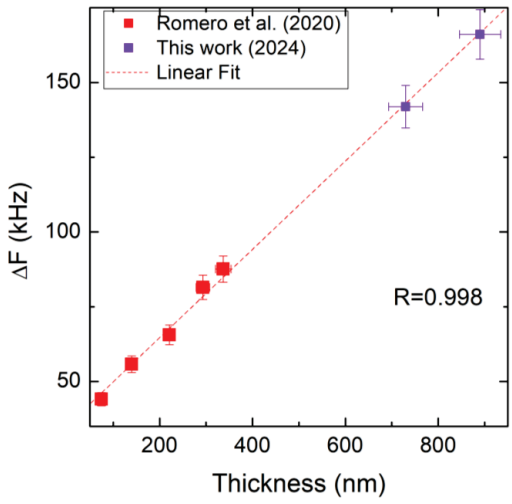

Figure 8. The difference between the values of the experimental and simulated frequencies as a function of the thickness, distinguishing Romero data [20] (red squares) and our data (violet squares).

This difference between the experiment and the numerical simulation is attributed to an effect of the damping on the resonance frequency that has not been perfectly described in the standard model reported in COMSOL.

Another aspect can be observed using these numerical simulations. As reported in Equation (8), the loss factor should be inversely proportional to the Q factor. If we look at the data reported in Figure 9, we can observe that only for the thicker layers do we observe this proportionality between the isotropic loss factor and the Q-factor. Instead, at reduced thickness, there is a large difference between the isotropic loss factor obtained by fitting the experimental data and the theoretical expected value. This is probably due to the large influence of the thinner films on the defects at the 3C-SiC/Si interface, which increase the isotropic loss factor of the material. For thicknesses higher than 700 nm, instead, the defects at the 3C-SiC/Si interface have a less pronounced effect on the mechanical properties of the resonator and the loss factor approach theoretical value depicted in Equation (8).

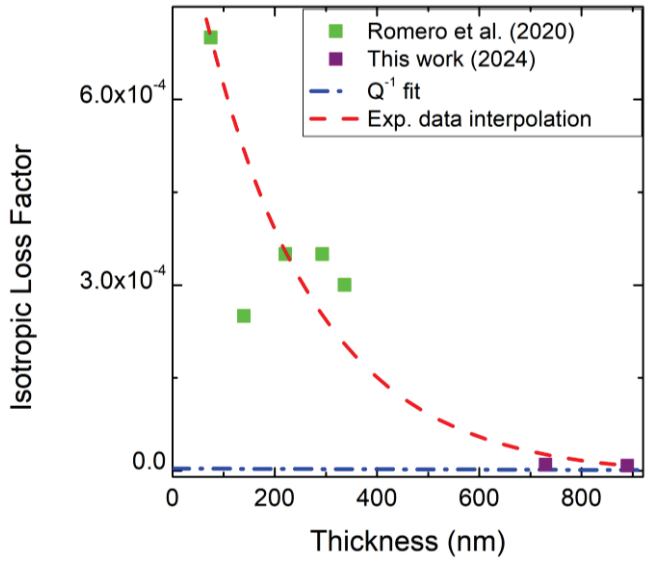

Figure 9. Relation between η vs. thickness : light green squares represent the isotropic loss factor of Romero et al.'s samples [20], while purple squares represent our data. The blue dashed–dotted curve is the Q^{-1} fit. The red dashed curve represents experimental data interpolation.

6. Conclusions

This work aims to verify if our data based on results from the literature confirm the results of the quality factor model presented by Romero et al. [20]. Combining all the equivalent 3C-SiC (111) dual-clamped beams with a low doping level and the same length, it is possible to compare seven different samples with thicknesses ranging from 0.075 to 0.89 µm. For all these wafers, the residual stress and dilution factor have been calculated, with analytic expressions, in addition to all the quality factor parameters distinguishing the two energy-dissipation mechanisms (intrinsic and external). In the intrinsic dissipation, the 3C-SiC films are associated with a bilayer system, in which there are two different layers: a rich-defect layer near the 3C-SiC/Si interface and a high-quality layer above the rich-defect layer, which has a lower defect density. The external dissipation mechanism occurs via clamping losses, determined by an analytic expression. Although in highly stressed film, the clamping loss is often neglected, in our case, we demonstrated how quality factors offer multiple contributions, both intrinsic and external. For all the samples, a quality factor with an average value of 5.5×10^5 was measured and increasing the 3C-SiC film thickness resulted in the quality factor reaching 6.3×10^5 in correspondence with 1 µm

thickness of the 3C-SiC layer. This is quite a high value that allows us to achieve a better sensitivity and resolution in application fields. A high coherence between our data and the results in the literature has been observed, so the quality factor model developed by Romero et al. [20] represents an improvement for the study of the properties of SiC layers with high resolution.

COMSOL simulations show that, by introducing an isotropic loss factor, it is possible to obtain the experimental Q-factor in the entire range of thicknesses listed this paper. The resonance frequencies have not been obtained with accuracy using the isotropic loss factor, so this numerical model should be improved to consider these differences, which increase with the thickness of the 3C-SiC layer. Finally, it has been observed that the isotropic loss factor is high for thin 3C-SiC layers and approaches the theoretical value for 3C-SiC thicknesses above 700 nm. This numerical model can also be used to observe the importance of the defective layer at the 3C-SiC/Si interface with regard to the performance of the analyzed MEMSs.

Author Contributions: Conceptualization, A.G., A.M., S.S., A.R. and F.L.V.; software, A.M.; formal analysis, A.G.; data curation, S.S., M.F., L.B. and A.R.; writing—original draft preparation, A.G., A.M. and F.L.V.; writing—review and editing, A.G., A.M., S.S., A.R. and F.L.V.; visualization, A.G.; supervision, F.L.V.; funding acquisition, F.L.V. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: Data will be made available on request.

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Conflicts of Interest: The authors declare no conflicts of interest.

Appendix A

According to the Q-factor model reported in [20] for 111 3C-SiC resonators, the overall Q factor of the devices can be expressed as follows:

$$Q^{-1} = D^{-1}Q_{int}^{-1} + Q_{clamp}^{-1} \tag{A1}$$

assuming the thermoelastic damping contribution is negligible because of the reduced thickness of the layers. In Equation (A1), Q is the overall Q-factor of the resonator, Q_{int}, Q_{clamp} are the intrinsic and clamp contributions to the Q-factor and D is a dilution factor given by

$$D^{-1}(h) \approx \left(2\lambda + \pi^2\lambda^2\right) \tag{A2}$$

with

$$\lambda = \frac{h}{L}\sqrt{\frac{E}{12\sigma(h)}} \tag{A3}$$

where E is SiC's Young's modulus, h is the thickness of the SiC layer, L is the length of the beam resonator and σ(h) is the average residual stress of the layer, depending on its thickness.

The clamp contribution to the Q-factor, due to the emission of acoustic phonons towards the bulk of the device during vibration, can be expressed as follows:

$$Q_{clamp} = \alpha \frac{3\rho_s}{2\rho}\sqrt{\frac{E_s\rho}{2\sigma(h)\rho_s}}\frac{L}{h} \tag{A4}$$

in which E_S is silicon's Young's modulus, ρ, ρ_S are the densities of SiC and Si, respectively, and α is a fitting parameter that is kept constant during the fitting procedure.

The intrinsic contribution to the Q-factor, on the other hand, can be calculated as follows:

$$Q_{int}^{-1}(h) = \left(\frac{h-h_0}{h}\right)\left\{\left[Q_{hq}^{surf}(h)\right]^{-1} + \left[Q_{hq}^{vol}(h)\right]^{-1}\right\} + \left(\frac{h_0}{h}\right)\left\{\left[Q_{def}^{surf}\right]^{-1} + \left[Q_{def}^{vol}\right]^{-1}\right\} \tag{A5}$$

where h_0 is the thickness of the defective SiC layer, whereas Q_{hq}^{surf}, Q_{hq}^{vol}, Q_{def}^{surf}, Q_{def}^{vol} are the surface and volume's contributions to the intrinsic Q-factor, respectively, due to the defective (h_0-thick) and high-quality SiC layers used to create the resonators.

The surface contributions to the intrinsic Q-factor can, in turn, be expressed as functions of the layer thickness h in the following way:

$$Q_{hq}^{surf} = \beta_{hq}(h - h_0) \tag{A6}$$

and

$$Q_{def}^{surf} = \beta_{def}(h - h_0) \tag{A7}$$

As can be seen from Equations (A1)–(A7), the overall Q-factor model proposed in [20] contains six fitting parameters, which are Q_{hq}^{vol}, Q_{def}^{vol}, β_{hq}, β_{def}, h_0, and α. These parameters can be determined in principle by a best-fitting procedure in which the model is compared with experimental Q-factor data possibly measured on resonators with different thicknesses (h).

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A 3.3 kV SiC Semi-Superjunction MOSFET with Trench Sidewall Implantations

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Abstract: Superjunction (SJ) technology offers a promising solution to the challenges faced by silicon carbide (SiC) Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) operating at high voltages (>3 kV). However, the fabrication of SJ devices presents significant challenges due to fabrication complexity. This paper presents a comprehensive analysis of a feasible and easy-to-fabricate semi-superjunction (SSJ) design for 3.3 kV SiC MOSFETs. The proposed approach utilizes trench etching and sidewall implantation, with a tilted trench to facilitate the implantation process. Through Technology Computer-Aided Design (TCAD) simulations, we investigate the effects of the *p*-type sidewall on the charge balance and how it affects key performance characteristics, such as breakdown voltage (BV) and on-state resistance ($R_{DS\text{-}ON}$). In particular, both planar gate (PSSJ) and trench gate (TSSJ) designs are simulated to evaluate their performance improvements over conventional planar MOSFETs. The PSSJ design achieves a 2.5% increase in BV and a 48.7% reduction in $R_{DS\text{-}ON}$, while the TSSJ design further optimizes these trade-offs, with a 3.1% improvement in BV and a significant 64.8% reduction in $R_{DS\text{-}ON}$ compared to the benchmark. These results underscore the potential of tilted trench SSJ designs to significantly enhance the performance of SiC SSJ MOSFETs for high-voltage power electronics while simplifying fabrication and lowering costs.

Keywords: SiC MOSFET; superjunction; semi-superjunction; trench etching; sidewall implantation; tilted trench

1. Introduction

Silicon carbide (SiC) Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) offer several advantages over traditional silicon (Si) devices due to the superior properties of the material, including a higher breakdown electric field, superior thermal conductivity, faster switching speeds, and lower on-state resistance [1]. These advantages enable SiC MOSFETs to handle higher voltages and operate at higher frequencies with greater efficiency, making them ideal for high-performance power electronic systems [2–4]. However, despite their advantages, SiC MOSFETs face significant challenges when targeting voltage ratings above 3000 V. The primary reason for these issues is the thick drift region required for high voltage blocking in SiC devices, which increases both resistance and the complexity

of fabrication. Therefore, silicon-based devices, such as Si IGBTs, continue to dominate this market segment due to the high conduction losses and increased fabrication costs of their SiC counterparts. As a result, there is a need for innovative design approaches that can maximize the inherent benefits of SiC while minimizing its limitations.

Superjunction (SJ) technology represents a promising approach to overcoming these challenges by surpassing the unipolar limit of SiC MOSFETs [5–7]. This technology improves the trade-off between conduction losses and breakdown voltage by alternating *p*-type and *n*-type pillars within the drift region. The fabrication of SiC SJ MOSFETs faces significant challenges, requiring advanced fabrication techniques and precise doping control to ensure optimal performance [8].

One of the main SJ fabrication methods is multi-epitaxial (ME) growth [9,10], which involves multiple cycles of epitaxial growth and ion implantation to create alternating *p*-pillars. While effective, this process is challenging for thick, deep structures due to the low diffusion coefficients of dopants and the inherent hardness of SiC, which complicates the fabrication and increases costs.

An alternative approach is trench-filling epitaxial (TFE) growth [11], which involves etching trenches into the *n*-type SiC substrate, refilling them with *p*-type epitaxial layers, and planarizing the surface using Chemical Mechanical Polishing (CMP). Although TFE growth offers more precise control over doping profiles, it also presents challenges in achieving uniform refill and comes with high fabrication costs.

To address these fabrication challenges while still harnessing the benefits of SJ technology, the semi-superjunction (SSJ) approach has emerged as a practical compromise [12–14]. Unlike full SJ designs, SSJ structures do not fully implement the superjunction architecture, which simplifies the fabrication process and reduces costs. Despite this simplification, SSJ designs can still provide significant performance improvements over traditional SiC MOSFETs, making them a valid option for high-voltage applications [15].

The authors previously introduced cost-effective methods for the fabrication of SJ Schottky Barrier Diodes (SBDs) using trench etching and sidewall implantations [16–18].

This paper presents, through a comprehensive numerical study, 3.3 kV SiC MOSFETs for a cost-effective and easy-to-fabricate design. The SJ effect is obtained through a process of trench etching and sidewall implantation, utilizing a tilted trench to simplify the fabrication process and improve manufacturability [19].

Two different designs, sketched in Figure 1, are analyzed: a planar gate SSJ (PSSJ) (Figure 1a) and a trench gate SSJ (TSSJ) (Figure 1b). This study focuses on the static performance of the proposed designs, specifically analyzing breakdown voltage (BV), on-state resistance ($R_{DS\text{-}ON}$), and electric field distribution. These parameters are evaluated using Technology Computer-Aided Design (TCAD) simulations performed with the finite element simulator Sentaurus, developed by Synopsys [20]. Although our study does not investigate switching behavior in detail [21,22], previous works [23] have shown that semi-SJ trench structures exhibit fast switching characteristics due to their majority-carrier nature. Given that the proposed SSJ MOSFETs operate under the same principle, a similar switching behavior is expected. Moreover, while we acknowledge the importance of self-heating [24,25], we do not focus on this phenomenon in our study. Our primary objective, however, is to compare the static performance of the proposed semi-superjunction (SSJ) designs against a standard design. The results are compared to current state-of-the-art devices at the 3.3 kV breakdown rating, aiming to demonstrate the potential of SSJ designs to optimize the performance and cost-effectiveness of high-voltage SiC MOSFETs.

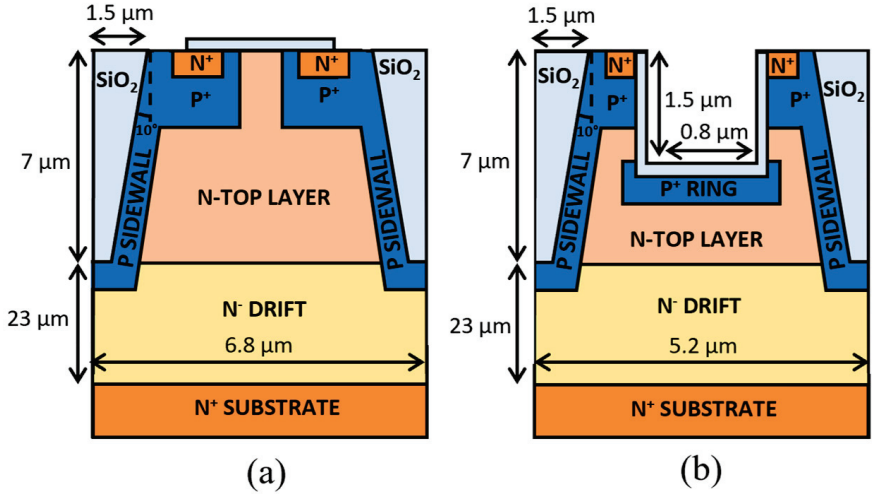


Figure 1. Sketch of the proposed devices. (**a**) Planar gate semi superjunction (PSSJ). (**b**) Trench gate semi superjunction (TSSJ). Not to scale.

2. Benchmark Structures

To accurately evaluate the performance enhancements provided by the proposed tilted trench semi-superjunction designs, it is essential to establish benchmark structures for comparison. The benchmarks chosen for this study are a standard planar MOSFET and an ideal vertical SSJ MOSFET. The planar MOSFET serves as a primary benchmark structure due to its widespread use in power electronics and provides a reference for the performance of traditional SiC devices under similar conditions. The ideal vertical SSJ MOSFET represents the theoretical best-case scenario for trench etching and sidewall implantation SSJ devices, serving to benchmark the upper limits of performance achievable with this technology. The study of the ideal case allows an understanding of the maximum potential improvements possible with this SSJ approach and the determination of whether there is a sufficient margin to explore the more practical, yet non-ideal, tilted trench design. The benchmark structures are sketched in Figure 2.

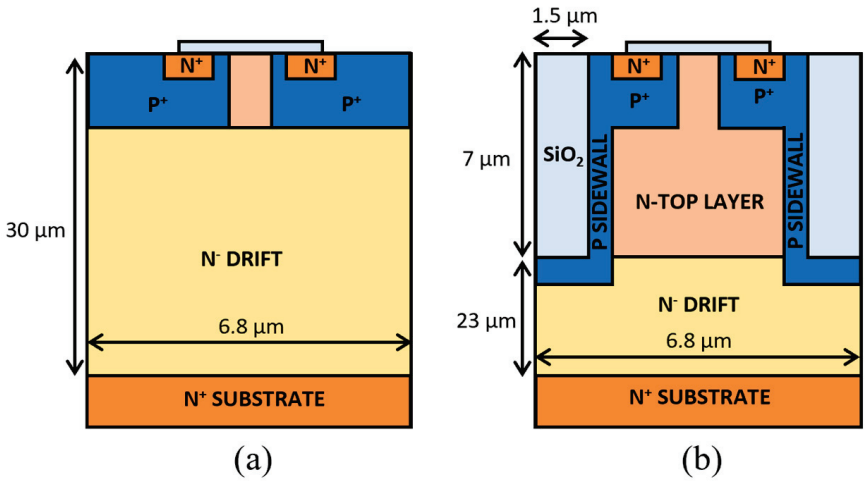


Figure 2. Sketch of the reference devices. (**a**) Planar (benchmark). (**b**) Vertical semi-superjunction (ideal). Not to scale.

All simulated structures in this work utilize a 4H-SiC substrate, which is 100 µm thick and has a constant nitrogen doping concentration of 1×10^{19} cm^{-3}. To achieve a BV greater than 3.3 kV, the devices have a drift region thickness of 30 µm with a constant doping concentration

of 3×10^{15} cm^{-3}. The *n*+ source region has a peak doping concentration of 1×10^{19} cm^{-3} and the *p* contact for the body region has a constant doping concentration of 1×10^{19} cm^{-3} to ensure good ohmic contact. More specifically, a Gaussian doping profile is assumed for the body and source regions, reflecting the realistic diffusion and implantation processes commonly used during device fabrication. In contrast, the epitaxial layer and substrate are modeled with constant doping concentrations. This approximation is widely adopted in device simulations due to the high uniformity typically achieved in epitaxial growth processes and the homogeneous nature of substrate materials. To capture the transition between the epitaxial layer and the substrate accurately, a Gaussian transition doping profile is applied at their interface, ensuring a smooth change in doping concentration and preserving the physical accuracy of the model. A 50 nm thick gate oxide is considered, with a fixed charge at the gate oxide/semiconductor interface of 2×10^{12} cm^{-3} [26,27]. The area factor is adjusted to consider a total area of the simulated devices of 1 cm^2.

2.1. Planar MOSFET

A standard planar MOSFET (Figure 2a) was simulated with a cell pitch of 6.8 µm to maintain consistency with the other simulated structures. The threshold voltage (V_{TH}) was around 4.5 V, as shown by the transfer characteristic in Figure 3a. A JFET width of 1.2 µm was considered, and a constant doping concentration of 6×10^{15} cm^{-3} was also included to improve the on-state conduction of the device [28]. The resulting output characteristic for a V_{GS} of 18 V is reported in Figure 3b. The corresponding $R_{DS\text{-}ON}$ is 14.3 mΩ·cm^2 [29]. The reverse characteristic is shown in Figure 3c, indicating a BV of 4000 V. The electric field (EF) distribution at 2 kV, reported in Figure 3d, shows that the electric field peak (1.7 MV/cm) is located at the bottom of the body region, while the gate oxide is free from EF pressure.

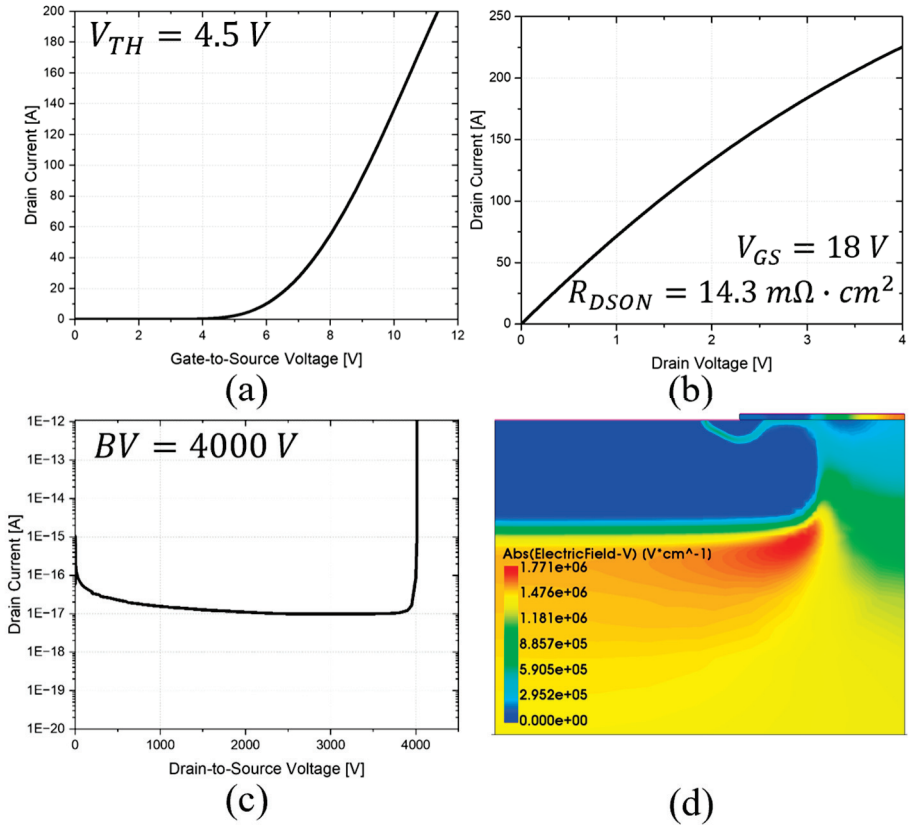


Figure 3. Planar structure performance. (**a**) Transfer characteristic. (**b**) On-state characteristic. (**c**) Off-state characteristic. (**d**) Electric field distribution at 2 kV.

2.2. Vertical Semi-Superjunction MOSFET

To achieve a uniform electric field distribution in the superjunction designs, a charge balance between the *n*-layer and the *p*-type sidewall implantation should be attained [30] (see Equation (1)).

$$Q_N = Q_P \tag{1}$$

This balance can be obtained following the formula reported in Equation (2).

$$N_D W_N = N_A W_P \tag{2}$$

where N_D and W_N are the doping concentration and width of the *n*-layer, respectively, and N_A and W_P are the doping concentration and width of the *p*-type sidewall, respectively. According to Equation (2), the ideal semi-superjunction is achieved when the trench angle is 0 degrees, resulting in a constant W_N along the trench and thus achieving a fully compensated charge between the *p*-type sidewall and the contiguous *n*-zone. This 0-degree trench configuration allows for the best performance with this design.

A vertical SSJ with trench etching and sidewall implantation was simulated as an ideal case. The design featured an oxide-filled trench 3 µm wide and 7 µm deep. A sidewall *p*-type implantation was considered to allow the SJ effect. The *p*-doping profiles along the sidewalls were modeled with Gaussian distributions to accurately reflect realistic implantation and diffusion processes. A fixed charge of 5×10^{12} cm^{-3} at the interface between the SJ trench and the semiconductor was considered [31] to take into consideration additional edge roughness. All other design parameters were consistent with those of the planar MOSFET. To ensure the charge balance, an *n*-top layer with a doping concentration (N_{TOP}) higher than the drift region was considered next to the oxide trench.

An analysis of its performance was conducted by varying the *p*-sidewall peak doping concentration and implantation depth (d_{SW}). Variations in the JFET *n*-top layer doping concentrations of 2×10^{16} cm^{-3} and 3×10^{16} cm^{-3}, as well as *p*-sidewall depths of 200 nm to 400 nm, were considered. The resulting behavior of the BV is reported in Figure 4a.

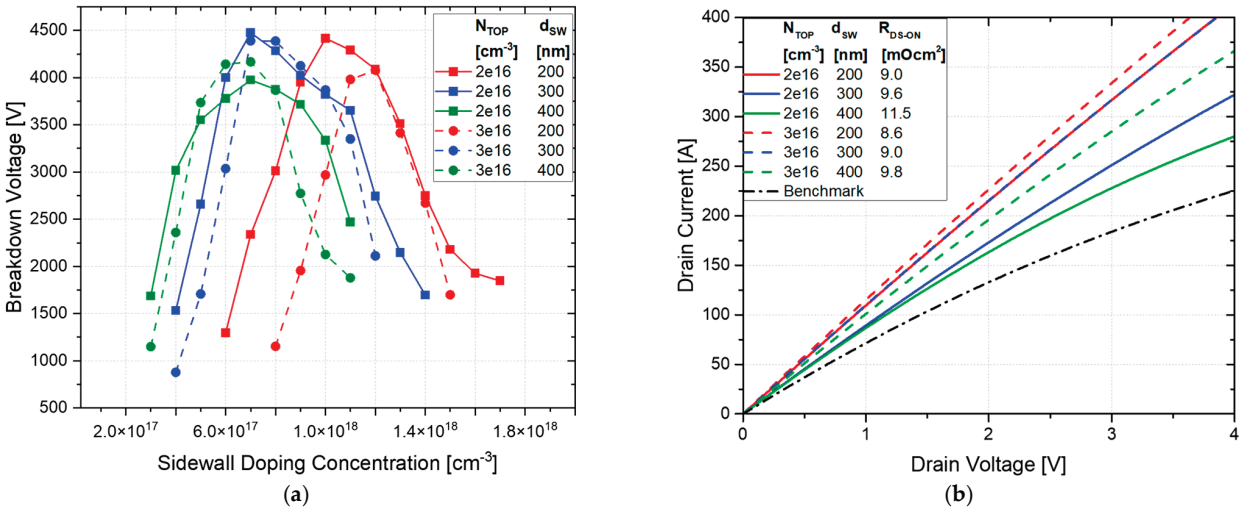


Figure 4. Vertical SSJ performance. (**a**) Analysis of the breakdown voltage versus sidewall peak doping concentration, varying N_{TOP} (solid line 2×10^{16} cm^{-3}, dotted line 3×10^{16} cm^{-3}) and sidewall depth (red 200 nm, blue 300 nm, green 400 nm) for the vertical SSJ. (**b**) On- state characteristics and $R_{DS\text{-}ON}$, varying N_{TOP} and sidewall depth for the vertical SSJ. The sidewall doping concentration is set to the values that provide the best charge balance for each combination of N_{TOP} and d_{SW}.

A wide implantation window was obtained for most of the design parameter combinations, improving the BV by up to 11.9% compared to the planar case.

A significant improvement in the on-state conduction was also achieved, with $R_{DS\text{-}ON}$ varying from 8.6 mΩ·cm^2 to 11.5 mΩ·cm^2, ensuring an improvement from 21.7% to 49.8%, as shown in Figure 4b. The on-state characteristics were simulated using the *p*-sidewall concentration that achieved the optimal charge balance for each combination of N-top layer doping and sidewall depth, according to Figure 4a. In Figure 5, the EF distribution at 2 kV is reported, showing reasonable values for the EF peak value.

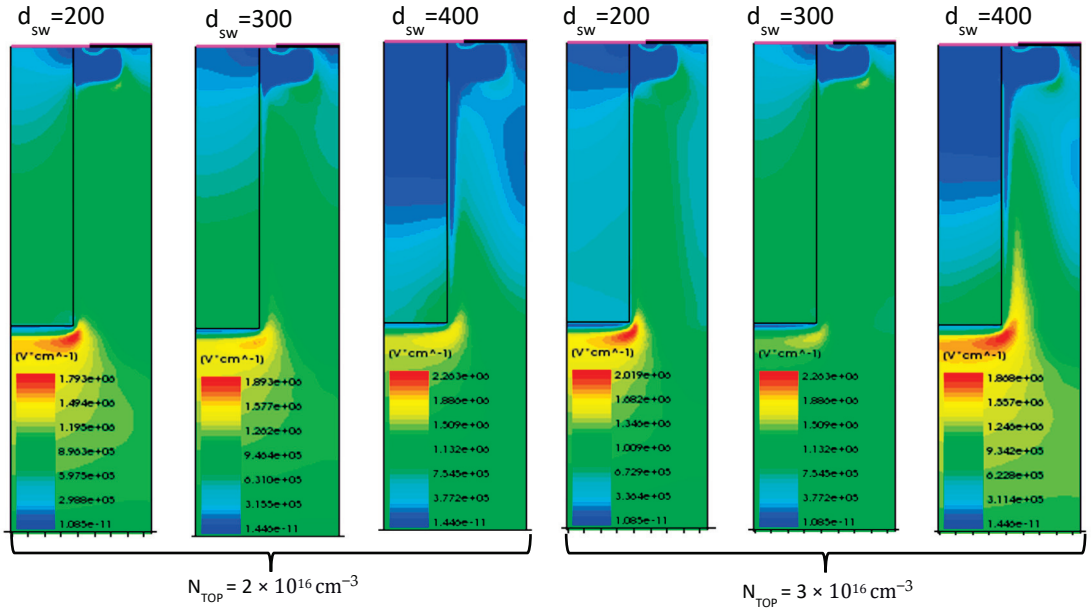


Figure 5. Electric field distribution at 2 kV, varying N_{TOP} and sidewall depth for the ideal vertical SSJ. The sidewall doping concentration corresponds to the optimal BV value for each case.

Despite significantly improved performance over the planar design, a 0-degree trench posed significant challenges for the implantation through the sidewalls. However, the promising results obtained from the ideal vertical SSJ case indicate that substantial performance enhancements are achievable through this technology. This suggests that there is a sufficient margin to explore the tilted trench design, which, although non-ideal, may offer a practical compromise between performance, fabrication feasibility, and cost.

2.3. Tilted Semi-Superjunction MOSFET

To overcome the challenges associated with implantation through a vertical sidewall and make the implantation process more feasible, a tilted trench with an angle of 10 degrees was considered, pivoting at the midpoint of the trench depth (i.e., 3.5 µm). This inclination facilitates the implantation process by providing better access to the trench sidewalls, reducing the difficulty of achieving uniform doping profiles. The details of the fabrication of SiC superjunction trenches have already been discussed by the authors in [32].

In an ideal vertical superjunction structure, the width of the *n*-type region (W_N) would remain constant along the trench depth to ensure uniform charge compensation between the *p*- and *n*-type regions. In the tilted trench design, the trench wall slope causes a variation in W_N along the trench depth, which affects the charge distribution. Specifically, when the *n*-top layer doping concentration is optimized to balance charges at the midpoint of the trench, this results in an overcompensation of positive charges (Q_P) above the pivot point and an overcompensation of negative charges (Q_N) below the pivot point. This uneven

charge distribution can lead to localized electric field peaks, potentially increasing the risk of premature breakdown or affecting the device's breakdown voltage.

The impact of this charge imbalance is further exacerbated at different depths of the trench. Above the pivot point, where Q_P is overcompensated, the electric field may be more concentrated, leading to higher field stress in these regions. Conversely, below the pivot point, the overcompensation of Q_N can create regions with a lower electric field intensity, which might reduce the overall effectiveness of the SJ effect. Therefore, while the tilted trench design simplifies fabrication, it necessitates the careful optimization of doping profiles and trench geometry to balance these competing effects and achieve the desired device performance.

An analysis of the performance of the proposed PSSJ and TSSJ designs is reported below.

Firstly, a planar channel semi-superjunction design with a tilted oxide trench (see Figure 1) is simulated, focusing on optimizing the SSJ effect while minimizing charge imbalance. To further exploit the SSJ effect, a TSSJ design is considered, incorporating a trench gate that is 0.8 μm wide and 1.5 μm deep. The absence of a JFET region in this design allows for a reduced cell pitch of 5.2 μm. Additionally, a *p*-ring with a high doping concentration of 5×10^{18} cm^{-3} is added at the bottom of the trench to shield the gate oxide from excessive electric fields, enhancing device reliability.

The analysis includes variations in sidewall doping concentration across different sidewall depths (200 nm, 300 nm, 400 nm) and different doping concentrations for the JFET *n*-top layer (2×10^{16} cm^{-3} and 3×10^{16} cm^{-3}), aiming to optimize the overall device performance in terms of BV and $R_{DS\text{-}ON}$. An overview of the doping concentrations and dimensions of the simulated structures is provided in Table 1.

Table 1. Overview of the doping concentrations and dimensions of the simulated structures.

	Value				Unit
	Planar	**Vertical SSJ**	**PSSJ**	**TSSJ**	
Drift doping	3×10^{15}				cm^{-3}
Body doping	1×10^{19}				
Source doping	1×10^{19}				
Substrate doping	1×10^{19}				
N-top layer doping	/	$2 \times 10^{16}, 3 \times 10^{16}$			
P-sidewall peak doping	/	$2 \times 10^{17} - 2 \times 10^{18}$			
Drift thickness	30				μm
Substrate thickness	100				
Cell pitch	6.8			5.2	
SJ trench depth	/	7			
SJ trench width	/	3			
P-sidewall depth	/	0.2, 0.3, 0.4		0.2, 0.3	
Gate trench width	/			0.8	
Gate trench depth	/			1.5	
SJ trench angle	/	0	10		°

3. Results and Discussion

The performance of the proposed designs in terms of BV, EF distribution, and $R_{DS\text{-}ON}$ was evaluated through TCAD simulations. These simulations provide insights into how varying design parameters, such as doping concentrations and trench geometry, influence the electrical characteristics of planar and trench SSJ MOSFETs.

3.1. Planar Semi-Superjunction

The behavior of the BV as a function of the sidewall peak doping concentration is reported in Figure 6a. The maximum achievable BV is 4101 V, obtained with an *n*-top layer doping concentration of 2×10^{16} cm^{-3} and a sidewall doping concentration and depth of 9×10^{17} cm^{-3} and 300 nm, respectively. For a JFET *n*-layer doping concentration of 2×10^{16} cm^{-3}, the BV across all sidewall depths approaches and indeed exceeds the benchmark value (4 kV) but remains below the ideal SSJ case (4.4 kV). This trend suggests that while the doping concentration is sufficient to establish a good electric field distribution, it does not fully optimize charge balancing. For a higher JFET *n*-top layer doping concentration (i.e., 3×10^{16} cm^{-3}), the BV is significantly lower. This decrease can be attributed to an increased imbalance in the charge distribution between the *n*- and *p*-type regions, resulting in localized electric field enhancements that reduce the overall breakdown voltage.

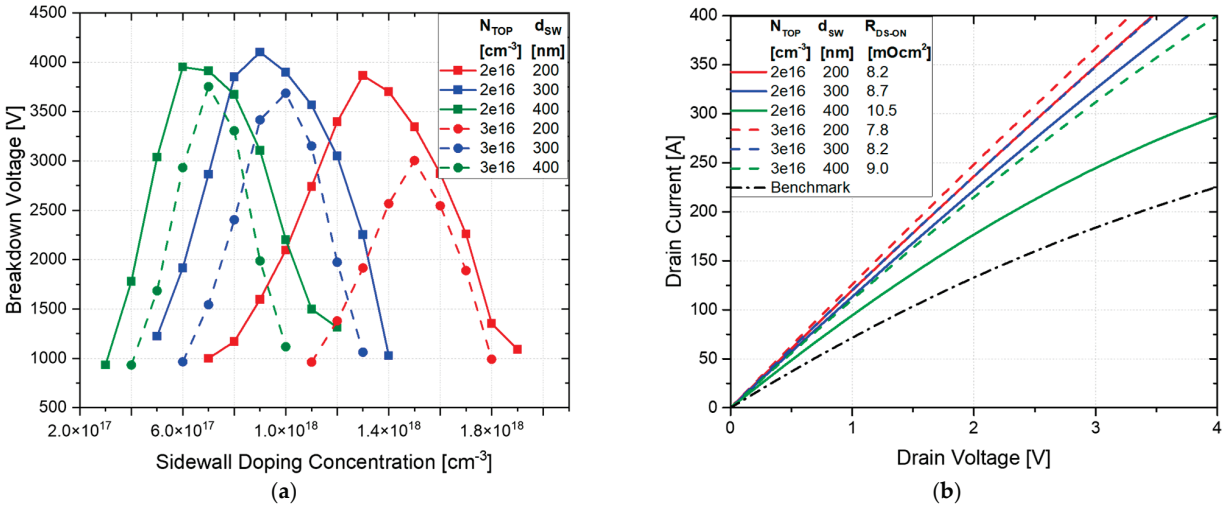


Figure 6. PSSJ performance. (**a**) Analysis of the breakdown voltage versus the sidewall peak doping concentration with varying N_{TOP} (solid line 2×10^{16} cm^{-3}, dotted line 3×10^{16} cm^{-3}) and sidewall depth (red 200 nm, blue 300 nm, green 400 nm) values for the PSSJ. (**b**) On-state characteristics and $R_{DS\text{-}ON}$, varying N_{TOP} and sidewall depth for the PSSJ. The sidewall doping concentration is set to the values that provide the best charge balance for each combination of N_{TOP} and d_{SW}.

Conversely, the lowest BV is observed for an *n*-top layer doping concentration of 3×10^{16} cm^{-3} with a sidewall depth of 200 nm as the high *n*-layer concentration and shallow *p*-sidewall result in maximum charge imbalance. This imbalance significantly reduces the effectiveness of charge compensation, leading to a BV of 3 kV.

Figure 6b shows the on-state characteristics and the relative $R_{DS\text{-}ON}$ values when varying the *n*-top layer doping concentration and sidewall depth. It is worth noting that the on-state performance is not significantly affected by the *p*-doped sidewall doping concentration. The $R_{DS\text{-}ON}$ decreases as the *n*-top layer doping concentration increases, whereas it increases when the sidewall depth decreases. This trend occurs because a higher doping concentration increases the number of charge carriers, reducing resistance, whereas a shallower sidewall enlarges the effective current conduction path, thereby reducing the overall resistance.

The best result is achieved with an *n*-top layer doping concentration of 3×10^{16} cm^{-3} and a sidewall depth of 200 nm, yielding an $R_{DS\text{-}ON}$ of 7.8 mΩ·cm^2. This configuration provides an effective conduction path that minimizes resistance. Conversely, the least efficient result is observed for a constant *n*-top layer doping concentration of 2×10^{16} cm^{-3} with a sidewall depth of 400 nm, resulting in an $R_{DS\text{-}ON}$ of 10.5 mΩ·cm^2. The deeper

sidewall and lower doping concentration reduce the effective carrier density and cause a narrower conduction path, increasing resistance.

Figure 7 shows the electric field distribution at 2 kV for the optimal breakdown voltage corresponding to each combination of sidewall depth and *n*-top layer doping concentration. A deeper sidewall doping leads to a more uniform EF distribution along the oxide trench while also reducing the peak electric field. This uniformity is critical for enhancing device reliability, as it minimizes the likelihood of field-induced failures.

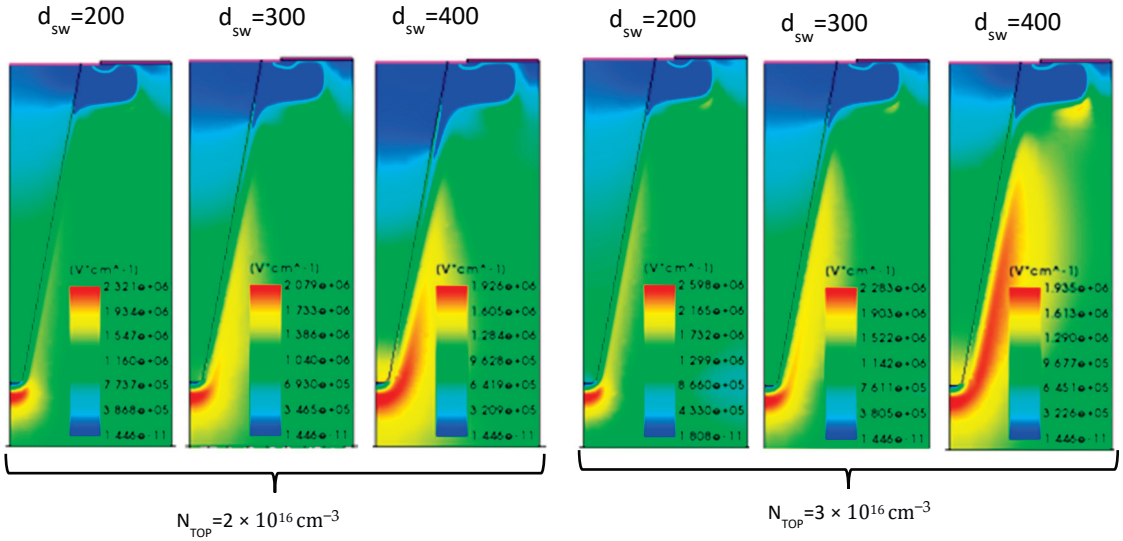


Figure 7. Electric field distribution at 2 kV, varying the N_{TOP} and sidewall depth for the PSSJ. The sidewall doping concentration corresponds to the optimal BV value for each case.

Table 2 reports an overview of the performance of this planar semi-superjunction design, including percentage variations relative to the benchmark planar structure. The optimal trade-off is observed in Case 2, with a BV of 4101 V and an $R_{DS\text{-}ON}$ of 8.7 mΩ·cm^2, improving the performance of the benchmark by 2.5% and 48.7%, respectively.

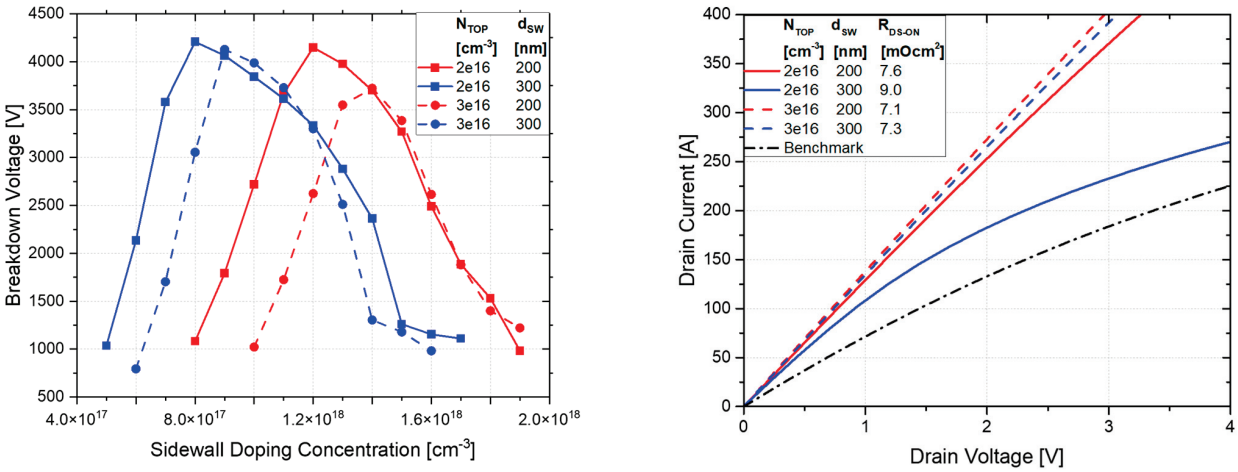
Table 2. Performance overview of the PSSJ and percentage variation relative to the benchmark.

Case	*N*-Top Layer Doping Concentration [cm^{-3}]	d_{SW} [nm]	BV [V]	$R_{DS\text{-}ON}$ [mΩ·cm^2]
1	2×10^{16}	200	3864 (−3.4%)	8.2 (−54.2%)
2		300	4101 (+2.5%)	8.7 (−48.7%)
3		400	3951 (−1.2%)	10.5 (−30.6%)
4	3×10^{16}	200	3003 (−28.7%)	7.8 (−58.8%)
5		300	3686 (−8.1%)	8.2 (−54.2%)
6		400	3752 (−6.4%)	9.0 (−45.5%)

3.2. Trench Semi-Superjunction

The BV versus the sidewall peak doping concentration for the trench gate semi-superjunction design is reported in Figure 8a. Similar trends to the planar structure are observed, but the reduced pitch in the trench design enables higher BV values across a

broader range of design parameter combinations. More specifically, the benchmark values are exceeded for most parameter combinations. The best BV value occurs again at a doping concentration of 2×10^{16} cm^{-3} with a sidewall depth of 300 nm, resulting in a BV of 4206 V, which improves the value of the benchmark by 5.0%.



(**a**) (**b**)

Figure 8. TSSJ performance. (**a**) Analysis of the breakdown voltage versus sidewall peak doping concentration, varying N_{TOP} (solid line 2×10^{16} cm^{-3}, dotted line 3×10^{16} cm^{-3}) and sidewall depth (red 200 nm, blue 300 nm, green 400 nm) for the vertical SSJ. (**b**) On-state characteristics and $R_{DS\text{-}ON}$, varying N_{TOP} and sidewall depth for the TSSJ. The sidewall doping concentration is set to the values that provide the best charge balance for each combination of N_{TOP} and d_{SW}.

The reduced pitch between the trenches further enhances electric field management, allowing for a higher BV. The reduction in SJ *n*-pillar width allows for better SJ charge balancing (towards the bottom of the SJ trench). The incorporation of a *p*-well below the gate trench shifts the EF peak away from the oxide, enhancing gate reliability and reducing the risk of oxide breakdown. As a result, the smaller cell pitch reduces the maximum EF compared to the PSSJ structure, further improving the electric field profile at 2 kV, as shown in Figure 9.

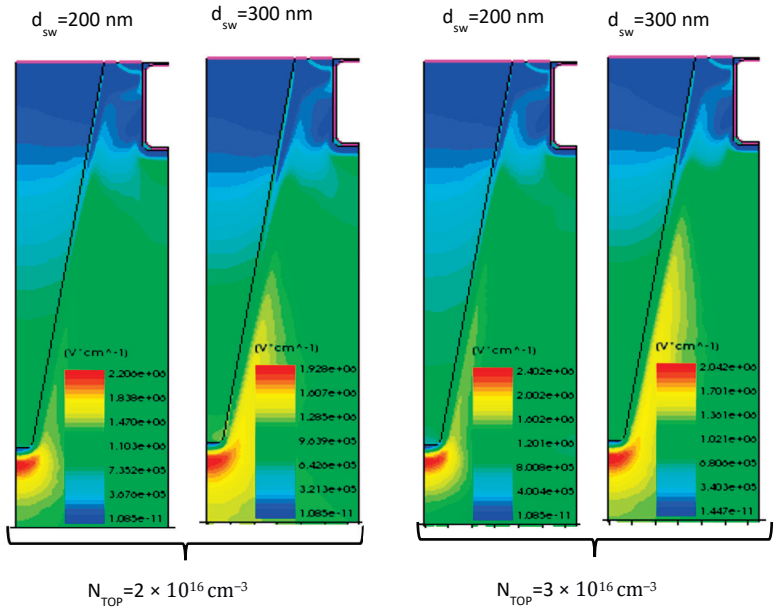


Figure 9. Electric field distribution at 2 kV, varying N_{TOP} and sidewall depth for the TSSJ. The sidewall doping concentration corresponds to the optimal BV value for each case.

The trench design also significantly enhances on-state conduction in certain cases, achieving much better performance compared to the standard planar and planar gate SSJ structures. Figure 8b presents the on-state characteristics and the corresponding $R_{DS\text{-}ON}$. The lowest $R_{DS\text{-}ON}$ value is 7.1 mΩ·cm^2 (67.3% lower than the benchmark), obtained with a doping concentration of the *n*-top layer of 3×10^{16} cm^{-3} and sidewall depth of 200 nm.

For lower *n*-top layer doping concentrations (e.g., 2×10^{16} cm^{-3}), the depletion region becomes excessively large for deeper sidewall dopings, hindering current conduction between the gate trench and the deep SJ trenches. In other words, the current path between the *p*-sidewall and the *p*-ring area becomes very narrow, obstructing the current flow, as shown in Figure 10. This narrow path limits carrier mobility and increases resistance. Thus, optimizing the trench width and sidewall depth is crucial for balancing $R_{DS\text{-}ON}$ and BV. According to this, a sidewall doping depth of 400 nm is not considered for this design to prevent worsening conduction performance. The cell pitch is determined according to the resulting JFET resistance, ensuring that the trench dimensions support efficient conduction without compromising breakdown performance. A summary of the performance of the trench structure is provided in Table 3. The best trade-off for the trench gate design is obtained in Case 4, with a BV of 4127 V and an $R_{DS\text{-}ON}$ of 7.3 mΩ·cm^2, improving the benchmark by 3.1% and 64.8%, respectively.

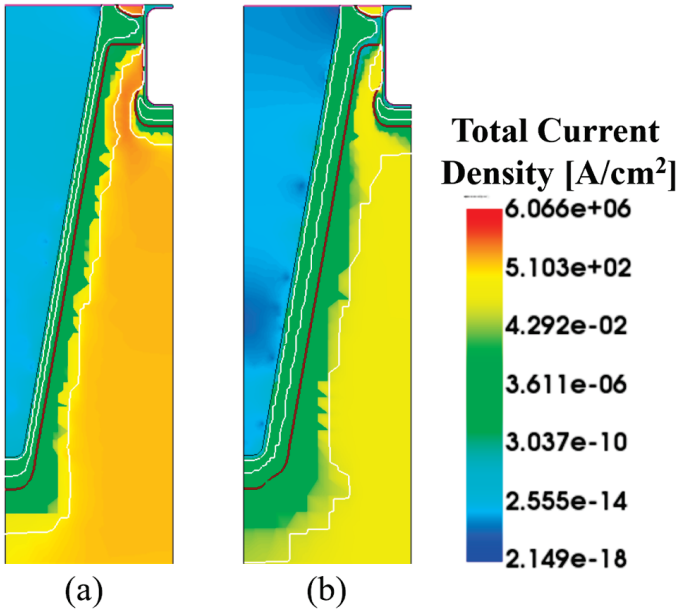


Figure 10. Total current density path for an *n*-top layer doping concentration of 3×10^{16} cm^{-3} and (**a**) d_{SW} = 200 nm; and (**b**) d_{SW} = 400 nm. In the figure is highlighted the junction line (black lines).

Table 3. Performance overview of the TSSJ and percentage variation relative to the benchmark.

Case	*N*-Top Layer Doping Concentration [cm^{-3}]	d_{SW} [nm]	BV [V]	$R_{DS\text{-}ON}$ [mΩ·cm^2]
1	2×10^{16}	200	4148 (+3.6%)	7.6 (−61.2%)
2		300	4206 (+5.0%)	9.0 (−45.5%)
3	3×10^{16}	200	3722 (−7.2%)	7.1 (−67.3%)
4		300	4127 (+3.1%)	7.3 (−64.8%)

3.3. The Graded Approach

As the width of the *n*-SJ layer near the trench varies due to the trench inclination, to perfectly balance the charge alongside the tilted trench, the *n*-top layer doping concentration should decrease as the *n*-width increases to maintain a constant charge density all across. This approach addresses the issue of unbalanced charges along the tilted trench by compensating for the varying widths of the *n*-region. In areas where the *n*-width is greater, the doping concentration is reduced to prevent excessive charge accumulation, while in narrower sections, the *n*-doping concentration is increased to ensure sufficient charge balance.

A simple and feasible approach to achieve this graded doping profile is to divide the *n*-top layer into several sections, each with a different doping concentration. This method is straightforward because different doping profiles can be easily achieved through multiple epitaxial growth steps at the initial drift epi growth stage, allowing for more precise control of the charge distribution between the *p*- and *n*-regions.

By tailoring the doping levels to the varying widths of the *n*-region, the graded approach can effectively balance the charge, enhancing the overall performance and reliability of the tilted trench SSJ design.

To explore the effectiveness of this graded approach, a simulation was performed on the PSSJ considering a sidewall depth of 300 nm and a peak *p*-doping concentration of 1×10^{18} cm^{-3}, which were found to be the optimal parameters for the constant *n*-top layer case. The *n*-top layer was divided into four sections, with doping concentrations of 5.0×10^{16} cm^{-3}, 2.5×10^{16} cm^{-3}, 2.1×10^{16} cm^{-3}, and 1.7×10^{16} cm^{-3}. The resulting doping profile is reported in Figure 11.

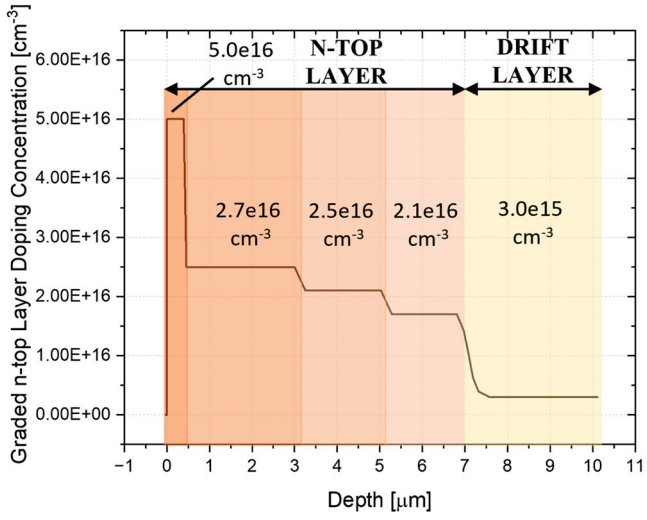


Figure 11. Graded *n*-top layer doping concentration.

The simulation showed a BV of 4055 V and an $R_{DS\text{-}ON}$ of 8.2 mΩ·cm^2. Therefore, the BV remains high (>4 kV), and the graded approach results in a further 6% improvement in $R_{DS\text{-}ON}$. An overview of the performance of all the analyzed designs is reported in Table 4. These results suggest that there is potential for further optimization by tuning the number of zones, their extension, and their doping concentration.

However, the graded approach might not be suitable for trench designs due to the presence of the *p*-ring, an external element that further disturbs charge balance. The *p*-ring complicates the implementation of a precise doping gradient, as it introduces additional variability in the electric field and charge distribution. Consequently, while the graded

approach shows promise for the PSSJ design, its applicability to trench-based designs may be limited.

Table 4. General performance overview and percentage variation relative to the benchmark.

Design	BV [V]	$R_{DS\text{-}ON}$ [mΩ·cm^2]
Benchmark	4000 (−)	14.3 (−)
PSSJ	4101 (+2.5%)	8.7 (−48.7%)
TSSJ	4127 (+3.1%)	7.3 (−64.8%)
Graded PSSJ	4055 (+1.4%)	8.2 (−54.2%)

4. Conclusions

This paper presents a detailed analysis of 3.3 kV SiC MOSFETs utilizing a tilted trench semi-superjunction design, demonstrating a cost-effective approach to improving device performance. Through TCAD simulations, we demonstrated the advantages of this design over conventional planar structures, showing an enhanced breakdown voltage and reduced on-state resistance. For the planar gate SSJ design, the best trade-off between on-state and blocking performance was achieved with a *p*-sidewall doping depth of 300 nm and a JFET *n*-top layer concentration of 2×10^{16} cm^{-3}, resulting in improvements of 2.5% in the BV and 48.7% in the $R_{DS\text{-}ON}$ compared to the benchmark. In the trench gate SSJ design, the trade-off was further optimized, with improvements over the benchmark of 3.1% for BV and 64.8% for $R_{DS\text{-}ON}$.

Additionally, the graded approach was explored by dividing the *n*-top layer into four zones, each with a different constant doping concentration. This method provided a further improvement of 6% in $R_{DS\text{-}ON}$ for the planar gate design without adding any significant fabrication complexity. These findings suggest that tilted trench SSJ designs offer a promising strategy for enhancing the performance and reliability of SiC MOSFETs, making them well suited for demanding power electronic applications.

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Analyzing the Impact of Gate Oxide Screening on Interface Trap Density in SiC Power MOSFETs Using a Novel Temperature-Triggered Method

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Abstract: This work introduces a novel temperature-triggered threshold voltage shift (T3VS) method to study the energy-dependent D_{it} distribution close to the conduction band edge in commercial 1.2 kV 4H-SiC MOSFETs with planar and trench gate structures. Traditional D_{it} extraction methodologies are complicated and require sophisticated instrumentation, complex analysis, and/or prior information related to the device design and fabrication, which is generally unavailable to the consumers of commercial devices. This methodology merely utilizes the transfer characteristics of the device and is straightforward to implement. The D_{it} analysis using the T3VS method shows that trench devices have significantly lower D_{it} in comparison to the planar devices, making them more reliable and efficient in practical applications. Furthermore, this study examines the impact of a novel room temperature gate oxide screening methodology called screening with adjustment pulse (SWAP) on the D_{it} distribution in commercial planar MOSFETs, utilizing the proposed T3VS method. The result demonstrates that the SWAP technique is aggressive in nature and can introduce new defect states close to the conduction band edge. Hence, additional care is needed during screening optimization to ensure the reliability and usability of the screened devices in the consequent applications.

Keywords: temperature-triggered threshold voltage shift method; interface trap distribution; gate oxide screening; SiC MOSFETs; planar vs. trench; cryogenic and high temperature

1. Introduction

Silicon carbide metal oxide semiconductor field-effect transistors (SiC MOSFETs) are gaining attention for a diverse range of applications in energy, automotive, and industrial sectors due to their excellent material properties such as wide bandgap, high thermal conductivity, and superior breakdown characteristics. SiC power MOSFETs with planar gate structures were commercialized in 2011 [1] and continued to dominate the market. However, devices with asymmetric and double trench [1,2] gate designs are gaining prominence due to their enhanced channel mobility [1] and superior short circuit withstand time [2]. In reality, trench MOSFETs exhibit considerable reliability concerns attributable to their design and manufacturing process. At the trench corner, electric field crowding happens under high gate bias, leading to the degradation of the gate oxide reliability [3].

Additionally, the gate oxide in trench MOSFETs is deposited instead of being thermally grown like in planar MOSFETs, affecting the quality of the oxide [2]. The gate oxide processing technique affects the variability in the interface state density (D_{it}) at the SiC/SiO_2 interface. The D_{it} in SiC MOSFETs is almost two orders of magnitude higher compared to their Si counterparts [4], which poses both performance and reliability concerns. First, the inversion channel mobility of SiC devices is still in the range of 30–50 cm^2/V-s [5–7], almost one order lower compared to the Si devices (>200 cm^2/V-s). Additionally, the high D_{it} leads to threshold voltage instability [8–10], jeopardizing the reliability of the device during operation.

On the other hand, the high density of extrinsic defects such as pits and holes, along with contamination in the oxide [11], poses significant issues in gate oxide reliability. The existence of these defects leads to high localized electric fields and/or increased current density within the gate oxide, as discussed in the oxide thinning model, leading to premature failure in the field [11,12]. As a result, proper screening needs to be implemented to effectively eliminate devices with poor gate oxide quality. Shi et al. [3] have demonstrated a high-voltage and high-temperature-based screening technique that can remove defective devices with negligible degradation in static characteristics such as threshold voltage (V_{th}) and intrinsic lifetime of the non-defective devices. But this methodology is limited to a screening oxide field (E_{screen}) of <9 MV/cm for a screening time (t_{screen}) of 100 ms–1 s to prevent a significant negative shift in V_{th} due to charge trapping [3,13,14], which reduces the screening efficiency. Jin et al. [15] have proposed a novel room temperature screening method called screening with adjustment pulse (SWAP) that employs an $E_{screen} \geq 9$ MV/cm for a t_{screen} of 10 s followed by an adjustment pulse (E_{adj}) of 8 MV/cm. This SWAP approach facilitates recovering the negative V_{th} shift due to the high E_{screen} by releasing the trapped holes while applying the E_{adj} pulse. This method allows for more aggressive screening with higher screening efficiency without the need for high temperature.

One of the towering concerns related to the SWAP technique is the potential introduction of the additional interface states close to the conduction band edge as a consequence of the high gate oxide fields. As the presence of the interface states affects both the reliability and performance of SiC MOSFETs [16], multiple studies have been carried out to extract the energy-dependent D_{it} profile, especially close to the conduction band edge, by employing different techniques such as thermal dielectric relaxation current (TDRC) and isothermal dielectric relaxation current (IDRC) [7,17,18], capacitance and conductance [6,19,20], thermally simulated current [21,22], subthreshold slope [23], and subthreshold hysteresis [24,25], or an amalgamation of two or more techniques. The standard capacitance-based D_{it} extraction method, commonly referred to as the high–low method [6,26], is the most dominant among many methodologies. Nevertheless, it lacks the sensitivity to identify fast interface states. The sensitivity of D_{it} extraction techniques can be enhanced by employing high-frequency input, low temperature, or equipment with extremely low-noise floors, or a combination of all of the above. Nevertheless, these procedures frequently exhibit limited adaptability and generally necessitate extremely sensitive apparatuses and/or intricate measurement and extraction processes [6].

In this paper we have proposed a novel and straightforward D_{it} extraction technique, called the temperature-triggered threshold voltage shift (T3VS) method, which has been further verified using commercial 1.2 kV 4H-SiC power MOSFETs with planar and trench gate structures. In this technique, a D_{it} distribution very close to the conduction band edge can be extracted by monitoring the variation in gate voltage with temperature at a constant drain current of 1 μA in a broad temperature range of 30 K to 450 K. Furthermore, this method is viable without needing the detailed knowledge of the device design or

fabrication parameters. By utilizing the novel D_{it} extraction methodology, this paper then examines the impact of the SWAP approach on the interface state density near the conduction band edge in commercial 1.2 kV planar SiC power MOSFETs.

2. Mathematical Analysis of the Temperature-Triggered Threshold Voltage Shift (T3VS) Method

In order to evaluate the energy-dependent D_{it} at the SiC/SiO_2 interface by utilizing the T3VS method, first the effect of temperature on threshold voltage (V_{th}) needs to be examined. Figure 1 shows the transfer characteristics of a planar MOSFET from Vendor F at T = 30 K (black curve) and T = 450 K (red curve) under a constant drain voltage (V_{ds}) of 100 mV.

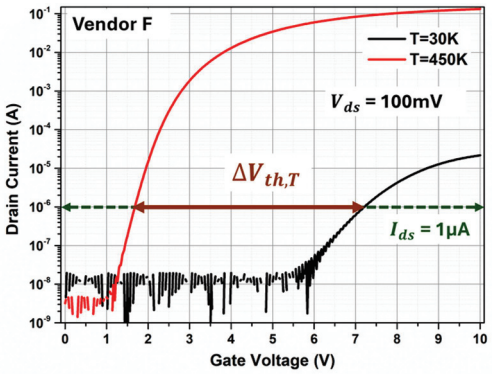

Figure 1. Transfer characteristics of Vendor F at T = 30 K and T = 450 K.

V_{th} can be extracted by measuring the gate voltage (V_{gs}) at a constant drain current (I_{ds}) of 1 μA. Mathematically, V_{th} can be written as [27],

$$V_{th} = 2\varphi_F + \varphi_{SS} + \frac{\sqrt{4q\epsilon_s\varphi_F N_A}}{C_{ox}} - \frac{Q_{it}}{C_{ox}} - \frac{Q_F}{C_{ox}} \quad (1)$$

where φ_F is the Fermi potential, φ_{SS} is the Si-SiC work function difference, q is the elementary charge, N_A is the acceptor concentration, ϵ_s is the permittivity of silicon carbide, C_{ox} is the oxide capacitance per unit area, Q_F is the fixed oxide charge per unit area, and Q_{it} is the interface trap charge per unit area.

As the temperature reduces, the Fermi level (E_F) moves closer to the valence band (E_v) in the p-bulk, increasing the φ_F [27]. The change in φ_F and bandgap (E_g) with temperature cumulatively affects the first three terms of (1) and has been found to be ~0.2 V [18] for different commercial SiC power MOSFETs.

By neglecting the effect of temperature change on Q_F, the change in V_{th} due to temperature ($\Delta V_{th,T}$) can be described as

$$\Delta V_{th,T} \sim \frac{\Delta Q_{it}}{C_{ox}} = \frac{q\Delta N_{it}}{C_{ox}} \quad (2)$$

where ΔN_{it} represents the change in the number of interface traps per unit area and can be expressed as

$$\Delta N_{it} = \int_{\varphi_{F,HT}}^{\varphi_{F,LT}} D_{it}(\varphi_F)d\varphi_F \quad (3)$$

Combining (2) and (3) we obtain

$$\Delta N_{it} = \int_{\varphi_{F,HT}}^{\varphi_{F,LT}} D_{it}(\varphi_F) d\varphi_F = \frac{\Delta V_{th,T} C_{ox}}{q} \tag{4}$$

The energy distribution of the traps can be calculated as

$$(E_{cs} - E_T) = \frac{E_g}{2} - q(\varphi_s - \varphi_F) \tag{5}$$

where $(E_{cs} - E_T)$ is the position of the trap level relative to the conduction band edge at the surface and φ_s is the surface potential within the range $\varphi_F < \varphi_s < 2\varphi_F$. The distribution of D_{it} ($eV^{-1}cm^{-2}$) with the variation in $E_{cs} - E_T$ (eV) can be extracted using (4) and (5).

3. Experimental Methodologies

3.1. Device Information

In this work, commercial 1.2 kV 4H-SiC MOSFETs with planar and trench gate structures were tested for D_{it} extraction. In order to study the effect of SWAP on D_{it}, planar MOSFETs from Vendor F were considered. Prior to screening and D_{it} experiments, a high-temperature (150 °C) gate oxide ramp-to-breakdown measurement was performed on a small sample from each vendor to estimate the gate oxide thickness (t_{ox}) considering the critical oxide electric field (E_{crit}) of 11 MV/cm [23,28,29]. The detailed information on the DUTs is listed in Table 1.

Table 1. Details of 1.2 kV SiC Power MOSFETs.

Vendor	Structure	Estimated t_{ox} [nm]	Current Rating [A]	On-Resistance [mΩ]
F	Planar	38	7.6	350
D	Planar	45	20	189
B	Asymmetric trench	57.1	4.7	350
G1	Double trench	58.1	17	160
G2	Reinforced double trench	39.6	26	62

3.2. Experimental Methodology to Determine D_{it}

To determine D_{it} distribution close to the conduction band edge using the T3VS method, DUTs were subjected to a large temperature variation of 30 K to 450 K. The low-temperature measurements (30 K–300 K) were carried out using a Lakeshore CCS-400/202 Cryostat (Lake Shore Cryotronics, Inc., Westerville, OH, USA). The DUT was maintained at a vacuum level of 0.1 mTorr while cooling inside the cryostat. High-temperature measurements (300 K–450 K) were conducted in a DX302 Yamato natural convection oven (Yamato Scientific Co. Ltd., Tokyo, Japan). Transfer characteristics were measured by using a Keysight B1506A Power Device Analyzer (Keysight Technologies, Colorado Springs, CO, USA). All measurements were performed once the temperature settled within 0.1 K of the target value.

3.3. SWAP Methodology

The gate oxide screening using SWAP methodology [15] for Vendor F was carried out at room temperature by utilizing a Keysight B1506A Power Device Analyzer (Keysight Technologies, Colorado Springs, CO, USA). The measurement methodology is graphically represented in Figure 2. At each step, the V_{th} of the DUT was measured at a constant drain current of I_{ds} = 1 mA. As a first step, each DUT was tested to determine $V_{th,pre}$. Then a screening pulse (E_{screen}) was applied for a time t_{screen}, followed by an adjustment pulse

(E_{adj}) for time t_{adj}. The voltage corresponding to the electric field (for example, V_{screen} related to E_{screen}, or V_{adj} related to E_{adj}) was calculated by multiplying the electric field with the t_{ox} of the device.

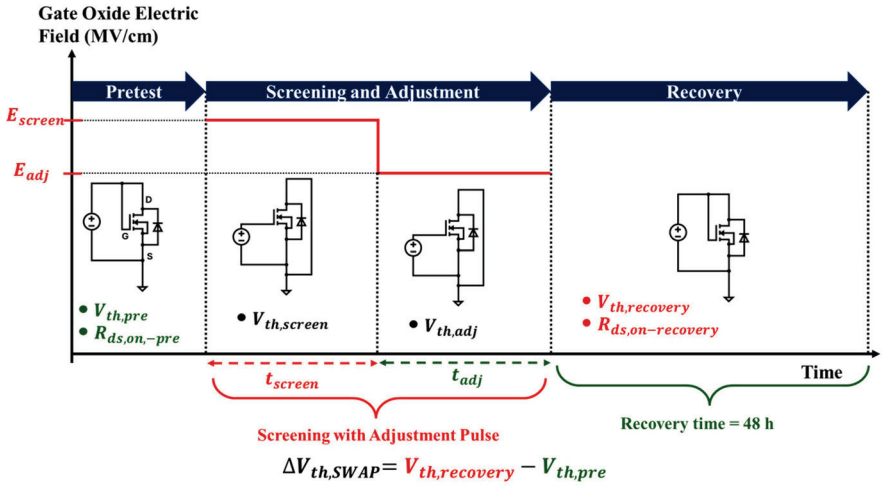

Figure 2. Test procedure of the SWAP methodology.

The measured threshold voltage after E_{screen} is called $V_{th,screen}$ and after E_{adj} is termed as $V_{th,adj}$. As a final step, the DUT was left to recover for 48 h at room temperature, and the threshold voltage after recovery ($V_{th,recovery}$) was then measured. The threshold voltage shift due to the SWAP screening ($\Delta V_{th,SWAP}$) and percentage of threshold voltage shift ($\%V_{th,SWAP}$) can be defined as

$$\Delta V_{th,SWAP} = V_{th,recovery} - V_{th,pre} \tag{6}$$

$$\%V_{th,SWAP} = (\Delta V_{th,SWAP}/V_{th,pre}) \times 100\%. \tag{7}$$

The effect of SWAP screening on the on-resistance ($R_{ds,on}$) of each DUT was monitored by measuring $R_{ds,on}$ at V_{gs} = 20 V and V_{ds} = 1.5 V. The on-resistance shift due to screening ($\Delta R_{ds,on-SWAP}$) and $\%\Delta R_{ds,on-SWAP}$ is defined as

$$\Delta R_{ds,on-SWAP} = R_{ds,on-recovery} - R_{ds,on-pre} \tag{8}$$

where $R_{ds,on-pre}$ is the pretest on-resistance and $R_{ds,on-recovery}$ is the on-resistance of the device after screening and 48 h of recovery.

$$\%\Delta R_{ds,on-SWAP} = (\Delta R_{ds,on-SWAP}/R_{ds,on-pre}) \times 100\% \tag{9}$$

4. Results and Discussion

4.1. D_{it} Extraction of Commercial 1.2 kV 4H-SiC MOSFETs Using T3VS Technique

This section shows the energy-dependent D_{it} distribution of commercial 1.2 kV 4H-SiC MOSFETs with planar and trench gate structures close to the conduction band edge, extracted using the T3VS method. Since this methodology is based on the V_{th} shift as a function of temperature as shown in (2), the baseline V_{th} and corresponding baseline D_{it} profile as a function of $(E_{cs} - E_T)$ need to be established at a baseline temperature ($T_{baseline}$). In this analysis, we have considered $T_{baseline}$ = 450 K. The subsequent investigation has been discussed below.

4.1.1. Effect of Temperature on V_{th} of the DUTs

Figure 3a shows the variation in V_{th} extracted at I_{ds} = 1 µA with respect to temperature (T) for all the DUTs. By considering the V_{th} at $T_{baseline}$ = 450 K as the baseline value, the shift in threshold voltage due to temperature ($\Delta V_{th,T}$) can be defined as

$$\Delta V_{th,T} = V_{th,T} - V_{th,450K} \tag{10}$$

where $V_{th,T}$ is the threshold voltage measured at a given temperature in K.

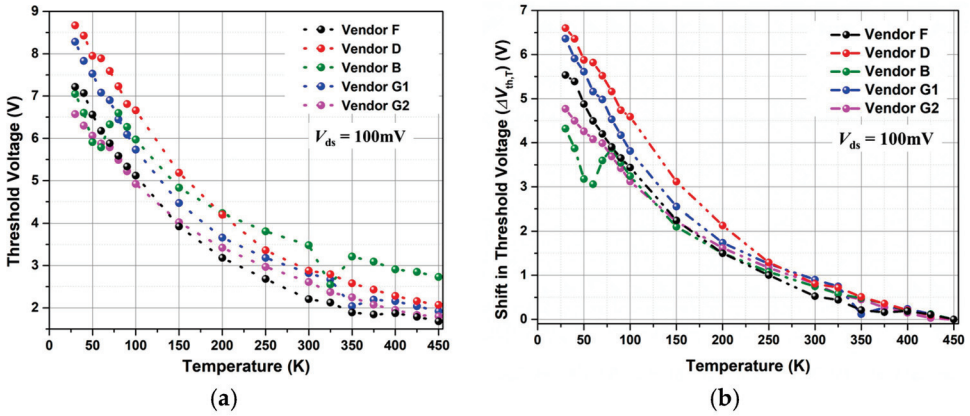

Figure 3. Variation in (**a**) threshold voltage and (**b**) $\Delta V_{th,T}$ as a function of temperature for all vendors.

The variation in $\Delta V_{th,T}$ for all the DUTs as a function of temperature is shown in Figure 3b. This large shift in threshold voltage (for example, $\Delta V_{th,30K}$ = 5.534 V for Vendor F) cannot be accounted for only by the temperature dependency of φ_F and E_g. Utilizing theoretical understanding [30] and considering $N_A = 2 \times 10^{17}/\text{cm}^3$ [27], the variation in φ_F and E_g as a function of temperature has been calculated and shown in Figure 4. It can be clearly seen that the maximum shift in φ_F and E_g is ~0.25 eV and 0.07 eV, respectively, when the temperature shifts from 450 K to 30 K.

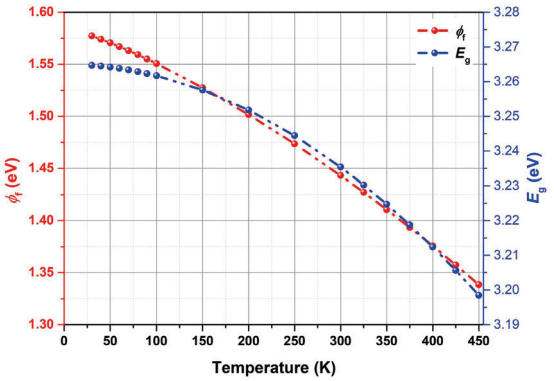

Figure 4. Variation in φ_F and E_g with temperature considering $N_A = 2 \times 10^{17}/\text{cm}^3$.

4.1.2. Baseline D_{it} Profile Extraction

As a next step, the baseline D_{it} profile was evaluated at $T_{baseline}$ = 450 K by using the subthreshold region of the transfer characteristics [23] of the DUT at 450 K and is termed as $D_{it,450K}$. The methodology is discussed below.

The subthreshold region drain current

$$I_{DS} = I_0 e^{\frac{qV_{gs}}{nkT}} \left(1 - e^{\frac{qV_{ds}}{kT}}\right) \tag{11}$$

and the ideality factor n is given as

$$n = \frac{q}{2.3kT}\left(\frac{\partial log I_{DS}}{\partial V_{gs}}\right)^{-1} = 1 + \frac{C_D + C_{it}}{C_{ox}} \tag{12}$$

where C_D is the depletion capacitance, C_{ox} is the oxide capacitance, and C_{it} is the interface trap capacitance per unit area.

The energy-dependent interface trap density is given as

$$D_{it} = \frac{C_{it}}{q} \tag{13}$$

and the energy distribution of the trap level $(E_{cs} - E_T)$ is

$$E_{cs} - E_T = \frac{E_g}{2} - q\left(\varphi_F - \frac{2.3kT}{q}\log\left[\frac{I_{DS}(2\varphi_F)}{I_{DS}(\varphi_s)}\right]\right) \tag{14}$$

where the surface potential (φ_s) is in the range of $\varphi_F < \varphi_s < 2\varphi_F$, and φ_F is the Fermi potential.

Using (13) and (14), $D_{it,450K}$ has been extracted for Vendor F and shown in Figure 5 (inset). Using the baseline $D_{it,450K}$ along with (4) and (5), the energy-dependent D_{it} distribution profile very close to the conduction band edge ($(E_{cs} - E_T) \sim 0.05$ eV) has been determined for Vendor F and is presented in Figure 5.

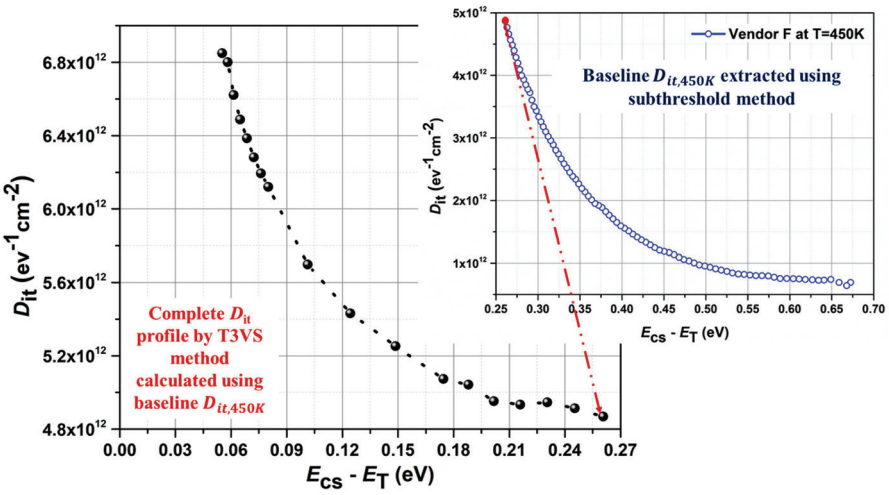

Figure 5. D_{it} profile as a function of $(E_{cs} - E_T)$ extracted using the proposed T3VS method for Vendor F. The baseline D_{it} profile extracted at $T_{baseline}$ = 450 K using the subthreshold method [23] is shown in the inset. The red line correlates the $D_{it,450K}$ with the complete D_{it} profile.

The extracted D_{it} profile, as shown in Figure 5, agrees with the previously reported D_{it} profiles close to the conduction band edge in SiC/SiO_2 systems [19,31], demonstrating this technique is both appropriate and reliable for use in commercial 1.2 kV SiC MOSFETs. Therefore, similar analysis was carried out for all the vendors, and the D_{it} distribution profile as a function of $(E_{cs} - E_T)$ has been extracted and shown in Figure 6. It can be seen that devices with planar gate structures (red and black curves) show higher D_{it} compared to devices with trench gate structures (pink, blue, and green curves). As a result, trench devices exhibit higher carrier density in the channel region [1]. Furthermore, the lower D_{it} very close to the conduction band edge ($(E_{cs} - E_T) \sim 0.05$ eV) for trench devices results in improved channel mobility and threshold voltage stability, making them more attractive

for real-world applications. Although this method is suitable to extract trap distribution very close to the conduction band edge, it fails to provide any information related to the trap properties, trap parameters such as thermal activation energy, capture cross section, or the origin of the trap states.

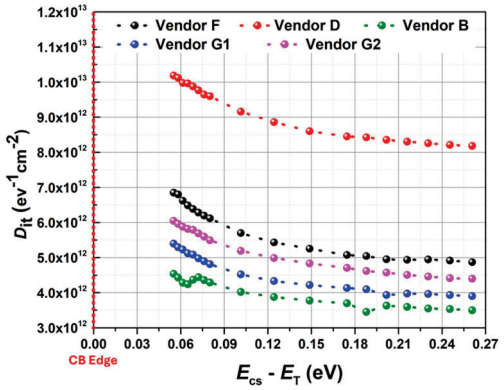

Figure 6. The extracted D_{it} profile as a function of $(E_{cs} - E_T)$ for all the vendors.

4.2. Effect of SWAP on D_{it} Distribution

To study the effect of screening on interface state density close to the conduction band edge in commercial devices using the T3VS method, a small batch of devices from Vendor F were subjected to the SWAP screening method followed by the D_{it} analysis. The D_{it} profile of the screened devices was compared with an unscreened one from the same batch with the same part and lot number, and the results are discussed below.

For the SWAP screening, we have applied the highest possible E_{screen} = 10 MV/cm for t_{screen} = 10 s, followed by an E_{adj} = 8 MV/cm for t_{adj} = 2 s [15], and the variation in V_{th} at each step has been measured and displayed in Figure 7a. The variation in $\%\Delta V_{th,SWAP}$ and $\%\Delta R_{ds,on-SWAP}$ has been calculated using (7) and (9), respectively, and shown in Figure 7b. It is evident that the maximum shifts in $\%\Delta V_{th,SWAP}$ and $\%\Delta R_{ds,on-SWAP}$ are 12.9% and 2.47%, respectively, for D1. Although the shift in on-resistance is within the permissible limit of ±5% [15] of their initial value, the shift in threshold voltage is significant.

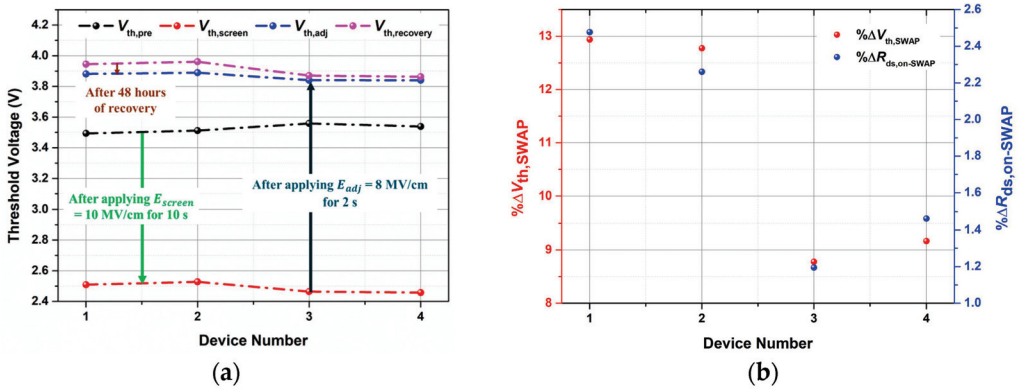

Figure 7. (**a**) The variation in threshold voltage during the SWAP process; (**b**) The percentage shift in threshold voltage and on-resistance due to the SWAP process.

This substantial shift in threshold voltage can be attributed to either a significant number of electrons injected and subsequently trapped in the gate oxide or the creation of new interface defect states [32] during the SWAP screening process. The increase of threshold voltage has also raised the on-resistance as shown in Figure 7b. The effect of SWAP screening on the interface states has been further studied by comparing the D_{it}

profiles of the screened devices with respect to the D_{it} profile of an unscreened device from the same vendor with the same part and lot number using the novel T3VS method as shown in Figure 8.

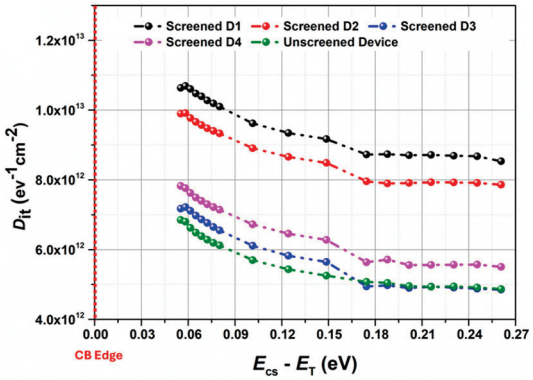

Figure 8. Extracted D_{it} profile as a function of $(E_{cs} - E_T)$ for screened (black, red, pink, and blue curve) and unscreened (green curve) devices from Vendor F.

It can be clearly seen that device D1, with the highest $\%\Delta V_{th,SWAP}$ and $\%\Delta R_{ds,on-SWAP}$, results in maximum degradation of the interface by introducing new defect states close to the conduction band edge, i.e., 0.05 eV $\leq (E_{cs} - E_T) \leq$ 0.26 eV. In order to better understand the degradation of the interface state due to SWAP screening, the change in the number of traps (ΔN_{it}) has been further calculated and is presented below.

Figure 9 shows the variation in the extracted ΔN_{it} for all the screened devices from Vendor F. It can be clearly seen that the increase in the total number of traps is significant ($\sim 10^{11}/\text{cm}^2$) under all the screening conditions. Therefore, it is possible to assert that the substantial alteration in threshold voltage is mostly attributed to the emergence of new defect states near the conduction band edge, which further prevents the restoration of the devices to their pristine state and hence affects their usability in ensuing applications. Moreover, it can be inferred that to implement the SWAP screening method on an industrial scale, the screening conditions need to be calibrated extremely carefully to prevent the formation of new defect states close to the conduction band edge so that the screened devices can be subsequently implemented in real-world applications.

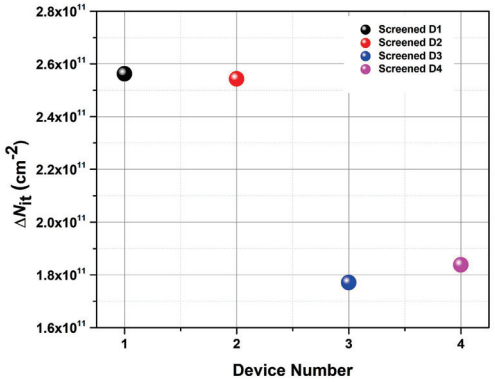

Figure 9. Extracted ΔN_{it} for screened devices from Vendor F.

5. Conclusions

This paper introduces a novel and simple temperature-triggered threshold voltage shift (T3VS) method to study the interface state density close to the conduction band edge in 1.2 kV 4H-SiC power MOSFETs with planar and trench gate structures. This

approach solely uses the transfer characteristics of the MOSFETs, making it incredibly straightforward to employ. Furthermore, no prior information related to the device design or fabrication process is needed to implement this technique. Then, this work studies the effect of a novel room temperature gate oxide screening methodology known as the SWAP technique in light of the interface defect state analysis. The D_{it} analysis on unscreened and screened planar devices from Vendor F further reveals that the SWAP screening is extremely aggressive in nature and can create new defect states close to the conduction band edge, which will harm the usability of the screened devices. In order to implement SWAP screening in practical scenarios, extreme care needs to be taken during the screening optimization to prevent the generation of any new defect states that could impair the reliability of the devices in real-world applications.

Author Contributions: Conceptualization, M.B., M.H.W. and A.K.A.; methodology, M.B. and M.J.; software, M.B.; validation, M.B., M.J. and H.Y.; formal analysis, M.B., M.J., H.Y., S.H., J.Q., M.H.W., A.S. and A.K.A.; investigation, M.B. and M.J.; resources, M.B. and M.J.; data curation, M.B.; writing—original draft preparation, M.B.; writing—review and editing, M.B., M.J. and H.Y.; visualization, M.B.; supervision, A.K.A.; project administration, A.S.; funding acquisition, A.S. All authors have read and agreed to the published version of the manuscript.

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Abbreviations

The following abbreviations are used in this manuscript:

T3VS	temperature-triggered threshold voltage shift
SWAP	screening with adjustment pulse
MOSFET	metal oxide semiconductor field-effect transistor
DUT	device under test

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A High-Density 4H-SiC MOSFET Based on a Buried Field Limiting Ring with Low Q_{gd} and R_{on}

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Abstract: In this study, we propose an optimized shield gate trench 4H-SiC structure with effective gate oxide protection. The proposed device has a split trench with a P+ shield region, and the P+ shield is grounded by the middle deep trench. Our simulation results show that the peak electric field near the gate oxide is almost completely suppressed. Compared with a conventional P+ shield device, our proposed structure achieves a 78% reduction in the Q_{gd} and a 108% increase in the FoM (figure of merit) simultaneously. Additionally, it is estimated that the device cell pitch can be reduced to 1.8 μm with a R_{on} below 0.94 mΩ·cm^2, in theory. These demonstrated device performance metrics, as well as its simple structure and good compatibility, make our proposed SiC MOSFET highly attractive for future high-performance applications.

Keywords: SiC; high density; gate oxide protection; distributed grounding

1. Introduction

Compared with conventional silicon (Si) material, silicon carbide (SiC) exhibits three fundamental material advantages that are critical for power electronics applications: (1) a wide bandgap (3.26 eV for 4H-SiC vs. 1.12 eV for Si), enabling high-temperature operation up to 600 °C; (2) an exceptionally high critical breakdown field strength (2.8 MV/cm for SiC versus 0.3 MV/cm for Si), allowing thinner drift layers and higher voltage blocking capability; and (3) superior thermal conductivity (4.9 W/cm·K for SiC compared to 1.5 W/cm·K for Si), which significantly improves heat dissipation [1,2].

From a fabrication perspective, the design methodology and processing techniques for SiC metal oxide semiconductor field-effect transistor (MOSFET) devices maintain strong compatibility with established silicon-based MOS device manufacturing flows. This includes similar photolithography processes, oxide deposition techniques, and metallization schemes, thereby facilitating the adoption of SiC MOSFETs as direct replacements for silicon power MOSFETs in existing power electronic systems [3,4].

The current technological roadmap for SiC MOSFET development prioritizes four key performance metrics: (i) the minimization of cell dimensions (targeting sub-micron features to increase the current density); (ii) a reduction in specific on-resistance ($R_{on,sp}$) through optimized doping profiles and channel mobility enhancement; (iii) the lowering of switching losses (E_{off}) via improved minority carrier lifetime control; and (iv) the enhancement of the gate oxide reliability through advanced interfacial passivation techniques [5,6]. Thermal management considerations are becoming increasingly crucial as device densities increase.

In terms of the device architecture, contemporary commercial SiC power MOSFETs predominantly employ either planar or trench gate configurations [7]. The planar topol-

ogy, while offering simpler fabrication and better gate oxide integrity, presents inherent geometrical constraints in minimizing the cell pitch due to the lateral separation required between adjacent JFET regions. In contrast, trench architectures enable more aggressive pitch scaling through vertical channel formation.

A reduction in the cell pitch yields multiple performance benefits: (a) a substantial decrease in the die area (enabling higher current ratings per unit chip size); (b) a lower specific on-resistance ($R_{on,sp}$) through increased channel density; (c) reduced input and output capacitances (C_{iss} and C_{oss}) due to smaller electrode overlaps; and (d) markedly improved switching efficiency, as evidenced by reduced energy losses during both turn-on (E_{on}) and turn-off (E_{off}) transitions [8–10]. Recent studies have demonstrated that every 1 μm reduction in cell pitch can provide an approximate 15–20% improvement in the overall figure of merit (FoM = $R_{on,sp} \times E_{off}$).

Nonetheless, trench SiC MOSFETs encounter certain issues, primarily associated with the gate oxide. Particularly, there exists a strong electric field at the trench bottom, which may give rise to gate oxide premature breakdown [11–13]. Numerous approaches have been proposed to mitigate the electric field based on numerical simulations [14–22]; however, these methods often entail complex structures and pose challenges in terms of process feasibility.

In contemporary SiC MOSFET designs, the self-aligned additional P+ shielding layer is commonly employed to significantly decrease the electric field. However, this approach also leads to an increase in the device's R_{on}, and the presence of a floating P+ region also introduces the issue of the charge storage effect [23,24].

A grounding P+-shield region at the bottom of a trench offers significant benefits, especially in terms of improved gate oxide protection, a well-researched area. However, it is difficult to achieve P+ grounding at the bottom of the trench in both process and device structure, which is currently a research focus of research institutions including Infineon and Rohm. Infineon has addressed this challenge by connecting the shield P+ to a 0 potential through a semi-enclosed trench structure [25]. Nevertheless, this technique results in the wastage of half of the channel area, thereby limiting further advancements in chip density. Rohm adopts a grounded source trench on both sides of each gate trench, which also faces the problem of low integration.

To address these challenges, we present a novel solution in this study: a buried field limiting ring device (P+ shield) grounded through a deep trench. The trench gate structure is divided into three distinct sections and the two side sections serve as conventional gates. Our proposed device fabrication process ensures full compatibility with high-density integration, high breakdown voltage (BV), low R_{on}, and various other advantages.

2. Structure Design and Fabrication Process

Figure 1a,b depict the schematic structures of the proposed and conventional P+ shield 4H-SiC trench gate MOSFETs. And the main structure and process parameters of the device are shown in Table 1. In the proposed device, the trench gate is divided into symmetrical components through the incorporation of a deep trench structure. The deep trench is embedded into the drift region to form a P+ shield grounded channel. As a result, the inverted p-n junction in the OFF state is pushed down into the drift region, effectively confining the depletion region outside the channel region. As a result, the peak electric field near the gate oxide is almost completely suppressed. In comparison to the conventional device, the proposed device maintains identical structures and doping profiles. The 4H-SiC substrate possesses a doping concentration of 7.0×10^{15} cm^{-3} to obtain a BV higher than 1200 V. The normal trench gate depth (1 μm), cell pitch (2.4 μm), total trench

width (1.6 μm), and ion implantation conditions for the P+ shield region are also kept consistent. The doping concentration of the P+ shield and P base are 2×10^{19} cm^{-3} and 2.5×10^{17} cm^{-3}, respectively.

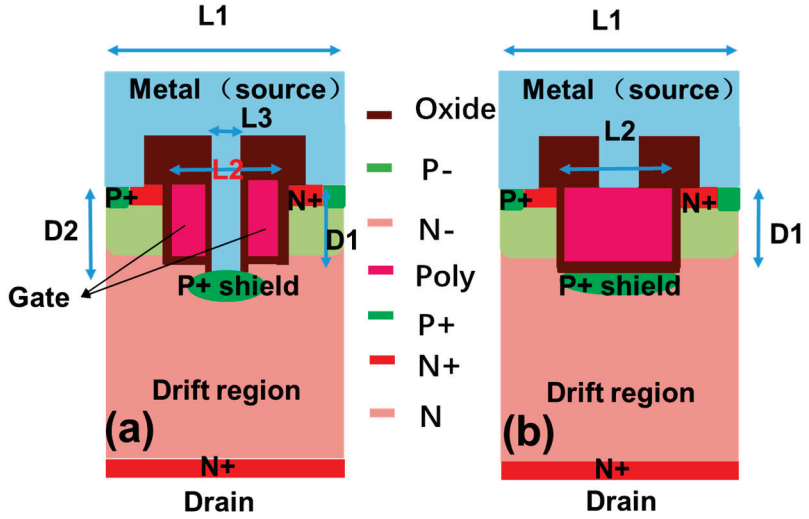

Figure 1. Schematic structure of (**a**) the proposed SiC MOS and (**b**) conventional P+ shield trench SiC MOS.

Table 1. Key device parameters.

Parameter	Proposed	Conventional
Gate oxide thickness (nm)	50	50
Trench gate depth D1 (μm)	1.0	1.0
D2 (μm)	1.2	
N-JFET doping (cm^{-3})	4×10^{16}	4×10^{16}
N-drift doping (cm^{-3})	7×10^{15}	7×10^{15}
N-drift thickness (μm)	10	10
Cell pitch L1 (μm)	2.4	2.4
Trench gate width L2 (μm)	1.6	1.6
L3 (μm)	0.3	

Figure 2 illustrates one available fabrication process for the proposed SiC MOSFET. (a) The N-drift is formed on the N+ substrate using epitaxial techniques, and then, the emitter P+N+ is formed by photolithography (PEP) and ion implantation (ion); (b) oxide deposition, PEP, oxide etching, and SiC etching to form a deep trench; (c) oxide deposition, etching to form side walls, and self-aligned bottom P-well injection; (d) annealing for ion activation and oxide etching; (e) oxide deposition and chemical mechanical polishing (CMP); (f) PEP and oxide etching; (g) SiC etching; (h) thermal oxidation process to form the gate oxide; (i) polysilicon deposition and etching; (j) oxide deposition; (k) PEP and oxide coating etching to form ground channels in the bottom of deep trench; (l) metal deposition.

All of the process steps are compatible with current manufacturing processes and require only one additional lithography mask. The proposed device has advantages of a simple structure and low cost, as the manufacturing cost is mainly related to the duration of lithography.

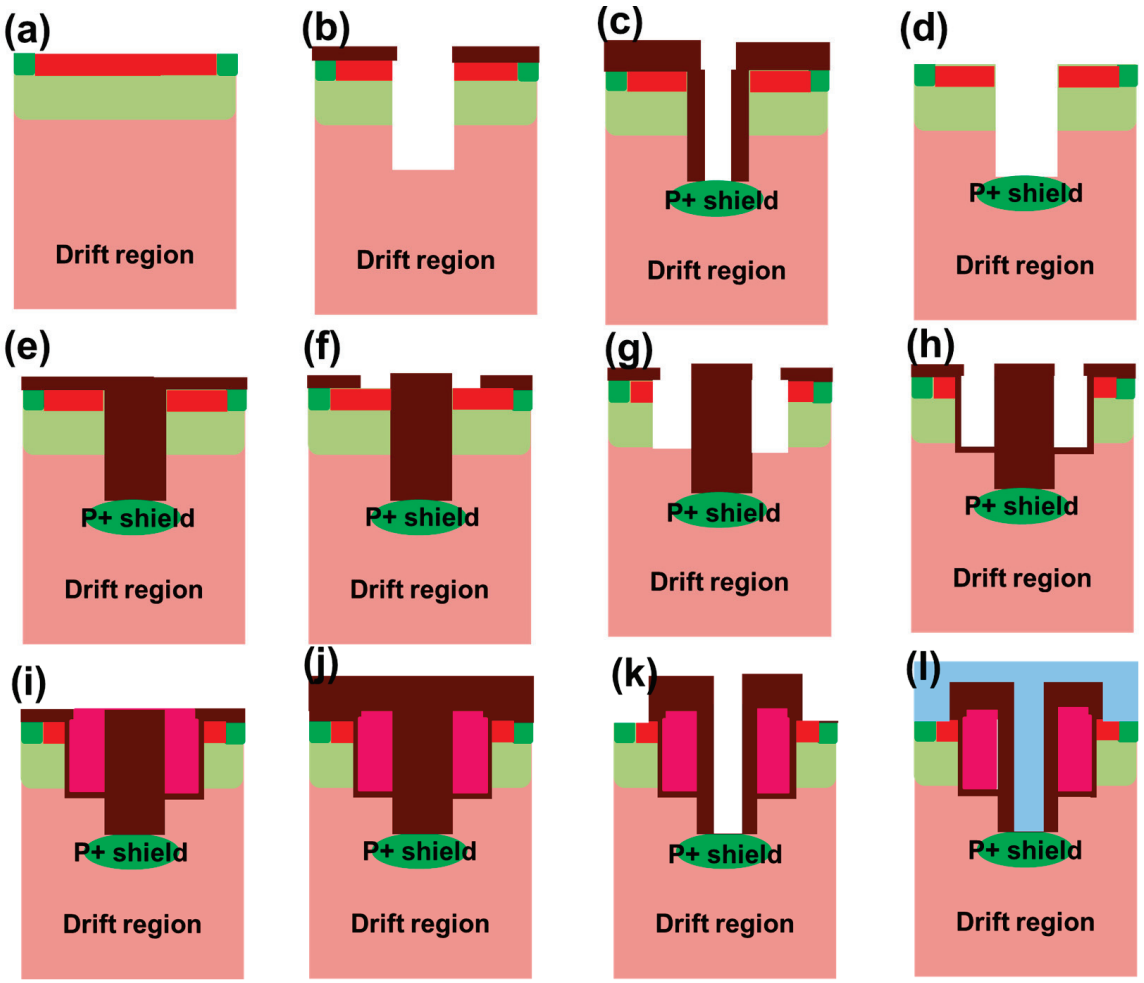

Figure 2. One possible fabrication process for the proposed SiC MOSFET. (**a**) The N-drift is formed on the N+ substrate using epitaxial techniques, and then, the emitter P+N+ is formed by photolithography (PEP) and ion implantation (ion); (**b**) oxide deposition, PEP, oxide etching, and SiC etching to form a deep trench; (**c**) oxide deposition, etching to form side walls, and self-aligned bottom P-well injection; (**d**) annealing for ion activation and oxide etching; (**e**) oxide deposition and chemical mechanical polishing (CMP); (**f**) PEP and oxide etching; (**g**) SiC etching; (**h**) thermal oxidation process to form the gate oxide; (**i**) polysilicon deposition and etching; (**j**) oxide deposition; (**k**) PEP and oxide coating etching to form ground channels in the bottom of deep trench; (**l**) metal deposition.

3. Simulation Results and Discussion

Two-dimensional (2D) simulation models are developed, utilizing the existing SiC MOSFET process as the foundation. The proposed device and conventional devices with and without a P+ shield are chosen to be compared. The crucial models are taken into account, including Shockley–Read–Hall recombination, Auger recombination, Okuto–Crowell impact ionization, incomplete dopant ionization, doping-dependent transport, band narrowing, barrier lowering, anisotropic material properties, non-local tunneling, and so on. The effect of the SiO_2/SiC interface traps is taken into consideration and the charge concentration is 2×10^{11} cm^{-2}. And the channel mobility below the SiC/SiO_2 interface is about 20–50 $cm^2 \cdot V^{-1}s^{-1}$ by modifying the parameters of the Lombardi model.

A. Breakdown characteristics

Figure 3a displays the electric field distributions in the OFF-state (VDS = 1340 V) for the investigated SiC MOSFETs. It is evident that the high-electric-field region primarily resides within the inverted PN junction formed by the P+ region and the drift region,

as the grounded P+ shield effectively diverts the electric field. The electric field at the trench gate corner has a considerably lower value of 0.41 MV/cm, which is well below the acceptable threshold of 3 MV/cm. In contrast, the electric field in the P+ shield region reaches 3.5 MV/cm, which is approximately nine times greater than that at the gate corner, with an ionization rate of about 1.28×10^{19} $cm^{-3}s^{-1}$. Consequently, the proposed device effectively suppresses early breakdown at the corner and resolves the degradation of dynamic on-resistance (R_{on}) associated with the floating P+ shield. In comparison to the conventional device without the P+ shield, the maximum electric field in the gate oxide of the proposed device decreases by 65.7% (from 3.5 to 1.2 MV/cm), as illustrated in Figure 3b, thereby achieving superior gate oxide reliability. The OFF-state breakdown characteristics of the studied devices are compared in Figure 3c. The BVs of the proposed device and the conventional device with the P+ shield region are above 1.3 kV, while the BV of the device without the P+ shield is only 750 V. The impact of the deep trench on the breakdown characteristics is also investigated in Figure 3d. A slight decrease in the effective thickness of the N-drift region from 1.5 to 2.4 μm results in a minor degradation in the BV. However, this slight decrease in the BV is well justified by the reduction in the gate oxide field, which is the limiting factor for device reliability.

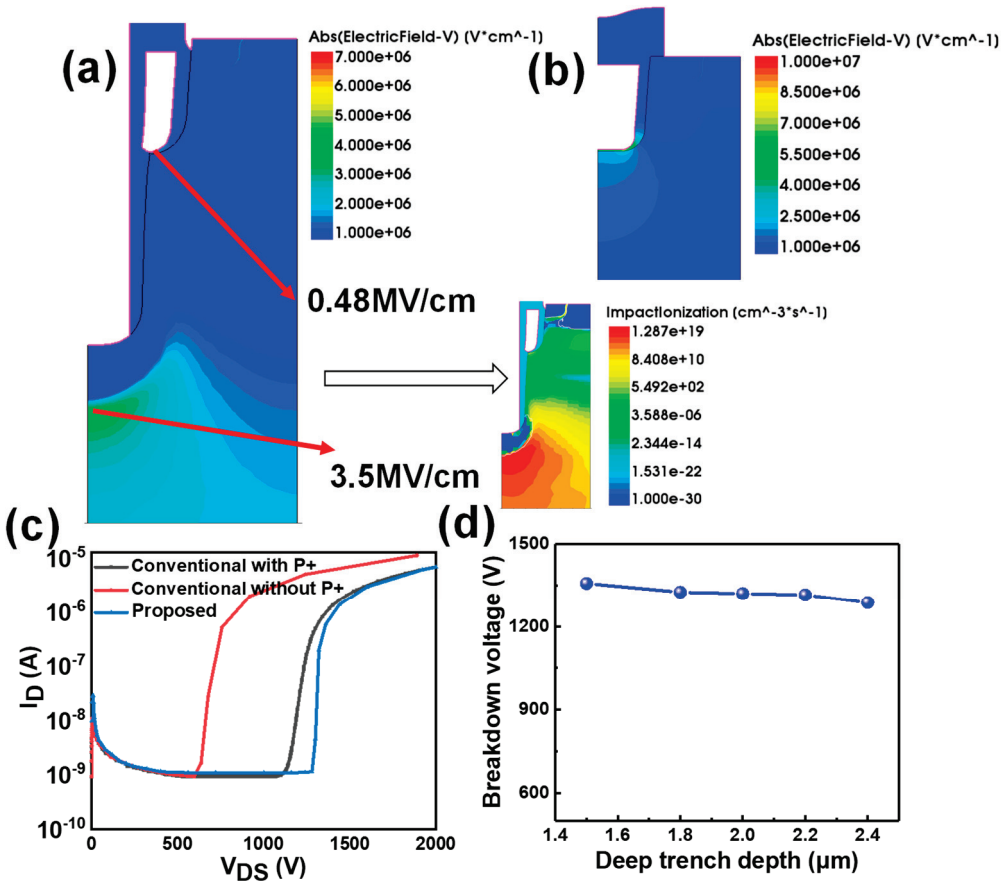

Figure 3. (**a**) The OFF-state electric field distributions in the proposed device at VDS = 1320 V (deep trench depth 2.4 μm). (**b**) The OFF-state electric field distributions in the conventional device without P+ at VDS = 750 V. (**c**) Breakdown characteristic of the proposed device and conventional devices with and without P+, respectively. (**d**) Relationship between deep trench depth and BV of the proposed device.

B. Conduction characteristics

As depicted in Figure 4a, the estimated R_{on} values for the proposed device, conventional device with the P+ shield, and conventional device without the P+ shield are 1.51, 100, and 1.28 mΩ·cm^2, respectively. The introduction of the P+ shield significantly affects the conduction characteristics by increasing the electron flow resistance near the sidewall. However, the proposed device successfully concentrates the distribution of the P+ region, minimizing the impact on the R_{on}. By optimizing the doping profile of the body region, the 17.8% increase in the R_{on} can be offset and improved. The depth of the deep trench has little effect on the R_{on}, as illustrated in the inserted picture in Figure 4a. Figure 4b presents a comparison of the trade-off relationship between the BV and R_{on} for the three devices. The proposed device achieves the optimal combination of a high BV and low R_{on} simultaneously. Moreover, a deeper depth allows the inverted PN junction in the OFF state to penetrate further into the drift zone. This enables the possibility of further reducing R_{on} by increasing the doping concentration of the JFET region during epitaxial growth (or by ion implantation), as depicted in Figure 4c, without compromising other characteristics. It should be noted that introducing a grounded deep trench in the device structure will increase the width of the trench, which may impede further reductions in the cell size. To address this challenge, a corresponding layout arrangement is proposed, as depicted in Figure 4d. The proposed layout design distributes grounding at intersections and centers, allowing sufficient space for grounding vias. In this design, the width of the cross-region is set to 1.414 times the length (1.414 L), providing ample room for the incorporation of grounding vias.

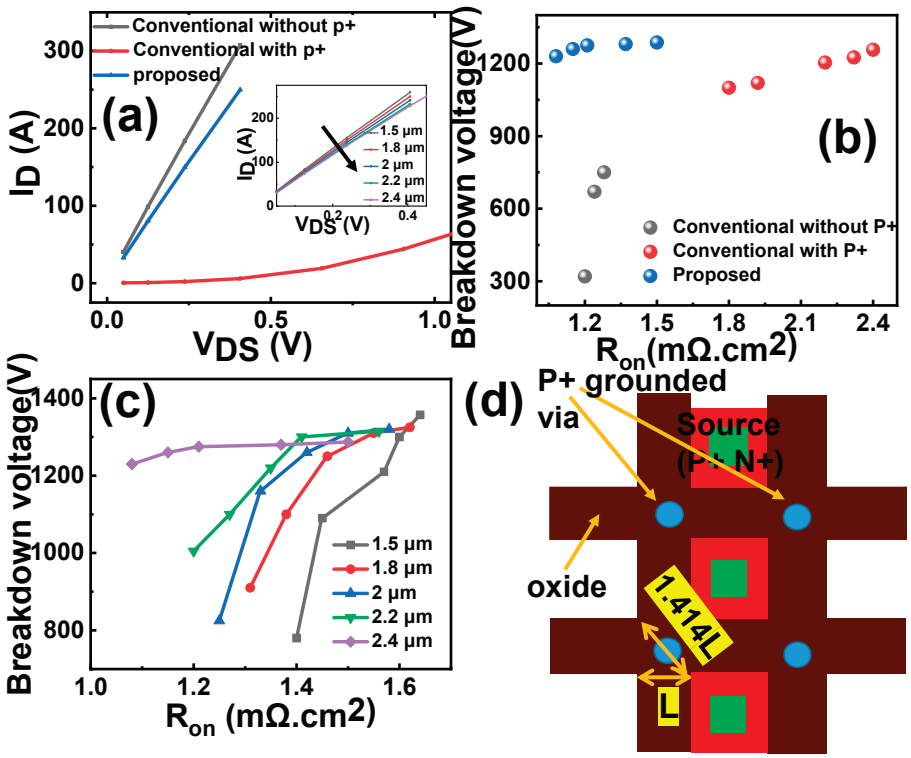

Figure 4. (**a**) ON-state characteristics of the proposed device and conventional devices with and without P+, respectively. (**b**) BV–R_{on} trade-off relationship of the proposed device and conventional devices with and without P+. (**c**) Trade-off relationship between BV and R_{on} with different trench depth. (**d**) Cell layout design of distributed grounding method.

By implementing the proposed layout arrangement as described, the device cell pitch can be effectively reduced to 1.8 μm. Furthermore, this reduction in cell pitch is

achieved while maintaining a desirable on-resistance (R_{on}) value below 0.94 mΩ·cm^2. This approach allows for the efficient utilization of space, optimizing the device's overall performance characteristics, and enabling the realization of a compact and high-performing device design.

C. Switching characteristics

The capacitance distribution of the proposed device is shown in Figure 5a. The dominating part of the Miller C_{gd} is decomposed into C_{gs}. The results show that the Q_{gd} values for the conventional and the proposed device are 330 nC/cm^2 and 67 nC/cm^2, respectively. The gate charge curve of the proposed device has almost no Miller platform. And the increased Q_{gs} can be further reduced by increasing the isolation oxide thickness of the deep trench. Compared with [26], the principle of our device to eliminate Q_{gd} is mainly to convert C_{gc} into C_{gs} through the split gate structure, and the optimization should be better, theoretically. While the reduced Q_G improves the switching speed, faster transitions may exacerbate transient oscillations in the gate or drain-source loop due to parasitic inductances. Techniques such as active gate shaping or PT-symmetric damping could be explored to mitigate such effects in future designs [27].

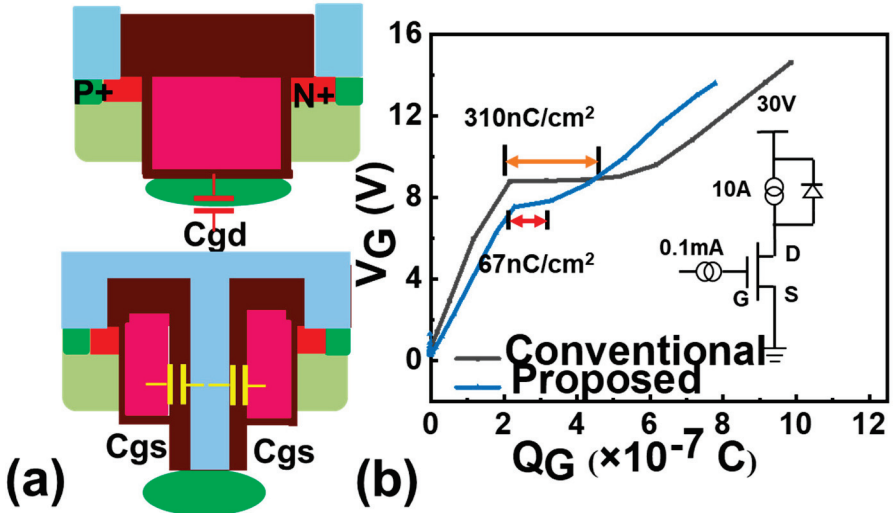

Figure 5. (**a**) Capacitance distribution diagram; (**b**) gate charge of the proposed device and conventional devices with and without P+. The inserted picture shows the test circuit configuration.

Table 2 summarizes the performance of the proposed and conventional devices. The proposed structure shows an overall better performance including a low R_{on}, low Q_{gd}, high BV, and high figure of merit FoM (FoM = BV^2/R_{on}).

Table 2. Comparison of performance parameters.

	Proposed	Con with +P	Con Without +P
R_{on} (mΩ·cm^2)	1.08	1.8	1.28
BV (V)	1230	1100	750
FoM (MW·cm^2)	1.4	0.672	0.43
Q_{gd} (nC/cm^2)	67	330	336

4. Conclusions

In summary, we have introduced a novel SiC MOSFET with a distributed grounded P+ shield. This device features a stepped trench and deep trench server as a P+ shield grounded channel. This way, the inverted p-n junction in the OFF state can be pushed

down into the drift region to effectively protect the gate oxide, providing enough margin for optimal doping in the body region. Compared with the conventional P+ shield device, a 78% reduction in the Q_{gd} and 108% increase in the FoM are realized simultaneously. Furthermore, the use of P-type polysilicon in the middle deep trench based on this structure can significantly reduce the Schottky barrier and solve the problem of the insufficient reverse conduction ability of the current body Schottky barrier diode. Overall, this is a technology with practical application prospects. This technology represents a fundamental advancement in SiC power device design by simultaneously solving three longstanding challenges, representing a significant advancement in high-voltage power device technology.

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Simulation Study on 6.5 kV SiC Trench Gate p-Channel Superjunction Insulated Gate Bipolar Transistor

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Abstract: This paper investigates 6.5 kV SiC trench gate p-channel IGBTs using Sentaurus TCAD simulations. The proposed superjunction structure is compared to conventional designs to highlight its advantages. The p-IGBT, fabricated on an n-type substrate, offers notable commercial advantages over n-IGBTs on p-type substrates. The n-shield can effectively protect the trench gate oxide in the corners of SiC. The n-shield and n-pillar can be either floating or grounded, with the floating shield condition significantly enhancing injection and improving forward conduction performance. The superjunction floating shield p-IGBT (SJFS-p-IGBT) improves forward conduction voltage (V_F) by 47% and 15% compared to conventional planar gate p-IGBT (CP-p-IGBT) and grounded shield p-IGBT (CGS-p-IGBT), respectively. For switching characteristics, the superjunction grounded shield p-IGBT (SJGS-p-IGBT) improves turn-off time (t_{off}) by 15% compared to the conventional floating shield p-IGBT (CFS-p-IGBT). The trade-off between V_F and turn-off energy (E_{off}) is analyzed, showing that the SJFS-p-IGBT offers a better trade-off. A negative temperature coefficient is observed at high buffer layer doping concentration and elevated temperatures, leading to an increase in V_F. This provides design guidance for devices operating in parallel at high temperatures. These results demonstrate the SJ's potential to enhance efficiency and performance for ultra-high voltage applications.

Keywords: SiC; trench gate; IGBT; superjunction; forward voltage; turn-off energy loss

1. Introduction

High-voltage and high-current IGBTs are primarily designed for medium to ultra-high-power applications such as industrial applications, switched-mode power supplies, and traction systems [1,2]. Silicon IGBTs have been utilized and approached their inherent limits [3–5]. Furthermore, their development in these applications is significantly constrained by material limitations in operating frequency, voltage rating, and temperature. As a wide bandgap material, power devices in SiC have gained considerable interest due to their superior material properties [6,7]. From several hundred volts to approximately 3.3 kV, SiC MOSFET has been widely used and commercialized [8,9]. However, for ultra-high-voltage applications exceeding 6.5 kV, due to a significant reduction in conduction loss by conductivity modulation, bipolar devices, such as IGBTs and thyristors, are favored over unipolar devices in 4H-SiC [10,11]. On the other hand, IGBTs show some advantages over thyristors. Firstly, an IGBT is controlled by the voltage at the gate, similar to a MOSFET, offering a high-input impedance with low driving power. Secondly, IGBT typically supports switching frequencies up to tens of kHz or even higher, while thyristors are typically used

below several hundred Hz. Thus, except for some ultra-high-power applications at low frequencies, most medium to high applications are dominated by IGBTs. Several studies have shown that superjunction (SJ) IGBT on Si has better turn-off energy (E_{off}) and forward conduction voltage (V_F) performance than conventional IGBT [12–14], resulting from the electric field distribution two-dimensional depletion expansion in the pillars. At the same time, charge balance in n- and p-pillars enables a thinner drift region thickness, which also helps improve storage charge for better E_{off} and V_F [15,16]. The investigation on SiC 6.5 kV trench gate p-IGBT is proposed for the first time in this work. P-IGBTs feature two distinct advantages over n-IGBTs in SiC. Firstly, they are economically more feasible primarily due to the lack of good conducting p-type SiC substrates. Secondly, p-IGBTs exhibit higher transconductance than n-IGBTs because the parasitic npn transistor in p-IGBTs has a higher common base current gain than the pnp transistor in n-IGBTs [17,18]. In the meantime, the trench gate structure is used to reduce the cell pitch size and increase channel density [19], counteracting the deficiency in poor p-channel mobility in SiC. In this paper, SiC 6.5 kV trench gate superjunction and conventional p-IGBTs are investigated using TCAD two-dimensional simulations. The E_{off} and V_F trade-offs with respect to critical parameters such as the buffer layer, the carrier lifetime, and the temperature are examined. Physics models include Shockley–Read–Hall (SRH), Auger, Okuto–Crowell avalanche model, doping-dependent mobility, high-field saturation mobility, and Incomplete Ionization [20]. Based on the results, 6.5 kV-class SiC trench gate superjunction p-IGBTs could be a strong candidate for power switches in ultra-high-power applications [21–23].

2. Device Structure

Figure 1 shows the cross-sectional view of a conventional trench gate p-IGBT, a trench gate superjunction p-IGBT, a conventional trench gate n-IGBT, and a planar gate p-IGBT in 4H-SiC. In the trench gate structures, the n-well is always connected through an n+ region to the emitter electrode in the third dimension to reduce cell pitch. In simulation, this is achieved by placing a virtual electrode on the side of the n-well at an appropriate location, similar to our previous study [24]. The n-shield region and n-pillar can be either grounded or floating in the third dimension, which can be realized through appropriate layout designs. The doping concentration and the thickness of the drift region are 1×10^{15} cm^{-3} and 45 μm, respectively, for a 6.5 kV-rated blocking voltage for conventional IGBTs [25]. For the SJ-IGBTs, the pillar doping concentration is about 1×10^{15} cm^{-3} for both n- and p-pillars. The pillar widths are 1 and 1.2 μm for n-pillar and p-pillar, respectively. With aggressive scaling, the cell pitch is assumed to be 2.2 μm, including a 1 μm-wide gate trench, and the trench depth is 1.5 μm. All the device parameters are chosen based on the previously reported results and the current capabilities of foundries. If the cell pitch is aggressively scaled to less than 2.2 μm, then V_F starts to increase due to significant junction field-effect transistor (JFET) effect. The gate oxide layer is uniform and 42 nm thick. To realize high-performance SiC superjunction (SJ) structures presents considerable challenges, primarily due to the need for advanced fabrication techniques and precise doping control to achieve superior device performance [26,27]. In this study, a multi-epitaxial (ME) growth technique is employed [28], which involves repeated cycles of epitaxial layer deposition and ion implantation to form n-pillars. To serve as an electric field stopping layer and to prevent punch-through of the drift region in the blocking state, a buffer layer with 2.5 μm thickness is applied. The channel length is 0.5 μm, and the inversion hole mobility is assumed to be around 12 cm^2/V-s based on previously reported numbers [29,30]. The depth of the shielding in the conventional grounded shied p-IGBT (CGS-p-IGBT) and the conventional floating shied p-IGBT (CFS-p-IGBT) is 1.1 μm. To

enhance forward conduction characteristics, a current spreading layer (CSL) is added on top of the drift layer [31,32]. Regarding the forward conduction operation, a JFET effect will occur between n-well and n+ shielding or adjacent n+ shielding regions, leading to an increase in specific on-resistance ($R_{on,sp}$). The CSL is a p-type region with a higher concentration than the drift region, providing more holes during forward conduction, thereby benefiting the conduction characteristics. The doping concentration of the CSL is 1×10^{16} cm^{-3}. The doping concentration of the n-substrate region is 1×10^{19} cm^{-3}. The carrier lifetime is assumed to be 1 μs unless indicated otherwise. The conventional trench gate grounded shied n-IGBT (CGS-n-IGBT) is designed with the same dimensions and doping concentrations as the CGS-p-IGBT, except for the opposite n-type and p-type dopants. The p-type substrate is assumed to be very thin to remove its resistance contribution. All the SJ devices have the same dimensions and doping concentrations above the CSL and the trench oxide as the conventional device, except for the drift region to support a fair comparison. The fabrication process schematic of the ME growth SJ trench gate p-IGBT is shown in Figure 2. (a) The p-drift region and p-buffer layer are formed on the n-substrate using epitaxial deposition technique; (b) phosphorus ion implantation to form n-pillars; (c) repeat ME technique for 30 times to form the SJ structure; (d) aluminum ion implantation to form CSL; (e) phosphorus ion implantation to form n-well; (f) aluminum ion implantation to form p+; (g) trench etch; (h) gate oxide deposition; (i) polysilicon deposition to form the gate; (j) inter-layer dielectric formation; (k) contact formation and metal deposition.

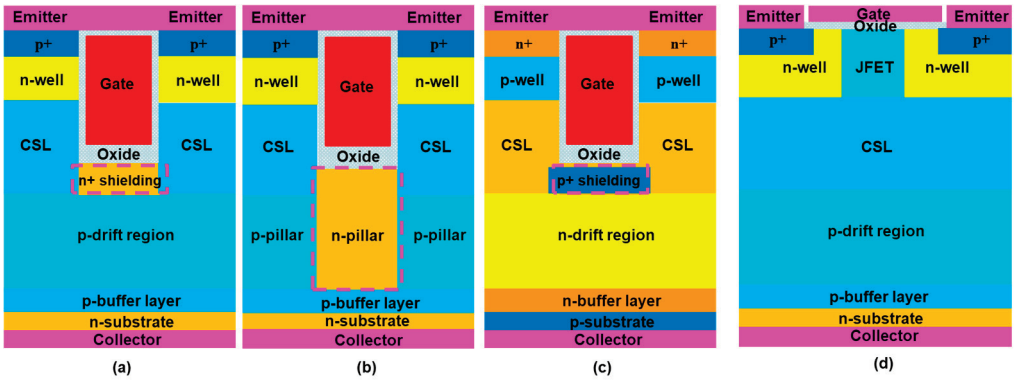

Figure 1. Schematic cross-section of (**a**) a conventional trench gate p-IGBT, (**b**) a superjunction trench gate p-IGBT, (**c**) a conventional trench gate n-IGBT, and (**d**) a conventional planar gate p-IGBT. The dashed n,p-shield region and n-pillar can be grounded or floating.

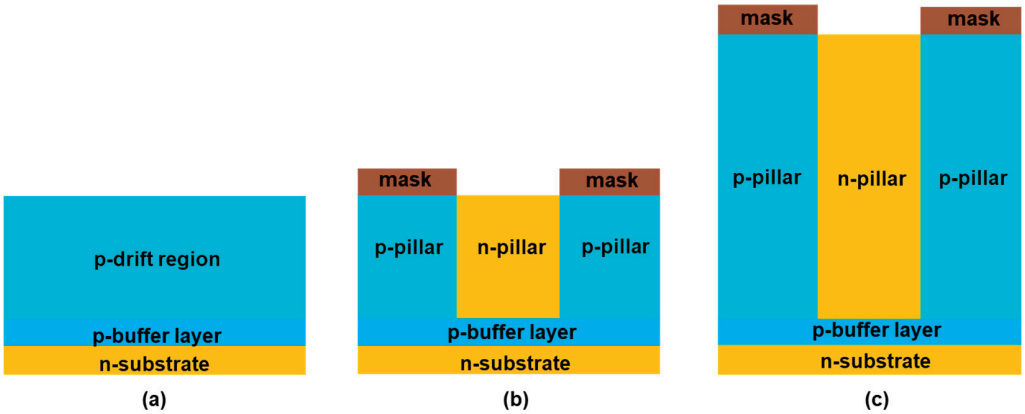

Figure 2. *Cont.*

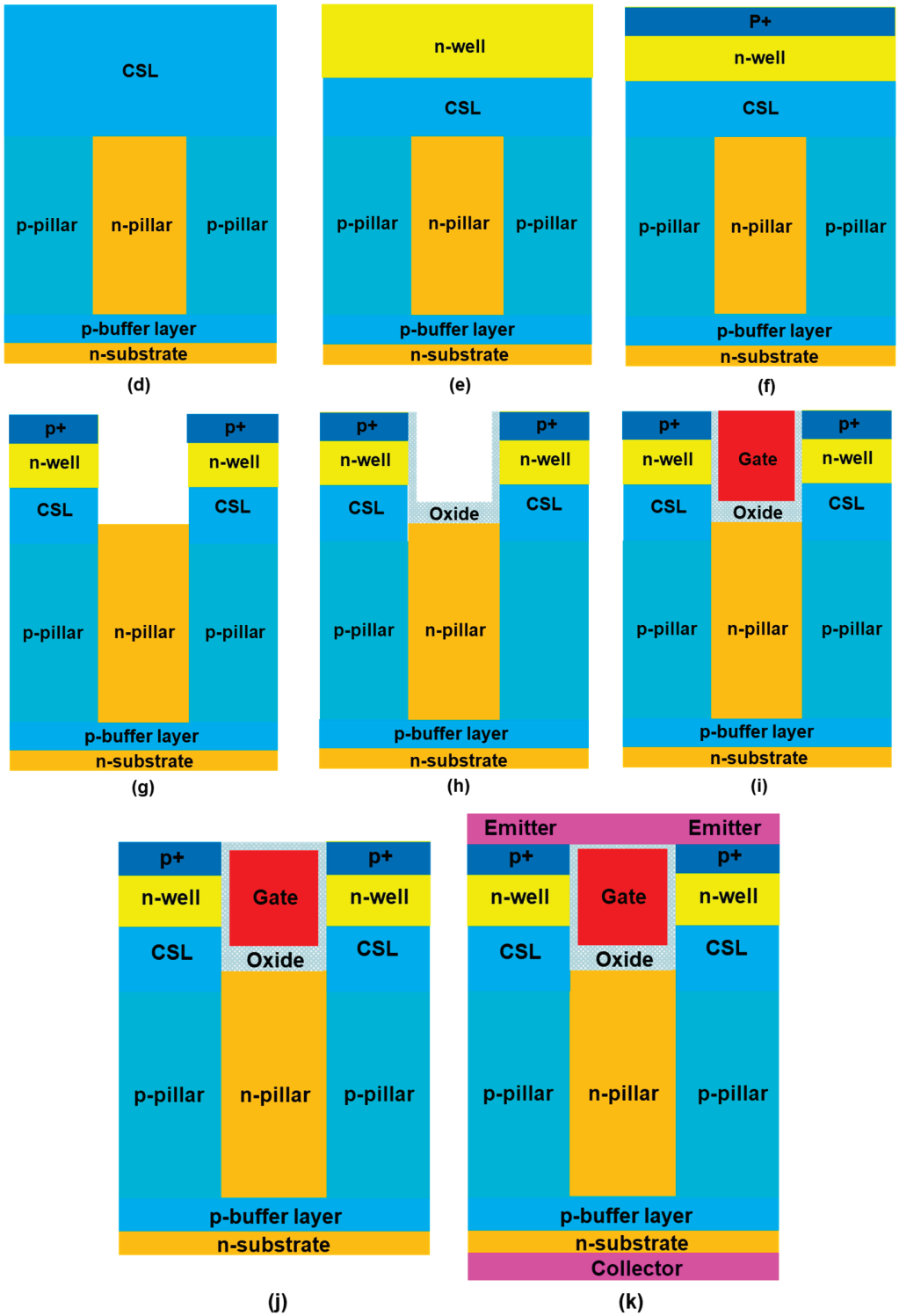

Figure 2. Schematic fabrication process of SJ trench gate p-IGBT. (**a**) The p-drift region and p-buffer layer are formed on the n-substrate using epitaxial deposition technique; (**b**) phosphorus ion implantation to form n-pillars; (**c**) repeat ME technique for 30 times to form the SJ structure; (**d**) aluminum ion implantation to form CSL; (**e**) phosphorus ion implantation to form n-well; (**f**) aluminum ion implantation to form p+; (**g**) trench etch; (**h**) gate oxide deposition; (**i**) polysilicon deposition to form the gate; (**j**) inter-layer dielectric formation; (**k**) contact formation and metal deposition.

3. Static Characteristics

Figure 3 illustrates the forward J_C–V_{CE} characteristics at a V_{GE} of −16 V for the trench gate p-IGBTs under study. For comparison, a CGS-n-IGBT, the n-channel mobility is set to be around 30 cm^2/V-s based on previously reported numbers in [33], and a conventional planar gate p-IGBT is also simulated based on the structure experimentally demonstrated in [31], denoted as conventional planar gate p-IGBT (CP-p-IGBT), where the cell pitch is 15 μm, including a 3 μm JFET. The drift region, as well as the CSL doping and thickness, are adjusted to be the same as those of the trench gate IGBT structure for the same voltage rating. An improved planar gate p-IGBT (IP-p-IGBT) is also included in this study with a reduced cell pitch of 4.4 μm, including a JFET width of 2.2 μm, channel length of 0.5 μm, and 1.2 μm p+ region width. In this case, the n+ region is connected in the third dimension, similar to the trench gate structure, to aggressively scale down the cell pitch of the planar gate IGBT. Further reducing the JFET width and the cell pitch will degrade performance due to pinch-off by the JFET effect. It should be noted that the cell pitch of a planar gate structure cannot be as small as a trench gate structure due to the lateral channel length and JFET width. The detailed device structure parameters are provided in Table 1.

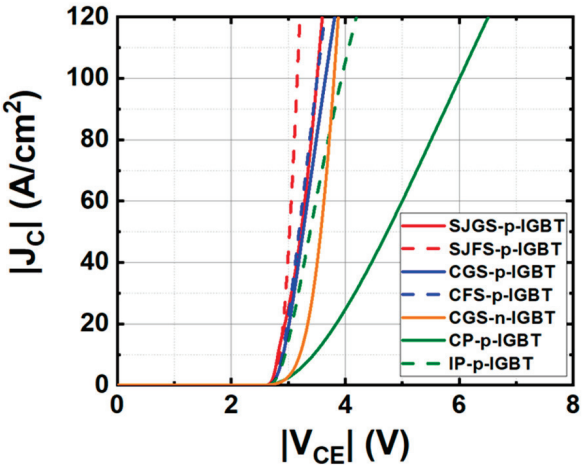

Figure 3. Simulated J_C–V_{CE} characteristics of the studied IGBTs.

Table 1. Device parameters of the IGBTs.

Parameters	Conventional Planar Gate p-IGBT	Improved Planar Gate p-IGBT	Conventional Trench Gate n-IGBT	Conventional Trench Gate p-IGBT	Superjunction Trench Gate p-IGBT
Buffer layer depth (μm)	2.5	2.5	2.5	2.5	2.5
Buffer layer doping (cm^{-3})	1×10^{18}	1×10^{18}	1×10^{18}	1×10^{18}	1×10^{18}
Drift region depth (μm)	45	45	45	45	45
Drift region doping (cm^{-3})	1×10^{15}	1×10^{15}	1×10^{15}	1×10^{15}	1×10^{15}
CSL doping (cm^{-3})	1×10^{16}	1×10^{16}	1×10^{16}	1×10^{16}	1×10^{16}
Channel length (μm)	1.5	0.5	0.5	0.5	0.5
JFET width (μm)	3	2.2	--	--	--
Cell pith (μm)	15	4.4	2.2	2.2	2.2

From Figure 3, the simulated V_F of CP-p-IGBT and IP-p-IGBT reaches as high as −6 V and −4.2 V, respectively, at J_C = −100 A/cm^2, while the V_F values of the trench gate IGBTs are all below −4 V. Due to the poor p-channel hole mobility in SiC, a large

cell pitch, as in the case of a planar gate p-IGBT, limits the hole current density, thereby reducing the back-injected electron density into the drift region, which is unfavorable for conductivity modulation. On top of that, the poor p-channel resistance contributes a significant voltage drop to the V_F. Since the cell pitch of the trench gate structure can be much smaller than that of the planar gate structure, the aforementioned drawbacks from poor p-channel mobility can be minimized. If we look further into the V_F values of CGS-p-IGBT, CFS-p-IGBT, SJGS-p-IGBT, SJFS-p-IGBT, and CGS-n-IGBT, they are −3.73 V, −3.57 V, −3.55 V, −3.20 V, and 3.82 V, respectively, comparable to reported simulation results for SiC n-channel IGBTs [33,34]. The first conclusion we can make at this point is that with a trench gate structure and a small cell pitch, the DC characteristics of SiC p-IGBTs are comparable to SiC n-IGBTs.

In general, the floating shield has superior forward characteristics. The increase in V_F with the grounded n-shield is caused by the reduction in minority carrier concentration because the grounded shield enables the extraction of minority carriers, which are electrons, with an external electrode. Conversely, the floating shield has better conductivity modulation since electrons are stored at the upper side of the drift region. Figure 4 shows the distribution of electron density and doping concentration along the drift region from emitter to collector in the investigated trench gate p-IGBTs when applying $V_{GE} = -16$ V and $V_{CE} = -4$ V. Thus, the V_F of the floating shield condition is lower than that of the grounded shield condition in both cases, consistent with [33]. The V_F of SJFS-p-IGBT is reduced by 15% compared to that of CGS-p-IGBT and further reduced by 28% compared to that of IP-p-IGBT.

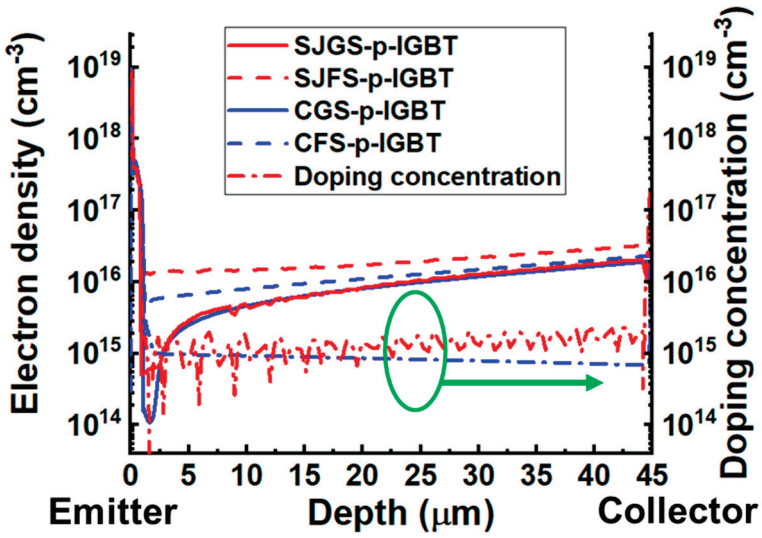

Figure 4. Distribution of electron density and doping concentration along the drift region from emitter to collector in the drift region of the investigated trench gate p-IGBTs.

Figure 5 shows the simulated breakdown characteristics ($V_{GE} = 0$ V) of all the structures. The BV values of all devices are above the targeted 6500 V, and the leakage currents are all below 1×10^{-3} A/cm^2. Figure 6 illustrates the electric field distribution of all trench gate devices at $V_{CE} = -6500$ V. The electric field at the bottom corners of the gate trench does not exceed 3 MV/cm in all cases, indicating that the n-shield region and n-pillar effectively mitigate the electric field in the oxide and preserve gate oxide integrity. The discussion in the following sections will focus on the proposed trench gate p-IGBT structures to further explore their switching performance to justify their potential in real applications.

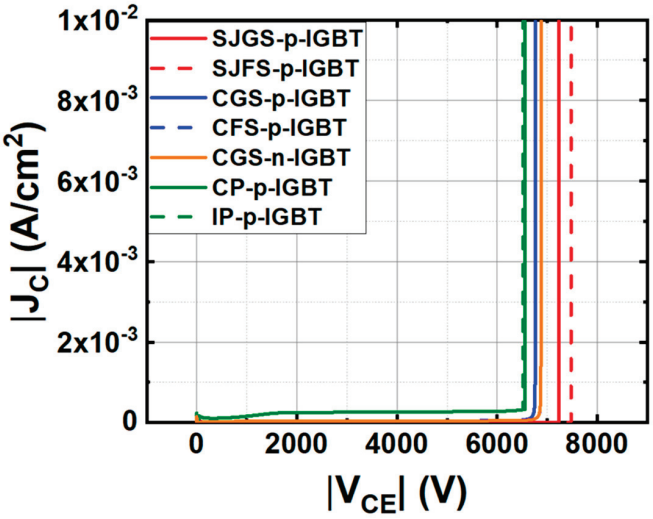

Figure 5. Blocking characteristics (V_{GE} = 0 V) of the studied IGBTs.

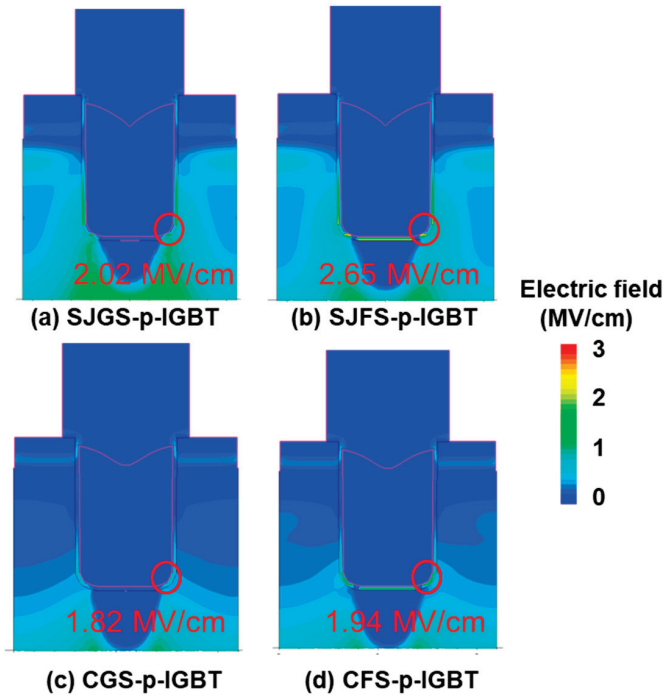

Figure 6. Electric field distribution in the off-state for the studied trench gate p-IGBTs at V_{CE} = −6.5 kV and V_{GE} = 0 V.

4. Dynamic Characteristics

The switching characteristics of the IGBTs are investigated using a double pulse test circuit shown in Figure 7. The supply voltage is V_{CC} = −4.5 kV, and the gate voltage V_G changes from −20 V to 5 V to turn the device on and off, respectively. The active area of the IGBT is scaled to 68 mm^2. The load inductance is 2.1 mH, and an external gate resistor R_G = 10 mΩ is used. The turn-off waveforms for all the structures are shown in Figure 8. The SJGS-p-IGBT exhibits a slightly shorter turn-off time (t_{off}). Since the electron density near the shield region in conduction is lower than that of both the SJFS-p-IGBT and CFS-p-IGBT, the V_{CE} potential builds up quickly at the beginning of the turn-off transient, which leads to shorter t_{off}.

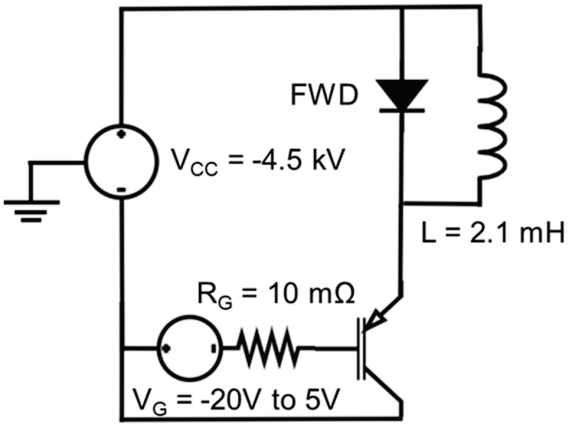

Figure 7. A clamped inductive load circuit for the switching characteristics of the studied IGBTs with an active area of 68 mm^2.

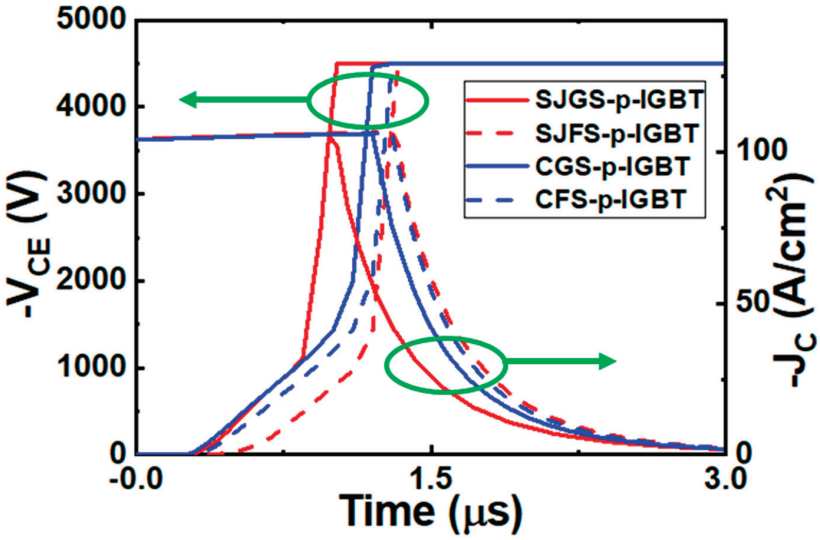

Figure 8. Turn-off voltage and current waveforms of the studied IGBTs.

Moreover, the t_{off} values of SJGS-p-IGBT, SJFS-p-IGBT, CGS-p-IGBT, and CFS-p-IGBT are calculated to be 1.7, 2, 1.9, and 2 μs, respectively. Generally, the superjunction structure has a slightly shorter t_{off} due to the drift region being fully depleted faster because of the two-dimensional expansion of the depletion region. Figure 9 illustrates the depletion region and the hole density distribution during the turn-off periods of SJGS-p-IGBT and CGS-p-IGBT. At 30 ns after turn-off, the depletion region in the SJGS-p-IGBT expands well into the drift region with the lateral depletion from pillars, while at 40 ns in the CGS-p-IGBT, the depletion region remains around the n-shield. Thus, a better t_{off} and E_{off} is expected from this effect.

It is noted that before 1 kV, the V_{CE} increases slowly. Since the electron density is higher at the collector side of the drift region, more excess carriers need to be removed to achieve the same voltage buildup. Thus, the V_{CE} increases slowly during this stage of the turn-off transient. This process is faster for the superjuction structure for the reason explained previously. After 1 kV, as the depletion region starts to extend into the buffer region where the doping concentration is higher, the electric field accumulates more rapidly, leading to a faster increase rate for V_{CE}. Eventually, when V_{CE} reaches the punch-through voltage, the collector current then decreases until it reaches zero, completing the turn-off process [33,35]. Different from the turn-off process, the differences in the turn-on waveform and turn-on energy are not significant among the IGBTs under study and, therefore, are not presented in this paper.

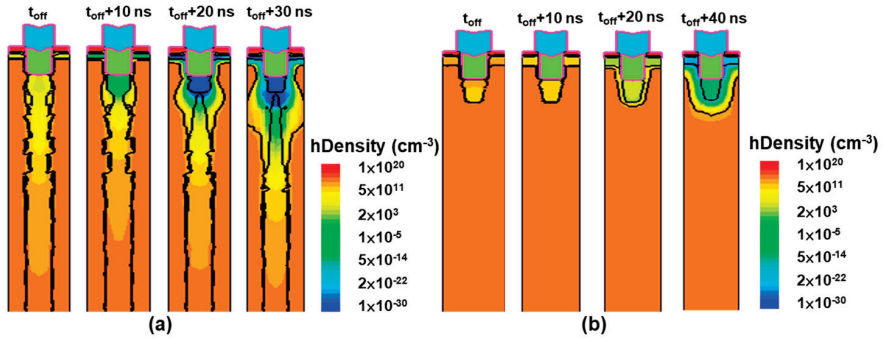

Figure 9. Hole density distribution and depletion region (denoted as the black line) during turn-off periods of (**a**) the SJGS-p-SJBT and (**b**) the CGS-p-IGBT.

5. Key Performance Parameters

5.1. Carrier Lifetime

To reduce switching loss, carrier lifetime control in the drift region is important. Due to the conductivity modulation of IGBTs, the drift region resistance primarily depends on the carrier lifetime in the drift region [36,37]. High-voltage bipolar devices require a long carrier lifetime to effectively modulate the conductivity of the thick drift region layer. In contrast, a short carrier lifetime hinders conductivity modulation, making the forward voltage high. Conversely, a long carrier lifetime will lead to a long reverse recovery time, which limits the switching frequency and increases switching loss [38]. Therefore, the carrier lifetime must be carefully controlled to achieve optimal performance. Figure 10 shows the trade-off between turn-off energy loss and forward voltage drop for all the structures. It is observed that the SJFS-p-IGBT shows the best V_F-E_{off} trade-off while the CGS-p-IGBT shows the worst trade-off among the IGBTs under study.

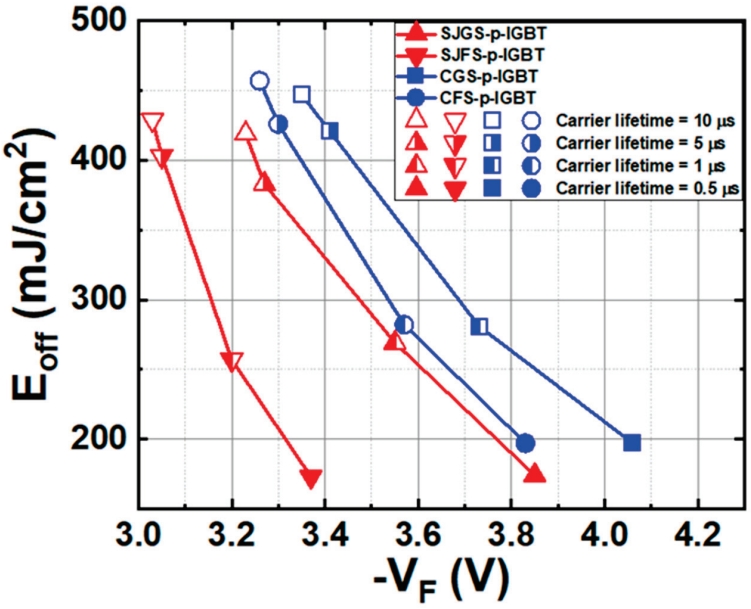

Figure 10. Trade-off curves of V_F and E_{off} of the studied IGBTs with different carrier lifetimes.

5.2. Buffer Layer Doping Concentration

The buffer layer concentration has a great impact on both the stored charge and the switching speed, and the mechanism is clearly explained in [39,40]. Figure 11 shows the trade-off between E_{off} loss and V_F as the buffer layer concentration increases from

1×18 cm^{-3} to 5×18 cm^{-3}. The E_{off} decreases dramatically because the carrier lifetime of the buffer layer decreases as the concentration increases, based on a concentration-dependent lifetime. The ambipolar diffusion length in the buffer layer becomes shorter than the buffer layer thickness, reducing the injection efficiency of electrons into the drift layer [39]. As a result, the V_F increases. The SJFS-p-IGBT shows the best V_F-E_{off} trade-off. Conversely, the CGS-p-IGBT exhibits a much worse V_F-E_{off} trade-off in comparison with the other IGBTs.

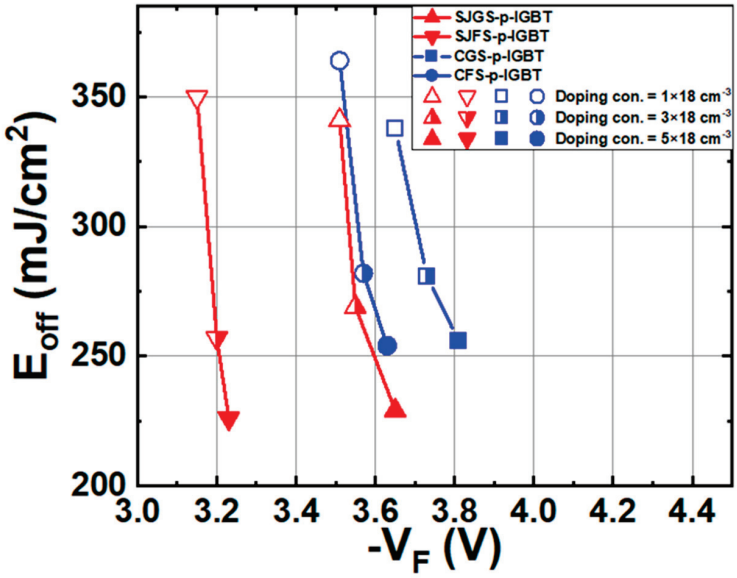

Figure 11. Trade-off curves of V_F and E_{off} of the studied IGBTs with various buffer layer doping concentrations.

5.3. Temperature Effect

The equivalent circuit model of a p-IGBT consists of a wide-base npn BJT and a p-channel MOSFET. Several studies [41–44] have indicated that a 4H-SiC npn BJT can show either positive or negative temperature coefficients for its common emitter current gain (β). The positive temperature coefficient is attributed to the increase in the carrier lifetime as the temperature rises. On the other hand, the negative temperature coefficient results from the incomplete ionization of acceptors in the base region [45]. With the temperature increasing, the hole concentration will increase, leading to a lower injection efficiency, and it is worse for higher p-type concentrations. Thus, the 4H-SiC npn BJT can have a lower current gain at a higher temperature. The p-buffer layer in the p-IGBT structure plays the same role and affects the emitter injection efficiency in the parasitic npn BJT. Figure 12 illustrates the β and V_F of the SJFS-p-IGBT at a collector current of 100 A/cm^2 at different temperatures for different buffer layer doping concentrations. A smaller current gain will be obtained at a higher temperature for all buffer layer doping concentrations, and this is more pronounced for $>3 \times 18$ cm^{-3}. It is shown that the V_F decreases monotonically as the temperature increases in the case of 1×18 cm^{-3}. However, as the buffer layer doping concentration is greater than 3×18 cm^{-3}, the V_F starts to show a positive temperature coefficient at a higher temperature, due to the reduced injection of minority carrier electrons from the n-substrate in this case. Hence, the buffer layer doping concentration must be considered when a positive temperature coefficient in V_F is preferred for paralleling 4H-SiC p-IGBT chips.

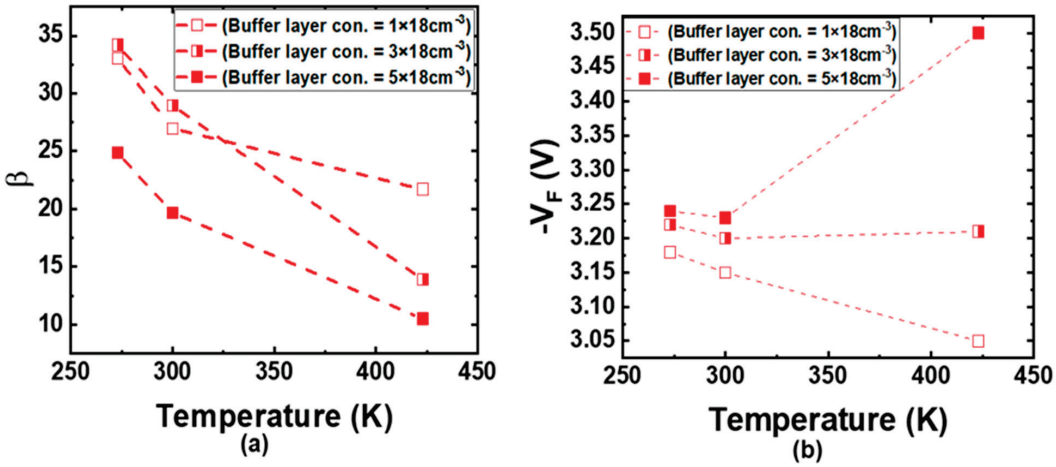

Figure 12. The temperature effect of the buffer layer doping concentration in a SJFS-p-IGBT on (**a**) common emitter current gain (β) for the parasitic npn BJT and (**b**) forward voltage at $J_C = -100$ A/cm^2.

6. Conclusions

In summary, the investigation on a novel SiC 6.5 kV trench gate p-IGBT with a superjunction structure is proposed in this work. The p-IGBT demonstrates greater commercial potential due to the adoption of a low-resistivity n-type substrate, which facilitates cost-effective manufacturing. The V_F and E_{off} trade-off of the device is examined by varying the buffer layer concentration, carrier lifetime, and temperature. From the simulated static characteristics, the SJFS-IGBT can improve the V_F by 15%, relative to the CGS-p-IGBT. For the switching characteristics, the SJFS-p-IGBT demonstrates 15% improvement in t_{off}, compared to the CFS-p-IGBT. Regarding the temperature effect, depending on the buffer layer doping concentration, all the structures exhibit noticeably negative temperature coefficients on the current gain, particularly when the buffer layer doping concentration is higher than 3×18 cm^{-3}. The reduced injection efficiency will turn the temperature coefficient from negative to positive, especially for high buffer layer doping concentrations and high temperatures. The results presented in this paper pave the way for the 4H-SiC trench gate p-IGBT with superjunction for ultra-high voltage applications.

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Conflicts of Interest: The authors declare no conflicts of interest.

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Numerical Simulations of 3C-SiC High-Sensitivity Strain Meters

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Abstract: In the simulation of 3C-SiC strain gauges in dynamic environment—particularly those involving vibrations and wave propagation—the accurate representation of energy dissipation is essential for reliable predictive modeling. This paper discusses the implementation of both isotropic and anisotropic damping models within COMSOL Multiphysics. In particular, it focuses on the use of an anisotropic loss factor, represented either as a scalar (η_S) for isotropic cases or as a symmetric 6×6 loss factor matrix (η_D) for anisotropic dissipation. This formulation enables the directional dependence of damping behavior to be captured, which is particularly important in composite materials, layered media, and metamaterials where energy dissipation mechanisms vary with orientation. The paper also explores the numerical implications of using anisotropic damping, such as its influence on eigenfrequency solutions, frequency response functions, and transient dynamic simulations. Furthermore, it highlights how the inclusion of directional damping can improve the correlation between simulated and experimental results in scenarios where standard isotropic models fail to capture key physical behaviors.

Keywords: COMSOL Multiphysics; loss factor matrix; anisotropic damping

1. Introduction

Dynamic systems are inherently dissipative; vibratory energy is gradually converted into heat or other forms of energy, leading to a reduction in oscillation amplitude. In finite element analysis (FEA) using COMSOL Multiphysics® (Version 6.1) [1], this damping behavior can be modeled using conventional damping parameters as well as more sophisticated approaches, such as anisotropic loss factors [2]. The isotropic loss factor (η_s) assumes uniform energy loss in all directions, while anisotropic damping employs a symmetric 6×6 loss factor matrix (η_D), where only the components in the upper-triangular portion are independently defined. This distinction is critical for accurately simulating the directional dependencies observed in heterogeneous materials, such as composites and layered structures. Several mathematical frameworks exist to describe damping in structural dynamics. Typically, the damping-induced decay of vibration amplitudes is modeled as an exponential decrease over time. The phase information contained in a complex-valued mode shape can reveal local phase shifts, offering insight into spatial variations in damping behavior. In COMSOL Multiphysics, the damping matrix is assembled by combining various damping contributions, which are then incorporated into the finite element model to capture phenomena like mode shape distortions and resonant peak broadening. The flexibility of COMSOL Multiphysics allows users to define loss

factors along different material orientations, thereby enhancing the predictive capability of numerical simulations. This capacity to represent anisotropic energy dissipation is particularly important in fields like aerospace engineering and seismic analysis, where the precise characterization of damping effects directly impacts performance reliability and safety. The accurate modeling of damping is not only essential for realistic dynamic simulations but also for improving the correlation with experimental data. Anisotropic damping is particularly relevant in fiber-reinforced composites and layered structures where energy dissipation varies with direction. Complex mode shapes allow for the identification of localized damping phenomena, while matrix-based damping formulations support frequency-dependent analyses.

2. Materials and Methods

The samples in this work are 3C-SiC double-clamped beam structures (Figure 1) previously fabricated and characterized at CNR-ISMN Bologna (Italy), with Novasic wafers from Zielinski in France [3]. These samples were originally fabricated for the investigation of the Model of Quality factors for (111) 3C-SiC resonators. All of the comprehensive descriptions of the epitaxial growth process [4,5], lithographic patterning, and etching steps used to fabricate the devices are available in the original publication [3].

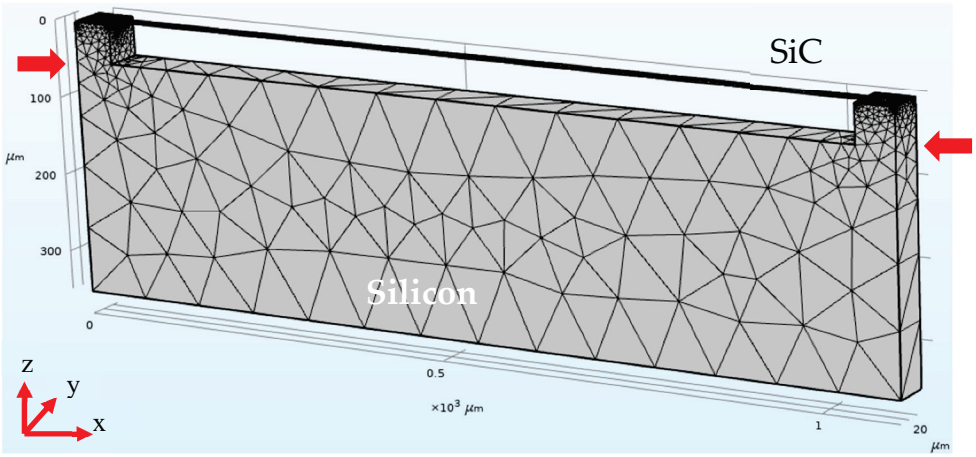

Figure 1. COMSOL simulated image of the sample: (111) 3C-SiC double-clamped beam grown on silicon substrate. The resulting mesh consisted of tetrahedral domain elements, triangular boundary elements, and edge elements. The red arrows, parallel to the x direction, indicate the force direction for the simulation of compressive/tensile stress.

The samples are (111) 3C-SiC film grown on silicon substrates, with a low doping concentration (<10^{16} cm^{-3}, NID—not intentionally doped), in a double-clamped beam configuration with a fixed width of 16 μm, lengths ranging from 200 to 1000 μm, and varying thicknesses. The complete list of samples is reported in Table 1.

Table 1. Wafer ID and film thickness of samples; specifically, wafers w_4 and w_5 refer to the samples used in the Romero at al. paper [6].

Wafer ID	w_1	w_2	w_3	w_4	w_5
Thickness (nm)	890	730	610	337	293

2.1. Finite Element Formulation

The dynamic behavior of a structural system is described through partial differential equations (PDEs), which are discretized using the finite element method (FEM) to yield a system of matrix equations. In matrix form, the equations of motion for a discretized structure are written as

$$M \cdot \ddot{u} + C \cdot \dot{u} + K \cdot u = f \tag{1}$$

where M is the mass matrix, C is the damping matrix, K is the stiffness matrix, u is the displacement vector, and f denotes the applied force vector. The damping matrix C can be formulated to include various damping contributions, with both isotropic and anisotropic components. The mass and stiffness matrices are determined through geometry and intrinsic material properties (i.e., density and Young's modulus), whereas the damping matrix reflects the energy dissipation mechanisms. The damping matrix C, which captures energy dissipation mechanisms, can be formulated using various approaches, including Rayleigh (mass and stiffness proportional), modal, or complex-valued formulations. For isotropic materials, scalar loss factors are often sufficient, but, in the case of anisotropic or composite structures, C must be constructed to reflect directional dependencies, typically via a symmetric 6×6 loss factor matrix. This anisotropic formulation is particularly relevant for orthotropic layers and fiber-reinforced composites, where damping varies with material orientation [7,8]. Although the eigenvalues of the anisotropic loss factor matrix obtained from COMSOL do not numerically match those of the stiffness matrices reported in the literature for materials like 3C-SiC or 4H-SiC, this discrepancy is expected due to their fundamentally different physical interpretations. The stiffness matrix describes the material's elastic response, while the loss factor matrix characterizes its energy dissipation behavior. However, both matrices are defined in the same Voigt space of strain components, and their eigenvectors represent principal deformation directions. The observed alignment between the principal directions of damping and elasticity suggests that the material exhibits directional mechanical behavior consistent with anisotropy. This justifies the adoption of an anisotropic damping model in our simulations, as it allows for a more accurate prediction of vibrational phenomena and eigenfrequencies, particularly in thin micro- and nano-scale films, where such effects become prominent.

2.2. Simulation Considerations in COMSOL Multiphysics

When performing structural dynamic analysis in COMSOL Multiphysics, it is essential to carefully consider the following aspects:

- Damping Representation: The choice between isotropic (scalar η_S) and anisotropic (matrix η_D) damping models should be guided by the material system under investigation.
- Energy Dissipation: The simulation should capture not only the decay rate of vibratory energy but also the phase relationships within the mode shapes. These details are crucial for a comprehensive understanding of damping effects.
- Discretization Accuracy: Finite element discretization provides an approximation of the true solution of the PDEs governing the system's behavior. Ensuring that the mesh is sufficiently refined is key to obtaining reliable and accurate results.
- Stress Analysis: In addition to damping effects, the distribution of internal stresses—both compressive and tensile—should be evaluated. For instance, when a bridge is deformed under load, the generated stress patterns offer valuable insight into the structural performance and possible failure mechanisms. (A representative stress image of a bridge can be included as part of the simulation outputs).

The choice between isotropic and anisotropic damping reflects not only material anisotropy but also the frequency-dependent nature of energy dissipation. Accurately capturing phase lag in mode shapes helps identify modal coupling and potential resonance risks [9,10].

To ensure the reproducibility and reference value of the simulation work, the mesh parameters were carefully defined, including the element type and the maximum and minimum element size. Particular attention was paid to the resolution near boundary regions and areas with expected high gradients in order to balance computational efficiency and solution accuracy. All mesh settings are documented to allow for consistent replication and validation of the numerical results. The resulting mesh consisted of 10,930 tetrahedral domain elements, 5276 triangular boundary elements, and 885 edge elements (Figure 1).

3. Results

The Q-Factor increases significantly with increasing thickness, especially between 500 and 700 nm (Figure 2). Beyond 700 nm, the Q-Factor stabilizes or shows a slight decrease. Using both models of isotropic and anisotropic dumping, it is possible to fit the experimental data with good accuracy. But, using this fitting, it is not possible to obtain with the same accuracy the resonance frequency for the different film thicknesses. The experimental values (black circles) range from ~4.05 $\times$ 10^5 at 300 nm to ~6.60 $\times$ 10^5 at 870 nm. The anisotropic loss factor model (green diamonds) shows excellent agreement, with errors below $\pm$5.5% across all thicknesses. The isotropic model (red squares) deviates by up to +1.7% at 600 nm and has reduced accuracy in thicker films. These results quantitatively confirm that the anisotropic damping model more closely reproduces the measured energy dissipation behavior, particularly in the upper thickness range. The Q-Factor of the value at 610 nanometers deviates from the fit of the experimental values (lower by about 30%) due to the residual stress (in Figure 2, the red cross indicates the expected value around 6 $\times$ 10^5).

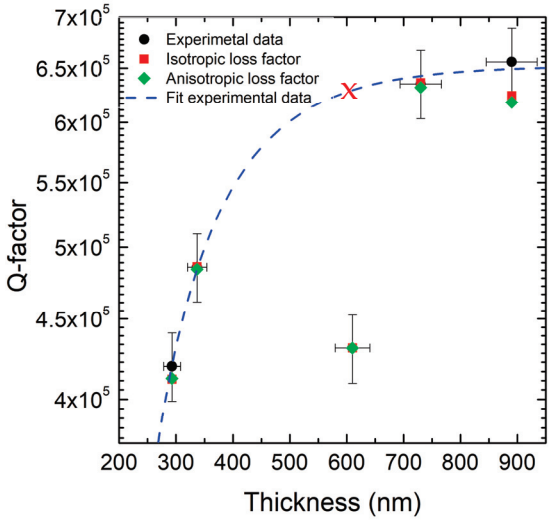

Figure 2. Plot of the Q-Factor as a function of the thickness of a material, expressed in nanometers (nm). The data represent three different conditions: experiment (black), isotropic loss factor simulation (red), and anisotropic loss factor simulation (green). The blue dashed line represents the theoretical fit of experimental data [3]. The red cross indicates the expected value of the experimental Q-Factor for a thickness of 610 nm.

In fact, the experimental data show an increase in frequency with thickness up to around 700 nm, followed by a slight decrease (Figure 3). The isotropic loss factor simulation overestimates the frequency for thinner films but significantly overestimates it for thicknesses

above 600 nm, showing a sharp increase not observed experimentally. In contrast, the anisotropic loss factor simulation closely follows the experimental trend across the entire thickness range, with a larger estimate of the resonance frequency only for the thinner layers. The agreement between experimental data and the anisotropic model is clearly better than with the isotropic one. This suggests that the material exhibits anisotropic behavior and that including anisotropy in the loss factor is crucial for accurately predicting eigenfrequencies. The isotropic simulation lacks key directional mechanical effects or damping mechanisms, which likely become significant at higher thicknesses—hence the large overestimation above 600 nm. The drop in the experimental frequency after 700 nm might be due to additional real-world effects not captured by the simulations, such as tension changes in mechanical properties (i.e., density, Young's modulus) and geometric effects (i.e., increased bending influence at greater thicknesses). The isotropic model systematically overestimates the frequency, with errors of up to +50%, while the anisotropic model shows a better fit with the experimental data.

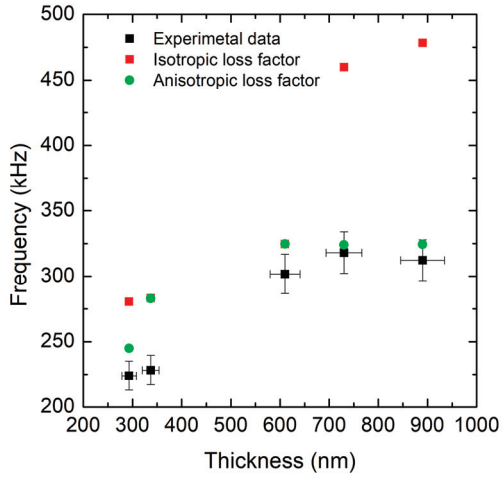

Figure 3. Red curve: COMSOL simulations considering the isotropic loss factor in the eigenfrequency analysis. Green curve (diamonds): COMSOL simulations considering the anisotropic loss factor in the eigenfrequency analysis. Black curve: Experimental data. A mesh convergence study was performed, confirming that the selected mesh parameters yield stable results with less than 1% variation in the first eigenfrequency. (Error bands: 5% for experimental resonance frequency and thickness).

The loss factor matrix (η_D) describes how damping losses vary along different material directions. The eigenvalues (a_{11}, a_{22}, a_{33}, a_{44}, a_{55}) represent the principal damping values along the main anisotropy axes. Specifically, a_{11}, a_{22}, and a_{33} correspond to the x, y, and z directions, respectively, while a_{44} and a_{55} are associated with the shear damping in the yz and xz planes. A summary of the eigenvalues, their associated directions, and the corresponding damping mechanisms is reported in Table 2. In Figure 4, a comparison between these eigenvalues shows how direction dependent the damping is (i.e., $a_{44} >> a_{11} >> a_{22}$ indicates strong damping along few directions). If the plot shows similar eigenvalues ($a_{11} \approx a_{22} \approx a_{33}$), the material is nearly isotropic in damping. If they differ significantly (i.e., $a_{11} > a_{22}, a_{33}$), the material is highly anisotropic, with losses dominated along one direction (e.g., fibers in a composite). In our case, a_{11} (black line) starts with relatively high values (~1.0×10^{-4}), peaking around 400 nm; after 400 nm, the value drops sharply to nearly 0 and remains negligible for thicknesses above 600 nm, indicating that losses along direction x are suppressed as the thickness increases.

The damping along x is dominant in thinner films because under these conditions, the longitudinal direction is the main site of deformation and dissipation. For thicker films, the stiffness along x increases, which means less deformation and dissipation. The red line, a_{22},

sharply increases for the lower thickness, and above 300 nm it almost remains constant (~10^{-5}). The sharp growth for a_{22} observed above 300 nm may signal a new regime, where losses in the y direction are increased, while for higher thickness the anisotropic losses are lower. The transverse direction is a thickness-dependent threshold, participating in dissipation when the flexural modes also involve the y axis. The green line, a_{33}, remains nearly constant over the entire thickness range (~2.5×10^{-5}), suggesting low sensitivity to thickness variations above 300 nm. Furthermore, a_{33} is the most stable, which could suggest that losses in direction z are less sensitive to thickness and generally minimal. The dissipation in the z direction is marginal. The blue line, a_{44}, decreases, reaching a minimum at 600 nm, and, after a slight increase, it stays constant. It then shows shear damping in the yz plane, which is initially significant, and then a slight decrease in thicker films due to the vibration modes' shift from torsion/shear to pure bending. For the cyan line, a_{55}, no great variation in value can be observed in the entire range of film thickness; in the xz plane, the shear damping is thickness independent. The significant reduction in the a_{ij} coefficients, particularly a_{11}, indicates lower anisotropic losses in the system, contributing to increased efficiency (higher Q-Factor).

Table 2. Table of the eigenvalues and related directions and damping.

Eigenvalue	Direction	Damping
a_{11}	x	Direction x
a_{22}	y	Direction y
a_{33}	z	Direction z
a_{44}	yz	Direction yz plane
a_{55}	xz	Direction xz plane

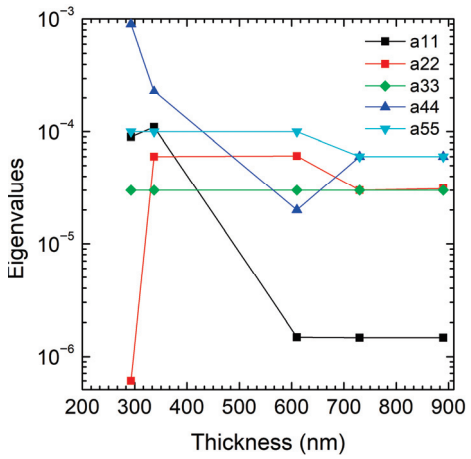

Figure 4. Plot of the eigenvalues as a function of the 3C-SiC film thickness (nm), distinguishing a_{11} (black dots), a_{22} (red dots), a_{33} (green dots), a_{44} (blue dots), and a_{55} (cyan dots).

In many practical applications, the inclusion of damping in eigenfrequency analyses is primarily aimed at estimating the attenuation levels of resonant modes. Although the effect of damping on the mode shapes and eigenfrequencies is often marginal, its accurate implementation is essential for predicting the performance of structures under dynamic loading conditions. The use of a matrix of anisotropic loss factors is particularly advantageous when dealing with systems in which energy dissipation is strongly dependent on material orientation during the propagation of elastic waves; this phenomenon is closely related to the attenuation tensor or the viscosity tensor, which represents the imaginary part of the complex elastic modulus. Compared to the Joffe model [11], this is a micromechanical approach used to predict the effective elastic properties of composite materials. The model

considers the contributions of the fibers and matrix phases, including their volume fractions and orientations, which represents the real part of the elastic modulus. Below, Voigt notation was used to simplify symmetric tensors (like stress/strain) into vectors/matrices as

$$C^* = C + iw\eta_D \tag{2}$$

where C and $\eta \in R^{6\times6}$ are C = real part = conservative elastic matrix and $iw\eta_D$ = imaginary part = attenuation tensor matrix.

Compared to the Joffe model—which focuses on micromechanical predictions of effective elastic properties based on fiber–matrix interactions—the anisotropic damping model used in this study directly incorporates directional energy dissipation through a 6×6 loss factor matrix. While the Joffe model captures the real part of the elastic modulus, our approach targets the imaginary part, which governs attenuation and damping. This distinction allows for more accurate modeling of vibrational decay and resonance behavior in 3C-SiC structures. The anisotropic damping matrix shares conceptual similarities with the viscosity tensor model, often used in wave propagation studies. However, our implementation in COMSOL enables direct integration into FEM simulations, offering better control over directional damping and improved correlation with experimental data. The directional damping captured by the anisotropic model aligns with the known anisotropic stiffness of 3C-SiC, as reported by Thomsen [7] and Yang et al. [8]. The propagation of elastic waves in such materials is governed not only by stiffness tensors but also by attenuation tensors. Our model bridges this gap by incorporating both elastic and dissipative anisotropy, enabling more realistic simulation of wave behavior in MEMS resonators.

By applying compressive forces to the bridge and then producing a compressive strain in the structures, it is possible to simulate the decrease of the resonance frequency for the different samples. From these simulations, in Figure 5a, it is possible to observe that the bridges that have the highest resonance frequency (w_2) and the highest tensile intrinsic stress are less sensitive to the compressive forces and produce the lowest deformation of the bridges. Instead, the thinner bridges, which are also those ones with the lowest tensile stress, show a larger deformation under the same compressive forces.

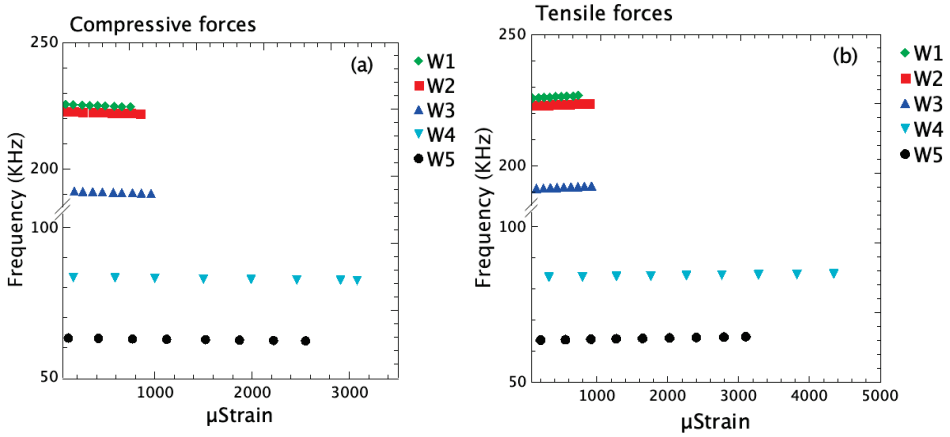

Figure 5. Relationship between μstrain and frequency (in kHz) under compressive force conditions, (**a**,**b**) tensile forces.

The frequency decreases as compressive strain increases. Thicker beams show higher initial resonance frequencies and lower sensitivity to compressive strain. Thinner beams show greater frequency shifts, indicating higher mechanical compliance and lower intrinsic tensile stress. The plot in Figure 5b shows how the strain varies as a function of frequency under the

application of tensile forces. Both w_4 and w_5 samples' configurations [6] show a strong strain response to tensile forces, which is even more pronounced than under compressive forces. The w_5 shows the highest strain among all, suggesting strong mechanical resonance or greater tensile compliance at that frequency. The w_1, w_2, and w_3 series respond weakly under tension, with very small strain magnitudes. The overall strain under tensile loading is higher than in the compressive case for the same configurations (w_4 and w_5), indicating that the material or the structure is more compliant or deformable when pulled than when compressed [12]. The frequency increases with tensile strain and the response is more pronounced than in compression, suggesting that the material is more compliant in tension. The percentage errors between simulated and experimental values for each sample are summarized in Table 3. All values are within ±7%, indicating very good agreement. The anisotropic model used in the simulation appears to accurately capture the strain sensitivity trends across all samples.

Table 3. Table of percentage errors between simulated and experimental values for each sample.

ID Sample	Compressive	Tensile	Error (%)
w_1	0.03	0.028	6.67
w_2	0.04	0.038	5
w_3	0.05	0.048	4
w_4	0.08	0.075	6.25
w_5	0.08	0.085	5.56

The percentage errors between simulated and experimental values are all within ±7%, indicating very good agreement. The anisotropic model used in simulation appears to accurately capture the strain sensitivity trends across all samples.

The graph in Figure 6 shows how the strain sensitivity of the double-clamped beam (expressed in Hz/μstrain) varies as a function of thickness under both compressive (black line) and tensile forces (red line). The strain sensitivity decreases with thickness (up to ~650 nm) for both compressive and tensile forces. This suggests that thinner structures or those with lower residual stress are more sensitive to both types of forces up to this point. Both curves reach a minimum sensitivity at around 650 nm. This indicates that very thin layers with low intrinsic residual stress have the highest strain sensitivity. Tensile sensitivity is consistently higher than compressive sensitivity for each thickness. This means the structure is more responsive to stretching than compression, possibly due to the material characteristics of the tensile strain. The anisotropic model used in the simulation appears to accurately capture the strain sensitivity trends across all samples.

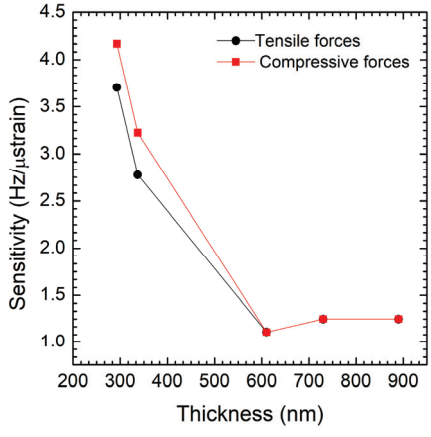

Figure 6. Strain sensitivity (Hz/με) as a function of film thickness (nm) under both compressive (black line) and tensile forces (red line).

In Figure 7, we have shown that for a fixed thickness of 890 nm (w_1), both experimental and simulated frequencies (black and light green, respectively) decrease as length increases. This trend aligns with typical mechanical resonance behavior, where longer structures resonate at lower frequencies. Simulated frequencies are consistently higher than the experimental ones, which may result from ideal conditions assumed in the simulations (i.e., no damping, perfect material properties). The study and the consideration of defect density have already been reported in previous work [3] in which a bilayer model was developed. The 3C-SiC film can be considered a double layer with rich defect density near the interface film/substrate and a high-quality layer above the rich defect, with a reduction of them but not a total elimination. The experimental Q-Factor values (red line) have small fluctuations across most lengths, and the simulated Q-Factor curve (blue line) follows a similar trend because it has been fitted on the experimental values. This suggests that 600 nm is an optimal length for maximizing the Q-Factor, which is crucial for sensing performance and energy efficiency in resonant systems. But, a discrepancy between the simulation and the experiment can be found; while trends are similar, simulated values for frequency are generally higher than the experimental ones.

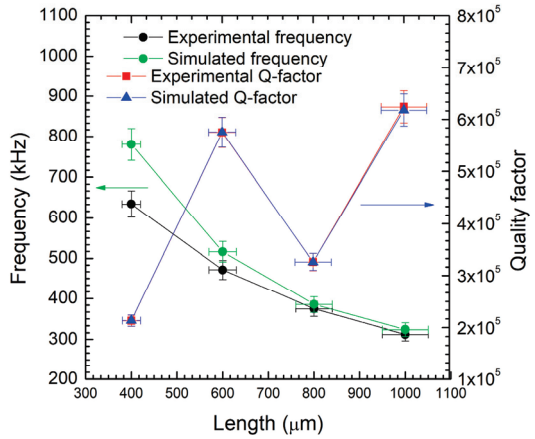

Figure 7. Frequency trends (kHz), both experimental (black line) and simulated (green line), and Q-Factor values, both experimental (red line) and simulated (blue line), as a function of the length (μm).

This discrepancy may arise due to real-world losses (i.e., air damping, fabrication imperfections) not accounted for in the simulations. The figure shows a clear inverse relationship between length and frequency and highlights 600 μm as the optimal length for high Q-Factor performance, both experimentally and in simulations. Despite some quantitative differences, simulation and experimental results are qualitatively consistent, reinforcing the validity of the model and the usefulness of this length for device optimization.

In Figure 8, for both compressive and tensile forces, strain sensitivity decreases as the length increases for a fixed thickness of 890 nm. This trend suggests that shorter structures are more sensitive to external mechanical loading. In a comparison between compressive and tensile forces, the compressive force sensitivity is slightly higher than compressive force sensitivity across all lengths, which is especially notable at intermediate values (e.g., ~700–800 μm). This may indicate that the device responds more effectively (in terms of frequency change) under compressive loading. The figure demonstrates that device length is a key factor influencing frequency-based sensitivity, with shorter devices offering higher sensitivity. Additionally, the system appears to be slightly more responsive under compressive stress, although the difference is relatively small. This information can

be useful when optimizing device geometry for strain sensing applications where high frequency sensitivity is critical.

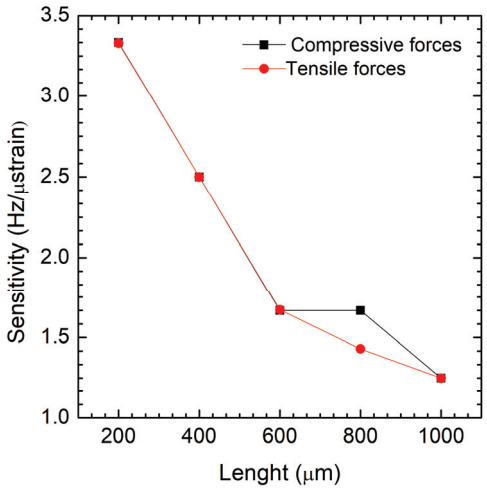

Figure 8. Strain sensitivity (Hz/με) as a function of film length under both compressive (black line) and tensile forces (red line).

4. Discussion

The results of this study make clear the need to include anisotropic damping models in the finite element simulation of 3C-SiC MEMS resonators. Especially for thicker films, better agreement between experimental and simulated resonance frequencies supports the idea that isotropic models cannot adequately represent the directional nature of energy loss in these substances. This finding is consistent with Romero et al.'s (2020) [6] evidence showing that to precisely simulate laminate structures, engineering the dissipation in crystalline micromechanical resonators calls for taking anisotropic loss mechanisms into account in FEM models. Similarly, Somesan and Barti (2020) [2] underlined the need for FEM models with transverse isotropic damping features. These findings support the approach used in this study, whereby COMSOL Multiphysics was presented with anisotropic damping utilizing a 6×6 symmetric loss factor matrix. Furthermore, the mechanical behavior of 3C-SiC beams reported here is consistent with Thomsen's (2014) [7] and Yang et al.'s (2020) [8] findings on the anisotropic elastic properties of silicon and silicon carbide, which emphasize a pronounced stiffness dependence in these materials. The eigenvalue analysis of the damping matrix conducted in this study also supports the claim that energy dissipation is directional and therefore anisotropic modeling is required. The strain sensitivity patterns seen under both compressive and tensile loading also support earlier conclusions. For example, the research by Flis et al. (2025) [9] showed that the precision of FEM simulations might be much impacted by damping coefficients derived from MEMS accelerometers. Showing how strain sensitivity changes with both thickness and length, the current study adds to this knowledge and offers insightful information for the creation of high-performance strain sensors.

Finally, the experimental approach used in this study supports the use of MEMS platforms for mechanical characterization, as discussed by NCSU (2023) [12]. Integrating experimental data with simulations helps one fully grasp the mechanical and damping characteristics of 3C-SiC MEMS devices, therefore guiding the development of more precise and dependable sensor design.

5. Conclusions

In conclusion, by using the anisotropic loss factor, a better prediction of the frequency response of the bridge structures has been made, especially at higher thickness. Through this model, both compressive and tensile forces have been applied to the structures, and it has been observed that higher strain sensitivity can be obtained for thinner layers and for shorter line lengths. The higher sensitivity of the thinner layers is probably related to the fact that these layers present a lower residual stress. The work shows that adding directionally dependent damping models to finite-element runs greatly improves how well those runs predict the dynamic response of tiny mechanical components, with 3C-SiC double-clamped beams serving as a key example. Unlike standard isotropic treatments, the new orientation-specific loss factor matrix captures energy loss linked to crystal direction and beam shape, allowing simulations to mirror reality far more closely. Data show that the anisotropic approach matches experimental measurements more closely, especially when estimating resonance frequencies for beams of different film thicknesses. The gap is largest for thicker layers over 600 nm, where the isotropic scheme misses frequency trends and produces unrealistically large response amplitudes. Eigenvalue analysis of the loss factor map points to the directional nature of damping: energy does not leak out evenly but rather in paths set by the materials' own anisotropy. The findings also stress that overall geometry—thickness, length, and the like—governs how much strain under load, whether pushing or pulling, actually feels like stress. Short, slender samples twist more easily, so their damping rate spikes; in contrast, hefty beams hold residual stress longer and bleed energy slowly. That pattern holds in both tensile and compressive tests, though the tensile case tends to produce sharper rises in sensitivity.

The indications reported in this work can be extremely useful to realize high-sensitivity strain meters.

Author Contributions: Conceptualization, A.M. and F.L.V.; methodology, F.L.V.; software, A.M.; validation, A.M., A.G. and S.S.; formal analysis, A.M.; investigation, A.G.; data curation, A.M.; writing—original draft preparation, A.M. and A.G.; writing—review and editing, A.M., A.G. and F.L.V.; visualization, A.G. and F.L.V.; supervision, F.L.V.; funding acquisition, F.L.V. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: Data will be made available upon request.

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Conflicts of Interest: The authors declare no conflicts of interest.

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SPICE Model for SiC Bipolar Transistor and TTL Inverter Degradation Due to Gamma Radiation

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Abstract: Silicon carbide (SiC) is a key material for electronics operating in harsh environments due to its wide bandgap, high thermal conductivity, and radiation hardness. In this work, we present a SPICE model for a 4H-SiC BJT and TTL inverter exposed to gamma radiation. The devices were fabricated using a dedicated SiC bipolar process at KTH (Sweden) and tested at the ^{60}Co Calliope (Italy) facility up to 800 krad $_{(Si)}$. Experimental data, including Gummel plots and inverter transfer characteristics, were used to calibrate and refine a VBIC-based SPICE model. The adjusted model accounts for both bulk and surface degradation mechanisms by extracting parameters of forward current gain (βF), saturation current (IS), base resistance (RB), and forward transit time (TF). Results show a uniform degradation of BJTs, primarily manifested as reduced current gain and increased base resistance, while the inverter maintained functional operation up to 600 krad$_{(Si)}$. Extrapolation of the SPICE model predicts a failure threshold near 16 Mrad$_{(Si)}$, far exceeding the tolerance of conventional silicon circuits. By linking radiation-induced defects at the material and interface levels to circuit-level behavior, the proposed model enables realistic design and lifetime prediction of SiC integrated circuits for satellites, planetary missions, and other radiation-intensive applications.

Keywords: SiC; SPICE; BJT; transistor; radiation; gamma radiation; IC; inverter

1. Introduction

In this study, we develop a SPICE model for 4H-SiC-based transistor–transistor logic (TTL) bipolar junction transistor (BJT) inverters that are built to handle high gamma radiation levels. Silicon carbide (SiC) is an attractive material for these applications because of its wide bandgap, excellent thermal conductivity, and high electrical field tolerance—features that make it a great candidate for use in aerospace and high-temperature electronics. For a broader review of SiC device applications under harsh environmental conditions, see, for example, [1,2].

An inverter carries out a basic, but crucial, logic operation called a "complementary", or "NOT" operation, which flips an input signal from 0 to 1 or vice versa. Such simple action is key to constructing more complex logic functions. However, logic and integrated circuits (ICs) that are used in extreme environments like outer space, where radiation levels are high, might act very differently compared to their behavior under normal operating conditions. This distinction between device- and circuit-level responses under total ionizing doses has been discussed in depth in [3,4]. Specifically, the way an inverter reacts to radiation can be quite different from how a single transistor responds [5], highlighting the need for

deeper investigation into these differences. Typically, a large number of expensive and time-consuming experiments are needed to assess the impact of different radiation levels on the SiC bipolar ICs, and therefore this research area is not very well-studied [6,7]. In the present work, we propose a way forward to study the impact of gamma irradiation on any SiC-based bipolar IC, without the need for additional experiments, through presenting a SPICE model of SiC bipolar transistors under a wide range of radiation conditions.

The core of this research is about fine-tuning a SPICE (Simulation Program with Integrated Circuit Emphasis) model for BJT and TTL inverters. The findings are not just useful for space tech, but also have applications in nuclear facilities and medical equipment, where electronic components must operate reliably under radiation exposure. The SPICE model helps us to better understand and enhance the durability and performance of SiC NPN inverters, showing that they can be a more reliable choice compared to traditional silicon-based options, and explain their behavior. This study takes a practical step towards improving electronics that can endure some of the toughest environments, both on and beyond Earth. Building on prior work in this domain [5,8,9], our study significantly extends understanding of SiC bipolar circuit low-power ICs. Although silicon carbide (SiC) is known for its advantages in high-temperature and radiation-rich environments [9–12], the literature on modeling SiC TTL inverters for such extreme conditions remains fragmented. Introducing SPICE models for SiC transistors under gamma radiation exposure addresses existing research gaps, offering a new perspective on designing radiation-hardened integrated circuits.

It is demonstrated that the effect of gamma rays is much lower for these chips than for corresponding Si circuits. Using our verified SPICE model shows that the inverter should be in operation even for doses far exceeding 16 $MRad_{(Si)}$.

The choice of the BJT structure over the more common Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is motivated by two key factors. First, SiC BJTs are inherently more resistant to radiation than their MOSFET counterparts [13,14]. Their bipolar structure relies on minority carrier injection (diffusion current) and does not depend on an inversion channel at the SiC/SiO_2 interface, which is a critical point of failure in MOSFETs due to radiation-induced charge trapping [3,13,14]. Second, this specific research builds upon a well-established and mature SiC bipolar process technology available at KTH [5,6,10], allowing for robust device fabrication and comparative analysis with existing data. Therefore, the BJT platform provides a superior foundation for developing radiation-hardened integrated circuits.

2. Experimental Section

2.1. Device Processing and Design

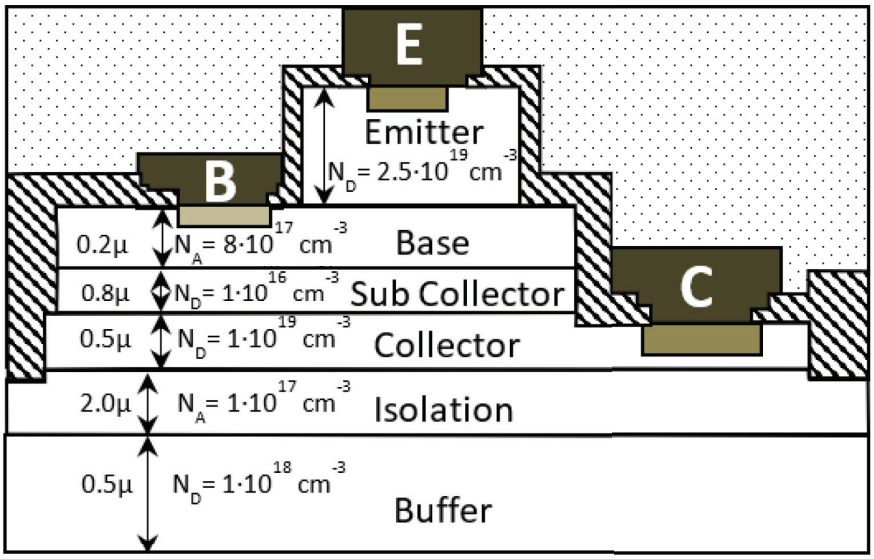
2.1.1. Discrete 3-Pad Devices

The SiC bipolar devices and integrated circuits were fabricated at the MyFab Electrum Laboratory, located at the KTH Royal Institute of Technology in Kista, Sweden. The manufacturing process adhered to a procedure that replicates the steps outlined in the referenced process descriptions [8,9,15,16].

The initial material used for processing was 100 mm, 4° off-axis, 4H-SiC n-type conducting wafers from Cree™. These wafers feature multiple epitaxial layers that were grown in a single sequence to reduce interface states between the layers. The cross-sectional structure of a single transistor is depicted in Figure 1.

The first epitaxial layer (bottom), known as the buffer layer (0.5 μm, $N_D = 1 \cdot 10^{18}$ cm^{-3}), is utilized to minimize defect formation during epitaxial growth. Subsequently, the p-type isolation layer (2 μm, $N_A = 1 \cdot 10^{17}$ cm^{-3}) serves to effectively isolate individual devices, owing to its substantial p-type doping concentration. The subsequent layers adhere to a standard design for low-voltage bipolar transistors: an n+ collector for contacts

(0.5 μm, $N_D = 1 \cdot 10^{19}$ cm^{-3}), a lower-doped sub-collector that blocks voltage (0.8 μm, $N_D = 1 \cdot 10^{19}$ cm^{-3}), a medium-doped p-base (0.2 μm, $N_A = 1 \cdot 10^{17}$ cm^{-3}), and a highly doped n+ emitter (2 μm, $N_D = 2.5 \cdot 10^{19}$ cm^{-3}) to complete the structure. The buried collector layers are positioned to establish low-resistance ohmic contacts with the lightly doped collector layers situated above them. The doping level and thickness of the base layer plays critical role in determining the device's gain, while the lightly doped collector layers are influencing the device's breakdown voltage. The top layer, the highly doped emitter layer, significantly enhances emitter injection efficiency and simultaneously reduces contact resistance, contributing to the overall performance of the device. The NPN transistors undergo a fabrication process involving three dry-etching steps, each designed to isolate the emitter, base, and collector regions, respectively. In the context of this research, it is important to clarify that a sacrificial thermal oxidation step is undertaken to remove approximately 10 nm of damaged SiC resulting from the dry-etching process. The entire surface is then passivated by a PECVD oxide layer, which is subsequently annealed in a N_2O environment (1100 °C, 5 h). The interconnections are made from TiW to increase the temperature tolerance of the devices [5] and investigate the radiation response of the interconnected materials. The thickness of the metal is 2 μm, processed in 2 steps.



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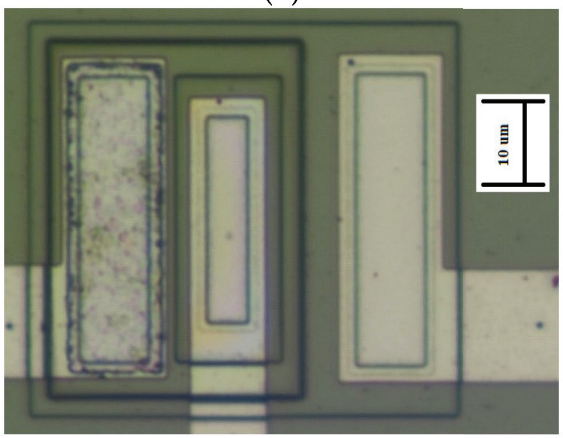

(**b**)

Figure 1. (**a**) The cross-section of the device (not scale), with the substrate and epitaxial layers' cross-sections; (**b**) a top-view of the transistor contact layout.

2.1.2. Inverter Design

The transistor–transistor logic (TTL) inverter is a foundational component in digital integrated circuits (ICs), essential for manipulating logical states. Due to the inherent TTL architecture, only NPN transistors are required for its implementation. The schematic of the designed TTL inverter, implemented with 4H-SiC BJTs, is depicted in Figures 2 and 3 [16]. This circuit comprises three primary stages characteristic of standard TTL configurations:

1. First Stage (Input Gate—Transistor Q_1): This stage functions as the input gate. In this design, an emitter transistor Q_1 is utilized to efficiently manage incoming signals.
2. Second Stage (Phase Splitter—Transistor Q_2): This stage's primary role is to invert and split the phase of the logic signal received from the first stage, preparing it for the final output stage.
3. Third Stage ("Totem-Pole" Output Configuration—Transistors Q_3 and Q_4): This crucial stage is implemented as a "totem-pole" output configuration, comprising two transistors (Q_3 and Q_4) that operate in a complementary fashion. This design ensures low output impedance in both high- and low-logic states. For instance, in the logic-high output state, transistor Q_3 is "ON", while Q_4 is "OFF", thereby driving the output to the desired logic level. Conversely, for a logic-low output, Q_3 is OFF and Q_4 is ON.
4. Diode Representation: In the schematic, the diode, typically present in TTL for level shifting, is replaced by an NPN transistor with its collector shorted to the base. This configuration ensures that the diode voltage drop precisely matches the base–emitter voltage drop of the subsequent transistor, optimizing signal levels.

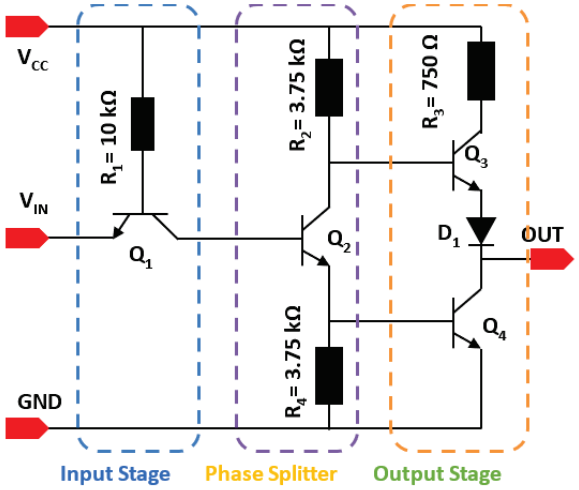

Figure 2. Schematic of the SiC TTL inverter.

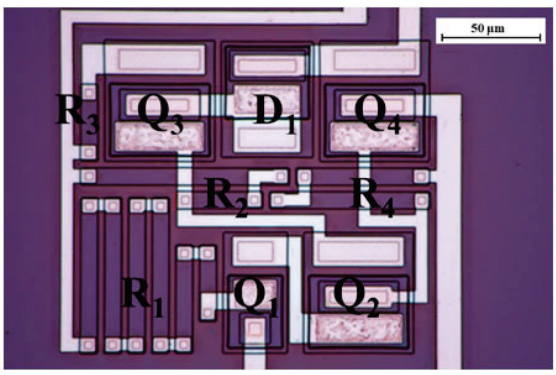

Figure 3. Corresponding layout of SiC inverter.

Figure 2 also presents the corresponding layout (top-view) of the SiC TTL inverter, illustrating the physical arrangement of the components on the chip.

2.2. Radiation Testing Facility and Conditions

Gamma radiation experiments were conducted at the ^{60}Co Calliope facility [17] with a photon mean energy of 1.25 MeV. A key advantage of this facility is that materials tested here do not become radioactive, allowing for immediate handling after irradiation. To ensure precise radiation dosing, we used the ESR–alanine dosimetry method. To combat issues like Compton backscattering from the lower-energy photons in the ^{60}Co spectrum, we added extra shielding, which included a 2 mm thick aluminum box topped with a 2 mm aluminum/lead lid to protect the devices under test (DUTs).

The devices were tested across a range of gamma ray doses and dose rates, employing an aluminum/lead (Al/Pb) filter to adjust the doses to the expected radiation conditions in space. The radiation dose rate was maintained at 9.975 $rad_{(Si)}$/s throughout the experiments at the DUTs.

Due to high energy of the photons and an activity of approximately 10^{13} Bq in the facility, we had to use long (18 m) lines in a 4-wire scheme to save the supply and measurement equipment. The experiment was performed under normal environment conditions. All measurements were conducted at a temperature of approximately 21 °C.

Since the project was carried out as part of space research, the following test doses presented in Table 1 are considered reasonable.

Table 1. Total ionizing dose benchmarks.

Environment	Duration	Typical TID ($rad_{(Si)}$)	Est. Dose in SiC ($rad_{(SiC)}$)
LEO (ISS)	1 year	~3000	~1500
GEO	5 years	~50,000	~25,000
Jupiter orbiter	1 year	~200,000	~100,000
Lunar Base	10 years	~15,000	~7500

Thus, a dose of 800 $krad_{(Si)}$ sufficiently covers (with an operational time and safety margin) the majority of missions that are not aimed at studying the sun and near-solar space.

2.3. Measurement Procedure

The testing of the devices was in adherence to semiconductor industry standards (MIL-STD-883L and MIL-STD-750 (Method 1019.9)) [18,19]. We assembled the setup such that these tests were performed in real-time with a remote setup that enabled both operation and immediate in situ characterization post-exposure. This method provides a clearer picture of gamma radiation's impact compared to previous approaches [5,6].

We conducted electrical measurements using National Instruments^{TM} equipment, taking special care to shield against radiation-induced noise and maintain calibration accuracy. The system comprised an NI PXIe-1078 chassis, a PXIe-4081 digital multimeter (DMM), two PXIe-4136 source-measure units (SMUs), a PXI-4110 programmable DC power supply, and an NI PXIe-2532 switching matrix. Due to the presence of a radiation field in proximity to the device under test (DUT), measurements were conducted remotely. We utilized 18.7 m shielded cables to minimize noise interference. Our protocol ensured that exposure times were always ten times longer than measurement durations to improve the reliability of our results. We documented the direct current (DC) characteristics of the SiC BJTs, keeping a steady V_{CC} of 15 V and varying V_{IN} from 0 to 15 V. We also

implemented a trimmed mean method to cut down on noise, which was particularly effective given the long cable lengths in our setup. To ensure measurement accuracy, each voltage and current value was sampled seven times. Subsequently, the highest and lowest 15% of the samples were discarded, and the mean of the remaining values was calculated. This averaging technique facilitated the measurement of low currents despite the use of extended cable lengths. Due to the remote measurement configuration and the implementation of quality control procedures, the duration of each test iteration, following radiation exposure, was 2 min. The radiation exposure time was set to be at least ten times greater than the measurement time, maintaining a critical 10:1 ratio between exposure and measurement periods.

The system was programmed to perform standard DC characterization tests, including Gummel plots and measuring I_C-V_{CE} output characteristics. For the Gummel plot measurements, the collector–emitter voltage (V_{CE}) was held constant at 15 V, while the base–emitter voltage (V_{BE}) was swept from 0 V to 15.6 V. Due to constraints imposed by the radiation environment and the use of extended cabling, a relatively large V_{BE} step size of 0.2 V was employed. A current compliance limit was enforced at 1 A for each terminal, with automatic adjustment capabilities to ensure adequate current resolution.

3. Results

3.1. Experimental Results from SiC BJT

Bipolar transistors, by their design properties, show higher radiation hardness compared to MOSFET devices [20,21]. This distinction arises from the specific mechanisms of current flow and voltage application in the crystal structure. While the basic mechanisms are presented in [21–24], this work focuses on the practical aspects of transistor behavior. In operational scenarios, transistors are predominantly used in the amplification mode (common-emitter configuration), or as logic switches. More detailed discussions are presented in [8,9]. The inverter behavior and experimental results are discussed in [25].

In Figure 4 the measured Gummel plot and amplification β of a typical transistor in our inverter as a function of increasing gamma exposure up to 800 $kRad_{Si}$ are shown. The dose rate for this measurement was kept at 9.975 $rad_{(Si)}/s$. As can be seen, the effect of the radiation can barely be seen on the logarithmic Gummel plot (Figure 4a), but the change in the amplification, although small, is clearly distinguished on a linear scale (Figure 4b).

The general characteristics of the devices align, to a large extent, with those of silicon-based transistors. However, for our SiC-based devices, due to the higher bandgap energy E_g, the TURN-ON processes start at higher voltages and there is a higher impact of base current observed in the high base–emitter voltage range. This phenomenon can be attributed to the geometric ratio between the emitter and base regions [26]. However, the observed characteristics enable the attainment of optimal base-to-collector current ratios, serving as a critical metric of transistor amplification efficiency. Since it is difficult to determine and analyze the data, and also because the main parameter/criterion is the current amplification β, we will look at the β characteristics in a separate figure.

The onset of base current dominance, where the collector current approaches saturation, is identified as an inherently unstable operating region. This variability is strongly influenced by deviations in the geometric accuracy of the transistor structure, which is determined by the quality of fabrication processes. Particular attention should be given to the slope of the collector top and the wall profiles of the transistor regions, as these parameters critically affect base performance.

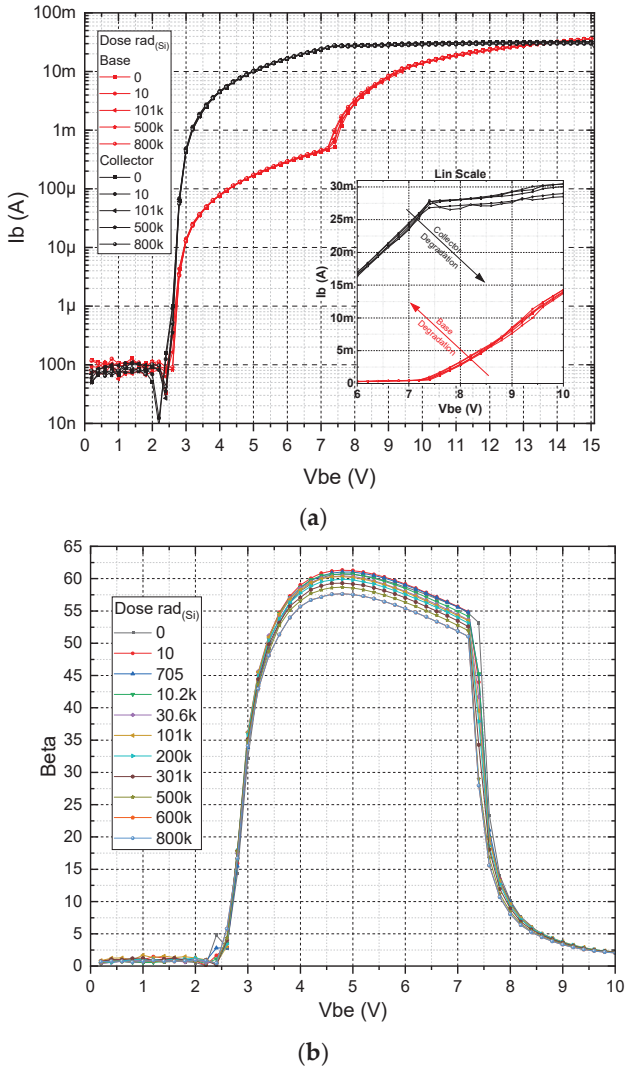

Figure 4. (**a**) Typical experimental Gummel plots for an integrated SiC BJT under various gamma doses. (**b**) Measured amplification factor β as a function of base–emitter voltage for increasing gamma ray exposure time.

3.2. SPICE-Simulated SiC BJT Characteristics

For the simulation of device characteristics, the NI Multisim v. 12 was used, which is built upon an advanced SPICE simulation engine. The VBIC (Vertical Bipolar Inter-Company) BJT [27,28] model was selected as it provides a comprehensive framework that includes parameters to account for non-ideal effects such as the Kirk effect at high injection levels and recombination phenomena at the emitter and collector junctions. These factors are essential for the modeling of SiC devices.

To ensure the accuracy of our simulations, the VBIC model's parameters were adjusted to align with the initial experimental data from our non-irradiated SiC BJTs. This initial calibration allowed us to establish a baseline model that accurately represents the experimental characteristics of the real devices. The extracted parameters from this process are provided in Appendix A. This calibrated model then served as a foundation for predicting the effects of very high gamma ray irradiation.

3.2.1. Initial SPICE Model Calibration

Figure 5 presents the characteristic behavior of the base and collector currents for the ideal SPICE-simulated SiC transistor for gamma doses up to 800 $kRad_{Si}$.

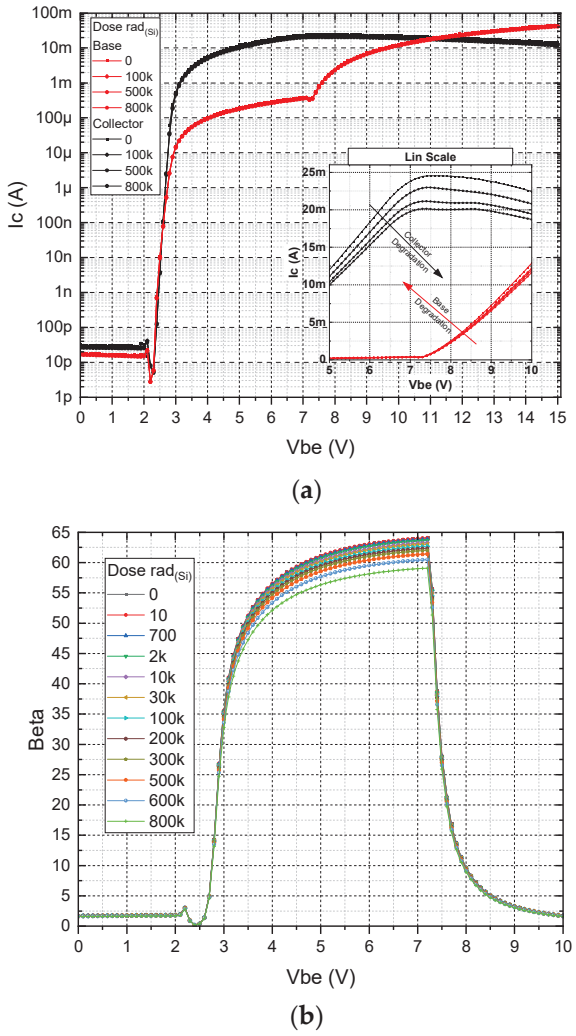

Figure 5. (**a**) Simulated ideal Gummel plot for SiC BJT under various gamma doses. (**b**) Simulated amplification factor β as a function of base–emitter voltage for increasing gamma ray exposure time.

Under ideal conditions, the dynamic behavior of the base and collector currents aligns closely with simulated results, demonstrating agreement in both the linear and saturation regions of operation. But with an extra part in the higher voltages 5.0–7.1 V it still increases, with a fast ramp-down after 7.1 V due to the boost of I_b, causing a rapid drop in β at voltages higher than 7.1 V.

When comparing the β behavior for experimental and simulated SiC BJTs, shown in Figures 4b and 5b, it is also evident that the there is a clear deviation at a V_{be} of about 5 V, where the measured values begin to drop while the simulations show an increased β. Ideally, beta should grow until the base current sharply overlaps the collector current.

The observed divergence in beta profiles at peak values is primarily attributable to common model imperfections, particularly the omission of coefficients accounting for interface irregularities and recombination losses at junction boundaries.

3.2.2. SPICE Adjustment

We focused on extracting both bulk- and surface-related [28–30] SPICE parameters: the saturation current (*IS*), the emission coefficient (*NF*), the surface generation current (*ISE*), and its corresponding ideality factor (*NE*). Additionally, the static current gain β was calculated for each dataset. The total collector current was modeled using a nonlinear fit of the following expression:

$$Ic = IS \times \exp\left(\frac{Vbe}{NF \times VT}\right) + ISE \times \exp\left(\frac{Vbe}{NE \times VT}\right)$$

where *VT* is the thermal voltage at 21 °C.

This equation is based on a modified version of the Gummel–Poon model [27] and its modification [28] and adjusted for two primary contributions to the total collector current, each corresponding to a distinct physical phenomenon:

Bulk Component: The first term, arising from Compton scattering, describes the ideal diffusion current through the bulk semiconductor region. Here, *IS* is the ideal saturation current and *NF* is the emission coefficient, which deviates from unity to account for non-ideal recombination effects within the bulk.

Surface Component: The second term is included to model non-ideal recombination currents at the device's surfaces and interfaces, particularly at the emitter–base junction's sidewalls. *ISE* represents the saturation current associated with these surface effects, while N_E is the corresponding ideality factor. This component becomes especially significant under conditions where surface degradation and trap generation are prominent, such as after exposure to ionizing radiation.

The use of this dual-exponential model is crucial for our study as it provides a framework for disentangling the effects of bulk and surface degradation. By fitting our experimental data to this model, we can individually track the changes in parameters like *IS*, *NF*, *ISE*, and *NE*, thereby gaining deeper insight into the physical mechanisms of radiation-induced degradation in the SiC BJTs. This approach allows for a precise analysis of how radiation-induced defects in both the semiconductor bulk and at the SiC/SiO_2 interface affect device performance.

In Figure 6, we compare the β values of the SiC BJT before exposure to the "standard", as well as the adjusted SPICE models.

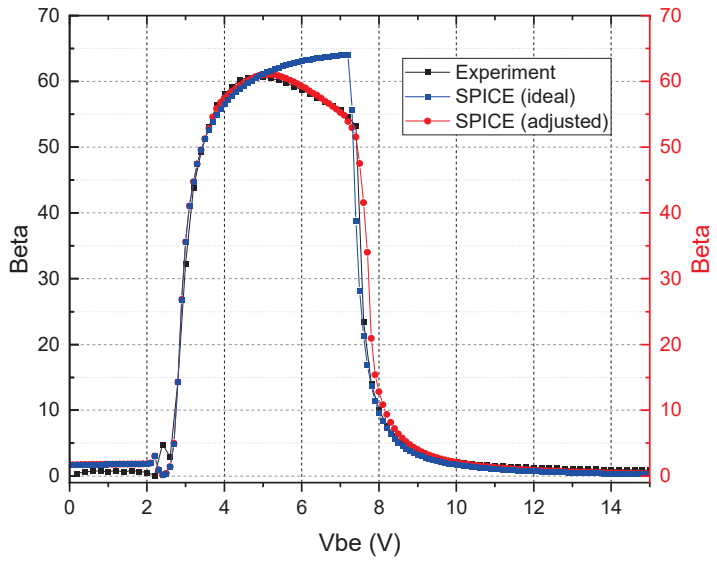

Figure 6. Comparison of ideal vs. experimental beta curves before radiation exposure.

3.2.3. Comparing SiC BJT Measurements and Initial and Adjusted SPICE Models

To understand the specifics of the degradation itself, its mechanisms and modes, we will refer to the work in [8]. It should be noted that the degradation is uniform. This paper presents the beta characteristics for the initial point (before irradiation) and the final irradiation point (800 $krad_{(Si)}$). The beta degradation plots are presented in Figure 7, where experimental curves are shown in gray, while SPICE-modeled beta characteristic curves for different doses are shown in various shades of red.

The comparison between experimental and SPICE model results underscores the challenges associated with developing accurate circuit-level models. The divergence in beta characteristics reflects the natural variability inherent in experimental conditions. Specifically, the initial beta increase (observed in the first measurement points) can be attributed to induced noise within the high-radiation environment, which affects both the DUT and associated transmission lines.

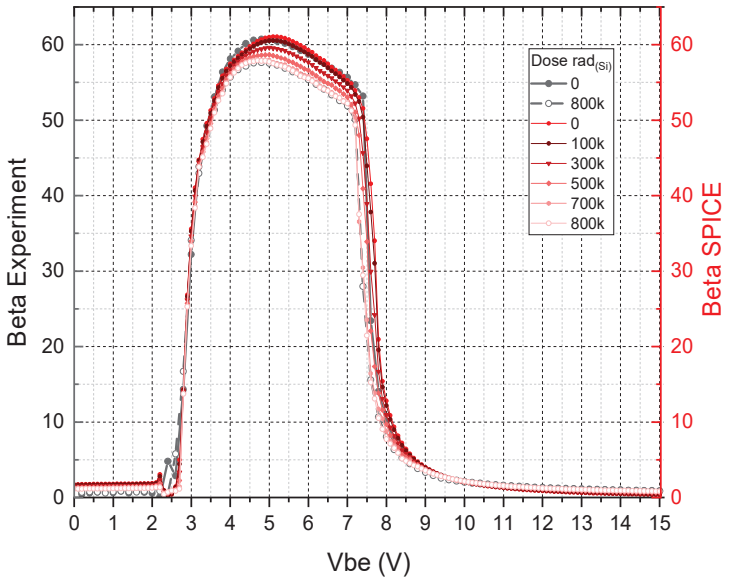

Figure 7. Degradation of beta during radiation exposure: experimental vs. (adjusted) SPICE model.

Despite these challenges, the results validate the robustness of the proposed model for engineering evaluations. The outcomes demonstrate the suitability of the approach for predicting transistor behavior under radiation exposure, offering valuable insights for the design of radiation-hardened integrated circuits.

To effectively design integrated circuits, accurate circuit-level models are essential for the included components. Given that the current gains and collector resistances of SiC BJTs can vary widely based on their design and manufacturing processes, it is necessary to develop a custom model or a series of models tailored to the observed electrical behaviors of the BJTs in question. When incorporating a newly designed BJT, the methodology depends on calibrated physical device simulations that forecast the electrical characteristics of the BJT.

The accuracy of the models is important for the design of analog and digital circuits, especially when specific criteria for power consumption are to be met; thus, selecting appropriate reference devices and accurately calibrating the simulation models are vital steps.

The VBIC model [31] was chosen for its ease of integration into SPICE and its capability to approximate bipolar transistor behaviors accurately with minimal parameters. The extraction process is further streamlined due to the straightforward physical interpretation of its parameters, reducing both complexity and time investment. The estimated values of

the parameters and their physical meaning are presented in Appendix A. The dynamics of maximum beta degradation and the convergence of experimental results and SPICE modeling are shown in Figure 8. The y-scale focuses on the β peak region and shows a very good fit between the experiments and simulations.

Based on the data in Appendix A, we note the dynamics of the main physical parameters, thanks to which it was possible to achieve a good match between the experimental results and the SPICE model.

The forward current gain β_F is found as follows:

$$BF(D) = BF_0 \cdot exp\left(-1.15 \times 10^{-5} \cdot D\right)$$

The saturation current I_S is found as follows:

$$IS(D) = IS_0 \cdot exp\left(ln(10) \cdot 4.3 \times 10^{-6} \cdot D\right)$$

The base resistance R_B is found as follows:

$$RB(D) = RB_0 \cdot \left(1 + 2.86 \times 10^{-6} \cdot D\right)$$

The forward transit time TF is found as follows:

$$TF(D) = TF_0 \cdot \left(1 + 2.14 \times 10^{-6} \cdot D\right)$$

Parameters with 0 index (BF_0, IS_0, RB_0, TF_0) are initial values before the exposure. D—Number for the total dose in krad$_{(Si)}$.

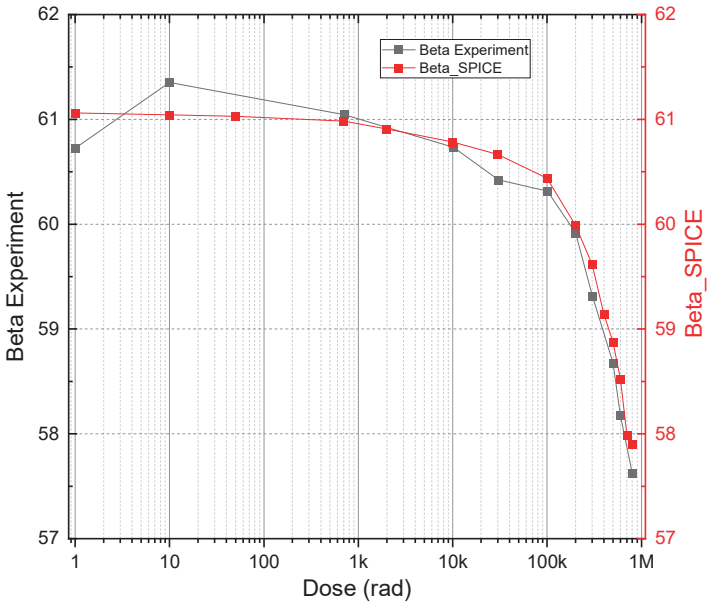

Figure 8. Dynamics of experimental and SPICE model maximum beta degradation.

3.3. Inverter Results

Due to experimental imperfections, data could only be obtained up to 600 krad$_{(Si)}$ on the same wafer as the transistor presented above.

A more detailed look at the experimental results and the physical mechanisms of degradation under radiation is presented in [9]. The measurement method and control of the central point of the "butterfly" were described in [32,33].

Figures 9 and 10 show the character of the inverter's degradation and the convergence of experimental results with the SPICE model.

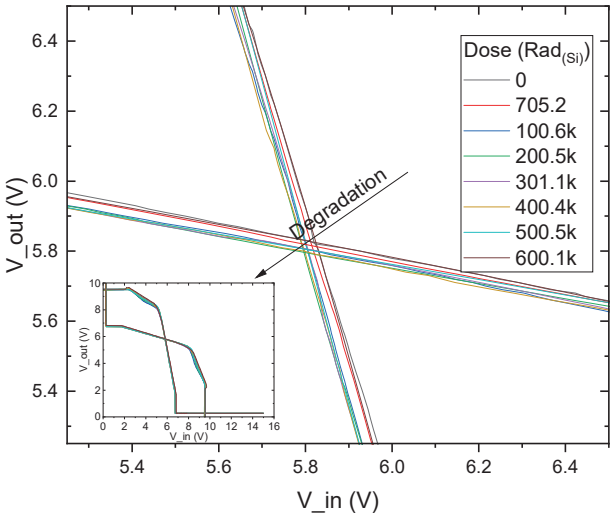

Figure 9. Inverter transfer characteristic degradation with radiation dose. The figure shows the central cross-cover of the transfer characteristics—input voltage versus output voltage. The inset shows the full characteristics.

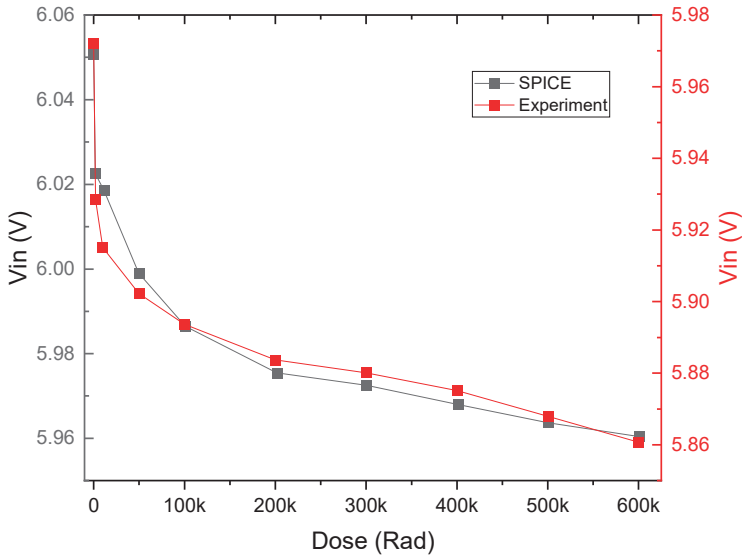

Figure 10. Inverter degradation with radiation dose: experimental vs. SPICE model.

Approximation of the model results showed the following.

For the transistor:

- $BF(D) = BF_0 \cdot exp(-4.21 \times 10^{-6} \cdot D)$
- $IS(D) = IS_0 \times 3.75 \times 10^{-46} \cdot exp(1.47 \times 10^{-5} \cdot D)$
- $RB(D) = RB_0 + 0.221 \cdot D$
- $TF(D) = TF_0 \cdot (1 + 2.14 \times 10^{-6} \cdot D)$

For the diode:

- $ISdiode(D) = 3.75 \times 10^{-46} \cdot exp(1.47 \times 10^{-5} \cdot D)$
- $N_{diode}(D) = 1.55$

Within the investigated range up to 600 krad$_{(Si)}$, the inverter maintains acceptable operation: the switching midpoint only shifts slightly, and both high- and low-level plateaus

remain distinct. Similar dose thresholds for silicon circuits are typically reported in the range of 10–100 $krad_{(Si)}$ [34,35]. To define a quantitative limit for inverter usefulness, we introduce a failure criterion corresponding to a 30% reduction in the switching midpoint with respect to its initial value.

Extrapolation of the dose-dependent by presented SPICE model gives a value to failure of the device in the order of approximately 16 $Mrad_{(Si)}$.

Analysis shows that the radiation degradation of the SiC-based inverter is primarily associated with changes in the BJT. A decrease in the current gain (BF) and an increase in the base resistance (RB) and transit time (TF) are the main factors that degrade the switching speed and reliability of the circuit. At the same time, the diode part of the inverter shows high radiation resistance, which makes it a more predictable element. This data is critically important for creating an accurate SPICE model capable of predicting the inverter's behavior under radiation conditions and, thus, contributing to the development of radiation-hardened integrated circuits.

4. Discussion

Analysis of the extracted SPICE parameters revealed clear signs of degradation as a function of the accumulated radiation dose, indicating damage occurring both in the bulk semiconductor and at the device interface. The observed changes were categorized into three primary degradation mechanisms, each impacting different aspects of inverter performance. We will first discuss the different effects of gamma rays on individual BJTs and then conclude on the total degradation effects of the whole inverter circuit.

Deterioration of Amplification and Switching Properties

The most significant changes were observed in parameters governing current amplification and switching speed. The forward current gain (β_F) was found to decrease with increasing dose, which is a direct physical consequence of an increased number of recombination centers within the base region. These radiation-induced defects shorten the minority carrier lifetime, consequently reducing the carrier transfer coefficient and leading to a substantial decrease in amplification efficiency. Simultaneously, the transistor's switching speed was affected by a linear increase in both base resistance (RB) and forward transit time (TF) with increasing radiation dose. An increase in RB slows down the charging and discharging of junction capacitances, while an increase in TF is directly linked to the reduced carrier lifetime. The combined effect of these factors leads to a pronounced decrease in the overall switching speed of the transistor, limiting its applicability in high-frequency circuits.

Increase in Leakage Currents and Power Consumption

Degradation was also evident in parameters related to leakage currents. The saturation current (IS) showed moderate fluctuations with dose. In some cases, IS increased, likely due to the generation of radiation-induced traps in the p-n junctions, leading to higher leakage currents and degraded energy efficiency. Conversely, a decrease in IS was observed in other instances, which may be attributed to a complex redistribution of internal fields. The emission coefficient (NF), indicating the ideality of the bulk emitter junction, increased significantly with dose, suggesting a strong deviation from ideal carrier transport caused by enhanced recombination via the Shockley–Read–Hall (SRH) mechanism in the base region [29].

Impact of Surface-Related Degradation

Even more pronounced changes were observed in parameters related to surface effects: ISE and NE. The surface generation current (ISE), which was negligibly small in the unirradiated state (ISE $\approx 1 \times 10^{-15}$ A), increased by more than three orders of magnitude at doses above 400 krad, reaching approximately 1×10^{-11} A. Simultaneously, the surface

emission coefficient (NE) sharply increased, exceeding values of 90. These dramatic shifts indicate a highly non-ideal and severely degraded surface recombination process, directly pointing to significant degradation of the SiC/SiO_2 interface [5,29,30] and underscoring the critical vulnerability of the device's surface to radiation damage. Similar surface-related degradation phenomena have been reported for SiC/SiO_2 interfaces under TID stress from charged particles as protons and ions, which are common in near-Earth space [36,37].

The physical interpretations of the steep increase in ISE and NE with radiation dose are consistent with established mechanisms of interface degradation in wide-bandgap semiconductors. Gamma irradiation induces positive fixed charges and interface traps both in the gate oxide and at the SiC/SiO_2 interface. These trapped charges distort the local electric field near the base–emitter junction, which in turn enhances recombination through interface states.

The buildup of positive charge in the oxide attracts electrons and alters the electric field, increasing leakage and generation currents, especially under low-injection conditions. The deviation from exponential I_c behavior at low V_{be} values confirms the presence of shallow-level traps and a high density of interface states. These effects are accurately captured by the sharp increases in I_{SE} and N_E, making these parameters reliable markers of interface degradation.

Degradation of the full SiC-based inverter is a direct consequence of the accumulated changes in the characteristics of its transistor bases. While the diode in the circuit demonstrates high radiation hardness (its ideality coefficient and junction capacitance remain stable), the degradation of the BJT determines the overall performance reduction in the inverter. In multi-stage circuits where transistors operate in series or parallel configurations, the degradation of each individual component cumulatively affects the behavior of the entire circuit.

The increase in base resistance (RB) and forward transit time (TF) in each transistor leads to a cumulative increase in switching delays, which critically reduces the maximum operating frequency of the entire inverter. The significant decrease in forward current gain (BF) impairs the current-amplification properties, which can lead to incomplete saturation of transistors, distortion of output logic levels, and a reduction in the noise margin. Furthermore, the increase in leakage current (IS) in each transistor of the circuit leads to a cumulative increase in the total static power loss of the entire inverter, reducing its overall energy efficiency.

Overall, the changes observed in the SPICE model parameters form a direct and physically meaningful link between the radiation-induced effects at the material level and the observable behavior at the circuit level. This enables more accurate modeling and reliability assessment of SiC BJTs operating in radiation-intensive environments.

However, it is important to acknowledge the limitations of the proposed SPICE model. The parameters were extracted from DC characteristics and, while accurately reflecting the TID effects on circuit performance metrics like current gain, the model does not explicitly account for two important factors:

First, the model is a "DC-centric" characterization and does not directly incorporate the dynamic effects or other transient phenomena. While the increase in the mentioned parameters predicts slower switching, a full model would require dynamic testing and more complex parameterization.

Second, the model is calibrated for a specific device geometry and fabrication process at KTH. While the physical mechanisms captured (bulk and surface recombination) are general, the precise dose-dependent expressions for BF, IS, RB, and TF are empirical and may require re-calibration for SiC BJTs from different fabs or with different designs/processing flows.

Despite these limitations, the model provides a highly practical, accurate, and efficient engineering tool for predicting the radiation hardness and reliability of SiC integrated TTL circuits for harsh environments.

5. Conclusions

In conclusion, we have developed and validated a SPICE model that accurately predicts the impact of gamma radiation on both individual integrated SiC BJTs and complex TTL inverters. The model's robustness and predictive power have been confirmed through a comprehensive comparison with experimental data. This work represents a significant step forward in understanding the degradation mechanisms of SiC-based integrated circuits in radiation-intensive environments. It is important to note that the model successfully demonstrated its applicability and accuracy for the devices described in the article, while also laying a methodological foundation for future research.

The analysis confirms that the primary cause of performance and reliability degradation in SiC inverters under radiation is the complex, cumulative degradation of their transistor components. We have demonstrated that the key parameters of the BJT model, such as forward current gain (BF), base resistance (RB), and saturation current (IS), show a clear and predictable dependence on the total ionizing dose. These patterns underscore the critical necessity of creating highly accurate SPICE models that can adequately account for radiation-induced parameter changes.

The experimental data and their precise alignment with our SPICE models highlight the importance of meticulous parameter tuning for ensuring the reliable operation of transistors in such harsh conditions. This achievement not only provides a foundational tool for the design of robust, radiation-hardened integrated circuits but also paves the way for further refinements in modeling methodologies and their broader application. Our findings also convincingly demonstrate the clear advantage of SiC TTL circuits over current Si technology, which is a pivotal step toward enabling a new era of reliable electronics for the exploration of space and other extreme environments.

With the well-calibrated model presented here, the projected "killing" dose for the SiC TTL inverter—defined as a 30% reduction in the switching midpoint—is approximately 16 $Mrad_{(Si)}$, i.e., orders of magnitude beyond typical silicon logic, which commonly exhibits functional degradation/failure in the 10–100 $krad_{(Si)}$ range [33,34].

Comparable findings regarding silicon logic degradation have been reported in [34,35], underscoring the relative robustness of SiC designs.

Author Contributions: Conceptualization, A.M. and A.H.; Methodology, A.M.; Software, A.M.; Validation, A.M.; Formal analysis, A.M.; Data curation, A.M.; Writing—original draft, A.M.; Writing—review & editing, A.M., A.H. and C.-M.Z.; Visualization, A.M.; Supervision, A.H. and C.-M.Z.; Project administration, C.-M.Z. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The original contributions presented in this study are included in the article. Further inquiries can be directed to the corresponding author.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

Table A1. Gummel transistor parameters as functions of radiation dose in rad.

SiC BJT SPICE Parameters								
Parameter	**Models**	**Units**	**0**	**100 k**	**300 k**	**500 k**	**700 k**	**800 k**
bf	Ideal maximum forward beta	-	75	38.49	25.37	21.47	19.75	18.17
is	Transport saturation current	[A]	3.75×10^{-46}	9.42×10^{-44}	2.98×10^{-42}	1.19×10^{-41}	2.37×10^{-41}	4.72×10^{-41}
vaf	Forward early voltage	[V]	600					
var	Reverse early voltage	[V]	45					
rb	Zero-bias base resistance	[Ohm]	1.40×10^{4}	3.64×10^{4}	5.04×10^{4}	5.60×10^{4}	5.88×10^{4}	6.16×10^{4}
TF	Forward transit time		1.05×10^{-10}	2.31×10^{-10}	3.10×10^{-10}	3.41×10^{-10}	3.57×10^{-10}	3.73×10^{-10}
vaf	Forward early voltage	[V]	600					
var	Reverse early voltage	[V]	45					
Inverter								
Parameter	**Models**	**Units**	**0**	**100 k**	**300 k**	**500 k**		**600 k**
bf	Ideal maximum forward beta	-	75	38.49	25.37	21.47		19.75
is	Transport saturation current	[A]	3.75×10^{-46}	9.42×10^{-44}	2.98×10^{-42}	1.19×10^{-41}		2.37×10^{-41}
vaf	Forward early voltage	[V]	600					
var	Reverse early voltage	[V]	45					
rb	Zero-bias base resistance	[Ohm]	1.40×10^{4}	3.64×10^{4}	5.04×10^{4}	5.60×10^{4}		5.80×10^{4}
TF	Forward transit time	-	1.05×10^{-10}	2.31×10^{-10}	3.10×10^{-10}	3.41×10^{-10}		3.57×10^{-10}
vaf	Forward early voltage	[V]	600					
var	Reverse early voltage	[V]	45					
Diode_IS	Diode transport saturation current	[A]	3.75×10^{-46}	9.42×10^{-44}	2.98×10^{-42}	1.19×10^{-41}		4.72×10^{-41}
Diode_N	Diode emission coefficient	-	1.55					
Diode_CJO	Diode zero-bias junction capacitance	[F]	8.00×10^{-40}					

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Optimization and Simulation on Gas Flow and Temperature Fields on the Homoepitaxial Growth of N-Doped 4H-SiC Wafers

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Abstract

The uniformity of nitrogen (N) doping concentration in 4H-SiC epitaxial wafers is a critical determinant of electrical consistency and device reliability. In this study, key chemical vapor deposition (CVD) growth parameters, including the C/Si ratio, H_2 carrier gas flow rate, flow split ratio, and growth temperature, were systematically adjusted to investigate their effects on the N doping concentration and uniformity of 6-inch 4H-SiC homoepitaxial layers. The relationships between these parameters and characteristic phenomena such as site-competition epitaxy, along-track depletion of carbon source, and the distinct "W-shaped" doping profile were comprehensively analyzed. Furthermore, simulations of the flow and temperature fields within the reaction chamber and across the SiC epitaxial wafer revealed that under optimized conditions a stable parallel flow field forms above the wafer, accompanied by a uniform temperature distribution, thereby creating an ideal environment for homogeneous N doping. This work provides both theoretical insight and practical guidance for enhancing doping uniformity in large-size SiC epitaxial wafers.

Keywords: N doping concentration; uniformity; CVD parameters; mechanism of site competition epitaxy; simulation

1. Introduction

Silicon carbide (SiC), owing to its superior physical properties including high breakdown electric field, high thermal conductivity, and high electron saturation drift velocity, has become an ideal substrate material for high-voltage and high-power electronic devices [1–3]. Among various polytypes of SiC, 4H-SiC exhibits a hexagonal crystal structure with ABAC stacking sequence, offering both high carrier mobility and excellent crystal stability, which makes it the preferred choice in industrial applications [4–6]. Nevertheless, the performance of devices based on 4H-SiC fundamentally depends on the quality of the epitaxial layers, among which the doping concentration and its uniformity are critical parameters. For n-type doping, nitrogen (N) is the most commonly used dopant, which provides conduction electrons by substituting carbon sites in the lattice. Previous study has shown that controlling the uniformity of N doping within 4% is essential for producing high-performance devices, including avoiding localized electric field crowding, facilitating uniform carrier transport in the drift region and JFET region, promoting homogeneous distribution of carrier mobility in the channel region, and so on [7]. Feng et al. [8] demonstrated

that appropriately increasing the doping concentration while maintaining the breakdown voltage can significantly reduce the specific on-resistance and effectively suppress capacitive feedback, thereby improving the high-frequency figure of merit (HF-FOM) and overall robustness of SiC MOSFETs. A recent study has also revealed that a uniform doping concentration is beneficial for enhancing the interfacial and electrical characteristics of 4H-SiC MOS capacitors [9]. However, achieving uniform nitrogen doping remains a significant challenge, largely owing to the complexity of the chemical vapor deposition (CVD) epitaxial growth process. This process involves coupled multi-physics and multiscale dynamics, encompassing gas-phase transport, surface reactions, and heat transfer.

From the perspective of gas-phase transport, the flow distribution of precursors (e.g., silicon and carbon sources) and the N_2 within the reaction chamber determines the flux uniformity delivered to different regions of the substrate surface [10–12]. A non-uniform flow field can lead to varying supply rates of reactants along the wafer radial direction, resulting in spatial inhomogeneity of N distribution [13,14]. Moreover, CVD reaction kinetics are strongly influenced by growth parameters. Larkin's "site-competition epitaxy" theory indicates a competitive relationship between N and lattice carbon (C) or silicon (Si) atoms during epitaxy, suggesting that any factors altering the C/Si ratio, such as carrier gas flow rate and growth temperature, affect the uniformity of N doping concentration and uniformity [15,16]. Significant progress has been achieved by optimizing individual parameters. For instance, Inoue et al. [17] investigated the dependence of N incorporation on step-flow velocity by controlling nitrogen doping concentrations (from ~10^{17} cm^{-3} to 10^{19} cm^{-3}), and their analysis using a two-site exchange model revealed improved doping uniformity with increasing nitrogen concentration. Notably, few studies have systematically examined the underlying influence mechanisms of flow field and temperature field distributions on the uniformity of N doping in SiC epitaxial wafers.

In light of this, this study proposes a synergistic optimization strategy combining process control with simulation to achieve theoretical insights and practical improvement in N doping uniformity. Through systematic adjustment of key CVD epitaxial growth parameters, including the C/Si ratio, carrier gas flow, and growth temperature, the optimal parameter for enhancing N doping uniformity was obtained. Subsequently, two-dimensional simulations were performed to establish the relationships between process parameters and the resulting flow and temperature fields inside the chamber. The experimental results indicate that a C/Si ratio of 0.95, a proper H_2 gas flow rate of 100 slm, and a growth temperature at 1610 °C yielded an N doping uniformity of 3.35%. Simulations under these conditions revealed a stable, parallel gas flow above the wafer surface, forming a uniform and well-defined concentration boundary layer. Moreover, the temperature distribution across the SiC surface showed a small variation, providing a favorable environment for uniform N doping. This study offers theoretical guidance for improving doping uniformity in large-size SiC epitaxial wafers and contributes to enhancing wafer yield and reliability.

2. Materials and Methods

2.1. Materials

High-purity ethylene (C_2H_4, 99.999%), nitrogen (N_2, 99.999%), and trichlorosilane ($SiHCl_3$, 99.999%) were purchased from NEWRADAR. High-purity hydrogen (H_2, 99.999%) was prepared by first generating H_2 through water splitting, followed by drying and purification. The 6-inch 4H-SiC substrate used in the experiments was purchased from Hebei Synlight Semiconductor Co., Ltd.

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2.2. Synthesis of N-Doped SiC

A PE106-type horizontal hot-wall reactor (Beijing NAURA Technology Group Co., Ltd.) was used for growing the SiC epitaxial wafer. The 6-inch 4H-SiC substrate was placed on a graphite heating susceptor for homoepitaxial growth. H_2 served as the carrier gas (varied from 90 to 110 slm) and C_2H_4 and $SiHCl_3$ acted as the C and Si sources, respectively. N_2 was used as the dopant and the flow rate fixed at 200 slm. The SiC epitaxial wafer was grown via CVD by adjusting growth parameters, with a chamber pressure of 10,000 Pa. The C/Si ratio was controlled by adjusting the flow rates of C_2H_4 and $SiHCl_3$, while the flow rate of the C_2H_4 gas was fixed at 200 slm. The temporal evolution of the CVD growth process, spanning a total duration of approximately 90 min, is depicted in Figure 1a. Prior to introducing the C and Si precursors, in situ HCl etching was performed at the growth temperature (T_2) to remove surface-damaged regions. Subsequently, a buffer layer was grown for 10 min to further suppress the propagation of substrate defects and improve the epitaxial layer quality. Finally, the epitaxial layer was grown for about 10 min at a growth rate of 60 μm·h^{-1}, yielding a controlled thickness of 10 μm for the SiC epitaxial wafer in this study.

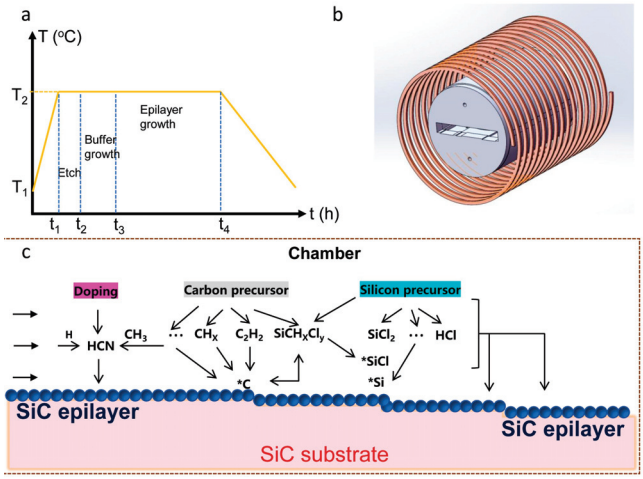

Figure 1. (**a**) CVD growth process along with time variation, including etching, buffer layer growth, and epitaxial wafer growth. (**b**) The geometric configuration of the growth zone in the CVD furnace. (**c**) The homogeneous epitaxial chemical reaction with N doping on SiC substrate.

2.3. Calculation of N Dopant Concentration and Uniformity

Capacitance-voltage (C-V) profiling with Hg Schottky contacts was used to detect the N doping concentration distribution of 6-inch 4H-SiC epitaxial wafers. For each SiC epitaxial wafer, thirteen-point concentration measurements were performed. The variance (σ), average value (*mean*, cm^{-3}), and uniformity (δ) of the N doping concentration were then calculated using the equations below [18–20]:

$$\sigma = \sqrt{\left(\sum_{i=1}^{n}(x_i - m)/(N-1)\right)} \quad (1)$$

$$mean = \sum_{i=1}^{n} x_i/N \quad (2)$$

$$\delta = \frac{\sigma}{mean}\cdot 100\%. \quad (3)$$

where x_i is the N doping concentration, cm^{-3}; N is the number of measurement points.

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2.4. Simulation

First, a multi-physics coupled geometric model of the reaction chamber was established based on the structure of reactor and operating conditions, as shown in Figure 1b. According to the actual chamber design, the SiC wafer was positioned in the center of the chamber during the simulation. This region provides a growth environment with uniform temperature and stable gas flow. Simultaneously, the SiC wafer rotates continuously at a low speed driven by an air-floating graphite holder to achieve more uniform growth conditions.

Given the thin thickness of the SiC epitaxial wafer, the influence of gas flow variations perpendicular to the epitaxial wafer on the concentration uniformity can be neglected [21]. Therefore, a two-dimensional field model was adopted, and COMSOL software was used to simulate the gas flow and temperature field distribution during the SiC epitaxial growth process [22]. The gas in the reactor was treated as an ideal gas, and the gas flow state was laminar. Since the SiC epitaxial growth involves multiple physical fields, including electromagnetic, flow, and temperature fields, the governing equations in the COMSOL laminar flow module were Maxwell Equations (4)–(7) [23], the continuity Equation (8) [24], the mass conservation Equation (9) [25], and the momentum conservation Equation (10) [26].

$$\nabla \cdot \mathrm{E} = \frac{\rho_q}{\varepsilon_0} \tag{4}$$

$$\nabla \cdot \mathrm{B} = 0 \tag{5}$$

$$\nabla \times \mathrm{E} = -\frac{\partial \mathrm{B}}{\partial t_0} \tag{6}$$

$$\nabla \times \mathrm{B} = \mu_0 \mathrm{J} + \mu_0 \varepsilon_0 \frac{\partial \mathrm{E}}{\partial t} \tag{7}$$

$$\frac{\partial \rho}{\partial t} + \nabla(\rho \cdot \mu) = 0 \tag{8}$$

$$\rho \nabla \cdot \mathrm{u} = 0 \tag{9}$$

$$\rho(\mathrm{u} \cdot \nabla)\mathrm{u} = \nabla \cdot [-\mathrm{pl} + \mathrm{K}] + \mathrm{F} \tag{10}$$

where ρ is the mass density of the fluid, g L^{-1} or slm; u is the fluid velocity, m s^{-1}; p is the static pressure of the fluid, Pa; l is the second-order unit tensor; K is the deviatoric stress tensor; and F is the volumetric force density, N m^{-3}.

3. Results

3.1. N Doping Mechanism During CVD Growth 4H-SiC Epitaxial Wafer

The mechanism for the CVD growth of N-doped 4H-SiC wafers in a H_2 carrier gas environment is illustrated in Figure 1c. At a high temperature of SiC epilayer growth, C_2H_4 decomposes into C_2H_2 to provide active C atoms (*C), while $SiHCl_3$ undergoes pyrolysis to generate $SiCl_2$, supplying active Si atoms (*Si). These species undergo complex chemical processes on the substrate surface via a step-flow growth mode, including adsorption, deposition, and desorption. Simultaneously, the introduced N_2 is converted into HCN during CVD, which serves as the primary source for N incorporation, thereby completing doping in SiC epitaxial wafers. The incorporation of N dopants is explained by the site-competition epitaxy mechanism, whereby N atoms compete with carbon sources for lattice sites during the growth of SiC [27]. This process is governed jointly by the temperature and flow fields, both of which are adjustable through growth parameters.

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3.2. Effect of C/Si Ratio

The background N dopant concentration was first examined at different C/Si ratios without introducing N_2 flow under a growth temperature of 1620 °C. As shown in Figure 2a, a measurable level of N incorporation was still observed in the SiC epitaxial wafer even in the absence of intentional N_2 supply into the reaction chamber. The N concentration varied with the C/Si ratio, reaching a maximum of 9.21 × 10^{13} cm^{-3} at a C/Si ratio of 0.9. The occurring N mainly originate from residual N sources inherent in the reaction chamber or the graphite susceptor inevitably, which become activated under high temperature conditions and subsequently incorporate into the SiC epitaxial wafer as dopants. To improve the N doping concentration, introducing N_2 gas flow during CVD growth can significantly increase the doping level, and the uniformity can be optimized by controlling the growth parameters. Given the competition between N atoms and C sources for lattice sites, modifying the C/Si ratio is crucial. Figure 2b shows the variation of N doping concentration as the C/Si ratio increases from 0.90 to 1.00 under fixed growth conditions of 1620 °C with adding N_2. A "W-shaped" profile was clearly observed. By measuring, the mean doping concentrations at C/Si ratios of 0.90, 0.95, and 1.00 reach 6.6 × 10^{15} cm^{-3}, 6.3 × 10^{15} cm^{-3}, and 6.1 × 10^{15} cm^{-3}, respectively (Figure 2c). It is evident that under a constant N_2 flow, the N doping concentration declines along with increasing the C/Si ratio. This is primarily attributed to a higher C/Si ratio favoring the competition of N atoms against C sources for lattice sites, demonstrating a distinct "site-competition epitaxy" mechanism [27]. Furthermore, at the C/Si ratio of 0.95, the mean doping concentrations at the wafer edge, near edge, and center decreased by approximately 3.29%, 5.71%, and 8.10%, respectively (Figure 2d). Figure 2e displays the measured doping uniformity. Clearly, the doping uniformity value reaches 4.1% at a C/Si ratio of 0.95, much lower than the wafer at C/Si ratio of 0.90 (4.6%), but a little higher than the wafer at C/Si ratio of 1.00 (4.0%). This phenomenon confirms that the C source exhibits a higher "along-track depletion" rate compared to the Si source. Therefore, increasing the C/Si ratio can compensate for the higher depletion of C sources toward the wafer center, which helps improve doping uniformity. However, an excessively high C/Si ratio may lead to increased step bunching and the formation of triangular defects, adversely affecting epilayer quality [28].

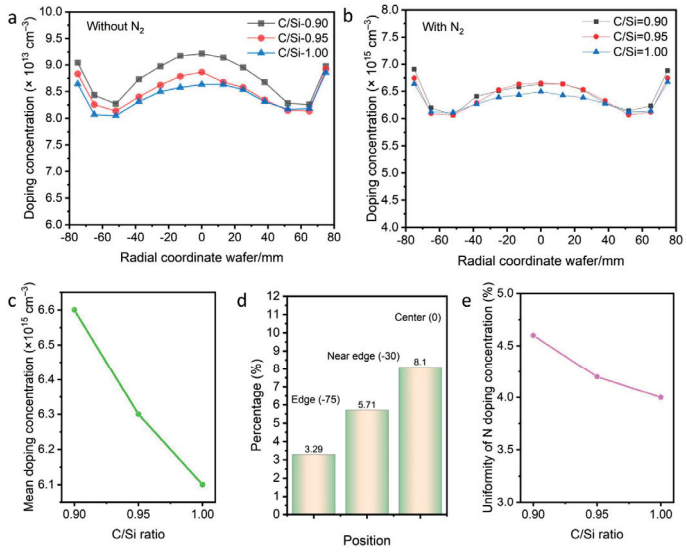

Figure 2. Doping concentration versus C/Si ratio in SiC epitaxial wafers without (**a**) and with N_2, (**b**) flow, (**c**) Mean doping concentration versus C/Si ratio in SiC epitaxial wafers with N2 flow, (**d**) Radial reduction in concentration at specific positions, (**e**) Uniformity of N doping concentration.

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The distribution of various defects is summarized in Figure 3 and Table 1. At C/Si ratios of 0.90, 0.95, and 1.00, the triangular defect counts were 25, 8, and 38, respectively. In comparison, step defects numbered 12, 14, and 35, whereas the counts for basal plane dislocations (BPDs) were 21, 6, and 4, respectively. By comparison, a C/Si ratio of 0.95 resulted in the minimum total defect count of 28. The increase in defect count with C/Si ratio is primarily due to non-stoichiometric conditions arising from ratios that are either too low or too high, which lead to deposition-related defects. Therefore, based on a comprehensive evaluation of doping uniformity and material quality, a C/Si ratio of 0.95 is determined to be optimal for the SiC epitaxial wafer growth.

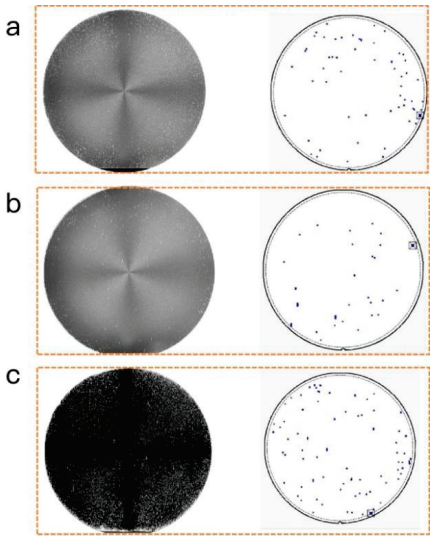

Figure 3. Defect characterization for C/Si ratios of 0.9 (**a**), 0.95 (**b**), and 1.00 (**c**).

Table 1. Statistical analysis of defect density as a function of C/Si ratio.

C/Si Ratio \ Defect Classification	Triangular Defects	Step Defects	BPDs	Total
0.9	25	12	21	58
0.95	8	14	6	28
1.0	38	35	4	77

3.3. Influence of Carrier Gas Flow

With a fixed C/Si ratio of 0.95, the effect of H_2 carrier gas flow rate on doping concentration and uniformity was investigated. As shown in Figure 4a, the doping concentration profile across the SiC epilayer exhibits a "W" shape at H_2 flow rates of 90, 100, and 110 slm. Moreover, the average N doping concentration varies significantly with changes in the H_2 gas flow. The reason is that, under constant process pressure, an increase in H_2 gas flow may lead to a decrease in the reactor temperature and an increase in the gaseous H_2 concentration. This slows down the depletion of source gases, particularly the C source, along the gas stream. Consequently, the optimal doping uniformity of 4.85% was achieved at an H_2 flow rate of 100 slm, compared to 5.20% and 5.03% at 90 and 110 slm, respectively (Figure 4b). This suggests that a proper H_2 carrier gas flow rate may enhance convection and heat transfer, while the adsorption/reaction of Si and C likely approaches saturation at a specific flow rate, yielding optimal N doping uniformity.

To investigate the relationship between doping uniformity and the gas flow field, the flow split ratio was varied as 1:2.9:1, 1:3.0:1, and 1:3.1:1 while keeping the total flow and

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C/Si ratio constant. Figure 4c shows the doping concentration profiles under different split ratios. As the central inlet flow increases, the doping concentration at the wafer center decreases while that at the edge increases. The smallest deviation between edge and center concentrations, along with the best overall uniformity of 3.45%, was observed at a split ratio of 1:3.0:1. At ratios of 1:2.9:1 and 1:3.1:1, the uniformity was 5.29% and 3.73%, respectively (Figure 4d). This confirms the significant impact of the flow split ratio on doping uniformity. A higher flow velocity results in a thinner boundary layer; regions with thinner boundary layers experience higher growth rates and consequently lower doping concentrations [29].

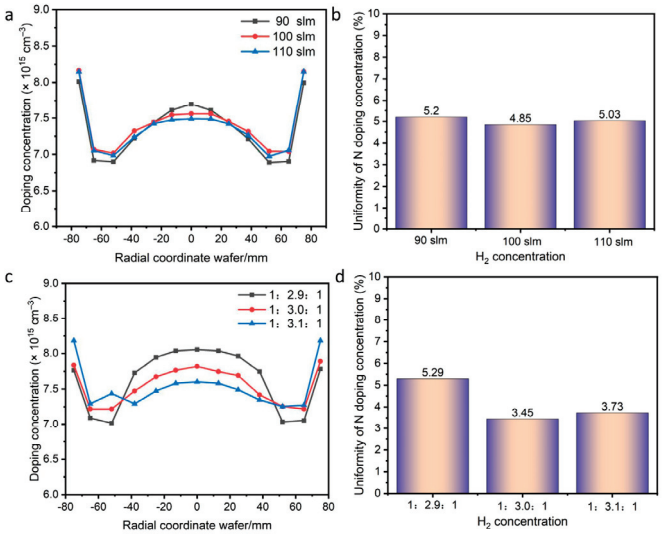

Figure 4. Doping concentration and uniformity versus key process parameters. (**a**,**b**) H_2 flow rate; (**c**,**d**) flow split ratio.

3.4. Influence of Temperature

Growth temperature is a fundamental parameter in SiC epitaxy. Selecting an appropriate temperature is crucial for achieving high N doping uniformity. In this work, the CVD growth temperature at 1600, 1610, and 1620 °C was conducted under specific C/Si and H_2 flow conditions. Figure 5a presents the doping concentration profiles at different growth temperatures. The profiles exhibit a "W" trend across the wafer. The average doping uniformity was 3.35% at 1610 °C, superior to 3.58% at 1600 °C and 3.44% at 1620 °C (Figure 5b), indicating that 1610 °C is more conducive to improving uniformity. This is primarily because the adsorption, migration, and incorporation of N atoms into the SiC lattice require overcoming an energy barrier. At lower temperatures, the mobility of dopant atoms is poor, leading to their non-uniform aggregation at specific sites and causing micro- and macro-scale concentration fluctuations. Conversely, excessively high temperatures may induce unstable natural convection, disrupting the ideal laminar flow and leading to in-plane doping non-uniformity.

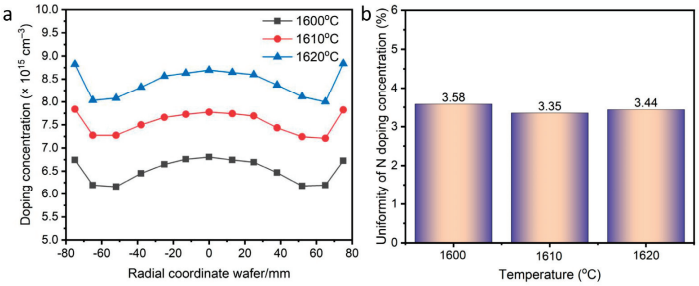

Figure 5. Doping concentration (**a**) and uniformity (**b**) at different CVD process temperatures.

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3.5. Simulation of Gas Flow and Temperature Fields

The "W"-shaped doping concentration profile observed in SiC epitaxial wafers is primarily attributed to the combined effects of gas flow dynamics, temperature field distribution, and reactant transport during epitaxial growth. To gain deeper insight into the correlation between doping uniformity and the gas flow field, simulations of the flow field during SiC epitaxial growth were performed. Figure 6a illustrates the geometry of the CVD reactor with gas flow direction. The H_2 carrier gas flow was first simulated in the CVD reactor, including the graphite susceptor. At a low H_2 flow rate of 90 slm (Figure 6b), the velocity contours over the wafer exhibit a complex pattern with pronounced gradients, indicating a flow regime dominated by viscous effects and non-uniform gas distribution, which leads to a higher N doping concentration at the edge. As the flow rate increases to 100 slm (Figure 6c), the contours become uniform and parallel, and the velocity difference between the edge and center regions is reduced. This optimum condition suggests the establishment of a stable, well-developed flow that enhances lateral uniformity, likely due to a thinned boundary layer and improved momentum transfer. However, a further increase to 110 slm (Figure 6d) disrupts this uniformity, resulting in a non-uniform contour pattern over the wafer. This degradation may be attributed to excessive flow momentum, which can induce flow instability, turbulence onset, or altered reactor temperature profiles, thereby compromising the ideal stagnation flow geometry achieved at 100 slm. Although the gas flow field was optimized by adjusting the H_2 flow rate, the velocity near the edge regions remained relatively high. This locally enhanced flow increases the atomic step density at step edges and prolongs the residence time of surface-adsorbed species, ultimately resulting in a higher N doping concentration in those areas.

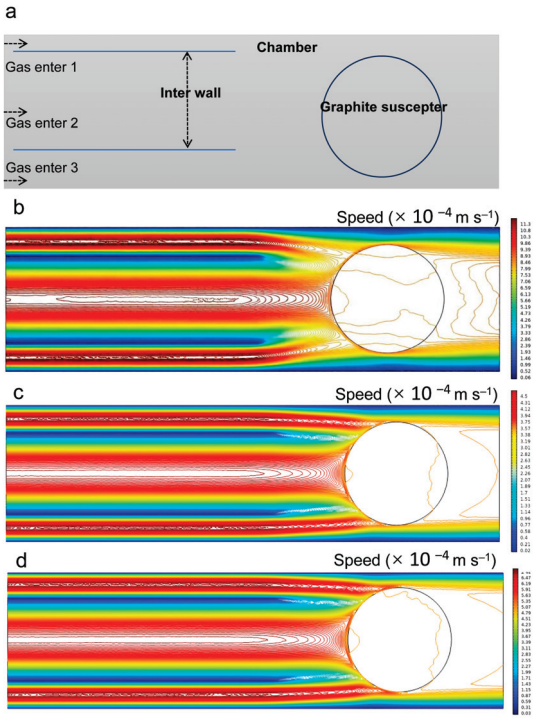

Figure 6. (**a**) Geometry of the CVD reactor with gas flow direction. Distribution of gas flow field in reaction chamber with different H_2 gas flow rates: (**b**) 90 slm, (**c**) 100 slm, (**d**) 110 slm.

The effect of the flow split ratio on the velocity field was also examined via the three gas inlets of the CVD reactor geometry. Figure 7 presents the simulated velocity field distributions at a fixed total flow of 100 slm with different split ratios. With a flow split

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ratio of 30:40:30 across the gas inlets (Figure 7a), the resulting velocity contours over the wafer area exhibit significant non-uniformity. This uneven flow distribution is attributed to an imbalance in momentum injection from the inlets, which disrupts the formation of a symmetric stagnation flow above the wafer, leading to localized regions of higher and lower velocity, which may lead to a "W-shape" distribution of N doping concentration. The most uniform and widely distributed velocity contours are achieved with a 20:60:20 flow split (Figure 7b). In this regime, the flow field effectively promotes consistent reactant transport and temperature distribution across the wafer. In contrast, a 10:80:10 split (Figure 7c) reintroduces significant contour unevenness, degrading uniformity. This demonstrates that the uniformity of gas flow fields is highly sensitive to the flow split balance, with the 20:60:20 ratio representing an optimal point between the extremes of excessive side flow (as in 30:40:30) and an overly dominant center flow.

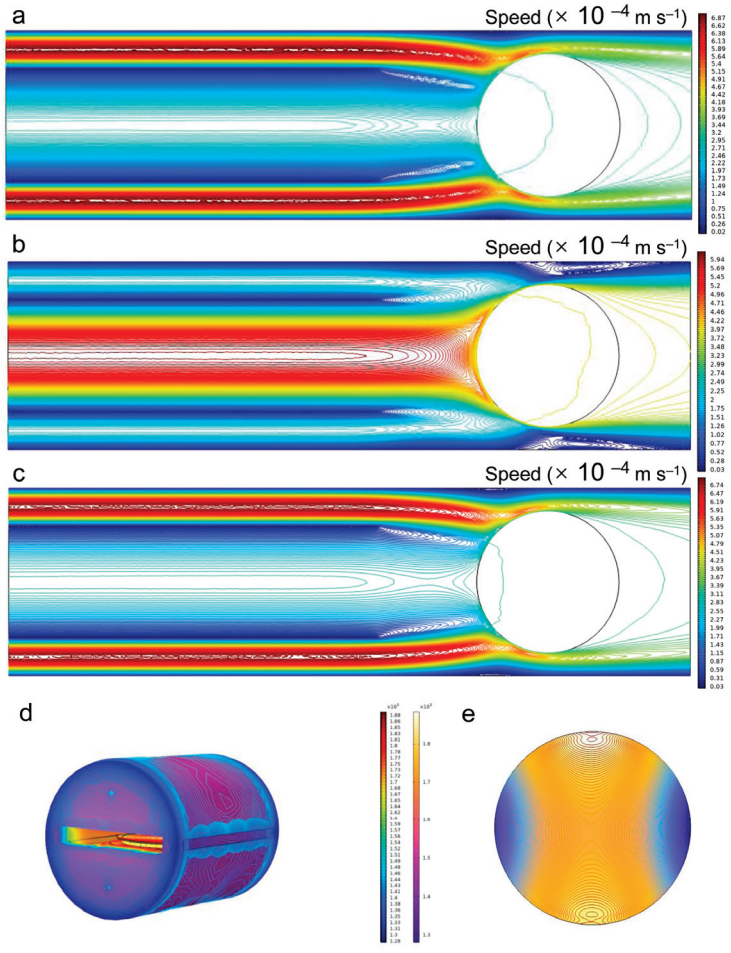

Figure 7. Distribution of gas flow field in reaction chamber with different H_2 gas flow rates: (**a**) 30:40:30, (**b**) 20:60:20, (**c**) 10:80:10. Distribution of temperature field in reaction chamber (**d**) and on the SiC epitaxial wafer (**e**) at 1610 °C.

Given the aforementioned advantage of 1610 °C for uniformity, the temperature field within the chamber at 1610 °C was simulated, including temperature contours and surface temperature plots (Figure 7d). The contours are essentially symmetric about the geometric center. A temperature gradient exists between the interior and the edge of the graphite growth cavity, primarily dictated by the geometry. The outer region of the insulation layer remains cooler, while the growth zone reaches the target temperature. This thermal difference may contribute to a higher concentration of N dopants in the central region.

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However, with the rotation provided by the gas-foil susceptor, the temperature gradient across the SiC wafer surface is significantly reduced. The temperature field across the SiC epilayer is displayed in Figure 7e. It indicates a temperature difference of 19.3 °C between the internal and edge regions within the 6-inch SiC epitaxial wafer. The higher temperature in the central region accelerates step migration, increasing the flux of N atoms passing through step edges per unit time and thus enhancing the doping concentration. Consequently, the simulated distributions of temperature and gas flow affect the atomic step density at step edges and the residence time of surface-adsorbed species, making the N doping concentration as a "W-shape" across the wafer. On the one hand, the higher temperature in the central region is beneficial for improving the N doping concentration at this region. On the other hand, the fast gas velocity near edge of wafer leads to local fluctuations in the C/Si ratio, thus making N dopant enrichment. According to the "site-competition epitaxy" theory, the above temperature and gas flow fields result in elevated doping concentrations in both the central and edge regions.

4. Conclusions

In summary, we systematically optimized the N doping uniformity in 6-inch 4H-SiC homoepitaxial layers through the combined CVD approach and multi-physics simulation. The experimental investigation of key growth parameters revealed a clear interdependence between process conditions and the resulting N doping uniformity. The observed "W-shaped" doping distribution was elucidated through the synergistic effect of site-competition epitaxy and along-track depletion of carbon. Consequently, the optimal parameter yielded a superior N doping uniformity of 3.35%, accompanied by a significant reduction in epilayer defects. Simulations of the flow and temperature fields provided physical insight into the experimental trends. Under the optimized conditions, a stable laminar flow and a uniform temperature distribution were achieved, creating a favorable environment for consistent dopant incorporation. This work not only identifies a practical CVD growth for high uniformity N doping in 4H-SiC epitaxial wafers but also establishes a coherent link between CVD parameters and N doping mechanisms with gas and temperature field distributions.

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