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CMOS-MEMS Fabrication Technologies and Devices

Edited by
Liangxing Hu, Korkut Kaan Tokgoz and Zhen Yang

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About the Editors

Liangxing Hu

Liangxing Hu is currently a Full Professor in Kunming Institute of Physics. He obtained Bachelor Degree in 2012, and completed his Doctoral Degree at Nanyang Technological University, Singapore in 2018. He has involved and completed several national research projects such as biomolecular nanomotors, femtosecond laser direct writing, CMOS-MEMS packaging and low-light level night vision technology, *etc.* In addition, he has published more than 50 peer reviewed articles and granted 5 patents.

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Since joining Sabancı University, he has led and contributed to several funded research projects on sub-THz wireless communication, energy-efficient sub-THz systems, PLLs, frequency multipliers, D-band phase shifters, OFDM wireline systems, and CMOS 2.0 signaling. His group works across circuit design, system modeling, hardware impairment analysis, compact modeling, edge-AI implementation, and near-memory computing. He currently supervises and co-supervises graduate and undergraduate researchers working on mmWave/sub-THz transceivers, phase noise and ISAC, AI-assisted modeling, FPGA/ASIC implementation of tiny neural networks, and processing-near-memory architectures.

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Zhen Yang received Ph.D. degree in electronic information and electrical engineering from Shanghai Jiao Tong University in 2016. He became a visiting assistant professor in Southern University of Science and technology from 2016 to 2017. From 2018 to 2020, he carried postdoctoral research at Ural Federal University in Russia and INESC Microsystems and Nanotechnologies in Portugal. From 2024 to 2025, He carried out research on biomedical sensing applications as a visiting scholar in National University of Singapore. He is currently a full associate professor in GuangXi Normal University. His research interests involve MEMS and BioMEMS technique, magnetic sensors, (GMR sensors, GMI biosensor, Fluxgate biosensor, Magnetic tunnel junction sensor), current sensors, pressure sensors, flexible sensor, biosensor, basic electronic components (RF inductor, variable capacitor, integrated filter, transformer, power micro-inductor) and related applications in different fields.

Preface

Electronics are extremely popular in our daily life. Semiconductors such as complementary metal oxide semiconductor (CMOS) and micro-electro-mechanical system (MEMS) are key devices in the electronic field. CMOS can be integrated with MEMS components within a single chip (3D integration) to produce compact and low-cost CMOS-MEMS devices for multiple applications (chemical sensing, energy harvesting, signal transmission, and others). Therefore, these devices' fabrication and integration are essential for the development of the society. This Special Issue aims to gather high quality research contributions dealing with MEMS devices integrated with CMOS, independently of fabrication technologies and final applications.

Liangxing Hu, Korkut Kaan Tokgoz, and Zhen Yang
Guest Editors

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Article

Investigation of the Specification Degradation Mechanism of CMOS Power Amplifier under Thermal Shock Test

Shaohua Zhou [1,2,†], Cheng Yang [1,2,†] and Jian Wang [1,2,*]

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Abstract: To investigate the critical specifications of a power amplifier (PA) under rapidly changing temperature conditions, we fabricated and tested a 0.3–1.1 GHz complementary metal–oxide–semiconductor (CMOS) PA under thermal shock tests. The results show that high- and low-temperature shocks can accelerate the degradation of critical specifications of PAs and that the critical specifications of PAs degrade with the increasing number of shocks. The main reason for the degradation of critical specifications of PAs with increasing thermal shock tests is the mismatch of thermal expansion coefficients of printed circuit boards (PCB) with FR-4 as a substrate. The results of this paper can provide a reference for the development of temperature-robust PAs design guidelines for the implementation of temperature-robust PAs using low-cost silicon technology.

Keywords: PCB; FR-4; CMOS; power amplifier; performance degradation; thermal shock

1. Introduction

The power amplifier (PA) is one of the core components of communication systems, which are the focus of study in the field of wireless broadband communication [1–3]. PAs are often used in harsh environments [4]. The characteristics of the PA have a significant temperature dependence [5]. When the temperature changes, so does the PA's performance, which in severe cases, may cause the system to fail to perform its intended function [6]. According to the literature, 31% of electronic equipment failures at U.S. coastal bases are caused by high temperatures and humidity [7–9]. Likewise, a change in the specification of a PA will cause the system in which it is located to fail [10]. Therefore, there is great interest in stabilizing the performance of a PA more quickly and efficiently so that it can operate properly in rugged environments [11]. Therefore, it is necessary to understand the temperature characteristics of a PA, mainly to stabilize the performance of PAs faster and more effectively.

The temperature characteristics of PAs are a hot topic of research. For example, the temperature characteristics of PAs at specific typical temperature points, such as −5 °C [12], 25 °C [13], 125 °C [9], etc., or the temperature characteristics of PAs in specific typical temperature ranges, such as −20 °C to 120 °C [14], −40 °C to 125 °C [10], 10 °C to 100 °C [15], etc., can be investigated. These studies generally reflect the properties of PAs at a specific typical temperature or in a typical temperature range, which are gradually changed throughout the study.

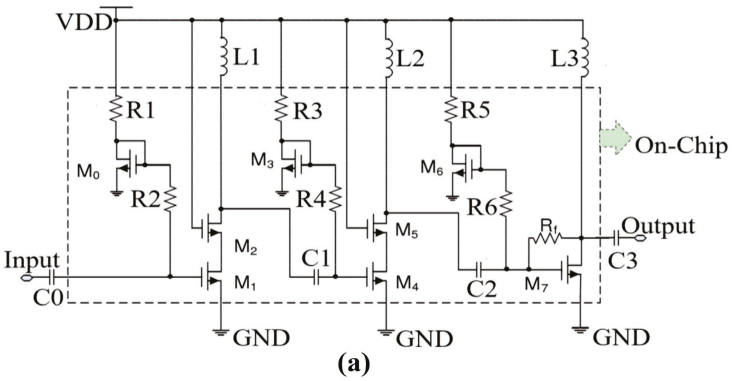
However, PAs sometimes must work in environments with rapid temperature changes. These rapid temperature changes will significantly impact the specification of PAs [14]. Therefore, it becomes an urgent problem to know the pattern and mechanism of the specification degradation of PAs under the working environment of rapid temperature changes [16].

High- and low-temperature shock experiments can better characterize the properties temperature of PA under rapid changes [17]. In this paper, high- and low-temperature shock experiments were carried out with a Class A PA of 0.3–1.1 GHz, and the phenomena and causes of PA specification degradation under high- and low-temperature shocks are discussed in detail.

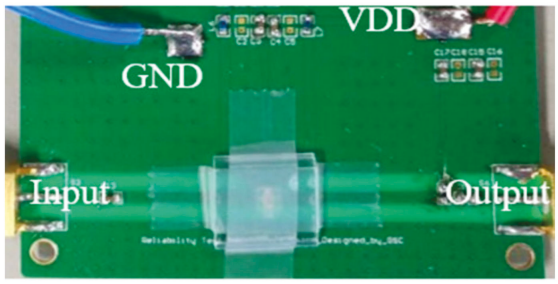
2. Designed PA and the Experimental Setup

2.1. The Designed PA

The schematic diagram of the 0.3–1.1 GHz CMOS Class-A PA used in the thermal shock experiments is shown in Figure 1a [18]. Considering that the linearity specification of the common source amplifier structure is better than that of the Cascode structure, a combination of a common source amplifier and resistive negative feedback structure was chosen for the third stage amplifier. The resistive negative feedback structure can match the impedance of the input and output circuits of the amplifier. At the same time, the resistive negative feedback structure can improve gain flatness and reduce nonlinear distortion. Therefore, the impedance matching of the amplifier output structure can be achieved without adding additional circuit components. The second stage amplifier was designed with a common source and gate Cascode structure. The cascaded structure of the PA can significantly improve the isolation at the input/output, and it will increase the output impedance of the transistor. The first stage amplifier was also designed with a common source and gate Cascode structure. The sizes of the transistors M0~M6 of PA used in this paper are 200 μm/0.35 μm, and M7 is a 400 μm/0.35 μm-thick oxide layer NMOS device. The on-chip stage spacing direct coupling capacitors C1 and C2 are selected to be 20 pF capacitors.



(a)



(b)

Figure 1. The 0.3–1.1 GHz CMOS PA: (**a**) The detailed schematic diagram; (**b**) the physical photograph.

2.2. Thermal-Shock Test

To study the effect of rapid temperature changes on PA specifications, we conducted thermal shock tests in the shock chamber (Vötsch VT^3 7006 S2). The logical relationship of the test system is shown in Figure 2a, and the physical deployment of the test system is shown in Figure 2b. In this chamber, the temperature regulation range is from +50 °C to +220 °C in the hot zone and from −80 °C to +70 °C in the cold zone.

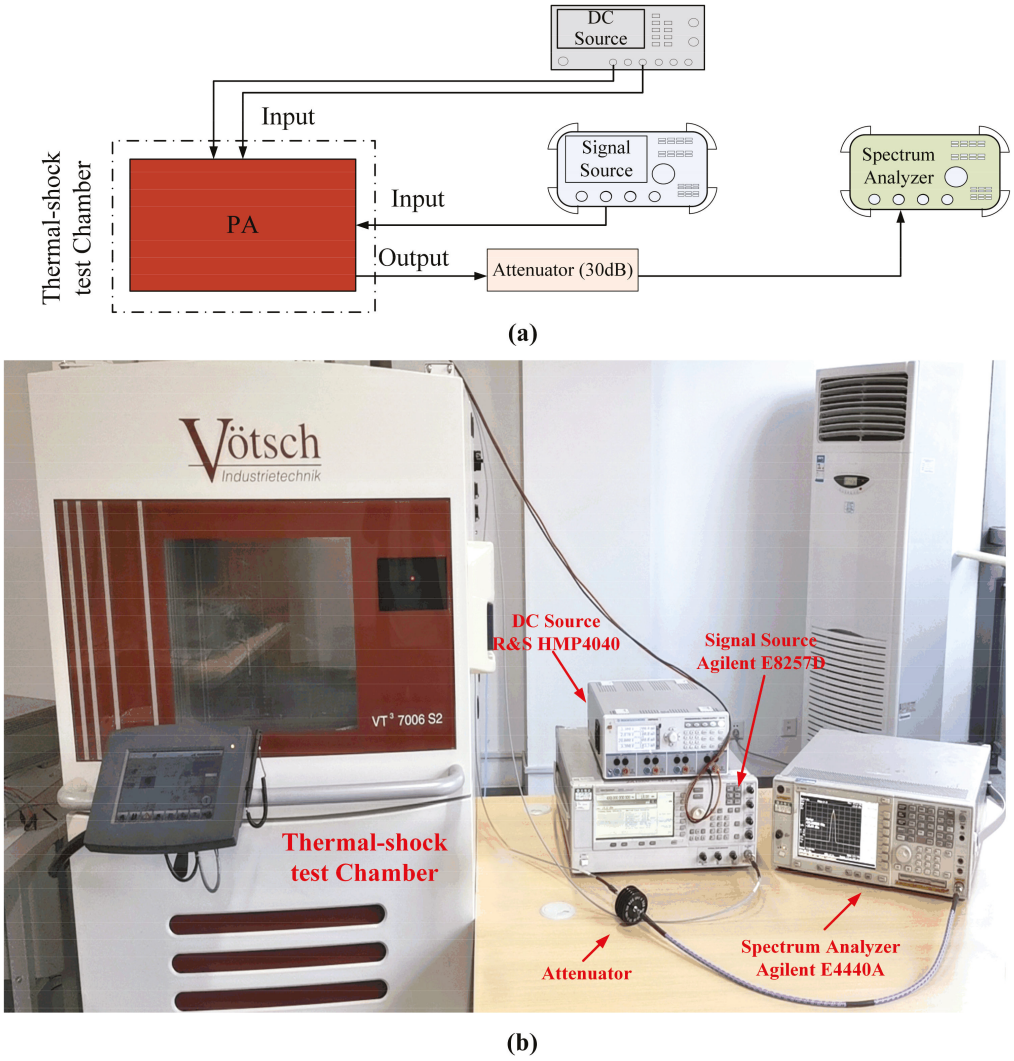


Figure 2. The thermal shock test environment. (**a**) The logical relationship of the test system; (**b**) the physical deployment of the test system.

As shown in Figure 3, the temperatures in the high-temperature and low-temperature regions are 125 °C and −40 °C, respectively. The PA stays in the high-temperature and low-temperature zones during each thermal shock cycle for 15 min, respectively. After five thermal shock cycles, the PA was left in the room temperature zone for 35 min so that it could be measured after thermal shock. The input power during the thermal shock cycle was always −20 dBm, which the Agilent E8257D provided. The voltage provided by the power supply during and after the completion of the shock measurement process was always 3.3 V. The input power provided by the signal source during the shock was −20 dBm. The input power provided by the signal source during the measurement process after the completion of the shock was from −10 dBm to 18 dBm. The measured frequency was 433 MHz.

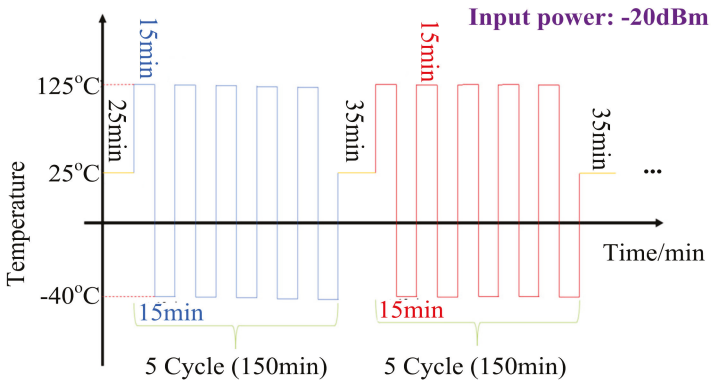


Figure 3. Schematic representation of the used thermal-cycling profile.

3. Results and Discussions

3.1. DC Current

The degradation of the DC current under shock and typical temperature experiments is shown in Figure 4. As seen from the results of the shock experiments, the current decreased from 113.4 mA (P_{in} = 8 dBm) to 110.7 mA after 25 cycles of thermal shock experiments. From a typical temperature experiment, the DC current of the PA decreased from 113.4 mA (P_{in} = 8 dBm) to 91.5 mA when the temperature rose from 25 °C to 90 °C.

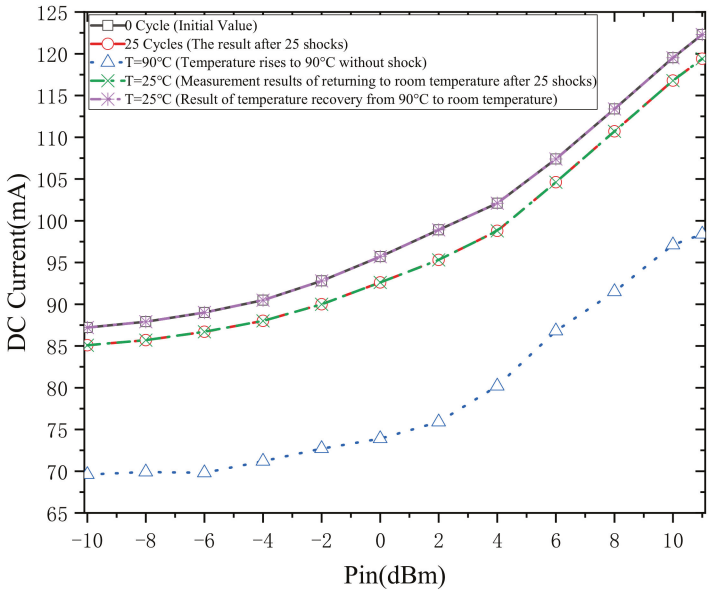


Figure 4. DC current of PA under thermal shock test and temperature test.

When the thermal shock experiment and the typical temperature experiment were completed, the two test objects were measured at room temperature. The measurement results show that the DC current of the PA could not be restored to the initial state of the PA after 25 cycles of the thermal shock experiment. However, the DC current of the PA after the typical temperature experiment can be restored to the initial state of the PA.

This indicates that the thermal shock experiment and the typical temperature experiment have different effects on the DC current of PA. It also shows that the effect of thermal shock experiments on PA is destructive and irreversible. Finally, the reasons for current degradation under two different experimental methods were analyzed.

In the saturation region, the drain current (I_{ds}) can be written as [19]:

$$I_{ds} = \frac{W_g \mu_n C_{ox}}{2L_g}(V_{gs} - V_{th})^2 \quad (1)$$

where W_g is the gate width, μ_n is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, L_g is the gate length, V_{gs} is the gate-to-source voltage, and V_{th} is the threshold voltage.

According to Equation (1), only the carrier mobility and the threshold voltage are temperature-dependent in the expression of the drain current. The two cases of thermal shock experiments and typical temperature experiments are discussed and analyzed.

3.1.1. Thermal Shock Experiment

The literature reported that thermal shock experiments will increase the threshold voltage [20,21]. Therefore, when the number of thermal shocks is changed, the expression for the drain current can be written as:

$$I_{ds-shock} = \frac{W_g \mu_n C_{ox}}{2L_g}(V_{gs} - V_{th-shock})^2 \tag{2}$$

According to Equations (1) and (2), the ratio before and after the drain current shock can be expressed as:

$$\frac{I_{ds}}{I_{ds-shock}} = \frac{(V_{gs} - V_{th})^2}{(V_{gs} - V_{th-shock})^2} \tag{3}$$

Furthermore, we can obtain the extraction of the root of this ratio as:

$$\sqrt{\frac{I_{ds}}{I_{ds-shock}}} = \frac{(V_{gs} - V_{th})}{(V_{gs} - V_{th-shock})} = \frac{(V_{gs} - V_{th})}{(V_{gs} - V_{th} - \Delta V_{th})} \tag{4}$$

where:

$$\Delta V_{th} = (V_{gs} - V_{th})(\sqrt{\frac{I_{ds}}{I_{ds-shock}}} - 1) / \sqrt{\frac{I_{ds}}{I_{ds-shock}}} \tag{5}$$

Additionally, the drain current of class-A PA can be expressed as:

$$I_{ds} = I_{DC} + i_{rf} \sin w_0 t \tag{6}$$

According to Equation (6), the change in drain current can be considered when the change in DC current so that it can be obtained:

$$\Delta V_{th} = (V_{gs} - V_{th}) \times 9.9 \times 10^{-3} \tag{7}$$

In this way, the increment of the V_{th} can be obtained. Therefore, the threshold voltage can also be quantitatively calculated. Through the above analysis, the main cause of current degradation due to high- and low-temperature shocks is the increase in V_{th}, which is irreversible.

3.1.2. Typical Temperature Experiment

In typical temperature experiments, the leading cause of drain current degradation is a decreased carrier mobility with increasing temperature. The expression for carrier mobility is [22]:

$$\mu_n(T) = \mu_n(T_0)\left(\frac{T}{T_0}\right)^{-m} \tag{8}$$

where T_0 = 300 K, m = 1.5~2.

According to Equations (1) and (8), the relationship between drain current and temperature is:

$$I_{ds}(T) = \mu_n(T_0)\left(\frac{T}{T_0}\right)^{-m} \frac{W_g C_{ox}}{2L_g}(V_{gs} - V_{th})^2 \tag{9}$$

The current degrades from 99 mA to 75.8 mA (P_{in} = 2 dBm), which is obtained according to Equation (9), the ratio of the drain current at room temperature T_R (identified as $I_{ds}(T_R)$) and temperature T (determined as $I_{ds}(T)$) can be expressed as:

$$\frac{I_{ds}(T_R)}{I_{ds}(T)} = \frac{\mu_n(T_0)\left(\frac{T_R}{T_0}\right)^{-m}}{\mu_n(T_0)\left(\frac{T}{T_0}\right)^{-m}} = \frac{\left(\frac{T_R}{T_0}\right)^{-m}}{\left(\frac{T}{T_0}\right)^{-m}} = \frac{\left(\frac{298}{300}\right)^{-m}}{\left(\frac{363}{300}\right)^{-m}} = \frac{99}{75.8} \approx 1.31 \tag{10}$$

Therefore, we can define m as 1.5.

Furthermore, the variation in carrier mobility with temperature, according to Equation (11), is known quantitatively as:

$$\mu_n(T) = \mu_n(T_0)\left(\frac{T}{T_0}\right)^{-1.5} \tag{11}$$

The degradation phenomena and mechanisms of currents under high- and low-temperature shock experiments and typical temperature experiments are different. The main cause of degradation under thermal shock experiments is the threshold voltage increase, and this degradation is irreversible. On the other hand, the degradation under typical temperature experiments is mainly due to decreased carrier mobility with temperature increases. Nonetheless, this degradation is reversible, and the current will return to the initial state after the temperature returns.

3.2. Output Power

Figure 5 shows the variation in the output power of the PA under high- and low-temperature shocks (frequency = 433 MHz). A significant thermal cycling effect is observed at all input powers. For example, the output power is 19.35 dBm (P_{in} = 10 dBm). After 25 shocks, its output power becomes 19.03 dBm, i.e., a decrease of 0.32 dBm. After 105 shocks, the output power decreases to 18.11 dBm.

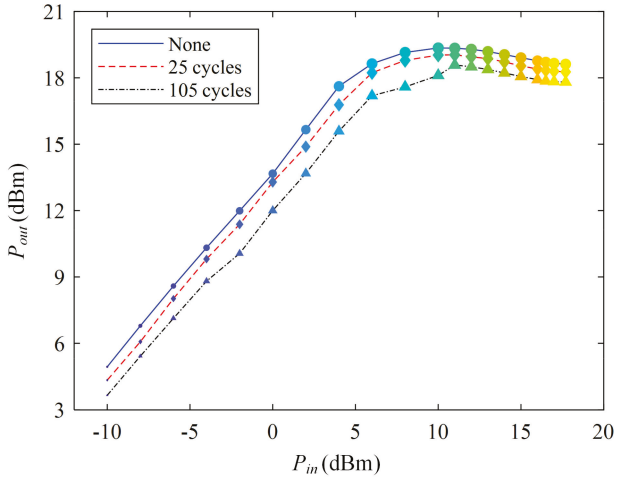


Figure 5. The output power of PA under thermal shock test.

The cause of output power degradation is the mismatch of the thermal expansion coefficient of the PCB material. The mismatch in the coefficient of thermal expansion of the material will cause an increase in the resistance of the solder joint, which makes the thermal loss of the resistance increase [21,23]. This means that, for a given PA input power, more energy is converted into heat in the PA. Then, the P_{out} will decrease for a given input power as the Joule heat in the solder joint increases. The P_{out} decreases as the thermal shock cycle increases.

3.3. Gain

Figure 6 shows the gain characteristics under different shocks. As shown in Figure 6, the measured gain of PA decreases with the thermal cycle. For example, the gain of the PA decreases by 1.51 dB and 0.85 dB after 105 thermal cycles for P_{in} = −4 dBm and P_{in} = 15 dBm, respectively.

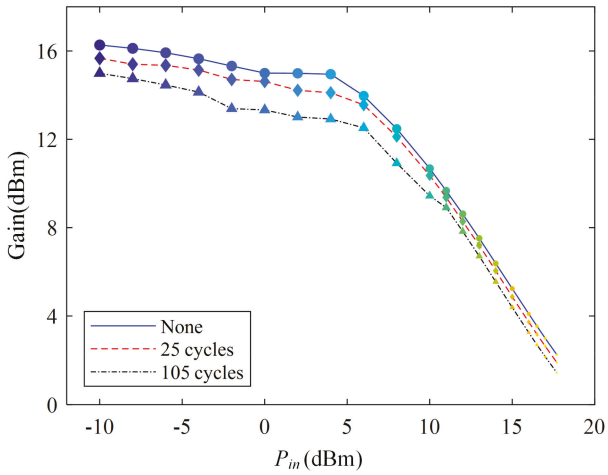


Figure 6. Gain of PA under thermal shock test.

The degradation of PA gain is similarly related to the mismatch of the thermal expansion coefficient of the PCB sheet material. A specific analysis is as follows.

The expression of gain is calculated by:

$$\text{Gain} = P_{out} - P_{in} \tag{12}$$

where P_{out} is the output power, and P_{in} is the input power.

From Section 3.2, the output power decreases with increasing high- and low-temperature shocks. According to Equation (12), The gain will decrease as the output power decreases. The gain degrades with the increase in high- and low-temperature shocks.

3.4. Power-Added Efficiency

Figure 7 shows the relationship between power added efficiency (PAE) and the number of high- and low-temperature shocks at 433 MHz. PAE decreases with the increase in high- and low-temperature impact times. For example, the PAE is 20.7% (P_{in} = 8 dBm). After 25 shocks, its PAE becomes 19.4%, indicating a decrease of 1.3% in PAE. After 105 shocks, the PAE decrease to 15.1%. When the input power is 16 dBm, the PAE decreases by 1.2% and 2.5% after 25 and 105 thermal cycles.

The following shows why PAE decreases with an increasing number of shocks. The expression of PAE is as follows [19]:

$$\text{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} \times 100\% \tag{13}$$

where P_{out} is the output power, P_{in} is the input power, and P_{DC} is the DC power.

According to Equation (13), PAE decreases as output power decreases. Furthermore, from Section 3.2, the P_{out} decreases with increasing high- and low-temperature shocks. Therefore, the PAE will also reduce with increasing high- and low-temperature shocks. The mismatch in the thermal expansion coefficient of the PCB material will cause the PAE to decrease.

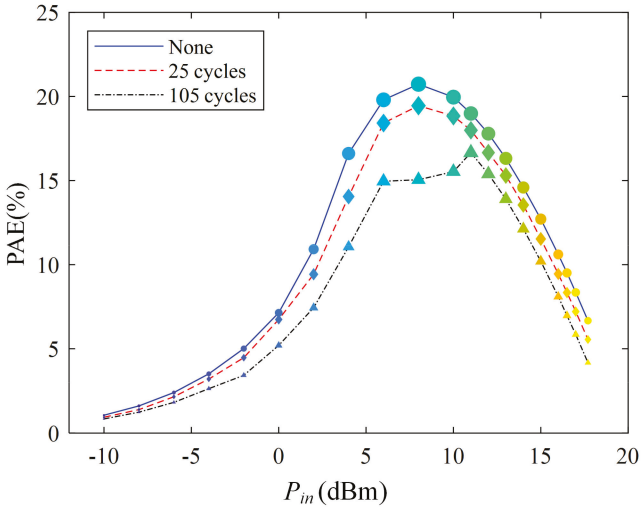


Figure 7. PAE of PA under thermal shock test.

4. Discussion and Conclusions

This paper takes a CMOS PA as an example to study the characteristics of the PA under high- and low-temperature shocks. The results of the experimental study showed that the critical specification of the PA degrades with the increasing number of high- and low-temperature shocks. From the previous analysis, we can observe that the main reason for the decrease in drain current is the increase in threshold voltage. Additionally, the main reason for the decrease in output power, gain and PAE is the thermal mismatch of PCB material. The change in the threshold voltage affects the transistor's performance and changes the operating state of the transistor. Thus, it affects the performance of the PA. The thermal expansion coefficient mismatch leads to increased resistance at the solder joints. The increase in resistance at the solder joints will increase the overall thermal power consumption of the circuit. This leads to a decrease in the output power of the PA. These two conditions affect the different specifications of the PA.

This experimental method used in this paper is different from the temperature experiments mentioned in the literature [9,10,12,14,15]. The experiments in the literature (refs [9,10,12,14,15]) are ordinary temperature experiments, which are reversible. After the temperature returns to room temperature, the circuit's performance also returns to its initial value. In contrast, the shock experiment between two temperatures conducted in this paper is destructive and irreversible. After the shock, the circuit's performance does not return to its initial value when the temperature returns to room temperature. To better illustrate this point, the degradation phenomena and mechanisms of PA critical specifications under thermal shock experiments and typical temperature experiments are specifically discussed and quantitatively analyzed in this paper, using the DC current of PA as an example. The experimental results show that the degree of influence and reason for the thermal shock test and temperature test on the degradation of PA's specifications are different.

High- and low-temperature shock tests can accelerate the degradation of critical specifications of PA, which is of great value and significance for the subsequent study of the lifetime of PA critical specifications. Furthermore, the thermal shock experimental method adopted in this paper can be transferred (or even directly replicated) to the degradation studies of the specifications of other electronic devices.

Author Contributions: Conceptualization, S.Z., C.Y. and J.W.; methodology, S.Z., C.Y. and J.W.; software, S.Z. and C.Y.; validation, S.Z., C.Y. and J.W.; formal analysis, J.W.; investigation, S.Z. and C.Y.; resources, J.W.; data curation, S.Z. and C.Y.; writing—original draft preparation, S.Z.; writing—review and editing, C.Y. and J.W.; visualization, S.Z. and C.Y.; supervision, J.W.; project administration, J.W.; funding acquisition, J.W. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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On-Chip Temperature Compensation for Small-Signal Gain Variation Reduction

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Abstract: Power amplifier (PA) specifications are closely related to changes in temperature; thus, the small-signal gain (S21) of PA decreases with the temperature increase. To compensate for the degradation caused by the decrease in S21, we present a compensation circuit that consists of two diodes and four resistors. At the same time, a differential stacked millimeter-wave wideband PA was designed and implemented based on this compensation circuit and 55 nm CMOS process. The post-layout simulation results showed that the fluctuation of S21 reduced from 2.4 dB to 0.1 dB in the frequency range of 25−40 GHz over the temperature range of −40 °C to 125 °C. Furthermore, the proposed on-chip temperature compensation circuit also applies to multi-stage cascaded microwave/mm-wave power amplifiers.

Keywords: millimeter-wave; CMOS; power amplifier; specification degradation; temperature compensation

1. Introduction

In today's highly developed communication industry, the spectrum resources for the low-frequency band are becoming increasingly scarce, which seriously restricts the development of the wireless communication industry. The millimeter-wave band has received much attention because of the abundant and unexplored spectrum resources. A PA is a key module of a millimeter-wave wireless communication system [1–3], and its performance directly determines the quality of a wireless communication system. Millimeter-wave communication systems, for example, wireless communication [4–7], radars [8–10], satellites [11,12], and navigation [13], usually operate in outdoor or extremely harsh places with significant temperature variations, and the specifications of PAs are closely related to the temperature variation. Temperature variation leads to the specification degradation of PAs [14–16], which makes the millimeter-wave wireless communication system unable to meet the normal operation requirements or even fail [17–20]. Therefore, reducing the effect of temperature change on the PA's specification degradation under the dynamic, temperature-changing operating environment has become an urgent problem.

To address the above issues, a lot of fruitful work has been carried out by domestic and international researchers. For example, in 2017, Javed S. Gaggatur et al. from the Indian Institute of Science and Technology proposed a technique for the performance compensation of integrated CMOS power amplifiers based on non-invasive temperature sensing, which is expected to compensate for degradation due to self-heating [21]. A new method for the temperature compensation of on-chip differential logarithmic amplifiers was proposed by Y. Wenger of the Technical University of Braunschweig, Germany, and A. Ghazinour of NXP Semiconductors in 2018 [22]. The results showed that better compensation is achieved in the temperature range of −40 °C to 125 °C. In 2018, Zhiming Chen et al. of the Beijing Institute of Technology proposed a new temperature compensation

method for K-band CMOS amplifiers [23], which achieves better compensation for PA gain in the temperature range of −45 °C to +125 °C. In 2020, Fariborz Lohrabi Pour et al. from Virginia Tech proposed a temperature-compensated power amplifier [24] that can operate reliably over a temperature range of −40 °C to +225 °C.

In summary, various temperature compensation techniques and methods have been successfully applied in the research and design of various single-stage and multi-stage power amplifiers. Still, little research has been reported on the temperature compensation of power amplifiers with stacked structures. However, the stacked structure is widely used to implement various high-output power PAs, because it increases the amplifier's output power [25].

Therefore, this paper presents a temperature compensation circuit for a stacked power amplifier consisting of only two diodes and four resistors. The proposed compensation circuit keeps the gain constant with the temperature by controlling the gate voltage. In addition, the compensation circuit uses the principle that the diode's threshold voltage decreases with the temperature increase. This study first investigated the temperature compensation circuit's operating principle and design method. Then, based on the proposed on-chip temperature compensation circuit and 55 nm CMOS technology, a differential stacked millimeter-wave wideband PA was implemented. As a result, the power amplifier's small-signal gain fluctuated from 2.4 dB to 0.1 dB in the temperature range of −40 °C to +125 °C, and the frequency range was 25−40 GHz.

2. Temperature Characteristics of Single-Stage Amplifier Gain

The gain of a single-stage PA decreases with increasing temperature [26], while the gain of a class AB PA increases with increasing gate voltage [27]. Therefore, the gain of the amplifier can be compensated by controlling the transistor gate voltage. The temperature characteristics of the gain of a single-stage PA are shown in Figure 1. When the gate voltage changes between 0.51 V and 0.61 V, the gain of the single-stage power amplifier remains unchanged in the range of −40 °C to +125 °C.

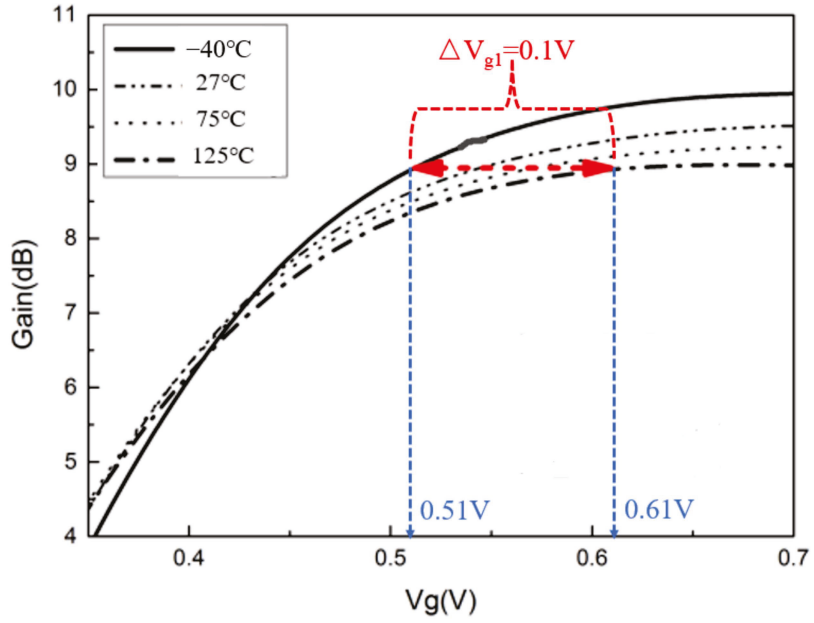


Figure 1. Temperature characteristics of gain of single-stage PA.

The transconductance in the saturated regions [28–30]:

$$g_{ms} = \frac{\partial I_D(sat)}{\partial V_{GS}} = \mu_n(T_0)\left(\frac{T}{T_0}\right)^{-3/2}\frac{WC_{ox}}{L}(V_{GS} - V_T), \quad (1)$$

where W is the gate width, μ_n is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, L is the gate length, V_{GS} is the gate voltage, V_T is the threshold voltage, V_{DS} is the drain voltage, and T_0 = 300 K.

Typically, the saturation voltage (V_{GS}-V_T) is chosen to be relatively large in order to obtain a large transconductance, so that the effect of the threshold voltage can be neglected. Moreover, its influence tends to dominate due to the exponential nature of carrier mobility [30]. Therefore, the transconductance usually decreases with increasing temperature, and the transconductance is usually considered as the gain of the transistor [29]. Consequently, the small-signal gain of the PA decreases with increasing temperature.

3. Principle and Design of Temperature Compensation Circuit

As described in Section 1, increasing the gate voltage can compensate for the change in amplifier gain. This temperature compensation circuit consists of two diodes and four resistors, as shown in Figure 2. The values of gate voltages V_{g1}, V_{g2}, and V_{g3} are determined by the V_r and V_{gc}. In Figure 2, D_1 and D_2 are diodes, R, R_1, R_2, and R_3 are resistors, and V_d and I are the current and voltage through the diodes, respectively. The compensation circuit shown in Figure 2 utilizes the mechanism whereby the threshold voltage of the diode decreases with increasing temperature.

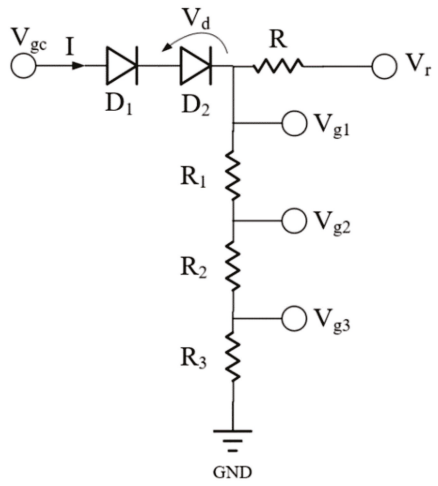


Figure 2. Schematic diagram of the compensation circuit.

To facilitate the presentation of the operating principle of the temperature compensation circuit, it is assumed that V_{gc} = 0. The following equation can be derived from Figure 2 [31].

$$-V_r = RI + 2V_d, \tag{2}$$

$$I = I_s\left\{\exp(\frac{qV_d}{nkT}) - 1\right\}, \tag{3}$$

where T is the temperature, and n is the ideal coefficient of the diode. I_s can be expressed as

$$I_s = SA^*T^2\exp(-\frac{q\phi_B}{kT}), \tag{4}$$

where A^* is the temperature-independent Richardson–Dushman constant, φ_B is the material-dependent Schottky barrier voltage, and S is the junction size of the diode. From (2), (3), and (4), it follows that V_{g1} is a function of T:

$$V_{g1} = 2\left\{\frac{kT}{q}\ln(\mathrm{SRA}^*) + \frac{2kT}{q}\ln(T) - \phi_B\right\}n, \tag{5}$$

where $V_{g1} = -2V_d$ (as shown in Figure 2).

Assume that $RI_s \ll -(V_r + 2V_d) \ll (1/RI_s)$. Then, from (4), the following equation can be derived.

$$\frac{\partial V_{g1}}{\partial T} = 2\frac{nk}{q}\{\ln(\mathrm{SRA}^*) + 2\ln(T) + 2\}, \tag{6}$$

If T is greater than -270 °C, we have $\partial V_{g1}/\partial T > 0$. V_{g1} increases with increasing temperature for T greater than -270 °C. The following equation can calculate the variation of V_{g1} (ΔV_{g1}) between two temperatures, T_H and T_L.

$$\begin{array}{l} \Delta V_{g1} = \int_{T_L}^{T_H} \frac{\partial V_{g1}}{\partial T} dT = \int_{T_L}^{T_H} 2\frac{nk}{q}\{\ln(\mathrm{SRA}^*) + 2\ln(T) + 2\} dT \\ = \frac{2nk}{q}(T_H - T_L)\ln(\mathrm{SRA}^*) + \frac{4nk}{q}(T_H ln(T_H) - T_L ln(T_L)) \end{array} \tag{7}$$

Therefore, the expressions for V_{g2} and V_{g3} can be obtained according to Figure 2 and Equation (5).

$$V_{g2} = V_{g1}\frac{R_2 + R_3}{R_1 + R_2 + R_3}, \tag{8}$$

$$V_{g3} = V_{g1}\frac{R_3}{R_1 + R_2 + R_3}, \tag{9}$$

According to (8) and (9), V_{g2} and V_{g3} are proportional to V_{g1}, increasing with temperature. Therefore, V_{g2} and V_{g3} also increase with temperature in order to realize gain compensation. The following explains the compensation circuit's principle to compensate for the PA's small-signal gain.

When the temperature increases, gate voltage V_{g1}, gate voltage V_{g2}, and gate voltage V_{g3} in the temperature compensation circuit all increase as the temperature increases. The increase in gate voltage V_{g1}, gate voltage V_{g2}, and gate voltage V_{g3} is equivalent to the rise in the magnitude of V_{GS} of Equation (1). When V_{g1}, V_{g2}, and V_{g3} increase with temperature, the transconductance of each layer of the stacked PA can be expressed as

$$g_1 = \frac{\partial I_D(\mathrm{sat})}{\partial V_{GS}} = \mu_n(T_0)\left(\frac{T}{T_0}\right)^{-3/2}\frac{WC_{ox}}{L}(V_{g1} + \Delta V_{g1} - V_T), \tag{10}$$

$$g_2 = \frac{\partial I_D(\mathrm{sat})}{\partial V_{GS}} = \mu_n(T_0)\left(\frac{T}{T_0}\right)^{-3/2}\frac{WC_{ox}}{L}(V_{g2} + \Delta V_{g2} - V_T), \tag{11}$$

$$g_3 = \frac{\partial I_D(\mathrm{sat})}{\partial V_{GS}} = \mu_n(T_0)\left(\frac{T}{T_0}\right)^{-3/2}\frac{WC_{ox}}{L}(V_{g3} + \Delta V_{g3} - V_T), \tag{12}$$

According to Equations (10)–(12), the transconductance (i.e., gain) of each layer increases with ΔV_{g1}, ΔV_{g2}, and ΔV_{g3}, i.e., with the increase in temperature. Thus, the compensation for the degradation of the gain of each layer with the increase in temperature is achieved.

It should be noted that the on-chip temperature compensation circuit described in this section does not have any additional requirements or constraints on the design of the PA. In addition, the compensation circuit was designed for a single-stage PA. Specifically, for a multi-stage PA, the parameters of each transistor stage are different. Then, it is necessary to determine the value of ΔV_g, similar to the one shown in Figure 1, based on the parameters of each transistor stage. From Equation (7), it can be seen that the parameters affecting ΔV_{g1} are mainly the junction size (S) and resistance (R) of the diode. Therefore, for a multi-stage PA, the design of the corresponding temperature compensation circuit can be completed by simply adjusting the values of S and R so that the ΔV_{g1} (as shown in Equation (7)) of each stage meets the requirements similar to the ΔV_{g1} in Figure 1.

4. Differential Stacked Millimeter-Wave Broadband PA

To verify the effectiveness of the proposed on-chip temperature compensation circuit, a differential stacked millimeter-wave wideband PA was implemented in this study. Figure 3

shows the schematic of a differential stacked millimeter-wave wideband PA, which is used to compensate for the degradation of small-signal gain. As shown in Figure 1, the required ΔV_{g1} is 0.1 V. Two diodes are connected in series to achieve ΔV_{g1} = 0.1 V.

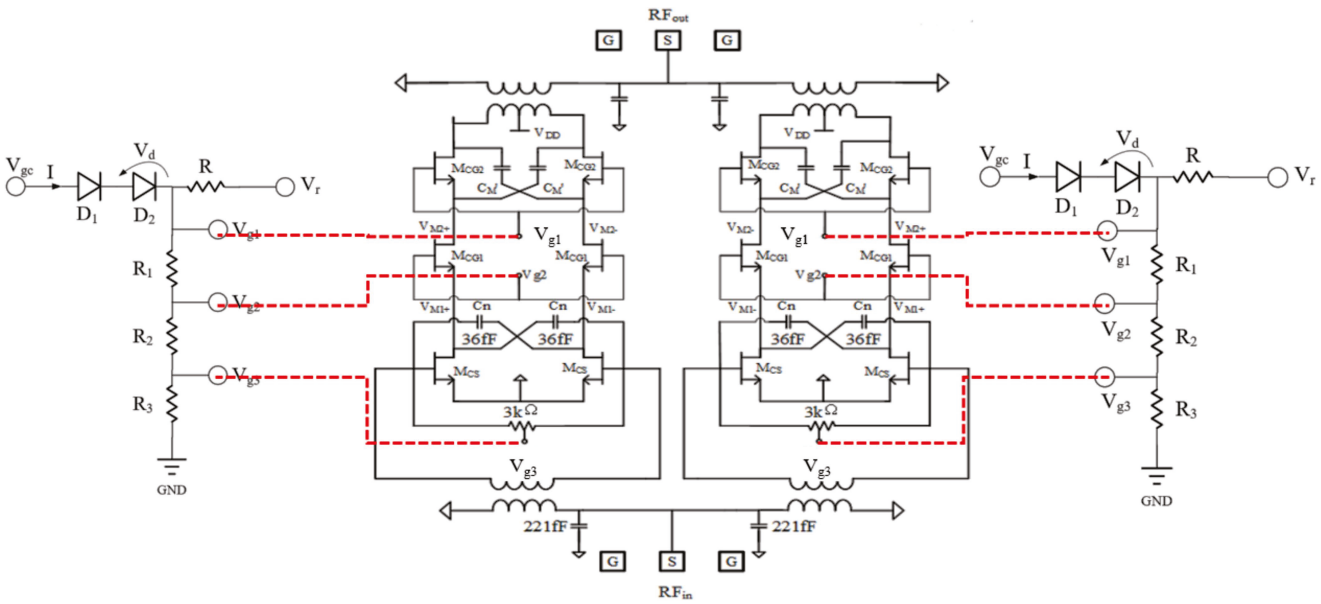


Figure 3. Schematic diagram of differential stacked PA, based on temperature compensation circuit.

Differential common-source structures [32,33] and stacked structures [34,35] are two circuit topologies commonly used in PA design. The differential common-source structure can suppress even harmonics. In contrast, the stacked structure can achieve a large output voltage swing (i.e., the transistors are connected in series to achieve a superposition of bias voltages and increase the output voltage swing of the PA) while ensuring that the transistors do not break down, thus increasing the output power of the PA. We designed and implemented a differential triple-stacked millimeter-wave broadband PA with on-chip temperature compensation based on the differential common-source structure and stacked structure.

The PA uses a two-way differential stacking structure to increase the output power and improve the stability of the PA by introducing a negative feedback network. To increase the bandwidth and reduce losses, on-chip transformers were used for the matching networks at the input/output of the PAs designed in this study. A thick metal layer was used in the design process for the on-chip transformer and interconnecting lines. As shown in Figure 3, the gate width/gate length of transistors M_{CG2}, M_{CG1}, and M_{CS} were 4 × 60 μm/60 nm, 4 × 60 μm/60 nm, and 3 × 60 μm/60 nm, respectively. Meanwhile, to improve power gain, isolation, and gain flatness, the neutralizing capacitor (C_n), shunt capacitor (C_{in}), and shunt resistor (R_g), respectively, were introduced in this study.

Although introducing a neutralization capacitor (C_n) can improve the stability of a PA to some extent, the PA will still be unstable when the parasitic capacitance (C_M) between the source and drain of transistor M_{CG2} is relatively large. This is also one of the main reasons for the instability of the stacked structure amplifier. Therefore, as shown in Figure 4, this study introduced another capacitor (C_M') in the negative feedback network of the top layer in order to improve stability. The capacitor (C_D) is the raw capacitance of the drain of transistor, M_{CG1}. The regulation of C_M' is used to achieve a balance between the three capacitors C_M', C_M, and C_D in order to achieve the stability of the PA.

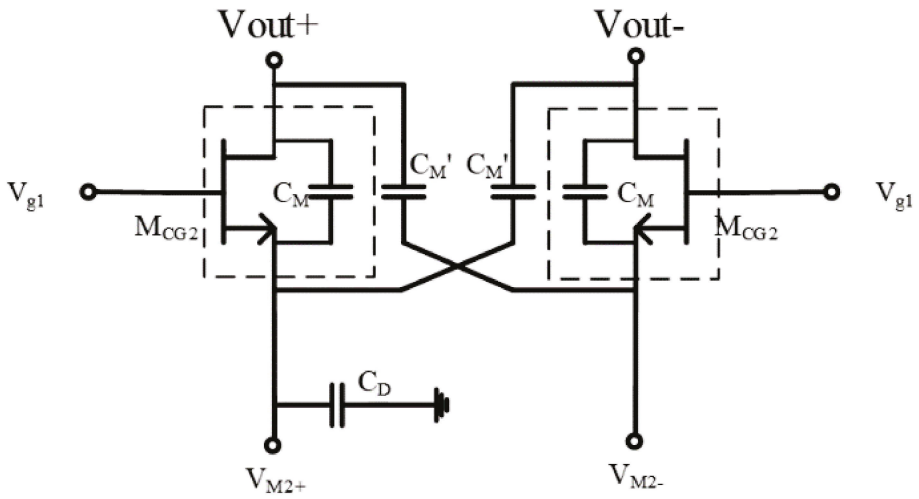


Figure 4. Schematic diagram of the negative feedback network.

The stability of the PA is shown in Figure 5. According to Figure 5, this PA's stability factor (K) in the range of 0–5 GHz was greater than 1 without introducing C_M', and the PA was in a stable state. The StabFact in the other frequency ranges was less than 1, and the PA was in an unstable condition. When C_M' was introduced into the PA, the stability factor of the PA in the whole frequency range was always greater than 1. As a result, the PA remained stable over the entire operating frequency range. This indicates that the introduction of capacitance (C_M') in the negative feedback network of the top layer of this stacked PA can effectively improve the stability of the PA.

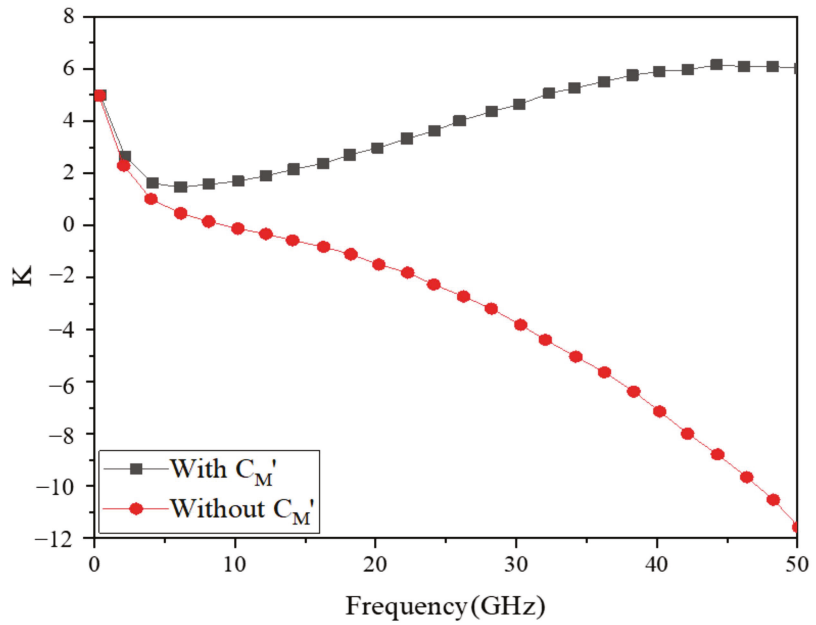


Figure 5. Stability factor of PA.

Figure 6 shows the core layout and overall layout of a differential stacked millimeter-wave wideband PA. The layout of the PA has a significant impact on the performance of the PA. Therefore, to simplify the RF signal path to reduce power consumption, we kept the layout of transistors M_{CG1} and M_{CG2} in the stacked structure, shown Figure 3, perpendicular to the direction of transistor M_{CS} when laying out the PA. The overall area of the PA chip was 0.378 mm^2.

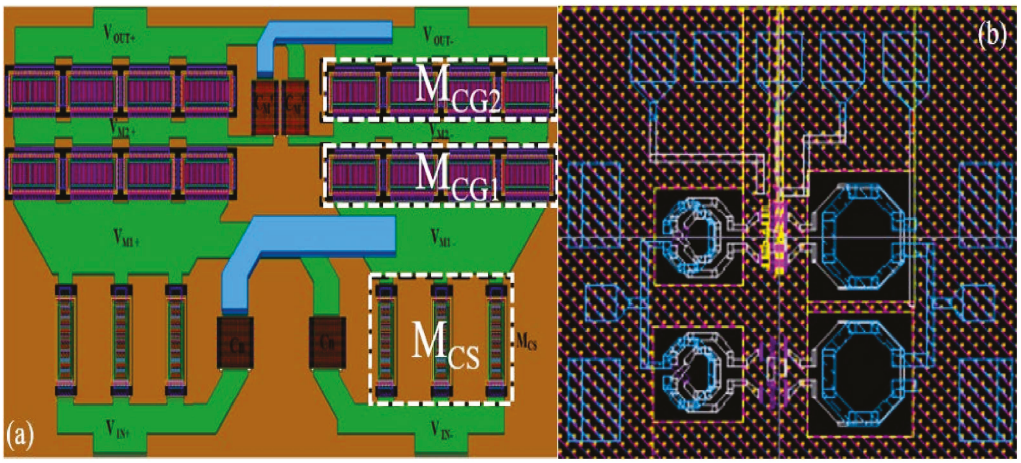


Figure 6. PA's overall layout and core layout: (**a**) core layout; (**b**) overall layout.

5. Results and Discussion

5.1. Small-Signal Gain at Different Temperatures

Figure 7 gives the small-signal gain versus temperature variation for the differential stacked millimeter-wave broadband power amplifier. Figure 7a,b show the results without and with temperature compensation circuits, respectively.

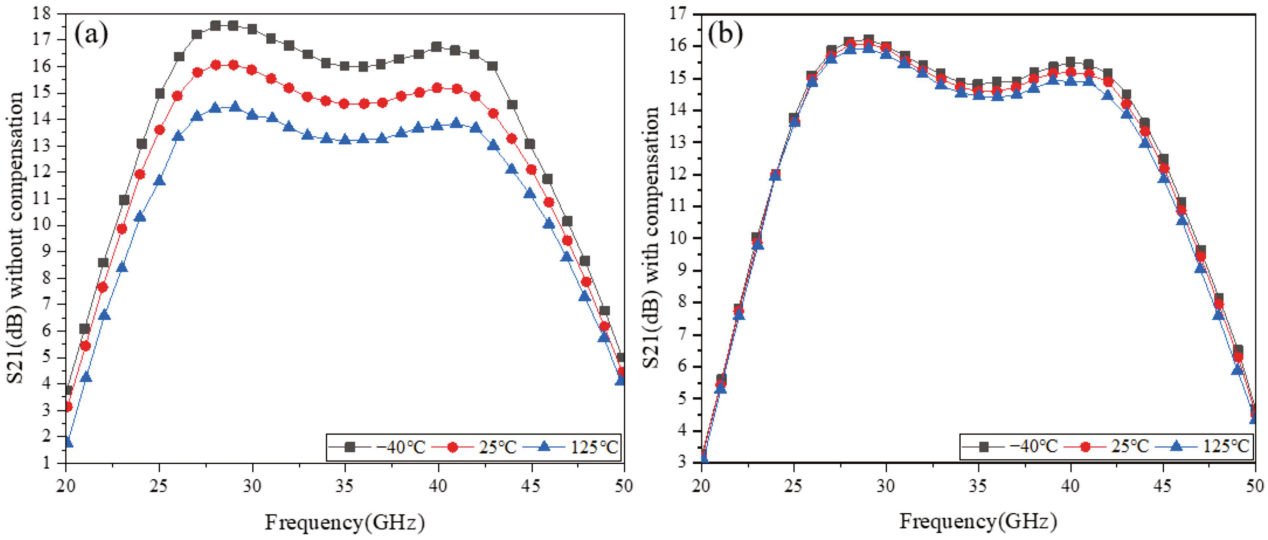


Figure 7. Small-signal gain versus temperature variation: (**a**) without temperature compensation; (**b**) with temperature compensation.

As seen in Figure 7, without the compensation, the small-signal gain varied by 2.4 dB in the frequency range of 25–40 GHz, while with the compensation, the small-signal gain varied by 0.1 dB in the frequency range of 25–40 GHz. The specific reasons are discussed below.

The small-signal gain is the transconductance [29], and the expression for the transconductance is

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{ds}}, \tag{13}$$

and the main factors affecting the transconductance are μ_n and I_{ds}, where the expression for the drain current in the saturation region is [36]

$$I_{ds} = \mu_n C_{ox} (\frac{W}{L})(V_{gs} - V_{th})^2, \tag{14}$$

where V_{gs} is the gate voltage, and V_{th} is the threshold voltage.

When V_{gs} increases, Ids also increases with the rise of V_{gs}. It is also known from Equation (13) that the small-signal gain increases as I_{ds} increases. When the temperature rises, μ_n decreases with the increase in temperature, resulting in a reduction in small-signal gain. With the compensation, I_{ds} increases as the temperature rises to effectively compensate for the degradation of the small-signal gain due to μ_n. In other words, the gate voltage V_{g1}, gate voltage V_{g2}, and gate voltage V_{g3} increase with the temperature, which increases the I_{ds}, and thus, compensates for the small-signal gain. This indicates that the on-chip temperature compensation circuit has a good compensation effect on the small-signal gain.

5.2. Output Power and PAE at Different Temperatures

The output power (P_{out}) and large-signal gain at the center frequency of the PA versus temperature are shown in Figure 8. As shown in Figure 8a, the P_{out} and large-signal gain with an on-chip temperature compensation circuit varied very little. In contrast, the PA's output power and large-signal gain without a temperature compensation circuit were more significantly affected by temperature variations.

The power-added efficiency (PAE) at the center frequency of the PA versus temperature is shown in Figure 9. It is worth noting that the effect of temperature on the PA's power-added efficiency was relatively large, regardless of whether it was with compensation. This indicates that the compensation circuit has a better compensation effect on the P_{out} and large-signal gain, while the compensation effect on the PAE is insignificant. The specific reasons are discussed below.

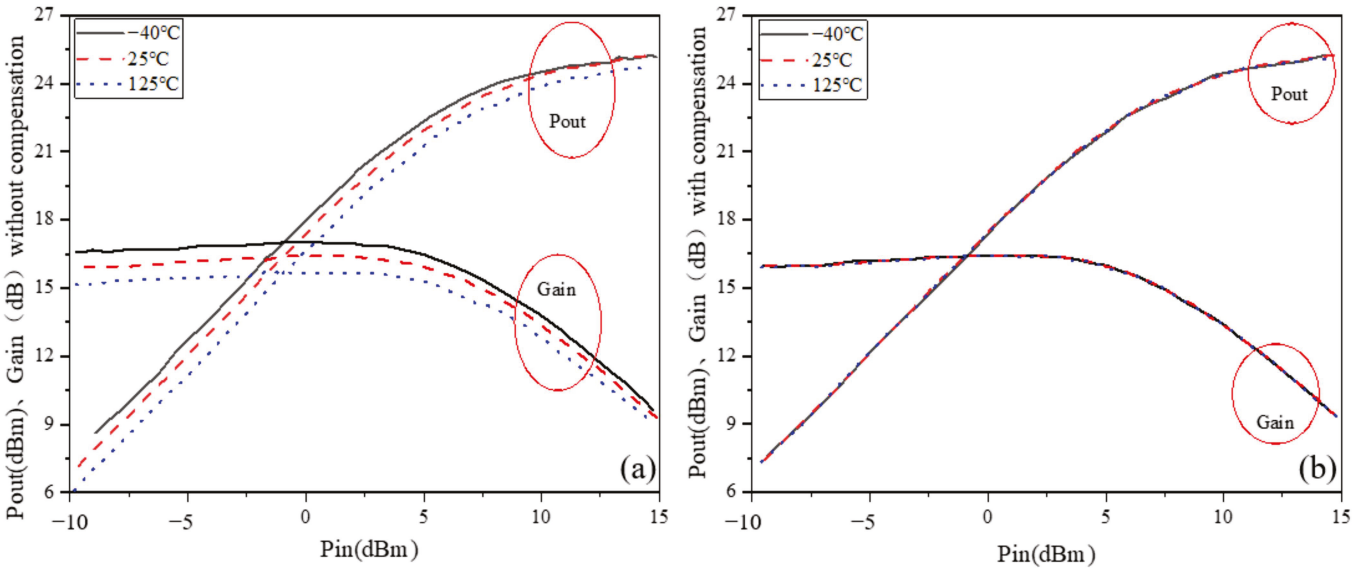


Figure 8. Output power versus temperature variation: (**a**) without temperature compensation; (**b**) with temperature compensation.

Literature studies have shown [37] that the on-state resistance between source and drain increases with temperature, which leads to a drop in the P_{out}. The expression for on-resistance is [37]

$$R_{on} = R_0 + kT^{\alpha} / \left| V_{gs} - V_{th} \right|^{\beta}, \quad (15)$$

where the constant k is a process parameter, R_0 is a constant independent of voltage and temperature, $\alpha \approx 1.5$, $\beta \approx 0.2$, V_{gs} is the gate voltage, and V_{th} is the threshold voltage.

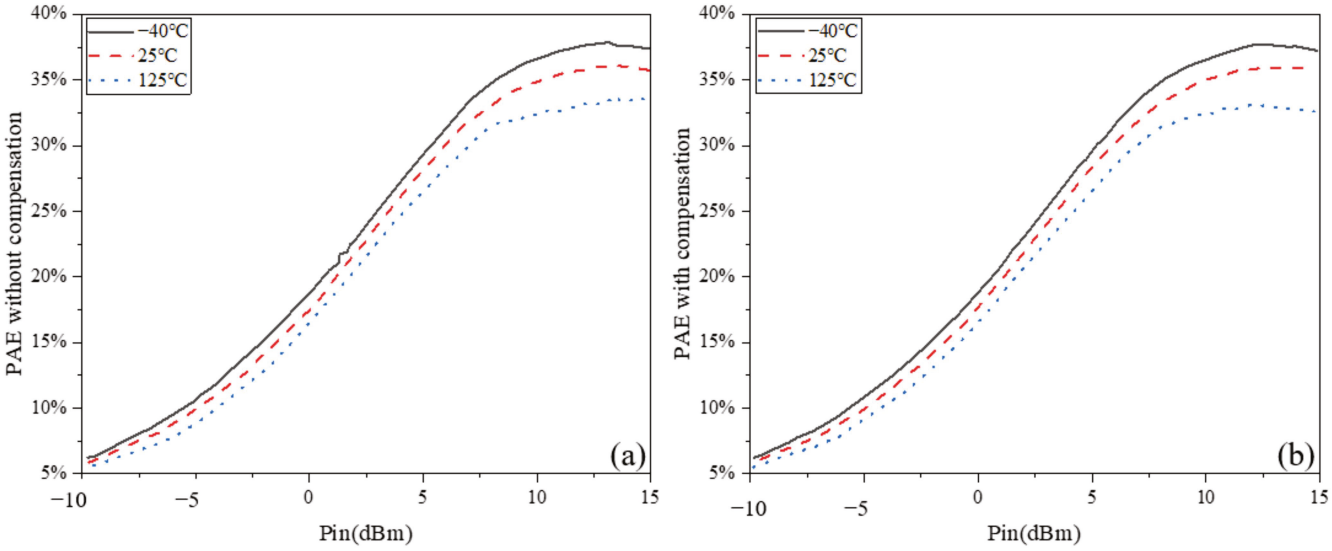


Figure 9. PAE versus temperature variation: (**a**) without temperature compensation; (**b**) with temperature compensation.

According to Equation (15), on-resistance increases with increasing temperature. Therefore, when the PA does not have a temperature compensation circuit, the P_{out} decreases with increasing temperature. On the other hand, when the PA is with compensation, the gate V_{gs} in Equation (15) increases with the temperature, causing the on-resistance to decrease with the gate voltage increase, thus achieving the compensation for the P_{out}. As a result, the compensation for the large-signal gain is also achieved. As for the PAE, the compensation circuit compensates for the P_{out} while increasing the DC power consumption of the PA [24]. Therefore, according to the definition of PAE, the PAE decreases with the increase in DC power consumption. Thus, with or without compensation, the effect of temperature change on PAE of PA is relatively significant [24].

Table 1 compares the amplifier's performance with on-chip temperature compensation circuits. Compared with the compensation circuit structures and methods in the literature [23,24,38–40], the temperature compensation circuit proposed in this paper has a simple structure, a smaller overall chip area, and a better compensation effect for small-signal gain and output power. Still, the compensation effect for PAE was poor. In addition, these post-layout simulation results can be regarded as a supplement to the measured results in Refs. [23,38–40]. This idea is consistent with Ref. [24], and these results are effective in the relative amount of change in small-signal gain, output power, and PAE before and after compensation.

Table 1. Performance comparison with previous works.

Reference	Ref. [23]	Ref. [38]	Ref. [39]	Ref. [40]	Ref. [24]	This Work ②
Circuit	PA	LNA	LNA	PA	PA	PA
Technology	90 nm	130 nm SOI	130 nm	40 nm	GaN HEMT	55 nm
Topology	2-stage	1-stage	1-stage	3-stage	1-stage	1-stage
Frequency (GHz)	26.5	2.4	15.2	79	4.5–5.5	25–40
Small-signal gain variation (dB)	1.2 (−45~125 °C)	0.9 (25~200 °C)	3.1 (−20~120 °C)	0.6 (10~100 °C)	0.4 (−40~225 °C)	0.1 (−40~125 °C)
Pout variation (dBm) (center frequency)	N/A	N/A	N/A	N/A	24.0 (−40~225 °C)	0.6 (−40~125 °C)

Table 1. *Cont.*

Reference	Ref. [23]	Ref. [38]	Ref. [39]	Ref. [40]	Ref. [24]	This Work ②
PAE variation (center frequency)	N/A	N/A	N/A	N/A	12% (−40~225 °C)	7.3% (−40~125 °C)
Area (mm^2)	0.5 ①	0.6 ①	0.6 ①	0.11 ①	6.6	0.378

Note: ① DC pads are not included. ② Post-layout simulation results.

Furthermore, in terms of the magnitude of small-signal gain variation with temperature, the compensation circuit can effectively compensate for the small-signal gain. This shows that the proposed compensation circuit for differential stacked millimeter-wave wideband PAs effectively compensates for the degradation of the small-signal gain of PAs due to temperature variations over a wide range.

6. Conclusions

This paper proposes a compensation circuit consisting of two diodes and four resistors for a PA with a stacked structure. To verify the effectiveness of the compensation circuit, we designed and implemented a differential triple-layer stacked structure millimeter-wave wideband PA.

With the temperature-compensation circuit, the small-signal gain variation improved from 2.4 to 0.1 dB in the temperature range between −40 °C and 125 °C. It was demonstrated that the proposed on-chip temperature compensation circuit effectively corrects the small-signal gain, large-signal gain, and P_{out} variations of a millimeter-wave PA with a multi-layer stacked structure over a wide temperature range. In addition, the proposed on-chip temperature compensation circuit also applies to multi-stage cascaded microwave/mm-wave power amplifiers.

Author Contributions: Conceptualization, S.Z., S.W. and J.W.; methodology, S.Z., S.W. and J.W.; software, S.Z. and S.W.; validation, S.Z., S.W. and J.W.; formal analysis, J.W.; investigation, S.Z. and S.W.; resources, J.W.; data curation, S.Z. and S.W.; writing—original draft preparation, S.Z.; writing—review and editing, S.W. and J.W.; visualization, S.Z. and S.W.; supervision, J.W.; project administration, J.W.; funding acquisition, J.W. All authors have read and agreed to the published version of the manuscript.

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Fabrication and Electrical Characterization of High Aspect Ratio Through-Silicon Vias with Polyimide Liner for 3D Integration

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Abstract: High aspect ratio (HAR) through-silicon vias (TSVs) are in urgent need to achieve smaller keep-out zones (KOZs) and higher integration density for the miniaturization of high-performance three-dimensional (3D) integration of integrated circuits (IC), micro-electro-mechanical systems (MEMS), and other devices. In this study, HAR TSVs with a diameter of 11 μm and an aspect ratio of 10:1 are successfully fabricated in a low-cost process flow. Conformal polyimide (PI) liners are deposited using a vacuum-assisted spin coating technique, and the effects of spin coating time and speed on the deposition results are discussed. Then, continuous Cu seed layers are fabricated by sequential sputtering and ultrasound-assisted electroless plating. Additionally, void-free and seamless Cu conductors are formed by electroplating. Moreover, a semi-additive method is used to fabricate the redistribution layers (RDLs) on the insulating layers of photosensitive PI (PSPI). Notably, a plasma bombardment process is introduced to remove residual PSPI in the contact windows between RDLs and central pillars. Results show that the resistance of a single TSV from a daisy chain of 144 TSVs with density of 2000/mm^2 is about 28 mΩ. Additionally, the S-parameters of a single TSV are obtained using L-2L de-embedding technology, and the experimental and simulated results agree well. The proposed low-cost fabrication technologies and the related electrical characterization of PI-TSVs are significant for the application of HAR TSVs in modern heterogeneous integration systems.

Keywords: three-dimensional (3D) integration; high aspect ratio (HAR) through-silicon vias (TSVs); polyimide (PI) liner; Cu seed layer; redistribution layers (RDLs); S-parameters

1. Introduction

With the continuous development of lithography technology, and manufacturing processes, novel structures such as fin-shaped field-effect transistors (Fin FETs) [1] and gate -all-around nanowire field-effect transistors (GAA nanowire FETs) [2] have been proposed to extend the Moore's law. However, the feature size of integrated circuits (ICs) is still approaching the physical limit [3]. At the same time, as the length of the global interconnects is increasing exponentially, the delay and power consumption caused by the interconnects gradually exceeds those of the transistors and even plays a decisive role in the performance of ICs [4]. Thanks to the introduction of vertical interconnects, three-dimensional (3D) integration technology features advantages, such as reduced length and power consumption of global interconnects, increased transmission bandwidth, smaller chip footprint, and improved integration levels [5,6]. Additionally, 3D integration can realize the heterogeneous integration of multiple devices of various materials, processes, and functionalities [7,8]. As one of the key technologies for 3D integration, through-silicon vias (TSVs) can provide vertical electrical interconnects among different device layers within a compact package. In 2007, Toshiba reported the integration of TSVs in commercial CMOS image sensors, which was the first application of TSV in mass-produced devices [8]. Since then, many semiconductor manufacturers have begun to launch their own TSV

products, and TSV technology has been vigorously developed and widely used. Recently, the trends in electronic products for a smaller size and better performance put forward higher requirements for TSVs, including reducing keep-out zones (KOZs), increasing interconnection density, decreasing parasitic parameters, etc. [9,10]. Therefore, the demand for high aspect ratio (HAR) TSVs with low parasitic parameters is very urgent.

Generally, the TSV usually consists of a liner, a barrier/adhesion layer, and a central conductor [11]. SiO_2 is widely used as the liner of TSVs and traditional SiO_2 liner is deposited by thermal oxidation or plasma-enhanced chemical vapor deposition (PECVD). However, the process temperature of thermal oxidation is too high, which is not suitable for the via-last process [12]. Additionally, the liner deposited by PECVD has many residual impurities and obvious thermal stresses [13], and it is difficult to keep continuous in HAR TSVs. Moreover, there is a huge mismatch in the coefficients of thermal expansion (CTEs) among Cu (CTE: 16.5 ppm/K), Si (CTE: 2.5 ppm/K), and SiO_2 (CTE: 0.5 ppm/K) [14,15], which leads to severe thermal reliability issues.

Recently, polymers such as polyimide (PI), benzocyclobutene (BCB), and epoxy resin are used as liners due to their lower Young's moduli and lower dielectric constants [16]. For example, compared with the SiO_2 liner, PI liner can achieve smaller parasitic capacitance, smaller leakage currenst, and better thermal reliability [17]. In HAR TSVs with a small diameter, PI liner with a high step coverage has been realized by our group through a low-cost vacuum-assisted spin coating technique [18]. This approach is simple to operate, and the process temperature is relatively low (no more than 240 °C). Additionally, the fabricated PI liner can smooth the scallops caused by Bosch etching, thus avoiding interface delamination and improving the mechanical stability of the TSVs [19].

So far, there is some literature on TSVs with PI liner (PI-TSVs) [20–23]. However, most of them focus on the fabrication and tests of blind TSVs without involving double-side redistribution layers (RDLs). Therefore, it is significant to propose a whole process flow for true PI-TSVs with RDLs, especially for those with HAR. Furthermore, although the leakage current and capacitance-voltage (C-V) characteristics of PI-TSVs have been studied [24–26], the radio frequency (RF) performance of PI-TSVs, such as S-parameters, is still lacking in investigation.

In this paper, HAR PI-TSVs with double-side RDLs are fabricated and the electrical characteristics, including direct current (DC) resistance and S-parameters, are evaluated. A low-cost fabrication flow suitable for HAR TSVs is proposed based on the optimizations on several key processes. The effects of spin coating time and speed on the deposition results are discussed to facilitate the formation of conformal PI liners in HAR TSVs. Additionally, sequential sputtering and electroless plating is used to fabricate continuous Cu seed layers. The addition of ultrasonic assistance during electroless plating increases the deposition efficiency and improves the uniformity of the Cu seed layers. Then, void-free and seamless Cu conductors are formed by electroplating. Subsequently, photosensitive PI (PSPI) is deposited as the insulating layer in the field area. A plasma bombardment process is proposed to remove the residual PSPI in the contact windows before fabricating RDLs using the semi-additive process. The resistance of a single TSV from a daisy chain of 144 TSVs is measured. Additionally, the S-parameters of a single TSV are obtained using L-2L de-embedding technology, which are in good consistence with the simulation results.

2. Process Design

Figure 1 shows the schematic of the fabrication processes for the HAR PI-TSVs proposed in this paper. First, blind vias are formed by deep reactive ion etching (DRIE) (Figure 1a). Then, PI liner is deposited through a vacuum-assisted spin coating technique, as shown in Figure 1b. After that, TiN is deposited as barrier by atomic layer deposition (ALD) (Figure 1c). Next, the Cu seed layer is fabricated by sequential sputtering and electroless plating (Figure 1d), and Cu central conductors are then formed by electroplating (Figure 1e). In order to smooth the wafer surface, a chemical mechanical polishing (CMP) process is adopted to remove the redundant Cu, TiN, and PI, as shown in Figure 1f. Then,

the PSPI insulating layer is deposited and patterned (Figure 1g), after which the front-side Cu RDLs are fabricated by a semi-additive process (Figure 1h). Next, the wafer is bonded upside down with a Pyrex 7740 glass holder using benzocyclobutene (BCB) as the bonding glue (Figure 1i). Subsequently, the back-side Si substrate is thinned and polished until the Cu pillars are exposed (Figure 1j). Finally, the back-side insulating layer and RDLs are also fabricated, as shown in Figure 1k,l. It can be seen that the proposed fabrication flow for the HAR PI-TSVs is low-cost, convenient, and compatible with IC processes. Actually, there are several key processes in the fabrication flow, such as the formation of liner, seed layer, and double-side RDLs, which will be discussed in detail next. Notably, in this work, some optimizations are performed on the key processes to facilitate the fabrication of the HAR PI-TSVs, including the investigation and control of spinning time and speed for the liner formation, the introduction of ultrasound assistance for the seed layer formation, the use of the PSPI insulating layer, and the proposed two-step plasma bombardment process to guarantee the connection between the Cu pillar and RDLs.

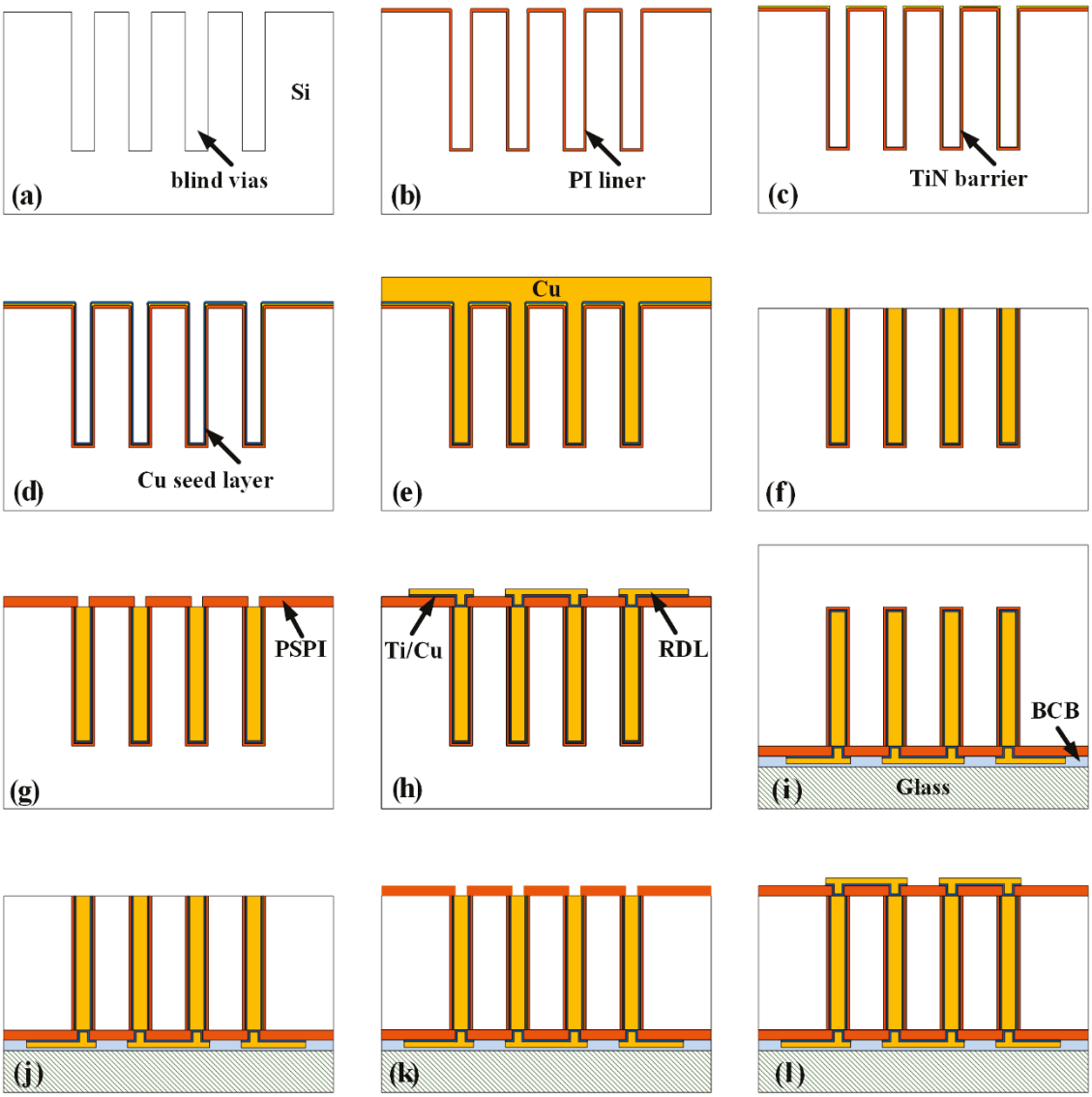


Figure 1. Schematic of the process flow for the HAR PI-TSVs: (**a**) Si DRIE, (**b**) vacuum-assisted spin coating of PI, (**c**) ALD of TiN, (**d**) sputtering and electroless plating of Cu seed layer, (**e**) Cu electroplating, (**f**) front-side CMP, (**g**) deposition of front-side PSPI insulating layer, (**h**) fabrication of front-side Cu RDLs, (**i**) permanent bonding, (**j**) back-side thinning and CMP, (**k**) deposition of back-side PSPI insulating layer, (**l**) fabrication of back-side Cu RDLs.

2.1. Vacuum-Assisted Spin Coating of PI

It is critical to deposit a conformal liner in the HAR TSVs for isolating the substrate from the central conductors and facilitating the following deposition of other layers. A low-cost and low-temperature process named the vacuum-assisted spin coating technique is used in this work to fabricate a conformal PI liner in the HAR TSVs. The process flow of the vacuum-assisted spin coating technique is shown in Figure 2, which mainly includes three steps: PI dispensing, vacuum treatment, and spin coating. Before the dispensing step, the as-etched substrate is first cleaned with acetone, isopropyl alcohol (IPA), and deionized water (DI water) with the assistance of ultrasound treatment, followed by an O_2 plasma clean to increase its adhesivity with PI. Then, PI (PI-5J, YiDun New Material Co., Ltd., China) with a specific viscosity is dispensed from the center of the sample outwards with a dropper until the sample surface is completely covered by PI (Figure 2a). After which, the sample is immediately transferred to a vacuum chamber (HASUC, DZF-6050) for a 5 min vacuum treatment. Due to the pressure difference between the trapped air inside the blind vias and the external vacuum environment, the trapped air can escape out rapidly and the PI will fully fill the interior of the blind vias (Figure 2b). Next, the PI inside the vias is spined out except for that attached to the sidewall through a two-step spin coating procedure. The low-speed state will shake off the excess PI in the field area and level the surface, while the PI inside the blind vias will be spined out under the actions of centrifugal force and intermolecular force in the high-speed state [14], leaving a thin PI layer on the sidewall of the vias, as shown in Figure 2c. Finally, the PI liner is cured in N_2 ambient; more details of this will be mentioned in Section 3.

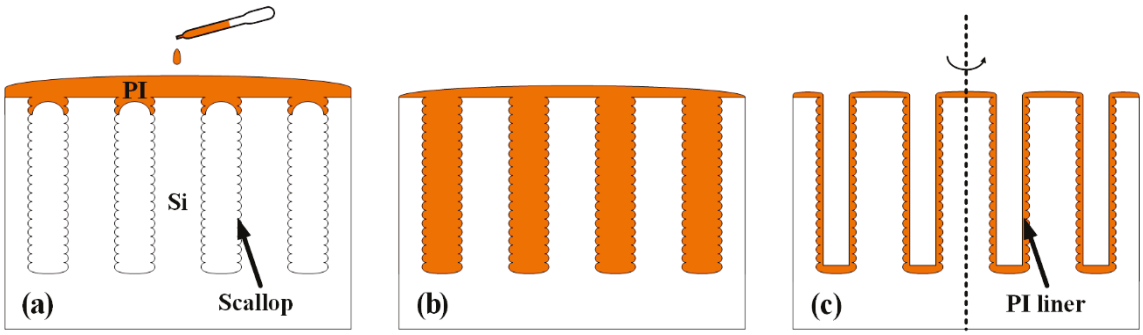


Figure 2. Schematic of the vacuum-assisted spin coating technique: (**a**) dispensing of PI, (**b**) vacuum treatment, (**c**) spin coating of PI.

2.2. Electroless Plating of Cu

The quality of the seed layer has a great influence on the result of upcoming Cu electroplating, and a continuous and dense seed layer is necessary to form a good central conductor. Since sputtering is not sufficient to fabricate continuous Cu seed layers in TSVs with aspect ratios exceeding 10:1, and the adhesion of electroless Cu to the TiN barrier is not so good, a combination of sequential sputtering and electroless plating is proposed to achieve continuous Cu seed layer deposition in HAR TSVs [27,28]. The electroless plating process mainly includes six steps, as shown in Figure 3. The sample is first immersed into DI water and a vacuum treatment is conducted to evacuate the air inside the vias. Then it is transferred to Conditioner solution to clean the sample surface. Immediately thereafter, the sample is placed in the pre-dip solution and another vacuum treatment is carried out to fully wet the reaction surface. Next, Pd ions are first adsorbed and then reduced on the via sidewall in the activator solution and reducer solution, respectively, which act as the catalysts to the Cu reduction. Finally, Cu seed layers can be formed by the reduction in Cu ions with the catalysis of Pd in the Electroless Cu solution. The solutions used in the electroless plating process are commercially available (Neoganth, Atotech Ltd., Germany). Notably, using ultrasonic assistance will help Cu ions to diffuse into the vias, thus enhancing the reaction efficiency and improving the step coverage of seed layers [29].

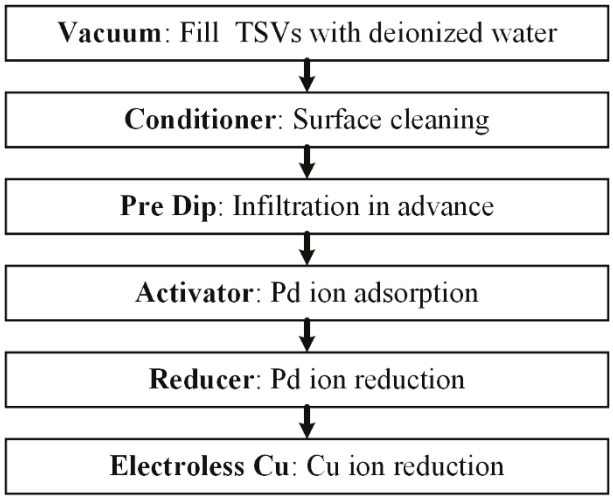


Figure 3. Steps of electroless plating of Cu.

2.3. Fabrication of PSPI Insulating Layer and Cu RDLs

After the formation of blind TSVs, the fabrication of double-side surface insulating layers and RDLs is also crucial for the TSVs to realize vertical electrical interconnections. PSPI (JAPB-101, 1000–1100 cP) is used as the field insulating layer in this work, and its deposition process is similar to that of photoresist. Actually, there are two key points in the fabrication of PSPI insulating layer. On the one hand, the contact window on the PSPI for the electrical connection between the TSV and the RDL should be located exactly on the central pillar and avoid exposing the substrate. Ideally, the center of the window is on the same line as the axis of the TSV, as shown in Figure 4a. However, due to factors such as the error of lithography alignment, the flatness of sample surface after CMP, and the steepness of the vias caused by DRIE, there are deviations in the actual lithography pattern, as shown in Figure 4b. In severe cases as shown in Figure 4c, there will be serious leakage between the RDL and the substrate due to the exposure of surrounding substrate, which will destroy the performance of the device. Therefore, in this paper, the diameter of the contact window is designed to be 4 μm smaller than that of the central pillar for larger tolerances. On the other hand, the contact window must be clean with no PSPI residues to ensure good contact between the RDL and the pillar. In this work, a plasma bombardment treatment is introduced to guarantee the removal of PSPI in the contact window, which will be discussed in detail in Section 3.

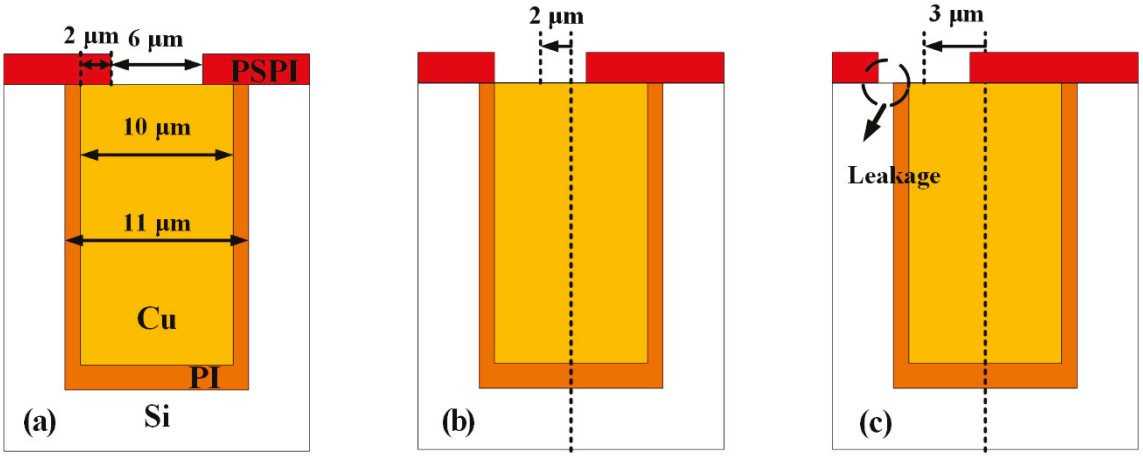


Figure 4. Schematic of lithography alignment of PSPI insulating layer: (**a**) ideal situation, (**b**) slight deviation, (**c**) serious deviation.

The RDLs are fabricated by the semi-additive process, as shown in Figure 5. The steps include: (a) First, the Ti barrier layer and Cu seed layer are sputtered on the PSPI layer in sequence. (b) Next, the photoresist is deposited and patterned to restrict the area for the RDLs. (c) Cu RDLs are then fabricated by electroplating. (d) After that, the photoresist is removed, and (e) another photoresist layer is deposited and patterned to protect the RDL area. (f) Finally, the exposed Cu seed layer and Ti barrier layer outside the RDL area are etched by wet etching and the photoresist is removed to complete the RDL fabrication.

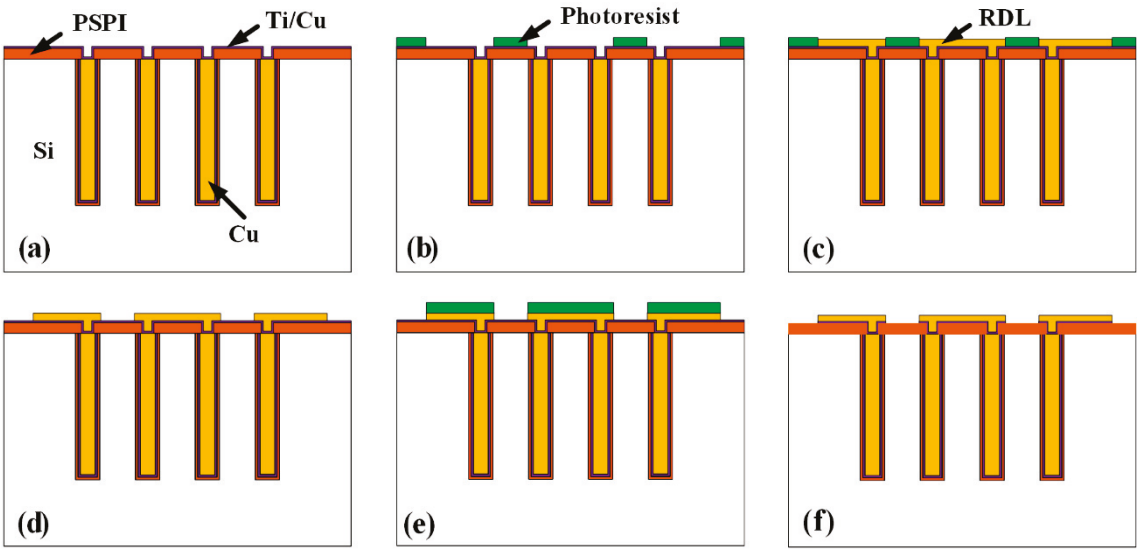


Figure 5. Schematic of the semi-additive process: (**a**) sputtering of barrier and seed layer, (**b**) patterning of RDL area, (**c**) RDL electroplating, (**d**) removal of photoresist, (**e**) patterning to protect RDL area, (**f**) wet etching of excess barrier and seed layer and removal of photoresist.

3. Fabrication

3.1. Deposition of PI Liner

First, blind vias with a diameter of 11 µm are etched by DRIE, as shown in Figure 6. The depth of the vias is about 126 µm, and the aspect ratio is as high as 11:1. Notably, the density of the blind vias is as large as 2000/mm^2.

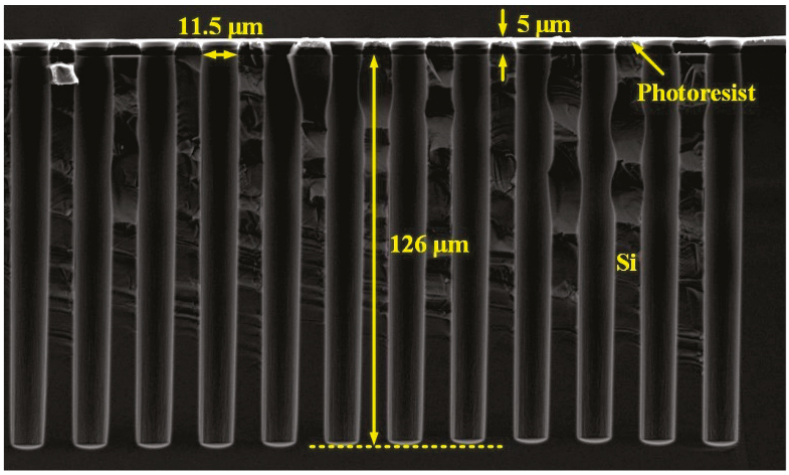


Figure 6. Cross sectional SEM image of the blind vias etched by DRIE.

The morphology of the PI liner deposited by the vacuum-assisted spin coating technique is affected by many factors, such as the spinning time and the spinning speed. In

order to explore the influence of these parameters on the deposition results, two groups of comparative experiments are carried out. In the first group, the spinning time of high-speed state is set to be 20 s, 40 s, and 60 s, individually, and the spinning speed is 2000 rpm. Figure 7a–c show the cross sectional SEM images of the fabricated PI liners with different spinning times. It is shown that as the spinning time increases from 20 s to 40 s, the thickness of the PI liner decreases for nearly all positions. Moreover, the uniformity of the PI liner from the top corner of the via to the near bottom is improved. This is because 20 s is too short for the PI on the via sidewall to reach a stable state between being spined out and remaining in situ. Therefore, with a longer spinning time, more PI is spined out especially for the positions where the PI layer is much thicker, and the liner becomes thinner and more conformal. However, as the driving forces such as centrifugal force, intermolecular force of PI, gravity of PI, and frictional force between PI and the via sidewall have already reach a balanced state for a spinning time of about 40 s, the PI thickness will not obviously decrease when the spinning time further increases to 60 s, as shown in Figure 7c. To evaluate the influence of the spinning speed, another PI liner is deposited with a spinning speed of 3000 rpm and a spinning time of 40 s, as shown in Figure 7d. Compared to Figure 7b, when the spinning speed increases from 2000 pm to 3000 rpm for 40 s, the PI thickness is reduced especially at the via middle as the centrifugal force is strengthened.

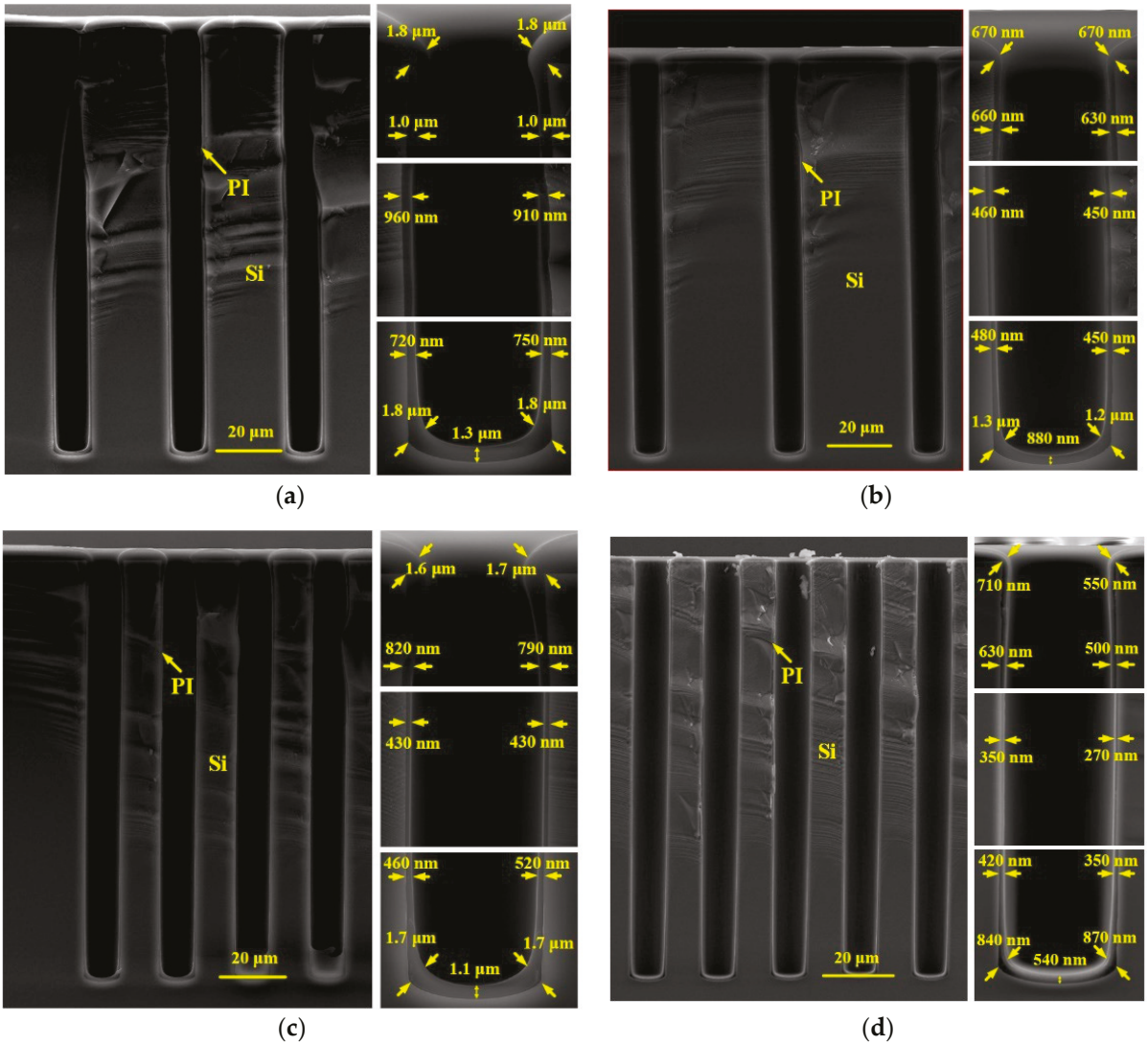


Figure 7. Cross sectional SEM images of PI liners deposited by vacuum-assisted spin coating technique: (**a**) 2000 rpm for 20 s, (**b**) 2000 rpm for 40 s, (**c**) 2000 rpm for 60 s, (**d**) 3000 rpm for 40 s.

In this paper, the spinning parameters of the high-speed state are set to be 2000 rpm for 40 s. Additionally, the viscosity of PI is about 4000 cP, the vacuuming time is 5 min, and the low-speed spinning state is 500 rpm for 12 s. In addition, the liner is cured at 240 °C for 4 h in N_2 ambient to fully polymerize the PI. As shown in Figure 7b, the PI liner is conformal, and the thickness is about 630–660 nm at the sidewall top, 450–460 nm at the sidewall middle, and 450–480 nm at the sidewall bottom, with a step coverage of above 15%. Moreover, the surface of PI is smooth without duplicating the sidewall scallops caused by Bosch etching. Considering that the PI layer on the top surface will be removed in further processes, the uniform and continuous PI layer at the via sidewall contributes to ensuring a good insulation characteristic of the final TSV. Notably, the highest process temperature in the vacuum-assisted spin coating technique is only 240 °C during the curing procedure, making it compatible with IC processes.

3.2. Deposition of Cu Seed Layer

Next, a uniform TiN barrier layer with a thickness of about 80 nm is deposited on the PI liner by ALD. Considering that the blind vias have a HAR of more than 10:1, neither conventional sputtering nor electroless plating can easily and effectively fabricate a continuous Cu seed layer in such HAR vias; therefore, a novel technique named sequential sputtering and electroless plating is used to fabricate a continuous Cu seed layers. First, sputtering is used to deposit 100 nm Cu as the pre-treatment for electroless plating. Then, electroless plating of Cu is performed to achieve a continuous seed layer inside the blind vias. Due to the limited capability of the sputtering machine (IMECAS, JS-3), a continuous Cu layer can only be realized within one-third of the depth of the blind vias, and there are only discrete Cu particles at the via middle and the via bottom after sputtering. Even so, the Cu particles are able to enhance the reaction efficiency of the upcoming electroless plating and guarantee the continuity of the seed layer especially at the via bottom [27].

During the electroless Cu step where Cu ions are reduced, the exchange rate of the solutes inside the blind vias is slow so that the growth rate of the seed layer at the via bottom is much slower than that at the via top. Moreover, the gas generated during the reduction will accumulate inside the blind vias and affect the transport of the reactants. Therefore, the electroless Cu plating will take a long time, and the deposited Cu seed layer will be thick at the via opening and thin at the via bottom without additional interference. In this work, an ultrasonic assistance is introduced to accelerate the transport of reactants, shorten the reaction time, and improve the step coverage of the Cu seed layers.

It should be noted that the seed layer is fragile at the beginning of the reaction, so there should be about 5 min before applying ultrasound assistance to protect the initial Cu layer. Additionally, the power, duration, and duty cycle of ultrasound will affect the morphology of the seed layer. In the case of low power or short duration, it is not enough to shatter the bubbles in the blind vias, and the transport of reactive substances is still limited. However, in the case of high power or long duration, it will affect the adhesion of Cu and even destroy the continuity of the seed layer. On the other hand, lower duty cycle and longer response time will bring in weaker ultrasonic intensity, which also means that the thickness of the seed layer at the field and openings will increase.

In this work, the ultrasonic power is 180 W, and it is turned on for 1 s per min. The total treatment time is 40 min. The thickness of the formed seed layer is about 500 nm at the via opening and about 40 nm at the via bottom, as shown in Figure 8. It can be seen that the Cu seed layer is continuous and dense, which can satisfy the requirements of electroplating. Cu electroplating is then conducted to fabricate central pillars, and the result is shown in Figure 9. It shows that the blind vias are fully filled by Cu with no obvious voids or seams, proving the quality of the fabricated seed layer.

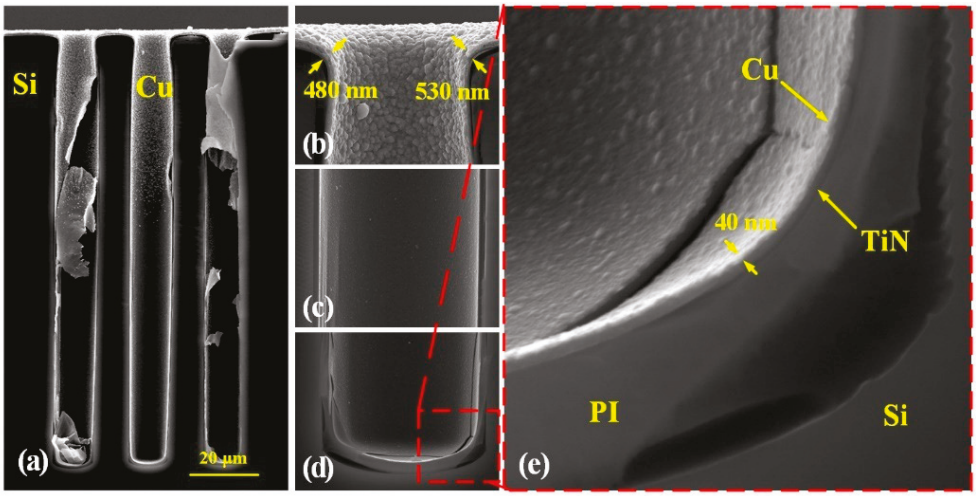


Figure 8. Cross sectional SEM images of fabricated Cu seed layer: (**a**) global view, (**b**) via top, (**c**) via middle, (**d**) via bottom, (**e**) enlarged view of via bottom.

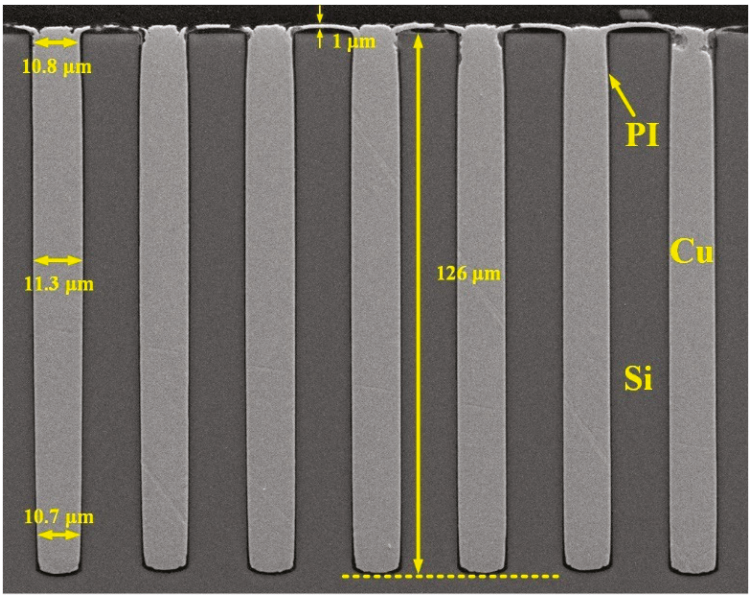
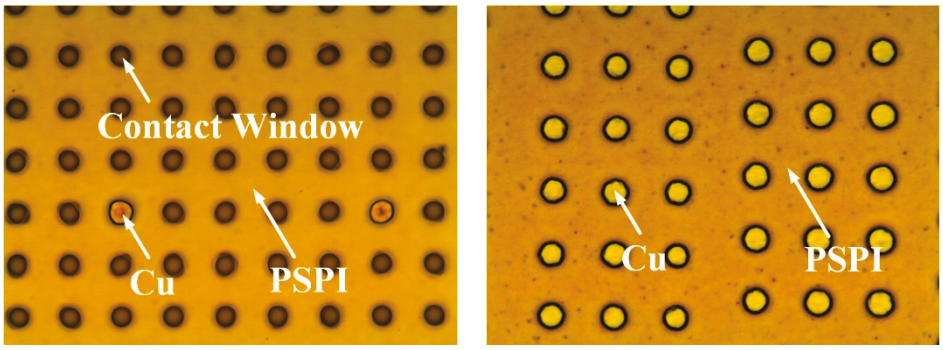


Figure 9. Cross sectional SEM image of blind TSVs after Cu electroplating.

3.3. Fabrication of PSPI Insulating Layer in Field Area

After the electroplating is completed, the Cu and PI in the field area are removed by CMP until the Si substrate is completely exposed. A PSPI layer is then coated and patterned as the surface insulating layer. As the patterning of PSPI is performed by lithography and development, there always leaves over a thin PSPI film of about 10 nm in the patterned window for the connection between the RDL and the Cu pillar, leading to the open circuit failure. Therefore, a two-step plasma bombardment process is proposed in this work to remove the residual PSPI film. First, O_2 plasma bombardment is used to clean the PSPI in the contact window, which results in the slight oxidation of the Cu pillar. Next, the Cu oxide layer is etched by Ar plasma bombardment. To verify the feasibility of the plasma bombardment process, two identical samples with PSPI layer on Cu layer are prepared. After development, one sample is treated by the proposed two-step plasma bombardment process and the two samples are then electroplated. The electroplating results are shown in Figure 10. It can be seen that only two contact windows of the sample without bombardment treatment are able to be plated, which is due to that most of the windows containing residual PSPI films. In contrast, all contact windows are successfully

plated after plasma bombardment, as shown in Figure 10b, indicating that the residual PSPI films are effectively removed. Therefore, the plasma bombardment process enables the formation of good electrical connections between RDLs and Cu pillars.



(**a**) (**b**)

Figure 10. Optical image of patterned contact windows on PSPI after electroplating: (**a**) without plasma bombardment, (**b**) with plasma bombardment.

After the fabrication of RDLs by the semi-additive process, the front side of the sample is bonded with a glass slide using BCB as the bonding glue. The back side of the sample is then thinned until about 10 µm away from the bottom of the blind vias. The remaining thickness is removed by CMP to reveal the Cu pillars, which can also reduce the surface roughness and mitigate the residual stress caused by thinning [30,31]. Note that there are no cracks on the exposed Cu pillars nor obvious wafer warpage after CMP. Finally, the back-side PSPI insulating layer and RDLs are also fabricated. The final fabrication result is shown in Figure 11. The TSVs are dense and intact with double-side RDLs, showing the feasibility of the proposed process flow.

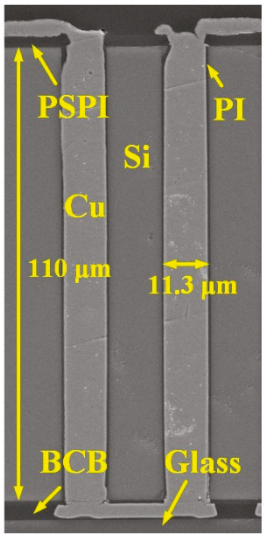
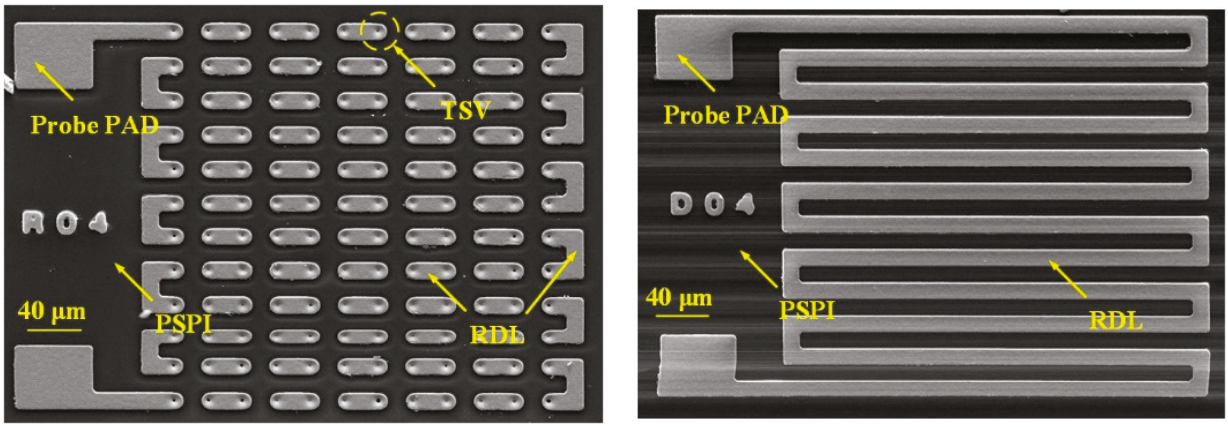


Figure 11. SEM image of fabricated TSVs with double-side RDLs.

4. Electrical Characterizations

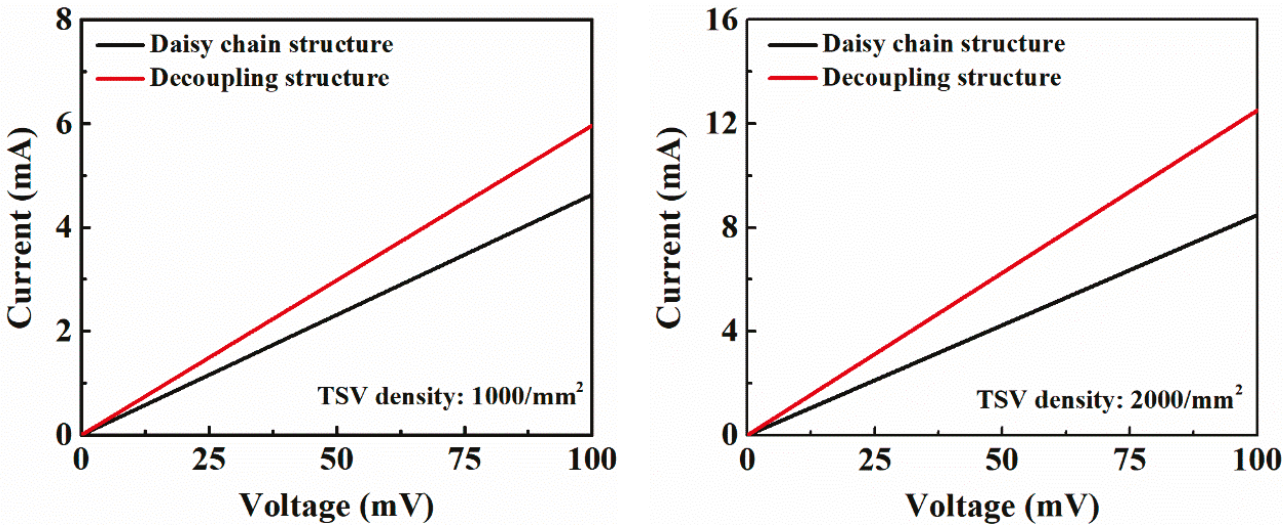
In this work, the DC resistance and S-parameters of the HAR PI-TSVs are tested. As shown in Figure 12, a daisy chain structure and its corresponding decoupling structure are designed to calculate the resistance of a single TSV. The daisy chain consists of 144 identical TSVs that are connected in series through RDLs. For each structure, the test voltage is applied to the probe pads by two test probes to measure its current–voltage (I–V) characteristic using Keysight B1500A. Then, the resistance of each structure is calculated according to the I–V curve. Furthermore, the resistance of a single TSV is obtained by subtracting

the resistance of the decoupling structure from that of the daisy chain structure, and then dividing by 144, which is the number of the TSVs in the daisy chain structure. The I–V characteristics of TSV daisy chains with distribution density of 1000/mm^2 and 2000/mm^2 and the corresponding decoupling structures are evaluated, as shown in Figure 13, and the resistances of a single TSV are calculated to be about 33 mΩ and 28 mΩ, respectively. Note that all the calculated resistances from more than ten groups of test structures for each TSV density fall within the 3σ range, where σ refers to the standard deviation, showing the good stability of the fabrication flow.



(**a**) (**b**)

Figure 12. SEM images of the test structures for the DC resistance of the PI-TSV: (**a**) daisy chain structure, (**b**) decoupling structure.



(**a**) (**b**)

Figure 13. Typical I–V curves of the daisy chain structures and the decoupling structures with: (**a**) TSV density of 1000/mm^2, (**b**) TSV density of 2000/mm^2.

To evaluate the RF performance of the PI-TSVs, the S-parameters of the TSVs are first simulated using an ANSYS High-Frequency Structure Simulator (HFSS), and the simulation structures are shown in Figure 14. First, the S-parameters of the four structures are simulated individually. Then, the S-parameters of a single TSV can be obtained by decoupling through the L-2L de-embedding method [32,33], where the S11 and the S21 at 40 GHz are −20.7 dB and −0.56 dB, respectively. The L-2L de-embedding structures are also fabricated and measured to obtain the actual S-parameters of the PI-TSV in this paper. Figure 15 plots the comparison between the simulated and measured S-parameters

of a single TSV. It can be seen that the trend of the tested S-parameters after de-embedding agrees with those of the simulated ones, except for that the former ones exhibit small fluctuations due to the intrinsic fluctuations of the RF test probes at high frequencies.

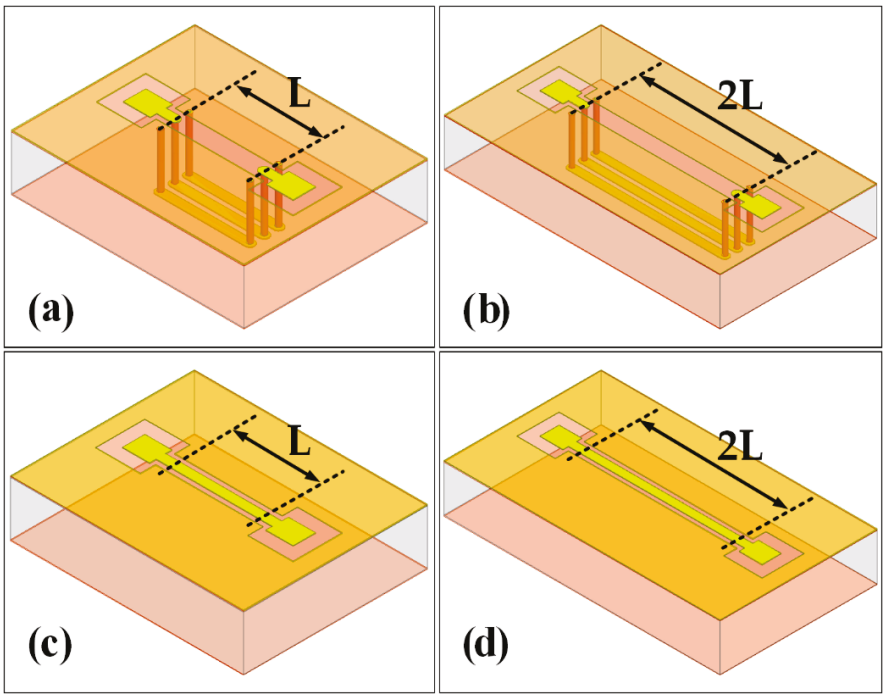


Figure 14. 3D models of the L-2L de-embedding structures. (**a**) TSVs and RDLs (L), (**b**) TSVs and RDLs (2L), (**c**) only RDLs (L), (**d**) only RDLs (2L).

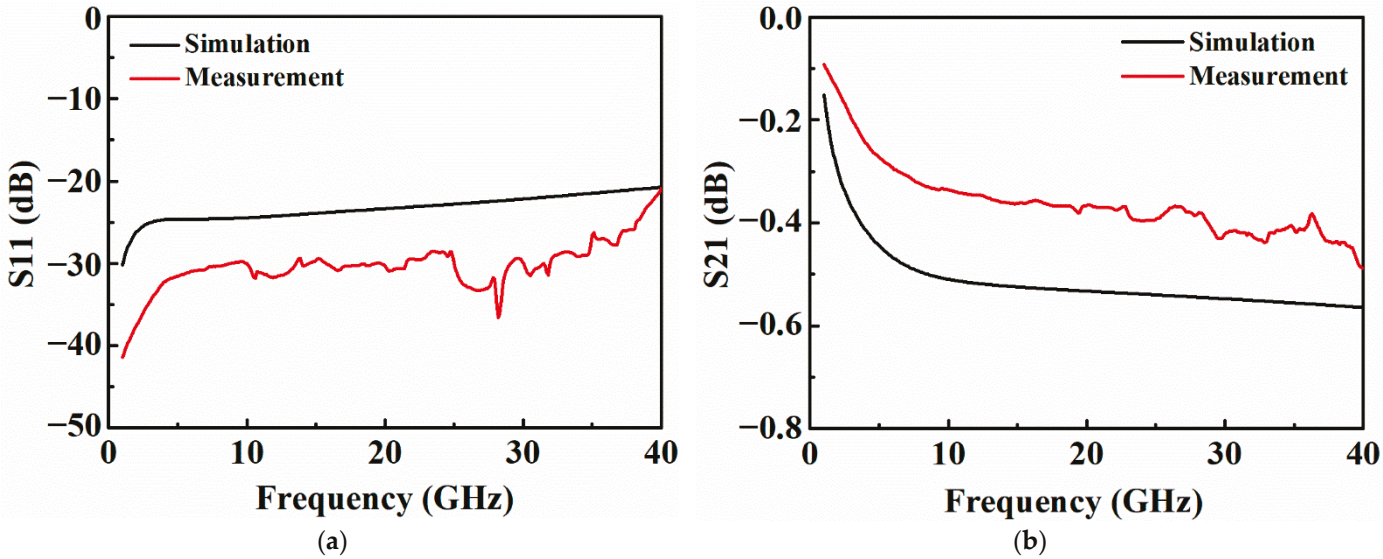


Figure 15. Comparison of the S-parameters of a single TSV between simulation and measurement: (**a**) return loss (S11), (**b**) insertion loss (S21).

5. Conclusions

In this paper, a low-cost and feasible process flow for HAR PI-TSVs is proposed. Conformal PI liner is deposited through a low-cost and low-temperature vacuum-assisted spin coating technique, and the influence of spinning time and speed is discussed. Additionally, a continuous and dense Cu seed layer is achieved by sequential sputtering and electroless plating with the assistance of ultrasound treatment, and then, void-free and seamless Cu

pillars are formed by electroplating. Moreover, PSPI is deposited as the insulating layer in the field area and a two-step plasma bombardment process is proposed to remove the residual PSPI in the contact windows, which improves the connection quality between Cu pillars and RDLs. Then, the RDLs are fabricated by the semi-additive process. HAR PI-TSVs with a diameter of 11 μm and depth of 110 μm are successfully fabricated with double-side RDLs, and the electrical performance, including DC resistance and S-parameters, is evaluated. The resistances of a single TSV in arrays with distribution density of 1000/mm^2 and 2000/mm^2 are measured to be about 33 mΩ and 28 mΩ, respectively. Additionally, the test results of the S-parameters of a single TSV are in good agreement with the simulation results. The proposed fabrication scheme and the electrical characterization of HAR PI-TSVs enrich the study on TSVs with polymer liners, and facilitate the application of HAR TSVs in the miniaturization of modern high-performance heterogeneous integration systems.

Author Contributions: Conceptualization, Z.C., L.X., Y.D. and Z.Z.; methodology, X.C., L.X. and Z.Z.; software, X.C. and Y.H.; validation, L.X. and Z.Z.; formal analysis, X.C., Z.C., L.X., Y.D. and Z.Z.; investigation, X.C., L.X., Y.H. and H.W.; resources, X.C., Z.C., L.X., Y.D. and Z.Z.; data curation, X.C., Y.H. and H.W.; writing—original draft preparation, X.C. and Z.Z.; writing—review and editing, X.C., Z.C., Y.D. and Z.Z.; visualization, X.C., L.X., Y.H. and Z.Z.; supervision, Z.C., Y.D. and Z.Z.; project administration, Z.C. and Y.D.; funding acquisition, Z.C. and Y.D. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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Thermoelectric Energy Micro Harvesters with Temperature Sensors Manufactured Utilizing the CMOS-MEMS Technique

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Abstract: This study develops a TEMH (thermoelectric energy micro harvester) chip utilizing a commercial 0.18 μm CMOS (complementary metal oxide semiconductor) process. The chip contains a TEMH and temperature sensors. The TEMH is established using a series of 54 thermocouples. The use of the temperature sensors monitors the temperature of the thermocouples. One temperature sensor is set near the cold part of the thermocouples, and the other is set near the hot part of the thermocouples. The performance of the TEMH relies on the TD (temperature difference) at the CHP (cold and hot parts) of the thermocouples. The more the TD at the CHP of the thermocouples increases, the higher the output voltage and output power of the TEMH become. To obtain a higher TD, the cold part of the thermocouples is designed as a suspended structure and is combined with cooling sheets to increase heat dissipation. The cooling sheet is constructed of a stack of aluminum layers and is mounted above the cold part of the thermocouple. A finite element method software, ANSYS, is utilized to compute the temperature distribution of the TEMH. The TEMH requires a post-process to obtain the suspended thermocouple structure. The post-process utilizes an RIE (reactive ion etch) to etch the two sacrificial materials, which are silicon dioxide and silicon substrate. The results reveal that the structure of the thermocouples is completely suspended and does not show any injury. The measured results reveal that the output voltage of the TEMH is 32.5 mV when the TD between the CHP of the thermocouples is 4 K. The TEMH has a voltage factor of 8.93 mV/mm^{2}K. When the TD between the CHP of the thermocouples is 4 K, the maximum output power of the TEMH is 4.67 nW. The TEMH has a power factor of 0.31 nW/mm^{2}K^2.

Keywords: thermoelectric energy micro harvester; complementary metal oxide semiconductor; microelectromechanical system; thermocouple; cooling sheet

1. Introduction

Thermoelectric energy micro harvesters (TEMHs) that are able to convert wasted heat into electric power are applied in various devices and systems [1], such as self-powered wireless devices [2], wearable devices [3], electronic devices [4], and health monitoring and tracking systems [5]. For instance, Leonov [6] developed a wearable electrocardiography system in which the power was supplied by 8 TEMHs. A wearable watch with a TEMH was presented by Torfs [7], where the TEMH was utilized to generate power from human body heat. Bavel [8] presented the used of TEMHs to supply a wireless electroencephalography headband for detecting brain signals.

Microelectromechanical system (MEMS) technology has employed microfabrication and micromachining to develop various micro-devices [9–12] and micro-transducers [13–17]. There were many thermoelectric energy micro harvesters made utilizing this technology. For instance, Su [18] developed a TEMH manufactured by utilizing the microfabrication and

bonding techniques. The TEMH was composed of p-type and n-type SiGe thermocouples, in which the total number of thermocouples was 1300. The hot part of the thermocouple was made on a silicon substrate, and the cold part of the thermocouple was made on another silicon substrate. Both the silicon substrates were bonded together using the bonding technique, and the thermocouples formed a cubic structure. The height of the legs for the thermocouple was 6 μm. The TEMH had an output voltage of 0.7 V when the TD (temperature difference) of the CHP (cold and hot parts) for the thermocouple was 50 °C. Peng [19] employed MEMS technology to develop a TEMH that contained eight thermoelectric cells. Each thermoelectric cell, designed in a circular shape, was composed of 25 thermocouples. The materials of the thermocouples were n-type polysilicon and p-type polysilicon. The measured results presented that the TEMH had an output voltage factor of 0.178 mV/mm^2K and a power factor of 1.47×10^{-3} pW/mm^2K^2. A TEMH with test structures, proposed by Zhang [20], was fabricated utilizing MEMS technology. In order to improve thermoelectric gathering and obtain a better performance, a metal heat sink was combined with the TEMH. The metal heat sink was put at the center of the TEMH. The output voltage factor and the power factor of the TEMH were 0.58 V/cm^2K and 2.76×10^{-2} $\mu W/cm^2k^2$, respectively. Noyan [21] proposed a TEMH which was fabricated utilizing silicon micromachining technology. The material of the thermocouples for the TEMH was SiGe nanowire that was deposited by a chemical vapor deposition on a micro-platform. The test results presented that the SiGe nanowire TEMH could harvest 7.1 $\mu W/cm^2$ at a waste heat temperature of 200 °C. Xie [22] utilized a CMOS process to fabricate a TEMH with a heat sink layer. The heat sink layer, made of aluminum and amorphous silicon, was deposited on the cold part of the TEMH, and it was able to enhance heat dissipation at the cold part of the TEMH. The thermocouples of the TEMH were constructed of n-type polysilicon and p-type polysilicon. The area of the TEMH was 1 cm^2. The measured results presented that the power factor of the TEMH was 0.052 $\mu W/cm^2K^2$. Yang [23] design an in-plane TEMH and made the TEMH using a CMOS process. The in-plane TEMH was established by thermocouples with n-type polysilicon and p-type polysilicon. To reduce electrical resistance and heat loss, the optimal dimensions of the thermocouple were analyzed. The legs of the thermocouple were 60 μm long and 2 μm wide. The area of the TEMH was 1.2×1.2 mm^2. The results showed that the power factor of the TEMH was 0.0473 $\mu W/cm^2K^2$, and its output voltage factor was 4.423 V/cm^2K. Sun [24] manufactured a micro-power generator that was a hybrid of a TEMH and a photoelectric generator utilizing a CMOS process. The thermocouples of the TEMH consisted of n-type polysilicon and p-type polysilicon legs, which had a length of 75 μm and a width of 20 μm. The test results showed that the output voltage factor of the TEMH was 0.316 V/cm^2K, and the power factor of the TEMH was 6.34×10^{-3} $\mu W/cm^2K^2$. The photoelectric generator had an efficiency of 4.11%. A flexible TEMH, presented by Glatz [25], was fabricated utilizing the photolithography and electrochemical deposition processes. The materials of the thermocouples for the TEMH were Ni and Cu, which were deposited on a flexible polymer substrate utilizing electroplating. The measured results presented that the power factor of the flexible TEMH was 0.83 $\mu W/cm^2K^2$. Huesgen [26] utilized a combination of bulk and surface micromachining processes to create a TEMH. The legs of the thermocouples for the TEMH were aluminum and n-type polysilicon. The hot part of thermocouples was fabricated as a suspended structure that could reduce the heat sink and increase thermoelectric gathering. The results showed that the TEMH had a power factor of 3.63×10^{-3} $\mu W/mm^2K^2$. Another flexible TEMH, developed by Glatz [27], was manufactured employing the electrochemical deposition process. The thermoelectric materials of the flexible TEMH were p-type and n-type Bi_2Te_3, which were electroplated on a polymer substrate. The test results presented that the power factor of the flexible TEMH was 0.29 $\mu W/cm^2K^2$. Wang [28] employed MEMS technology to create a TEMH. The thermoelectric materials for the TEMH were p-type and n-type Bi_2Te_3 nanowire arrays. The electrochemical deposition was utilized to coat a Bi_2Te_3 nanowire array on a porous alumina template. The TEMH was designed as a laminar structure. The p-type Bi_2Te_3 nanowire array had a Seebeck coefficient of 260 $\mu V/K$ and the n-type Bi_2Te_3 nanowire array had a Seebeck coefficient of -188 $\mu V/K$. Kao [29] proposed a TEMH made utilizing a commercial

CMOS process. The TEMH consisted of 24 thermocouples, which were made of n-type polysilicon and p-type polysilicon. The results showed that the power factor of the TEMH was 6.4×10^{-2} nW/cm^{2}K^2. Table 1 summarizes the performances of the TEMHs.

Table 1. Performances of THMEs.

Authors	Voltage Factor (mV/mm^{2}K)	Power Factor (nW/mm^{2}K^2)
Peng [19]	0.178	0.00147
Zhang [20]	5.8	0.276
Xie [22]	-	0.52
Yang [23]	44.23	0.473
Sun [24]	3.16	0.0634
Glatz [25]	-	8.3
Huesgen [26]	-	3.63
Glatz [27]	-	2.9
Kao [29]	-	0.00064

The CMOS process is usually utilized to manufacture IC (integrated circuit) components. Recently, this process has not only been used to fabricate IC, but also MEMS devices. The approach that uses the CMOS process to make MEMS devices is called the CMOS-MEMS technique [30–33]. There have been various micro-devices [34–36] developed by the technique. In this study, a TEMH with temperature sensors is designed and made utilizing the CMOS-MEMS technique. The temperature sensors are utilized to monitor the temperature of the CHP of the thermocouples. To enhance heat dissipation, the cold part of the thermocouples is designed as a suspended structure and combined with the cooling sheets. Micro-devices developed by the COMS-MEMS technique have the advantages of small volume, easy fabrication, and fast mass-production [37,38]. Compared to the MEMS technology, the CMOS-MEMS technique is easier to use in manufacturing micro-devices and achieving mass-production. These TEMHs [19–21,25–28] were fabricated using the MEMS technology. The fabrication of the TEMH in this work is easier than that of Peng [19], Zhang [20], Noyan [21], Glatz [25], Huesgen [26], Glatz [27], and Wang [28]. The power factor of the TEMH in this work exceeds that of Peng [19], Zhang [20], Sun [24], and Kao [29].

2. Design and Analysis of the Thermoelectric Energy Micro Harvester

Figure 1 shows the structure of the thermoelectric energy micro harvester with temperature sensors. The TEMH is designed based on the Seebeck effect. A series of 54 thermocouples is used to form the TEMH. Each thermocouple is constructed by matrial-1 and material-2 strips. Material-1 and material-2 are p-type polysilicon and n-type polysilicon, respectively. Thermocouples have a hot part and a cold part. The hot part of thermocouples is anchored on the silicon substrate, and the cold part of thermocouples is a suspended structure. In order to reduce the heat sink on the hot part of thermocouples, a thick silicon dioxide layer deposited on the hot part of the thermocouples because silicon dioxide is a low thermal conductivity material. To increase the heat sink on the cold part of the thermocouples, the cooling sheets are designed and set on the cold part of thermocouples. The working principle of the TEMH is that heat source inputs from the silicon substrate and conducts to the hot part of the thermocouples; then the heat source conducts to the cold part of the thermocouples and the cooling sheets. The heat source is dissipated by the cold part of thermocouples and the cooling sheets. When the thermocouples have a TD between the CHP, the TEMH generates an output voltage. To measure the temperature at the CHP of thermocouples in real time, the temperature sensors are designed and set near the cold parts and hot parts of the thermocouples. The TEMH area is 0.96 mm^2. Each thermocouple has a length of 180 μm, a thickness of 0.2 μm, and a width of 26 μm.

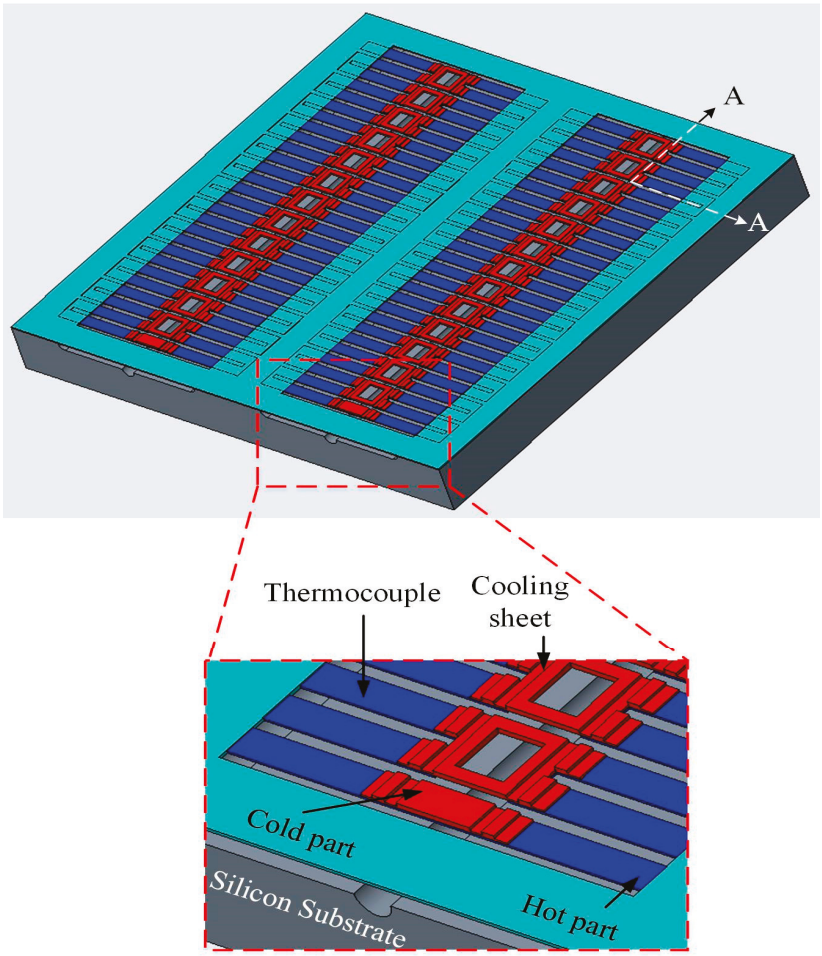


Figure 1. Structure for the TEMH (thermoelectric energy micro harvester).

The TD between the CHP of the thermocouples that deeply effect the output voltage and output power of the TEMH is an important factor for the TEMH. A finite element method software, ANSYS, is utilized to analyze the temperature distribution for the TEMH. First, it is necessary to construct the TEMH model according to the structure in Figure 1. The hot part of the thermocouples is located on the silicon substrate, and the cold part of the thermocouples is a suspended structure. Then, the TEMH model is meshed, and the triangular element is used to analyze the TEMH. There are about 45,000 elements generated. The boundary condition is that the hot part of the thermocouple is fixed. The material properties of the TEMH must be inputted into the ANSYS software. In the TEMH, the materials include silicon, aluminum, polysilicon, and silicon dioxide. Table 2 lists the thermal conductivity of the materials. The thermal conductivity of silicon is 150 W/m·K, and the thermal conductivity of aluminum is 236 W/m·K. The thermal conductivity of polysilicon is 31.5 W/m·K, and the thermal conductivity of silicon dioxide is 1.42 W/m·K. The thermal conductivity of these material is inputted into the ANSYS. The thermal flux is 30 pW/μm^2K, which value is inputted into the ANSYS. Finally, the software carries out the computation for the temperature distribution of the TEMH. The computation of temperature distribution for the TEMH using the ANSYS is shown in Figure 2. The results present that the maximum temperature occurring at the hot part of the thermocouples is 36.587 °C, and the minimum temperature occurring at the cold part of the thermocouples is 32.747 °C. The CHP of the thermocouples have a TD of about 4 °C.

Table 2. Thermal conductivity of materials.

Material	Silicon	Aluminum	Polysilicon	Silicon Dioxide
Thermal conductivity (W/m·K)	150	236	31.5	1.42

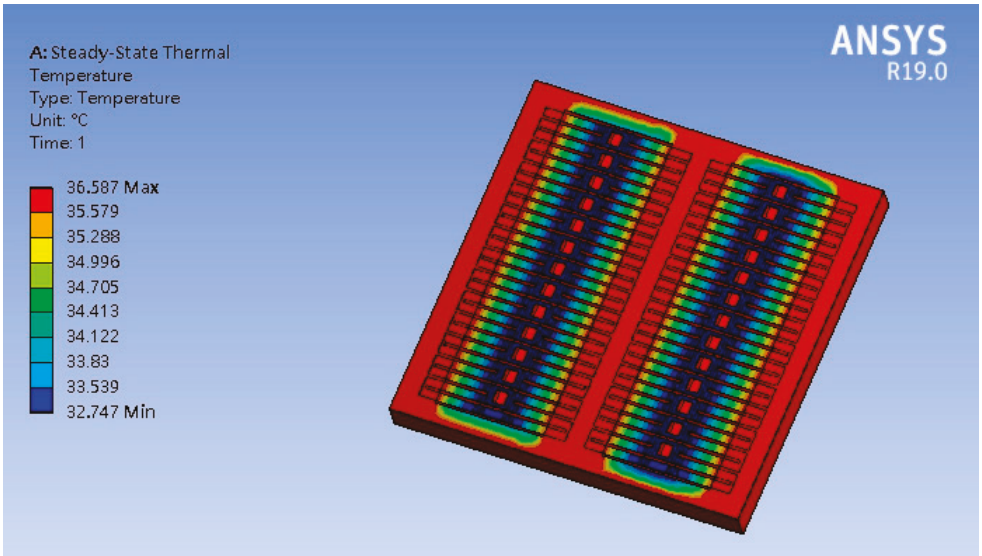


Figure 2. Computation of temperature distribution for the TEMH using the ANSYS.

The thermoelectric energy micro harvester produces an output voltage, as it has a TD between the CHP of the thermocouples. The output voltage of the TEMH is given by [39],

$$V_o = m(\beta_1 - \beta_2)(T_{ht} - T_{cd}) \quad (1)$$

where m is thermocouple number, β_1 is the Seebeck coefficient of material-1, β_2 is the Seebeck coefficient of material-2, T_{ht} is the hot part temperature of the thermocouple, and T_{cd} is the cold part temperature of the thermocouple. According to Equation (1), the output voltage of the TEMH relies on the thermocouple number, TD ($T_{ht} - T_{cd}$), and the Seebeck coefficient difference ($\beta_1 - \beta_2$). Increasing the thermocouple number could enhance the output voltage of the TEMH. The TD of the CHP of the thermocouple is proportional to the output voltage of the TEMH, so enhancing the TD could increase the TEMH output voltage. The Seebeck coefficient of the thermocouple materials is an important parameter. If both materials in the thermocouple show a large difference in the Seebeck coefficient, then the TEMH has a high output voltage. The Seebeck coefficient difference of thermocouples for the TEMH is 161 μV/K [23]. The value is substituted into Equation (1) to compute the output voltage for the TEMH. Figure 3 shows the output voltage for the TEMH under different TD. The results showed that the output voltage for the TEMH enhances as the temperature difference increases, and the output voltage for the TEMH is proportional to the TD between the CHP of the thermocouples. As shown in Figure 2, the output voltage for the TEMH changes from 8.7 mV at a TD of 1 K to 34.8 mV at a TD of 4 K. The evaluation of the output voltage factor for the TEMH is 9.4 mV/mm^{2}K.

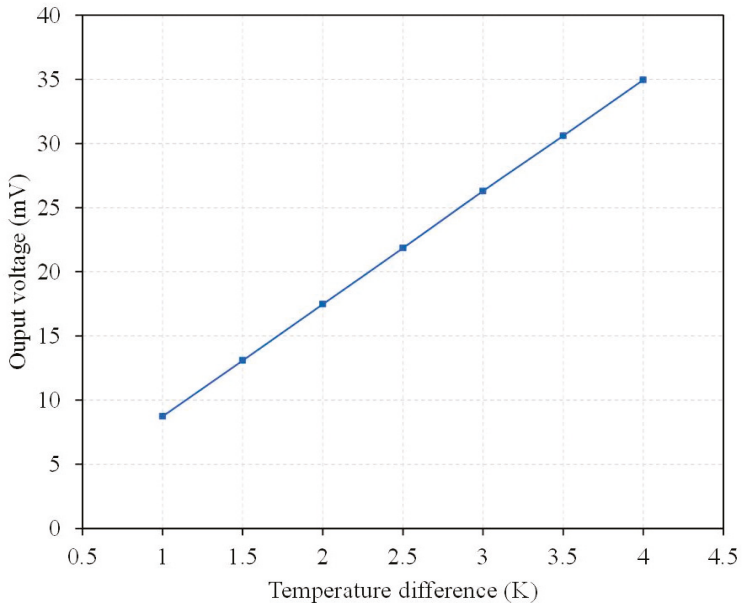


Figure 3. Evaluation of the output voltage for the TEMH.

When the thermoelectric energy micro harvester connects with an external load resistance, the output power of the TEMH can be obtained. Suppose that the external load is equal to the internal resistance of the TEMH, then the maximum output power of the TEMH can be expressed as [40],

$$P_{max} = \frac{V_o^2}{4R_i} \tag{2}$$

where V_o represents the output voltage of the TEMH and R_i is the internal resistance of the TEMH. According to Equation (2), the maximum output power of the TEMH relies on the output voltage and internal resistance of the TEMH. The greater the output voltage produced by the TEMH, the higher the maximum output power generated by the TEMH. Reducing the internal resistance of the TEMH could increase the maximum output power of the TEMH. To enhance the maximum output power of the TEMH, we design a low internal resistance for the thermoelectric energy micro harvester. The internal resistance of the thermoelectric energy micro harvester can be expressed as [25],

$$R_i = \left(\frac{\rho_1 l_1}{w_1 t_1} + \frac{\rho_2 l_2}{w_2 t_2} \right) \tag{3}$$

where ρ_1 is the resistivity of material-1 for the thermocouple, l_1 is the length of material-1 for the thermocouple, t_1 is the thickness of material-1 for the thermocouple, w_1 is the width of material-1 for the thermocouple, ρ_2 is the resistivity of material-2 for the thermocouple, l_2 is the length of material-2 for the thermocouple, t_2 is the thickness of material-2 for the thermocouple, and w_2 is the width of material-2 for the thermocouple. In Equation (3), the first team ($\rho_1 l_1 / w_1 t_1$) means the resistance of material-1 and the second team ($\rho_2 l_2 / w_2 t_2$) means the resistance of material-2. The internal resistance of the TEMH relies on the resistivity, length, width, and thickness of material-1 and material-2 for the thermocouples. The more the resistivity of material-1 and material-2 for the thermocouple increases, the higher the internal resistance of the TEMH becomes. As the length of material-1 and material-2 for the thermocouple increases, then the internal resistance of the TEMH increases. Oppositely, as the thickness and width of material-1 and material-2 for the thermocouple reduce, the internal resistance of the TEMH increases. In the design for the thermoelectric energy micro harvester, there are 54 thermocouples. The dimensions of each thermocouple are explained as follows: the length of material-1 is 180 μm; the length of material-2 is 180 μm; the width of material-1 is 26 μm; the width of material-2 is 26 μm; the thickness of material-2 is

0.2 μm; and the thickness of material-2 is 0.2 μm. The number and dimensions of the thermocouples are substituted into Equation (3). The internal resistance of the TEMH is obtained, and the value is 56.5 kΩ. To analyze the maximum output power of the TEMH, Equation (2) is employed to evaluate the TEMH maximum output power. The output voltage of the TEMH in Figure 3 and the internal resistance of 56.5 kΩ are substituted into Equation (2). The maximum output power of the TEMH is obtained. The evaluation of the maximum output power for the thermoelectric energy micro harvester is shown in Figure 4. The results show that the maximum output power of the TEMH increases as the TD between the CHP for the thermocouple increases. The maximum output power for the TEMH is 0.34 nW at a TD of 1 K. When the TD increases to 4 K, the maximum output power becomes 5.41 nW. The evaluation of the power factor for the TEMH is 0.36 nW/mm^{2}K^2.

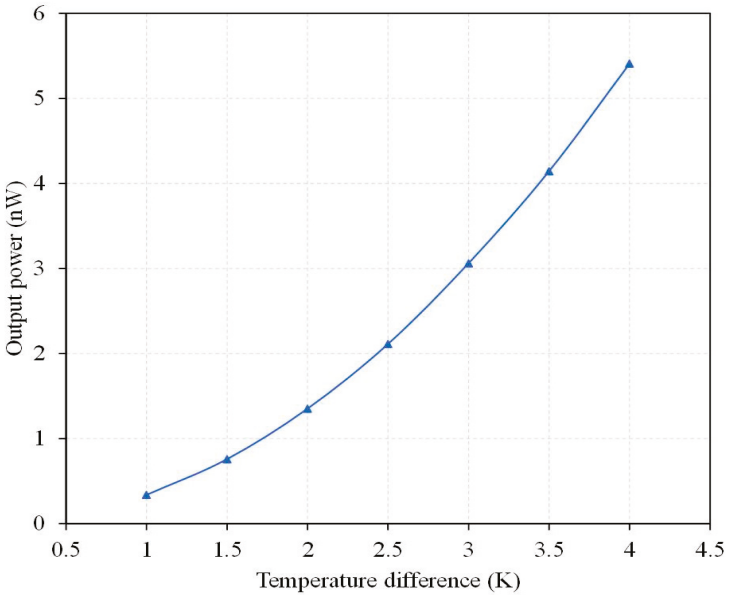


Figure 4. Evaluation of the maximum output power for the TEMH.

To monitor the temperature of the CHP for the thermocouples, the temperature sensors are designed. The temperature sensors are placed near the CHP for the thermocouples. The temperature sensors are the thermoresistive type. Polysilicon is used as the material for the temperature sensors because polysilicon has an excellent thermoresistive property. All the temperature sensors are made of a polysilicon strip and have the same dimensions, with a length of 1300 μm and a width of 0.95 μm. The initial resistance for the temperature sensor can be expressed as [41],

$$R_0 = R_{st}\frac{L_{st}}{W_{st}} \tag{4}$$

where R_{st} is the sheet resistance for the temperature sensor, L_{st} is the length for the temperature sensor, and W_{st} is the width for the temperature sensor. According to Equation (4), the initial resistance of the temperature relies on the sheet resistance, length, and width of the polysilicon strip. The more the sheet resistance and length of the polysilicon strip increase, the higher the initial resistance of the temperature sensor becomes. The polysilicon sheet resistance for the temperature sensors is 8.3 Ω/sq [42] at room temperature. The sheet resistance of 8.3 Ω/sq, the length of 1300 μm, and the width of 0.95 μm are substituted into Equation (4). The initial resistance for the temperature sensor is obtained, and the value is 11.36 kΩ. The resistance change of the temperature sensor is given by [41],

$$R_s = R_0[1 + \alpha_{TCR}(T_s - T_i)] \tag{5}$$

where R_0 is the initial resistance for the temperature sensor, α_{TCR} is the TCR (temperature coefficient of resistor) for the temperature sensor, T_s is the temperature change, and T_i

is the initial temperature for the temperature sensor. According to Equation (5), the resistance change of the temperature sensor relies on the temperature change, initial resistance, and TCR for the temperature sensor. The more the temperature increases, the higher the resistance of the temperature increases. The TCR of the temperature sensor is 1500 ppm/°C [23,42]. The TCR of 1500 ppm/°C and the initial resistance of 11.36 kΩ are substituted into Equation (5). The resistance change for the temperature sensor is obtained. The evaluation of the resistance change for the temperature sensor is shown in Figure 5. The results show that the resistance of the temperature sensor at room temperature is 11.36 kΩ. When the temperature increases to 373 K, the resistance of the temperature sensor becomes 12.72 kΩ.

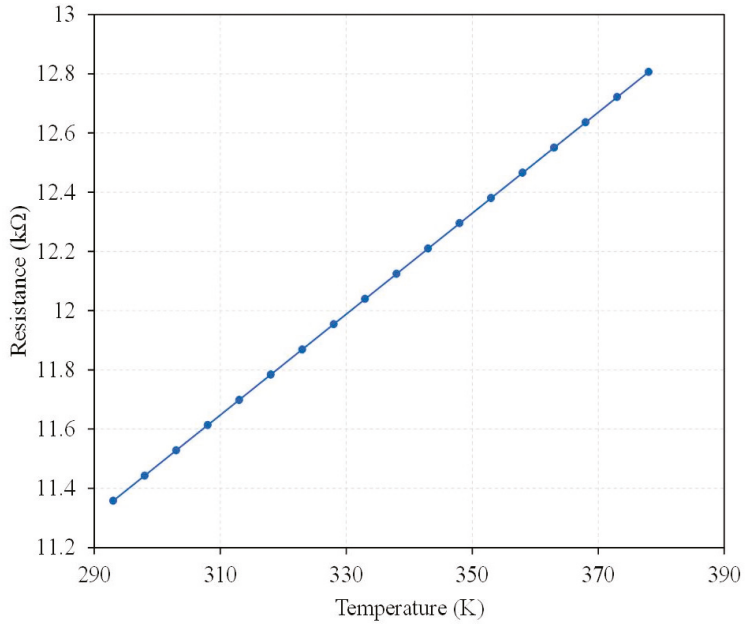


Figure 5. Evaluation of resistance change for the temperature sensor.

3. Fabrication of the Thermoelectric Energy Micro Harvester

The thermoelectric energy micro harvester was manufactured utilizing the TSMC (Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan) 0.18 μm CMOS (complementary metal oxide semiconductor) process. In addition to the CMOS process, the TEMH required a post-process because the TEMH required a suspended thermocouple structure. The 0.18 μm CMOS process contains one polysilicon layer and six metal layers. The material of the metal layers is aluminum. The thermocouples in the TEMH consist of n-type and p-type polysilicon layers. The hot part of the thermocouple is fixed on the silicon substrate. The cold part of the thermocouple is a suspended structure with cooling sheets. The cooling sheets are made up of a stacked structure that is composed of six metal layers, and the cooling sheets are used to enhance the heat dissipation. An integrated circuit software, Cadence, was employed to design the layout of the TEMH. According to the structure in Figure 1, the layout of the TEMH was established; then, TSMC carried out the fabrication of the TEMH using the CMOS process using this layout.

Figures 6–8 illustrate the process flow of the TEMH. Figure 6 presents a cross section of the TEMH along the AA line (Figure 1) after the CMOS process. As shown in Figure 6, the TEMH chip contained the thermocouples and temperature sensors. The temperature sensor was made of polysilicon in the CMOS process. To enhance the TD of the CHP for the thermocouples, the thermocouples must be made as a suspended structure. A post-process was utilized to etch the sacrificial materials to obtain the suspended thermocouple structure. In the TEMH, there are two sacrificial materials. One is silicon dioxide, and the other is silicon substrate. Figure 7 presents a cross section of the TEMH after the etching of the silicon oxide layer. The sacrificial silicon oxide is positioned between the polysilicon

strips of the thermocouples. In the post-process, an RIE (reactive ion etch) was utilized to etch the sacrificial silicon oxide until the silicon substrate was exposed. The source of CF_4/O_2 was supplied into the RIE to etch the silicon oxide. The etching conditions were RF power 150 W, pressure 20 mTorr, gas flow CF_4 20 sccm, with O_2 1 sccm. Figure 8 presents a cross section of the TEMH after etching of the silicon substrate. The sacrificial silicon substrate is positioned under the cold part of the thermocouple. In the post-process, an RIE was employed to remove the sacrificial silicon substrate until the cold part of the thermocouples was suspended. The source of SF_6/O_2 was supplied into the RIE to etch the silicon substrate. The etching conditions were RF power 350 W, pressure 15 mTorr, gas flow SF_6 28 sccm, with O_2 4 sccm. As shown in Figure 8, the RIE SF_6/O_2 etched silicon was an isotropic etching.

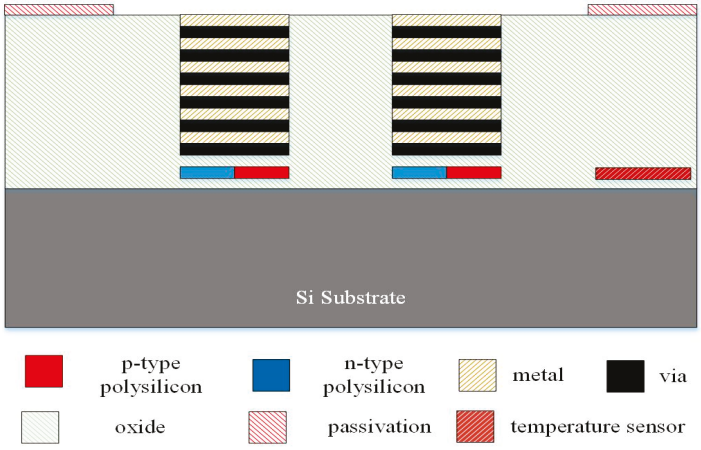


Figure 6. Cross section of the TEMH after the CMOS process.

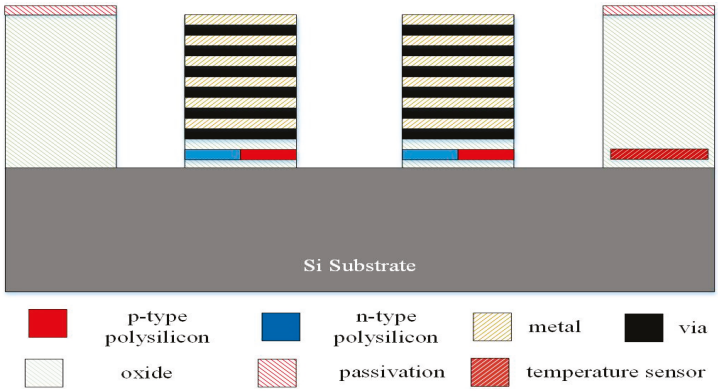


Figure 7. Cross section of the TEMH after etching of the silicon oxide layer.

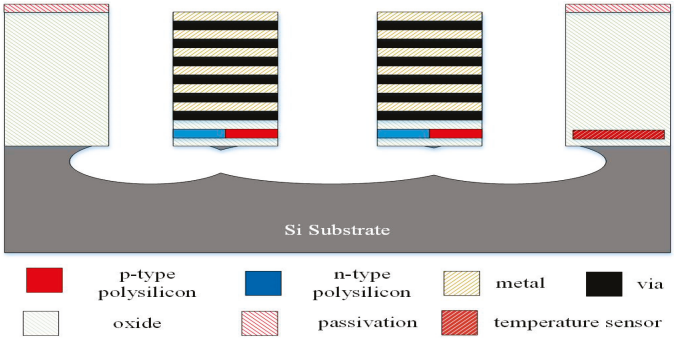


Figure 8. Cross section of the TEMH after etching of the silicon substrate.

An SEM (scanning electron microscope, NCHU, Taichung, Taiwan) was employed to measure the profile and structure of the TEMH. Figure 9 shows the profile of the TEMH taken by the SEM. As shown in Figure 9, the structure of the TEMH is complete, and the structure of thermocouples and the gap between the thermocouples can be clearly viewed. Figure 10 demonstrates the view of the TEMH taken by an optical microscope. As shown in Figure 10, the temperature sensors are respectively set near by the CHP of the thermocouples. Figure 11 shows a partial image of the TEMH taken by an optical microscope. As shown in Figure 11, the brown color in the picture shows the polysilicon strips of the thermocouples, which are regular and repeated structures.

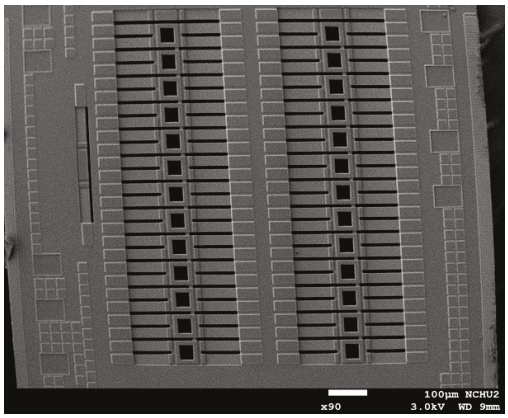


Figure 9. TEMH image taken by SEM.

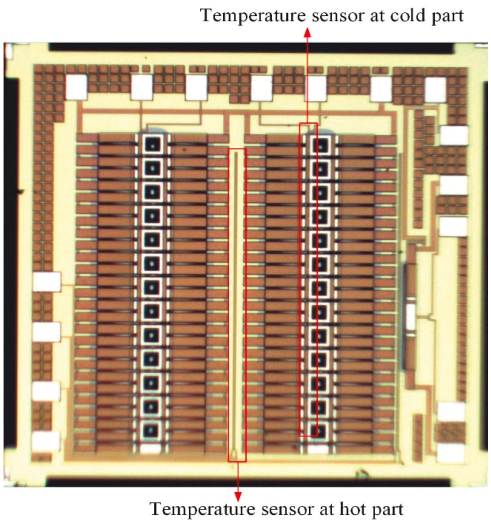


Figure 10. The TEMH taken by optical microscope.

To determine if the cold part of the thermocouple was suspended, the cross-sectional structure of the TEMH was measured utilizing the SEM. Figure 12 shows cross-sectional image of the TEMH taken by the SEM. As shown in Figure 12, the cold part of the thermocouple is suspended, and it has a large cavity under the thermocouple. This means that the sacrificial silicon substrate is completely removed through the post-process, and the thermocouples have not incurred any damage during the post-process. To enhance heat dissipation, the cooling sheets were designed and mounted on the cold part of the thermocouples. A cooling sheet was measured utilizing the SEM to observe its structure. Figure 13 shows a cross-sectional image of a cooling sheet taken by the SEM. As shown in Figure 13, the cross-sectional structure of the cooling sheet, which is composed of metal-1 to metal-6, is clearly visible.

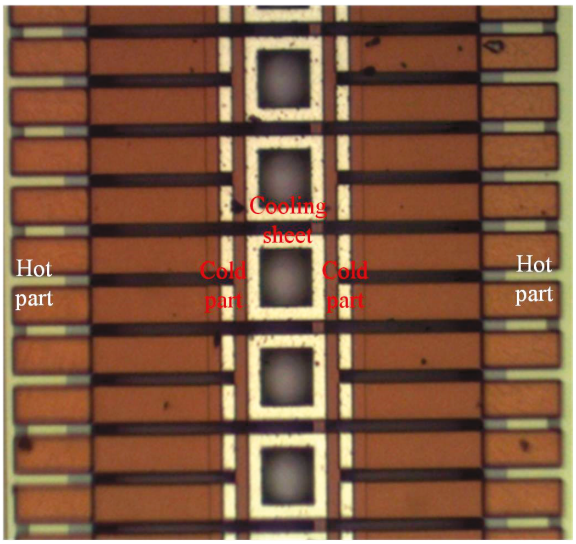


Figure 11. A partial image of the TEMH taken by an optical microscope.

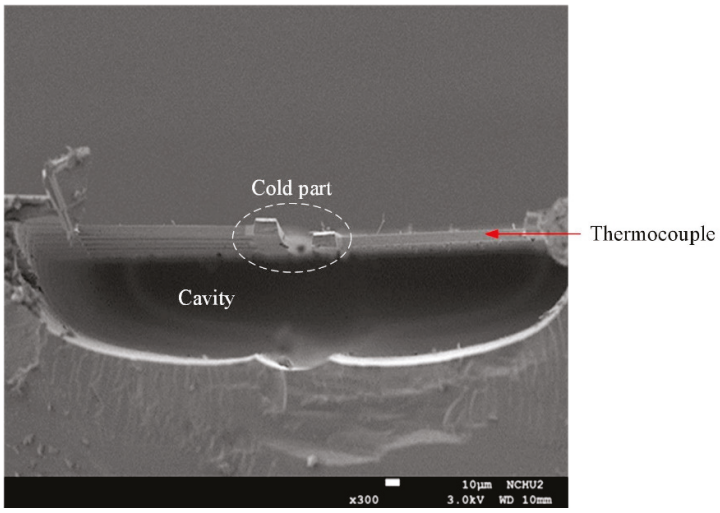


Figure 12. Cross-sectional image of the TEMH taken by SEM.

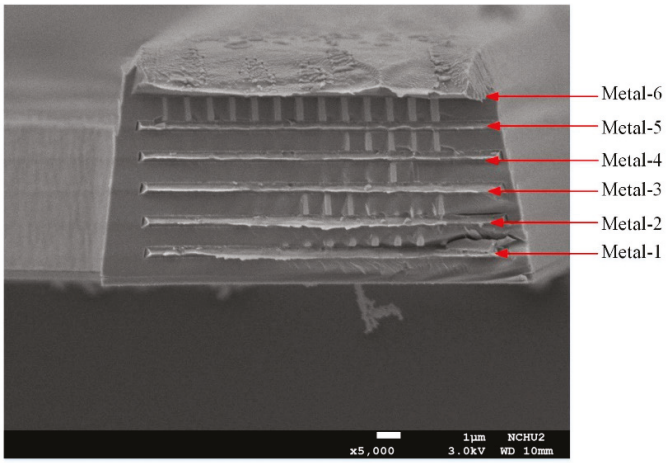


Figure 13. A cooling sheet image taken by SEM.

Finally, the performance of the TEMH must be tested. Before testing, the TEMH chip must be wire bonded. Figure 14 shows an image of wire bonding for the TEMH chip. The TEMH was mounted on a PCB (printed circuit board), and a wire bonder was utilized to connect the pads of the TEMH chip to the PCB.

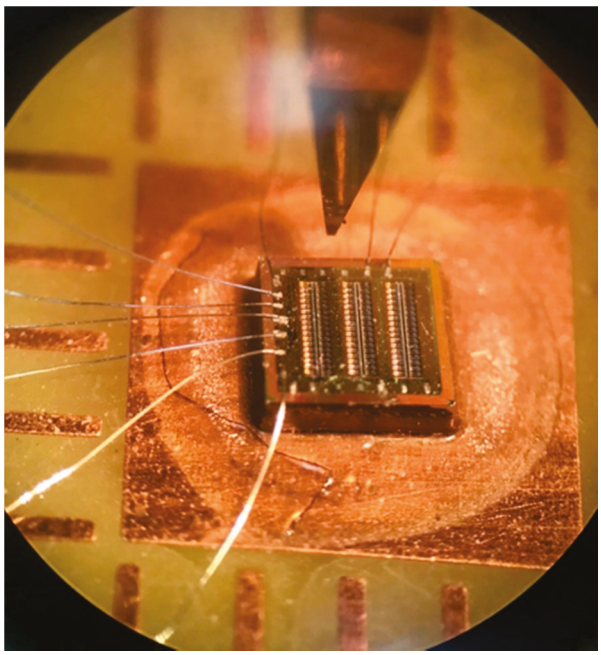


Figure 14. Wire bonding for the TEMH.

4. Results

There were two kinds of temperature sensors in the thermoelectric energy micro harvester. One was mounted near the hot part of the thermocouples, and the other was mounted near the cold part of thermocouples. The temperature sensors could monitor the temperature for the CHP of the thermocouples in real time. To characterize the performance of the temperature sensors, a heat chamber was utilized to test the temperature sensors. The heat chamber could generate a heat source and provide a testing temperature to the temperature sensors. First, the TEMH chip was mounted in the heat chamber. Then, the output signal ports of the temperature sensors were connected to a digital multimeter, which was utilized to measure the output for the temperature sensors. When the heat chamber supplied a testing temperature to the temperature sensors, the sensor produced a change in resistance. The resistance of the temperature sensors was measured utilizing the digital multimeter. Figure 15 shows the measurement of resistance for the temperature sensors under various temperatures. As shown in Figure 15, the resistance change of the temperature sensor at the hot part of the thermocouples is linear, and the slope of the curve is 0.017 kΩ/K. The resistance change of the temperature sensor at the cold part of the thermocouples is also linear, and the slope of the curve is 0.017 kΩ/K. The two kinds of temperature sensors used a linear output and had the same slope of curve.

To understand the actual performance of the thermoelectric energy micro harvester, a set of experimental devices were established for testing the TEMH. Figure 16 shows the experiment setup for testing the actual performance of the TEMH. The experiment needed to have a controller, a heater, a fan, and digital multimeters. The controller employed to control the heater and the fan could tune the heating of the heater and the speed of the fan. The heater provided the heat source, and the fan supplied the cooling source required by the TEMH. The digital multimeters were utilized to detect the resistance of the temperature sensors and the output voltage of the TEMH. First, the TEMH chip was mounted in the experimental device, as shown in Figure 16. Then, the output ports of the temperature sensors and the TEMH were connected to the digital multimeters. When

the heat source of the heater conducted to the TEMH and the CHP of the thermocouples obtained a TD, the TEMH generated an output voltage that was recorded by utilizing the digital multimeter. The temperature at the CHP of the thermocouples was monitored by utilizing the temperature sensors.

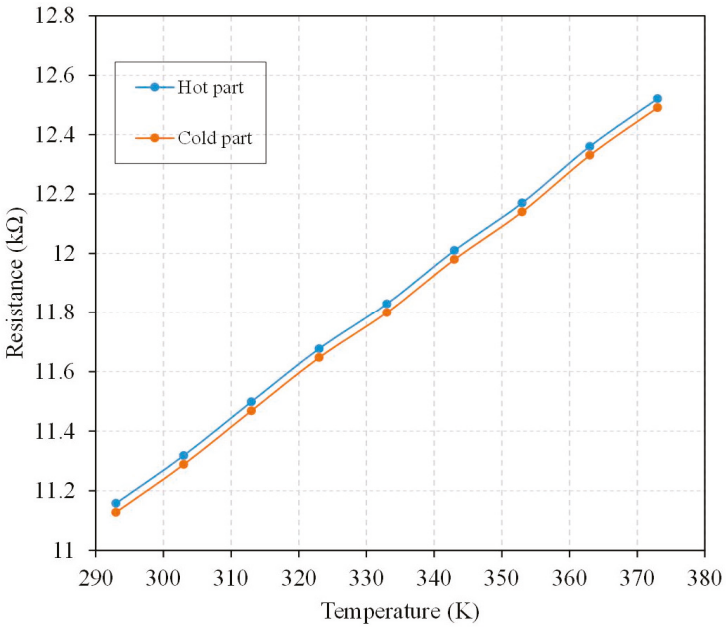


Figure 15. Measurement of resistance for the temperature sensors under various temperatures.

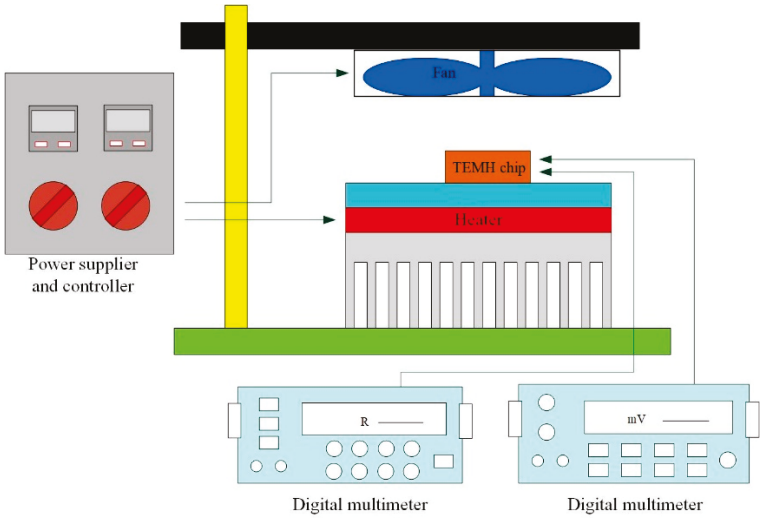


Figure 16. Measurement setup for the TEMH.

The output voltage of the TEMH was measured. Figure 17 shows the measured results of output voltage for the TEMH. The results revealed that the TEMH had an output voltage of 8.2 mV, as the TD was 1.1 K. When the TD increased to 4 K, the output voltage became 32.5 mV. The slope of the curve in Figure 17 was 8.57 mV/K, so the output voltage factor of the TEMH was 8.93 mV/mm^{2}K. Compared to the simulated results, the measured output voltage factor for the TEMH had an error percentage of 5%.

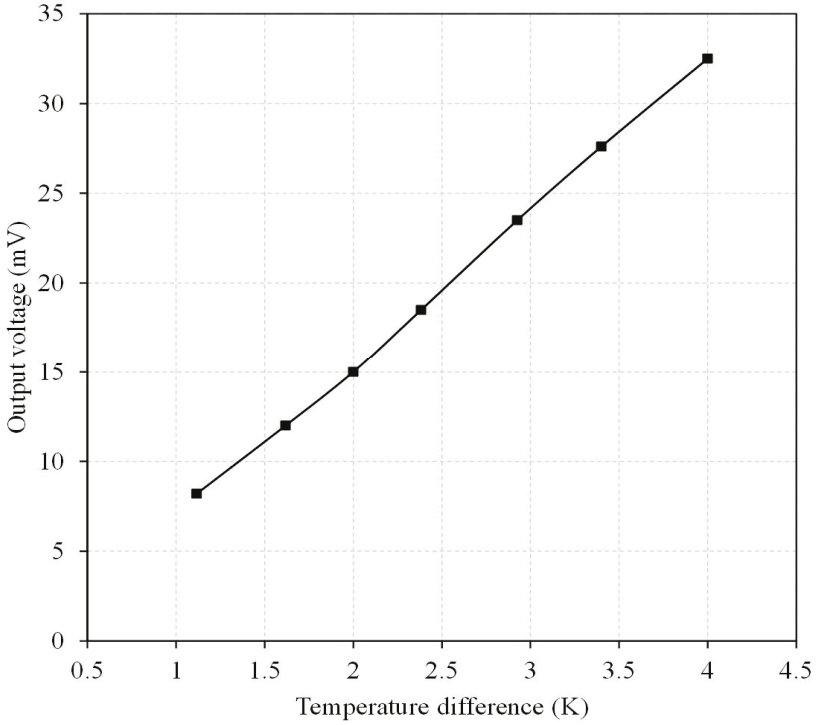


Figure 17. Measured results of output voltage for the TEMH.

According to the measurement results, the thermoelectric energy micro harvester had an internal resistance of 56.5 kΩ. The output power of the TEMH could be obtained through Equation (2). The measured output voltage in Figure 17 and the internal resistance of 56.5 kΩ were substituted into Equation (2). The maximum output power of the TEMH was obtained. Figure 18 presents the measured results of maximum output power for the microgenerator. The results revealed that the TEMH had a maximum output power of 0.3 nW, as the TD was 1.1 K. When the TD increased to 4 K, the maximum output power became 4.72 nW. The area of the TEMH was 0.96 mm^2. The measured power factor of the TEMH was 0.31 nW/mm^2K^2. The evaluated power factor for the TEMH was 0.36 nW/mm^2K^2. Compared to the evaluated power factor, the measured power factor for the TEMH had an error percentage of 13%. This is due to that was the variation of the thermoelectric coefficient for the thermocouples which resulted from the doping process, creating an error in the output voltage factor and the power factor of the TEMH.

Peng [19] developed a TEMH that had an output voltage factor of 0.178 mV/mm^2K and a power factor of 1.47×10^{-3} pW/mm^2K^2. A TEMH presented by Zhang [20] had an output voltage factor of 0.58 V/cm^2K and a power factor of 2.76×10^{-2} $\mu W/cm^2k^2$. Xie [22] fabricated a TEMH with the power factor of 0.052 $\mu W/cm^2K^2$. Yang [23] proposed an in-plane TEMH in which the output voltage factor and power factors were 4.423 V/cm^2K and 0.0473 $\mu W/cm^2K^2$, respectively. Sun [24] manufactured a hybrid TEMH. The output voltage factor of the TEMH was 0.316 V/cm^2K and the power factor of the TEMH was 6.34×10^{-3} $\mu W/cm^2K^2$. A flexible TEMH, developed by Glatz [25], had a power factor of 0.83 $\mu W/cm^2K^2$. Huesgen [26] made a TEMH with a power factor of 3.63×10^{-3} $\mu W/mm^2K^2$. A flexible TEMH, fabricated by Glatz [27], had a power factor of 0.29 $\mu W/cm^2K^2$. Kao [29] presented a TEMH with a power factor of 6.4×10^{-2} nW/cm^2K^2. In this work, the output voltage factor and power factor of the TEMH were 8.93 mV/mm^2K and 0.31 nW/mm^2K^2, respectively. Compared to the TEMHs of Peng [19], Zhang [20], Xie [22], Yang [23], Sun [24], Huesgen [26], Glatz [27], and Kao [29], the power factor of the TEMH in this work exceeded that of Peng [19], Zhang [20], Sun [24], and Kao [29].

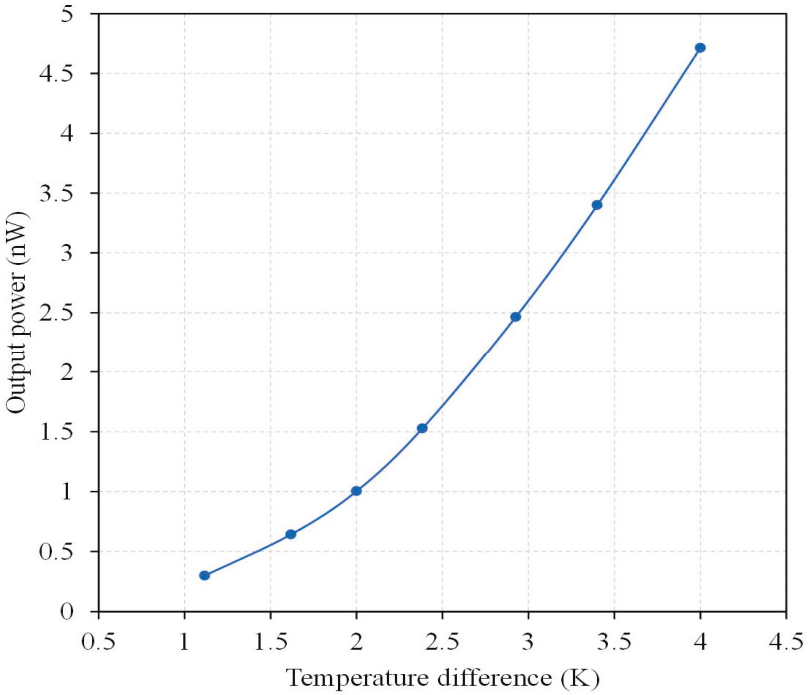


Figure 18. Measured results of maximum output power for the TEMH.

5. Conclusions

The thermoelectric energy micro harvester was successfully manufactured employing the commercial CMOS process. The TEMH was constructed using a series of 54 thermocouples. The hot part of the thermocouple was fixed on the silicon substrate. The heat source conducted heat to the thermocouple through the silicon substrate. The more the TD at the CHP of the thermocouples increased, the higher the output voltage and output power of the TEMH became. To obtain a higher output voltage and output power of the TEMH, the cold part of the thermocouples was fabricated as a suspended structure and combined with cooling sheets. The cooling sheets that were mounted above the cold part of the thermocouples could increase heat dissipation so that the TD at the CHP of the thermocouples increased. To form the suspended thermocouple structure, the TEMH required a post-process to remove the sacrificial materials. The post-process involved two steps. One was to etch the sacrificial silicon dioxide utilizing RIE CF_4/O_2, and the other was to etch the sacrificial silicon substrate using SF_6/O_2. The results showed that the structure of the thermocouples was completely suspended and did not exhibit any injury. The measured results revealed that the TEMH had an output voltage of 32.5 mV when the TD at the CHP of the thermocouples was 4 K. The TEMH had a voltage factor of 8.93 mV/mm^2K. The maximum output power of the TEMH was 4.72 nW when the TD at the CHP of the thermocouples was 4 K. The TEMH had a maximum power factor of 0.31 nW/mm^2K^2.

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Communication

An Experimental Investigation of the Degradation of CMOS Low-Noise Amplifier Specifications at Different Temperatures

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Abstract: To investigate the relationship between the specifications degradation of a low-noise amplifier (LNA) and temperature, we experimentally investigated the degradation characteristics of the specifications of the LNA at different temperatures. The small-signal gain (S21) of the LNA decreases with increasing temperature. This paper discusses and analyzes the experimental results in detail, and the reasons for the degradation of LNA specifications with temperature changes are known. Finally, we have tried to use the structure already available in the literature for the PA temperature compensation circuit for the temperature compensation of the LNA. The results show that the existing circuit structure for PA temperature compensation in the literature can also effectively compensate for the S21 and NF degradation of the LNA due to the temperature increase.

Keywords: CMOS; specification degradation; temperature; LNA

1. Introduction

A low-noise amplifier (LNA) is used in the first stage of a radio frequency (RF) transceiver to amplify a signal with low noise [1]. At the same time, the specification of the LNA will change with the change in temperature because the parameters of semiconductors are very sensitive to the change in temperature [2,3]. Therefore, their system will fail when the specifications of LNAs decrease with the temperature change; thus, they cannot meet the minimum requirements required for the system's normal operation.

Current research on LNAs focuses on the optimization of performance specifications, such as bandwidth [4–6], linearity [7–9], gain [10,11], noise figure [12,13], and power consumption [14–16]. For example, in 2016, G. Nikandish et al. [4] proposed a feedback amplifier circuit to increase the bandwidth of the LNA. In 2016, Sunhwan Jang et al. from the United States published a paper entitled "A High-Gain Power-Efficient Wideband V-Band LNA in 0.18 μm SiGe Bipolar Complementary Metal-Oxide Semiconductor (BiCMOS)", in which Sunhwan Jang et al. used an effective wideband gain shaping method to improve the gain of LNAs at low power consumption [11]. Furthermore, at the 2018 18th Mediterranean Microwave Symposium, O. Memioglu et al., scholars from Middle East Technical University, presented a cascaded topology with excellent noise figures consisting of cascaded topology with inductive source degradation of co-sourced devices [7]. In 2020, Yuito Sawayama et al. from Okayama Prefectural University in Japan achieved a low-noise figure LNA by replacing the primary inductor with an external inductor in the input matching circuit [13]. In 2021, Roman Yu. Musenov, an academic from Russia, et al. proposed a single-ended low-power LNA based on 90 nm CMOS technology, which achieves low power consumption by employing current reuse techniques [15]. These studies focus on

improving the bandwidth, linearity, and gain of LNAs, and reducing the noise figure and power consumption.

In this paper, we investigate the relationship and law of degradation of LNA specifications with temperature changes, taking 50 MHz–450 MHz CMOS LNAs as an example. The reasons for the degradation of LNA specifications, such as gain and noise figure with increasing temperature, are discussed and analyzed. Based on this, we also designed a circuit for compensating the temperature characteristics of this LNA, which consists of a diode and two resistors. The simulation results show that this compensation circuit can effectively compensate for the degradation of S21 and NF due to temperature. The results can provide a theoretical reference for the design of the temperature compensation circuit of LNA. On the other hand, it can provide effective guidance for optimizing the system design.

2. Structure and Experimental Setup of LNA

2.1. The Structure of LNA

The schematic diagram of the LNA and the chip micrograph are shown in Figures 1 and 2, respectively.

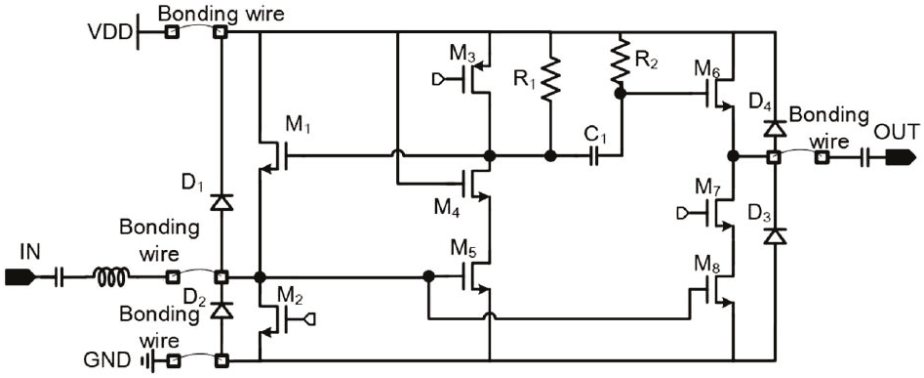


Figure 1. The schematic diagram of the LNA [17].

As shown in Figure 1, the LNA is manufactured using a 0.18 um CMOS process [17]. In this LNA, a shunt feedback structure is used in the matching stage to reduce the noise factor of the LNA [17]. The load of the matching stage uses a PMOS (positive channel metal oxide semiconductor) current source in parallel with a resistor, mainly to relax voltage headroom and achieve adequate performance in process corners [17,18].

Figure 2 shows a micrograph of the chip of the LNA, which was gold wire bonded to a PCB (printed circuit boards) board to facilitate temperature characterization experiments in an environmental chamber. The left and right ends of the PCB are the input and output, respectively, which are connected to the test system via a 50-ohm matched subminiature version A (SMA). In addition, external inductors and resistors are used at the input and output of the PCB to achieve better matching. Two supply voltages are used for this LNA, 1.8 V and 3.3 V, respectively.

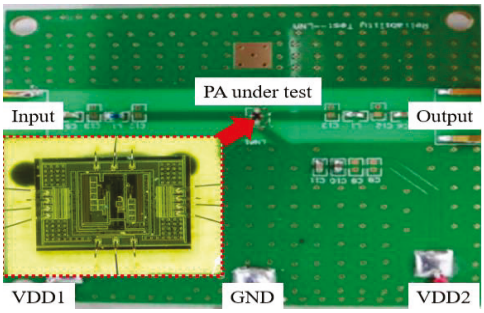


Figure 2. The micrograph of the chip of the LNA.

2.2. Experimental Environment and Setup

As shown in Figure 3, the experiments were conducted in a chamber (SC^3 1000) that can support conducting high- and low-temperature experiments from −40 °C to 125 °C. However, due to the constraints of the experimental cable, only the temperature characteristics of the LNA from −40 °C to 90 °C are investigated.

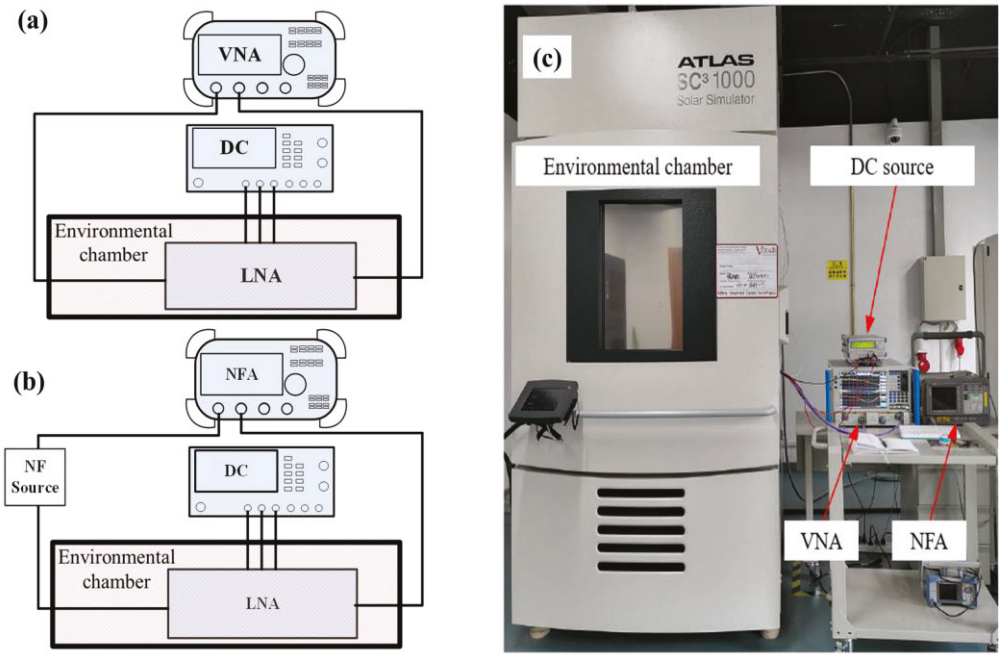


Figure 3. Measurement environment and setup: (**a**) a schematic diagram of the S-parameter measurement; (**b**) a schematic diagram of the NF measurement; (**c**) a physical diagram of the measurement environment.

In the experimental process, we focused on the temperature characteristics of the gain and noise figure. The gain and noise figures were measured with a vector network analyzer (VNA) (AV3672B) and a noise figure analyzer (N8975A). In addition, a Rohde & Schwarz power supply (NGMO2) was used for the power supply required in the experiments.

3. Results and Discussions

3.1. The S21

The temperature characteristics of the LNA gain are shown in Figure 4. From the figure, we can see that S21 is not only a function of temperature, but also a function of frequency. As the temperature increases, the S21 of the LNA gradually decreases. S21 decreases with increasing frequency, only differing at individual points. This may be caused by jitter in the measurement system during the measurement process.

The specific causes of the degradation of the gain of the LNA with increasing temperature are discussed below.

The expressions for I_{DS} in the linear and nonlinear regions, respectively, are [19,20]

$$I_{DS-linear} = \frac{W\mu_n C_{ox}}{2L}\left[2(V_{GS} - V_{TH})V_{DS} - {V_{DS}}^2\right] \quad (1)$$

$$I_{DS-nonlinear} = \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_{TH})^2 \quad (2)$$

where W is the gate width, μ_n is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, L is the gate length, V_{GS} is the gate voltage, V_{TH} is the threshold voltage, and V_{DS} is the drain voltage.

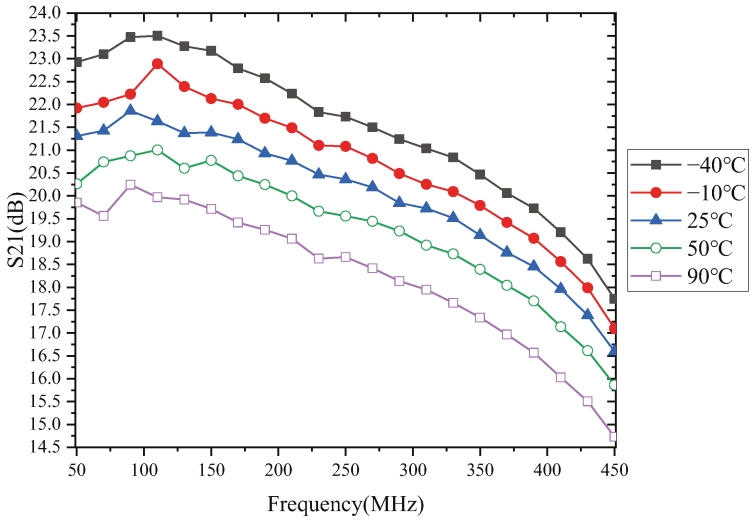


Figure 4. Measured gain with frequency variations.

According to Equations (1) and (2), the transduction in the linear and nonlinear regions is [19,20]

$$g_{m-linear} = \sqrt{2\mu_n \frac{WC_{ox}}{L} I_{DS-linear}} \tag{3}$$

$$g_{m-nonlinear} = \sqrt{2\mu_n \frac{WC_{ox}}{L} I_{DS-nonlinear}} \tag{4}$$

where the expression for the carrier mobility is [21]

$$\mu_n(T) = \mu_n(T_0)\left(\frac{T}{T_0}\right)^{-m} \tag{5}$$

where T_0 = 300 K, m = 1.5~2.

According to Equation (5), the μ_n degrades with increasing temperature. And according to Equations (3) and (4), it is known that the transconductance of both linear and nonlinear regions is positively related to carrier mobility. Therefore, the transconductance of both linear and nonlinear regions will degrade with increasing temperature. In addition, the transconductance is the gain [19,20]; thus, the LNA's gain is also degraded as the temperature increases. Therefore, the decrease in S21 with increasing temperature decreases carrier mobility with increasing temperature.

We already know that the S21 degrades as the temperature rises. Figure 4 shows that when the temperature change range is the same, the S21 changes at different frequencies are also different. For example, Figure 5 shows the evolution of S21 in the temperature range of −40 °C to 90 °C.

As shown in Figure 5, S21 decreases by 3.54 dB, 3.2 dB, and 3.02 dB for 70 MHz, 230 MHz, and 450 MHz, respectively, when the temperature increases by 130 °C. This indicates that the μ_n is temperature-dependent and frequency-dependent.

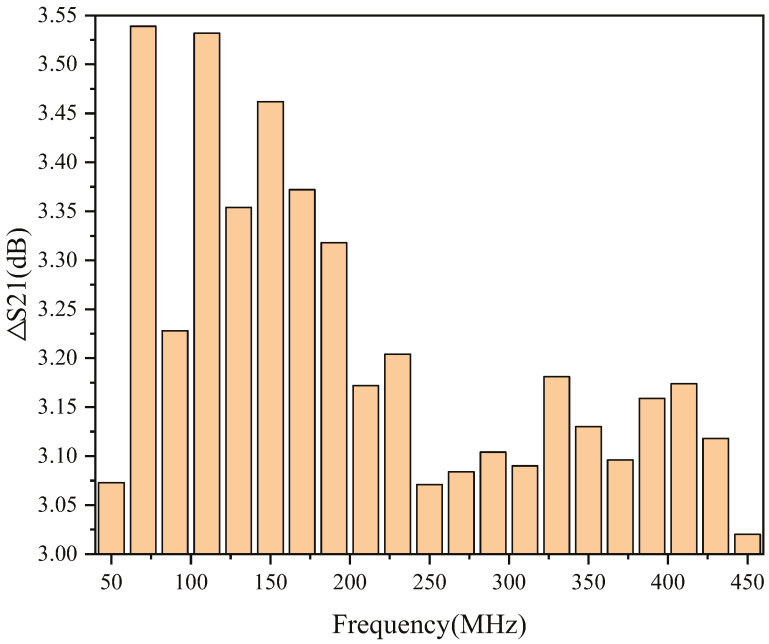


Figure 5. Variation of S21 in the temperature range from −40 °C to 90 °C.

3.2. The Noise Figure (NF)

The noise figure of the LNA as a function of temperature is shown in Figure 6. As shown in Figure 6, the noise coefficient of the LNA increases with temperature; this means that the noise performance of the LNA degrades with increasing temperature. In addition, the noise figure of the LNA varies with frequency rather than monotonically. That is, the noise figure of the LNA increases or decreases with increasing frequency. This indicates that the noise figure of the LNA is not only a function of temperature, but also a function of frequency.

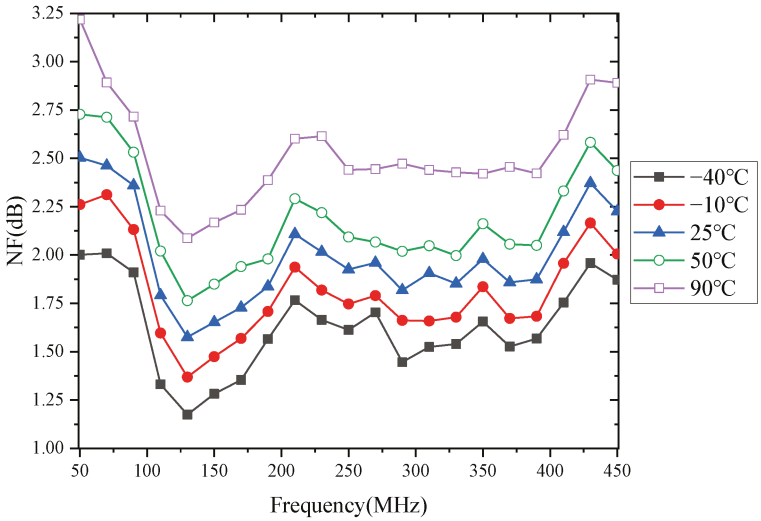


Figure 6. Measured noise figure with frequency variations.

The following is a specific discussion of the causes of the increase in the noise coefficient of the LNA with increasing temperature. The expression of the NF_{min} of LNA is [22]

$$NF_{\min} = 1 + 2\pi K(C_{gs} + C_{gd})\sqrt{\frac{R_s + R_d}{g_m}} \quad (6)$$

where K is the Fukui constant, C_{gs} and C_{gd} are the gate-source and gate-drain capacitance, R_s and R_d are the source and drain resistance, and g_m is the transconductance.

The transconductance degrades with increasing temperature. In addition, the source/drain resistance also increases with temperature. Therefore, according to Equation (6), the increase in source/drain resistance and the degradation of the transconductance will increase the NF_{min} of the LNA as the temperature increases. Consequently, there is an increase in the LNA noise figure with the temperature rise. This indicates that the increase in source/drain resistance and the transconductance degradation are the two main reasons for the rise in the noise figure with increasing temperature.

It is already known from Figure 6 that the noise figure of the LNA increases with temperature. This is because the NF changes differently for different frequencies in the same temperature variation range. For example, Figure 7 shows the variation of the noise figure to varying frequencies in the field of −40 °C to 90 °C. As shown in Figure 7, the noise figure at 50 MHz, 270 MHz, and 450 MHz increases by 1.22 dB, 0.74 dB, and 1.02 dB, respectively, when the temperature increases from −40 °C to 90 °C. This also shows that the μ_n is not only temperature-dependent but also frequency-dependent.

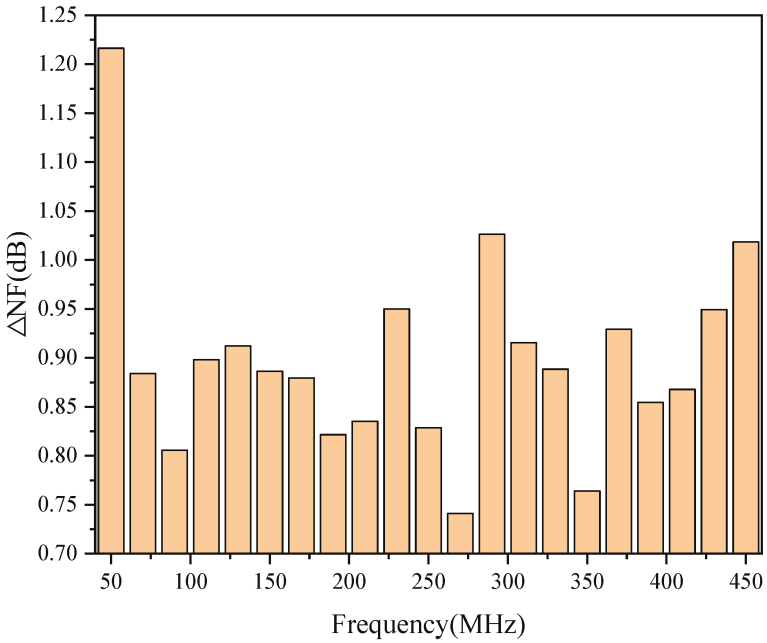


Figure 7. Variation of the NF in the temperature range from −40 °C to 90 °C.

4. On-Chip Temperature Compensation for LNAs

A circuit structure for multistage PA temperature compensation was proposed in the literature [23]; based on this structure, we propose a temperature compensation circuit for stacked PAs [24]. Considering the simple structure of this compensation circuit and our existing research base, in this subsection, we try to use the temperature compensation circuit structure for the multistage PA proposed in the literature [23] for the compensation of S21 and NF of the LNA. Furthermore, we explore whether the compensation circuit structure presented in [23] can be used for the temperature compensation of other microwave/RF circuits such as LNAs in addition to multistage PAs. The structure of the circuit used for LNA temperature compensation in this subsection is the same as that used for the multistage PA temperature compensation circuit in the literature [23], as shown in Figure 8. As shown in Figure 8, this compensation circuit consists of a diode (D_1) and two resistors (R and R_1).

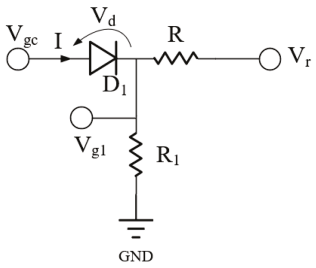


Figure 8. Temperature compensation circuit structure for the LNA [23].

Since the circuit structure used is the same as that of the literature [23], the temperature compensation principle of this temperature compensation circuit for the LNA is also the same as that of the literature [23]. Therefore, to avoid repetition, it is not presented again.

According to the literature [23], when the temperature increases from T_L to T_H, Equations (1) and (2) can be expressed, respectively, as

$$I_{DS-linear} = \frac{W\mu_n C_{ox}}{2L}\left[2((V_{GS} + \Delta V_{g1}) - V_{TH})V_{DS} - {V_{DS}}^2\right] \tag{7}$$

$$I_{DS-nonlinear} = \frac{W\mu_n C_{ox}}{2L}((V_{GS} + \Delta V_{g1}) - V_{TH})^2 \tag{8}$$

where ΔV_{g1} is the variation of V_{g1} between two temperatures (T_H and T_L).

According to Equations (7) and (8), the I_{DS} will increase with the increase of ΔV_{g1}. Furthermore, from Equations (3) and (4), the transconductance is proportional to the drain current; i.e., it increases with the increase of the I_{DS}. This means that the temperature compensation circuit increases the transconductance with the rise in the ΔV_{g1}; thus, the temperature compensation of the transconductance is realized. That is, the compensation of S21 is realized.

Figure 9 gives the simulation results of S21 with and without compensation, from which when the temperature increases from −40 °C to 90 °C, S21 changes by 0.4 dB with compensation, while S21 changes by 3.5 dB without compensation; this indicates that the compensation circuit is effective in compensating S21 with a temperature change.

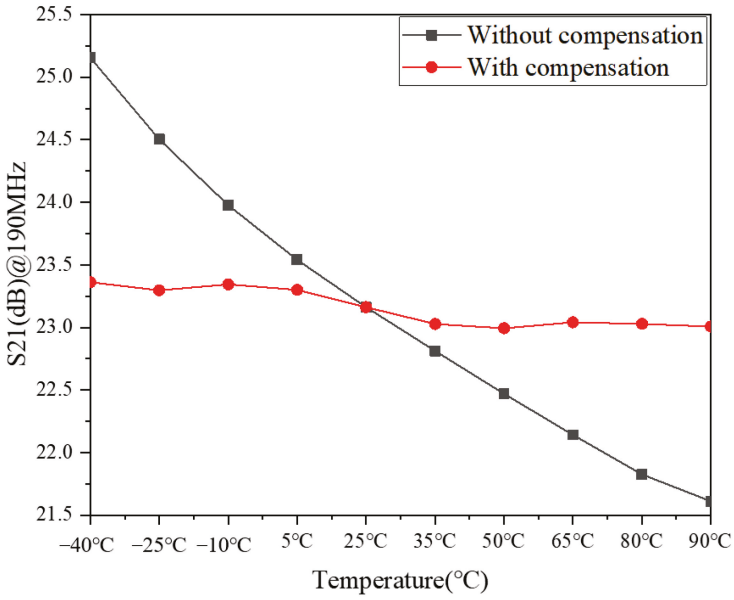


Figure 9. Simulation results of S21 with and without compensation.

From Equation (6), NF will decrease with the increase of the transconductance. Therefore, under the temperature compensation circuit, NF will reduce with the rise of the ΔV_{g1};

thus, this will achieve the temperature compensation of NF. The simulation results for the NF with and without compensation are shown in Figure 10. It can be seen from this that the NF with temperature compensation varies less with temperature, while the NF without temperature compensation increases with temperature. Specifically, when the temperature increases from −40 °C to 90 °C, the NF changes by 0.02 dB with temperature compensation, while the NF changes by 0.3 dB without temperature compensation. This indicates that the temperature compensation circuit effectively compensates for the NF degradation with temperature increase.

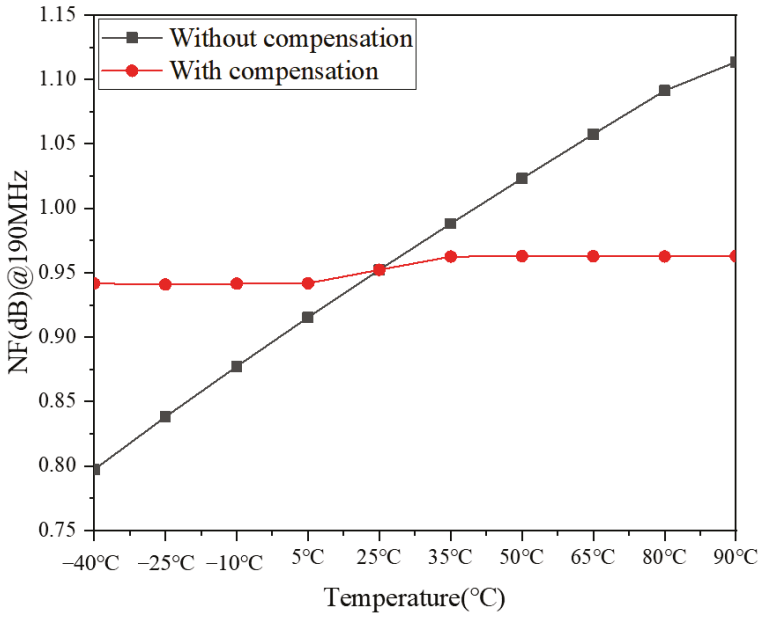


Figure 10. Simulation results of the NF with and without compensation.

The above is the working principle of the temperature compensation circuit proposed in this subsection, mainly to increase the transconductance by increasing the gate voltage to achieve the compensation of S21 and NF with temperature change. The simulation results in Figures 9 and 10 show that the temperature compensation circuit structure proposed in the literature [23] applies not only to the temperature compensation of PA, but also to the temperature compensation of LNA.

5. Conclusions

This paper investigates the key specifications of LNAs, such as gain and noise figures, from an experimental point of view at different temperatures using a CMOS 50 MHz–450 MHz LNA as an example. The S21 decreases with temperature increase while the noise figure increases. Furthermore, it is found that one of the leading causes of the degradation of the gain and noise characteristics is the degradation of the transconductance. The results can guide temperature-compensated circuit design to complement the degradation of the specification. On the other hand, it is also proved that the temperature compensation circuit structure proposed in the literature [23] applies to the temperature compensation of PAs and can be used for the temperature compensation of LNAs.

The specification degradation of the LNA is not only related to temperature, but also to humidity, high- and low-temperature shock, and time. Therefore, future work in this paper will consider the relationship between the specification degradation of the LNA with humidity, the number of high- and low-temperature shocks, and time.

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An Ultra-Compact MEMS Pirani Sensor for In-Situ Pressure Distribution Monitoring

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Abstract: In this study, we designed a microelectromechanical system (MEMS) Pirani vacuum sensor with a compact size. Specifically, the sensor was successfully fabricated based on the Pirani principle and using a commercial eight-inch MEMS foundry process. The sensor fabrication process was carried out using only four photomasks and the proposed sensor had an ultra-compact fabricated size (<2.2 × 2.2 mm^2). A vacuum measurement system was set up to comprehensively evaluate the fabricated sensors. The results demonstrated that the MEMS Pirani vacuum sensor has a high responsivity in the low-pressure domain from 100 Pa. The proposed sensor with a 953.0-Ω heater exhibited an average responsivity of 11.9 mV/Pa in the preferred range of 100 to 7 Pa and 96.0 mV/Pa in the range of 7 to 1 Pa. The sensor may be potentially suitable in many applications, such as vacuum indicators for processing equipment, health monitoring systems for social infrastructure, and medical and health applications.

Keywords: MEMS; Pirani sensor; vacuum test; simple process; lift-off

1. Introduction

Vacuum monitoring technology for industrial equipment is becoming increasingly important. With the boom in the semiconductor market, the relative industry has become increasingly dependent on vacuum technology [1–3]. Since the invention of the Pirani vacuum gauge in 1906, it has been widely used in various application fields because of its low cost and easy operation [4]. The principle of the Pirani vacuum gauge is a well-known subject. In the gauge, a heating resistance wire is suspended in a gas environment and dissipates heat to gas molecules [5,6]. The vacuum degree changes the number of molecules that can increase or decrease heat dissipation. Hence, measuring heat dissipation is an indirect method of measuring a vacuum. Traditional Pirani vacuum sensors have underwent years of development and have been used in diverse fields [7–9]; however, they are also subject to constraints, such as high cost and a large size, and they are difficult to mass-produce. The state of the art and development of microelectromechanical system (MEMS) technologies have revolutionized various industries, especially vacuum sensor technology [10–12]. The MEMS-based Pirani sensor not only has a low production cost and the ability to save power consumption [13,14], it also facilitates easy integration in measurement systems [15,16].

Although many high-performance Pirani vacuum gauges based on MEMS techniques have been developed, they usually have a relatively complex structure and a large size [17,18]. To adapt to the requirements of more specified application fields, the MEMS Pirani sensors should be as compact as possible for large-scale arrays at a low cost. This study sought to develop a MEMS Pirani sensor that can afford in-situ measurements of uneven pressure distributions (mainly within 1–100 Pa) in narrow working spaces, while exhibiting quick responses. An ultra-compact MEMS Pirani vacuum sensor was developed in this study via a simple MEMS fabrication process. All structures of the proposed sensor

were constructed using only four photomasks with the lift-off processes throughout the production, except for the back release in the final step.

2. Experimental of the MEMS Pirani Sensor

2.1. MEMS Pirani Sensor Conception

Figure 1 shows the conception and potential application of the proposed MEMS Pirani sensor. We designed a series of super-miniaturized MEMS Pirani vacuum sensors based on the simulation calculation results. The sensor was successfully fabricated on an 8-inch MEMS production line. We performed a comprehensive evaluation of the sensor, and the microstructures of the fabricated vacuum sensor were observed using scanning electron microscopy (SEM). After completing the test package and device signal processing circuit, the output voltages of the fabricated sensor devices with different resistor lengths under different pressures were evaluated comprehensively. We measured the internal resistance changes and temperature increase of the proposed sensor resistor caused by applying different voltage and pressure values. The developed MEMS Pirani vacuum sensor has several advantages. It is based on the MEMS process enabling it to have compact die size for saving space in the sensor terminal assembly, which will reduce costs. Moreover, the sensor can be fabricated using a simple process, which further reduces costs. According to the test results, the fabricated sensor has a large working range, from atmosphere pressure to <0.1 pascals. Thus, the sensor can be used in many applications. Owing to its cost effectiveness, the MEMS Pirani vacuum sensor can be considered for many applications, such as vacuum measurements for processing equipment, health monitoring systems for social infrastructures, and medical and health applications.

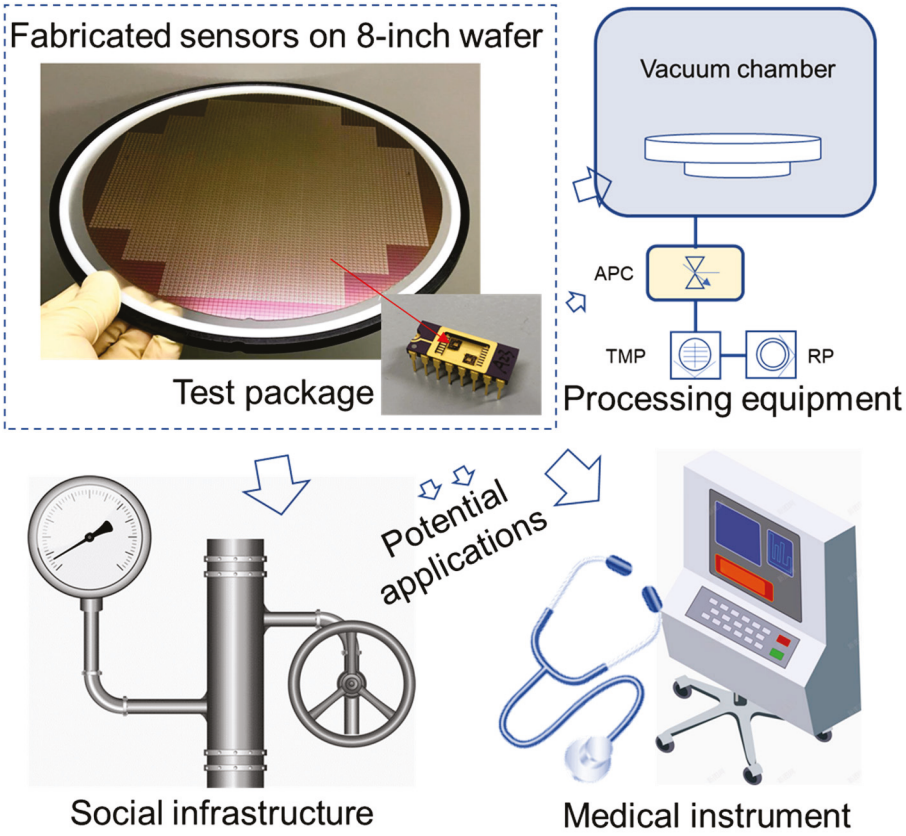


Figure 1. Conception and potential application of the MEMS Pirani vacuum sensor. Inserts are an optical image of the sensors fabricated on the eight-inch wafer and a package sensor for evaluation.

2.2. Sensor Design

Calculations and finite element method (COMSOL Multiphysics, COMSOL Inc. Burlington, MA, USA) were used to validate the structure segment of the Pirani vacuum sensor. Figure 2 shows the calculation results of the thermal power of a typical sensor structure. N_g, N_c, and N_r denote the sensing elements that lose heat by gas convection, solid conduction, and radiation, respectively. The calculation provides the design guidelines for obtaining the desired structure by adjusting the size and parameters of the sensor. In the simulation process, the geometrical and characteristic parameters of the sensor components and materials were set. The following structural materials were used: platinum (Pt) for the sensor resistor and extended electrode and silicon nitride (Si_3N_4) for thermal insulation. The key parameters of the sensor structural materials were as follows: the thickness of Pt and Si_3N_4 were set to 200 and 300 nm, and their thermal conductivities to 71.0 and 20.0 W/mK, respectively. The density of Pt and Si_3N_4 were 21,450 and 3100 kg/m^3 and the electrical conductivities were 8.9E6 and 0 S/m, respectively. The vacuum loading conditions for different sensor designs, which had different lengths of Pt resistors from 860 to 8600 μm, were set at simulated pressures from 1000 hPa to high vacuum.

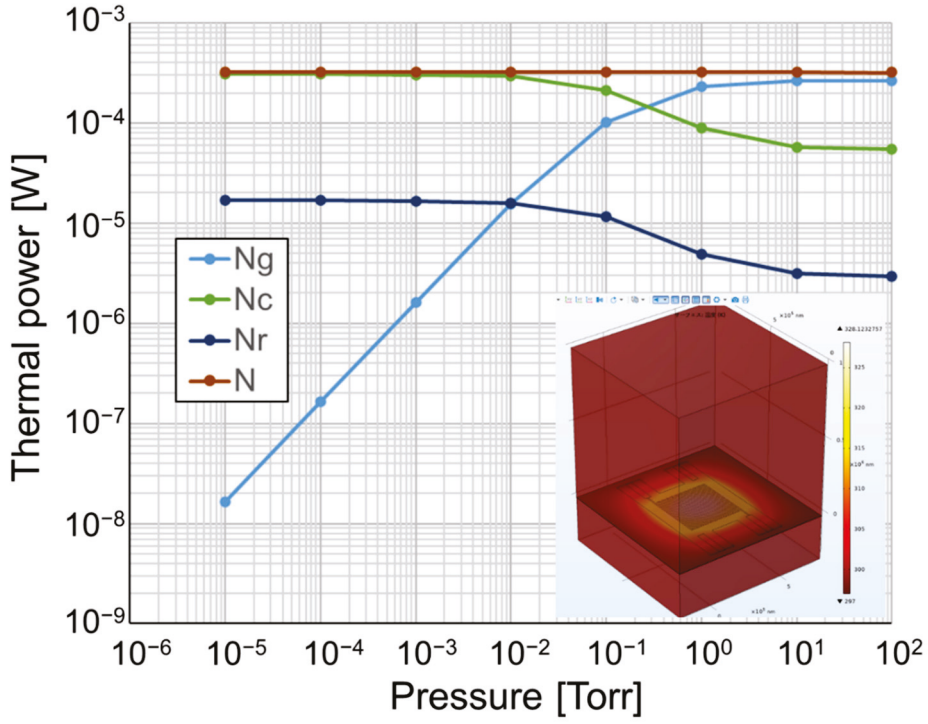


Figure 2. Calculation results of the thermal power of a typical sensor. The inset shows the simulation results of the temperature of a sensor with longest resistor design, indicating its temperature increase for an applied voltage.

The inset shows that the simulation results of the temperature of a typical sensor increase under an applied voltage. The core components of the vacuum sensors, which are the resistor, heat-insulating layer, and beams, are comprehensively modeled and simulated. On a flat surface, the border area is 1 × 1 mm^2, slightly larger than the heat-insulating layer and beams. In the longitudinal direction, because the main heat exchange of the sensor occurs on the upper surface, the simulation boundaries are set as 1 mm above the front side and 0.3 mm above the back side. A sufficient boundary can approximate the actual thermal diffusion conditions around the sensor, and the simulation accuracy of the sensor can be improved accordingly. The simulation results show that the surface temperature of the sensor with the longest resistor increases to 55 °C in atmospheric conditions.

Figure 3 shows the schematic view of the Pirani vacuum MEMS sensor design with the sensor's surrounding circuit (Figure 3b). A Wheatstone bridge was used as a detection circuit to measure the change in the resistance of the heater resistor due to temperature/vacuum changes. The heater and reference resistors are designed with the same pattern. In the Wheatstone bridge, the ratio between the heater resistor and reference resistor is 1:2 by connecting two reference resistors into one unit. The heater and reference resistors on the sensor chip and the variable resistors were packaged on the Wheatstone bridge balance adjustment and zero-point debugging circuit board. We assume that the heater resistor can generate a specific temperature difference when the vacuum value changes. In addition, the absolute temperature of the heater would not be so high as to reduce the service life. Thus, the critical structure of the proposed sensor and the temperature rise of heater resistors with different resistance values in different vacuum conditions are simulated. All the simulations and calculations aim to devise optimized design principles for realizing the sensor with an ultra-compact size. The distribution of the temperature field of the Pirani sensor was considered, and the optimized width size of the thermal insulation Si_3N_4 layer and the insulation window can be determined at 500 μm and 900 μm, respectively. The resistor beam width was determined to be 8 μm by considering the desired sheet resistance of the proposed resistor and the reasonable accuracy and stability of MEMS fabrication. The simulation results may exhibit a deviation error from the actual measurement results. Under the influence of various factors such as the constraints, the simulation environment deviates from experimental conditions. The two main influencing factors in this deviation are the deviation of the material parameters and dimensions of the sensor. The material parameters set in the simulation are the parameters in the COMSOL material library, ideal values that inevitably deviate from the actual values in the fabricated device. In contrast, the dimensions of the vacuum sensor in the simulation follow the design size entirely, and the fabricated sensor structure size is slightly affected by MEMS processing. Therefore, the simulation process provides a trend reference for sensor design. After the sensor fabrication trial and comprehensive evaluation, the measurement results should be used to check and improve the simulation process. Thus, the ideal model using the design guideline can be approached efficiently and accurately.

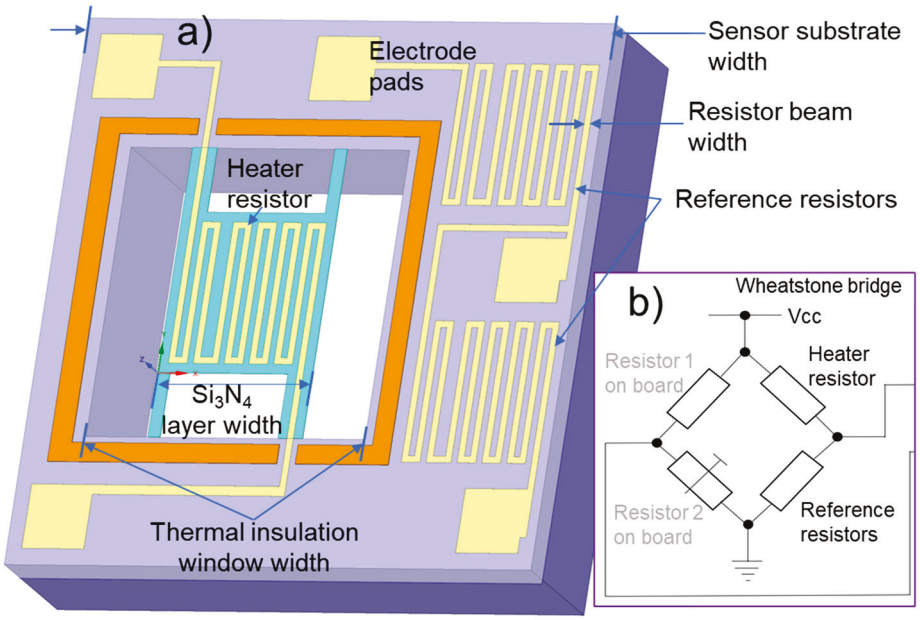


Figure 3. Schematic view of the Pirani vacuum MEMS sensor design with surrounding circuit. (**a**) Pirani vacuum MEMS sensor design; and (**b**) schematic view of the sensor's surrounding circuit.

2.3. MEMS Fabrication Processes

The sensor fabrication process started with an 8-inch and 300-μm thickness Si wafer. The device fabrication was performed by the MEMS process using 4 photomasks shown in Figure 4 and described as follows:

1. After the initial wafer cleaning and passivation-layer generation, a 300-nm heat-insulating layer of Si_3N_4 was generated on the top surface of the Si wafer by using a vertical furnace equipment (VF-3000, Koyo Co., Ltd. Tenri, Nara, Japan);
2. The lift-off photoresist used for the Pt layer was uniformly coated on the surface and well patterned; a sputtering equipment (SME-200E, Ulvac Co., Ltd. Chigasaki, Kanagawa, Japan) was used to deposit the Pt and gold (Au) metal films on the wafer. The layers of Ta_2O_5/Pt with a thickness of 20 nm/200 nm were generated on the top surface of the photoresist, and the resistor and electrode pads were fabricated by a lift-off process;
3. After Au layer lift-off photoresist coating and patterning, a 500-nm-thickness Au layer was generated on the Pt electrodes for wire and package bonding;
4. The Si_3N_4 layer was patterned by dry etching, and Si was released by wet etching from the backside. To pattern the Si_3N_4 layer and remove the photoresist layer and other residuals after all the processes, dry etching was performed (E-628, Panasonic Co., Ltd. Moriguchi, Osaka, Japan). Finally, O_2 plasma was used to remove the amorphous fluoropolymer material and other residuals.

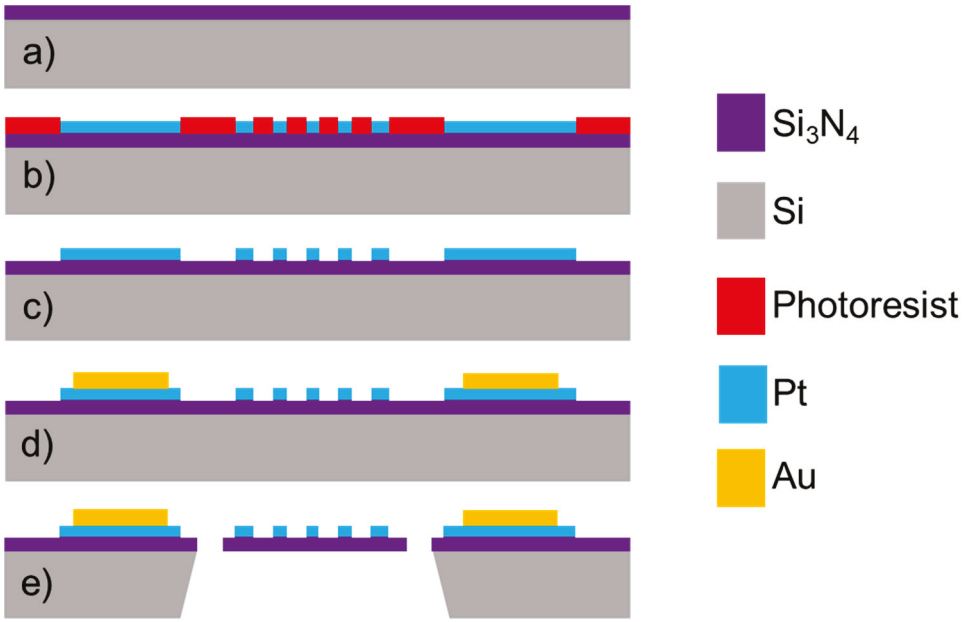


Figure 4. Schematic fabrication sequence of the MEMS Pirani vacuum sensor. (**a**) Si_3N_4 layer generation; (**b**) metallic electrode sputtering; (**c**) lift-off processes with photoresist; (**d**) Au-pads generation and patterning; and (**e**) sensor structure release.

2.4. Evaluation Methods

Figure 5 shows the evaluation system for the MEMS Pirani vacuum sensor and measurement board. Figure 5a,b show the optical photograph and flowchart, respectively, of the measurement system used to evaluate the vacuum sensor. First, an oil rotary vacuum pump (GLD-100A, Ulvac Co., Ltd. Chigasaki, Kanagawa, Japan) and a turbo molecular pump (TH350, Osaka Vacuum Industrial Co., Ltd. Osaka, Japan) were set at the front of the test system, which was turned on and operated continuously. The rotary vacuum pumps were connected to the vacuum chamber through the pipe. The vacuum degree in the vacuum chamber was controlled and adjusted using the vacuum controller (APCS-001, All Vacuum Create Co., Ltd. Hitachinaka, Ibaraki, Japan) and mass-flow controller

(FCST1005LC, Fujikin, Co., Ltd. Osaka, Japan). A low-noise power supply unit was used to provide power to the sensor, and a data logger (DL, Hv gl2000, Graphtec Co., Ltd. Yokohama, Kanagawa, Japan) was used to record the results. An analog pressure full-range cathode Pirani gauge (M-361CP-SP/N25, Ulvac Co., Ltd. Chigasaki, Kanagawa, Japan) and two capacitance manometers (CDG045Dhs, Inficon Co., Ltd. Kawasaki, Kanagawa, Japan) were used to monitor the pressure in the chamber as a reference pressure gauge. Figure 5c is the optical photograph of the packaged vacuum sensor set on the measurement board. A 1 euro cent coin is used to compare with the measurement board to highlight the compact size of the proposed sensor system. A high-performance instrumentation amplifier (InAmp, AD8429, Analog Devices Co., Ltd. Wilmington, Massachusetts, USA) was used as the measurement circuit. In reasonable circuit designs, the amplifier can provide 4 signal amplification functions, namely 1-, 10-, 100-, and 1000-times, for the measurement circuit. In this study, we used the 10-times amplification function for sensor system evaluation.

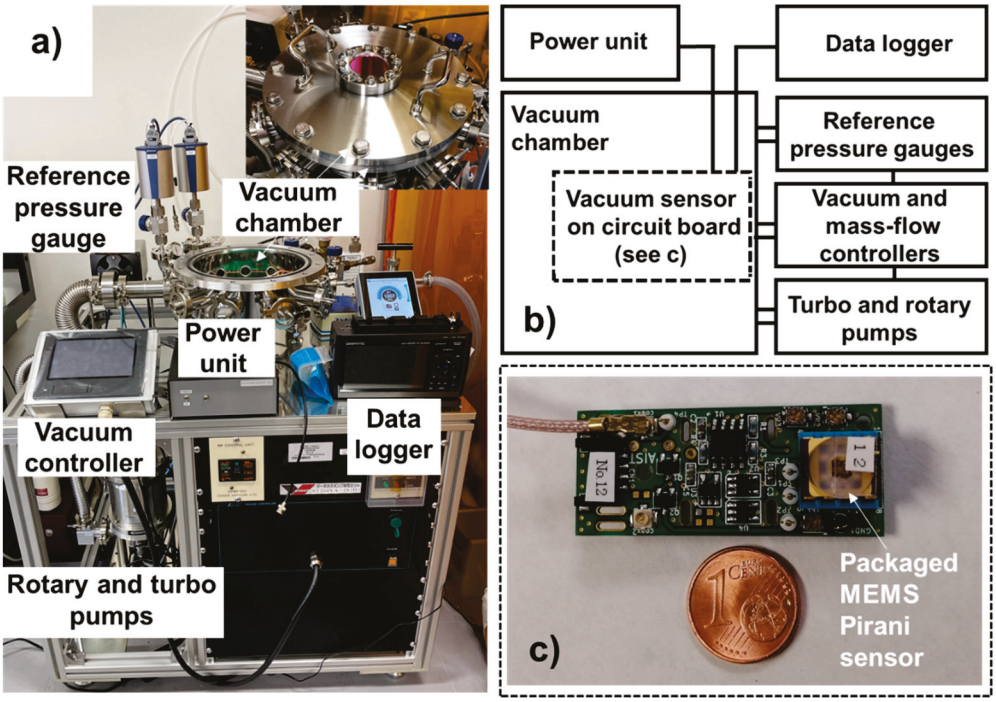


Figure 5. (**a**) MEMS Pirani vacuum sensor evaluation system and measurement board. (**b**) Optical photograph and configuration flow chart of the evaluation system. (**c**) Optical photograph of the packaged vacuum sensor set on the measurement board.

3. Measurement Results and Discussion

3.1. SEM Observation

To evaluate the accuracy of the fabricated microstructure of the Pirani MEMS sensor, SEM (S-3000H, Hitachi Co., Ltd. Tokyo, Japan) was used to observe the fabricated vibration sensor. Figure 6a shows a SEM image of a typical vacuum sensor structure. As the figure shows, the vacuum sensor structure has an area of 2.2 × 2.2 mm^2 and a thickness of 300 μm. The fabricated sensor layout realizes a final device die area of fewer than 5 mm^2, which can significantly reduce the sensor production cost in foundries. The heater resistor is located on the 300-nm-thick Si_3N_4 square-shaped thermal insulation film, supported by four Si_3N_4 beam flexures. The Si_3N_4 square area has the same length and width of 500 μm, and the supporting beam flexure has a length of 200 μm and a width of 160 μm. The surrounding Si substrate cages the square-shaped film and supporting beam flexures. The typical vacuum sensor has a resistor on the square-shaped film and two reference resistors on the surrounding Si substrate to perform the differential operation that eliminates the effect of ambient temperature on the sensor, except for the barometric parameters. Figure 6b

shows a magnified SEM image of the reference resistor on the chip. The 200-nm-thick micro–nano structure of the metallic resistor line was precisely partnered after the lift-off MEMS process. An appropriately partnered metallic resistor line can effectively suppress intense changes in local resistance and ensure the internal resistance consistency of different resistors. Figure 6c shows the backside structure of the sensor after the backside release process. The backside releasing process is etching through the wafer and precisely opening a thermal insulation window with dimensions of 900 μm × 900 μm at the front side. Figure 6c also shows the etched boundary of the surrounding Si substrate; the Si substrate materials were sufficiently etched and had a smooth surface. The compact-sized MEMS Pirani sensor was appropriately fabricated, and the proposed sensor can be effectively realized for in-situ pressure distribution monitoring in instrument systems, with a low manufacturing cost and high integration features.

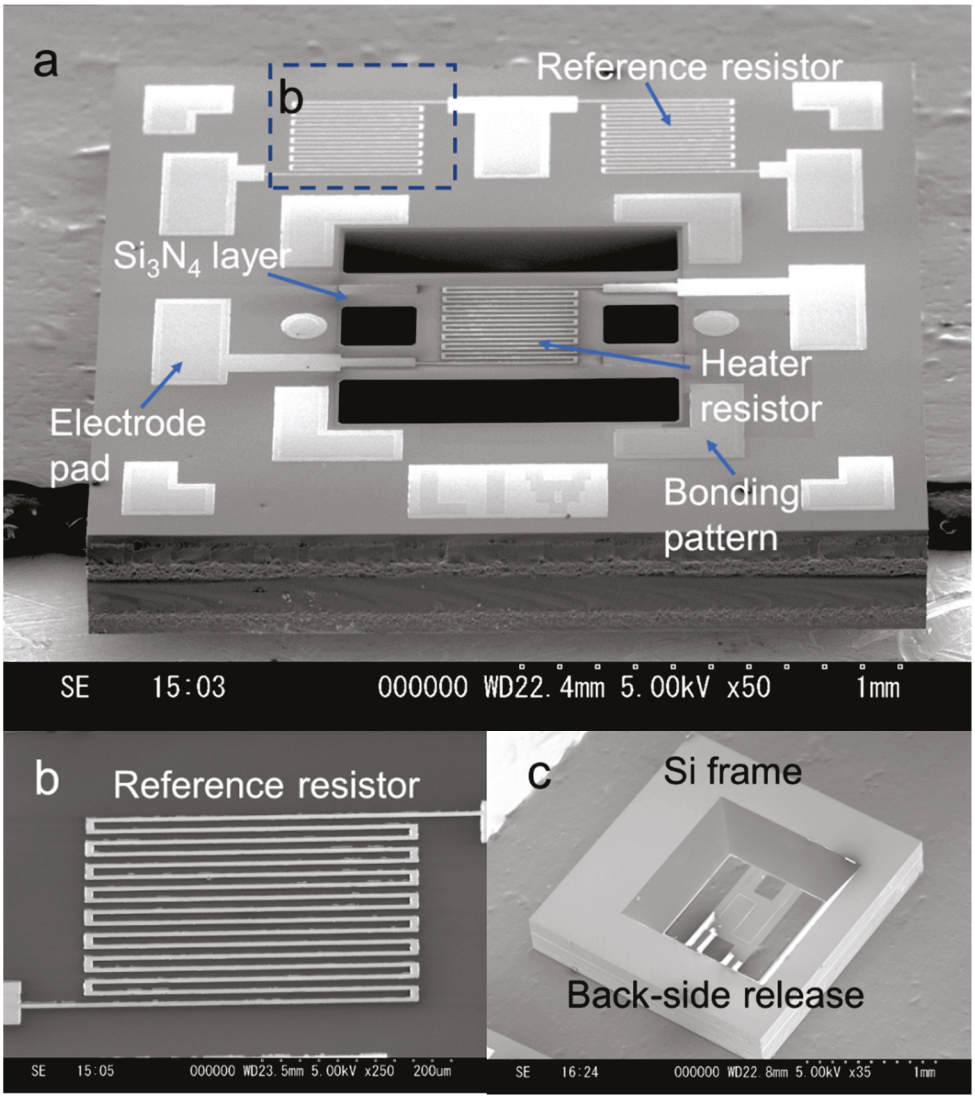


Figure 6. (**a**) SEM image of the proposed vacuum sensor. (**b**) The magnified SEM image of a reference heater with square-wave layout structures. (**c**) The sensor structure after the back side releasing process.

3.2. Vacuum Measurement for Different Size Sensor Resistors

Figure 7 shows the measured output voltage of the fabricated sensor device for the different resistor lengths under different pressures. The voltage source was used to apply a working voltage of 3 V to the sensors. The experiment was performed at a stable room

temperature of 25 °C. The performance of 5 vacuum sensors with heating resistors with resistance from 420.5 to 953.0 Ω in the air was measured. The signal test circuits set a 10× amplifier and a low-pass filter to reduce the sampling difficulty. The results demonstrate that the 5 sensors with different resistors have a reasonable response to vacuum pressures from 10,000 to 0.1 Pa. Comparing the voltage outputs of the five different sensors, the sensor with the smallest internal resistance had the highest voltage output. Because air pressure has a greater influence on temperature increase of the sensor with low internal resistance, the developed sensor system had a voltage output of 3.30 V at 1 Pa (see 420.5-Ω sensor output in Figure 7).

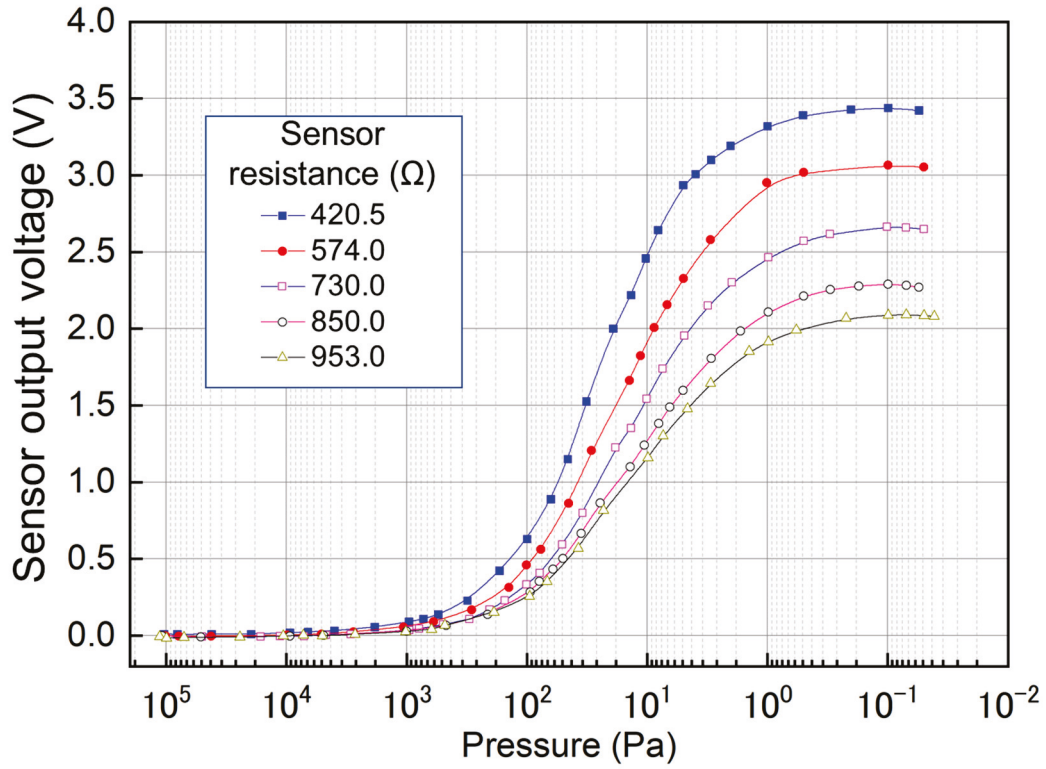


Figure 7. Measured output voltage of the fabricated sensor device with different resistors ranging from 420.5 to 953.0 Ω under different pressure conditions.

A careful observation of the results shows that the sensors had relatively low responsivity in the pressure range from the atmospheric pressure to 1000 Pa. The sensor's output curve was not completely linear; this is an inherent characteristic of Pirani vacuum sensors [19]. The measured sensors had a high response domain from 100 Pa; for example, the 953.0-Ω-resistance sensor had an average responsivity of 11.9 mV/Pa in the range of 100 to 7 Pa and that of 96.0 mV/Pa in the range of 7 to 1 Pa. Compared to the standardized sensor [18], the proposed sensor has reasonable responsivity within our preferred measurement pressure range but has features such as smaller membrane and die size, and a less complex structure without a heat sink. The previous study [6] used an SOI wafer for fabrication, which has limitations on the gap thickness between the membrane and substrate, while we used an Si wafer and a backside release process. Additionally, the similar sensor [6] used Ni as the heater resistance, which naturally has higher responsivity but lesser chemical stability than Pt used in the proposed sensor. Although the proposed sensor has similar responsivity to the compared sensor, we believe that this result will be of great significance to researchers in this field.

According to the measured results, the response domain can be divided into several ranges. The proposed Pirani sensors biased by constant voltage had different average responsivity to each pressure range, as shown in Table 1. In the high vacuum range

from 0.1 to 1 Pa, the highest responsivity of the sensor with 730.0-Ω heater is up to 226.7 mV/Pa. Meanwhile, in the low vacuum from 1000–10,000 Pa, the responsivity decreased to 0.0045 mV/Pa. The proposed sensor sought to achieve the best response in a field from 1 to 100 Pa. Although the 420.5 and 574.0-Ω sensors have a slightly high average responsivity, considering that the relatively low calorific value can improve sensor system stability, the sensors with the larger resistance can realize a high-stable sensor system while ensuring a relatively high responsivity.

Table 1. The average sensor responsivity derivative of the output voltage curve of Figure 7 is shown.

Heater Resistance Value	Average Responsivity of the Sensor System with 10-Times Amplification (mV/Pa)				
	0.1–1 Pa	**1–7 Pa**	**7–100 Pa**	**100–1000 Pa**	**1000–10,000 Pa**
420.5 Ω	131.1	95.5	22.0	0.630	0.0086
574.0 Ω	123.5	137.5	18.0	0.420	0.0059
730.0 Ω	226.7	113.1	15.0	0.349	0.0045
850.0 Ω	206.6	113.3	13.8	0.281	0.0035
953.0 Ω	197.1	96.0	11.9	0.248	0.0030

Experiments wherein a constant current was supplied to the sensor were also implemented. The constant-current source provided an applied current from 1 to 5 mA to the sensor at a stable room temperature of 25 °C. The sensor can reasonably respond to the atmospheric pressure up to a high vacuum. The sensor's output is similar to the constant voltage supplying experiment, that is, among the voltage outputs of the proposed sensor with different applied current values, the sensor has the most significant output for the largest applied current.

3.3. Resistance and Temperature Change of Sensor Resistor under Varying Applied Voltage and Pressure

To directly evaluate the heating characteristics of the fabricated Pirani sensor, we also measured the resistance and temperature changes of the typical senor resistor under varying the applied voltage and pressure. A thermal imager camera (PI640, Optris Co., Ltd. Berlin, Germany) was used to measure the temperature of the proposed vacuum sensor. Figure 8 depicts the resistance and temperature change as the voltage is applied to the typical sensor resistor. The voltage source (U8002A, Keysight Technologies, Inc. Santa Rosa, CA, USA) was used to apply voltages from 0.3 to 3 V at steps of 0.3 V. The experiment was carried out in atmosphere conditions, where the ambient air pressure was 1000 hPa. Figure 8 shows that with an increase in the applied voltage, the temperature and internal resistance of the sensor resistor increase correspondingly. The rate of increase in resistance agrees with the rate of increase in temperature of the sensor resistor. The measured temperature on the surface of the sensor resistor increased from room temperature with no applied voltage to 56.7 °C for an applied voltage of 3 V.

Figure 9 shows the temperature and resistance changes as a function of the ambient pressure. Because the ratio between the heating and reference resistors is 1:2, the voltage source was used to provide a fixed applied voltage of 1 V. The experiment was conducted in an ambient air pressure environment from atmospheric pressure to 0.1 pa. As shown in Figure 9, the temperature and internal resistance of the typical sensor resistor increase correspondingly with a decrease in pressure. The results of membrane surface temperature experiments showed that the proposed MEMS Pirani sensor with a 953.0-Ω-heater exhibits a relatively lower surface temperature. This feature improves the safety and stability of the sensor system while reducing its power consumption.

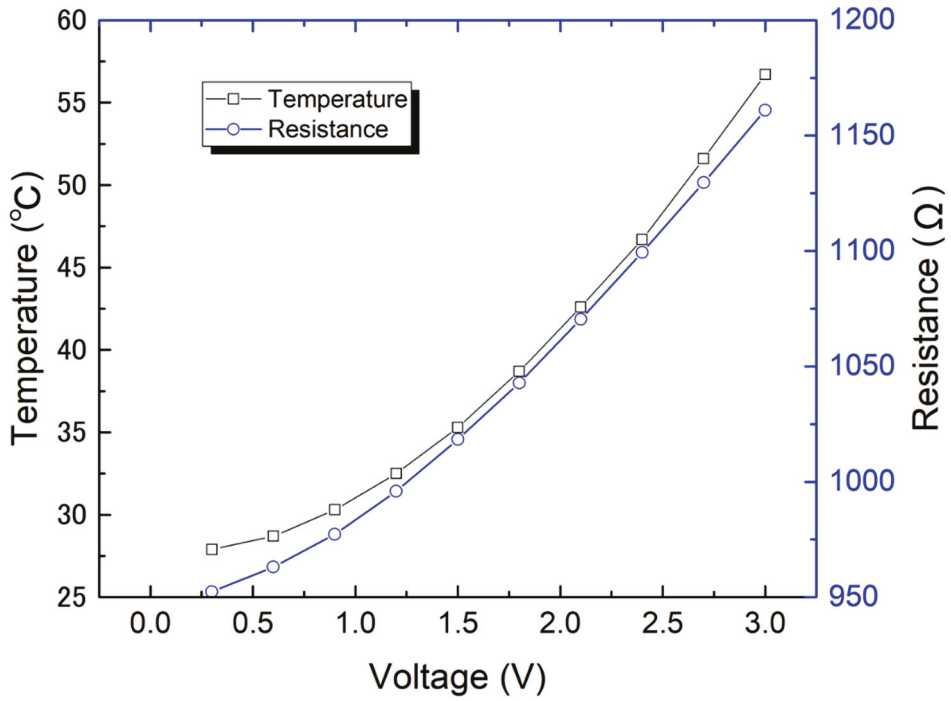


Figure 8. Measured surface temperature and heater resistance of the fabricated 953.0-Ω-heater sensor device for increasing the applied voltage from 0.3 to 3 V.

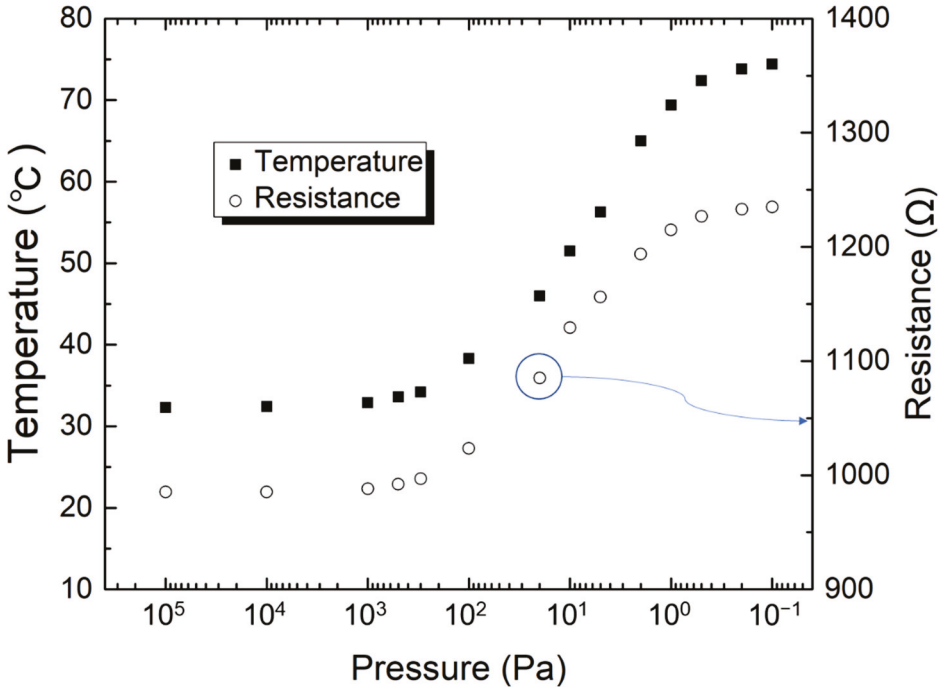


Figure 9. Measured surface temperature and heater resistance of the fabricated 953.0-Ω-heater sensor device for decreasing the applied pressure from 100,000 to 0.1 Pa.

4. Conclusions

A compact MEMS Pirani vacuum sensor with a high responsivity output was successfully fabricated using a commercial eight-inch MEMS foundry process. The sensor fabrication process is a simple process that uses only four photomasks, and the sensor is fabricated with an ultra-compact size (<2.2 × 2.2 mm^2). The fabricated Pirani vacuum sensors were evaluated comprehensively, and the results demonstrated that the MEMS Pirani

vacuum sensor has a high response in the low-pressure domain from 100 Pa. The proposed sensor (with 953.0-Ω heater) system exhibited an average responsivity of 11.9 mV/Pa in the preferred range of 100 to 7 Pa and that of 96.0 mV/Pa in the range of 7 to 1 Pa.

Author Contributions: The device structure simulation and design were conceived by L.Z., S.M. and J.L. The fabrication process of the proposed device was designed by L.Z., J.L., H.T. and E.H. The device signal processing circuit was completed by J.L. and L.Z. The device evaluation was performed by L.Z., J.L. and H.T. The first draft of the manuscript was written by L.Z. All authors have read and agreed to the published version of the manuscript.

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Impact of Various Thermistors on the Properties of Resistive Microbolometers Fabricated by CMOS Process

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Abstract: Microbolometers based on the CMOS process has the important advantage of being automatically merged with circuits in the fabrication of larger arrays, but they typically suffer from low detectivity due to the difficulty in realizing high-sensitivity thermistors in the CMOS process. In this paper, two resistive microbolometers based on polysilicon and metal Al thermistors, respectively, are designed and fabricated by the standard CMOS process. Experimental results show that the detectivity of the two resistive microbolometers can reach a maximum of 1.78×10^9 cmHz$^{1/2}$/W at 25 μA and a maximum of 6.2×10^8 cmHz$^{1/2}$/W at 267 μA. The polysilicon microbolometer exhibits better detectivity at lower bias current due to its lower effective thermal conductivity and larger resistance. Even though the thermal time constant of the polysilicon thermistor is three times slower than that of the metal Al thermistor, the former is more suitable for designing a thermal imaging system with sensitive and low power consumption.

Keywords: salicide polysilicon thermistor; microbolometers; standard CMOS process; uncooled infrared detector

1. Introduction

Uncooled thermal imaging focal plane arrays (FPAs) have attracted worldwide attention and become a dominant technology for commercial thermal imaging applications such as scientific research, medical imaging, even consumer electronics, and automotive assisted driving [1–5] due to the low cost, small size, light weight, and high reliability. Nowadays, the thermosensitive devices in most mass-produced uncooled FPAs [6,7] are vanadium oxide (VOx) [8–10] or amorphous silicon (α-Si) microbolometers [11–14]. Although the VOx/α-Si microbolometers dominate the commercial market due to their high sensitivity [15,16], the complex fabrication process of these bolometers based on microelectromechanical systems (MEMS) and the need for specific production lines limit their large-scale use in the civilian field.

Microbolometers based on standard complementary metal oxide semiconductor (CMOS) processes have the attractive advantages over VOx/α-Si bolometers, such as they can integrate both detectors and readout circuits and achieve outstanding uniformity that other technologies cannot achieve [17]. The microbolometer employed p+-active/n-well diode is designed using a standard 0.35 μm CMOS process and a simple post-CMOS process [18,19]. The responsivity of 4970 V/W at 20 μA bias is measured with a detectivity of 9.7×10^8 cmHz$^{1/2}$/W and a thermal time constant of 35.8 ms. Moreover, an n-well resistive detector having a detectivity of 8.9×10^8 cmHz$^{1/2}$/W and a thermal time constant of 21 ms is prepared using the same process [20]. However, since the n-well is easily etched by the subsequent post-CMOS process, the performance of such a detector is unstable, and the uniformity thereof is poor. In recent years, an infrared microbolometer composed of

an umbrella-like absorber and a snake-like structure embedded with a thermocouple has been proposed [21] and prepared using the TSMC (Taiwan Semiconductor Manufacturing Company Limited) 0.18 μm standard CMOS process and the in-house post-CMOS process, which has a responsivity of 885.9 V/W, detectivity of 9.5×10^7 cmHz$^{1/2}$/W, and thermal time constant of 26 ms. However, it cannot exhibit better performance due to the weak Seebeck effect. In order to further improve the detector performance, an absorber having plasmonic metamaterial is integrated into the thermoelectric infrared sensor [22]. As a result, a detectivity of 6.13×10^8 cmHz$^{1/2}$/W can be reached. According to the preceding description, while the microbolometers can be fabricated by standard CMOS process, their detectivity is lower than that of VOx/α-Si microbolometers (~10^9) [23] due to the poor sensitivity of the material to infrared radiation. Therefore, for CMOS-based infrared detectors, it is of great significance to explore and find a kind of thermal sensitive materials that can improve the performance of detectors in the standard CMOS process.

In this paper, a microbolometer employing salicide polysilicon as the thermistor is designed and fabricated using a standard 0.18 μm CMOS process and is compared with an Al microbolometer fabricated by a similar process. Through simulation and experiment, the transient temperature rise, thermal conductance, temperature coefficient of resistance, voltage responsivity, detectivity, and thermal time constant are thoroughly studied. The experimental results reveal that the salicide polysilicon material is more suitable for microbolometers based on the standard CMOS process because of its high resistivity and low thermal conductivity. The results can serve as a useful practical and theoretical reference for the development of standard CMOS infrared detectors in the future.

2. Structural Design and Fabrication

2.1. Structural Design

Figure 1 shows a schematic diagram of the proposed microbolometer structure, which utilizes fully compatible materials (substrate Si, poly-Si, SiO_2, Al) and design rules for the standard CMOS process. As shown in the isometric view in Figure 1a, the microbolometer includes an absorber supported by two serpentine legs, a thermistor, and a thermally isolated cavity located at the bottom of the absorber. The absorber and the supporting legs are mainly made of SiO_2, which is served as dielectric layers in the CMOS process. The thermally isolated cavity is prepared by a simple post-CMOS process, and its main function is to prevent the heat conduction between the absorber and the Si substrate so as to achieve the purpose of increasing the temperature rise of the absorber. The thermistors of the proposed microbolometer can be designed as salicide polysilicon or metal Al layers. The proposed microbolometer stacks of metal, SiO_2, and poly-Si layers are shown in the cross-section views in Figure 1b,c, in which the red dotted lines are chosen to indicate the location of the thermistor. Furthermore, the thermistor is designed to be serpentine in order to increase the resistance of the thermistor as much as possible in the same area, thereby improving the output electrical signal. The microbolometer works by absorbing external infrared radiation through the absorber and converting it into heat, which changes the temperature of the absorber and the resistance value of the thermistor, resulting in an electrical signal that is read out by the circuit adjacent to it.

The absorption spectrum of the absorber in the range of 7–13 μm is simulated by Lumerical FDTD (finite-different time-domain) solutions software produced by Lumerical Solutions Company in Canada, and the results are shown in Figure 2a. As can be seen from the figure, there are strong absorption regions in three wavelength ranges, specifically 7.5–8.5 μm, 9.5–10.2 μm, and 11.5–13 μm, which correspond to the absorption region of SiO_2 to infrared radiation [24,25]. At a wavelength of 10.2 μm, the absorptivity can be as high as 78%. Based on the finite element method, the transient thermal properties of the microbolometer structures are numerically simulated by Ansys workbench software. The thermal parameters of SiO_2 in the simulation are the density of 2200 kg/m^3, the thermal conductivity of 1.4 W/m·K, and specific heat of 730 J/kg·K. The metal Al has a density of 2689 kg/m^3, a thermal conductivity of 237 W/m·K, and specific heat of 951 J/kg·K. The

above values are from the materials database of Ansys workbench simulation software. In order to calculate the temperature rise and evaluate the thermal conductance and thermal time constant of the microbolometer, a uniformly distributed heat power of 14 nW is applied to the surface of the SiO_2 absorber, and the simulated environment is a vacuum. In addition, the initial temperature and boundary conditions at the ends of the two supporting legs are set to 300 K. The transient temperature profile obtained from the Ansys workbench simulation is shown in Figure 2b and can be represented by the following Equation (1):

$$\Delta T(t) = \frac{\eta P}{G_{eff}}[1 - \exp(-t/\tau)] = \Delta T_s[1 - \exp(-t/\tau)] \quad (1)$$

where η is an average absorptivity, P is the power of infrared radiation irradiated on the sensor, G_{eff} is the effective thermal conductance, and t and τ are the simulated time and the thermal time constant, respectively. ΔT_s is the temperature rise at a steady state. The transient thermal simulation and the fitted results by Equation (1) are shown in Figure 2b. It is distinctly that the temperature rise of the salicide polysilicon microbolometer is significantly higher than that of the microbolometer using metal Al as the thermistor. In addition, it can be seen from the graph that the temperature rise of the metal Al microbolometer gradually tends to be stabilized and eventually reaches 18.5 mK when the time is greater than 50 ms, while the temperature rise of the salicide polysilicon microbolometer gradually tends to be stabilized and finally reaches 48.3 mK when the time is greater than 150 ms. According to the fitted data, the thermal time constants of the salicide polysilicon microbolometer and the metal Al microbolometer are 34.2 ms and 11.5 ms, respectively, and the thermal conductances are 2.90×10^{-7} W/K and 1.25×10^{-6} W/K, respectively. The metal Al microbolometers are known to have a fast responsivity speed because they have metal Al wires with higher thermal conductivity in the support legs.

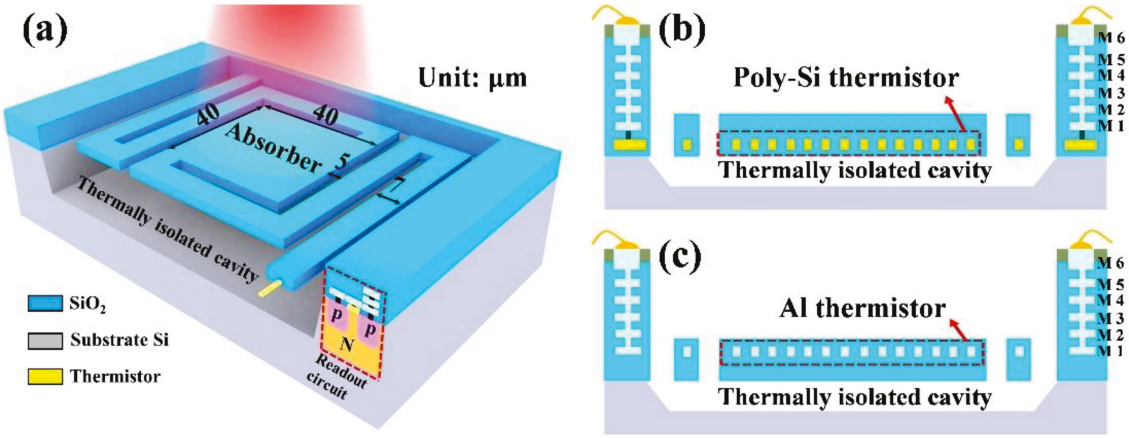


Figure 1. (**a**) 3D schematic illustration of the proposed microbolometer using 0.18 μm standard CMOS technology. The cross-section views of the suggested microbolometer with (**b**) salicide polysilicon thermistor and (**c**) metal Al.

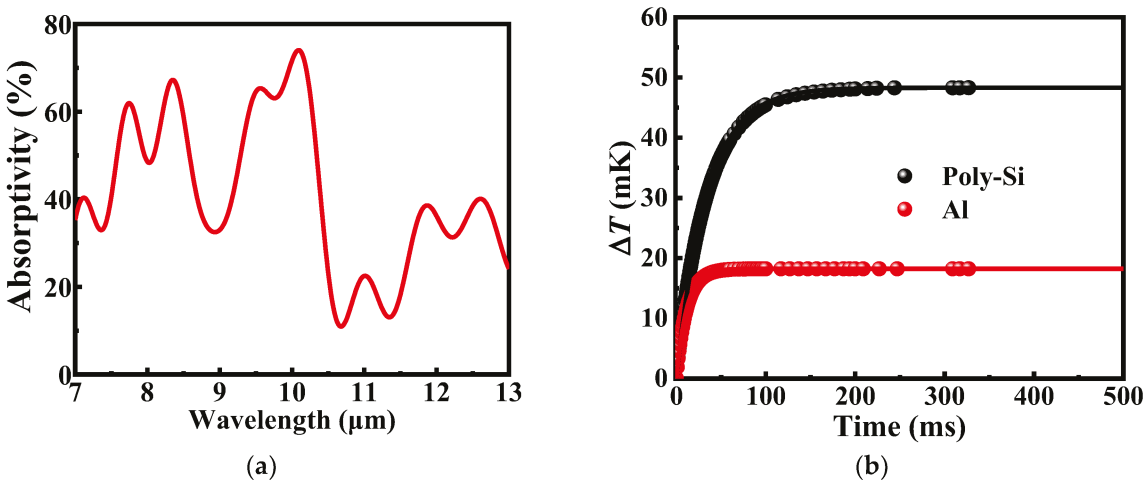


Figure 2. (**a**) the simulated absorption spectra in the range of 7–13 μm of both microbolometers by FDTD software, (**b**) the simulated temperature rises of microbolometer as a function of time by Ansys workbench software. The curves represent the fitting result of simulated data by Equation (1).

2.2. Structural Fabrication

A series of cross-sectional schematic diagrams representing the fabrication process flow of the proposed microbolometer is shown in Figure 3. The basic chip structure in Figure 3a is fabricated using a 0.18 μm standard CMOS process, in which a polysilicon layer, the SiO_2 dielectric layer, a metal Al layer, and a Si_3N_4 passivation layer are prepared and patterned by a foundry. The thermistors represented by yellow can be made of polysilicon or metal Al layer. The main role of the metal Al layer represented by gray in this structure is to act as a mask in the subsequent simple post-CMOS process. The structures that have undergone different post-CMOS processes are shown in Figure 3b–d. Firstly, the basic structure is etched by an inductively coupled plasma (ICP) with C_4F_8 gas, in which process the metal Al is used as a hard mask to protect and define the shape of the microbolometer. The etching process will continue until the window for etching the Si substrate is fully exposed, and the Si_3N_4 and SiO_2 located in the upper part of the Al mask have been completely removed during this process, as illustrated in Figure 3b. After that, the chip is immersed in a tetramethyl ammonium hydroxide (TMAH) solution containing Si powder and $(NH_4)_2S_2O_8$ for wet etching to remove Si at the bottom of the absorber, and thereafter, the Si substrate is subjected to anisotropic etching to form a trapezoidal etching cavity, and the detector is separated from the Si substrate, as shown in Figure 3c. Finally, the metal Al mask is removed cleanly by ICP etching using a mixture of BCl_3 and Ar gas, and the final microbolometer structure is completed, as shown in Figure 3d. Figure 3e,f show optical micrographs of the fabricated polysilicon microbolometer and metal Al microbolometer, respectively. Both the microbolometers have clear edges, complete structures, good hanging conditions, intact support arms, and no obvious deformation. The thermally isolated cavity from which the detector is removed is trapezoidal and angular, as shown in Figure 3g. These characteristics indicate that the two microbolometers with the thermally isolated cavity are effectively constructed and have a prominent shape and durability.

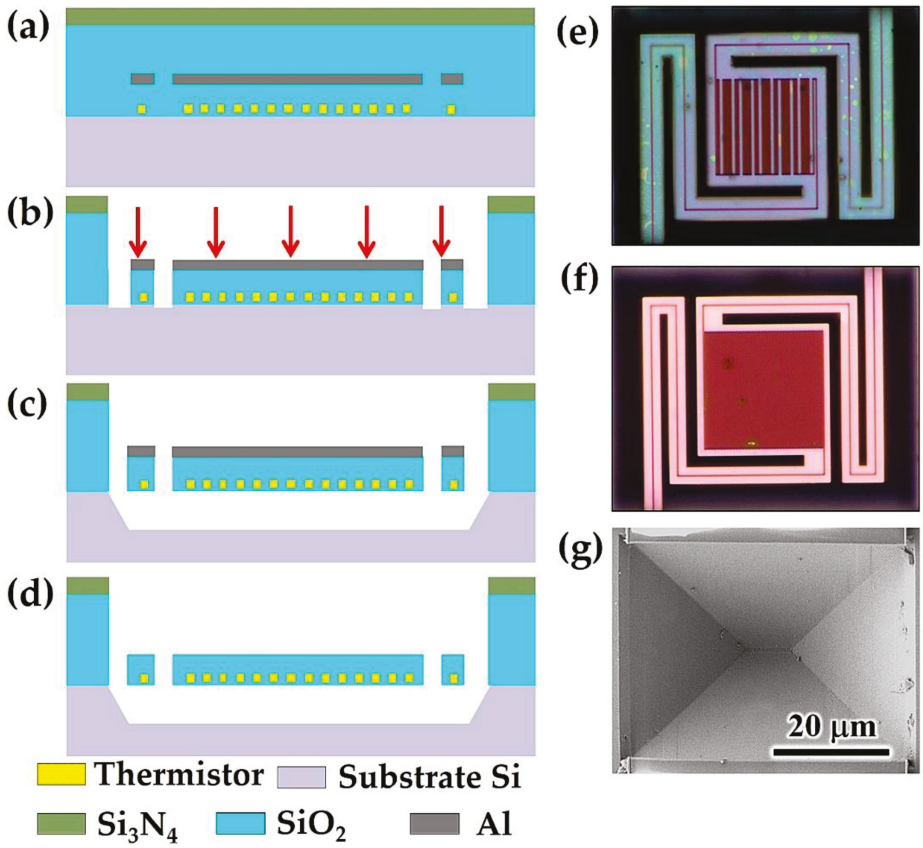


Figure 3. The fabrication processes and images of the proposed IR sensor, (**a**) the CMOS chip prepared by a standard 0.18 μm CMOS processes, (**b**) Si_3N_4 and SiO_2 dry etching by ICP using the C_4F_8 gas, (**c**) the Si substrate wet etching using the TMAH solution with Si powder and $(NH4)_2S_2O_8$ to suspend the detector structure for thermal isolated, and (**d**) the metal Al mask layer etching using the mixture of BCl_3 and Ar gases, the suspended (**e**) salicide polysilicon microbolometer and (**f**) metal Al microbolometer after post-COMS process, (**g**) the thermally isolated cavity at the bottom of the microbolometer that separated from the Si substrate.

3. Experimental Results and Discussions

To obtain the temperature coefficient of resistance (TCR), the resistance values of the microbolometers are measured every 10 °C in the range of 0–40 °C. The variation of the resistance R with the temperature rise ΔT for the microbolometer can be expressed as the following Equation (2).

$$R = R_r \alpha \Delta T + R_r \tag{2}$$

where α is the TCR of the salicide polysilicon material, and R_r is the resistance of the thermistor at room temperature. The measured results of the salicide polysilicon microbolometer and the metal Al microbolometer are shown in Figure 4. It can be seen that the resistances of the two microbolometers gradually increase as temperature increases, which indicates that the resistances of the two microbolometers exhibit a very good linear change with the temperature, respectively. The TCRs for the salicide polysilicon microbolometer and the metal Al microbolometer can be obtained from the fitted results by Equation (2), and they are 0.35% and 0.37%, respectively.

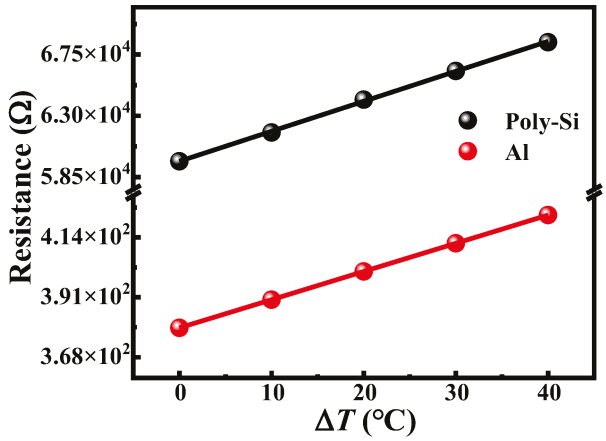


Figure 4. Variation of resistance of design salicide polysilicon and metal Al microbolometers with temperature difference range of 0–40 °C. The lines represent the linear fitting results by Equation (2).

The effective thermal conductance G_{eff}, which directly affects the performance of the microbolometer, is investigated further by measuring the resistance change in the vacuum caused by the self-heating effect of the bias current. The relationship between the resistance and effective thermal conductance can be expressed by the following Equation (3) [21]:

$$\frac{1}{R} = \frac{1}{R_r} - \frac{\alpha}{G_{eff}} {I_b}^2 \tag{3}$$

where G_{eff} is the effective thermal conductance, I_b is the bias current. Figure 5 shows the inverse of the resistance measured in the vacuum chamber as a function of the square of the bias current. It can be found that the measured experimental data can fall on the fitted straight line represented by Equation (3). The fitted results of Figure 5a estimate the G_{eff} of the salicide polysilicon microbolometer to be 3.45 × 10^{-7} W/K, while the value of the Al microbolometer (Figure 5b) is 1.53 × 10^{-6} W/K, which are extremely similar to the simulation results of 2.90 × 10^{-7} W/K and 1.25 × 10^{-6} W/K, respectively.

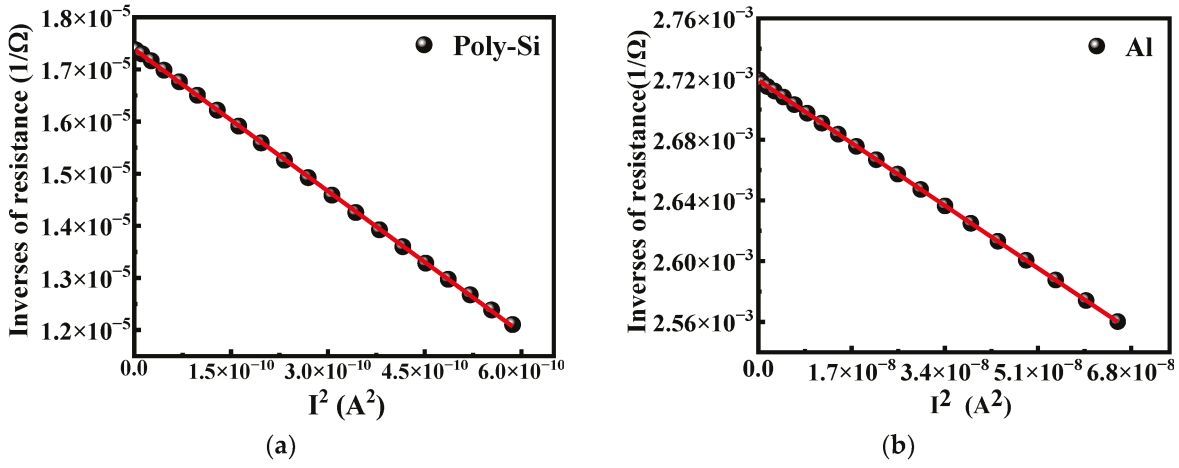


Figure 5. The inverse of the resistance as a function of square of the bias current measured in vacuum condition of (**a**) salicide polysilicon and (**b**) metal Al microbolometers. The line represents the linear fitting by Equation (3).

Figure 6 shows the voltage responsivity of the microbolometers as a function of bias current. The graphs show that the voltage responsivity increases linearly with increasing bias current for both the salicide polysilicon microbolometer (Figure 6a) and the metal Al microbolometer (Figure 6b). The difference is that the salicide polysilicon microbolometer can

have a higher voltage responsivity at a lower bias current, while the metal Al microbolometer still has lower voltage responsivity than the salicide polysilicon microbolometer even at a large bias current. The fundamental reason for this is that the resistance of metal Al is two orders of magnitude lower than that of salicide polysilicon, and the thermal conductance of the former is also much higher than that of the latter.

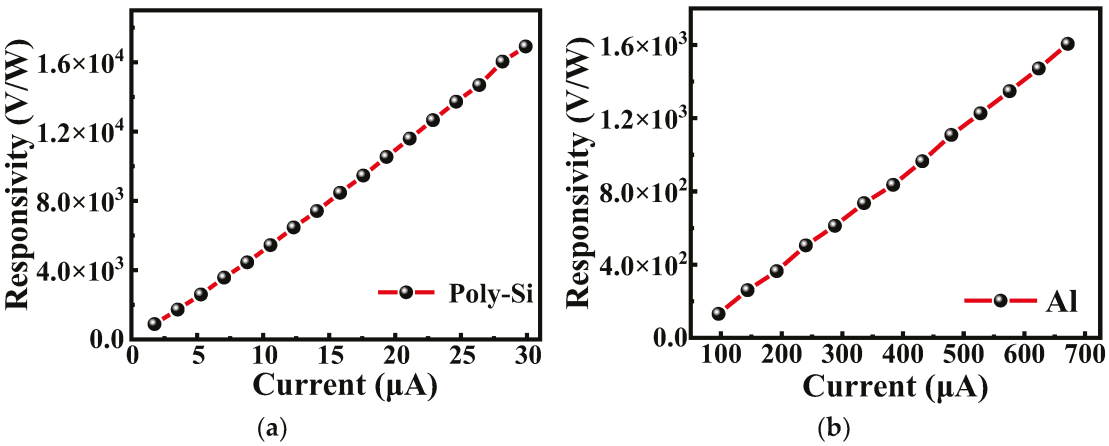


Figure 6. The responsivity as a function of bias current of (**a**) salicide polysilicon microbolometer and (**b**) metal Al microbolometer.

Figure 7 shows the voltage noise power spectral density (NPSD) of the microbolometers measured under vacuum pressure less than 5 Pa in the frequency range from 1 Hz to 100 kHz. The polysilicon microbolometer has a continuous $1/f$ noise ranging from 1 Hz to 1000 Hz [26,27], and the noise power spectral density remains almost constant when the frequency range is larger than 1000 Hz, which means that the noise is mainly thermal noise independent of frequency, as shown in Figure 7a. As shown in the inset of Figure 7a, as the current increases from 1.7 μA to 26 μA, the noise voltage V_n of the salicide polysilicon microbolometer increases from 3.23×10^{-6} V to 4.22×10^{-6} V, and the magnitude of the increase gradually as the bias current increases. Figure 7b shows that the noise of the metal Al microbolometer is mainly $1/f$ noise in the frequency range of 1 to 100 kHz, and this noise increases significantly with the increase of the bias current. The inset of Figure 7b shows that the value increases from 4.2×10^{-7} V to 1.6×10^{-6} V when the current is increased from 95 μA to 680 μA. In addition, with the increase of the current, the magnitude of the increase of the noise voltage is more obvious than that of the salicide polysilicon microbolometer.

The detectivities D^* of the salicide polysilicon microbolometer and the metal Al microbolometer can be calculated [28] using the experimental data of voltage responsivity R_v and noise voltage V_n at the same bias current, and the results are shown in Figure 8a,b. As the bias current increased, the detectivities of the two microbolometers both first increased and then decrease. The detectivity of the salicide polysilicon microbolometer reaches a maximum value of 1.78×10^9 cmHz$^{1/2}$/W at a bias current of 25 μA, while the detectivity of the metal Al microbolometer reaches a maximum value of 6.2×10^8 cmHz$^{1/2}$/W at a bias current of 267 μA. The reason why the salicide polysilicon microbolometer is able to achieve a higher detectivity compared to the metal Al microbolometer is because the polysilicon thermal material has superior voltage responsivity compared to metal Al material due to its larger resistance and lower thermal conductivity.

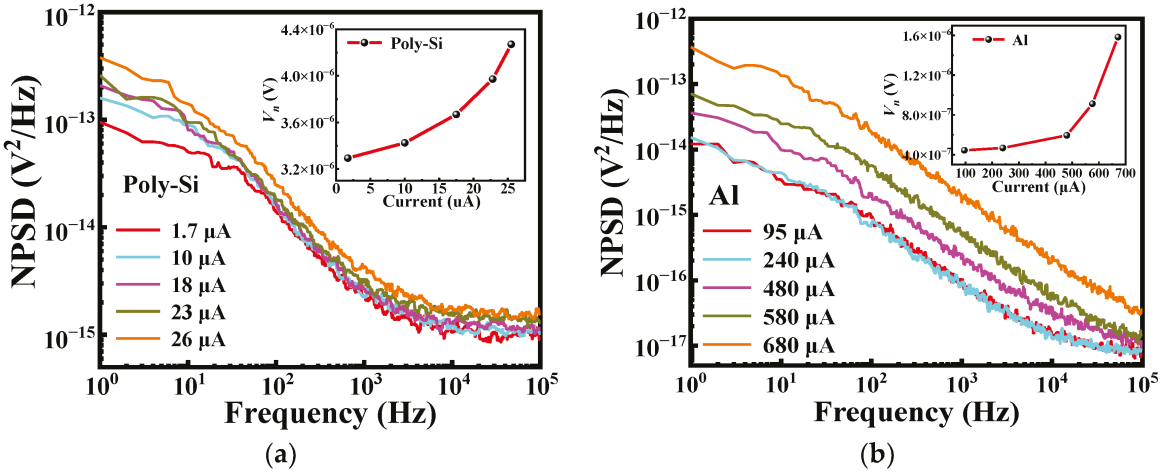


Figure 7. The noise power spectral density of (**a**) the salicide polysilicon microbolometer and (**b**) metal Al microbolometer under the vacuum condition at different bias currents. The inset shows bias currents dependence noise voltage of under the bandwidth of 10 kHz.

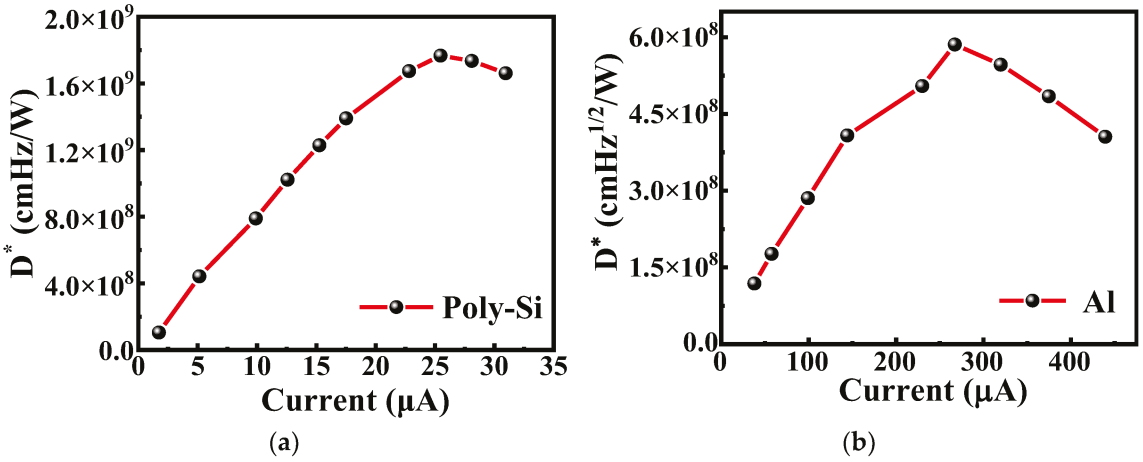


Figure 8. Evaluated detectivity of (**a**) the salicide polysilicon microbolometer and (**b**) metal Al microbolometer under various bias currents.

Figure 9 shows the voltage responsivity as a function of chopping frequency for determining the thermal time constant of the two microbolometers. The R_v of the salicide polysilicon microbolometer decreases gradually from 3.63×10^4 V/W to 1.5×10^4 V/W as the chopping frequency increases from 4 Hz to 150 Hz. However, the voltage responsivity of the metal Al microbolometer dropped significantly after 10 Hz, decreasing gradually from 1.02×10^3 V/W to 1.31×10^2 V/W. The experimental data are fitted by the line representing the equation of reference [29], and the thermal time constants of 36.7 ms and 10.2 ms can be obtained. These values are substantially close to the simulated values of 34.2 ms and 11.5 ms for the silicide polysilicon microbolometer and the metal Al microbolometer, respectively. The small difference between them is due to the testing environment being a non-ideal vacuum environment.

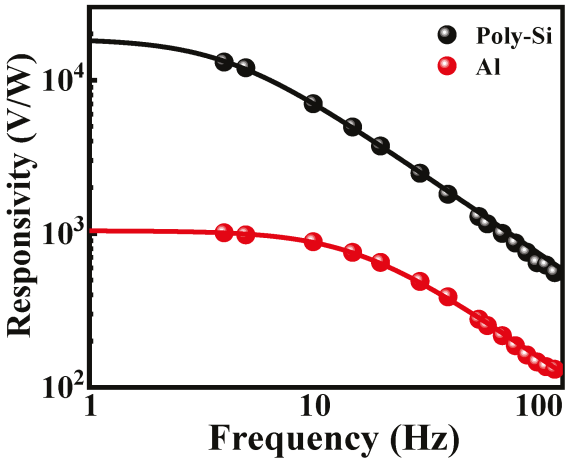


Figure 9. The responsivity measured in vacuum of the salicide polysilicon and metal Al microbolometer concerning modulation frequency.

Although the metal Al microbolometer has a faster response speed from the perspective of the thermal time constant, salicide polysilicon has obvious advantages in improving the performance of microbolometers. The voltage responsivity and detectivity of the microbolometer can be expressed by Equations (4) and (5):

$$R_v = \frac{I_b R \alpha \eta}{G_{eff}} \tag{4}$$

$$D* = \frac{R_v \sqrt{A_d \Delta f}}{V_n} \tag{5}$$

where the A_d is a photosensitive area of the microbolometer, and Δf is electrical bandwidth. The V_n is the noise voltage of the microbolometer mainly comes from the thermal noise when the thermistor works, which can be expressed by the following Equation (6):

$$V_n = \sqrt{4KTR\Delta f} \tag{6}$$

where the K is the Boltzmann constant of 1.38×10^{-23} J/K, T is the working temperature of 300 K. Then, the Equations (4) and (6) are brought into Equation (5) to get the final detectivity formula as:

$$D* = \frac{I_b \sqrt{R}}{G_{eff}} \cdot \frac{\alpha \eta}{2} \sqrt{\frac{A_d}{KT}} \tag{7}$$

In which, the η, A_d, K, and T of two microbolometers are the same constant because their structures and working conditions are identical. In addition, the α of salicide polysilicon and metal Al are 0.35% and 0.37%, respectively, and their difference is very small, so they can also be approximately regarded as equal. Thus, it can be found that when the I_b is the same, the D^* is proportional to $\sqrt{R}$, and inversely proportional to G_{eff}. In this study, compared with the Al microbolometer, the R of the polysilicon microbolometer is significantly greater (Figure 1) and G_{eff} is significantly smaller (Figure 2). Although the I_b has increased to 267 μA of Al microbolometer in the experimental test, its voltage responsivity and detectivity are still not as high as those of the polysilicon microbolometer, which are measured at a bias current of 25 μA. From this, it can be known that salicide polysilicon not only has high resistivity but also has the advantage of low thermal conductivity, which means that it can obtain a higher voltage responsivity under the condition of a smaller bias current. A smaller bias current is beneficial to the design of low-power readout circuits, and a larger voltage responsivity is beneficial to the extraction of infrared radiation signals. Furthermore, the polysilicon of the microbolometer is wrapped by SiO_2 compared with the P^+/n-well microbolometer [18], which makes it unaffected by etching

in the post-CMOS process and can maintain better stability and uniformity. Compared with thermocouple microbolometers [21], the microbolometers used salicide polysilicon as a thermistor can more easily obtain higher detectivity. A more detailed comparison of the microbolometer with other types of detectors is described in the previous work [29]. From the above discussion, it can be known that the salicide polysilicon is more suitable for preparing uncooled infrared detectors based on standard CMOS processes.

4. Conclusions

The microbolometers with salicide polysilicon and metal Al as a thermistor, respectively, are designed and fabricated by a standard 0.18 μm CMOS process and simple post-CMOS process. According to the simulation results, the temperature rise of the microbolometer with salicide polysilicon as a thermistor can reach 48.3 mK, but the temperature rise of the microbolometer with metal Al as a thermistor is only 18.5 mK. The experimental results show that the polysilicon microbolometer can achieve a detectivity of 1.78×10^9 cmHz$^{1/2}$/W at 25 μA, while the metal Al microbolometer only achieves the best detectivity of 6.2×10^8 cmHz$^{1/2}$/W even at a high bias current of 267 μA due to its low resistance value and high thermal conductivity. The salicide polysilicon microbolometers are more suitable for thermistors of uncooled infrared detectors based on the standard CMOS process because they have larger resistance and lower thermal conductivity, enabling them to achieve a greater detectivity at a lower bias current.

Author Contributions: Y.G. is responsible for the design of the microbolometers, the simulation in this paper, and the writing of the paper; H.M. and J.L. are responsible for data testing and collection; Y.L. and X.J. are responsible for revising the paper. All authors have read and agreed to the published version of the manuscript.

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Article

Selective Sensing of Mixtures of Gases with CMOS-SOI-MEMS Sensor Dubbed GMOS

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Abstract: The need to achieve digital gas sensing technology, namely, a technology to sense and transmit gas-enabled digital media, has been recognized as highly challenging. This challenge has motivated the authors to focus on complementary metal oxide semiconductor silicon on insulator micro electro-mechanical system (CMOS-SOI-MEMS) technologies, and the result is a new pellistor-like sensor, dubbed GMOS, with integrated signal processing. In this study, we describe the performance of such sensors for the selective detection of mixtures of gases. The novel key ideas of this study are: (i) the use of the GMOS for gas sensing; (ii) applying the Kalman filter to improve the signal-to-noise ratio; (iii) adding artificial intelligence (AI) with tiny edge approach.

Keywords: MEMS; gas sensor; SOI; MOS; data analytics; classification; machine learning; tinyML; Kalman filtering

1. Introduction

In recent years, the need for mobile, low cost, and low power gas sensors has increased dramatically. Such gas sensors are needed for safety in homes and cars, monitoring air quality, the wellbeing of people, as well as industrial process control and precision agriculture. In practice, all these applications require data logging and, hence, digital sensing systems become essential.

The need to achieve digital gas sensing technology, namely, a technology to sense and transmit gas-enabled digital media (such as pictures and music) has been recognized as highly challenging. This challenge has motivated the authors to focus on CMOS-MEMS (micro electro-mechanical system) technologies, and the result is a new pellistor-like sensor, dubbed GMOS. Since the first report in 2018, several papers describing GMOS have been reported by the same group [1–6].

The main uniqueness of the GMOS sensor is its ability to detect selectively different gases. Selectivity is achieved by measuring a fundamental physical property—heat of exothermic reaction and ignition temperature, instead of measuring relative changes of resistance, as in metal oxide semiconductor gas sensors [1]—thus enabling selectivity (see Section 3).

Currently, no commercial devices, apart from bulky and expensive gas chromatographs, can selectively detect ethanol and acetone in mixtures. The compact commercial ethanol and acetone sensors are, in fact, the TVOC (total volatile organic compound) sensors that detect all these compounds together, for example, SPG40—Sensirion [7], ZMOD4410—Renesas [8], based on MOX chemiresistors, and MiniPID 2WR—Ionsense, based on the photo-ionization principle [9]. Among the research papers, there were few attempts to measure ethanol selectively, however, the selectivity of ethanol measurement was not evaluated relative to acetone [10,11]. Table A1 compares GMOS with the commercial sensors. The values are taken from the datasheets of the commercial products.

In real-life applications, there is an even more challenging task: to selectively measure mixtures of gases. This study focuses on applying the Kalman filter [12–17] to improve the signal-to-noise ratio, and subsequently, to add tiny edge machine learning to enable better analysis of gas mixtures.

Section 2 describes the role of the CMOS-SOI-MEMS technology towards high-perform ance infra-red (IR) sensing systems based on thermal sensors. Section 3 describes the role of the CMOS-SOI-MEMS technology towards a digital gas sensing system. Section 4 describes the role of the Kalman filter in improving the signal-to-noise ratio. Finally, the tiny edge revolution [18,19], which makes the GMOS smarter by applying machine learning (ML) techniques based on the tiny edge ML, is briefly described.

2. The Role of CMOS-SOI-MEMS Fabrication Technology for Uncooled Thermal Sensors

Since the 1980s, the CMOS (complementary metal oxide semiconductor) has remained the dominant microelectronic technology for well established advantages. CMOS technology maintains the essential advantages of low power consumption, high noise tolerance, wide operating voltage, and operating temperature range. Furthermore, it rapidly and continuously improves the integration degree and intrinsic speed. Therefore, CMOS technology has become the most important technology in VLSI (very large scale integration) [20].

CMOS MEMS (micro-electric mechanical systems) are micro-machined systems in which MEMS devices are integrated with CMOS circuitry on a single chip to enable miniaturization and performance improvement. With the advancement of both CMOS and micromachining technologies, CMOS MEMS have also evolved tremendously in recent years [21].

The CMOS-SOI-MEMS technology, which includes a buried oxide layer (SOI), enables wafer level processing and packaging in a standard CMOS-SOI FAB. Metallization layers provide built-in masks for MEMS processing. The back-side handle is removed by deep reactive ion etch (DRIE), and the buried oxide (BOX) layer provides an etch stop. Front-side dielectric layers are removed by RIE, while front-side metal masks are removed by etching. With this method, a thermally insulated transistor is achieved. The CMOS-SOI-MEMS unique technology provides good alignment, which is determined by CMOS-SOI technology (1 μm in the present study), and there is no need for expensive masks. This technology has already enabled thermal IR sensors, dubbed digital TMOS (thermal MOS) [22,23]. The excellent performance of digital TMOS in terms of linearity, reproducibility, and accuracy, while achieving low-power and low-cost performance, is also attributed to the CMOS-SOI-MEMS technology. Extending this approach to digital gas sensing (dubbed GMOS) is currently under extensive development by the authors [1–6].

3. GMOS Design and Operation Principles Based on CMOS-SOI-MEMS

The key element—GMOS multi-gas sensor—is a product of modern VLSI microelectronics, MEMS, nanomaterials, computer algorithms, machine learning, and wireless communication. The GMOS design and operating principles are described in detail in references [1–6]. Here, we review the innovation and the unique property of selectivity.

The breakthrough innovation is in implementation of the suspended MEMS-TMOS transistor for detection of very low gas concentrations. The transistor is integrated with a reaction micro-hotplate covered by catalytic nanoparticles on which exothermic combustion reaction of gas molecules takes place. Such a transistor can detect tiny changes in temperature caused by the exothermic gas reaction. As a result, our sensor demonstrates very high sensitivity and the ability to detect sub-ppm concentration of ethylene, ethanol, and other gases.

Exploiting this fact, that each gas has a specific ignition temperature, and measuring signal/temperature characteristics, our sensor demonstrates excellent selectivity to ethylene in the presence of other gases, which makes it competitive over all existing commercial gas

sensors. Fabricated using matured VLSI technology, GMOS offers low price and consumes low power.

4. Application of Kalman Filter to Improve the Signal to Noise Ratio of the GMOS—Illustrating Experimental Results

4.1. Introduction to Estimation Theory and the Kalman Filter

Noise is an integral part of life, which sets a fundamental limit on all electronic circuits and systems operation. Most of the processes are random and not deterministic. Random processes and noise in general are pattern-less, but not property-less [24]. Hence, one good method is the use of estimation theory to analyze data measurements taken from a system.

In particular, optimal estimation theory deals with the development of optimal estimators or algorithms to provide an updated optimal estimate of the system's state being observed using new measurements (data) [12,16].

The Kalman filter is one of the most important estimation algorithms. It helps produce estimations of the state of the system. Additionally, it may be applied for both static and dynamic systems (whereas the system changes or not over time), as well as both stationary and nonstationary environments. The Kalman filter approach includes the generalization of the system into a mathematical model to obtain the optimal state, enabling the prediction of the future system based on past estimations and reducing the noise in the measured value. Generally, the algorithm has a smoothing effect on the system's measurements, which converge toward the true value. The algorithm requires only the last estimation for each iteration, thus minimizing memory requirements, which also makes the filter suited for real-time systems [12–17].

GMOS, our gas sensor, changes I–V characteristics based on the gas reactions. Our given signal (i.e., voltage measurement) is noisy (electrical circuits, the sensor itself, etc.). The Kalman filter may help provide more accurate and precise real-time estimations, taking the different random noises into account.

This paper focuses on improvements, which were made to GMOS, but a brief, simple mathematical explanation will be given. There are several fundamental equations that define Kalman filters.

As each time sample is taken, the state update equation defines the filtered output.

$$\begin{cases} \hat{X}_n = \hat{X}_{n-1} + K_n \cdot \left(Z_n - \hat{X}_{n-1}\right) = (1 - K_n) \cdot \hat{X}_{n-1} + K_n \cdot Z_n \\ 0 \le K_n \le 1 \end{cases} \quad (1)$$

The equation states that the new filter estimation, $(\hat{X}_n)$, is the previous one, $(\hat{X}_{n-1})$, plus the difference between the new measurement, (Z_n), and the previous estimate, multiplied by a weight factor, K_n ('Kalman gain'). Generally, the Kalman gain tends to be higher when the measurement uncertainty (the variance of the measurements errors, the differences between the measurements, and the true values) is low and the estimate uncertainty (estimation of the difference between the true values and the filter estimates) is high, and vice versa. Usually, Kalman gain tends to decrease as the quantity of the measurements increases. The filter, therefore, 'prefers' new measurements at the start, but as the estimate becomes more accurate, new measurements have less impact (if the estimate does not match the measured values, the Kalman gain will become larger). We also used the following equations:

$$\begin{cases} K_n = \frac{p_{n-1}}{p_{n-1}+r} \\ p_n = (1 - K_n) \cdot p_{n-1} + \left|Z_n - \hat{X}_n\right| \cdot q \end{cases} \quad (2)$$

where p_{n-1} is the extrapolated estimate uncertainty, r is the measurement uncertainty, and q is the process noise. The estimate error represents the difference between the true values and the estimates. On the contrary, the measurement uncertainty, r, represents the difference between the true values and the measurements. The measurement error

is random, hence, it may be described by a variance. The parameter q represents the uncertainty of the model (system noise). Both q and r are given as inputs to the algorithm.

One should know that the filter performance also depends on the input noise parameters (q and r). If the latter are wrong, the accuracy of the filtering might be reduced. Furthermore, inaccurate estimations may continue to accumulate, therefore, the user will continue to receive inaccurate results.

4.2. Experimental Results

As explained above, Kalman filter helps improve the SNR (signal-to-noise ratio), as may be seen in Figure 1.

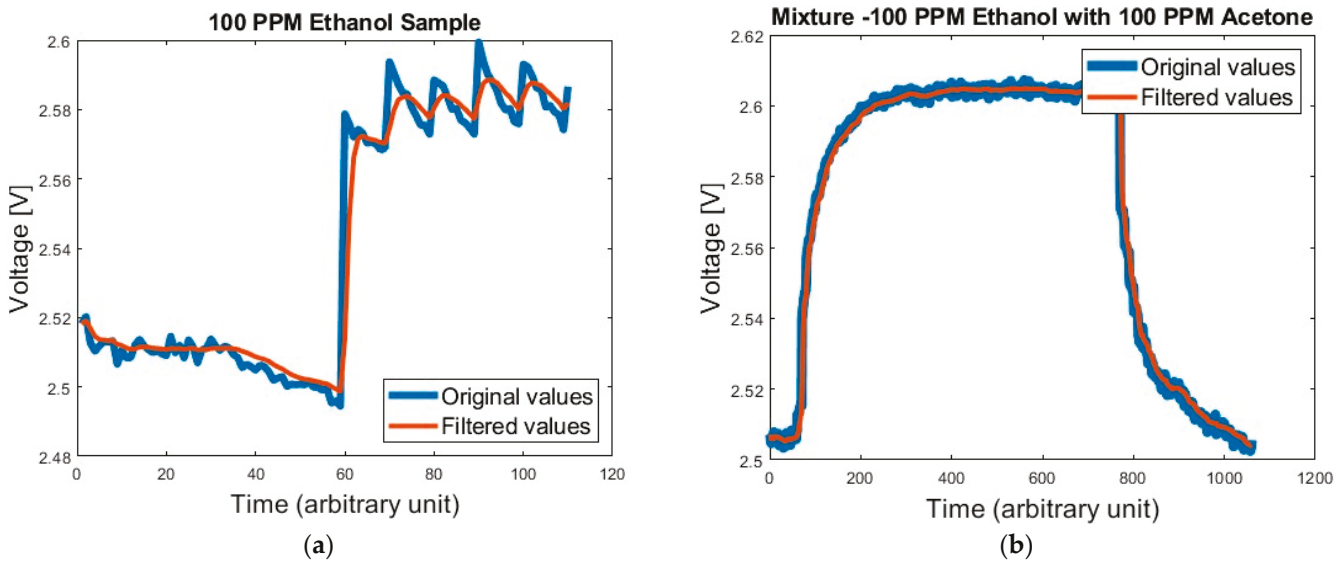


Figure 1. Examples to the readout improvements made by the Kalman filter. The original data and the filtered data may be seen. The filtered output is smoother and more resistant to noise. (**a**) 100 PPM Ethanol. (**b**) A mixture of 100 PPM ethanol and 100 PPM acetone.

As may be seen, after applying the Kalman filter, the output is smoother and less affected by noise. The filtered output might have a slight delay (of the order of ~2 s) compared to original data. Even so, those delays do not harm GMOS performance.

5. TinyML for Gas Classification

Machine learning (ML) is the use of algorithms that are capable of learning and adapting. The resource-intensive nature of ML is one of its major problems. For neural networks, for instance, large training sets and great computer power are usually required. Thus, there is a potential for ML solutions in small and resource-constrained systems and edge devices [18]. An emerging subfield of machine learning called tinyML, combines embedded systems with machine learning. Devices can run ML applications addressing power and resource constraints (while no data is transmitted to the cloud).

To improve GMOS ability of gas analysis (in real-time), which includes both gas types, as well as gas concentrations, we added a pre-trained neural network, which is written to an Arduino controller [19]. The system is shown in Figure 2.

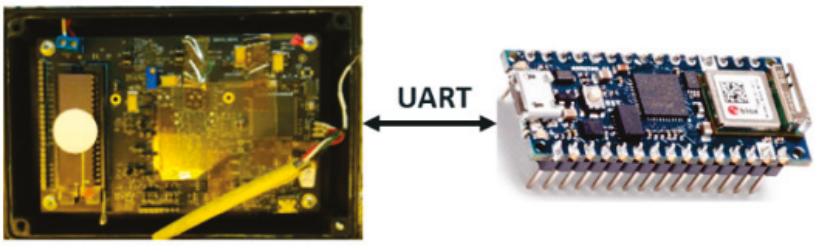


Figure 2. A schematic depiction. An Arduino controller requesting samples from GMOS over UART.

The neural network was trained using GMOS measurements, mainly the voltage measurements, of different gas types (acetone and ethanol). UART (universal asynchronous receiver transmitter) is used to communicate between the Arduino controller and GMOS. The process includes the controller requesting data from GMOS, data pre-processing, and feature extraction (which later are transmitted as inputs to the neural network). Having a preprocessing data block is crucial, since measurements are always relative to a reference voltage (prior to gas insertion). As a result, we prefer to make sure that all raw data has an equal initial voltage, thus improving the performance of our system.

The preliminary neural network includes three classes (possible gas classifications):

- Ethanol—100 PPM
- Acetone—100 PPM
- None of above (no gas was inserted)

For this task, we achieved 100% success on our test set, as our samples were perfectly classified that may be seen in Figure 3. For our system, the current added latency is 1 ms.

	ACETONE	ETHANOL	NOGAS
ACETONE	**100%**	0%	0%
ETHANOL	0%	**100%**	0%
NOGAS	0%	0%	**100%**
F1 SCORE	1.00	1.00	1.00

Figure 3. The confusion matrix. Using tinyML, we were able to correctly classify the test set.

We are currently expanding the system, adding more gas types (also as mixtures, as was shown before), as well as different concentrations.

6. Conclusions

This paper presents GMOS's ability to detect selectively different gases while being updated by more algorithms to enable better real-time analysis of gases. This ability, selectivity, differs GMOS from other sensors in the market. The GMOS technology, CMOS-SOI-MEMS, enables low-power and low-cost operation while maintaining high accuracy. The ability to detect very low gas concentrations (sub-ppm) is also achieved by the implementation of the suspended MEMS-TMOS transistor for detection. As GMOS is under extensive development, more algorithms are being added to improve the sensor's performance. Both the Kalman filter and the tinyML, which were presented in the article, enable better real-time gas analysis performance. The combination of the CMOS-SOI-MEMS technology with advanced algorithms and AI/ML techniques will improve the performance of the GMOS sensors.

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editing, Y.N.; visualization, A.K.; supervision, Y.N.; project administration, Y.N.; funding acquisition, Y.N. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

Table A1. Performance comparison of different kinds of sensors for ethylene and acetone detection.

Parameter	GMOS	SPG40	ZMOD4410	MiniPID 2
Size [mm^3] (without evaluation board)	2.2 × 1.6 × 0.3	2.44 × 2.44 × 0.85	3.0 × 3.0 × 0.7	~20 × 20 × 16
Technology	CMOS-SOI-MEMS	MOX (metal oxide)	MOX (metal oxide)	PID (photoionization detector)
Minimum detection limit	20 [ppb]	0.3 [ppm]	160 [ppb]	0.5 [ppb]
Range	~5000 [ppm]	1000 [ppm]	1000 [ppm]	~4000 [ppm]
Selectivity	Selectively [3]	TVOC [2]	TVOC	TVOC
Supply voltage [V]	5	3.3	1.7–3.6	3–3.6
Power consumption	20 [mW]	~8.5 [mW]	Down to 160 [μw]	100 [mW] [1]
Response time [s]	<10	10–30	10	<3
Price	Under development	~10$	~4.3$	1150$
Typical applications	Air quality, fruit refreshment diagnostics, breath control	Indoor air quality	Indoor air monitoring, detection of hazardous materials	Air quality, monitoring

[1] At 3.3 [V]; [2] Total Volatile Organic Compounds (non-selective), [3] Selectively detects various gases, such as: Ethanol, Acetone, Ethylene, CO, NH_3 (also as mixtures).

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A CMOS-MEMS Pixel Sensor for Thermal Neutron Imaging

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Abstract: A monolithic pixel sensor with high spatial granularity (35 × 40 μm^2) is presented, aiming at thermal neutron detection and imaging. The device is made using the CMOS SOIPIX technology, with Deep Reactive-Ion Etching post-processing on the backside to obtain high aspect-ratio cavities that will be filled with neutron converters. This is the first monolithic 3D sensor ever reported. Owing to the microstructured backside, a neutron detection efficiency up to 30% can be achieved with a ^{10}B converter, as estimated by the Geant4 simulations. Each pixel includes circuitry that allows a large dynamic range and energy discrimination and charge-sharing information between neighboring pixels, with a power dissipation of 10 μW per pixel at 1.8 V power supply. The initial results from the experimental characterization of a first test-chip prototype (array of 25 × 25 pixels) in the laboratory are also reported, dealing with functional tests using alpha particles with energy compatible with the reaction products of neutrons with the converter materials, which validate the device design.

Keywords: solid-state detectors; front-end; monolithic sensors; microstructured sensors; thermal neutron detectors

1. Introduction

Thermal neutron imaging is a highly useful analytical technique that finds applications across different fields. The contrast in neutron imaging, as in X-ray imaging, depends on the cross section of each material composing the sample. The attenuation of X-rays increases with the atomic number of the elements, whereas the trend for neutrons with respect to material mass is the opposite. As a result, thermal neutrons can penetrate deeply in most metals, so they can be used for non-destructive investigations of bulk metal components. In addition, neutrons are suitable for investigating lightweight materials, such as those containing hydrogen or water [1]. The most important applications of neutron imaging are in nuclear engineering for nuclear reactor monitoring [2], in material science for studying the internal structure of materials [3], in archeology for studying ancient artifacts and sites [4], and in homeland security [5].

For many decades, ^{3}He detectors have been the "gold standard" for thermal neutron detection due to their high efficiency and low sensitivity to gamma radiation [6]. However, the end of the Cold War led to a decrease in ^{3}He production, which caused a rise in its price and the need for alternative detection solutions. Among such alternatives are gas detectors, scintillators, and solid-state detectors [5]. These detectors are chosen based on their spatial accuracy and active area requirements. Boron-lined proportional detectors, boron trifluoride proportional detectors, and lithium scintillators are the most common alternatives to ^{3}He. Each of these options has its own advantages and disadvantages in terms of efficiency, cost, and toxicity.

Solid-state neutron detectors are suitable for applications that require high spatial resolution and small active areas. Microchannel plates (MCPs) with proper doping are a viable option providing a good trade-off between high detection efficiency (up to 70%)

and high spatial resolution (15 μm), although discriminating gamma-ray interactions with MCPs is difficult since the induced signals are similar to neutrons [7]. Semiconductor detectors are also used with two possible design approaches. The first one involves using neutron-sensitive semiconductors (such as $LiInSe_2$, LiSe, or BN), where most of the charge from the neutron reaction is directly transduced within the sensor itself, resulting in a very high efficiency [8]. This approach is challenging due to issues such as crystal quality and defects that can reduce the signal charge collection. Fabrication technologies for these materials are not well established, although promising results have recently been reported [9]. The second approach involves coating semiconductor (mainly silicon) sensors with thin films of neutron converter materials. ^{157}Gd and ^{113}Cd are materials with the highest thermal neutron cross sections, but their reaction products are γ-rays, which are challenging to distinguish from the background gamma radiation. Hence, other converters such as ^{10}B or ^{6}Li, despite having lower cross sections, are preferred because their reaction products are charged particles, which favor γ-ray discrimination. This reduces interference and enhances the accuracy of neutron detection. However, the short range of the reaction products is also a disadvantage, mainly because of reaction product self-absorption in the converter layer. Another issue for coated detectors is the dead layer (caused, e.g., by metal contacts, high doping regions, and surface passivation layers) between the active area of a semiconductor detector and the converter layer. In the case of planar detectors coated with ^{10}B and/or ^{6}Li films, these problems cause the neutron detection efficiency to be at most a few % [10]. Nevertheless, interesting results in neutron imaging have been reported for coated planar pixel sensors coupled to readout chips from the Medipix family [11], as well as for coated imaging devices such as CCDs [12] and CMOS pixels [13,14].

A significant improvement in detection efficiency can be obtained using three-dimensional structures, which are obtained via MEMS techniques. These devices feature deep cavities on their detector surface, which will be filled with neutron-converting materials. As a result, the effective converter thickness and surface area are decoupled from the ranges of reaction products, resulting in a high neutron absorption probability without affecting the detection of reaction products. In addition, if these cavities are designed correctly, conversion products generated in the opposite directions can be collected, and γ-ray rejection can be enhanced. This method has been pursued by various research groups with remarkable results. For instance, Kansas State University [15] and Lawrence Livermore National Laboratory [16] have attained neutron detection efficiency of nearly 70% and 50%, respectively. A comprehensive review of these detectors can be found in [17]. While the primary objective of these accomplishments is to substitute ^{3}He gas-filled proportional neutron counters for homeland security purposes, some of the suggested approaches can be adapted to create pixelated systems that could be utilized in the field of neutron imaging.

In this paper, we present a monolithic pixel sensor for thermal neutron imaging developed in the framework of the INFN DEEP_3D project (Detectors for neutron imaging with Embedded Electronics Produced in 3D technology) [18]. The detector is fabricated using CMOS SOI technology with Deep Reactive-Ion Etching (DRIE) post-processing on the backside, aiming at obtaining high aspect-ratio cavities to be filled with neutron converters. This is the first microstructured CMOS monolithic radiation sensor ever reported, with potential impact on neutron imaging and beyond. In fact, from the technological point of view, DEEP_3D can be considered a first attempt in the direction to combine the advantages of 3D detectors, with their excellent radiation hardness [19], and monolithic design with high performance and compactness [20].

The device concept builds upon the approach that we have previously tested with a custom technology in the INFN HYDE project (HYbrid DEtectors of neutrons) [21,22], aiming at improving both detection efficiency and spatial resolution.

The ultimate, long-term goal of the project is the development of a high-performance detector for the study of archeological samples (e.g., works of art made of heavy materials such as bronze and iron), which requires objects to be analyzed in non-destructive tests with high spatial resolution and relatively low neutron fluxes to avoid material activation. The

performance of existing neutron imaging systems is not satisfactory for these applications, mainly because of a too low detection efficiency, often lower than 1%, that calls for using large facilities with bright neutron sources to carry out experiments in a reasonable time frame. In order to advance the state of the art, owing to the much higher efficiency expected with the proposed 3D approach, the DEEP 3D project aims at developing a portable system for in-field neutron tomography. In this application, the DEEP_3D detector will be combined with a small accelerator-material target acting as a neutron source and a moderator layer that can be used for neutron tomography.

The remaining part of this paper is organized as follows: the prior art developed in the HYDE project is reviewed in Section 2; the DEEP_3D device is reported in Section 3, covering technological aspects, device simulations, pixel circuit operation principle, and chip design; Section 4 presents the data acquisition systems; and the experimental results are reported in Section 5. Discussion and outlook follow in Section 6.

2. HYDE Detectors

HYDE detectors are microstructured sensors for thermal neutrons made with a simplified, quasi-2D technology: they consist of planar detectors with high aspect-ratio cavities added on the ohmic side (see Figure 1) [21,22]. The substrate is a high-resistivity (HR) p-type material, and the junction side is patterned in n^+ pixels, which are isolated at the surface by a p-spray layer [23], whereas a uniform p^+ region is present on the ohmic side. With reference to Figure 1, the working principle of this detector technology can be described as follows: when a neutron interacts with the converter material, depending on the chosen converter, it produces α particles and other ions (^{7}Li and ^{3}H for ^{10}B or ^{6}Li, respectively) with a given energy [17]. The goal of the silicon sensor is to detect these charged particles (ideally both of them), which will deposit their energy close to the walls of the cavities to generate electron–hole pairs. Holes will be collected at the backside p^+ contact, where reverse bias is applied at the chip periphery. Conversely, electrons will move toward the frontside n^+ pixels and induce current pulses, which are fed to external amplifiers.

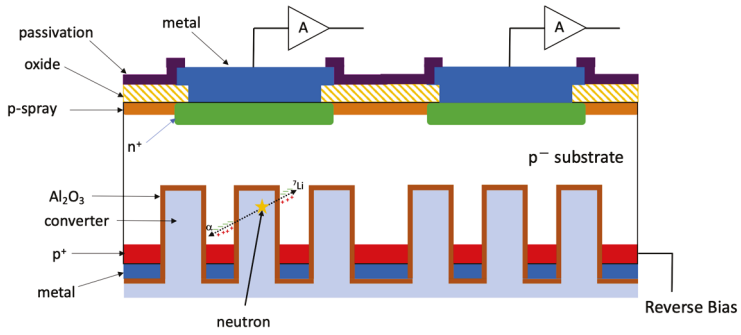


Figure 1. Schematic cross section of a HYDE2 detector (not to scale).

The pixel pitch is 55 µm for compatibility with readout chips of the MEDIPIX/TIMEPIX family [24]. The cavities are etched using DRIE (Deep Reactive-Ion Etching [25]) at the end of the process, using the backside metal as a mask for etching. By doing so, the walls and the bottom of the cavities are not doped: while this reduces the dead layer thickness, it requires the cavities to be passivated in an alternate way. For this purpose, a thin (~50 nm) layer of Al_2O_3 is deposited based on Atomic Layer Deposition (ALD). After annealing, the Al_2O_3 layer exhibits a negative fixed charge in the order of -10^{12} cm^{-2}, which can effectively suppress surface generation/recombination arising from the residual damage due to DRIE [21,22,26,27]. However, it should be noted that the presence of the negatively charged Al_2O_3 layer prevents the silicon regions in between the cavities from being fully depleted. As a result, the electron–hole pairs generated by the reaction products within these regions must move first via diffusion, leading to relatively slow signals in the order of several microseconds. This property was used in [22] to achieve a good γ-ray suppres-

sion without signal loss through pulse-shape analysis of signals processed with different shaping times.

HYDE devices are designed with a cobweb shape for the layout of the cavities, featuring elementary blocks of the same size for the pixel pitch, i.e., 55 μm (see Figure 2 left). Initially, the sizes of the cavities and of the silicon walls in between them were designed for a boron converter, which was expected to yield the best results in terms of detection efficiency and spatial resolution at a given pixel pitch [28]. Several technological experiments were performed, and they indicated that limiting the depth of DRIE of the cavities to approximately 25 μm would be necessary. This measure aims to prevent mechanical and thermal problems caused by heat generated during the etching process, since the narrow walls around the cavities make it difficult to dissipate this heat.

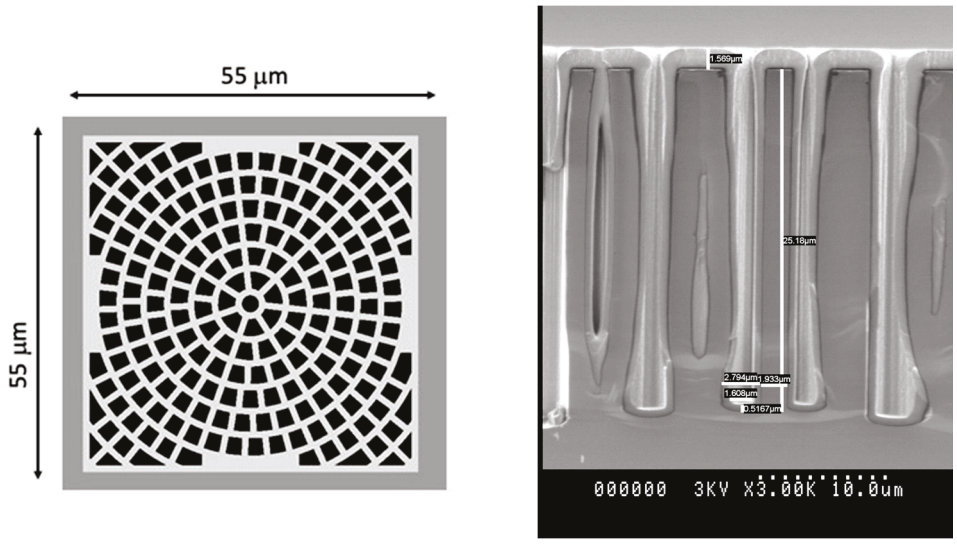


Figure 2. (**Left**) Layout of cavity cobweb (version for ^{10}B converter) in a pixel of HYDE detectors. (**right**) Scanning electron microscopic graph of cavities partially filled with ^{10}B using LPCVD at LLNL.

Preliminary results were obtained from diode structures having ~25 μm deep cavities partially filled with ^{10}B using Low-Pressure Chemical Vapor Deposition (LPCVD) at the Lawrence Livermore National Laboratory (LLNL), Livermore, USA (see Figure 2 right). Under exposure to thermal neutrons from a moderated alpha-beryllium source at Politecnico di Milano, Italy, a detection efficiency of ~7% was measured [27], which was lower than expected because of an insufficient thickness of the boron layer in the tested sample (~500 nm).

For HYDE pixel detectors, the need for bump bonding to the readout chip poses significant problems when using a boron converter. In fact, the temperature necessary for the LPCVD of boron (~350 °C) is not compatible with detector assemblies after bump bonding. In principle, the deposition of boron could be made on bare silicon sensors before bump bonding, thereby protecting the pixel side from undesired boron deposition. However, this approach may negatively impact the surface quality, thus hindering the bump bonding process. For these reasons, it was decided to process a few wafers of detectors with a different mask for cobweb cavities, which were redesigned with larger geometries suitable for a ^{6}LiF converter. Pixel sensors from these wafers were bump bonded to the TIMEPIX readout chip [24] at ADVACAM Oy (Espoo, Finland). The hybrid detectors were assembled in a FitPix system at the Czech Technical University in Prague. They are currently being tested after filling the cavities with ^{6}LiF powder [29].

3. DEEP_3D Detectors

3.1. Device Description

Porting the HYDE concept to monolithic technology makes bump bonding unnecessary, thus allowing the use of a boron converter. For this purpose, a CMOS process enabling the full depletion of a HR p-type substrate is required. Possible solutions could be CMOS technologies used so far for depleted Monolithic Active Pixel Sensors (MAPS), where the electronic circuits are insulated from the HR substrate via deep p-wells [20]. Our choice was to use the 0.2 µm CMOS single Silicon-on-Insulator (SOI) technology developed by the Japanese High-Energy Accelerator Laboratory, KEK, and produced by the Lapis Semiconductor Co. Ltd. [30].

A sketch of the DEEP_3D device concept in this technology is shown in Figure 3. SOI technologies provide the most effective isolation between the CMOS transistors, made in a thin silicon layer, and the sensor active layer through a buried oxide (BOX) layer. The sensor layer consists of a float-zone, p-type silicon substrate with a nominal thickness of 300 µm and a resistivity of 7 kΩ cm, yielding a full depletion voltage of ~140 V. The isolation between the n^+-charge collection electrodes at the Si-SiO_2 interface is ensured by the buried p-well implants acting as p-stops [23], not shown in Figure 3.

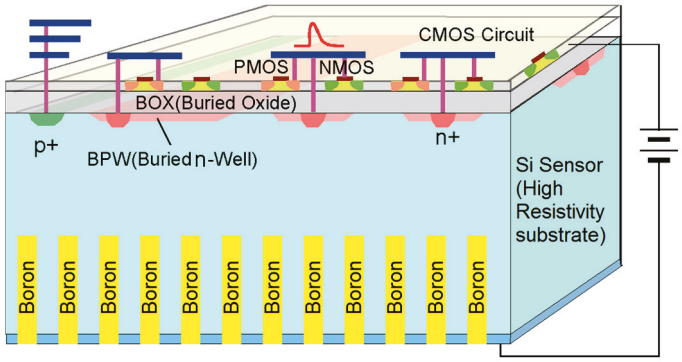


Figure 3. Sketch of the DEEP_3D device based on CMOS SOI technology (not to scale).

The process is free from latch-up, and the cross section for single-event upsets is very small. The thickness of the HR substrate can be tailored from ~500 µm down to ~50 µm. After substrate thinning, a good ohmic contact is obtained by backside implantation, laser annealing, and metal deposition. Single SOI technology has a drawback known as the back-gate effect, which changes the electrical properties of CMOS transistors due to the voltage applied to the device's backside [30]. In addition, the buildup of trapped charge in the BOX layer due to ionizing radiation can also lead to a similar effect. The back-gate effect is suppressed by the presence of buried wells, biased to ground and underneath the circuits, which, however, are not effective against the charging of the BOX layer. The latter problem could be solved using a double-SOI process [31], but a single SOI technology is deemed appropriate for a proof of concept.

After the CMOS-SOI chip fabrication is completed, the device requires backside post-processing, including etching of the cavities by DRIE, passivation of the cavities with Al_2O_3 by ALD, and boron filling. The cobweb layout of the cavities was designed following the results from the Geant4 simulations, as described in the following section.

3.2. Geant4 and TCAD Simulations

Monte Carlo simulations were performed using the toolkit Geant4 [32]. One million neutrons at a thermal energy of 0.25 meV were generated with a perpendicular and uniform spatial distribution along the xy-surface of the device. The reaction products (α particles and ions) that released energy in the silicon substrate were counted using a threshold of 50 keV. The ratio between the number of reaction products and the neutrons defined the efficiency. From a methodological point of view, the geometry of the cavities was defined

using CAD and imported directly into Geant4 as described in [33]. The engine physical simulator model appropriate for this simulation was QGSP BERT HP, using the neutron cross section contained in the GDML library, and the density of ^{10}B was considered by including enriched B at 99% and ^{11}B at 1% with a density of 2.46 g/cm^3. The simulations were carried out with neutrons impinging from both sides of the detector. Figure 4 compares the simulation results for different combination of geometrical sizes of the cavities (in the range from 2.8 to 5 µm) and the walls in between them (in the range from 1.1 to 5 µm). Since boron deposition filled the cavities completely (which had a depth of 25 µm) and only 1 µm of boron was considered at the surface, irradiations from the two sides yielded very similar results, with a slightly better efficiency for the irradiation from the side opposite to the cavities. The importance of using small dimensions for the cavities and the walls was evident, with efficiency values decreasing from ~30% to ~12% as the sizes increased from the smallest ones to the largest ones.

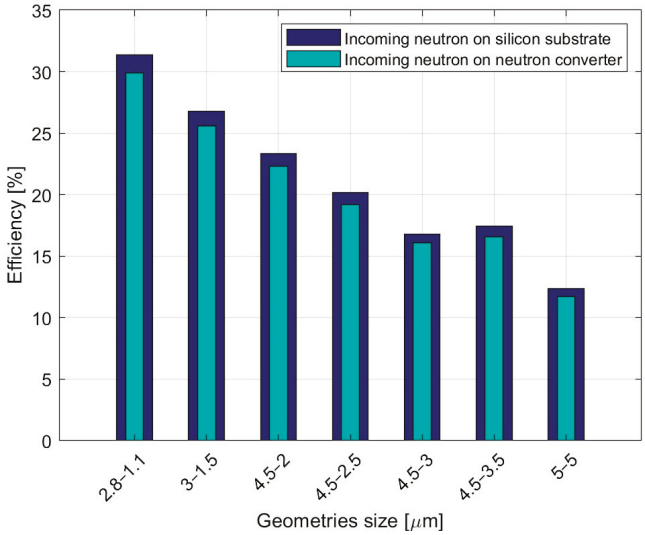


Figure 4. Geant4 simulation of thermal neutron detection efficiency in HYDE 2 devices of different geometrical sizes (the widths of the cavities and of the silicon walls in between them are given in micrometers), with a 50 keV energy threshold.

TCAD simulations were performed using Synopsys Sentaurus to demonstrate the effective collection of the charge generated when a secondary particle hits the sensitive area. The simulation domain considered was a single 3D pixel, and α-particle simulations were conducted. The reverse bias was 100 V, i.e., slightly below the depletion voltage of the non-etched portion of the substrate. The depth of the cavities was 25 µm. A worst-case scenario was considered for the Al_2O_3 passivation layer with a low negative fixed charge density of -10^{12} cm^{-2} and a very large surface recombination velocity of 10^4 cm/s to account for a high residual damage from DRIE.

Figure 5 shows the transient current response induced by alpha particles of 1.47 MeV (i.e., the most probable energy for a neutron reaction with ^{10}B) entering the active volume in two different positions, as shown in the inset of Figure 5 (upside down), which were chosen as representative of two extreme cases: (1) at the bottom of the cavities (red line), and (2) at the surface on top of the regions in between the cavities (black line). In case 1, the signal is fast with a pronounced current peak because charge carriers are generated close to the edge of the depleted region and mainly move by drift. The charge collection efficiency in this case is 100%. Conversely, in case 2, charge carriers have to initially move by diffusion, so that the current peak is much smaller and lasts for a few microseconds. The charge collection efficiency in this case is ~80%, with the charge loss being due to the considered worst-case recombination effects in the cavities.

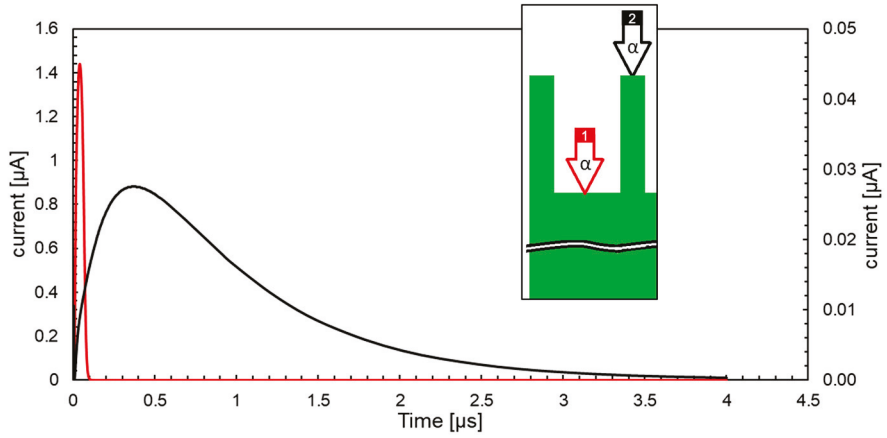


Figure 5. TCAD simulation of output current signal transients for alpha particles hitting position 1, located at the bottom of the cavities (red line, left current axis), and position 2, at the surface on top of the regions in between the cavities (black line, right current axis).

3.3. Chip Design and Pixel Operation

A micrograph of the DEEP_3D chip is shown in Figure 6. It includes an array of 25 × 25 pixels, each having a size of 35 × 40 μm^2; the CMOS circuitry for the voltage and current references; and the IO ring with all the analog and digital components along the edges. In addition, a test structure is present to enable testing the pixel functionality independently of its array implementation. It consists of two pixels, one featuring the same front-end circuit used in the pixel array and another one composed of a charge pre-amplifier and a feedback circuit. The total area of the chip is 2.9 × 2.9 mm^2.

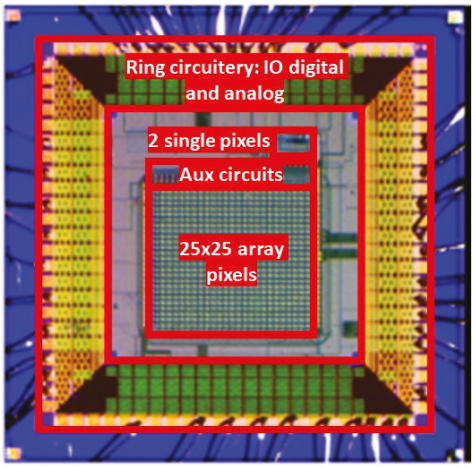


Figure 6. Photograph of the DEEP_3D chip, with different blocks highlighted.

The pixel CMOS circuitry is shown in Figure 7, while the corresponding layout is shown in Figure 8. The sensor output current is fed to a charge pre-amplifier which input branch uses a telescopic cascode topology (transistors M1–M4), with gain enhancement obtained by means of the auxiliary PMOS cascode (transistors M5–M6). This ensures a gain higher than 10^4, which, considering the values of capacitance of the single pixel and of the feedback capacitors, allows the efficient detection of the collected charge generated by an event. To reduce power consumption and increase the input stage gain, the fixed current for each branch of the circuit and the size of the transistors have been calculated to ensure that all the preamplifier transistors are operating in weak inversion. Two different values of capacitance, i.e., 150 fF and 100 fF, can be selected by an external gain control signal for the feedback circuit of the charge pre-amplifier, thus yielding two levels of gain suitable for the different signals expected from the reaction products of the boron and lithium converters.

On-chip MIM capacitors are used to this purpose, which, in this technology, have a specific capacitance of 1.5 fF/μm^2. The constant current rate circuit (MF and Mfb) [34] is responsible for discharging the feedback capacitor, enabling all the transistors to fit within the limited pixel size. This design accommodates slow current signals from the low electrical-field sensor region, where charges move only by diffusion, at the expense of a loss of linearity for small charge signals.

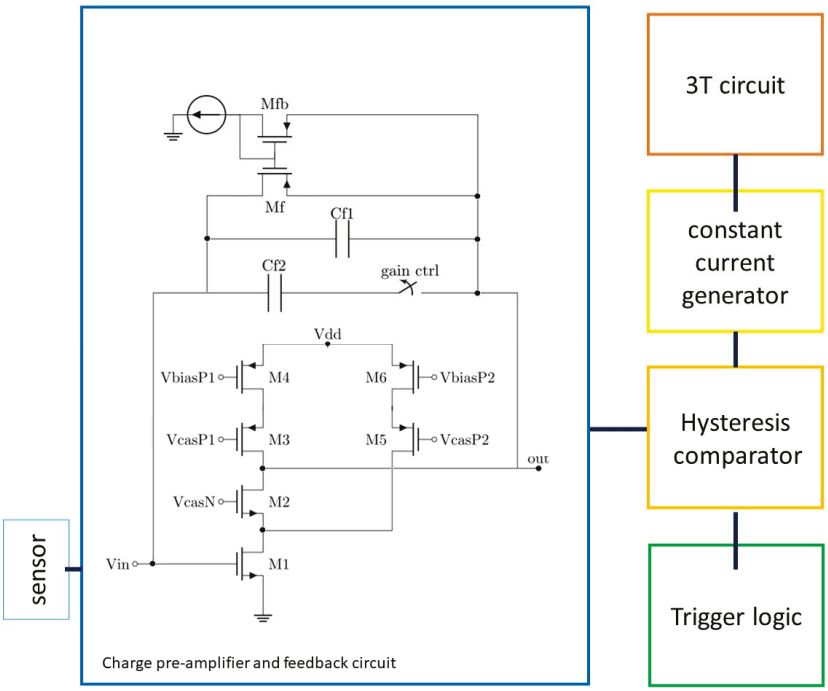


Figure 7. Schematic diagram of the pixel circuit.

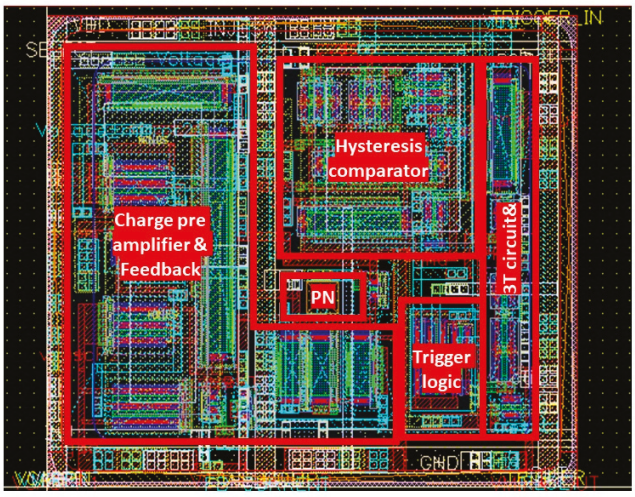


Figure 8. Pixel layout with a size of 35 × 40 μm^2 with different blocks highlighted. The feedback capacitors, which cover more than 80% of the pixel area and are placed on the entire pixel surface, are not shown.

The remaining parts of the pixel circuit are shown as blocks in Figure 7 since they are based on standard circuits. The output of the charge pre-amplifier is fed to a comparator with hysteresis, which is designed to withstand fluctuations in noise. The comparator converts the analog pulse to a digital signal, the duration of which corresponds to the energy of the detected reaction product. The comparator output signal is fed to two

different branches: a digital trigger logic which output signal remains high until reset, and a switch in an auxiliary circuit that, when activated, charges a capacitor with a constant current. By doing so, a time-over-threshold (ToT) technique can be exploited, storing the signal amplitude information on the capacitor used as an analog memory. The capacitor can be fully charged within the time of a few μs, which is tunable depending on the sensor signal. The capacitor is connected to a 3T circuit [35], enabling reading of the corresponding voltage value pixel by pixel. To summarize the signal path in the pixel circuit, the sensor output, which is usually short (a few μs) and has a low intensity of current (in the μA range), becomes a signal of a few millivolts and tens of microseconds after the charge preamplifier. The time-over-threshold of this signal provided by the comparator charges an internal capacitor, which, when charged by using a constant current, stores a voltage proportional to the input charge. The 3T circuit can then measure the value of this voltage when the pixel's information is required. The power consumption of a single pixel is in the order of 10 μW with 1.8 V power supply.

Additional circuits are required to control the operation of the pixel matrix. These circuits include selection circuits for rows and columns, analog amplifiers to support the 3T pixel circuits, and general trigger logic. The selection of rows and columns is achieved using a shift register composed of a chain of 25 D flip-flops with a reset function. Digital circuitry is responsible for injecting the bit into the first shift register. The general trigger circuit collects information from all the pixel triggers and records the presence of an event by transmitting the information outside the matrix.

DEEP_3D is the first 3D monolithic device, a promising candidate to significantly innovate the field of neutron imaging. Its more direct competitors are based on planar neutron detectors, i.e., the hybrid detector developed by the Czech Technical University in Prague based on the Medipix-2 chip [11,28] and the monolithic SOI sensor developed by KEK [14]. Since a planar detector coated with a neutron converter is involved in both of these cases, the neutron detection efficiency is limited at most to 3–4%, whereas with DEEP_3D, it is estimated to achieve an efficiency up to 30% in the best case. The spatial resolution is directly proportional to the pixel size. Since each pixel in the DEEP_3D device includes a charge pre-amplifier and other circuits that make the chip fast enough and enable successive analysis (e.g., gamma discrimination), its size of 35×40 μm^2 is not the smallest in this panorama, but it is still small enough compared to the Medipix-2 device (55×55 μm^2), which also includes complex circuitry. The KEK device has a smaller pixel size of 17×17 μm^2, due to a simpler circuit topology, and an estimated spatial resolution of ~4 μm, but its efficiency is only 1.5%.

4. Data Acquisition System

The data acquisition boards' general schematic and a photograph of the measurement setup are shown in Figure 9. To begin, the DEEP_3D chip is connected to a PCB board through wire bonding, followed by its installation on a primary board. This main board comprises eight reference current generators, a reference voltage, and links to the FPGA board. For this project, a Digilent Zedboard was utilized as the FPGA board, which is an evaluation and development board utilizing the Xilinx Zynq-7000 All Programmable SoC (AP SoC). The FPGA board, operating at 100 MHz, generates the necessary digital signals for controlling the sensor chip, resulting in highly precise signal timing despite the sensor's relatively low frame rate. To save power, the maximum frame rate is limited to 0.8 kHz, but it can be doubled by increasing the amplifier current. The analog signal is acquired using the FPGA's inner ADC with a resolution of 12 bits and stored in a FIFO register before being immediately transferred to the FPGA's RAM via Direct Memory Access (DMA), which optimizes data transfer to avoid dead times. The chip trigger event occurs only when the incident particle releases enough charge to exceed the fixed trigger level.

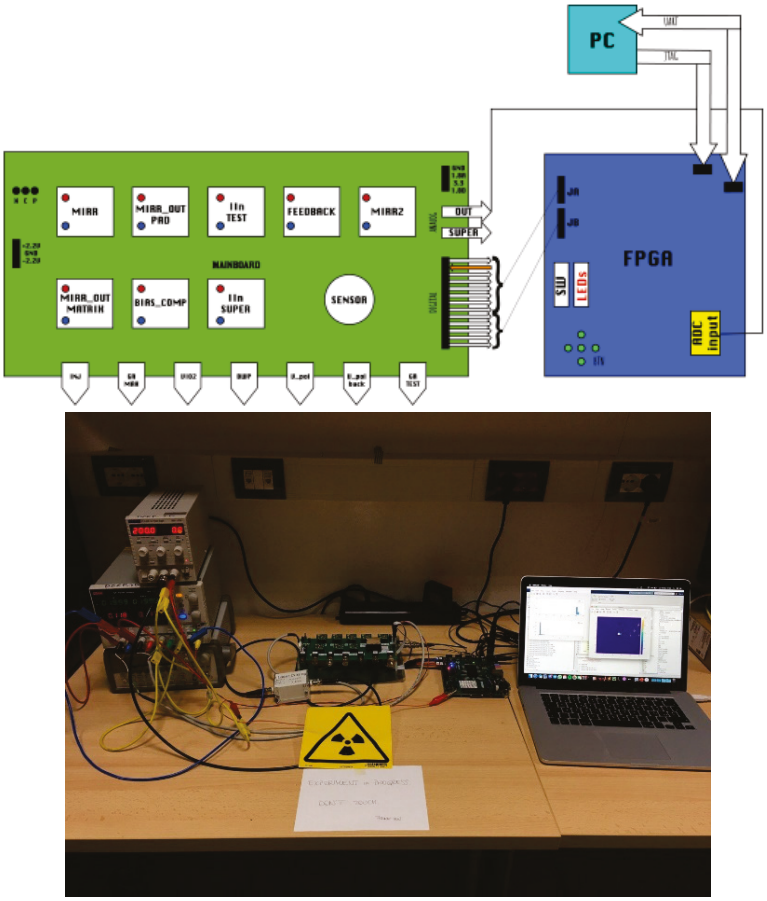


Figure 9. (**Top**) Block diagram of the data acquisition system and (**bottom**) photograph of the measurement setup in the laboratory.

The internal microprocessor, which is programmed in C language, handles data transfer to the PC via a serial port. The acquired data are then processed using the Matlab software. To minimize power consumption, the IO ring amplifiers are switched off after acquisition until the next trigger event.

5. Results

Before proceeding to device post-processing, the chip functionality was tested using a ^{241}Am source, which decays 100% via α transitions to ^{237}Np. The source available in our laboratory has a low nominal activity of 3 kBq. The α energy's primary peak is 5.5 MeV, providing an accurate emulation of the reaction products resulting from neutrons colliding with the converter materials.

The initial tests were conducted on the test structure with the pre-amplifier and its feedback circuit. The output signal from the pre-amplifier was further amplified by a buffer stage and acquired by an oscilloscope. Given the small pixel size of only 35×40 µm^2 and the limited activity of the source, the event probability was relatively low, with a rate of 1 event every ~12 min. Figure 10 displays the typical response to an α particle: both the signal amplitude (~0.8 V) and the decay time (~300 µs) are in good agreement with values predicted by the simulations and can be utilized for feedback circuitry tuning.

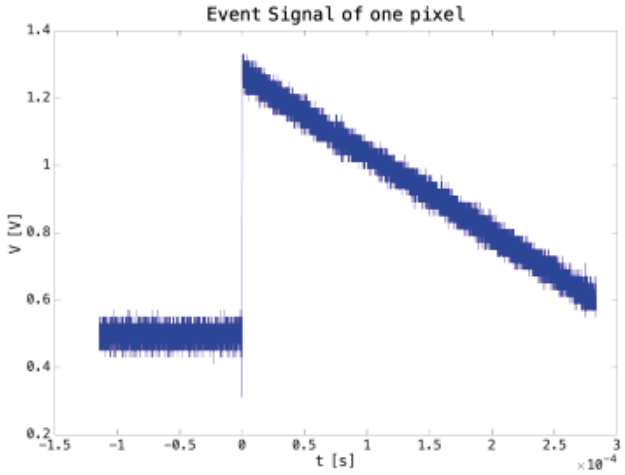


Figure 10. Output signal from the charge pre-amplifier output in response to an α particle from a ^{241}Am source. The source is placed at ~1 cm from the CMOS side of the sensor, and both feedback capacitors are selected to manage all the charge released from the ^{241}Am source.

For the measurements on pixel arrays, the following procedure was used:

- Acquisition of dark signals: Prior to placing the α source on the sensor, measurements were taken in dark conditions. The FPGA firmware allowed acquisition even without a trigger event from the chip. To obtain an average value for the dark signals, the mean of individual pixels was computed, which also evaluated the uniformity of the matrix. The distribution of the mean pixel values was then calculated and fitted to a Gaussian curve. The distribution was found to be narrow, with a mean value of $\mu = 0.90$ V and a standard deviation of $\sigma = 0.03$ V.
- Removal of defective pixels: any pixels that could trigger incorrect detection events were identified and removed from future analyses by setting them to zero.
- Acquisition of alpha particle events: real detection events were acquired.
- Removal of dark signals and data analysis: the acquired data were adjusted by subtracting the dark signals to eliminate any offset, and the data were analyzed accordingly.

5.1. Irradiation from the Frontside (CMOS Side)

To analyze the behavior of the front-end electronics when signals are fast, frontside irradiation was performed. In this case, the source was placed approximately 2 cm from the sensor surface.

Since substrate depletion begins at the n^+/p^- junction near the buried oxide, the motion of generated charge occurs primarily by drift, leading to fast signals. However, prior to reaching the sensing component, α particles must pass through several layers (e.g., passivation, metals, dielectrics, and electronics), thus causing a non-negligible energy loss. The reverse bias was set to −75 V, resulting in partial depletion of the high-resistivity substrate.

Figure 11a shows the map of signal acquisition in the dark, while Figure 11b shows the acquisition of a single α-particle event obtained by subtracting the acquired data from the dark acquisition. In the case of frontside irradiation, charge-sharing effects between neighboring pixels are seldom observed due to the fast charge collection (the charge cloud does not have sufficient time to diffuse far from the generation point) and the lower amount of charge generated after energy loss in the electronic layers.

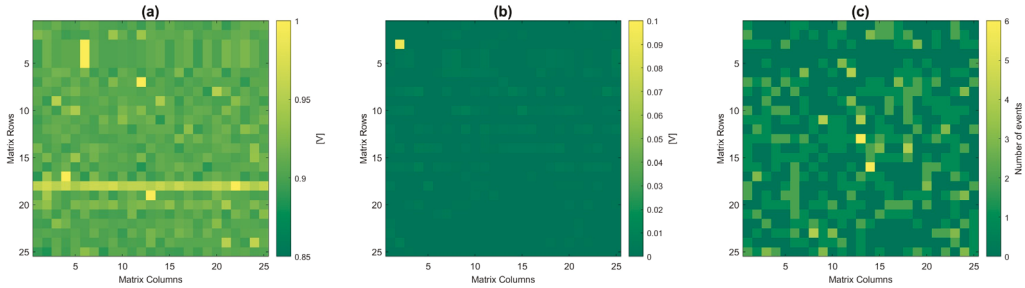


Figure 11. Hit maps for frontside irradiation: (**a**) acquisition of dark signals; (**b**) acquisition of single α event; and (**c**) 36 h acquisition with at least one event in most unmasked pixels.

To test the entire matrix, the acquisition procedure was carried out for a relatively long period of time (~36 h) due to the low activity of the source. The resulting hit map is shown in Figure 11c. Most unmasked pixels have recorded at least one event.

5.2. Irradiation from the Backside (Sensor Side)

When irradiating from the backside, the reverse bias was increased to −200 V so that the 300 µm thick high-resistivity substrate could be fully depleted. To expose the backside to α particles, a hole of 2.5 mm diameter was drilled on the PCB and the sensor was placed on top of it, while the radiation source was placed underneath at a distance of approximately 2 mm from the board. It is worth noting that the tested sensor has a layer of metal deposited on the backside that shields it from ambient light.

As the neutron converter was placed on the backside, more events were acquired compared to the frontside case, for a total of ~40 h. Figure 12 leftshows the hit map, where, again, most of the pixels are operational, and only one row appears insensitive, possibly due to a defect on this specific chip.

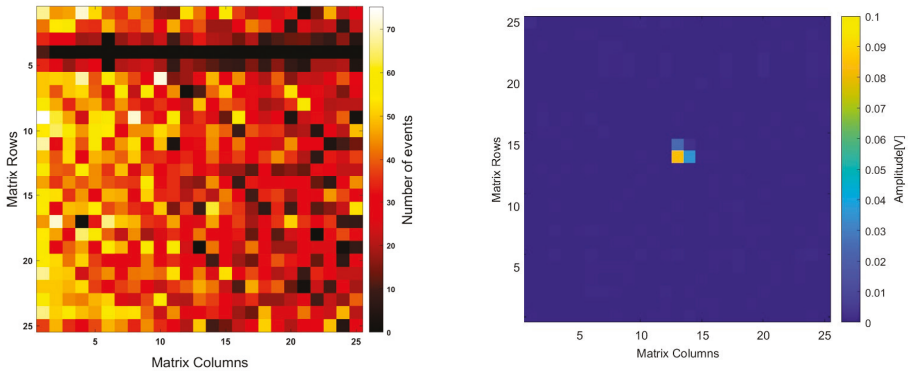


Figure 12. Hit maps for backside irradiation: (**left**) 40 h acquisition, and (**right**) detail of single α event with charge sharing among three adjacent pixels.

Because of the inaccurate technique employed to produce the hole on the PCB, the matrix was not centered perfectly over the hole, and this is reflected in the hit distribution along the matrix. It is worth noting that in the case of backside irradiation, charge sharing between pixels is clearly present, as also shown in Figure 12 right for a single α-particle event. This feature is particularly important for particle discrimination (e.g., for γ-ray suppression), as already demonstrated in previous studies [36].

6. Discussion and Outlook

The initial tests performed in the laboratory at the University of Trento demonstrated that the chip works correctly and in accordance with the design specifications. The power consumption is ~10 µW per pixel at 1.8 V power supply, well matching the design value. The theoretical gain of the charge preamplifier is inversely proportional to the feedback

capacitance, and using both feedback capacitors in parallel gives a total capacitance of 250 fF and a gain of 4 V/pC. Upon exposure to alpha particles of 5.5 MeV, the measured output signal amplitude is ~0.8 V, corresponding to a gain of ~3.3 V/pC, which is in good agreement with the expected gain while taking into account the uncertainties due to parasitic capacitances and the energy loss of α particles in air and in the dead layers. Additionally, the decay time of the preamplifier output signal (~300 μs) is consistent with the constant current used in the reset circuit.

The sensor breakdown voltage is larger than 200 V, and it allows a wide operational margin beyond the full depletion voltage. The signals induced by α particles were acquired for a relatively long exposure time (~40 h), thus confirming the correct functionality of the entire pixel front-end circuit and of the external readout circuit and trigger logic. In the case of frontside irradiation, individual pixels were mostly activated, which was consistent with the limited diffusion of the charge generated close to the pixel junction. On the contrary, charge-sharing events were observed in the case of backside irradiation, as expected from the lateral diffusion of the charge cloud (>5 μm) as it drifted through the entire thickness of the substrate.

Due the low activity of the available α source, it would have taken several weeks to accumulate significant statistics, making it impossible to build an energy spectrum or capture an image. Despite this limitation, the measurement results are encouraging and suggest it is possible to proceed with the backside post-processing that is necessary to make the device sensitive to neutrons.

For the etching of the cavities using DRIE and their passivation, we are collaborating with the Leibniz Institute of Photonic Technology (Jena, Germany), where preliminary tests have been carried out on bare silicon samples (individual dice having a size comparable to the DEEP_3D chip). For this purpose, a mask with a cobweb layout of 55 μm pitch is used, and etching tests have been performed. As an example, Figure 13 left shows a scanning electron microscopic image of the cavities after the DRIE step: the etching depth (~18 μm) is close to the target value (~25 μm), but the width of the cavities is larger than the nominal value, leading to thinning of the separation walls. Further tests are under way to optimize the etching recipe before applying it to real device samples.

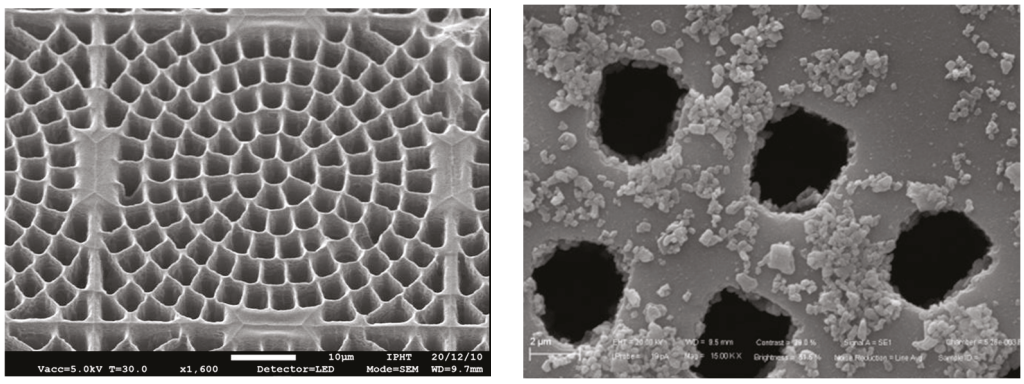


Figure 13. Scanning electron microscopic pictures of (**Left**) cobweb cavities etched by DRIE at Leibniz-IPHT, and (**Right**) deposition test of alumina nanoparticles at the University of Trento.

For boron deposition, besides relying on external collaborations using Chemical Vapor Deposition or Atomic Layer Deposition, we are pursuing an alternative approach similar to that used for ^{6}LiF deposition, which consists of dispersing nanoparticles of $^{10}B_4C$ (pure boron at the nanoparticle scale has a very high risk of being flammable) in a non-polar liquid that is deposited on the etched surface and fills the cavities by capillarity. After evaporation, only the $^{10}B_4C$ grains will remain. With multiple depositions, it should be possible to fill the cavities. Preliminary tests have been conducted with encouraging results using alumina nanoparticles instead of boron carbide (see Figure 13 right).

Author Contributions: Conceptualization, R.M. and G.-F.D.B.; methodology, R.M. and G.-F.D.B.; software, R.M.; validation, R.M.; formal analysis, R.M.; investigation, R.M.; resources, R.M. and G.-F.D.B.; data curation, R.M.; writing—original draft preparation, R.M.; writing—review and editing, G.-F.D.B.; visualization, R.M.; supervision, G.-F.D.B.; project administration, R.M. and G.-F.D.B.; funding acquisition, R.M. and G.-F.D.B. All authors have read and agreed to the published version of the manuscript.

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A Novel Miniature and Selective CMOS Gas Sensor for Gas Mixture Analysis—Part 4: The Effect of Humidity

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Abstract: This is the fourth part of a study presenting a miniature, combustion-type gas sensor (dubbed GMOS) based on a novel thermal sensor (dubbed TMOS). The TMOS is a micromachined CMOS-SOI transistor, which acts as the sensing element and is integrated with a catalytic reaction plate, where ignition of the gas takes place. The GMOS measures the temperature change due to a combustion exothermic reaction. The controlling parameters of the sensor are the ignition temperature applied to the catalytic layer and the increased temperature of the hotplate due to the released power of the combustion reaction. The solid-state device applies electrical parameters, which are related to the thermal parameters. The heating is applied by Joule heating with a resistor underneath the catalytic layer while the signal is monitored by the change in voltage of the TMOS sensor. Voltage, like temperature, is an intensive parameter, and one always measures changes in such parameters relative to a reference point. The reference point for both parameters (temperature and voltage) is the blind sensor, without any catalytic layer and hence where no reaction takes place. The present paper focuses on the study of the effect of humidity upon performance. In real life, the sensors are exposed to environmental parameters, where humidity plays a significant role. Humidity is high in storage rooms of fruits and vegetables, in refrigerators, in silos, in fields as well as in homes and cars. This study is significant and innovative since it extends our understanding of the performance of the GMOS, as well as pellistor sensors in general, in the presence of humidity. The three main challenges in simulating the performance are (i) how to define the operating temperature based on the input parameters of the heater voltage in the presence of humidity; (ii) how to measure the dynamics of the temperature increase during cyclic operation at a given duty cycle; and (iii) how to model the correlation between the operating temperature and the sensing response in the presence of humidity. Due to the complexity of the 3D analysis of packaged GMOS, and the many aspects of humidity simultanoesuly affecting performane, advanced simulation software is applied, incorporating computational fluid dynamics (CFD). The simulation and experimental data of this study show that the GMOS sensor can operate in the presence of high humidity.

Keywords: gas sensor; pellistor; CFD; TMOS; GMOS; humidity

1. Introduction

1.1. SMO Sensors and GMOS Sensors

In recent years, the need for mobile, low-cost and low-power gas sensors has increased dramatically. Such gas sensors are needed for safety in homes and cars, monitoring air quality, the well-being of people as well as industrial process control and sustainable smart agriculture [1–8]. During the past few decades, SMO (Semiconductor Metal Oxide, also

referred to as MOX) gas sensors have become a leading technology in domestic, commercial and industrial gas-sensing systems because of their following features: low cost, adequate sensitivity and easy to measure response (a change in resistivity). However, these sensors have problems in reproducibility, stability and selectivity.

1.2. GMOS Sensor

A completely different class of gas sensors, known as pellistors, measures the temperature change due to a combustion exothermic reaction. Traditional pellistor sensors use a thermal sensor to measure temperature change. The sensor is usually a resistor, but thermopiles and pyroelectric ceramics have also been reported.

In the last decade, a thermal sensor (dubbed TMOS) based on CMOS-SOI technology has been studied and reached maturity; it is now mass-produced in a commercial fab [9,10]. The sensing element is a suspended MOSFET transistor (Figure 1a) that operates at subthreshold, and therefore requires low power consumption.

These advantages of TMOS have been applied to fabricate a new combustion-type, pellistor-like gas sensor (dubbed GMOS). To fabricate a GMOS, an integrated heating resistor is added to a TMOS thermal sensor (Figure 1b) and the catalytic layer is applied on the top surface of the pixel. The feasibility of GMOS sensing and its advantages have been reported in several publications [11,12]. In contrast to SMO or MOX sensors, where the sensing element interacts with the gas, the GMOS sensing element—the micromachined CMOS transistor—does not interact directly with the gas, and therefore has potential for long-term stability.

The present paper complements the series of papers published in micromachines analyzing the innovative GMOS sensor [13–15]. In the first two previous papers, the sensing [13] and electrical [14] properties of this sensor were described. The third paper focused on the investigation of the sensing mechanism, modeling the underlying thermodynamic and chemical processes, by applying advanced tools for 3D simulation of fluid dynamics [15].

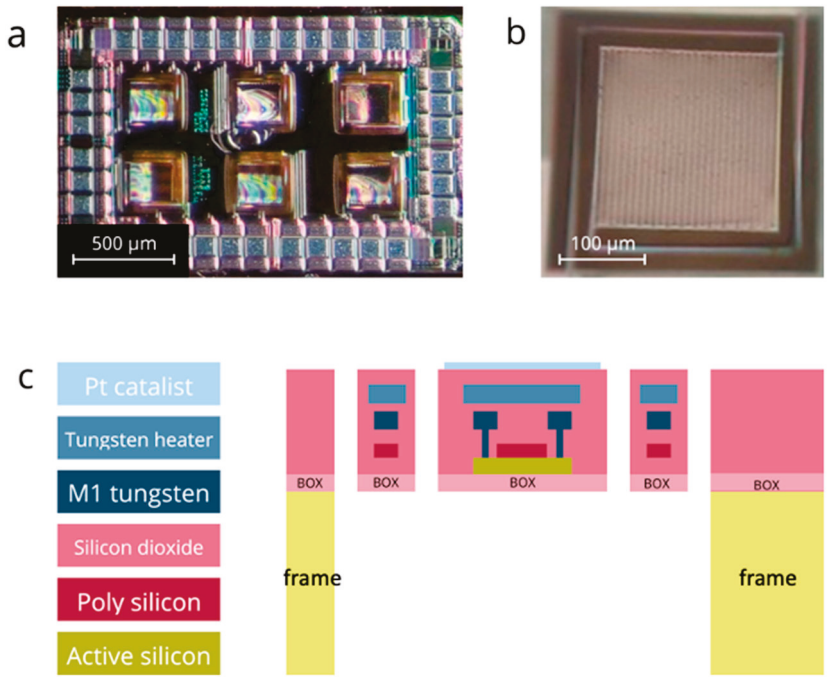


Figure 1. (**a**) The microscopic image of the GMOS sensing die with six sensing pixels. The die size is 2000 µm × 1380 µm; (**b**) The microscopic image of a single sensing pixel. The pixel size is 213 µm × 213 µm. (**c**) The cross-section scheme of the GMOS sensing pixel deposited above the buried oxide (BOX). The figure is from [15].

This study focuses on the effect of humidity on the performance of GMOS. The sensors are calibrated in the lab. However, in real life, the sensors are exposed to environmental parameters, where humidity plays a significant role. Humidity is high in the storage rooms of fruits and vegetables, in refrigerators, in silos, in fields as well as in homes and cars. Humidity affects the thermal conductivity and thermal diffusivity of air as well as other thermophysical properties and the enthalpic heat of combustion of the analyte, and accordingly the simulation and 3D modeling of the GMOS are revisited in this study.

Due to the complexity of the 3D analysis of packaged GMOS, and the many aspects of humidity simultaneously affecting performance, advanced simulation software is applied, incorporating computational fluid dynamics (CFD). The implementation of CFD modeling provides valuable data about the thermal properties of the investigated device. The simulation and experimental data of this study exhibit that the GMOS sensor can operate in the presence of high humidity.

This paper is organized as follows. The thermophysical properties of humid air are reviewed in Section 2. In Section 3, the static and dynamic operation of the GMOS designed with a bridge-like readout in the presence of humidity are revisited. The simulation results are presented in Section 4, followed by the experimental results in Section 5. Finally, Section 6 concludes the paper.

2. The Thermophysical Properties of Humid Air

Humid air has different thermal transport properties compared to dry air and this affects the static as well as dynamic response of gas sensors. The thermophysical properties of humid air at the temperature range between 0 and 100 °C as well as at higher temperatures, as a function of humidity and temperature, are required for ordinary heat transfer engineering calculations.

An investigation into the thermophysical and transport properties of humid air at a temperature range between 0 °C and 100 °C based on simulation can be found in [16]. A recent review paper on CMOS thermal sensors supports the data of the earlier paper [17], as shown in Figure 2.

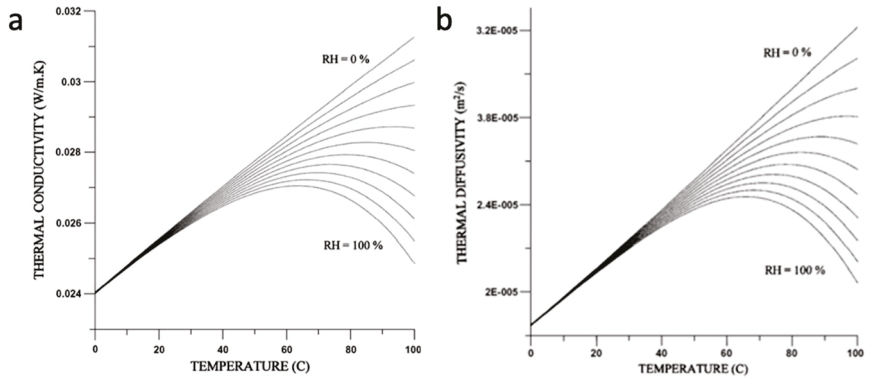


Figure 2. In the presence of moisture, (**a**) the thermal conductivity of air decreases; similarly, (**b**) the thermal diffusivity of air decreases. The decrease starts at approximately 40 °C and the effect becomes more pronounced as temperature and moisture increase. Figures obtained from [16] with permission.

Table 1 is an overview of the main physical parameters required for the modeling and simulation of the GMOS sensors in the presence of humidity.

Figure 1 shows how the thermal conductivity and diffusivity of air change with temperature for different values of relative humidity. It shows that for a given temperature, the specific thermal conductivity decreases significantly above 50° C as humidity increases. A maximum value of thermal conductivity is developed for each fixed relative humidity curve, which moves towards higher temperatures as the relative humidity decreases. This maximum typically moves from the temperature of 60 °C to about 95 °C as the relative humidity (RH) decreases from saturation-level conditions to about RH = 40%.

Table 1. Typical thermophysical parameters of dry air and water vapors.

Parameter	Description	Dry Air at 300 K	Water Vapor at 300 K	Note
k $\left[\frac{W}{m \cdot K}\right]$	Thermal conductivity	0.026	0.023	Lower for water vapor
$\alpha\left[\frac{m^2}{s}\right]$	Specific thermal diffusivity	1.9×10^{-5}	1.2×10^{-5}	Lower for water vapor
$c\left[\frac{J}{Kg \cdot K}\right]$	Specific heat capacity	1006.43	1857.72	Higher for water vapor
ρ [Kg/m^3]	Density	1.225	0.5542	As temp. increases, the density decreases

These results can be understood if we pay attention to the fact that the thermal conductivity of water vapor is lower than that of air. To really feel intuitively why at higher temperatures there is a much stronger effect of humidity, we need to remember that air can hold much larger amounts of water vapor at higher temperatures. If in the gas box at the lab there is a certain amount of water vapor, as temperature increases, the relative humidity decreases.

For this reason, humidity compensation of the measurements becomes especially important as temperature increases. To compensate for this effect, a separate humidity sensor is integrated into the sensing system, hoping that with the right algorithm we can take this effect into account.

Table 1 indicates that the thermal heat capacitance of water vapor is larger than that of dry air. This tells us that the presence of humid air will affect the transient response of the sensor and cause a decrease in the maximum achievable temperature. Accordingly, we need to re-visit the static and dynamic modeling of the GMOS sensor to consider the effect of the parameters of Table 1.

3. Revisiting the Static and Dynamic Operation of the GMOS Designed with a Bridge-like Readout in the Presence of Humidity

GMOS Sensor

The oxidation reaction of the sensed gas is ignited at a given temperature, which is specific for the measured gas and the catalytic layer (denoted below by T*—see references [11,15]). To achieve the ignition temperature, the catalytic layer's temperature is increased by Joule heating dissipated by the resistor in contact with the reaction plate. The value of the required resistor is determined by the following heat flow equation:

$$C_{th}\frac{d(T-T_0)}{dt} + G_{th}(T-T_0) = P_{Joule-heating} + P_{reaction} \quad (1)$$

where, at steady state,

$$T = T_0 + \Delta T_J + \Delta T_R = T_0 + \frac{P_{Joule-heating}}{G_{th}} + \frac{P_{reaction}}{G_{th}} \quad (2)$$

T_0 is the frame temperature (see Figure 1c), which is determined by the ambient temperature and

$$P_{Joule-heating} = I^2R(T) = \frac{V^2}{R(T)} \quad (3)$$

We apply voltage V to avoid thermal runaway, since the heating resistor, denoted by $R(T)$, has positive TCR (Temperature Coefficient of Resistance). See Section 4.

$P_{reaction}$ is the power released by the exothermic oxidation reaction [11].

$$\Delta T_{reaction} = \frac{P_{reaction}}{G_{th}} \quad (3a)$$

At steady state, in the absence of a reaction, the Joule heating increases the TMOS temperature as follows:

$$\Delta T_J = \frac{I \cdot V}{G_{th}} = \frac{I^2 \cdot R(T)}{G_{th}} = \frac{V^2}{R(T) \cdot G_{th}} \tag{3b}$$

where $R(T)$ is the resistor heating the reaction plate and V is the applied voltage to the heater. Equation (3) enables us to design the required resistor value, which will achieve the specific ignition temperature denoted by T* for each measured gas. G_{th} is a function of both temperature and humidity. At this point, we remind the reader that the Joule heating required to ignite the TMOS to its ignition temperature (above 100 °C) is far larger than the power released by the exothermic reaction, which is typically below 1 °C for low concentrations of analytes. Therefore, a differential electrical readout is mandatory, as described below (see Figure 3).

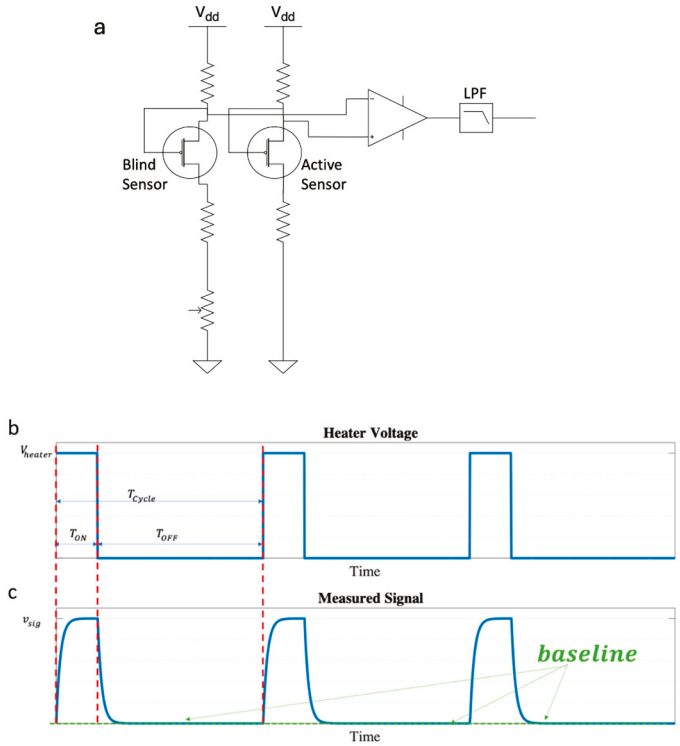


Figure 3. (**a**) Schematics of the differential, bridge-like circuit controlling the operation point at subthreshold; (**b**) the heating cycle imposed by the circuit in the form of periodic pulses, denoted by Tcycle; (**c**) the measured signal as a function of time correlates with the heater voltage pulses. The measured signal is defined relative to the baseline, which is presented. The vertical dashed red lines relate the data of (**b**,**c**) in the same time interval.

The GMOS signal voltage is directly related to the change in the output voltage of the TMOS transistor operating at a subthreshold level and the temperature increase ΔT obtained from the power released by the exothermic oxidation of the analyzed gas:

$$v_{sig} = \Delta T \left(\frac{dV_{DS}}{dT} \right)_{I_{op};T_{op}} = \frac{P_{reaction}}{G_{th,eff}} \left(\frac{dV_{DS}}{dT} \right)_{I_{op};T_{op}} \tag{4}$$

where $\frac{dV_{DS}}{dT}$ is the temperature sensitivity of the TMOS sensor at a given operation point and temperature, I_{op} and T_{op}, respectively [11,13]. The above analysis describes the relation between the temperature parameters that control the performance of the thermal sensor and the voltage parameters that are induced and measured. At this point, we remind the reader

that temperature and voltage are both intrinsic parameters (following the thermodynamic definition) and must be defined relative to a reference point. For a single pixel, the reference is the frame, which is held at T_0 and is determined by the ambient temperature and humidity. The frame is shown in Figures 1c and 4c.

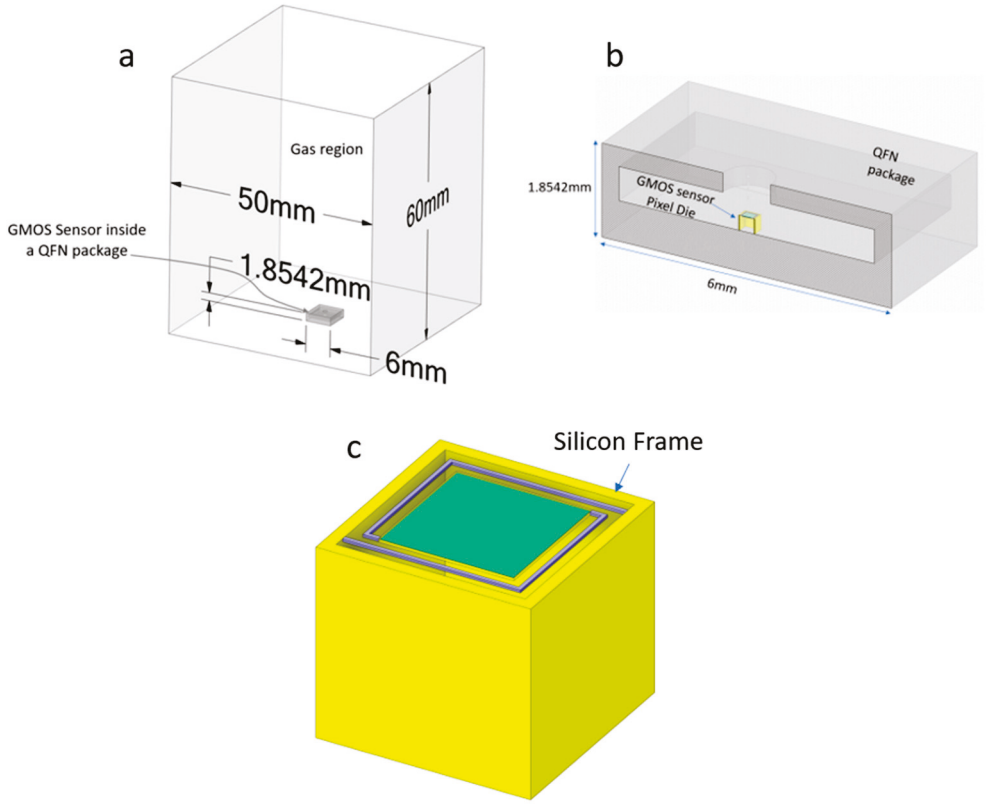


Figure 4. The model for simulation: (**a**) The gas region including the QFN (Quad Flat Non-Lead) package, simulating the gas box at the lab only smaller to reduce simulation time. (**b**) A cross-section of the QFN package where the GMOS sensor is mounted. The QFN dimensions correspond to the commercial chip carrier, which we use. (**c**) The modeled single pixel of the GMOS sensor die, where the frame is shown. The top layer is the micromachined reaction plate and held with two arms to conserve planarity.

The differential readout concept is shown in Figure 3.

The front-end analog readout is based on a "bridge-like" differential circuit, which measures the voltage difference between the GMOS sensor with the catalytic layer (dubbed "active") and an identical micro-machined TMOS without it (dubbed "blind"). The differential approach removes the baseline DC current, allowing higher dynamic range and higher accuracy. It removes the baseline drift—a major issue in the field of gas sensors [18,19].

Furthermore, since the TMOS sensor which measures the temperature increase is operated at a subthreshold level, another major challenge is to control the operation points (V-out 1 and V-out 2). The bridge-like readout addresses this issue as well. A calibration block corrects the residual mismatch between the active and blind pixels and provides the required small DC current (tens of nano-amps) needed to bring the front-end output to a mid-supply level. Calibration is performed at Joule power up and down (Joule power off) and within constant time intervals, as needed. The differential readout enhances sensitivity and selectivity and reduces drift and aging.

We now repeat the modeling by referring to what we apply and measure in the differential mode, namely, using the "blind" sensor as the reference.

$$\begin{gathered}(T-T_0)_{active}=\Delta T_J+\Delta T_R=\frac{P_{Joule-heating}}{G_{th}}+\frac{P_{reaction}}{G_{th}}\\(T-T_0)_{blind}=\Delta T_J=\frac{P_{Joule-heating}}{G_{th}}\\(T-T_0)_{active}-(T-T_0)_{blind}=\left[\frac{P_{joule-heating}}{G_{th}}\right]_{active}-\left[\frac{P_{joule-heating}}{G_{th}}\right]_{blind}+\left[\frac{P_{reaction}}{G_{th}}\right]_{active}\end{gathered} \tag{5}$$

We now assume that the T_0 of both the active and blind sensors is the same (the frame is common to both pixels). We also assume that G_{th} is the same since it is determined by the air and the environment (see simulations in Section 4).

Accordingly,

$$T_{active}-T_{blind}=\left[\frac{P_{reaction}}{G_{th}}\right]_{active} \tag{6}$$

Assuming that the electrical circuit compensates for the mismatch between the two heating channels, an increase in temperature due to the reaction is obtained.

In the absence of a reaction, we calibrate the baseline, which is the first two terms of the right side of (5). Equation (6) is affected by humidity since G_{th} is affected by humidity. However, the simulations and measurements indicate that G_{th} is determined by the ambient temperature, which is less than 50 °C in our measurements. Hence, the effect of humidity on Equation (6) is negligible.

During this calibration, when we apply the voltage step, the pixel follows the transient heat equation.

$$C_{th}\frac{d(T-T_0)}{dt}+G_{th}(T-T_0)=P_{Joule-heating} \tag{7}$$

where C_{th} is the thermal capacitance of the device. At t = 0, the first term of (7) is dominant, and we observe a "jump" in the temperature:

$$\begin{gathered}C_{th}\frac{d(T-T_0)}{dt}\sim\frac{V^2}{R(T)Gth}\\\frac{d(T-T_0)}{dt}\sim\frac{V^2}{Cth\times R(T)Gth}\end{gathered} \tag{8}$$

The decay time is determined by the thermal parameters of the pixel, namely, C_{th} and G_{th}. Since the C_{th} of humid air is larger than that of dry air, the decay towards steady state is slower in the presence of humidity, as confirmed by the measured results (see Section 5).

Once we introduce the gas, and there is an exothermic reaction, the active pixel temperature is slightly elevated, and the measured signal above the baseline is

$$\begin{gathered}\Delta T=T_{active}-T_{blind}=\left[\frac{P_{reaction}}{G_{th}}\right]_{active}\\\Delta V_{sig}=(\Delta T)\left(\frac{dV_{output}}{dT}\right)_{I_{op};T_{op}}=\frac{P_{reaction}}{G_{th}}\left(\frac{dV_{output}}{dT}\right)_{I_{op};T_{op}}\end{gathered} \tag{9}$$

As discussed above, a calibration is performed for each applied heating voltage to null the temperature difference of 5, while there is no reaction.

4. Simulation Results

The simulation tool is ANSYS Fluent 2022a [20]. The parameters of Tables 2 and 3 are mainly based on the properties reported in the software's library of materials.

Table 2. The physical properties of the gas.

	k [W/m·K]	**C [J/Kg·K]**	**Viscosity [Kg/m·s]**	**Molecular Weight [Kg/kmol]**
Dry air	See Appendix A	1006.43	1.7894×10^{-5}	28.966
Water vapor	0.0261	See Appendix A	1.34×10^{-5}	18.01534

Table 3. The physical properties of the solids.

	k [W/m·K]	c [J/Kg·K]	Density [Kg/m^3]
Tungsten	174	132	19,300
Silicon	40	700	2329
Silicon Dioxide	1.4	745	2200
Lead	35	0.13	11,342

The boundary conditions are imposed on the edges of the structure shown in Figure 4. A gas chamber with dimensions of 50 mm × 50 mm × 60 mm was modeled as shown Figure 4a. The bottom of the chamber was designated as a "wall" boundary with a fixed temperature of 300 K. The sides of the chamber were defined as "pressure inlet" boundaries, while the top was designated as a "pressure outlet" boundary. For simulations involving humid air, the thermal properties of the sides and top were set to a constant temperature of 300 K and the desired mass fraction of water vapor.

The Quad Flat Non-Lead (QFN) package, comprising lead and housing the GMOS sensor, was modeled as illustrated in Figure 4b. The dimensions of the package are 6 mm × 6 mm × 1.85 mm. A constant temperature boundary condition of 300 K was enforced on the bottom surface of the package.

Within the Fluent software environment, the Energy model was activated to facilitate thermal simulation. Furthermore, the Species Transport model was activated to capture the behavior of humid air within the computational domain. To optimize computational resources and execution time, only a single pixel of the GMOS sensor die was simulated within the QFN package. The Joule heating generated by the heating resistor was modeled as a volumetric heat source, with the power dynamically adjusted based on the heater resistance. This dynamic adjustment was necessary due to the temperature-dependent variation in the resistance of the heating element.

Figure 5 exhibits the tungsten heating resistor value as function of the temperature:

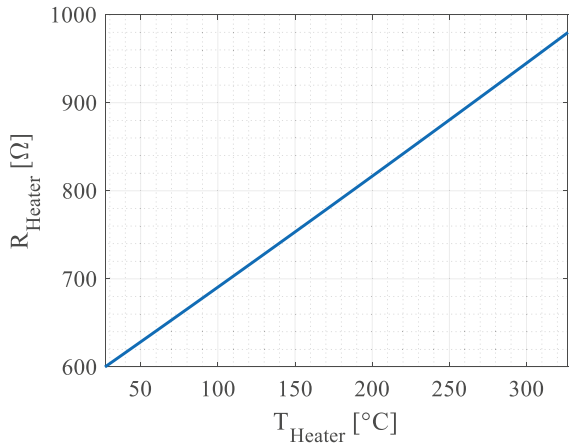


Figure 5. The tungsten heater resistance value as function of the resistor temperature. The TCR (Temperature Coefficient of the Resistor) is given by the fab that manufactured the dies [21].

$R(T)$ is given by (10)

$$R_{heater}(T) = R_0\left(1 + TCR_1 \cdot (T - T_0) + TCR_2 \cdot (T - T_0)^2\right) \quad (10)$$

where $TCR_1 = 2.05 \times 10^{-3}$; $TCR_2 = 0.2 \times 10^{-6}$.

Leveraging the capabilities of Ansys Fluent, this research utilizes computational fluid dynamics (CFD) simulations to model and analyze the temperature, relative humidity within the fluid/gas region, and the heat generated by the gas reactions. Figure 6 illustrates

the steady-state results of the simulation for an applied heater voltage of 3 V and a relative humidity of 50% in the surrounding environment.

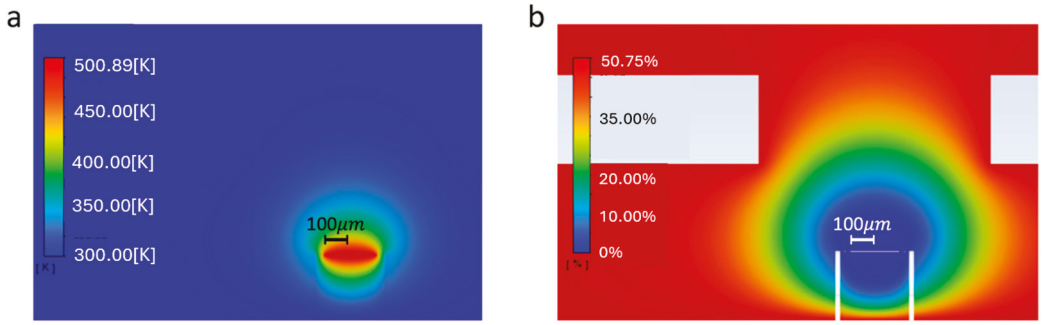


Figure 6. Steady-state simulation results: (**a**) Temperature; blue is around 300 K; the temperature is increased only in the vicinity of the heating resistor on the device; the color bar of (**a**) represents the temperature of the heated membrane (the highest temperature represented by the red color at the edge 500.89 K) and the blue color represents the temperature of the ambient at 300 K. (**b**) Relative humidity; red is around 50% relative humidity; in the vicinity of the packaged device, the relative humidity is very low because of the high temperature imposed on the reaction plate. The color bar of (**b**) represents the relative humidity near the heated membrane (the lowest relative humidity represented by the blue color at the edge 0.07%) and the red color represents the relative humidity in the ambient at 50.75%.

4.1. Steady-State Simulations

Thermal properties of the reaction membrane were determined through the analysis of simulation results. Figure 7 depicts the steady-state maximum temperature of the plating reaction of the active pixel as a function of the applied heater voltage.

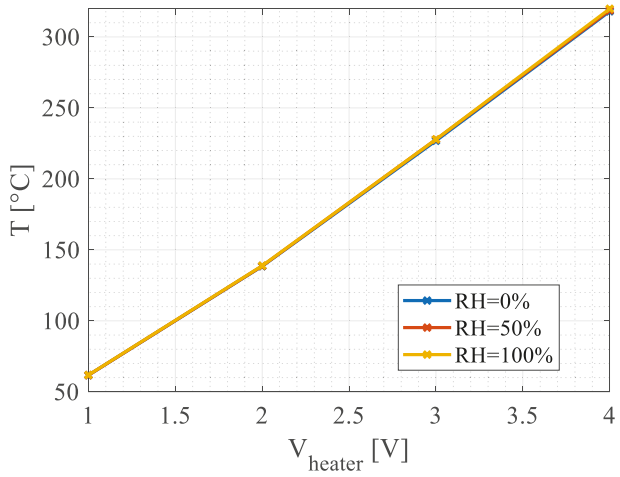


Figure 7. The reaction plate temperature of the active pixel as function of the heater voltage and the environment's relative humidity. The effect of humidity in the packaged device is small—less than 0.5 K, as shown in higher applied ignition temperatures (above 3 V).

For a given applied heater voltage, at steady state, the temperature hardly increases with humidity. This is explained below. A crucial thermal parameter for the device is its thermal conductance, denoted by G_{th}. This parameter quantifies the ease with which heat flows through the device. A lower thermal conductance results in a higher heating temperature for the thermal sensor, leading to improved responsivity.

Under steady-state conditions, the thermal conductance can be expressed as follows:

$$G_{th}(T) = \frac{P(T)}{\Delta T}\left[\frac{W}{K}\right] \tag{11}$$

Leveraging the simulation results, the thermal conductance of the device was determined. Figure 8 presents the values calculated by simulations. As expected, G_{th} increases with temperature. As explained in Section 2, for a given heater voltage and hence temperature, G_{th} is slightly reduced if humidity increases.

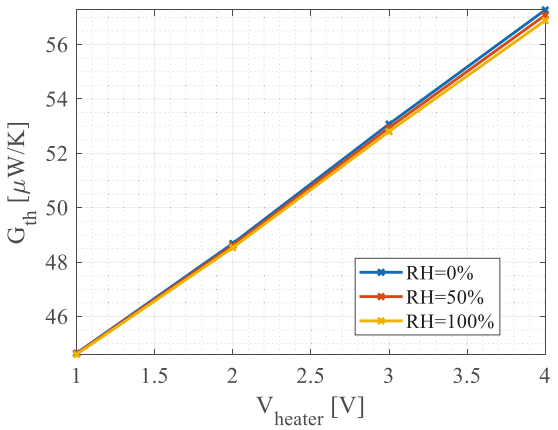


Figure 8. The device's thermal conductance as function of the heater voltage and the environment's relative humidity. *Gth* increases with temperature. At the highest heating voltage, *Gth* is slightly reduced as the relative humidity increases.

4.2. Transient Simulations

The transient response of a thermal sensor is well established and is like the exponential charging of a capacitor since temperature is an intrinsic parameter (according to the thermodynamic concept) like voltage.

The transient response of the device is approximated by the following equation:

$$T(t) = \frac{P(T)}{G_{th}(T)}\left(1 - e^{-\frac{t}{\tau_{th}}}\right) + T_0 \tag{12}$$

where T_0 is the initial temperature of the device at t = 0, and τ_{th} is the thermal time constant/response of the device. At the steady state, $T - To = P(T)/G_{th}(T) = 292.6\ [K]$; therefore, with the above equation, the thermal time constant is evaluated from the transient simulation results. From Figure 9, the thermal time constant is ~8 [ms]. It should be noted that this simulation only relates to humid air stabilization and does not include a combustion reaction.

The thermal time constant can be estimated by C_{th}/G_{th} and is given by

$$\tau_{th} = \frac{C_{th}}{G_{th}} \tag{13}$$

where C_{th} is the thermal capacitance of the device.

The operating temperature is an important feature of many gas sensors. The precise detection and control of the heater temperature is crucial for an understanding of the sensor, as this is one of the main parameters defining the sensing response (see Figure 3c). The highly sensitive temperature sensor (TMOS) implemented in the GMOS setup as a sensing element can also be used as thermometer for the detection of operating temperature. The simulated heater temperature as a function of Joule heating voltage, for various humidity values, is shown in Figure 7. These results are presented in Figures 10–13, shown below.

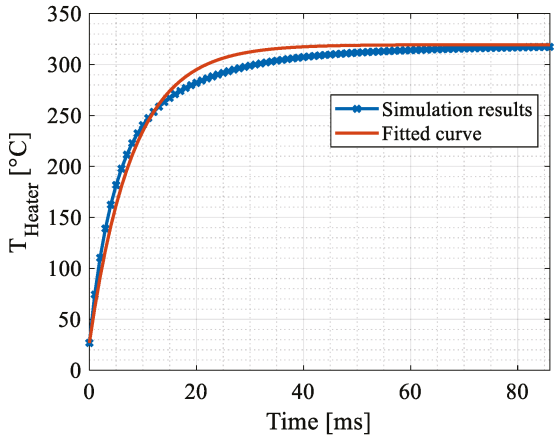


Figure 9. Transient simulation results of the heater temperature. The applied voltage was set to 4 [V] and the environmental relative humidity was set to 50%.

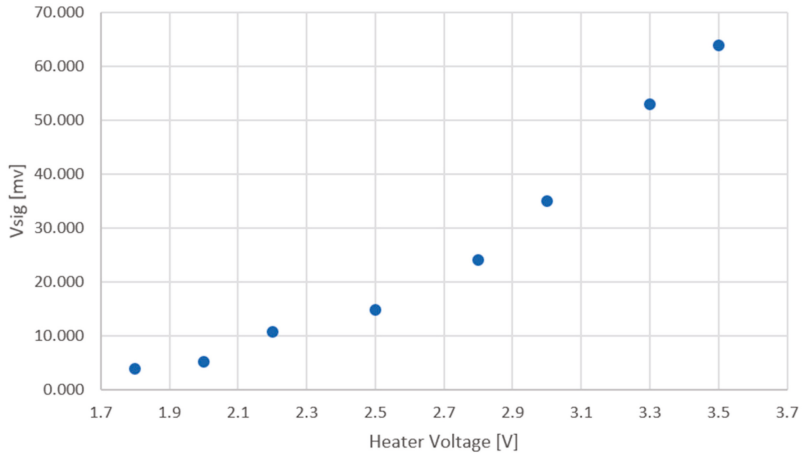


Figure 10. Measured results for 100 PPM of ethanol as an example gas, in the presence of moderate humidity of 50%. The signal voltage is plotted against the heater voltage.

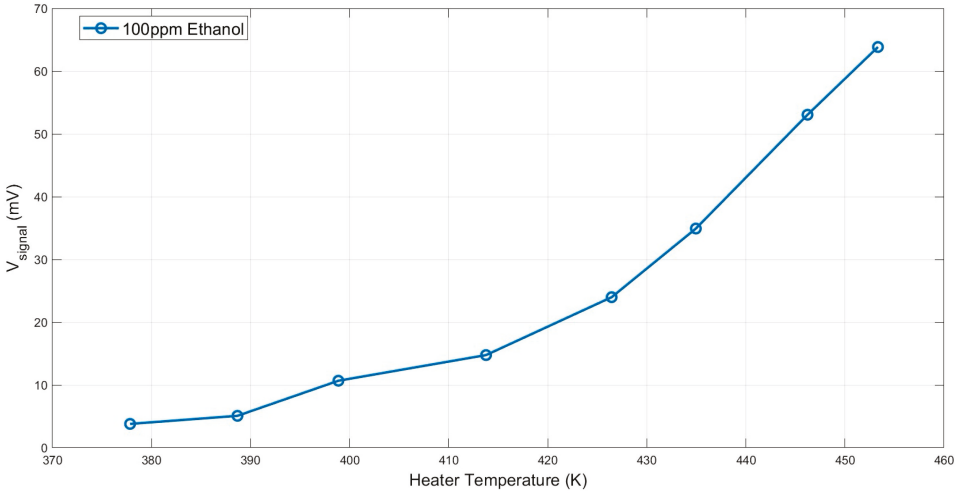


Figure 11. Measured results for 100 PPM of ethanol as an example gas, in the presence of moderate humidity of 50%, as a function of the heater temperature.

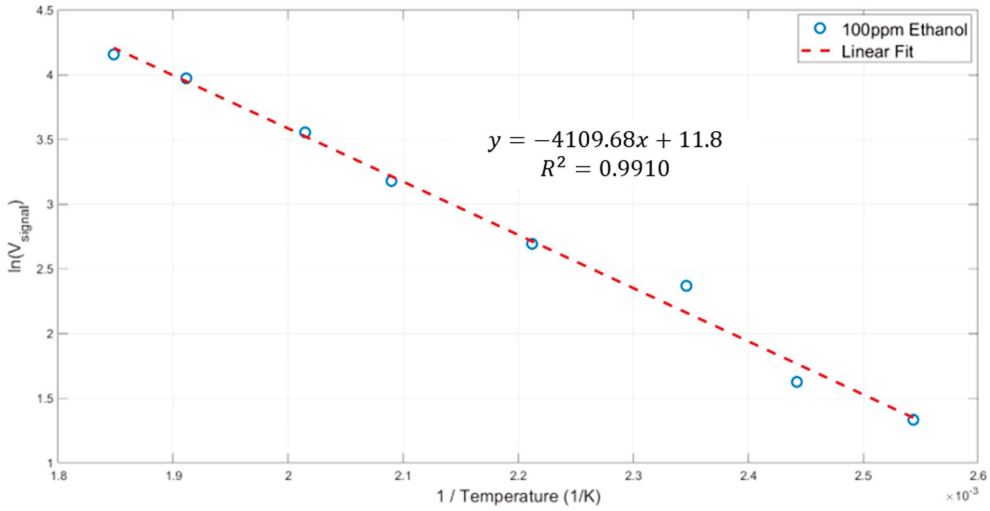


Figure 12. ln(V) signal as a function of 1/T yielding the energy of activation for ethanol.

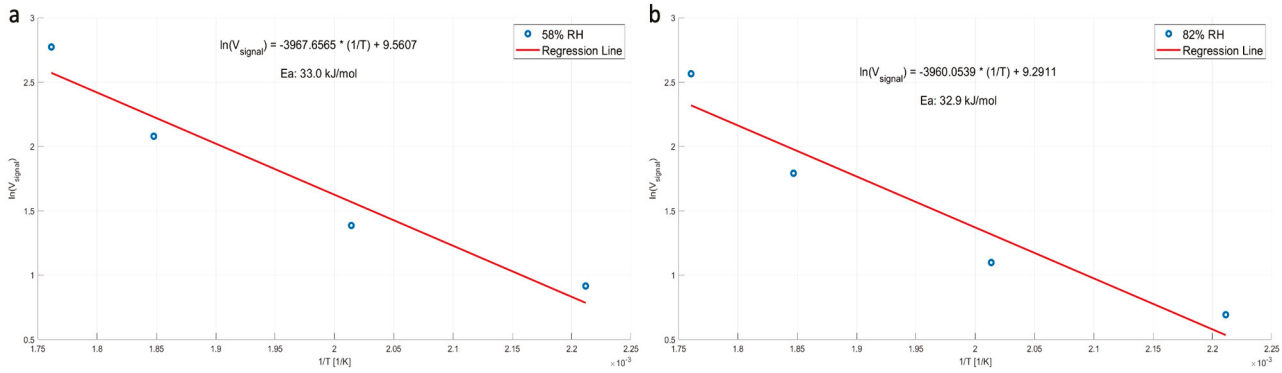


Figure 13. ln(V) signal as a function of 1/T yielding the energy of activation for 30 PPM of ethylene: (**a**) 58% relative humidity; (**b**) 82% relative humidity. The activation energy is practically the same at both humidity values. The measurements were performed at ambient (lab) temperature of 23 °C.

5. Measured Results

The measurements were performed in 6 L hermetic chamber. The humidity was maintained by a Petri dish filled with water and placed inside the chamber next to the GMOS sensing system, including gas, temperature, and humidity sensors. The gases were introduced to the chamber from calibrated gas/air mixtures (provided by GasTech, Zoringen, Germany) upon stabilization of the humidity level. The sensing procedure was repeated after the removal of water and ventilation of the chamber. The measurements were performed at an ambient (lab) temperature of 23 °C. The GMOS pixel temperatures varied from 452 K to 567 K using heater voltages of 2.5, 3.0, 3.5 and 3.8 V.

In the measurement setup described above, the temperature increase of the TMOS is translated into v_{sig}, while the heater temperature is determined by the voltage applied to the heating resistor denoted by V_{heater} depending on the humidity (see Figure 7). The value of v_{sig} is directly proportional to the gas concentration C_g, while the ignition temperature (T*) is specific to the gas for a given catalytic layer, thus enabling both the identification as well as concentration determination of the analyzed gas.

Figure 10 exhibits the measured results for 100 PPM of ethanol as an example gas, in the presence of moderate humidity of 50%.

Based on the simulation, the heater temperature on the x axis is now presented in Figure 11.

Such measurements enable us to determine the energy of activation for ethanol combustion with the ink under study.

We assume that we are in the surface reaction regime and that the measured voltage signal is determined by the Arrhenius formula. The slope yields Ea/R, where R = 8.314 J/mol·K.

The slope of 4109 × R yields Ea = 34 kJoule/mole for the ink under study. The reported Ea value of ethanol upon introduction to the metallic Pt catalyst is ~54 KJ/mol. As expected, the nanoparticle ink outperforms the metallic platinum. The energy of activation is not affected by the humidity or concentration. This is a remarkable characteristic of the GMOS sensor. It should be noted that Pt ink is not the best catalytic layer for ethanol. Ethanol is just an example gas.

Ethylene was measured and analyzed in the same manner, yielding an energy of activation of 33 kJ/mole at low and high humidity, as shown in Figure 13, for a concentration of 30 ppm.

6. Summary and Conclusions

The main research problem of this study is focused on the effect of humidity on the innovative catalytic combustion pellistor-like gas sensor, dubbed GMOS. This study is important since in real-life applications, the sensor's performance is expected to not be affected by humidity. Humid air has different thermal transport properties compared to dry air and this affects the static as well as the dynamic response of all gas sensors.

To gain an intuitive understanding of the many parameters that affect GMOS performance, we first reviewed the thermophysical properties of humid air. Surprisingly, the Web (World Wide Web) reports conflicting results and limited information for the temperature and humidity dependence of gas mixtures (dry air and water vapor) upon density, viscosity, specific heat capacity, thermal conductivity, and thermal diffusivity at total barometric pressure of 1 atmosphere [22]. Ref [22] is not new but it describes the status of the insufficient data that exists even today.

The detection mechanism of commercial chemical gas sensors relies on the chemical reaction between a gas and chemically active material. Semiconductor Metal Oxides (SMOs, also referred to as MOX), which are the most prevalent gas sensors, are affected by humidity, resulting in high drift, since the sensing oxide adsorbs water vapors [6,7,17]. Filters may be used to mitigate this issue, but this approach increases sensor cost and is never dependable for long-term service.

The problem of chemical sensor stability over time is often known as "sensor drift". It consists of non-deterministic temporal variations in the sensor's response when it is exposed to the same analytes under identical conditions. Even in commercially available MOX sensors, the drift phenomenon is still not totally understood since several contributing aspects are simultaneously present. However, as discussed above, a major cause of drift is the fact that SMO or MOX sensors adsorb water vapors [18,19].

This study presents the advantages of the GMOS sensor. The printed catalytic layer does not adsorb water and its response is stable in a wide range of humidities. We have studied the effect of humidity both experimentally as well as by simulation, in a vacuum-tight gas box, using ethanol and ethylene as the example gases. It is experimentally shown that the measured activation energy of the printed ink does not depend on humidity, thus proving that it is inert to this effect.

Humidity does affect the correlation between the applied heating voltage and the ignition temperature at high temperatures. This results in a temperature bias between the active and blind sensors. This affects the baseline of the sensor and can be solved by an optimized circuit design.

In summary, the main research problem in this study is to demonstrate the performance of the GMOS sensor in the presence of high humidity. Humidity affects the thermophysical properties of the gas under study in a conflicting and non-intuitive manner. Moreover, the overall performance of the GMOS sensor depends on many parameters, such as the readout circuit, electrical operation point, and the printed ink, as discussed in the previously reported parts. Therefore, we study here the effect of humidity by advanced simulation software, incorporating Computational Fluid Dynamics (CFD). The simulation

is validated by analytical modeling and by experiments. The bottom line of this study is that pellistor-like GMOS sensors can perform well even in the presence of humidity. Finally, a caveat: Please note that electronics hardware is not tolerant of high humidity. PCBs manufacturers offer special protective coatings to address this issue.

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Conflicts of Interest: Author Dima Shlenkevitch was employed by the company TODOS Technologies. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Appendix A. Parameters for Simulation

The thermal conductivity of air as function of the temperature is not given by the software. It is taken from [16].

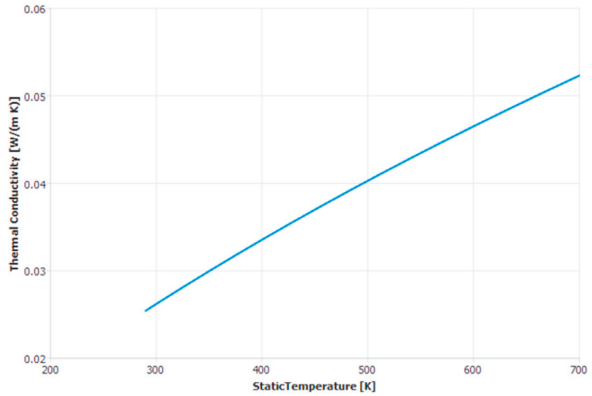


Figure A1. Air thermal conductivity as a function of the temperature.

The specific heat capacity of the water vapor as function of the temperature:

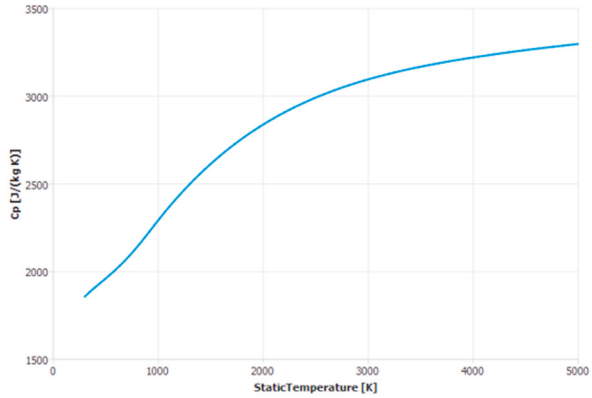


Figure A2. Specific heat capacity of water vapor as function of the temperature. Provided by the software [20] database.

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