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High-Reliability Semiconductor Devices and Integrated Circuits, 3rd Edition

Edited by
Yiqiang Chen, Yi Liu and Changqing Xu

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Guest Editors

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Editorial

Editorial for Special Issue "High-Reliability Semiconductor Devices and Integrated Circuits, 3rd Edition"

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Semiconductor devices and integrated circuits are increasingly deployed in automobiles, avionics, aerospace platforms, radiation-monitoring systems, high-power optoelectronics, and other safety- or mission-critical applications. In these fields, reliability is not determined by a single device parameter or failure mechanism. Instead, it depends on the combined influence of material properties, device structures, circuit architectures, packaging technologies, manufacturing variations, environmental stresses, and system operating conditions. Continued transistor scaling and increasing integration density make coupled aging mechanisms and circuit-level reliability modeling increasingly important, while dynamic operation, packaging interactions, ionizing radiation, and extreme environmental loads can further alter device and system performance [1–4].

Continued device scaling and system integration have therefore increased the complexity of reliability analysis. Radiation exposure may generate defects, modify charge transport and electrical parameters, and ultimately degrade device or circuit functionality [3]. Thermal cycling, mechanical loading, and other extreme conditions can initiate microstructural evolution, interfacial damage, and fatigue in electronic interconnections [4,5]. At the same time, high-performance sensing and readout circuits must maintain wide dynamic range, low noise, fast response, and acceptable power consumption under demanding operating conditions. These coupled effects motivate physics-of-failure analysis, compact and multiscale modeling, and AI-assisted design-for-reliability methods that can accelerate prediction and design optimization [1,5,6].

The Special Issue "High-Reliability Semiconductor Devices and Integrated Circuits" provides a platform for recent advances in device physics, reliability modeling, environmental-effect analysis, circuit design, numerical simulation, and engineering-oriented performance prediction. The eight contributions collected in this Special Issue cover strong-magnetic-field effects, radiation detector degradation, single-event-rate prediction, radiation-aware circuit simulation, packaging fatigue, wide-bandgap ultraviolet detectors, multimodal infrared readout circuits, and high-dynamic-range logarithmic amplifiers. Together, these works illustrate a transition from isolated reliability characterization toward multiscale, application-oriented, and design-integrated reliability research.

Liao et al. (Contribution 1) investigated the electrical behavior of vertical NPN bipolar junction transistors under strong magnetic fields. By analyzing terminal currents, current gain, carrier trajectories, potential distributions, and Hall voltage, the authors showed that magnetic fields modify the carrier distribution and current-transport path within the device. The inherent structural asymmetry of the vertical BJT produces a pronounced magnetic

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anisotropy, causing the device response to depend strongly on the direction of the applied field. Based on these observations, an interference-resistant structural design was proposed to suppress performance degradation along magnetically sensitive directions. This work provides both physical insight and a device-level optimization strategy for semiconductor components operating in complex magnetic environments.

Zhang et al. (Contribution 2) presented a multimodal CMOS readout integrated circuit for short-wave infrared image sensors. The proposed analog front end combines dual-mode buffered-direct-injection and direct-injection pixels with a column-parallel 12-bit two-step single-slope analog-to-digital converter. The readout circuit dynamically selects the injection mode according to the detector-current condition, balancing the high injection efficiency and bias stability of the buffered structure against the lower power consumption of direct injection. A four-terminal comparator and dynamic reference-voltage compensation are further introduced to mitigate charge leakage and offset. Fabricated in a 0.18 μm CMOS process for a 64 × 64 array, the circuit demonstrates a wide dynamic range, controlled noise, and practical power consumption. The work highlights the importance of adaptive circuit architectures in improving the robustness of sensor interfaces across varying signal and background conditions.

Wang et al. (Contribution 3) developed a high-dynamic-range logarithmic amplifier using a 180 nm SiGe BiCMOS process. A nine-stage fully differential limiting-amplifier chain and a ten-stage rectifier provide a dynamic range exceeding 80 dB over a wide frequency band. The proposed logarithmic-slope adjustment circuit allows the detector response to be configured through an external resistor, accommodating different input-power requirements. A dedicated power-down control mechanism reduces standby power consumption while preserving fast normal-mode response. By jointly considering dynamic range, bandwidth, response time, configurability, and power management, this work offers a practical circuit solution for radar, optical receivers, field-strength meters, and other high-precision electromagnetic measurement systems.

Du et al. (Contribution 4) revisited the prediction of single-event rates in semiconductor circuits. The study analyzes the limitations of conventional rectangular–parallelepiped and integral rectangular–parallelepiped models, particularly when linear energy transfer and measured upset cross-section are used without fully considering particle energy, particle type, target geometry, and radiation–matter interaction mechanisms. The authors derived a set of generalized single-event-rate estimation equations from the probabilistic characteristics of single-event effects and extended the traditional sensitive-volume concept by introducing an interaction volume. The resulting formulation establishes a relationship between the projected single-event area and the event-rate cross-section and can be simplified for engineering applications. Validation on representative circuits demonstrates the potential of the model for more general and physically informed radiation-rate prediction.

Ryzhov et al. (Contribution 5) proposed a radiation-aware corner-analysis methodology for CMOS analog integrated circuits. The approach combines process, voltage, and temperature variations with radiation-induced parameter shifts and is implemented using the open-source QUCS-S and Ngspice environments. A radiation-sensitive field-effect-transistor SPICE macromodel was developed to represent threshold-voltage variation with radiation dose, while percentile-based parameter extraction was used to account for device-to-device and process-corner variations. The authors further proposed a monolithic RADFET radiation sensor integrating the sensing device and CMOS readout circuit on the same die. This work extends conventional PVT analysis into a broader radiation–process–voltage–temperature design framework and demonstrates the growing potential of open-source EDA tools for high-reliability analog design.

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Kopyev et al. (Contribution 6) studied the photoresponse and internal-gain behavior of vertical Ni/β-Ga_2O_3 Schottky-barrier-diode ultraviolet detectors. The fabricated devices exhibit strong rectification, solar-blind ultraviolet sensitivity, self-powered operation, and increasing responsivity and detectivity under reverse bias. The external quantum efficiency exceeds 100%, indicating significant internal photoconductive gain. Through bias-dependent electrical and temporal characterization, the authors associated this gain with charge trapping and modulation of the effective Schottky barrier. The study clarifies the relationship between electric field, response dynamics, and internal amplification in ultra-wide-bandgap photodetectors, providing useful guidance for the design of sensitive and energy-efficient ultraviolet sensing systems.

Ouyang et al. (Contribution 7) examined the degradation of a p-NiO/β-Ga_2O_3 heterojunction X-ray detector after gamma-ray irradiation. The device was characterized under operating bias before and after exposure to a total dose of 13.5 kGy(Si). The results show that trap-assisted conduction affects the pre-irradiation response, while gamma irradiation increases the net carrier concentration and electric field in the β-Ga_2O_3, causing Poole–Frenkel emission to dominate the reverse leakage current. These changes reduce detector sensitivity, output linearity, and response speed. The work provides important evidence that even radiation detectors fabricated from nominally radiation-resistant ultra-wide-bandgap materials can undergo substantial performance degradation during long-term operation. It also emphasizes the need to evaluate detector sensitivity and radiation tolerance simultaneously rather than independently.

Cheng et al. (Contribution 8) investigated solder-layer reliability in microchannel-cooled high-power diode lasers for space applications. Using finite-element analysis and the Anand constitutive model, the authors evaluated stress, strain, and fatigue under thermal cycling and random vibration for two packaging configurations. The critical stress–strain regions were found at the solder-layer edges, with failure expected to initiate preferentially along the laser-cavity direction. Random-vibration stresses remained below the solder yield strength, indicating elastic deformation and high-cycle fatigue, whereas thermal cycling produced the dominant accumulated damage. By combining thermal and vibration damage, the study predicted the total fatigue life of both package structures and demonstrated that packaging configuration has a substantial influence on service lifetime. This contribution provides an engineering basis for reliability-oriented packaging optimization of semiconductor lasers in space environments.

Taken together, these contributions reveal several important directions in high-reliability semiconductor research.

First, reliability analysis is moving beyond conventional electrical-stress evaluation toward a broader treatment of special environments. Strong magnetic fields, ionizing radiation, thermal cycling, vibration, and high-energy particle interactions influence different physical layers of electronic systems. Their effects may begin with changes in carrier transport or defect states but can ultimately alter circuit accuracy, detector sensitivity, package lifetime, or system-level availability. Establishing the links between environmental conditions and functional performance is therefore essential.

Second, wide-bandgap and ultra-wide-bandgap semiconductors are becoming increasingly important for high-reliability sensing and power applications. The two β-Ga_2O_3-based detector studies demonstrate both the considerable advantages and the unresolved reliability challenges of these materials. High responsivity, solar-blind operation, low dark current, and self-powered detection can coexist with trap-controlled conduction, bias-dependent gain, and cumulative radiation degradation. Future work should place greater emphasis on the interaction among material defects, interface states, electric-field distribution, and long-term environmental exposure.

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Third, reliability must be incorporated into circuit and system design rather than evaluated only after implementation. The multimodal infrared readout circuit adapts its operating mode to changing detector conditions, while the logarithmic amplifier combines signal-range expansion with adjustable slope and standby-power control. The radiation-aware corner-analysis approach similarly treats radiation dose as an additional design dimension alongside process, voltage, and temperature. These examples illustrate that adaptive operation, calibration, and environment-aware simulation are increasingly important elements of reliable integrated-circuit design.

Fourth, physically grounded prediction and high-efficiency simulation remain central research needs. Generalized single-event-rate models are required as device geometries and radiation-interaction mechanisms become more complex. At the circuit level, reliability evaluation should account for statistical process variation and environmental degradation simultaneously. At the package level, fatigue models must connect localized stress–strain distributions to realistic mission profiles. Combining physical models, experimental data, statistical methods, and efficient numerical tools will be crucial for reducing evaluation cost without sacrificing credibility.

Finally, high-reliability design is inherently multiscale. Device geometry determines carrier transport in magnetic fields; defects and interfaces govern photoconductive gain and radiation degradation; circuit architectures determine noise, dynamic range, and power consumption; and packaging structures govern mechanical and thermal lifetime. Future reliability platforms should therefore support coordinated analysis across materials, devices, circuits, packages, and systems.

Further progress is expected from multiphysics digital twins, radiation-aware process design kits, uncertainty-quantified compact models, automated reliability optimization, and artificial-intelligence-assisted design-space exploration. Data-driven methods may improve parameter extraction, degradation prediction, and adaptive control, but their reliability will depend on the quality and representativeness of the underlying physical and experimental data. The most promising direction is therefore not to replace physical analysis with intelligent methods, but to integrate physical knowledge, numerical simulation, experimental validation, and machine learning into a unified reliability-design framework.

The studies presented in this Special Issue demonstrate the diversity and vitality of current research on high-reliability semiconductor devices and integrated circuits. They also show that reliable electronic systems require coordinated advances in materials, device structures, circuit techniques, environmental modeling, and packaging design. We hope that these contributions will stimulate further interdisciplinary research and support the development of more robust semiconductor technologies for automobiles, aerospace systems, radiation environments, sensing platforms, and other demanding applications.

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List of Contributions:

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Article

Analysis and Optimization of Vertical NPN BJT for Strong Magnetic Fields

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Abstract: This study systematically investigates the electrical characteristics of the vertical NPN bipolar junction transistor (VNPN BJT) in the strong magnetic field environment, focusing on analyzing the effects of magnetic field direction and intensity on key parameters such as terminal current and current gain (β). The simulation results show that the magnetic field induces changes in the carrier distribution, thereby affecting the current transport path. Through the in-depth analysis of electron motion trajectories, potential distribution, and Hall voltage, this paper reveals the physical mechanisms behind the device's characteristic changes under the magnetic field and discovers that the inherent asymmetry of the BJT structure induces significant magnetic anisotropy effects. On this basis, a design for interference-resistant structures in strong magnetic field environments is proposed, effectively suppressing the adverse effects of magnetic-field-sensitive directions on BJT performance and significantly improving the device's stability in complex magnetic field environments.

Keywords: BJT; magnetic field; asymmetry; current gain

1. Introduction

In strong magnetic field environments, the transport behavior of charge carriers within semiconductors can be profoundly altered. Phenomena such as current path reconfiguration, carrier mobility degradation, and voltage drift emerge, leading to significant variations in device parameters and functional reliability. In lightly doped silicon, the magnetic field alters the space-charge regions, resulting in a pronounced magnetoresistive effect [1,2].

Experimental investigations have confirmed the presence of such magnetoresistive phenomena in a range of semiconductor devices, including p–n junctions, MOSFETs, and JFETs [3–6]. Moreover, optoelectronic components such as avalanche photodiodes and silicon-based light-emitting diodes exhibit notable variations in performance when subjected to high magnetic fields, reflecting the broader influence of magnetic environments on both electronic and photonic functionalities [7–9]. Therefore, studying the behavior of semiconductor devices under strong magnetic fields is of both significant theoretical interest and practical engineering value for device design and application in high-magnetic-field environments. For bipolar junction transistors (BJTs), their behavior under a magnetic field is more complex due to the presence of multiple PN junctions, exhibiting strong directional and nonlinear characteristics.

This paper addresses the above issues by establishing a vertical NPN BJT model using the Sentaurus TCAD simulation platform (Version 0-2018.06-SP2). We analyze the effects of different magnetic field strengths on the device's electrical behavior in two typical magnetic field directions: perpendicular to both the device surface and the main current direction. The research objectives include the following: systematically evaluating the impact of magnetic field on the BJT's output characteristics, current gain, as well as the variations in collector, base, and emitter currents; revealing the carrier path deviation induced by the magnetic field, Hall voltage formation, potential distribution changes, and depletion region expansion; constructing and explaining the physical mechanisms of performance degradation in BJTs under magnetic fields; and providing a theoretical basis for the future optimization and anti-magnetic design of BJT structures in magnetic field environments.

2. Model and Methods

This paper models a standard silicon-based VNPN structure, as illustrated in Figure 1.

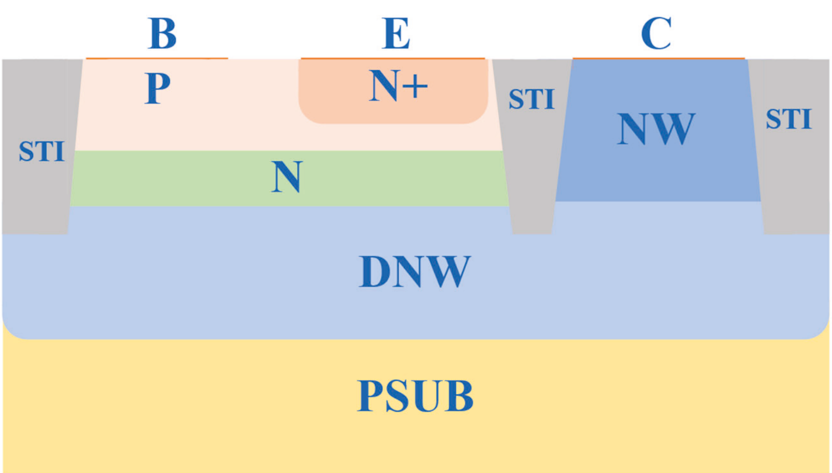

Figure 1. Structure of the standard vertical NPN BJT device.

The main mobility models for semiconductor carriers include lattice vibration scattering, ionized impurity scattering, and Coulomb scattering between carriers. These three types of scattering are interrelated, and their contribution to total mobility is defined as μ_1. After an external magnetic field is applied, carriers are scattered by the magnetic field, further altering their mobility. The mobility induced by the magnetic field is referred to as Hall mobility μ_{hall}. According to the Hall effect model, the relationship between conductivity σ and Hall mobility is given by the following [10]:

$$\mu_{\text{hall}} = |R_H \sigma| \tag{1}$$

where R_H represents the Hall coefficient. The total mobility considering the magnetic field effect is given by the following:

$$\mu = \frac{\mu_I \mu_{hall}}{\mu_I + \mu_{hall}} \tag{2}$$

Under a steady-state magnetic field, the transport behavior of electrons and holes is influenced by the Lorentz force, causing their effective mobility to change, which in turn affects the current density. The corrected expressions for electron and hole current densities are given by the following [11]:

$$J_n{}^* = \frac{1}{1 + (\mu_n{}^* \mathrm{B})^2}[(q\mu_n n\mathrm{E}) + (q\mathrm{D_n}\nabla n) + \mu_n{}^*\mathrm{B} \times (q\mu_n n\mathrm{E} + q\mathrm{D_n}\nabla n)] \tag{3}$$

$$J_p{}^* = \frac{1}{1 + (\mu_p{}^* \mathrm{B})^2}[(q\mu_p p\mathrm{E}) + (q\mathrm{D_p}\nabla p) + \mu_p{}^*\mathrm{B} \times (q\mu_p p\mathrm{E} + q\mathrm{D_p}\nabla p)] \tag{4}$$

where J_* denotes the current density contributed by either electrons or holes, while μ_* represents the corresponding mobility. q is the elementary charge and n and p are the electron and hole concentrations, respectively. The electric field strength is denoted by E, and the magnetic flux density is denoted by B, and both are treated as vectors. Additionally, D_* stands for the diffusion coefficient associated with the respective carriers.

These equations indicate that when a magnetic field B is applied perpendicular to the current direction, the densities of electrons and holes change. These changes affect the distribution of current density and the transport mechanism [12–15]. Therefore, under the influence of the magnetic field, the conductive characteristics of the BJT must be recalculated and analyzed. This is carried out based on the corrected mobility and current density equations shown in Formulas (3) and (4), which describe the working state of the PN junction device in the magnetic field.

In this study, the applied magnetic field is directed perpendicular to the modeled 2D plane. The direction pointing outward from the plane is defined as the positive Z-direction, while the direction pointing inward is defined as the negative Z-direction. The effect of the magnetic field on carrier mobility is mainly reflected in the shift in their motion direction, which can be analyzed based on the direction of the Lorentz force. According to the previous theoretical analysis and the Lorentz force expression $F = qv \times B$, the trajectories of the carriers are altered under the magnetic field, thereby modifying the overall current transport direction. These trajectory shifts under both positive and negative Z-direction magnetic fields are illustrated in Figure 2, which depicts the motion of electrons in the BJT influenced by the Lorentz force.

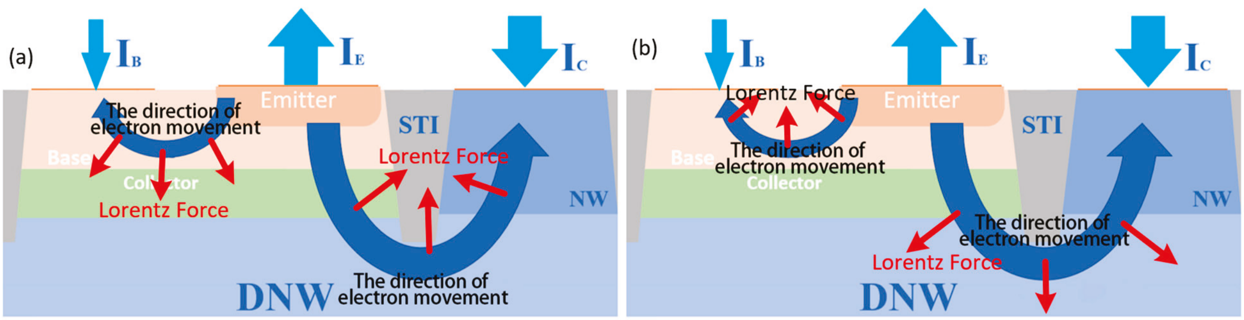

Figure 2. The direction of electron motion in the BJT under the influence of the Lorentz force for (**a**) positive Z-direction magnetic field and (**b**) negative Z-direction magnetic field, respectively.

3. Results and Discussion

3.1. The Change in Carrier Density Inside the Device

The main impact of the magnetic field on a BJT occurs in the active region, where it alters the direction of carrier motion, thereby changing the carrier distribution. As shown in Figure 3, the current density in the active region exhibits the most significant variation under the magnetic field. The framed region is the active area, where the current density changes most significantly under the magnetic field. A clear reduction in the current density is observed as the magnetic field strength increases, with a more pronounced decrease under the negative Z-direction magnetic field. In contrast, for the carriers in the buried layer and deep well, the change in current density due to the magnetic field is minimal.

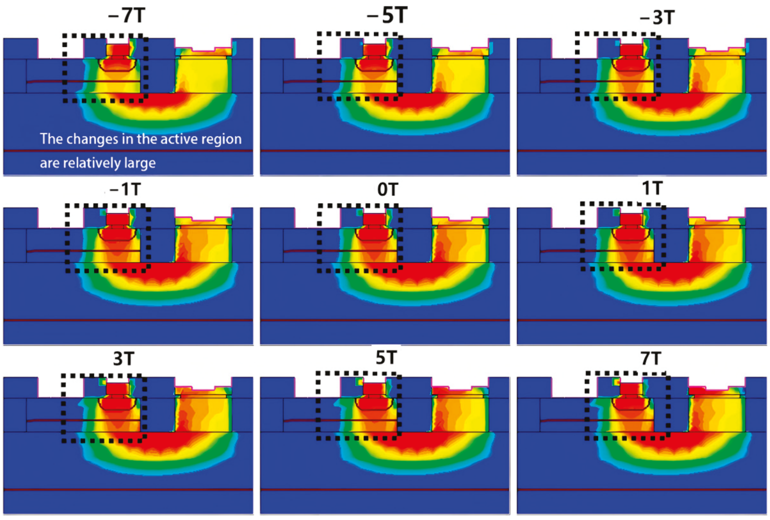

Figure 3. Current density distributions of the BJT under the magnetic field with different directions and strengths.

3.1.1. Change in Collector Current Formation

For the collector current, the relationship to be followed is as follows:

$$I_C = I_{nc} + I_{rb} + I_{CBO} \tag{5}$$

where I_{nc} represents the main current formed by electrons flowing through the collector region, I_{rb} is the recombination current in the base region, and I_{CBO} is the reverse saturation current. The reverse saturation current I_{CBO} is a small current generated by the reverse bias of the PN junction between the collector and the base. Its value is usually very small and can typically be neglected. In practical cases, the collector current I_C is mainly contributed by I_{nc}, so in the analysis of collector current, I_{rb} and I_{CBO} can be neglected, and only the dominant role of I_{nc} in the overall output current is discussed.

When a magnetic field along the negative Z-direction is applied, the electrons forming the collector current I_{nc} in the active region shift to the left, causing an overall leftward shift in the carriers. The degree of this shift becomes more significant as the magnetic field strength increases. Although the total mobility remains unchanged, the transverse mobility increases relative to the longitudinal mobility, which decreases. Given that the primary direction of carrier movement in the active region of a VNPN device is longitudinal, the decrease in longitudinal mobility directly leads to a reduction in the effective mobility, which in turn causes a decrease in the collector output current I_C. In Figure 4, the black arrows represent the velocity vectors of electrons, where the direction indicates the motion direction and the length reflects the motion velocity. The white arrows indicate the direction of the Lorentz force acting on the electrons. It is observed that the magnetic field causes a noticeable deflection in the electron trajectories but has little effect on their absolute velocity. This suggests that the magnetic field mainly alters the direction of carrier motion rather than significantly changing their mobility. In Figure 5, under the negative Z-direction magnetic field, I_{nc} shifts leftward, while under the positive Z-direction magnetic field, it shifts rightward. As shown in Figures 4 and 5, the application of a negative Z-direction magnetic field leads to a clear leftward shift in electron motion direction and a corresponding leftward deviation in current density within the active region.

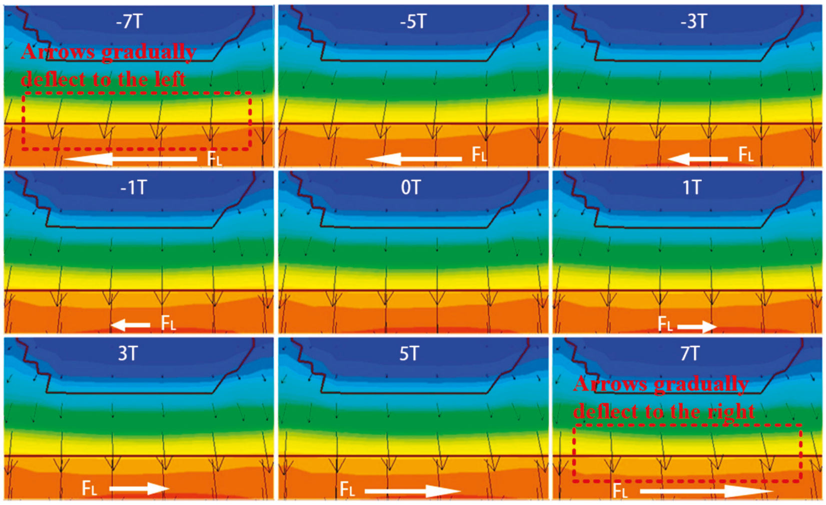

Figure 4. Velocity vectors of electron motion in the active region under different magnetic field directions and strengths.

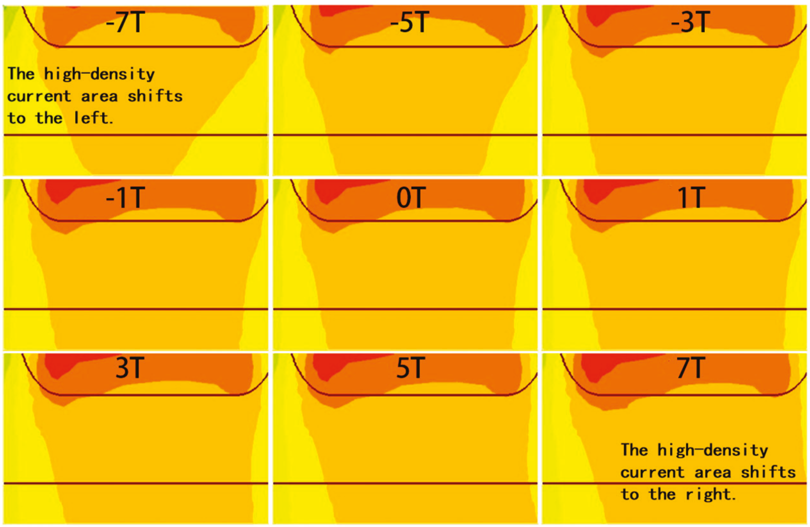

Figure 5. Variation in I_{nc} in the active region under magnetic fields from −7 T to 7 T.

In contrast, when a magnetic field along the positive Z-direction is applied, the electron movement direction shifts to the right, causing the carriers in the active region to also shift rightward, leading to a similar decrease in effective mobility. However, due to the structure of the VNPN device, the active region's right side is adjacent to the shallow trench isolation (STI) region. During the transverse shift, the electrons encounter this insulating structure, and their motion is halted. As a result, electrons accumulate at the boundary between the active region and the STI region. This accumulation of electrons further induces the establishment of a Hall voltage, which compensates, to some extent, for the carrier displacement caused by the magnetic field. Due to this mechanism, the effect of a positive Z-direction magnetic field on the collector current is noticeably weaker than that of a negative Z-direction magnetic field, which means that the decrease in I_C is less under the positive Z-direction magnetic field. Figures 4 and 5 also illustrate the rightward shift in electron motion direction and the corresponding drift of current density toward the STI boundary under the positive magnetic field. As shown in Figure 6, under the positive Z-direction magnetic field, there is a clear accumulation of electrons at the right-hand boundary, which leads to a local reduction in potential. In addition, the electric field within the active region slightly tilts to the right, indicating that the Hall voltage has been superimposed on the original internal electric field.

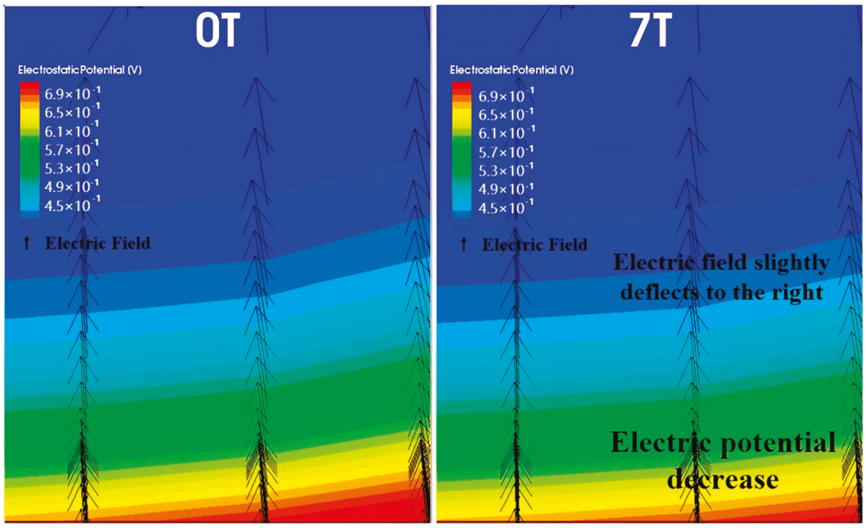

Figure 6. Electron accumulation on the right side due to the positive Z-direction magnetic field, creating a Hall voltage and lowering the potential on the right side of the active region.

Under the condition that the voltages at the three device terminals remain equal, applying an external magnetic field usually leads to a decrease in the collector current I_C, with the current decay becoming more pronounced as the magnetic field strength increases. Overall, the suppression effect of the negative Z-direction magnetic field on the device current is significantly stronger than that of the positive Z-direction magnetic field. When the magnetic field strength is −7 T, the collector current decreases by the maximum amount, reaching 5.52%.

Since the emitter current I_E is typically approximated as equal to the collector current, the trends of the two currents are highly consistent, as shown in Figure 7. As I_C decreases, the emitter current also shows a similar decreasing behavior. It is worth noting that the current does not decrease in the range of 0–2 T; instead, a slight increase is observed. This suggests that a weak magnetic field in the positive Z-direction may facilitate current transport by reducing the carrier drift distance. At the magnetic field of −7 T, the decrease in I_E reaches its maximum value of 5.77%. These results further confirm the significant impact of the magnetic field, especially the negative Z-direction magnetic field, on the current transport characteristics of the device.

3.1.2. Change in Base Current Formation

For the base current, ignoring the reverse saturation current I_{CBO}, the relationship to follow is as demonstrated below:

$$I_B = I_{pe} + I_{rb} \tag{6}$$

where the base hole drift current I_{pe} represents the current formed by holes drifting across the emitter junction. According to the mobility expression under the magnetic field, the effective carrier mobility in a magnetic field is inversely proportional to the square of the mobility under the zero magnetic field condition. Therefore, the greater the mobility under the zero magnetic field, the more significant the change in mobility caused by the magnetic field. Since the intrinsic mobility of holes is about one-fourth that of electrons, the change in mobility under the magnetic field is relatively small. In the device simulation of this study, it was observed that even under a strong magnetic field of up to 7 T, the change in the hole current density remains extremely weak. Hence, when analyzing the magnetic field's effect on the base current, the hole drift current I_{pe} can be considered almost unchanged. As shown in Figure 8, the spatial distribution of the hole current density in the base region exhibits no significant change under the influence of the magnetic field.

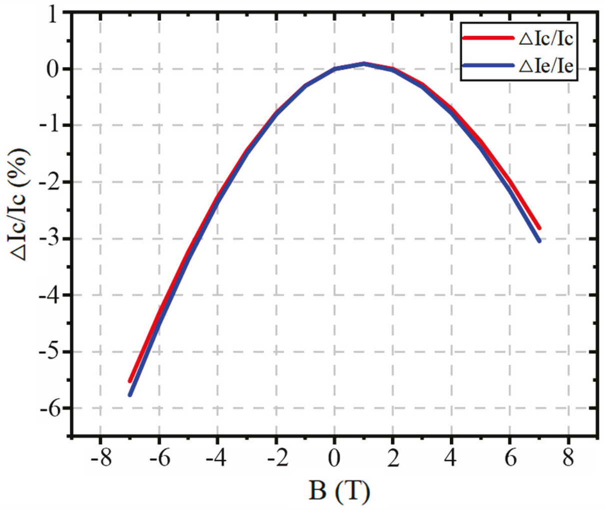

Figure 7. Collector and emitter currents generally show a decreasing trend as the magnetic field strength increases, with greater suppression under the negative Z-direction magnetic field.

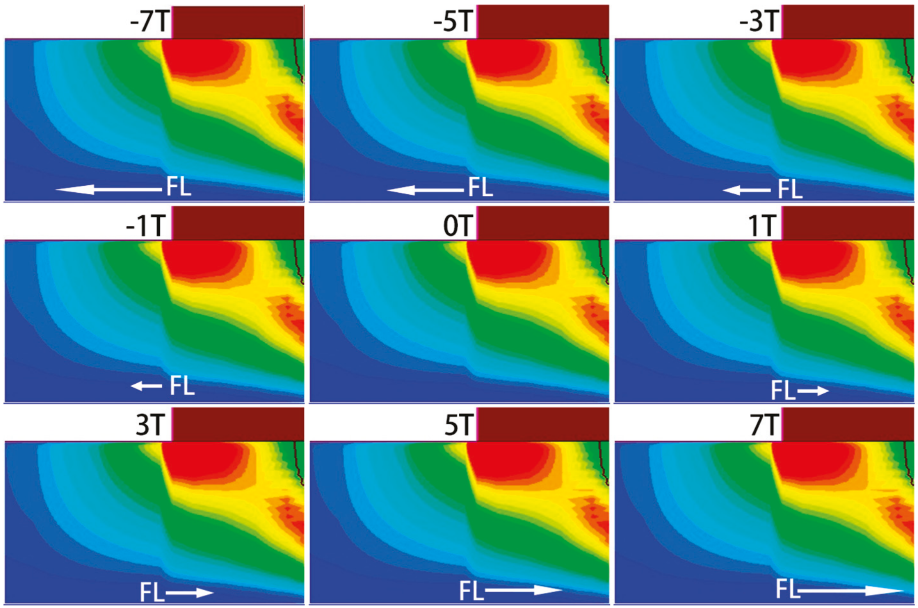

Figure 8. The effect of the magnetic field on the hole current in the base region is minimal.

The recombination current I_{rb} is analyzed based on the recombination rate R_v and the effective area of recombination. This analysis focuses only on non-radiative recombination in the BJT, including SRH recombination and Auger recombination.

The relationship between recombination current density and recombination rate is usually given by the following:

$$J_{rec} = q \cdot R_V \cdot A \tag{7}$$

where R_v is the recombination rate and A is the effective recombination area.

Both the SRH recombination rate R_{SRH} and Auger recombination rate R_{Auger} show the same trend under the magnetic field. As illustrated in Figures 9 and 10, which show the spatial distributions of SRH and Auger recombination rates, respectively, the recombination rate and recombination area both decrease to some extent under a positive Z-direction magnetic field, while both increase significantly under a negative Z-direction field. In Figures 9 and 10, the positive Z-direction magnetic field reduces the recombination area and rate, while the negative Z-direction magnetic field increases both. The change in the recombination area is closely related to the redistribution of carriers in the base region. The magnetic field influences electron trajectories, altering the recombination behavior in the base region. Under the negative Z-direction magnetic field, electrons in the base region are more likely to recombine, leading to an increase in the recombination current J_{rec}. In contrast, under the positive Z-direction magnetic field, the recombination process is somewhat suppressed, resulting in a decrease in J_{rec}.

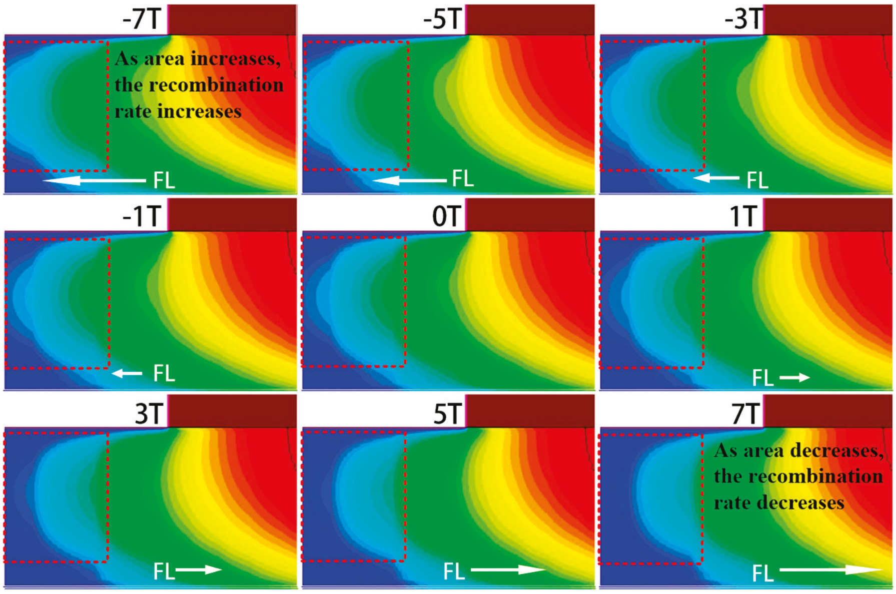

Figure 9. Change in SRH recombination rate R_{SRH}.

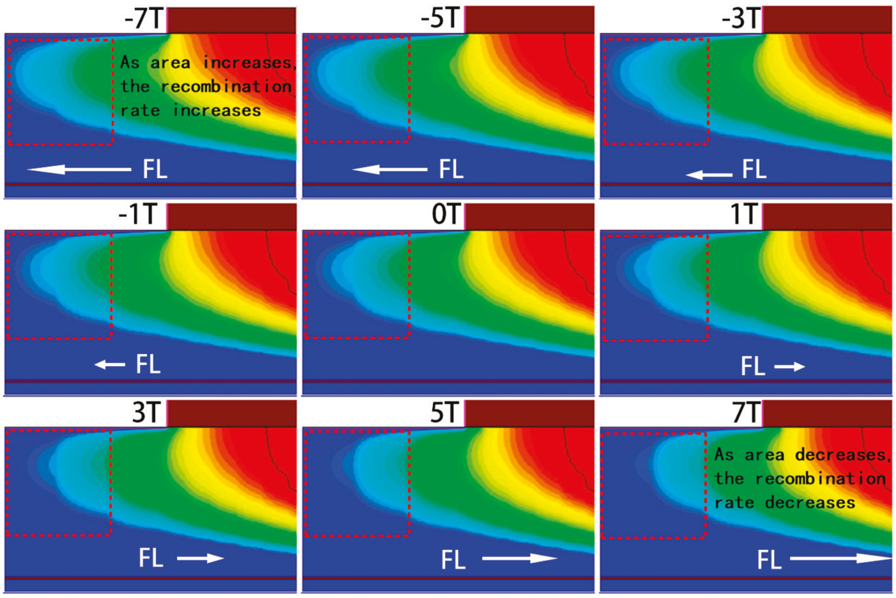

Figure 10. Change in Auger recombination rate R_{Auger}.

Therefore, for the base current, as the magnetic field strength increases, the base current also increases. As shown in Figure 11, the base current increases significantly under the negative Z-direction magnetic field, while it decreases under the positive Z-direction field. In the TCAD simulation, the base current reaches its maximum at 7 T in the negative Z-direction, increasing by more than 40%. Contrastively, in the positive Z-direction, the base current decreases by up to 4.2% with a magnetic field strength of 7 T. This result further demonstrates that the negative Z-direction magnetic field has a stronger enhancing effect on the base current.

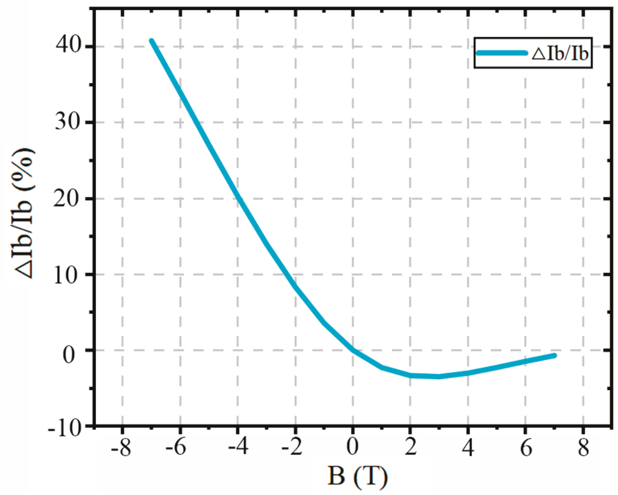

Figure 11. The base current increases significantly under the negative Z-direction magnetic field, while it decreases under the positive Z-direction magnetic field.

3.2. Variation in BJT Current Gain

The Z-direction magnetic field changes the recombination behavior in the base region and generally suppresses the collector current, resulting in a variation in the BJT's current gain. Based on the expressions for collector and base currents, the current gain of the BJT can be defined as follows:

$$\beta = \frac{I_{nc}}{I_{pe} + I_{rb}} \tag{8}$$

When a negative Z-direction magnetic field is applied, the dominant collector current I_{nc} decreases with the increasing magnetic field strength, while the base recombination current I_{rb} increases significantly. The hole current I_{pe} which is less sensitive to changes in the magnetic field, remains almost constant. Therefore, under a negative Z-direction magnetic field, the current gain of the BJT decreases. In contrast, under a positive Z-direction magnetic field, although I_{nc} also decreases with increasing magnetic field strength, I_{rb} shows a slight decrease, with the change being smaller than that of I_{nc}. The slight reduction in the base current partly compensates for the decrease in collector current, so while the current gain still decreases under the positive Z-direction magnetic field, the reduction is less pronounced compared to that of the negative Z-direction magnetic field. It is worth noting that in the range of 0–2 T under the positive Z-direction magnetic field, a slight increase in I_c is observed, resulting in a minor enhancement in the current gain β around the magnetic field strength of 2 T.

As shown in Figure 12, from the simulation, it is observed that as the magnetic field strength increases, the output current of the device gradually decreases. As the magnetic field strength increases, the output current decreases overall, with the negative Z-direction magnetic field causing a more significant suppression effect compared to the positive Z-direction magnetic field. This highlights the anisotropy of the device's response to the magnetic field. This trend is particularly evident under the negative Z-direction magnetic field, and its magnitude is significantly greater than that observed under the positive Z-direction field. By further plotting the relationship between current gain β and magnetic field, with the β value at a base current of I_B = 10 μA as a representative indicator, the simulation results show that β generally continues to decrease with the increasing magnetic field strength, with a more significant drop under the negative Z-direction magnetic field. To provide a more intuitive depiction of the magnetic field's effect on the device's amplification ability, a normalized metric MR(β) is introduced. The normalization formula is as follows:

$$\mathrm{MR}(\beta) = \left(\frac{\beta_B - \beta_0}{\beta_0}\right) \times 100\% \tag{9}$$

where MR(β) represents the change in the current gain β under the magnetic field, β_B is the current gain under different magnetic field conditions, and β_0 is the initial value of β without the magnetic field. This formula shows the variation in β under different magnetic field conditions, and based on this formula, we further plot the relationship curve of MR(β) with the magnetic field B. From Figure 13, it is clearly evident that the negative Z-direction magnetic field has the most significant effect on the current amplification ability of the BJT.

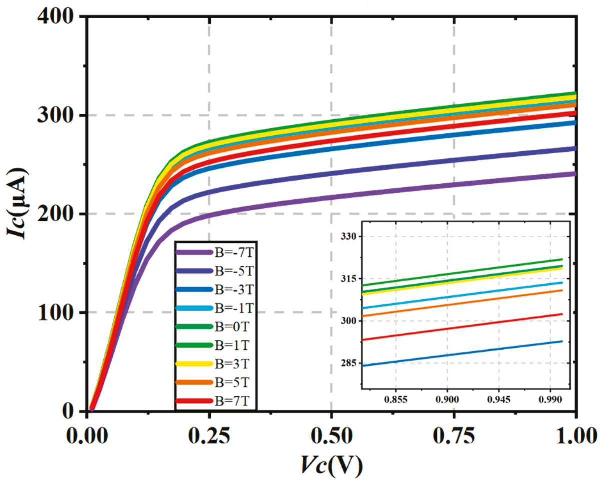

Figure 12. Output characteristics of the BJT under the magnetic field ranging from −7 T to +7 T.

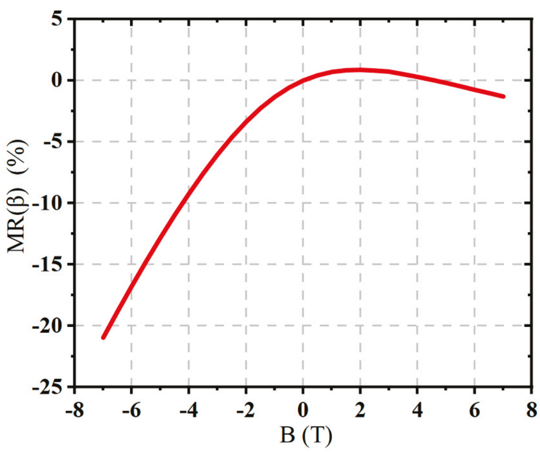

Figure 13. MR(β) as a funtion of the magnetic field B for the BJT. The current gain decreases overall as the magnetic field strength increases, with a significantly larger drop under the negative Z-direction magnetic field.

4. Structure Optimization

Based on the above analysis, the magnetic field direction that most significantly impacts the electrical performance of the BJT is the negative Z-direction. The main reason for this is the asymmetry present in the device structure. Under the positive Z-direction magnetic field, the shallow trench isolation (STI) region on the right side of the base effectively prevents carriers from further shifting to the right. However, in the negative Z-direction magnetic field, there is no corresponding structural barrier on the left side of the device, causing the carrier's shift path to extend, thereby making the influence of the magnetic field more pronounced.

To address this asymmetry effect, this paper proposes a structural optimization scheme to enhance the stability of the device under strong magnetic fields. Specifically, on the traditional VNPN structure, an additional STI structure (referred to as the second STI region) is added to the left side of the emitter region and the right side of the base electrode, as shown in Figure 14. Its depth is similar to that of the BE junction but slightly smaller than the original STI depth, ensuring that the intervention on carriers is controlled and does not affect the normal conduction path.

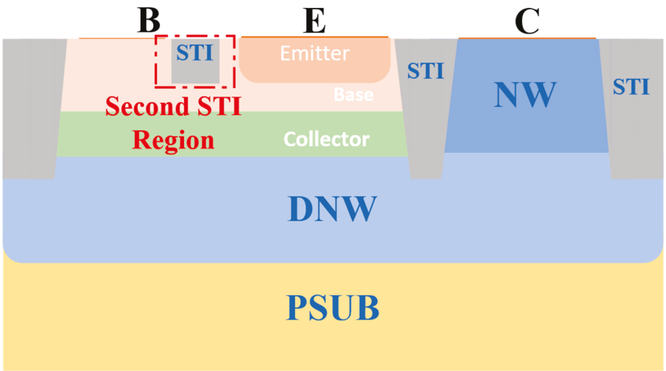

Figure 14. The optimized structure resistant to strong magnetic interference.

After the addition of the second STI region, the electron motion direction inside the BJT is illustrated in Figure 15.

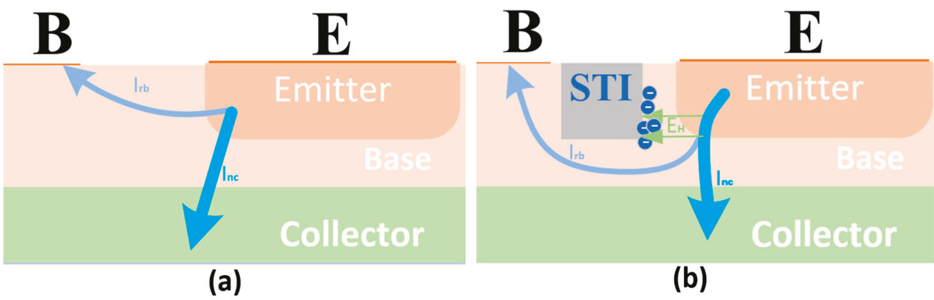

Figure 15. Motion paths of electrons in the base region under negative Z-direction magnetic field: (**a**) before optimization; (**b**) after optimization. Overall, the STI region accumulates carriers and generates a Hall field that induces a Lorentz force opposite to the magnetic deflection, thereby correcting the carrier trajectory. It also ensures that the recombination path of Irb remains extended regardless of the presence of a magnetic field, improving the current stability.

The significant enhancement of the base recombination current I_{rb} under the negative Z-direction magnetic field is the main factor leading to the decrease in current gain β. Therefore, the core goal of the optimization design is to suppress the increase in I_{rb} induced by the negative Z-direction magnetic field and balance the shift behavior of the dominant current I_{nc} under the magnetic field. The newly added second STI region can effectively suppress the transverse shift in carriers under the negative Z-direction magnetic field, thus hindering the shortening of the recombination path and reducing the loss due to the base recombination current. Additionally, this STI structure limits the excessive shift in I_{nc}, suppressing the increase in its path under the negative Z-direction magnetic field, which would otherwise reduce the effective mobility.

Furthermore, the spatial accumulation of electrons in the second STI region helps establish a Hall voltage. The electric field generated by this voltage has an opposite direction to the Lorentz force, thus partially counteracting the magnetic field's driving effect on carrier displacement. This mechanism further stabilizes the transmission path of I_{nc}, effectively reducing the interference of the magnetic field on the transport of the dominant current.

Figure 16 shows the electron density distributions in the structures with and without the second STI region under both zero magnetic field and negative Z-direction magnetic field conditions. For the original BJT structure, under the negative Z-direction magnetic field, the main conductive region in the base experiences a decrease in the electron density due to the displacement of electrons. However, in the optimized structure, the second STI region blocks the further displacement of electrons, significantly slowing down the decrease in electron density under the negative Z-direction magnetic field, thus effectively reducing the impact of the negative Z-direction magnetic field on the BJT and improving the stability of the device in the strong magnetic environment. The optimized structure effectively mitigates the electron displacement caused by the magnetic field, resulting in a smaller reduction in the electron density and improved current stability.

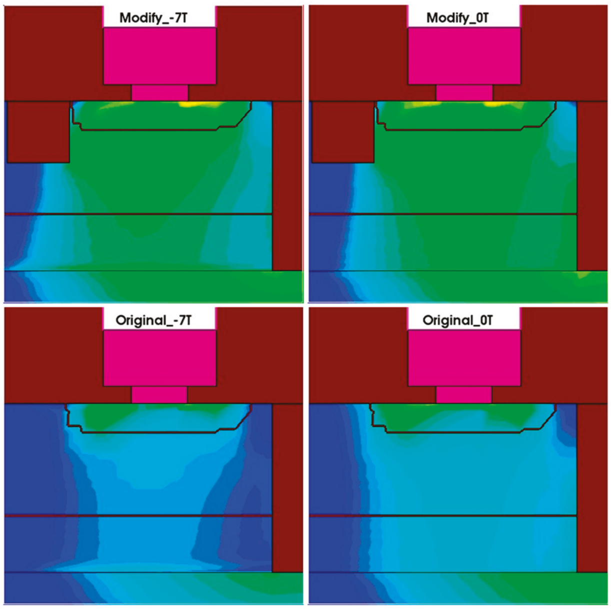

Figure 16. Comparison of electron density distributions in the active region under the negative Z-direction magnetic field and zero magnetic field for both the original and optimized structures.

Figure 17 shows the changes in the recombination regions in the structures with and without the second STI region under zero magnetic field and negative Z-direction magnetic field. The recombination region in the optimized structure is less affected by the magnetic field, indicating that Irb is also less influenced. Under the negative Z-direction magnetic field, the motion trajectory of electrons forming the recombination current I_{rb} increases, causing the recombination region to expand, which leads to an increase in the base current and a subsequent decrease in the current gain. After introducing the second STI region, the effect of the negative Z-direction magnetic field on the recombination current and recombination region is suppressed, limiting the increase in the base current, thus effectively slowing down the decrease in the current gain.

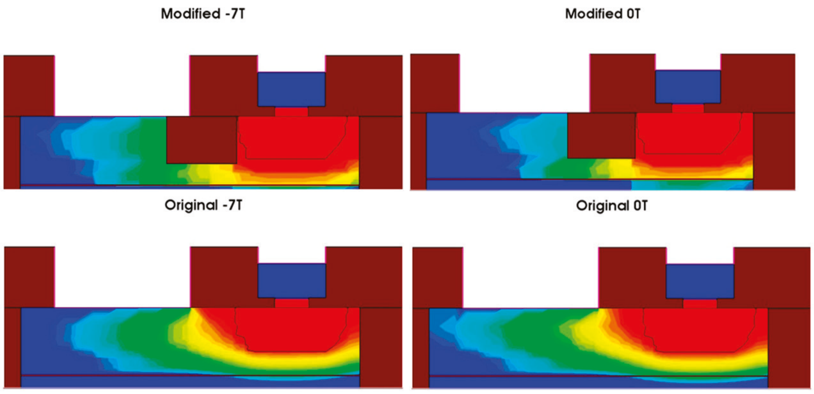

Figure 17. Comparison of recombination regions in the optimized and original BJT structures under negative Z-direction magnetic field and zero magnetic field.

Figure 18 compares the MR(β) curves of the original and optimized BJT structures, with and without the second STI region. As shown in Figure 18, the improved structure significantly enhances the resistance to the negative Z-direction magnetic field. Under a 7 T magnetic field along the negative Z-direction, the MR(β) of the original BJT is -42.9%, while the MR(β) value of the optimized structure decreases to -4.61%. This represents a reduction of nearly 10 times, demonstrating the optimization effect of the second STI region on the BJT's resistance to the strong magnetic interference.

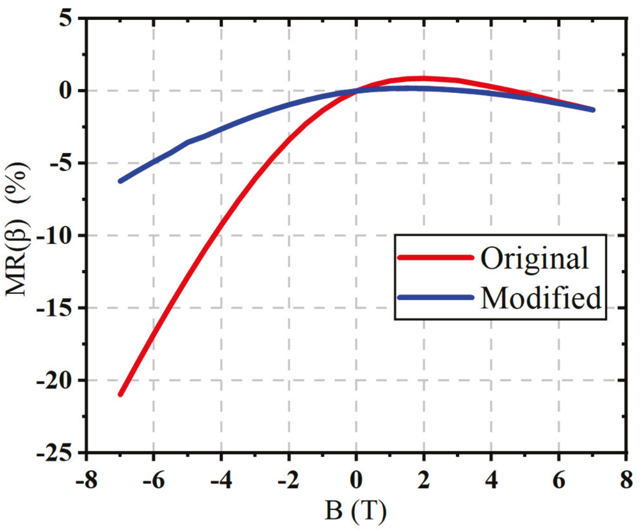

Figure 18. Comparison of MR(β) curves for the original and optimized BJT structures.

5. Conclusions

This paper uses TCAD simulation to study the electrical characteristics of the vertical NPN bipolar junction transistor (VNPN BJT) under the strong magnetic field environment. The results show that the magnetic field induces carrier displacement and change in mobility, which in turn affects the collector current, base current, and current gain β. Among these, the effect of the negative Z-direction magnetic field is particularly significant, mainly due to the asymmetry in the device structure, leading to more severe carrier displacement.

To improve the device's stability in strong magnetic environments, this paper proposes a structural optimization scheme by introducing a second STI region to the left of the emitter region and adjacent to the right side of the base electrode. This structure effectively suppresses the carrier displacement and base recombination behavior, significantly slowing down the decrease in β. The simulation results confirm that the optimized structure shows significantly enhanced interference resistance under the negative Z-direction magnetic field, demonstrating strong potential for engineering applications.

Author Contributions: Investigation, J.Z., J.L. and K.H.; Resources, R.D.; Data curation, F.M.; Writing—original draft, K.G.; Writing—review & editing, X.L. and C.X.; Project administration, Y.L. and Y.Y. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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A Multimodal CMOS Readout IC for SWIR Image Sensors with Dual-Mode BDI/DI Pixels and Column-Parallel Two-Step Single-Slope ADC

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Abstract: This paper proposes a dual-mode CMOS analog front-end (AFE) circuit for short-wave infrared (SWIR) image sensors, which integrates a hybrid readout circuit (ROIC) and a 12-bit two-step single-slope analog-to-digital converter (TS-SS ADC). The ROIC dynamically switches between buffered-direct-injection (BDI) and direct-injection (DI) modes, thus balancing injection efficiency against power consumption. While the DI structure offers simplicity and low power, it suffers from unstable biasing and reduced injection efficiency under high background currents. Conversely, the BDI structure enhances injection efficiency and bias stability via an input buffer but incurs higher power consumption. To address this trade-off, a dual-mode injection architecture with mode-switching transistors is implemented. Mode selection is executed in-pixel via a low-leakage transmission gate and coordinated by the column timing controller, enabling low-current pixels to operate in low-noise BDI mode, whereas high-current pixels revert to the low-power DI mode. The TS-SS ADC employs a four-terminal comparator and dynamic reference voltage compensation to mitigate charge leakage and offset, which improves signal-to-noise ratio (SNR) and linearity. The prototype occupies 2.1 mm $\times$ 2.88 mm in a 0.18 μm CMOS process and serves a 64 $\times$ 64 array. The AFE achieves a dynamic range of 75.58 dB, noise of 249.42 μV, and 81.04 mW power consumption.

Keywords: CMOS readout integrated circuit (ROIC); buffered direct injection (BDI); direct injection (DI); short-wave infrared (SWIR); two-step single-slope ADC (TS-SS ADC)

1. Introduction

Infrared focal plane arrays (IRFPAs) are pivotal in advanced photodetection systems for night vision and thermal imaging [1–6]. As the interface between infrared detectors and signal processors, the ROIC critically determines imaging quality through its charge-handling capability, noise performance, and dynamic range [7]. Although DI and BDI injection circuits have been extensively studied, their inherent performance trade-offs remain a central challenge for next-generation IRFPAs.

Recent high-resolution SWIR ROICs based on CTIA or digital front-ends underscore the demand for low-noise, high-throughput ADCs [8–10]. Emerging focal-plane arrays based on novel semiconductor detectors require a front-end that can accommodate both ultralow dark current (<1 nA) and large photocurrent (>20 nA). Within ROIC architectures, pixel-level current injection methods significantly affect signal fidelity and detector bias stability. The DI [11] approach, characterized by its minimalist structure, is advantageous in terms of compactness and ultra-low power consumption. However, its performance rapidly degrades under large photocurrents or variable illumination conditions due to insufficient injection efficiency and susceptibility to bias drift arising from impedance mismatch between the detector and the integration node. By contrast, the BDI [12] topology integrates a local buffer—typically a source follower or an operational amplifier—to decouple the detector from the integrator. This configuration substantially improves injection efficiency and bias stability, thereby enabling superior linearity and noise performance. Nevertheless, the inclusion of an active buffer incurs significant penalties in area and static power, which limits scalability, especially in large-format, power-constrained sensor arrays [13,14].

Concurrently, the analog-to-digital conversion stage imposes another critical performance bottleneck. The chip-level ADCs exhibit lower power consumption but are hindered by slow quantization speeds, making them unsuitable for high-frame-rate scenarios. Column-level ADCs strike a balance by combining the resolution advantages of pixel-level designs with the speed and power efficiency of chip-level implementations [15]. Therefore, column-parallel ADCs have become the de facto standard in high-resolution IRFPA architectures, balancing throughput and power efficiency. Successive-approximation-register (SAR) ADCs have achieved up to 14-bit resolution within 2 μs [16]. However, the large capacitor-DAC (CDAC) array incurs considerable area overhead, rendering SAR ADCs impractical for ultra-large-format sensors. Recent work has explored alternative architectures. Zhao et al. demonstrated a 12-bit two-stage cyclic ADC in 110 nm CMOS achieving 11.4 bit ENOB at 1 MS/s with only 0.185 mW per column (Walden FoM = 68.5 fJ/step) [17]. Cheng et al. reported a 4th-order noise-shaping SAR ADC in 28 nm CMOS yielding 94.3 dB SNDR over 100 kHz bandwidth and a Schreier FoM of 184 dB at 5 MS/s for just 107.4 μW [18]. Catania et al. further showed that inverter-based ΔΣ modulation can achieve >12 ENOB and 79.4 dB SNR at an ultra-low 71.5 nW power budget for wearable sensors [19]. While these approaches push FoM and resolution limits, they require multiple high-speed amplifiers, large capacitor networks, or complex feedback loops that constrain pixel pitch and complicate large-scale integration. Among available ADC designs, single-slope (SS) ADCs are notable for their architectural simplicity and inherent linearity. Compared to SAR and cyclic ADCs, SS ADCs significantly reduce column fixed-pattern noise (CFPN) by leveraging uniform ramp signals across all columns [20–22].

However, their serial quantization process imposes a substantial speed constraint—requiring 2N clock cycles for N-bit resolution—which is inadequate for high-frame-rate imaging. To mitigate this limitation, hybrid two-step single-slope (TS-SS) ADCs have been introduced. These converters decouple coarse and fine quantization, effectively reducing the number of required clock cycles to $2^M + 2^N$ for M + N bit resolution. Despite their improved speed, conventional TS-SS architectures suffer from critical non-idealities, including parasitic charge leakage and comparator offset, particularly during the fine quantization phase. These effects can significantly degrade signal-to-noise ratio (SNR), increase differential nonlinearity (DNL), and undermine conversion accuracy under low signal or high-speed conditions.

In response to these challenges, this work proposes a high-performance dual-mode AFE architecture tailored for SWIR image sensors. The design features a dynamically reconfigurable DI/BDI pixel interface that adapts to varying photocurrent conditions to optimize trade-offs between power consumption and injection efficiency. In parallel, a precision-optimized 12-bit TS-SS ADC is developed, incorporating a novel four-terminal comparator and dynamic reference voltage compensation. This approach effectively suppresses charge leakage and improves fine-ramp linearity, resulting in enhanced conversion fidelity. Fabricated in a standard 0.18 µm CMOS process, the proposed AFE achieves a measured dynamic range of 75.58 dB and power consumption of 81.04 mW. The ADC achieves an effective number of bits (ENOB) of 6.12 and a spurious-free dynamic range (SFDR) of 48.26 dB at 4 MS/s. These results demonstrate the proposed architecture's suitability for high-sensitivity, low-power imaging systems operating in complex and dynamic environments.

2. System Architecture

Figure 1 gives a system-level view of the AFE, timing controller, and column ADC. Photocurrent from the pixel feeds a DI/BDI front-end, whose output is sampled by a two-phase track-and-hold (T/H). A global timing controller broadcasts coarse-/fine-ramp edges while locally gating column clocks to overlap integration with conversion. A 12-bit TS-SS ADC digitizes the held voltage and streams the data to a column serializer. The proposed AFE architecture is designed to support high-sensitivity, low-noise readout and digitization of short-wave infrared (SWIR) signals, as shown in Figure 2.

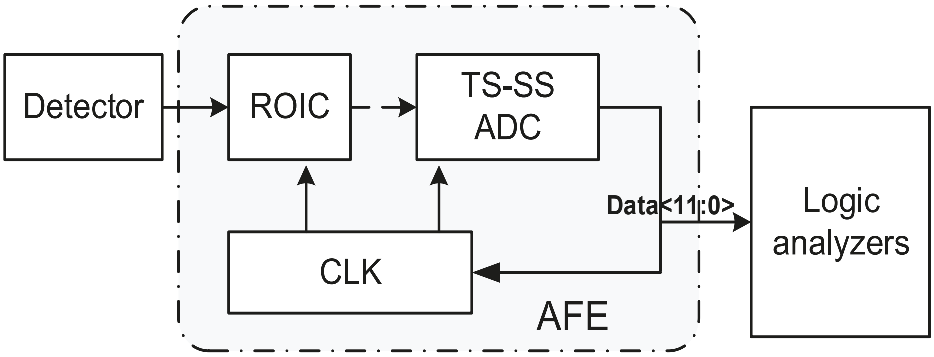


Figure 1. System-level block diagram of the SWIR AFE comprising the pixel array, DI/BDI front-end, timing controller, and TS-SS ADC.

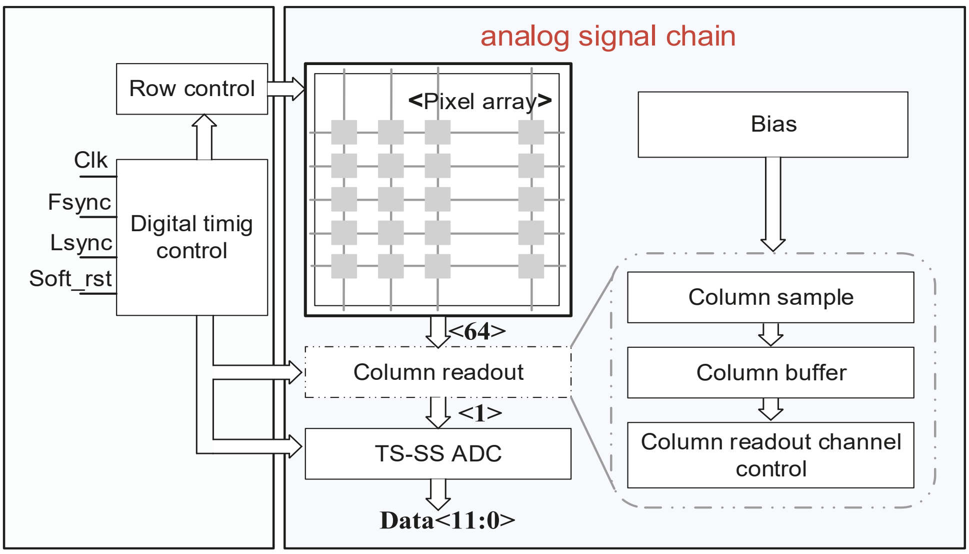


Figure 2. The analog front-end circuit framework.

2.1. Analog Front-End with Dual-Mode

The AFE includes a dual-mode pixel array, column-level sample-and-hold (S/H) circuits, output buffers, and a column-parallel TS-SS ADC. As shown in Figure 3, each pixel features a reconfigurable injection front-end capable of toggling between DI and BDI modes. Unlike the CdS/CdTe neutron-detector model with poly-Si TFT amplifiers [23], the HGFET pixel offers gate-controlled gain and sub-nA dark current, necessitating a 10^3 dynamic range without per-pixel gain switching [21]. Dual-mode injection is the best choice. The selection is dynamically controlled through a dedicated mode-switching transistor embedded at the pixel level. In DI mode, the photocurrent generated by the detector is directly integrated onto the storage capacitor. This configuration minimizes static power consumption and is suitable for low-light or power-constrained applications. In contrast, BDI mode activates a local buffer—typically implemented as an operational amplifier—to decouple the detector from the integration node. This enhances bias voltage stability and significantly improves injection efficiency under high background illumination or fluctuating signal levels. Following pixel-level integration, analog voltages are transferred onto column-level capacitors through row selection, then buffered by source followers to preserve signal fidelity during readout. These buffered voltages are subsequently digitized by the TS-SS ADCs located at the bottom of each column.

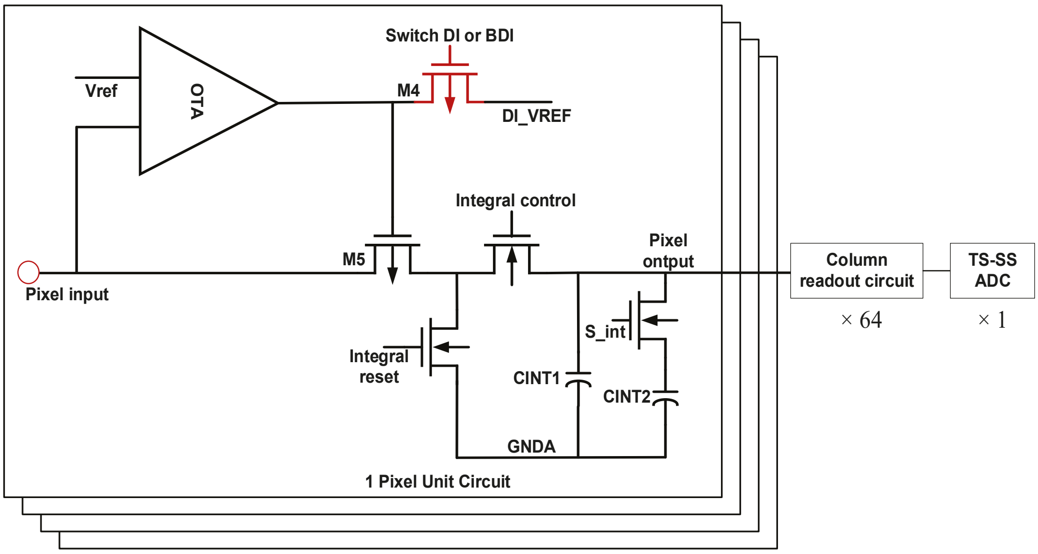


Figure 3. Dual-mode injection circuit diagram.

2.2. TS-SS ADC Design

The column-parallel ADC structure integrates several key components: an S&H unit, a four-terminal comparator, coarse and fine ramp generators, and digital calibration logic, as shown in Figure 4. A central innovation of the ADC is the incorporation of a four-terminal comparator architecture, which mitigates the effects of parasitic charge leakage during the fine quantization phase. Conventional TS-SS ADCs typically connect the top plate of the storage capacitor to the fine ramp generator. This introduces parasitic capacitance that interacts with the held charge, leading to ramp distortion, degraded linearity, and increased signal-dependent errors. In the proposed design, the bottom plate of the storage capacitor is instead tied to ground, effectively decoupling the ramp generator from the capacitor node. This approach eliminates the dominant leakage path, ensuring consistent ramp slope and improving SNR.

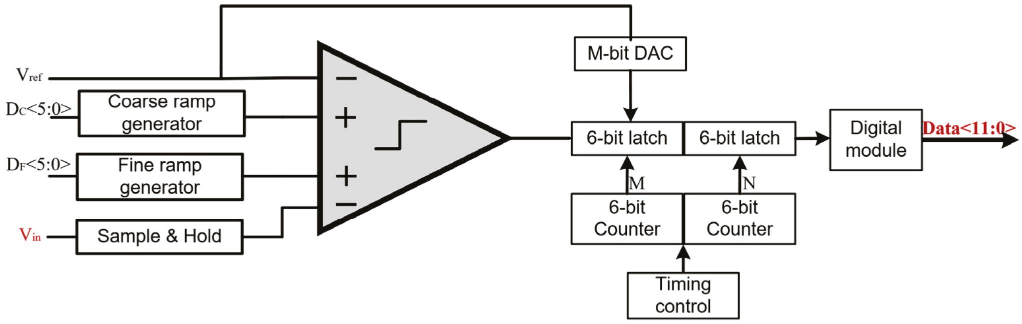


Figure 4. The diagram of the TS-SS ADC.

2.3. Digital Timing Control

The digital module, synchronized to an external 20-MHz master clock, row sync (LSYNC), and frame sync (FSYNC) signals, generates precision timing signals, as shown in Figure 5. Triggered by three external signals—master CLK, LSYNC, and FSYNC—the digital module generates the timing control signal required by the readout circuit. These inputs govern the pixel selection sequence, ADC conversion cycles, and data readout windows. The controller generates phase-aligned clock signals for pixel integration, sample-and-hold activation, ramp generation, and digital readout. All control signals are passed through level shifters to ensure compatibility between digital logic and analog voltage domains. The system also supports programmable integration time and region-of-interest (ROI) windowing, allowing for flexible operation under varying scene dynamics and application-specific requirements.

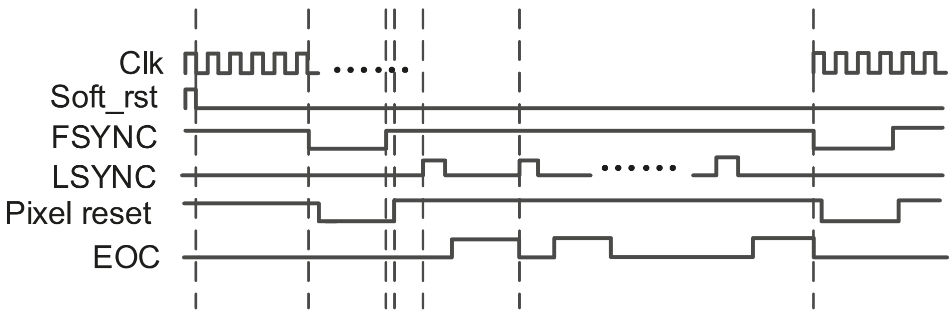


Figure 5. Digital timing control.

3. Silicon-Based ROIC Design

The ROIC plays a pivotal role in bridging the interface between the detector array and the ADC, thereby determining the system's noise floor, linearity, and signal integrity. To support adaptive performance across a wide dynamic range and varying illumination conditions, the proposed ROIC employs a dual-mode injection front-end architecture, capable of dynamically switching between DI and BDI modes at the pixel level.

3.1. Dual-Mode Pixel Injection Structure

Each pixel incorporates a reconfigurable input stage consisting of a photodetector, an integration capacitor, and a mode-switching transistor that determines the operational mode of the pixel. When operating in DI mode, the photocurrent generated by the detector is directly integrated onto the capacitor without any intermediate amplification. This mode is particularly advantageous in low-light scenarios or systems with stringent power budgets, as it minimizes the static power consumption and area overhead by eliminating active elements. In contrast, BDI mode leverages a local feedback amplifier to buffer the detector node from the integration capacitor. The op-amp maintains the detector bias at a constant voltage while enabling more efficient current injection through the main integrating transistor. The op-amp amplifies source-node voltage fluctuations by a factor of (Av + 1), effectively enhancing the transconductance (gm) of injection transistor M5. This configuration enhances the pixel's linearity and suppresses signal-dependent bias variation, thereby improving the system's dynamic performance in high-illumination or fast-transient environments. The transition between DI and BDI modes is governed by a single transistor (M4), which toggles the connection between the buffer amplifier and the pixel front-end. This transistor-based control scheme ensures seamless, real-time reconfiguration of the injection structure without the need for external reprogramming or power cycling.

3.2. Transconductance and Injection Efficiency

To quantitatively analyze the performance advantages offered by the dual-mode architecture, the photodetector is modeled as a parallel network comprising a current source (I_{ph}), an equivalent capacitance (C_d), and a conductance (g_{ds}), as shown in Figure 6. The photocurrent is routed through a MOS injection transistor (M_5), whose transconductance (g_{m1}) governs the efficiency of signal injection. The behavior of g_{m1} depends strongly on the transistor's operating regime. When M5 operates in saturation, its transconductance is governed by:

$$\mathbf{g}_{msat} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \tag{1}$$

where μn is the electron mobility, C ox is the gate oxide capacitance, and W/L is the transistor aspect ratio. In subthreshold operation, gm exhibits distinct behavior due to exponential current-voltage relationships:

$$\mathbf{g}_{msub} = \frac{\mu_n C_{ox} \frac{W}{L} \frac{KT}{q}}{(V_{GS} - V_{TH})} \tag{2}$$

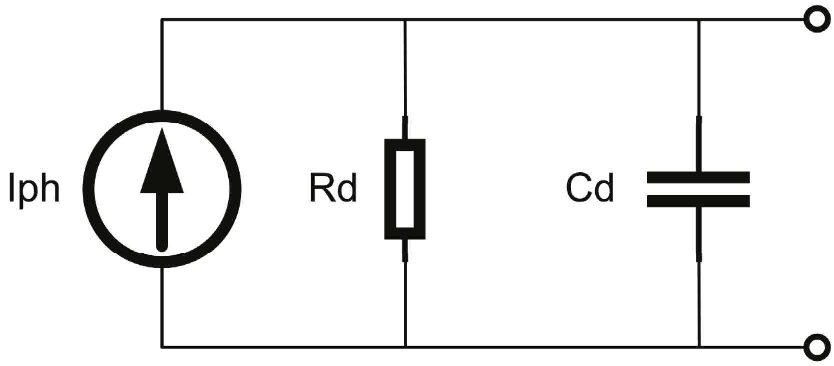


Figure 6. Small-Signal Model of the Photodetector.

Here, k is Boltzmann's constant, T is the absolute temperature, and q is the electron charge. Subthreshold operation enhances transconductance efficiency, reducing sensor bias fluctuations (<0.1% nonuniformity error) and improving sensitivity.

- Injection Efficiency in BDI/DI Modes:

Injection efficiency (Y) is defined as the ratio of the effective integrated photocurrent ($_{Iint}$) to the total generated photocurrent (I_{ph}), serving as a critical metric for evaluating the front-end's charge transfer performance. In DI mode, the injection efficiency is limited by the detector's output impedance and is approximately expressed as:

$$Y_{DI} = \frac{g_{m1}}{g_{m1} + g_{ds}} \tag{3}$$

where g_{ds} is the detector conductance. In BDI mode, the presence of the feedback amplifier effectively multiplies the transconductance by the amplifier gain A_v, leading to an improved efficiency model:

$$Y_{BDI} = \frac{(A_v + 1)g_{m1}}{(A_v + 1)g_{m1} + g_{ds}} \tag{4}$$

Here, A_v is the op-amp voltage gain. This relationship indicates that as A_v increases, the injection efficiency asymptotically approaches unity.

4. Silicon-Based ADC Design

The performance of the ADC plays a decisive role in determining the overall signal fidelity of infrared image sensors, particularly in systems requiring high frame rates and wide dynamic range. To address the latency and non-idealities inherent in conventional single-slope architectures, a column-parallel TS-SS ADC is proposed, incorporating architectural enhancements that significantly improve resolution, linearity, and energy efficiency.

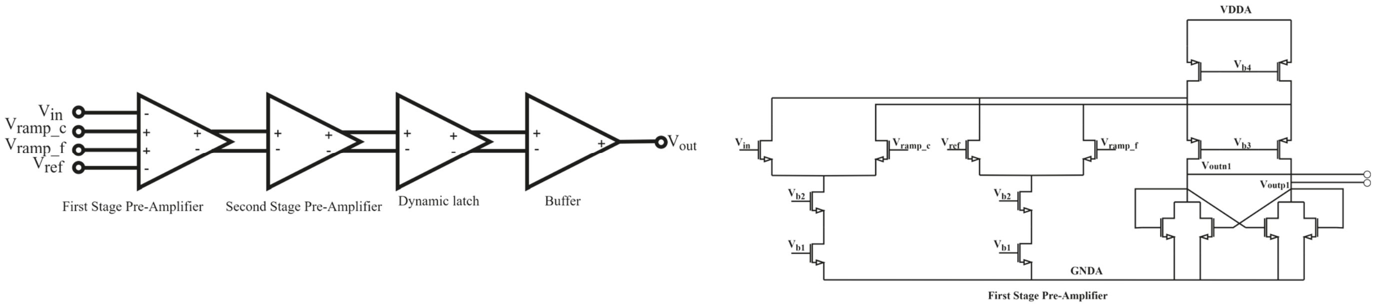
4.1. Four-Terminal Comparator Architecture

We compared three comparator architectures—a standard op-amp-based design, a dynamic latch, and our implemented Differential Difference Amplifier (DDA). Pure op-amp comparators suffer from elevated 1/f noise under low SWIR photocurrents and require extensive per-column offset trimming, while dynamic latches introduce dead-time for offset-cancellation cycles, reducing throughput. The DDA, however, inherently suppresses column-to-column common-mode offset without additional calibration steps and maintains low input-referred noise, making it the optimal choice for large-scale SWIR focal planes.

After the charge leakage of the storage capacitor, the slope of the fine slope signal will be reduced, and a quantization dead zone will be generated. In more serious cases, the comparator may fail to trigger in the fine quantization stage. To suppress this issue, the proposed ADC incorporates a four-terminal comparator, wherein the bottom plate of the sampling capacitor is tied to GND, rather than connected to the fine ramp, as shown in Figure 7a. This architectural decoupling eliminates the primary leakage path through the parasitic capacitance and ensures stable voltage retention throughout the quantization period. The comparator comprises two stages:

- First Stage—Differential Difference Amplifier: Provides high open-loop gain and common-mode rejection, enabling accurate resolution of small voltage differences during both coarse and fine quantization. Figure 7b depicts a partial transistor-level schematic of the four-terminal dynamic comparator. The core employs a cross-coupled NMOS latch with PMOS active loads. Two auxiliary switches momentarily tie the storage capacitor C_H to the latch tail during reset, canceling kick-back.
- Second Stage—Diode-Loaded Inverter: Offers high-speed signal regeneration with minimal propagation delay, ensuring rapid latching behavior at the threshold crossing.

By structurally isolating the ramp signal from the storage node and incorporating a precision amplifier front-end, the comparator exhibits superior sensitivity and immunity to charge injection artifacts.

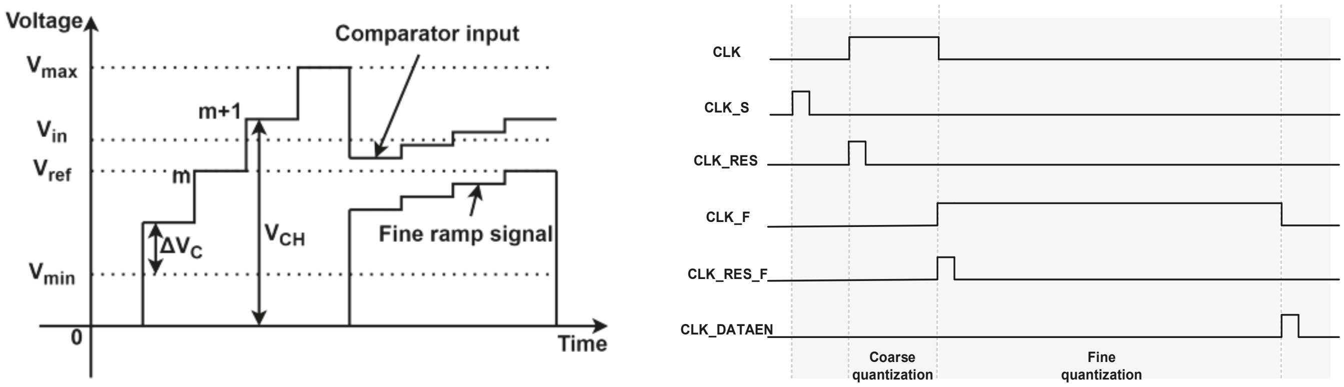


(**a**) (**b**)

Figure 7. (**a**) Structure diagram of the four-terminal comparator; (**b**) Schematic of the first state amplifier.

4.2. Quantization Scheme with Redundant Bit Allocation

To overcome nonlinearity introduced by device mismatches and transition glitches, a hybrid quantization algorithm is adopted. The total 12-bit resolution is achieved through a coarse-fine division of 6 bits each, supplemented by a 1-bit redundancy mechanism that facilitates digital post-correction. Figure 8a shows our two-step conversion. First, a 6-bit coarse counter generates a global ramp and latches the MSBs. The residue amplifier then subtracts this coarse voltage from the input. Next, a 6-bit fine ramp—extended with one redundant bit—captures the LSBs. Finally, digital correction logic aligns MSB and LSB codes, removing any ±1 LSB offset via the redundant bit to produce the 12-bit output.



(**a**) (**b**)

Figure 8. (**a**) The relationship between the signals; (**b**) Timing design.

The quantization process proceeds as follows:

- Coarse Phase: A 6-bit counter generates a globally distributed voltage ramp, enabling parallel acquisition of the most significant bits (MSBs) across all columns. This ramp resolves the voltage to a 64-level approximation.
- Fine Phase: A higher-resolution ramp is applied to the fine quantization stage, covering a dynamic range of 2ΔV to fully span the residue from the coarse stage. To account for transition errors, the fine ramp includes one extra redundant bit.
- Digital Correction: Post-processing logic combines the coarse and fine quantization results. As shown in Figure 9, an adder aligns the fine MSB with the coarse result, and a subtractor removes a fixed digital offset introduced by the redundancy, yielding a final 12-bit output with minimized DNL.

- Simulation and silicon measurements demonstrate that the proposed scheme suppresses non-monotonicity and reduces worst-case DNL to below 0.2 least significant bits (LSB), even in the presence of offset voltage mismatch and charge redistribution.

Coarse Quantification		C_5	C_4	C_3	C_2	C_1	C_0						
Fine Quantification	+						F_6	F_5	F_4	F_3	F_2	F_1	F_0
		D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	-	0	0	0	0	0	0	1	0	0	0	0	0
		T_{11}	T_{10}	T_9	T_8	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0

Figure 9. Schematic diagram of quantization result processing.

4.3. Switch Charge Injection Compensation

Switch charge injection is a dominant source of nonlinearity in TS-SS ADCs. When switches open during coarse quantization, the injected charge (Q_{inj}) alters the voltage on C_H:

$$Q_{inj} = \delta(WL)_{S1}C_{ox}(V_{GS} - V_{TH}) = \delta(WL)_{S1}C_{ox}(V_{DD} - (M+1)\Delta V - V_{TH}) \tag{5}$$

where δ is the charge injection ratio, (WL) S1 is the switch transistor dimensions, and M represents the coarse quantization result. This charge induces a voltage shift (ΔV_{CH}) on C_H:

$$\Delta V_{CH} = \frac{Q_{inj}}{C_H} = \frac{\delta(WL)_{S1}C_{ox}(V_{DD} - (M+1)\Delta V - V_{TH})}{C_H} \tag{6}$$

To counteract this perturbation, a 6-bit current-steering digital-to-analog converter (DAC) is introduced to adjust the reference voltage Vref dynamically. This compensation voltage aligns the comparator decision threshold with the expected ramp trajectory:

$$V_{DAC(m)} = \Delta V_{CH}(m) + V_{ref} \tag{7}$$

This adjustment ensures the comparator input remains linear:

$$V_{in} = m\Delta V - VS - \frac{1}{2}\Delta V + i\Delta F \tag{8}$$

Through this scheme, the static and dynamic characteristics of the TS-SS ADC can be effectively improved to ensure the high precision and stability of the analog-to-digital conversion. Figure 8a shows the relationship between the input signal Vin, the coarse ramp voltage, the fine ramp voltage and the storage capacitor ΔV_{CH} during the quantization process.

4.4. ADC Timing and Control Strategy

The ADC operates in three phases, synchronized to a 20-MHz master clock as shown in Figure 8b:

- Sampling Phase: The pixel output voltage is sampled and held (CLK_S high);
- Coarse Quantization Phase: The 6-bit counter generates V_{Coarse} (CLK high), resolving MSBs within 64 cycles;
- Fine Quantization Phase: A 7-bit counter drives V_{fine} (CLK_F high), with redundancy and DAC compensation refining the least significant bits (LSBs);
- All transitions are synchronized to a 20 MHz master clock and governed by global synchronization signals (LSYNC, FSYNC), ensuring deterministic latency and pipeline compatibility. The entire column-parallel array can thus operate in parallel without temporal skew, enabling real-time readout of high-resolution frames. A foreground

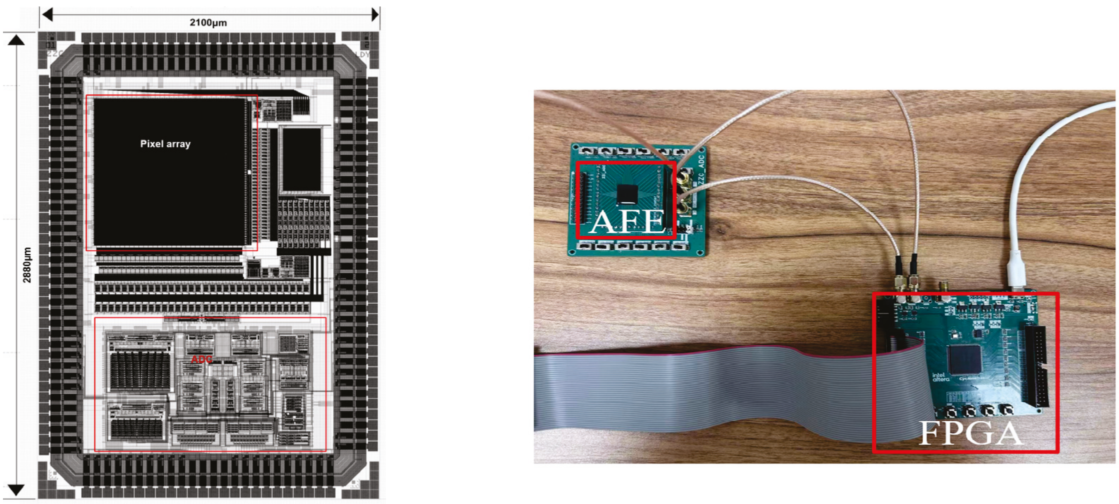
redundancy-based calibration removes coarse-stage transition errors, while the on-chip PLL offers background time-base calibration that trims the fine-ramp slope to <0.05% error.

4.5. Charge-Injection Compensation DAC

The switch network that connects the coarse-stage residue to the fine-ramp capacitor injects ± charge when turning off, producing a deterministic staircase on the fine ramp and degrading INL by up to 0.7 LSB. To cancel this error, a 6-bit DAC sinks a programmable bias current from the fine-ramp buffer. During reset, the same switches are held closed so the injected charge is mirrored into the DAC sink node; by trimming the DAC code, the net charge ΔQ is nulled.

5. Experimental Results

The proposed dual-mode AFE was fabricated in a standard 180 nm 1P7M CMOS process. The layout is shown in Figure 10a, with an area of 2100 µm × 2880 µm. The silicon prototype includes a 64 × 64 pixel array with reconfigurable DI/BDI pixel front-end, column-level TS-SS ADCs, and supporting digital control logic. As shown in Figure 10b, all measurements were conducted at room temperature (25 °C) under a 3.3 V supply, using a programmable logic analyzer and a high-precision current source to emulate detector output currents. A programmable low-noise current source delivered photocurrent replicas from 100 pA to 100 nA based on a Verilog-A SWIR photodetector model extracted from Ref. [24]. In some experimental tests, an external resistor array was used to simulate the current input of the detector. Output data (12-bit × 64 columns) were captured through LVDS pairs into a TLA6402 Logic Analyzer and de-skewed in MATLAB (Version: 9.13.0 (R2022b)) for FFT and code-density analysis. No photodetector array was bonded in this tape-out; full electro-optical tests are planned for the second silicon revision. It should be noted that the evaluation board was a first-revision four-layer design aimed at rapid silicon bring-up rather than optimum analog performance. The open bench-top environment exhibited a −62 dB spur due to ambient mains hum.

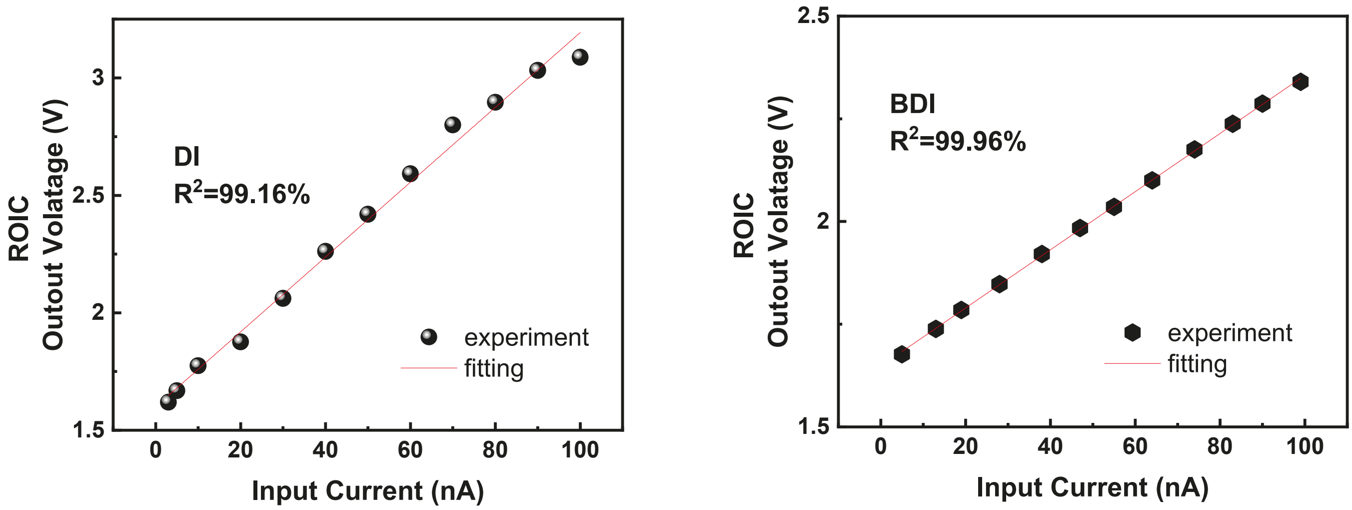


(**a**) (**b**)

Figure 10. (**a**) The layout of the AFE; (**b**) the test system.

5.1. ROIC Performance

To assess the effectiveness of the dual-mode readout structure, we first performed isolated measurements on the ROIC by bypassing the ADC. A linear ramp current input ranging from 0.1 nA to 100 nA was applied, and the output voltage was recorded for both DI and BDI configurations, as shown in Figure 11a,b. In BDI mode, the ROIC demonstrated a maximum linearity of 99.56%, compared to 98.7% in DI mode. This improvement is directly attributed to the buffer amplifier's ability to maintain a constant detector bias and decouple signal-dependent impedance variations. Moreover, the feedback mechanism in BDI significantly reduces nonlinearity under large-signal operation by preserving the integrity of the integration node potential. These results confirm that BDI mode is more suitable for high dynamic range or bright-scene conditions, while DI mode offers acceptable linearity at significantly reduced power consumption, making it preferable in low-illumination, power-constrained scenarios.



(**a**) (**b**)

Figure 11. (**a**) BDI linearity; (**b**) DI linearity.

5.2. ADC Performance Evaluation

Figure 12a demonstrates that the TS-SS ADC attains 6.12-bit ENOB and 48.26 dB SFDR at 4 MHz. Three dominant error sources were identified:

- Residual fine-ramp distortion due to second-order parasitic leakage around CH even after the four-terminal comparator decoupling, shortening the effective LSB range and degrading SNR.
- Clock-edge jitter of 18 ps rms propagates to 0.55 LSB timing uncertainty during the 7-bit fine ramp, removing ~0.4 bits.
- Board-level parasitics further reduce the measured ENOB: (i) supply noise contributes 0.6 bits per IEEE Std-1241 SNR scaling; (ii) ramp-line capacitance increases the effective LSB by 0.5 LSB. These losses are extrinsic and will be mitigated by a six-layer PCB with isolated analog grounds, on-board LDO filtering, differential ramp routing, and an aluminum enclosure. The output digital code of the ADC was tested with an incremental voltage step of 0.1 V. Each voltage generates 4096 digital codes, and the average value of the digital codes is taken to fit the line that coincides with the scatter plot. The four-terminal comparator eliminates charge leakage, achieving 99.89% linear ramp slope accuracy, as shown in Figure 12b. The architecture achieves

4220 fJ/conv-step (ADC-core) while offering dual-mode BDI/DI flexibility at the system level.

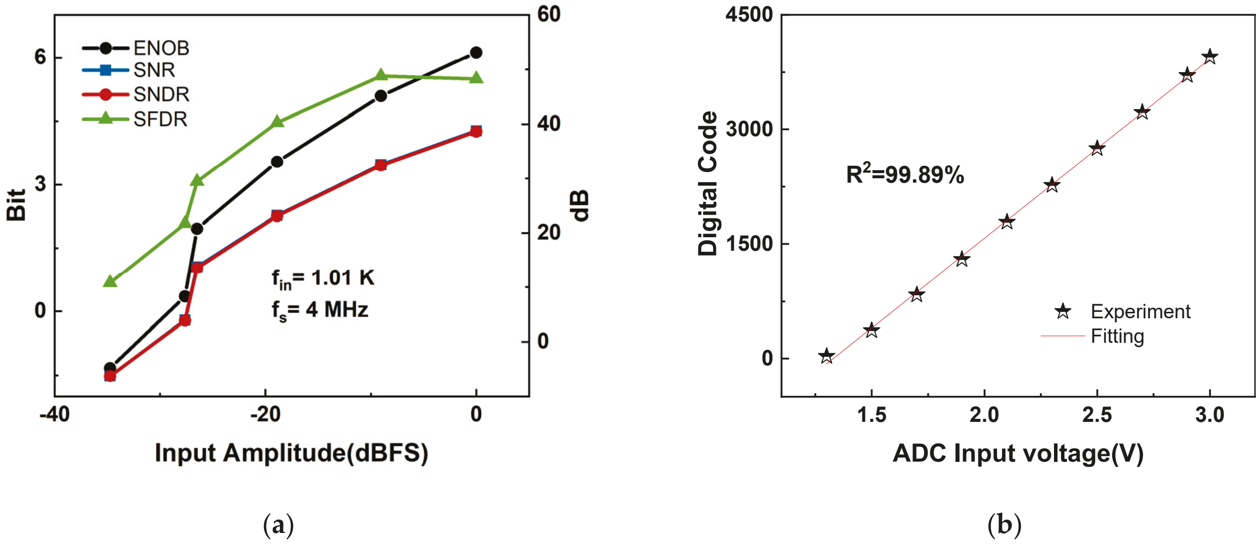


Figure 12. (**a**) Measured output spectrum, ENOB/SNR/SNDR/SFDR versus input frequency; (**b**) the relationship between the input voltage signal ADIN of the ADC and the integrated voltage output.

5.3. Pre- vs. Post-Layout Simulation Correlation

Table 1 overlays ADC spectra from schematic-level (pre-layout), RC-extracted post-layout (PEX) netlists, and measured silicon in BDI mode. Table 1 quantifies ENOB, SFDR and SNDR. Post-layout parasitics degrade ENOB by 0.12 bit, attributable to additional routing capacitance. The extra 5.63-bit drop from PEX to silicon stems from PCB supply noise, clock jitter, comparator kick-back underestimated in PEX, and package bond wire inductance.

Table 1. Performance comparison with pre-layout, RC-extracted post-layout (PEX) netlists, and measured silicon in BDI mode.

Parameter	Pre-Layout	Post-Layout	Silicon Data
SFDR (dB)	81.55	87.67	48.3
SNDR (dB)	73.26	73.14	38.65
ENOB (bit)	11.87	11.75	6.12

5.4. Comparative Analysis

Finally, the dynamic range of the AFE was tested, and the test results are shown in Figure 13a,b. Both AFE chips in BDI and DI modes can achieve signal acquisition and processing of detector arrays. In DI mode, the AFE exhibits 98.7% linearity, whereas BDI mode attains 99.56%, owing to the buffer's ability to stabilize detector bias. As shown in Figure 13c, measured power consumption under different operating conditions is summarized as follows:

- DI Mode: 74.98 mW (static + dynamic);
- BDI Mode: 81.04 mW (≈8% increase over DI).

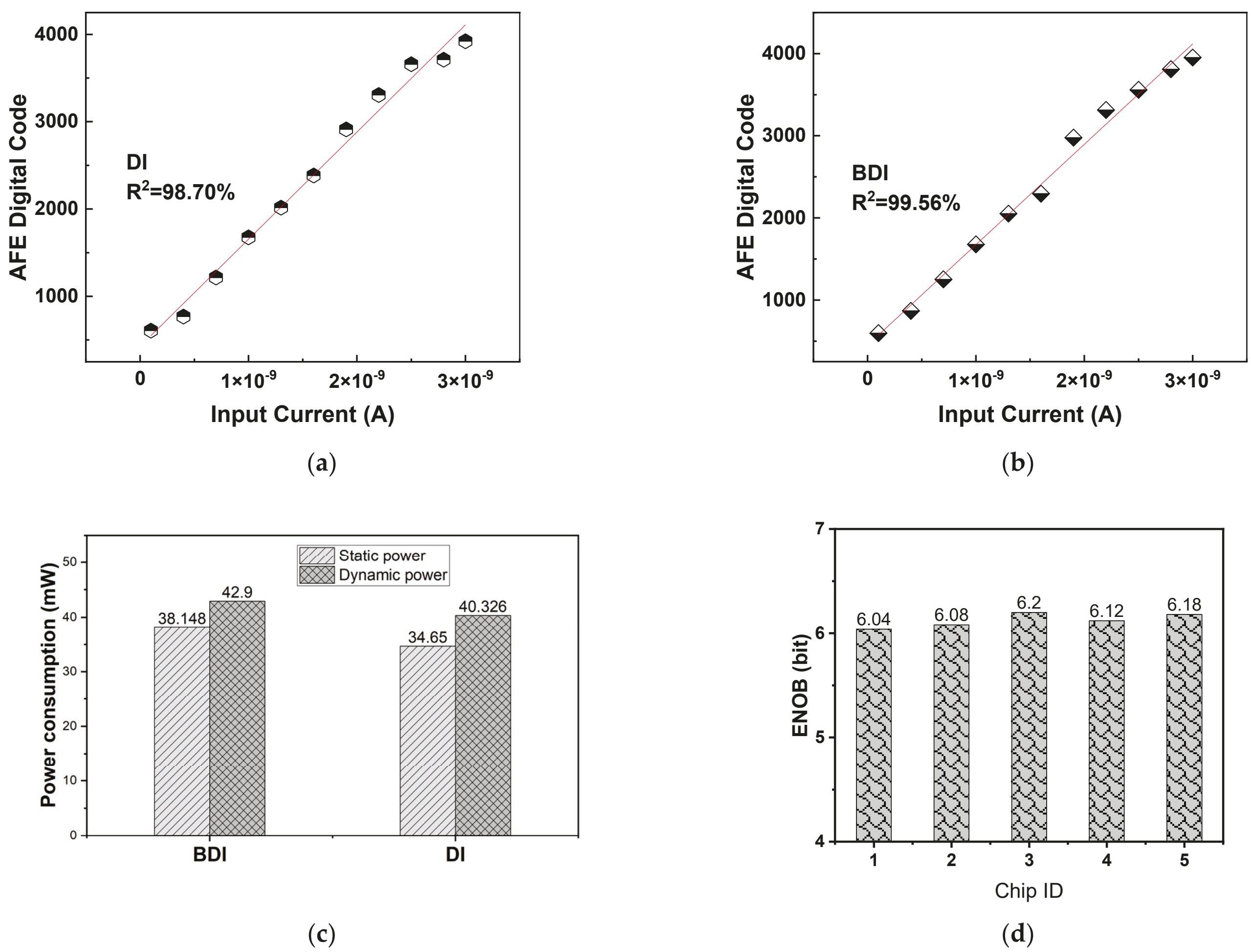


Figure 13. (**a**) The relationship between the input current signal and the output digital code of the AFE in DI mode; (**b**) the relationship between the input current signal and the output digital code of the AFE in BDI mode; (**c**) power consumption of BDI and DI modes; (**d**) measured ENOB versus die.

The additional power in BDI mode is attributable to the buffer amplifier and associated bias circuits. Nonetheless, this modest increase is justified by significant improvements in injection efficiency, bias stability, and readout linearity. The trade-off capability between power and performance highlights the effectiveness of the proposed dual-mode structure in dynamic or mission-adaptive imaging systems. Designers can select DI or BDI mode in real time based on ambient light level or system power state. We have measured five dies from the same wafer lot. Figure 13d shows the ENOB (6.12 $\pm$ 0.08 bit). The tight distributions (<1% variation) confirm robustness against process drift.

To further validate the competitiveness of the proposed AFE, a comprehensive comparison with prior art is presented in Table 2.

Table 2. Performance comparison with AFEs.

Parameter	[25]	[26]	[27]	[28]	[29]	[30]	This Work
Process	180 nm CMOS	350 nm CMOS	180 nm CMOS	180 nm CMOS	350 nm CMOS	180 nm CMOS	180 nm CMOS
Pixel array	640 × 512	10 × 8	640 × 512	32 × 32	128 × 128	200 × 200	64 × 64
Pixel size (μm^2)	15 × 15	30 × 30	20 × 20	22.5 × 22.5	50 × 50	5 × 5	15 × 15

Table 2. *Cont.*

Parameter	[25]	[26]	[27]	[28]	[29]	[30]	This Work
Supply (V)	1.8	5	3.3/1.8	NA	NA	3.3/1.8	3.3
Voltage Swing (V)	1	2	<2	1.5	1.4	/	1.5
Pixel input type	BDI	DI/BDI	DI	SFD/CTIA	BDI	/	DI/BDI
Input current (A)	100f-100n	1p-10n	N/A	15p-3n	22n-112n	/	100p-100n
Power (mW)	N/A	9.94	N/A	N/A	N/A	0.108 (only column ADC)	74.976/81.048
Linearity	99.95%	98%/99%	N/A	98.9%	95.8%	/	98.7%/99.5%
Area (mm × mm)	11.13 × 8.78	/	15 × 15.6	/	/	/	2.1 × 2.88
ADC type	/	/	/	/	/	Column parallel SS ADC	TS-SS ADC
ADC resolution (bit)	/	/	/	/	/	11	6.12

- Pixel Size: Among dual-mode AFEs, this work achieves the smallest pixel pitch (15 μm), enhancing spatial resolution and integration density;
- Injection Range: The widest current sensing range (100 pA to 100 nA) is achieved, supporting both ultra-low signal and high-flux scenarios;
- Linearity: Linearity in BDI mode (99.56%) matches or exceeds that of high-end fixed-mode ROICs, validating the efficacy of buffer-assisted injection;
- Power Efficiency: Despite its dual-mode capability and integrated 12-bit ADC, the power remains within the same order as single-mode designs, emphasizing circuit efficiency. The 74.976 mW/81.048 mW figure refers to the full dual-mode front-end (BDI + DI) plus column ADC array and on-chip timing controller, whereas Ref. [26] reports a BDI/DI front-end. Isolating our ADC core yields 0.01 mW/pixel; however, Ref. [28] reaches 0.12 mW/pitch.

6. Conclusions

This work presents a dual-mode CMOS analog front-end for image sensors, integrating a dynamically reconfigurable BDI/DI ROIC and a 12-bit TS-SS ADC. Key innovations include the following:

- Dual-Mode Pixel Architecture: The BDI/DI hybrid input stage enables dynamic switching between high injection efficiency (99.56% at 100 nA) and low power consumption (74.96 mW), achieving a 75.58 dB dynamic range in BDI mode and 8% power savings in DI mode. The feedback op-amp in BDI mode stabilizes detector bias voltage, reducing nonlinearity to <0.1% under varying photocurrent levels;
- Four-Terminal Comparator ADC: By grounding the storage capacitor's bottom plate, charge leakage is eliminated, ensuring 99.95% linearity in the fine ramp signal;
- Dynamic reference-voltage compensation enables 48.3 dB SFDR and a measured 6.12-bit ENOB over a 100 pA–1 nA photocurrent range.

The proposed architecture is particularly suited for applications requiring high sensitivity and adaptability, such as night vision, medical imaging, and industrial inspection. Future work will focus on further optimizing high-speed quantization stability and integrating on-chip temperature compensation for harsh environments.

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Conflicts of Interest: The authors declare no conflicts of interest.

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A High Dynamic Range and Fast Response Logarithmic Amplifier Employing Slope-Adjustment and Power-Down Mode

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Abstract: Based on the GSMC 180 nm SiGe BiCMOS process, a parallel-summation logarithmic amplifier is presented in this paper. The logarithmic amplifier adopts a cascaded structure of nine-stage fully-differential limiting amplifiers (LA) to achieve high dynamic range. The ten-stage rectifier completes the conversion of amplified voltage to a logarithmic current signal. A log slope adjuster is proposed. It can provide slopes of 17–30 mV/dB by configuring an off-chip resistor to meet the detection requirements of different input power. Meanwhile, a power-down control unit is designed to reduce the power consumption to only 162 μW in standby mode. The post-simulation results show that under 5 V power supply voltage, the dynamic range exceeds 80 dB and the 3 dB bandwidth is 20 MHz–4 GHz. It also has a fast response time of 42 ns with a power consumption of 109 mW in normal operation mode.

Keywords: logarithmic amplifier; limiting amplifier; log slope; power-down; response time

1. Introduction

In high-precision electromagnetic measurement systems such as radar, optical receiver and field strength meters, the input signal power is extremely weak. In order to achieve high-precision signal amplification within a wide dynamic range, logarithmic amplifiers have replaced automatic gain control loops (AGC) as a more effective solution in recent years [1–4]. Early logarithmic amplifiers have mostly adopted segmented detection architectures, which rely on multi-stage diode detectors in series to achieve signal compression. These circuits have a simple structure and high reliability, but they have defects such as large temperature drift and complex calibration. In addition, due to the disadvantages of limited dynamic range, large area, and insufficient compatibility with integrated circuit technology, further development cannot be achieved [5–8].

With the advancement of the CMOS and SiGe processes, the logarithmic amplifier has also developed rapidly. Its technological evolution mainly revolves around three core challenges: dynamic range expansion, temperature stability improvement, and bandwidth breakthrough. Lakshminarayanan et al. proposed an RF power detector that achieves a dynamic range of 52 dB with bandwidths of 100 MHz–4 GHz and logarithmic linearity of ±1 dB. It realized a good compromise between logarithmic accuracy and dynamic range [9]. Yong et al. presented a high dynamic range logarithmic amplifier using four channel amplification and current summation techniques with a dynamic range of 70 dB and power consumption of only 19 mW. However, its bandwidth is only 1 MHz, which makes it unsuitable for RF systems and only suitable for low-frequency signal analysis [10].

Ahuja et al. presented an ultra-low power CMOS logarithmic amplifier for low-frequency IoT sensing. This circuit has a dynamic range of 50 dB with a power supply of 1.5 V, while consuming only 14.63 µW. But its bandwidth is limited to 10 Hz–40 kHz. Hence, it is mainly used in physiological signal detection systems, and cannot adapt to the frequency response requirements of field strength meters [11]. Wongnamkam et al. designed a fully-differential logarithmic amplifier for 2.4 GHz ISM applications, which realized a voltage gain of 43 dB under a single 2.5 V power supply. However, it consumes a static current of 73.5 mA that results in power consumption of up to 183.75 mW. Hence, it has significant limitations in its energy efficiency [12]. Chuang et al. proposed a logarithmic amplifier using InP InGaAs double heterojunction technology, with a bandwidth of 22 GHz. However, its power consumption is as high as 650 mW [13].

In response to the collaborative design challenges of dynamic range, bandwidth, and energy efficiency, this paper proposes a logarithmic amplifier that integrates power-down mode and log slope adjuster. By implementing a dynamic power management strategy, the static power consumption can be reduced to 162 µW. The logarithmic amplifier is implemented based on a parallel-summation structure of 9-stage limiting amplifiers with dynamic range of over 80 dB and 3 dB bandwidth of 20 MHz–4 GHz. At the same time, to meet the detection requirements of different input power, a logarithmic slope adjustment scheme is proposed. By configuring off-chip resistors, the slope can be effectively adjusted to achieve signal detection over a large input range.

2. Circuit Architecture and Design

The logarithmic amplifier adopts a parallel-summation structure. As shown in Figure 1, it consists of nine-stage fully-differential limiting amplifiers (LA), ten-stage full-wave rectifiers, bandgap, log slope adjuster and output stage.

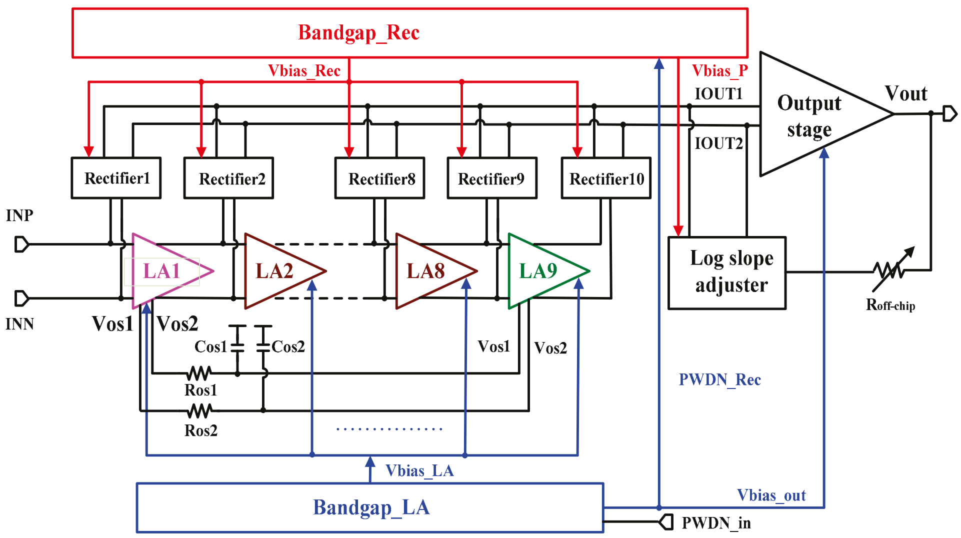

Figure 1. Architecture of proposed logarithmic amplifier.

Nine cascade limiting amplifiers are used to achieve signal gain expansion, and each amplifier output is equipped with a rectifier. The input dynamic range is determined by the gain and the number of cascaded logarithmic amplifier stages. The more stages there are, the larger the dynamic range which can be obtained [14]. Each limiting amplifier provides 10 dB gain and expands the input dynamic range through step-by-step gain compression. The voltage output by each limiting amplifier is input into the rectifier. The rectifier converts the output of each stage into current and sums them up at the input of output stage. The summed current signal is finally converted into a single-ended voltage through the output stage for output. The log slope adjuster introduces an off-chip adjustable resistor, combined with an internal bias adjustment circuit, to dynamically control the weight of the superimposed current, ultimately achieving adjustable slope. Two bandgaps provide bias to limiting amplifiers and rectifiers, respectively, which can avoid crosstalk between the two. The Bandgap_LA is controlled by the external power-down signal PWDN_in, which outputs signal PWDN_Rec to control the Bandgap_Rec and itself to be in normal operation or low-power standby mode, respectively. Cascaded limiting amplifiers can effectively expand the output dynamic range. However, due to the inter-stage DC coupling, when the common-mode voltage drifts, it is easy to cause oscillation [15]. Therefore, this design adds an offset correction circuit composed of Cos1/Cos2 and Ros1/Ros2. Capacitors Cos1 and Cos2, along with resistors Ros1 and Ros2, form a low-pass filter to filter out high-frequency components in feedback signals. The DC component of the voltage in the offset is fed back to the first limiting amplifier, thereby reducing the inter-stage offset caused by DC coupling.

The first to ninth limiting amplifiers use an A/0 structure, as shown in Figure 2. The input is Vin and the output is Vout. When Vin is small, Vout is amplified by A times. While Vin can reach or become larger than V_1, Vout is limited to the maximum value of AV_1.

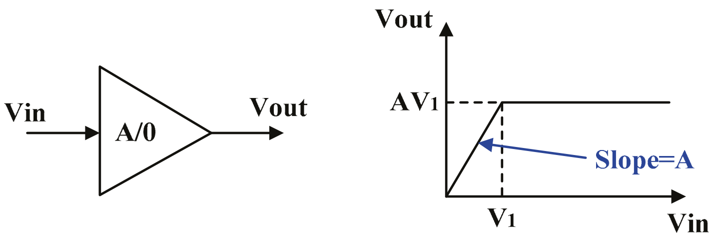

Figure 2. The basis of A/0 limiting amplifier.

When the input V_{in} is less than V_1, the limiting amplifier exhibits a linear amplification trend with an amplification factor of A. When Vin is greater than V_1, the amplifier enters a limiting state and outputs a fixed value [16,17]. The voltage transfer characteristic (VTC) of the A/0 limiting amplifier can be obtained as

$$Vout = \begin{cases} AV_{in} & 0 < V_{in} < V_1 \\ AV_1 & V_{in} > V_1 \end{cases} \tag{1}$$

Figure 3 shows the bias circuit of the first limiting amplifier that is mainly composed of the bias transistor Qbias and resistors Rb1 and Rb2. To simplify the design, the bias is directly generated by connecting Qbias and resistors Rb1/Rb2 in series from the power supply. The main purpose of Qbias is to reduce the temperature coefficient of the bias and obtain a more stable input common-mode bias. The common-mode operating voltage is set at 3.9 V.

Figure 4 shows the first limiting amplifier. This circuit adopts a single-stage common-emitter structure. The tail current source transistor Q3 is biased by the bias Vbias_LA output from the Bandgap_LA, and the parallel capacitor C1 serves as a decoupling element to filter out high-frequency noise. The collector current of Q3 is determined by the bias network composed of R3 and R4. This current directly constrains the transconductance of Q1 and Q2, which determines the log amplifier's bandwidth and gain. In order to further improve gain, a cross-coupled resistor composed of Q4 and Q5 is introduced. Because the output resistance is $-2R_{out}$, it effectively increases the voltage gain by increasing the equivalent output impedance. Transistors Q8 and Q9 form a common-mode voltage extractor, which is used to extract the common-mode output from the limiting amplifier to the rectifier. Because the gain of the first limiting amplifier is 10 dB (3.16), the output Vout is:

$$VOUTN - VOUTP = 3.16 \cdot (INN1 - INP1) \tag{2}$$

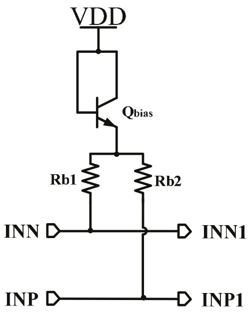

Figure 3. Input common-mode bias circuit.

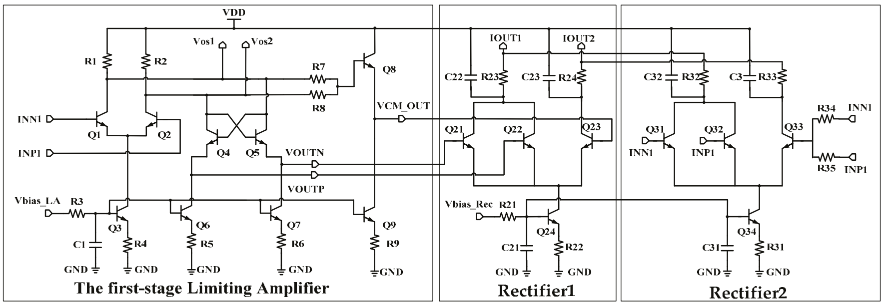

Figure 4. Limiting amplifier #1 and rectifiers.

The first limiting amplifier embeds two rectifiers, which respectively detect the input/output of the limiting amplifier and generate differential output currents that are logarithmically related to them. The rectifier adopts a three-port common-emitter structure, in which the differential and common-mode input are connected to rectifier2, while the differential-mode output of the first limiting amplifier and its common-mode output are connected to rectifier1 [18]. The bias of the rectifier is provided by the Bandgap_Rec, and the stability of its static operating current directly determines the logarithmic conversion accuracy. This design effectively expands the dynamic response range by simultaneously feeding differential voltage components into the multi-stage rectifier. Its working principle is that the multi-stage structure can process signals of different power in segments, while maintaining linearity and expanding the detection range [19].

In rectifier1, the output common-mode voltage of the limiting amplifier is V_{cm}, the output differential-mode voltage is V_{id}, and I_{c21}, I_{c22}, and I_{c23} are the collector currents of Q21, Q22, and Q23, respectively. The mathematical proof is as below:

$$V_{cm} + \frac{V_{id}}{2} - V_{be21} = V_{cm} - V_{be23} \tag{3}$$

$$V_{cm} - \frac{V_{id}}{2} - V_{be22} = V_{cm} - V_{be23} \tag{4}$$

And $I_c = I_s \cdot e^{\frac{V_{be}}{V_T}}$, so

$$V_T \ln \frac{I_{c21}}{I_{s21}} - V_T \ln \frac{I_{c23}}{I_{s23}} = \frac{V_{id}}{2} \tag{5}$$

$$V_T \ln \frac{I_{c23}}{I_{s23}} - V_T \ln \frac{I_{c22}}{I_{s22}} = \frac{V_{id}}{2} \tag{6}$$

Choose Q23 emitter area to be twice the emitter area of Q21 and Q22,

$$I_{s23} = 2I_{s22} = 2I_{s21} \tag{7}$$

And

$$I_{c21} + I_{c22} + I_{c23} = I_{c24} \tag{8}$$

combine (5), (7) and (6), (8), respectively.

$$\frac{I_{c21}}{I_{c23}} = \frac{1}{2}e^{\frac{V_{id}}{2V_T}} \tag{9}$$

$$\frac{I_{c23}}{I_{c22}} = 2e^{\frac{V_{id}}{2V_T}} \tag{10}$$

Combine (8), (9), (10), so

$$I_{c21} = \frac{1}{2} \cdot \frac{I_{c24} \cdot e^{\frac{V_{id}}{2V_T}}}{1 + \frac{1}{2}(e^{\frac{V_{id}}{2V_T}} + e^{-\frac{V_{id}}{2V_T}})} \tag{11}$$

$$I_{c22} = \frac{1}{2} \cdot \frac{I_{c24} \cdot e^{-\frac{V_{id}}{2V_T}}}{1 + \frac{1}{2}(e^{\frac{V_{id}}{2V_T}} + e^{-\frac{V_{id}}{2V_T}})} \tag{12}$$

$$I_{c23} = \frac{I_{c24}}{1 + \frac{1}{2}(e^{\frac{V_{id}}{2V_T}} + e^{-\frac{V_{id}}{2V_T}})} \tag{13}$$

Then the output current of the rectifier is

$$\Delta I = IOUT1 - IOUT2 = I_{c21} + I_{c22} - I_{c23} = I_{c24} \cdot \tanh^2\left(\frac{VOUTN - VOUTP}{4V_T}\right) \tag{14}$$

The intermediate seven limiting amplifiers adopt a structure similar to the first one, as shown in Figure 5. An emitter follower is added between the main limiting amplifier and the common-mode extractor as a buffer to isolate inter-stage interference. The input of the emitter follower is coupled to the output of the main limiting amplifier, and the common-mode component of buffer output is made to be consistent with the common-mode of the main amplifier by adjusting the Vce of Q4 and Q6. The rectifier synchronously extracts the common-mode voltage and differential output by the limiting amplifier to generate output current that is logarithmic to the input voltage.

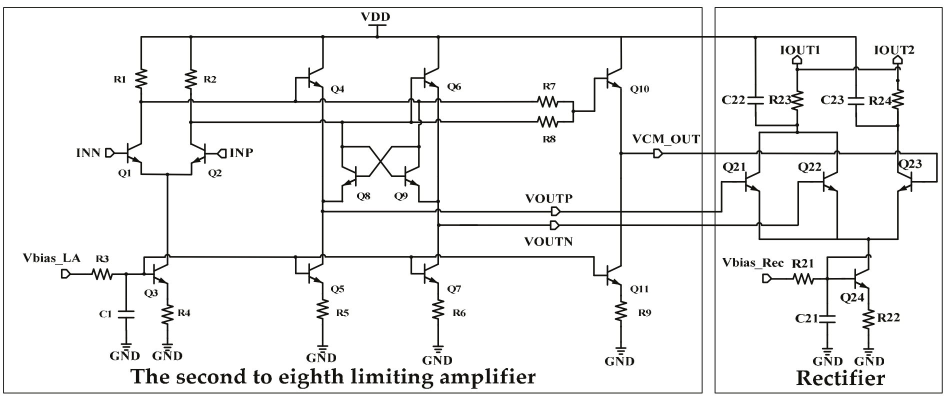

Figure 5. Limiting amplifiers from #2 to #8 and rectifier.

The ninth limiting amplifier is basically the same as that of the previous stage, as shown in Figure 6. This limiting amplifier adds an offset amplifier to extract the output offset of the nine-stage limiting amplifiers, which is fed back to the first limiting amplifier in the form of a current to reduce the inter-stage offset [20,21].

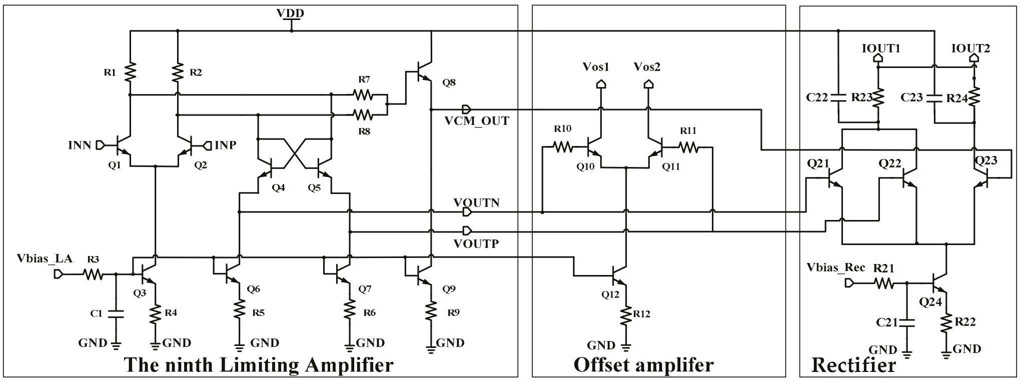

Figure 6. Limiting amplifier #9, offset amplifier, and rectifier.

As shown in Figure 7, the output stage is a current mirror that converts differential input current to single-ended output voltage. By neglecting the base current and the Early effect, for node A and node B, respectively,

$$\frac{V_{DD} - V_A}{R_1} + IOUT2 = Iout + I_1 \tag{15}$$

$$\frac{V_{DD} - V_B}{R_2} + IOUT1 = I_2 \tag{16}$$

By setting transistors Q1 and Q2 to be exactly the same, with resistors R1 = R2, and combining (15) and (16)

$$\frac{V_B - V_A}{R_1} = Iout + IOUT1 - IOUT2 \tag{17}$$

For the voltage of node C

$$V_A - I_1 \cdot R_4 + V_{be4} = V_B - I_2 \cdot R_5 + V_{be5} \ \Rightarrow \ V_A = V_B \tag{18}$$

Put (18) into (17), then

$$Iout = IOUT2 - IOUT1 \tag{19}$$

Finally, it can be obtained

$$Vout = Iout \cdot R_6 = (IOUT2 - IOUT1) \cdot R_6 \tag{20}$$

It can be seen from (20) that the difference in output current of rectifier is converted into a single-ended output voltage. The value of resistor R6 needs to be carefully designed. On one hand, it is necessary to ensure that the output voltage has sufficient amplification gain; and on the other hand, it is necessary to ensure that I1 is small and will not generate excessive power consumption in the output stage.

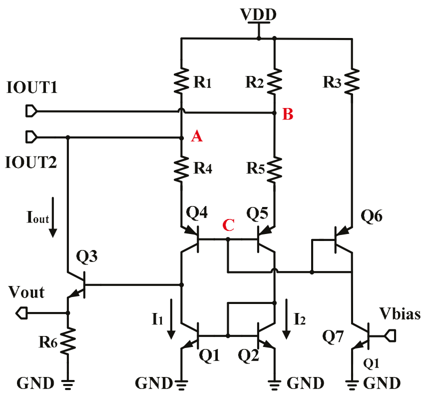

Figure 7. Output stage.

The log slope adjuster is shown in Figure 8, which is a two-stage amplifier and constructs a feedback loop with the output stage through an external adjustable resistor $R_{off\text{-}chip}$. The output current of rectifiers has inherent deviation, and if directly fed into the output stage, it will cause saturation. The log slope adjuster adjusts the base voltage of Q4. Hence, the base voltage of Q10 varies, thereby controlling the difference between the output currents IOUT1 and IOUT2. When $R_{off\text{-}chip}$ increases, $V_{be,Q4}$ decreases. Then $I_{c,Q4}$ and the gain of amplifier increases, which improves output voltage. Therefore, $V_{be,Q10}$ rises to increase the output current IOUT1/IOUT2 and the log slope. However, if the $R_{off\text{-}chip}$ decreases, the amplifier gain and output voltage also reduce. Therefore, $V_{be,Q10}$ and the output current IOUT1/IOUT2 decrease, which finally reduces the log slope. This scheme dynamically injects the compensation current into the input of the output stage to calibrate the logarithmic transfer function. This mechanism achieves an adjustable log slope while avoiding output stage saturation.

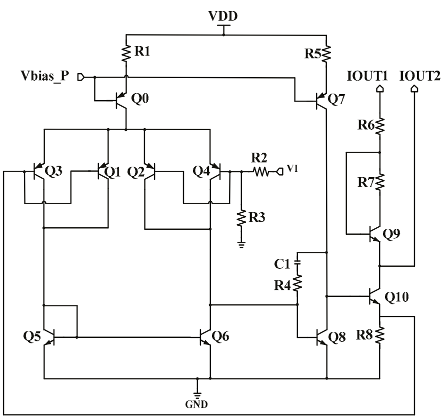

Figure 8. The log slope adjuster.

In Figure 9, the power-down circuit is actually a comparator. Because R1 = R2, it compares the input PWDN with VDD/2. If PWDN is high, then the base voltage of transistor Q5 becomes low. Hence, the bias current will be nullified and the Bandgap_LA will be turned off. At the same time, the output PWDN_Rec also becomes low, and the Bandgap_Rec circuit is also turned off. At this point, the overall logarithmic amplifier enters low-power standby mode. When PWDN is low, the Startup circuit works normally and starts the Bandgap core. During the power-on process, capacitor C2 is charged to remove the Bandgap from the dead zone, ensuring that the circuit can start normally. Because

$$I_{R_{12}} \cdot R_{12} = \Delta V_{be} = V_{be14} - V_{be16} = V_T \cdot \ln n \tag{21}$$

ΔV_{be} has a positive temperature coefficient, and

$$V_A = \Delta V_{be} + V_{be,Q16} = V_T \cdot \ln n + V_{be,Q16} \tag{22}$$

Since $V_{be,Q16}$ has a negative temperature coefficient, V_A with a zero temperature coefficient is achieved to bias Q19. In addition, the currents of R_{15} and R_{16} also have a positive temperature coefficient. At the output node, due to the negative temperature dependence of $V_{be,22}$, it can be obtained

$$Vout = I_{R_{16}} \cdot R_{16} + V_{be23} \tag{23}$$

We thus obtained the output Vout with zero temperature coefficient. To compensate for high-order nonlinearity of V_{be}, resistor R9 is connected in series with the output terminal and fed back to the base of two transistors Q14/Q16. Due to the positive temperature dependence of resistors, by superimposing the parabolic curve of first-order compensation with the positive temperature curve of the resistor, and adjusting the value of resistor R9, a reference of high-order compensation can be obtained.

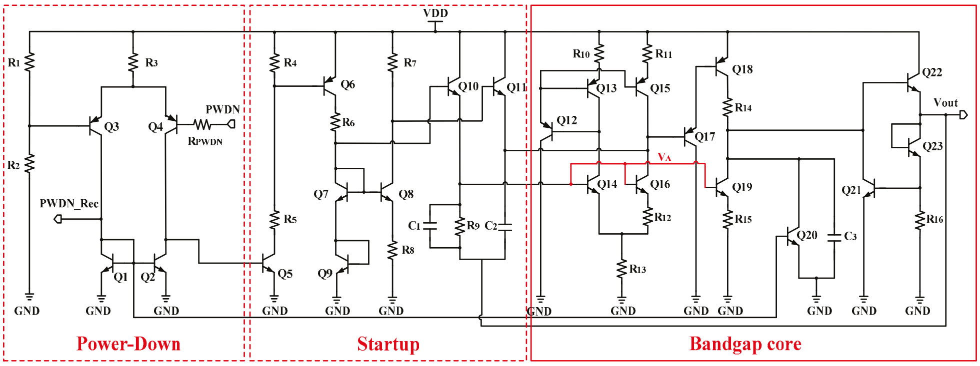

Figure 9. Bandgap_LA.

3. Post Simulation Results

The logarithmic amplifier is realized using 180 nm 1P6M SiGe BiCMOS technology. The power supply voltage is 5 V, and the power consumption during normal operation is 109 mW. The power consumption in power-down mode is reduced to 162 µW. The layout is shown in Figure 10, with an area of 1230 µm × 1010 µm.

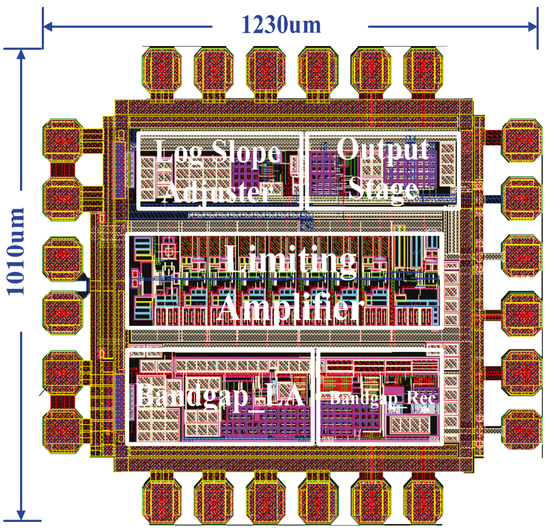

Figure 10. Layout of logarithmic amplifier.

As shown in Figure 11, under the temperature of 25 °C, when the input frequency is 50 MHz, 2.5 GHz, and 4 GHz, the dynamic ranges are 85 dB, 83 dB, and 82 dB, respectively. The log slopes are 16.8 mV/dB, 16.9 mV/dB, and 17.1 mV/dB, respectively, and the minimum detectable input power is −85 dBm, which is also the noise floor. Within the dynamic range, the log error range is as shown in Figure 12, and the overall range is within ±1 dB.

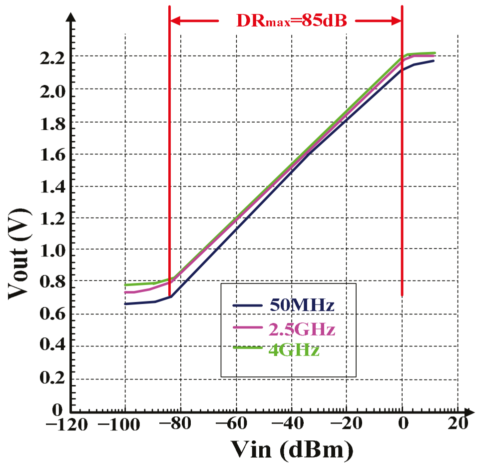

Figure 11. Output versus Vin.

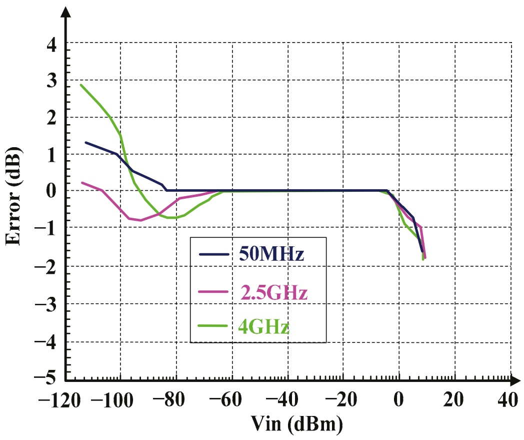

Figure 12. Log Conformance versus Vin.

The AC response of the logarithmic amplifier is shown in Figure 13. With a power supply voltage of 5 V, the 3 dB bandwidth is 20 MHz–4 GHz, and the overall gain reaches 90 dB.

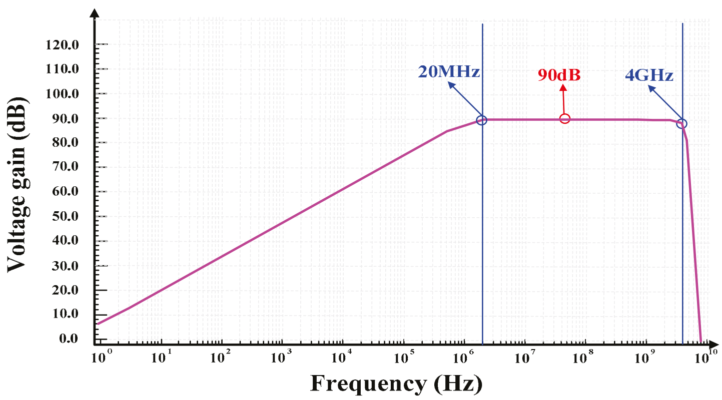

Figure 13. AC response.

Figure 14 shows the logarithmic output results of adjusting $R_{off\text{-}chip}$ at different values. The value varies within the range of 1 kΩ–18 kΩ, and the log slope range is 16.8 mV/dB to 30.1 mV/dB. The output voltage also increases with the increase of resistance.

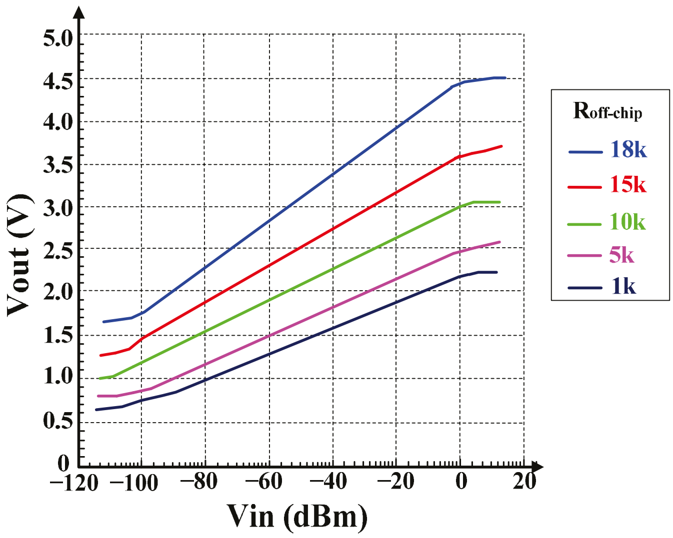

Figure 14. Vout Versus $R_{off\text{-}chip}$.

When the input frequencies are 50 MHz and 4 GHz respectively, the output is as shown in Figure 15. The response times for the output to rise from 10% to 90% amplitude are 42 ns and 44 ns, respectively, which means it has fast response to sudden input.

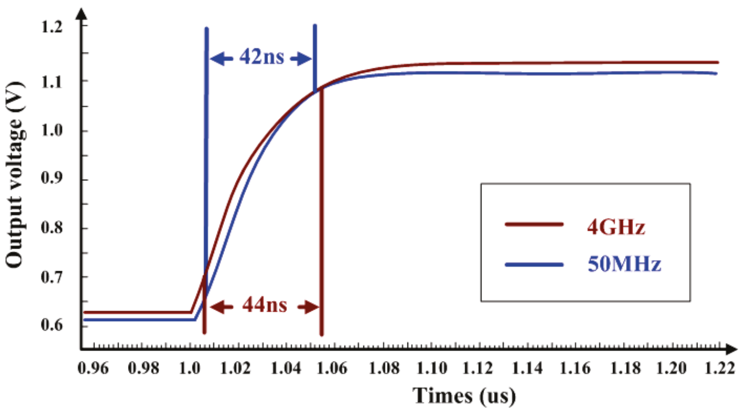

Figure 15. Response Time of 50 MHz and 4 GHz.

A comparison results of this work with others is shown in Table 1. Due to the use of the nine-stage limiting amplifier with 10 dB-gain each, a largest dynamic range has been achieved. Meanwhile, the sum of current of each stage improves the response time. Compared with previous achievements in parameters such as bandwidth, log error, and response time, it has realized a good compromise. At the same time, with a power supply of 5 V, our design also has a log slope adjuster and a power-down mode, which has more completed functions than other works. Because more limiting amplifiers are cascaded, a portion of power consumption is sacrificed to achieve performance improvement. The figure of merit (FoM) can be expressed as the ratio of power consumption to dynamic range and bandwidth, i.e., mW/(dBm × GHz). The smaller the FoM, the better the performance.

Table 1. Performance comparison.

Parameter	[10]	[12]	[14]	[22]	[23]	This Work
Process	180 nm CMOS	350 nm CMOS	130 nm CMOS	180 nm CMOS	180 nm CMOS	180 nm SiGe BiCMOS
Power supply (V)	3.3	2.5	2	1.8	1.8	5
Bandwidth (GHz)	0.001	2.4	16	1.8	10.6	4
Dynamic range (dB)	70	43	43	29	20	85
Log error (dB)	N/A *	N/A	±1.5	±1	±2.4	±1
Response Time (ns)	N/A	N/A	N/A	N/A	N/A	42
log slope adjustment	N/A	N/A	No	No	No	Yes
Pdc (mW)	19	184	35.2	16	10.8	70
FoM (mW/(dBm × GHz))	271.4	1.78	0.051	0.31	0.051	0.21

* "N/A" means the parameter is not listed in the paper.

4. Conclusions

Based on the GSMC 180 nm SiGe BiCMOS 1P6M process, a high dynamic range and fast response logarithmic amplifier is presented. In order to meet the detection requirements of different input power, a log slope adjuster is proposed, which can adjust the slope of the logarithmic output by adjusting the off-chip resistor. Meanwhile a power-down function is also added, which can significantly reduce power consumption in standby mode. The post-simulation results show that at a power supply voltage of 5 V, 3 dB bandwidth of 4 GHz is achieved, while the logarithmic error is only ±1 dB. The dynamic range can reach over 80 dB with a response time of 42 ns. Meanwhile the adjustable log slope range is 16.8–30.1 mV/dB. Under normal operation and power-down modes, the power consumption is 109 mW and 162 μW, respectively.

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Article

Research on a General SER Rate Prediction Model Based on a Set of Configuration Parameters Related to SER

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Abstract: This article comprehensively analyzes the new developments and challenges faced by several typical prediction models in the field of radiation effects in recent years. The models discussed include the RPP model, the extended RPP (rectangular parallelepiped) model, and the IRPP (integral rectangular parallelepiped) model. The article conducts a comprehensive analysis of the limitations of the assumption that uses the linear energy transfer (LET) of incident particles and the SEU (single-particle upset) cross-section (without considering the energy and type of ions) to predict the rate of single-particle effects (SEUs). Additionally, the article points out that with the continuous progress of integrated circuit technology, the geometric shape of the target circuit, the energy of the incident particles, the type of particles, and more precise physical models corresponding to the interaction between radiation and matter have become increasingly important in evaluating the sensitivity to single-particle effects (SEEs). Subsequently, based on the probability characteristics of SEE, a series of general estimation equations for the SEE rate are derived, considering particle energy, particle type, and the probability of influence at a specific moment. Then, by introducing the concept of interaction volume, the concept of sensitive volume is further expanded, and using these general equations, the relationship between the SEE rate cross-section and the SEE projected area is derived, simplifying the SEU rate prediction equation to a form that can be directly used in engineering applications. Finally, the article emphasizes a complete method of applying the general prediction equation to engineering to estimate the radiation disturbance performance of two typical verification circuits, and provides the corresponding prediction results.

Keywords: SER; RPP; IRPP; LET; MC; SER rate prediction

1. Introduction

Particle radiation, whether from space and Earth's environment or from artificial sources such as particle accelerators, radioactive particle sources, and nuclear radiation environments, can affect the normal operation of electronic components. When the effects are caused by the passage of a single particle rather than the cumulative effect of many particles, it is referred to as SER [1]. SER is induced by the random incidence of particles of different types, energies, and angles of incidence [2]. Since the early recognition of SER as a factor influencing reliability in space and terrestrial environments, the observed single-event effects have been classified into two main categories: soft errors (such as Single-Event Upsets or Single-Event transients) and hard errors (such as Single-Event Latch Up, Single-Event Burnout, Single-Event Gate punch-through, etc.). Furthermore, various methods have been developed, such as the RPP and IRPP models, to measure and predict their frequency [3–13].

Up to now, the most widely used prediction models and computer codes for SER Rate are the RPP and IRPP models [13–16], which are based on energy deposition and charge collection. These models have been factually established for nearly 40 years to predict the error rates of different process circuits or devices in various space environments [17]. Over the years, their extensive usability and effectiveness have been validated through continuous verification with on-orbit data, demonstrating their fundamental quality and prompting ongoing improvements in their past applications [18].

The RPP model is simplified into a single integral about chord length and LET distribution by adopting many assumptions that are independent of device size and difficult to prove physically, realizing the simplicity and ease of use of the prediction model form [19]. These assumptions are the basis of the RPP prediction model. If any of them is in doubt, the prediction results will be suspicious [20–26]. Moreover, since the RPP model is a single sensitive model, any generalization and expansion of more complex systems will propagate its assumptions. The RPP model is based on energy deposition, because in the absence of such additional information as device structure or circuit topology, energy (or equivalent charge) is the only available effect characterization quantity. The correlation between the deposited energy and the circuit SER effect is realized by a single sensitive body. Therefore, an effective extension of the RPP model is to redefine the sensitive body.

The basic new physical basis of the IRPP model compared with the RPP model lies in the relaxation of the assumption that the inversion can be characterized by a single critical charge or effective energy [18]. The IRPP model assumes that there is a series of critical energies due to changes between cells in the measurement. In this case, the measurement cross-section of an integrated circuit composed of many nominally identical cells (such as memory) will deviate from the expected result of a single cell.

Essentially, the randomness of the radiation effect is attributed to the initial radiation and subsequent radiation transfer, and the circuit is assumed to be deterministic. Here, we first demonstrate a series of general equations (Monte Carlo simulation and engineering test evaluation) that can be used to predict the rate of SER from the perspective of particle energy, particle type, and effect probability at a certain time, and these equations can be simplified into familiar analytical forms when making sufficiently extreme simplifying assumptions. The strength of the MC (Monte Carlo) method is that even without these simplified assumptions, it is still treatable, which in principle can achieve more accurate estimates. Then, the concept of sensitive body is extended, the concept of interaction body is introduced, and the corresponding relationship between the SER rate cross-section and the SER projected area is revealed by using the general equation. The SER Rate prediction equation is simplified into an analytical form that can be directly used in engineering. Finally, the complete idea and the prediction results of the radiation resistance performance of two typical verification circuits by using the prediction equation in engineering are emphatically provided.

2. Mathematical Foundations of Rate Prediction

The key indicator for analyzing SER is the SER Rate in a given radiation environment. The purpose of this section is to describe a comprehensive mathematical framework that can be used for predicting the SER Rate, expanding upon the approach first proposed by Weller et al. [27].

2.1. General Single-Event Effect Rate Equation

Peterson et al. have conducted a thorough review of the mathematical foundations for predicting SER Rate [18]. However, the computational methods they described begin with a direct and deterministic relationship between energy deposition and the properties of the incident particles. In this work, we employ a general model to analyze the prediction of SER Rate, which allows us to calculate the probability of any effect caused by a single quantum of radiation. In this model, the term "event" is used to describe the interaction between the radiation quantum and the system being analyzed. The process initiated by a single radiation quantum is referred to as an "effect." For each event, there exists a probability associated with this "effect". The foundation of predicting SER Rate is based on the calculus of these probabilities.

First, suppose that the research subjects, such as sample devices, circuits, or systems, exist within or around a spatial region referred to as the "world". Assume that the world is a convex body, and the surface normal unit vector at position $\vec{x}$ is denoted as $\hat{n}\left(\vec{x}\right)$.

The research subjects are relatively stationary in the world reference system. The size of the world is unspecified with respect to both the absolute size and the relative size of the research object, and it is assumed that the occurrence of effects is entirely determined by the physical processes occurring within the world.

According to the sources of particle radiation surrounding the research subjects, particle radiation sources can be divided into two independent categories: particles entering the world from external sources, such as cosmic rays, and particles originating from within the world itself, such as those produced by spontaneous radioactive decay.

The external radiation source is completely specified at every point on the world surface by the flux distributions $\hat{u}\Phi\left(z, E, \hat{u}, \vec{x}, t_x\right)$. The internal radiation source is specified by a local generation rate $G\left(z, E, \hat{u}, \vec{x}, t_x\right)$. Here, z denotes the type of particle, such as γ-rays, protons, α-particles, heavy ions, etc. With heavy ions further defined by their atomic number and mass number, E is the particle energy, $\hat{u}$ is a unit vector specifying the particle direction, $\vec{x}$ is a vector specifying a point of origin on the world surface or within the world volume, and t_x is the time at which the flux is sampled at location $\vec{x}$. The units of the flux are, for example, particles per second, per square centimeter, per MeV, per steradian. The units of the volume generation rate are particles per second, per cubic centimeter, per MeV, per steradian. A typical space environment contains many species, z.

The physical behavior of the system is determined by the probability per unit time $P\left(z, E, \hat{u}, \vec{x}, t_x; \xi, t\right)$ that a quantum of type z, which has initial energy E, direction $\hat{u}$, and position $\left(\vec{x}, t_x\right)$, will result in an effect during the interval dt at time t. The argument ξ represents a set of configuration parameters on which this probability may depend. For example, in the RPP model, the size of the RPP and the critical energy E_c are such parameters. Given these three definitions—flux, generation rate, and effect probability—the SER Rate at time t for configuration parameters ξ can be expressed as:

$$
\begin{aligned}
R_e(\xi, t) = & \sum_z \int_{All\ E} dE \int d\Omega \oint dS \left(-\hat{n}\left(\vec{x}\right) \cdot \hat{u}\right) \times H\left(-\hat{n}\left(\vec{x}\right) \cdot \hat{u}\right) \\
& \times \int_{-\infty}^{t} dt_x \Phi\left(z, E, \hat{u}, \vec{x}, t_x\right) P_e\left(z, E, \hat{u}, \vec{x}, t_x; \xi, t\right) \\
& + \sum_z \int_{All\ E} dE \int d\Omega \int dx^3 \int_{-\infty}^{t} dt_x \Phi_i\left(z, E, \hat{u}, \vec{x}, t_x\right) P_e\left(z, E, \hat{u}, \vec{x}, t_x; \xi, t\right)
\end{aligned}
\tag{1}
$$

Here, $H(x)$ is the Heaviside unit step function. Reading from the inside out, the integrals in the first term are over all times t_x prior to t; over the whole of the world surface area S; over all particle directions Ω, where $d\Omega$ denotes the differential solid angle in the

$\hat{u}$ direction; and over all particle energies E. In the second term, the surface integral is replaced by a volume integral over all of the volume enclosed by the world surface. In both terms, the sum is over all species in the respective radiation environment. In the first term, the step function $H(x)$ constrains the surface and angular integrals to contributions for which $\hat{n}\left(\vec{x}\right) \cdot \hat{u} < 0$(that is, inward) [28]. The minus sign appears because the world surface is described by an outward normal vector, while only particles on the world surface that are directed inward are capable of producing an effect. The second term contains no such constraints because spontaneous emission of radiation in any direction within the volume defined by the world surface is potentially significant.

Next, based on the intrinsic characteristics of radiation effects, several forms of Equation (1) are presented under different assumed conditions:

Assumption 1. *The local generation rate of internal radiation sources is zero.*

Assumption 2. *Particle flux is relatively time independent.*

For nearly all scenarios of interest regarding SER, there is no apparent relationship between the duration of SER and variations in average flux. Therefore, it can be assumed that the flux is time independent. Combined with Assumption 1, this allows Equation (1) to be transformed into:

$$\begin{aligned} R(\xi,t) = \sum_z \int_{All\ E} dE \int d\Omega \oint dS\left(-\hat{n}\left(\vec{x}\right) \cdot \hat{u}\right) \\ \times H\left(-\hat{n}\left(\vec{x}\right) \cdot \hat{u}\right) \Phi\left(z,E,\hat{u},\vec{x}\right) \\ \times \int_{-\infty}^{t} dt_x P\left(z,E,\hat{u},\vec{x},t_x;\xi,t\right) \end{aligned} \tag{2}$$

Assumption 3. *Radiation transport and effects are instantaneous, and the effect probability P is independent of time.*

When both the total time for radiation transport and the occurrence time of the effects are very short, this type of effect is referred to as an "instantaneous" effect [27]. In the limit case of instantaneous effects, it can be expressed using the Dirac delta function:

$$\begin{aligned} P\left(z,E,\hat{u},\vec{x},t_x;\xi,t\right) = \\ \lim_{\varepsilon\to 0} P\left(z,E,\hat{u},\vec{x},t_x;\xi\right)\delta(t_x - t + \varepsilon) \end{aligned} \tag{3}$$

Thus, Equation (2) can be further simplified to:

$$\begin{aligned} R(\xi,t) = \sum_z \int_{All\ E} dE \int d\Omega \oint dS\left(-\hat{n}\left(\vec{x}\right) \cdot \hat{u}\right) \\ \times H\left(-\hat{n}\left(\vec{x}\right) \cdot \hat{u}\right) \Phi\left(z,E,\hat{u},\vec{x}\right) P\left(z,E,\hat{u},\vec{x},t;\xi\right) \end{aligned} \tag{4}$$

In this case, it is clear that if the effects are independent of time, then the SER Rate is a constant:

$$\begin{aligned} R(\xi) = \sum_z \int_{All\ E} dE \int d\Omega \oint dS\left(-\hat{n}\left(\vec{x}\right) \cdot \hat{u}\right) \\ H\left(-\hat{n}\left(\vec{x}\right) \cdot \hat{u}\right) \Phi\left(z,E,\hat{u},\vec{x}\right) P\left(z,E,\hat{u},\vec{x};\xi\right) \end{aligned} \tag{5}$$

Assumption 4. *The particle radiation environment is homogeneous and isotropic.*

Since the flux is isotropic, the particle flux is no longer a function of the starting point and direction, that is:

$$\Phi\left(z, E, \hat{u}, \vec{x}\right) = \Phi(z, E) \tag{6}$$

The prediction of the error rate for a specific effect is obtained by constructing the appropriate probability distribution function and performing the specified integrals. The starting point for calculating the error rate may be Equations (1), (2), (4), and (5), depending on the specific situation.

2.2. The Projected Cross-Sectional Area

In order to establish a correspondence between the aforementioned general SER Rate equation and other equations involving cross-sections, the concept of the sensitive volume familiar in SER studies is extended by introducing the concept of the interaction volume. The interaction volume is the region where physical processes that can directly lead to observable effects occur. It is clear that the sensitive volume is a special form of the interaction volume, but the concept of the interaction volume is more general, especially in the fields of nuclear and particle physics. For example, if the effect is a nuclear reaction, the interaction volume is a sphere with a radius equal to the sum of the radii of the two interacting nuclei. When the interaction volume is described by a cross-section, whether differential or integral, the following assumptions are involved:

Assumption 1. *The effect is instantaneous and time independent.*

Assumption 2. *Interactions only occur within the interaction volume and not before the incident particles reach the interaction volume.*

This assumption implies that the world volume can be reduced to conform to the interaction without losing generality.

Assumption 3. *The trajectories of the incident particles are all parallel and uniformly distributed over the projected area of the interaction volume.*

Thus, the flux distribution associated with a particle beam can be expressed as:

$$\Phi(z, E, \hat{u}, \vec{x}) = \Phi_0 \delta(E - E_0) \delta^2(\hat{u} - \hat{u}_0) \delta_{zz_0} \tag{7}$$

Here, Φ_0 is the flux in particles/(cm^2·s), which is assumed to be independent of $\vec{x}$, in accordance with assumption #3; δ and δ^2 are the one- and two-dimensional Dirac delta functions; and the subscripted is the Kronecker delta.

Combined with hypothesis # 1, substitute Equation (7) into Equation (5), and according to the Dirac Delta function equivalence relationship equation and the properties of the Kronecker Delta function [29], Equation (5) can be further simplified:

$$\begin{aligned} R(\xi) = \Phi_0 \oint dS(-\hat{n}(\vec{x}) \cdot \hat{u}_0) H(-\hat{n}(\vec{x}) \cdot \hat{u}_0) \\ \times P(z_0, E_0, \hat{u}_0, \vec{x}; \xi) \end{aligned} \tag{8}$$

Assumption 4. *The beam intensity is uniform within the sampled cross-sectional area and is independent of the initial position point.*

That is:

$$P(z_0, E_0, \hat{u}_0, \vec{x}; \xi) = P(z_0, E_0, \hat{u}_0; \xi) \tag{9}$$

Thus, Equation (8) is transformed into:

$$R(z_0, E_0, \hat{u}_0; \xi) = \Phi_0 P(z_0, E_0, \hat{u}_0; \xi) \\ \times \oint dS \left(-\hat{n}\left(\vec{x}\right) \cdot \hat{u}_0 \right) H\left(-\hat{n}\left(\vec{x}\right) \cdot \hat{u}_0 \right) \tag{10}$$

where the full integral represents the projected area of the interaction volume surface in the $\hat{u}_0$ direction, denoted as $S_N(\hat{u}_0)$. Therefore:

$$R(z_0, E_0, \hat{u}_0; \xi) = \Phi_0 P(z_0, E_0, \hat{u}_0; \xi) S_N(\hat{u}_0) \tag{11}$$

According to the definition of the interaction cross-section as the ratio of the effect rate to the flux:

$$\sigma(z_0, E_0, \hat{u}_0; \xi) \equiv \frac{R(z_0, E_0, \hat{u}_0; \xi)}{\Phi_0} \tag{12}$$

The correspondence between the effect probability and the projected area can be expressed as follows:

$$P(z_0, E_0, \hat{u}_0; \xi) = \frac{\sigma(z_0, E_0, \hat{u}_0; \xi)}{S_N(\hat{u}_0)} \tag{13}$$

In engineering, $\sigma(z_0, E_0, \hat{u}_0; \xi)$ represents the SER data measured in ground tests, while $P(z_0, E_0, \hat{u}_0; \xi)$ is an expression concerning a set of configuration parameters ξ related to SER in integrated circuits. Here, in order to correspond with the cross-section $\sigma(z_0, E_0, \hat{u}_0; \xi)$, $S_N(\hat{u}_0)$ will be referred to as the projected cross-section or intrinsic cross-section.

From the expressions of Equations (12) and (13), we can observe:

(1) For effects that essentially have unit probability $P(z_0, E_0, \hat{u}_0; \xi) \simeq 1$, such as SEUs induced by highly ionizing heavy ions, the size of the SER cross-section is equal to the projected area $S_N(\hat{u}_0)$ of the interaction volume in the $\hat{u}_0$ direction.

(2) For integrated circuits constructed from basic units with the same SER Rate (or sensitivity), the reliability distribution of the projected cross-section $S_N(\hat{u}_0)$ can be physically characterized using the Weibull function, owing to the reliability of previous data processed using this function. At this point, the exact value of the configuration parameter ξ in Equation (17) can be determined through the best Weibull fit of $S_N(\hat{u}_0)$. Of course, for other cases when circuits are specified, the projected cross-section $S_N(\hat{u}_0)$ must also correspond to some exact distribution function, although it does not necessarily have to satisfy Weibull distribution.

(3) During high-energy particle irradiation, the circuit exhibits a certain degree of saturation characteristics, meaning $P(z_0, E_0, \hat{u}_0; \xi) = 1$. At this point, the cross-section $\sigma(z_0, E_0, \hat{u}_0; \xi)$ is equal to the projected area $S_N(\hat{u}_0)$ of the interaction volume/world surface in the $\hat{u}_0$ direction. Of course, $P(z_0, E_0, \hat{u}_0; \xi)$ can also be greater than 1, indicating a supersaturation characteristic, which corresponds to a situation where one incident particle induces multiple effects, such as Multiple Bit Upsets in SEU.

(4) When the particle energy and type are fixed, the size of the projected area $S_N(\hat{u}_0)$ is determined by the configuration parameter set ξ related to the effects on the circuit and the initial position parameters $\hat{u}_0$ of the incident particles. Therefore, if the position of the incident particles is fixed or unchanged, the distribution of $P(z_0, E_0, \hat{u}_0; \xi)$ can be used to infer the consistency of the configuration parameter set ξ related to SER, providing important performance evaluation means for radiation-hardened integrated circuit designers.

(5) Equations (12) and (13) provide important bases for evaluating the radiation-hardened performance of circuits in engineering. In practice, the effect cross-section of the circuit can be directly calculated based on test data using the definition of Equation (12), such as the SEU cross-section, single-event transient cross-section, single-event burnout

cross-section, etc. Then, according to Equation (13), the projected area $S_N(\hat{u}_0)$ of the interaction volume within the circuit in different $\hat{u}_0$ directions can be calculated, which represents the overall radiation-hardened performance of the circuit.

(6) The derivation process of Equations (12) and (13) does not require specifying the shape of the interaction volume. The effect rate is only related to the projected area of the interaction volume and the effect probability; thus, this model has good universality.

2.3. SER Rate Prediction

When the radiation environment is known, Equation (1) can be used to calculate the occurrence rate of any SER, and its probability $P\left(z, E, \hat{u}, \vec{x}, t_x; \xi, t\right)$ can be determined. It is equally applicable to individual transistors, functional IP modules, entire integrated circuits, or large systems. For engineering purposes, to obtain conservative predictions with high confidence, or at least known confidence levels, the fundamental issue is the appropriate approximation of the physical system (assumption conditions). For space SER, Equation (11) can be directly extended into a very important relationship:

$$R(\xi) = \sum_{All\ E} \sum_{z} \sum_{\hat{u}} \Phi\left(z, E, \hat{u}, \vec{x}\right) P\left(z, E, \hat{u}, \vec{x}; \xi\right) S_N(\hat{u})$$

That is, summing is over all particle types z, all energy fluxes E, and all directions of particles. Here, $\Phi\left(z, E, \hat{u}, \vec{x}\right)$ represents the differential directional flux of particles in a specific direction $\hat{u}$, energy E, and particle type z.

Assuming that the spatial particle radiation environment is uniform and isotropic, this equation can be further simplified in conjunction with Equation (6):

$$R(\xi) = \sum_{All\ E} \sum_{z} \sum_{\hat{u}} \Phi(z, E) P(z, E, \hat{u}; \xi) S_N(\hat{u}) \tag{14}$$

This equation outlines the steps for estimating the on-orbit SER Rate using projected cross-sections: First, define the expression $P(z, E, \hat{u}; \xi)$, which contains a set of configuration parameters ξ related to the probability of circuit effects. Then, based on ground test data, obtain the distribution function $S_N(\hat{u})$ that reflects the intrinsic SEU characteristics of the circuit through best fitting. Finally, according to the characterization of space particle properties, such as particle flux $\Phi(z,E)$, the on-orbit effect rate of microelectronic circuits can be estimated using Equation (14).

3. Example Applications of Rate Prediction

Here, we choose a spherical coordinate system where the z-axis is aligned with the normal to the circuit plane. The unit vector $\hat{u}$ of the incident particle direction can be characterized by the azimuthal angle φ in the (ZOY) plane and the inclination angle θ in the (XOY) plane, which are used to constrain the direction of the incident particles. Referring to the relevant literature [30], $P(z, E, \hat{u}; \xi)$ is defined (of course, it can also be another expression) as:

$$\begin{aligned} P(z, E, \hat{u}; \xi) &\equiv P(\theta, \varphi) \\ P(\theta, \varphi) &= \sqrt{\left({A_P}^2 \cos^2 \varphi + B^2 \sin^2 \varphi\right) \sin^2 \theta + \cos^2 \theta} \end{aligned} \tag{15}$$

Clearly, the set $\{A_P, B\}$ represents a group of configuration parameters related to the probability of circuit SER mentioned in Equation (14), that is, $\xi = \{A_P, B\}$. The values of A_P and B can be determined through a best fitting method.

Equation (14) can be equivalently transformed into a triple integral concerning E, θ, and φ:

$$R(\xi) = \sum_z \int \int \int dE \sin\theta d\varphi d\theta \\ \times\Phi(z, E)P(z, E, \hat{u}; \xi)S_N(\hat{u}) \tag{16}$$

If each summation term in the equation represents an isotope from the periodic table, then calculating all the elements in the periodic table would yield hundreds of summation terms.

Since the data set obtained from ground accelerator simulation experiments pertains to LET (Linear Energy Transfer) and SER Rate, in order to directly utilize this data, we will combine the method proposed by Heinrich for calculating LET spectra to equivalently convert the energy E in Equation (14) into another quantity, LET. During this equivalent transformation process, the following assumptions need to be made:

Assumption 1. *The energy deposited in the sensitive volume equals the energy loss of the particles passing through that sensitive volume, and the magnitude of the energy loss can be calculated using its LET.*

For very short particle track lengths, this assumption may not hold [31]. This is due to the finite range of secondary electrons may cause some of the energy lost by ions to escape from the sensitive volume.

Assumption 2. *Ions with the same LET produce the same effects.*

This assumption implies that charged particles can be grouped and processed using the LET spectrum calculation method proposed by Heinrich [32].

The experimental basis for this assumption is limited; in fact, some exceptions have been discovered, such as two ions with different velocities but the same LET and different track structures. Although it currently appears that most exceptions have a negligible impact on SER Rate predictions, some laboratories are investigating this issue.

Assumption 3. *Variations in LET along the ion track within the sensitive volume can be neglected.*

This assumption is primarily used to exclude the following issue: ions with the same LET may have different ranges, thereby depositing different amounts of energy within the same volume. Range effects are a potential problem in accelerator simulations, but they are not encountered in the high-energy environments found in space.

Based on the above assumptions, Equation (16) can be further equivalently transformed into a single triple-integral calculation:

$$R(\xi) = \int_0^{\infty} \int_0^{2\pi} \int_0^{2\pi} d\varphi d\theta dL \\ \times\Phi(L, \theta, \varphi)P(\theta, \varphi)S_N(\theta, \varphi) \sin\theta \tag{17}$$

Since the flux is isotropic (a typical assumption for calculating heavy ion effect rates), the LET spectrum is the same in all directions. Therefore, the integral over angles in the triple integral of the SER prediction Equation (17) can be moved inward, and:

$$\Phi(L, \theta, \varphi) = 4\pi\Phi(L)$$

Here, $\Phi(L, \theta, \varphi)$ is referred to as the differential omnidirectional flux.

Furthermore, if we denote:

$$S_{AVG}(L) = \frac{2}{\pi}\int_0^{\frac{\pi}{2}} \int_0^{\frac{\pi}{2}} P(\theta, \varphi)S_N(\theta, \varphi) \sin\theta d\varphi d\theta \tag{18}$$

Here, $S_{AVG}(L)$ S_{AVG} is referred to as the average directional cross-section related to the effect probability. If the particle flux is symmetric both vertically and horizontally, then the average directional cross-section $S_{AVG}(L)$ can be further simplified as:

$$S_{AVG}(L) = \frac{2}{\pi}\int_{0}^{\frac{\pi}{2}}\int_{0}^{\frac{\pi}{2}} P(\theta,\varphi)S_N(\theta,\varphi)\sin\theta d\varphi d\theta \tag{19}$$

Thus, SER prediction Equation (17) transforms to:

$$R(\xi) = 4\pi\int_{0}^{\infty} \Phi(L)S_{AVG}(L)dL \tag{20}$$

Thus, based on the effect probability function $P(z,E,\hat{u};\xi)$, a general SER prediction model has been derived. Next, we will utilize ground heavy ion test data to predict the on-orbit error rate of two types of space-grade integrated circuits and provide a detailed prediction process.

3.1. Heavy Ion Experiment

In the next section, we will provide examples of overturn rate prediction for two test devices. The device information is shown in Table 1. First, use the best fit between the cross-section measured from the small-angle test and the directional cross-section obtained from Equation (13) to determine the two fitting parameters A_P and B in (15). In order to facilitate the calculation of these two parameters, the following two points should be focused on in the experimental scheme: first, in addition to the directional effect, other factors, such as counting statistical restrictions, particle range, or different test conditions, must result in the discrete distribution of the test data being small enough. The purpose is to clearly distinguish the direction dependence of the sectioning. Second, in the process of measuring the test section, the range of the test ion must be long enough. Within the range of the observed tilt angle, the direction dependence of the section must be clearly observed. The typical practice is to change the tilt angle θ between 0 ° and 60 °, φ taking 0 ° and 90 °, respectively. Then, the Weibull function is selected to best fit the direction section, extrapolate the direction section to a larger angle, and obtain the saturated direction section of the two devices. Finally, combined with the specific space orbit environment, the estimated error rate of the distribution is obtained.

Table 1. Test device information.

Device	Process	Capacity (Kbits)	Unit Structure	Bias (V)
MT168C	28 nm Bulk silicon CMOS process	16 × 8	6 T	0.85
MD328A	28 nm Bulk silicon CMOS process	32 × 8	Double DICE	0.85

Both heavy ion test campaigns were performed at the SER irradiating Facility on the HI-13 Tandem Accelerator in the China Institute of Atomic Energy, Beijing, and the Heavy Ion Research Facility in Lanzhou (HIRFL) in the Institute of Modern Physics, Chinese Academy of Sciences, which supplied high-energy ions. The devices were irradiated by the C, F, Cl, Ge, and Bi particles listed in Table 2. Provided in the table are the particles, LET, the incident tilt angle θ, the incident azimuth φ, and the SEU cross-sections σ. Applied flux was measured within ±10%, and the beam homogeneity was within ±10%. The typical heavy ion fluence rate was ~1×10^4 ions/cm^2/s for the SER test. The incident tilt angle was varied from 0° to 60°, and the incident azimuth was taken to be 0° and 90°, respectively.

In the table, the unit of LET is MeV·cm^2/mg, the unit of θ and φ is degree, and the unit of σ is /cm^2.

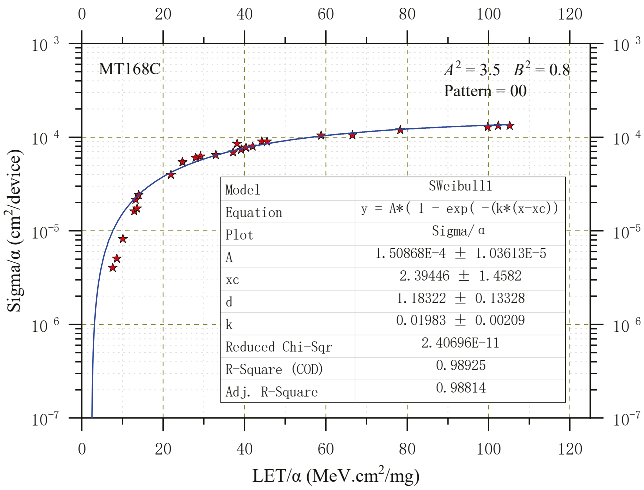
Table 2. The particles and the SEU cross-section at HI-13 and HIRFL.

Particles	LET	θ	φ	σ_{MT168C}		σ_{MD328A}	
				00	**FF**	**00**	**FF**
F	4.06	0	0	0.00	0.00	0.00	0.00
Cl	12.9	0	0	1.62×10^{-5}	3.24×10^{-5}	1.22×10^{-3}	1.52×10^{-2}
Ge	37.2	0	0	6.89×10^{-5}	1.18×10^{-4}	6.80×10^{-3}	1.68×10^{-1}
Br	42	0	0	7.95×10^{-5}	1.41×10^{-4}	8.75×10^{-3}	1.78×10^{-1}
Bi	99.8	0	0	1.28×10^{-4}	2.16×10^{-4}	1.82×10^{-2}	4.41×10^{-1}
F	4.06	30	0	0.00	0.00	0.00	0.00
F	4.06	45	0	0.00	0.00	0.00	0.00
F	4.06	60	0	0.00	0.00	0.00	0.00
Cl	12.9	30	0	1.04×10^{-5}	3.13×10^{-5}	8.44×10^{-4}	1.20×10^{-2}
Cl	12.9	45	0	7.56×10^{-6}	2.83×10^{-5}	7.16×10^{-4}	9.60×10^{-3}
Cl	12.9	60	0	6.82×10^{-6}	2.19×10^{-5}	6.39×10^{-4}	9.39×10^{-3}
Ge	37.2	30	0	7.93×10^{-5}	1.18×10^{-4}	6.53×10^{-3}	1.55×10^{-1}
Ge	37.2	45	0	8.09×10^{-5}	1.16×10^{-4}	7.89×10^{-3}	1.19×10^{-1}
Ge	37.2	60	0	6.73×10^{-5}	1.19×10^{-4}	6.33×10^{-3}	8.93×10^{-2}
Br	42	30	0	8.23×10^{-5}	1.39×10^{-4}	8.25×10^{-3}	1.83×10^{-1}
Br	42	45	0	9.04×10^{-5}	1.51×10^{-4}	8.64×10^{-3}	9.90×10^{-2}
Br	42	60	0	9.25×10^{-5}	1.11×10^{-4}	9.15×10^{-3}	9.94×10^{-2}
Bi	99.8	30	0	1.51×10^{-4}	2.54×10^{-4}	2.11×10^{-2}	5.01×10^{-1}
Bi	99.8	45	0	1.57×10^{-4}	2.92×10^{-4}	2.14×10^{-2}	5.44×10^{-1}
Bi	99.8	60	0	1.76×10^{-4}	2.86×10^{-4}	1.99×10^{-2}	4.99×10^{-1}
F	4.06	30	90	0.00	0.00	0.00	0.00
F	4.06	45	90	0.00	0.00	0.00	0.00
F	4.06	60	90	0.00	0.00	0.00	0.00
Cl	12.9	30	90	2.10×10^{-5}	3.93×10^{-5}	1.80×10^{-3}	1.80×10^{-2}
Cl	12.9	45	90	1.64×10^{-5}	3.19×10^{-5}	1.64×10^{-3}	1.64×10^{-2}
Cl	12.9	60	90	2.21×10^{-5}	3.50×10^{-5}	1.81×10^{-3}	1.81×10^{-2}
Ge	37.2	30	90	8.28×10^{-5}	1.29×10^{-4}	7.98×10^{-3}	1.69×10^{-1}
Ge	37.2	45	90	6.99×10^{-5}	1.52×10^{-4}	6.59×10^{-3}	2.19×10^{-1}
Ge	37.2	60	90	7.15×10^{-5}	1.13×10^{-4}	9.84×10^{-3}	1.61×10^{-1}
Br	42	45	90	8.55×10^{-5}	1.28×10^{-4}	8.15×10^{-3}	2.04×10^{-1}
Br	42	60	90	8.29×10^{-5}	1.46×10^{-4}	8.89×10^{-3}	2.08×10^{-1}
Bi	99.8	30	90	1.29×10^{-4}	2.01×10^{-4}	1.74×10^{-2}	4.24×10^{-1}
Bi	99.8	45	90	1.26×10^{-4}	1.88×10^{-4}	1.68×10^{-2}	3.95×10^{-1}

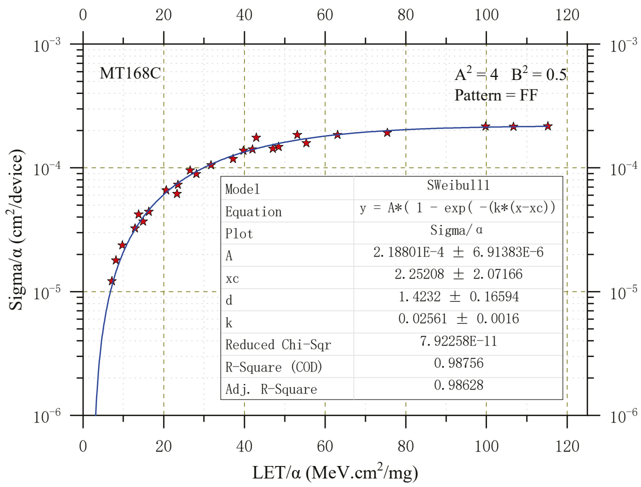
SELs were detected in any steps.

3.2. Heavy Ions Results

A complete specification of the directional cross-section requires not only values for A_P and B but also that the normal-incident cross-section be specified. Assuming that Equation (13) is correct, it is convenient to fit points with Weibull curves. The normal-incident cross-section curve is obtained with the least squares fit optimizing Weibull parameters, which were provided in the inset of Figures 1 and 2, where the ordinate sigma/α represents the normal SEU cross-section obtained after the data σ in Table 2 undergoes transformation by Equation (13), and $A_P{}^2$ and B^2 are the corresponding parameters in transformation Equation (15). Note that A^2 is not the square of A, as in the Weibull function.



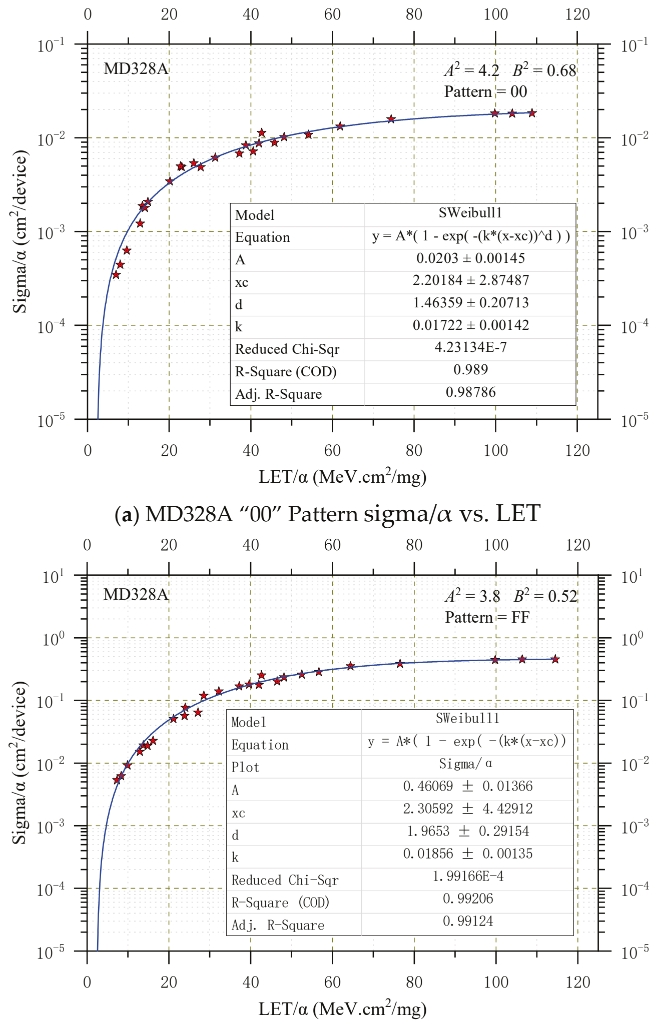
(**a**) MT168C "00" Pattern sigma/*α* vs. LET



(**b**) MT168C "FF" Pattern sigma/*α* vs. LET

Figure 1. SWeibull1 fit for MT168C heavy ion.

The smooth curves shown in Figure 1 for the normal-incident cross-section of MT168C under two patterns, '00' and 'FF', represent the best fit that can be found. But it probably is the simplest and is slightly conservative at the lower LETs, where its curvature does not conform to that indicated by the data points. The corresponding Weibull fitting parameters were automatically labeled on Figure 1a,b during the fitting process in Origin 2022 software. When the internal memory stored the '00' pattern, the Weibull parameters were obtained: A = 1.51×10^{-4}, $X_C = 2.40$, k = 1.98×10^{-2}, and d = 1.18 approximately; the parameters obtained from the best fit for α(θ,φ) are $A^2 = 3.5$ and $B^2 = 0.8$. When the internal memory stored the 'FF' pattern, the Weibull parameters were obtained: A = 2.19×10^{-4}, $X_C = 2.25$, k = 2.56 × 10^{-2}, and d = 1.42 approximately; the parameters obtained from the best fit for α(θ,φ) are A^2 = 4.0 and B^2 = 0.5.



(**a**) MD328A "00" Pattern sigma/α vs. LET

(**b**) MD328A "FF" Pattern sigma/α vs. LET

Figure 2. SWeibull1 fit for MD328A heavy ions SEU cross-sections as a function of LET.

Figure 2 shows the heavy ion in the normal-incident SEU cross-section of MD328A under two patterns, '00' and 'FF'. The normal cross-section sigma/α VS LET satisfies the SWeibull1 function very well. Based on the Weibull fitting parameters labeled on Figure 2a,b, when the internal memory stored the '00' pattern, the four Weibull parameters were obtained: A = 2.03 × 10^{-2}, X_C = 2.20, k = 1.72 × 10^{-2}, and d = 1.46 approximately; the parameters for α(θ,φ) are A^2 = 4.2 and B^2 = 0.68. When the internal memory stored the 'FF' pattern, the Weibull parameters were obtained: A = 4.61 × 10^{-1}, X_C = 2.31, k = 1.86 × 10^{-2}, and d = 1.96 approximately; the parameters for α(θ,φ) are A^2 = 3.8 and B^2 = 0.52.

From Figures 1 and 2, it can be observed that the single-event sensitivity is significantly higher when the graph is in the 'FF' pattern compared to the '00' pattern. This difference may stem from the slightly greater contribution of n-channel transistors to SEU compared to p-channel transistors [33,34].

3.3. SEU Prediction

When predicting the on-orbit SEU rate of the two devices, the interplanetary weather condition considered is galactic cosmic rays (GCRs) only [35], the atomic number of the heaviest element to be included in the LET spectra is 92, and the atomic number of the lightest element to be included in the LET spectra is 2. The integrated flux after passing through 3 mm aluminum is shown in Figure 3. The radiation resistances of these two circuits were evaluated separately. The LET value corresponding to 10% of the saturated cross-section is taken as the LET threshold [36]. When writing MT168C device in modes '00' and 'FF', the SEU rate is 6.01×10^{-6}/device-day and 9.31×10^{-6}/device-day, respectively. When device MD328A writes graphics '00'and 'FF', the SEU rate is 1.48×10^{-4}/device-day and 1.16×10^{-3}/device-day, respectively.

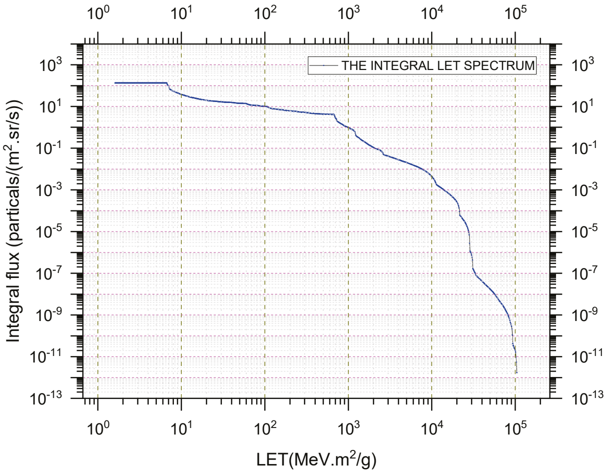


Figure 3. Integral flux spectrum of GCR after passing through 3 mm aluminum.

4. Conclusions

In this paper, we have employed foundational knowledge of probability theory, spatial analytic geometry, and vector algebra to establish a SER Rate prediction model. This approach differs slightly from the traditional mathematical foundations of SER prediction models and varies in the number and extent of simplified physical assumptions; some physical assumptions are even not considered at all.

When applying the MC method for numerical simulation prediction, the general model for SER Rate can represent a highly multi-dimensional integral, which is widely regarded as the most effective numerical simulation method in such cases. Furthermore, there is clear evidence that moderately increasing the descriptive details of energy deposition and charge collection can lead to accurate SER Rate predictions, even in complex compositions.

We validated our ideas through two application examples. Based on specific assumptions about the model, known processes, system application characteristics, and analysis of experimental data, we provided a comprehensive thought process, along with corresponding estimation results. This aims to help radiation effects engineers fully understand and apply the aforementioned model.

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Corner Simulation of CMOS Analog Integrated Circuit Taking into Account Radiation Influence

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Abstract

This paper proposes a corner analysis approach for CMOS circuits taking into the account radiation effects. The presented simulation approach is implemented using the open-source design automation (EDA) software QUCS-S 25.2.0 and Ngspice 45. It was developed a radiation-sensitive field-effect transistor (RADFET) SPICE macromodel representing threshold voltage shift versus radiation dose. The extraction procedure for this model is based on statistical measurements of pMOS transistors and process corner models (Slow, Typical, Fast) and involves percentile analysis. The article proposes an original design of the RADFET-based radiation sensor with RADFET device and CMOS readout circuit placed on the same die, which allows us to simplify the dosimeter schematic. The sensor output parameter dependency on process parameters, supply voltage, and temperature was investigated using the proposed simulation approach.

Keywords: electronic design automation (EDA); microelectronics; RADFET; radiation effects; parameter extraction; compact model; circuit simulation

1. Introduction

Taking into account the influence of manufacturing process variation and fluctuations in supply voltage and temperature is essential for analog integrated circuit design [1–3]. The classic approach to analyzing these influences is corner analysis or PVT analysis, derived from the words Process, Voltage, and Temperature [4]. Specialized mostly proprietary electronic design automation (EDA) tools such as Cadence Spectre [5] or SymSpice [6,7] are used to evaluate circuit sensitivity to these variations. A set of SPICE models taking account process parameter variation [8] must be provided for this analysis type as part of process design kit (PDK). The usage of open-source EDA tools and PDKs like IHP OpenPDK [9] or Google Skywater PDK is becoming a trend of the recent years. It has been shown that open solutions may serve as a replacement for proprietary software [10,11].

The design of radiation-hardened ICs [12] is an important task for areas such as radiation therapy medical equipment, aerospace and satellite equipment design. RADFET sensors readout circuits [13–15] are another case where the radiation effects must be taken into the account. Most of the present works on this subject are dedicated to digital circuit design [16–18] or consider the analog design of digital cells [19]. The design of radiation-hardened analog ICs is not fully covered in the available publications and presents an actual task. For radiation-hardened or radiation sensing analog circuits, ionizing radiation can also be considered as a corner parameter while performing PVT analysis. This is because radiation exposure alters the parameters of both active and passive circuit components, and these changes superimpose on the variations caused by PVT [4]. Circuit simulation software based on SPICE does not provide a unified way to introduce a radiation influence in the standard SPICE devices library. The common approach is to develop a semiconductor device model taking into account radiation effects. This task may be solved by Verilog-A compact model development [20–22] or using a more simple approach involving standard SPICE model modification [23,24]. All the models proposed in [20–22,24] are developed for a single "typical" or "nominal" device and do not incorporate the process variation of the technology. For instance, work [24] presents averaged characteristics, with results shown as single, smooth curves without indicating sample-to-sample variations. In works [20,21], the SPICE model parameters are extracted from measurements of specially fabricated test transistors with fixed dimensions, neglecting variations between different devices. A similar approach is demonstrated in [24]. The results show good agreement with experimental data. However, parameter variation between individual devices is not considered. Therefore, these models do not assess the potential spread in characteristics. Thus, existing radiation-aware SPICE models describe the average behavior of a device but provide no information on the process-induced spread of its characteristics.

Therefore, while these models are valuable for predicting nominal post-irradiation behavior, they are fundamentally incapable of predicting the statistical spread of circuit performance. This represents a significant gap in the design flow for radiation-hardened circuits, as it leaves designers blind to the yield impact of process variation under radiation.

The novelty of the presented work is the following:

1. It introduces a process corner analysis approach specifically for the RADFET device. This allows taking into account the manufacturing process variation and fluctuation influence, supply voltage and temperature variance.
2. It integrates this radiation-aware corner analysis into a holistic PVT simulation flow using the open-source tools QUCS-S and Ngspice, at a level comparable to commercial EDA tools.
3. It was proposed a radiation sensor design when the both RADFET sensor and readout circuit are placed on the same die. The benefit of the proposed design is that all transistors may be formed in the single chip as matched pairs and no external current source is required for sensor readout. This allows us to simplify the analog part of the dosimeter schematic.

The main purpose of this research is to investigate the feasibility of this approach and provide a practical workflow for evaluating the combined impact of process variation, voltage, temperature, and ionizing radiation on circuit performance.

The rest of the paper is organized as follows. Section 2 provides a detailed description of the used approach to represent the RADFET model and considers a procedure for corner parameter extraction of the MOSFET model for the technology node used. Section 3 considers corner simulation of the current mirror circuit used for readout of the RADFET sensor and gives a result comparison for proprietary and open-source circuit simulation tools. Finally, Section 4 gives an outcome of the paper and the summary of the achieved results.

2. RADFET Model Design

2.1. Simulation Software and Technology Node Used

QUCS-S is an open-source cross-platform circuit simulator [11,25,26] with a powerful EDA with intuitive GUI and support for modern simulation engines, namely Ngspice [27], Xyce [28] and QucsatorRF. The key feature of QUCS-S is an advanced performance for RF

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circuit design [10,29] and out-of-the-box tools for microelectronic schematic implementation and compact model debugging, including the Verilog-A synthesizer [22].

QUCS-S allows fast switching of the SPICE-compatible simulation backend, and the Ngspice simulation engine was selected for this research. Ngspice is an open-source simulator operating in command line (CLI) mode. It is actively integrated into modern open PDKs, such as IHP Open PDK [30] and Skywater 130A PDK [31]. Ngspice is used for simulating Hot Carrier Degradation, Single-Event Upset (SEU), Single-Event Effects (SEEs), and aging [31].

In this article, the corner models were developed using data from a Parametric Control Monitor (PCM) [32] fabricated on a single semiconductor wafer in full compliance with the CD4000 integrated circuit manufacturing technology, which is also used for the RADFET [33,34]. This technology corresponds to a long-channel CMOS process with minimum channel lengths of about 5 µm. The selection of the micron technology node is required by the compatibility of the readout circuit with the RADFET sensor technology. The submicron technology has a very limited application for RADFET sensor design because a relatively thick gate dielectric is required for sensor operation. IV curve measurements from 16 pMOS transistor samples with fixed dimensions of L = 5 µm and W = 100 µm were used. Based on this data, the parameters for a SPICE model Level 1 [35] were extracted for each transistor. These parameters are the following: threshold voltage `VTO` (V), transconductance `KP` (A/V^2), bulk threshold parameter `GAMMA` ($\sqrt{V}$), and channel length modulation `LAMBDA` (1/V). The parameter extraction method was similar to that described in [36,37].

The corner models were selected using the following procedure. A sorted series was constructed for each of the SPICE model parameters VTO, KP, and LAMBDA. And the distribution percentiles were calculated based on these series. The 10th and 90th percentiles were used for the "Slow" (PMOS_SS) and "Fast" (PMOS_FF) corner definitions, respectively. The typical model (PMOS_TT) was selected as the one whose parameters were closest to the median values of the distributions. This procedure corresponds to a multivariate statistical corner selection approach, where representative devices are chosen from the joint parameter distribution rather than constructed by independent parameter scaling, as commonly applied in statistical circuit analysis. Such multivariate selection preserves physically consistent parameter combinations and is widely used in statistical circuit analysis [2,32,38]. In this context, the term "worst-case" refers only to the most extreme parameter combinations among the extracted corner models and does not imply a statistically defined worst-case of the entire technological process and are not intended to represent statistically defined PDK corners or to be used for yield analysis.

The RADFET corner model was constructed using parameter deviations derived from pMOS transistors because the RADFET sensor structure is fully compatible with the basic technology node and differs only by device geometry. Therefore, no additional corner parameter measurement is required for the RADFET device. In micron technologies the influence of geometry on the parameter spread is significantly lower than in deep submicron technologies [39]. Therefore, the obtained variation coefficients can be used as an approximate estimate of the process spread for transistors of the same technology.

2.2. PMOS Corner Models

The parameters of the PMOS_SS corner are lower than those of the typical PMOS_TT corner by approximately 0.83% for the KP parameter and 9.02% for the Lambda parameter, and higher by 0.40% for the VTO parameter. Conversely, the parameters of the PMOS_FF corner are lower by 12.78% for the KP parameter and 0.01% for the VTO parameter, and higher by 4.25% for the Lambda parameter. These deviation values will be used further to construct the RADFET transistor macromodel.

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Figure 1 shows a comparison of the output I-V characteristics of the pMOS transistors for the different corner models.

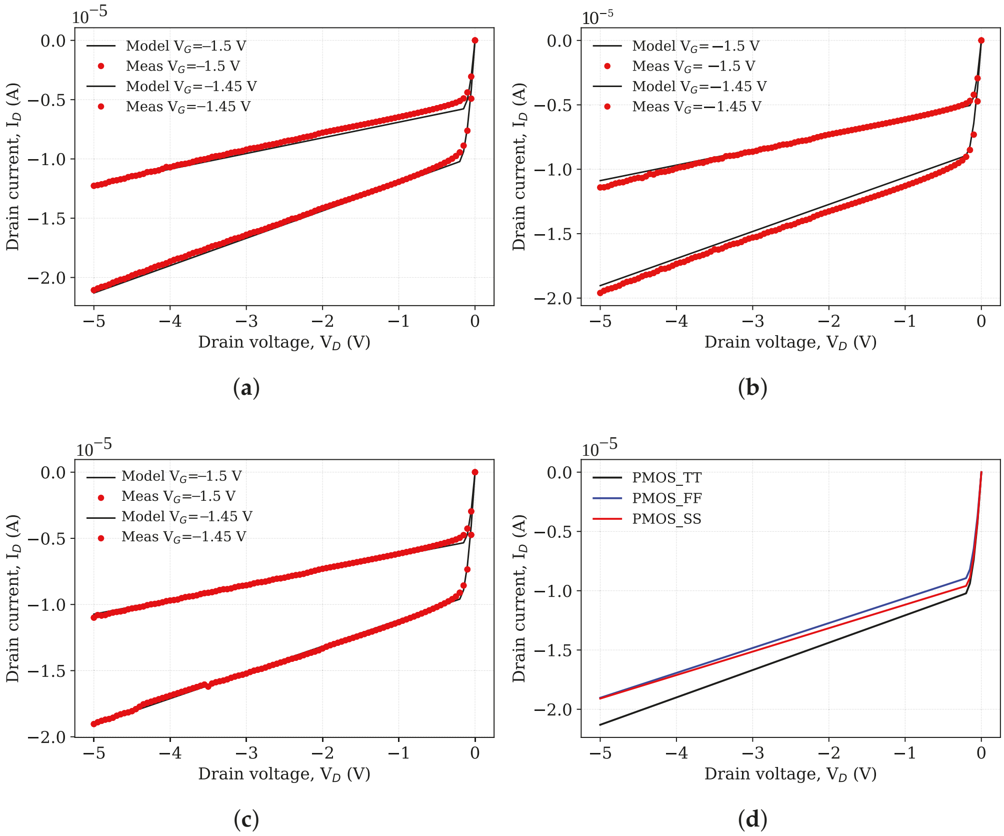

Figure 1. Output I-V characteristics of pMOS transistors for different process corners: (**a**) Typical corner (PMOS_TT). (**b**) Fast corner (PMOS_FF). (**c**) Slow corner (PMOS_SS). (**d**) PMOS corner comparison at V_G = −1.5 V.

The typical corner corresponds to a median representative point in parameter space and therefore is not required to exhibit electrical characteristics lying between PMOS_SS and PMOS_FF models.

The I-V curves of the PMOS transistors were measured using the Keysight B1500A semiconductor device analyzer at a nominal temperature of 27 °C. Figure 2 shows the photo of the measurement setup. It consists of a B1500A curve tracer itself and the wafer probe station connected to it and it allows us to measure the I-V curves of the samples on the wafer.

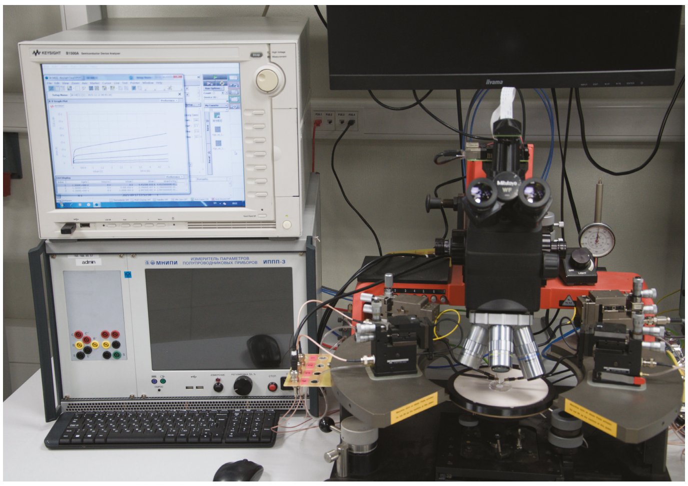

Figure 2. Semiconductor devices I-V curve measurement setup.

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2.3. RADFET SPICE Macromodel Design

The RADFET is a MOS transistor acting as an ionizing radiation dose sensor. The operation principle of the RADFET devices is based on the threshold voltage shift dependency on the accumulated radiation dose because of charge trapping in the gate dielectric [33]. Typically the PMOS transistors are serving as RADFETs.

The RADFET does not belong to the standard SPICE primitive device set and requires the design of a custom model. There exist several approaches to resolve this task. The research [22] proposes a compact model representing effects such as nonlinear dependency of threshold voltage shift on accumulated dose, saturation, fading, and device operation under gate bias up to the Fowler–Nordheim injection mode [40,41]. Another more simple approach is the modification of the existing SPICE MOSFET model by passing the threshold voltage shift on the accumulated dose as the model parameter. For example, the research [20] uses the EKV v2.6 model [37,42] as the basic model and adds empirical dependencies for the model parameters `VTO`, `GAMMA`, `KP`, and `E0` on the accumulated dose. This approach will work for every SPICE model representing the RADFET for the basic technology node. In the present article, we have used a Level 1 SPICE model as the basic RADFET sensor model and added the dependency of threshold voltage of the accumulated dose, because the full simulation of the RADFET sensors, including the effects mentioned above, was not required. A similar approach was presented by a group of researchers from Nis University in their article [24].

The macromodel was constructed using measurement data on the threshold voltage shift of a p-channel MOSFET with $W/L = 700$ µm/6 µm versus the radiation dose taken from [22,33]. The initial threshold voltage was -1.2 V. A threshold voltage dependency on the accumulated dose was approximated by linear function as proposed by [24]. This approximation could be described by the following equation:

$$\Delta V_{th} = V_{th0} + D \cdot S \tag{1}$$

where V_{th0} is the initial threshold voltage, D represents the accumulated dose expressed in rads, S is the sensor's sensitivity to radiation expressed in V/rad.

The parameter value $S = 6.16 \times 10^{-5}$ V/rad was determined using the least squares method, resulting in an root mean square error (RMSE) value of 2.63×10^{-11}.

Figure 3 shows the log-log plot of the threshold voltage shift versus the accumulated dose. The experimental data are represented by markers, while the approximating curve is shown as a solid line. The selected RADFET sensor operates in the region where this dependency may be considered as linear.

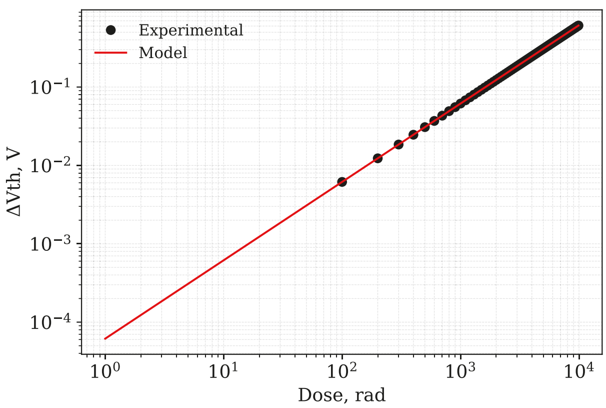

Figure 3. Threshold voltage shift versus accumulated dose for the RADFET.

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3. Corner Simulation Taking into Account Radiation Effect

3.1. Current Mirror Circuit for Biasing RADFET

There exist different approaches to design the readout circuit for the RADFET sensor. Usually the RADFET sensor should be connected to current source IC (for example LM334) after the exposure to measure the threshold voltage shift. The dosimeter design presented in [43] uses this circuit. We propose another approach for readout circuit design based on using a current mirror. The usage of the current mirror has an advantage that it uses the same technology node for the RADFET and the readout circuit. This makes it possible to design a chip set containing the RADFET and its readout circuit.

The current mirror schematic which is used for our research is shown in Figure 4. It consists of two PMOS stacks: M1, M4, M6 from the reference branch and M2, M5, M7 from the output branch. The polysilicon resistor R1 defining the current is connected to one branch of the mirror. The RADFET sensor M3 is connected to another branch. The threshold voltage of the RADFET sensor is measured at the mirror output (node labeled D–drain). The `.PARAM` block defines the parameter variable *D* representing the accumulated dose. This variable is passed to M3 instance parameters.

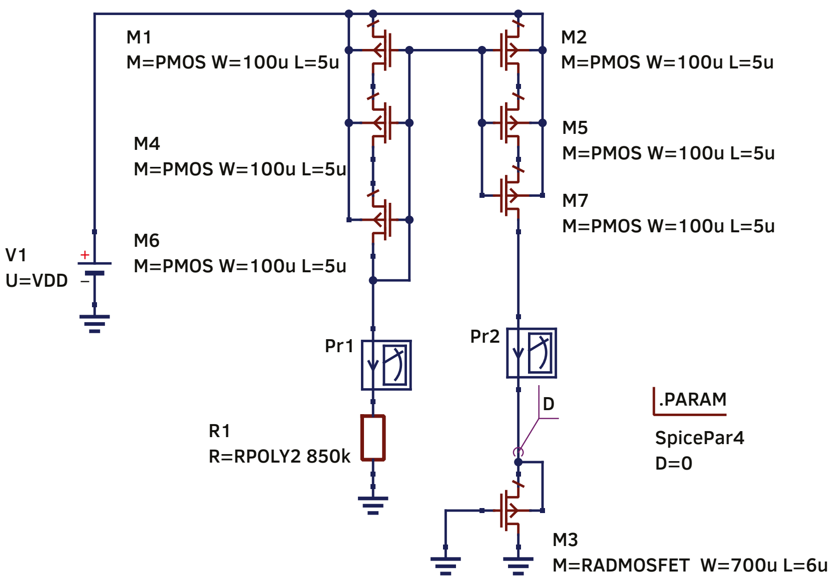

Figure 4. Current mirror with the RADFET transistor in QUCS-S.

To improve current matching and reduce the impact of channel-length–dependent threshold voltage variation, each PMOS transistor in the current mirror is implemented as a series connection of identical shorter transistors with their gates tied together, following the approach described in [3].

The simulation of the RADFET transistor's threshold voltage shift under ionizing radiation was implemented using the nested loop parameter sweep of the *D* variable and supply voltage DC sweep. The accumulated dose *D* is swept in a range from 0 to 10 krad. The supply voltage is swept in a range from 9 to 11 V which corresponds to a 10% supply variation.

The SPICE model library contains three sets of polysilicon resistor models (minR, maxR, typ) and three sets of PMOS transistor models (PMOS_TT, PMOS_SS, PMOS_FF). The polysilicon resistor models were obtained using measurements from 32 samples. The process variation for the RADFET was implemented using multipliers k1, v1, and l1, which were derived from the current mirror pMOS transistors. The content of the library is shown in the Listings 1 and 2.

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Listing 1. SPICE model library for polysilicon resistors.

```
* Typical corner
.LIB res_typ
.MODEL RPOLY2 R(RSH=1400, TC1=-0.0014, TC2=3.6E-6 TNOM=27)
.ENDL
* min RSH corner
.LIB minR
.MODEL RPOLY2 R(RSH=1200, TC1=-0.0014, TC2=3.6E-6 TNOM=27)
.ENDL
* max RSH corner
.LIB maxR
.MODEL RPOLY2 R(RSH=1600, TC1=-0.0014, TC2=3.6E-6 TNOM=27)
.ENDL
```

Listing 2. SPICE model library for pMOS transistors and RADFET.

```
* pMOSFET library
.LIB PMOS_TT
.param k1=1 v1=1 l1=1
.param S=6.16e-05 VT=1.2
.MODEL PMOS PMOS (Level=1 VTO=-1.2925 KP=2.302e-05 LAMBDA=0.2364 GAMMA=0.290
+ TNOM=27)
.MODEL RADMOSFET PMOS (Vt0=-(VT*v1+D*S) Kp=(5m*k1) Gamma=3.97u
+ Phi=0.6 Lambda=(1.87m*l1) Tox=100n TNOM=27)
.ENDL

.LIB PMOS_SS
.param k1=0.9917283727656981
.param v1=1.0040197249360854
.param l1=0.90984315841993
.param S=6.16e-05 VT=1.2
.MODEL PMOS PMOS (Level=1 VTO=-1.2977 KP=2.283e-05 LAMBDA=0.2151 GAMMA=0.290
+ TNOM=27)
.MODEL RADMOSFET PMOS (Vt0=-(VT*v1+D*S) Kp=(5m*k1) Gamma=3.97u
+ Phi=0.6 Lambda=(1.87m*l1) Tox=100n TNOM=27)
.ENDL

.LIB PMOS_FF
.param k1=0.8721575100916387
.param v1=0.9999170424701207
.param l1=1.0425197000956137
.param S=6.16e-05
.param VT=1.2
.MODEL PMOS PMOS (Level=1 VTO=-1.2924 KP=2.007e-05 LAMBDA=0.2465 GAMMA=0.290
+ TNOM=27)
.MODEL RADMOSFET PMOS (Vt0=-(VT*v1+D*S) Kp=(5m*k1) Gamma=3.97u
+ Phi=0.6 Lambda=(1.87m*l1) Tox=100n TNOM=27)
.ENDL
```

The following procedure was used to evaluate the impact of process variation, temperature, and supply voltage fluctuations on the performance of the circuit under investigation.

The analysis was conducted at the following extreme corner combinations:

- Temperature: −60 °C and 125 °C;
- Supply voltage: 9 V and 11 V;
- Resistor models: minR and maxR;
- Transistor models: PMOS_FF and PMOS_SS.

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For each combination, radiation exposure simulation was performed with a dose ranging from 0 to 10 krad. The results were compared with the typical corner set (27 °C, 10 V, PMOS_TT, res_typ).

3.2. Simulation Results

The performed simulations show the impact of various corners on the output voltage stability of the investigated circuit under radiation. The most significant parameter is temperature with a maximum deviation of 10.59% at 125 °C.

Process variations and supply voltage fluctuations demonstrated a smaller impact: no more than 0.03% for supply voltage fluctuations within a range of ±0.5 V and 0.4% for process variations.

Table 1 provides a summary of the output voltage deviations obtained from the corner analysis.

Table 1. Summary of corner analysis.

Parameter	Max. Deviation, %	Mean Deviation, %	Worst Case
Corner model	0.44	0.14	PMOS_SS/minR
Temperature	10.59	7.67	125 °C
Voltage supply	0.03	0.02	9V

The relative deviations of the output voltage from the nominal corner depending on radiation dose for different corners are shown in Figure 5.

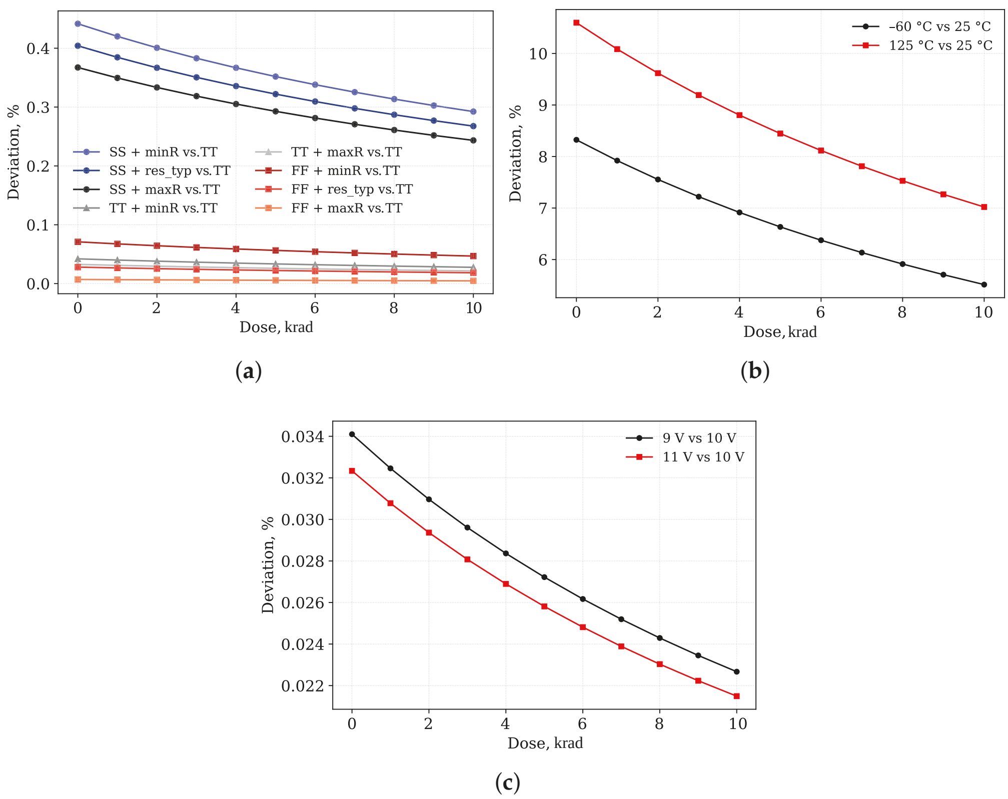

Figure 5. Relative deviation of output voltage from nominal corner versus absorbed radiation dose for different conditions: (**a**) process corners (relative to TT), (**b**) temperature (relative to 25 °C), (**c**) supply voltage (relative to 10.0 V).

To evaluate the impact of the corner parameters on the RADFET, a circuit with an ideal current source was simulated. The ideal current source eliminates dependence on supply voltage and any variations associated with the formation of the reference current. The simulated circuit is shown in Figure 6.

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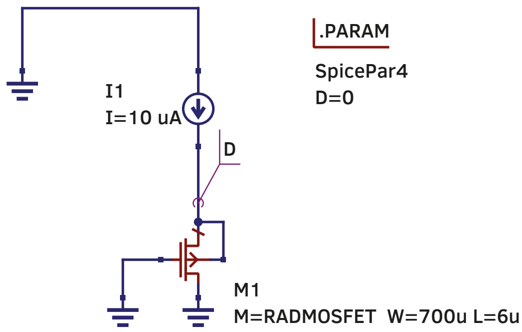

Figure 6. Simplified circuit using an ideal current source to bias the RADFET.

For comparison of the simulation results, Figure 7 shows the simulation results of the RADFET at the worst temperature corner (125 °C) under two conditions: with an ideal current source and with a current mirror.

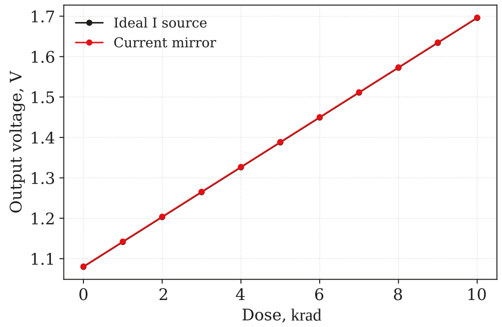

Figure 7. Comparison of RADFET simulation results with an ideal current source biasing and a current mirror biasing at the worst-case temperature corner.

As shown in Figure 7, the differences between the two circuit designs are minor. The maximum deviation is 0.09% indicating that the biasing method has negligible influence.

The observed temperature sensitivity can be explained by the physical properties of MOS transistors. Even when the RADFET is biased by an ideal current source (Figure 6), temperature remains the dominant factor affecting output voltage stability. Specifically, temperature has an effect on two key parameters: carrier mobility (μ) decreases, while threshold voltage ($|V_{th}|$) also decreases with temperature. Although $|V_{th}|$ reduction slightly increases drain current, this effect is dominated by the dominant mobility degradation. SPICE simulations confirm that the mobility degradation dominates this competition, resulting in an overall decrease in output voltage with temperature.

The operating point was simulated and internal parameters were obtained for a RADFET using the circuit diagram shown in the Figure 6.

However, NGSPICE does not directly calculate parameters such as carrier mobility (μ) and threshold voltage ($|V_{th}|$). Therefore, two related quantities were extracted instead: the V_{on} parameter (turn-on voltage) and the normalized transconductance. SPICE simulators assume $V_{on} \approx V_{th}$ for the most of practical cases. The normalized transconductance is defined as

$$g_{m_{norm}} = \frac{g_m}{(W/L)} \tag{2}$$

where g_m is the small-signal transconductance and (W/L) is the transistor's aspect ratio.

For long-channel devices operating in strong inversion, g_m can be approximated as

$$g_{m_{norm}} \approx \mu \cdot C_{ox} \cdot (V_{gs} - V_{th}) \tag{3}$$

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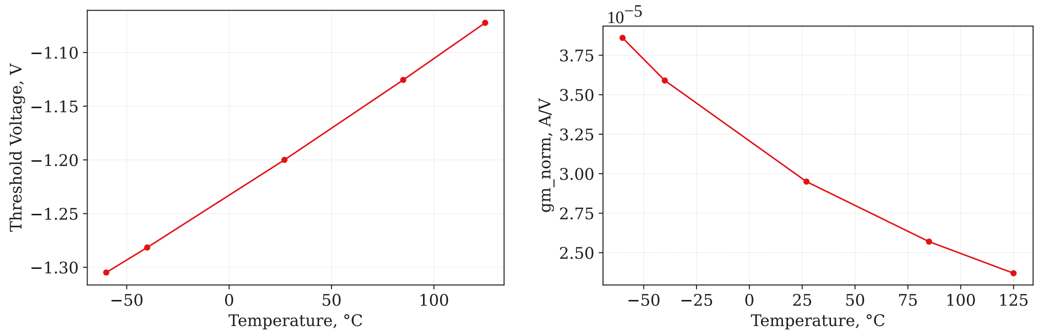
From this relation, it follows that $g_{m_{norm}}$ is directly proportional to carrier mobility and is ideal for demonstrating temperature dependence.

The simulation results shown in Figure 8, illustrate the dependence of the threshold voltage and normalized transconductance on temperature.



(**a**) (**b**)

Figure 8. Results of the operating point analysis: (**a**) Threshold voltage vs. temperature. (**b**) Normalized transconductance vs. temperature.

The effect of temperature in the SPICE Level 1 models used is taken into account using built-in analytical temperature relationships [39]. Only the nominal reference temperature (TNOM) is specified in the parameters, while the operating temperature is set globally, and the simulator automatically recalculates the transistor parameters according to the model's internal temperature dependencies.

3.3. Deterministic Estimation of Current Mirror Mismatch

In addition to the process variations in corner models, local transistor mismatch is a significant source of uncertainty for current mirrors. Mismatch refers to the local spread of parameters between nominally identical transistors and arises from random microscopic fluctuations in the process [44]. For current mirrors, mismatch results in differences in the electrical characteristics of transistors, which causes the output current to deviate from the nominal value even with identical device parameters.

The model described in [44] requires knowledge of the process mismatch coefficients A_{VT} and A_{β}, which, as shown, are strictly process-dependent quantities and must be extracted experimentally. This model is a generally accepted empirical description of local mismatch in MOS transistors and is widely used as an analytical basis for specifying random parameter variations in Monte Carlo simulations of analog integrated circuits [2,45]. Furthermore, the relative current spread in current mirrors is determined not only by the mismatch coefficients but also by the transistor's operating mode: according to the results of [44], the contribution of the mismatch threshold voltage to the relative current spread decreases with increasing overdrive voltage V_{ov}.

In this article, a deterministic worst-case mismatch estimate is used to evaluate the impact of mismatch on a current mirror circuit. The simulation uses the inclusion shown in Figure 7, where the current deviation is accounted for through the equivalent change in the ideal source current. Conservative upper bounds for the mismatch coefficients from [44] were used in the calculations. These estimates provide experimental data for a wide range of CMOS technologies, including technologies with an oxide thickness of 100 nm, which corresponds to the used CD4000-compatible technology.

The effect of mismatch on current is considered for two boundary values:

$$I = I_{nom}(1 \pm 3\sigma_I / I) \quad (4)$$

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where I_{nom} is the nominal value of current and σ_I / I is the standard deviation of current due to mismatch.

This approach provides a rapid estimate of the circuit sensitivity to mismatch at the initial stage of analysis and is widely used during early design phases when statistically characterized process models are unavailable. It does not replace full Monte Carlo simulation with characterized SPICE models containing mismatch parameters.

The relative current variation σ_I / I was estimated using the classical Pelgrom mismatch model (5) from [44].

$$\sigma_I / I = \frac{1}{\sqrt{WL}} \sqrt{\frac{4A_{VT}^2}{V_{ov}^2} + A_\beta^2} \tag{5}$$

For this purpose, the minimum possible overdrive voltage within the operating PVT conditions of the circuit was considered. This condition corresponds to the PMOS_TT corner combined with minimum load resistance, a supply voltage of 9 V, and a temperature of −125 °C.

The obtained value of σ_I / I = 0.06. The dominant contribution is exerted by $\sigma_V t$ = 2.5 mV.

It should also be noted that radiation exposure can further enhance the mismatch of transistor parameters. As shown in [46], the total ionizing dose leads to an increase in the parameter spread due to the combined effect of technological variations and differences in the electrical modes of the transistors during irradiation. Thus, mismatch in a radiation environment is a function not only of the technological spread but also of the cumulative dose. In this study, the radiation-induced contribution to mismatch is not separately modeled and is not considered as an area for further research. In this study, for each considered radiation dose, a separate calculation of the standard deviation of the parameters was performed, which made it possible to take into account the dependence of mismatch on the cumulative dose. The Figure 9 shows shows the dependence of the output voltage on accumulated radiation dose for the upper and lower bounds of the mismatch variation.

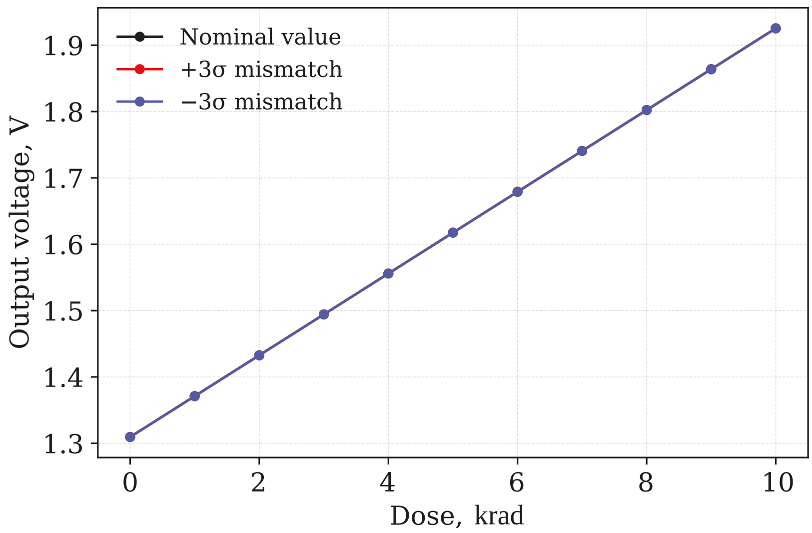

Figure 9. Output voltage dependency on accumulated dose for nominal and $\pm 3\sigma$ mismatch conditions.

The maximum relative output voltage deviation due to transistor parameter mismatch was determined as the largest ratio of the difference between the $\pm 3\sigma$ levels and the nominal value to the nominal level over the entire range of doses studied. It was found that the relative mismatch does not exceed 8.4×10^{-5} V.

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3.4. Simulation of RADFET Sensor and Readout Circuit Placed on the Same Die

In Section 3.1 we have considered a case when the RADFET sensor and readout circuit were formed separately and connected only at the readout phase. We propose an approach when the readout circuit and sensor are placed in the same chip. The usage of current mirror as the readout circuit makes this design possible. The schematic representing the proposed solution is presented in the Figure 10. The key differences from the schematic shown in the Figure 4 is that all three MOSFETs are exposed to radiation. The PMOS transistors M1 and M2 serves as a current source, and PMOS transistor M3 serves as the radiation sensor. The polysilicon resistor R1 is also exposed to radiation, but the degradation of its parameters may be neglected. It was shown in the research in [47,48] that the degradation of polysilicon films starts from doses higher than 10^6 rads. This value is out of the typical RADFET sensor operating range.

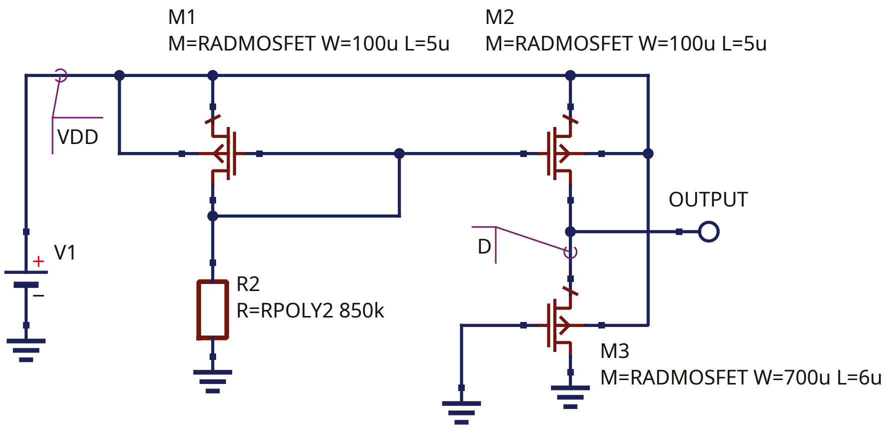

Figure 10. RADFET sensor combined with readout circuits; all transistors are exposed to radiation.

The sensor output is the drain of M3 transistor (node label D). The voltage at this node has a linear dependency on the accumulated dose. Figure 11 shows the simulated dependency of the sensing circuit output voltage (node D) on the accumulated radiation node. This dependency is compared to the dependency obtained for the ideal current source readout circuit and non-irradiated current mirror. The comparison shows no visible difference if all four transistors placed on the same die and irradiated at the same time. The observed difference lies within 1% tolerance.

The drain current of M3 MOSFET (output current) has a weak dependency on the radiation dose (Figure 12), because the threshold voltage shift of the M1 and M2 transistors (current mirror) is compensated. It could be seen that the M3 drain current changes within 10% for the dose changed within the sensing circuit operating range. This current may be set near the ZTC point of the M3 transistor. The simulation shows that the difference of the measured threshold voltage shift using ideal current source and proposed sensor schematic is within 0.1% over the operating range from 0 to 10 krad.

Summarizing all the above, we can conclude that the proposed circuitry allows us to form the RADFET sensor and readout current source in a single chip. This monolithic IC will not require an external current source for readout and its output could be connected directly to the ADC input of a digital dosimeter.

The proposed RADFET sensor and readout circuit were simulated under the same PVT corner combinations as described earlier. Table 2 summarizes the difference between the two implementations of the readout circuit.

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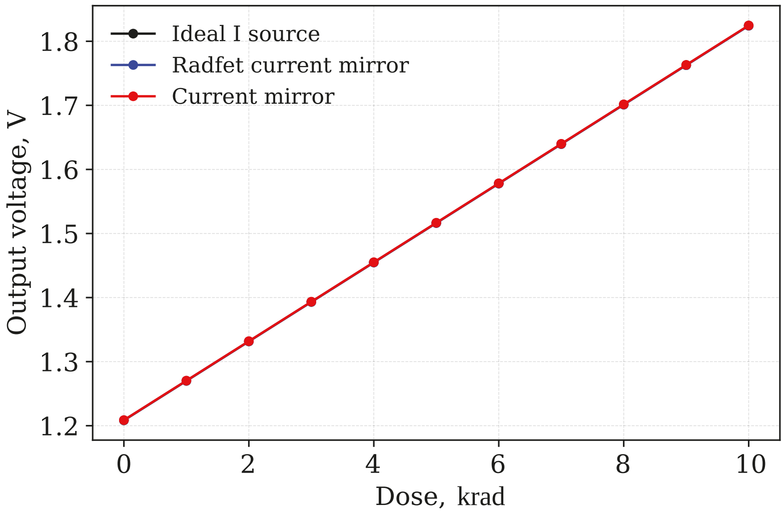

Figure 11. RADFET The dependency of sensor output voltage in absorbed dose

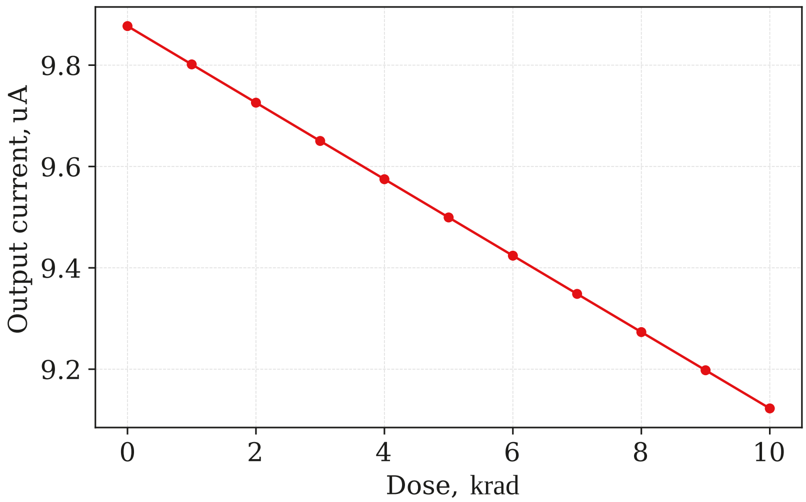

Figure 12. M3 MOSFET drain current dependency on accumulated dose.

Table 2. Difference between simulation results of the two current mirror implementations.

Parameter	Max. Deviation, %	Mean Deviation, %	Std. Deviation, %
Corner model	−0.0035	−0.0021	−0.0002
Temperature	0.0144	0.01321	−0.0026
Voltage supply	−0.0028	−0.0023	−0.0006

The simulation results demonstrate that the circuit in which only the RADFET sensor is exposed to radiation and the circuit in which all transistors are exposed exhibit almost identical sensitivity to PVT variations. Temperature variation remains the dominant corner (approximately 10%), whereas the influence of process and supply voltage variations stays below 0.4% and 0.04%, respectively. These results support the feasibility of integrating both the RADFET sensor and its readout circuit on the same die. Also it should be noted that the RADFET used inside the readout circuit had geometry different from the device used during SPICE model extraction. However, for the used micron-scale technology, this approximation does not introduce significant inaccuracy.

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3.5. Simulation Result Comparison with Proprietary EDA Tools

To validate the accuracy of the performed simulations using open-source EDA, a comparative analysis was conducted with the commercial EDA SymicaDE v5.5. This software package uses Spectre-compatible netlist syntax and a primitive devices library and could be used for analog IC design for micron and submicron technology nodes from the DC to RF domains [7]. The same circuit netlist and corner models were used in both simulation environments. However, a minor modification was required for the threshold voltage parameter due to differences in SPICE model implementation between the simulators. In the netlist for SymicaDE, the initial threshold voltage was defined as `.param VT = -1.2`. Figures 13 and 14 show screenshots of the simulation session in SymicaDE, confirming the equivalent setup and parameter configuration.

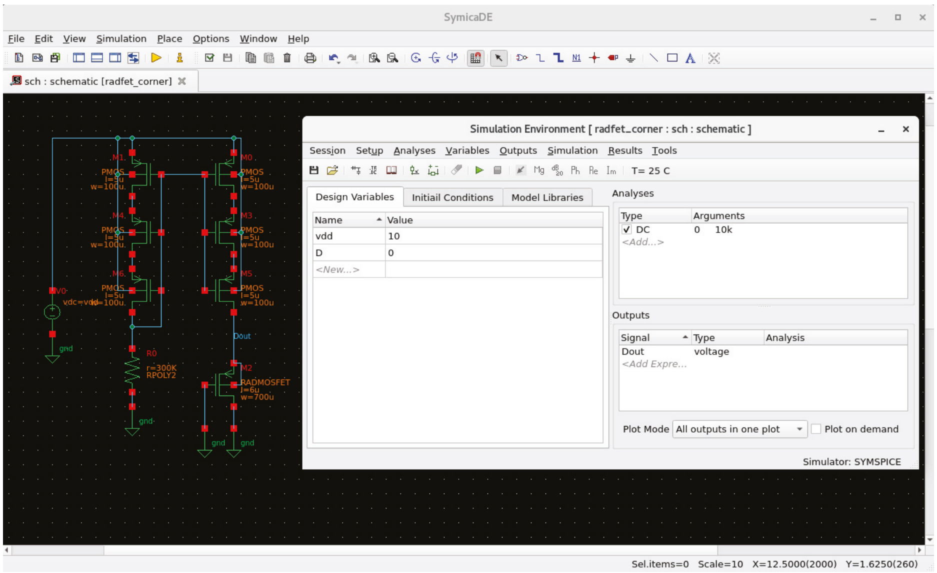

Figure 13. Screenshot of configuration in the SymicaDE environment.

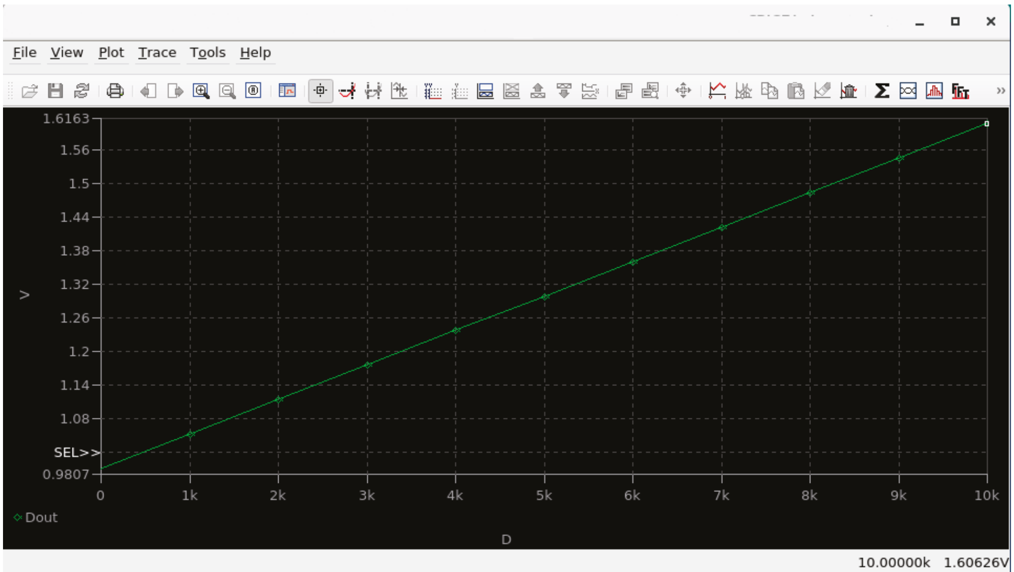

Figure 14. Screenshot of simulation results in the SymicaDE environment.

Figure 15 shows the simulation results of the RADFET at the worst corners.

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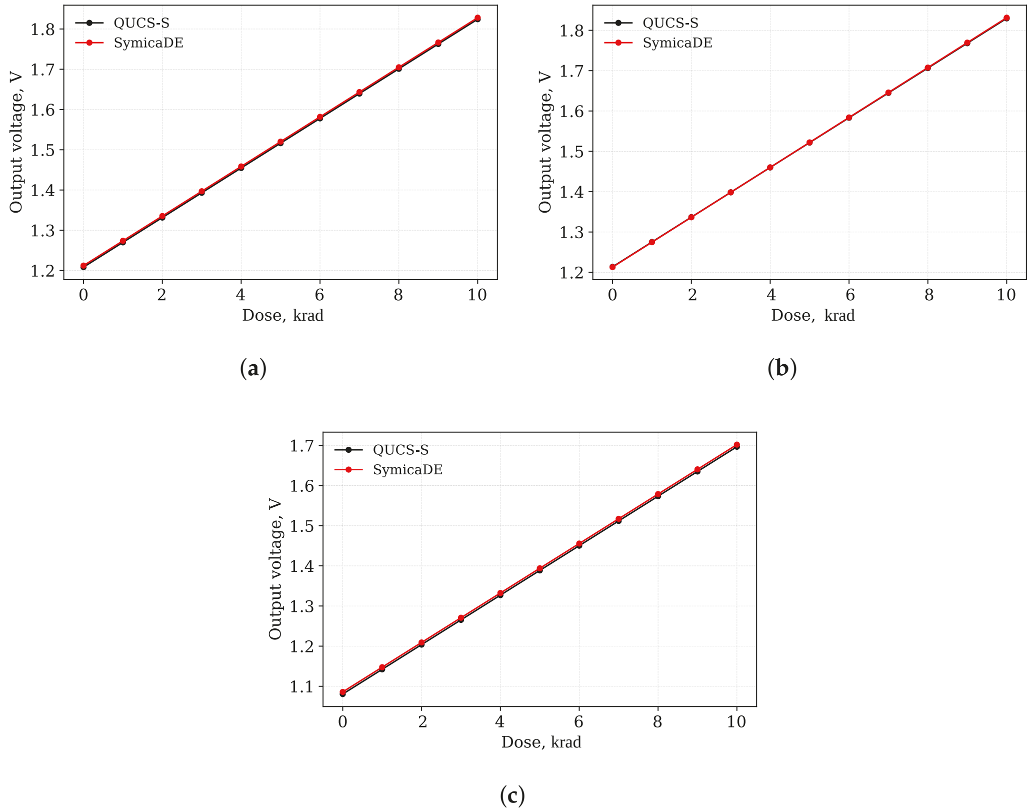

Figure 15. Comparison of simulation results between QUCS-S/Ngspice and SymicaDE: (**a**) Output voltage vs. radiation dose for the voltage worst corner (9 V). (**b**) Output voltage vs. radiation dose for the process worst corner (PMOS_SS/minR). (**c**) Output voltage vs. radiation dose for the temperature worst corner (125 °C) .

The maximum observed deviation in the output voltage between the two tools was less than 1% across all worst-case corners with the maximum deviation for temperature being 0.49%.

4. Conclusions

This article proposes a complete corner analysis approach for a radiation-hardened analog circuit, implemented entirely with open-source EDA. The results show good agreement with simulations performed in commercial EDA SymicaDE. Simulation results confirm the effectiveness of the QUCS-S/ngspice combination for comprehensive corner analysis, including radiation effects. The percentile-based extraction and scaling of SPICE model parameters (VTO, KP, LAMBDA) represents a practical workflow for integrating radiation-aware corners into existing open-source circuit simulators.

Our analysis reveals that the dominant corner affecting circuit is temperature. The influence of process variation and supply voltage was significantly lower. This result underscores the critical role of a holistic approach that concurrently considers temperature, radiation, and process corners.

The original radiation sensor circuitry has been proposed and simulated using the presented approach. The key feature of the proposed sensor design is that the both the RADFET sensor and current mirror readout circuit are placed on the same die. This solution allows us to simplify the dosimeter circuit.

The SPICE level 1 MOSFET model (Shichman–Hodges) provides a simple extraction procedure and good representation of MOSFET device behavior for micron technology nodes. However, several limitations related to the usage of the level 1 model should be noted. The temperature dependencies in this model are defined in a completely analytical manner, without additional SPICE parameters such as TCV, BEX, KT1 for the EKV model if we used it as the core model. These simplifications are acceptable for the technology node used in the paper but would require refinement for predictive use and extension to other types of RADFET devices in production-grade design. For more complex models like EKV-RAD or BSIMSOI RAD, radiation impact statistics collection for multiple RADFET devices, special current source design development, and taking into account the influence of radiation may be required to improve the simulation accuracy.

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Conflicts of Interest: Author Sergei Ryzhov was employed by the company JSC "Experimental Design Bureau of Microelectronics (OKB MEL)". The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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Article

Photoconductive Gain Behavior of Ni/β-Ga_2O_3 Schottky Barrier Diode-Based UV Detectors

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Abstract

A vertical Ni/β-Ga_2O_3 Schottky barrier diode was fabricated on an unintentionally doped bulk (−201)-oriented β-Ga_2O_3 single crystal and investigated with a focus on the underlying photoresponse mechanisms. The device exhibits well-defined rectifying behavior, characterized by a Schottky barrier height of 1.63 eV, an ideality factor of 1.39, and a high rectification ratio of ~9.7×10^6 arb. un. at an applied bias of ±2 V. The structures demonstrate pronounced sensitivity to deep-ultraviolet radiation (λ ≤ 280 nm), with maximum responsivity observed at 255 nm, consistent with the wide bandgap of β-Ga_2O_3. Under 254 nm illumination at a power density of 620 μW/cm^2, the device operates in a self-powered mode, generating an open-circuit voltage of 50 mV and a short-circuit current of 47 pA, confirming efficient separation of photogenerated carriers by the built-in electric field of the Schottky junction. The responsivity and detectivity of the structures increase from 0.18 to 3.87 A/W and from 9.8×10^8 to 4.3×10^{11} $Hz^{0.5}cmW^{-1}$, respectively, as the reverse bias rises from 0 to −45 V. The detectors exhibit high-speed performance, with rise and decay times not exceeding 29 ms and 59 ms, respectively, at an applied voltage of 10 V. The studied structures demonstrate internal gain, with the external quantum efficiency reaching 1.8×10^3%.

Keywords: gallium oxide; ultraviolet photodiode; self-powered mode; internal gain

1. Introduction

Monoclinic β-Ga_2O_3 (gallium oxide) has recently attracted significant attention as a promising ultra-wide bandgap semiconductor because of its large bandgap E_g = 4.5–4.9 eV, high breakdown electric field E_{br} = 8 MV/cm, and outstanding Baliga's figure of merit ≈ 3444, which surpass those of SiC (340) and GaN (870) [1–5]. β-Ga_2O_3 substrates can be grown by melt-based bulk growth techniques [6,7], resulting in crystals with low dislocation densities (~10^3 cm^{-2}), high structural quality, and commercial wafer diameters reaching up to ~4–6 inches [1,2,8–10]. These technological advantages, combined with its intrinsic electronic properties, position β-Ga_2O_3 as a leading material for next-generation power electronic devices, such as Schottky barrier diodes (SBDs), which are key components in energy conversion systems for electric vehicles, air-conditioning, and power distribution [11–14].

In addition to power electronics, β-Ga_2O_3 has emerged as a highly promising material for solar-blind ultraviolet (UV) photodetectors operating in the 200–280 nm wavelength range without the need for optical filters [15–20]. The large bandgap ensures intrinsic solar blindness, while its capability for forming high-quality metal–semiconductor interfaces enable the realization of SBD-based photodetectors with low dark current, high responsivity, low power consumption, and self-powered operation [21,22].

Beyond conventional photodetection, β-Ga_2O_3 devices also hold potential for functional optoelectronic applications, such as photonic switches and light-controlled electronic components [23]. The ability of β-Ga_2O_3 Schottky diodes to combine rectifying behavior typical of power devices with strong photosensitivity under UV illumination makes them suitable candidates for use as photo-controlled switches (photokeys) [24]. Such devices can operate in both forward and reverse bias modes, enabling a tunable balance between sensitivity and signal-to-noise ratio, which is particularly attractive for integrated optoelectronic circuits and intelligent power systems [25].

In the classical description of Schottky barrier diodes, photoelectric gain mechanisms are not explicitly considered. However, numerous recent studies have reported exceptionally high photoelectric characteristics, where the external quantum efficiency exceeds 100%, indicating the presence of internal gain effects [26,27]. The dominant gain mechanism proposed in these works is typically associated with a reduction in the effective Schottky barrier height, caused by the accumulation of photogenerated holes in trap states near the metal/β-Ga_2O_3 interface [28]. This charge trapping leads to barrier modulation and enhanced electron injection, resulting in amplified total current. Most studies on Ga_2O_3-based photodetectors have focused on device characterization within a limited bias voltage range, often without considering the electric-field dependence of the response and recovery times [29,30]. As a result, the correlation between bias-dependent photoresponse dynamics and internal gain mechanisms remains insufficiently understood. A systematic analysis of these dependencies is essential for developing a more comprehensive understanding of the physical processes governing ultraviolet photoresponse formation in Ga_2O_3-based structures.

In this work, the electrical and photoelectric characteristics of Ni/(−201)β-Ga_2O_3 Schottky barrier diodes are systematically investigated. It is demonstrated that the fabricated structures exhibit a pronounced photoelectric gain, with the external quantum efficiency exceeding 10^3%. The phenomenon of photo-gain in SBDs is analyzed over a wide bias voltage range, and the dominant internal gain mechanism responsible for the enhanced photoresponse is identified. The electric-field dependence of the photoconductivity rise and decay times is investigated.

2. Materials and Methods

Unintentionally doped β-Ga_2O_3 commercial wafers (Tamura Corp., Tokyo, Japan) with a (−201) surface orientation, a thickness of 650 μm, and a donor concentration of ~10^{17} cm^{-3} were used as substrates for the fabrication of vertical Schottky barrier diodes (SBDs). Prior to the formation of the ohmic contact, the substrate surface was etched in hot hydrochloric acid (HCl 30%) and subsequently rinsed in deionized water. Immediately before metal deposition, the surface was cleaned using oxygen plasma.

The ohmic contact was formed by electron-beam evaporation of Ti (80 nm) followed by a protective Ni layer (30 nm), and a subsequent annealing process was performed in nitrogen at 300 °C for 30 min. Schottky barrier contacts were patterned using photolithography, and an 80 nm Ni layer was deposited to form the rectifying electrodes. The use of Ni enables a reduction in on-resistance compared to metals such as Pt, Pd, and Ir, which provide higher barrier heights [31,32]. Additionally, Ni is a more cost-effective metal and can be readily deposited via electron-beam evaporation or magnetron sputtering [31–33]. The diameter of the Schottky barrier contact is 0.5 mm. In the final step, the substrate was

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divided into individual 2 mm × 2 mm chips using disk sawing. A schematic of the device structure is shown in Figure 1.

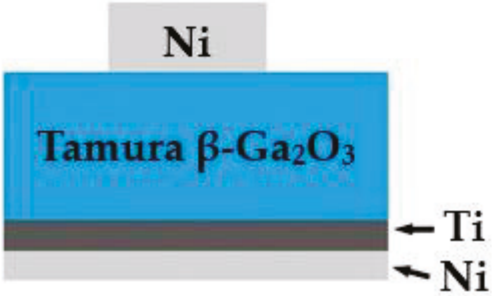

Figure 1. A schematic view of SBD-based on Ni/β-Ga_2O_3.

Optical transmission spectra were obtained using a deuterium lamp D-2000, Micropack (Orlando, FL, USA) in the wavelength range of 250–450 nm. The transmitted radiation was collected by an Ocean Optics Flame spectrometer (200–850 nm operating range) with a spectral resolution of 1 nm. Time-resolved photocurrent measurements were performed using a LeCroy 104XS digital oscilloscope (Chestnut Ridge, NY, USA) with 1 GHz bandwidth and a UV LED with a maximum intensity at λ = 255 nm.

Current–voltage (*I*–*V*/*J*–*V*) and capacitance–voltage (*C*–*V*) characteristics were measured using a Keithley 2636A source (Cleveland, OH, USA) meter and an Agilent E4980A RLC meter (Santa Rosa, CA, USA), respectively. *C*–*V* measurements were performed at 1 kHz with an AC signal of 100 mA. The electrical and photoelectric characteristics of the structures were measured under room temperature and ambient-humidity conditions.

A krypton-fluorine lamp VL-6.C (Marne-la-Vallée, France) was used as the source of irradiation at wavelength λ = 254 nm and the light power density P = 620 μW/cm^2. Measurements of the electroconductive characteristics of the SBD were carried out at dark conditions in a sealed Nextron MPS-CHH chamber (Busan, Korea) equipped with microprobes.

Dependencies of the photo-to-dark current ratio (PDCR), responsivity R, detectivity D, and external quantum efficiency (EQE) of samples on λ and U were computed by means of following formulas, respectively [34]:

$$PDCR = \frac{I_L}{I_D}, \tag{1}$$

$$R = \frac{I_{ph}}{S \times P}, \tag{2}$$

$$D = R\sqrt{\frac{S}{2eI_D}}, \tag{3}$$

$$EQE = R\frac{hc}{e\lambda} \times 100\%, \tag{4}$$

where I_L—total current under UV irradiation, I_{ph} is the photocurrent, $I_{ph} = I_L - I_D$; h is the Planck constant, c is the speed of light in vacuum; e is the electron charge, and S—diode surface area, P—optical power density of the irradiation, and λ—wavelength of the irradiation.

The rise t_r and the fall t_d times were determined as the time interval between the 0.9 and 0.1 levels of the maximum I_L.

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3. Results

The optical transmission spectrum of the Ga_2O_3 film in the 250–450 nm range shows a strong wavelength dependence typical of a wide-bandgap semiconductor. The transmittance remains very low below approximately 280 nm, indicating strong optical absorption in the deep-UV region where photon energies exceed the bandgap of Ga_2O_3. As the wavelength increases beyond 280 nm, the transmission gradually rises, reaching about 80% near 350 nm. The sharp absorption edge observed near 270–280 nm corresponds to the fundamental bandgap absorption of β-Ga_2O_3, confirming its suitability for solar-blind ultraviolet photodetection. Based on the measured transmission spectrum, the spectral dependence of the absorption coefficient α was obtained using the following expression [35]:

$$\alpha(\lambda) = -\frac{1}{d}\ln\left(\frac{\sqrt{(1-R)^4 - 4T^2R^2} - (1-R)^2}{2TR^2}\right), \quad (5)$$

where d is the thickness of the gallium oxide substrate (650 μm), T is the transmittance, and R is the reflectance. A plot of the squared absorption coefficient (α^2) versus photon energy ($h\nu$) was then plotted to determine the optical bandgap (E_g) of the β-Ga_2O_3 substrate (Figure 2, inset). The E_g value for β-Ga_2O_3 is 4.58 ± 0.05 eV.

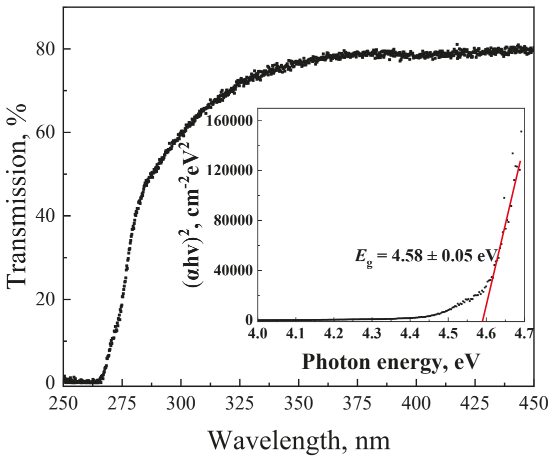

Figure 2. Transmission spectrum of the β-Ga_2O_3 bulk (insert: α^2 versus photon energy).

The capacitance–voltage (C–V) characteristics of the Ni/β-Ga_2O_3 Schottky structures were measured over the voltage range of −5 to 1 V (Figure 3). The net donor concentration N_d and Schottky barrier height Φ_b values were determined from the analysis of the $S_{eff}{}^2/C^2$ vs. V curves using the following expressions, respectively [36,37]:

$$N_d = \frac{2}{e\varepsilon_r\varepsilon_0 b}, \quad (6)$$

$$\Phi_b = \frac{eN_d\varepsilon_r\varepsilon_0 A}{2}, \quad (7)$$

where ε_r = 10 arb. un. is the dielectric constant for β-Ga_2O_3, ε_0 is the dielectric constant, b is the slope of the linear section of the C–V characteristic in coordinates of $S_{eff}{}^2/C^2$ vs. V, and A is the intersection of the $S_{eff}{}^2/C^2$ curve with the y-axis. The net donor concentration was determined to be 9.6×10^{16} cm^{-3}, and the Schottky barrier height was found to be 1.63 eV.

Figure 4a (black curve) shows the current–voltage (I–V) characteristics of the Schottky barrier diode measured under dark conditions and under illumination at a wavelength of 254 nm. The forward dark current increases from 500 fA to 2.4 μA as the bias voltage rises from 0.01 V to 1 V. According to the thermionic emission (TE) model (Equation (7)), as

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well as using the Cheung's method (Equation (8)), the following diode parameters were extracted: saturation current density (J_s), series resistance (R_s), ideality factor (n), Schottky barrier height (Φ_b), ON-voltage (U_{on}) and ON-resistance (R_{ON}) [33,34]. The obtained values are 6.3×10^{-16} A $\times$ cm^{-2}, 39 kΩ, 1.39, 1.58 eV, 0.9 V, and 28 $\Omega \times$ cm^2, respectively. The diode exhibits a high rectification ratio of approximately 9.7×10^6 arb. un. at an applied voltage of $\pm$2 V, confirming the excellent rectifying behavior.

$$J = J_s(e^{\frac{eU}{nKT}} - 1), \quad (8)$$

$$V = JR_sS_{eff} + n\Phi_b + \frac{nKT}{e} \times \ln(\frac{J}{AT^2}), \quad (9)$$

where R_s is the series resistance of SBD and H is the defined function, S_{eff} is the effective anode area, A* = 33.5 A/(cm^{-2} $\times$ K^{-2}) is the Richardson constant, and Φ_b is the height of the Schottky barrier.

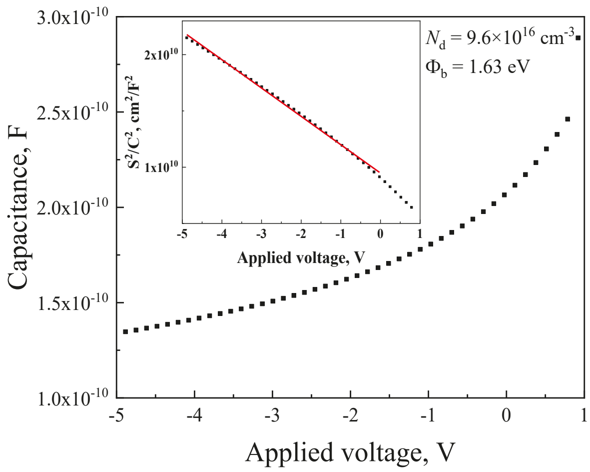

Figure 3. *C–V* characteristics of the SBD based on Ni/β-Ga_2O_3. Inset shows the dependence of $S_{eff}{}^2/C^2$ vs. V.

An increase in the total current of the photodiodes is observed under both reverse and forward bias upon UV illumination at a wavelength of 254 nm with a power density of 620 µW/cm^2 (Figure 4a, red curve). As the reverse bias is increased from 0 to −45 V, the total current rises from 495 pA to 106 µA, while under forward bias, it reaches 148 µA at +2.5 V. The detectors are capable of operating without an external bias, exhibiting a self-powered mode with an open-circuit voltage (U_{oc}) of 0.05 V and a short-circuit current (I_{sc}) of 47 pA.

The photoelectric characteristics of the photodiodes were calculated from the measured *I–V* data. The responsivity increases from 2 µA/W to 3.87 A/W as the reverse bias is raised from 0 to −45 V and reaches 3.7 A/W at a forward bias of +2.5 V (Figure 5a). This indicates the presence of internal photoconductive gain, as the theoretical responsivity does not exceed 0.21 A/W [38]. The responsivity ratio at the same magnitude of applied voltage ± 2.5 V is R(+2.5 V)/R(−2.5 V) = 1275 arb. un. A similar trend is observed for the external quantum efficiency (EQE), which increases from 12×10^{-3}% to 1.8×10^3% under forward bias and to 1.9×10^3% under reverse bias (Figure 5b). The detectivity of the SBD increases from 9.8×10^8 to 4.3×10^{11} Hz$^{0.5}$cmW^{-1} as the reverse bias rises to −45 V. The detectivity at a forward bias of 2.5 V was 1.7×10^{11} Hz$^{0.5}$cmW^{-1}. The maximum PDCR value of 1.6×10^4 arb. un. is observed at a bias of −2.5 V, while further increasing the reverse voltage to −45 V leads to a decrease in the I_L/I_D ratio to approximately 10 arb. un. due to the sharp rise in dark current (Figure 5c).

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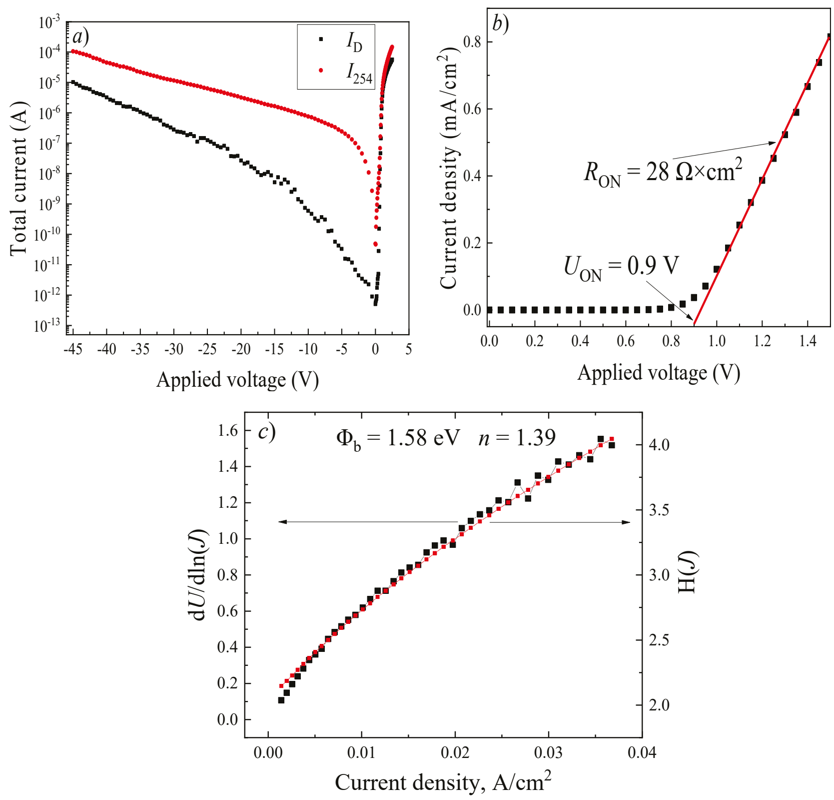

Figure 4. I–V characteristics of the SBD under dark conditions and under exposure to irradiation at λ = 254 nm and P = 620 μW/cm^2 (**a**); Forward branch of J–V characteristic of the SBD based on Ni/β-Ga_2O_3 (**b**); Cheng's method plots of dV/dln(J) vs. J and $H(J)$ vs. J for the SBD based on Ni/β-Ga_2O_3 (**c**).

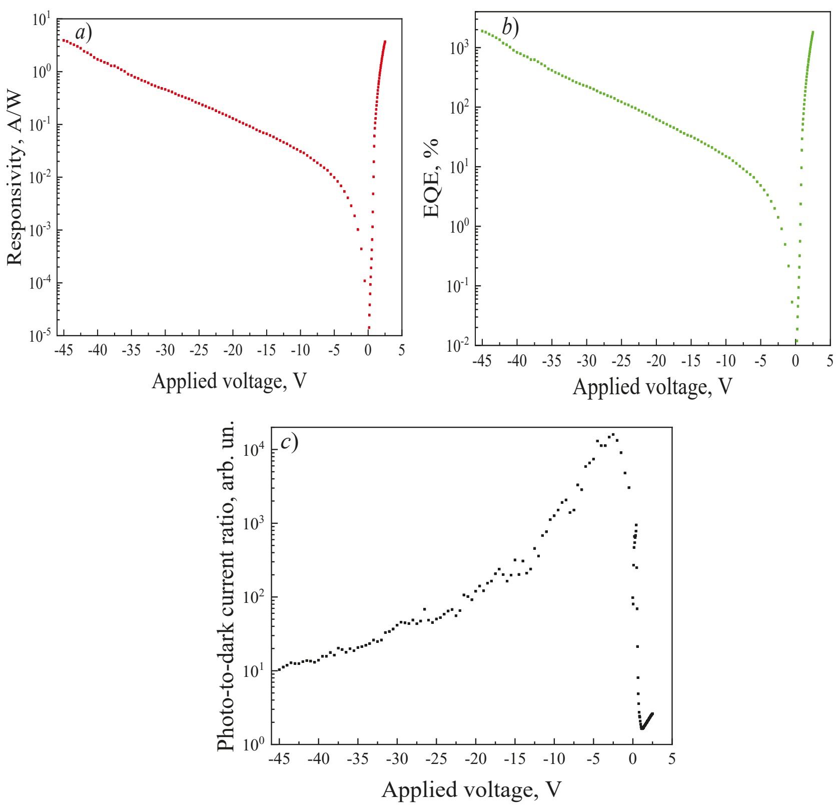

Figure 5. Dependencies of the responsivity (**a**), EQE (**b**), and PDCR (**c**) of the SBD structures on U at λ = 254 nm and P = 620 μW/cm^2.

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The dependence of responsivity on optical power density was measured for SBD based on Ni/Ga_2O_3 (Figure 6a). In the range from 190 to 530 μW/cm^2, a linear section is observed; further increase in power leads to a smaller growth of responsivity.

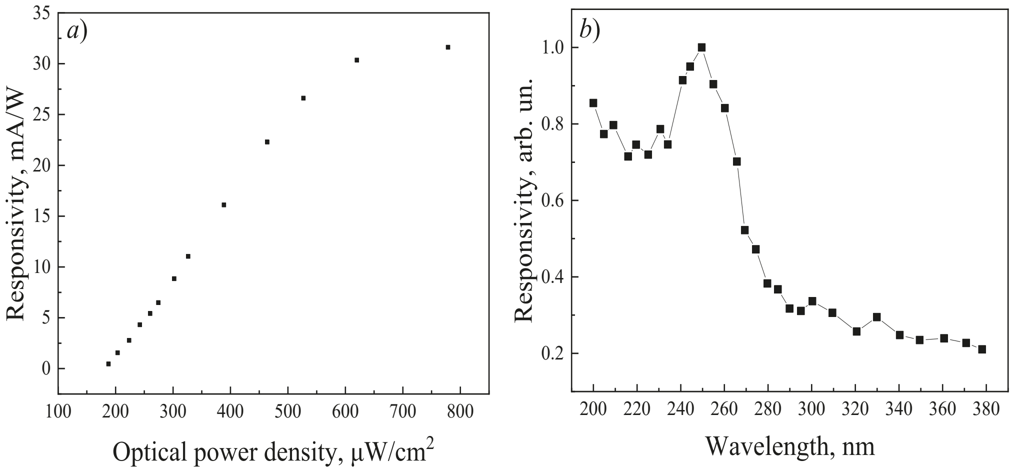

Figure 6. Dependence of the responsivity on the optical power density (**a**) and spectral dependence of the responsivity (**b**) of the Ni/β-Ga_2O_3 Schottky barrier diode at $U = -10$ V.

Figure 6b shows the spectral dependence of the responsivity of the β-Ga_2O_3-based photodiode in the wavelength range of 200–380 nm. A pronounced increase in responsivity is observed starting from approximately 280 nm, reaching a maximum at 255 nm. The residual sensitivity at wavelengths above 260 nm is attributed to defect-related states in the β-Ga_2O_3 substrate, which is further supported by the presence of an Urbach tail in the transmission spectrum (Figure 2) [39].

Figure 7 shows the time-dependent photocurrent response of the β-Ga_2O_3-based photodiode under periodic ultraviolet illumination at bias voltages of 0.7, 1, 5, and 10 V. As the applied voltage increases, the photocurrent amplitude rises, indicating enhanced sensitivity; however, the response speed decreases. The rise time increases slightly from 19 to 26 ms, while the decay time nearly doubles from 29.8 to 59.5 ms as the bias voltage increases from 0.7 to 10 V (Table 1). Additionally, the transient photocurrent curves display asymmetric rise and decay behaviors, which are associated with carrier trapping and release processes occurring at defect states within the β-Ga_2O_3 crystal [40].

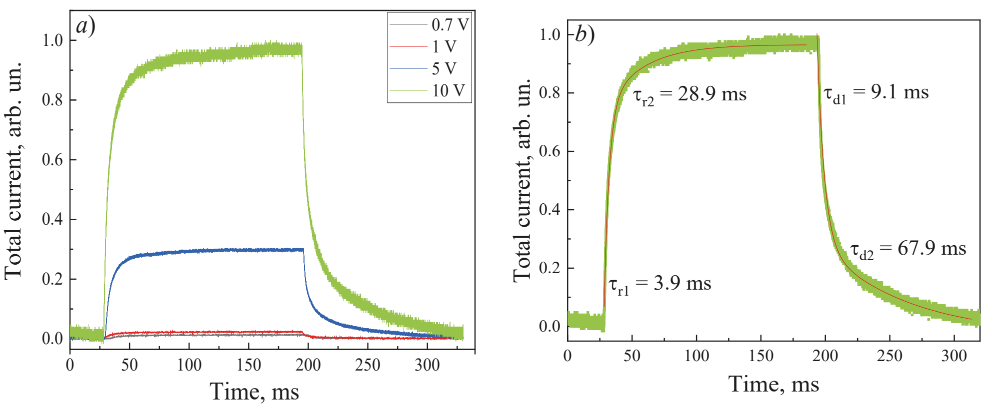

Figure 7. Time-dependent normalized total current of the Ni/β-Ga_2O_3 Schottky barrier diode under 255 nm irradiation at different reverse bias voltages (**a**) and at a fixed bias voltage of 10 V (**b**), with biexponential fitting (red curve).

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Table 1. Dependence of the photoelectric characteristics of the Ni/β-Ga_2O_3-based photodiode on the applied bias.

Applied Reverse Bias, V	Responsivity, mA/W	EQE, %	t_r, ms	t_d, ms	τ_{r1}/τ_{r2}, ms	τ_{d1}/τ_{d2}, ms
0.7	25	17	19	29.8	4.0/25.5	7.1/34.3
1	44	24	29	35	4.4/29.7	6.8/39.7
5	99	48.4	18.3	47.3	4.1/26.2	7.8/51.3
10	305	149	26	59.5	3.9/28.9	9.1/67.9

The time-dependent photocurrent response of the structures can be approximated by biexponential functions using the following expressions:

$$I(t) = I_L - A_1 \times exp\left(-\frac{t}{\tau_{r1}}\right) - A_2 \times exp\left(-\frac{t}{\tau_{r2}}\right), \quad (10)$$

$$I(t) = I_D + B_1 \times exp\left(-\frac{t}{\tau_{d1}}\right) + B_2 \times exp\left(-\frac{t}{\tau_{d2}}\right), \quad (11)$$

where t is the time; A_1, A_2, B_1, and B_2 are constants; and τ_{r1}, τ_{r2} and τ_{d1}, τ_{d2} are the rise and decay time constants of the photoconductivity, respectively. The biexponential behavior indicates the presence of fast (τ_{r1}, τ_{d1}) and slow (τ_{r2}, τ_{d2}) components. The fast-response components of τ_{r1} and τ_{d1} are typically a result of the rapid changes in carrier concentration caused by the generation and recombination of carrier charges during light on/off cycles. The slow-response component of τ_{r2} and τ_{d2} are due to the carrier trapping/releasing from defects [41].

4. Discussion

The Schottky barrier height determined from the *I*–*V* characteristics was 1.58 eV, while the value obtained from the *C*–*V* measurements was slightly higher, 1.63 eV. This difference can be attributed to the presence of interface states at the Ni/β-Ga_2O_3 interface, which lead to a lower effective barrier height extracted from *I*–*V* analysis compared to the equilibrium value derived from *C*–*V* measurements [42,43].

The sensitivity of the β-Ga_2O_3-based detectors to ultraviolet radiation arises from two main mechanisms: band-to-band carrier generation and carrier generation via defect-related states. Band-to-band generation dominates in the deep-UV range, where photon energies exceed the wide bandgap of β-Ga_2O_3 (~4.58 eV), while defect states contribute to residual sensitivity at longer wavelengths, as evidenced by the Urbach tail in the transmission spectrum (Figure 2) and the spectral dependence of the responsivity (Figure 7) [44].

In gallium oxide-based photodetectors, three main photogain mechanisms are generally considered: photoconductive gain, barrier-lowering at the Schottky interface, and avalanche multiplication [28,45]. In the present Ni/Ga_2O_3 diodes, avalanche multiplication can be excluded, since even at a reverse bias of −45 V the estimated electric field does not exceed 500 kV/cm (assuming the full voltage drops across the depletion region), and the observed photoresponse dynamics are inconsistent with avalanche processes [46]. Therefore, the photoresponse must originate from either barrier-lowering or photoconductive gain. A pronounced photocurrent enhancement is observed under forward bias, where the total photocurrent significantly exceeds the dark current, which is atypical for conventional photodiodes. Notably, the external quantum efficiency reaches 1800% at a forward bias of 2.5 V, where the influence of the Schottky barrier is minimal, yet a strong gain persists. This behavior indicates that barrier-lowering alone cannot account for the observed photoresponse, and that the dominant gain mechanism is photoconductive in nature. The photoconductive gain in these Schottky diode-based detectors is analogous

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to that in classical photoconductors. It is facilitated by the relatively high series resistance (R_s = 39 kΩ), which causes a significant portion of the applied voltage to drop across the bulk of the Ga_2O_3 layer rather than being confined to the space-charge region near the Schottky contact. Under reverse bias, the contribution of photoconductive gain decreases. This is further confirmed by the responsivity ratio at ±2.5 V, which reaches 1275 arb. un.

However, it should be noted that, according to the literature, the diffusion length of charge carriers in β-Ga_2O_3 does not exceed 500 nm [47,48]. In this case, if the ring area formed around the Ni contact is considered as the effective active region, the calculated values of R and EQE reach 3.97×10^4 A/W, and 1.9×10^7%, respectively.

The detectors exhibit high responsivity under forward bias, reaching 3.7 A/W at +2.5 V; however, a higher signal-to-noise ratio is observed under reverse bias conditions. This behavior can be explained by the different carrier transport and recombination mechanisms dominating in each regime. Under forward bias, strong carrier injection and the presence of defect-assisted trapping leads to internal gain and enhanced responsivity, but also increase the dark current, thereby reducing the signal-to-noise ratio. In contrast, under reverse bias, the electric field efficiently separates photogenerated carriers and suppresses excess current flow, resulting in lower noise and improved detectivity.

The enhancement in sensitivity comes with a trade-off in response speed (Table 1). The reduction in response speed with increasing applied bias is attributed to the decreased probability of carrier recombination and capture. As carriers traverse the bulk more rapidly due to their higher drift velocity, the likelihood of their being captured by defect states decreases, which in turn slows the recombination of excess carriers [49]. On the other hand, an increase in reverse bias expands the depletion region, activating additional trap states that were not involved at lower bias [50]. The capture and release processes associated with these traps also contribute to the slower transient response. These combined mechanisms explain the observed increase in rise and decay times from 19–26 ms and 29.8–59.5 ms, respectively, as the applied bias increases from 0.7 to 10 V (Table 1, Figure 7). The asymmetric shape of the transient photocurrent curves further indicates the complex dynamics of carrier trapping and emission from defect states in the β-Ga_2O_3 crystal [51].

Overall, the results demonstrate that β-Ga_2O_3 is a highly functional material, combining pronounced rectifying behavior with strong sensitivity to ultraviolet radiation. The diode characteristics of Ni/β-Ga_2O_3 structures ensure low leakage currents and stable operation under dark conditions, while the material exhibits high UV responsivity. This combination of properties, including high photocurrent, significant internal gain, low noise, and the possibility of self-powered operation, makes these devices particularly promising for phototransistor and light-controlled switching applications. The high signal-to-noise ratio under reverse bias and strong responsivity under forward bias enable effective switching between "on" and "off" states, confirming the potential of β-Ga_2O_3 for fast-response, energy-efficient optoelectronic devices.

5. Conclusions

In this work, we have demonstrated a high-performance deep-ultraviolet photodetector based on a vertical Ni/β-Ga_2O_3 Schottky barrier diode fabricated on bulk single-crystal β-Ga_2O_3 substrates. The device exhibits excellent rectifying behavior with a Schottky barrier height of 1.63 eV, a low leakage current density of 6.3×10^{-16} A × cm^{-2}, and a high rectification ratio of ~9.7×10^6 arb. un. The maximum responsivity and external quantum efficiency reach 3.87 A/W and 1.9×10^3%, respectively, indicating internal gain due to carrier trapping and release processes. The detectivity achieves 4.3×10^{11} $Hz^{0.5}cmW^{-1}$, confirming excellent sensitivity to deep-UV radiation. The device exhibits fast photoconductive response, with rise and decay times of 19 ms and 29 ms, respectively, confirming its

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high-speed switching performance. These results highlight the potential of bulk β-Ga_2O_3 as a functional material for self-powered UV photodetectors combining high responsivity, fast response, and good stability.

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Article

Performance Degradation of Ga_2O_3-Based X-Ray Detector Under Gamma-Ray Irradiation

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Abstract: X-ray response performances of a p-NiO/β-Ga_2O_3 hetero-junction diode (HJD) X-ray detector were studied before and after γ-ray irradiation at −200 V, with a total dose of 13.5 kGy(Si). The response performances of the HJD X-ray detector were influenced by the trap-assistant conductive process of the HJD under reverse bias, which exhibited an increasing net (response) current, nonlinearity, and a long response time. After irradiation, the Poole–Frenkel emission (PFE) dominated the leakage current of HJDs due to the higher electric field caused by the increased net carrier concentration of β-Ga_2O_3. This conductive process weakened the performance of the HJD X-ray detector in terms of sensitivity, output linearity, and response speed. This study provided valuable insights into the radiation damage and performance degradation mechanisms of Ga_2O_3-based radiation detectors and offered guidance on improving the reliability and stability of these radiation detectors.

Keywords: gallium oxide; hetero-junction; semiconductor detector; X-ray detection; γ radiation

1. Introduction

The ultra-wide bandgap semiconductor gallium oxide (Ga_2O_3) has the characteristics of low intrinsic carrier concentration and high irradiation resistance, which make Ga_2O_3-based devices promising prospects in the applications of high-energy physics, nuclear reaction monitoring, and space electronics [1–5]. Nowadays, Ga_2O_3-based radiation detectors have drawn great attention and have been designed for neutrons, charged particles, and X-ray detection [6–10]. However, when these radiation detectors are exposed to radiation during operation, their performance degrades. Although the effects of radiation on Ga_2O_3-based devices have been widely investigated recently [11–15], their impact on the performance of radiation detectors has rarely been studied. Gamma rays (γ-rays) are a type of high-energy electromagnetic radiation produced by the de-excitation of atomic nuclei. Their prevalent presence in the universe and nuclear fusion environments, coupled with the challenges associated with effective shielding, has led to significant interest in studying the total dose radiation damage inflicted by γ-rays on semiconductor devices [16–18]. Therefore, studying the degradation of detector performance in a γ radiation environment helps explore the service life of detectors in space and radiation monitoring applications.

In this paper, a p-NiO/β-Ga_2O_3 hetero-junction diode (HJD) X-ray detector was fabricated and tested under X-ray irradiation before and after gamma ray exposure. The gamma radiation was provided by a ^{60}Co source, which provided a dose rate of 0.5 Gy(Si)·s^{-1} in the point of space where the detector was placed. The detector was irradiated at −200 V, the maximum value allowed by the Keysight B2902, which is also the operating bias voltage during X-ray detection. This online mode, which indicates that the detector was biased under irradiation, simulated an actual monitoring environment for the radiation detector. The current-voltage (*I*-*V*), capacitance-voltage (*C*-*V*), and temperature-dependent *I*-*V* (*I*-*V*-*T*) characteristics of the HJD X-ray detector were under dark conditions before and after irradiation. In addition, the X-ray response performances to X-ray dose rates and switching modes were conducted.

2. Experiments

A β-Ga_2O_3 sample from NCT company, with a lightly Si-doped epitaxial layer (grown by the hydride vapor phase epitaxy (HVPE) method) grown on a Sn-doped β-Ga_2O_3 (001)-oriented substrate (650 µm, with Sn doping concentration > 2 × 10^{18} cm^{-3}), was used in this study. The p-NiO/β-Ga_2O_3 HJD X-ray detector was fabricated with an incorporated guard ring to reduce the high electric field at the edges of metal contacts. Figure 1a shows the preparation process of NiO/β-Ga_2O_3 HJDs. Initially, the samples were cleaned with acetone and isopropanol, followed by a four-cycle de-ionized (DI) water rinse and N_2 blow drying. Subsequently, a Ti/Au metal layer (50 nm/100 nm) was deposited by electron beam evaporation as the cathode, followed by rapid thermal annealing at 470 °C for 60 s in N_2 ambient to form ohmic contacts. A SiO_2 layer was then deposited via plasma-enhanced chemical vapor deposition (PECVD) at 350 °C for 8 min as an implantation mask. The incorporated guard ring (GR) pattern was formed by photolithography, and triple-energy N^{++} ion implantation was performed with doses of 8 × 10^{12} cm^{-2} (30 keV), 2.3 × 10^{13} cm^{-2} (160 keV), and 3 × 10^{13} cm^{-2} (360 keV), targeting a box-like doping profile (1.5 × 10^{18} cm^{-3}, 0.5–0.6 µm in depth). The SiO_2 mask and photoresist (PR) were subsequently removed by buffered oxide etch solution (BOE) etching. Then, a second photolithography step patterned the NiO region, followed by a 200 nm NiO film deposition via magnetron sputtering (5 mTorr, Ar/O_2 = 1:1, 130 W) and lift-off process. Post-deposition annealing at 300 °C for 60 s in O_2 ambient was applied to enhance NiO crystallinity. Finally, the anode structure, a 500 µm rounded-corner square (30 µm in radius), was defined by aligned photolithography, and a Ni/Au metal layer (50 nm/150 nm) was deposited via electron beam evaporation and lift-off to complete the device. After fabrication, the detector was packaged on a printed circuit board (PCB) to facilitate testing, as shown in Figure 1b.

The irradiation and radiation response experiments were conducted in a shielding room at room temperature. The HJD X-ray detector was designated for γ-ray irradiation with a total dose of 13.5 kGy(Si) at a bias voltage of −200 V. The γ-ray was generated by the ^{60}Co source provided by the Northwest Institute of Nuclear Technology (NINT), and the dose rate at the irradiated HJD X-ray detector was 0.5 Gy(Si)·s^{-1}. Before and after the γ-ray irradiation, the typical current-voltage (*I*-*V*) and capacitance-voltage (*C*-*V*) characterizations in dark conditions and X-ray response performances of the HJD X-ray detector were measured by a Source Measure Unit (B2902A, Agilent). A hot plate (CH600-190) was used in the *I*-*V*-*T* measurement to provide the temperature for the detector. The X-ray source used in this study was a miniature X-ray tube with a tungsten anode (60 kV, 12W X-ray source, Moxtek, USA) provided by the NINT, which generates a wide continuous spectrum composed by the bremsstrahlung and the characteristic L-lines of tungsten. The average photon energy of X-ray photons was at around 10 keV when the X-ray tube accelerating voltage was set at 30 kV, and the X-ray dose rate was calibrated by Unidos dosimeter to be 383 mGy·s^{-1} for air at a distance of 2 cm from the source. In addition, for the γ-ray and X-ray irradiation experiments, the detector was irradiated from the anode side. In this paper, all test results following irradiation refer specifically to on-line irradiation.

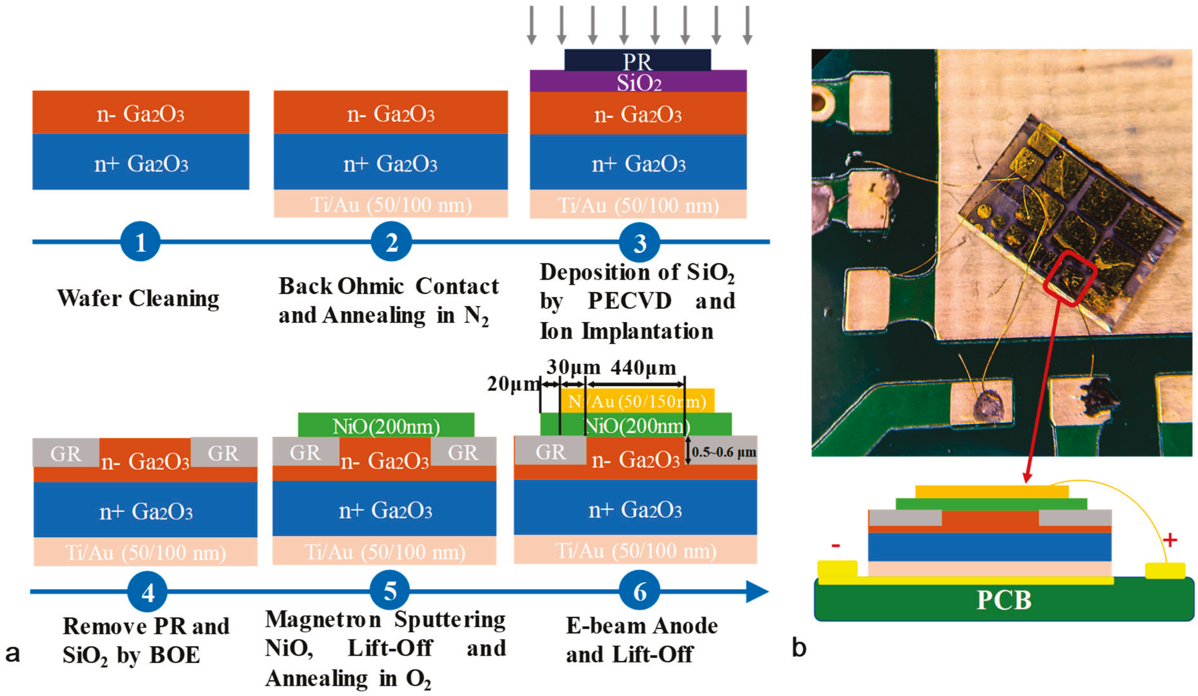

Figure 1. (**a**) The preparation process of NiO/β-Ga_2O_3 HJD X-ray detectors with N+-implanted incorporated guard ring. (**b**) The diagram of the fabricated detector packaged on a PCB.

3. Results and Discussion

Figure 2 displays the typical current-voltage (*I-V*) characteristics of pristine and irradiated HJDs at 300 K. The HJD X-ray detector exhibited similar *I-V* curves before and after γ-ray irradiation. Slight changes in the I-V curves of the HJD X-ray detector were observed after irradiation, such as higher forward current density, turn-on voltage, and leakage current density at high reversed bias. These results exhibited the opposite phenomenon against the study of the offline γ radiation effects (offline means the devices were irradiated without applied bias voltages) on the Ga_2O_3 diodes [19–21], which obtained higher on-resistance and lower leakage current after irradiation.

The *C-V* measurement was conducted to determine the reasons for the changes in the *I-V* curves shown in Figure 2. Figure 3a illustrates the typical *C-V* characteristics of the pristine and irradiated HJDs measured at 100 kHz. According to Equation (1), the net carrier concentration (N_D-N_A) can be extracted from the C^{-2}-V curves shown in Figure 3b. Given the high doping concentration of ~10^{19} cm^{-3} for the NiO layer, the extracted net carrier concentration was mainly attributed to that of β-Ga_2O_3. Thus, the net carrier concentration of Ga_2O_3 increased from 1.38×10^{16} cm^{-3} to 3.07×10^{16} cm^{-3} after 13.5 kGy(Si) γ-ray irradiation, which was opposite to the decreased net carrier concentration revealed by offline radiation [19–21]. The difference between online and offline irradiation results was attributed to an extra electric field within the HJD detector when online irradiation occurred, and, in this case, the radiation-generated current exacerbated the impact of defects in the interface of NiO/Ga_2O_3 and the materials introduced by irradiation [22]. Consequently, the increased net carrier concentration of the β-Ga_2O_3 epitaxial layer caused by γ-ray irradiation reduced the on-resistance and increased the forward current. However, few papers have reported the increasing net carrier concentration after γ-ray irradiation, and the radiation damage mechanism in Ga_2O_3 should be studied further. In addition, the increased net carrier concentration in n-type Ga_2O_3 might have left up the fermi level of the electron and increased the barrier height between the p-NiO and n-Ga_2O_3, leading to a larger turn-on voltage after irradiation.

$$N_D - N_A = -\frac{2}{q\varepsilon_0\varepsilon_r A^2}\frac{1}{\frac{dC^{-2}}{dV}} \tag{1}$$

where C is the measured capacitance of the HJD detector, N_A is the acceptor concentration of β-Ga_2O_3, N_D is the donor concentration of Ga_2O_3, A is the effective area of the HJD, ε_0 is the permittivity of vacuum, and ε_r is the static dielectric constant of the β-Ga_2O_3.

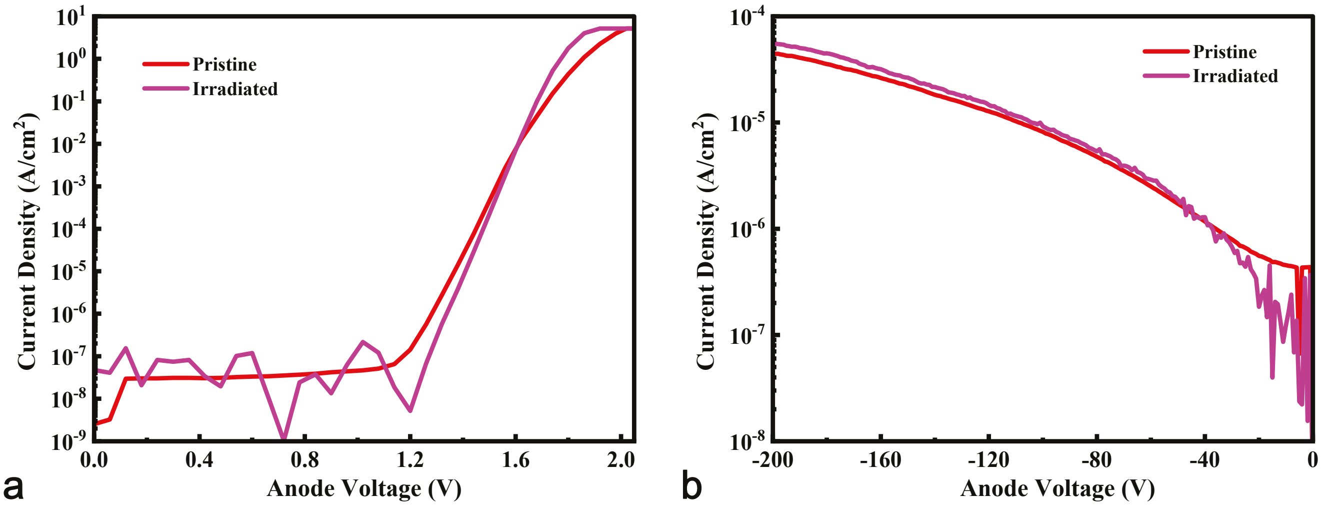

Figure 2. Typical (**a**) forward and (**b**) reverse *I-V* characteristics of pristine and irradiated HJDs X-ray detectors at 300 K.

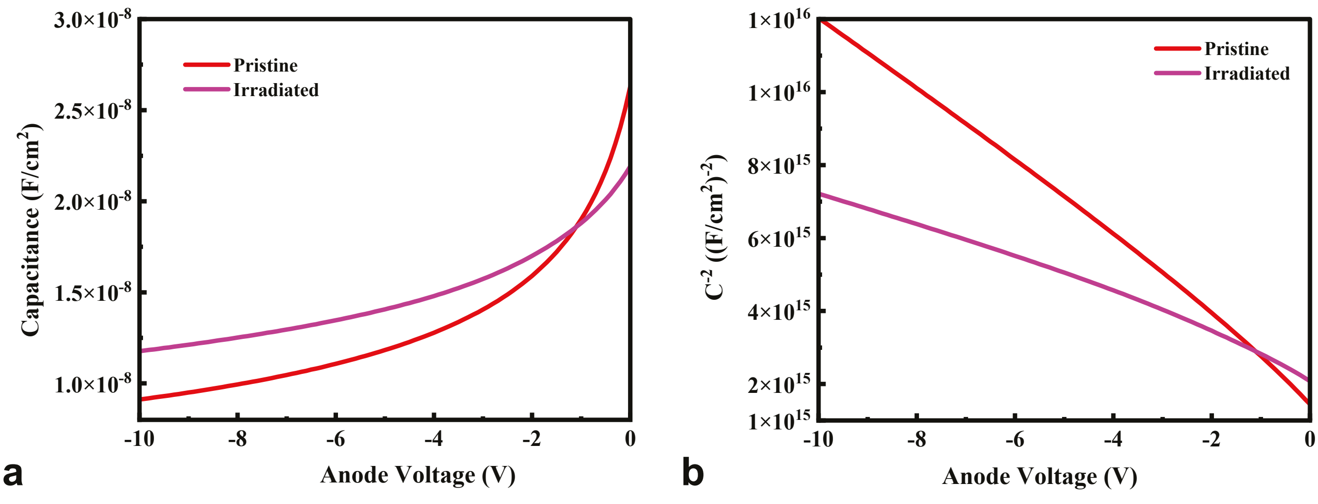

Figure 3. (**a**) Typical *C-V* and (**b**) C^{-2}-*V* characteristics of the pristine and irradiated HJDs X-ray detectors at 300 K.

The X-ray response current was measured under the sweep mode from 0 V to −200 V, with a sampling rate of 1 V/60 ms. Figure 4 shows the net current (I_{net}) of the HJD X-ray detector at various dose rates before and after irradiation, where the net current was defined as the output current under X-ray illumination ($I_{\text{x-ray}}$) minus the dark current (I_{dark}). The net current of the HJD X-ray detector increases with the bias voltage increasing both before and after irradiation. This phenomenon was observed in the Pt/Ga_2O_3 SBD X-ray detector [7] and the p-NiO/β-Ga_2O_3 HJD X-ray detector [23] without an incorporated guard ring, which was associated with leakage current due to the photoconductive mechanism caused by traps/defects in the Ga_2O_3 material. Moreover, because the net carrier concentration increased after irradiation, the electric field in the irradiated detector was higher than that in the pristine detector, resulting in a shorter width of the depletion region of the irradiated detector. Therefore, the irradiated detector showed an increased net current associated with photoconductive gain at bias voltages from 0 V to 200 V due to the high electric field. In contrast, the pristine detector showed transparent photoconductive gain only at higher bias voltages and dose rates, which could be attributed to the space charge effects [24].

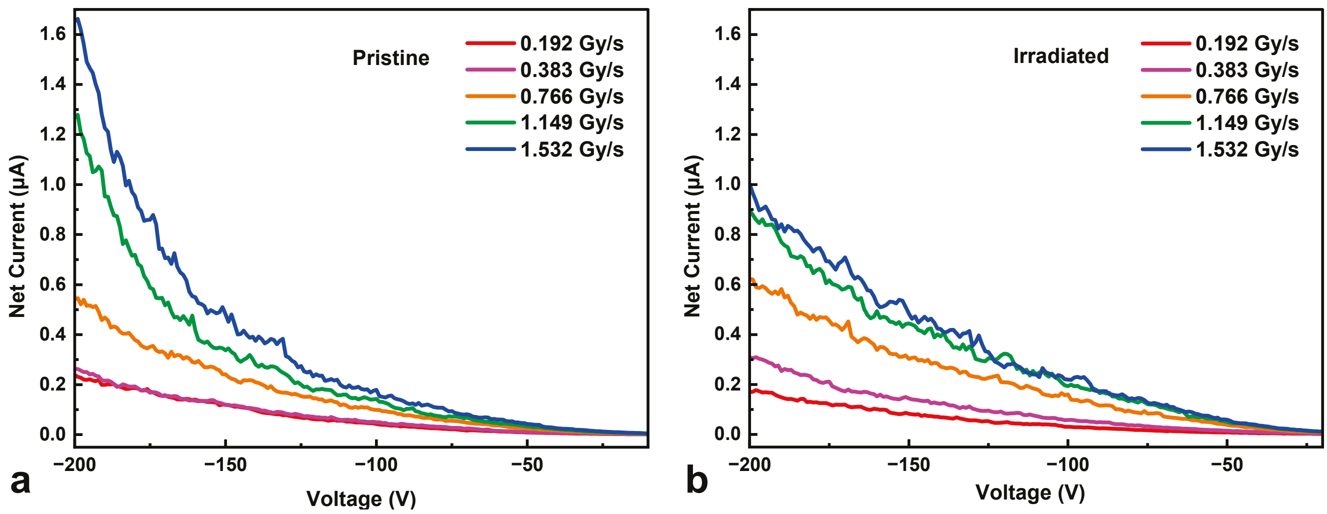

Figure 4. The net current of (**a**) pristine and (**b**) irradiated HJD X-ray detectors at various dose rates against bias voltages.

Figure 5 shows the light-to-dark ratio of the HJD X-ray detector before and after irradiation as a function of the X-ray dose rate from 0.192 $Gy \cdot s^{-1}$ to 1.532 $Gy \cdot s^{-1}$. The irradiated HJD detector exhibited a higher light-to-dark ratio at low bias voltages while showing a lower light-to-dark ratio at high bias voltages than the pristine detector. Specifically, before irradiation, the pristine detector exhibited a non-monotonic light-to-dark ratio curve. In section I, the net current increased with the width of the depletion region and faster than the low leakage current, and the light-to-dark ratio increased with the bias voltages. As the voltage increased, the rate of leakage current also rose, leading to a decrease in the light-to-dark ratio in section II. When the bias voltage reached around -130 V, a high net current was obtained at high dose rates of 1.149 $Gy \cdot s^{-1}$ and 1.532 $Gy \cdot s^{-1}$, leading to an increased light-to-dark ratio with the bias voltages in section III. In contrast, the irradiated HJD detector exhibited a decreased light-to-dark ratio overall. At low bias voltages (section I), the pristine detector showed a lower ratio than that of the irradiated detector because γ-ray irradiation caused an increase in the barrier height between p-NiO and n-Ga_2O_3, resulting in a decrease in leakage current. However, the net current of the irradiated device was restricted, and the leakage current continued to rise, leading to a steady decline in the light-to-dark ratio as the bias voltage increased.

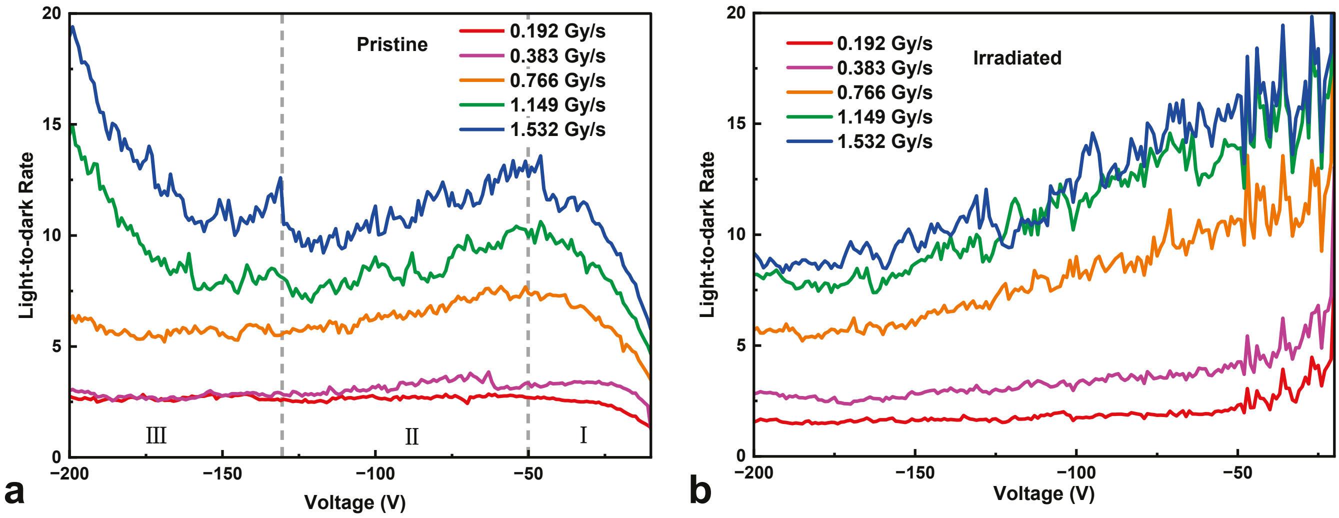

Figure 5. The light-to-dark ratio of (**a**) pristine and (**b**) irradiated HJD X-ray detectors at various dose rates against bias voltages.

To quantitatively evaluate the X-ray detection performances of the HJD X-ray detector before and after irradiation, the sensitivity (*S*) and the noise-equivalent dose rate (*NED*) were further calculated. The sensitivity is defined as the ratio between the net current and the incident X-ray dose rate reaching the detector (*D*) [23]:

$$S = \frac{I_{net}}{D} \tag{2}$$

The noise-equivalent dose rate is defined as the incident X-ray dose rate that gives a signal-to-noise ratio of one in a 1 Hz bandwidth, which is a measure of the detection limitation of the detector and can be described by the following Equation (3) [23], where I_{dark} is the dark current (leakage current) of the detector, and q is the electron charge:

$$NED = D\frac{\sqrt{2qI_{dark}}}{I_{net}} \tag{3}$$

Figures 6 and 7 plot the sensitivity and noise-equivalent dose rate versus reverse bias voltage at various dose rates from 0.192 Gy·s^{-1} to 1.532 Gy·s^{-1} for the HJD X-ray detectors before and after irradiation, respectively. The sensitivity of the HJD X-ray detector increased with the bias voltage before and after irradiation. Between the biased voltages from 0 to −160 V, the discrepancy of the sensitivity curve of the pristine detector at high dose rates was less than that of the net current, indicating a good linear relationship between net current and X-ray dose rates. The curves separated at bias voltages from −160 V to −200 V, and the output linearity was broken, which was associated with the trap-related photoconductive current and space charge effects. In contrast, for the HJD X-ray detector after irradiation, the sensitivity curves exhibited a clear difference, meaning that a sub-linear output occurred. The pristine HJD detectors exhibited linear outputs below −100 V, and the irradiated HJD detectors did not exhibit good linear outputs at various bias voltages. Hence, they are not suitable for X-ray dose rate detection. Moreover, attributed to the low dark current of the HJD X-ray detector, the *NED* decreased with bias voltages before and after irradiation. The *NED* of the irradiated HJD X-ray detector was higher than that before irradiation because the sensitivity decreased after the γ-ray irradiation. In addition, Figure 8 shows the net currents against X-ray dose rates of the pristine and irradiated HJD X-ray detectors at various bias voltages. The pristine detector exhibited sub-linearity only at a high bias voltage of −200 V. In comparison, the irradiated detector exhibited sub-linearity during the range from 0 V to −200 V, showing consistency with previous analysis.

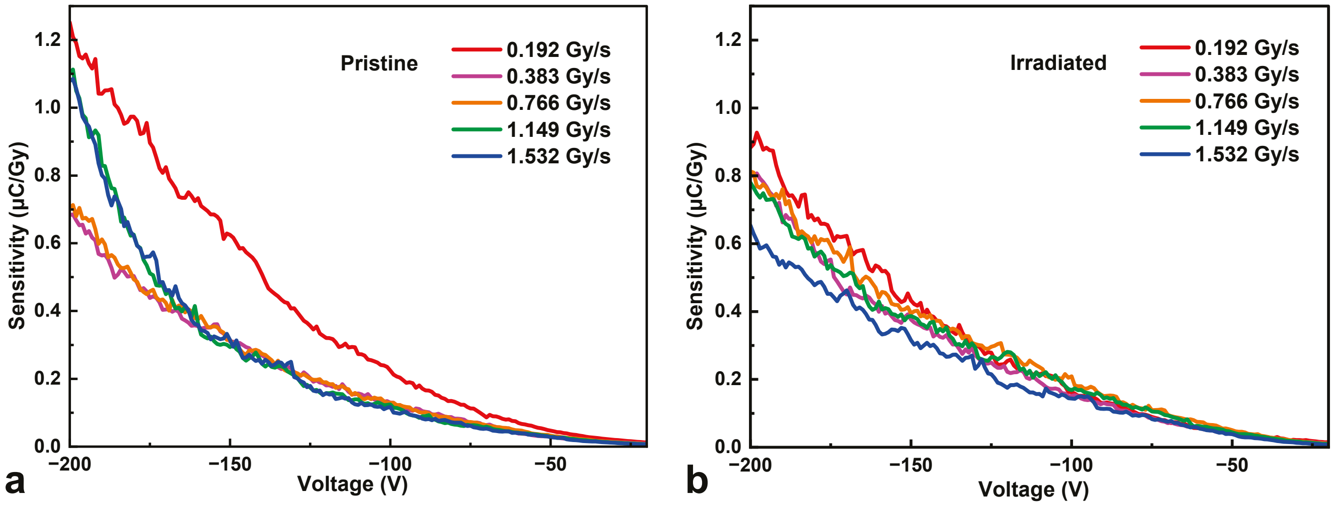

Figure 6. Sensitivity of (**a**) pristine and (**b**) irradiated HJD X-ray detectors at various dose rates against bias voltages.

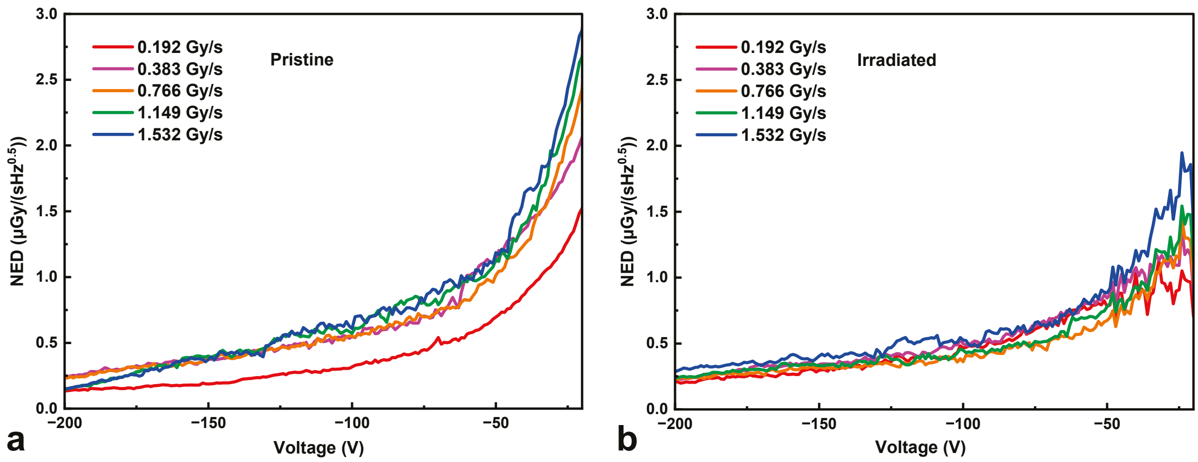

Figure 7. The noise equivalent dose rate (*NED*) of (**a**) pristine and (**b**) irradiated HJD X-ray detectors at various dose rates against bias voltages.

Figure 9 reveals the transient response of the pristine and irradiated HJD X-ray detectors under switching X-ray illumination with a switching period of 10 s and a sampling rate of 20 ms. When the detector was biased at 0 V, the response current was equal to the photovoltaic current. In this mode, the response current was determined by the pn junction quality. It was clear that, after the γ-ray irradiation, the HJD X-ray detector exhibited a worse response to the switching X-ray at 0 V, meaning a worse junction characteristic of the HJD device caused by the irradiation. Moreover, The HJD before and after irradiation exhibited stable transient responses to the switching of X-ray illumination when biased at −200 V. Figure 9c,d show the absolute value of response current. However, the response time of the detector at −200 V was influenced by the photoconductive effect [7,19]. In this mode, the capture and release of the photo-generated carriers by the deep-level traps have a specific lifetime, leading to a relatively long response time. To study the trap-related time constant (τ) of the HJD X-ray detectors before and after irradiation, the fitting curve was performed at the dose rate of 0.766 Gy·s^{-1} using exponential decay functions [25]:

$$I(t) = I_0 + \sum_{i=1}^{n} I_i \exp[-(t - t_0)/\tau_i] \tag{4}$$

where $I(t)$ is the response current with a function of time of the HJD detector, t is the time, t_0 is the initial time when the X-ray illumination is turned on or off, I_0 is the steady current with/without X-ray illumination of the HJD detector, τ is the time constant, and I is the coefficient of time response for the τ.

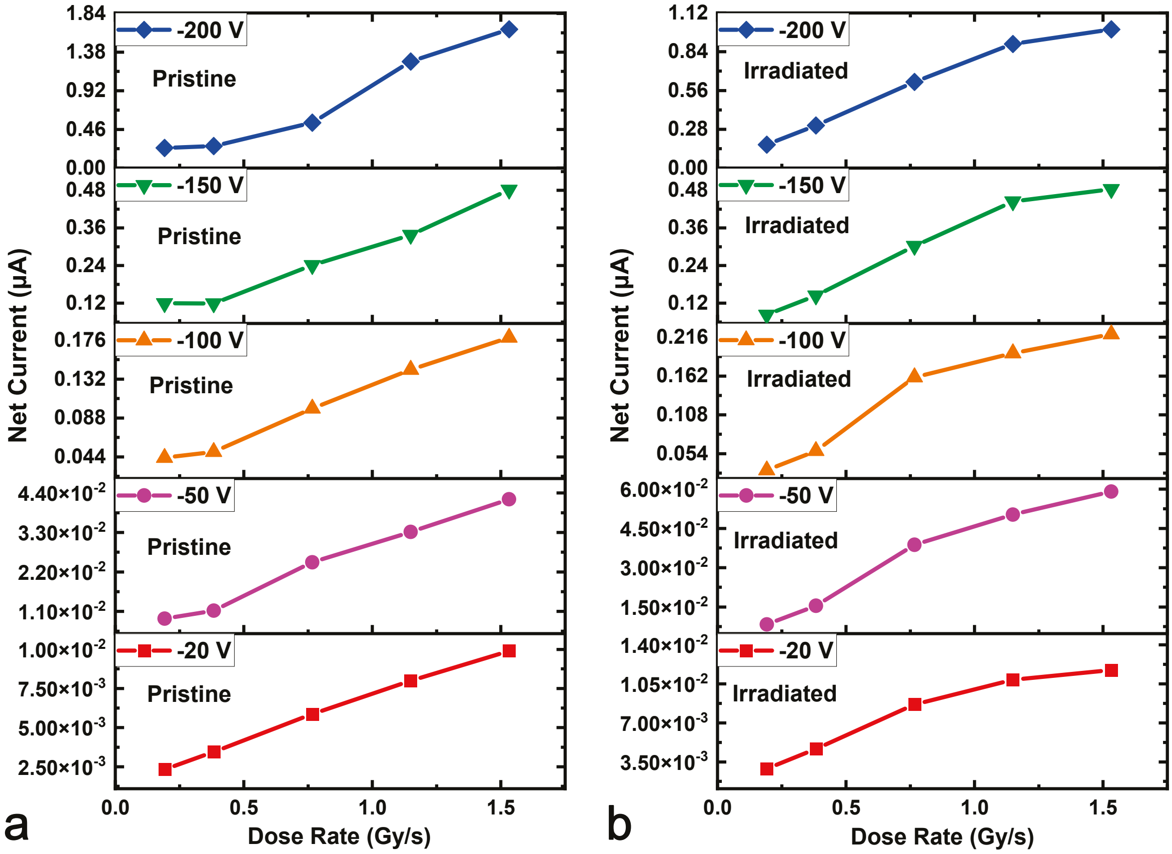

Figure 8. The net currents against X-ray dose rates of the (**a**) pristine and (**b**) irradiated HJD X-ray detectors at various bias voltages.

Figure 10 shows the fitting curves in one period of the HJD X-ray detector before and after irradiation. Two different time constants are obtained for both response curves to reveal the factors that affected the response/recovery time of the detector, where the response time is defined as the duration time required for the current to increase from 10% to 90% of the difference between the maximum and minimum currents. Conversely, the recovery current is defined as the time it takes for the current to decrease from 90% to 10% of that same difference. For the pristine detector, the response time constants were 0.60 s and 2.10 s with the coefficients 0.73 and 0.13, and the recovery time constants were 0.27 s and 3.23 s with the coefficients 0.99 and 0.37. For the irradiated detector, the response time constants were 0.24 s and 1.61 s with the coefficients 0.29 and 0.41, and the recovery time constants were 0.31 s and 3.81 s with the coefficients 0.55 and 0.32. More fitting information can be found in Table 1. Although the response time constants of the pristine detector seem longer than the irradiated detector, the coefficient of the short constant of the pristine detector was larger, leading to a faster response time. The longer response time indicated that the photoconductive mode was enhanced after the γ-ray irradiation. This result might be caused by the higher electric field in the irradiated detector due to the increased net carrier concentration or new type of traps generated by the γ-ray irradiation, which should be studied further.

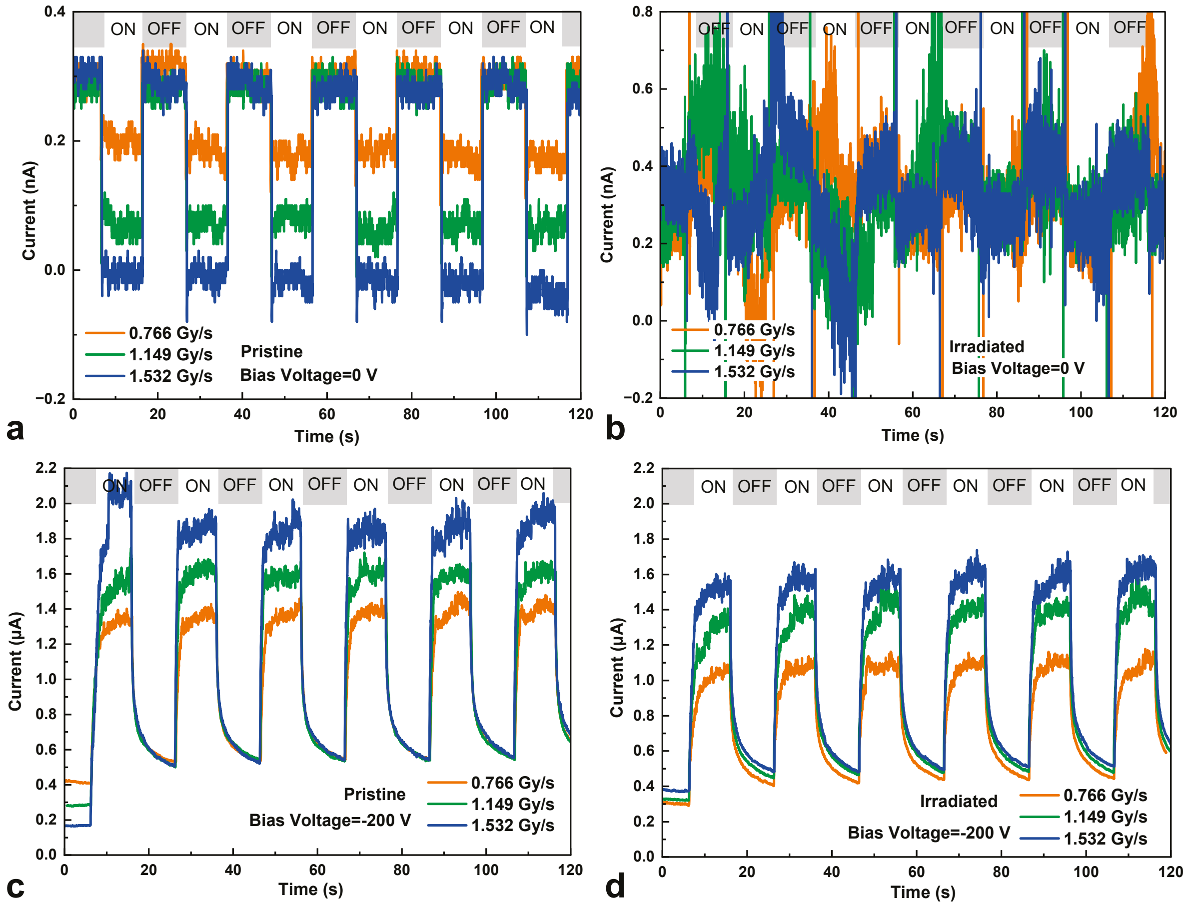

Figure 9. The transient response of the pristine and irradiated HJD X-ray detectors to the switching of X-ray illumination at biases of (**a**,**b**) 0 V and (**c**,**d**) −200 V.

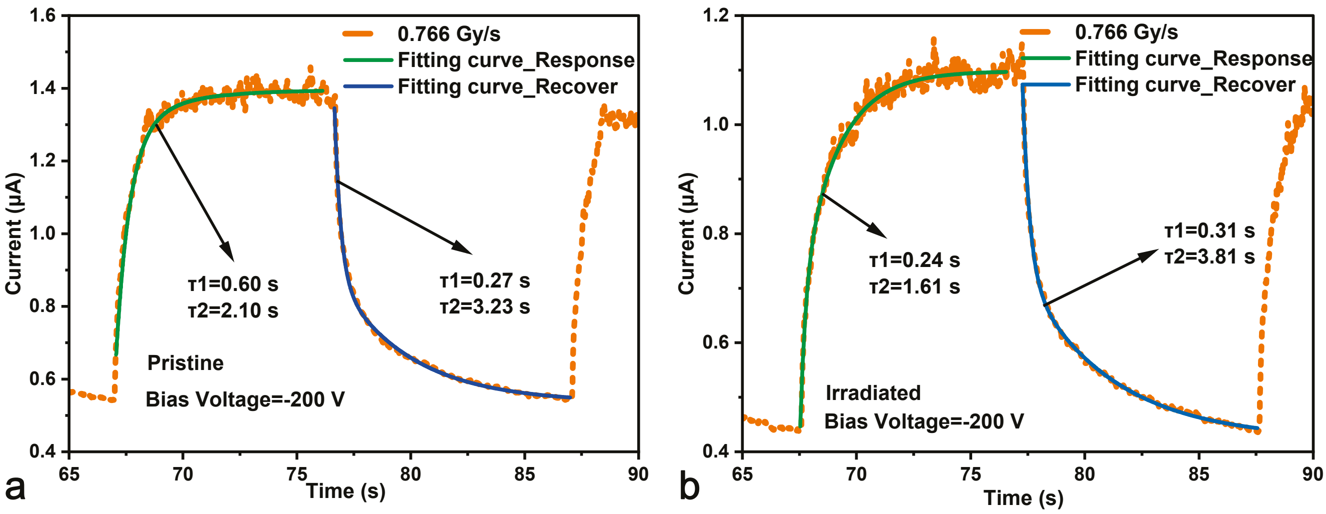

Figure 10. The transient response and the fitting curves of the (**a**) pristine and (**b**) irradiated HJD X-ray detectors to the switching of X-ray illumination at biases of −200 V in one period.

Table 1. The response/recovery time of the HJD detector before and after radiation.

Parameters	Pristine (Res./Rec.)	Irradiated (Res./Rec.)
Response time	2.92 s	4.37 s
Recovery time	5.03 s	5.16 s

In our previous study [7,23,25], the long-time constant-associated leakage current at high bias voltages mainly contributed to the electric-field-enhanced thermal emission process, such as the Poole–Frenkel emission (PFE). In this case, the reverse *I-V-T* characteristics of the HJD X-ray detector from 0 V to −200 V before and after irradiation were measured. The fitting results indicate that the PFE model was not suitable for the pristine detector but suitable for the irradiated detector. Figure 11a plots the J/E vs. $E^{0.5}$ curve of the irradiated detector, according to the following Equation (5) [26]. To extract the relevant parameters in Equation (7) or (8) [15,26], $m(t)$ and $b(t)$ of the pristine and irradiated detectors are also plotted in Figure 11b,c. After the linear fitting process, the ε_∞ and $q\phi_t$ were calculated, as shown in Table 2.

$$J = CE_b \exp\left[-\frac{q\left(\phi_t - \sqrt{qE_b/\pi\varepsilon_0\varepsilon_\infty}\right)}{kT}\right] \tag{5}$$

$$\log(J/E_b) \equiv m(T)\sqrt{E_b} + b(T) \tag{6}$$

$$m(T) \equiv \frac{q}{2.3kT}\sqrt{\frac{q}{\pi\varepsilon_0\varepsilon_\infty}} \tag{7}$$

$$b(T) \equiv -\frac{q\phi_t}{2.3kT} + \log C \tag{8}$$

where E_b is the max electric field in the p-NiO/β-Ga_2O_3 HJD interface, $q\phi_t$ is the barrier height of electron emission from the trap states, ε_0 is the permittivity of vacuum, ε_∞ is the high-frequency relative dielectric constant, q is the electron charge, k is the Boltzmann constant, T is the temperature, and C is a constant.

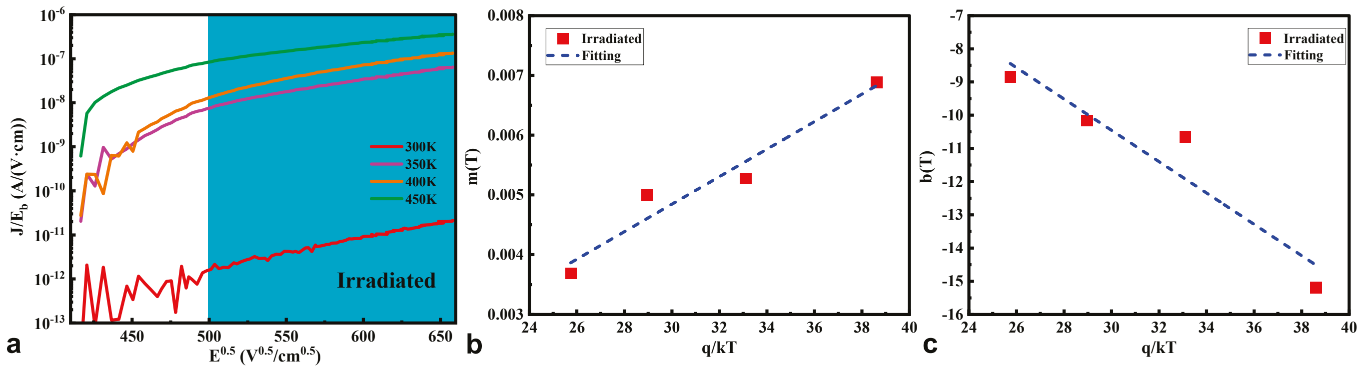

Figure 11. (**a**) The reverse *I-V-T* characteristics of the irradiated HJD X-ray detectors measured in a temperature range of 300 K to 450 K. (**b**) The m(T) curves and (**c**) the b(T) curves, as functions of q/kT for the measured irradiated HJD X-ray detectors (blue region).

Table 2. Extracted PFE parameters of the irradiated detector.

Parameters	Irradiated
ε_∞	2.27
$q\phi_t$	1.07 eV

After the γ-ray irradiation, the E_b was increased due to the increased net carrier concentration of β-Ga_2O_3, and, thereby, the PFE process was enhanced. The Arrhenius plot of m(t) versus 1/kT allows us to estimate the high-frequency relative dielectric constant. The extracted ε_∞ after irradiation was 2.27, close to the commonly used value of 3.60 [27], and the extracted energy level of the electron trap was located at 1.07 eV below the minimum value of the conduction band (E_c) of β-Ga_2O_3 material. This trap was considered the primary trap state causing the PFE process [28] and was usually associated with donor-like oxygen divacancies in β-Ga_2O_3 [29].

4. Conclusions

In this study, a p-NiO/β-Ga_2O_3 HJD X-ray detector was tested under X-ray illumination before and after an online 13.5 kGy(Si) γ-ray irradiation at bias at -200 V. The X-ray response of the HJD X-ray detector was influenced by the trap-associated leakage current mechanism before and after irradiation. For instance, the net (response) current of the detector increased with bias voltages much faster than the expanding rate of the depletion region of HJD, and the output linearity against X-ray dose rates and response time characteristics worsened. Moreover, after irradiation, the net carrier concentration of β-Ga_2O_3 increased from 1.38×10^{16} cm^{-3} to 3.07×10^{16} cm^{-3}, leading to a lower on-resistance, a larger barrier height of the HJD and a shorter width of the depletion region at a specific bias voltage. Thus, the reverse leakage current at low bias voltage was suppressed but increased at higher bias voltage due to the strengthening of the electric field. As a consequence, the PFE process was enhanced after the γ-ray irradiation. However, the underlying mechanisms for Ga_2O_3-based devices remain to be further investigated. In addition, the sensitivity of the HJD X-ray detector was lower at -200 V. The nonlinearity outputs against X-ray dose rates were observed from 0 V to -200 V. In addition, the transient response to switching X-ray illumination of the HJD X-ray detector was also degraded after irradiation; the response noise at 0 V increased, and the response time at -200 V increased from 2.92 s to 4.37 s. In short, the net carrier concentration of β-Ga_2O_3 increased, and the trap (E_c—1.07 eV of β-Ga_2O_3 material)-associated PFE process enhanced after the γ-ray irradiation, limiting the sensitivity, linearity, and transient response performances of the HJD X-ray detector. In order to better improve the service life of the HJD X-ray detector in the irradiated environment, it is necessary to study the method of inhibiting the leakage current related to trap behavior.

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Conflicts of Interest: The authors declare no conflicts of interest.

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Numerical Simulation of Thermal Cycling and Vibration Effects on Solder Layer Reliability in High-Power Diode Lasers for Space Applications

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Abstract: High-power laser diodes (HPLDs) are increasingly used in space applications, yet solder layer (SL) reliability critically limits their performance and lifespan. This study employs finite element analysis to evaluate SL failure mechanisms in microchannel-cooled HPLDs with two packaging configurations under thermal cycling and vibration. Based on the Anand constitutive model, contour plot analysis revealed that the critical stress–strain regions in both SLs were located at their edges. The stress–strain values along the X-axis of the SLs exceeded those in other axial directions, and SL failure would preferentially initiate from the edges along the cavity length direction. During random vibration analysis with excitation applied along the Z-axis, the equivalent stresses in both SLs exceeded X-/Y-axis levels. However, these values remained far below their yield strengths, indicating that only elastic strain and high-cycle fatigue occurred in the SLs. The calculated thermal fatigue lives of the two SLs were 2851 cycles and 5730 cycles, respectively. Their random vibration fatigue lives were determined as 5.75×10^7 h and 8.31×10^7 h. Using damage superposition under combined thermal-vibration loading, the total fatigue lives were predicted as 14,821 h and 29,786 h, respectively, with thermal cycling-induced damage dominating the failure mechanism.

Keywords: space environment; high-power laser diode; solder layer; thermal cycling; random vibration; life prediction

1. Introduction

Laser diode (LD) has displayed rapid development since 1962 when the world's first LD came into being, with increasing types and expanding application scope [1–5]. As a class of laser-generation devices with semiconductor materials as the operating substance, LD has gradually become one of the indispensable photoelectric devices in modern science and technology following decades of development. HPLDs, due to their small volume and mass, high electro-optical conversion efficiency, long service life, and wide wavelength covering range, have been extensively applied in such fields as industry, military, communication, optical storage, and laser medicine in recent years [6,7]. With the development of semiconductor technology, LDs have become the research object of many scholars, and a lot of progress has been made in the basic theory and physical mechanism research, material research, manufacturing process research, etc., which has prompted the development of the HPLDs towards high power, high efficiency, and miniaturization.

The SLs are an essential part of the packaging structure of the HPLDs. The SL serves as the medium that connects the LD chip to the heat sink (HS), N-foil, insulating layer, and other layer structures. The SL plays several key roles in the operation of an HPLD. The SL assumes the task of electrical connection so that the HPLD can transmit electrical signals; it also assumes the task of mechanical connection and can play the role of a stress buffer, the LD chip fixed in the HS, so that it cannot fall off; it also provides a space to make the package chip to form a heat dissipation path, reducing the impact of the heat generated on the chip. Once the SL has a problem, it will inevitably lead to the HPLD as a whole not working properly. In the field of electronic packaging reliability, interface (this paper for the SL) reliability engineering has always occupied the core research position. Therefore, how to improve the environmental adaptability of the SL of the HPLD has become the focus of improving the reliability of the HPLD in harsh environments.

In laser packaging, the SLs are used for connection in multiple places. According to the research results of Ephraim Suhir [8], Zhangpu [9], and others [10–12], it is determined that the SL connecting the chip and the HS play a key role in the reliability of the HPLD, that is, the marked place in Figure 1. Ephraim Suhir et al. [8] used the finite element method to systematically simulate the SL of the HPLD. They simulated the steady-state and transient thermal behaviors of conduction-cooled HPLDs in continuous wave (CW) mode and explained the important influence of SL reliability on the overall performance and service life of HPLDs from the perspective of thermal stress: On the one hand, the SL has low yield strength and few fatigue cycles, making it the "weak link" connecting the HS and the chip. Under cyclic thermal stress, the SL usually starts to age and fail before other structures; on the other hand, the SL provides a "buffer zone" between the chip and the HS. By matching the coefficient of thermal expansion (CTE), it offsets part of the interaction between the chip and the HS under thermal stress, reduces the thermal deformation of the chip, and prolongs the service life of the device. In addition, the model designed in this paper can calculate the transient peeling stress and shear stress of the SL in CW mode. Therefore, in order to reduce the calculation amount and simplify the name, unless otherwise specified, the term "SL" in the following text refers to the SL connecting the bar chip and the microchannel heat sink (MCHS).

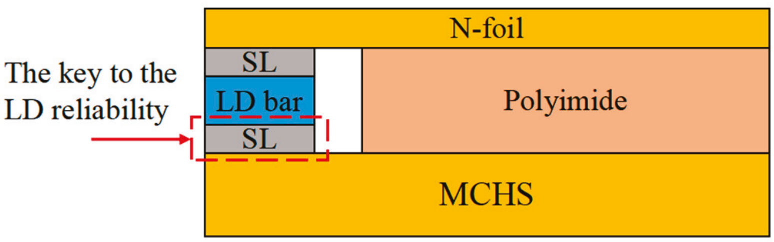


Figure 1. The critical SL affecting laser reliability.

Applied to the space environment LD in the process of processing, loading and adjusting, transportation, launching and orbiting, etc., the LD will be subjected to a variety of complex, harsh environmental effects, such as high temperatures, low temperatures, high- and low-temperature cycling, acceleration overload, random vibration, and so on. Therefore, the environmental adaptability of the LD has put forward higher requirements. Failure mechanism analysis shows that temperature loading (55%) and mechanical vibration (20%) together constitute the dominant factor in the dual-stress-coupled failure mechanism, while the remaining 25% of the failures are attributed to other environmental stress compounding effects (humidity, barometric pressure perturbation, etc.). This failure distribution characteristic confirms [13–17], at a statistical level, the engineering necessity of establishing a reliability assessment system based on the accelerated thermal–vibration biaxial degradation effect. The environmental adaptability requirements [18] cover 13 types of environmental stress conditions (thermal cycling, random vibration, etc.), which would result in a waste of resources if full-scale tests of the same intensity were used. According to the statistical analysis of failure inducers of electronic devices [19], thermal cycling and random vibration are located in the top two. Therefore, these two main triggers are selected as the loading conditions for environmental tests to be studied in depth in this paper. W. Wright et al. [20] conducted reliability testing of commercial high-power fiber-coupled LDs for space applications, performing mechanical, vibration, and thermal cycling, radiation testing, and destructive part analysis and verifying that they met the 5000 h service life requirement through a 500 h accelerated life test. The test device was stable under a 20 krad radiation dose, −40 to 60 °C thermal cycling, and 20 g vibration but failed due to a package defect during constant acceleration testing. Pol Ribes-Pleguezuelo et al. [21] focused on the small diode-pumped laser of the Raman Laser Spectrometer of the Exomars mission to evaluate soldering and bonding through thermal cycling, random vibration, sine vibration, and shock testing. Vibration and shock tests evaluated the performance stability of the laser under solder and adhesive assembly processes. The adhesive-assembled laser showed no significant damage after the vibration and shock tests, but the output power continued to drop during thermal cycling, the optical performance deteriorated, and the laser resonance cavity showed gradual misalignment. The low-stress weld-assembled lasers showed good stability of the main optical parameters after functional thermal cycling and mechanical and ion radiation tests, with no obvious output power degradation or damage.

In the field of military electronic equipment reliability verification, MIL-STD-810F pointed out that [18] the use of simulation environment test methods in the product development period not only can significantly shorten the test cycle and reduce costs but also ensure that the product meets the adaptability of the actual service environment requirements. Most of the existing electronic packaging reliability research focuses on the traditional microelectronics packaging field of various types of solder joint failure behavior and for optoelectronic integrated devices—the HPLD chip SL, especially, in the multi-field coupling effect of the interface reliability of the systematic research is relatively scarce.

In this paper, the three-dimensional physical model of two kinds of microchannel packaged HPLDs is established, and the reliability of the SL of the two kinds of packaged HPLDs is compared and studied under the effects of thermal cycling, random vibration, and thermal–vibration coupling. Under the loading conditions of thermal cycling and random vibration, the fatigue failure position of the SL is studied, the maximum equivalent stress and strain distribution at this position are analyzed, and the fatigue life of the SL is predicted under the combined action of thermal vibration and vibration coupling loading.

2. Numerical Model and Theoretical Analysis

2.1. Physical Geometric Model

The author's research team [22] proposed an optimized MCHS packaging form for space environment in a previous study. The optimized package form improves the heat transfer efficiency and heat dissipation performance of the HPLD, and the maximum temperature of the HPLD was reduced from 52.44 °C to 41.23 °C. The optimized package form has good overall performance. This paper presents a comparative study of the HPLDs using pre-optimization and post-optimization package forms. The cross-sectional diagram of the HPLD package structure before optimization is shown in Figure 2a. Schematic cross-section of the HPLD package structure after optimization is shown in Figure 2b. As shown in Figure 3a, lasers were equipped with a microchannel water-cooled packaging structure, which consisted of an MCHS, SLs, an LD bar, an insulating film, and a copper sheet. The bar was packaged with P surface adown and welded at the front end of the microchannel water-cooled HS with SL. Distilled water flowed into the internal MCHS from the water inlet, fully exchanged heat with the copper wall, took away the heat generated by the bar during operation, and finally flowed out from the water outlet, as shown in Figure 3b. The parameter of the MCHS was 27 mm × 10.8 mm × 1.5 mm, and the MCHS was composed of five layers of stitch-welded oxygen-free high-conductivity copper, as shown in Figure 3c. The LD bar studied in this paper had a bar wavelength of 808 nm, a ridge width of 150 µm, a filling factor of 30%, a cavity length of 1000 µm, and 19 light-emitting points. At 25 °C, the injection current was 50 A, the maximum output power was 55.31 W, the electro-optical conversion efficiency was 58.74%, the slope efficiency was 1.21 W/A, and the divergence angles of the slow and fast axes of the laser die were less than 10° and less than 39°, as shown in Figure 3d. The properties of each material are shown in Table 1.

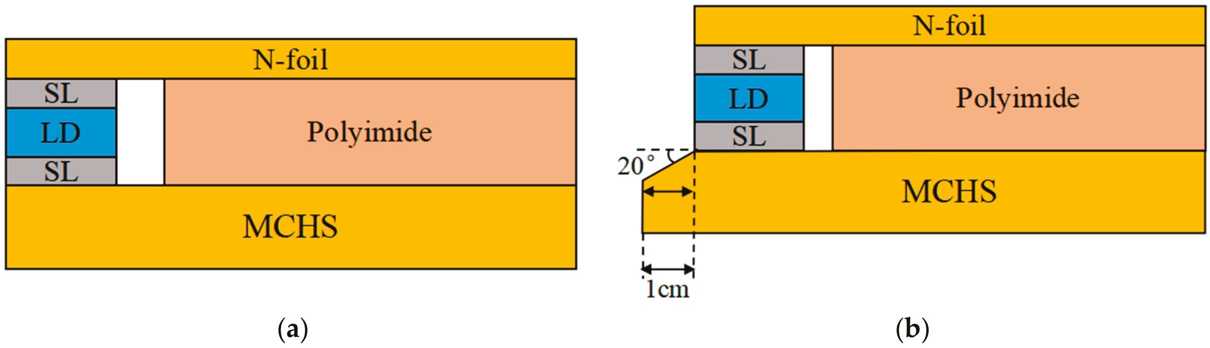


Figure 2. Schematic diagram of the LD packaging. (**a**) Before optimization and (**b**) after optimization.

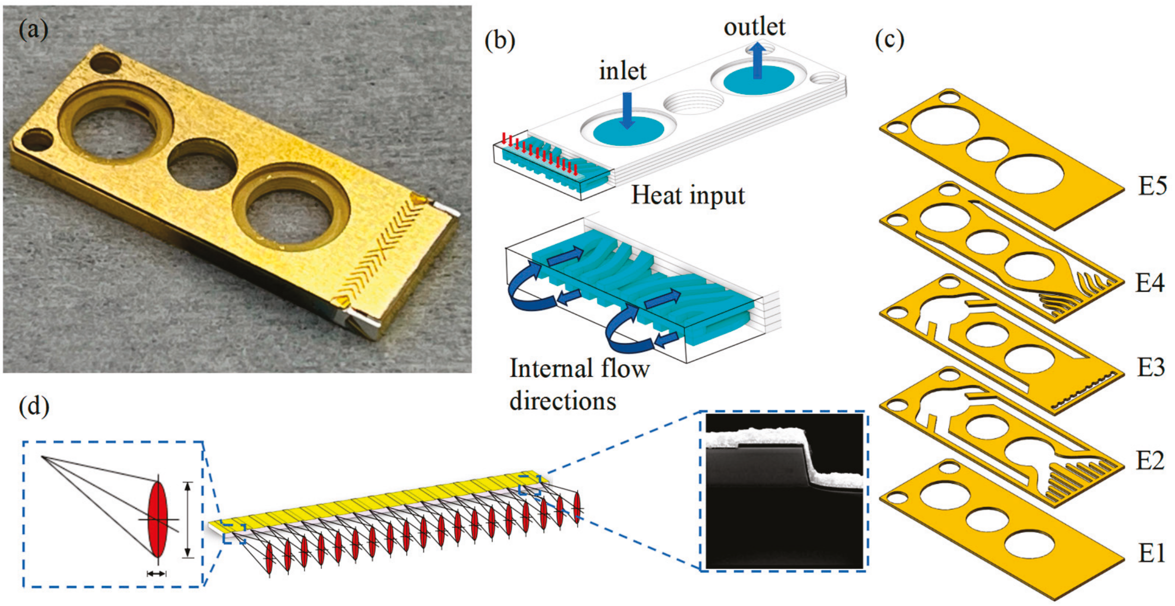


Figure 3. Schematic diagram of the LD. (**a**) Physical diagram of the LD in the MCHS package; (**b**) schematic diagram of the MCHS heat dissipation; (**c**) internal structure of the MCHS, E1, E2, E3, E4, and E5 are the Bottom Layer, Inlet Layer, Separating Layer, Outlet Layer, and Top Layer, respectively; and (**d**) the LD bar and its local magnification.

Table 1. Material properties of each layer in the LD.

Materials	Density (Kg/m^3)	Young's Modulus (10^9 Pa)	CTE (10^{-6} 1/K)	Poisson's Ratio	Thermal Conductivity (W/(m·K))	Specific Heat Capacity (J/(kg·K))
Cu	8930	115	16.5	0.36	398	384.56
GaAs	5310	86	6.4	0.3	44	320
In	7290	11	31	0.45	82	233
Au	19,280	74	14.2	0.42	315	128.7
Polyimide	1300	3.1	25	0.34	0.15	1100

2.2. Anand Viscoplastic Principal Model

In this study, Anand's intrinsic model with multi-mechanism coupling properties was selected for mechanical characterization of indium solder under thermal loading for its viscoplastic behavior characteristics [23].

The core equations of the Anand model consist of the flow equation and the evolution equation:

The flow equation describes the relationship between strain rate and stress:

$$\varepsilon_{\mathrm{p}} = \mathrm{Asinh}\left(\frac{\xi\sigma}{s}\right)^{1/\mathrm{m}} \exp\left(-\frac{Q}{RT}\right) \tag{1}$$

where ε_{p} is the inelastic strain rate, A is a constant, Q is the activation energy, R is the gas constant, T is the absolute temperature, ξ is the stress factor, and m is the strain rate sensitivity factor. All temperature parameters used in subsequent calculations based on this formula have been uniformly converted to the SI unit Kelvin (K) to ensure its correct application.

The evolution equation describes the evolution of the deformation impedance S:

$$S = \left[\left|1 - \frac{S}{S^*}\right|^{\mathrm{a}} \mathrm{sign}\left(1 - \frac{S}{S^*}\right) h_0\right] \varepsilon_{\mathrm{p}} \tag{2}$$

$$S^* = \hat{S}\left[\frac{\varepsilon_p}{A} exp\left(\frac{Q}{RT}\right)\right]^n \tag{3}$$

where a and h_0 are the material strain hardening parameters, S^* is S the saturation value, and $\hat{S}$ is the coefficient of deformation resistance saturation value.

The nine parameters in the Anand model: A, Q/R, ξ, S', n, m, a, h_0 and initial deformation resistance S_0 can be obtained from uniaxial tensile experiments at several sets of different strain rates and temperatures. The Anand parameters for indium used in this paper are shown in Table 2.

Table 2. Parameters of Anand model for indium.

Parameters	Numerical Value
$Q/\mathrm{J{\cdot}mol^{-1}}$	78,124
ξ	49.97
m	0.300
$A/1{\cdot}\mathrm{s}^{-1}$	2.33×10^8
h_0/MPa	500
a	1
S_0/MPa	28.3
$\hat{S}$/MPa	28.3
n	0.005

2.3. Fatigue Life Prediction Model

2.3.1. Fatigue Life Prediction Model Under Thermal Loading

For the fatigue life prediction of failure-prone structures such as solder balls, solder joints, and SLs in chip packaging, experts and scholars have proposed a variety of models and methods. Among them, the modified Coffin–Manson model proposed by Engelmaier is one of the classic theories, which is widely used to predict the life of the SL under fatigue load based on the level of plastic deformation and by studying the stress level of the material, strain amplitude, and other factors.

The Coffin–Manson fatigue life prediction model was improved by Engelmaier et al. to be mathematically expressed as [24]

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma_p}{2\varepsilon_f}\right)^{\frac{1}{c}} \tag{4}$$

$$c = -0.442 - 6\times10^{-4}T + 1.74\times10^{-2}\times\ln(1+f) \tag{5}$$

$$\Delta\gamma_p = \sqrt{3}\Delta\varepsilon \tag{6}$$

where $\Delta\gamma_p$ is the equivalent shear strain amplitude, $\Delta\varepsilon$ is the equivalent plastic strain amplitude, c is the modified fatigue toughness index, f is the frequency of cycling, T is the temperature average, ε_f is the fatigue toughness coefficient, and its empirical value = 0.325.

2.3.2. Fatigue Life Prediction Model Under Random Vibration Loading

For the fatigue failure of welded layers induced by random vibration loads, the current life prediction methods mainly form two types of analytical frameworks in the frequency domain and time domain. In this study, an evaluation system based on the energy analysis method in the frequency domain is constructed, and the prediction system is constructed by integrating Manson's high perimeter fatigue theory, the three-band technique, and the linear fatigue damage accumulation criterion.

(1) Manson's high-frequency fatigue equation

Its core Manson–Coffin relational equation originated from a large number of fatigue test studies, and the mathematical characterization of the total fatigue life was finally derived by superimposing the plastic strain life curve with the elastic strain life curve [25]:

$$\frac{\Delta\varepsilon_t}{2} = \frac{\Delta\varepsilon_{el}}{2} + \frac{\Delta\varepsilon_{pl}}{2} = \frac{\sigma_f'}{E}\left(2N_f\right)^b + \varepsilon_f'\left(2N_f\right)^c \tag{7}$$

where $\Delta\varepsilon_t$ is for the total strain amplitude; $\Delta\varepsilon_{el}$ is for the elastic strain amplitude; $\Delta\varepsilon_{pl}$ is for the plastic strain amplitude; σ_f' is for the fatigue strength coefficient; E is for the material elastic modulus; b is for the fatigue strength index; ε_f' is for the fatigue plasticity coefficient; and c is for the fatigue plasticity index.

The generalized slopes of the elastic and plastic terms are -0.12 and -0.6, respectively, which can be obtained by substituting the two terms into the following equation:

$$\Delta\varepsilon_t = 3.5\frac{\sigma_u}{E}N_f^{-0.12} + \varepsilon_f^{0.6}N_f^{-0.6} \tag{8}$$

where σ_u is the tensile ultimate strength of the material.

When elastic strain occurs, Manson's empirical equation for high week fatigue is

$$\Delta\varepsilon_t = \Delta\varepsilon_{el} = 3.5\frac{\sigma_u}{E}N_f^{-0.12} \tag{9}$$

$$\varepsilon = \frac{\Delta \varepsilon_t}{2} = 3.5\frac{\sigma_u}{2E}N_f^{-0.12} \quad (10)$$

The SL material is indium, taking its modulus of elasticity at room temperature as 13 GP and its tensile ultimate strength as 4.5 MPa, and the empirical formula for Manson's high week fatigue is

$$\varepsilon = 0.00061N_f^{-0.12} \quad (11)$$

(2) Three-band technology

The reliability of the three-band technique as an effective method for stochastic vibration fatigue analysis has been verified by a large amount of experimental data. The technique is based on the assumption that the vibration acceleration obeys a Gaussian distribution, where the vertical axis represents the probability density and the horizontal axis characterizes the ratio of the instantaneous acceleration to the Root Mean Square (RMS) acceleration response value. The probability distribution of the vibration response is characterized by the typical three zones: The ±1σ interval covers 68.27% probability, the ±2σ interval accumulates to 95% probability, and the ±3σ interval reaches the highest probability share of 99%.

The fatigue damage index accumulated by the object in random vibration conditions during the next hour can be calculated from Equations (12)–(14).

$$n_1 = N_0^+ T_v(3600s/h)(0.6831) \quad (12)$$

$$n_2 = N_0^+ T_v(3600s/h)(0.2710) \quad (13)$$

$$n_3 = N_0^+ T_v(3600s/h)(0.0433) \quad (14)$$

The probability of an instantaneous acceleration occurring is 99.7%, which tends to be close to 1. Therefore, the maximum acceleration level is usually considered to be horizontal in engineering practice.

Expression (15) is for the number of positive zero passes (N_0^+) of the displacement [26]:

$$N_0^+ = \frac{1}{2\pi}\left[\sum \frac{P_i f_i Q_i^2}{\Omega_i^2} / \sum \frac{P_i f_i Q_i^2}{\Omega_i^4}\right]^{\frac{1}{2}} \quad (15)$$

(3) Fatigue damage accumulation theory

When the material is subjected to alternating stresses exceeding its fatigue threshold, each load cycle triggers a progressive accumulation of microstructural damage. This damage mechanism is irreversible, and its cumulative effect will lead to material failure when it reaches the critical threshold, which constitutes the core mechanism of fatigue damage evolution theory. At present, Miner's linear cumulative damage criterion is commonly used as the classical model in engineering practice, which realizes the life prediction through the linear superposition of damage degrees.

For random vibration, the time-varying amplitude loads on the structure need to be handled by the load spectrum discretization method. The three-band hierarchical technique shown in Figure 4 discretizes the continuous random vibration signal into three characteristic load intervals based on the principle of stress amplitude hierarchy, and this quantitative method provides an effective engineering solution path for fatigue assessment of variable amplitude loads.

$$D_v = \sum (n_i/N_i)(i = 1,2,3) \quad (16)$$

$$D_v = \frac{n_1}{N_1} + \frac{n_2}{N_2} + \frac{n_3}{N_3} \quad (17)$$

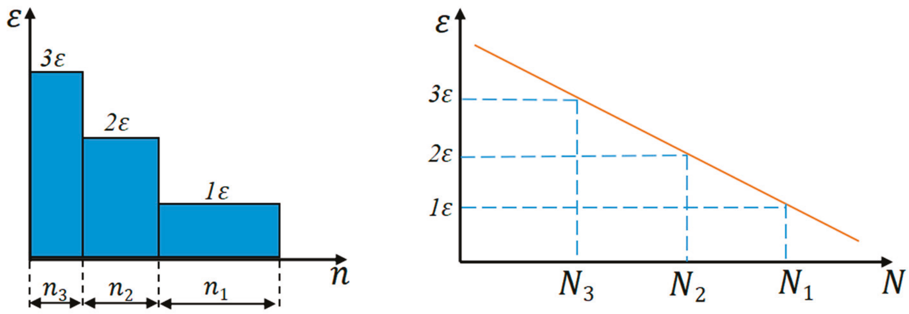


Figure 4. Random loads of different magnitudes.

2.3.3. Fatigue Life Prediction Model Under Thermal–Vibration Coupled Loading

During the entire life cycle of an HPLD, the compound environmental stresses during transportation and use can cause critical interface failures. Especially in aerospace and military high-reliability application scenarios, multi-physical field coupling effects (mechanical vibration and thermal cycle synergy) in the SL region will induce a synergistic crack expansion effect. The composite strain energy generated by such multi-axial stresses significantly shortens the fatigue life cycle of the SL through the damage accumulation mechanism, which ultimately leads to the loss of structural integrity of the SL. Figure 5 shows a schematic diagram of the stresses and strains generated by the combined action of random vibration and thermal cycling on the SL.

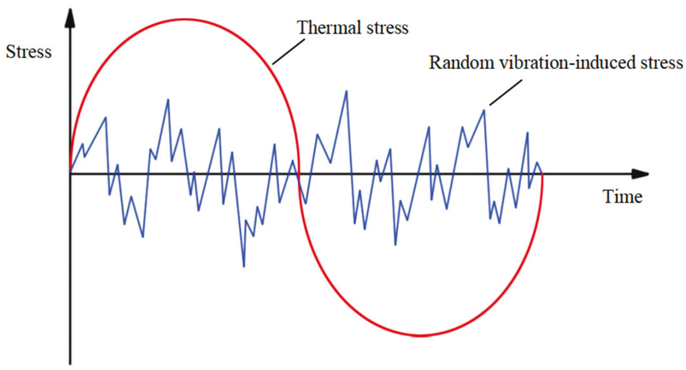


Figure 5. Stress diagram caused by the combination of thermal cycling and random vibration.

In this multi-field coupling environment, the composite load effect can be quantitatively modeled based on the principle of linear damage superposition. The damage coupling equation established using the Miner criterion can transform the nonlinear damage process triggered by mechanical vibration and thermal cyclic loading into linearly superimposable damage coefficients so as to construct a life prediction model of the SL under the action of multiple physical fields.

$$D_{total} = D_{th} + D_v = \frac{n_{th}}{N_{th}} + \frac{n_v}{N_v} = n_{th}\left(\frac{f_v/f_{th}}{N_v} + \frac{1}{N_{th}}\right) \quad (18)$$

where D_v is the fatigue damage factor caused by vibration fatigue; D_{th} is the fatigue damage factor caused by thermal cycling fatigue; n_{th} is the actual thermal cycling cycles; f_v is the structural vibration frequency; and f_{th} is the thermal cycling frequency.

Under the composite loading environment, the random vibration will always have the process of converting from the frequency domain to the time domain and then coupling with the thermal cycle. Therefore, when the thermal vibration coupling is considered comprehensively, the energy dissipation path of the SL under the action of nonlinear damage mechanism can be obtained, and its theoretical solution is shown in the engineered life assessment model shown in Equation (19).

$$N_f = \frac{D}{\left(\frac{f_v/f_{th}}{N_v} + \frac{1}{N_{th}}\right)} \tag{19}$$

where N_f is equivalent to the number of thermal fatigue cycles.

3. Simulation Evaluation of the SL Reliability Under Thermal Cyclic Loading

3.1. Analyzing Processes

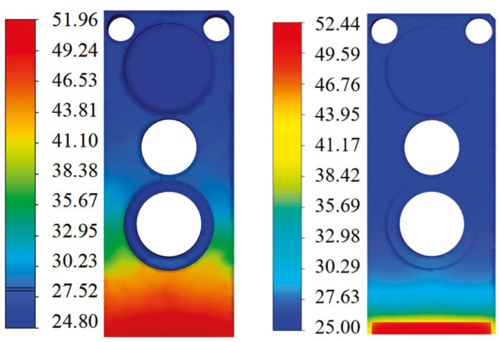
Finite element software (ANSYS2023R1) was applied to establish the three-dimensional model of the HPLD. In order to reduce the amount of operation and improve the speed of operation, without affecting the simulation results, the HPLD was reasonably simplified, only retaining the structures such as the bar, the SL, the MCHS, etc. and ignoring the other structures that have a small impact on heat dissipation. The mapping method was used to divide the mesh, and the mesh encryption was carried out for the key areas of concern such as the bar and the interconnection interface below, with a mesh size of 1×10^{-4} m, and the mesh size of the MCHS part of the mesh is 5×10^{-4} m. Combined with the space environment, the conditions were set up, and the microchannel water-cooled encapsulation of the MCHS was set to be fixed at the bolt holes on the microchannel, and the temperature was cyclically loaded to the whole model.

The grid sensitivity was verified. When the number of grids was 17,785, the error between the result and the number of grids was less than 1%. It is proven that the selected grid size has good accuracy and a fast running speed, as shown in Table 3.

Table 3. Grid sensitivity analysis.

Mesh Count	Maximum Stress (MPa)	Maximum Strain (mm)	Maximum Stress Error	Maximum Strain Error
5142	8.0845	0.00073495	9.52%	9.61%
10,689	8.7305	0.0007949	2.29%	3.12%
17,785	9.0162	0.00082052	0.91%	0.92%
26,385	8.935	0.00081309		

The thermal simulation results before and after the model simplification are shown in Figures 6a and 6b, respectively. It can be seen that the difference in the maximum temperature between the two is 0.48 °C, which has a relatively small influence on the results.



(**a**)the initial model (**b**)the simplified model

Figure 6. Temperature distribution cloud diagrams before and after model simplification.

Based on the NASA Goddard Space Flight Center issued by the space flight environment with the HPLD array qualification guide [26] and MIL-STD-883 standard [27] to develop the thermal cycle load, the temperature range is 218.15 K to 358.15 K. The initial temperature was set to 298.15 K, the rate of change in the temperature was 25 K/min, the lowest temperature and the highest temperature were maintained for 10 min, the cycle was 31.2 min, the model 10 cycles were carried out, and the temperature loading was carried out in accordance with Figure 7.

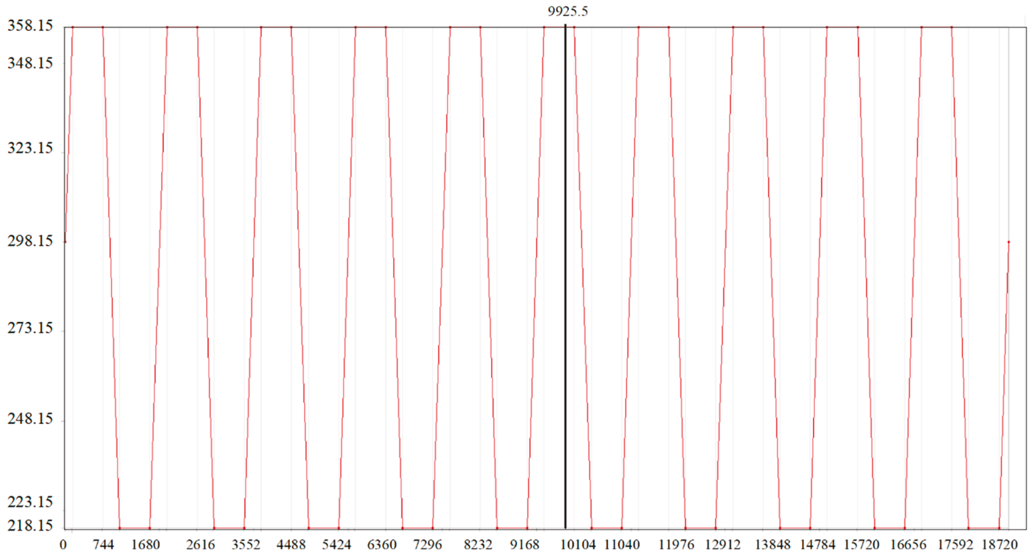


Figure 7. Temperature cycling load.

3.2. Results and Analysis

Comparison of the performance of the SL of the HPLD using the MCHS package before and after optimization is as follows: The strain distribution cloud (Figures 8a and 9a) is shown, and the stress distribution cloud (Figures 8b and 9b) is shown. Before optimization, the maximum plastic strain is concentrated in the four corners of the SL, in which node 4505 is confirmed as the failure hazard point by thermal cycle analysis, and the corresponding maximum stress value reaches 9.016 MPa; after optimization, the hazardous area is shifted to the edge of the SL, and node 4518 becomes the new strain concentration point, and the maximum stress value is reduced to 8.40 MPa. The data show that the maximum stress in the SL is reduced to 0.621 MPa after optimization of the structure. The data shows that the maximum stress in the SL is reduced by 0.621 MPa after structural optimization, which effectively improves the reliability of the package.

Figure 8. Equivalent stress and strain distribution cloud diagram of the SL before optimization.

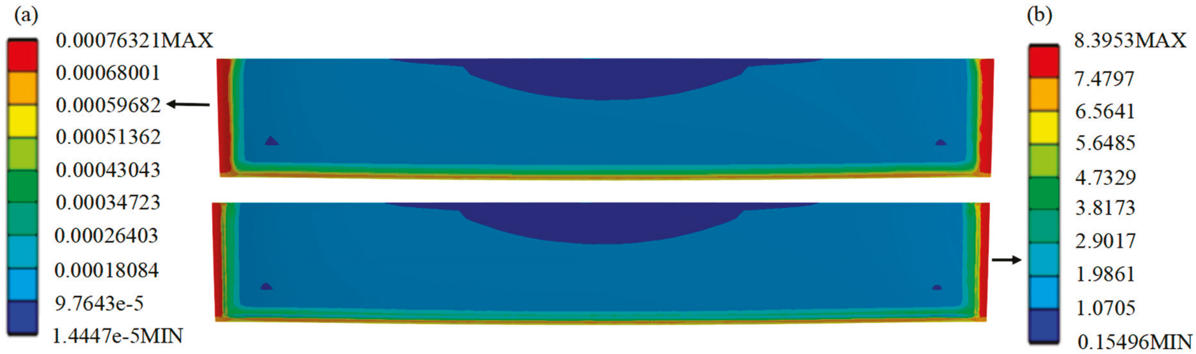


Figure 9. Equivalent stress and strain distribution cloud diagram of the SL after optimization.

During the thermal cyclic loading process, the multi-axial stress coupling effect of the SL is triggered by the gradient distribution of the thermal expansion coefficients of the SL, the bar, the MCHS, the insulating film, and the copper foil. For the numerical analysis of this complex stress field, the Von Mises yield criterion becomes the preferred solution.

In the Von Mises yield criterion [28], the equivalent stress is described in terms of components of the stress tensor as

$$\sigma_s = \sqrt{\frac{1}{2}\left[(\sigma_1-\sigma_2)^2+(\sigma_2-\sigma_3)^2+(\sigma_3-\sigma_1)^2\right]} \tag{20}$$

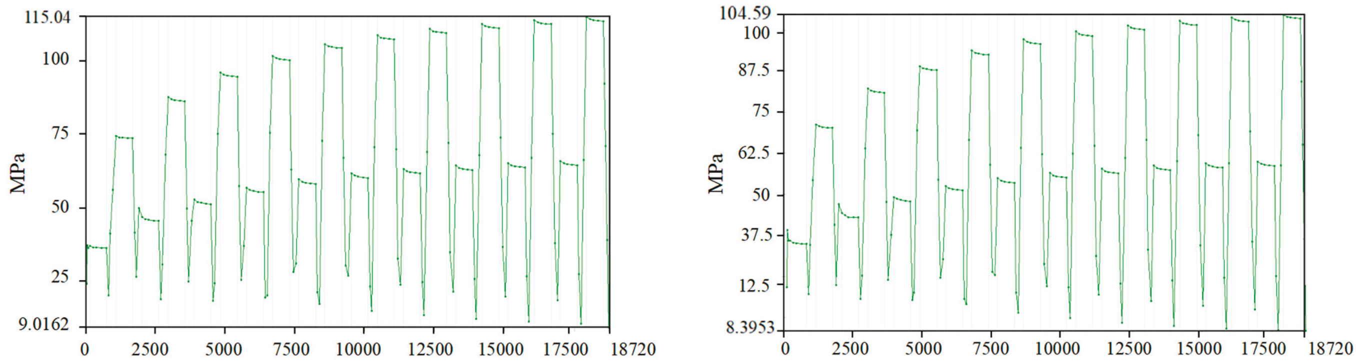
According to the Von Mises criterion, the specific energy of shape change, when flow occurs under unidirectional stretching, is calculated by making $\sigma_1 = \sigma_s$, $\sigma_2 = \sigma_3 = 0$, and the shear yield strength of indium K = 10 MPa:

$$\sigma_s = \sqrt{\frac{1}{2}\left[(\sigma_1-\sigma_2)^2+(\sigma_2-\sigma_3)^2+(\sigma_3-\sigma_1)^2\right]} = \sqrt{3}K = 1.732 \times 10 = 17.32 \text{ MPa}$$

The Von Mises stress at the point of maximum stress is much smaller than the equivalent stress so that thermal cyclic loading does not have a destructive effect on the SL.

For the HPLD using optimized pre- and post-MCHS packages, the hazardous areas of stress and strain on the SL are located at the edges of the SL, showing a diffusion from the middle to both sides. The SL is characterized by a significant anisotropic stress distribution: The axial stress (Z-direction) shows a quasi-uniform distribution, while a gradient stress field is formed in the transverse direction (X-direction). Based on the coupling of the stress field characteristics in the symmetry axis region and the thermal deformation mechanism, a significant stress gradient distribution is observed inside the SL: The equivalent stresses in opposite directions in the neighboring symmetry axis cancel each other out to form a low-stress region; with the increase in the distance from the axis, an isotropic stress superposition phenomenon is gradually observed at the edge of the SL, with an exponential decay in the canceling efficiency. Under thermal cyclic loading, the in-plane shear deformation caused by the difference in thermal expansion coefficients between the bar and the SL material shows a non-uniform distribution—the edge region produces significant warpage strain concentration due to the weak geometric constraints, while the center region is subjected to bi-directional constraints for relatively coordinated deformation. These reasons lead to an increasing trend of stress–strain in the SL along the X-axis from the center to both sides. Based on this stress field evolution law, cracks preferentially sprout in the high-stress singularity region and then expand along the direction of the maximum principal stress gradient (in the cavity length direction), eventually forming a penetrating failure path.

Figure 10 shows the equivalent stress plots of the SL of the HPLD with the MCHS package before and after optimization, respectively. As seen from the data curves, the stress change of the SL shows a synchronous fluctuation law with the temperature cycle. When the temperature remains stable, a small release of internal material stress occurs; while in the temperature rise and fall stage, the stress level all climbs up, and the stress increase generated by the cooling process is more significant than that of heating. This temperature–stress linkage reveals the sensitive response of the material to changes in the thermal environment.



(**a**) (**b**)

Figure 10. Equivalent stress curve diagram of the SL. (**a**) Packaging before optimization and (**b**) packaging after optimization.

3.3. Fatigue Life Prediction Under Thermal Loading of the SL

For the entire HPLD's SL, the edge region of the SL is the most likely to fail; through the above analysis, it can be seen that in the case of thermal cyclic loading, the deformation of the SL is mainly due to the mismatch of the coefficients of thermal expansion between the materials caused by plastic deformation. Therefore, the life prediction model in this paper is based on plastic deformation to calculate the fatigue life of the SL. After the simulation solution is stabilized, the value of the equivalent plastic strain range in the hazardous region of the SL is the difference in the maximum value of the equivalent plastic strain.

The equivalent plastic shear strain range of the HPLD's SL encapsulated before optimization is

$$\Delta\gamma_p = \sqrt{3}\Delta\varepsilon = 0.009927$$

Substituting the data into the formula gives the following:

$$T = \frac{-55 + 85}{2} = 15$$

$$f = 24 \times 60 \times 60 \div 18720 \approx 4.6$$

$$c = -0.442 - 6 \times 10^{-4} \times 15 + 1.74 \times 10^{-2} \times \ln(1 + 4.6) = -0.42$$

$$N_f = 2851$$

Similarly, the life of the optimized packaged HPLD's SL under thermal cyclic loading conditions is 5730 cycles.

The thermal fatigue life of the SL before and after optimization is 2851 cycles and 5730 cycles, respectively. The thermal fatigue life prediction shows that the life of the optimized packaged HPLD's SL is twice as long as the life of the original packaged HPLD's SL. The optimized and improved packaged HPLD's SL life has been significantly improved, which can better cope with the harsh service environment and ensure the thermal reliability of HPLS in the space environment.

4. Simulation Evaluation of the SL Reliability Under Vibration Loading

4.1. Analyzing Processes

When performing modal analysis, continuing to use only the HPLD for vibration analysis will result in the loss of modes and a large error in the subsequent calculations, so this subsection uses the LD module for the simulation and analysis; the model is shown in Figure 11. The HPLD is located inside the module, and the laser is consistent with the above. The LD module shell material is 6061-T6 aluminum alloy, with dimensions of 80 mm × 40.5 mm × 13 mm, and the physical parameters are shown in Table 4.

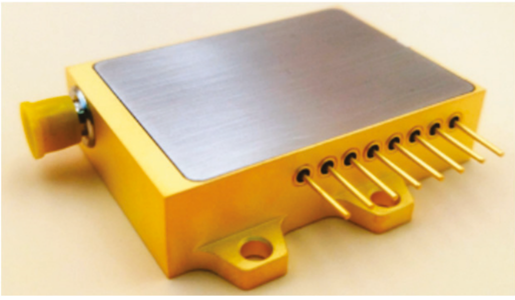


Figure 11. LD module.

Table 4. Material parameters of the LD module housing.

Material	Density/kg·m^{-3}	Young's Modulus/GPa	Poisson's Ratio	Shear Modulus/GPa	Bulk Modulus/GPa
6061-T6	2713	69.04	0.33	25.955	67.686

4.2. Results and Analysis

(1) Modal analysis

According to the vibration theory, the modal study of the LD module is carried out by using Subspace for modal analysis. Constraining the degrees of freedom of the nodes attached to the bolt holes, the first six orders of modal frequencies are shown in Table 5, and the modal analysis of the LD module is carried out to obtain the first six orders of vibration patterns of the LD module before and after the optimization, as shown in Figure 12A,B, and the 1st–6th orders of modal patterns are shown in Figure 12a–f, respectively.

Table 5. First six natural frequency modes of the LD module.

Order/Hz	1st	2nd	3rd	4th	5th	6th
Frequency before optimization	2261.2	3271.4	3917.5	4984.7	5200.6	5587.1
Frequency after optimization	2265.3	3271.5	3916.1	4984.7	5199.7	5600.1

The intrinsic frequency is an inherent property of the structure itself, independent of external excitation. The intrinsic frequency of the structure obtained from the modal analysis can avoid the resonance of the structure during the design process. Comparison of Figure 12A,B shows that the vibration pattern before and after optimization is almost the same, which indicates that the optimization improvement will not adversely affect the intrinsic frequency of the LD.

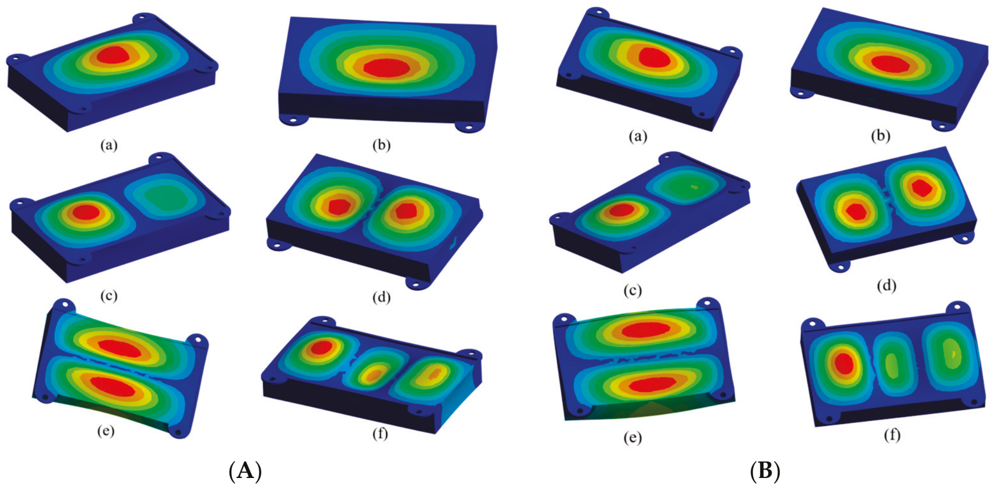


Figure 12. Mode shapes of the first six vibration modes of the LD module. (**A**) Before optimization and (**B**) after optimization.

(2) Random vibration analysis

In the study of structural dynamics, the spectral analysis method can effectively solve the dynamic response problem under broadband excitation by combining the structural modal characteristics with the excitation spectral features. The random vibration excitation to which the LD module is subjected is an acceleration excitation, which is loaded through the bolted joints in the finite element model. According to the test guidelines published by the Goddard Space Flight Center, the power spectral density analysis function is used to input the acceleration power spectral density (PSD) as shown in Table 6, and each of the three directions of X, Y, and Z axes need to be tested.

Table 6. Acceleration power spectral density.

Frequency/Hz	PSD
20	0.052 g^2/Hz
20–50	+6 dB/octave
50–800	0.32 g^2/Hz
800–2000	−6 dB/octave
2000	0.052 g^2/Hz
Overall	20.0 grms

Through the analysis and solution of random vibration, the stress and strain cloud diagrams under the HPLD as a whole and the SL 3σ before optimization are shown in Figure 13, Figure 14, and Figure 15, respectively, in which the red box selects the enlargement for the stress–strain distribution cloud diagram of the SL, and the yellow box selects the enlargement for the HPLD at the maximum stress. As a result, the overall module equivalent force of the LD is prominent in the HPLD and module shell contact corners, easy to occur stress concentration; acceleration excitation is applied in the Z-axis direction, resulting in the equivalent force being much larger than the other two axes and its equivalent force value of 13.076 MPa. Analyzing the stress–strain distribution of the SL, the maximum stress of the SL is located in the SL at the edge of the SL, and its equivalent force under the 3σ are, respectively, 0.0365 MPa, 0.0167 MPa, and 0.652 MPa, and the acceleration excitation is applied in the direction of the Z-axis, which produces the equivalent stresses that are also much larger than the other two axes but much smaller than its yield limit. Only elastic strain occurs in the SL under this random vibration load, and its fatigue mode is high-cycle fatigue.

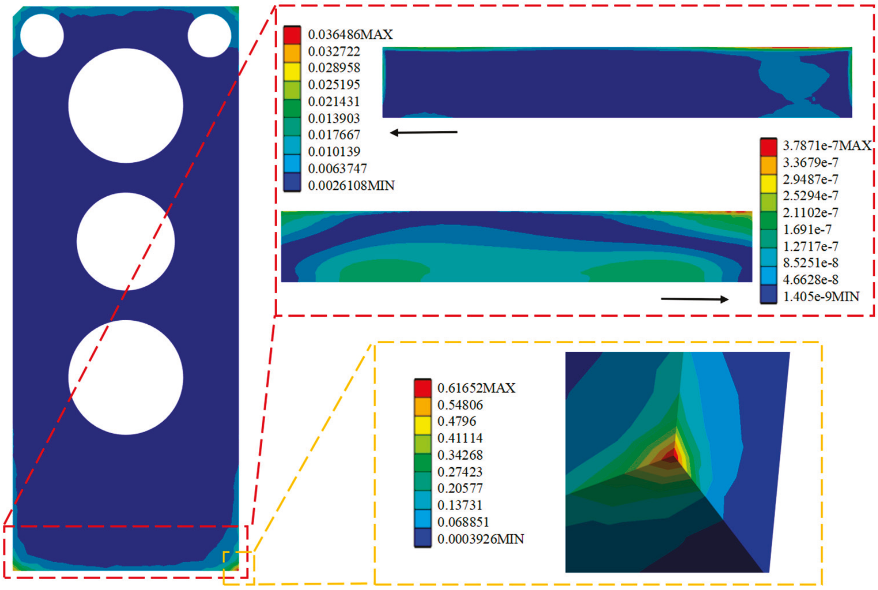


Figure 13. Apply acceleration excitation along the X-axis direction to the model before optimization.

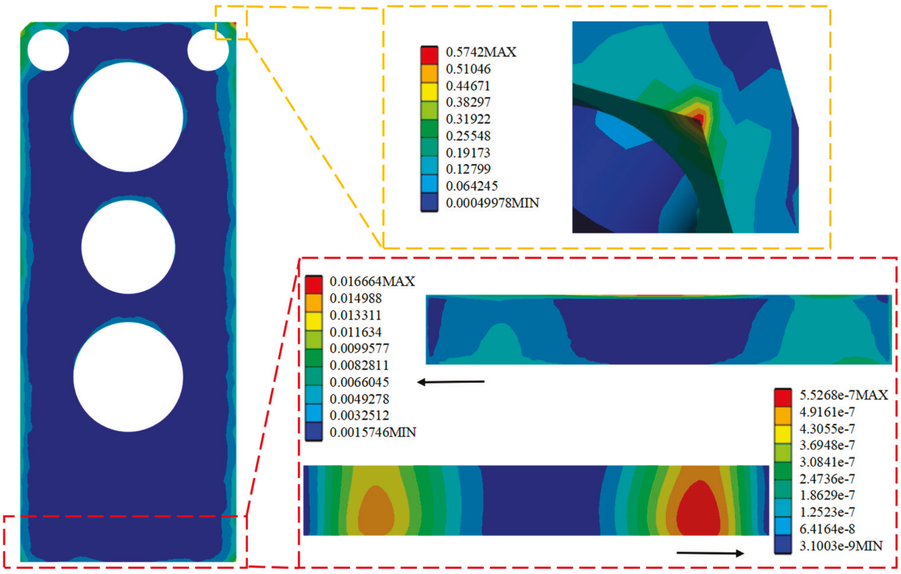


Figure 14. Apply acceleration excitation along the Y-axis direction to the model before optimization.

By analyzing and solving the random vibration, the optimized stress and strain maps under the HPLD as a whole and the SL 3σ are shown in Figure 16, Figure 17, and Figure 18, respectively, in which the red box selection zooms in on the stress–strain distribution map of the SL, respectively, and the yellow box selection zooms in on the maximum stress of the HPLD. It is concluded that the overall module equivalent stress of the LD occurs prominently at the contact corner of the HPLD and the module housing. Acceleration excitation is applied to the Z-axis direction, the equivalent force is much larger than the other two axes, and its equivalent force value is 14.135 MPa. Analyzing the stress–strain distribution of the SL, the maximum stress of the SL is located at the edge of the SL, and the equivalent force under its 3 is 0.0413 MPa, 0.0165 MPa, and 0.782 MPa, respectively, and the equivalent force under acceleration excitation is applied to the Z-axis direction, and the equivalent force is the same as that in the Z-axis direction. The equivalent force generated is also much larger than the other two axes but much smaller than its yield limit. Only elastic strain occurs in the SL under this random vibration load, and its fatigue mode is high-cycle fatigue.

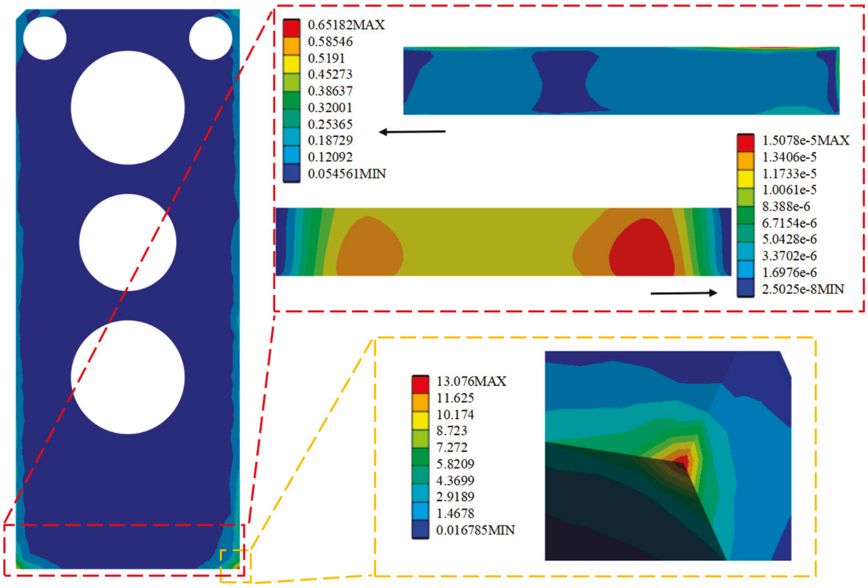


Figure 15. Apply acceleration excitation along the Z-axis direction to the model before optimization.

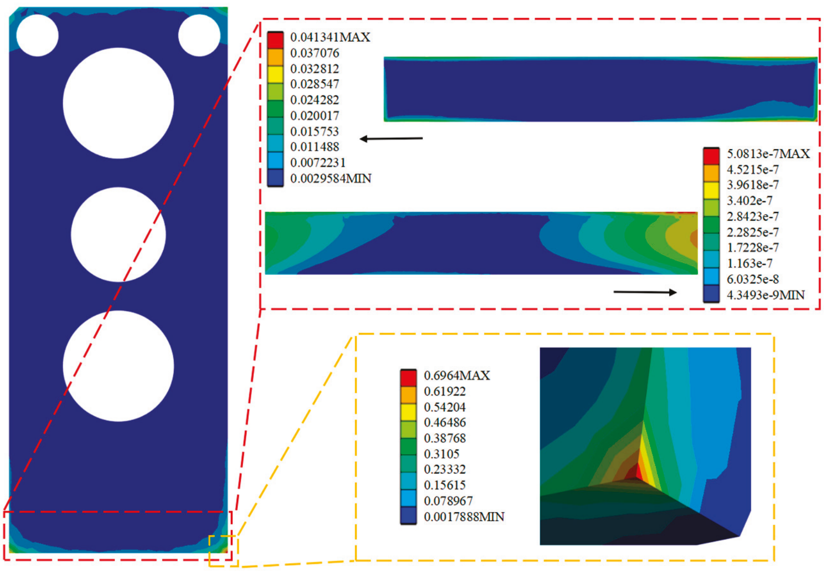


Figure 16. Apply acceleration excitation along the X-axis direction to the optimized model.

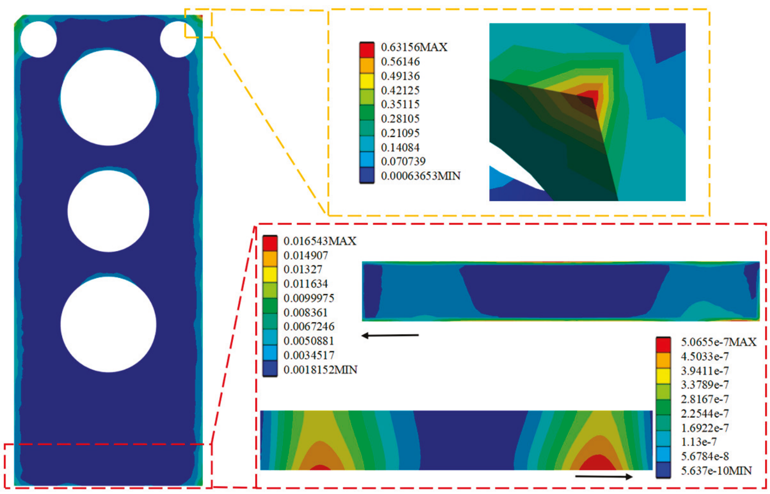


Figure 17. Apply acceleration excitation along the Y-axis direction to the optimized model.

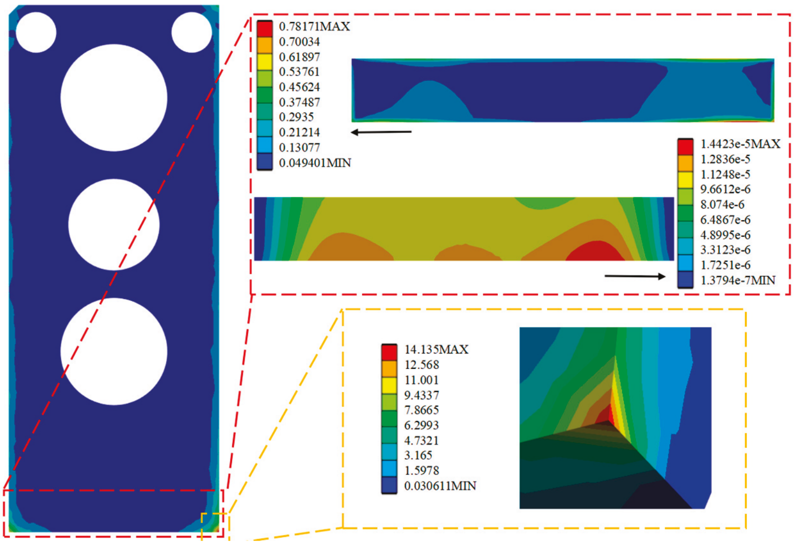


Figure 18. Apply acceleration excitation along the Z-axis direction to the optimized model.

4.3. Fatigue Life Prediction Under Vibratory Loading of the SL

The strain values of the SL before and after optimization can be obtained from the finite element strain analysis results, respectively. Under the conditions of 1σ, 2σ, and 3σ strain levels, the corresponding number of fatigue cycles can be calculated as shown in Tables 7 and 8, where X, Y, and Z indicate the acceleration excitation applied to the X, Y, and Z axes directions, respectively.

Table 7. Pre-optimization of the laser SL fatigue cycles.

	N_1	N_2	N_3
X	5.02×10^{30}	1.56×10^{28}	5.31×10^{26}
Y	2.15×10^{29}	6.68×10^{26}	2.28×10^{25}
Z	2.33×10^{17}	7.23×10^{14}	2.46×10^{13}

Table 8. Post-optimization of the laser SL fatigue cycles.

	N_1	N_2	N_3
X	4.34×10^{29}	1.35×10^{27}	4.58×10^{25}
Y	4.45×10^{29}	1.38×10^{27}	4.70×10^{25}
Z	3.38×10^{17}	1.05×10^{15}	3.57×10^{13}

Calculate the cumulative number of vibration cycles at each strain level before and after optimization, respectively:

(1) Before optimization

$$n_1 = 2261.2 \times 3600 \times 0.6831 \approx 5560652.59$$

$$n_2 = 2261.2 \times 3600 \times 0.2710 \approx 2206026.72$$

$$n_3 = 2261.2 \times 3600 \times 0.0433 \approx 352475.856$$

(2) After optimization

$$n_1 = 2265.3 \times 3600 \times 0.6831 \approx 5570735.15$$

$$n_2 = 2265.3 \times 3600 \times 0.2710 \approx 2210026.68$$

$$n_3 = 2265.3 \times 3600 \times 0.0433 \approx 353114.964$$

The fatigue life of the SL under random vibration conditions is predicted as follows:

$$T_v = 1/D_v = 1/\left(\frac{n_1}{N_1} + \frac{n_2}{N_2} + \frac{n_3}{N_3}\right)$$

The solution is obtained: T_v = 1.24 $\times$ 10^{21} h.

Similarly, the predicted values of fatigue life under other conditions T_v is shown in Table 9.

Table 9. Pre- and post-optimization of the SL fatigue life.

	Pre-Optimization	**Post-Optimization**
X	1.24×10^{21}	1.07×10^{20}
Y	5.31×10^{19}	1.10×10^{20}
Z	5.75×10^{7}	8.31×10^{7}

As can be seen from Table 8, the predicted lifetime of the SL of the HPLD under random vibration load in the Z-axis direction is much smaller than that in the other two axes. The life prediction study of the HPLD under random vibration load should focus on the Z-axis direction, and the life of the sSL under random vibration load applied in the Z-axis direction should be taken as the life of the SL under random vibration load. As a result, the lifetimes of the SL under random vibration loads in the package form before and after the use of optimization are 5.75 $\times$ 10^7 and 8.31 $\times$ 10^7 h, respectively, which are in accordance with the specified requirements.

5. Simulation Evaluation of the SL Reliability Under Thermal Vibration Coupled Loading

From the above, it can be seen that the thermal fatigue life of the SL before the optimization is 2851 cycles, and the individual thermal cycle period is 18,720 s. Under the 1 h composite loading (thermal–vibration coupling) condition, the thermal cycle fatigue damage factor can be deduced as

$$D_{th} = \frac{1}{2851 \times 18720/3600} = 0.00006745$$

The total damage factor is calculated by considering both thermal cycling fatigue and random vibration fatigue:

$$D_{total} = D_{th} + D_v = 0.00006745 + 0.0000000174 = 0.00006747$$

The fatigue life of the SL under thermal vibration load loading is

$$T_{total} = \frac{1}{D_{total}} = 14821 \text{ h}$$

Similarly, the fatigue life of the optimized SL under thermal vibratory loading is 29,786 h.

In the study of the cumulative effect of damage, comparing the damage factor of the SL under thermal cyclic loading and under random vibration loading, the thermal fatigue damage factor is significantly higher than the vibration damage. It can be seen that the fatigue life of the HPLD's SL under thermal vibration load is mainly affected by the thermal cyclic load, and the life decay mainly originates from the microcrack expansion mechanism dominated by thermal cycling.

6. Conclusions

In this paper, the reliability study of thermal cycling, random vibration, and thermal vibration coupling is carried out for the SL of the HPLD, and the finite element model of the HPLD is established and solved. Under the two loading conditions of thermal cycling and random vibration, the fatigue failure of the SL is studied, and the maximum equivalent stress and strain distribution at this position are analyzed, and the fatigue life of the SL is predicted when the thermal vibration coupling load is applied together, and the main conclusions are as follows:

(1) When the thermal cycle load is loaded, the Anand viscoplastic intrinsic model is used to describe the mechanical properties of the SL, and it is found by observing the graphs that the dangerous areas of stress and strain on the SL before and after the optimization are located in the edge area of the SL; the difference in stress–strain in the X-axis direction of the SL is larger than that in the direction of the other axes; and the failure of the SL will be prioritized from the edge of the SL along the direction of the length of the cavity.

(2) The first six orders of vibration patterns and the intrinsic frequency of the LD module are obtained through modal analysis, and then the acceleration PSD load is applied to the LD module for random vibration analysis. The acceleration excitation is applied in the Z-axis direction, and the equivalent stress produced by the SL before and after optimization is much larger than that applied to the other two axes, but numerically, it is much smaller than its yield strength, and the SL only undergoes elastic strain and high circumferential fatigue under this random vibration load.

(3) The fatigue life prediction model under thermal cycling obtains the fatigue life of the hazardous area of the SL before and after optimization to be 2851 cycles and 5730 cycles, respectively; the fatigue life prediction model under random vibration load obtains the fatigue life of the hazardous area of the SL to be 5.75×10^7 h and 8.31×10^7 h, respectively; the fatigue life of the superposition of the damage of thermal vibration load obtains the fatigue life of the SL to be 14,821 h and 29,786 h, respectively. 29,786 h, and the damage under thermal cyclic loading is dominant.

The lifetime of the SL in the optimized package structure is greater than the lifetime of the SL before optimization, which is mainly due to the increase in fatigue lifetime of the SL during thermal cyclic load loading. This result is inextricably linked to the pre-optimization of moving the bar back to improve the heat dissipation path and increase the heat dissipation efficiency.

Electronic products working in the space environment are subjected to more loads than just thermal cycling and random vibration, and although other loads have a lower chance of causing the failure of electronic products, they cannot be ignored. Radiation, impact, and other factors also affect the life of electronic products in the space environment, so the same needs to study and analyze these factors. Restricted by the experimental conditions and other restrictions, this paper is carried out through the finite element simulation software, and in order to reduce the calculation time, the LD model has been partially simplified, such as wanting to make the results closer to the actual situation, the need for more accurate and detailed modeling simulation and experimental verification. This paper focused solely on the analysis of conventional indium solder technology. Future research should prioritize investigating processing techniques for solder layers with varying thicknesses and different solder materials, such as hard solders (e.g., Au-Sn). The aim is to reduce stress while ensuring longevity, thereby providing additional options for the application of high-power diode lasers in extreme environments. In the actual thermal cycling and random vibration environment, thermal cycling and random vibration will interact with each other to accelerate the process of the SL failure, and the simple use of linear superposition is not a true and accurate prediction of the fatigue failure of the SL. How to establish a fatigue life model that can predict the fatigue life of the SL is the focus of subsequent research.

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