electronics

Volume 2

Applications of Power Electronics

Edited by
Frede Blaabjerg, Tomislav Dragičević and Pooya Davari

Printed Edition of the Special Issue Published in *Electronics*

www.mdpi.com/journal/electronics

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Frede Blaabjerg
Tomislav Dragičević
Pooya Davari

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Special Issue Editors
Frede Blaabjerg
Aalborg University
Denmark

Tomislav Dragičević
Aalborg University
Denmark

Pooya Davari
Aalborg University
Denmark

Editorial Office
MDPI
St. Alban-Anlage 66
4052 Basel, Switzerland

This is a reprint of articles from the Special Issue published online in the open access journal *Electronics* (ISSN 2079-9292) from 2018 to 2019 (available at: https://www.mdpi.com/journal/electronics/special_issues/appli_power_elec)

For citation purposes, cite each article independently as indicated on the article page online and as indicated below:

LastName, A.A.; LastName, B.B.; LastName, C.C. Article Title. *Journal Name* **Year**, *Article Number*, Page Range.

Volume 2
ISBN 978-3-03921-020-6 (Pbk)
ISBN 978-3-03921-021-3 (PDF)

Volume 1-2
ISBN 978-3-03921-148-7 (Pbk)
ISBN 978-3-03921-149-4 (PDF)

Cover image courtesy of Frede Blaabjerg.

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About the Special Issue Editors

Frede Blaabjerg (professor) worked with ABB-Scandia, Randers, Denmark, from 1987 to 1988. He obtained his Ph.D. in electrical engineering at Aalborg University in 1995. He became an assistant professor in 1992, an associate professor in 1996, and a full professor of power electronics and drives in 1998. In 2017, he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania and Tallinn Technical University (TTU) in Estonia. His current research interests include power electronics and its applications, such as in wind turbines, PV systems, reliability, harmonics, and adjustable-speed drives. He has published more than 600 journal papers in the field of power electronics and its applications. He is the co-author of four monographs and editor of ten books in power electronics and its applications. He has received 29 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award in 2014, and the Villum Kann Rasmussen Research Award in 2014. He was the Editor-in-Chief of *IEEE Transactions on Power Electronics* from 2006 to 2012. He was a distinguished lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011, as well as from 2017 to 2018. In 2018, he became the president elect of the IEEE Power Electronics Society. He serves as vice-president of the Danish Academy of Technical Sciences. He was nominated in 2014, 2015, 2016, and 2017 by Thomson Reuters as one of the world's 250 most cited researchers in engineering.

Tomislav Dragičević (associate professor) received his M.Sc. degree in 2009 and his industrial Ph.D. degree in electrical engineering in 2013 from the Faculty of Electrical Engineering and Computing, University of Zagreb, Zagreb, Croatia. From 2013 to 2016, he was a postdoctoral research associate at Aalborg University, Aalborg, Denmark. Since March 2016, he has been an associate professor at Aalborg University. He was a visiting guest professor at Nottingham University, Nottingham, U.K., during the spring/summer of 2018. His principal fields of interest include overall system design of autonomous and grid-connected dc and ac microgrids and application of advanced modeling and control concepts to power electronic systems. Dr. Tomislav has authored and coauthored more than 140 technical papers (more than 55 of them are published in international journals, mostly *IEEE Transactions*) in his domain of interest, eight book chapters, and a book. His research interests include overall system design of autonomous and grid-connected dc and ac microgrids and application of advanced modeling and control concepts to power electronic systems. Dr. Dragičević is the recipient of the Končar Prize for the best industrial Ph.D. thesis in Croatia and the Robert Mayer Energy Conservation Award. He serves as an associate editor for the *IEEE Transactions on Industrial Electronics* and for the *Journal of Power Electronics*.

Pooya Davari (associate professor) received B.Sc. and M.Sc. degrees in electronic engineering from the University of Mazandaran, Babolsar, Iran, in 2004 and 2008, respectively, and a Ph.D. degree in power electronics from Queensland University of Technology (QUT), Brisbane, Australia, in 2013. From 2005 to 2010, he was involved in several electronics and power electronics projects as a development engineer. From 2010 to 2014, he investigated and developed high-power high-voltage power electronic systems for multidisciplinary projects, such as ultrasound application, exhaust gas emission reduction, and tissue-materials sterilization. From 2013 to 2014, he was a lecturer with QUT. He joined the Department of Energy Technology, Aalborg University, Aalborg, Denmark, in 2014, as a

postdoctoral researcher and he is currently an associate professor there. His current research interests include EMI/EMC in power electronics, WBG-based power converters, active frontend rectifiers, harmonic mitigation in adjustable-speed drives, and pulsed power applications. Dr. Davari received a research grant from the Danish Council of Independent Research in 2016.

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Article

Online Optimal Switching Frequency Selection for Grid-Connected Voltage Source Inverters

Saher Albatran [1,*], Issam A. Smadi [1], Hamzeh J. Ahmad [1] and Ahmed Koran [2]

[1] Department of Electrical Engineering, Faculty of Engineering, Jordan University of Science and Technology, Irbid 22110, Jordan; iasmadi@just.edu.jo (I.A.S.); hjahmad13@eng.just.edu.jo (H.J.A.)

[2] Department of Electrical Power Engineering, Hijjawi Faculty for Engineering Technology, Yarmouk University, Irbid 21163, Jordan; akoran@yu.edu.jo

* Correspondence: saalbatran@just.edu.jo; Tel.: +962-272-01000

Received: 27 October 2017; Accepted: 11 December 2017; Published: 15 December 2017

Abstract: Enhancing the performance of the voltage source inverters (VSIs) without changing the hardware structure has recently acquired an increased amount of interest. In this study, an optimization algorithm, enhancing the quality of the output power and the efficiency of three-phase grid connected VSIs is proposed. Towards that end, the proposed algorithm varies the switching frequency (f_{sw}) to maintain the best balance between switching losses of the insulated-gate-bipolar-transistor (IGBT) power module as well as the output power quality under all loading conditions, including the ambient temperature effect. Since there is a contradiction with these two measures in relation to the switching frequency, the theory of multi-objective optimization is employed. The proposed algorithm is executed on the platform of Altera® DE2-115 field-programmable-gate-array (FPGA) in which the optimal value of the switching frequency is determined online without the need for heavy offline calculations and/or lookup tables. With adopting the proposed algorithm, there is an improvement in the VSI efficiency without degrading the output power quality. Therefore, the proposed algorithm enhances the lifetime of the IGBT power module because of reduced variations in the module's junction temperature. An experimental prototype is built, and experimental tests are conducted for the verification of the viability of the proposed algorithm.

Keywords: grid-connected inverter; power electronics; multi-objective optimization; switching frequency; total demand distortion; switching losses

1. Introduction

Renewable energy resources play a major role in the current world's energy generation. To interconnect renewable energy resources, grid connected three-phase VSIs are widely utilized [1]. However, the increased number of connections between the VSIs and the grid should never degrade the power quality, particularly at the point of common coupling (PCC), while the total harmonic distortion (THD) should never go beyond a specific limit to prevent harmonics related problems. It is possible to reduce the THD with the switching frequency (f_{sw}) being increased. However, when the f_{sw} is increased, the switching losses are likewise increased and, therefore, this can result in a reduction in the inverter's efficiency as well. Consequently, f_{sw} is typically, but not optimally, chosen as a trade-off between the output power quality and the efficiency at a specific loading condition. Since the operating conditions of the VSI are continuously varying, the variable switching frequency (VSF) enables the inverter switching losses to be decreased in regions where the harmonic content is insignificant, and, in the same sense, the harmonic content can be reduced in the regions where the inverter losses are highly insignificant.

The performance of the three-phase grid connected VSIs is highly dependent on the selected f_{sw}. Therefore, literature has proposed numerous algorithms of the VSF to enhance the inverter's efficiency [2,3], inverter's transient response [4], and the acoustic noise of induction motor [5]. Switching frequency is varied either within the fundamental period [6–9], or based on the operating conditions [10–12], such that the switching losses or the THD are minimized. In [6], the proposed algorithm is formulated based on the current-ripple analysis of the three-phase inverters in a time-domain. The idea was geared toward the reduction of f_{sw}, while maintaining the peak current ripple under a certain limit; consequently, there is a reduction in the average f_{sw}, and thus a reduction in switching losses. Application of the above algorithm can be found in [7,8] as well. In [9], the switching frequency trajectory was derived using calculus of variations and based on the current ripples analysis relative to the single-phase inverters in time-domain, in order to reduce the switching losses while meeting certain THD requirements. This method suffers from computational complexity and requires heavy offline calculations. In [10], the efficiency of single-phase inverter is incrementally enhanced, while satisfying standard THD; the result of the algorithm was an increase in the efficiency of the inverter in comparison with the conventional sinusoidal pulse-width modulation (SPWM) as well as the space-vector pulse-width modulation (SVPWM). In any case, the aim of the aforementioned methods was to enhance the efficiency of the inverter, while ensuring that the THD is continuously positioned to the highest allowable limit. An offline technique was proposed by the authors of [11] for the minimization of the losses of VSIs based on multi-objective optimization, where the proposed algorithm was used to control synchronous motors. Meanwhile, the target is characterized based on the weighted combination of the peak-to-peak ripple of electromagnetic torque and switching losses, in a way that a fair balance is achieved. In [12], an optimization process was applied on the electric and hybrid vehicle motor drive, in which f_{sw} was varied with different modulation indices or input voltages. Concurrent switching losses minimization and dead-time compensation study was presented in [13] under various power levels and different power factors. Compared with discrete pulse width modulation techniques, switching losses were reduced by 15%.

The switching losses were reduced at high current-levels in [14] by proposing new SVPWM strategies in which the number of switch commutations of the quasi-Z-source inverter is reduced. In [15], a lower number of commutations is achieved by the proposed optimization. The variable switching frequency reduces about 19% of the switching losses compared with constant switching frequency for similar output current quality. Analytical variable switching frequency is presented in [16] according to the modulation index and a predefined current ripple band. The switching frequency varies within the fundamental cycle (sub-fundamental) to reduce the switching losses of two level inverter traction drive system. In [17], the switching loss is analyzed under different discontinuous SVPWM techniques for balanced two-phase load fed by a three-leg inverter. The algorithm tried to balance the switching losses of each phase-leg at lower current ripple. In [18], 3D-SVPWM of four-leg VSI was presented to reduce the switching losses of the proposed shunt compensator by 33%. The efficiency of a grid-tied full bridge inverter is improved in [19] using the variable switching frequency scheme. The authors minimize the switching losses at predefined THD using a bipolar modulation scheme. Variable switching frequency was used in [20] to reduce switching losses and electromagnetic interference (EMI) noise of a common voltage oriented SPWM rectifier considering the restrictions on voltage ripple at the direct current (DC) link.

The THD and the maximum torque ripple of the permanent magnet synchronous machine are optimized in [21]. For this target, the authors presented a finite control set model based on a predictive control scheme. A new behavioral model for losses in power semiconductors was proposed in [22] where the impacts of gate resistance and gate voltage are considered. A summary of the several behavioral models existing in literature and industry was listed.

The major contribution this paper puts in place is the proposition of an efficient and practically sound VSF algorithm whereby there is an online variation of f_{sw} at various loading conditions, including the ambient temperature effect. The intensive calculations that are typically required with the exiting f_{sw}

variation-laws are avoided in the proposed algorithm. Moreover, the benefits of the proposed algorithm include the improvement of the inverters' switching devices and packaging reliability by reducing the variations in the junction temperature, which has a direct effect on the lifetime of the inverter. The attractiveness of this algorithm lies in its simplicity, in which the online computation of the optimal switching frequency can be easily done. Most of the algorithms that have been introduced in the literature suffer from computational complexity that makes them lack practical sound. The advantages of this new proposed algorithms can be summarized in four main points: (1) easy to be implemented using micro-controllers; and (2) the proposed procedure can be generalized for any power converter that includes multi-level inverters regardless of the control mode and the used technology of the power device. However, the proposed mathematical derivations are discussed on an IGBT power module of Infineon® FP50R06KE3 (Neubiberg, Germany). The same procedures are valid for different technologies that have different power loss analysis. (3) The proposed procedure does not require offline computations and lookup tables; and, (4) since the temperature is considered in the proposed algorithm, the algorithm can reduce the thermal stress on the inverter during high ambient temperature by reducing the switching frequency. Conversely, if the energy loss parameters are not directly given from the manufacturer datasheets, the parameters can be experimentally characterized.

The remaining parts of this study are organized as follows. Short summary of the architecture and the control mode of operations of VSIs are presented in Section 2. Section 3 presents the estimation of power losses. Section 4 presents the thermal modeling of the IGBT power module. Section 5 presents the time-domain current ripple analysis. Section 6 presents the proposed variable switching algorithm. Section 7 presents a discussion of the experimental validation. Finally, Section 8 concludes the paper.

2. Voltage Source Inverters

VSIs are crucial components in the alternating current (AC) microgrids and modern power systems. To ensure power system reliability, integrating distribution generators (DGs) with existing power systems has some technical and practical constraints. One of these main limitations is power system stability. Voltage stability becomes more important if the microgrid is off-grid (i.e., isolated microgrid) or if connected with a relatively weak power system. The controllability of the VSIs and the DGs adds effective and supportive actions that can improve the performance of the power systems and microgrids in steady state and transient modes of operation [23].

VSIs can be categorized into three main modes of operation and control schemes. The first one is usually named as a grid-forming power converter in which the VSI is working as a conventional AC source. The voltage and the frequency are controlled and stabilized; however, the output current is load dependent. The uninterruptible power supply (UPS) is an appropriate example of grid-forming VSI. The UPS delivers certain voltage and frequency, where the input of the UPS is also considered as a DC, regardless of being from isolated batteries or converted from an online AC power supply.

The second category is known as grid-feeding power converters. Under this mode of operation, the voltage control is not targeted in the control scheme of the VSI. Moreover, the VSI is working as a current source to supply the desired real and reactive powers. Feeding an energized power system adds more restrictions to the VSI and synchronizing the voltage at PCC is crucially important to track the desired real and reactive power set points. In the previous two modes of operation, either the voltage or the current is controlled. For power system stability, it is occasionally important to control both the output voltage and current. This category is known as grid-supporting power converters and can be classified into two modes: (1) besides supplying the demanded active and reactive powers, it must contribute to stabilizing the voltage and/or the frequency of the grid-connected systems; and (2) the supplied active and reactive powers are subjected to the output voltage magnitude. The voltage magnitude and frequency have higher priority in the second mode than the first mode, and, hence, they can be implemented either in islanded or grid connected microgrids [23].

The proposed algorithm is not limited to one topology or control mode from the aforementioned architectures. However, for the sake of discussion and clarity, the grid-forming scheme is taken as

an example in this paper. Figure 1 shows the grid-forming scheme associated with the proposed algorithm, as executed in the FPGA, which will be discussed in detail throughout the paper. To this end, any control scheme ends by generating the power reference to the pulse width modulator. The second and the important side for the modulator is generating the carrier signal and the switching frequency that are related to the proposed work. The inputs of the VSF algorithm are the loading measurements and the measured temperature.

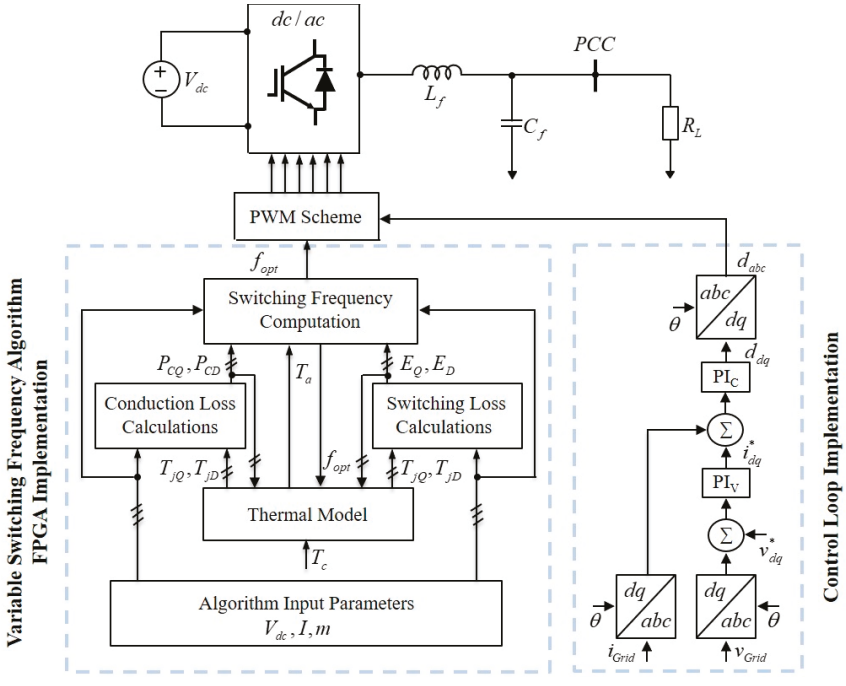

Figure 1. Grid-feeding VSI associated with the proposed VSF algorithm. PWM: pulse width modulation.

3. Estimation of Power Losses in IGBT Power Modules

Basically, the occurrence of power losses in the inverters must be appropriately dissipated to prevent system malfunction because of overheating. The design of the cooling systems, which take responsibility for the dissipation of power losses should be optimized to prevent system failure due to insufficient design or higher costs due to overestimation. The power losses rely on the utilized modulation scheme, loading conditions and the used semiconductor switch. The behavioral model alongside loss parameters taken from the device datasheet has been adopted in this paper due to its simplicity as in [24]. Moreover, in [25,26], the adopted behavioral model provides a good estimate of the actual losses as can be deduced from their comparative analysis.

Furthermore, the antiparallel diode and IGBT encounter power losses, which include driving losses and blocking losses. These losses tend to be insignificant and can be ignored [27]; the diode turn-on losses can be ignored as well [28]. Therefore, significant power losses are usually caused by: (i) the conduction losses [26,29], (ii) the switching losses (IGBT turn on and off losses), (iii) and the diode turn-off losses (the reverse recovery losses). A typical inverter module datasheet is comprised of valuable information regarding switching and conduction losses of its specific IGBT and diode. The datasheet information will be utilized for the estimation of the significant power losses that occur in the inverter, which will be further discussed and derived in detail in the subsections that follow.

3.1. Conduction Losses

The on-state voltage of IGBT (V_{CE}) varies with the collector current as depicted from the device voltage–current (V–I) curves at different junction temperatures (T_j) as shown in Figure 2. Due to this, it is possible to find the IGBT's on-state voltage as a function of the collector current. Moreover, the IGBT's on-state voltage relies on the on-state resistance (R_{CE}), including the threshold voltage of the IGBT (V_{CE0}). In Figure 3, R_{CE} is the reciprocal of the slope connecting points 1 and 2 of the linearized V–I curve while V_{CE0} is the extrapolation of this curve to the voltage-axis. Meanwhile, the on-state resistance and the threshold voltage are temperature dependent, and, hence, this dependency should be considered. This can be achieved by interpolating R_{CE} and V_{CE0} for a given junction temperature as in Equations (1) and (2) and Figure 4:

$$R_{CE}(T_j) = 5.82 \times 10^{-7} T_j^2 - 3.07 \times 10^{-5} T_j + 2.38 \times 10^{-2}, \quad (1)$$

$$V_{CE0}(T_j) = -9.10 \times 10^{-6} T_j^2 + 22.76 \times 10^{-5} T_j + 71.54 \times 10^{-2}. \quad (2)$$

As a result, an approximation of the IGBT on-state voltage can be given as

$$V_{CE}(t) = V_{CE0} + R_{CE} i_c(t), \quad (3)$$

where $i_c(t) = i_{pk} \sin(\omega t)$ is the phase-current that flows through the entire IGBT while conducting, $i_{pk}(t)$ is the output phase current peak value and ω is the angular frequency in rad/s.

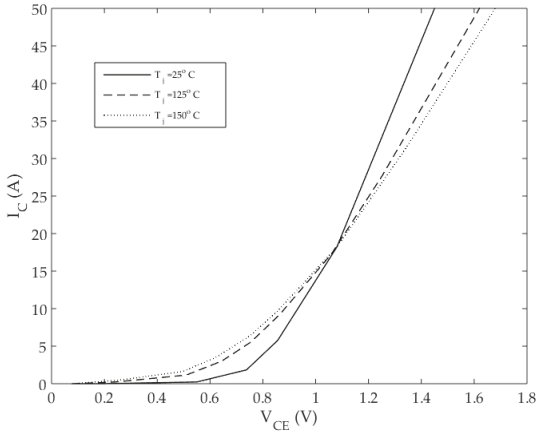

Figure 2. Infineon IGBT V–I curves for power module (Part number: FP50R06KE3) under different junction temperatures [30].

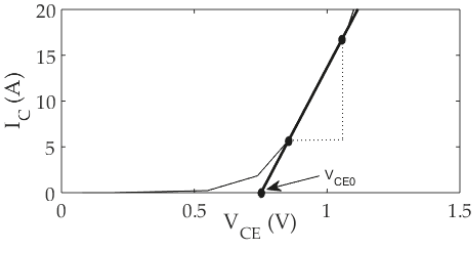

Figure 3. Linearization of V–I curves for IGBT.

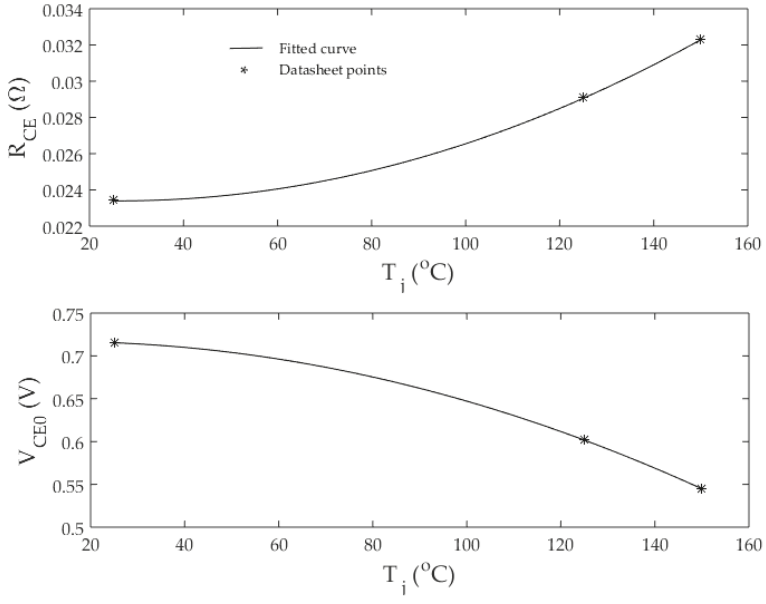

Figure 4. Interpolation of R_{CE} and V_{CE0} for different junction temperatures.

To estimate the average conduction losses of the IGBT for one fundamental phase–current period (P_{CQ}), the average losses in each switching period (T_{sw}) are lumped together, and then divided by the total number of the switching pulses as

$$P_{CQ} = \frac{1}{N}\sum_{n}\frac{1}{T_{sw}}\int_{(n-1)T_{sw}}^{nT_{sw}} i_c(t)V_{CE}(t)dt, \tag{4}$$

where N is considered as the total sum of pulses for each fundamental period and n is the switching pulse index.

In a case whereby f_{sw} is highly relative to the fundamental frequency, which is the typical case for SPWM inverter, it is possible to assume that the collector current is constant during every T_{sw}, that is,

$$i_c((n-1)T_{sw}) \cong i_c(nT_{sw}). \tag{5}$$

The IGBT is conducting for D_nT_{sw} at the nth switching cycle, where D_n is the duty cycle of the voltage pulses. Therefore, Equation (4) can be rewritten as

$$P_{CQ} = \frac{1}{N}\sum_{n}\frac{1}{T_{sw}}\int_{(n-1)T_{sw}}^{(n-1+D_n)T_{sw}} i_c(t)V_{CE}(t)dt. \tag{6}$$

Taking Equations (3) and (5) into account, and evaluating the integral in Equation (6) yields

$$P_{CQ} = \frac{1}{N}\sum_{n}\frac{1}{T_{sw}} i_c(nT_{sw})[V_{CE0} + R_{CE}i_c(nT_{sw})]D_nT_{sw}. \tag{7}$$

For the summation given in Equation (7), integration can be used to approximate it considering the assumption of f_{sw} is much higher than the fundamental frequency, and this assumption will be used throughout this study. Subsequently, the current flows through the IGBT at half period when its antiparallel diode is not conducting, and the integration is evaluated over half of the fundamental period (T) as in Equation (8):

$$P_{CQ} \cong \frac{1}{T}\int_{0}^{T/2} i_c(t)[V_{CE0} + R_{CE}\, i_c(t)]D(t)dt. \tag{8}$$

For SPWM modulation, the duty cycle as a function of time can be written as in Equation (9) [24]:

$$D(t) = \frac{1 + m\sin(\omega t + \theta)}{2}, \tag{9}$$

where θ is considered as the angle difference between the output phase current and output phase voltage in radian and m is the modulation index. Then, an evaluation of the integral yields:

$$P_{CQ} = \frac{V_{CE0}\, i_{pk}}{2\pi} + \frac{R_{CE} {i_{pk}}^2}{8} + \left(\frac{V_{CE0} i_{pk}}{8} + \frac{R_{CE} {i_{pk}}^2}{3\pi}\right) m\, \cos(\theta). \tag{10}$$

The same procedure used to compute the IGBT conduction losses will be used to compute the conduction losses of the antiparallel diode as well. A linear approximation of the V–I characteristics of the diode can be given as

$$V_f(t) = R_f\, i_f(t) + V_{f0}, \tag{11}$$

where V_{f0} is the threshold voltage of the diode and R_f is the forward resistance of the diode. The dependency of V_{f0} and R_f on the junction temperature is expressed in Figure 5 and Equations (12) and (13):

$$R_f(T_j) = -4.16 \times 10^{-8} T_j^2 + 5.27 \times 10^{-6} T_j + 2.14 \times 10^{-2}, \tag{12}$$

$$V_{f0}(T_j) = -9.22 \times 10^{-6} T_j^2 - 39.76 \times 10^{-5} T_j + 86.91 \times 10^{-2}. \tag{13}$$

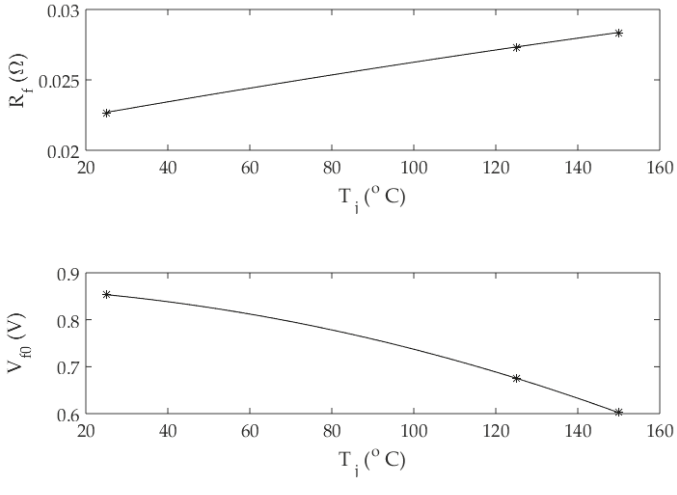

Figure 5. Interpolation of V_{f0} and R_f for different junction temperatures.

The diode is conducting for $(1 - D_n)T_{sw}$ at the nth switching cycle. Taking this into consideration and following the same adopted procedure in deriving the conduction losses in the IGBT, the diode conduction losses can be written as in Equation (14):

$$P_{CD} = \frac{V_{f0}\, i_{pk}}{2\pi} + \frac{R_f i_{pk}^2}{8} - \left(\frac{V_{f0} i_{pk}}{8} + \frac{R_f i_{pk}^2}{3\pi}\right) m\, \cos(\theta). \tag{14}$$

3.2. Switching Losses

The turn-on and off energy losses for every T_{sw} are provided in the device datasheet. Those are losses that rely substantially on the collector current (i_c), the IGBT's junction temperature (T_{jQ}), DC-link voltage (V_{dc}), and turn-on ($R_{g,on}$) and turn-off ($R_{g,off}$) gate resistances. For all the previous dependencies to be considered, 3D-curve fitting techniques are used for energy losses to be expressed based on the parameters above. With the use of the surface fitting, the turn-on and the turn-off energy losses (E_{on} and E_{off}) are expressed in terms of i_c and T_{jQ}, as shown in Figure 6 and Equations (15) and (16). After that, the derived equations must be scaled to include the effect of a specific $R_{g,on}$, $R_{g,off}$ and V_{dc} as in Equations (17) and (18):

$$E_{on}(i_c, T_j) = 30.34 \times 10^{-3} i_c + 75.79 \times 10^{-6} i_c^2 + 1.2 \times 10^{-4} i_c T_j, \tag{15}$$

$$E_{off}(i_c, T_j) = 46.92 \times 10^{-3} i_c - 3.939 \times 10^{-4} i_c^2 + 6 \times 10^{-5} i_c T_j, \tag{16}$$

$$E_{on} = \frac{V_{dc}}{V_{dc,test}} \frac{E_{on}(R_{g,on})}{E_{on}(R_{g,on,test})} E_{on}(i_c, T_{jQ}), \tag{17}$$

$$E_{off} = \frac{V_{dc}}{V_{dc,test}} \frac{E_{off}(R_{g,off})}{E_{off}(R_{g,off,test})} E_{off}(i_c, T_{jQ})\ . \tag{18}$$

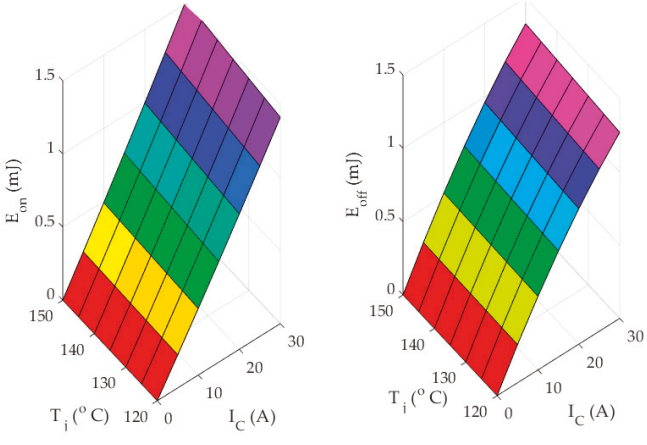

Figure 6. Interpolation of E_{on} and E_{off} for different collector currents and junction temperatures.

The notation 'test' represents the value that is utilized in the measurements of the energy losses test. Based on Equations (17) and (18), the average losses due to switching for every fundamental period (P_{swQ}) are given as in Equation (19):

$$P_{swQ} = \frac{1}{NT} \sum_n \Big(E_{on} + E_{off}\Big). \tag{19}$$

In Equation (19), E_{on} and E_{off} are functions of the collector current ($i_c(t) = i_{pk}\sin(\omega t)$). Based on estimation, it is assumed that the switching power losses are sinusoidal, while Equations (17) and (18) define the sine function peak of E_{on} and E_{off}, respectively, at the peak evaluation of the collector current. An approximation of the summation in Equation (19) can be given by the integration as in Equation (20):

$$P_{swQ} = \frac{1}{T}\left[\left(E_{on} + E_{off}\right)f_{sw}\right]\int_0^{T/2}\sin(\omega t)dt = \frac{E_{on} + E_{off}}{\pi}f_{sw}. \tag{20}$$

3.3. Reverse Recovery Losses

Following the same procedure in Section 3.2 but for the diode, Figure 7 shows the reverse recovery energy losses as functions of i_f and T_j and Equation (21) is the corresponding 3D-curve fitted equation:

$$E_{rec}(i_f, T_j) = 20.64 \times 10^{-3} i_f - 4.827 \times 10^{-4} i_f^2 + 7 \times 10^{-5} i_f T_j. \tag{21}$$

As a result, the formulations for the reverse recovery losses are expressed as:

$$E_{rec} = \frac{V_{dc}}{V_{dc,test}}\frac{E_{rec}(R_{g,on})}{E_{rec}(R_{g,on,test})}E_{rec}(i_f, T_j)\,, \tag{22}$$

$$P_{swD} = \frac{E_{rec}}{\pi}f_{sw}. \tag{23}$$

The total IGBT module power losses can be finally formulated as in Equation (24):

$$P_T = 6\left(P_{CQ} + P_{CD} + P_{swQ} + P_{swD}\right). \tag{24}$$

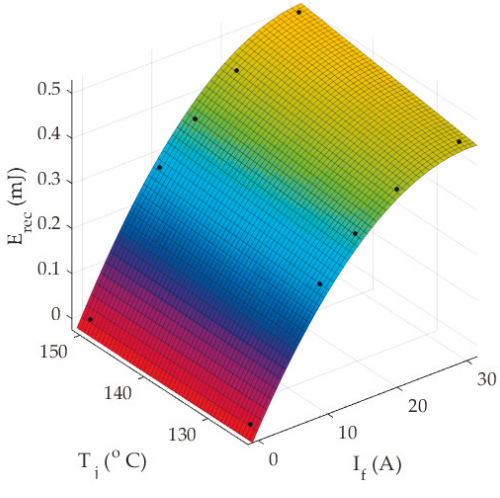

Figure 7. Interpolation of E_{rec} for different diode currents and junction temperatures.

4. Thermal Modeling of the IGBT Power Module

Power losses that occur in a semiconductor switch are the main cause of rise of its junction temperature; therefore, a thermal model that estimates the junction temperature from the power losses has to be constructed. Thermal models can be steady-state models such as thermal resistance networks in which only the steady-state temperatures can be estimated, or dynamic models such as

the well-known Foster and Cauer models that can estimate the transient behavior of the temperature when it changes from one steady-state point to another [31]. For gird-tied inverters, the time interval between two consecutive active-power set-points is much larger than the time constant of the thermal model in general. Since the aim of this study is to develop an algorithm that changes the switching frequency with the change in the steady-state operating conditions (mainly the active-power) as will be described later, thermal transients can be ignored. Hence, a steady-state thermal model is adopted in this study. In steady-state operating conditions, a specific IGBT conducts for a half-cycle, whereas its anti-parallel diode conducts for the other half, which causes the junction temperature to increase during the half-cycle of conduction and decrease during the other one; this causes a junction temperature ripple that the steady-state thermal model cannot estimate. However, for 50–60 Hz operation, the junction temperature ripple is much smaller than the average value of the junction temperature; therefore, a steady-state thermal model can be used. To account for the rise of the instantaneous junction temperature above its average value, the maximum junction temperature that corresponds to the maximum power dissipation is set to a value lower than the maximum operating junction temperature defined in the datasheet of the semiconductor device; this practice is a norm when it comes to the design of cooling systems of semiconductors.

Using the analogy between the electrical and thermal systems, it becomes possible to construct a thermal network whereby each resistor represents the thermal resistance regarding a particular material or path, while each current source represents a source of power loss. Moreover, the temperature difference across a particular material is represented by the voltage difference across the resistor [32].

The thermal resistance of a material in °C/W is defined as its resistance to heat flow across a temperature gradient. In the datasheet of the IGBT modules, the thermal resistances (R_x) of the major heat flow paths are provided, the notation 'x' can be {j,C,S,A} to denote the junction, case, sink and ambient, respectively. In addition, the zero-order thermal resistance network [26] of the IGBT module shown in Figure 8, is adopted in this study. This thermal model matches the fast-computational time associated with the proposed online variable switching frequency algorithms. The thermal resistance of the heat sink is denoted as (R_{SA}). Based on Figure 8, the following relations can be deduced:

$$T_s = 6\big(P_Q + P_D\big)R_{SA} + T_a, \tag{25}$$

$$T_c = 6\big(P_Q + P_D\big)R_{CS} + T_s, \tag{26}$$

$$T_{jQ} = P_Q\, R_{jCQ} + T_c, \tag{27}$$

$$T_{jD} = P_{loss,D}\, R_{jCD} + T_c, \tag{28}$$

where T_s is the heat sink temperature, T_a is the ambient temperature, T_c is the case (or base-plates), T_{jQ} is the IGBT's junction temperature, and T_{jD} is the diode's junction temperature. All the temperatures are in °C.

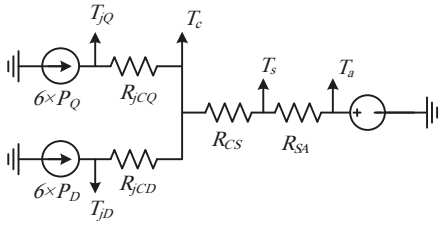

Figure 8. The IGBT power module's thermal resistance network.

5. Time Domain Current Ripple Analysis

Figure 9 shows the circuit diagram of the grid connected inverter, which includes an inductor (L) to represent the grid-inductance in series with a sinusoidal voltage source (v_g) for the grid to be represented. This representation is valid for any inverter that supplies motor loads and/or grids [33].

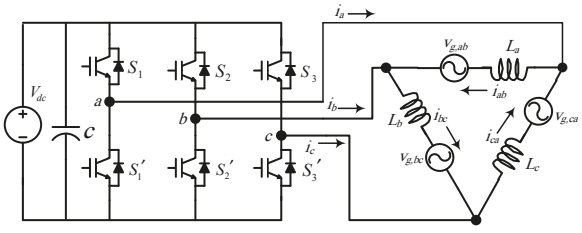

Figure 9. Δ-load connected to VSI.

Before proceeding with the current-ripple analysis based on time domain, the following assumptions are made:

- The input voltage is ripple-free.
- f_{sw} is relatively higher compared to the fundamental frequency.
- The modulating signals during each T_{sw} remain constant.
- The impact of dead-time is neglected.

From the circuit diagram of Figure 9, the voltage between phases a and b can be written as

$$v_{ab} = v_{g,ab} + L\frac{di_{ab}}{dt}, \tag{29}$$

where v_{ab} is the inverter's output line-line voltage, i_{ab} is the phase-current, and $v_{g,ab}$ is the line-line grid voltage.

As mentioned earlier, the load current consists of the ripple component and the fundamental-frequency component. Therefore, i_{ab} can be written as

$$i_{ab} = \bar{i}_{ab} + \hat{i}_{ab}, \tag{30}$$

where $\bar{i}_{ab}$ is the load current fundamental component and $\hat{i}_{ab}$ is the load current ripple component. Substituting Equation (30) in Equation (29), yields Equation (31), and then the load current ripple component can be expressed as in Equation (32):

$$v_{ab} = v_{g,ab} + L\left(\frac{d\bar{i}_{ab}}{dt} + \frac{\hat{i}_{ab}}{dt}\right), \tag{31}$$

$$\hat{i}_{ab} = \int \frac{v_{ab} - v_{g,ab}}{L} dt. \tag{32}$$

The term $d\bar{i}_{ab}/dt$ doesn't appear in Equation (32) because of the assumption that the fundamental component is constant within T_{sw}. The inductor resistance can be neglected, and since f_{sw} is much greater compared to the fundamental frequency, the current ripple component is placed under the assumption of rising and falling in a linear manner around the fundamental value. Using linear approximation, each segment of the current ripple is given as

$$\hat{i}_{ab} = \frac{t_2 - t_1}{L}(v_{t2} - v_{t1}), \tag{33}$$

where $\hat{i}_{ab}$ is the current ripple segment over the interval of time $(t_2 - t_1)$, v_{t1} is the voltage at time t_1 and v_{t2} is the voltage at time t_2.

The ripple component and the output line-line voltage of the load current at T_{sw} are shown in Figure 10. The ripple of the load current can be given as

$$\hat{i}_{ab} = -\frac{t - t_0}{L} v_{g,ab}; \text{ for } t_0 \le t \le t_1, \tag{34}$$

$$\hat{i}_{ab} = -\frac{T_0}{L} v_{g,ab} + \frac{t - t_1}{L}\left(V_{dc} - v_{g,ab}\right); \text{ for } t_1 \le t \le t_3, \tag{35}$$

$$\hat{i}_{ab} = -\frac{t - t_4}{L} v_{g,ab} + \frac{T_1 + T_2}{L}\left(V_{dc} - v_{g,ab}\right) - \frac{T_0}{L} v_{g,ab}; \text{ for } t_3 \le t \le t_4. \tag{36}$$

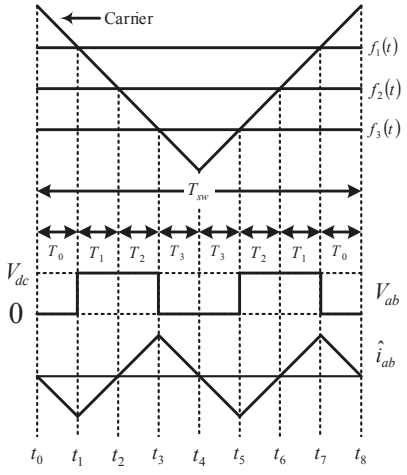

Figure 10. Load current ripple and output line-line voltage during a switching period.

The ripple current mean square value over T_{sw} (i.e., $\hat{I}^2_{ab}$) can be expressed as

$$\hat{I}^2_{ab} = 2f_{sw}\int_{t_0}^{t_0+t_4} \hat{i}^2_{ab}dt = \frac{2V^2_{dc}f_{sw}}{L^2}\left\{\int_0^{T_0} t^2dt + \int_0^{T_3} t^2dt + \int_0^{T_1+T_2}\left[-T_0 + \left(\frac{V_{dc}}{v_{g,ab}} - 1\right)t\right]^2 dt\right\}, \tag{37}$$

$$\hat{I}^2_{ab} = \frac{2V^2_{dc}f_{sw}}{L^2}\left[\frac{T_0^3}{3} + T_0^2(T_1 + T_2) - \left(\frac{V_{dc}}{v_{g,ab}} - 1\right)T_0(T_1 + T_2)^2 + \left(\frac{V_{dc}}{v_{g,ab}} - 1\right)^2\frac{(T_1+T_2)^3}{3} + \frac{T_3^3}{3}\right]. \tag{38}$$

The time intervals T_0, T_1, T_2 and T_3 can be related to T_{sw} as

$$T_0 = \left(\frac{1}{4} - \frac{1}{4}f_1(t)\right)T_{sw}, \tag{39}$$

$$T_1 = \left(\frac{f_1(t) - f_1(t)}{4}\right)T_{sw}, \tag{40}$$

$$T_2 = \left(\frac{f_3(t) - f_2(t)}{4}\right)T_{sw}, \tag{41}$$

$$T_3 = \left(\frac{1}{4} + \frac{1}{4}f_1(t)\right)T_{sw}, \tag{42}$$

$$f_1(t) = m\sin(\omega t);\ f_2(t) = m\sin\left(\omega t + \frac{2\pi}{3}\right);\ f_3(t) = m\sin\left(\omega t + \frac{4\pi}{3}\right). \tag{43}$$

Substituting Equation (43) in Equations (40), (41), and (42) yields

$$\hat{I}_{ab}^2 = \left(\frac{V_{dc}}{Lf_{sw}}\right)^2 \frac{m^2}{64}\sin^2\left(2\pi ft + \frac{\pi}{6}\right) \times \left[1 - \sqrt{3}m\sin\left(2\pi ft + \frac{\pi}{6}\right) + \frac{3}{4}m^2\right]. \tag{44}$$

To find the current ripple root mean square (*rms*) value over a fundamental period ($\hat{I}_{h,rms}$), Equation (44) is integrated over the fundamental period as in Equation (45):

$$\hat{I}_{h,rms} = \sqrt{\frac{1}{\pi}\int_{-\pi/6}^{5\pi/6} \hat{I}_{ab}^2\, d\omega t}. \tag{45}$$

It should be noted that the integration was conducted over the period $[-\pi/6, 5\pi/6]$ and the symmetry justifies integration over a half period. Substituting Equation (44) in Equation (45) gives

$$\hat{I}_{h,rms} = \frac{mV_{dc}}{16Lf_{sw}}\sqrt{2 - \frac{16\sqrt{3}}{3\pi}m + \frac{3}{2}m^2}. \tag{46}$$

If it is a Y-connected load, Equation (46) yields

$$\hat{I}_{h,rms} = \frac{mV_{dc}}{16\sqrt{3}Lf_{sw}}\sqrt{2 - \frac{16\sqrt{3}}{3\pi}m + \frac{3}{2}m^2}. \tag{47}$$

The THD in the inductor current THD_i is given as

$$THD_i = \frac{\hat{I}_{h,rms}}{\overline{I}_{ab,rms}}, \tag{48}$$

where $\overline{I}_{ab,rms}$ is the fundamental current's *rms* value.

6. The Proposed VSF Algorithm

Generally, the manufacturers of grid-tied inverters specify the PWM switching frequency f_{sw} as a design value with respect to the rated operating conditions. Increasing f_{sw} reduces the *rms* value of the current ripple and therefore the total demand distortion *TDD* is reduced as well. However, the value of f_{sw} is limited by the heat dissipation capability of the semiconductor power switches and their associated cooling system. When the operating point of the inverter is below the rated conditions, the cooling system appears to be oversized since it is possible to increase the switching frequency and hence enhance the quality of the output current. Using the aforementioned premise, each operating condition can be considered as a design problem; however, the switching frequency is the only degree of freedom that is available in the problem design. Therefore, an algorithm that is able to improve the output power quality of the grid-tied inverter without changing the physical structure of the system is significant from an industrial point of view [34].

Increasing f_{sw} will increase the power losses and hence reduce the efficiency. However, the output power quality is improved. Since increasing or decreasing f_{sw} will improve one feature of the system and degrade the other, this means that a conflict between two desired objectives is met, which is a typical multi-objective optimization problem. In such problems, there is no unique optimal solution but rather a set (maybe infinite) of optimal solutions. The selection of one solution among the set of solutions is a degree of freedom left to the preference of the designer [35,36].

To obtain an optimal solution with a reduced computational complexity that is strictly required for an algorithm that can determine the optimal f_{sw} online (i.e., without heavy offline calculations that are stored in lookup tables), a weighted-sum objective function is defined as follows:

$$Min \quad \Psi(f_{sw}) = (1-w) \times TDD\,(f_{sw}) + w \times P_{sw}(f_{sw}), \tag{49}$$

where Ψ is the optimization cost function to be minimized. f_{sw} is bounded by the upper and the lower permissible bounds, $f_{sw,l}$ and $f_{sw,u}$, respectively. $w \in \begin{bmatrix} 0 & 1 \end{bmatrix}$ is the trade-off factor. To this end, since each individual goal has distinct value, it is advisable to normalize both objectives in order to avoid misleading solutions as

$$\Psi_n = w\frac{P_{sw,total} - P^{ideal}_{sw,total}}{P^{nadir}_{sw,total} - P^{ideal}_{sw,total}} + (1-w)\frac{TDD - TDD^{ideal}}{TDD^{nadir} - TDD^{ideal}}, \tag{50}$$

where Ψ_n is the normalized cost function, TDD^{ideal} is the TDD at $f_{sw,u}$, TDD^{nadir} is the TDD at $f_{sw,l}$, $P^{ideal}_{sw,total}$ is the least expected switching losses, and $P^{nadir}_{sw,total}$ is the highest acceptable switching losses.

Furthermore, the optimal value of f_{sw} (f^{opt}_{sw}) can be found by equating the first order derivative of Equation (50) to zero, that is:

$$\frac{d\Psi_n}{df_{sw}} = w\frac{1}{f_{sw,u} - f_{sw,l}} - (1-w)\frac{f_{sw,u}f_{sw,l}}{f_{sw,u} - f_{sw,l}}\frac{1}{f^2_{sw}} = 0. \tag{51}$$

Rearranging Equation (51) yields

$$f^{opt}_{sw} = \sqrt{\frac{1-w}{w} f_{sw,l} \times f_{sw,u}}. \tag{52}$$

As the operation and the loading conditions are varying, there is a change in the energy losses. Therefore, $f_{sw,u}$ changes. In other words, for every new condition that emerges, a new optimization problem is solved. The maximum allowable switching frequency ($f_{sw,u}$) can be expressed based on switching energy losses given in Equation (53). However, $f_{sw,l}$ is restricted by the highest allowable TDD, which is assumed to be 5%. The minimum allowable switching frequency can be expressed as in Equation (54):

$$f_{sw,u} = \frac{\pi\, P^{nadir}_{sw,total}}{6(_{on} + E_{off} + E_{rec})}, \tag{53}$$

$$f_{sw,l} = \left(\frac{mV_{dc}}{16\sqrt{3}L}\sqrt{2 - \frac{16\sqrt{3}}{3\pi}m + \frac{3}{2}m^2}\frac{1}{I^{rated}_{L,rms}}\right)\frac{1}{0.05}. \tag{54}$$

Making use of Equations (53) and (54), (52) can be rewritten as

$$f^{opt}_{sw} = \sqrt{\frac{1}{0.05}\left(\frac{mV_{dc}}{16\sqrt{3}L}\sqrt{2 - \frac{16\sqrt{3}}{3\pi}m + \frac{3}{2}m^2}\frac{1}{I^{rated}_{L,rms}}\right)} \times \sqrt{\frac{\pi\, P^{nadir}_{sw,total}}{6\,(_{on} + E_{off} + E_{rec})}} \times \sqrt{\frac{1-w}{w}}. \tag{55}$$

The highest permissible losses are limited by the highest allowable T_{JQ} and T_{JD}. This value has to be evaluated for each new ambient temperature. Based on the thermal layout in Figure 8, the highest permissible total losses for each diode ($P_{D\max}$) at a given ambient temperature can be given as in

Equation (56) and the highest permissible losses for each IGBT ($P_{Q\max}$) can be related to Equation (56) as shown in Equation (57):

$$P_{D\max} = \frac{T_{jD,\max} - T_a}{R_{JCD} + 6\left(R_{CS} + R_{SA} + \frac{R_{jCD}}{R_{jCQ}}(R_{CS} + R_{SA})\right)}, \tag{56}$$

$$P_{Q\max} = \frac{R_{jCD}}{R_{jCQ}} P_{D\max}. \tag{57}$$

From Equations (56) and (57), the highest permissible losses ($P^{nadir}_{sw,total}$) can be evaluated with a consideration of just the switching loss aspect as follows:

$$P^{nadir}_{sw,total} = 6\left(P_{D\max}\left(1 + \frac{R_{jCD}}{R_{jCQ}}\right) - P_{CD} - P_{CQ}\right). \tag{58}$$

Figure 1 shows the implementation of the proposed algorithm in the FPGA platform. The operating conditions including the modulation index, the DC-link voltage, and grid current, and the power factor are used to estimate the conductions losses utilizing Equations (10) and (14) and the energy switching losses evaluating Equations (17), (18) and (22). From the power and energy losses' estimates, the optimal switching frequency is computed from Equation (55). Since the junction temperatures and power losses are mutually dependent, an iterative solution must be used as in Figure 11. It should be mentioned that the effect of the ambient temperature is taken into consideration as feedback from the case temperature, since the IGBT power module includes a thermistor that can be measured as in Figure 1.

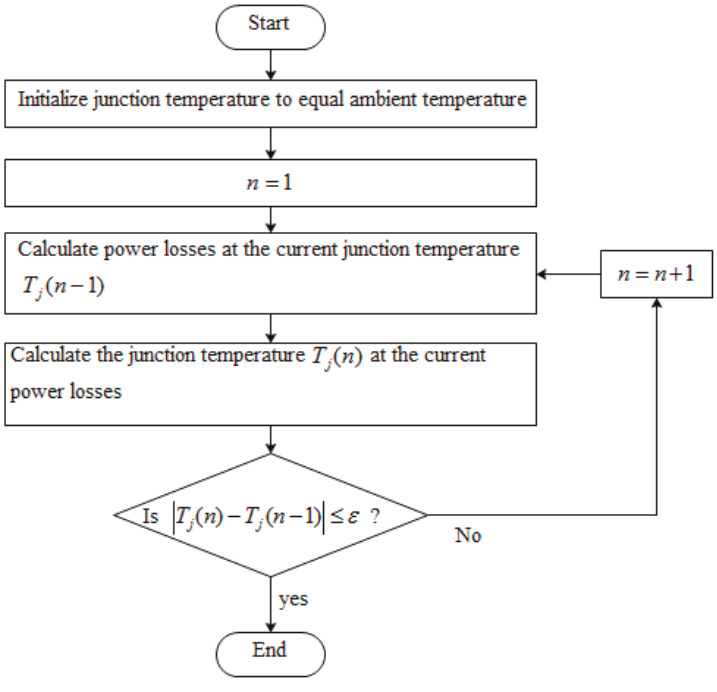

Figure 11. Flowchart of the iterative calculation of junction temperature.

7. The Experimental Results

Validating the significance of this proposed algorithm requires the setup of an experiment as in Figure 12. The experimental tests were performed on three-phase IGBT power module (Part Number: FP50R06KE3) cascaded with passive low pass inductor and capacitor (LC) filter output and supplying a Y-connected resistive load. Table 1 illustrates the system parameters and Table 2 depicts the optimal switching frequency at different loading conditions alongside total switching losses, *TDD*, and case temperature assuming a weighting factor of 0.6. As is evident, the proposed algorithm varies f_{sw} to obtain the best balance between the *TDD* and the switching losses based on inverter's loading conditions including the ambient temperature. When this system is at heavy loads, switching losses are high; therefore, the algorithm reduces f_{sw}, while keeping the *TDD* below the 5% limit (IEEE standard 519-2014). However, at light loads, the switching losses becomes low; hence, the algorithm increases the switching frequency for the output current quality to be enhanced.

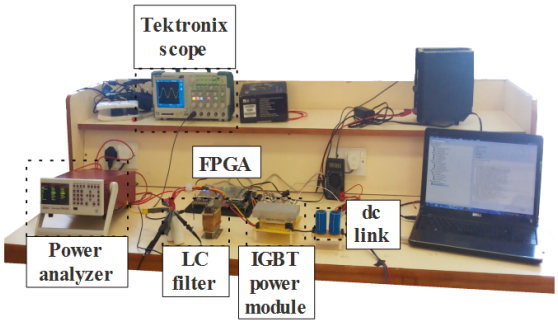

Figure 12. Experimental test-bed.

Table 1. The three-phase system parameters.

Parameters	Values
Ambient temperature (T_a)	20 °C
Filter inductance (L)	1.7 mH
Modulation index (m)	1
Filter capacitance (C)	10 µF
Input dc voltage (V_{dc})	200 V
Rated output current ($I_{L,rated}$)	5 A
Heat sink thermal resistance (R_{SA})	1.5 °C/W

Table 2. Algorithm response to load variation.

% of Rated Power	f_{sw} (kHz)	$P_{sw,total}$ (W)	*TDD* %	T_c (°C)
10	37.5	4.63	1.69	28.08
20	26.5	6.53	2.39	32.08
30	21.7	7.98	2.92	35.47
50	16.9	10.26	3.76	41.51
75	13.8	12.51	4.58	48.53
100	13.0	14.37	4.89	55.41

The measurement of the *TDD* was carried out by measuring the total harmonic distortion of the output current (THD_i) at certain loading conditions using the harmonic analysis functionality provided by a Tektronix oscilloscope (Model Number: TPS2024B). According to IEEE-519 *TDD* is defined as "*the total root-sum-square harmonic current distortion, in percent of the maximum demand load*

current". The calculated *TDD* is obtained from THD_i, the *rms* value of load current (i_{rms}) and the *rms* value of the rated current (i_{rms}^{rated}) as in Equation (59)

$$TDD = THD_i \frac{i_{rms}}{i_{rms}^{rated}}. \tag{59}$$

The measurement of the switching losses is initiated by measuring the steady-state case temperature at each operating condition by which the total power losses can be estimated. To extract the switching losses component, the experiment is performed again with fixed switching frequency while keeping other operating conditions unchanged, and, as a result, the conduction losses are unchanged as well. Since the switching losses are almost linearly related to the switching frequency, the switching losses can be deduced.

The following steps describe the experimental procedure in which switching losses are extracted:

(1) Measure the case (base plate) temperature by the solid state temperature sensors (negative temperature coefficient (NTC) thermistor) R_{NTC}. The temperature characteristic of this thermistor is shown in Figure 13 and Equation (60):

$$T_c = \frac{-26.48R_{NTC}^2 + 346.9R_{NTC} + 211.4}{R_{NTC}^2 + 5.345R_{NTC} + 0.9036}. \tag{60}$$

(2) From the measured case temperature and based on re-arranging of Equations (24)–(28), the total power losses is determined by Equation (61)

$$P_T = \frac{T_c - T_a}{R_{SA} + R_{CS}}. \tag{61}$$

(3) Under the same loading conditions, the switching frequency is varied, case temperature is measured, and losses are calculated.

(4) Based on the calculated power losses, the following set of Equations (62)–(65) can be computed:

$$P_T(f_{sw1}) = P_{CQ} + P_{CD} + \frac{E_{on} + E_{off} + E_{rec}}{\pi} f_{sw1}, \tag{62}$$

$$P_T(f_{sw2}) = P_{CQ} + P_{CD} + \frac{E_{on} + E_{off} + E_{rec}}{\pi} f_{sw2}, \tag{63}$$

$$P_T(f_{sw2}) - P_T(f_{sw2}) = \frac{E_{on} + E_{off} + E_{rec}}{\pi} (f_{sw2} - f_{sw1}), \tag{64}$$

$$P_T = \frac{P_T(f_{sw2}) - P_T(f_{sw2})}{f_{sw2} - f_{sw1}} f_{sw1}, \tag{65}$$

where f_{sw1} is the switching frequency of interest and f_{sw2} is the second switching frequency.

Validating how effective the proposed algorithm requires the experimental system to be tested with a fixed f_{sw} while constantly keeping the *TDD* at 2.5%. f_{sw} is selected as 25 kHz, which is approximately the middle point relative to the variable frequency range, with the system being tested under the same load conditions. Table 3 summarizes the performance of the inverter. Comparing the results from Tables 3 and 4, there is a reduction of the switching power losses at full load by about 51.6% using the proposed VSF algorithm, while the *TDD* is below the 5% limit. The decrease in the switching losses with the use of the proposed VSF algorithm is justified by the fact that the weight of 0.6 automatically leads the algorithm to favor the reduction of the switching power losses. Figure 14 gives the measured efficiency curves, which is for the whole inverter system alongside the fixed and VSF algorithms. It is obvious that the inverter efficiency is enhanced for a large array of load conditions.

Table 4 indicates a comparison between the calculated and experimental results. It can be shown that the power losses and *TDD* models are highly accurate.

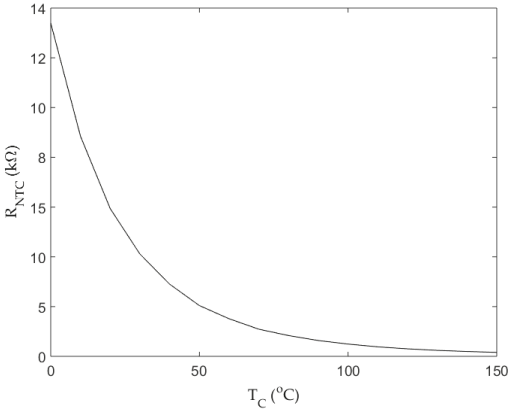

Figure 13. Infineon temperature characteristic of the NTC thermistor [30].

Table 3. Inverter performance f_{sw} = 25 KHz.

% of Rated Power	$P_{sw,total}$ (W)	T_c (°C)
10	3.10	25.73
20	6.14	31.49
30	9.18	37.28
50	15.17	48.97
75	22.53	63.76
100	29.73	78.76

Table 4. Comparison between the experimental and calculated results.

% of Rated Power	f_{sw} (kHz)	$P_{sw,total}$ (W)		*TDD* %	
		Cal.	Meas.	Cal.	Meas.
10	37.5	4.63	5.31	1.69	1.83
20	26.6	6.53	6.97	2.39	2.28
30	21.7	7.98	8.33	2.92	3.15
50	16.9	10.26	11.42	3.76	3.92

To further highlight the significance of the proposed algorithm, the California Energy Commission (CEC) efficiency of the inverter is measured under the fixed and VSF algorithms, the CEC efficiency is 97.3% using the proposed VSF algorithm, and 96.39% with the fixed f_{sw}. Therefore, it can be deduced from comparing the efficiencies of both algorithms that f_{sw} can be increased without degrading the efficiency of the inverter.

An interesting property related to the proposed VSF algorithm is the fact that the junction temperature variation under different load conditions tends to be lower than that one under fixed f_{sw}. As can be shown in Figure 15, the case temperature rate of change with the VSF algorithm is less than that of the fixed f_{sw}. This property holds even if more weight is given to the *TDD*. In other words, regardless of the selected weighting factor, the temperature profile when using the proposed algorithm will always have a slope that is under the one when using the fixed switching frequency. The importance of this property comes from the fact that the lifetime of the inverter is inversely proportional to the junction temperature difference [37–39].

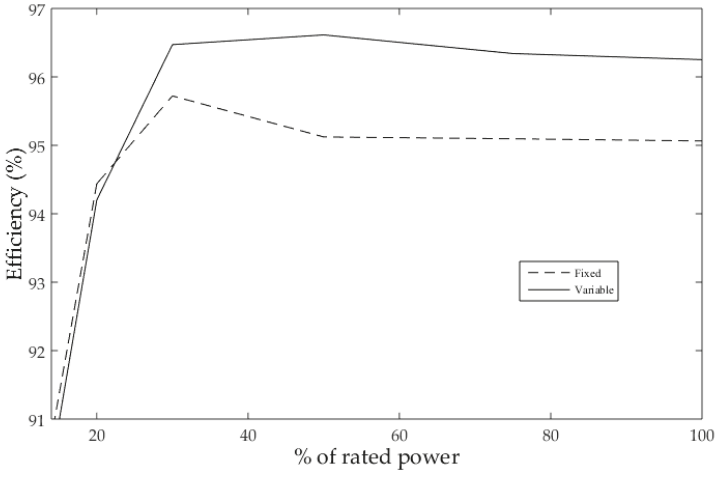

Figure 14. Measured efficiency curves.

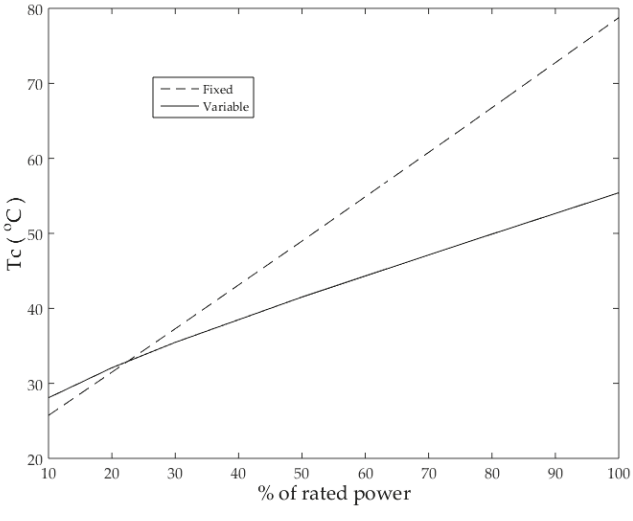

Figure 15. Calculated output case temperature variation with fixed and the proposed VSF PWM.

8. Conclusions

This study achieves the development of an online adaptive switching algorithm. In this algorithm, f_{sw} tends to be varied online according to the loading conditions and the ambient temperature. Depending on the models developed in Sections 2 and 3, f_{sw} was expressed based on the operating conditions, and an optimization issue was created using the multi-objective optimization theory. It was shown that the algorithm increases over all the inverter's efficiency from 96.39% to 97.3% at full load without degrading the output power quality. The inverter's lifetime can be increased because of the limited case temperature rate of change as well. The implementation of the developed algorithm is straightforward and the optimization can be performed online without complex computations, by which the intensive offline calculations and lookup tables are totally avoided.

Acknowledgments: Besides the open access fees, this research was supported by the deanship of research at Jordan University of Science and Technology (Grant number: 20150010).

Author Contributions: S.A. and H.J.A. designed the research idea and the experimental setup. I.A.S. and A.K. updated the literature review and improved the quality of presentation. I.A.S. and A.K. reviewed the estimation of power loses equations in IGBT power module. I.A.S. and H.J.A. analyzed the results. A.K. and S.A. did the graphical work. All authors participated in providing answers to all comments from reviewers. All authors read and approved the final manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

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Article

A Reduced Switch AC-AC Converter with the Application of D-STATCOM and Induction Motor Drive

Chaitanya Jibhakate [1,*], Madhuri Chaudhari [1] and Mohan Renge [2]

[1] Department of Electrical Engineering, Visvesvaraya National Institute of Technology, Nagpur 440010, India; macavc@yahoo.com

[2] Department of Electrical Engineering, Shri Ramdeobaba College of Engineering and Management, Nagpur 440013, India; mrenge@rediffmail.com

* Correspondence: chaitanya.jibhakate@students.vnit.ac.in; Tel.: +91-909-611-5118

Received: 10 May 2018; Accepted: 5 July 2018; Published: 10 July 2018

Abstract: In this paper, a reduced switch AC-DC-AC converter is used as a distribution static compensator (DSTATCOM) and induction motor drive. The AC-DC-AC nine switch converter (NSC) is a reduced switch topology of conventional 12-switch back to back converter. With a 25% reduced switch count, NSC has lower losses when operated at constant frequency mode compared to twelve switch converter (TSC). The idea is to operate NSC input terminal as an active front-end rectifier to mimic synchronous generator (SG) operation. The induction motor is connected at the output of the NSC for irrigation application where no speed regulation is required. In distribution generation (DG), a large capacitor bank is used to deliver required reactive power. This may lead to over-voltage at the point of common coupling (PCC) when the load is turned off. To manage reactive power transfer at PCC, a control scheme is developed for NSC such that it can absorb or deliver reactive power with induction motor drive. Similar to SG, V-curve and inverted V-curve is plotted. The simulation and hardware results prove the feasibility of the proposed system.

Keywords: nine switch converter; synchronous generator; digital signal controller; static compensator, distribution generation

1. Introduction

DG system recently getting more popular concerning gradual depletion of conventional sources. Several government policies such as subsidized solar panels and incentives on interest rebate of the windmill encourage more generation of solar and wind energy. With the increase in the connection of these renewable energy sources to the grid give rise to power quality issues [1–3]. It is necessary to maintain the acceptable voltage range at PCC with the varying load conditions. To keep bus voltage healthy, it is necessary to control reactive power transfer at loading and low load condition. At loading condition, sufficient reactive power must be available to avoid voltage dip at PCC. In addition, under low load condition, reactive power must be controlled to circumvent unacceptable voltage rise. To regulate reactive power transfer a FACTS device D-STATCOM has been utilized [4–7].

In this paper, in view of controlling reactive power transfer, the D-STATCOM is integrated with induction motor drive using nine switch AC-DC-AC converter. The NSC is recently introduced reduced switch topology of conventional twelve switch converter (TSC) [8–16]. Various AC-AC topologies are available in the literature. In matrix converter, to increase lifespan of converter the common DC-link is eliminated at the cost of an increase in the number of active switches. It requires 18 active switches for AC-AC conversion. Thus; switch associated losses and complexity increases [17]. The effort is taken to reduce the switch count of matrix converter known as sparse matrix converter. However, with reduced

switch count in sparse matrix converter, power flow become unidirectional [18,19]. Retaining common DC-link capacitor, another reduced switch topology found in [20], known as the B8 converter. It is the combination of two B4 converter which is connected back to back. In the B4 converter, four active switches form two phase legs while for third phase two split capacitors midpoint is used. The drawback of this arrangement is balancing two split capacitor voltage with large DC-link voltage variation [21].

The conventional AC-DC-AC converter for induction motor drive is made up of diode bridge rectifier followed by six active switches inverter. The disadvantage of this topology is that the input grid current is non-sinusoidal and has poor power factor operation. To improve quality of input current, the diode bridge rectifier is further replaced by active six switches converter known as back to back converter. It requires twelve active switches for AC-DC-AC conversion. In the proposed AC-DC-AC induction motor drive, only nine active switches are required which gives sinusoidal input current with desired power factor. The NSC turns out to be a better alternative for AC-DC-AC with reduced switch count. Many applications of NSC are found in literature because of its two three-phase terminal connection. It is used in an uninterrupted power supply (UPS) [13]. It is used to interface solar panels, battery, and ultra-capacitor output to the grid for DG system [14]. A compact battery charging system for an electric vehicle with the six-phase motor drive is reported in [11,12]. Depending on the terminal connection of NSC, it can be operated as DC-AC-AC, AC-DC-DC, and AC-DC-AC. Of course, with the reduce switch count, there are some operating constraints of the NSC. Application criteria of the NSC reported in [15,16] clearly mentioned that the NSC when operated as AC-DC-AC with different frequency operation is not recommended as it requires double DC-link voltage when compared to TSC operation. It also states that, when NSC is operated in common AC-DC-AC frequency mode then along with reduced switch count, losses in the NSC are lesser when compared to TSC.

Considering the advantages of the NSC operated in common AC-DC-AC frequency mode, in the proposed system the three-phase induction motor is connected at the output which will run at constant speed. For irrigation application, a centrifugal pump is connected to the induction motor. In this application, there is no requirement of controlling speed. As induction motor is operated at lagging power factor, a control scheme is developed such that the NSC with induction motor can be operated as lagging, unity, and leading power factor. Operating the NSC at leading power factor can deliver reactive power to PCC. The NSC, when operated as lagging power factor, can absorb reactive power from PCC of the grid. The idea is to operate the NSC to mimic synchronous generator at the input side and induction motor drive for irrigation application at the output side.

This paper is organized as follows, Section 2 gives system description and operation of NSC. The generation of the gate signal and operating constraint is explained in Section 3. The control logic of the proposed system is given in Section 4. Simulation and experimental results are presented in Sections 5 and 6 respectively. Finally, the conclusion is drawn in Section 7.

2. System Description and Operation of NSC

Figure 1 shows the overall single-line diagram of the three-phase power system connection. The NSC is connected at PCC with interfacing source inductance (L_s). Along with the NSC, a different rating of reactive loads are also connected at the PCC. The V_s is the grid phase voltage at PCC. The i_s, i_l, and i_a are the source, reactive load, and NSC currents respectively. The aim is to maintain the unity power factor at PCC such that no reactive power exchange at the PCC. To achieve this, the NSC is controlled so that, when the inductive load is connected, NSC will deliver reactive power and when the capacitive load is connected, NSC will absorb reactive power. Figure 2 shows phasor representation of the operation of the NSC. In Figure 2a, at PCC along with the NSC, an inductive load is connected. Thus NSC is operated at leading power factor (i_a leads V_s) such that V_s is in phase with i_s. Similarly when the capacitive load is connected at the PCC, the NSC is operated at lagging power factor (i_a lags V_s) resulting in-phase operation of V_s and i_s. As shown in Figure 1, a different rating of reactive load is connected at PCC to test the operation of NSC as DSTATCOM.

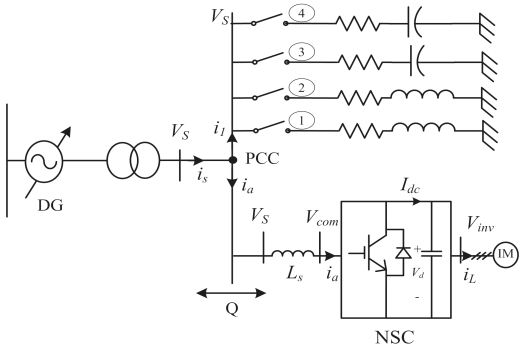
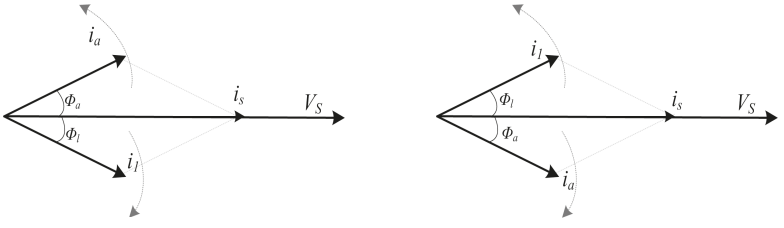


Figure 1. Single-line diagram of three-phase power system connection.



(**a**) NSC operated at leading power factor

(**b**) NSC operated at lagging power factor

Figure 2. Phasor representation of operation of NSC. (**a**) NSC operated at leading power factor; (**b**) NSC operated at lagging power factor.

Figure 3 shows the arrangement of NSC operated as DSTATCOM and induction motor drive. The terminal a, b, and c are the input points and the terminals x, y, and z are the output points of the NSC. For simplicity it is assumed that upper six switches (S_1, S_2, S_4, S_5, S_7, S_8) act as a DSTATCOM and lower six switches (S_2, S_3, S_5, S_6, S_8, S_9) act as a inverter to drive induction motor which is coupled to the centrifugal pump. The V_{com} and V_{inv} are the input and output terminal voltage of the NSC. The V_{com} is the function of DC-link voltage (V_d). The reactive power transfer depends on the difference between a magnitude of V_s and V_{com}. The voltage V_s is constant, thus by varying V_{com}, reactive power transfer can be altered. As V_{com} is a function of V_d, to charge DC-link capacitor (C_d) active power from PCC to NSC is transferred by varying power angle 'δ' between V_s and V_{com}. As the input terminal of the NSC is operated as active front end converter, to synchronize NSC at PCC, instantaneous angle 'θ' of the PCC voltage is tracked. To measure this angle 'θ', three-phase voltage is sensed by using voltage sensor. Synchronous reference frame phase lock loop (SRF-PLL) is implemented in the logic controller to extract angle 'θ' [22]. In practical, to interface voltage sensor signal and logic controller, signal conditioning circuit is required. Along with sensing voltage, a current sensor is required to calculate the active and reactive power of the converter. Another voltage sensor is required to measure DC-link capacitor voltage. As V_{inv} is the output of the NSC, which is the function of DC-link voltage. To keep V_{inv} magnitude constant, the modulation index of an inverter is changed according to the variation in DC-link voltage. To get desired gate pulses of the NSC, logic is developed in a logic controller. The controller ePWM (enhance pulse width modulation) pulses of the controller are processed by buffer circuit, an isolation circuit, and gate driver circuit to operated active power switches.

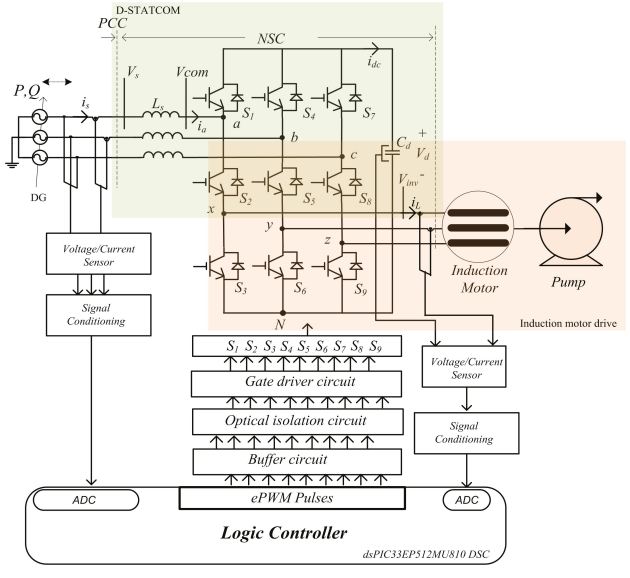


Figure 3. Arrangement of NSC operated as DSTATCOM and induction motor drive.

3. Generation of Gate Signal and Operating Constraints of the NSC

The AC-DC-AC NSC is operated as rectifier and inverter simultaneously. For rectifier and inverter operation two modulating references, Ref_{rec} and Ref_{inv} respectively is compared with a single carrier signal (V_{c}). For front-end rectification operation, Ref_{rec} must be synchronized to the PCC. Thus; SRF-PLL is implemented to track instantaneous angle 'θ' of the grid. Also, to control active power transfer between PCC and NSC, the reference Ref_{rec} is shifted by an angle 'δ' with respect to the PCC voltage. Figure 4 shows the PCC voltage and phase shifted references by an angle 'δ'. The Three-phase modulating references of the NSC are given by-

$$\begin{aligned}
Ref_{\text{rec_a}} &= m_{\text{r}} sin(\theta + \delta) + V_{\text{dc_offset}} \\
Ref_{\text{rec_b}} &= m_{\text{r}} sin(\theta - 120^{\circ} + \delta) + V_{\text{dc_offset}} \\
Ref_{\text{rec_c}} &= m_{\text{r}} sin(\theta + 120^{\circ} + \delta) + V_{\text{dc_offset}} \\
Ref_{\text{inv_x}} &= m_{\text{i}} sin(\theta + \delta) - V_{\text{dc_offset}} \\
Ref_{\text{inv_y}} &= m_{\text{i}} sin(\theta - 120^{\circ} + \delta) - V_{\text{dc_offset}} \\
Ref_{\text{inv_z}} &= m_{\text{i}} sin(\theta + 120^{\circ} + \delta) - V_{\text{dc_offset}}
\end{aligned} \tag{1}$$

where m_r and m_i are the modulation indices of Ref_{rec} and Ref_{inv}. The angle 'θ' is an instantaneous angle of the PCC voltage tracked by SRF-PLL. The angle 'δ' is a phase shift angle. To understand the generation of the gate signal of the NSC, one leg of the NSC is considered. There are eight possible switching states. Table 1 shows switching states and associated pole voltages. Among that eight switching states only three valid states are possible for the operation of the NSC. From Table 1, it is observed that pole voltage V_{aN} is always greater than or equal to V_{xN}. Hence; modulating reference Ref_{rec} is always kept above Ref_{inv}. Thus; to achieve switching constraint a small DC-offset is added and subtracted from Ref_{rec} and Ref_{inv}. The switching constraint is applied to avoid short circuit of a DC-link capacitor or open circuit condition of the inductive load. Figure 5 shows the generation of gate pulses and pole voltage. When Ref_{rec} is greater than the V_{c}, gate signal for S_1 is generated.

When Ref_{inv} is lower than the V_c, gate signal for S_3 is generated. Applying XOR logic to the gate signal of S_1 and S_3, gate signal for S_2 is obtained.

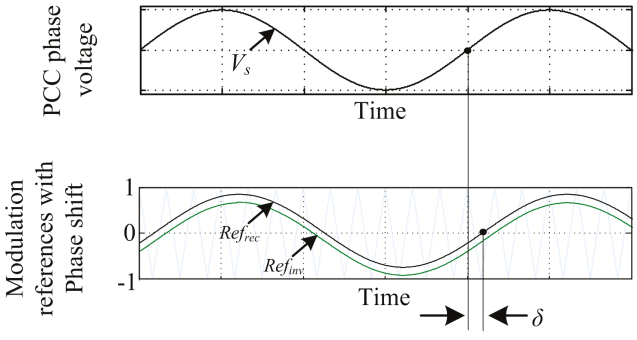


Figure 4. PCC voltage and phase shifted references by an angle 'δ'.

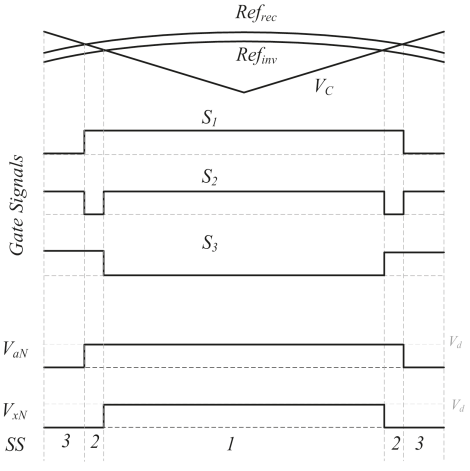


Figure 5. Generation of gate pulses.

Table 1. Switching states.

Switching States (SS)	S_1	S_2	S_3	V_{aN}	V_{xN}
Valid states					
1	1	1	0	V_d	V_d
2	1	0	1	V_d	0
3	0	1	1	0	0
Forbidden states					
4	1	1	1	0	0
5	0	0	0	0	0
6	1	0	0	V_d	0
7	0	1	0	0	0
8	0	0	1	0	0

4. Control Logic of the Proposed System

To control NSC, sinusoidal pulse width modulation technique is incorporated. A common DC-link is shared for both the rectifier and inverter operation. The rectifier input and inverter output voltage is a function of DC-link voltage and it is given by

$$V_{com} = Ref_{rec}\ V_d/2 \tag{2}$$

$$V_{inv} = Ref_{inv}\ V_d/2 \tag{3}$$

In the proposed system, NSC is connected to PCC with the source inductance. Figure 6 shows the single line diagram of the connection of the NSC to PCC with L_s which have its internal resistance R_s. The PCC voltage $V_s\angle 0$ is a reference voltage while $V_{com}\angle\delta$ is a variable voltage as it depends on the dc-link voltage of the NSC. The reactive power flow depends on the voltage magnitude of $|V_s|$ and $|V_{com}|$ and the active power flow depends on power angle between V_s and V_{com}. From Figure 6, rectifier input voltage V_{com} is given by

$$V_{com} = V_s - (R_s + jX_s)i_a \tag{4}$$

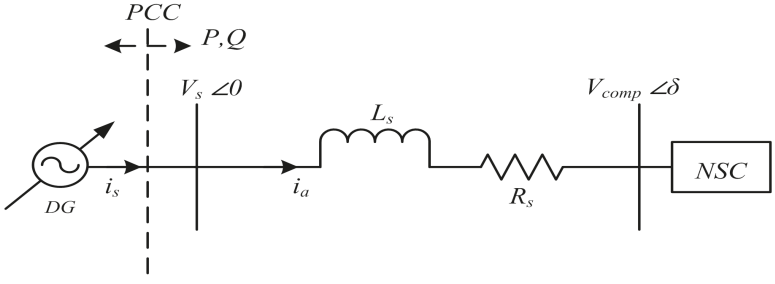


Figure 6. Single line diagram of the connection of the NSC to PCC.

Resolving i_a in *d*-*q* plane,

$$i_a = i^*_{ad} + ji^*_{aq} \tag{5}$$

where i_{ad}-active component, i_{aq}-reactive component. By controlling i_{ad} and i_{aq} current component of the NSC active and reactive power flow of the NSC is controlled. From (5) and (4)

$$V_{com} = (V_s - R_s i^*_{ad} + X_s i^*_{aq}) - j(R_s i^*_{aq} + X_s i^*_{ad}) \tag{6}$$

The magnitude and angle of V_{com} is given by

$$V_{com} = |V_{com}|\angle\delta \tag{7}$$

where

$$|V_{com}| = \sqrt{(V_s - R_s i^*_{ad} + X_s i^*_{aq})^2 + (R_s i^*_{aq} + X_s i^*_{ad})^2} \tag{8}$$

$$\angle\delta = tan^{-1}\frac{(R_s i^*_{aq} + X_s i^*_{ad})}{(V_s - R_s i^*_{ad} + X_s i^*_{aq})} \tag{9}$$

To calculate i^*_{aq} current reference, reactive power of the PCC is continuously monitored. In addition, to calculate i^*_{ad} reference output power of the NSC is measured. The active and reactive power in *d*-*q* reference is given by

$$P(t) = \frac{3}{2}[V_d(t)i_d(t) + V_q(t)i_q(t)] \tag{10}$$

$$Q(t) = \frac{3}{2}[-V_d(t)i_q(t) + V_q(t)i_d(t)] \tag{11}$$

Aligning the *d*-axis of the input and out voltage of the NSC with the d-axis of the synchronous reference frame.

For input side of the NSC

$$V_d = V_{comd} \tag{12}$$

For output side of the NSC

$$V_d = V_{invd} \tag{13}$$

As the *q*-axis is orthogonal to the reference axis

$$V_q = 0 \tag{14}$$

By using Equations (10)–(14), active power of NSC input and output is given by

$$P_{in} = \frac{3}{2}[V_{comd}\ i_{ad}] \tag{15}$$

Bu using Equations (6), (10), and (11), real power at the inverter output side is given by:

$$P_{out} = \frac{3}{2}[V_{invd}\ i_{Ld}] \tag{16}$$

where i_{Ld} is a *d*-axis component of the load current. Assuming NSC to be lossless converter and applying power balance criteria,

$$P_{in} = P_{out} \tag{17}$$

$$\frac{3}{2}[V_{com}\ i_{ad}] = \frac{3}{2}[V_{invd}\ i_{Ld}] \tag{18}$$

As the same dc-link is shared by the rectifier and inverter, V_{comd} and V_{invd} is given by:

$$V_{comd} = Ref_{rec}\ V_d/2 \tag{19}$$

$$V_{invd} = Ref_{inv}\ V_d/2 \tag{20}$$

The m_r and m_i are the only variable in Ref_{rec} and Ref_{inv}, Thus; by using Equations (18)–(20)

$$i_{ad} = [\frac{m_i}{m_r}]i_{Ld} \tag{21}$$

Equation (21), gives relation between source current and load current in terms of modulation index of rectifier and inverter reference. The i_{Ld} is active component of the load current. Thus;

$$i_{ad} = [\frac{m_i}{m_r}]i_L\ cos\phi_o \tag{22}$$

where ϕ_o is load phase angle. The $i_L cos\phi_o$ is calculated from measured output power. Thus; i^*_{ad} reference is generated. To calculate i^*_{aq}, reactive current component ($i_s sin\phi$) of the PCC current is measured. The aim is to maintain zero reactive power at PCC. Thus, the $i_s sin\phi$ is compared with zero reference so as get desired i^*_{aq}. Figure 7 shows the proposed control diagram. The calculated i^*_{ad} and i^*_{aq} is fed to the phase shift generator block which generates desired phase shift to control active power or to charge

DC-link capacitor at desired voltage level. The extracted PLL angle θ and angle δ is used to generate desired gate pulses for the operation of NSC.

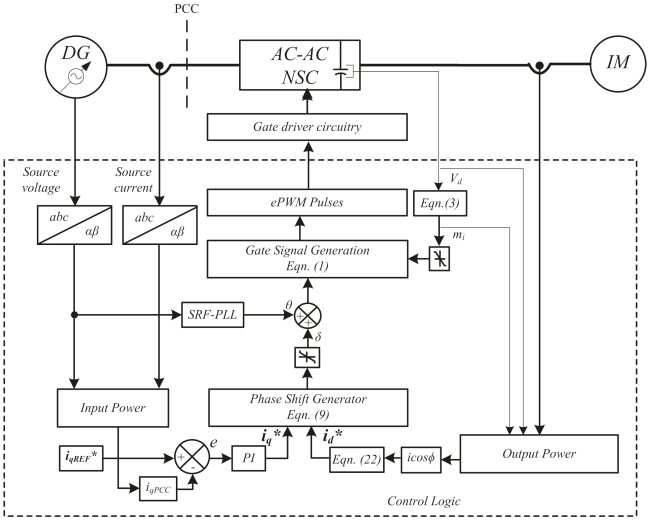


Figure 7. Control scheme.

5. Simulation Result

The MATLAB simulation is carried out considering different load conditions at PCC. The simulation parameters are given in Table 2. To maintain unity power factor operation at PCC, the reference current i^*_{qREF} is kept as 0. Referring to Figure 1, to test the dynamic performance of the proposed control technique different reactive loads are connected for different time duration. The time duration of different load connection is given in Table 2. The switching frequency (F_{sw}) of the NSC is 9 kHz. The modulation index of a rectifier is kept constant at 0.8, whereas modulation index of an inverter is varying to keep V_{inv} constant. To satisfy switching constraint a small dc-offset of 0.1 pu is added only in rectifier references. The NSC input and output line voltages are shown in Figure 8.

Table 2. Simulation parameter.

V_s	**3-Phase, 400 V, 50 Hz**
Induction Motor	5.4 hp, 4 pole, 400 V, 50 Hz
L_s, R_s, m_r, F_{sw}	10 mH, 1.63 Ω, 0.8, 9 kHz
Load at PCC parallel to NSC drive	
1-R-L	25 Ω, 0.1 H [0–1 s]
2-R-L	25 Ω, 0.3 H [1–2 s]
No-load	[2–3 s]
3-R-C	25 Ω, 30 μF [3–4 s]
4-R-C	25 Ω, 60 μF [4–5 s]

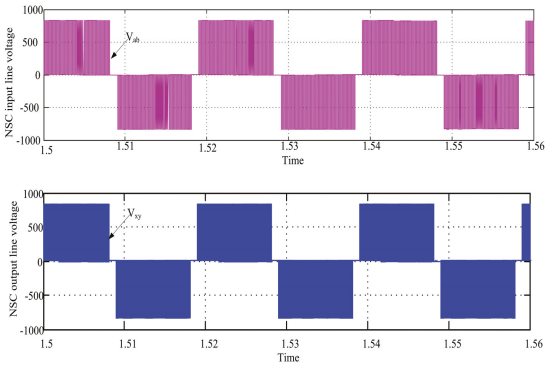


Figure 8. NSC input and output line voltages: V_{ab}, V_{xy} (500 V/div, 10 ms/div).

Figure 9 shows the exchange of the three-phase reactive power transfer under varying load conditions. During 0–1 s, 3100 VAR reactive power (Q_{load}) is absorbed by the R-L load. Thus; to maintain zero reactive power (Q_{ref}) transfer at PCC, NSC delivers −3100 VAR (Q_{NSC}) so that actual reactive power (Q_{act}) is equals to Q_{ref}. Similarly, during 1–2 s, 1550 VAR is absorbed by an R-L load, thus NSC provided −1550 VAR to the PCC. During 2–3 s, no load is connected parallel to the NSC, thus there is no exchange of reactive power at PCC. During 3–4 s, an R-C load is connected which delivers −1400 VAR reactive power, thus NSC absorbs 1400 VAR from PCC. Similarly, for 4–5 s, R-C load delivers −2450 VAR, thus NSC absorbs 2450 VAR from PCC to maintain zero reactive power at PCC.

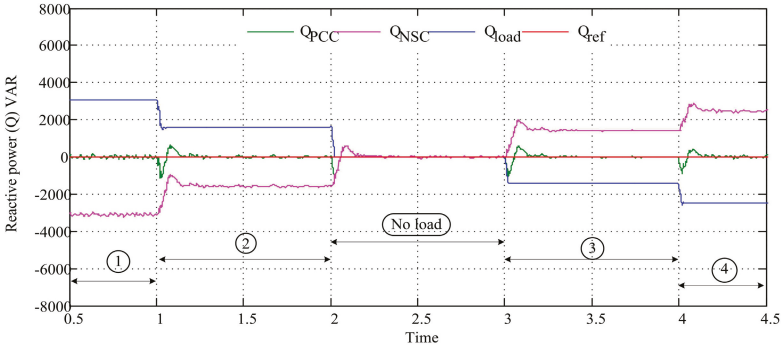


Figure 9. Exchange of three-phase reactive power at PCC: Q (2000 VAR/div, 0.5 s/div).

Figures 10 and 11 show the effect of varying load conditions on the NSC phase current (i_a) and power factor of the NSC respectively. Figure 10a shows, during 0–1 s the NSC is operated at 0.8 leading power factor (i_a leads V_s). After the change in load, NSC changed its operation to 0.93 leading power factor. When there is no load connected parallel to the NSC at 2 s, the NSC switched its operation from 0.93 lead to 0.999 unity power factor (i_a in-phase to V_s) as shown in Figure 10b. Figure 10c shows at 3 s when an R-C load is connected at PCC, the NSC is operated at 0.95 lagging power factor (i_a lags V_s). At 4 s when an R-C load is changed, the NSC shifted its operation from 0.95 lagging power factor to 0.86 lagging power factor as shown in Figure 10d.

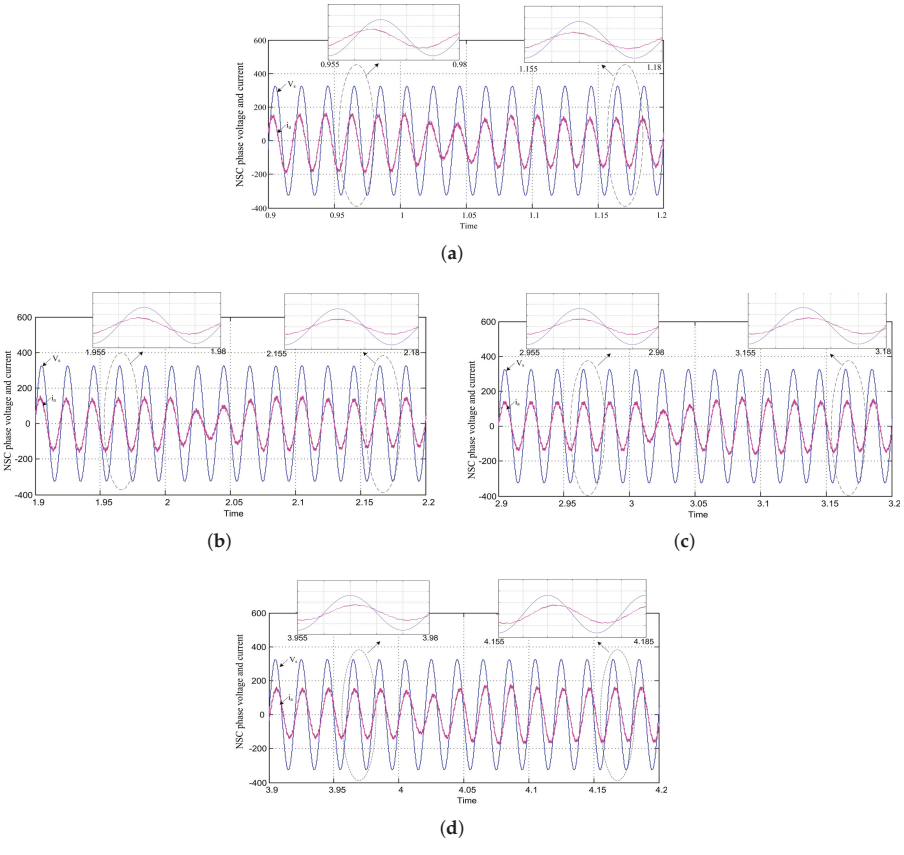


Figure 10. Phase voltage and NSC phase current under various load conditions: V_s, 15 * i_a (200 V/div, 200 A/div, 50 ms/div).

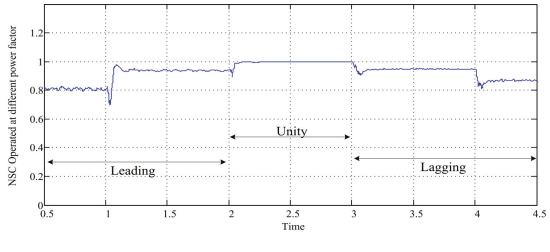


Figure 11. NSC operated at different power factor: (0.2 pu/div, 0.5 s/div).

Figures 12 and 13 show a change in DC-link capacitor voltage and the angle δ respectively. As earlier discussed, the reactive power transfer from NSC to PCC depends on voltage magnitude of V_s and V_{com}. As V_{com} depends on DC-link voltage, with the changed in DC-link voltage V_{com} varies and thus reactive power transfer varies. In a simulation, at first, NSC delivered reactive power thus at that instant required DC-link is more. With the change in load, NSC changed its operation from delivering to absorbing reacting power. Thus, according to a required magnitude of V_{com}, DC-link voltage is varied as shown in Figure 12. To charge or discharge the DC-link capacitor the angle δ is varied as

per desired DC-link voltage requirement and finally, it settled down. As a common DC-link is shared for rectifier and inverter function of the NSC, with the change in DC-link voltage V_{inv} also changes. To maintain V_{inv} constant, m_i is varied to keep NSC output voltage constant. Figure 14 show change in modulation index of the inverter. Figures 15 and 16 show induction motor three-phase current and speed under dynamic load variations at PCC.

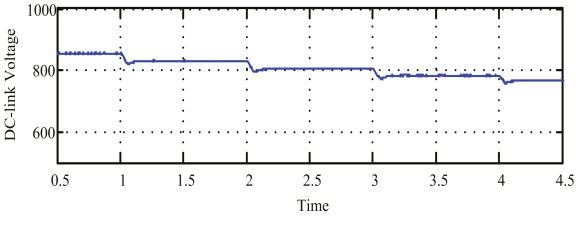


Figure 12. DC-Link capacitor voltage: (200 V/div, 0.5 s/div).

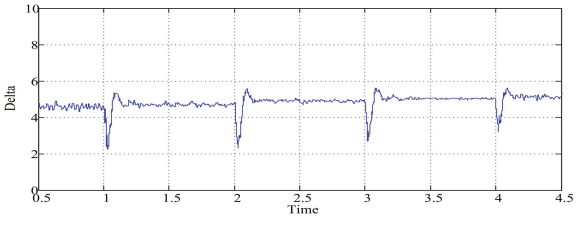


Figure 13. Change in angle delta (δ): (2 deg/div, 0.5 s/div).

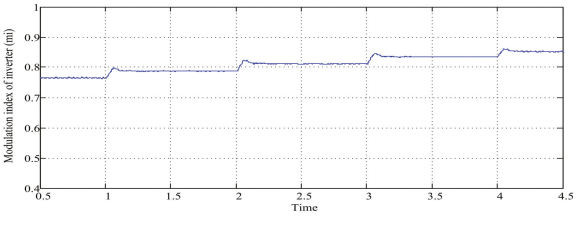


Figure 14. Change in modulation index of inverter: m_i (0.1 pu/div, 0.5 s/div).

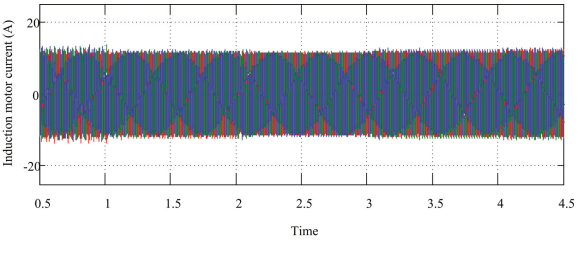


Figure 15. Three-phase induction motor current: i_L (10 A/div, 0.5 s/div).

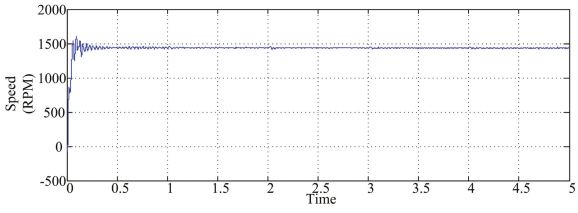
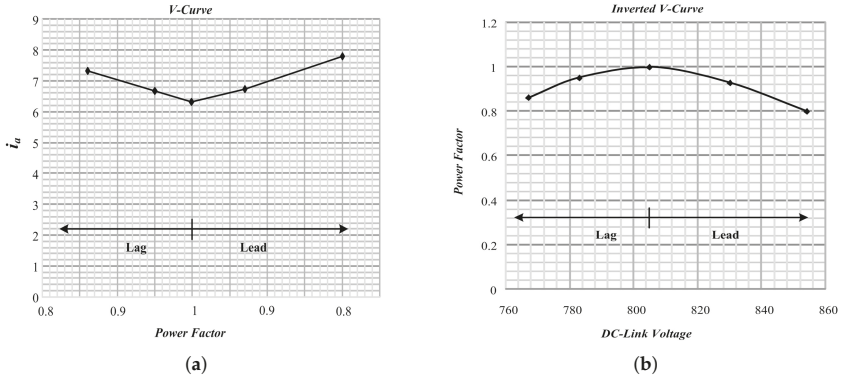


Figure 16. Induction motor speed: (500 RPM/div, 0.5 s/div).

The simulation results are summarized in Table 3. It is observed that the input rectifier operation of the NSC mimics the operating principle of the synchronous generator. The synchronous generator delivers reactive power when its field is over-excited and absorbs reactive power when its field is under-excited. The V-curve and inverted V-curve is obtained by varying field excitation of the synchronous motor. A Similar phenomenon is observed in case of the NSC. By controlling DC-link voltage of the NSC reactive power transfer can be controlled. From simulation results shown in Table 3, V-curve and inverted V-curve is plotted in Figure 17.

Table 3. Simulation results.

[V_s = 230 V/phase, m_r = 0.8]							
	i_a(A) % THD	cosϕ_a	V_{ab1} (V) % THD	V_d (V)	Q_{NSC} (VAR)	V_{xy1} (V) % THD	i_L (A) % THD
① 0–1 s	7.8 4.5%	0.8 lead	424.2 32.10%	854	−3100	400 32.24%	7.8 4.9
② 1–2 s	6.72 4.9%	0.93 lead	412.3 32.16%	830	−1550	400 32.24%	7.8 4.8
No-load 2–3 s	6.318 4.93%	0.999 unity	400 32.16%	805	0	400 31.91%	7.8 3.8
③ 3–4 s	6.67 4.58%	0.95 lag	388.9 32.01%	783	1420	400 31.7%	7.8 4.0
④ 4–5 s	7.32 4.36%	0.86 lag	380.7 31.97%	767	2450	400 31.56%	7.8 4.89



(**a**) (**b**)

Figure 17. V-curve and inverted V-curve of the NSC.

6. Experimental Setup and Result

The experimental setup of the NSC with induction motor connected to the source through the source inductance is shown in Figure 18. The experimental parameters are given in Table 4. The Hioki 3197 power quality analyzer is used to measure various system parameters. The source voltage is kept constant at 110 V. Three LV20-P voltage sensors are used to measure source voltage to track instantaneous source angle (θ) for the rectifier operation of the NSC. The NSC input (V_{ab}) and output (V_{xy}) line voltages are shown in Figure 19.

Table 4. Parameter of Experimental Setup.

Item	Specification
AC Source	0–110 V
Source Inductance	10 mH
IGBT	KGT25N120NDH
Gate driver IC	MIC4425
DSP	dsPIC33EP512MU810
Software	MPLAB X IDE v2.10
Sensors	LV-20P, LA-25P
Induction Motor	1 hp, 4 Pole,110 V, 50 Hz

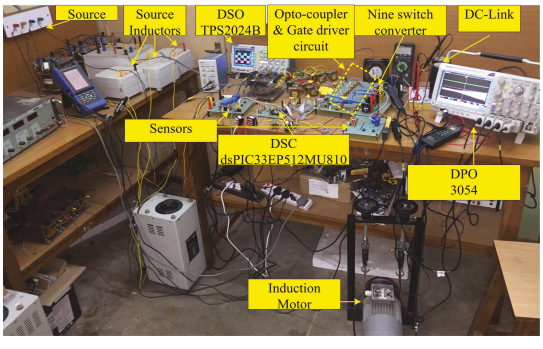


Figure 18. Experimental setup.

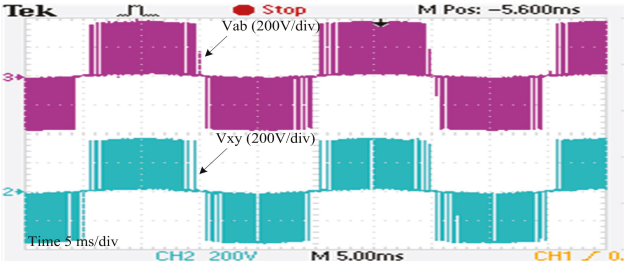


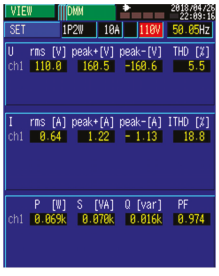
Figure 19. NSC input and output voltages: V_{ab}, V_{xy} (200 V/div, 5 ms/div).

To demonstrate reactive power transfer between source and NSC, i^*_{qREF} reference is varied. The operation of NSC is tested for different power factor conditions.

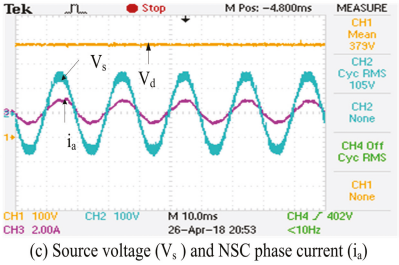
6.1. NSC Operated at Unity Power Factor Condition

To operate NSC with induction motor drive at unity power factor, reference i^*_{qREF} is kept as 0 pu. The phase angle between V_s and i_a is 4.5° as shown in Figure 20a. Ideally, as i^*_{qREF} is 0, the angle between V_s and i_a must be equal to zero. However, due to the presence of harmonics in the system, a small reactive power is consumed by the harmonics present in pulsating nature of the input and output voltages. Figure 20b shows various parameters of the system. It is observed that a small reactive power of 16 VAR is absorbed by the NSC. The power factor is almost unity i.e., 0.974 PF. Figure 20c shows the phase voltage and phase current are in phase. The DC-link voltage is 380 V. The NSC phase current is 0.64 A.

(a) Phase angle between V_s and i_a



(b) System parameters

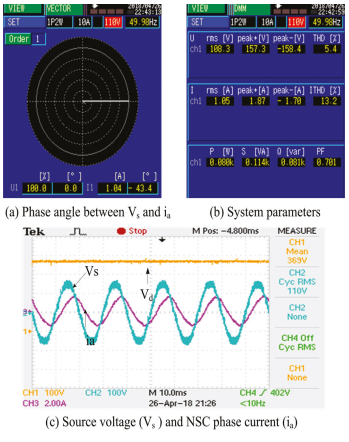


(c) Source voltage (V_s) and NSC phase current (i_a)

Figure 20. Unity power factor operation of the NSC i^*_{qREF} = 0 pu: V_d, V_s, i_a (100 V/div, 100 V/div, 2 A/div, 10 ms/div).

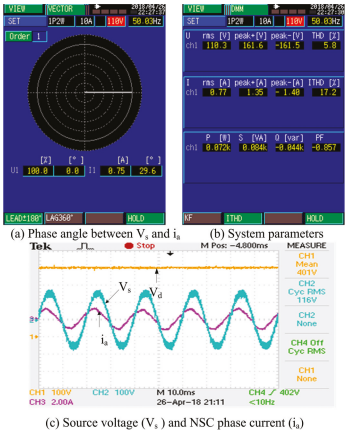
6.2. NSC Operated at Lagging Power Factor Condition

The lagging power factor operation of the NSC is tested for two conditions; i^*_{qREF} = 0.7 pu, and i^*_{qREF} = 0.3 pu. As shown in Figure 21a, when i^*_{qREF} is 0.7 pu, 81 VAR reactive power is absorb by the NSC. The phase angle between V_s and i_a is 43.4° (lag) i.e., 0.701 PF. The amplitude of phase current i_a increased to 1.05 A as compared to the unity power factor operation. The DC-link voltage is droped to 369 V. As shown in Figure 22b, when i^*_{qREF} is 0.3 pu, 33 VAR reactive power is absorb by the NSC. The phase angle between V_s and i_a is 22.2° lag i.e., 0.896 PF. The amplitude of i_a and DC-link voltage is 0.70 A and 371 V respectively.



(**a**) i^*_{qREF} = 0.7 pu (**b**) i^*_{qREF} = 0.3 pu

Figure 21. Lagging power factor operation of the NSC: V_d, V_s, i_a (100 V/div, 100 V/div, 2 A/div, 10 ms/div).



(**a**) i^*_{qREF} = −0.4 pu (**b**) i^*_{qREF} = −0.6 pu

Figure 22. Leading power factor operation of the NSC: V_d, V_s, i_a (100 V/div, 100 V/div, 2 A/div, 10 ms/div).

6.3. NSC Operated at Leading Power Factor Condition

The leading power factor operation of the NSC is also tested for two conditions; i^*_{qREF}= −0.4 pu, and i^*_{qREF}= −0.6 pu. As shown in Figure 22a, when i^*_{qREF} is −0.4 pu, 44 VAR reactive power is delivered by the NSC. The phase angle between V_s and i_a is 29.6° (lead) i.e., 0.857 PF. The amplitude of phase current i_a increased to 0.88 A as compared to the unity power factor operation. The DC-link voltage is increases to 401 V. As shown in Figure 22b, when i^*_{qREF} is 0.6 pu, 65 VAR reactive power is delivered by the NSC. The phase angle between V_s and i_a is 40.6° (lead) i.e., 0.751 PF. The amplitude of i_a and DC-link voltage is 0.88 A and 408 V respectively.

The positive reactive power shown in Figure 21 states that reactive is absorb by the NSC. The negative reactive power shown in Figure 22 states that the reactive power is delivered by NSC.

Thus, the NSC with induction motor drive can be operated to absorb or to deliver reactive power to the connected source. Figure 23 show induction motor phase current on half load. The V-curve and inverter V-curve is plotted from experimental results is shown in Figure 24.

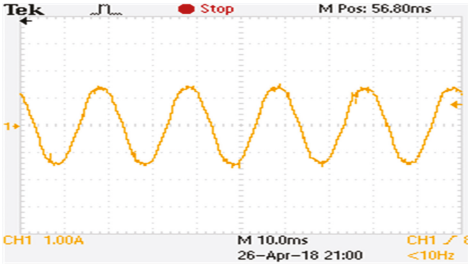
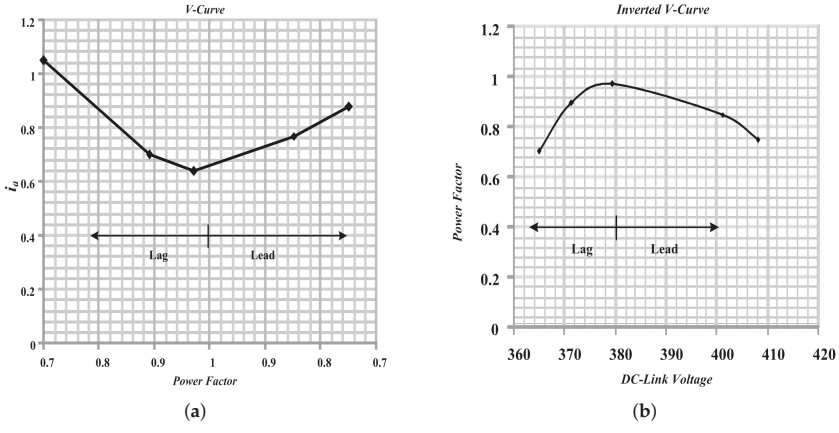


Figure 23. Induction motor current: i_L (1 A/div, 10 ms/div).



(**a**) (**b**)

Figure 24. Experimental V-curve and inverted V-curve of the NSC.

Comparing V-curve of simulation and experimental showed in Figures 17a and 24a, it is observed that the amplitude of the NSC phase current (i_a) is minimum near unity power factor. The amplitude of i_a increased as the power factor lowered on both the lagging as well as leading side. Referring to Figure 6, the power factor at the PCC depends on the voltage magnitude of V_s and V_{com}. The PCC voltage V_s is constant and the magnitude of the V_{com} is directly depends on DC-link voltage (V_d) as per (2). Thus; controlling V_d, power factor at the PCC is controlled. Comparing inverted V-curve of simulation and experimental results showed in Figures 17b and 24b, as the DC-link voltage increases power factor shifted from lagging to leading. Ideally, when the magnitude of the V_s and V_{com} is equal, the power factor at PCC must become zero. However, practically, there is a small voltage drop across the internal resistance of the source inductance. This drop varies with the amplitude of the current flowing through it. Thus; for different loading conditions, values of V-curve and inverter V-curve are different but nature of curve remain same. In experimental results switching and conduction losses are present whereas in simulation switches are ideal. Thus, there is a slight difference in the shape of V-curve and inverter V-curve of the NSC for simulation and experimental results.

7. Conclusions

In this paper, the compact AC-DC-AC NSC is used as DSTATCOM and induction motor drive application. The switch count is reduced by 25% as compared to the conventional TSC. The control scheme is developed to operate NSC so as to mimic the operation of SG. The NSC can absorb or deliver reactive power at the PCC with induction motor drive. The NSC with induction motor drive is operated at desired power factor of the PCC. To verify simulation results, an experimental prototype is developed in the laboratory. The V-curve and inverted V-curve is obtained from simulation and experimental results are found similar in nature. Due to the presence of internal resistance of the source inductance and the switching losses in the experimental results, there is a slight difference in the shape of V-curve and inverted V- curve of the simulation and experimental results. The experimental results proved the practicability of the proposed control scheme to operate NSC as DSTATCOM and induction motor drive.

Author Contributions: C.J., M.C. and M.R. developed the concept: C.J. designed and performed the experiments: C.J. and M.C. wrote the paper; M.R. analyzed the data. These authors contributed equally to this work.

Funding: This research received no external funding.

Acknowledgments: Authors acknowledges the VNIT, Nagpur for providing infrastructure support.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations and symbols are used in this manuscript:

DG	Distribution generation
NSC	Nine switch converter
DSTATCOM	Distribution static compensator
TSC	Twelve switch converter
SG	Synchronous generator
PCC	Point of common coupling
FACTS	Flexible Alternating Current Transmission System
V_s	Phase voltage of grid
i_s	Phase current of grid
i_1	Phase current of reactive load connected across NSC
i_a	Phase current of NSC
V_{com}	NSC input phase voltage
V_{inv}	NSC output phase voltage
i_L	NSC output phase current
ϕ_a	Angle between V_s and i_a
ϕ_1	Angle between V_s and i_1
ϕ_0	Angle between V_{inv} and i_L
V_d	DC-link voltage
θ	Instantaneous angle of the grid
δ	Power angle between V_s and V_{com}
Ref_{rec}	Modulation references for rectifier operation
Ref_{inv}	Modulation reference for inverter operation
V_c	Carrier reference
m_r	Modulation index of Ref_{rec} and Ref_{inv} respectively
L_s	Source inductance
R_s	Internal resistance of the source inductor
a,b,c	Input terminals of the NSC
x,y,z	Output terminals of NSC
N	Common point of negative dc-link voltage
V_{aN}	Pole voltage between terminal a and N
V_{xN}	Pole voltage between terminal x and N

Id*	Generated active current reference
Q_{rec}	Reactive power at PCC
Q_{NSC}	Reactive power of NSC
Q_{load}	Reactive power of other load connected across NSC
Q_{ref}	Desired reactive power at PCC
V_{ab1}	Fundamental component of the NSC input line voltage
V_{xy1}	Fundamental component of NSC output line voltage

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On-Line Application of SHEM by Particle Swarm Optimization to Grid-Connected, Three-Phase, Two-Level VSCs with Variable DC Link Voltage

Umut Güvengir [1], Işık Çadırcı [2] and Muammer Ermiş [1,*]

[1] Electrical and Electronics Engineering Department, Middle East Technical University, Ankara TR 06800, Turkey; umut.guvengir@tubitak.gov.tr

[2] Electrical and Electronics Engineering Department, Hacettepe University, Beytepe, Ankara TR 06800, Turkey; cadirci@ee.hacettepe.edu.tr

* Correspondence: ermis@metu.edu.tr; Tel.: +90-312-210-2364

Received: 4 July 2018; Accepted: 16 August 2018; Published: 20 August 2018

Abstract: This paper is devoted to an otablen-line application of the selective harmonic elimination method (SHEM) to three-phase, two-level, grid-connected voltage source converters (VSCs) by particle swarm optimization (PSO). In such systems, active power can be controlled by the phase shift angle, and reactive power by the modulation index, against variations in the direct current (DC) link voltage. Some selected, low-odd-order harmonic components in the line-to-neutral output voltage waveforms are eliminated by calculating the SHEM angle set continuously through the developed PSO algorithm on field-programmable gate array (FPGA)-based computing hardware as the modulation index is varied. The use of powerful computing hardware permits the elimination of all harmonics up to 50th. The cost function of the developed PSO algorithm is formulated by using an optimum number of particles to obtain a global optimum solution with a small fitness value in each half-cycle of the grid voltage and then updating the SHEM angle set at the beginning of the next full-cycle. Since the convergence of the solution to a global minimum point depends upon the use of correct initial values especially for a large number of SHEM angles, a generalized initialization procedure is also described in the paper. Theoretical results are verified initially using hardware co-simulation. They are also tested using a small scale photovoltaic (PV) supply prototype developed specifically for this purpose. It is demonstrated that the 5th, 7th, 11th, 13th, 17th, and 19th sidekick harmonics are eliminated by on-line calculation of seven SHEM angles through the developed PSO algorithm on a moderately powerful XEM6010-LX150, USB-2.0-integrated FPGA module. All control and protection actions and the calculation of SHEM angles are achieved by a single FPGA chip and its peripherals within the FPGA board.

Keywords: field-programmable gate array; particle swarm optimization; selective harmonic elimination method; voltage source converter

1. Introduction

Various modulation schemes have been employed in inverter circuits, such as space vector modulation (SVM), pulse width modulation (PWM), and the selective harmonic elimination method (SHEM). The main feature of the SVM scheme is the fast dynamic response obtained, whereas the SHEM has superior harmonic performance for a given switching frequency. The performance of the best PWM modulation techniques is somewhere between the SVM and SHEM [1]. On-line application of SHEM to voltage source converters (VSCs) for the elimination of low-order output voltage harmonics, however, has not been reported yet in the literature due to the computational overhead of the digital implementation on processors.

In grid-connected VSCs of either two-level or multilevel types, the SHEM angles can be determined by solving a set of nonlinear algebraic equations. The resulting mathematical model contains sinusoidal terms and the number of equations in the model is equal to the number of switching angles. Two main groups of techniques have been presented in the literature to solve these nonlinear equations. Iterative methods, such as the Newton–Raphson method [2,3] and the homotopy algorithm [4–7], are given in the first group. Some other iterative numerical techniques have been proposed in [8–11], and the Walsh-function-based analytical technique has been adopted in [12]. In [13,14], to find the solutions for all modulation indices, theories of resultants and symmetric polynomials have been employed, which are then used to solve the polynomial equations obtained from transcendental equations. It has been shown in [13] that such SHEM equations do not have a solution set for some unfeasible modulation index values of the inverter.

In the second group, SHEM is considered as an optimization problem, which is investigated through evolutionary search algorithms. Evolutionary search algorithms have been used to solve various industrial problems in recent years. Easier solutions can be found to these problems by this way as compared to the analytical methods, and in some cases, they constitute the unique way to find a feasible solution [15]. The global optimum solution can be found by these algorithms for complete elimination of certain harmonics or optimum switching angles can be offered in cases where a feasible solution cannot be found. Some major evolutionary search algorithms which have been applied can be cited as the genetic algorithm (GA) [16–18], particle swarm optimization (PSO) [2,19,20], ant colony optimization [21], the bee algorithm [22], and the bacterial foraging algorithm [23].

Until now, SHEM has been applied off-line in industry applications of grid-connected converters by using lookup tables (LUTs). Among these, distribution-type, two-level static synchronous compensator (STATCOM) systems based on a current source converter (CSC) with a variable direct current (DC) link current are reported in [24–26], two-level voltage source converter (VSC)-based distribution-type STATCOM systems with variable DC link voltages in [27], and a transmission-type cascaded multilevel converter-based STATCOM system with constant DC link voltage in [28,29]. On the other hand, VSCs with variable DC link voltages are widely used in photovoltaic (PV) and traction applications, in which the modulation index value for the VSC changes in a wide range as the DC link voltage varies. In such applications, the off-line SHEM using LUTs for determination of switching angle sets is disadvantageous primarily due to the stepwise control of the modulation index value resulting in minimization of selected harmonics instead of their elimination, and secondarily due to the infeasible region of the solution space [30] and the need for a large LUT storage area [31].

To solve these problems, researchers have searched for an effective way to apply SHEM on-line in order to allow for continuous control of SHEM angles. The generalization ability of an artificial neural network (ANN) has been applied in [30] to cope with this problem. The switching angles have been calculated beforehand for different DC source values using GA, then the switching angles have been determined for different DC link voltage magnitudes at each phase of the multilevel inverter in real-time by adopting the ANN to train the controller. By this way, the ANN can be used instead of a LUT, thus introducing its inherent capability to generalize the solution space into the problem with proper training. In [31], another approach was investigated for on-line applications of SHEM, where an analytical procedure was employed for computation of all pairs of valid switching angles in five-level, H-bridge cascaded inverters. Here, a fully analytical calculation is allowed for the switching angles using Chebyshev polynomials and Waring equations. This procedure can be implemented in real-time using either a digital signal controller, a programmable logic device, or a field-programmable gate array (FPGA), as claimed in [31], due to its limited complexity. On the other hand, digital control techniques applied to voltage source inverters in renewable energy applications were reviewed in [32]. On-line optimal switching frequency selection for grid-connected voltage source inverters was presented in [33].

In this paper, calculation of SHEM angles in real-time is described by using a PSO algorithm, specifically developed for this purpose, and a digital computing hardware. An on-line application of SHEM is important especially for grid-connected inverters with variable DC link voltages in order

to eliminate all odd-order characteristic power system harmonics up to the 50th. The initialization procedure for the PSO algorithm is generalized to ensure the convergence of the solution to a global optimum by assuming that the modulation index, and hence the inverter's output voltage, is initially zero. A timing diagram for the on-line application of SHEM is given in the paper, in which the number of SHEM angles, up to 17, is calculated in each half-cycle of the supply voltage waveform, and the firing instants of all power semiconductors of the grid-connected inverter are updated in the next full-cycle. Keeping the switching pattern constant in each full-cycle avoids the generation of DC component and even-order voltage harmonics. The proposed method is verified by a hardware co-simulation work, and the theoretical results are justified in the field on a small-size photovoltaic (PV) supply by calculating on-line seven SHEM angles on a moderately powerful FPGA board. In the prototype PV supply, active power control is implemented by phase shift angle control, reactive power control by variation of the modulation index, and elimination of selected sidekick voltage harmonics (5th, 7th, 11th, 13th, 17th, and 19th) in the inverter's output phase voltage by SHEM.

2. Problem Description

2.1. Possible Application Areas of SHEM

Possible application areas of SHEM are summarized in Figure 1. The common properties of these applications are: (i) few MVA apparent power rating, (ii) Connection to an available three-phase, medium-voltage grid bus though a dedicated coupling transformer, and (iii) 690 V or 1 kV voltage rating for the grid-side VSC. The application of SHEM is suitable for the gray-shaded converters in Figure 1. In these three-phase, two-level VSCs, either high voltage insulated gate bipolar transistor (HV-IGBT) type or integrated gate commutated thyristor (IGCT) type power semiconductors are used in practice. IGBTs and IGCTs in these converters can be switched, respectively, in the range of 1.5 kHz and 500 Hz in practical applications because of their relatively high switching losses. SHEM best matches the needs of such applications, i.e., minimum harmonic current distortion on the grid side and high conversion efficiency. In the near future, with the advents in SiC power MOSFET technology, these new power semiconductors can be switched at much higher frequencies in such applications. In the systems shown in Figure 1a–c, the DC link voltage is variable depending upon the operating condition. In the system in Figure 1d, the DC link voltage may be kept constant or varies in a narrow range. However, in the systems in Figure 1e,f, the DC link voltage may be varied only for performance concerns.

In most of these applications, the grid-side inverter or rectifier is connected to the grid by using a dedicated coupling transformer as shown in Figure 1. If the leakage reactance of the coupling transformer is not sufficiently large for minimization of total demand distortion (TDD), a small series inductor bank may be connected on the converter side of the system. On the other hand, for small-size systems, the grid connection is achieved by using an LCL filter or its derivatives, since an inductance-only filter is not sufficient to suppress high-order harmonic components which are not eliminated by SHEM.

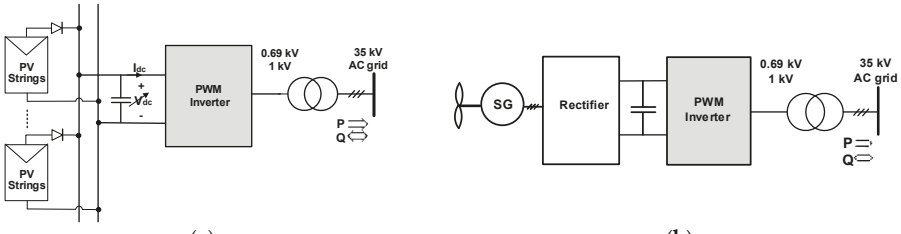

Figure 1. *Cont.*

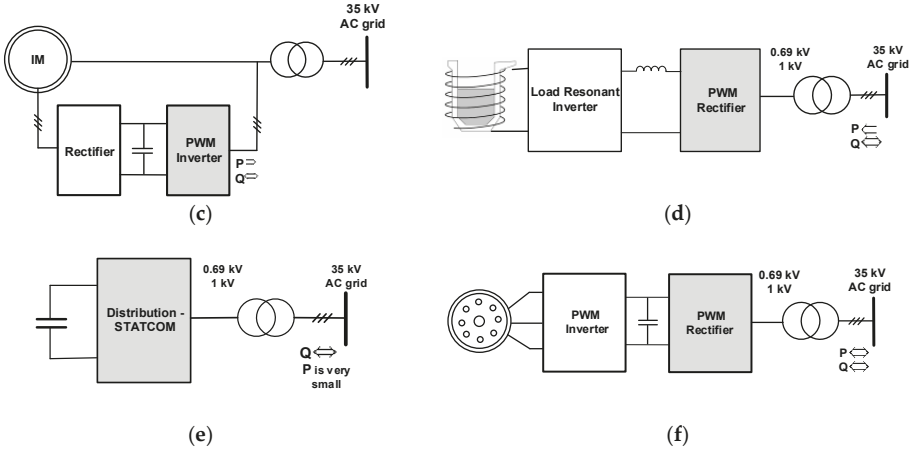

Figure 1. Possible application areas of the selective harmonic elimination method (SHEM) in grid-connected voltage source converter (VSC) applications. (**a**) Single-stage grid-connected photovoltaic (PV) supply, (**b**) wind energy conversion system with a permanent magnet synchronous generator (SG), (**c**) Subsynchronous slip-energy recovery drive or double-output induction generator, (**d**) Medium-power induction melting furnace, (**e**) Distribution static synchronous compensator (STATCOM), and (**f**) Variable frequency alternating current (AC) motor drive. PWM, pulse-width modulator.

2.2. Switching Techniques for SHEM

Various switching techniques that can be used in the application of SHEM are clearly described in [34]. Line-to-line converter voltage harmonics can be directly eliminated by the three-phase line-to-line technique (TLL), and line-to-neutral converter output voltage harmonics by the three-phase line-to-neutral techniques (TLN1 and TLN2). In the TLL technique, a 2 times higher switching frequency and a higher DC link voltage are required in comparison with those of the TLN2 technique in order to eliminate the same number harmonics and to give the same grid voltage. Similar conclusions can be drawn also for the TLN1 technique. In view of PV applications with direct power conversion, the TLN1 and TLN2 techniques are more suitable to maintain the maximum power-point voltage, V_{mpp}, and hence the DC link voltage of the inverter within an acceptable range, e.g., 600–900 V for thin-film PV arrays. On the other hand, TLN1 differs from the TLN2 technique by the number of harmonics to be eliminated from the voltage waveform. This number is even for the TLN1 technique, whereas it is odd for the TLN2 technique. It can be examined from the line-to-neutral voltage waveform in Figure 2 that an odd number of notch angles α_1 to α_5 exists, resulting in the elimination of an even number of characteristic power system harmonics, i.e., the 5th, 7th, 11th, and 13th in the line-to-neutral voltage waveform. In SHEM, the first notch angle is always used to control the fundamental voltage component. Triplen harmonics, such as the 3rd, 9th, and 15th, will be cancelled out in line-to-line voltage waveforms although they are present in line-to-neutral voltage waveforms. There will be no even-order characteristic power system harmonics, such as the 2nd, 4th, 6th, 8th, etc., in line-to-neutral voltage waveforms because of the quarter-wave odd symmetry [24,27,35,36]. The converter's switching frequency f_c can be expressed as in (1) for TLN1 and TLN2 techniques:

$$f_c = (2N+1)f_1 \begin{cases} N \text{ is odd for TLN1} \\ N \text{ is even for TLN2} \end{cases} \quad (1)$$

where, f_1 is the frequency of the fundamental component and N the total number of harmonics to be eliminated, including the fundamental component to be controlled.

If TLN2 were chosen, a higher-order harmonic component, the 13th for $N = 4$ or the 19th for $N = 6$ among the sidekick harmonics (the 11th and 13th for $N = 4$ or the 17th and 19th for $N = 6$) could not be eliminated. Therefore, in this research work, the TLN1 technique is preferred.

The Fourier series expansion of the line-to-neutral voltage waveform in Figure 2 gives the magnitude of the nth characteristic power system harmonic, b_n, obtained from (2).

$$b_n = \frac{4}{n\pi}\frac{V_{dc}}{2}\left[-1 - 2\sum_{k=1}^{N}(-1)^k \cos(n\alpha_k)\right] \tag{2}$$

where, n is the odd harmonic order, V_{dc} the DC link voltage, and α_k the switching angle for $k = \{1, 2, \ldots, N\}$.

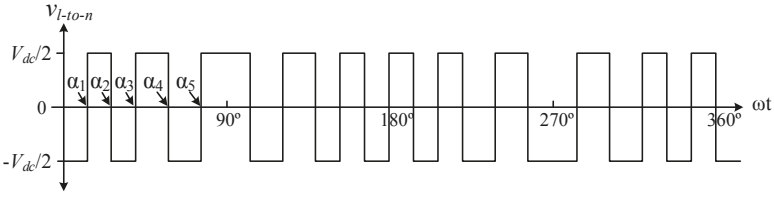

Figure 2. Line-to-neutral voltage in the TLN1 technique for five switching angles.

N transcendental equations with N unknowns ($\alpha_1, \alpha_2, \ldots, \alpha_N$) in (3) are then obtained by setting the fundamental voltage component to a prespecified value and equating the remaining $N - 1$ harmonics all to zero.

$$\begin{bmatrix} 2\cos(\alpha_1) & -2\cos(\alpha_2) & \cdots & 2(-1)^{N+1}\cos(\alpha_N) \\ 2\cos(5\alpha_1) & -2\cos(5\alpha_2) & \cdots & 2(-1)^{N+1}\cos(5\alpha_N) \\ \vdots & \vdots & \ddots & \vdots \\ 2\cos(X\alpha_1) & -2\cos(X\alpha_2) & \cdots & 2(-1)^{N+1}\cos(X\alpha_N) \end{bmatrix} = \begin{bmatrix} 1 + \frac{\pi b_1}{2V_{dc}} \\ 1 \\ \vdots \\ 1 \end{bmatrix} \tag{3}$$

where $X = 3N - 2$ and α constraints $0 < \alpha_1 < \alpha_2 < \cdots < \alpha_N < \frac{\pi}{2}$.

A simultaneous solution of the set of transcendental equations in (3) is necessary to obtain a solution set for α_1 to α_N. Since these equations are nonlinear, either an iterative method or an evolutionary search algorithm is required.

2.3. Need for On-Line SHEM

The technical specifications of a three-phase, two-level, and grid-connected VSC with some selected harmonics eliminated by SHEM are assumed to be as follows.

- It provides conversion of the desired amount of DC power to AC over a wide DC link voltage range, e.g., V_{dc} = 600 V to 900 V for the thin-film PV systems in Figure 1a.
- Active power control is achieved by controlling the phase shift angle, δ, of the VSC output voltage with respect to the supply voltage.
- The reactive power generated or consumed by the VSC should be adjusted to any prespecified value by varying the magnitude of the VSC's output voltage by controlling the modulation index over the entire operating range.

The need for on-line SHEM is justified by carrying out two case studies as given below.

Case Study I: Constant SHEM Angle Set with Variable DC Link Voltage

The three-phase, grid-connected VSC can be represented by the single-line diagram shown in Figure 3.

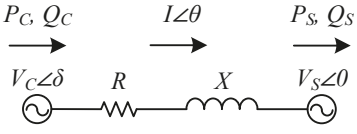

Figure 3. Single-line diagram of the simplified three-phase system.

The output series filter reactor's internal resistance component, R, and/or the coupling transformer's leakage impedance is much smaller than the inductive reactance component, X, and phase-shift angle, δ, between the fundamental component of converter voltage, V_c, and the fundamental component of supply voltage, V_s, phasors is very small, then $sin\delta \approx \delta$ and $cos\delta \approx 1$ [27,36]. Under these assumptions, the active and reactive powers generated by the VSC, (P_c, Q_c), and active and reactive powers consumed by the grid, (P_s, Q_s), can be approximated by expressions in (4) to (6).

$$P_C \cong P_S \cong 3\frac{V_C V_S}{X}\delta \tag{4}$$

$$Q_C \cong 3V_C\frac{V_C - V_S}{X} \tag{5}$$

$$Q_S \cong 3V_S\frac{V_C - V_S}{X} \tag{6}$$

Since V_s and X in (6) are constant, Q_s can be adjusted to any preset value only by controlling V_c. The relationship between the rms value of the fundamental component of the VSC's output voltage, V_c, and the variable DC link voltage, V_{dc}, is given by the modulation index expression in (7). Since M is kept constant for a constant SHEM angle set, as V_{dc} changes there will be no control on V_c and hence on Q_s. Therefore, the use of constant SHEM angles in the control system of grid-connected inverters with variable DC link voltages is to be avoided.

$$M = \frac{\pi\hat{V}_c}{2V_{dc}} = \frac{\pi\sqrt{2}V_c}{2V_{dc}} \tag{7}$$

Case Study II: Off-line SHEM by the Look-Up Table Method

In order to avoid the drawbacks of constant SHEM angles in the reactive power control of grid-connected inverters with variable DC link voltages, M and hence V_c should be adjusted by using several sets of SHEM angles as V_{dc} changes. The common approach to this problem is the computation of several SHEM angle sets and their storage in an internal or external random access memory (RAM)/read-only memory (ROM) in the form of (a) LUT(s). This approach makes necessary the discretization of M control range into d number of steps for N number of total harmonics to be controlled over the entire operation range of the resulting system, which yields a $d \times N$ LUT. Since M and hence SHEM angles α_1 to α_N are controlled stepwise instead of by on-line continuous control, the required value of M at any particular operating point will be rounded to the nearest M number stored in the LUT. This may result in a significant error in V_c and hence Q_s values when the row number, d, of the LUT is kept low. Therefore, d should be as high as possible. A $d \times N$ LUT will be impractical if a huge number of harmonics is to be eliminated.

The effects of the order of a LUT on the discretized values of M, the corresponding V_c, and Q_s for unity power factor operation are examined by considering 5×7 and 41×7 LUTs and the associated

results are given in Table 1 for two different values of DC link voltage ($V_{dc\ (min)}$ = 600 V, $V_{dc\ (max)}$ = 900 V, and X = 3.14 Ω at 50 Hz). In this paper, theoretical results are verified on a sample small-scale PV system as described in Section 4. This small-scale prototype is connected to a 400-V, 50-Hz grid. The performance of real-time SHEM in adjusting M, and hence V_c to its set value of 230 V in order to bring $Q_s = Q_{s(set)}$ to zero is also given in Table 1 for the same problem. As can be understood from the results marked by red colored values in Table 1, V_c and Q_s deviate significantly from their set values in the case of a small-sized LUT. Deviations from the set values can be significantly lowered as the size of the LUT increases (marked by yellow color in Table 1). In order to alleviate the problem arising from the discrete LUT method in variable DC link voltage applications, linear interpolation can be used between consecutive M steps.

Table 1. Errors in Reactive Power Adjustment Arising From Off-line SHEM Based on the Look-Up Table (LUT) Method for Unity Power Factor (PF) Operation.

Parameter	Off-Line SHEM				On-Line SHEM	
	5 × 7 LUT		41 × 7 LUT			
V_{dc} (V)	600	900	600	900	600	900
M (required)	0.852	0.568	0.852	0.568	0.852	0.568
M (realized)	0.9	0.6	0.85	0.57	0.852	0.568
V_C ($V_{rms,\,1-n}$)	243.1	243.1	229.6	230.9	230	230
Q_S (VAr)	2877	2877	−88	198	0	0
P_s (W)	1350	1675	1350	1675	1350	1675
δ (°)	1.449	1.797	1.534	1.892	1.531	1.900

At the present time, with the advances in digital electronics area by using a powerful FPGA module or parallel computing hardware, such as a Graphical Processing Unit (GPU), enormously large SHEM angles can be calculated on-line to control M continuously. The performance of the on-line SHEM by using a single FPGA module to control seven harmonics is also given in Table 1 by the green-colored area.

3. Application of PSO to SHEM

In grid-connected PV inverter applications, since the supply frequency is constant (f_1 = 50 or 60 Hz), SHEM angles should be updated once in a full-cycle (20 or 16.67 ms) with $2\pi/3$ and $4\pi/3$ phase-shifted signals for the remaining two phases. Therefore, on-line calculation of SHEM angles should be carried out in a total execution time less than a period of grid voltage, i.e., 20 ms for 50 Hz applications. However, variable-frequency alternating current (AC) motor drive applications need lower calculation times when the applied motor frequency is higher than the rated frequency. In this research work, the equations in (3) will be solved by the PSO technique, which is an evolutionary search algorithm.

In order to evaluate the fitness values of each particle at each time frame, a cost function should be formulated as required by the PSO. SHEM equations should be put into a format so that each particle is assigned a real fitness value. Then, boundaries of the solution space are defined, and an initial population of swarms is generated in this solution space. Finally, PSO parameters are set, so that the PSO algorithm is ready to find a feasible global optimum to the optimization problem.

3.1. Particle Swarm Optimization (PSO)

The stochastic population-based optimization technique called particle swarm optimization (PSO) has been developed by Dr. Russell Eberhart and Dr. James Kennedy in 1995 [37]. It is initialized with a random or heuristic population which consists of particles such as birds, fish, and insects. Each particle in this research work is a vector composed of seven SHEM angles and in order to assess whether it can be a potential global solution or not, it is evaluated with a fitness function. The particles search the

problem space via cognitive and social interaction by pursuing the current optimum particles. The personal best location (*pbest*) is defined as the coordinates of the particle which is associated with the best personal fitness value acquired so far. The global best location (*gbest*), however, is defined as the location with the best fitness value which all of the population has reached. In each time frame, each particle updates its velocity towards its *pbest* and *gbest* locations. Separate random numbers [38] are employed to weight the total acceleration terms of local and global searches. The velocity, v_i, and position, x_i, update equations are as given in (8) and (9), respectively.

$$v_i(t+1) = K \times \begin{bmatrix} \beta v_i(t) + c_1 \times rand \times (pbest_i(t) - x_i(t)) \\ +c_2 \times rand \times (gbest(t) - x_i(t)) \end{bmatrix} \tag{8}$$

$$x_i(t+1) = x_i(t) + v_i(t+1) \times \Delta t \tag{9}$$

where, β is the inertia weight which dictates the velocity of the particles in the next time frame, the acceleration constants c_1 and c_2 are, respectively, the cognition and social factors which are, respectively, related to the diversification and intensification of the search procedure. *rand* is chosen as a random number between 0 and 1, which defines the explorative capability of the particle over the search space, and K is the constriction factor to guarantee the convergence of the algorithm given in (10), which has been found in [38].

$$K = \frac{2}{\left|2 - \varphi - \sqrt{\varphi^2 - 4\varphi}\right|} \tag{10}$$

where, $\varphi = c_1 + c_2$ and $\varphi > 4$.

Figure 4 shows the basic flowchart of the PSO algorithm. Whenever the global best fitness, f, reaches a value less than a prespecified limit, e.g., $f = 1 \times 10^{-9}$ in this application, the algorithm terminates for each PSO calculation window.

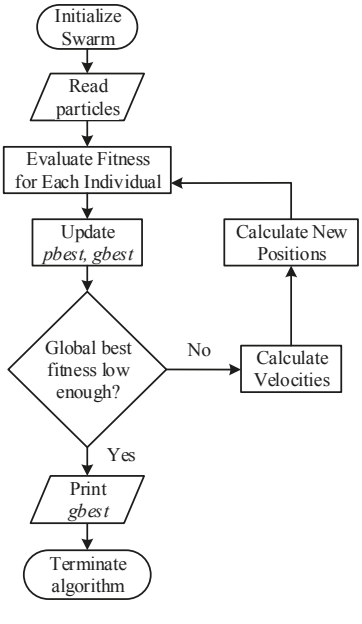

Figure 4. Flowchart of the particle swarm optimization (PSO) algorithm.

3.2. Determination of Cost Function

In this application, the TLN1 technique is chosen to eliminate the six lowest-order sidekick harmonics, given as the 5th, 7th, 11th, 13th, 17th, and 19th, in the output voltage waveform of the inverter since even-order harmonics are not present if an odd quarter-wave symmetric pattern is used, and all triplen harmonics are eliminated in the line-to-line voltages for a three-phase, three-wire system. This results in a switching frequency of 750 Hz. For this sample application, the equation set in (11) is to be solved.

A new set of equations given in (12) is obtained by rearranging equations in (11) and using the M expression given in (7). The cost function T_n, and the fitness value, f, of a SHEM angle set can be expressed by squaring the left hand sides of the equations in (12) and then summing them up as given in (13). In (13), γ should be set to a value higher than 10 to converge the solution more rapidly. Furthermore, T_1 in (12) has crucial importance in determining V_c and hence adjusting Q_s to the prespecified set value.

$$\begin{aligned} b_1 &= \tfrac{4}{\pi}\,\tfrac{V_{dc}}{2}\left[-1-2\sum_{k=1}^{7}(-1)^k\cos(\alpha_k)\right]=\hat{V}_c \\ b_n &= \tfrac{4}{n\pi}\,\tfrac{V_{dc}}{2}\left[-1-2\sum_{k=1}^{7}(-1)^k\cos(n\alpha_k)\right]=0 \end{aligned} \tag{11}$$

where, $\hat{V}_c=\sqrt{2}V_c$ is the peak value of the fundamental line-to-neutral voltage at the inverter output, V_{dc} is the DC link voltage, b_n is the peak value of the nth harmonic component (n = 5, 7, 11, 13, 17, and 19) as given in (2), and α_k is the SHEM angle to be determined for k = 1, 2, . . . , 7.

$$\begin{aligned} T_1 &= -1-\left[2\sum_{k=1}^{7}(-1)^k\cos(\alpha_k)\right]-M=0 \\ T_n &= -1-\left[2\sum_{k=1}^{7}(-1)^k\cos(n\alpha_k)\right]=0 \end{aligned} \tag{12}$$

$$f=\mu(\gamma T_1^2+T_5^2+T_7^2+T_{11}^2+T_{13}^2+T_{17}^2+T_{19}^2) \tag{13}$$

where γ and μ are the penalty values, respectively, for M and the angle constraint in (14).

$$0<\alpha_1<\alpha_2<\alpha_3<\alpha_4<\alpha_5<\alpha_6<\alpha_7<\frac{\pi}{2} \tag{14}$$

μ can be set to 10 for this sample application in order to eliminate invalid SHEM angle sequences rapidly during the on-line application of SHEM.

3.3. Results of the PSO Algorithm

The parameters used in the PSO algorithm are first optimized in the MATLAB environment. Among these, the most important parameters affecting how fast the PSO algorithm converges are the swarm size, s, and the number of time frames, Ntf. The variations in fitness value, f against s, and Ntf are given in Figures 5 and 6, respectively. The ideal value of f is zero. From Figures 5 and 6, the optimum swarm size and number of time frames are chosen to be s = 250 and Ntf = 200, which correspond to a decadic logarithmic error, i.e., $\log_{10} f = -9$. The optimized and default values of all parameters used in the PSO algorithm are as given in Table 2. SHEM angles from α_1 to α_7 are found against M by running the PSO algorithm in the MATLAB environment with optimized parameters in Table 2.

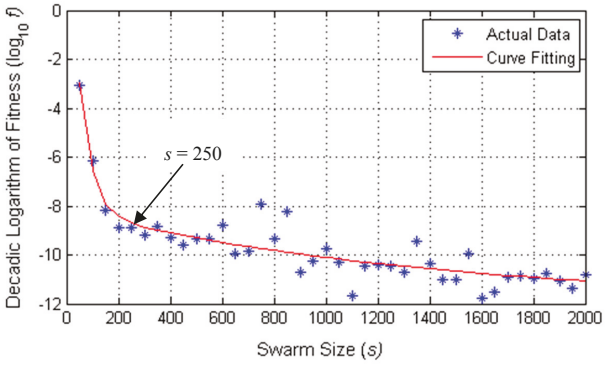

Figure 5. Fitness values expressed as decadic logarithmic error against swarm size.

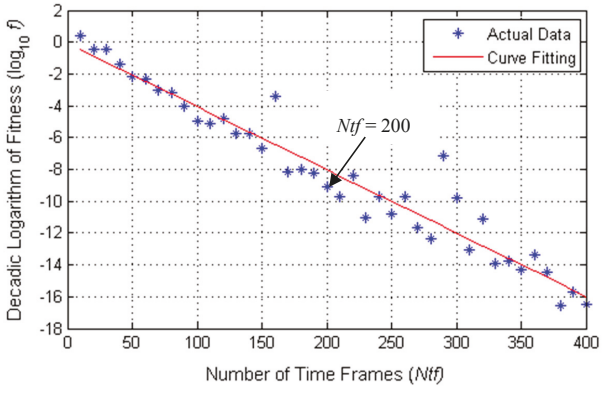

Figure 6. Fitness values expressed as decadic logarithmic error against the number of time frames.

Table 2. Optimized Parameters of PSO Algorithm (optimized parameters are marked by *, and others are default parameters).

Symbol	Parameter	Value
β	Inertia weight	1
c_1	Cognition factor	2.8
c_2	Social factor	1.3
K	Constriction factor	0.729
s	Swarm size *	250
Ntf	Number of time frames *	200
γ	Modulation index penalty *	100
μ	Angle constraint penalty *	10

Random initialization of the PSO algorithm at time $t = 0$ (at start-up) can be made by utilizing the constraints defined for the problem by equating the initial value of M and hence the fundamental component of inverter's output voltage to zero. Randomly chosen initial values usually cause convergence of the solution to a local minimum, especially for large numbers of SHEM angles, N. When the problem is generalized to eliminate all odd-order power system harmonics up to the 50th according to IEEE Std. 519-2014 [39] and IEC 61000-4-30 [40], the initial values of N number of SHEM angles can be distributed in the range of either,

Case (I) from 0 to $\xi = 90°$, or
Case (II) from 0 to $\xi = 60°$,

with respect to the zero crossing point on the rising edge of the fundamental line-to-neutral voltage waveform. Initial values of N number of SHEM angles can therefore be determined from the first equation in (12) by setting M to zero as given in (15).

$$M = -1 + 2\cos(\alpha_1) - 2\cos(\alpha_2) + 2\cos(\alpha_3) - 2\cos(\alpha_4) + \ldots + 2\cos(\alpha_{N-2}) - 2\cos(\alpha_{N-1}) + 2\cos(\alpha_N) = 0 \quad (15)$$

In case (I), the SHEM angles are distributed between 0 and 90°, where the first SHEM angle α_1 is set to zero, and the last angle α_N to 90°. The angles from α_2 to α_{N-1} are distributed to p sections, where $p = (N + 1)/2$, so as to eliminate pairwise the remaining cosine terms in (15). For $N = 7$, in the case study, $\alpha_1 = 0$, $\alpha_2 = \alpha_3 = 15°$, $\alpha_4 = 60°$, $\alpha_5 = \alpha_6 = 75°$, and $\alpha_7 = 90°$. In order to cancel out the first term (−1) in (15), α_4 is set to 60°. Although the initialization procedure with $M = 0$ for case (I) which distributes SHEM angles over the quarter wave from 0 to 90° gives quite accurate results on the PSO algorithm for a low number of harmonics to be eliminated (for $N = 3$, 5, 7, and 9), this is not true for $N > 9$. However, in case (II), the SHEM angles are distributed between 0 and 60°, i.e., the last SHEM angle should be set to 60°, thus canceling the first term in (15). On the other hand, angles α_1 to $\alpha_{N\text{-}1}$ are evenly distributed to $p = (N + 1)/2$ sections so as to cancel pairwise the remaining cosine terms. The generalization procedure for initial values of SHEM angles for case (II) is summarized in Table 3. The initialization procedure in case (II) is simpler and more general than that of case (I).

Table 3. Generalized initialization procedure for SHEM angle sets. (N can be chosen to be any value among 3, 5, 7, . . . , 17; $N = 17$ eliminates all odd-order characteristic power system harmonics up to the 50th).

Initial Values of SHEM Angles, $\alpha_1, \ldots, \alpha_N$ to give $M = 0$							
α_1	α_2	α_3	α_4	α_k	α_{N-2}	α_{N-1}	α_N
$\frac{60}{p}$	$\frac{60}{p}$	$\frac{60}{p} \times 2$	$\frac{60}{p} \times 2$	. . .	$\frac{60}{p} \times (p-1)$	$\frac{60}{p} \times (p-1)$	60°

There may be more than one solution for SHEM angles for any number N between 3 and 17. As an example, for $N = 7$, the optimum values of SHEM angles (α_1, α_2, . . . α_7) and the corresponding fitness values as a function of M are obtained by distributing the initial values in the range from 0 to 90° (case (I)) as given in Table 4. However, Table 5 shows the optimum values of SHEM angles and fitness values for the same problem when the initial values of those angles are chosen according to the generalized procedure in Table 3 (case (II)). As can be understood from Tables 4 and 5, the optimum values of SHEM angles are different for the same problem owing to the use of different initial values. Since the f values are very low, both solutions can be considered to be the global optimum points found by the PSO algorithm.

Much lower f values could be obtained by using time frames higher than 200 (Table 2) at the expense of a longer execution time. In this research work, the results given in Table 4 are used in the implementation.

The control range of M is divided into three subregions:

(a) *Impractical M* values in which the difference between any two consecutive SHEM angles is less than 0.1°. The associated M values and the critical angles are marked by red color boxes in Tables 4 and 5. As an example, the typical turn-off times for 1700 V 300 A SiC power MOSFET and HV IGBT are nearly 0.27 µs and 1.8 µs, respectively. Deadbands of 0.5 µs and 3 µs can be chosen in the implementation for these power semiconductors. These values for deadbands correspond to ~0.01° and ~0.06° for 50-Hz grid applications, respectively. In higher power applications, IGCT (alternatively ETO) requires a nearly 10-µs deadband, which corresponds to ~0.2°. Therefore, operation at $M \geq 0.95$ is impractical for all power semiconductors.

(b) $M \leq 0.10$ and $0.9 \leq M < 0.95$ values are not recommended for implementation especially for Si IGBTs, which are marked by yellow color circles in Tables 4 and 5.

(c) The remaining M control range in Tables 4 and 5 defines safe operating M values.

Table 4. SHEM Angles Found by the PSO Algorithm for $N = 7$ and Case I. (Yellow M: Not recommended, Red M: Impractical).

M	SHEM Angles, Degree							f
	α_1	α_2	α_3	α_4	α_5	α_6	α_7	
0.10	0.48	14.51	14.92	60.83	74.18	75.77	89.28	2.19×10^{-5}
0.20	1.23	14.69	15.54	61.66	73.42	76.62	88.57	4.37×10^{-7}
0.30	1.86	14.56	15.81	62.49	72.63	77.44	87.87	4.02×10^{-8}
0.40	2.52	14.49	16.12	63.33	71.86	78.27	87.18	8.43×10^{-9}
0.50	3.19	14.48	16.47	64.19	71.10	79.13	86.51	4.42×10^{-9}
0.60	3.87	14.51	16.83	65.07	70.37	80.04	85.89	2.51×10^{-9}
0.70	4.56	14.58	17.20	66.01	69.69	81.03	85.35	2.44×10^{-9}
0.80	5.25	14.70	17.59	67.15	69.20	82.26	85.06	4.74×10^{-9}
0.90	5.92	14.88	17.99	69.88	70.35	84.64	85.89	7.50×10^{-5}
0.95	5.94	14.89	17.93	69.24	69.25	88.77	89.27	3.03×10^{-2}

Table 5. SHEM Angles Found by PSO Algorithm for $N = 7$ and Case II. (Yellow M: Not recommended, Red M: Impractical).

M	SHEM Angles, Degree							f
	α_1	α_2	α_3	α_4	α_5	α_6	α_7	
0.10	14.14	15.31	29.14	30.57	44.15	45.76	59.16	2.23×10^{-5}
0.20	13.33	15.68	28.26	31.14	43.24	46.47	58.33	4.94×10^{-7}
0.30	12.48	16.01	27.35	31.69	42.33	47.19	57.48	8.22×10^{-8}
0.40	11.61	16.32	26.41	32.22	41.38	47.92	56.61	1.12×10^{-8}
0.50	10.72	16.59	25.42	32.71	40.39	48.62	55.71	5.52×10^{-9}
0.60	9.80	16.80	24.37	33.13	39.31	49.31	54.78	5.06×10^{-9}
0.70	8.84	16.90	23.21	33.41	38.09	49.92	53.76	3.22×10^{-9}
0.80	7.81	16.77	21.83	33.33	36.53	50.33	52.50	7.14×10^{-9}
0.90	6.56	15.87	19.68	31.60	33.37	48.11	48.63	8.41×10^{-5}
0.95	5.92	14.74	17.79	29.10	30.10	49.09	49.10	2.78×10^{-2}

In order to justify the usefulness of the PSO algorithm and the generalized initialization procedure in applying SHEM for the elimination of odd-order power system harmonics up to the 50th, optimum SHEM angles have been found for $N = 7$, 9, 11, 13, 15, and 17, and sample results corresponding to $M = 0.7$ are given in Table 6. The results of these analyses show that the PSO algorithm can be successfully used in an on-line application of SHEM provided that powerful computing hardware is available for each case.

Table 6. SHEM Angles for $N = 7$, 9, 11, 13, 15, and 17, and $M = 0.7$ Optimized by PSO Usıng the Generalized Initialization Procedure in Table 3.

N	SHEM Angles for M = 0.7, Degree																	f
	α_1	α_2	α_3	α_4	α_5	α_6	α_7	α_8	α_9	α_{10}	α_{11}	α_{12}	α_{13}	α_{14}	α_{15}	α_{16}	α_{17}	
7	8.84	16.90	23.21	33.41	38.09	49.92	53.76	-	-	-	-	-	-	-	-	-	-	3.22×10^{-9}
9	7.15	13.24	18.70	26.20	30.45	39.15	42.56	52.10	55.08	-	-	-	-	-	-	-	-	8.24×10^{-9}
11	5.99	10.88	15.67	21.56	25.44	32.20	35.38	42.85	45.54	53.50	55.94	-	-	-	-	-	-	7.50×10^{-9}
13	5.17	9.23	13.49	18.31	21.86	27.35	30.33	36.39	38.92	45.44	47.66	54.47	56.54	-	-	-	-	9.30×10^{-9}
15	4.54	8.01	11.85	15.91	19.18	23.77	26.56	31.62	34.03	39.48	41.59	47.35	49.24	55.20	56.99	-	-	4.89×10^{-9}
17	4.04	7.08	10.56	14.06	17.09	21.02	23.65	27.96	30.25	34.91	36.93	41.86	43.66	48.81	50.47	55.75	57.34	7.77×10^{-9}

4. On-Line Application of SHEM to a Small-Scale PV Supply

SHEM is applied on-line by PSO to a laboratory prototype of a small-scale PV supply consisting of a two-level, three-phase, and grid-connected IGBT inverter with variable DC link voltage. It performs direct power conversion to the AC grid, and is equipped with a FPGA-based digital control system. If the PV inverter were connected to the PV array via a boost-type DC-DC converter, a DC link voltage control strategy could be adopted for reducing the TDD in grid-connected PV inverters as recommended in [41].

4.1. Description of the Laboratory Prototype

The circuit diagram of the power stage and block diagram of the prototype's FPGA-based controller is given in Figure 7. An IGBT module (SKiiP 12AC12T4V1), a DC link capacitor, and an FPGA board are mounted on a common printed circuit board (PCB). The controller features are (a) elimination of selected harmonics (5th, 7th, 11th, 13th, 17th, and 19th) in the output voltage waveforms of the voltage source inverter (VSI), (b) maximum power-point tracking, and (c) reactive power control. The PCB of the laboratory prototype, the grid connection of the PV inverter through an LCL filter, and the flat-roof mounted thin-film PV arrays are shown in Figure 8.

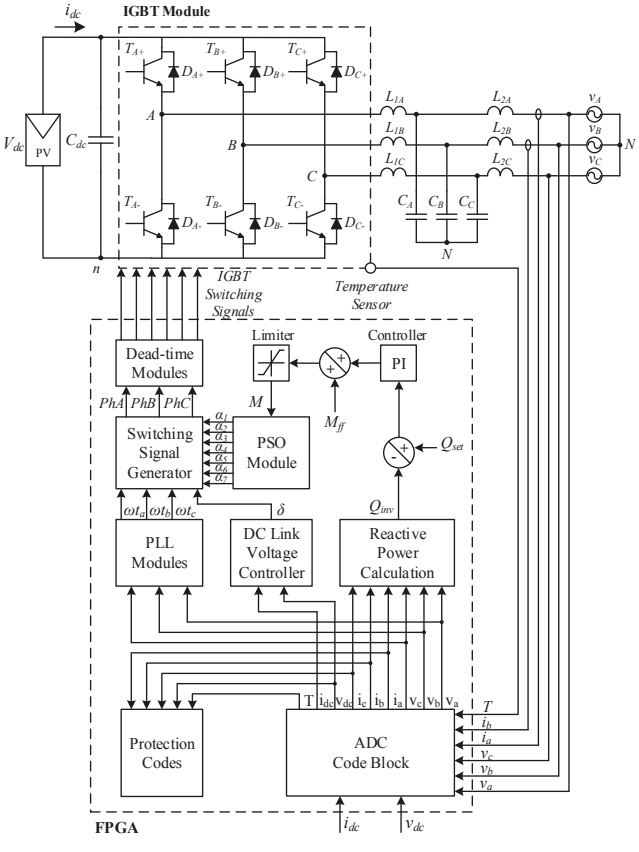

Figure 7. Three-phase two-level grid-connected inverter controlled by a field-programmable gate array (FPGA). ADC, analog-to-digital converter.

In order to implement the worst operating condition in the laboratory, i.e., a step change in V_{dc} from 600 V to 900 V, the power stage is supplied from a solar simulator (Chroma 62150H-1000S) and Q_{set} in Figure 7 is set to zero for unity power factor operation. However, for steady-state operation, the power stage is supplied from the thin-film PV array shown in Figure 8c.

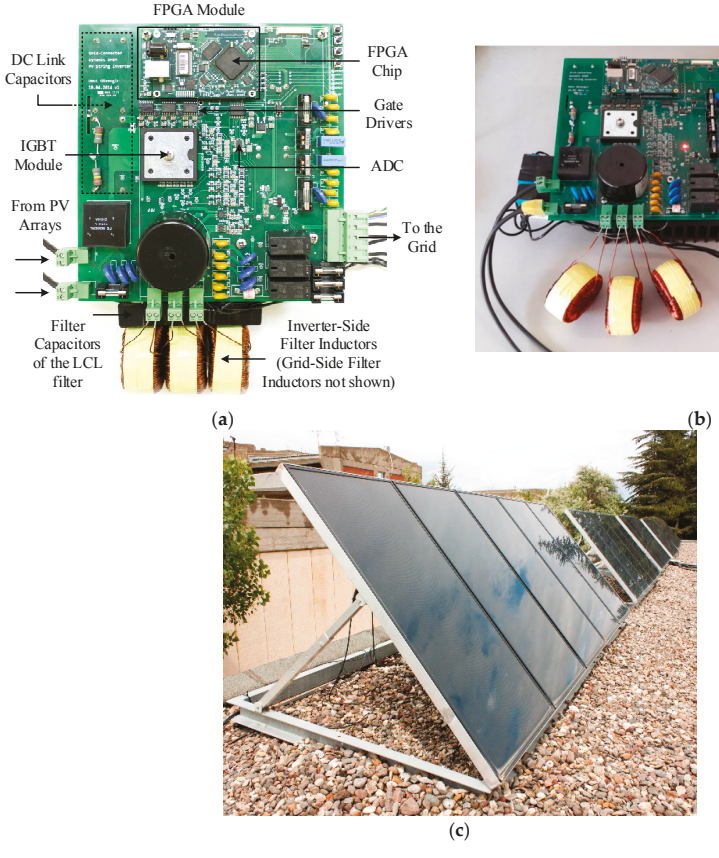

Figure 8. Experimental setup. (**a**) Power stage and controller (206 × 196 mm double-layer printed circuit board (PCB)), (**b**) Grid connection of PV inverter through an LCL filter, (**c**) Two strings of the thin-film PV panels used in the experiments.

4.2. FPGA Implementation of On-Line SHEM

In order to apply the on-line SHEM to the grid-connected, two-level, three-phase VSI, powerful computing hardware having very fast computational capability, a parallel operation ability, and a sufficient number of input/output (I/O) ports is required. In the sample application, all calculation steps of the seven SHEM angles by the PSO algorithm and the necessary control actions should be completed in a time period of less than a complete cycle (20 ms for a 50-Hz application). The numbers of digital inputs to the computing hardware and outputs which will be applied to the gate driver circuits of the power stage are, respectively, 8 and 6 as shown in Figure 7. The timing diagram in Figure 9 summarizes the operational principles of the sample system in Figure 7, including all control actions and on-line application of SHEM. All of these functions are performed by only one common FPGA board. The phase-locked loop (PLL) modules of all phases run for each 20-µs period. The instantaneous

reactive power, Q_{inv}, is calculated in each 20-µs period to update M. The PSO module is running in synchronism with the phase A supply line-to-neutral voltage waveform to calculate SHEM angles in every positive half-cycle of v_{an}. New SHEM angles for the power semiconductors of the inverter circuit are then updated only once in the next full-cycles of the v_{cn}, v_{an}, and v_{bn} voltage waveforms successively in order to avoid generation of DC and even-order voltage harmonics. On the other hand, the MPPT algorithm runs continuously to update δ every second.

In this research work, an XEM6010-LX150 USB-2.0-integrated FPGA module from Opal Kelly is chosen in the implementation which satisfies the requirements mentioned above [42]. This module consists of a Xilinx Spartan-6 XC6SLX150-2FGG484 FPGA to perform all control actions of the VSI together with an analog-to-digital converter (ADC) µchip (ADC128S102) [43].

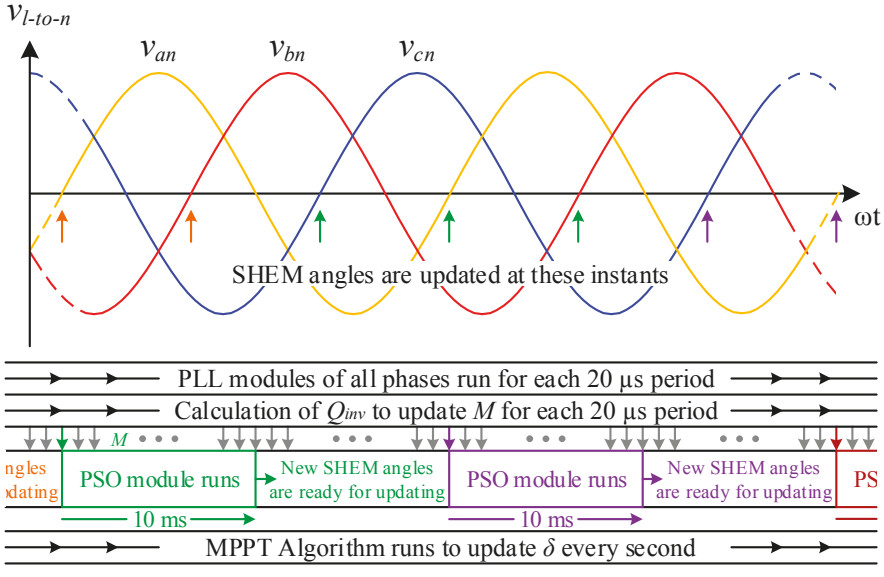

Figure 9. Timing diagram illustrating all control actions and on-line application of SHEM for the sample system in Figure 7.

The implementation of the on-line SHEM was realized by utilizing a fixed-point library in the very high level design language (VHDL) code. The developed software is composed of two parts, one of which performs calculations sequentially, while the other carries out parallel operations. VHDL code runs at a 10 MHz system clock frequency, while the RAM blocks should run at a maximum 30 MHz clock frequency in order to be able to follow the operations in one clock period. The flow of the PSO algorithm is as illustrated in Figure 10. In this research work, it is aimed at determining SHEM angles α_1 to α_7 in a time period less than or equal to 10 ms. For this purpose, the 10 ms time period is divided into 200 time frames. Each time frame can be considered as an iteration in two steps, A and B. Therefore, each iteration will take 50 µs of time. In the first phase, A, in Figure 10 of each iteration, (12)–(14) are solved in a consecutive manner for 250 individuals, whereas for each individual the same equations are solved simultaneously. Each iteration in phase A utilizes values for SHEM angles obtained in phase B in the previous iteration as being their initial values.

At the end of phase A of each iteration, the *pbest* values in (8) for 250 individuals and the *gbest* value in (8) for the population are calculated. As can be seen from the velocity update Equation (8), the algorithm uses two random numbers between 0 and 1 for random searching of particles in the search

space. For this reason, random number generation has been employed in the VHDL code by using a pseudo random number generator (PRNG) [44].

A linear feedback shift register (LFSR) is a PRNG using sequential shift registers to produce binary random numbers in a certain periodic sequence, whose period can be increased by using more registers. Therefore, a more random sequence with respect to the frame of the algorithm can be acquired [45]. A 12-bit LFSR was used for this purpose in the code. In phase B of the same iteration, the velocity in (8) and new positions in (9), i.e., new α_1 to α_7, are calculated for each individual consecutively. The new positions for 250 individuals will then be applied to the phase A of the next iteration as the initial values. In phase A of the last iteration step, the 200th iteration, 250 SHEM angle sets, one for each individual, are obtained and among these the one having the lowest fitness value (*gbest*) is chosen as the solution of the problem in phase S of the 200th time frame in Figure 10. These are the updated SHEM angles (e.g., those calculated in the green-colored PSO module box in Figure 9) that will be applied to gate driver circuits of the power stage in the next full-cycles of the v_{cn}, v_{an}, and v_{bn} voltages as illustrated by green-colored arrows in Figure 9.

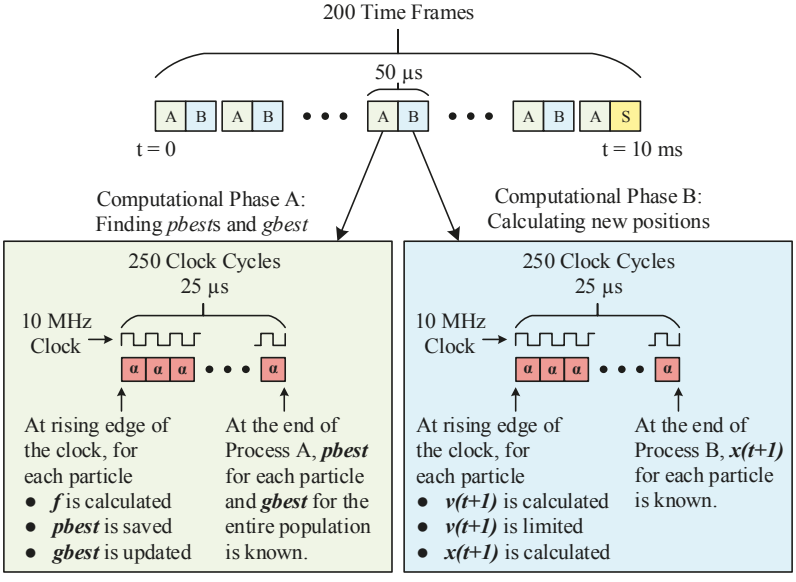

Figure 10. Implementation of the PSO module.

In the next positive half-cycle of the line-to-neutral voltage v_{an} (e.g., the violet-colored PSO module box in Figure 9), the PSO algorithm starts to run afresh regardless of whether the value of M remains the same or not. The PSO algorithm is initialized according to the lattice diagram given in Figure 11. Note that this diagram is a generalized one to cover all possibilities for N from 3 to 17. The first individual is the swarm leader, which tends to guide other individuals towards the solution. To initialize the PSO algorithm in the new positive half-cycle, the first individual utilizes the final values of the SHEM angles α_1 to α_N calculated in the previous positive half-cycle as the initial values of α_1 to α_N.

Only the initial value vectors corresponding to the 2nd and 250th individuals are marked on Figure 11, while the others are evenly distributed according to the lattice structure. The maximum SHEM angle ξ can be chosen as either 60° or 90°. In the prototype system, $N = 7$ and $\xi = 90°$ were used. The performance of the FPGA implementation of on-line SHEM is verified in the following subsection experimentally by applying a step variation to M from 0.1 to 0.9.

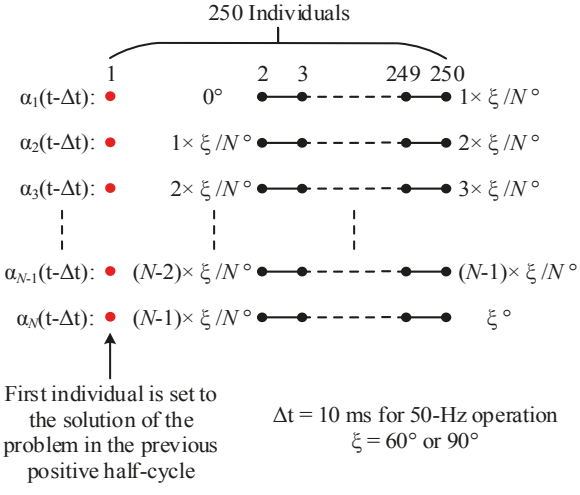

Figure 11. Generalized lattice structure used for population initialization in each positive half-cycle of line-to-neutral voltage.

4.3. Hardware Co-Simulation Results

The FPGA program written in VHDL code is run in real-time to determine the system clock frequency limits and to verify the correct operation of primarily the PSO submodule and secondarily the PLL, DC link voltage controller, and reactive power calculation submodules via Opal Kelly's FrontPanel interface. In order to observe the performance of the on-line application of SHEM, a step change is given to M from 0.1 to 0.9 in the PSO module and the resulting responses of the SHEM angles α_1 to α_7 are recorded by using a digital storage oscilloscope (DSO) through digital-to-analog converters (DACs). The step change in M from 0.1 to 0.9 corresponds to a variation in V_{dc} much wider than 900 to 600 V. This is because M would vary in the range from 0.5 to 0.9 for a V_{dc} variation range from 900 V to 600 V in the field application.

The responses of the PSO module against the step change in M are as given in Figure 12 in both the transient-state and the steady-state. The 10-ms window, which corresponds to a half-cycle of 50 Hz grid voltage, is marked by a blue-colored pulse. Steady-state values of SHEM angles read on the DSO screen for M = 0.1 and 0.9 are also marked by purple-colored pulses on the records given in Figure 12. These records show that on-line calculation of SHEM angles by the PSO algorithm works rapidly and successfully, and in nearly 5 ms of time the SHEM angles α_1 to α_7 reach their final values even for a drastic step variation of M from 0.1 to 0.9.

In the hardware co-simulation test, the SHEM angles determined by the PSO module are also captured from Opal Kelly's FrontPanel interface for different values of M in the range from 0.1 to 0.9 as given in Table 7. It is worth noting that the SHEM angles in Table 7 are more accurate than the corresponding DSO readings. That is the main reason why the steady-state values of SHEM angles for M = 0.1 and 0.9 in Figure 12 are slightly different from the corresponding values in Table 7. Fitness values of SHEM angle calculations against M variations are given in the last column of Table 7.

In the implemented system, higher f values have been obtained in comparison with the target fitness value of $f = 1 \times 10^{-9}$ in Figures 5 and 6. This is attributed to the fact that the random number generator in the FPGA module is implemented to produce 12-bit random numbers and SHEM angles are realized as 24-bit fixed-point logic vectors. Twenty-four-bit random number generation and 32-bit fixed-point logic vector usage would give much lower f values. Nevertheless, when the SHEM angles calculated by the FPGA and corresponding to the worst case fitness value of 2.489×10^{-4} in Table 7

are applied to the MATLAB model of the PV supply, the individual low-order 5th, 7th, 11th, 13th, 17th, and 19th harmonic contents of the output line-to-line voltage waveform are found to be less than 0.5% with respect to the fundamental value. Thus, the fitness values in Table 7 are found to be quite acceptable in this application.

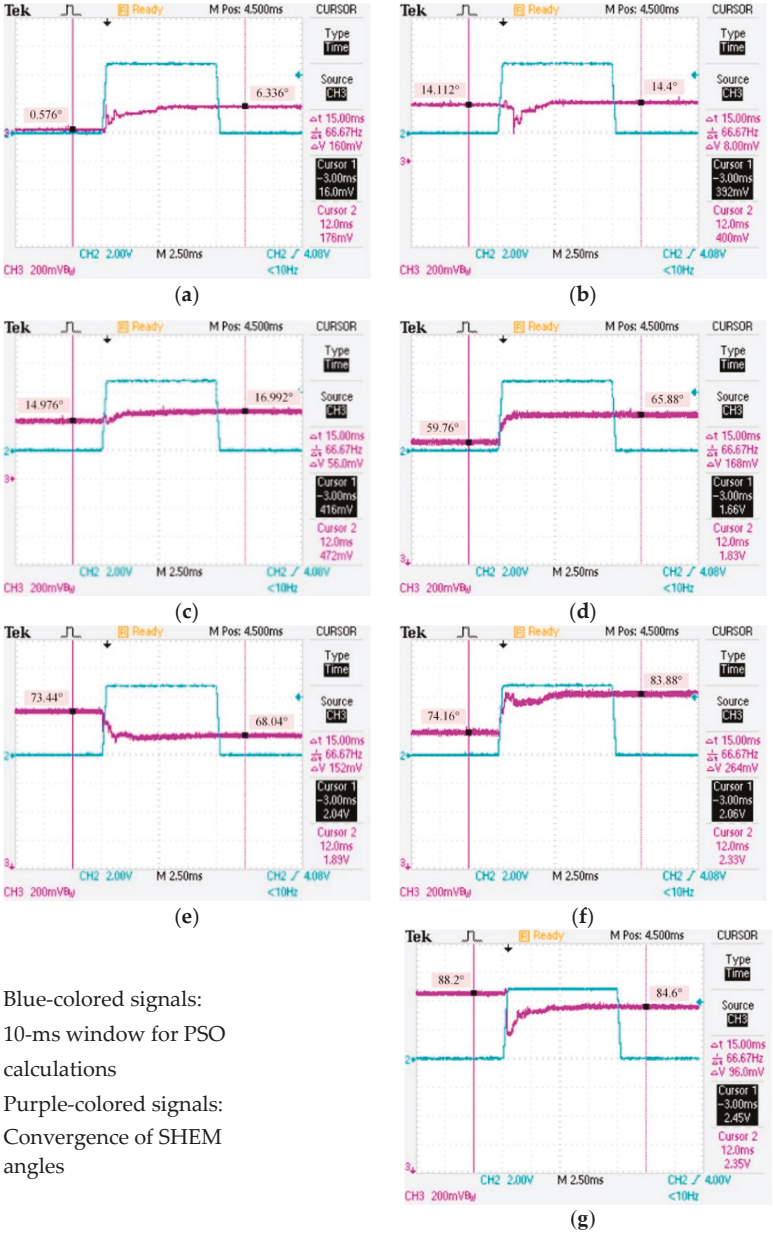

Figure 12. Online calculation of SHEM angles for a step change in M from $M = 0.1$ to 0.9. (**a**) α_1, (**b**) α_2, (**c**) α_3, (**d**) α_4, (**e**) α_5, (**f**) α_6, (**g**) α_7 (5 V $\equiv$ 180°).

Table 7. SHEM Angles Found by Hardware Co-simulation.

M	$\alpha_1(^\circ)$	$\alpha_2(^\circ)$	$\alpha_3(^\circ)$	$\alpha_4(^\circ)$	$\alpha_5(^\circ)$	$\alpha_6(^\circ)$	$\alpha_7(^\circ)$	f
0.10	0.541	14.606	15.018	60.805	74.234	75.794	89.289	1.216×10^{-5}
0.20	1.217	14.677	15.524	61.637	73.439	76.619	88.583	2.384×10^{-7}
0.30	1.864	14.583	15.838	62.481	72.649	77.441	87.868	1.192×10^{-6}
0.40	2.544	14.522	16.188	63.347	71.843	78.293	87.170	2.408×10^{-5}
0.50	3.154	14.612	16.429	64.168	71.110	79.115	86.521	1.860×10^{-5}
0.60	3.843	14.510	16.816	65.048	70.391	80.003	85.916	7.153×10^{-7}
0.70	4.555	14.590	17.219	66.012	69.694	81.034	85.359	1.907×10^{-6}
0.80	5.253	14.728	17.616	67.138	69.186	82.275	85.053	1.907×10^{-6}
0.90	5.895	14.865	17.923	70.053	70.572	84.427	85.767	2.489×10^{-4}

4.4. Limitations of Computing Hardware in On-line Application of SHEM

In this research work, on-line application of SHEM is implemented by using a XEM6010-LX150 USB-2.0-integrated FPGA module containing a Xilinx Spartan-6 XC6SLX150-2FGG484 FPGA to calculate seven SHEM angles continuously. Table 8 shows the utilization report of the chosen FPGA while running only the PSO code and also the total code including all control and protection actions. As can be understood from the last row of Table 8, the chosen FPGA is working at its limit from the viewpoint of the number of DSP48A1 slices. Each DSP slice contains an 18-bit × 18-bit multiplier and a 48-bit accumulator to perform high-performance arithmetic and signal-processing actions.

Table 8. Utilization report of FPGA Used in the Experimental System to Calculate Seven SHEM Angles in Real-Time.

Slice Logic Utilization	Available Number	Used		Utilization	
		PSO Code	Total Code	PSO Code	Total Code
Slice Registers	184304	5080	9920	2%	5%
Slice LUTs	92152	8142	32794	8%	35%
Fully-Used LUT-FF Pairs	37683	2652	5031	7%	13%
Bonded IOBs	338	24	57	7%	16%
Block RAM/FIFO	268	84	104	31%	38%
BUFG/BUFGCTRL/BUFHCEs	16	2	3	12%	18%
DSP48A1s	180	105	177	58%	98%

One hundred and five DSP slices have been used to run the PSO code and 177 of the available 180 DSP slices have been used to run the total code in each half-cycle of the supply voltage waveform. It is obvious that in order to calculate a higher number of SHEM angles up to 17, high-performance computing is required. This can be achieved either by (a) using a much more powerful FPGA chip, which has much higher DSP slices, such as 740, 1920, and 3600, than the one used in the research work, (b) operating more than one moderately powerful FPGA for parallel computing, or (c) using a proper GPU together with a real-time operating system.

4.5. Field Test Results

The field performance of the real-time SHEM angle calculations by the PSO algorithm has been obtained on the prototype of a small-scale, grid-connected PV supply in Figure 8a with direct DC-to-AC conversion. Line-to-line voltage waveforms of the PV inverter and the corresponding harmonic voltage spectra are given in Figures 13 and 14 when $V_{mpp} = V_{dc} = 560$ V and 667 V, respectively. These results show that the recommended method eliminates the target low-order harmonics ($n \leq 19$) successfully. For elimination of all odd-order harmonics up to the 49th, 17 SHEM angles, instead of seven, are to be calculated on-line by using a PSO algorithm with higher computational complexity and more powerful digital computing hardware. This would increase the switching frequency from 750 Hz to 1750 Hz according to (1).

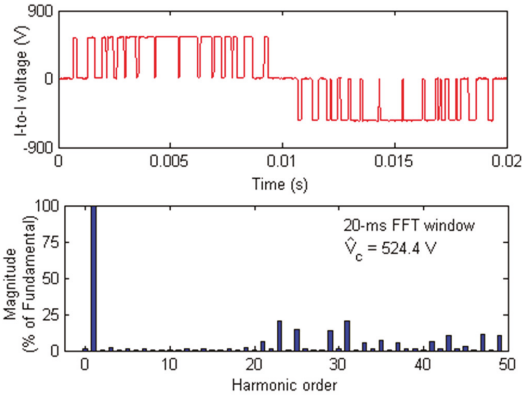

Figure 13. Line-to-line (l-to-l) voltage output of the VSC at the top when V_{dc} = 560 V, and its harmonic spectrum at the bottom.

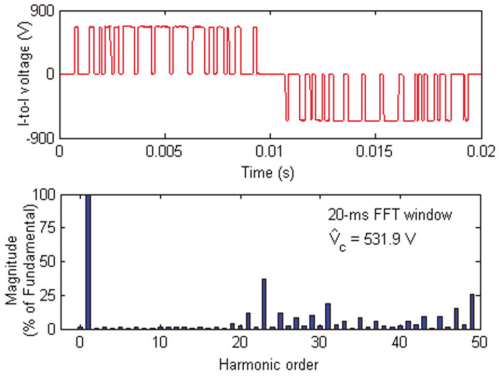

Figure 14. Line-to-line (l-to-l) voltage output of the VSC at the top when V_{dc} = 667 V, and its harmonic spectrum at the bottom.

The 400-V line-to-line grid bus to which the prototype PV supply delivers power is slightly distorted (THD $\cong$ 1.8%) owing to the presence of the 3rd, 5th, and 7th harmonic voltage components. The line current waveform injected into the grid and its harmonic spectrum are as shown in Figure 15 when the PV supply delivers 800 VA to the grid at 0.8 p.f. lagging (the inverter is operating in its capacitive region). Although the TDD of the line current for the given test conditions is 4.1%, it contains some low-order harmonics, such as the 3rd, 5th, and 7th, which are not produced by the PV inverter, but sinked by the LCL filter tuned to 291 Hz and connected to the grid terminals. Harmonic current contributions of the PV inverter and the grid can be separated by using the method recommended in [46,47]. If the grid voltage waveform were a less distorted one, the TDD of the line current waveform would be much lower than 5%.

Since the reactive power delivered to the grid is determined by Q control loop and SHEM angles, and hence the magnitude of the fundamental component of the inverter's output voltage, the performance of the resulting system is tested in the field for different Q_{set} values. Since in this application of instantaneous p-q theory only the average values of v_d, v_q, i_d, and i_q are taken into account, Q and Q_{set} are the actual and set values of the reactive power at 50-Hz supply frequency, respectively. Figure 16 shows the readings of an energy analyzer corresponding to Q_{set} = 0 and Q_{set} =

500 VAr. In these snapshots, the apparent power and active power readings include also harmonic effects, while the Q values are calculated only from the fundamental components. These results show the success of the PSO module, DC link voltage, and reactive power controller blocks.

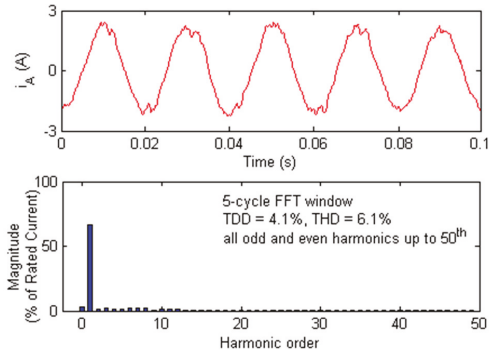

Figure 15. Grid-side line current of PV supply at the top, and its harmonic spectrum at the bottom when delivering 800 VA to the grid at V_{dc} = 667 V. TDD, total demand distortion.

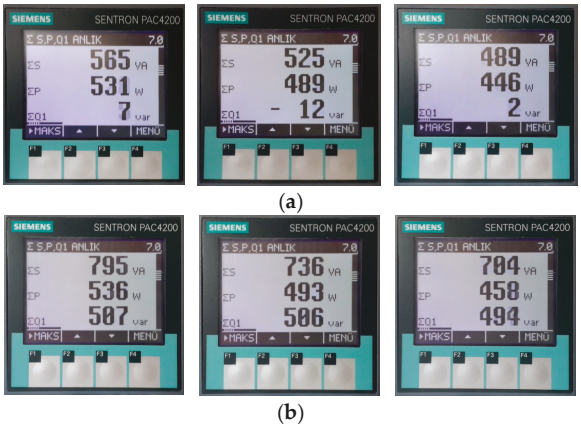

Figure 16. Field records of energy analyzer. (**a**) Q_{set} = 0, and (**b**) Q_{set} = 500 VAr.

5. Conclusions

An off-line application of SHEM provides stepwise control of SHEM angles resulting in minimization of the selected harmonic components instead of their elimination. However, in the on-line application, switching angle sets can be continuously controlled by on-line calculation of SHEM angles, resulting in much better harmonic elimination performance and minimization of THDs. As reported in this paper for the first time, the six low, odd-order voltage harmonics of a grid-connected VSI with variable DC link voltage in a small-scale PV supply are eliminated on-line by using the developed PSO algorithm running on am FPGA controller successfully. The global best solution of the PSO algorithm is obtained with 250 individual particles, i.e., switching angle sets, within 200 time frames, resulting in a relatively small fitness value in the range from 10^{-7} to 10^{-4} depending on the modulation index, M. For a step change in M, all switching angles converge to the solution within a time period less than one half-cycle of the grid voltage, thus updating the switching instants of power semiconductors in every full-cycle of the output voltage.

In order to eliminate all voltage harmonics up to the 50th continuously and rapidly, very powerful digital computing hardware is needed. This is an important requirement especially for variable frequency traction and industrial AC motor drives, where the motor drive is to be operated frequently at frequencies much higher than the rated frequency. In general, the maximum number of harmonics that can be eliminated or minimized in SHEM applications is dictated by the operational capabilities of power semiconductors employed in the VSC, such as the optimum switching frequency and turn-on and turn-off times. As an example, an SiC power MOSFET, as a wide-band-gap device permits the elimination of a number of harmonics much higher than that of IGBT-based VSCs in an on-line application of SHEM. Each recorded harmonic is the vectorial sum of the harmonic current component injected by the PV supply, and the associated one sinked by the LCL filter from the grid. Therefore, the harmonic current contribution of the prototype system can be assessed only by using a proper measurement and calculation method. On the other hand, the elimination of a much higher number of harmonics at the expense of a higher switching frequency would reduce significantly the size of the LCL filter and hence the amount of low-order harmonics sinked from the grid.

Author Contributions: U.G. carried out all necessary derivations and implemented the FPGA-based grid-connected inverter operated by SHEM. M.E. and I.Ç. conceived of the presented idea and contributed to the application of SHEM to the grid-connected PV inverter. All authors discussed the results and contributed to the final manuscript.

Funding: This research received no external funding

Acknowledgments: The PV panels and all electronic components used in this research work were provided by the TÜBİTAK MAM Energy Institute, Ankara Branch.

Conflicts of Interest: The authors declare no conflict of interest

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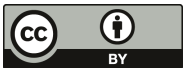

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Review

Control Strategies of Mitigating Dead-time Effect on Power Converters: An Overview

Yi Ji [1], Yong Yang [1], Jiale Zhou [1], Hao Ding [1], Xiaoqiang Guo [1,*] and Sanjeevikumar Padmanaban [2]

[1] Department of Electrical Engineering, Yanshan University, Qinhuangdao 066004, China; an_orange123@163.com (Y.J.); dryangyong@126.com (Y.Y.); zjl_ysu@163.com (J.Z.); dinghao@ysu.edu.cn (H.D.)

[2] Department of Energy Technology, Aalborg University, 6700 Esbjerg, Denmark; san@et.aau.dk

* Correspondence: gxq@ysu.edu.cn; Tel.: +86-137-8507-0194

Received: 24 December 2018; Accepted: 26 January 2019; Published: 8 February 2019

Abstract: To prevent short-circuits between the upper and lower switches of power converters from over-current protection, the dead time is mandatory in the switching gating signal for voltage source converters. However, this results in many negative effects on system operations, such as output voltage and current distortions (e.g., increased level of fifth and seventh harmonics), zero-current-clamping phenomenon, and output fundamental-frequency voltage reduction. Many solutions have been presented to cope with this problem. First, the dead-time effect is analyzed by taking into account factors such as the zero-clamping phenomenon, voltage drops on diodes and transistors, and the parameters of inverter loads, as well as the parasitic nature of semiconductor switches. Second, the state-of-the-art dead-time compensation algorithms are presented in this paper. Third, the advantages and disadvantages of existing algorithms are discussed, together with the future trends of dead-time compensation algorithms. This article provides a complete scenario of dead-time compensation with control strategies for voltage source converters for researchers to identify suitable solutions based on demand and application.

Keywords: dead-time compensation; power converters; harmonics

1. Introduction

Power converters are widely used in industrial applications, such as photovoltaic (PV) power systems [1], adjustable speed drive systems [2], and wind energy systems [3]. With the development of power electronics technology and switching power devices, more advanced converters are receiving widespread attention. A dual output single-phase current source inverter has been proposed for microgrid applications. It utilizes six switches to handle power flows to two independent loads with the same or different voltage ratings [4]. The interaction of the cyber twin model by a cyber integration layer with the physical device is needed for effective control of the system. The interest in grid-tied PV transformer-less inverters has increased rapidly because of their higher efficiency and lower cost compared to traditional line transformer inverters. Some new transformer-less have been proposed such as ESI [5], CH5 [6]. The results show that the novel topologies change the common-mode behavior, which consequently allows a significant reduction of ground leakage current. On the other hand, the high-frequency-based medium voltage inverters are used in renewable energy. However, the power quality is compromised as a result of the increase in common mode noise currents by the high inter-winding parasitic capacitance in high-frequency link transformers. To solve this problem, the modified design of a toroid ferrite core transformer offers more resistance to temperature increases without the use of any cooling agent or external circuitry power sources for power transmission [7].

In practice, the power switches (e.g., Insulated Gate Bipolar Transistor (IGBT)) of the voltage source converter have non-ideal features, such as rising and falling time. In order to avoid short circuits of power switches, the dead time is mandatory for operating voltage source converters [8,9], that is, a dead time is set between the driving signals of the upper and lower switches on each bridge arm. In the case of a single pulse, the dead-time effect is not obvious in a speed control system with a low carrier frequency and low performance requirement. However, the dead-time effect in one cycle has a cumulative effect. When the converter operates at low speed and high switching frequency, the accumulated dead-time effect will cause the voltage and current to contain a large number of harmonic components, and will generate a zero-current-clamping phenomenon. The greater the switching frequency is, the more adverse this phenomenon is. Moreover, in the case of frequency conversion, the speed regulation and dead-time effect causes the motor to generate a large pulsating torque and additional loss. Therefore, the dead-time compensation is one of the most important issues for power converters.

There are two kinds of algorithms for dead-time compensation. One compensates by both software and hardware. The hardware detection circuit is used to judge whether the anti-parallel diode is turned on for the current direction detection. The compensated voltage signal is obtained by comparing the actual voltage and voltage reference. Software is used for the compensation algorithm. The major limitation of this method is that the reliability of the hardware detection circuit cannot be guaranteed, and the complexity of the system is increased. The other method is to simply use the software compensation algorithms only. This kind of method does not require a hardware detection circuit, and is simple and flexible for practical implementations. The classification of the dead-time compensation methods is shown in Figure 1. In general, dead-time compensation methods are divided into three methods: time compensation method; average voltage compensation method; and other methods, which use existing mature modulation technologies. Among these, the time compensation method is most widely used, with other methods using closed loop control.

The remainder of the paper is organized as follows. First, the dead-time effects on the harmonics of the output voltage are elaborated. Second, the different dead-time compensation methods are classified and summarized in detail, and the advantages and disadvantages of various methods are discussed.

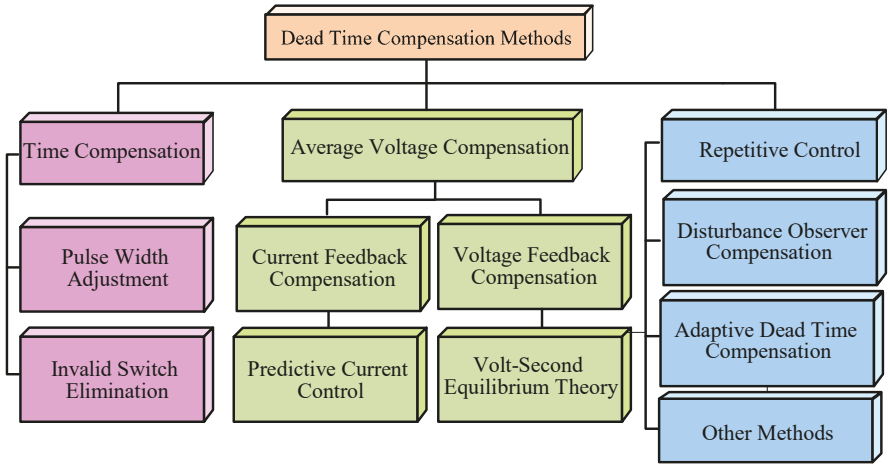

Figure 1. Classification of dead-time compensation algorithms.

2. Dead-time Effect Analysis

In practice, there are voltage source converters [10] and current source converters [11]. The former is the main topic of this paper. Assuming that when the current flows into the grid, the direction is positive, the driving signal waveform and output voltage waveform of the power switch are shown in Figure 2. The elements of Figure 2 are as follows:

Figure 2a is the waveform of the switch driving signal in the ideal state without dead time.

Figure 2b is the waveform of the switch driving signal with a dead-time state.

Figure 2c is the ideal waveform of the output voltage.

Figure 2d is the actual waveform of the output voltage when $i > 0$.

Figure 2e is the actual waveform of the output voltage when $i < 0$.

Figure 3 takes phase A as an example to analyze the effect of dead time on the output voltage and current.

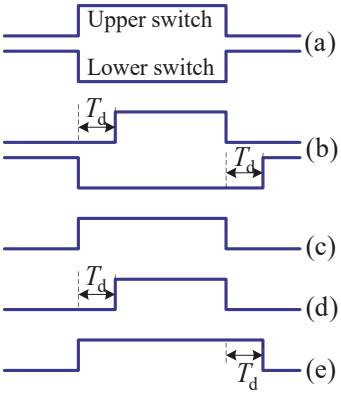

Figure 2. Power switch device driving waveform and output voltage waveform.

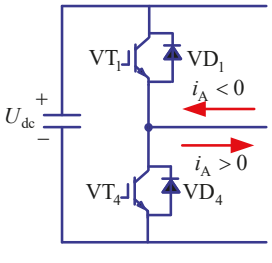

Figure 3. Phase a of voltage source inverter.

2.1. Effect of Dead Time on Output Voltage

From Figure 2, it is clear that there is an error between the actual and ideal values of the output voltage. The error voltage of phase A can be obtained as follows, where T_d is the dead-time, and f_c is the switching frequency:

$$\Delta u_A = \begin{cases} f_c T_d U_{dc} & i_A > 0 \\ -f_c T_d U_{dc} & i_A < 0 \end{cases} \quad (1)$$

Three-phase phase voltage errors can be analyzed from the Fourier series point of view, as shown in Equation (2), where $n = 1, 3, 5, 7, 11, 13, \ldots$, and ω is the angular frequency of the output voltage.

$$\begin{cases} \Delta U_{\mathrm{AN}} = \frac{4}{\pi} f_c T_d U_{\mathrm{dc}} \sum_n^{\infty} \frac{1}{n} \sin(n\omega t) \\ \Delta U_{\mathrm{BN}} = \frac{4}{\pi} f_c T_d U_{\mathrm{dc}} \sum_n^{\infty} \frac{1}{n} \sin\left[n\left(\omega t - \frac{2}{3}\pi\right)\right] \\ \Delta U_{\mathrm{CN}} = \frac{4}{\pi} f_c T_d U_{\mathrm{dc}} \sum_n^{\infty} \frac{1}{n} \sin\left[n\left(\omega t - \frac{4}{3}\pi\right)\right] \end{cases} \tag{2}$$

The output voltage of phase A by taking the dead-time effect into account can be expressed as:

$$\begin{aligned} U_{\mathrm{A0}} &= M U_{\mathrm{dc}} \sin(\omega t + \varphi) + \Delta U_{\mathrm{AN}} \\ &= \left[M U_{\mathrm{dc}} \sin(\omega t + \varphi) + \frac{4}{\pi} f_c T_d U_{\mathrm{dc}} \sin(\omega t)\right] + \frac{4}{\pi} f_c T_d U_{\mathrm{dc}} \left[\frac{1}{3}(3\omega t) + \frac{1}{5}(5\omega t) + \frac{1}{7}(7\omega t) + \ldots\right] \end{aligned} \tag{3}$$

where M is the modulation index and φ is the power factor angle. The harmonic voltage amplitude decreases as the harmonic order rises. The higher harmonics can be filtered by a low-pass filter, while the low-order harmonics are difficult to attenuate and result in undesirable voltage distortion.

2.2. Zero-Current-Clamping Phenomenon Caused by Dead Time

Zero-current clamping means that the current is close to zero in any direction during dead time. Due to the freewheeling action of the freewheeling diode, the current magnitude decreases. When the magnitude of the current is near zero, the dead time begins. Then, when the current drops to zero, the reverse voltage on the diode will prevent the reverse increase of the current, which keeps the current near zero during the remaining dead time. When the output voltage is almost zero, the zero-current-clamping phenomenon causes current distortion and torque ripples. Henceforth, dead-time compensation becomes mandatory for voltage source converters.

Figure 4 is a schematic diagram of zero-current clamping of a voltage source inverter. From Figure 4, the following conclusions can be drawn as follows:

(1) The zero-current clamping of the inverter dead time occurs near the current zero crossing, and the current is clamped near zero during the entire dead time.
(2) The current is little affected by the dead time for a period of time before zero crossing, and it is clamped to near zero for a period of time after zero crossing.

Therefore, during the period of zero-current clamping, it is inaccurate to compensate the voltage error by judging the current direction based on the current only.

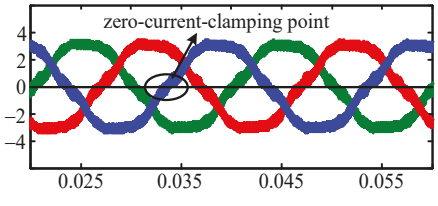

Figure 4. Zero-current clamping diagram.

3. Dead Time Compensation Methods

3.1. Pulse Width Adjustment Method

The pulse-width adjustment method (also named the time compensation method) changes the pulse-width by lagging or leading the turn-on or turn-off time of the power device according to the dead-time insertion, so as to compensate for the effect of dead time [12,13]. It requires the direct adjustment of real-time pulse-width in each switching cycle. Therefore, it is relatively complex to implement. Figure 5 is a schematic diagram of the pulse-width adjustment method, where the

dead-time compensation method based on pulse-width adjusts to ensure that the output voltage waveform is the same as the ideal waveform.

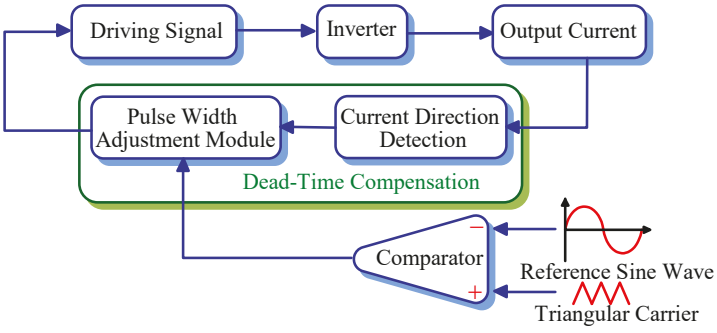

Figure 5. Schematic diagram of pulse-width adjustment method.

In order to solve the problems of phase voltage and phase current distortion and zero-current clamping caused by dead time, a novel adaptive dead-time compensation strategy is proposed in [14]. The strategy does not require current polarity detection. In the synchronous rotating coordinate system, the observed q-axis disturbance voltage is adjusted by a proportional integral (PI) controller to obtain the dead-time compensation time. The dead-time compensation time is allocated according to the ratio of the action time of the two non-zero space voltage vectors.

A tri-carrier Sinusoidal Pulse-Width Modulation (SPWM) used to eliminate dead-time effects is proposed in [15]. It directly modifies the modulation strategy to remove dead-time. It also can reduce current harmonics and suppress the current ripple on the AC side of voltage source converters. Triple carriers are used to modulate the modulating wave. According to the current direction after filtering, the driving signals are obtained by simple logic operations. This method can improve the performance of the induction motor (IM).

A dead-time compensation scheme is presented for a six-switch three-phase output inverter in [16]. The error is compensated by extension or reduction of the switching conduction period. The extended object, which is a turn-on or turn-off period for each switch, is varied by the direction and the magnitude relationship of the output current in each phase.

In order to simplify the time compensation algorithm, a method for measuring the narrow pulse width of a pulse train through a single-channel time analyzer is reported in [17]. This provides no limit to the dead time of the measurement channel. Simultaneously to the periodic jitter measurement of the pulse train, it can estimate both pulse-width measurement error and minimum pulse width, which is determined by specifying a relative measurement error.

Furthermore, the dead-time compensation method presented in [18] reduces the delay time and minimum pulse width. Therefore, it is able to completely compensate for voltage distortion, even if the input signal includes narrow pulses.

In [19], the dead time at the initial stage of the pulse-width modulation (PWM) generation is introduced. The protection algorithm ensures that the two series switches are not conducted at the same time and no switch is turned on during the dead time.

In the voltage source converter, due to the effect of dead time, the fifth and seventh current harmonics are generated in the stationary reference frame, and the corresponding sixth current harmonic is generated in the *d*-*q* synchronous reference frame, respectively. A proportional integral (PI) current regulator in the synchronous frame is used to compensate the distortion results from the dead time [20].

A correction strategy of major contributors that causes voltage distortion has been put forward by analyzing and quantifying the contributors [21]. Unlike the previous reported solutions,

the contributors to voltage distortion are analyzed and quantified. The duty cycle of each phase is adjusted as a function of current feedback or current command to mitigate the voltage distortion due to switch dynamics.

The effect of dead time of a three-level neutral-point clamp (NPC) voltage source converter is discussed in [22]. The self-balancing space vector pulse-width modulation (SVPWM) is presented to improve the effect of dead-time compensation. It provides a cost-effective pulse-based dead-time compensation for three-level voltage source converters.

The effect of dead-time, as well as minimum and maximum pulse-width effects, on the continuous and discontinuous pulse-width modulations, is discussed in [23]. Considering that the controller is not able to compensate for dead time in the case of minimum pulse-width, two compensation methods are developed. One solution, used for the moderate modulation index, is to switch between DPWM (Discontinuous Pulse-Width Modulation) methods to avoid a distorted region and allows a loss-optimized DPWM method. It is used for the maximum part of the operating time. Another method, used for the high modulation index, is proposed to maintain the linearity of the fundamental voltage component. The above two methods are able to reduce the sixth voltage harmonics.

A new integrated dead-time space vector pulse-width modulation technique is proposed to control a voltage source inverter in [24]. The proposed algorithm is modified to ensure the duty ratios are independent of sampling time T and carrier frequency f_c. After the duty ratios are generated by using the modified modulation technique, an integrated dead-time insertion block is used for given T and f_c by taking the three-phase duty ratios as inputs.

The fixed dead-time control strategy may lead to unwanted body-diode conduction or momentary cross-conduction. Considering that the optimum dead time varies with the load current, it is important to continuously adjust the dead time in a cycle-by-cycle manner. An improved solution is proposed to predict the optimal dead time and eliminate the cross-conduction and body-diode conduction [25]. It is able to adjust the optimum timing for both the rising and falling edges of the output switching waveform for the converter.

In [26], the impact of the dead time on common-mode voltage is discussed. A modified pulse-width modulation method is presented to eliminate common-mode voltage due to the dead-time effect. Another dead-time compensation method superimposes the square wave on the triangle wave [27]. The triangle carrier and the square wave have the same frequency. The amplitude of the square wave is equal to that of the dead time. It is simple to implement in practice. Based on a back calculation of the current phase angle, a new on-line dead-time compensation method is proposed in [28]. A detailed switching characterization with dead-time effect in all operation states is discussed in [29]. A dead-time compensation method for a three-level voltage-source inverter is proposed in [30]. It is based on the fact that the voltage error caused by dead time depends on current polarity, and inserts the dead time at the instant of turning on and off of switches. The algorithm is simple and eliminates current harmonics.

It can be concluded from the above that the advantage of the pulse-width adjustment method are that the compensation accuracy is high, the voltage is compensated and has no error, and the compensation method is only related to the polarity of the current. It is simple and intuitive, and has good real-time performance. However, the pulse-width is simultaneously directly adjusted during each switching cycle, which occupies a large amount of computing resources of the controller, and the ambiguity of the zero-crossing point of the current affects the accuracy of the compensation.

3.2. Average Voltage Compensation Method

The average voltage compensation method averages the deviation voltage that is caused by the difference between the output voltage and ideal output voltage waveform [31]. Dead-time compensation is completed by feeding forward the averaged deviation voltage. Compared with the pulse-width adjustment method, it is much simpler. Figure 6 shows a schematic of the average voltage compensation technique and elaborates in detail.

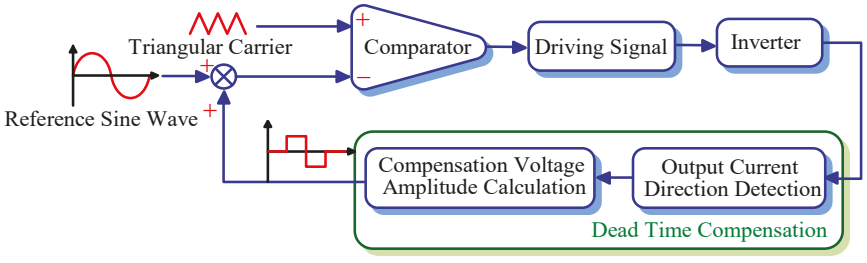

Figure 6. Schematic diagram of average voltage compensation method.

The direction of the output current of the converter is sgn(i_a):

$$\mathrm{sgn}(i_a) = \begin{cases} 1 & (i_a > 0) \\ -1 & (i_a < 0) \end{cases} \tag{4}$$

The dead-time voltage required for each modulation period in bipolar modulation is:

$$U_{tdm} = -\frac{\mathrm{sgn}(i_a) \cdot 2t_d}{T_s} \cdot V_{dc} \tag{5}$$

where T_s is the switching period, V_{dc} is the DC voltage and t_d is the dead-time.

The compensated voltage U_{tdm} superimposed on the modulating wave voltage and compared with the carrier to obtain a PWM driving signal. This kind of method has the same issues as the pulse-width adjustment method, such as compensation error around the zero-crossing region. The major reason for this is that the compensation voltage is determined by the current detection signal. Therefore, the accuracy of current detection directly affects the compensation accuracy.

In order to minimize the harmonic current distortion caused by dead time, a simple dead-time compensation technique is proposed in [32]. With a suitable PI current controller, the proposed technique easily be added into the synchronous reference frame current (cf. *d*-*q* axis) control. With the proposed technique, the output of the PI current controllers can be limited to lower values to reduce an integral windup problem and improve control capability of the system.

A new dead-time elimination method is proposed in [33]. It uses a low voltage detector circuit connected in parallel to each device to measure the terminal voltage of power switches. It can reduce voltage distortion.

An accurate compensation based on the average-value theory is presented in [34]. The compensation factor is adjusted according to the accumulated error within a half period of the output current. The proposed method evaluates initial compensation voltage according to the dead-time and switching cycle, and a proportional factor is introduced to the compensation voltage. The exact compensation factor is obtained by minimizing the harmonic component of the current in the synchronous frame. The compensation voltage introduced by the dead-time, turn-on/off delay and voltage drop across the power switches can be accurately identified by the proposed method. Another method based on the virtual inductor is proposed for dead-time compensation in [35]. It is able to reduce current distortion. Another improved compensation based on the average error voltage is proposed in [36]. Different from conventional methods, which have amplitude and phase errors at the output voltage, it can achieve dead-time compensation with much less amplitude and phase errors. A new distortion voltage compensation method for eliminating the effect of dead-time on zero-current clamping is proposed in [37]. The modeling analysis of the dead-time effects on parallel converters is discussed in [38]. It is useful to evaluate the impact of dead-time on the circulating current of voltage-source converters.

In summary, the average voltage compensation method is simple and convenient, easy to implement, and feasible. However, the zero-crossing detection accuracy is not high enough, and error compensation will occur, causing new harmonics in the output voltage and current.

3.3. Current Feedback Method

The current feedback dead-time compensation method determines the compensation voltage by detecting the polarity of the output current of the converter [39]; a schematic diagram is shown in Figure 7. In practice, it is affected by the dead-time, amplitude and frequency of the current. Actually, the zero crossing of the current is not easy to detect. Moreover, the necessary current filters also exacerbate the difficulty of detection of the current polarity, especially when this method is implemented in software. Severe detection delay will destroy the correct compensation of dead-time.

The current feedback needs to detect the polarity of the phase current and convert the polarity of the current into a square wave voltage, which is added to the modulation wave of each phase. This square wave voltage causes the inverter to generate a current phase that is the same as the error of the compensation voltage. Generally, in the control system, there are three kinds of methods used to detect the polarity of the current:

A. Direct detection of current zero-crossing point

This method determines the modulation plus or minus compensation voltage according to the current sign. Its key characteristic is its simplicity, but it needs to accurately detect the current zero-crossing point, especially when the frequency is relatively low, or else it will lead to incorrect compensation because the current zero-crossing point is not obvious.

B. Prediction of zero-crossing point

This method is an improvement of method (A), realizing the advance detection of the current zero-crossing point, which is usually used for high-frequency bands. It has a good compensation effect.

C. Dead-time compensation based on rotor magnetic field orientation

The method performs coordinate transformation on the three-phase output current, then calculates the current vector angle according to the synchronous rotation angle of the rotor field orientation, and finally compensates for the dead time according to the current vector angle. Usually, the three-phase output current pulse has a better compensation effect.

Figure 7 shows a schematic of current feedback compensation. It is known that, due to the influence of dead-time, the output current contains harmonics. A method named the current harmonic filter method calculates the compensation voltage by filtering the sixth current harmonic in the *d-q* synchronous rotating coordinate system [40,41]. The output current of the grid-tied inverter contains odd-numbered harmonics because of dead-time and nonlinear characteristics of the switching devices. A new compensation algorithm using the second-order generalized integrator (SOGI) is proposed to reduce the dead-time effect [42]. By using synchronous reference frame, even-harmonic components are generated by the dead-time effect. Accordingly, SOGI detects the specific frequency used to reduce the dead-time effect. This algorithm does not require any additional hardware or other information, except phase current and grid angle information. The output current harmonics are effectively eliminated by controlling the error terms of *d-q* axis currents.

A novel method of compensating for dead-time effects, which uses a feed-forward approach for the standard compensation and a feedback loop with adaptive harmonic compensator to suppress the persistent sixth harmonic components in the *d-q* axis current, is presented in [40]. This method does not rely on parameter calculation.

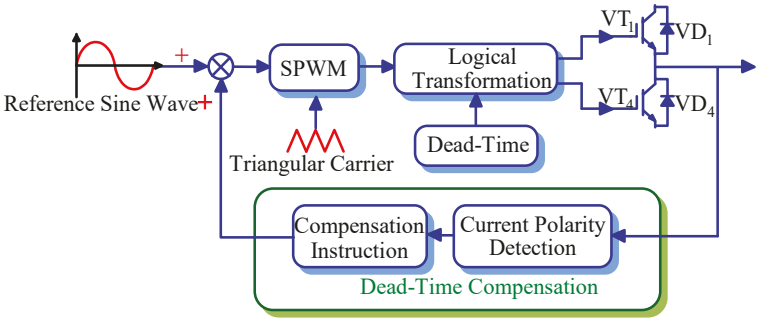

Figure 7. Schematic diagram of current feedback compensation method.

In [41], a novel online dead-time compensation strategy for a vector controlled permanent-magnet synchronous motor (PMSM) is proposed. The output of the adaptive method is a slowly time-varying voltage, which is used to compensate for output voltage distortion. Although the current harmonic filtering method does not depend on current polarity detection and motor parameters, it is affected by the zero-current-clamping phenomenon.

In a voltage source converter, the dead-time effect can be divided into the controlling dead-time effect and switching dead-time effect. The switching dead-time effect includes the turn-on and turn-off time delay of the power devices, the voltage drop of the power devices, and the influence of parasitic capacitance. In order to reduce the switching dead-time effect, a dead-time compensation method to reduce the influence of zero-current-clamping and parasitic capacitance has been raised [43]. The method is used to calculate the three-phase compensation voltage according to the polarity of the three-phase current and the compensation time, and to correct the error polarity of the compensation voltage caused by the zero-current-clamping phenomenon. Since the magnitude of the compensation voltage varies with the current, this method has the disadvantage that the reference quantity is the amount of change when the voltage polarity is corrected.

The polarity of the current is often difficult to determine accurately, mainly because the accuracy of the current detection is affected by the dead-time, amplitude and frequency of the current, thus the output current of the converter is distorted in the zero region and the current zero-crossing point is more difficult to determine.

The dead-time effect is created by using the change of the slope of the current waveform caused by dead time to compensate for the deviation voltage [44], but this method relies on the correct judgment of the polarity of the current. If the polarity is judged incorrectly, it will lead to a worse compensation effect.

In order to reduce the voltage error and current waveform distortion caused by dead time, current feedback control is applied to a three-phase power factor correction rectifier and power device ripple filter with a small capacitance value using a high feedback coefficient [45]. Since the small capacitor on the AC side easily leads to system instability under a high feedback coefficient [46], this method cannot effectively suppress the current ripple due to dead time.

A method compensating for dead-time harmonics by including a harmonic compensator with a current controller is proposed in [47]. A multiple-parallel resonant controller is adopted, which enables selectively canceling out the harmonic components or a repetitive controller mitigates all harmonics below the Nyquist frequency.

For the well-known problem of determining the current polarity in the zero-crossing region of the current, a solution to minimize the voltage distortion in the zero-crossing region is discussed [48]. In the proposed solution, the polarity of the current and its instantaneous value is employed to correct the pulse-width. The experimental results show that the compensating term is maintained at a fixed value no matter the polarity and magnitude of the current flowing through the power switch.

For the problem of a low current with multiple zero-crossing points during a switching period, a new method which uses a model for calculating the voltage error caused by dead time has been put forward [49]. This determines the dwell time and integrates the volt-seconds for a half period of the triangular carrier. Each half period of the triangular carrier split to time segments. The resulting error voltage is used to calculate a new compensated duty factor. Another method that uses the model to calculate the deviation voltage caused by dead time is introduced in [50]. It uses a model to split each half period of the triangular carrier into time segments where the slopes of the currents in all phases and the output voltage of all semiconductor phase legs are constant. It determines the duration of each time segment and integrates the voltage-seconds for a half period of the triangular carrier. The resulting error voltage can be used to calculate a new duty cycle to compensate for dead time.

As is known, the amplitude of the square wave modulated by SPWM is basically constant, and the amplitude can be estimated without additional hardware. The structure is simple, easy to implement, and has a practical application value. On the other hand, the compensation effect is greatly affected by the current detection accuracy, and accuracy of the zero-crossing point of the current detection becomes the decisive factor in determining the compensation effect.

3.4. Voltage Feedback Method

The voltage feedback dead-time compensation method compares the actual output voltage of each phase with the reference output voltage to obtain the deviation voltage, and superimposes the deviation voltage with the reference voltage to obtain a new reference voltage [51]. Because each comparison must be corrected at the next switching cycle and the output voltage must be accurately detected, this method also has hysteresis and is complicated to implement. Figure 8 shows a schematic of voltage feedback compensation.

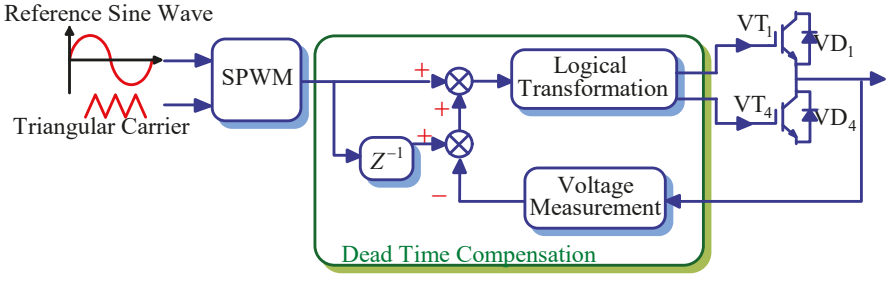

Figure 8. Schematic diagram of the voltage feedback compensation method.

The error voltage vector caused by the dead-time effect of the PWM inverter is given by [52]. Using the vector synthesis method, the formulae for calculating the amplitude and phase of the composite voltage vector are deduced, and the characteristics of the composite voltage vector are analyzed by simulation. In order to ensure that the actual opening time of the switch tube is equal to the ideal given opening time, a dead-time compensation method is proposed. Combined with the characteristics of SVPWM, a simplified formula is obtained. In order to eliminate the error voltage vector, a dead-time voltage compensation method is proposed. According to the difference between SPWM and SVPWM, the equations for dead-time voltage compensation in the stator three-phase stationary frame and the two-phase stationary frame are calculated separately. The experimental results show that the proposed compensation method can improve the output performance of the inverter.

In some control strategies, it is necessary to use the output voltage to calculate some state values, but it is difficult to accurately measure the output voltage of the converter. Therefore, the reference voltage is often used in place of the actual output voltage. However, due to the effect of the dead time of the power devices, the output voltage is distorted, resulting in inconsistency with the reference

voltage. Therefore, the reference voltage is used instead of the output voltage after compensating the output voltage [53].

The classical dead-time compensation scheme is to add an extra voltage command to counteract the voltage error using a similar approach. The compensation signal is generated based on the precise analytical voltage. The voltage deviation can be compensated by adjusting pulse-width accordingly.

According to the current feedback compensation methods, the distortion of the output voltage results in the generation of fifth and seventh harmonics in the current of the stationary coordinate system, and the generation of the sixth harmonic in the current of the synchronous rotating coordinate system. Various harmonic attenuation methods are proposed [54–58]. The output signal of the PI current regulator in the synchronous coordinate system, which is used to compensate for voltage distortion, is selected and processed in [59]. This method reduces voltage distortion by compensating the *d*-axis output voltage and the *q*-axis current regulator.

It is known that the deviation voltage is directly detected, and that the error caused by the dead-time effect can be eliminated and is not affected by the change of the load current. This structure is complicated, and an additional voltage detecting circuit is needed. The small dead-time value requires real-time and accurate detection.

3.5. Adaptive Dead-Time Compensation Method

During processing and analysis, the adaptive control method automatically adjusts the processing method, sequence, parameters, boundary conditions, or constraint conditions to adapt to the statistical distribution characteristics and structural characteristics of the processed data to obtain the best treatment effect.

An adaptive observer-based method, which does not require current polarity detection, is brought forward in [14]. This method uses the PI controller to adjust the *q*-axis disturbance voltage observed in the synchronous rotating coordinate system to obtain the compensation time of dead time. On the basis of conventional SVPWM [60], in each sector, the compensation time is allocated according to the ratio of the dwell time of the two non-zero space voltage vectors. Finally, the dwell times of the two vectors, respectively, are compensated by the allocated compensation time. An adaptive estimation principle diagram of compensation time based on disturbance observer is shown in Figure 9, where PI is the proportional integral controller, u_{qdis} is the *q*-axis disturbance from the disturbance observer. The compensation time is obtained by the disturbance and the PI regulator.

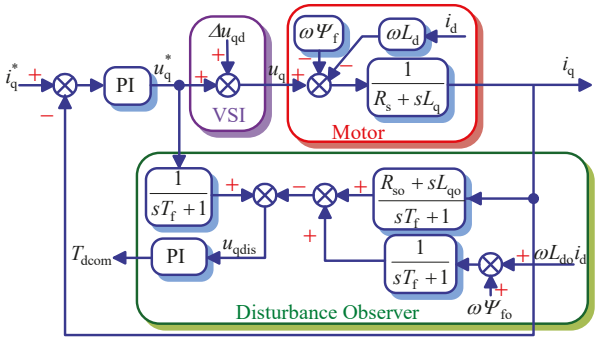

Figure 9. Adaptive estimation of dead-time compensation time based on disturbance observer.

The conventional sliding mode observer (SMO) collects the rotor position angle by identifying rotor position angle, and needs to introduce a phase-locked loop (PLL) to realize the reverse control. It has certain limitations, including massive calculation, slow dynamic response and complex methods, and not taking the effect from the inverter dead time on the estimation model into consideration during

the identifying process. To solve the problems, a new sensorless control method for the adaptive SMO based on a rotating coordinate system and considering dead-time has been proposed [61]. Based on the conventional hypothetical rotational co-ordination system approach, and combined with the model motor approach, this method takes the rotation speed of the hypothetical coordination system as a controlled variable and improves the response speed. Meanwhile, the voltage change triggered by the inverter's dead time is taken into consideration and the motor current control is achieved through the SMO, which reduces the error between the model and actual motor current to be zero. This method can be realized easily and achieves the motor's positive-negative rotation control.

A dead-time optimization technique for a two-level voltage source converter using turn-off transition monitoring is proposed in [62]. By tracking the change of the load on-line, the method can adaptively calculate the optimum width of the inductor current zero-crossing region to eliminate the dead-time effect of the zero-crossing region and the non-zero-crossing region, respectively. This technique can effectively eliminate dead time regardless of the load during the entire modulation period. This method not only reduces the output voltage's fundamental distortion and low harmonic content, but also introduces the adaptive algorithm, greatly reducing the accuracy requirements of the current sampling device and effectively improving the practicality of the dead-time elimination method and the reliability of system.

In [63], an adaptive dead-time compensation strategy to obtain fundamental phase voltage for inverter-fed vector-controlled PMSM drives proposed. A phase dead-time compensation voltage (DTCV), which is used to compensate for the disturbance voltage, is transformed into q-axis DTCV in the rotor reference frame. The relationship between dead-time compensation time (DTCT) and the q-axis DTCV, when the d-axis current is zero, is investigated. In this study, the q-axis DTCV is considered to be the same as the q-axis interference voltage. Adaptive DTCT is used to determine the amplitude of the phase DTCV. Since only the amplitude of the phase DTCV is adjusted, this method has less influence on the estimation delay of the disturbance observer.

There is a dead-time problem in the PWM control of the motor, and it seriously affects the performance of the motor. In order to eliminate the influence of noise, an adaptive filtering method has been presented [64]. The response speed of the filter is improved by the dynamic convergence coefficient. Experimental results show that this filtering method is highly suitable for dead-time compensation, which is based on the current vector. Compared with other noise removal methods, the algorithm is concise and easy to program.

Based on the influence of dead time on the PMSM inverter, a dead-time compensation method based on the Kalman filter has been brought forward [65]. This method is used to filter system noise and the generation of fifth and seventh harmonics in the α and β static coordinate frame, so as to obtain the direction of the three-phase current and the error voltage vector reduced by dead time. According to the error voltage vector, the dead-time effect can be suppressed. The experimental results show that the proposed method can effectively improve the output current waveform of the inverter and the performance of the PMSM system.

In [40], an adaptive dead-time compensation method based on sixth harmonic elimination is proposed. In order to improve the performance of the control algorithm, the method uses an adaptive harmonic filter to suppress the sixth harmonic. PI controllers are used in the proposed method. These controllers have appropriate parameters and effectively suppress the sixth harmonic current in the d-q axis.

Aiming at the online dead-time compensation for PMSM, which is controlled by a vector, a new online dead-time compensation strategy has been discussed [41]. The proposed method is composed of two parts. The first independent part of the parameter is an adaptive method based on the monitoring of harmonic distortion in the d-axis current. Therefore, the criterion is defined as the sum of squared direct axis current between the two zero-crossing points of the phase current. The criterion is minimize by the PI controller, and the output of the PI controller is a slowly time-varying voltage, used to

calculate the compensation voltage. This method is extended by the constant voltage disturbance observer of the PMSM model.

Some industrial processes are affected by not only different gain and time constants, but also dead-time. For such industrial processes, the present classic self-regulating regulator is not applicable because it needs the time delay of the process.

In order to control the switching time and simultaneously eliminate the power losses caused by body-diode conduction, power-stage shoot-through current and inductor reverse current, an adaptive inverter-based dead-time controller for synchronous DC-DC converter is proposed in [66]. To achieve even faster comparison, an inverter is used to replace the high-speed comparators in the proposed dead-time controller. In addition, a two-step (coarse- and fine-tuning) dynamic delay generator is proposed for accurate switching time and a wider dead-time correction range comparing to the conventional design. Thanks to the novel adaptive dead-time controller, it is able to dynamically adjust the dead-time to its optimal value with a very wide load range.

An adaptive-linear-neuron (ADALINE)-based dead-time compensation method used for vector-controlled PMSM drives is put forward in [67]. Four ADALINEs are employed in the proposed method. Two ADALINEs are used for estimating the sixth-order harmonic components of *d-q* axes currents, and the other two used for generating the compensation voltages of *d-q* axes. Without any additional hardware and complicated signal processing algorithms required, the method is easy to implement.

Because of fault tolerance, adaptive dead-time compensation has the ability to adapt to changes in dynamic behavior of controlled objects, parameters and operating conditions. On the other hand, the disadvantage of this method is that simple fuzzy processing of information will lead to reduced control accuracy and dynamic quality of the system, and the design is not systematic and cannot define control objectives.

3.6. Predictive Current Control

The predictive current control method uses predictive control to control the voltage source converter; that is, to use the known state of the present sampling point, the circuit model, and the reference current of the next sampling point to predict the voltage that can make the output current reach the desired current [68]. This method is implemented only with software. Figure 10 shows the schematic of predictive current control.

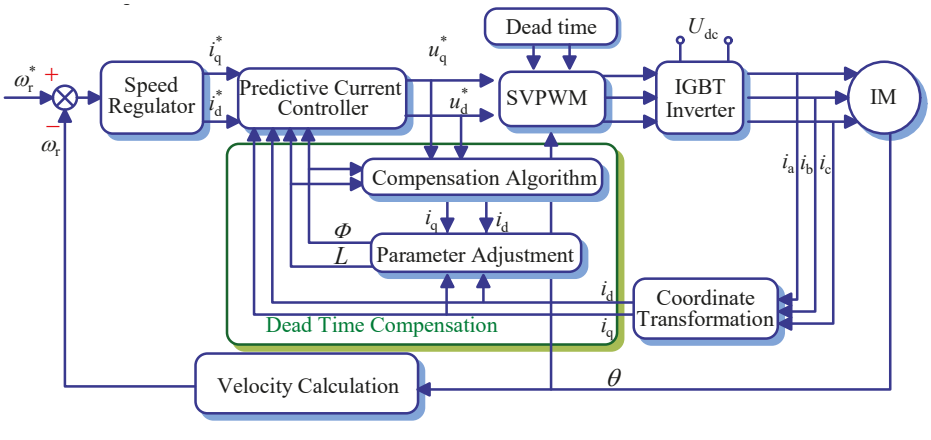

Figure 10. Adaptive estimation of dead-time compensation time based on disturbance observer.

In order to improve the adaptability of the system, a novel closed-loop adaptive method is proposed in [69]. The method uses the duty ratio instead of the average deviation voltage, and feeds

forward the duty cycle of the compensation time. Simultaneously, the method uses the predictive current controller (PCC) to regulate the phase current. The method is simple to implement, has high computational efficiency, and is easily added to the existing PCC. This method can enhance the dead-time suppression capability of the PCC without modifying the internal structure.

With dead-time compensation, a control method of a doubly-fed induction generator with a three-level midpoint-clamped inverter with dead-time compensation is described in [70]. The principle of the proposed control scheme is to use a dynamic model to predict the voltage value, the rotor current and the DC bus capacitor voltage vector of the next sample point. However, dead time also can cause errors in the established model. Therefore, taking dead time in the model into account, active and reactive power can be estimated based on the stator flux and rotor currents to compensate for dead-time effects. The cost function in this prediction algorithm considers active power, reactive power, and the error between the reference capacitor voltage and the actual. The algorithm selects the optimal switching state of the minimum value function to achieve the purpose of reducing the switching frequency and the common mode voltage.

A predictor structure derived from the filtered Smith predictor is discussed clearly in [71]. The structure is used to simplify the tuning in the robustness of model predictive controllers (MPCs) and improve robustness. The stability and robustness of linear MPCs are analyzed, and this method is extended to nonlinear MPCs of a class of nonlinear systems. The key idea of this method is to separate the predictive structure from the optimization phase in order to guarantee input-to-state stability and constraint satisfaction by using an equivalent dead-time free system.

Although the MPC technique can easily deal with the dead-time effect due to its internal prediction structure, in order to improve robustness an appropriate predictor for the MPC algorithm needs to be defined. A filter-based Smith prediction structure is put forward in [64]. This prediction structure simplifies the traditional prediction algorithm and improves robustness. The key to this method is to separate the predictor structure from the optimization phase so that stability can be guaranteed using an equivalent system without dead time so that the constraints are satisfied.

A predictive method which allows the compensation of dead-time in a Voltage Source Inverter (VSI) feeding an Induction Motor (IM) with the control of SVPWM is discussed in [72]. Based on the step-by-step analytical prediction of the stator phase currents, the method modifies the reference space vector of the feeding voltage. In this way, the effects of dead time can be taken into account and compensated for. It is known that the predictive current control can be used to eliminate the adverse effects of control delays. This method is essentially a control algorithm based on an accurate mathematical model, and its control effect depends on the accuracy of the parameters of the grid-connected converter and, especially, the accuracy of the filter inductor.

3.7. Dead-Time Compensation Method Based on Disturbance Observer

The basic idea of the disturbance observer is to construct a disturbance signal observer based on the error between the actual model and the reference model. The dead-time compensation method based on the disturbance observer uses a disturbance voltage observer based on making the output current as the input of the observer, and to estimate the disturbance voltage caused by dead time. The estimated disturbance voltage is used to compensate for dead time [73].

This method is implemented only with software; Figure 11 shows a schematic of the dead-time compensation method based on the disturbance observer [74]. In Figure 11, the reference input voltage u_{sr}* consists of the input reference and the disturbance voltage.

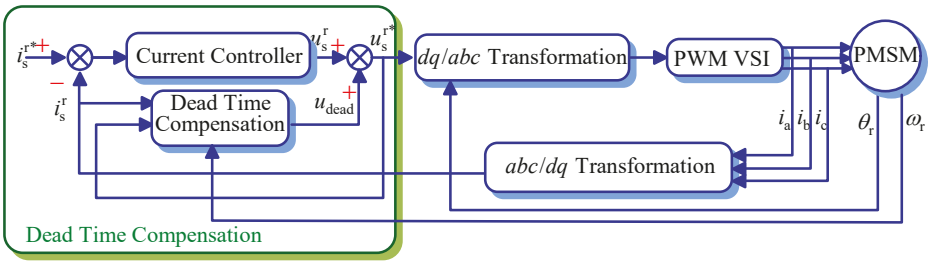

Figure 11. Schematic diagram of disturbance observer method.

A novel procedure for PI feedback and lead-lag filter design is introduced in [75]. The proposed controller uses a robust tuning rule that is complemented be filters and is used for improving reference current and measurable disturbance responses. When perfect measurable disturbance compensation is not possible due to dead time, the proposed control provides a smaller integral error.

In order to improve the static and dynamic output performance of Uninterrupted Power Supply (UPS) inverters without adding sensors, a digital control strategy is proposed in [76]. This strategy uses the area equivalence principle to equate the dead-time voltage with a square-wave disturbance voltage, and regards the output current as the disturbance current of the control system, and the feed-forward control is used to compensate voltage and current. Because this method uses the differential operation of the output voltage to obtain the output filter capacitor current value, even if the current sensor is not used, the quasi-double loop control of the UPS inverter is still achieved.

In [77], an auto-tuning control system based on the modified Smith-predictor is proposed for use as an effective dead-time compensator. In order to improve the anti-interference ability, the system adds a feedback loop, used in a cascade structure. At the same time, this study provides several optimization rules of the main controller.

In the presence of interval parameter uncertainty, a novel method used to tune a PI compensator with dead time has been proposed [78]. Based on the optimization of load disturbance rejection, the method constrains the magnitude of the sensitivity and complementary sensitivity functions.

A simple and direct compensation technique to solve voltage distortion in a three-phase VSI has been introduced [79]. The proposed method calculates the practical voltage drop of the power devices in a sampling period according to the current polarity. The average voltage deviation is calculated by the difference between the actual voltage and reference voltage. The SVPWM switching intervals of each phase are derived by the average output voltages, and calculated according to the current polarity and nonlinear voltage distortion to compensate for the output voltage errors. The proposed compensation method is extremely easy to implement without any additional cost and software burden.

A new dead-time compensation method using the signal of the integrator output of the synchronous *d*-axis current regulator has been proposed [80]. The method can reduce voltage distortion by compensating for the output voltages of the *d*-*q* axis current regulator. This method does not require an additional hardware circuit, and can be adapted not only for the steady state but also for transient states.

This method relies on a simple principle and simple control structure, and needs few measurement parameters. Though it is easy to implement, the tracking step size of the method cannot balance response speed and accuracy. If the search step is too small, the search speed becomes slower; if the search step is too long, it is easy to cause oscillation and affect system stability.

3.8. Invalid Switch Elimination Method

The invalid switch elimination method, which is only valid for switches needing anti-parallel diodes such as IGBTs, has been the main method researched by scholars in recent years. The principle

is that by analyzing the effective device of the converter, the invalid power device in the same bridge arm can be turned off, and the anti-parallel diode is freewheeling, so that there is no need for adding dead time. Therefore, the phenomenon of straight through of the upper and lower tubes of the same bridge arm can be avoided [81]. Because wrong current polarity detection can cause severe voltage distortion, even if the invalid switch elimination method does not consider turn on-off time and the voltage drop of power devices, it requires high-accuracy current polarity detection. The single-phase VSI circuit is an example for analyzing the mechanism of dead-time elimination.

The following is an analysis of the principle of an invalid switch elimination method outside the threshold range. Instantaneously, the output current $i_a > 0$, the driving signals of VT_1, VT_4 are turned on, and the inverter is in the power device conducting-state, as shown in Figure 12a. VT_1 and VT_4 are turned on, and VT_2 and VT_3 are turned off; when the driving signal of VT_1 is turned off, the inverter is in the diode freewheeling state, as shown in Figure 12b. At this time, VT_1 is turned off and VD_2 is freewheeling. From the above analysis, no matter whether VT_2 has a driving signal, i_a does not flow through VT_2, so VT_2 can be called the invalid switch. Therefore, the driving signal of VT_2 can be closed when $i_a > 0$. Similarly, when the output current $i_a < 0$, the driving signal of VT_1 can be closed. This method not only ensures that the upper and lower power devices on the same bridge arm will not pass through, it does not affect the inverter output current i_a waveform.

Because the polarity of the current changes frequently around the zero-crossing point, the invalid switch elimination method needs to add a threshold near the zero-crossing point [82]. Outside the threshold range, the invalid power device driving signals are turned off; within the threshold range, the inactive power device is reused, and the dead time is added to the driving signals of the upper and lower power devices in the same bridge arm. The key to this kind of method is how to select the threshold range. If the value is not accurate enough, the phenomenon of inaccurate compensation will occur near the threshold value, thus introducing harmonics.

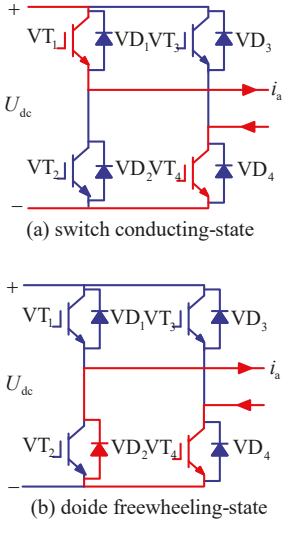

Figure 12. Current flow direction when the phase current $i_a > 0$.

Based upon the fact that the self-commutation switch device of an inverter phase would not turn on even though the gate-driving signal is supplied, the dead-time minimization algorithm is proposed in [83]. Using this method, the number of inverter switches is almost reduced to half that of the conventional method.

The invalid switch elimination method is adopted in dead-time compensation, used in the vector controlled PMSM system [84]. Above the threshold, the control strategy is based on the invalid switch elimination method; below the threshold, the dead-time compensation strategy is adopted to eliminate the voltage error caused by the current fluctuations and zero-current-clamping phenomena. This new strategy improves system stability and achieves desired control performance.

A novel IGBT gate-drive method is easily implemented in the IGBT gate driver of a PWM voltage source converter [85]. Using this method, the upper and lower IGBT gate drivers on the same bridge arm can receive the ideal complementary PWM signal without dead time. If the freewheeling diode conducts current, the gate driver turns off the IGBT, which parallels with this diode. This novel method can effectively operate with low current, low output frequency.

A dead-time elimination scheme for a converter that is controlled by PWM is proposed in [86]. The presented scheme proposes a current polarity detection circuit, which requires one power source only for a converter and a PWM control method without dead time. The proposed method dramatically improves output voltage loss and current distortion.

A novel strategy of dead-time elimination method for an H-bridge VSI and a new current polarity detection circuit used to remove dead time between signals are presented in [87]. The proposed detection circuit is based on the conduction states of two low anti-parallel diodes, and requires one power supply. Moreover, this proposed circuit can accurately detect low current polarity even at low output frequencies unlike current sensors.

A SVPWM control method based on a hybrid voltage vector has been put forward to avoid the effect of dead time [88]. This paper presents a novel method to compensate for dead-time effects by combining the 180° conduction type and 120° conduction type. In this method, an arbitrary space voltage vector is synthesized with the 12 basic voltage vectors. As a result, the novel control algorithm without dead time reduces the waveform distortion and harmonic content of the output voltage and improves the utilization of the DC bus voltage.

The invalid switch elimination method mainly relies on the accurate detection of the conduction state of each power device, so a hardware detection circuit is introduced in [89]. Due to the increase of hardware circuits, these methods have the disadvantages of increased experimental costs, poor reliability, and noise generation.

Based on the dead-time elimination method, a new switching strategy for PWM power converters has been proposed [90]. This strategy uses the polarity information of the reference current instead of the real current.

In [91], in order to deal with the dead-time control around the zero-current-crossing points, an immune algorithm based on the dead-time elimination PWM control strategy is proposed. This algorithm restricts the control sequence to a specified level around the zero-crossing region. Compared with traditional methods, the method can resolve the problem of detection around zero-the crossing point without a hardware detection circuit.

The dead-time effect in a synchronous *d*-*q* reference frame is studied in [92], and an average model of the inverter capable of capturing the low-frequency harmonic content in the load current along with the fundamental component is also developed. The average models are shown to consume less computation time.

In addition to the invalid switch method, other scholars proposed methods of not setting the dead time from the perspective of the control method [93]. A new dead-time elimination method for a nine-switch converter is proposed in [94]. The proposed method assumes that the unique switching elements of the nine-switch converter to operate at several subintervals are divided during a fundamental period. Due to the unidirectional conducting characteristics of the switching unit, the nine-switch converter can operate without dead time. In addition, for a special subperiod in which no switching unit can be used, a novel driving signal conversion method is proposed to eliminate dead time. A non-dead-time SPWM control strategy for a grid-connected inverter based on a modulation function is put forward in [95]. The phase separation control is used to achieve the decoupling of the

three-phase grid-connected current and modulation function. Then the decoupled grid-connected current modulation function is used to perform the dead-time SPWM control. This control strategy is simple and effective, further guarantees the reliability of the dead-time modulation strategy, and removes the dependence of the traditional method on the hardware detection circuit.

The invalid switch elimination method enables the driving pulses of the upper and lower switching devices to alternate according to the current polarity. However, there is a certain degree of ambiguity in current zero-crossing and it is difficult to measure. Because the double second-order generalized integrator frequency-locked loop (DSOGI-FLL) has the noise-attenuation and frequency-adaptability characteristics, it is used to detect the current polarity. The DSOGI-FLL-based invalid switch elimination method is proposed in [96], and an improvement in the form of a delay compensation term is inserted in the DSOGI-FLL to compensate for both the current measurement delay and the control delay to minimize the current zero-crossing distortion. A dead-time elimination method of PWM controlled inverter is introduced in [97]. This method accurately determines the direction of the load current by detecting the operating conditions of the power devices and their antiparallel diodes. A low-cost circuit used to detect the operation of anti-parallel diodes is introduced in this study. Compared with complex compensators, this method has the characteristics of simple logic and flexible implementation.

It is known that the control is simple and convenient, easy to implement, and feasible. But this method cannot completely eliminate the influence of dead time, and it is necessary to set a certain dead time in a special interval.

3.9. The Volt-Second Equilibrium Theory Method

The volt-second equilibrium theory method divides the factors that cause output voltage distortion into the effects of dead time, switching time, and the voltage drop of the power device [98]. This method builds the converter circuit model off-line to achieve online compensation, and quantifies the effect of each factor on voltage distortion, since current polarity, detection and voltage error at the zero-crossing point of the current are the two key points of this method. Most of the dead-time compensation methods based on the volt-second equilibrium theory directly use the current sensor to detect the current polarity, but at the zero-crossing point, the current polarity detection is affected by the zero drift and noise.

Accurate current polarity judgment is achieved by detecting the situation of the two freewheeling diodes conducting in the same phase bridge [82]. However, the complicated hardware is required for this solution.

A feed forward voltage-second balancing strategy used in online conditions for monitoring data of SiC devices is employed in high frequency VSI applications [99]. The turn-off delay and rise/fall time of drain-source voltage signals are sent to the micro-controller, which is used in an algorithm to actively adjust the duty cycle of the driving signals to match the voltage-second of the non-ideal output voltage with an ideal output voltage-second. The monitoring system also allows the method to eliminate the need for accurate current detection.

A technique to compensate the effect of dead time in sinusoidal a PWM VSI is proposed in [100]. In order to avoid unfeasible pulse-widths of the driving signals, the compensation is implemented by adjusting the switching frequency. The variation of the switching frequency is defined by a simple scalar equation that can easily be included in the software of any drive system.

A feedback–feedforward phase voltage compensation method, based on derived expression of error voltage is proposed in [101]. Using a simple hardware circuit is used to obtain the actual output of the VSI as feedback with which precise compensation amplitude can be calculated. This method can also detect the current polarity by reconstructing the phase current from filtered current components with a Kalman filter. Using this method to compensate for dead time can improve the system stability.

For the duty cycle error of the drive signal, most studies use off-line compensation methods; however, these take a lot of time. In order to achieve online measurement of the error of the voltage

duty cycle, a simple hardware circuit is designed in [102]. However, due to the parasitic capacitor of the power device, the slope of the terminal voltage will change at the zero-crossing point of the current. At the same time, this kind of hardware circuit will produce more duty cycle errors.

Based on the power device circuit, some models are formulated in [103]. These models mainly consider the parasitic capacitance, but rely on current detection, so the accuracy of the voltage error calculation at the zero-crossing point of current is still relatively low. Although the methods based on the principle of volt-second equilibrium seem to be accurate, this method needs to solve the problem of weak current measurement in a noisy environment.

A new method of deadtime effect compensation based on additional current measurements realized by analog-to-digital converters is proposed in [104]. Because the measurements are carried out at the time instants specified by a PWM strategy, they can easily estimate the voltage error caused by dead time. The voltage error is compensated for during the next switching period by modification of a reference voltage. Experimental results prove that the change of the time instant of additional measurements will give better results in the case of other low-pass filter parameters.

3.10. Repetitive Control

Dead time can be seen as a periodic disturbance signal that can be compensated by a repetitive controller [105]. Repetitive control is based on the internal model principle [106]. The internal model principle means that if the signal generator contains a reference command in a stable closed-loop system, the controlled output can follow the reference command without a steady-state error. If the system requires a zero steady-state error for the sinusoidal input, the model of the sine function should be included in the stable closed-loop transfer function. Due to the limited system bandwidth, it is impossible to eliminate all harmonics. The repetitive controller is mainly used to reduce the low-order harmonic distortion caused by dead time.

Figure 13 is a discrete block diagram of a repetitive controller used to compensate dead-time, where $r(k)$ is the reference sinusoidal signal, $y(k)$ is the output voltage of the inverter, $d(k)$ is the disturbance signal caused by the dead-time, $e(k)$ is the error voltage, and $r_c(k)$ is the reference instruction after being compensated. The transfer function $P(z^{-1})$ represents the SPWM inverter model, $Q(z^{-1})$ is a band limited filter, and $S(z^{-1})$ is a compensator of the repetitive control loop. The repetitive controller calculates the compensation voltage according to the output voltage error, and the compensation voltage is added to the initial sinusoidal reference value for dead-time compensation.

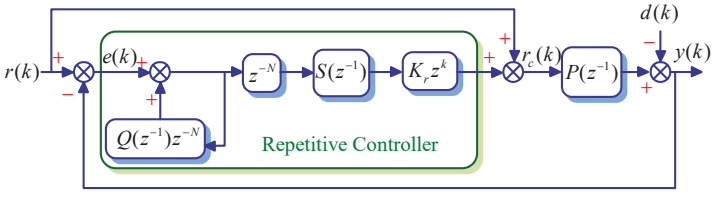

Figure 13. Schematic diagram of repetitive control.

Repetitive control can effectively suppress the harmonic current of the grid due to the infinite gain at each harmonic of the full frequency band. However, because repetitive control is equivalent to an infinite number of resonant terms connected in parallel, it also has problems, such as a narrow resonant frequency band and poor resistance to frequency fluctuation. Therefore, there is a control delay, which will affect the dynamic response of the system.

4. Discussion and Conclusion

The advantages and disadvantages of dead-time compensation methods and the inadequacies of various compensation methods are summarized in this article.

For the pulse-width adjustment method, due to the ambiguity of the zero-crossing point, the pulse width needs to be adjusted in each switching cycle in order to improve the accuracy of the current polarity determination. The existing method is either computationally complicated or increases the complexity of the system, so is still difficult to apply industrially.

Compared with the pulse-width adjustment method, the average voltage compensation technique is simple and convenient to control, and easy to implement. However, if the zero-crossing point detection accuracy is insufficient, the error compensation phenomenon will still occur. To solve this intractable problem, the voltage error is estimated online as a disturbance. The estimated value is fed back to the closed-loop control to avoid direction detection of the zero-crossing point or to reduce the accuracy requirement for direction detection.

In order to avoid the inaccuracy of current detection, the voltage feedback compensation technique directly detects the deviation voltage to eliminate the error caused by the dead-time effect. This method needs to add a complicated voltage detection circuit, and the detection circuit in actual industry will reduce the reliability and stability of system, so this method has almost no application.

The compensation effect of the current feedback compensation method is greatly affected by the accuracy of voltage or current detection. The accuracy of the current zero-crossing-point detection becomes the decisive factor determining the compensation effect. However, compared with the voltage feedback compensation technique, since the current needs to be detected in the control system, this method can estimate the feedback current without additional hardware, and the current detection is easier than the voltage detection. This method is simple in structure and easy to implement, and is widely used in practical industries, but requires increased detection accuracy.

The volt-second balance principle also relies on correct detection of the polarity of the current, and current polarity detection is greatly affected by zero drift and noise, which can easily cause false compensation. At the same time, this method requires a significant amount of software calculation, occupies lot of space resources, and is not easy to implement.

Due to the presence of high-frequency noise in the current detection channel, in the vicinity of the current zero-crossing point, error compensation will occur following error detection, which will aggravate the influence of the dead time. Therefore, all the above traditional compensation schemes have a common problem, namely, solving the current zero-crossing detection problem. In order to improve the traditional current detection methods, methods such as the invalid switch elimination method, the predictive current control method, and the adaptive method are proposed. However, these methods all require complicated software calculations, so are difficult to implement.

As with the voltage feedback compensation method, in order to avoid the direction detection of the current zero-crossing-point or to reduce the accuracy requirement for the direction detection, the invalid switch elimination method can eliminate dead time in most cases based on the optimization of the on/off state of a switching device, but cannot completely eliminate the dead-time effect. The method needs to set a certain dead time in a special interval by setting a threshold. For improvement of the invalid switch elimination method, one method is to set the threshold value, with the linear compensation within the threshold and the fixed value compensation beyond the threshold. Another method is to calculate the zero-crossing area width to improve zero-crossing detection.

Dead-time compensation methods based on disturbance observation means the disturbance voltage vector is no longer related to the polarity of the three-phase current, avoids detecting the polarity of the phase current, and can realize online real-time compensation for the dead-time effect. The method is simple to implement, better suppresses the zero-current-clamping phenomenon, and is widely used in industry, but requires a large amount of software calculation.

Similar to the disturbance observer, predictive current control does not need to detect the current direction, greatly simplifies the calculation process, and saves system resources. It is a low-cost and high-efficiency dead-time compensation method. Compared with traditional methods, it effectively improves the dynamic performance and steady state accuracy of the system. However, errors of system parameters can have a detrimental effect on dead-time compensation.

Similarly, the adaptive dead-time compensation method does not need to detect the current direction, which can effectively suppress the zero-current-clamping phenomenon. This improves the low-speed running performance of the system, which is simple and easy to implement. At the same time, this method can observe and compensate the dead-time effect in real time online, and avoid the undesired phenomenon of dead time caused by offline measurement. However, the fuzzy processing of information will lead to the reduction of control precision and dynamic quality of the system.

The repetitive control theory was developed for the characteristics of the dead zone effect and the periodicity of the output voltage distortion caused by phase-controlled rectification. It is applied to the control of the output voltage waveform of the inverter. Since this control operation is simple and has good reliability, the repetitive control technique has been widely used. However, repetitive control only suppresses periodic disturbances, and does not work for non-periodic disturbances.

Looking at the various dead-time effect compensation methods mentioned in the paper, we can clearly identify the research hotspots and trends of the dead-time compensation methods:

(1) The traditional dead-time compensation schemes need to solve the zero-crossing-point current direction detection problem to avoid the zero-current-clamping phenomenon and the detection error of current direction. This problem can be solved in one of two ways: one is to develop a new method to avoid current detection, while the other is to improve the detection accuracy of current zero-crossing from the perspective of software and hardware.
(2) Combining the intelligent control theory with the dead-time compensation algorithm optimizes the existing dead-time compensation methods and improves the compensation effect. The existing relevant literature attempts to combine intelligent control theory with dead-time compensation, but only in the laboratory stage, and is far from reaching the point of industrial application.
(3) Develop higher-precision voltage and current detection instruments to improve detection accuracy. Hence, the existing compensation methods can be further applied.

Finally, the dead-time compensation is a key part for power converter, which directly affects the output performance, stability and reliability of the control system. Although in-depth research on dead-time compensation has been conducted and many solutions have been proposed, there are still certain problems or limitations for these algorithms in practical applications, especially for high and very high switching frequency operation of power converters with SiC and GaN devices [107]. The principles of various compensation methods have been comprehensively introduced and discussed in this article. This paper provides a useful reference regarding the selection and further research of dead-time compensation methods for power converters.

Author Contributions: This paper was a collaborative effort among all authors. investigation, Y.J., Y.Y., X.G.; review and editing J.Z., H.D., S.P.

Funding: This work is supported by the National Natural Science Foundation of China (51777181), Lite-On Research Funding, State Key Laboratory of Reliability and Intelligence of Electrical Equipment (No. EERIKF2018002), Hebei University of Technology, and Postdoctoral Research Program of Hebei Province (B2018003010).

Conflicts of Interest: The authors declare no conflict of interest.

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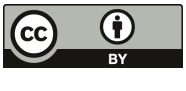

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EMI Filter Design for a Single-stage Bidirectional and Isolated AC–DC Matrix Converter

Diogo Varajão [1,2,*], Rui Esteves Araújo [1,2], Luís M. Miranda [2] and João A. Peças Lopes [1,2]

[1] Faculty of Engineering, University of Porto, Rua Doutor Roberto Frias, 4200-465 Porto, Portugal; raraujo@fe.up.pt (R.E.A.); jpl@fe.up.pt (J.A.P.L.)

[2] INESC TEC—Institute for Systems and Computer Engineering, Technology and Science; Rua Doutor Roberto Frias, 4200-465 Porto, Portugal; luis.m.miranda@inesctec.pt

* Correspondence: diogo.varajao@fe.up.pt; Tel.: +351-225-081-808

Received: 17 September 2018; Accepted: 9 November 2018; Published: 12 November 2018

Abstract: This paper describes the design of an electromagnetic interference (EMI) filter for the high-frequency link matrix converter (HFLMC). The proposed method aims to systematize the design process for pre-compliance with CISPR 11 Class B standard in the frequency range 150 kHz to 30 MHz. This approach can be extended to other current source converters which allows time-savings during the project of the filter. Conducted emissions are estimated through extended simulation and take into account the effect of the measurement apparatus. Differential-mode (DM) and common-mode (CM) filtering stages are projected separately and then integrated in a synergistic way in a single PCB to reduce volume and weight. A prototype of the filter was constructed and tested in the laboratory. Experimental results with the characterization of the insertion losses following the CISPR 17 standard are provided. The attenuation capability of the filter was demonstrated in the final part of the paper.

Keywords: EMI filter; electromagnetic compatibility; AC–DC power converters; electromagnetic interference filter; matrix converters; current source; power density; battery energy storage systems; battery chargers

1. Introduction

Power electronics is making profound changes within the transportation sector [1,2] and the electric power system [3,4]. Bidirectional AC–DC converters are required for several applications, such as battery energy storage systems (BESS) [2,5], chargers for electric vehicles (EVs) [6–8], uninterruptible power supplies (UPS) [9], solid-state transformers (SST) [10], and DC microgrids [11]. The development of new wide bandgap power semiconductors combined with enhanced modulations and control techniques are contributing for the miniaturization and efficiency improvement of the power electronics converters [12]. This is followed by an increase of the switching frequency of the power semiconductors. As a result, conducted emissions (CE) with higher intensity are generated in the measurement range of the electromagnetic compatibility (EMC) standards. In this way, an additional effort is necessary in the design of the electromagnetic interference (EMI) filter included in the input of the power converters in order to comply with the standards [13]. A careful dimensioning of the EMI filter is also essential to ensure the adequate power factor in all operating range and to achieve a high power quality without penalizing the efficiency, volume and cost of the system.

Matrix converters (MC) are one of the most interesting families of converters due to its unique and attractive characteristics [14]. By employing an array of controlled four-quadrant power switches, the MC enables AC–AC conversion without any intermediate energy storage element [15]. The high-frequency link matrix converter (HFLMC) is a single-stage bidirectional and isolated AC–DC energy conversion system [16]. The new modulation proposed in [17] and patented in [18] allows independent control of active and reactive power (PQ control) as well as the DC current in the

battery pack. By exploring the MC attributes, circuit volume and weight can be reduced, and a longer service life is expected when compared with equivalent DC-link based solutions [16,19,20]. However, due to its complex power structure, it presents EMC challenges that have to be studied in order to ensure compliance with the international standards by designing the necessary EMI filter.

Several approaches for the design of differential-mode (DM) and common-mode (CM) filtering stages for direct and indirect matrix converters (MC) were proposed in [20–33]. However, in spite of the long history of this question, until now there has been no complete systematization regarding which topologies and damping methods should be used for each DM and CM filtering stage. Among these works, there are also some procedures of design and formulas that simply do not match between different papers, which may mislead or confuse the reader. Additionally, these works do not show the complete design process from the requirements specification until the experimental characterization of the insertion losses. According to our best knowledge, this is the first work in literature that propose a complete design of EMI filter for the HFLMC. The main contribution of this paper is setting up a systematic methodology for the design process of the HFLMC's EMI filter for CISPR 11 Class B pre-compliance. This design process also takes into account the modeling of the measurement equipment, such as the Line Impedance Stabilizing Network (LISN) and the Test Receiver (TR), in order to better predict the effectiveness of the designed EMI filter. Furthermore, a practical way to characterize the insertion losses according the CISPR 17 standard is fully described and supported by experimental results. It is worth noting that this is the same procedure followed by the manufacturers to characterize their EMI filters. In addition, this is the typical information available in the EMI filter datasheet and is very useful to compare the effectiveness of different filters.

The manuscript is organized as follows: the HFLMC is briefly presented in Section 2. Then, the applicable standards and the measurement approach of CE are described in Section 3. The detailed design of DM and CM filtering stages is explained in Sections 4 and 5, respectively. Section 6 presents the proposed integration strategy of the different filtering stages. The experimental results are shown in Section 7. Finally, Section 8 draws conclusions and proposes future work.

2. High-Frequency Link Matrix Converter

Figure 1 shows the HFLMC proposed for single-stage bidirectional and isolated AC–DC energy conversion. Each bidirectional switch S_{xy} is composed of two transistors: S_{xy1} and S_{xy2} ($x = a, b, c$ and $y = P, N$) in a common-source configuration. Command signals for the power semiconductors are generated by the modulation proposed in [17] and patented in [18]. The MC applies voltage v_p to the high-frequency transformer (HFT) [34]. The full-bridge produces i_o by impressing v_s in the HFT secondary. Finally, the output filter reduces the ripple in the DC current i_{DC} that charges and discharges the battery pack.

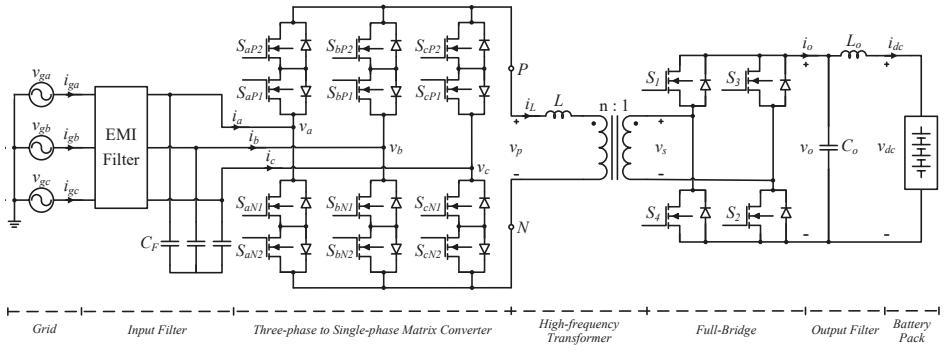


Figure 1. Circuit schematic of the high-frequency link matrix converter.

The EMI filter is projected to attenuate the noise present on currents $i_{a,b,c}$ generated by the three-phase to single-phase matrix converter. For this reason, the matrix converter side is considered the input of the filter and the grid side the output. It is expected that the conducted noise existent in currents $i_{ga,b,c}$ be within the limits specified in the international standards.

3. Standards and CE Measurement

The CE are generated by harmonics present in the input current of the MC, $i_i = [i_a, i_b, i_c]$, where i_a, i_b and i_c are the phase currents. EMC standards classify the CE according to the frequency range [35]. Low-frequency harmonics are typically measured up to 2 kHz (40th harmonic) as defined by IEC 61000-3-2 [36]. Section 6 presents the low-frequency (LF) harmonics measured for this converter and compared with IEC 61000-3-2 Class A limits. Regarding the HF conducted emissions, CISPR 11 [37] specifies the limits for frequencies from 150 kHz to 30 MHz. These emissions can be estimated by simulating the converter operation without any input filter at nominal conditions: $P_{nom} = 10$ kW, line-to-neutral grid voltage $V_{g,ln} = 230$ V, grid frequency $f_g = 50$ Hz and output voltage $V_{DC} = 380$ V. A simulation model of the HFLMC was implemented in GeckoCIRCUITS (v1.7.2 Professional, Gecko-Simulations A.G., Dübendorf, Switzerland) [38]. This software has a measure block that performs analysis according to the CISPR 16 [39] standard using the time domain simulation data. Similar to a test receiver (TR), it is possible to select different signal processing options: average (AVG), quasi-peak (QP) or peak detection. The first step of the filter design is to specify the maximum admissible CE levels. Due to the type of application, the QP limits of the CISPR 11 Class B curve will be considered. A line impedance stabilizing network (LISN) is connected between the grid and the device under test (DUT) in order to provide a known impedance and ensure the reproducibility of the measurements [40]. Then, a TR calculates the CE in "dBµV" through the measurement of the voltage at the LISN output port, V_{TR}. An equivalent impedance of 50 Ω/50 µH is specified by the CISPR 16 standard for the TR/LISN. The LISN's transfer function from V_{TR} to DUT's input current is [41]:

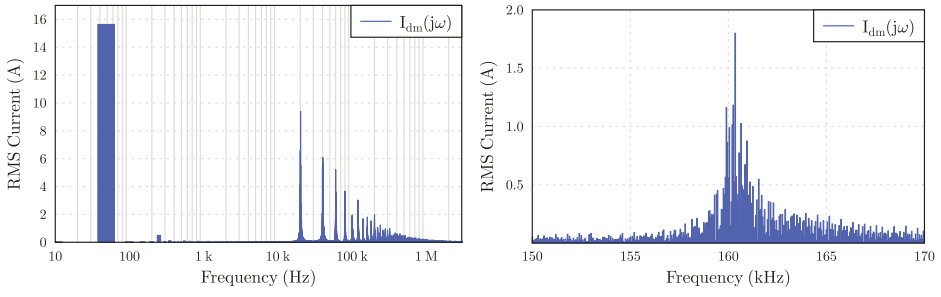
$$G_{LISN}(s) = \frac{V_{TR}(s)}{I_{dut}(s)} = \frac{s^2 L_{LISN} C_{LISN} R_{TR}}{s^2 L_{LISN} C_{LISN} + s R_{TR} C_{LISN} + 1}, \quad (1)$$

where $R_{TR} = 50\,\Omega$, $L_{LISN} = 50$ µH and $C_{LISN} = 250$ nF.

4. Design of Differential-Mode Filter

4.1. Spectrum of the Converter Input Current

Due to the symmetry of the converter and the measurement system, the DM input filter can be projected considering a single-phase equivalent circuit [27]. Figure 2a shows the spectrum of the input current of one phase, $I_{dm}(j\omega)$, obtained from simulation. Since no circuit element is connected between the lines and the ground (PE), only DM current is present at $I_{dut}(s)$. As can be seen, the first significant harmonic content appears around the switching frequency, $f_s = 20$ kHz. Other harmonics are also present at frequencies multiple of f_s. The first switching frequency harmonic inside the measurement range appears at 160 kHz. A zoom around this frequency is depicted in Figure 2b.



(**a**) (**b**)

Figure 2. (**a**) frequency spectrum of the converter input current $I_{dm}(j\omega)$; (**b**) zoom around the first switching frequency harmonic above 150 kHz.

4.2. Spectrum of the Measured Voltage

The spectrum of V_{TR} can be determined by the multiplication of $I_{dm}(j\omega)$ with Equation (1). Figure 3 depicts the spectrum of $V_{TR}(j\omega)$ at the LISN's output terminals along with the maximum and minimum estimation of the CE levels using QP detection. The exact QP values will be between the Max_{TR} and Min_{TR} curves. Further details about the modeling of the TR and the determination process of these curves are described in [23].

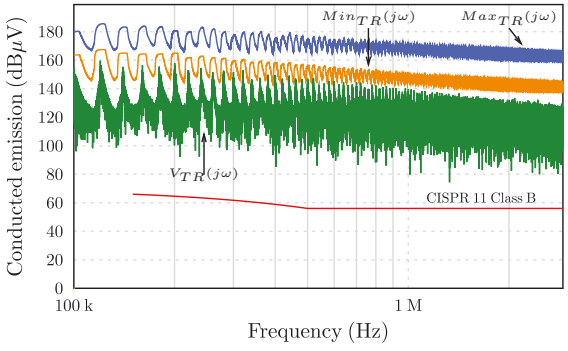


Figure 3. TR measurement without the DM filter: maximum and minimum estimation of CE along with the spectrum of $V_{TR}(j\omega)$.

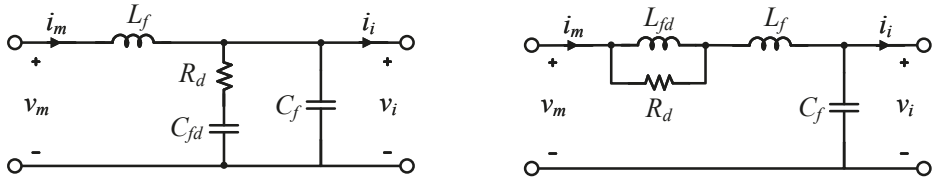
4.3. Required Attenuation

The required attenuation for the DM filter can be estimated without the need for calculating the exact QP values. The predicted CE level at 160 kHz by Max_{TR} curve is 182.9 dBμV. By analysing this curve, the next switching frequency harmonic appears at 180 kHz and requires lower attenuation. Thus, the filter design will focus on the emissions at 160 kHz. The limit specified at this frequency by CISPR 11 is $Limit_{CISPR,160kHz} = 65.5$ dBμV. A margin of 6 dB is added in order to account for possible inaccuracies in CE estimation, and also for the parasitics of the inductive and capacitive components [41]. In this way, the design process can be faster since the parasitic effects are not considered in the first step. Finally, the required attenuation of the DM filter at 160 kHz is:

$$Att_{req,DM} = Max_{TR,160kHz} - Limit_{CISPR,160kHz} + Margin = 123.4 \text{ dB}. \quad (2)$$

4.4. Topology

In theory, there are a large number of filter topologies that can be employed for EMI filtering. However, a low number of topologies are used due to cost and complexity reasons [41]. The second-order *LC* circuit is a very common topology employed as the input filter of MC [42]. In order to minimize the resonance that occurs at the filter, natural frequency, active and passive damping solutions were proposed in [21,22,43]. Passive damping is achieved by adding a resistor in series or in parallel with an inductor or capacitor. Considering the simple *LC* circuit, it was demonstrated in [25] that the minimum power losses are obtained with a resistor connected in parallel with the inductor. Moreover, this solution also reduces the global cost and volume of the input filter [14]. More complex damping networks can be obtained by adding an additional inductor or capacitor in series or in parallel with the damping resistor [22]. The objective of these damping networks is to provide passive damping to a filter without increasing excessively the power dissipation. By modifying the peak output impedance, this damping aims to facilitate the controller design and avoid large oscillations during transients [41]. Figure 4 shows two *LC* filter topologies with single resistor damping networks [22]. Both have a high frequency attenuation asymptote given by $1/(\omega^2 L_f C_f)$, which is identical to the original undamped *LC* filter. For the shunt *RC* damping network, C_{fd} blocks the DC current in order to avoid significant power losses in R_d. However, the large total capacitance reduces the power factor for low-power operation making this solution unattractive.



(**a**) (**b**)

Figure 4. Two *LC* filter topologies with single resistor damping networks. (**a**) shunt *RC* damping network; (**b**) series *RL* damping network.

Regarding the series *RL* damping network, L_{fd} provides a DC bypass to avoid significant power dissipation in R_d. Therefore, both inductors must be rated for the peak DC current. The output impedance of the *LC* filter is dominated by the inductor impedance at a low frequency and by the capacitor impedance at a high frequency [44]. Both asymptotes intersect at the filter resonant frequency:

$$f_0 = \frac{1}{2\pi\sqrt{L_f C_f}}. \tag{3}$$

As previously discussed, $V_{TR}(j\omega)$ is dependent on the DUT's input current. Therefore, $I_{dm}(j\omega)$ must be reduced in order to generate CE within the imposed limits. Transfer function $H_{lcrl}(s)$, which relates I_{dm} with I_i, is defined in Equation (4). The magnitude of $H_{lcrl}(s)$ characterizes the attenuation capability of a single-stage *LC* filter with series *RL* damping network (cf., Figure 4b):

$$H_{lcrl}(s) = \frac{sL_{fd} + R_d}{s^3 C_f L_f L_{fd} + s^2 C_f R_d (L_f + L_{fd}) + sL_{fd} + R_d}. \tag{4}$$

A compromise between damping and the size of L_{fd} must be done during the design process [44]. The damping ratio n_d defines the relation between inductor L_{fd} and L_f. For practical purposes, a unitary damping ratio is interesting since only one type of inductor needs to be built/purchased.

According to [41], this solution also results in acceptable losses on R_d. As demonstrated in [22], the optimum damping resistance for the series RL damping network can be calculated as:

$$R_d = \sqrt{\frac{L_f}{C_f}} \frac{1+n_d}{n_d} \sqrt{\frac{2(1+n_d)(4+n_d)}{(2+n_d)(4+3n_d)}}. \quad (5)$$

Figure 5 shows the impact of different damping factors in terms of resonance of $H_{lcrl}(s)$ for $C_f = 20$ µF and $L_f = 60$ µH. As expected, the peak in the magnitude is reduced when the damping is increased. Simultaneously, the frequency at which this peak occurs also decreases as damping rises. Nevertheless, the low and high frequency asymptotes are not affected by the damping factor.

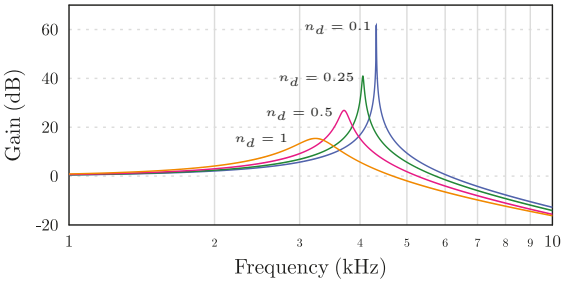


Figure 5. Impact of different damping factors in transfer function $H_{lcrl}(s)$.

For a given attenuation, the cascade connection of multiple LC filter stages allows the reduction of volume and weight when compared to a single-stage LC filter [44]. This is achieved by increasing the cutoff frequencies of the multiple stages resulting in smaller inductance and capacitance values. Nevertheless, the interaction between cascaded LC filter stages can provoke additional resonances and increased output impedance. An approach to reduce this interaction is by selecting gradually smaller cutoff frequencies as it nears the filter output [22]. In other words, higher attenuation is required for the stages near the filter output to improve system stability.

4.5. Components

In order to provide the required attenuation, a three-stage filter as shown in Figure 6 is employed. Stage 1 and Stage 2 are formed by LC filters with series RL damping networks, and Stage 3 is an undamped LC filter formed by C_3 and L_3.

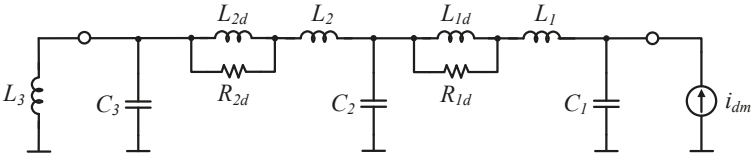


Figure 6. Equivalent single-phase circuit of the DM filter.

The DM capacitors draw reactive current from the grid, which decreases the operating power factor (PF). In order to have a minimum power factor during a light load operation, the total capacitance must be limited to the converter nominal power. In [45], the authors suggest that the PF must be at least 0.9 for operation at 10% of P_{nom}. Other authors consider that a 0.8 power factor for the same operating conditions is reasonable [28]. The capacitance limitation can also be specified in terms of the absolute value for the reactive power. For instance, in [20], it is proposed that the reactive power drawn by the input filter must be restricted to 15% of P_{nom}. Assuming a small voltage drop for the

fundamental component across the filter inductors, the total reactive power absorbed can be calculated by Equation (6). Considering this last criteria, the maximum capacitance per phase must be restricted to $C_{f,total} \leq 30$ µF:

$$Q_{C_f} \approx 3 \cdot 2\pi \cdot f_g \cdot C_{f,total} \cdot V_{g,ln}^2. \tag{6}$$

4.5.1. Stage 1

The matrix converter is a voltage-fed topology and behaves as a current source at its input. Capacitor C_1 (C_F in Figure 1) is placed at the MC input in order to limit the voltage ripple and ensure a correct system operation. For the worst operations conditions, the peak current at the MC input is $\hat{I}_i = 37$ A. By defining $\delta_{vCf,pp}$ as the maximum peak-to-peak voltage ripple, the minimum required capacitance can be calculated as [46]:

$$C_1 \geq \frac{\hat{I}_i}{1.1 \cdot V_{g,ln} \cdot 2\pi \cdot f_s \cdot \delta_{vCf,pp}}. \tag{7}$$

By limiting $\delta_{vCf,pp}$ to about 5–10% of the nominal input voltage [41,46], the minimum required capacitance must be between 11.6 and 23.2 µF. Due to the discrete availability of capacitance values and also for practical implementation reasons, capacitor C_1 is selected to 20 µF.

The magnitude of the LF current harmonics can be affected if the resonant frequency (f_0) of the different filter stages is near the measurement range (up to 2 kHz). However, the resonant frequency must be significantly lower than the switching frequency in order to provide sufficient attenuation at $f = f_s$. Therefore, it is common to choose a resonant frequency between 20 times the grid frequency and about one-third of the switching frequency [26]. Considering this criteria, the resonant frequency for Stage 1 must be between 1 and 6.66 kHz. As previously discussed, the attenuation for this stage must be higher than the other stages, resulting in a lower resonant frequency for Stage 1 when compared to Stage 2. The attenuation for Stage 1 is selected as $Att_{Stage1} = 0.5 \cdot Att_{req,DM}$, which by the following:

$$f_{0,Stage1} = \frac{160kHz}{\sqrt{10^{\frac{Att_{Stage1}}{20}}}} \tag{8}$$

results in $f_{0,Stage1} = 4588$ Hz. Considering C_1 and Equation (3), L_1 is calculated as 60 µH. For $n_{1d} = 1$, the damping network is composed by $L_{1d} = 60$µH and $R_{1d} = 3.4\ \Omega$ according to Equation (5).

4.5.2. Stage 2

For practical reasons, L_2 and L_{2d} are selected to be equal to L_1 and L_{1d}. By defining $Att_{Stage2} = 0.35 \cdot Att_{req,DM}$, the resonant frequency of Stage 2 needs to be $f_{0,Stage2} = 13316$ Hz. Considering L_2 and Equation (3), C_2 is calculated as 2.3 µF. Due to the discrete availability of capacitance values, C_2 is selected to be 2.2 µF. Finally, the unitary damping ratio results in $R_{2d} = 10\ \Omega$.

4.5.3. Stage 3

The third stage of the filter is composed by C_3 in combination with L_3. During test experiments, L_3 corresponds to the inner inductance of the LISN, L_{LISN}. For normal operation, L_3 coincides with the grid inductance, L_g. Although the grid inductance can vary significantly depending of the PCC, for this analysis, $L_g = 50$ µH is considered, following the reference network defined in IEC 61000-3-3 [47]. This stage must provide the remainder attenuation, which can be written as $Att_{Stage3} = Att_{req,DM} - Att_{Stage1} - Att_{Stage2}$. Therefore, the resonant frequency of Stage 3 needs to be $f_{0,Stage3} = 53204$ Hz. Considering $L_3 = 50$ µH, the respective capacitor is chosen to be $C_3 = 180$ nF.

4.6. Evaluation of the DM Filter

By combining all three stages, the complete transfer function H_{dm} from I_i to I_{dm} can be obtained. Figure 7 depicts the frequency response of the DM filter. As required, a 123 dB attenuation is provided at 160 kHz. The effect of the damping networks is perceptible by comparing the gain at $f_{0,Stage1}$ and $f_{0,Stage2}$ with the gain at $f_{0,Stage3}$.

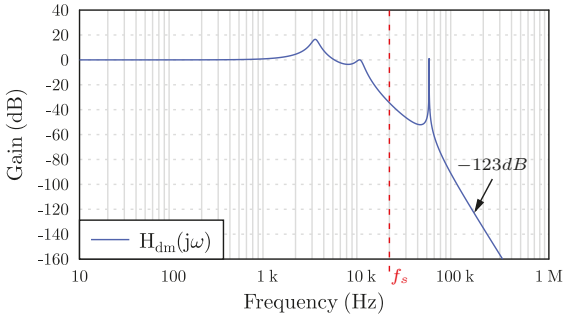


Figure 7. Frequency response of the DM filter: magnitude of H_{dm}, the transfer function from I_i to I_{dm}.

Figure 8 depicts Max_{TR} and Min_{TR} for the converter operation with the DM filter. As can be seen, the maximum curve for the predicted QP values is below the limits specified by the CISPR 11 Class B curve and the selected margin of 6 dB can be observed. Thus, the DM filter design is considered to be concluded.

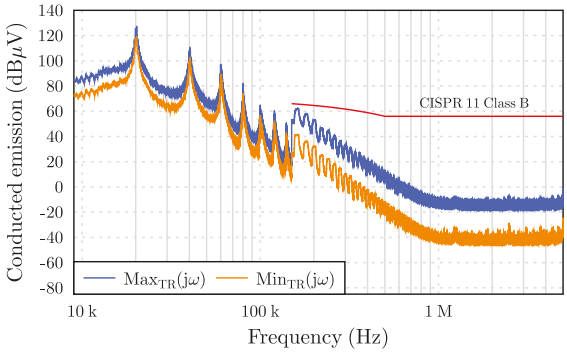


Figure 8. TR measurement with DM filter: maximum and minimum estimation of CE.

5. Design of the Common-Mode Filter

5.1. Common-Mode Voltage

The CM voltage generated by the matrix converter induces a circulating current, i_{cm}, through the converter and the ground (see Figure 9). This current closes the loop through the TR/LISN impedance resulting in CE that must be within the limits specified by CISPR 11. Silicon Carbide (SiC) MOSFET C2M0025120D is used for the converter implementation. The parasitic capacitance from the semiconductor to the heat sink per unit area is approximated by 20 pF/cm^2 [32]. Considering this reference value, the parasitic capacitance of all the matrix converter's semiconductors is $C_{gh} = 600$ pF. Regarding the transformer interwinding capacitance and the stray primary side wiring capacitance, it is difficult to estimate these values without making measurements. For this reason, a 1.2 nF capacitance is added to the simulated circuit in order to take into account these parasitics. Thus, a total parasitic

capacitance to ground $C_g = 1.8$ nF is considered. The resulting CM voltage, v_{cm}, impressed by the MC is represented in Figure 9. This voltage has approximately 110 V_{rms} and a peak equal to $\hat{V}_{g,ln}$.

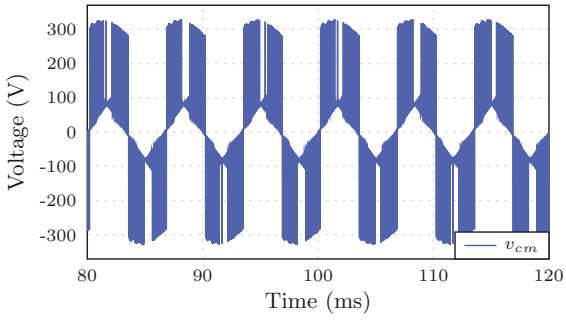


Figure 9. Common-mode voltage impressed by the matrix converter.

The frequency spectrum of the simulated RMS common-mode current ($i_{cm}(j\omega)$) for this operating point is shown in Figure 10. A zoom around the first switching harmonic inside the measurement range is shown in Figure 10b.

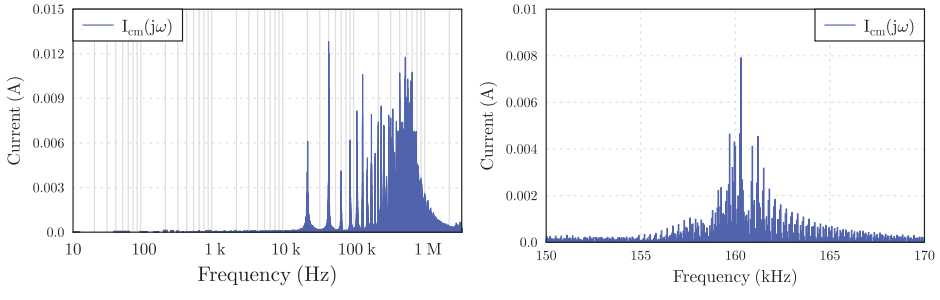


Figure 10. (**a**) frequency spectrum of the common-mode current $I_{cm}(j\omega)$; (**b**) zoom around the first switching frequency harmonic above 150 kHz.

5.2. Spectrum of the Measured Voltage

The converter and the measurement system can be reduced to its single-phase equivalent CM circuit as represented in Figure 11. It is important to note that, from the CM point of view, the three line-to-ground capacitors of each stage are in parallel. Thus, the effective common-mode capacitance is equal to the sum of the three capacitor values [48]. The LISN and the TR are modeled by its equivalent CM impedance. v_{cm} is modeled by an ideal voltage source.

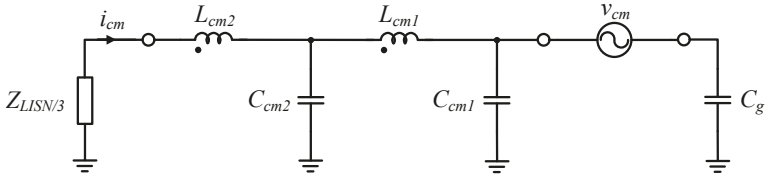


Figure 11. Equivalent single-phase circuit of the CM filter.

The C_g connected to the ground represents the parasitic capacitance. The spectrum of V_{TR} can be determined by the multiplication of $I_{cm}(j\omega)$ with the LISN's transfer function $G_{LISN,CM} = G_{LISN}/3$. Figure 12 depicts the spectrum of V_{TR} at the LISN output terminals along with the Max_{TR} and Min_{TR} using QP detection.

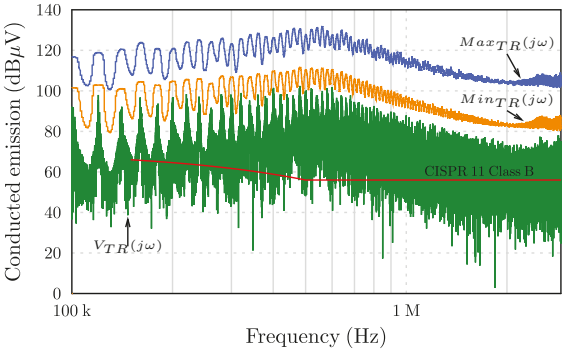


Figure 12. TR measurement without CM filter: maximum and minimum estimation of CE along with the spectrum of $V_{TR}(j\omega)$.

5.3. Required Attenuation

The required attenuation for the CM filter can be estimated without the need of calculating the exact QP values. The predicted CE at 160 kHz by $Max_{TR}(j\omega)$ curve is 123.7 dBμV. The limits specified in the CISPR 11 Class B for CM are equal to the DM. Considering the limit at 160 kHz and including a margin of 6 dB, the required attenuation of the CM filter at 160 kHz is $Att_{req,CM} = 64.2$ dBμV.

5.4. Topology

In order to limit i_{cm}, the EMI filter must maximize the mismatch between the power source and the converter impedances [49]. *LC* circuits are usually employed for the common-mode filter [50]. In contrast with the DM filter, no additional damping needs to be added by external elements. The CM inductors are connected in series with the lines in order to provide a high-impedance for the common-mode noise. The three windings of the inductor are wound on the same core, which forms a common-mode choke. Because the power line currents are symmetrically displaced in each winding, the magnetic flux produced in the core by these currents cancels.

5.5. Components

In order to provide the required attenuation a two-stage CM filter is employed (see Figure 11). Stage 1 and Stage 2 are formed by undamped LC filters that make the connection between the lines and the ground (PE). The maximum value of the line-to-ground capacitance is limited by the leakage requirements imposed by several safety agencies [48]. This safety measure is necessary for protection of personnel against electric shock under fault conditions.

According to IEC 60950, the ground leakage current for Class I equipment must be limited to $I_{leak,max} = 3.5$ mA at 50 Hz. This requirement has a great impact on the CM filter design. Considering the upper limit of the grid RMS voltage, a maximum total CM capacitance per phase of $C_{cm,max} = 44$ nF is calculated by:

$$C_{cm,max} = \frac{I_{leak,max}}{1.1 \cdot V_{g,ln} \cdot 2\pi \cdot f_g}. \tag{9}$$

According to [41], for maximum attenuation given a minimum total capacitance, each stage shall present the same value. In order to provide some margin to the imposed limit of $C_{cm,max}$, a total capacitance per phase of 20 nF is chosen. Therefore, capacitors C_{cm1} and C_{cm2} must be 10 nF. Considering this capacitance, the value of the CM choke of each stage is then chosen to provide half of the required CM attenuation ($Att_{Stage1-2,CM} = 0.5 \cdot Att_{req,CM}$). Thus, the cut-off frequency should be $f_{0,Stage1-2,CM} = 25.2$ kHz. Taking this frequency into account, inductor L_{cm1} and L_{cm2} are selected to 1.3 mH.

5.6. Evaluation of the CM Filter

By combining the two stages, the complete transfer function H_{cm} from I_i to I_{cm} is obtained. Figure 13 depicts the gain of the CM input filter. As required, a 64 dB attenuation is provided at 160 kHz.

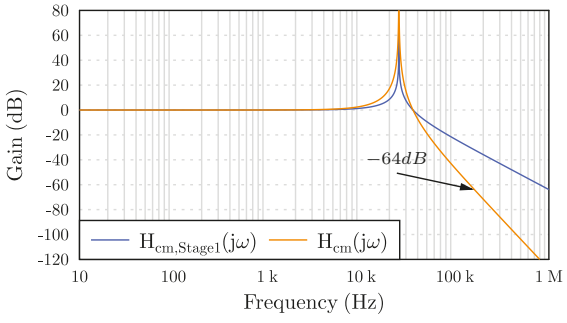


Figure 13. Frequency response of the CM filter: magnitude of H_{cm}, the transfer function from I_i to I_{cm}.

Figure 14 depicts the maximum and minimum estimation of the CE for the converter operation with the CM filter. As can be seen, the maximum curve for the predicted QP values is below the limits specified by CISPR 11. Thus, the CM filter design is considered to be concluded.

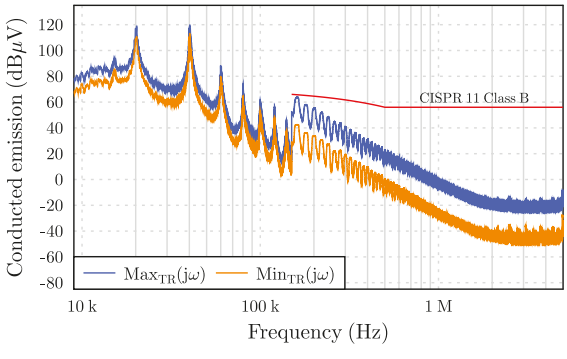


Figure 14. TR measurement with CM filter: maximum and minimum estimation of CE.

6. Integration of DM and CM Filter

The final step for the design of the EMI filter is the integration of the DM and CM stages. There are several ways to perform this integration. Due to the imperfect coupling between the three windings of a CM choke, some leakage inductance is present in L_{cm1} and L_{cm2}. The inductors of both DM and CM filters can be combined in each stage, so that this leakage inductance can be employed as part of the required DM inductance. Using this strategy, a small DM inductor can be employed reducing

the volume and weight of the filter. Figure 15 shows the complete circuit of the EMI filter. All of the components are listed in Table 1.

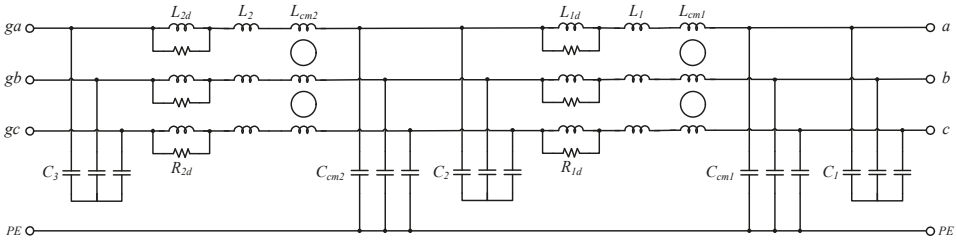


Figure 15. Complete circuit of the EMI filter comprising the DM and the CM filtering stages.

Table 1. Components for the EMI filter.

Component	Specification
C_1	EPCOS, MKP B32928C3206K, X2, 20 µF, 305 V_{ac}
C_2	EPCOS, MKP B32924C3225K, X2, 2.2 µF, 305 V_{ac}
C_3	Murata, GA3 GB563K, X7R, 56 nF, 250 V_{ac} (×3)
L_1, L_2, L_{1d}, L_{2d}	Micrometals, Iron Powder T184-52, 21 turns, 12 AWG
R_{1d}	Bourns, SMD CRS, 3.3 Ω, 2 W
R_{2d}	Bourns, SMD CRS, 10 Ω, 2 W
C_{cm1}, C_{cm2}	Murata, Ceramic DE2F3KY, Y2, 10 nF, 250 V_{ac}
L_{cm1}, L_{cm2}	Schaffner, RB8532-16-1M3, 1.3 mH, 16 A

Toroidal cores are preferred for the DM inductors (L_1, L_{d1}, L_2, L_{d2}) since they create a low external magnetic field, reducing the magnetic coupling with other elements in the circuit. Iron powder material is selected since it presents a much higher saturation flux density than ferrites, resulting in a more compact inductor [41]. The distributed air-gap is also a constructive advantage when compared with ferrites. Cores from Micrometals [51] were chosen mainly due to its low-cost and availability in the market. The −52 material is suitable to be used in differential-mode filter applications. This material features a nominal saturation flux of 1.0 T and can be operated at temperatures up to 110 °C. Core size T184 was selected in order to maintain inductance for the required energy storage. The inductor was constructed in a single layer in order to reduce the winding parasitic parallel capacitances. Furthermore, a solid round conductor is employed to take advantage from the increased resistance with frequency [41]. Using GeckoMAGNETICS software (v1.4.4 Professional, Gecko-Simulations A.G., Dübendorf, Switzerland) [52], the required number of turns was projected so as to obtain the nominal inductance at half of the peak current. This criterion takes into account the 9.1 µH leakage inductance of the CM chokes (L_{cm1}, L_{cm2}). The losses for the designed DM inductors are estimated at 2.1 W with a 15 °C temperature rise at P_{nom}. Core T184-52 has a product of number of turns by the current (NI) of 951 at 80% saturation flux density, B_{sat}. Dividing this number by 21 turns, it can be concluded that at least 45.3 A can flow in this inductor without provoking saturation while keeping a 20% margin.

Voltage surges due to electrical discharges and under voltages during load steps can appear at the MC input. Since the aforementioned voltages are usually high, metallized polypropylene capacitors (MKP) are selected for C_1 and C_2 due to its higher ripple current capacity and lower ageing when compared with electrolytic capacitors [45]. Moreover, capacitors from class X2 need to be chosen

since they are specifically for "across-the-line" applications. Capacitors from class X2 can withstand pulse peak voltages up to 2.5 kV in accordance with IEC 60664. Ceramic capacitors for C_3, C_{cm1} and C_{cm2} are preferred since a small capacitance is required, leading to a compact construction and low parasitics. Due to safety reasons, CM capacitors are from class Y2, which is specifically for "line-to-ground" applications.

According to the IEC 60950 standard, the capacitors connected across the lines should be discharged to a voltage lower than 60 V in less than 10 seconds after a supply disconnection. This is required since both DM and CM capacitors remain charged to the value of the mains supply voltage at the instant of disconnection. If a hand or any other body part touch two pins of the mains supply plug at the same time, the capacitors will discharge through that body part. This discharge can be quite painful and for this reason, resistors of large value are connected across the lines in parallel with such capacitors. In this EMI filter, 130 kΩ SMD resistors with a power rating of 2 W are employed.

Figure 16 shows a photo of the assembled EMI filter. The PCB also includes current sensors, relays and fuses for protection. C1 capacitors are mounted in another board near the SiC MOSFETS in order to reduce the parasitic inductances.

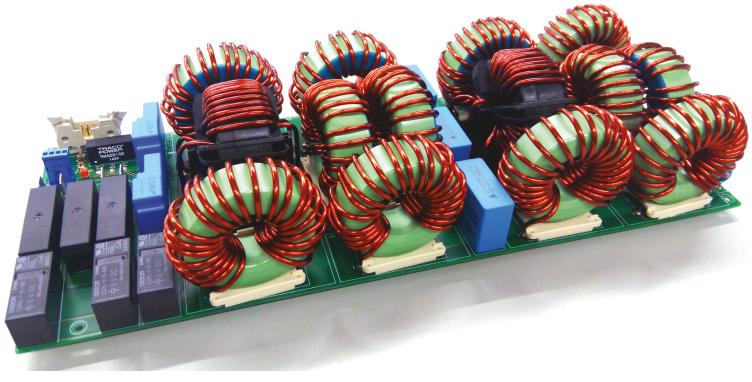


Figure 16. Photo of the EMI filter implementation.

As discussed in Section 3, low-frequency current harmonics are generated by the converter and are mainly dependent of the employed modulation. However, the resonant frequencies of the EMI filter could make interference in this measurement range. A final simulation with the integration of the DM and CM filters was performed. Figure 17 shows the measured low-frequency harmonics of the grid current and compares it with the IEC 61000-3-2 [36] Class A limits. As can be seen, the limits of the standard were not exceeded and the effectiveness of the EMI filter is verified.

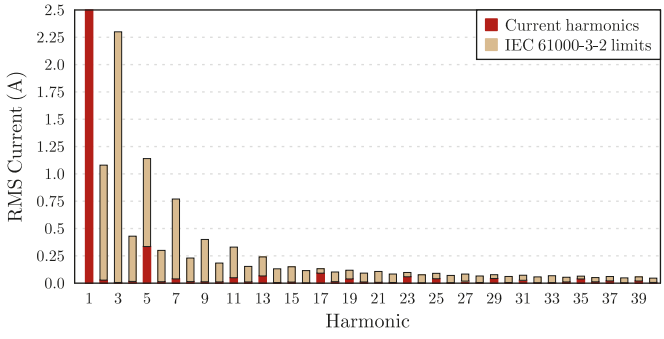


Figure 17. Low-frequency harmonics of grid current compared to IEC 61000-3-2 limits: simulation with the EMI filter comprising the DM and CM filters.

7. Experimental Results and Discussion

A prototype of the HFLMC was designed and built to test the capability to generate grid currents with a high-power quality [17]. Figure 18 shows the three grid currents and the battery current in both charger and inverter mode. As can be seen, the grid currents are well controlled (*d*-*q* control) and form a perfectly symmetric three-phase system. Since the HFLMC performs a single-stage power conversion, there is no significant energy storage between the grid and the battery. As a consequence, the battery current has a very fast dynamic response when a power flow inversion occurs at the grid side, such as at instant 140 ms.

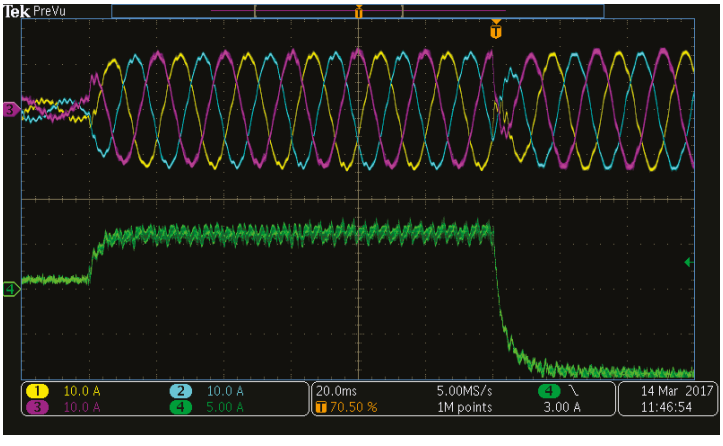


Figure 18. Experimental results of the HFLMC operating in charger and inverter mode: grid currents (i_{ga}, i_{gb}, i_{gc}) [yellow, blue, magenta] and battery current (i_{DC}) [green].

The low-frequency harmonics of the grid currents were also measured in the laboratory using the PA1000 Power Analyzer from Tektronix (Beaverton, OR, USA). The total harmonic distortion (THD) is 2.58 % at 10.2 Arms in charger mode and 3.44 % at 9.0 Arms in inverter mode. From the measurements, all the harmonics are within the limits specified by the IEC 61000-3-2 standard.

EMI filters are usually characterized by the insertion loss (IL) that is a measure of the interference suppression capability of a filter [35]. IL can be determined by using the scattering s-parameters defined for the 2-port network circuits. The most accurate way to measure s-parameters is using a vector network analyzer (VNA) [53]. The test procedure is specified in CISPR 17 [54] standard. Figure 19 shows the test circuits used for measuring the IL for the DM and CM stages. The VNA

generates a signal with a pre-defined power and variable frequency at its port 1. This signal is then propagated through the DUT and measured at the VNA port 2. CISPR 17 specifies that the source and load impedances of the VNA must be equal to $Z_0 = 50\ \Omega$. Since the impedances are matched, IL coincides with the magnitude of the forward transmission coefficient S_{21}, as defined by Equation (10):

$$IL = -20 \cdot log_{10}|S_{21}|, dB. \tag{10}$$

Balanced-unbalanced transformers, also known as "baluns", must be connected to the VNA ports in order to isolate the DUT from the ground plane during DM measurements, as represented in Figure 19a. Moreover, the baluns are essential to provide very high CM rejection.

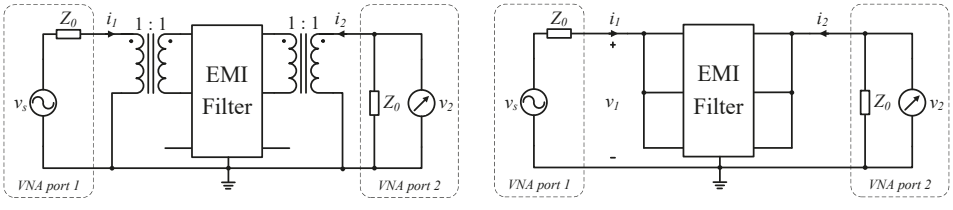


Figure 19. Test circuits for measuring the insertion losses in EMI filters. (**a**) differential-mode (symmetrical); (**b**) common-mode (asymmetrical).

The Coilcraft PWB1010LB [55] wideband transformer (Coilcraft, Cary, IL, USA) was mounted in a shielded housing with BNC receptacles as shown in Figure 20a, resulting in a 50 Ω : 50 Ω balun with a 3.5 kHz to 125 MHz bandwidth. A Rohde–Schwarz ZVL 3 (Rohde–Schwarz, Munich, Germany) with an operating frequency range from 9 kHz to 3 GHz was employed for the measurements. Coaxial cables with a characteristic impedance of 50 Ω were used to connect the DUT to the measurement equipment. The test bench with the baluns and the VNA is shown in Figure 20b.

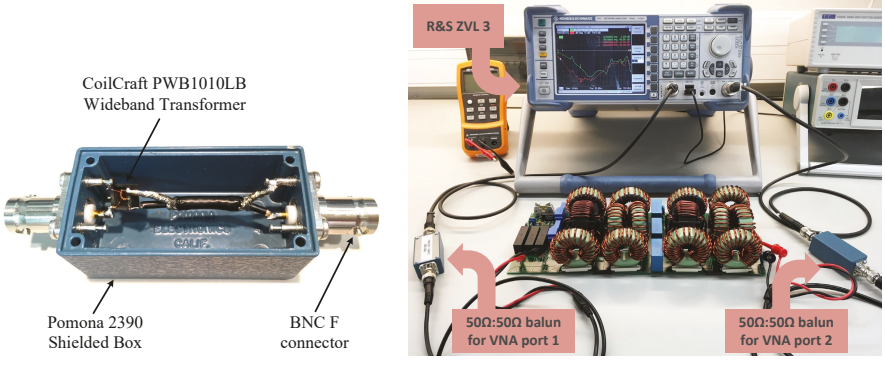


Figure 20. Differential-mode S_{21} parameter measurement. (**a**) photo of the constructed balun; (**b**) photo of the test bench.

The DM S_{21} parameter was measured between phase A and B while the other lines remained unconnected. Figure 21a depicts the obtained results for the DM Stage 2 and also for the series of Stage 1 and 2. As measured by the R&S ZVL 3, $S_{21,dm,Stage2} = -50.2$ dB for Stage 2 and $S_{21,dm,Stage1-2} = -92.4$ dB for Stage 1 and 2. The former result is inferior when compared with

the expected 104.9 dB. This is justified since the measurements are performed with a power of 20 dBm (equivalent to 100 mW). For this power level, the DM inductors have a higher inductance as explained in Section 6. Consequently, a shift in the resonant frequency occurs, resulting in a smaller attenuation. However, this is not a problem since, for higher currents, the effective inductance is within the expected range.

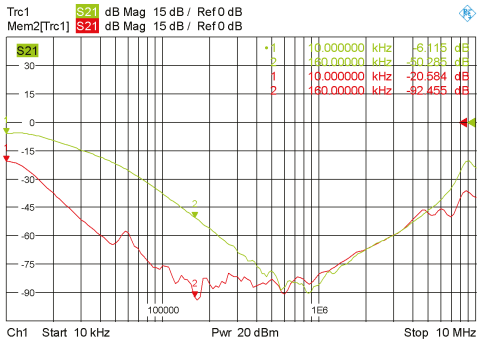


Figure 21. S_{21} parameter of the EMI filter measured with R&S ZVL 3 VNA. (**a**) differential-mode $S_{21,dm,Stage2}$ [Trc1] and $S_{21,dm,Stage1-2}$ [Mem2]; (**b**) common-mode $S_{21,cm,Stage1}$ [Trc1] and $S_{21,cm,Stage1-2}$ [Mem2].

For the CM S_{21} parameter measurement, the baluns are not needed since the ground plane of the VNA is directly connected to the PE terminal of the EMI filter. Figure 21b depicts the obtained results for the CM Stage 1 and also for the series of Stage 1 and Stage 2. As specified in Section 5, each stage must provide half of the required attenuation, more specifically 32.1 dB. As can be seen, $S_{21,cm,Stage1} = -31.2$ dB for one stage and $S_{21,cm,Stage1-2} = -62.0$ dB for the complete CM filter. These values are clearly aliened with the predicted ones.

With the results exported by the R&S ZVL 3, the insertion losses were computed using Equation (10) and depicted in Figure 22. It is clearly noticed that parasitic effects limit the achievable insertion losses and degraded the EMI filter performance for frequencies above 1 MHz. This can be explained by the parasitic series inductance of capacitors and the capacitance across the choke coils [56]. There are modeling methods for passive components that can be used to predict the high frequency parasitic effects that typically create EMC degradation [57]. For the current project, the required attenuation at these high-frequencies is less than the attenuation required at 160 kHz. This margin can be observed at the curves represented in Figures 8 and 14. Therefore, the performance of the filter is not compromised and complies with the specifications.

Electromagnetic field (EMF) simulation tools for analyzing EMI offer more accurate results than the tools based on circuit simulators. However, EMF simulation needs a high number of computational resources and are expensive tools. In order to meet the time requirements of the development cycle of the products, it is often only applied to very simplified models. The main weakness of this method is precisely the fact that parasitic elements of the components are not modeled, since it would require significant additional effort that is not compatible with the straightforward design approach that proposed. As a consequence, some components could have to be changed after the experimental pre-compliance tests in order to ensure the expected attenuation capability in the high-frequency range.

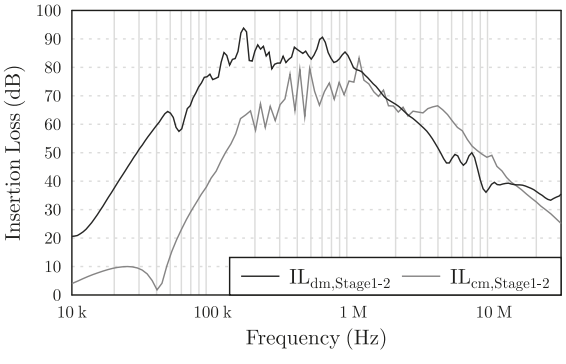


Figure 22. Measured insertion losses for DM filter [$IL_{dm,Stage1-2}$] and CM filter [$IL_{cm,Stage1-2}$].

The main strength of this design method is to present a framework for quickly obtaining a project of the EMI filter that can be also extended to other current source converters. This can be of high value for engineers that need a practical and guided way to design an EMI filter for their projects. For sure, some time-savings can be obtained since the main input for this project is the frequency spectrum of the converter input current and the common-mode voltage. As previously demonstrated, these inputs can be obtained through simulation or experimental measurements.

8. Conclusions

This paper details a step-by-step design method for the DM and CM filters of the HFLMC. This procedure can be extended to other current source converters provided that the spectrum of the input current is known. The conducted emissions are determined by a simulation model that includes the modeling of the measurement system. Each filtering stage is projected based on the required attenuation for CISPR 11 Class B pre-compliance. Both filters are integrated in a synergistic way in order to reduce volume and weight. A prototype of the filter was constructed and tested in the laboratory. An experimental test bench was mounted to determine the insertion losses according to the CISPR 17 standard. The obtained results confirm that the attenuation capability of the filter is in the expected range. Therefore, the effectiveness of the EMI filter regarding both LF harmonics and HF conducted emissions is confirmed.

9. Patents

D. Varajao, L. M. Miranda, and R. E. Araujo, "AC/DC converter with a three to single phase matrix converter, a full-bridge AC/DC converter and HF transformer," U.S. Patent 9,973,107 B2; United States Patent and Trademark Office (USPTO), Alexandria, VA, USA, 15 May 2018 (Priority date: 13 August 2014).

Author Contributions: D.V. made the step-by-step design of the filter including the verification based on software simulation. R.E.A. supervised the filter design and suggested the the experimental validation approach. L.M.M. and D.V. constructed the EMI filter and implemented the test bench for insertion losses' characterisation. All of the authors participated in the discussion of the results. D.V. and R.E.A. wrote the paper in consultation with L.M.M. and J.A.P.L.

Funding: This work was supported in part by the ERDF—European Regional Development Fund through the Operational Programme for Competitiveness and Internationalisation (COMPETE 2020 Programme), in part by National Funds through the Portuguese funding agency, FCT—Fundação para a Ciência e a Tecnologia, within the project SAICTPAC/0004/2015—POCI-01-0145-FEDER-016434, and in part by the FCT under Scholarship SFRH/BD/89327/2012.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

AC–DC	Alternating Current to Direct Current
AVG	AVG
BESS	Battery Energy Storage Systems
BNC	Bayonet Neill–Concelman
CE	Conducted Emissions
CISPR	International Special Committee on Radio Interference
CM	Common-Mode
DM	Differential-Mode
DUT	Device Under Test
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EV	Electric Vehicles
HF	High-Frequency
HFLMC	High-Frequency Link Matrix Converter
HFT	High-Frequency Transformer
IEC	International Electrotechnical Commission
LISN	Line Impedance Stabilizing Network
LF	Low-frequency
MC	Matrix Converter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MKP	Metallized Polypropylene Capacitors
PCB	Printed Circuit Board
PE	Protective Earth (Ground)
PF	Power Factor
PK	Peak
QP	Quasi-Peak
RMS	Root Mean Square
THD	Total Harmonic Distortion
TR	Test Receiver
VNA	Vector Network Analyzer

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Reliability of Boost PFC Converters with Improved EMI Filters

Haoqi Zhu, Dongliang Liu *, Xu Zhang and Feng Qu

College of Automation, Hangzhou Dianzi University, Hangzhou 310018, China; hqzhu23@163.com (H.Z.); ZX_HDU@163.com (X.Z); qfeng137@163.com (F.Q)

* Correspondence: liudl@hdu.edu.cn; Tel.: +86-18767187825

Received: 9 November 2018; Accepted: 4 December 2018; Published: 8 December 2018

Abstract: The switching device in a power converter can produce very serious electromagnetic interference (EMI). In order to solve this problem and the associated reliability and stability issues, this article aimed to analyze and model the boost power factor correction (PFC) converter according to the EMI conduction path. The sources of common-mode (CM) and differential-mode (DM) noise of the boost PFC converter were analyzed, and the DM and CM equivalent circuits were deduced. Furthermore, high-frequency modeling of the common-mode inductor was developed using a precise model, and the EMI filter was designed. According to the Class B standard for EMI testing, it is better to restrain the EMI noise in the frequency range (150 kHz to 30 MHz) of the EMI conducted disturbance test. Using this method, a 2.4-kW PFC motor driving supply was designed, and the experimental results validate the analysis.

Keywords: common-mode inductor; high-frequency modeling; electromagnetic interference; filter

1. Introduction

With the rapid development of electronic technology, power converters are widely used in various fields [1]. The application of the product requires the power to be converted to maintain high reliability and stability. In order to pursue higher performance and smaller size, the switching frequency of power devices is becoming increasingly higher [2,3]. With the continuous improvement of the switching frequency in power devices, its reliability became a common and urgent problem that needs to be solved. The reliability of the power converter is affected by the manufacturing process and actual operating conditions.

Scholars from various countries conducted extensive research on the reliability of converter devices and their power devices [4–6]. Power converters usually consist of switching devices, storage devices, driving devices, and signal processing and control circuits. The reliability of the converter is determined comprehensively by the reliability of each part. All kinds of capacitive elements, especially aluminum electrolytic capacitors, are key factors which affect the reliability of power converters. However, research shows that the power switching device is the most likely part to lose efficacy among the components of the converter. As the most fragile component of the power electronic switching device, the reliability of the power switching device determines the reliability of the entire device to some extent. Studying the reliability of power devices is the basis for improving the reliability of power converters [7]. The discussion of reliability in this paper is based on the influence and suppression of the interference caused by power converters in actual operation. When the device is operated beyond the rated voltage or current range, it may cause excessive electrical stress and damage to the power device [8,9]. Under excessive electrical stress, part of the device will locally overheat. When the hot-spot temperature reaches the melting point of the material, the material will melt, causing damage to the device. When the circuit interference is relatively strong, the disturbance

will form a strong inrush current through the parasitic parameters in the circuit, which will cause the power device (diode, rectifier bridge, metal-oxide-semiconductor field-effect transistor (MOSFET), etc.) to be damaged. The power switching device has a high current voltage, which causes great switching loss and strong interference. The rapidly changing dI/dt and dV/dt of the power device causes a strong interference current through the parasitic parameters in the circuit, which influences the reliability and stability of the power converter [10]. The interference current caused by the power device is mainly the common-mode (CM) current, which is the conduction interference in the converter. This can be suppressed by an electromagnetic interference (EMI) filter. Therefore, the conduction interference in the circuit of the power converter needs to be analyzed and suppressed in order to improve its reliability and stability.

Because current power converters are widely used, the electromagnetic compatibility (EMC) problem became increasingly important, a serious problem of which is the EMI [11]. The conducted interference and radiation interference need to be suppressed for correct functioning of the power converter. The radiated EMC effect of the power converter was introduced in Reference [12], and magnetic dipole array-based time-domain (TD) modeling of the electromagnetic near-field (NF) using a printed circuit board (PCB) was presented. Modeling of metallic wire susceptibility to the disturbances caused by electromagnetic near-field radiation by electronic structures in radio frequencies was introduced to suppress radiated EMC coupling of a power converter in Reference [13]. Furthermore, scholars also studied the influence of temperature and bandwidth on a power converter's lumped components [14]. These studies are helpful for the suppression of EMC in power converters.

The noise between the power converter system and ground is known as CM noise, and two power transmission paths are called differential-mode (DM) noise. In order to limit the EMI noise, a series of EMC standards were developed. These standards define the frequency range and the maximum amplitude of the allowable EMI noise. EMI filters are usually added to the circuit in order to solve the EMI issue. Analysis of EMC is based on three factors: jamming source, coupling path, and disturbed object. EMI filters can reduce the interference signal, cut off or change the propagation path of a jamming signal, and increase the anti-jamming ability of the disturbed object. For restraining the conduction EMI of power converters, we start with reducing the interference source and changing the conduction path.

Boost power factor correction (PFC) converters are widely used; thus, this paper investigated the use of boost PFC converters [15–18]. Firstly, the EMI of the boost PFC converter needed to be analyzed. The switch drain source voltage of the boost PFC converter was considered as the EMI source. According to the EMI conduction path, the causes of CM and DM interference were analyzed. The boost PFC's DM and CM equivalent circuits were derived. For the conduction interference in the circuit, an appropriate EMI filter circuit was selected. In addition, the high-frequency modeling of the common-mode inductor was analyzed in the circuit, which effectively suppressed the EMI. Finally, an EMI filter based on the improved CM inductor was designed for a PFC motor drive application. The experimental and commercial test results are presented, and the superiority of the proposed EMI filter and the reliability of the boost PFC converter are verified.

2. EMI Analysis of the Boost PFC

Due to the strong EMI found in the PFC boost circuit during testing, it affected the normal operation of the circuit. Therefore, we needed to analyze the conduction interference in the circuit. The conduction EMI of the boost PFC converter can be analyzed from two aspects: DM interference and CM interference. The DM current is transmitted between two wires, which is independent of the ground wire. The amplitude and phase of the two wires are the same, and the interference voltage is formed on the signal line. Through the parasitic capacitance of the interference source, the CM current is introduced into the ground along the ground transmission from the signal line return, where the same amplitude and phase opposite in each wire and ground, at the same time, form the interference

voltage. When the impedance of two wires in the converter is unbalanced, the distribution of the CM current is different between two conductors. Thus, the CM noise becomes the DM noise to some extent.

The drain source voltage (V_{DS}) of the power devices of the boost PFC converter can be considered as the noise voltage source of the CM and DM interferences. It is generally considered that the DM current is mainly caused by the ripple current of the inductor, and the CM current flows mainly from the drain electrode of the switch tube and the parasitic capacitor of the protector, as shown in Figure 1.

When the current of the inductor L_0 is discontinuous, the junction capacitance of inductor L_0, the switching device, and the rectifier bridge D_1–D_4 will induce resonance. The input voltage, after being rectified, will produce voltage spikes that will not only damage the rectifier bridge and switching devices, but also cause common-mode interference. Therefore, the DM capacitor C_{X1} is usually added behind the rectifier bridge to suppress the voltage spike. At this point, since the capacitance value of differential-mode capacitor C_{X1} is larger than the junction capacitance value of the rectifier diode and the switch tube, the voltage of capacitor C_{X1} remains substantially constant when the inductor current is discontinuous. When the rectifier bridge is on, the DM capacitor provides a low-impedance path for the L and N lines, which suppresses the differential-mode interference. If without capacitor C_{X1}, due to impedance imbalance in the circuit, some of the DM current in the boost PFC converter is generated by the CM current.

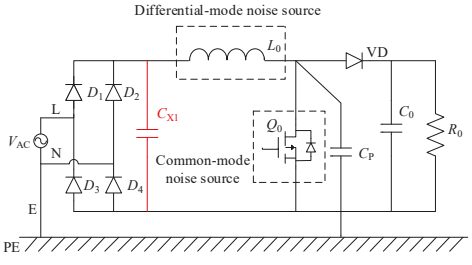
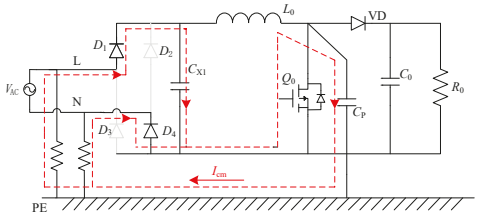


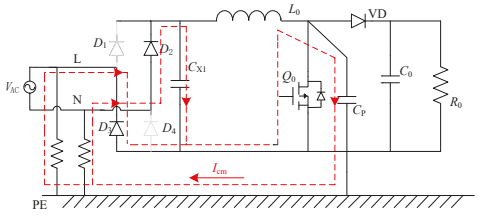
Figure 1. Common-mode (CM) and differential-mode (DM) interference sources in the boost power factor correction (PFC) converter.

When the rectifier bridge is on, due to the DM capacitance C_{X1}, the CM current from the chassis almost meets the equivalent impedance. At this time, the CM noise almost equally flows into the L and N lines, where we avoid the CM interference transformation position difference caused by the line impedance unbalance. As shown in Figure 2, the diodes in grey do not conduct. When the input voltage is positive, D_1 and D_4 conduct; however, the noise reversely flows through diode D_4 because the alternating current (AC) power grid voltage makes the diode conduct. In the negative half-cycle, D_2 and D_3 will conduct, and a similar analysis can be performed. The addition of C_{X1} will result in harmonics of the input current and needs to ensure that the frequency is higher than 150 kHz. A C_{X1} capacity resistance that is much less than 50 Ω can effectively suppress the mixed interference (the DM interference in part from the CM interference).

As shown in Figure 3, the rectifier bridge is off and the CM current passes the test resistor on the L line and D_1, which produces the interference voltage. Obviously, when the CM current does not flow through the L-line and N-line resistors, the DM voltage is generated. In order to inhibit the problem caused by the impedance imbalance, a DM capacitor can be added.

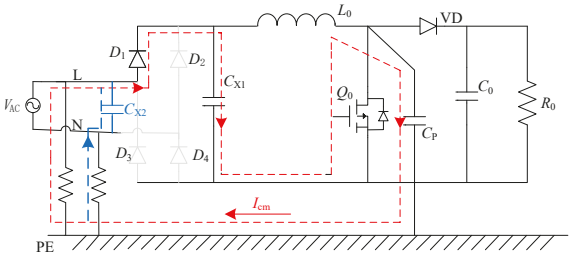


(a) D_1 and D_4 turn on

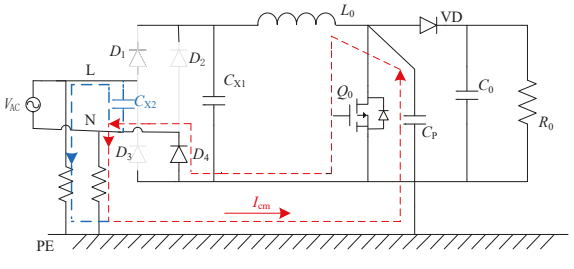


(b) D_2 and D_3 turn on

Figure 2. Common-mode current path.



(a) D_1 turn on (C_P charging)



(b) D_4 turn on (C_P discharging)

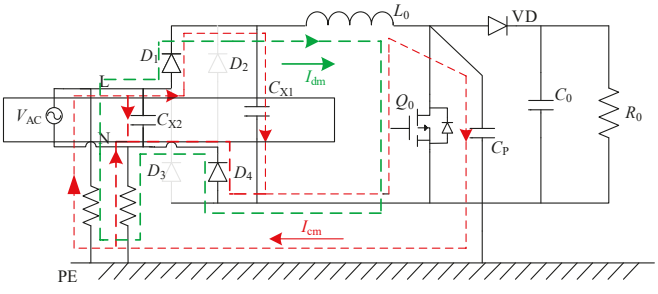
Figure 3. Common-mode current when the rectifier bridge is off.

3. Boost PFC CM and DM Equivalent Circuits

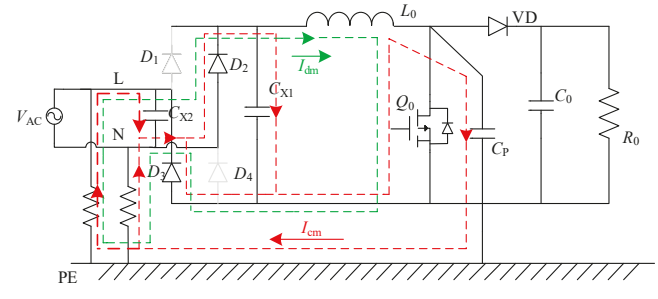
In Figure 4, the CM and DM interference paths of the boost PFC converter are given, where the capacitors C_{X1} and C_{X2} are added according to the above discussion. The green dotted line represents the DM interference path, and the red dashed line represents the CM interference path.

$$V_{CM} = \frac{V_{DS} \cdot \pi f C_P R_{LN}}{\sqrt{(\pi f C_P R_{LN})^2 + 1}} \tag{1}$$

$$V_{DM} = \frac{V_{DS} \cdot R_{LN}}{2\sqrt{R_{LN}^2(4\pi^2 f^2 L C_X - 1)^2 + 16\pi^2 f^2 L^2}} \tag{2}$$



(a) D_1 and D_4 are on



(b) D_2 and D_4 are on

Figure 4. Electromagnetic interference (EMI) paths when the rectifier bridge is on with the filter capacitors.

Figure 5 shows the CM and DM equivalent circuit of the boost PFC converter. According to Figure 4, the filter capacitors C_{X1} and C_{X2} are parallel. Make $C_X = C_{X1} + C_{X2}$. In the CM interference branch, C_X is connected in series with the test resistor R_{LN} on the branch. When the impedance of C_X is smaller than the test resistance R_{LN}, it can be considered that the filter capacitor C_X is short-circuited, and the test resistance of the L and N lines is equivalent to the parallel connection. Therefore, the test resistance on the CM interference equivalent circuit is $R_{LN}/2$, and its CM interference voltage is V_{CM}. The CM interference equivalent circuit is shown in Figure 5a. The transmission gain $|TG_{CM}(f)|$ of the CM voltage is derived as below.

$$|TG_{CM}(f)| = \left|\frac{R_{LN}}{R_{LN} + \frac{2}{j2\pi f C_P}}\right| = \frac{\pi f C_P R_{LN}}{\sqrt{(\pi f C_P R_{LN})^2 + 1}} \tag{3}$$

Due to the parasitic capacitance C_P in the circuit, generally, $\pi f C_P R_{LN} << 1$, and the amplitude of the CM interference voltage is derived as below.

$$V_{CM} = V_{DS} \times |TG_{CM}(f)| = V_{DS} \times \pi f C_P R_{LN} \tag{4}$$

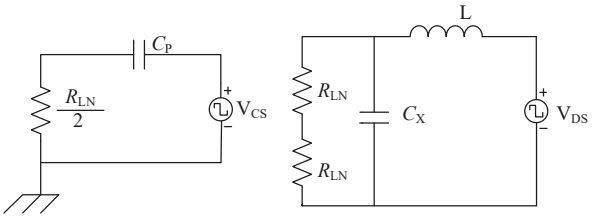


Figure 5. Common-mode and differential-mode equivalent circuits of the boost PFC converter.

Obviously, with the increase of frequency f, the CM interference voltage V_{CM} will increase at a slope of 20 dB/dec. The parasitic capacitance has an obvious influence on CM interference.

Meanwhile, the decrease of voltage V_{DS} will reduce the CM interference.

In the DM interference branch, the DM current flows through the test resistor R_{LN} of the L and N lines in sequence. Therefore, the test resistance on the DM interference equivalent circuit is $2R_{LN}$, and the DM interference voltage is V_{DM}. The DM interference equivalent circuit is shown in Figure 5b. The transmission gain $|TG_{DM}(f)|$ of the CM voltage is derived as below.

$$|TG_{DM}(f)| = \left| \frac{2R_{LN}//(\frac{1}{j2\pi fC_X})}{2R_{LN}//(\frac{1}{j2\pi fC_X}) + j2\pi fL} \right| = \frac{R_{LN}}{2\sqrt{R_{LN}^2(4\pi^2 f^2 LC_{X-1})^2 + 16\pi^2 f^2 L^2}} \quad (5)$$

Usually, when the frequency f is higher than 150 kHz, $4\pi^2 f^2 LC_X >> 1$ and $4\pi^2 f^2 LC_X R_{LN} >> \pi fL$. The amplitude of the DM interference voltage is derived as below.

$$V_{CM} = V_{DS} \times |TG_{DM}(f)| = V_{DS} \frac{1}{8\pi^2 f^2 LC_X} \quad (6)$$

Obviously, with the increase of frequency f, the DM interference voltage V_{DM} will decline at a slope of -40 dB/dec. Meanwhile, it can be seen from the formula that, in the boost PFC converter, increasing the boost inductor can obviously reduce the DM interference, and decreasing the rate of the up or down of switching devices can reduce the DM interference.

From the above analysis, for the DM and CM interferences, the noise source is the switching device. The DM interference will be converted into CM interference. The parasitic parameters of the boost PFC converter have an impact on the DM and CM interferences. However, the influence is different. The boost inductance mainly affects the DM interference, and the parasitic capacitance between the switching device and the radiator shell mainly affects the CM interference.

4. Model of the CM Inductor and EMI Filter Design

4.1. The High-Frequency Model of CM Inductor

Since the common-mode inductor can achieve a very large inductance value in a very small magnetic core, it is widely used in EMI filters, as it can restrain EMI's common-mode noise interference very well. In the EMI conduction frequency range, the CM inductor will be affected by the leakage inductance and various parasitic parameters when working at high frequencies, such that its characteristics will change nonlinearly with the frequency. In order to improve the design of EMI filters and to accurately select a common-mode inductor, it is necessary to establish a suitable common-mode inductor high-frequency model in the EMI interference frequency range.

The CM model is more complex, and because of the nonlinearity of the magnetic element, the parameters of the common-mode equivalent model vary with the frequency [19–21]. Based on

these reasons, a more complex model was used to characterize the high-frequency modeling of CM inductors. The improved model, shown in Figure 6, was based on the traditional Foster model [22]. The first level mainly consisted of the core characteristics (influence of iron core, layer number, and turn number), the second level determined the position and amplitude of the second resonant peak, and the third level determined the phase frequency characteristics before and after the second resonance peak, in which stray capacitance C_1 is mainly related to the lead length of the common-mode inductor. The n-order Foster model can be expressed by n-harmonic peaks.

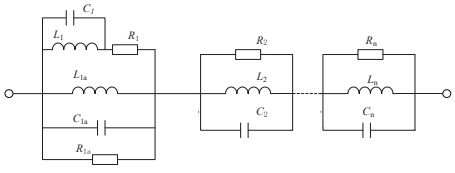


Figure 6. Common-mode inductor high-frequency model.

In order to verify the feasibility of the model, an impedance analyzer was used to test the CM inductance sample, and the scanning frequency range was 150 kHz to 30 MHz. Figure 7 shows the comparison results, fitted using MATLAB.

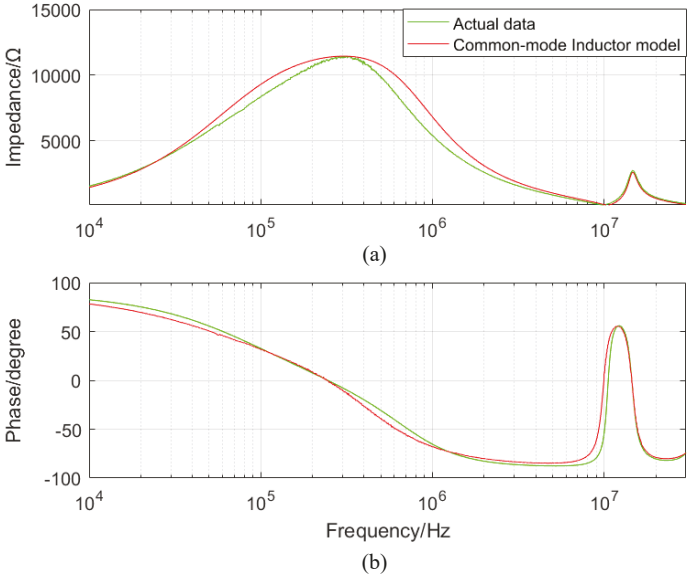


Figure 7. MATLAB fitting comparison.

According to the simulation results in Figure 7, the high-frequency model of the CM inductor (see Figure 6) in this paper had a better fitting effect both in impedance (see Figure 7a) and in phase (see Figure 7b). Thus, the model circuit shown in Figure 6 can reflect the change of the CM impedance in the frequency range of 10 kHz to 30 MHz. This improved model is suitable for all kinds of power converters with EMI filters, for example, PFC boost converters, bridgeless converters, and so on.

4.2. EMI Filter Design

The EMI filter's attenuation of conducted EMI can be expressed as the voltage insertion gain. The voltage insertion gain is defined as the ratio of the interference voltage measured before and after

adding the EMI filter. Similarly, CM and DM equivalent circuits of the EMI filter need to be established, and then the CM and DM attenuation effects of the filter are considered, respectively. The filtering effect of EMI filters is not only related to its own parameters, but is also closely related to interference source impedance. Therefore, in order to design EMI filters efficiently, it is necessary to choose an appropriate filter topology according to different impedance characteristics. In medium and high power of the converters, due to strong common-mode interference, two-stage EMI filters are usually used to suppress interference. In general, the leakage inductance of a CM inductor is used as a DM inductor when designing an EMI filter. Figure 8 shows the two-stage EMI filter topology. In Figure 8, C_{Y1} and C_{Y2} are CM capacitors and their values are equal, C_{X1}–C_{X3} are DM capacitors, and L_{CM1} and L_{CM2} are CM inductors.

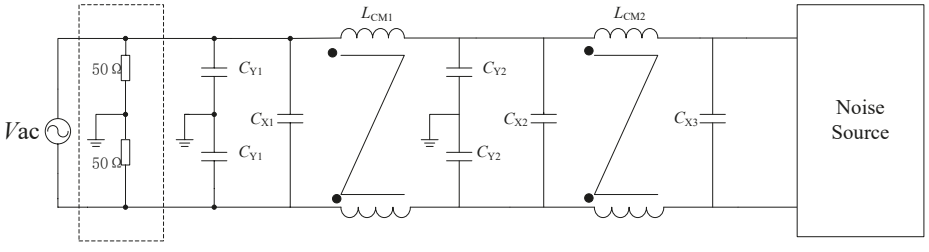


Figure 8. The EMI filter topology.

The attenuation of an EMI filter can be represented by the voltage insertion gain. The common-mode equivalent circuits are shown in Figure 9. The differential-mode equivalent circuits are shown in Figure 10.

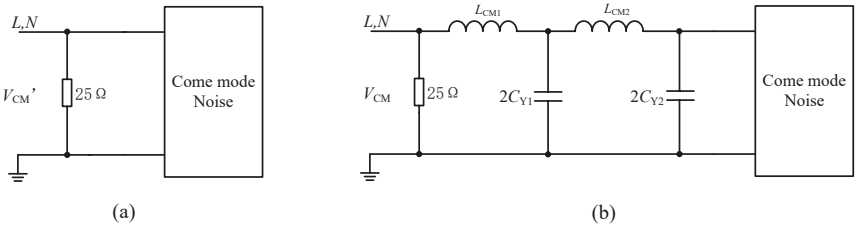


Figure 9. Common-mode equivalent circuits.

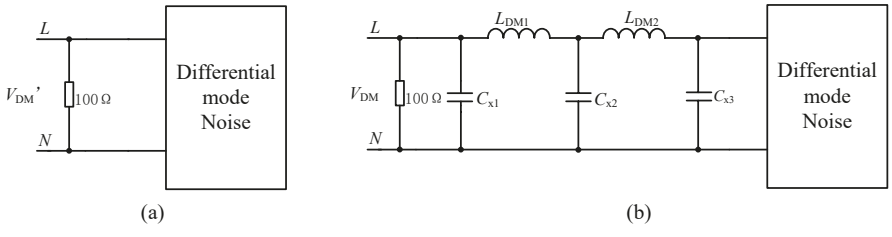


Figure 10. Differential-mode equivalent circuits.

The attenuation can be exemplified by the common-mode equivalent circuit. The CM interference voltage is V'_{CM} when the filter is not added, and the CM interference voltage is V_{CM} when the filter is added. Therefore, the CM insertion gain is derived as below.

$$\begin{aligned} G_{CM}(s) &= \frac{V'_{CM}}{V_{CM}} \\ &= L_{CM1}L_{CM2}2C_{Y1}2C_{Y2}s^4 + L_{CM2}2C_{Y1}2C_{Y2}R_{CM}s^3 \\ &+[L_{CM2}2C_{Y1} + 2L_{CM1}(C_{Y1} + C_{Y2})]s^2 \\ &+2R_{CM}(C_{Y1} + C_{Y2})s + 1. \end{aligned} \tag{7}$$

Figure 11 shows a simplified common-mode equivalent model. According to Equations (8)–(11), the insertion loss of the common mode can be calculated.

$$Z_{CM1} = R + Z_{L1}; \tag{8}$$

$$Z_{CM2} = Z_{L2} + Z_{Y1} \times \frac{Z_{CM1}}{Z_{Y1} + Z_{CM1}}; \tag{9}$$

$$G_{CM} = (Z_{Y2} + Z_{CM2}) \times \frac{Z_{Y1} + Z_{CM1}}{Z_{Y1} + Z_{Y2}}; \tag{10}$$

$$I_L = 20log_{10}\sqrt{(Re|G_{CM}|)^2 + (Im|G_{CM}|)^2}\,. \tag{11}$$

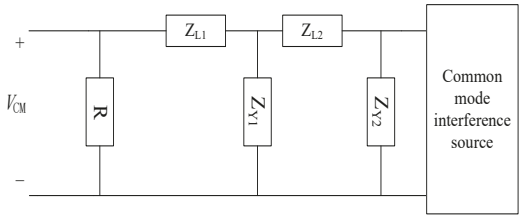


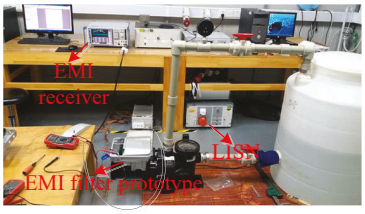
Figure 11. Common-mode equivalent circuit simplified diagram.

According to the previous analysis of the boost PFC circuit and the high-frequency modeling of the common-mode inductor, the high-frequency attenuation performance of the EMI filter can be evaluated more accurately. Meanwhile, it will better suppress the interference of the boost PFC circuit, which helps the reliability of power converters.

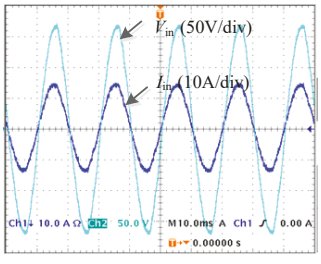
5. Experimental Results

Based on the above analysis, the EMI filter was designed, and the boost PFC converter was optimized. The experimental platform of a 2.4-kW boost PFC motor was built, and the experimental prototype is shown in Figure 12a. Figure 12b is the experimental EMI test platform. Figure 12c shows the input voltage and input current waveforms of the boost PFC converter system. Figure 12d shows the output voltage waveforms. Figure 13 shows the EMI conduction test results of the experimental prototype. Clearly, as shown in Figure 13, the 2.4-kW boost PFC test platform could successfully pass the EMI test. The power factor (PF) of the prototype was very high, and the system could run stably for a long time, thus ensuring the security, reliability, and stability of the system.

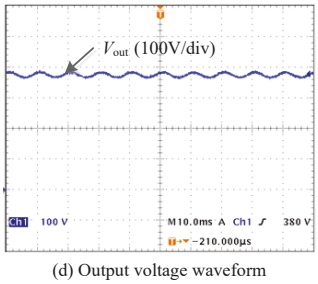
(a) Experimental prototype



(b) Experimental test platform



(c) Input voltage and current waveform



(d) Output voltage waveform

Figure 12. Experimental results.

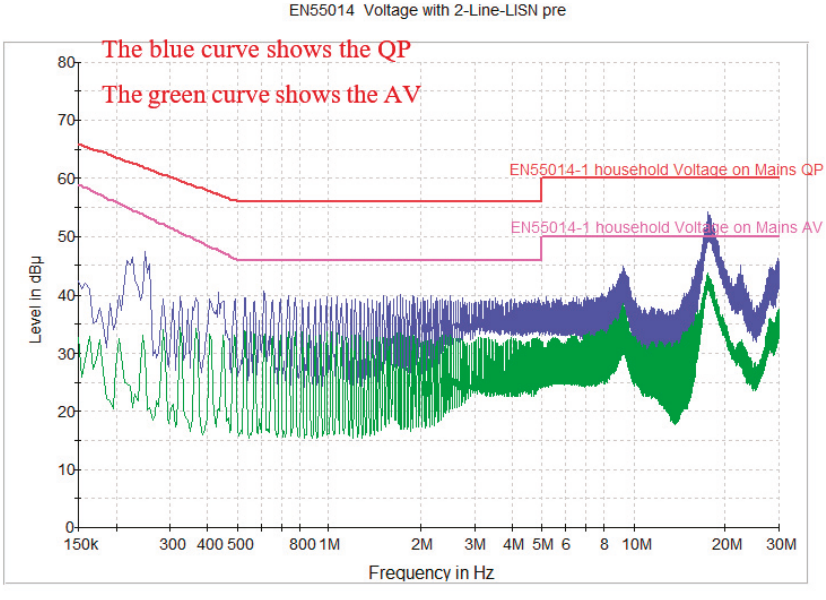


Figure 13. EMI conduction test results.

6. Conclusions

A boost PFC converter can be used to analyze and suppress the EMI issue of power converters. Here, CM and DM interferences of the boost PFC converter were analyzed and discussed in detail. To alleviate the EMI challenges in the reliability of the entire converter system, a common-mode inductor was designed accordingly and modeled. Using MATLAB simulations, it was found that the improved model, based on the traditional Foster model, could better represent the impedance/

frequency characteristics of the common-mode inductor. In addition, the design of the EMI filter could better suppress the CM and DM interferences of the boost PFC converter. EMI-conducted interference could be suppressed using this method. Thus, the reliability of the boost PFC converter was improved. Finally, both simulation results and experimental tests validated the analysis and results.

Author Contributions: H.Z. and D.L. conceived the main idea, performed the testing and data analysis, and wrote the manuscript. X.Z. and F.Q. gave suggestions and contributed with data processing.

Funding: This research was funded by the National Natural Science Foundation of China (NSFC) under the grant number of 51877059.

Acknowledgments: The authors are particularly grateful to the team of Guozhu Chen of Zhejiang University for their help.

Conflicts of Interest: The authors declare no conflicts of interest.

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Active EMI Reduction Using Chaotic Modulation in a Buck Converter with Relaxed Output LC Filter

Van Ha Nguyen [1], Hai Au Huynh [2], SoYoung Kim [2,*] and Hanjung Song [1,*]

[1] Department of Nanoscience and Engineering, Nano Circuit Design Laboratory, Inje University, Gimhae, Gyeongsangnam-do 05834, Korea; nguyenha@oasis.inje.ac.kr

[2] Department of Electronic, Electrical and Computer Engineering, College of Information and Communication Engineering, Sungkyunkwan University, Suwon, Gyeonggi-do 16410, Korea; huynhhaiau292@gmail.com

* Correspondence: ksyoung@skku.edu (S.K.); hjsong@inje.ac.kr (H.S.); Tel.: +82-31-299-4934 (S.K.); +82-55-320-3873 (H.S.)

Received: 10 September 2018; Accepted: 16 October 2018; Published: 16 October 2018

Abstract: DC-DC buck converters are widely used in portable applications because of their high power efficiency. However, their inherent fast switching releases electromagnetic emissions, making them prominent sources of electromagnetic interference (EMI). This paper proposes a voltage-controlled buck converter that reduces EMI by using a chaotic pulse-width modulation (PWM) technique based on a chaotic triangular ramp generator. The chaotic triangular ramp generator is constructed from a simple on-chip chaotic circuit linked with a symmetrically triangular ramp circuit. The proposed converter can thus operate in the chaotic mode reducing the EMI without requiring any EMI filters. Additionally, using the triangular ramp signal can relax the requirement for a large LC output filter in chaotic mode. The effectiveness of the proposed scheme was experimentally verified with a chaotic triangular ramp generator embedded in a voltage-mode controller buck converter using a 0.18 μm Complementary Metal Oxide Semiconductor (CMOS) process. The measurement results from a prototype showed that the EMI improvement from the proposed scheme is approximately 14.53 dB at the fundamental switching frequency with respect to the standard fixed-frequency PWM reference case.

Keywords: electromagnetic interference; chaotic PWM; DC-DC buck converter; CMOS chaotic circuit; triangular ramp generator; spread-spectrum technique; system in package

1. Introduction

The size of portable/wearable electronic devices is being decreased by integrating circuits, such as analog circuits, high-speed digital circuits, high-speed memories, RF circuits, and antennas, into a single system-on-chip (SoC) or system-in-package (SiP) [1]. It is desirable that these devices be small and light-weight, and have a long battery life. Because of their high power conversion efficiency, switched-mode DC-DC converters are widely used in portable electronic devices [2]. However, the high periodical switching frequency of DC-DC converters produces switching noise, which leads to spectrum noise tones at the fundamental switching frequency and its harmonics, causing serious EMI problems. Those problems are particularly serious in SoC/SiP applications that include sensitive blocks, especially RF or sensor circuits [3,4].

Several a posteriori solutions have been proposed to reduce the EMI of DC-DC converters. The work in [5] found that the printed circuit board (PCB) layout has a great effect on the EMI problem and proposed a method of PCB layout optimization to reduce EMI. The research in [6] presented a method to reduce ringing EMI noise by using a passive loss-less snubber cell. An EMI filter is also a common approach to solving the EMI problem [7]. Those schemes, however, need extra

components [5,6], which increases the manufacturing cost and PCB area and make them unsuitable for compact SoC/SiP applications.

The source of EMI in a DC-DC converter is its switching activity; therefore, reducing the EMI should address the switching activity. Such a solution would both eliminate the need for extra passive off-chip components and produce a better low-frequency EMI performance than previous solutions [8]. In the literature, spread-spectrum techniques have been widely applied to the controller of the DC-DC converter to reduce EMI at the design stage. This a priori approach concentrates on preventing EMI directly at the switching signal. In the spread-spectrum technique, the shape of the power spectrum is altered to reduce the harmonic peaks. The first spread-spectrum technique for EMI reduction used carrier frequency modulation (CFM) [9,10]. The approach presented in [9] obtains a flattened power spectrum by using sinusoidal modulation where the driving signal is a sinusoid. The implementation of this approach is simple, but the EMI reduction performance is not optimized, because it creates a U-shaped power spectrum that peaks at two endpoints. The work in [10] used a cubic waveform as the driver signal to mitigate the peaks at the two end-points of the U-shaped power spectrum while maintaining the sinusoid-based modulation, but that technique significantly increased the complexity of the circuit. Either a triangular waveform or a sawtooth waveform was later adopted to replace cubic waveform because that circuit is easier to implement, and the triangular waveform offered an EMI performance similar to that with the cubic waveform-based modulation [11–13]. Therefore, the most common method currently used to implement the CFM spread-spectrum technique is triangular-based frequency modulation [13]. The limitation of the CFM method is the periodic characteristic of the driver signal, which creates a discrete modulated power spectrum. Therefore, chaos-based random pulse-amplitude modulation was proposed by several researcher [14,15]. Assuming that a uniform random distribution could be obtained using a chaos generator, the resulting EMI spectrum would be continuous. Several methods have been proposed to approximate a random source [14,15]. The approach presented in [14] proposed a self-tuning offset and amplitude-adaptive ramp control for the buck and boost converters. That solution achieved a significant EMI improvement in both the buck and boost converters, but it is costly and applicable only at PCB level. The offset and amplitude tuning method improves the EMI, but it causes stability problems for the DC-DC converter.

Recently, the spread-spectrum technique has expanded to new effective schemes that use randomized/chaotic pulse-width modulation (RPWM/CPWM) [16–18]. This spectral modification scheme is realized by operating the converter in aperiodic mode. An analog chaotic generator (Chua's oscillator) was used in [16] to form CPWM for the converter. That method achieved a good performance on EMI reduction and was simple and flexible in its design. Unfortunately, Chua's oscillator circuit requires many off-the-shelf passive inductors and capacitors (in μH and μF ranges), which makes it unsuitable for compact applications. The work reported in [17] presented an on-chip CMOS-based CPWM generator for a DC-DC converter. The digital chaotic sequence generator replaced the constant switching frequency generator in the DC-DC converter. However, that CPWM scheme was only modulated by chaotically hopping among a set of 4 fixed frequency levels, which generated an upper limit for its reduction of EMI. Another approach, based on the spread-spectrum concept called frequency hopping [18], used the RPWM technique. It randomly distributes the switching frequency among a set of 8-fixed frequencies; thus, it reduces the spectrum only around the pre-defined frequency sets. Additionally, that method requires a uniform distribution random circuit, which is costly and difficult to implement. In general, existing RPWM/CPWM schemes have undesirably high output-voltage and inductor-current ripples, which have gone unconsidered in most previous studies.

Motivated by all those concerns, we here propose a dual-mode PWM/pulse-frequency modulation (PFM) voltage-controlled buck converter with EMI reduction under chaotic mode operation. The proposed solution achieves a significant EMI reduction and mitigates the aforementioned shortcomings of previous works. First, we propose a simple and fully on-chip CMOS chaos generator associated with a strict N-shaped chaos map to generate controllable chaotic signals. A strictly mathematical model for the proposed chaos map circuit is derived via the stroboscopic sampling method, and its chaotic behaviors are deeply analyzed via the Lyapunov exponent theory and a bifurcation diagram. Second, we design a symmetrical triangular ramp generator to work with the chaos-generator to form a chaotic ramp generator for EMI reduction. Finally, we design, fabricate, and test a prototype implementation of the dual-mode PWM/PFM buck converter with the chaotic triangular ramp generator using a 0.18 μm CMOS process. The result measured from the prototype shows an EMI improvement of approximately 14.53 dB with respect to the standard PWM reference case, while maintaining a reasonable output ripple magnitude. This proposed scheme can be applied to any voltage mode-controlled converter and has a feature that enables the user to tune a single converter to various electromagnetic compatibility norms.

The rest of this paper is organized as follows: in Section 2, the concept for the EMI-improved SiP buck converter and the requirements that affect the selection of the ramp generator for EMI reduction are presented. The section then deals with the implementation of the proposed chaotic circuit and the chaotic ramp generator. The simulation results are presented and discussed in Section 3, and the experimental results and EMI comparison with other state-of-the-art schemes are presented in Section 4. Finally, Section 5 concludes this research work.

2. Proposed Chaos-Based EMI Reduction with On-Chip Chaotic Ramp Generator

2.1. SiP Dual-Mode PWM/PFM Buck Converter with Chaos-Based EMI Reduction Scheme

Buck converters are indispensable in most battery-powered devices due to their simple power conversion step and high power efficiency. To maintain high power efficiency over a wide range of load currents, dual-mode PWM/PFM buck converters are widely used [19,20]. Figure 1 shows a simplified schematic diagram of our EMI-improved buck converter, along with the concept for a SiP buck converter powered by a battery represented by a voltage source (VBAT). The buck converter is controlled by a PWM/PFM controller to turn ON/OFF the high-side and low-side switches (HSW/LSW) with non-overlapping pulses CPWMP/CPWMN. To eliminate the conduction loss when the converter enters low load conditions, a comparator is utilized to output a zero-current detection (ZCD) signal to turn off the LSW by comparing the switching node voltage (VSW) and the ground. The bandgap reference (BGR) circuit outputs a reference level of 1.2 V to regulate the output voltage of the converter. Also, in the block diagram, (EA) represents the error amplifier, and equivalent series resistance (ESR) and direct current resistance (DCR) represent the parasitic resistances inside the inductor and capacitor of the LC filter, respectively. This work presents a DC-DC buck converter that features an automatic mode change between PWM and PFM depending on the load current level. The corresponding output to load is in the range from 50 mA to 500 mA. When the load current is higher than 200 mA, the converter operates in PWM mode. When the load current is lower than 200 mA, the converter automatically switches into PFM mode, in which the power stage operates intermittently, based on the load demand. In PFM mode, the switching activity is reduced to minimize the switching loss and maintain the high power efficiency of the converter.

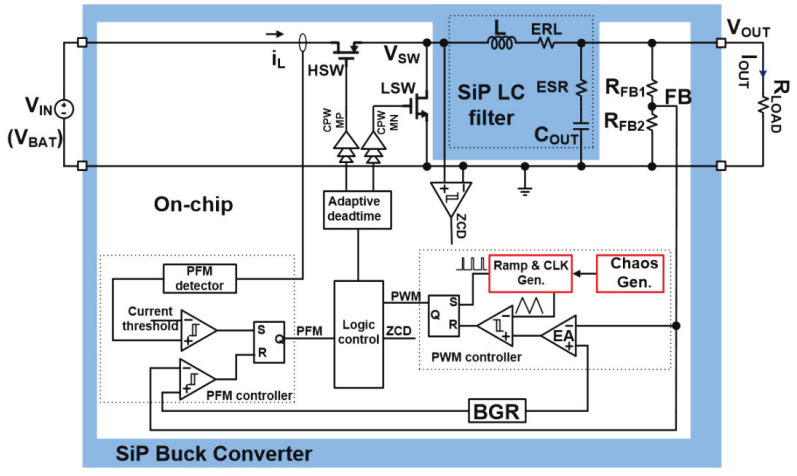


Figure 1. System-in-package (SiP) buck converter with chaos-based electromagnetic interference (EMI) reduction. The highlighted chaotic ramp and clock generator forces the converter to operate in chaotic mode for EMI reduction.

Figure 2 shows the proposed scheme for generating a chaotic PWM signal for EMI reduction in a type-III compensation network. Type-III compensation is normally used for its optimized loop bandwidth and fast transient response in a voltage-mode-controlled converter that operates in continuous conduction mode (CCM) mode, as compared to type-I and type-II counterparts [21]. In this scheme, a fully on-chip N-shaped chaos generator circuit is proposed. Additionally, a new design for a symmetrically triangular ramp generator is implemented. The chaotic output of the N-shaped chaos generator (V_{Chaos}) is applied to control the triangular ramp generator (to V_H or V_{BR}) and generate a chaotic triangular signal (V_{CTR}). The V_{CTR} signal is then compared with the slow-varying signal at the output (V_{EA}) of the error amplifier to generate the CPWM to control the high side switch (HSW) and low side switch (LSW) power switches. In chaotic operation mode, the switching period, T_{SW}, varies chaotically, and the duty cycle also changes from cycle to cycle. However, the average duty cycle is constant, which means the output voltage follows the pre-determined value as expected. The inductor current and output voltage are also chaotic, so their associated spectra can spread over a certain frequency range. In this way, the EMI is significantly reduced using the characteristics of the broadband frequency spectrum in the chaotic signal. Most importantly, the scheme proposed here modulates the switching frequency (F_{SW}) continuously in a defined range. This is equivalent to hopping among an infinite set of switching frequencies, which results in the full elimination of the peaks in the power spectrum present in the standard fixed-frequency PWM mode. Therefore, EMI reduction can be higher than that offered by previous solutions [17,18].

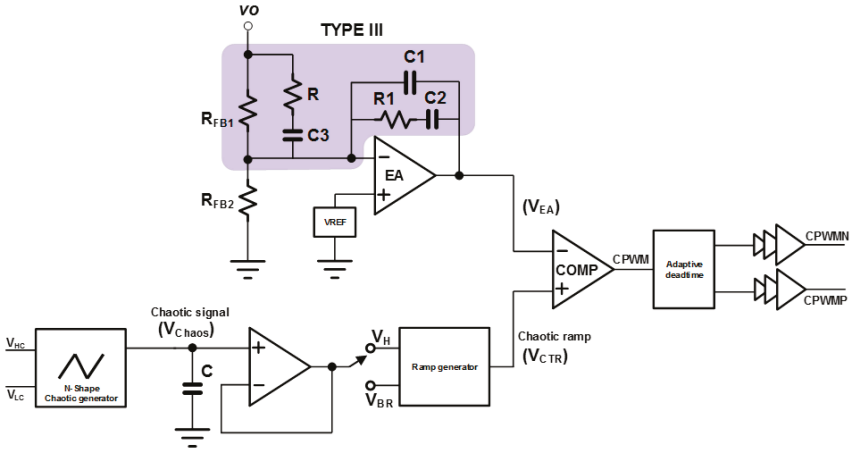


Figure 2. Proposed scheme for synthesizing a chaotic pulse-width modulation (PWM) signal with an N-shaped chaotic generator for a buck converter using a type-III compensator network.

As described in the previous sections, EMI reduction via the spread-spectrum technique is always achieved at the cost of a performance reduction in the buck converter, including: (1) an increase in the output voltage ripple; (2) a increase in inductor current ripple; and (3) a reduction in power efficiency. However, those negative side-effects have often been neglected in the literature [16–18]. All of those factors require an increase in the size of passive LC output filter [8,22]. However, in the design of SiP buck converters, a large LC is not recommended, because the space inside the package is limited. This work mitigates those negative side-effects of the spread-spectrum technique by using a ramp generator to generate a triangular signal instead of a sawtooth. The triangular signal mitigates the ripple of the inductor current, thereby relaxing the requirement for large LC output filter. The overall specifications of our DC-DC converter are listed in Table 1. The details of the implementation of the proposed scheme are explained and discussed in Sections 2.2 and 2.3 below.

Table 1. Designed buck converter specifications.

Parameter	Description	Quantity
V_{IN}	Input voltage range (Battery)	2.7–4.2 V
V_{OUT}	Output voltage range	1.0–1.8 V
$I_{OUT,max}$	Maximum load current	500 mA
$V_{rip,(max)}$	Maximum output ripple	50 mV
F_{SW}	Switching frequency	1–2 MHz
L_{OUT}	Inductor (in package)	2.2 µH
C_{OUT}	Output capacitor (in package)	2.2 µF

2.2. Fully Integrated On-Chip Chaos Generator with N-Shaped Map

Chaotic sources have previously been proposed as a cheap replacement for a random signal in the spread-spectrum technique [23]. The chaotic signal plays a key role in the distribution of harmonics when a converter operates in the chaotic mode. So far, several CMOS chaos generators have been reported [23–25]. Those circuits, however, are not completely straightforward to design due to their lack of governing models [23], non-robust chaos with regard to variable circuit parameters [24], bulk, low frequency, and high power requirements [25].

In this section, a new, fully integrated on-chip, CMOS chaos generator is presented with its associated mathematical chaos map. The chaos map model can be strictly derived from the circuit operation, thus making the analysis and design simple and accurate. Because the chaos exists in a wide continuous range, the chaos robustness with respect to the unavoidable error introduced by physical variations in circuit devices can be significantly relaxed. Also, the compact design and low power consumption of the proposed chaos generator make it a good pseudo-random source. To achieve EMI reduction in the DC-DC buck converter, the output of the N-shaped chaos generator is injected into a triangular ramp generator to construct a chaotic ramp generator as explained in detail in Section 2.3.

2.2.1. N-Shaped Chaos Generator

For the simplicity of the analysis, the proposed N-shaped chaos generator (CG) is simplified and shown in Figure 3. The circuit consists of one capacitor C that is either charged or discharged through two current sources/sinks (I_1 and I_2), respectively; the remaining part contains a controller with two comparators, two SR latches, one AND gate, one XOR gate, and one SPDT (single pole double through) switch. In the proposed chaos generator, the only state variable is the capacitor voltage $v(t)$.

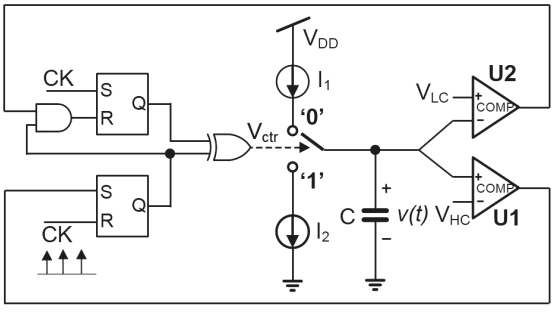


Figure 3. Simplified block diagram of the proposed N-shaped chaos generator.

The operation of the chaos generator can be represented by a finite state machine (FSM), as shown in Figure 4a. The state machines S1 and S3 correspond to the charging of capacitor C at every rising edge of the clock (CK) or when $v(t)$ reaches the upper limit V_{HC}; the state S2 corresponds to its discharging when $v(t)$ reaches the low limit (V_{LC}). The dynamics of the proposed chaotic circuit can be represented by a 1-D piece-wise map, a so-called stroboscopic map. Assuming that at t_H, the capacitor voltage reaches V_H, which triggers the control signal V_{ctrl} to be HIGH (Q = 1), capacitor C is discharged through I_2 as follows:

$$v(t) = V_{HC} - \frac{I_2}{C}(t - t_H) \tag{1}$$

Also, at the beginning of the next period (t_k), V_{ctr} is triggered to be LOW (Q = 0) by the clock signal, and capacitor C is charged by I_1:

$$v(t) = V_k + \frac{I_1}{C}(t - t_k) \tag{2}$$

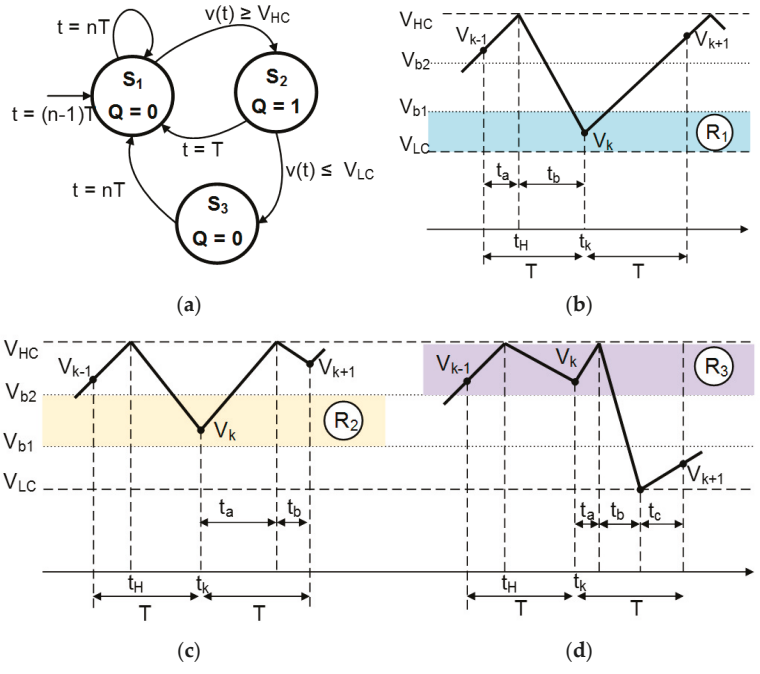


Figure 4. Operation of the N-shaped-based chaos generator: (**a**) Finite state machine. (**b**–**d**) Capacitor voltage waveform.

The 3 possibilities that the FSM can evolve depend on the value of state variable $v(t)$ at t_k. First, the state space is separated into 2 sub-spaces (R_1 and $R_2 + R_3$), depending on boundary condition V_{b1}, which is defined as the voltage level at which the capacitor voltage is charged from V_{LC} to V_{b1} within one clock cycle T. V_{b1} is calculated from discharging Equation (2) as follows:

$$V_{HC} = V_{b1} + \frac{I_1}{C}T \rightarrow V_{b1} = V_{HC} - \frac{I_1}{C}T \; (V_{b1} < V_{HC}) \tag{3}$$

- Sub space R1: At t_k, if $V_k < V_{b1}$, the capacitor will continue charging on the next clock cycle as shown in Figure 4b, corresponding to FSM S_1. However, if $V_k > V_{b1}$, the subspace higher than V_{b1} can be divided into 2 other sub spaces, R_2 and R_3, depending on a second boundary condition, V_{b2}.
- Sub space R2: The capacitor continues charging until $v(t)$ reaches V_{HC} and then discharge for the time durations t_a and t_b, respectively. Figure 4c shows the representative waveform for this case with the charging period t_a and discharging period t_b, which can be deduced from Equations (1) and (2): $t_a = I_1/C \times (V_{HC} - V_k)$; $t_b = T - t_a = T - I_1/C \times (V_{HC} - V_k)$. For this case, $t_a + t_b = T$.
- Sub space R3: The capacitor continues charging until $v(t)$ reaches V_{HC}, then it discharges to V_{LC} for the periods t_a, t_b, and t_c, as shown in Figure 4d. In this case, $t_a + t_b < T$; therefore, t_c can be calculated as $t_c = T - t_a - t_b = T - I_1/C \times (V_{HC} - V_k) - C/I_2 (V_{HC} - V_{LC})$. In this case, t_b is different from before and can be calculated using the discharging equation $V_{LC} = V_{HC} - I_2/C \times t_b$. The second boundary condition can be derived by the setup $t_c = 0$:

$$\begin{aligned} &t_c \geq 0 \rightarrow T - t_a - t_b = T - \tfrac{I_1}{C}(V_{HC} - V_k) - \tfrac{C}{I_2}(V_{HC} - V_{LC}) \geq 0 \\ &\rightarrow V_{b2} = V_{HC} - \tfrac{I_1}{C}T + \tfrac{I_1}{I_2}(V_{HC} - V_{LC}) \end{aligned} \tag{4}$$

Now, the N-shaped map of the chaos generator that relates the value of state variable $v(t)$ at every clock instant can be written as follows:

$$V_{k+1} = \begin{cases} V_k + \frac{I_1}{C}T, \text{ with } V_{LC} < V_k \leq V_b \\ V_{HC} - \frac{I_2}{C}T + \frac{I_1}{C}(V_{HC} - V_k), \text{ with } V_{b1} < V_k \leq V_{b2} \\ V_k + T\frac{I_1}{C} - (V_{HC} - V_{LC})(1 + \frac{I_1}{I_2}), \text{ with } V_{b2} < V_k < V_{HC} \end{cases} \quad (5)$$

Furthermore, that N-shaped map can also be normalized and parametrized:

$$x_k = \frac{V_k}{V_{HC}};\ T_1 = T\frac{I_1}{V_{HC} \times C};\ T_2 = T\frac{I_2}{V_{HC} \times C}; x_{b1} = \frac{V_{b1}}{V_{HC}}; x_{b1} = \frac{V_{b2}}{V_{HC}}; \quad (6)$$

Thus, the normalized chaos map of the proposed chaos generator can be presented as:

$$x_{k+1} = f(T_1, T_2; x_k) = \begin{cases} x_k + T_1 \text{ with } 0 < x_k < x_{b1}; \\ 1 - T_2 + \frac{T_2}{T_1}(1 - x_k) \text{ with } x_{b1} < x_k < x_{b2}; \\ x_k + T_1 - \left(1 - \frac{V_{LC}}{V_{HC}}\right)\left(1 + \frac{T_2}{T_1}\right); \text{ with } x_{b2} < x_k < 1; \end{cases} \quad (7)$$

2.2.2. Dynamical Analysis of the Chaos Map

Before implementing the chaos generator at the circuit level, the proposed mathematical model for the chaos generator is realized to find the range of system parameters at which the circuit outputs chaotic signal. The dynamic behavior of a chaotic system can be qualitatively studied through Lyapunov exponents. The Lyapunov exponent of the N-shaped map is theoretically calculated as follows [26]:

$$\lambda = \lim_{n\to\infty} \frac{1}{n} \sum_{j=1}^{n} \ln\left|f'(x_j)\right| \quad (8)$$

where $f'(.)$ is the derivative of the chaotic map $f(.)$ and can be derived as:

$$f'(x) = \begin{cases} 1 \text{ with } 0 < x_k < x_{b1}; \\ -\frac{T_2}{T_1} \text{ with } x_{b1} < x_k < x_{b2}; \\ 1; \text{ with with } x_{b2} < x_k < 1; \end{cases} \quad (9)$$

Hence, the Lyapunov exponent is calculated as follows:

$$\lambda = \lim_{n\to\infty} \frac{1}{n}\left(i \times \ln 1 + j \times \ln\left|-\frac{T_2}{T_1}\right| + k \times \ln 1\right) = \lim_{n\to\infty} \frac{j}{n}\left(\ln\left|\frac{T_2}{T_1}\right|\right),\ i + j + k = n \quad (10)$$

where n is the number of x points use in the calculation, i, j, k are the number of times that x belongs to three ranges $[0, x_{b1}]$, $[x_{b1}, x_{b2}]$, and $[x_{b2}, 1]$, respectively.

According to Equation (7), when $T_2/T_1 > 1$ and $\lambda > 0$, the map produces periodic doubling bifurcation; in other words, a chaotic signal is generated [26]. Otherwise, if $T_2/T_1 < 1$ and $\lambda < 0$, the system output has a periodic state or converges to a stable point. The chaotic dynamics can also be observed via the bifurcation diagram. For example, when $T_1 = 0.5$ and T_2 is gradually increased from zero, the bifurcation diagram appears as shown in Figure 5, from which the dynamic behaviors of the point, periodicity, and chaos (dense area) can be observed. The bifurcation diagram also highlights the robustness of the chaos generation from the map versus the system parameter (T_2); there is no intermittent-periodic window inside the bifurcation diagram, unlike in previously reported work [16]. The circuit parameters for designing the N-shaped chaos generator in the next section can be selected easily based on the bifurcation diagram shown in Figure 5. The dynamics behaviors of the chaotic map can be further examined in another reported work [27].

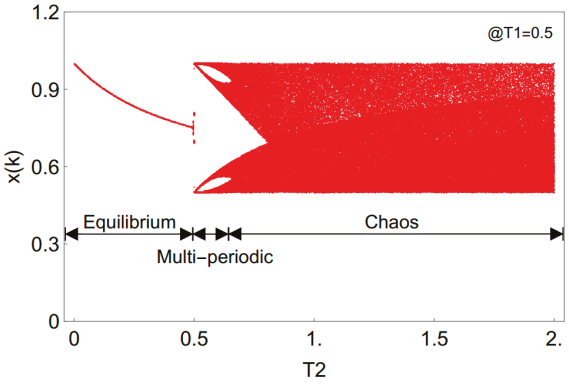
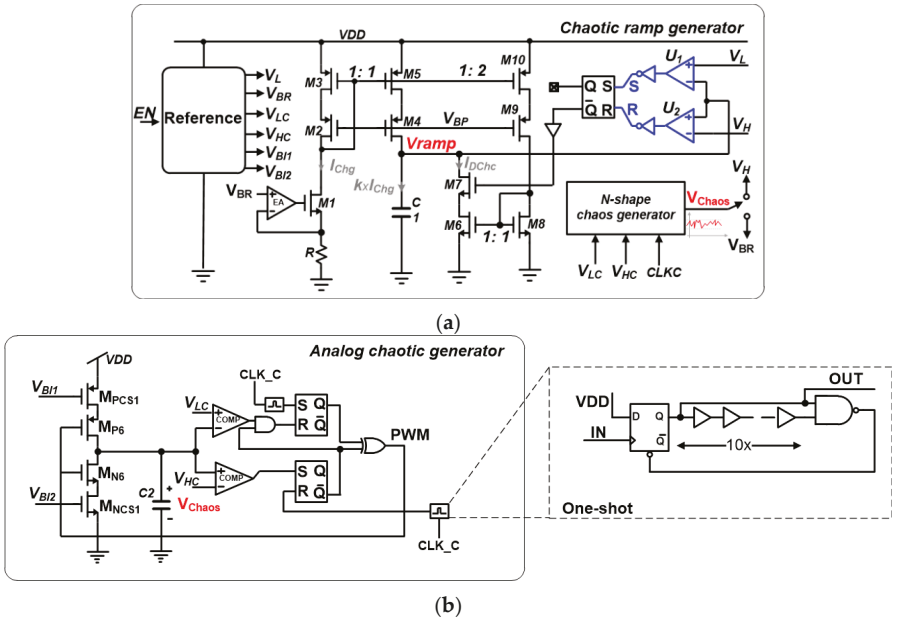


Figure 5. Bifurcation diagram versus T_2 of the mathematical model of the proposed N-shaped chaos generator. The range of T_2 associated with the dense area of the diagram shows chaotic behavior and can be used later to design Complementary Metal Oxide Semiconductor (CMOS) chaotic circuit.

2.3. Design of Chaotic Triangular Ramp Generator

In the voltage mode of a DC-DC buck converter, a ramp signal is needed to modulate the PWM signal. Basically, there are two different possible forms for the ramp signal, a sawtooth ramp signal and a triangular ramp signal. The studies in [4] demonstrated that a symmetrically triangular ramp signal with equal rising and falling slopes can effectively mitigate the inductor current imbalance effect; therefore, it can also mitigate the aforementioned side-effects of the spread-spectrum technique without influencing the inductor current spectrum (and therefore the EMI performance). We therefore propose a PWM ramp generator that generates a triangular signal to reduce EMI and minimize the side-effects caused by the inductor current imbalance in the chaotic operation mode.

The detailed implementation of the proposed chaotic triangular ramp generator is shown in Figure 6a. The proposed chaotic triangular ramp generator consists of a triangular ramp generator linked with the proposed N-shaped chaotic circuit. Unlike a sawtooth ramp generator, in which the discharging time is much smaller than the charging time, the time for charging and discharging should be equal in a triangular ramp generator. Therefore, a current source/sink is used to control the charging/discharging speed to optimize the accuracy. This requirement preserves the memoryless property of the steady state inductor current, especially, when the switching frequency changes from cycle-to-cycle in chaotic operation mode. In the proposed triangular ramp generator shown in Figure 6a, the V-I converter (constructed from a error amplifier (EA), resistor (R), transistor (M1) and a wide-swing current source using cascade current mirror (M2–M5)) controls a charging current $I_{Chg} = V_{BR}/R$. This current is copied by the current mirrors M6 and M8M10 to form a current sink that controls the discharging current I_{DChg}. As mentioned before, the charging and discharging time for timing capacitor C_1 must be equal, so $I_{DChr} = 2I_{Chg}$. This is implemented by setting a current ratio between current mirrors M4–M5 and M9–M10 as 2:1. The operation of the proposed triangular ramp generator can be briefly described as follows: Assume that at the beginning, after an initial reset event (with the triangular signal at low threshold limit (V_L)), the switch M7 is OFF and capacitor C1 is slowly charged with charge-current I_{Chg} until the capacitor voltage (ramp) reaches the upper limit (V_H). At that point, the comparator trips, and the switch M7 switch is turned ON, which discharges the ramp to V_L by the current sink M6 with $I_{DChg} = 2I_{Chg}$. When the triangular signal ramps down to V_L, another cycle begins [28]. To reduce the asymmetry of the triangular ramp signal caused by current mismatches in the current mirrors, the length of the transistors in the current mirror should be large.



(**a**)

(**b**)

Figure 6. Proposed design of chaotic triangular ramp generator: (**a**) Chaotic ramp generator; (**b**) N-shaped chaos generator.

Figure 6b shows the implementation of the proposed N-shaped chaos generator. In this circuit, the inverter MN6–MP6 plays the role of the SPDT switch, whereas the transistors MPCS1 and MNCS1 act as the current source I_1 and current sink I_2, respectively. The one-shot circuit is used to generate short pulses for the SR latches because the clock signal (CLK) ideally consists of an impulse train at the rate f = 1/T. Practically, these impulses are approximated by narrow pulses and implemented using the one-shot circuit. The N-shaped chaotic circuit parameter was designed based on the selection of the mathematical model's parameters T_1 and T_2. For this work, T_2 is selected inside the chaos region (as shown in Figure 5) for robust chaos generation against the variation inherent in process fabrication as mentioned in [27]. With the proposed N-shaped chaos generator, the output is chaotic, as long as $T_2/T_1 > 1$. This condition can be easily met, irrespective of the variation of capacitor C_2 (usually up to 30% of the design value). Because $T_1 = T \times I_1/(V_H C)$, $T_2 = T \times I_2/(V_H C)$; therefore, setting the ratio $T_2/T_1 > 1$ is equivalent to setting the ratio $I_2/I_1 > 1$. This can be easily controlled at the circuit level using a basic current mirror and matching the layout between the current source/sink (M_{PCS1} and M_{NCS1}).

The triangular ramp generator and N-shaped chaotic circuit are connected together to construct the chaotic ramp generator. The switching frequency of the triangular ramp generator proposed in Figure 7 can be expressed as [29]:

$$f_{SW} = \frac{1}{T} = \frac{I_{Chg}}{2C(V_H - V_L)} \tag{11}$$

where V_H and V_L are the high and low bounds of the triangular ramp signal, respectively. Clearly, Equation (7) shows that two parameters can define the switching frequency of the triangular ramp generator: the ramp bounds (V_H and V_L) and the charging current I_{Chg} of the triangular signal. To alter the switching frequency from cycle to cycle, one or both parameters can be modulated using the generated chaotic signal (V_{chaos}) from the N-shaped chaotic generator.

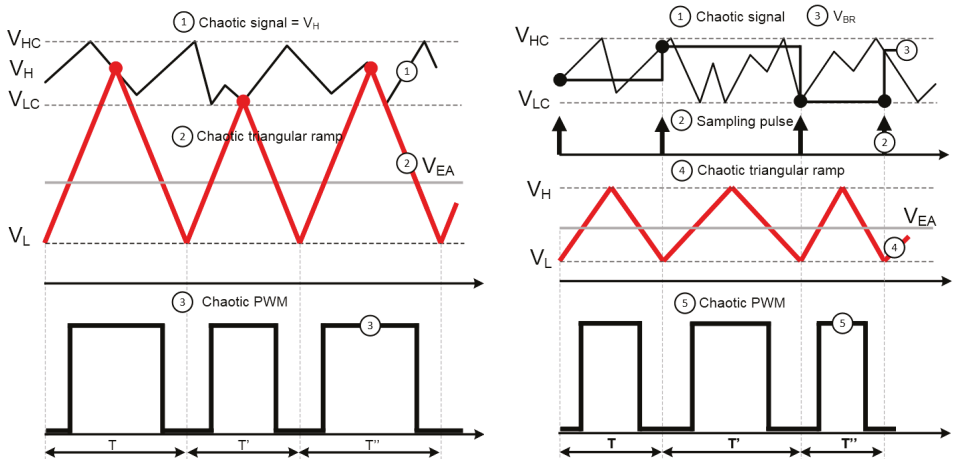


Figure 7. Modulation of chaotic triangular ramp signal: (**a**) peak modulation; (**b**) slope modulation.

For the first scheme (peak modulation), keeping the low bound (V_L) and the charging current (I_{Chg}) unchanged causes the switching frequency of the ramp generator to depend only on the high bound (V_H). The chaotic signal generated from the N-shaped chaos generator can then be fed directly into the V_H of the comparator, making $V_H = V_{chaos}$; therefore, the switching frequency of the ramp generator is chaotically modulated. Figure 7a depicts the timing diagram for that method. For the second method (slope modulation), the chaotic signal generated from the N-shaped chaos generator can be indirectly fed into the V-I converter at V_{BR}, making $V_{BR} = V_{chaos}$. Its timing diagram is shown in Figure 7b. In this scheme, the chaotic signal is converted into chaotic charging/discharging currents; therefore, the ramp signal and switching frequency are also chaotic. The chaotic signal from the N-shaped ramp generator cannot be fed directly into V_{BR} because that continuous chaotic signal also changes the charge/discharging current within one cycle. Therefore, the chaotic signal is sampled only at the end of each cycle by an impulse (S) signal from the low-threshold comparator (U1) inside the ramp generator circuit. This configuration keeps the charging/discharging current (I_{Chg}/I_{DChg}) unchanged until the end of the current cycle and eliminates disturbances on the triangular waveform. The switching frequency deviation (ΔF_{SW}) in the chaotic mode is set near the fixed-frequency mode at 1.2 MHz and the frequency envelope of the chaotic triangular ramp signal is in the range of:

$$(f_{SWL}; f_{SWH}) = \left(\frac{I_{Chg}}{2C(V_{Hmax} - V_L)}; \frac{I_{Chg}}{2C(V_{Hmin} - V)}\right) = \left(\frac{I_{Chg}}{2C(V_{HC} - V_L)}; \frac{I_{Chg}}{2C(V_{LC} - V_L)}\right) \quad (12)$$

for the peak modulation and:

$$(f_{SWL}; f_{SWH}) = \left(\frac{I_{Chg(min)}}{2C(V_H - V_L)}; \frac{I_{Chg(max)}}{2C(V_H - V_L)}\right) = \left(\frac{\frac{V_{LC}}{R}}{2C(V_H - V_L)}; \frac{\frac{V_{HC}}{R}}{2C(V_H - V_L)}\right) \quad (13)$$

for the slope modulation. By using Equations (12) and (13), the circuit parameters of the chaotic ramp generator such as C1, I_{Chg}, VH, VL, VHC, and VLC can be derived for implementation. The derived values of VHC, VLC from Equations (12) and (13) in combination with the normalized and parametrized Equation (6) presented in Section 2.2 can then be used to calculate the circuit parameters for N-shape chaos generators T, I1, I2 and C. It should be noted that the N-shaped chaos generator confines its chaotic signal at the output within a defined band [V_{LC}; V_{HC}] by two comparators. This assures that the frequency deviation of the chaotic ramp signal can be accurately controlled.

This characteristic adds extra controllability to the chaotic ramp generator as the frequency deviation can be customized.

Of the two methods for generating the chaotic triangular ramp signal presented above, the peak level injection offers easier implementation. The slope modulation is more complex because it samples the chaotic signal and thus needs an additional sampling circuit. The slope modulation scheme also requires a high bandwidth V-I converter because the speed for converting the chaotic signal into chaotic current needs to be fast enough for the charging current to switch from one level to another at the beginning of each cycle. In practice, the bandwidth of the V-I converter is set to at least 10 times the switching frequency. In designing the triangular circuit, because the ramp down slope of the triangle is lower than that of the sawtooth ramp generator, the design of the comparator is simple, and the power consumption of the comparator is low. Additionally, because the ramp amplitude directly affects the stability of the buck converter in voltage mode [21], the compensation network of the converter using a triangular ramp generator with peak modulation should be designed carefully. For the slope modulation method, the amplitude of the ramp signal is kept constant, and the stability does not change once the compensation network is fixed.

3. Simulation Results

Before fabricating a chip, we examined the performance of the proposed EMI-improved buck converter through a simulation. The chaotic ramp generator presented in the previous section was applied to the dual-mode PWM/PFM buck converter in Figure 1 to examine the EMI reduction performance. The simulation was conducted for both the standard mode and the chaotic mode for ease of comparison. The nominal switching frequency F_{SW} for the standard mode was set to 1.2 MHz, and the chaotic frequency range was set at +/−10% of the F_{sw} (1.08 MHz to 1.32 MHz) and +/−20% of F_{sw} (0.96 MHz to 1.44 MHz).

In the standard mode, the design parameters of the triangular ramp were set at V_{BR} = 0.6 V, C = 3 pF, V_H = 1.5 V and V_L = 0.8 V to achieve a nominal of F_{SW} = 1.2 MHz. To achieve the frequency deviations of +/−10% and +/−20% around the nominal switching frequency F_{SW}, the bounds of the chaotic signal (V_{Chaos}) applied to the V_{BR} of the ramp were set at V_{HC} = 0.66 V, V_{LC} = 0.514 V, V_{HC} = 0.71 V, and V_{LC} = 0.46 V, in accordance with Equation (9). In the chaotic mode, the mean value of F_{SW} = 1.2 MHz is defined using the mean value of V_{HC} and V_{LC}. Following the condition of T2/T1 > 1 or I2/I1 > 1 to output the chaotic signal, the parameters of the N-shaped chaotic circuit were set at: C = 3 pF, I1 = 1 μA, I2 = 6 μA, and CK = 1 MHz for both cases. The simulation setup for the converter was: V_{IN} = 3 V, V_{OUT} = 1.8 V, I_{OUT} = 250 mA, L = 2.2 μH and C_{OUT} = 2.2 μF. The ESR value of the capacitor (ESR = 30 mΩ) and the other components of the compensation network were selected from commercial elements to give a good predictable result when comparing the simulation with the real test chip measurement results.

Figure 8 shows the simulation results for the converter when operating in the chaotic mode with the chaotic triangular ramp generator using slope modulation. Clearly, the chaotic signal from the N-shaped chaos generator is sampled at the beginning of each switching cycle and then fed into the V-I converter at the V_{BR} of the triangular generator. As a consequence, the converter operates in the chaotic mode. The inset figure of inductor current shows that it varies chaotically; therefore, the EMI performance will be improved. The chaotic operation of the buck converter can also be easily confirmed from the phase portrait of two internal chaotic states (inductor current and output voltage) shown in Figure 9b. Compared to the standard mode shown in Figure 9a, in which the operation is stable between two equilibrium points and can thus be presented by only one trajectory, the chaotic operation shows a complex pattern, including multiple un-repeated trajectories that represent chaos.

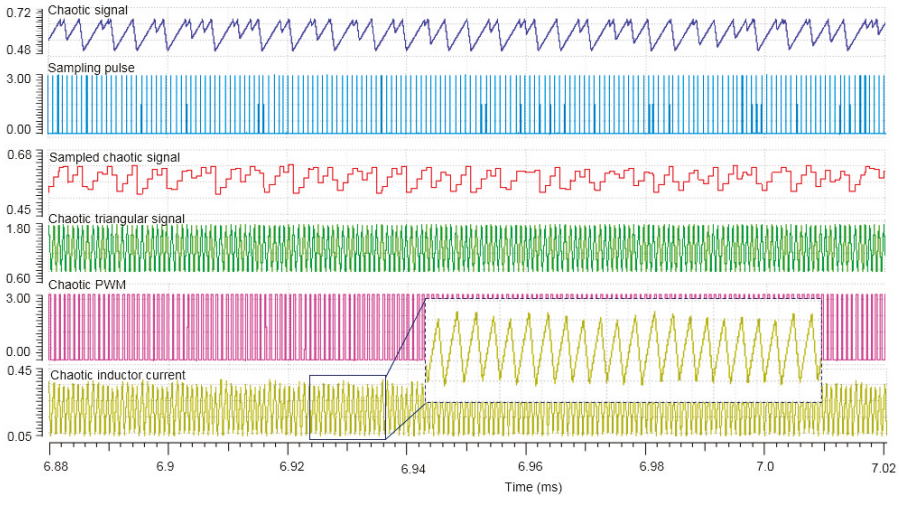


Figure 8. Steady-state time-domain simulation results of the converter in chaotic mode using chaotic triangular ramp generator with slope modulation.

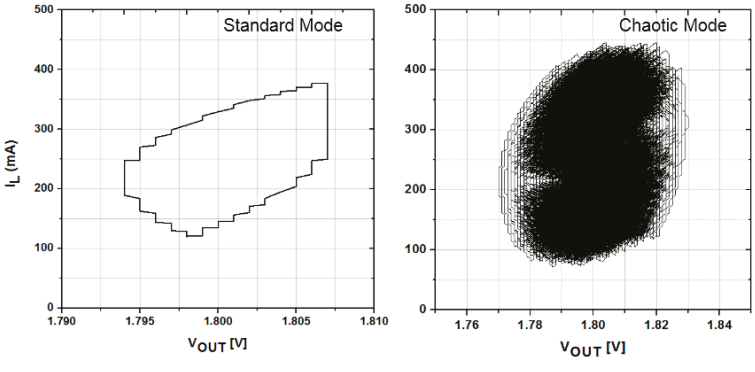
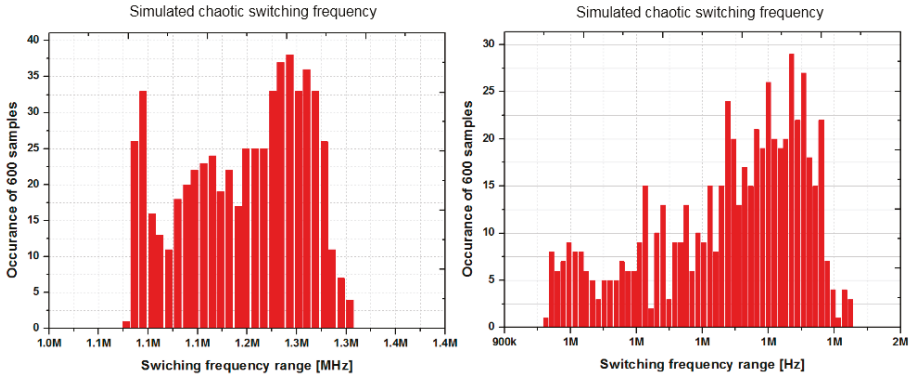


Figure 9. Operation mode of buck converter under phase-portrait view between two internal states (output voltage and inductor current): (**a**) Standard mode. (**b**) Chaotic mode.

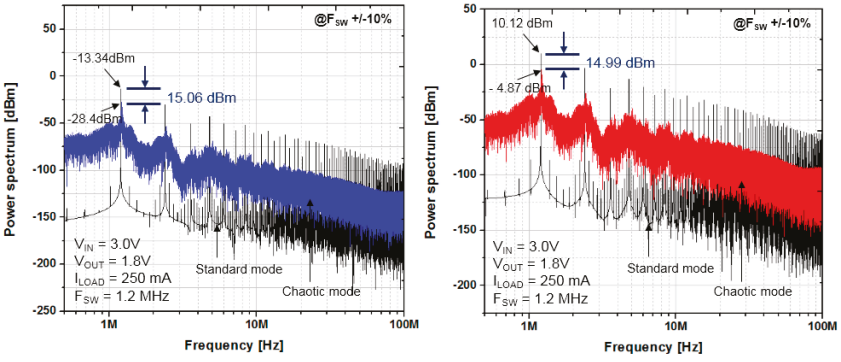
The simulated switching frequency distribution of the chaotic triangular ramp generator using slope modulation is shown in Figure 10. To achieve the most flattened power spectrum, a uniformly distributed switching frequency is most desirable [18]. As seen in Figure 10, the distribution of the chaotic switching frequency is not uniformly distributed over the desired frequency range. However, the frequency spreads out continuously in the pre-defined range; therefore, harmonic peaks in the power spectrum in chaotic mode are expected to disappear.



(**a**) (**b**)

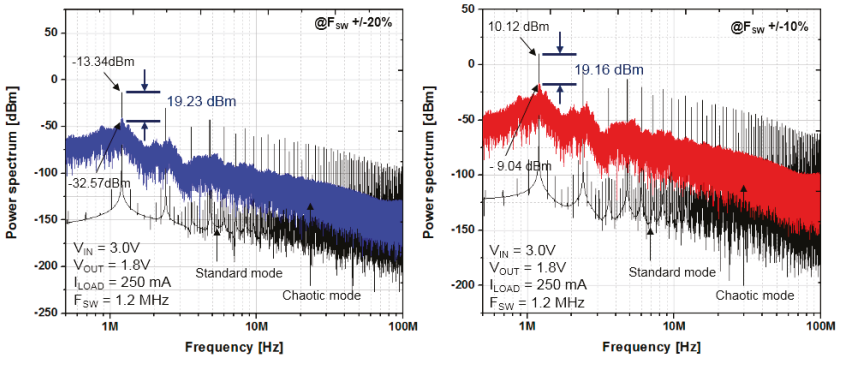
Figure 10. Simulated distribution of the switching frequency in chaotic mode using slope modulation: (**a**) 1.2 MHz +/− 10% (1.08 MHz to 1.32 MHz); (**b**) 1.2 MHz +/− 20% (0.96 MHz to 1.44 MHz).

Generally, the EMI reduction of the switched-mode dc-dc converters using spread spectrum technique can be verified by analyzing the power spectrum [16–18]. The power spectrum of the switching node and the output node were calculated using the available spectrum analyzer tool in Cadence software. Because of the intended target is to show the power spectrum up to 30 MHz, the resolution bandwidth (RBW) for the calculation of power spectrum was 6.67 kHz. The selected bandwidth for the spectrum analyzer in Cadence was also setup at 5 GHz for capturing all the harmonics for the analysis. Figures 11 and 12 show the simulated power spectra of the output node and switching node under different conditions of frequency deviation under I_{LOAD} = 250 mA. The spectrum of the converter in the standard mode with a fixed switching frequency of F_{SW} = 1.2 MHz is included as a benchmark for comparison with the chaotic mode. Clearly, the power is densely concentrated at the fundamental frequency of 1.2 MHz and its harmonics when the converter operates in standard mode, whereas the spectrum is continuous and the amplitudes of the spectral peaks are reduced in chaotic operations. This is because the total emitted energy does not change; instead, the energy gets spread over a wider frequency range, thereby reducing peak emissions [30]. To determine the optimal frequency deviation in the chaotic mode in terms of EMI reduction performance and minimize the negative side-effects, the proposed design was simulated for 2 cases. For the first case, the switching frequency was chaotically varied within +/−10% of F_{SW}, which reduced the fundamental harmonic peak from −13.34 dBm to −28.4 dBm at the output node and improved the peak at the switching node from 10.12 dBm to −4.87 dBm. The improvement of the power spectrum of the output node is similar to that of the switching node, and the EMI reduction for this case is approximately 15 dBm. For the second case, when the frequency deviation is increased to +/−20% of F_{SW}, the EMI reduction is approximately 19 dBm.



(**a**) (**b**)

Figure 11. Simulated power spectrum in chaotic mode (with slope modulation) with F_{SW} +/− 10% (1.08 MHz to 1.32 MHz): (**a**) Output node; (**b**) Switching node (@V_{DD} = 3.0 V, Vo = 1.8 V, Io = 500 mA, L = 2.2 µH, C = 2.2 µH).



(**a**) (**b**)

Figure 12. Simulated power spectrum in chaotic mode (with slope modulation) with F_{SW} +/− 20% (0.96 MHz to 1.44 MHz): (**a**) Output node; (**b**) Switching node (@V_{DD} = 3.0 V, Vo = 1.8 V, Io = 500 mA, L = 2.2 µH, C = 2.2 µH).

As shown in the power spectra in Figures 11 and 12, as the frequency deviation increases, the power spectra can be effectively spread over a wider frequency range, thereby reducing the peaks at the harmonic frequencies to much lower levels. In previous works using the randomized modulation technique [17,18], the power at the harmonic frequencies was spread out around discrete fixed-frequency levels. In particular, using the theory reported in [18], and assuming that randomness was assured, the theoretical reduction (ideal case) in the power spectrum using 2, 4, and 8 switching frequencies was 6 dB, 12 dB, and 18 dB, respectively. Using the spread-spectrum chaotic modulation proposed here, the reduction in the power spectrum can easily be more than 18 dB without the requirement of randomness because the power spectrum is spread continuously out rather than clustered around discrete frequency harmonics. Also, the hardware implementation of this proposed system is much simpler than that in the previous work. Therefore, the proposed design outperforms those earlier works.

Theoretically, the inductor current imbalance effect caused by the time-varying switching frequency in chaotic mode can be eliminated by using the triangular ramp generator. In fact,

the non-idealities, such as the non-ideal triangular ramp and the delay in the drivers and controller, will cause a small imbalance in the inductor current; therefore, in fact, the low-frequency ripple caused by the chaotic switching frequency still exists [4,28]. This perturbation will be injected into the output voltage at the switching frequency. A feedback network in response to perturbation at such a high rate of change cannot occur in a voltage-mode converter with limited bandwidth (0.2–0.3 switching frequency (F_{SW})), so the perturbation from the inductor current imbalance is injected into the output node. THis increases the output voltage ripple compared to the fixed-frequency PWM operation mode. After a few cycles, the amount of output voltage ripple accumulates, and the feedback network will start to respond and remove the redundant voltage. Figure 13 shows the simulation results for the inductor current ripple and the output voltage ripple when the converter operates in chaotic mode. As seen in this figure, the converter output ripple increases compared to the standard fixed-frequency mode (and the mean value of the output voltage is considered to be unchanged). In particular, the output ripple is more than two-fold (28 mV vs. 13.36 mV of standard mode) with F_{WS} +/− 10%, while the output ripple is more than three-fold that of standard mode when the switching frequency deviation ΔF_{SW} is increased to +/− 20% (36 mV vs. 13.36 mV of standard mode). Clearly, the output voltage ripple in the chaotic PWM mode is much higher than in the standard fixed-frequency PWM mode.

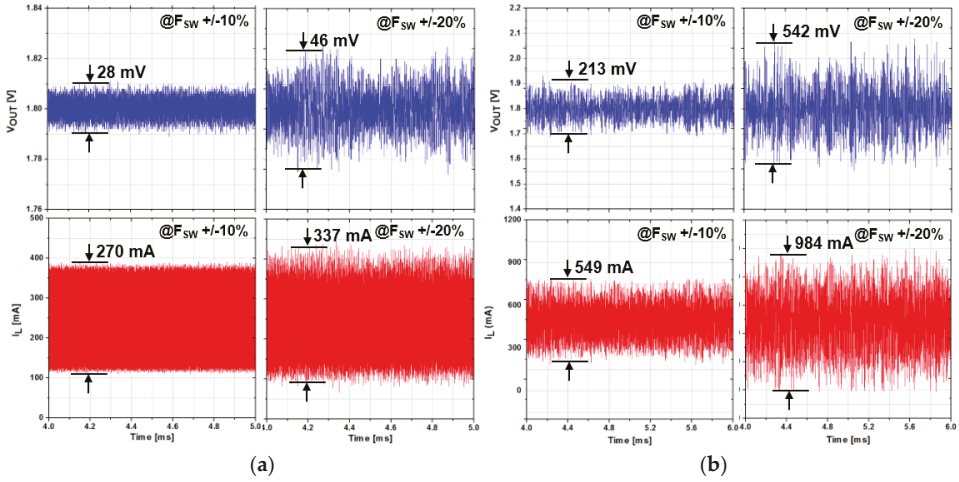


Figure 13. Simulated output voltage and inductor current waveform in chaotic mode: (**a**) Using ramp generator with slope modulation; (**b**) Ramp generator with peak modulation. Standard mode: V_{OUT_ripple}: 13.36 mV, I_{L_ripple}: 257 mA (@ Simulation condition: Io = 250 mA). (F_{SW} +/− 10% (1.08 MHz to 1.32 MHz); F_{SW} +/− 20% (0.96 MHz to 1.44 MHz)).

As presented previously, there are two schemes for chaotic modulation in the triangular ramp generator: peak modulation and slope modulation. All of the simulated results above are based on the triangular ramp generator using slope modulation. To re-confirm the advantages of slope modulation, we also checked the performance of the converter with the ramp generator using peak modulation. Under the same frequency deviation condition with peak modulation, the output ripple rose to 213 mV and 549 mV, and the inductor current ripple rose to 549 mA and 984 mA, respectively, for 10% and 20% of switching frequency deviation. This confirms that peak modulation should not be used in the chaotic ramp generator even if the EMI performance could be improved significantly because of the large trade-offs in the output voltage ripple and inductor current ripple.

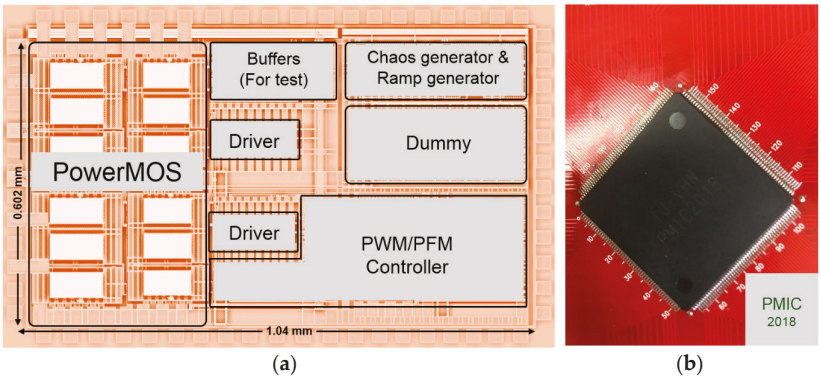
The results from the simulation showed that the frequency deviation (ΔF_{SW}) should be small to limit the effects on the output ripple and the inductor current ripple, but it should also be large

to achieve a significant EMI reduction. Therefore, the value of ΔF_{SW} should be determined by balancing the trade-off between the ripple performance and the EMI of the converter. The switching frequency deviation should not usually be more than 20% because of the large trade-offs on the primary performance, such as output voltage ripple, inductor current ripple, and power efficiency. For example, when ΔF_{SW} was higher than 20%, the output voltage ripple was increased by orders of up to 10 mV, which is unacceptable for practical use. Additionally, the high inductor current ripple with the triangular ramp using peak modulation adds difficulty in designing the PWM/PFM controller, because the load current is indirectly sensed through the inductor current when switching between the PWM/PFM modes. Because the inductor current ripple changes from cycle-to-cycle, unexpected ring switching will happen between PWM and PFM. Therefore, the triangular ramp generator using slope modulation is more appropriate because of it much lower ripple. Finally, it is important to understand that the effect of a fixed frequency of the clock (CK) in the chaotic circuit does not affect the EMI reduction performance of the proposed scheme, as was found in [18], because the operation of the converter is asynchronous with the clocking signal (CK) of the chaos generator. As shown by the power spectrum when the converter is in chaotic mode (Figures 11 and 12), it does not peak at CK = 1.2 MHz.

4. Experimental Results and Discussion

4.1. EMI Reduction Performance of the Proposed Scheme

To verify the proposed chaotic PWM scheme and compare it with a fixed-frequency PWM, a buck converter with the proposed chaotic ramp signal generator and slope modulation was designed and fabricated using a 3.3 V, 0.18 µm, CMOS one-poly six-metal-layers process. The active chip area was 0.626 mm^2 (0.602 µm × 1.04 mm), excluding bonding pads, where the power transistors occupy 520 × 365 μm^2. The chip photograph and the chip mounted on PCB for testing are shown in Figure 14. The experimental setup is shown in Figure 15 and the list of component values for the prototype is shown in Table 2. The terminal MODE (MODE = 0:Fixed-frequency PWM, MODE = 1:Chaotic PWM) can switch between the standard fixed-frequency PWM mode and the proposed chaotic PWM mode. Unless otherwise stated, all of the following results were measured using an input voltage of 3.3 V.



(**a**) (**b**)

Figure 14. (**a**) Chip layout of the chaotic-PWM (pulse-width modulation) voltage-mode buck converter; (**b**) Chip microphotograph; chip test on printed circuit board (PCB) (the top).

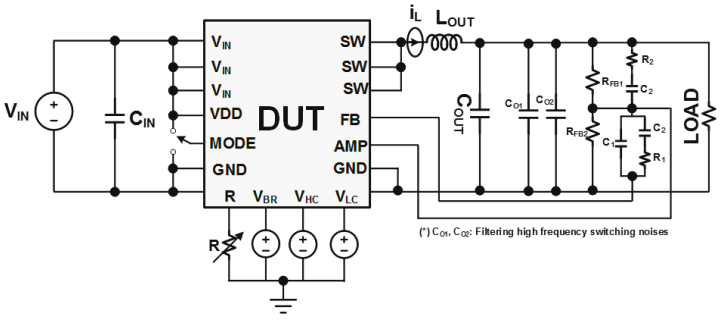


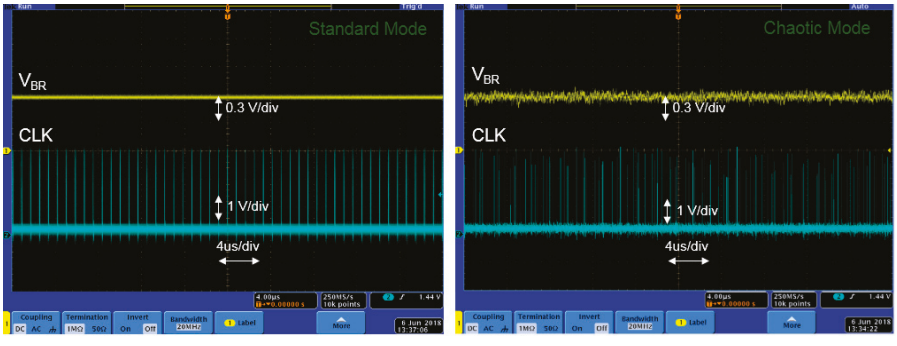
Figure 15. Experimental setup of the monolithic EMI-improved SiP buck converter. R is the current biasing current resistor of the V-I converter for the triangular ramp generator, and the V_{BR}, V_{HC}, and V_{LC} of the triangular ramp generator are easy to tune.

Table 2. List of component values used in test setup.

Parameter	Quantity
C_{IN}	10 µF
L_{OUT}	2.2 µH
C_{OUT}	2.2 µF
R_{FB1}	4.3 kΩ
(*) R_{FB2}	9.47 kΩ
C_1	15 pF
C_2	1 nF
C_3	470 pF
R_1	4.7 kΩ
R_2	560 Ω

(*) R_{FB2}: Controlled by a variable resistor (internal V_{REF}: 1.238 V).

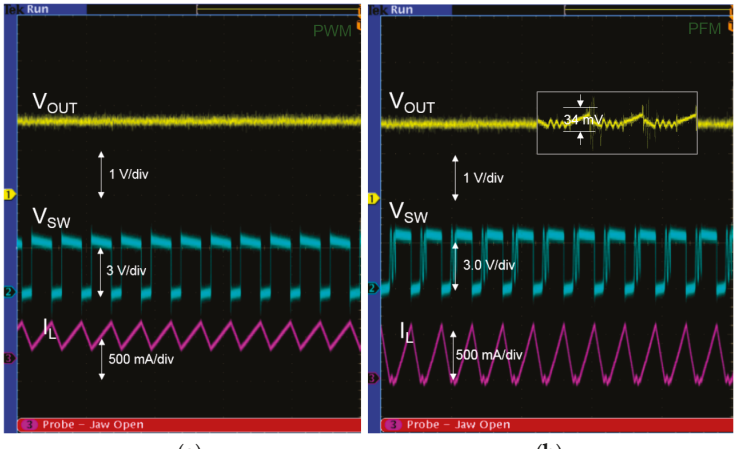
First, we constructed an experiment to examine the operation of the ramp generator to verify its functional operation before checking the EMI performance of the proposed scheme. Figure 16 shows the measurement results for the ramp generator in two modes (controlled by the MODE terminal). Because the parasitic capacitor on the voltage probe terminal of the measurement equipment is quite high (up to 10 pF) compared to the internal capacitor of the ramp and clock generator (2 pF in this study), the ramp signal should not be measured directly. Instead, an on-chip reading buffer was embedded to measure the clock signal inside the chip. The biasing current resistor (R) of the V-I converter for the triangular ramp generator is off-chip in order to tune the biasing current of the ramp generator in the prototype. When the MODE terminal is connected to the GND, the triangular ramp generator works in standard mode, whereas it works in chaotic mode when the MODE terminal is connected to the V_{DD}. Figure 16a,b shows the measurement results from the triangular ramp generator for the standard mode and the chaotic mode (F_{SW} +/− 20%), respectively. Clearly, the switching frequency is a constant for the standard mode when a fixed V_{BR} is used and chaotic when chaotic V_{BR} generated from the N-shaped chaos generator is used. The measured constant F_{SW} is approximately 1.2 MHz (MODE = 0 V, V_{BR} = 0.61 V), and the measured chaotic switching frequency is in the range from 1.06 MHz to 1.37 MHz (MODE = V_{DD}; V_{BR} is chaotic when internally connected to the N-shaped chaos generator; V_{HC} = 0.73 V, V_{LC} = 0.41 V (tuned values)). The experimental result for the triangular ramp generator matches well with the simulation result, with only a small mismatch caused by chip fabrication.



(**a**) (**b**)

Figure 16. Measurement result of the chaotic ramp generator: (**a**) Standard mode: triangular ramp generator with fixed switching frequency of 1.2 MHz (1.214 MHz); (**b**) Chaotic mode: ramp generator with chaotic switching frequency at F_{SW} +/− 20%. (Channel 1: V_{BR}; Channel 2: clock impulse signal. The width of measured impulse: ~15 ns; (X: 4 us/div, Y: 0.3 V/div)).

To test the EMI reduction in chaotic mode, the operation of the designed PWM/PFM buck converter in standard mode with a fixed switching frequency was also confirmed. Figure 17 shows the experimental results of the converter in standard mode under different load conditions (250 mA–PWM and 150 mA–PFM). The measured output ripples were 17 mV and 28 mA for the PWM and PFM modes, respectively.



(**a**) (**b**)

Figure 17. Measurement results for the fabricated chip in standard mode: (**a**) PWM mode (I_{OUT} = 250 mA); (**b**) pulse-frequency modulation (PFM) mode (I_{OUT} = 150 mA).

Because the switching node (rather than the output) is the dominant source of EMI [18], we evaluated the EMI performance by looking at the peaks in the power density spectrum of the inductor current (I_L), aiming to reduce it compared with its fixed-frequency counterpart. To evaluate the effectiveness of the proposed scheme, the inductor current of the buck converter in both the standard and chaotic mode was measured and analyzed using the discrete Fourier transform in MATLAB to estimate the EMI reduction. Figure 18a shows the measured inductor current in standard mode (top) and chaotic mode (bottom) with 10% switching frequency deviation, and Figure 18b shows their associated power spectrum analyses. The peaks that appear at the multiples of the

fundamental frequency, F_{SW}, are dramatically suppressed compared to the standard mode, similar to the simulation results in the previous section. The observed peak reduction at the first harmonic is about 14.53 dB, which agrees closely with the simulation result (15 dB). In fact, these differences come from the statistical properties of the chaotic output trajectory (in other words, the statistics of the chaotic frequency distribution). Also, the peak of the first harmonic of the power spectrum is at approximately 1.214 MHz for the standard mode, whereas the highest peak harmonic in the chaotic mode is at 1.2 MHz. Thus, the chaotic frequency distribution is focused at 1.2 MHz in chaotic mode, which slightly lowers the power spectrum reduction level of the proposed scheme. Additionally, the low spectrum peaks in the low-frequency range (lower than the minimum chaotic switching frequency) come from the low-frequency disturbance of the inductor current when the chaotic PWM is applied. However, it is still much lower than the other peaks, so it is not a concern related to EMI.

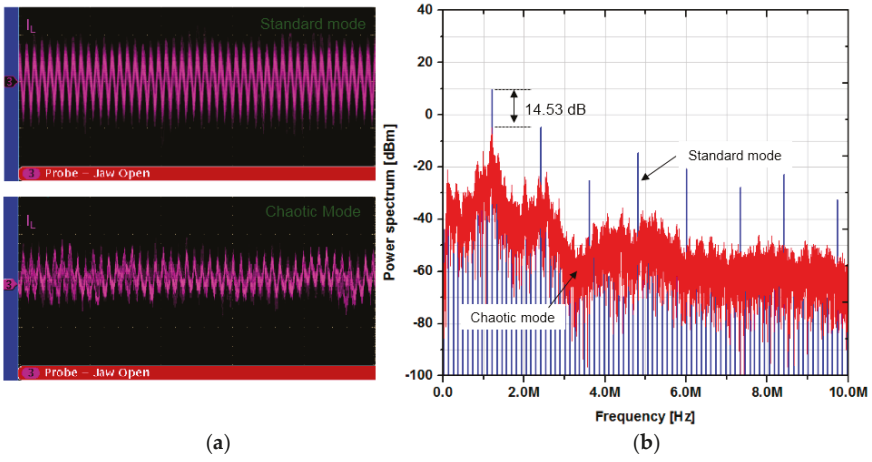


Figure 18. Measurement result of the fabricated chip: (**a**) Inductor current of the standard mode (top) and chaotic mode (bottom) (measurement mode: AC coupling @DC level: 0 V); (**b**) Power spectrum calculation results.

Comparisons with the standard are necessary to demonstrate the effectiveness of the proposed method. The EMI measurements of the buck converter in standard and chaotic modes are shown in Figure 19 along with the CISPR22 A-B limit. The EMI reduction obtained from the measurement is 14.36 dB at the fundamental switching frequency. The results show that operating the converter in chaotic mode reduces the EMI in the low-frequency range, which is consistent with the power spectrum analysis. The proposed method reduces the EMI of the DC-DC converter and satisfies the EMI standard is indicated in CISPR 22. In the test setup, the LISN (impedance stabilizer network) is located between the input power supply and the DC-DC converter under test [17]. Power spectrum analyzer is set at RBW = 3 kHz, and the frequency range of the measurements is 0.5–30 MHz.

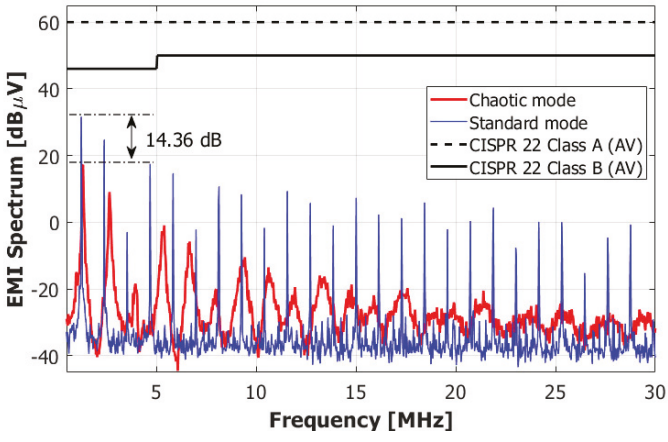


Figure 19. Conducted emission measurement of the buck converter.

The EMI performance of the proposed chaotic PWM scheme and other state-of-the-art works using the spread-spectrum technique are compared in Table 3. The proposed scheme achieved better EMI performance than the other alternatives compared. The performance of the proposed scheme can be explained by the fact that the chaotic switching frequency in the proposed scheme is continuously spread out within a certain frequency range rather than swept at several random fixed-frequency levels, as presented in [17,18]. In addition, the randomized PWM methods in [17,18] are usually costly because of their complex designs and the difficulty of confirming randomness. The most appealing advantage of the proposed scheme is that it can be easily embedded into any PWM buck converter using a standard ramp generator without modifying the overall structure. Therefore, the proposed scheme offers a cheap and effective solution for practical usage.

Table 3. EMI reduction performance of the proposed scheme and stage-of-the-art alternatives.

Ref.	Implementation Method	Modulation Technique	EMI Reduction	Switching Frequency	Compatibility for On-Chip Integration
[17]	CMOS @ 0.35 μm	Random PWM	12.85 dB	0.89–1.44 MHz	Suitable
[18]	CMOS @ 0.18 μm	Random PWM (Frequency hopping)	12.6 dB	1.4–2.1 MHz	Suitable
[19]	Hybrid	Chaotic PWM	10 dB [1]	60 +/− Δf [2]	No
This work	CMOS @ 0.18 μm	Chaotic PWM	14.53 dB	1.04–1.31 MHz	Suitable

[1] Extracted from figure; [2] Δf is not determined.

4.2. Reducing the Side Effects of the Proposed EMI-Improvement Scheme

The main purpose of a DC-DC converter is power conversion; therefore, the power efficiency of a converter must be maintained in a reasonable range whatever EMI reduction technique is used. Figure 20 shows the measured power efficiency at different load currents. The maximum power efficiencies of the converters are 84% and 83.1% for the fixed-frequency PWM mode and chaotic PWM mode, respectively. There is no difference in the power efficiency between the two PFM modes because they are common and are not included in EMI reduction. When the converter operates in PWM at moderate and heavy loads (200 mA to 450 mA), the power efficiency of the chaotic mode is less than that of the standard mode. The maximum power efficiency degradation is at the maximum load condition of 450 mA, with a reduction of 2% in power efficiency, mainly from the conduction loss, because the average switching frequency of the converter in chaotic mode and fixed-frequency in

standard mode is approximately equal. When the converter operates in the chaotic mode, the ripple range of the inductor current increases, which results in an increase in the RMS inductor current. As a consequence, the power loss on the inductor and the on-resistance of the power switches also increases.

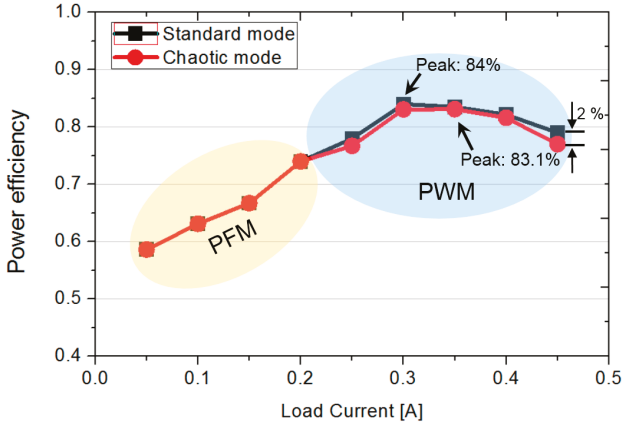
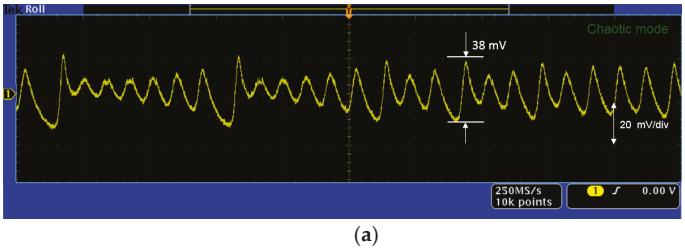


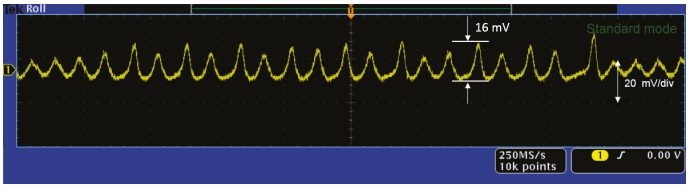
Figure 20. Measured power conversion efficiency at standard fixed-frequency mode and chaotic frequency mode with F_{SW} +/− 10%. The maximum power efficiency reduction of 2% is at 450 mA of load current.

Figure 21 shows the measured output voltage ripple in two modes. In this experiment, additional capacitors were added (as shown in Figure 3) to eliminate the high-frequency noises caused by the switching operation of the power switches. The measurements show an output voltage ripple of 38 mV and 16 mV for chaotic mode and standard mode operations, respectively. Compared to the output voltage ripple when the converter operates in PFM mode (Figure 17b), the ripple of the converter in PWM chaotic mode is approximately the same. This can be solved by increasing the capacitor value at the output but that increases the power module and adds additional costs. However, compared to the active EMI reduction with an input filter, this scheme is still much better, and therefore, it can be used for many applications. For a further demonstration, we conducted an experiment in which we increased C_{OUT} to 4.7 uF. The output voltage ripple decreased from 38 mV to 27 mV (approximately equal to the output voltage ripple when the converter enters PFM mode at a light load). It should be noted that this might result in instability. As a consequence, the compensation network should be redesigned to balance EMI performance with other factors, depending on the specific application.



(**a**)

Figure 21. *Cont.*



(**b**)

Figure 21. Measurement of output voltage ripple: (**a**) Chaotic mode and (**b**) Fixed-frequency mode (Measurement Mode: AC coupling @ DC level: 0 V).

5. Conclusions

In this paper, we have proposed and implemented a SiP buck converter with a fully on-chip chaotic triangular ramp generator for EMI reduction. The on-chip chaotic triangular ramp generator is constructed from an N-shaped chaos generator linked with a symmetrical triangular ramp generator. The on-chip chaos generator generates a controllable chaotic signal and applies it to modulate the slope of the triangular signal. The proposed modulated triangular signal based on the N-shaped chaotic circuit is then applied to the spread-spectrum control of a dual-mode PFM/PWM SiP buck converter with EMI reduction. To verify the effectiveness of the proposed scheme, the proposed EMI-improved buck converter was fabricated in a standard 0.18 μm CMOS process, and the experimental results verified the effectiveness of the proposed technique. The proposed scheme experimentally achieved up to 14.53 dB EMI reduction. In the simulation, extending the spread-spectrum bandwidth increased the EMI reduction amount to 19.13 dB with a 20% deviation in the switching frequency. The modulated triangle signal reduces the inductor current imbalance when the converter operates in chaotic mode. Therefore, the magnitude of the output voltage ripple and inductor current ripple of our design is lower than that in other works. This relaxes the required LC value for the output filter of the DC-DC converter. Due to its simplicity of implementation, high EMI improvement, and LC size relaxation, the proposed scheme can effectively solve EMI issues in many applications, especially on-chip and in-package solutions.

Author Contributions: V.H.N. developed the concept and implemented the chip layout. V.H.N. and H.A.H. performed all the experiment, thoroughly analyzed the data and wrote this research article. H.S. and S.K. technically supervised the research work.

Funding: This work was supported by the National Research Foundation of Korea through the Korea Government (MSIP) under Grant NRF-2017R1A2B2003240. This work was also supported by Inje University research grant 2018.

Acknowledgments: The authors would like to thanks Tung Ngoc Nguyen École de Technologie Supérieure, University of Quebec, for his fruitful discussion and guidance. Thanks to IDEC-Korea for their support on CAD tool and chip fabrication.

Conflicts of Interest: The authors declare no conflicts of interest.

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Automatic EMI Filter Design for Power Electronic Converters Oriented to High Power Density

Graziella Giglia [1,*], Guido Ala [1], Maria Carmela Di Piazza [2], Giuseppe Costantino Giaconia [1], Massimiliano Luna [2], Gianpaolo Vitale [2] and Pericle Zanchetta [3]

[1] Dipartimento di Energia, Ingegneria dell'Informazione e Modelli Matematici, Università degli Studi di Palermo, Viale delle Scienze, 90128 Palermo, Italy; guido.ala@unipa.it (G.A.); costantino.giaconia@unipa.it (G.C.G.)

[2] Istituto di Studi sui Sistemi Intelligenti per l'Automazione, Consiglio Nazionale Delle Ricerche, via Dante 12, 90141 Palermo, Italy; dipiazza@pa.issia.cnr.it (M.C.D.P.); luna@pa.issia.cnr.it (M.L.); vitale@pa.issia.cnr.it (G.V.)

[3] Department of Electrical and Electronic Engineering, University of Nottingham, University Park, Nottingham NG7 2RD, UK; Pericle.Zanchetta@nottingham.ac.uk

* Correspondence: graziella.giglia@unipa.it

Received: 18 December 2017; Accepted: 16 January 2018; Published: 18 January 2018

Abstract: In this paper, a complete computer aided procedure based on the power density concept and aimed at the automatic design of EMI filters for power electronic converters is presented. It is rule-based, and it uses suitable databases built-up by considering information on passive components available from commercial datasheets. The power density constraint is taken into consideration by imposing the minimization of the filter volume and/or weight; nevertheless, the system in which the automatically designed filter is included satisfies the electromagnetic compatibility standards limits. Experimental validations of the proposed procedure are presented for two real case studies, for which the performance and the size of the best filter design are compared with those related to a conventionally designed one.

Keywords: EMI filter; power converter; power density; optimal design; electrical drives

1. Introduction

The use of power electronic converters is very common in many industrial applications such as in the aeronautic and automotive fields, in hybrid vehicles, and in the electric aircraft context. This trend usually generates a reduction of the installation cost, but low volume and weight requirements are very important to facilitate installation, handling, and maintenance operations of the power converter. High power density power electronic converters are becoming increasingly essential for future markets [1,2].

The use of power devices with high speed commutation makes such systems unintentional EMI sources. Therefore, EMI attenuation solutions are necessary to ensure both the reliability and the electromagnetic compatibility of the system of which the power electronic converter is a part. In particular, EMI filtering is required to ensure the compliance with the emission limits imposed by the stringent technical standards [3–12], and behavioral models of electric motors can also be used to predict conducted interferences [13]. It is worth noting that electromagnetic compatibility and power density in power electronic converters are closely related issues.

The EMI filter is a part of the power electronic converter and it can significantly influence its size and weight. In order to address this issue, besides satisfying EMI limits, a further reduction of the filter size/weight is a requirement of crucial importance in the design phase [1,14,15].

The power density feature of EMI filters has been treated in scientific literature, but the presented techniques cannot be applied in a general way. In fact, some of these techniques propose only the use of high-performance magnetic materials to reduce the inductor core's size [15]. In [16], some aspects for the design of high-density EMI filters for DC-fed motor drives are discussed and, in particular, grounding issues, circuit topologies, and some strategies to reduce the overall filter size are covered. In [17], the impedance interaction between the EMI filter and the noise propagation path, and its influence on the common mode (*CM*) filter design, are investigated; by applying this method, the impedance-mismatching concept is used to obtain a reduction of the *CM* inductor value that can potentially achieve a high power density. However, this method is only applied to a *CM* EMI filter design.

Other approaches propose the use of genetic algorithms to perform an EMI filter design [18]. In those cases, optimal solutions are usually obtained with a great number of iterations, thus resulting in a time consuming task.

In [19], the authors present software for designing EMI filters, limited only to one filter topology; the authors do not include the possibility of a discrete differential mode (*DM*) choke selection. Moreover, the paper only provides data about the *CM* core size, and the choice is not based on optimization.

In [20,21], a minimization of the filter volume is performed by using interpolated volumetric parameters. This approach can only be applied to the *DM* filter components and not to *CM* components because a parametrization of the volume curves is not possible for most of the commercially available *CM* chokes. Finally, a systematic approach for the volume optimization of a two-stage *DM* and *CM* EMI filter, essentially based on the ratio between the *CM* and *DM* inductance of the first filter stage, is proposed in [22].

After having defined both the EMI filter topology and the component values, the EMI filter can be setup according to a considerable number of feasible configurations. The conventional design of EMI filters, based on a trial and error approach, requires significant effort in terms of time, and it does not guarantee the optimal choice of filter components to obtain the maximum power density.

The first results of a rule-based computer-aided general procedure for the optimal design of EMI filters in terms of volume minimization have been proposed in [23] by the same authors.

In this paper, a comprehensive automatic procedure has been set-up; the procedure allows the design of the best filter configuration in a simple and fast way. Power density impact evaluation (i.e., volume, weight) of the filter configuration has been carried out, thus achieving useful results for engineers and scientists. The proposed algorithm can be implemented using any software programming environment and has a low computational demand.

Furthermore, suboptimal configurations can be compared with each other and with the best one so as to allow the designer to make the final choice and to also match further commercial constraints, if there are any.

The proposed procedure starts from the basic principle of conventional EMI filter design and considers the additional objective of pursuing the best power density for the EMI filter. A suitable test set-up enables one to obtain an experimental assessment of the automatic design procedure by comparing volume, weight, and performance.

2. The Rule-Based Computer-Aided EMI Filter Design Procedure

A multistage EMI filter configuration usually provides a stronger filter attenuation; consequently, it determines a higher cutoff frequency value than that obtained with a single stage filter. Furthermore, a higher value of the cutoff frequency leads to smaller values of the filter components and to physically smaller components. Therefore, even if the number of passive components is larger in a multistage configuration, overall, the latter may exhibit a smaller volume/weight than a single stage filter as has been demonstrated for the *DM* mode in [20]. However, it depends on the *CM* and *DM* required attenuations, on the electrical characteristics of the power electronic circuit under study, and on the

adopted filter components. A verification of all feasible configurations is necessary to assess which of them allows one to obtain the best power density; the achievement of a trade-off is not a trivial task due to the broad variety of components that the market offers. Therefore, the choice of the best filter design, in terms of maximization of the power density, is not ensured by following a conventional design procedure.

The proposed design procedure is a rule-based algorithm that takes into account the characteristics of the filter application: the power electronic circuits, the constraints of the filter design, and the databases of commercial components for the setup of the EMI filters. The flowchart of the design method is shown in Figure 1, in which *AWG* is the conducting wire diameter; n_{stages} is the number of filter stages; N_{max} is the maximum number of turns for each core; C_y and C_x define the capacitance of phase-to-ground and phase-to-phase capacitors, respectively; V_{C_rated} and C_{rated} indicate the capacitor rated voltage/capacitance, respectively; V_N is the rated voltage of the power converter; and B_{max} and B_{sat} are the maximum/saturation magnetic induction values, respectively.

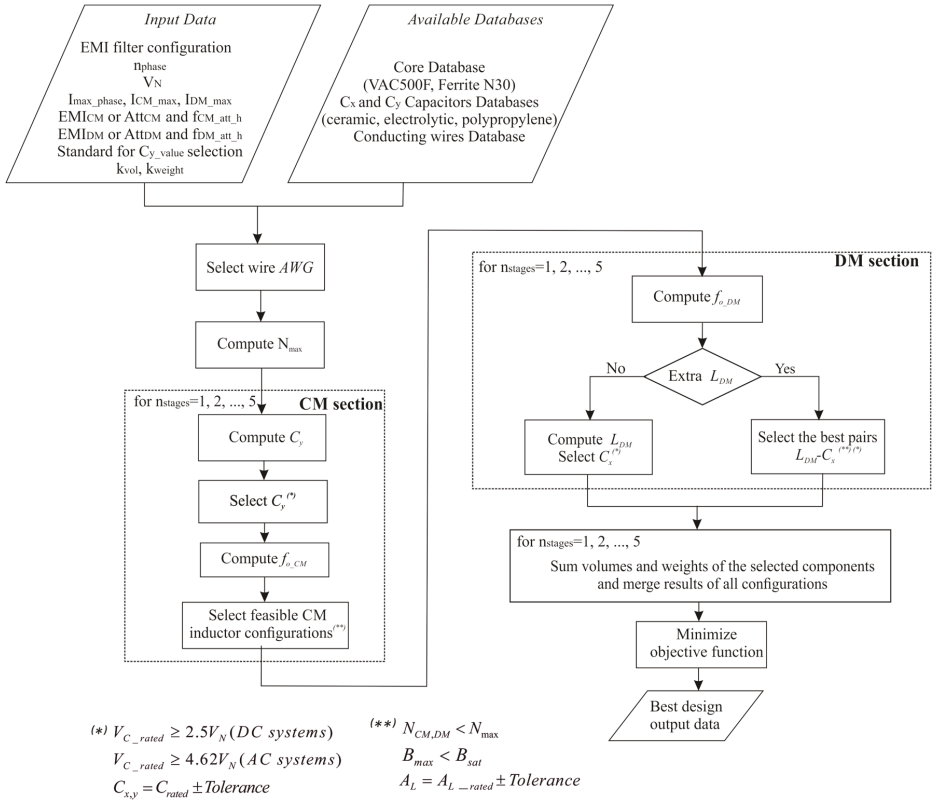

Figure 1. Flowchart of the proposed design method.

Firstly, the designer must define the following *Input Data*:

- *EMI filter topology* (e.g., Γ, Π, T);
- n_{phase}: number of AC phases or DC lines of the power electronic system;
- V_N: rated voltage of the power converter;
- I_{max_phase}: maximum operating current;

- I_{CM_max}, I_{DM_max}: maximum value of the *CM* and *DM* currents;
- *Standard for* C_{y_value} *selection*: the *CM* capacitance value limits the ground current and thus it is related to safety issues. Either the SAE AES 1831 standard or the maximum ground leakage current are taken into consideration to define the capacitance value;
- k_{vol}, k_{weight}: coefficients provided by the designer which allow one to obtain the best design, assuming any linear combination of volume and weight as the objective function;
- filter design can be performed either on the basis of the measured *CM*/*DM* spectra (EMI_{CM}, EMI_{DM}), or by explicitly giving the required *CM*/*DM* attenuations (Att_{CM}, Att_{DM}) and the CM/DM component frequencies to be attenuated ($f_{CM\_att\_h}$ and $f_{DM\_att\_h}$). In the first case, the algorithm identifies the crucial point among the more relevant peaks at the lowest frequencies on the EMI spectra. Then, it computes the required attenuations for the *CM* and *DM* noise as expressed in (1) and (2), respectively:

$$Att_{CM} = A_{h\_CM} - A_{max} + \Delta \tag{1}$$

$$Att_{DM} = A_{h\_DM} - A_{max} + \Delta \tag{2}$$

where A_{h_CM} and A_{h_DM} are the amplitudes of the frequency spectrum components to be attenuated; A_{max} is the maximum amplitude allowed by the standard; and Δ is a safety margin (usually 6 dBμV).

For the reader's convenience, it is worth recalling that EMI filters are generally low-pass passive filters realized with inductors and capacitors. The adopted arrangements can be Γ, Π, and T with longitudinal inductors and transversal capacitors. The choice of the passive filter topology is related both to the theoretical attenuation value of the chosen filter configuration (i.e., 40 dB/dec for Γ type L-C single stage, 60 dB/dec for Π or T type L-C single stage, etc.) and to the equivalent impedance magnitude of the equipment under test (EUT) and of the noise receiver. Therefore, a preliminary step for a proper EMI filter design is to suitably choose the filter topology by taking into account the criterion of maximum impedance mismatching between the source and the receiver.

Three databases of devices available on the market have been set up. The first one includes magnetic cores and it is populated with the following relevant data:

- core material and model;
- geometric dimensions and weight;
- inductance factor A_L (μH/1 turn) at 10 kHz and the value of flux density saturation;
- A_L tolerance.

The cores database currently contains components that allow an EMI filter design for applications up to some kW.

Furthermore, a second database of Y-type (*CM* noise reduction) and X-type (*DM* noise reduction) capacitors has been created. Ceramic Y-type capacitors, and aluminum electrolytic and polypropylene X-type capacitors for applications with high frequency ripple currents have been included. In particular, the aluminum electrolytic capacitors have a rated voltage of 160 V, 250 V, and 400 V, and a nominal capacitance range of 10 μF to 330 μF, whereas the polypropylene capacitors have a minimum rated voltage of 560 V_{DC}/275 V_{AC} (a lower rated voltage for this specific capacitor is not commercially available) and a nominal capacitance range of 0.01 μF to 10 μF.

The commercial capacitors database is populated with the following relevant data:

- brand, material, series, model, and package;
- rated capacitance and voltage;
- capacitance tolerance;
- geometric dimensions and weight.

Finally, a third database, including conducting wires, is provided. Hence, the volume/weight contribution given by the inductor wires (which may be relevant when dealing with rated power of

hundreds of Watts and beyond) is included in the EMI filter calculations, and more effective results can be obtained.

After having defined the input data, the conventional design procedure steps are automatically repeated for different arrangements and finally the one which exhibits the best power density is selected.

It has to be underlined that a multi-stage filter may occupy a reduced volume in comparison with a single stage one, as stated in [20]; therefore, the rule-based algorithm analyses all feasible EMI filter designs considering a number of filter stages (n_{stages}) up to five. The evaluation of a maximum number of five stages has been considered by the authors as a reasonable choice.

As shown in Figure 1, the first operation phase is the selection of wire size (AWG) on the basis of the maximum operating current entered by the designer. Then, the maximum number of achievable turns (N_{max}) on each toroidal core of the database is computed as:

$$N_{max} = \frac{2\sigma_{winding}}{360^{\circ}} \frac{I.C.}{D_{wire}} \tag{3}$$

where $I.C. = \pi(ID_{core} - D_{wire})$ is the inner circumference of the toroidal core, ID_{core} is the inner diameter of the toroidal core, D_{wire} is the wire diameter, and $\sigma_{winding}$ represents the maximum angle that the winding subtends on half of the core. It is acceptable to assume that $\sigma_{winding}$ is equal to 145° (Figure 2).

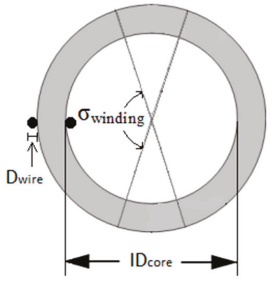

Figure 2. Toroidal core: geometric parameters for Equation (3).

Then, the procedure performs the *CM* and *DM* filter design as described below.

2.1. CM Section Design

The procedure calculates, for $n_{stages} = 1, \ldots, 5$, the *CM* capacitance ($C_{CM}$) and the *CM* inductance (L_{CM}) as follows:

$$L_{CM} = \frac{1}{C_{CM}(2\pi f_{o\_CM})^2} \tag{4}$$

$$C_{CM} = n_{phase} C_y \tag{5}$$

The cutoff or corner frequency ($f_{o\_CM/DM}$) is evaluated by considering that the attenuation of an L-C filter starts at this frequency and is rising with Att_intr_{CM/DM_filter}, which is the inherent filter attenuation strictly related to its topology (e.g., 40 dB/dec for Γ type L-C single stage, 60 dB/dec for Π or T type L-C single stage, etc.). Thus, the required corner frequency can be evaluated according to:

$$Att_{CM/DM} = n_{stages} \times Att\_intr_{CM/DM\_filter} \log\left(\frac{f_{CM/DM\_att\_h}}{f_{o\_CM/DM}}\right) \tag{6}$$

thus obtaining:

$$f_{o\_CM/DM} = \frac{f_{CM/DM\_att\_h}}{10^{\left(\frac{Att_{CM/DM}}{n_{stages} \cdot Att\_intr_{CM/DM\_filter}}\right)}} \tag{7}$$

As already underlined, the more relevant peaks of the EMI spectra are identified together with the corresponding frequencies. Then, for each of these frequencies, the required attenuations are evaluated for the *CM* and *DM* noise as expressed in (1) and (2), respectively. The corner frequency is then evaluated by (7) for each of the previous relevant frequencies and among them, the lowest frequency is selected as the cut-off frequency of the L-C filter; this frequency is usually lower than 150 kHz.

Then, the number of turns (N_{CM}) needed to set up the required inductance is computed by (8):

$$N_{CM} = n_{phase}\sqrt{\frac{L_{1\_CM}}{A_L}} \tag{8}$$

where $L_{1\_CM} = n_{phase}L_{CM}$ is the inductance value of the single *CM* choke winding. Equation (8) (and also (9) in the following) is derived by considering that for a highly symmetric magnetic core such as the toroidal inductor, the Ampere-law enables one to express the inductance as follows: $L = N^2 A_L$, where A_L is the inverse of the core reluctance evaluated along the centerline of the core l: $A_L = \frac{\mu A}{l}$, A is the cross section area of the core, and μ is the magnetic permeability. Then, the minimum volume C_y capacitor is chosen from the database according to the design constraint $V_{C_{y\_rated}} \geq k \times V_N$, where k is a multiplier factor (equal to 2.5 for DC systems and 4.2 for AC systems [24]). In accordance with the computed value for the *CM* inductance, the cores allowing the effective realization of the *CM* choke (i.e., $N_{CM} < N_{\max}$) are selected from the database, also verifying the absence of cores saturation.

2.2. DM Section Design

It is possible to choose two alternative procedures by taking into consideration either the leakage inductance of the *CM* choke (*No extra* L_{DM}) or a *DM* inductor (*Extra* L_{DM}). The selection between the "*No extra* L_{DM}" and "*Extra* L_{DM}" procedures is performed by the designer. Moreover, both the procedures can be performed sequentially and then the most appropriate in terms of volume/weight can be selected.

Both procedures include the evaluation of the corner frequency versus the number of stages. Then:

- the "*No extra* L_{DM}" procedure computes, for n_{stages} = 1, . . . , 5, the leakage inductance of the feasible *CM* chokes and the corresponding computed value for the *DM* capacitance.

  After the computation of the C_{DM} capacitance, the algorithm selects the capacitor with the minimum volume, according to the design constraint $V_{C_{x\_rated}} \geq k \times V_N$
- in the "*Extra* L_{DM}" procedure, for n_{stages} = 1, . . . , 5, the *DM* inductance candidate values are obtained on the basis of the X-capacitors values (ranging between 10 nF and 330 µF). For each *DM* core, the number of turns is then computed as follows:

$$N_{DM} = \sqrt{\frac{L_{1\_DM}}{A_L}} \tag{9}$$

where $L_{1\_DM} = L_{DM}/2$ is the inductance value for each *DM* core. The cores permitting an effective realization are extracted from the database, in accordance with the $N_{DM} < N_{\max}$ constraint and ensuring no saturation. Finally, the feasible L_{DM}-C_x pairs that permit one to setup the *DM* section according to the design constraints $V_{C_{x\_rated}} \geq k \times V_N$, are selected.

The "*Extra* L_{DM}" may be more appropriate when the use of a higher L_{DM} value is preferred to diminish the value or the size of *DM* capacitors.

The verification of the absence of the *CM*/*DM* cores saturation ($B_{max} < B_{sat}$), performed in the design of both sections, allows one to obtain no degradation of the noise mitigation capability of the designed filter configurations.

The procedure also takes into account the component tolerances; in fact, neglecting the tolerances could degrade the filter performance. The capacitors database contains components with a tolerance range of ±20%; the cores database contains components with a tolerance of the A_L value from −25% to +45% and from −30% to +30% for the vitroperm and ferrite materials, respectively. The negative tolerance percentage determines a degradation of the filter performance because it implies an actual value of the component lower than the nominal one and consequently a cutoff frequency higher than that required; hence, the filter will begin to attenuate at a higher frequency than the desired one. This issue is taken into account by choosing the commercial components based on the value related to the negative tolerance.

Finally, the EMI filter volume and weight of all realizable arrangements are computed and the one with the best power density is selected. A comparison among suboptimal results and the best arrangement is also allowed.

The filter configurations obtained by the automatic procedure are related to the specific components included in the databases, whose number and typology can be increased, if needed.

3. Experimental Setup

The automatic design procedure has been validated by experimental investigations by using a suitably devised test bench.

A PWM IGBT Voltage Source Inverter (VSI) supplying a three-phase load has been considered. The inverter is setup by a STGIPS10K60A power module and an Altera Cyclone III FPGA board realizing the PWM.

The inverter switching frequency is set to 20 kHz and the output voltage is 48 V.

A DC Line Impedance Stabilization Network (LISN) is used, with a voltage potentiality up to 600 V [25].

In order to assess the validity of the proposed approach, two case studies are considered with different three-phase loads:

- Case study #1: a 220 W induction motor, commonly used both in vehicles (road and marine vehicles, aircraft) and in DC systems, such as those installed in some residential/commercial smart buildings [26,27];
- Case study #2: a symmetric resistive load with low-power (7.2 W).

The experimental configuration scheme is given in Figure 3.

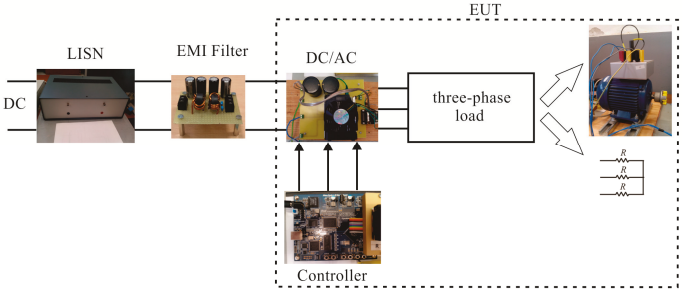

Figure 3. Block diagram of the experimental rig.

4. Experimental Validation and Discussion

Experimental measurements and plate values are the inputs required for the proposed computer-aided design methodology.

The EMI measurements have been carried out by using an RF current probe R&S EZ-17 (20 Hz–100 MHz, maximum DC current equal to 300 A) and an R&S FSH4 (100 kHz–3.6 GHz) spectrum analyzer. A Tektronix TDS7254B 2.5 GHz–20 GS/s–4 channels oscilloscope has been employed for the time domain measurements.

Figure 4 shows the *CM* and *DM* EMI spectra obtained for the two case studies. Both measured spectra show similar low frequency outlines, mainly due to the harmonics of the switching frequency. On the other hand, the induction motor drive has a significant impact on the high frequency EMI profile. Therefore, as expected, the load affects the noise emission profile. In fact, the test bench of case study #1 and #2 is the same, and it differs only for the three-phase load.

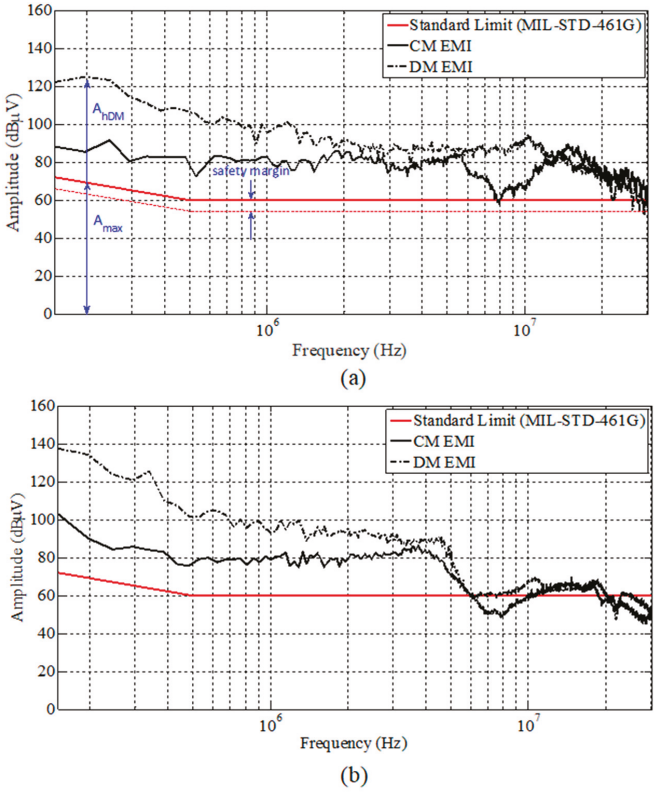

Figure 4. Measured *CM* and *DM* EMI for (**a**) three phase induction motor load (**b**) three phase resistive load. In (**a**) the parameters reported in Equations (1) and (2) are also shown.

In both case studies, the limit curve of the Military Standard 461G [28] has been used as the EMI limit standard, a Γ-Π topology for the EMI filter has been considered (Figure 5), the SAE AS 1831 standard has been used for C_y selection, and volume optimization has been selected due to space constraints (k_{vol} = 100% and k_{weight} = 0%).

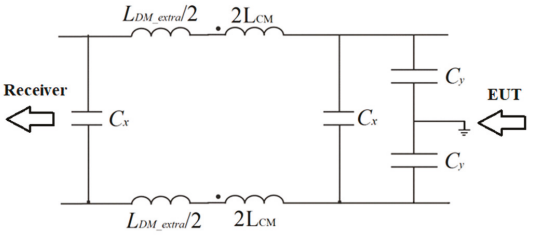

Figure 5. Γ-Π filter topology (single stage) for the experimental setup.

In the first case study, the measured *CM*/*DM* spectra are used as input data; the following filter parameters have been returned by automatic processing:

- Att_{CM} = 30 dBμV@150 kHz;
- -Att_{DM} = 60 dBμV@170 kHz.

In Table 1, the input data used to run the rule-based algorithm are reported.

Table 1. Input data for the rule-based algorithm–case study #1.

System Type	DC System
V_N	48 V
I_{max_phase}	5 A
I_{cm_max}	32 mA
I_{dm_max}	150 mA
k_{vol}	100%
k_{weight}	0%

In the second case study, the following filter parameters have been obtained by the automatic processing of the measured *CM*/*DM* spectra:

- Att_{CM} = 25 dBμV@150 kHz;
- Att_{DM} = 60 dBμV@150 kHz.

In Table 2, the input data used to run the rule-based algorithm are reported.

Table 2. Input data for the rule-based algorithm–case study #2.

System Type	DC System
V_N	48 V
I_{max_phase}	150 mA
I_{cm_max}	45 mA
I_{dm_max}	60 mA
k_{vol}	100%
k_{weight}	0%

For case study #1, the best design leads to a double stage (n_{stages} = 2) filter without extra *DM* inductors among a total amount of 910 practicable arrangements.

For case study #2, the filter chosen for the experimental validation is one of the 1038 feasible configurations proposed by the design procedure, corresponding to the 28th one. Even if it is not the best configuration in terms of minimum volume, it has been chosen because it is a double stage (n_{stages} = 2) filter with an extra L_{DM}: in this way, it is also possible to validate the design procedure in the case of separate *DM* inductors.

Both EMI filters have been set-up. The benchmark is a single stage EMI filter designed and built-up by the conventional procedure [15,29].

To be significant, the filter performance comparison requires the consideration of the same test rig; for this reason, the comparison is performed with the EMI filter designed in [15], highlighting the improvement. The benchmark filter has been designed by using a high permeability nanocrystalline magnetic material for the *CM* choke. This material has the highest permeability and lowest coercive field strength, ensuring minimal eddy current losses and an outstanding frequency vs. permeability behavior. Furthermore, it is worth noting that the conventional design procedure, in which the cutoff frequency is lower than the power converter switching frequency, determines the same filter in both case studies.

In Tables 3 and 4, the size and performance of the automatically designed filters and the benchmark filter are compared.

Table 3. Filter design output data–case study #1.

	Conventional Design	**Automatic Design**
Number of Stages	1	2
L_{CM}@10 kHz	0.8 mH	126 µH (each stage)
CM inductor core dimensions (mm × mm × mm)	27.9 × 13.6 × 12.5	12 × 8.0 × 4.5 (each stage)
CM core A_L@10 kHz	65.5 µH (Vitroperm 500F, model T60006-L2025-W380)	28 µH (Vitroperm 500F, model T60006-L2012-W902) (each stage)
Number of turns per CM winding	5	3 (each stage)
C_{CM}	200 nF	100 nF (each stage)
C_y	100 nF, ceramic, 250 V, (Murata RDER72E104K2)	47 nF, ceramic, 250 V, (Murata RDER72E473K2) (each stage)
L_{DM}@10 kHz	1.6 µH ($L_{leakage}$ = 0.2% L_{CM})	252 nH ($L_{leakage}$ = 0.2% L_{CM}) (each stage)
C_{DM}	47 µF, electrolytic, 400 V, (Panasonic EEUEE2G470)	33 µF, electrolytic, 160 V, (Kemet ESG336M160AH4) (each stage)
Wire size	15 AWG	15 AWG
Volume	25.87 cm^3	13.88 cm^3 (all stages)
Weight	44 g	19.12 g (all stages)

More compact filters are obtained with the automatic procedure, as expected. A reduction of about 56% in weight and about 46% in volume is reached in case study #1; a reduction of about 67% in weight and about 62% in volume is obtained in case study #2.

The automatic processing of the rule-based algorithm allows one to analyze a quite large search space, in order to obtain the arrangement determining the minimum volume/weight: the filter volume ranges from 13.88 cm^3 up to 6591 cm^3 and from 5.46 cm^3 up to 6135.84 cm^3 in the worst configuration, respectively, for case study #1 and #2.

The proposed automatic design algorithm stores data related to all feasible configurations. Therefore, it also allows one to perform extra analyses which are not possible with a manual design procedure. In particular, it allows one to compare the best EMI filter design to the suboptimal results: thus, the final choice is left to the designer; moreover, it is possible to evaluate whether an extra safety margin can be obtained whilst maintaining the same optimal value of the objective function.

Table 4. Filter design output data–case study #2.

	Conventional Design	**Automatic Design**
Number of Stages	1	2
L_{CM}@10 kHz	0.8 mH	56 µH (each stage)
CM inductor core dimensions (mm × mm × mm)	27.9 × 13.6 × 12.5	14.1 × 6.6 × 6.3 (each stage)
CM core A_L@10 kHz	65.5 µH (Vitroperm 500F, model T60006-L2025-W380)	28 µH (Vitroperm 500F, model T60006-L2012-W902) (each stage)
Number of turns per CM winding	5	2 (each stage)
C_{CM}	200 nF	100 nF (each stage)
C_y	100 nF, ceramic, 250 V, (Murata RDER72E104K2)	47 nF, ceramic, 250 V, (Murata RDER72E473K2) (each stage)
L_{DM}@10 kHz	1.6 µH ($L_{leakage}$ = 0.2% L_{CM})	459 µH (Extra L_{DM}) (each stage)
DM inductor core dimensions (mm × mm × mm)	n.a.	11.2 × 5.1 × 5.8 (two for each stage)
DM core A_L@10 kHz	n.a.	25.5 µH (Vitroperm 500F, model T60006-L2009-W914) (2 for each stage)
Number of turns per DM winding	n.a.	3 (each stage)
C_{DM}	47 µF, electrolytic, 400 V, (Panasonic EEUEE2G470)	33 nF, polypropylene, 560 V, (Kemet 46KF23301P02) (each stage)
Wire size	15 AWG	21 AWG
Volume	25.87 cm^3	9.88 cm^3 (all stages)
Weight	44 g	14.42 g (all stages)

Figure 6 shows the distribution of the 100 best designs around the first best configuration selected by the algorithm. It can be observed that, in the first case study, a relevant number of EMI filter designs are without extra *DM* inductors. Instead, in the second case study, the low value of the operating current reduces the likelihood of saturation of the magnetic core in the *DM* section design procedure; therefore, the configurations with extra *DM* inductors are more numerous, as shown in Figure 6b.

Moreover, the automatic design procedure has been repeated considering fixed input parameters and only increasing the *CM* attenuation value, starting from the minimum required value. The following range has been swept:

- [30, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 52, 54, 56] dBµV in case study #1;
- [25, 30, 35, 40, 45, 50, 55, 60, 65] dBµV in case study #2;

The obtained results for both volume and number of stages are shown in Tables 5 and 6. It can be noted that in both cases, the *CM* attenuation of the filter can be risen to an extra 10 dBµV safety margin without increasing the design volume. As a consequence, a better filter performance can be obtained, balancing the unavoidable non-idealities in the filter realization.

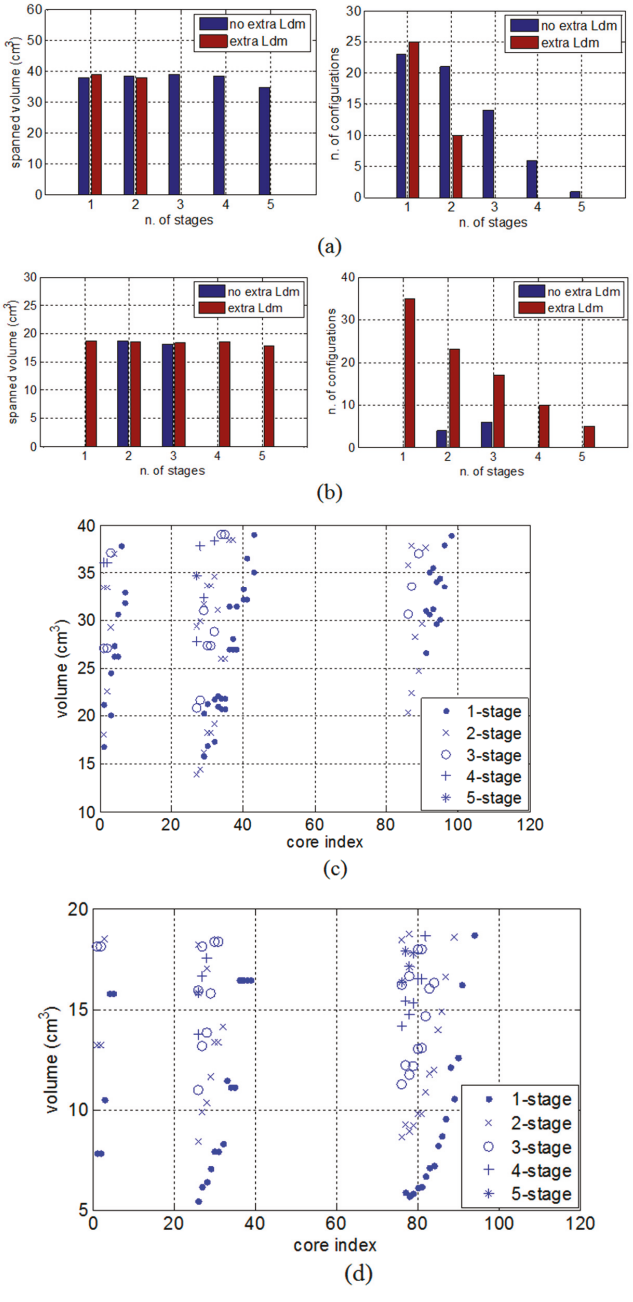

Figure 6. Scatter plot and distribution of the best 100 configurations in case study #1 (**a**,**c**) and in case study #2 (**b**,**d**).

Table 5. Volume and number of stages of the best design depending on the required *CM* attenuation–case study #1.

CM Attenuation (dBμV)	Number of Stages	Volume (cm^3)
30	2	13.88
32	2	13.88
34	2	13.88
36	2	13.88
38	2	13.88
40	2	13.88
42	1	15.8
44	1	15.8
46	2	16.2
48	2	16.2
50	2	16.2
52	2	18.1
54	2	18.1
56	2	18.3

Table 6. Volume and number of stages of the best design depending on the required *CM* attenuation–case study #2.

CM Attenuation (dBμV)	Number of Stages	Volume (cm^3)
25	1	5.46
30	1	5.46
35	1	5.46
40	1	6.19
45	1	6.94
50	1	7.79
55	2	8.43
60	2	8.43
65	2	9.88

In the end, EMI measurements have been carried out in case studies #1 and #2 without any filter, with the conventionally designed filter, and with the automatically designed filter, to assess the filter mitigation performance.

The obtained filters show a good behavior since the filtered EMI meets the limit imposed by the standard under consideration, as shown in Figure 7. Despite the achievement of a higher compactness and power density, the proposed EMI filter design method enables compliance with the reference standard of the power electronic system under consideration, without a significant computational effort.

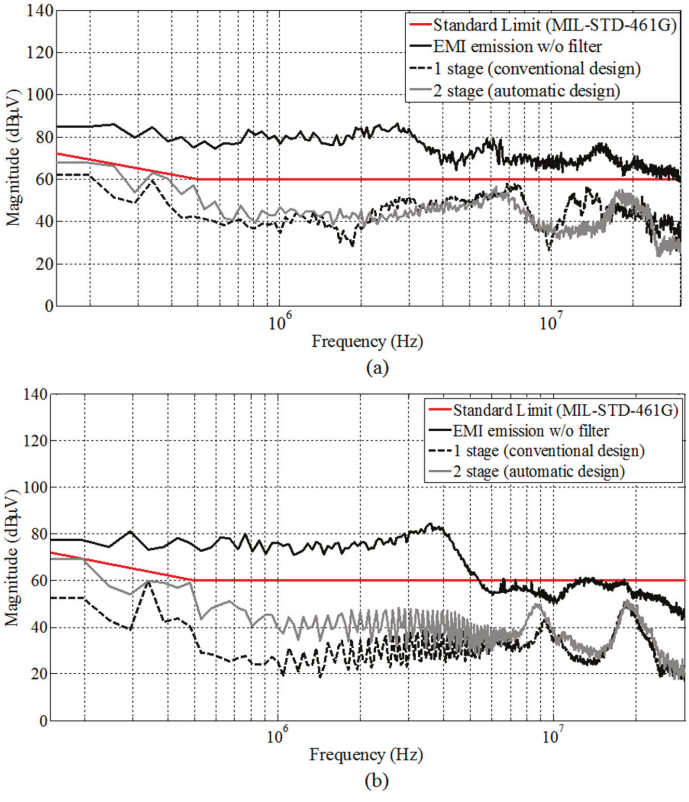

Figure 7. Measured EMI with and without EMI filters (**a**) case study #1; (**b**) case study #2.

5. Conclusions

This work proposes an automatic design procedure oriented at obtaining high performing EMI filters with the minimum volume/weight.

The design procedure relies on a suitably devised rule-based algorithm and on databases of magnetic cores, capacitors, and conducting wires suitably selected among those offered by the market. It takes as inputs some relevant parameters that are evaluated from noise measurements and others defining the system arrangement. It outputs the best filter components in terms of performance, volume, and weight. Furthermore, the design procedure allows one to compare the most suitable EMI filter design to the suboptimal results, thus allowing the designer to have a final choice on the configurations to be selected. All the design steps, options, outputs, and design-related additional analyses are handled by the rule-based algorithm without a relevant computational effort. The proposed procedure has been experimentally validated in two case studies, both in terms of performance and increased power density. In addition to the compliance of the power electronic system under study with the reference standard, it has allowed us to achieve EMI filters with a considerable power density and higher compactness if compared with the conventional design.

In particular, an EMI filter size comparison has been carried out, obtaining a reduction of about 56% in weight and about 46% in volume in the first case study, and of about 67% in weight and about 62% in volume in the second case study.

Author Contributions: Guido Ala, Maria Carmela Di Piazza, Graziella Giglia, and Gianpaolo Vitale conceived the research activity; Graziella Giglia and Pericle Zanchetta gave advice on the filter design strategy; Guido Ala, Maria Carmela Di Piazza, and Gianpaolo Vitale conceived the proposed design procedure; Graziella Giglia and Massimiliano Luna performed the software implementation of the rule-based algorithm; Maria Carmela Di Piazza, Massimiliano Luna, Graziella Giglia, and Gianpaolo Vitale devised the test bench; Guido Ala, Giuseppe Costantino Giaconia, and Graziella Giglia contributed to the layout and the measurement set-up; Graziella Giglia performed the filter design and experimental tests; Guido Ala, Maria Carmela Di Piazza, Graziella Giglia, Massimiliano Luna, and Gianpaolo Vitale analyzed the experimental results; Guido Ala, Maria Carmela Di Piazza, and Graziella Giglia wrote the manuscript. All the authors revised and approved the final manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

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Article

4T Analog MOS Control-High Voltage High Frequency (HVHF) Plasma Switching Power Supply for Water Purification in Industrial Applications

T. N. V. Krishna [1,†], P. Sathishkumar [1,†], P. Himasree [1], Dinah Punnoose [2], K. V. G. Raghavendra [1], Himanshu [1], Bandari Naresh [1], R. A. Rana [1] and Hee-Je Kim [1,*]

[1] School of Electrical Engineering, Pusan National University, Busandaehak-ro 63 beongil 2, Busan 46241, Korea; vamsik.tirumalasetty@gmail.com (T.N.V.K.); sathishnano2013@gmail.com (P.S.); himabindu1685@gmail.com (P.H.); raghavendra999@gmail.com (K.V.G.R.); himanshuhimanshu820@gmail.com (H.); naresh1.bandari@gmail.com (B.N.); ronak.eleindia@gmail.com (R.A.R.)

[2] Department of Computer Science and Engineering, Hindusthan Institute of Technology and Science, Chennai 603103, India; dinahpunnoose@gmail.com

* Correspondence: heeje@pusan.ac.kr; Tel.: +82-51-510-2364

† Both authors equally contributed to this work.

Received: 7 September 2018; Accepted: 8 October 2018; Published: 11 October 2018

Abstract: High-power plasma power supply is very useful for many industrial and medical applications. Plasma is generated artificially in the laboratory or industry by applying the electric or magnetic field. In this manuscript, we presented the simple 4T analog MOS control high voltage high frequency inverter circuit as a plasma power supply using modulation index technique. The presented plasma power supply operated at 25 kHz frequency and 10 kV peak to peak voltage. It generates a 0 V to 10 kV controllable electric field. The generated electric field is applied and produces plasma, which can be used for many industrial applications. A 10 kV to 5 kW plasma power supply has been practically developed based on the proposed topology and experimentally tested and, additionally, excellent output power conversion efficiency is achieved. From these results, the 4T analog MOS control high voltage high frequency (HVHF) plasma switching power supply is verified.

Keywords: 4T analog MOS control; high frequency switching power supply; water purification; modulation index

1. Introduction

Plasma is an ionized gas, into which sufficient energy is provided to free electrons from atoms or molecules. It sometimes allow species, ions, and electrons to coexist [1]. The most important thing is that plasmas are the high common state of matter in the universe and even on earth. Plasma is a gas that has been energized to the point that some of the electrons break free from, but travel with, their nucleus. Gases can become plasmas in several ways, but all include pumping the gas with energy. A spark in a gas will create plasma. Plasma is an electrically inoffensive medium of unbound positive and negative particles. Although they are not 'free' in the sense of not experiencing forces. Moving charged particles generate an electric current within a magnetic field, and any movement of a charged plasma particle affects and is affected by the fields created by the other charges. In turn, this governs collective behavior with many degrees of variation [2,3].

Basically, plasma is generated artificially in the laboratory or industry by the application of an electric or magnetic field through a gas. Although there are several means for plasma generation, in all cases, there must be a plasma power source to produce and sustain it [4]. Plasma can apply a voltage, and subsequently ionization can occur, as shown in Figure 1, which presents a discharge tube as a

simple example. The potential difference and subsequent electric field pull the bound electrons toward the anode, while the cathode pulls the nucleus [5]. As the voltage is increased, the current stresses the material by increasing electric polarization. Once the polarization exceeds the dielectric limit, electrical breakdown occurs, where the material transforms from being an insulator to a conductor. The underlying fundamental process is called an avalanche, where collisions between electrons and neutral gas atoms produce more ions and electrons.

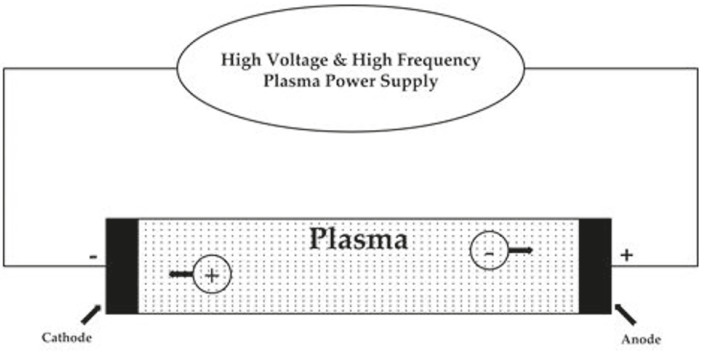


Figure 1. Simple representation of plasma discharge tube.

Plasma requires high voltage high frequency (HVHF) switching power supply as a source. HVHF is being used for many industrial applications [6–8], such as water purification, static charge removers, fluorescent tubes, plasma arc welding, plasma cutting, textiles, surface modification [9,10], biomedical applications [11–13], plasma displays, radicals, plasma needles [14], corona discharges [15], medical applications, and ozone generators [16]. Medical uses are an exciting new area for plasma applications that can be used in the treatment of diseases and cancer. In essence, the ozone generator is used for sterilization [17] and imprinting plastic and metal items, and involves the ionization of air. Ozone is produced in nature in two ways: corona discharge and ion propulsion method. A corona discharge in nature is called a lightning strike caused by a high voltage DC discharge of electricity. Ion propulsion is another interesting method in near future plasma applications, because it allows spacecraft to travel vast distances.

Various power sources, such as DC, RF, and microwave, are being developed in laboratories and industries to generate electrical current by applying very high voltage high frequency electric fields through a gas. On the other hand, the operation of plasma sources has different requirements according to the applications. Therefore, in most cases, to match with the application requirements, different voltages and different frequency pulsating DC systems are being developed for generating required electric filed to produce electric current. In the present study, a high voltage high frequency plasma power supply was presented, which produces the essential plasma source for water purification in industrial applications [18–20]. In this design, we use a modulation index technique that controls the amplitude and frequency.

According to review [21], Weltmann and Woedtke designed the plasma source for sterilizing medical devices. They developed a high voltage and high frequency plasma source using a pulsed sinusoidal voltage of 10 kV/20 kHz. A high voltage and high frequency power supply was designed for an ozone generator, which is one of the plasma applications, for use in air and water disinfection [22]. This laboratory-built power supply using a high voltage ferrite transformer and a PLC microcontroller was used to energize a dielectric barrier discharge ozone generator. Cui jiuxia et al. designed a high voltage power supply for electro curtain applications [23]. The developed circuits achieved a high power factor, high efficiency, rapid fault response, and low ripple systems. For plasma torch applications, a high power converter circuit was designed, including a rectifier and filter system,

and a converter circuit was designed using ferrite material with high frequency and output voltage with a rapid time [24]. For plasma immersion ion implantation applications, they designed pulsed modulators with a high voltage system. A PLC-based pulse modulator and PLC driving system is presented, and the PLC system is very powerful for optimizing ion-implantation. The protection circuit was also designed for short circuits [25]. The other proposal is for surface treatment by plasma immersion ion implantation. This design consists of three basic circuits: pulse forming network, hard-tube pulsar, and Blumlein line [26].

The authors of [27] demonstrate the advantages of parallel and series configuration of flyback converters for pulsed power applications. Thus, the concept is to increase the voltage level and rise time of the generated pulses while emphasizing the modularity concept. There are two kinds of experimental sections that occured, one is 4 kV output voltage and other is 20 kV output voltage, while the repetition rate of frequency is 1 kHz. On other hand, the authors of [28] demonstrate how the proposed topology operates independently from the load while preserving high repetition rate. The control algorithm is designed in a way that it can prevent from any possible faults and protect the system from the over-voltage. The designed system is between 1 kV and 3 kV with different circumstances. We presented high voltage high frequency plasma power supply with 10 kV, 5 kW, and 25 kHz; repetition rate of frequency is high. We presented both voltage and current protection circuits to prevent the system from having any issues. Mainly, this plasma power supply presents the line regulation circuit to maintain a stable output regardless of changes in the input voltage, load, or connected device.

In the work of [29], the experimentations have been conducted based on a high-voltage DC power supply and a high-voltage pulse generator for point-to-point and point-to-plane geometries. In addition to the employed geometry, the ambient also plays an important role on electric field formation. Thus, the electric field distribution was simulated for both aforementioned geometries in air–water medium. In this case, the high electric field strength for both geometries appears across the point electrode. This is because of the fact that the water conductivity makes the electric field distribution for both geometries almost similar. Here, the water conductivity was selected to be 200 μS/cm, the same as the tap water used in the experimentation phase. In this research paper, gas can produce an electric or a magnetic field in plasma. We presented the plasma power supply with 10 $kV_{p\text{-}p}$, which is applied to the plasma load for water purification. The pros of the design are simplicity, cost-efficiency, and quick purifying of the water. The cons of the system are heat, explosion risk, and its time-consuming nature.

The plasma has requirements based on the applications. For example, the helicon plasma will work at 13.56 MHz with radio frequency levels up to 120 kW; microwaves at 28 GHz, which requires up to 30 kW; and ion cyclotron heating operates at 7–9 MHz, which will work until 30 kW [30]. This paper presented a fully analog-controlled high voltage high frequency (HVHF) plasma switching power supply. The developed HVHF topology applies for water purification in industry. Water purification is the kind of removing dust particles, undesirable chemicals, suspended solids, and gases from water. The goal is to produce water for a specific purpose. Most water is disinfected for human consumption, but water purification may also be designed for a variety of other purposes, including fulfilling the requirements of medical, pharmacological, chemical, and industrial applications.

There are some plasma technologies that are regularly used for water purification, such as ozone, electron beam, and electrical discharge. We presented the electrical discharge technique, which generates ions and electrons with very high energy as active species. The active species will remove the dust particles and unwanted waste particles. Because of their physical and chemical properties, the substantial amount used for the electrodes affects the chemical process of plasma in water, necessitating a study of difference in electrode substantial in plasma discharge used in organic solution removal. The objective of this work is explained on water purification by plasma technology has been presented and experimentally verified. A plasma power supply with an output voltage of 10 kV was connected to the plasma load to start the electrical discharge. In this design,

the input of 200 V AC to 240 V AC is applied to the plasma power supply and will generate 10 kV_{p-p} alternating current. This high voltage of AC is connected to the plasma load, which is applied to the water. The effects of variable modulation index on the total harmonic distortion (THD) content of the resulting inverter output are studied.

The 10 kV, 5 kW presented 4T analog MOS control HVHF plasma switching power supply was developed in the laboratory and a generated high frequency electric field was applied, which produces the required electric power for plasma. Section 2 presents a detailed explanation of the HVHF power supply, which is a combination of diode bridge rectifier, high voltage and high frequency PWM inverter, high frequency transformer, filter design, and line-regulation. The modulation technique is explained in Section 3. The experimental setup of the HVHF power supply and practical work are reported in Section 4. The experiment results and discussion on the HVHF with the power conversion efficiency of design are presented in Section 5. Finally, Section 6 reports the conclusions on research and development of the system.

2. High Voltage High Frequency Plasma Power Supply

The block diagram of the HVHF plasma switching power supply is shown in Figure 2. A single phase AC source was applied as the input to the designed power supply. A diode full bridge rectifier circuit was designed as the initial stage of the plasma power supply. The circuit rectifies the 220 V AC voltage to DC output voltage [31–39], which can be adjusted from 0 V to 300 V. A high frequency inverter circuit was designed and located, following by the rectifier DC link capacitor, which receives the DC voltage from the rectifier and converts it to a high frequency pulsating DC output voltage. The full-bridge PWM topology with high switching frequency was developed as an inverter circuit for the designed plasma power supply. A high voltage and high frequency transformer was designed and placed at the output of the inverter side. The high frequency pulsating DC output was connected to the primary side of the transformer. The transformer was designed with a ferrite PL-13 U core that could transform 290–300 V to 10 kV high voltage. The secondary side of the transformer that transformed the high voltage was connected to the plasma source, which was designed with titanium, quartz tube, and metal.

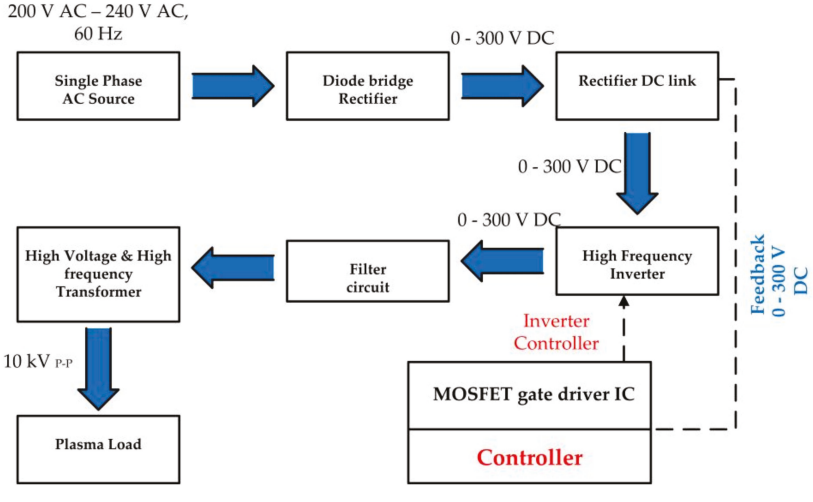
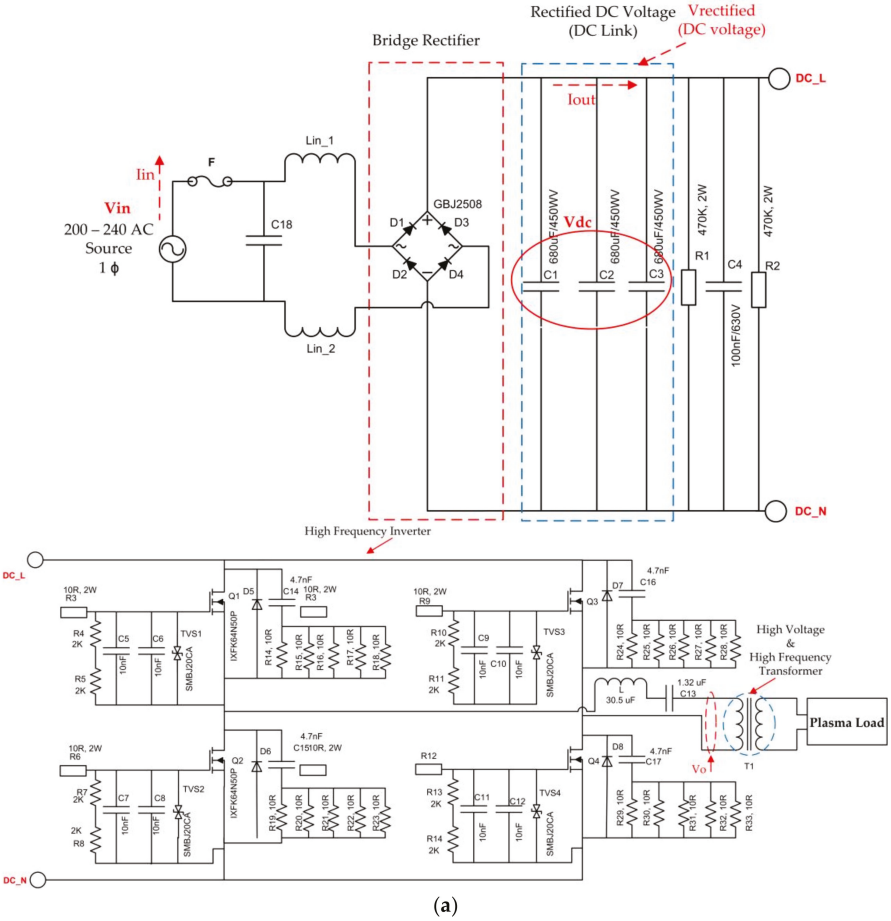


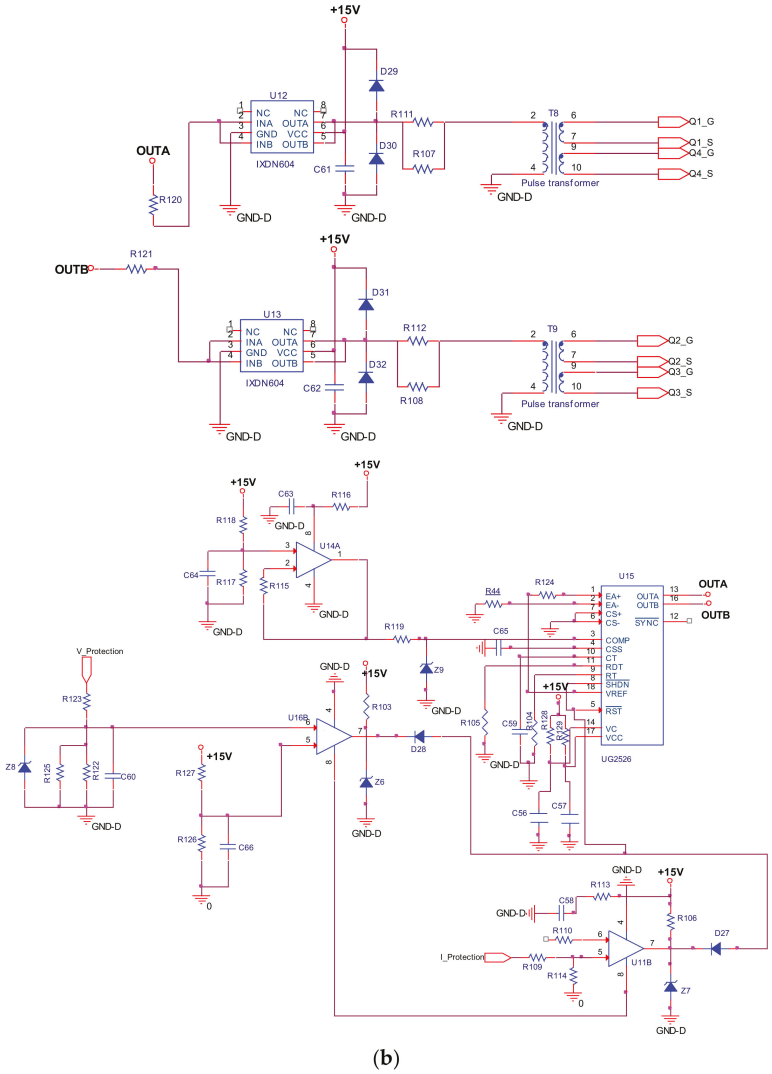
Figure 2. Block diagram of the high voltage high frequency (HVHF) plasma switching power supply.

Figure 3 shows the schematic diagram of 4T analog MOS control plasma switching power supply. The single phase AC voltage was applied to the circuit. The GBJ2506 bridge rectifier was used along with the DC link capacitors. The designed rectifier full bridge consisted of four diodes that were arranged as shown in Figure 3.



(**a**)

Figure 3. *Cont.*



(**b**)

Figure 3. Schematic diagram of 4T analog MOS control HVHF plasma switching power supply. (**a**) Power circuit of HVHF plasma. (**b**) MOSFET driver circuit of the PWM inverter.

2.1. High Voltage High Frequency PWM Inverter

A high switching frequency high power PWM inverter circuit was designed and placed followed by the rectifier of the plasma power supply, as shown in Figure 3. The IXFK64N50P MOSFET was used as a switching device in the PWM full bridge inverter. The chosen MOSFET allowed a 500 V and 64 A maximum. This has a lower drain source resistance (85 m ohms) and fast intrinsic diode. An inverter driver circuit was designed along with a regulating pulse width modulator IC (UC2526) to operate the full bridge PWM inverter as shown in Figure 3b. The driver circuit generates two complementary PWM signals operating at 25 kHz with a 0.5 µs dead band. The MOSFET driver IXDN604SIA is dual high speed gate drivers are especially well suited for driving the MOSFETs and IGBTs. Each of the two outputs can source and sink 4 A of peak current while producing voltage rise and fall times of less than

10 ns. The input of each driver is virtually immune to latch up, and proprietary circuitry eliminates cross conduction and current shoot through. The pulse width modulator IC UC2526 is designed for fixed frequency. When the Q1, Q4 MOSFET switches ON and the Q2, Q3 MOSFET switches off, a positive DC voltage is obtained at the output. When the Q2, Q3 MOSFET switches ON and the Q1, Q4 MOSFET switches off, a negative DC voltage is obtained at the output. The MOSFET switches are switched alternately with a controlled duty ratio to convert input DC voltage into high frequency AC voltage suitable for exciting the plasma load. The PWM driver circuit was designed using 4 A dual low side ultrafast MOSFET drivers (IXDN604SIA). The 25 kHz inverter circuit can generate up to a 640 V peak to peak square wave voltage. The designed plasma power supply consisted of an over voltage, over current, and over temperature protection circuit. These protection circuits shut down both the phase controller and PWM controller in any unusual circumstances.

The switching sequence is designed so that switches Q1 and Q4 are ON for the time duration $0 \leq t \leq T_1$ and switchs Q2 and Q3 are ON for the time duration $T_1 \leq t \leq T_2$. When switch Q1 and Q4 are turned ON,

$$\mathrm{Vout} = \frac{\mathrm{Vi}}{2} \tag{1}$$

When switches Q2 and Q3 only are turned ON,

$$\mathrm{Vout} = -\frac{\mathrm{Vi}}{2} \tag{2}$$

The waveform of the output voltage and switch currents for a load are shown in Figure 1.

The rms value of the output voltage is Vout is

$$\mathrm{Vout,\ rms} = \frac{1}{\mathrm{T1}} \int_0^{\mathrm{T1}} \frac{\mathrm{V_i^2}}{4} \mathrm{dt} = \frac{\mathrm{Vi}}{2} = \frac{Vi}{2} \tag{3}$$

The instantaneous output voltage (Vout) is rectangular in shape. The instantaneous value of Vout can be expressed in Fourier series as follows:

$$\mathrm{Vout} = \frac{\mathrm{a_0}}{2} + \sum_{\mathrm{n=1}}^{\alpha} \mathrm{a_n} \cos(n\omega t) + \mathrm{b_n}\ \sin(n\omega t) \tag{4}$$

As a result of the quarter wave symmetry along the time axis (Figure 4d), the values of a_0 and a_n are zero. The value of b_n is given by

$$\mathrm{b_n} = \frac{1}{\pi} \int_{-\frac{\pi}{2}}^{0} -\frac{\mathrm{Vi}}{2}\, \mathrm{d}(\omega t) + \int_0^{\frac{\pi}{2}} \frac{\mathrm{Vi}}{2} \mathrm{d}(\omega t) = \frac{2Vi}{n\pi} \tag{5}$$

Substituting the value of b_n from Equation (5) into Equation (4),

$$\mathrm{Vout}\ = \sum_{\mathrm{n}\ =1,3,5\ldots}^{\alpha} \frac{2\mathrm{Vi}}{n\pi} \sin(n\omega t) \tag{6}$$

The current through the load (iL) is given by

$$\mathrm{iL} = \sum_{\mathrm{n=1,3,5\ldots}}^{\alpha} \frac{1}{\mathrm{R}} \frac{2\mathrm{Vi}}{\mathrm{n}\pi}\ \sin(\mathrm{n}\omega t) \tag{7}$$

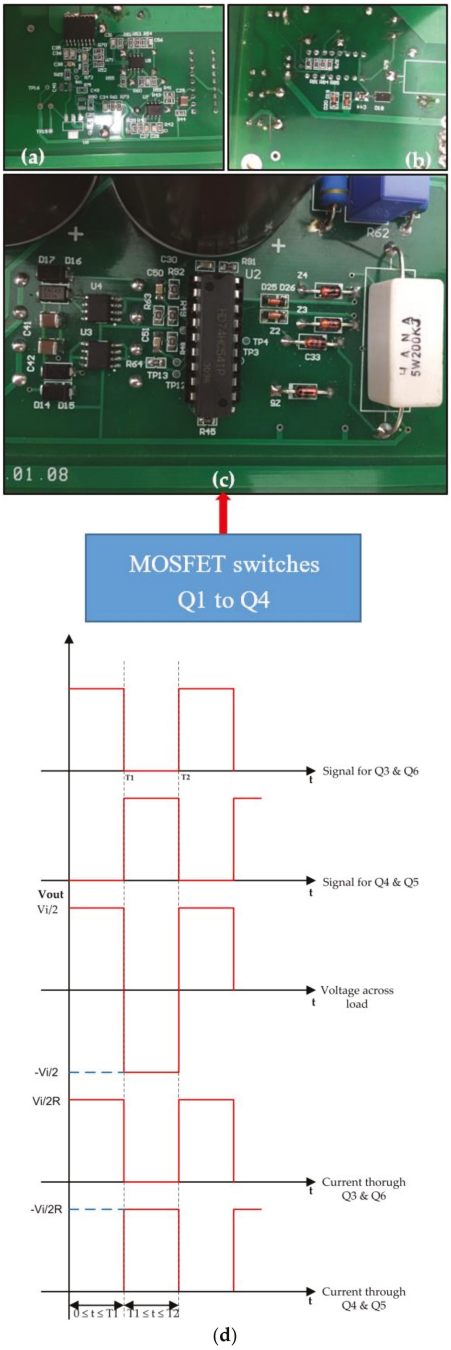


Figure 4. HVHF plasma power source driver and protection circuits. (**a**,**b**) Voltage and current protection circuit; (**c**) MOSFET driver circuit; (**d**) current and voltage waveforms of PWM inverter.

2.2. Filter Design

This filter contains two components. An inductor connected in series with the capacitor, which is why this low pass is also referred to as an LC low pass filter. The primary side of transformer voltage Vo is employed parallel to the capacitor. The output frequency of the plasma power supply is 25 kHz. The inductor L is more approachable to the surge of frequency. As the frequency rises, the inductive reactance of the coil X_L increases, while the capacitance X_C of the capacitor drops.

The formula for computing the LC filter is

$$\mathrm{LC} = \frac{1}{1 - \omega^2 LC} \tag{8}$$

In this design, L is the inductor and C is the capacitor.

The inductive resistance X_L rises with frequency while the capacitive reactance X_C is inversely proportional to it and it falls down as the frequency increases. The cutoff frequency is the frequency at which $X_C = X_L$. Thus, at a frequency greater than the cutoff frequency, X_C is less than X_L. At a lower frequency, X_C is greater than X_L.

The cut-off frequency is

$$\mathrm{fc} = \frac{1}{2\pi\sqrt{LC}} \tag{9}$$

The L–C Circuit Damping Method

The loads connected to the PWM inverter circuit may damage the L–C filter circuit by providing some damping. The load effects on the L–C filter can be enlightened from the energy point of view.

The voltage (and current) that spins around inside L–C circuits can be greater that the initial voltage that 'kick starts' the alternating capacitor charge and discharge and inductor 'discharge and charge' (via its magnetic field). In an inductor, the voltage across it is proportional to the rate of change of current flowing through it.

Or

$$\mathrm{V} = L \times \left(\frac{d(I)}{dt}\right) \tag{10}$$

The constant of proportionality, *L*, is the inductance that we associate with the coil. Thus, a rapidly discharging capacitor connected in parallel with the inductor can increase voltage level higher than the initial voltage across the capacitor.

2.3. High Voltage High Frequency Transformer

A high voltage high frequency step-up transformer [40] was designed in the laboratory, as shown in Figure 5. The transformer step-up the inverter output voltage to a 10 kV peak to peak voltage and achieve galvanic isolation. A 100 nf capacitor is connected as a high pass filter between the inverter output and the primary winding of the high voltage transformer. It obtains the sine wave current waveform from the square wave voltage. The secondary side of the transformer output was connected to a quartz tube (plasma source), which was made of metal and titanium. The three high voltage capacitors were connected in parallel as a DC link with a value of 2040 μF, 450 V.

The necessity of the transformer is mainly for a high voltage value at the secondary side, a specific shape for industrial applications. The high voltage high frequency transformer was designed for the plasma power supply, and has the following electrical specifications: output voltage Vout = 10 kV; output power Pout = 5 kW. As per design, high switching frequency will decrease the height and size of the transformer. However, further reduction by higher frequency switching cannot be achieved because of the insulation requirement. The natural resonant frequency of the high voltage transformer is also a restriction. Additionally, high frequency switching will require high driving power. As a compromise, fs = 25 kHz is selected as the switching frequency.

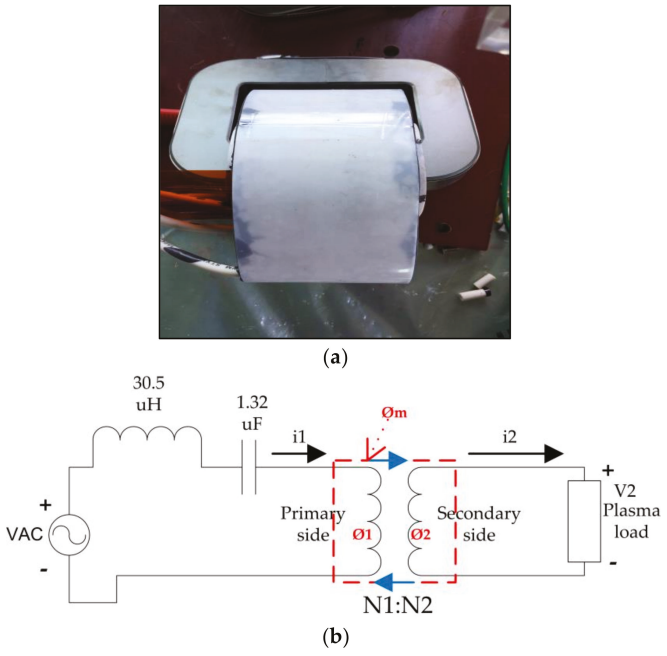


Figure 5. (**a**) High voltage high frequency transformer; (**b**) transformer equivalent circuit.

2.3.1. Turns Ratio

The DC link voltage is approximately 300 V DC, which is obtained by the rectifier. The output voltage is 10 kV. So the output–input ratio should be 33.33. Both the turn's ratio of the transformer and plasma power supply contribute to the final voltage boost. Thus, in practice, the step-up coefficient of the plasma power supply is used as design margin and the turn's ratio of the high voltage transformer is selected as 33.33.

2.3.2. Magnetic Selection

Power ferrites are employed as the magnetic material due to the high resistivity and low eddy current losses under high frequency. PL-13, UU120 is designated to accommodate the big winding turns and to fulfill the insulation requirement.

The turn's number of the primary and the secondary side winding, n1 and n2, can be calculated by (11) and (12), respectively, which yields n1 = 23, n2 = 770.

$$n1 = \frac{Vi \times 10^4}{4Bmax\ Ae\ Fs} \tag{11}$$

$$n2 = 33.33 * n_1 \tag{12}$$

2.3.3. Wire and Wiring Design

The secondary winding plays a main role in the output voltage side. In practice, the secondary winding is wounded into five slots, each slot contains five layers. This assembly can limit the voltage across each slot and decrease the layer-to-layer voltage. Primary side used Ritz wire and secondary side high voltage Copper wire is used and results in a small leakage inductance. Considering the skin effect and the current value, the wire specifications and the current density are as follows: primary

winding—0.2 mm Ritz wire, 3 A/mm^2; Secondary winding—AWG16 high voltage cable copper wire, 1 A/mm^2.

Primary and secondary windings have resistances, which means that the source voltage VAC is not the same as the induced primary voltage e_1; that is, VAC $\neq e_1$. Similarly, $V_2 \neq e_2$. The source voltage of primary side of transformer is coming from inverter output side. In deriving the equivalent circuit for the two-winding transformer of Figure 5b, the characteristics of an actual transformer described earlier need to be modeled.

Consider the primary circuit. A voltage equation around the loop may be written as

$$\mathrm{VAC} = \mathrm{R1i1} + \mathrm{N1}\frac{\mathrm{d}\lambda 1}{\mathrm{dt}} = \mathrm{R1i1} + \mathrm{N1}\frac{\mathrm{d}Ø1}{\mathrm{dt}} \tag{13}$$

where

R1 is the resistance at the primary side
N1 is the number of primary windings

2.4. Advantages and Disadvantages of the Circuit

Advantages:

- The power supply circuit has a smaller size.
- It is lightweight.
- It has excellent power conversion efficiency from 75% to 85%.
- This design has high output range.
- Less heat produced in plasma power supply design.
- Simple application.

Disadvantages:

- This design has only one output range.
- It causes harmonic distortion.
- High frequency noise.
- More complex.

3. Modulation Technique

There are some differences between amplitude modulation index and frequency modulation index. The deviations of amplitude modulation index are values used are 0.3 to 1.0 with 0.1 increments. The reference frequency signal f_r describes the inverter output frequency, with its peak amplitude and control the modulation ratio m_a. The PWM inverter has constant DC input for generating certain frequency. The modulation index m_a, also known as the amplitude modulation ratio, is well-defined as (14) [41–43].

$$m_a = \frac{\mathrm{Vr}}{\mathrm{Vc}} \tag{14}$$

The variation of m_a can be produced by changing in the modulation signal. The effect of m_a on the total harmonic distortion (THD) of the inverters are illustrate in Table 1.

In addition, the results of a single phase PWM inverter are illustrated in Figure 3 respectively. The effect of modulation index on THD of the inverter before using a filter is given in Table 1. It can be seen that the least value of THD equals 2.08% is at modulation index m_a equals 0.9.

The outcome of a filter on the THD and the output voltage waveform are presented in Figure 6 respectively.

Table 1. Effect of modulation index on total harmonic distortion (THD) of the PWM inverter before using filter.

m_a	THD%
0.3	7.45%
0.4	9.74%
0.5	5.13%
0.6	6.03%
0.7	3.37%
0.8	3.42%
0.9	2.08%
1	2.81%

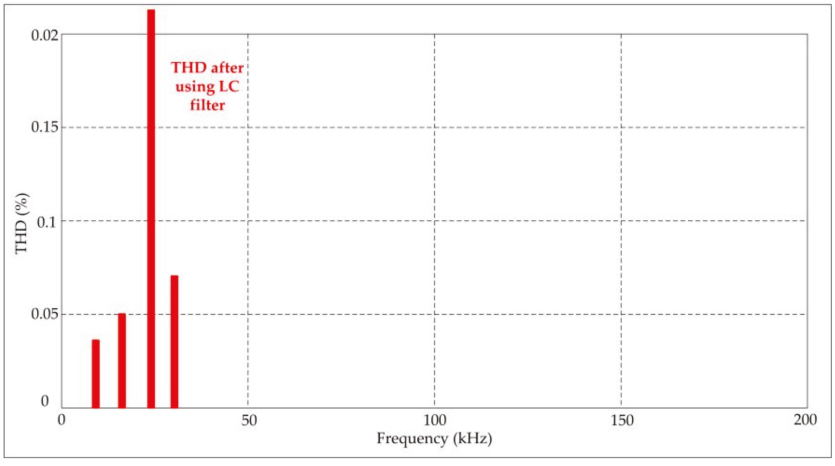


Figure 6. Effect of total harmonic distortion (THD) frequency modulation index.

4. Experimental Setup

The proposed HVHF plasma power supply was verified by operating the 5 kW plasma source in a laboratory. The single phase 220 V AC, 60 Hz grid power was applied as an input to the HVHF switching plasma power supply. A variable AC source, which can vary the input voltage up to 240 V AC, was used to verify the input saturation. As illustrated, this switching power supply is based on PWM inverter topology. This topology uses a high voltage high frequency step-up transformer to boost the voltage up to 10 kV peak to peak. The low pass LC filter was connected in series with the primary side of the transformer to achieve a sine wave current from pulsating DC voltage. The repetition rate is can be used to adjust the power and to obtain high frequency sine waveform. The repetition rate is set to 25 kHz to generate symmetrical waveform and avoid transformer saturation. The plasma power source as a load for 10 kV, 5 kW high power systems, which was designed using metal and titanium.

Here, high voltage MOSFET (IXFK64N50P) is used as power switches. IXDN604SIA gate drive modules are used to drive the MOSFETs and provide the necessary isolation between the switching signal ground and the power ground. Table 2 presents the HVHF switching plasma power supply specifications.

Table 2. The 10 kV, 5 kW PWM inverter for plasma power source design specification.

Parameter	Ratings
Input voltage	200 V AC–240 V AC
power	5 kW
Output voltage	10 kV_{P-P}
Switching frequency	25 kHz
DC link capacitor	2040 μF

5. Results and Discussion

The HVHF plasma switching power supply design and workings are discussed below based on the experimental results. The experiments are made by applying output voltage 10 kV peak to peak. To verify the circuit, the experiments were carried out with a variable AC voltage and different input power.

Figure 7 shows the shows the DC voltage converted from the single phase AC sine wave with different input power.

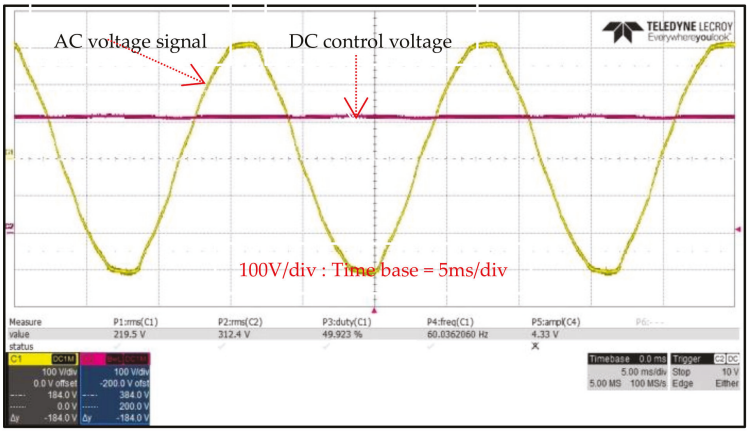


Figure 7. Full wave bridge rectifier resultant output waveform.

The high frequency PWM inverter output waveforms and gate signals are shown in Figure 8. The inverter output and high frequency square wave voltages were obtained from the DC input voltage from the bridge rectifier circuit. Figure 8a shows the two complementary 50% duty cycle PWM signals produced by the analog PWM controller. The two complementary PWM control signals synchronized with each other and consist of dead band, which avoids short circuit in full bridge. The controlled PWM signals were applied to the gate terminal of the MOSFET switches to switch the MOSFET on and off. Figure 8b presents the output voltage of inverter waveforms at various input voltages and Figure 8c presents output current waveform (5 A/div) of the inverter, respectively.

Figure 9 presents the HVHF plasma switching power supply output waveforms. Figure 9a shows the output voltage waveform of the transformer secondary side with the 10 kV. Figure 9b shows the output current waveform of inverter (5 A/div). The respective output current (500 mA/div) waveforms of the transformer secondary side that flow through the plasma source, as shown in Figure 9c. The output current of the inverter side was changed to a sinewave because of the series connected filter.

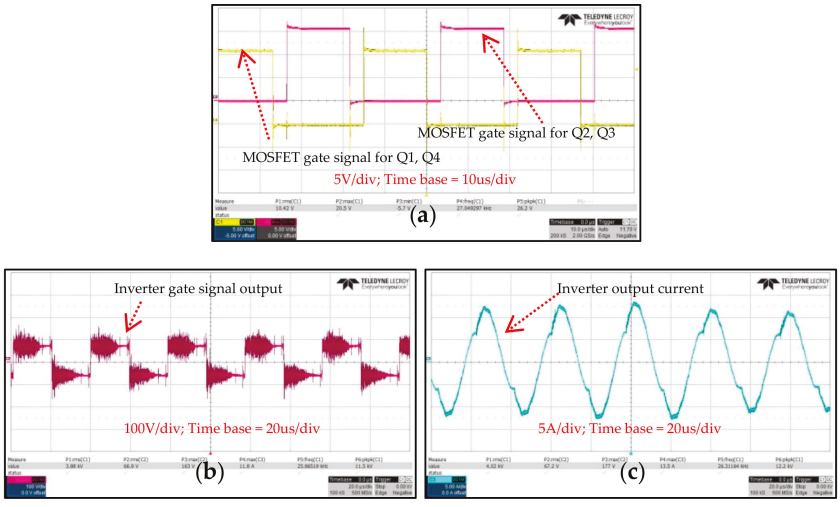


Figure 8. High frequency PWM inverter control and output waveforms. (**a**) MOSFET gate signals; (**b**) inverter gate signal output; (**c**) inverter output current.

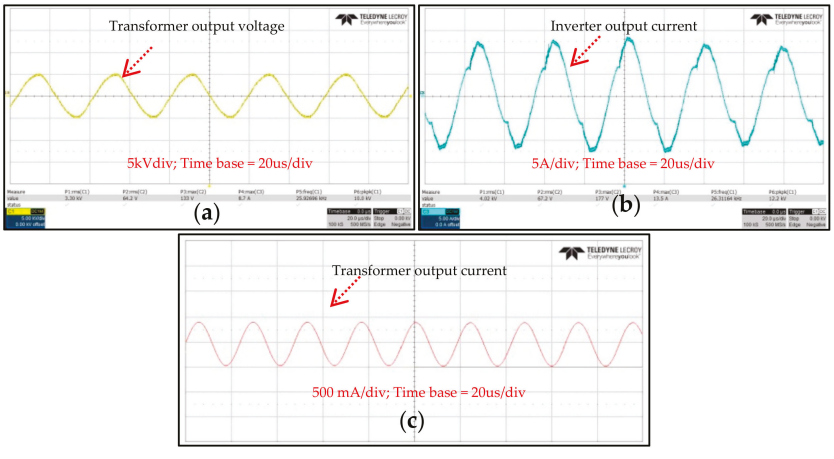


Figure 9. HVHF plasma switching power supply output waveforms. (**a**) Transformer output voltage; (**b**) Inverter output current; (**c**) Transformer output current.

Figure 10 shows the HVHF plasma power supply characteristics waveforms with and without regulation. Figure 10a presents the input voltage versus output DC controllable voltage and Figure 10b exhibits the input voltage versus output current. This comparison graph results are reported with and without regulation. When different AC input voltages were applied (200 V AC to 230 V AC) to the proposed HVHF plasma power supply, the DC output voltage also varied from 259 V to 310 V. The large saturation in output voltage will affect the plasma source and lead to damage. Therefore, a line regulation circuit was designed to avoid this saturation in the output. The low cost line regulation achieved low output changes (282 V to 291 V) for the input voltage saturation from 200 V to 240 V, as shown in Figure 10a. An output current of 407 mA to 484 mA was generated without regulation, whereas 455 mA to 472 mA was generated with regulation, as shown in Figure 10b. Therefore,

the proposed HVHF plasma power supply achieves a reliable output voltage and current for the plasma power source and assured safe operation.

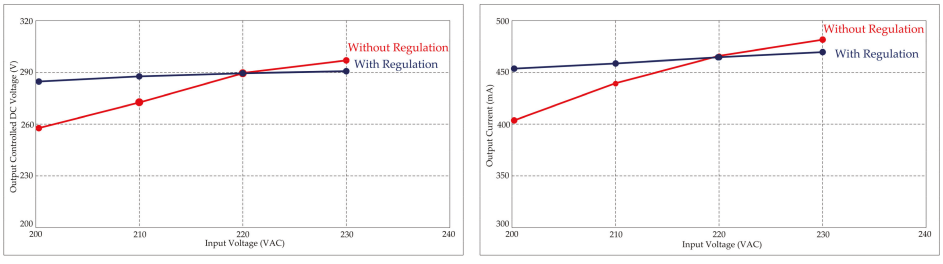


Figure 10. HVHF plasma switching power supply characteristic waveforms with and without regulation. (**a**) Input voltage vs. output DC controllable voltage; (**b**) input voltage vs. output current.

Efficiency Optimization

Figure 11 shows the power conversion efficiency. The MOSFET switches are used for high repetition rates (25 kHz), and excellent output power conversion efficiency is achieved from 75% to 85%, as shown in Figure 11. In order to examine the applied properties of the pulse generation arrangement, a set of prototypes was constructed. Basic experiments were plasma power supply design based on a topology depicted in Figure 3a (As in manuscript). The power supplied with an initial voltage is 200 VAC to 240 VAC and the DC initial voltage is 300 V DC. Capacitors were implemented using high voltage type with the value of C1 = C2 = C3 = 680 µF each. The overall the output voltage of system is 10 $kV_{p\text{-}p}$. All the electrical waveforms were recorded using Teledyne Lecroy (350 MHz, 2 GS/s). Voltage pulse was measured by Teledyne Lecroy HighVoltage probe. Current was measured by a current monitor.

The capacitance is chosen at the outside side, namely C13 = 1.32 µF. The efficiency given below was calculated on the basis of energy balance of the DC link capacitors. This was measured using the half period voltage and current product.

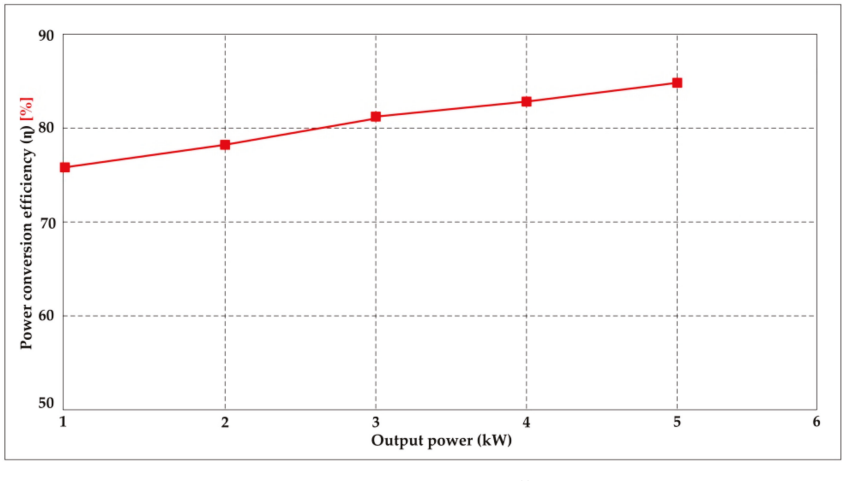


Figure 11. Power conversion efficiency.

6. Conclusions

A simple 4T Analog MOS control high voltage high frequency (HVHF) plasma switching power supply has been presented for water purification in industrial applications. The presented HVHF switching plasma power supply was controlled with fully analog control system and which is used by modulation index technique. The 10 kV, 5 kW plasma power source was designed and was used for operations for water purification in the industry. The presented plasma power supply operated at 25 kHz frequency and 10 kV peak to peak voltage. It generates 0 V to 10 kV controllable electric field. From the experimental results, the presented power supply is able to transmit 5 kW output AC power. Additionally, excellent output power conversion efficiency is achieved. This 4T analog MOS control HVHF switching plasma power supply has been practically developed based on the proposed topology and experimentally verified. The pros of the design are simplicity, cost-efficiency, quick purifying of the water. The cons of the system are explosion risk and its time-consuming nature. In future, a simple line regulation circuit with opto-isolated feedback is going to be designed for the 10 kV, 5 kW switching power supply, which comes with low cost, reliability, and high efficiency.

Author Contributions: T.N.V.K., P.S., and H.-J.K. conceptualized the idea of the research project. T.N.V.K., P.S., P.H., and D.P. designed the 10 kV, 5 kW high voltage high frequency plasma switching power supply with line regulation and protection circuit. T.N.V.K., P.S., and D.P. designed and developed the analog control and driver circuits. P.H., D.P., and K.V.G.R. developed PCB artwork for HVHF plasma power supply. H., B.N., and R.A.R. designed the high frequency transformer. T.N.V.K. and coauthors made the experimental setup and did the experiment. The data was analyzed and verified by H.-J.K. The paper was written by T.N.V.K. and P.S.

Funding: This research was supported by BK21PLUS, Creative Human Resource Development Program for IT Convergence.

Acknowledgments: This research was supported by Brain Korea 21 Center for Creative Human Resource Development Program for IT Convergence of Pusan National University.

Conflicts of Interest: The authors declare no conflict of interest.

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Review

Electrical Circuit Modelling of Double Layer Capacitors for Power Electronics and Energy Storage Applications: A Review

Immanuel N. Jiya [1,*], Nicoloy Gurusinghe [2] and Rupert Gouws [1]

[1] School of Electrical, Electronic and Computer Engineering, North-West University, Potchefstroom 2520, South Africa; rupert.gouws@nwu.ac.za

[2] Faculty of Engineering and Physical Sciences, Queen's University Belfast, Belfast BT7 1NN, UK; nicoloy@yahoo.com

* Correspondence: jiyahills@gmail.com; Tel.: +27-7206-51493

Received: 31 August 2018; Accepted: 19 October 2018; Published: 23 October 2018

Abstract: There has been increasing interests in the use of double layer capacitors (DLCs)—most commonly referred to as supercapacitors (SCs), ultra-capacitors (UCs), or hybrid capacitors (HCs)—in the field of power electronics. This increased interest in the hybridization of energy storages for automotive applications over the past few years is because of their advantage of high power density over traditional battery technologies. To facilitate accurate design and simulation of these systems, there is a need to make use of accurate and well validated models. Several models have been postulated in literature, however, these models have various limitations and strengths, ranging from the ease of use down to the complexity of characterization and parameter identification. The aim of this paper is to review and compare these models, specifically focusing on the models that predict the electrical characteristics of DLCs. The uniqueness of this review is that it focusses on the electrical circuit models of DLCs, highlighting the strengths and weaknesses of the different available models and the various areas for improvement.

Keywords: double layer capacitor (DLC) models; energy storage modelling; simulation models

1. Introduction

The effects and threats of global warming to the world have driven the increased development of high efficient and environmentally friendly alternative sources of energy for use. This has fueled the research into renewable energy sources for both domestic and industrial use [1–9]. Energy storage seems to be the biggest challenge in the advancement towards renewable energy solutions. Hybridization of energy storage has been the theme of many research studies in the field of power electronics and energy management [10–23], as it is considered to have great promise as an effective economic solution towards improving the performance of energy systems. Double layer capacitors (DLCs) have been proved to be very useful in hybridization of energy storages; this is due to their higher power density characteristics as compared to batteries [10–12,24].

DLCs are energy storage devices that use a double layer formed on a large surface of microporous material, such as activated carbon [25–29]. DLCs currently are of two major types, the supercapacitors (SCs) or ultra-capacitors (UCs) and the hybrid capacitors (HCs). The distinctive differences between the SCs and HCs is that the negative and positive electrode (anode and cathode, respectively) of the SCs are both made from activated carbon, whereas in the case of the HCs, the electrodes (either the cathode or anode, or both) are made from a lithium doped material—this results in the HCs having more energy density than the SCs [30,31]. This difference is illustrated in [32]; the HC's chemistry exhibits a combination of the lithium-ion battery and a SC. However, in spite of the differences in their

energy and power characteristics, it has been established that they both have the same electrical model and characterization method [30].

With the growing interest in the use of DLCs for power electronics and energy storage applications, power electronic designers and engineers are constantly faced with the vital task of accurately designing and selecting suitable DLCs for their applications. More often than not, the design process is carried out in a simulation environment using high fidelity computer software. However, in order to accurately simulate the electrical behavior of the components in a software environment, it is important to correctly use the electrical models of the components in order to get an accurate view of their electrical behavior in response to a load. Unfortunately, many models of DLCs exist in literature and choosing the right DLC model to use is an exhausting task. New designers in DLC design and selection for various applications will find the content of this paper very helpful, as it will bring them up to speed on the state of the art and what parameters are required for the use of any of the electrical models. This paper is unique because it focusses on the electrical applications and end use models rather than the models that focus on predicting chemical characteristics of the DLCs. Considering these factors, the timeliness and uniqueness of this review cannot be overemphasized. The goal of this paper is to review the many available electrical models of DLCs for power electronics applications in order to bring to light both their limitations and advantages, as well as the opportunities for further research into the subject of electrical modeling of DLCs. Additionally, this paper also seeks to raise awareness regarding the need for more research into the existing electrical models in order to address the limitations of these models, which are highlighted in this paper.

This paper is presented in the following order: the second section provides a brief history and an overview of the structure of DLCs, the third section reviews the modelling of conventional capacitors and presents the various double layer capacitor models, Section 3.8 compares all the models of the DLCs reviewed in order to bring to light their comparative advantages as well as their disadvantages. The conclusion and recommendations of this review paper are presented in the fourth section.

2. History and Structure of DLCs

The concept of double layer capacitance was first described by Hermann von Helmholtz, a German physicist, in 1853 [33]. One hundred and four years later, General Electric Company received the first patent of electrochemical capacitors based on the structure of double layer capacitance as described by Hermann von Helmholtz; their capacitor utilized porous carbon electrodes, using the double layer mechanism for charging [34]. In the same year, a Japanese company, Nippon Electric Company (NEC), received a license to use a technology that had been initially patented to Standard Oil; this technology was a device that stored energy in double layer interface. With this technology, the first market-ready electrochemical capacitors were produced for application in memory back-ups of computers in the same year, 1957 [35,36]. However, this was not a successful attempt until in 1971, when the same Japanese company, NEC, produced the SC, which then became the first commercially successful double layer capacitor [36,37]. Since then, the development of DLCs has been quite rapid. With improvements as the years went by, other companies, such as Maxwell technologies, Panasonic, Nesscap, AVX, Cap XX, Taiyo Yuden, Yunasko, etc., to mention just a few, have joined the race to push the frontiers of DLCs further.

The schematic construction of DLCs is shown in Figure 1. A DLC consists of three basic layers: the electrolyte, the separator, and the positive and negative electrodes. It exploits the double layer of charge formed when a voltage is applied to an electrode immersed in an electrolyte [38]; this is most likely where the name double layer capacitors originate.

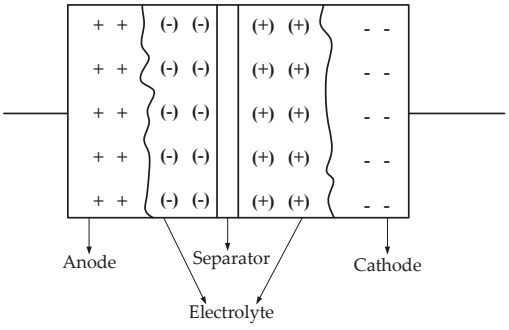

Figure 1. Basic structure of double layer capacitors (DLCs) showing the four main components of its construction.

The electrolyte and electrodes used in the construction of DLCs have to be selected interdependently, as these two largely directly affect the power and energy density of the capacitor cell. There are two types of electrolytes currently in use for DLCs and they are the aqueous and organic electrolytes. However, the organic electrolyte is most commonly used in commercial devices; this is because the organic electrolyte gives room for achieving higher voltages and very low self-discharge, and does not require chemical modification of the electrode [39]. There are various types of materials being used for the electrodes, such as metal-oxides, conducting polymer, and carbon, to mention just a few. However, carbon has been more commonly utilized because of its low cost and availability [36]. Different treatments of carbon are being researched for the improvements of the electrode, which has a direct impact on the power density of the cell [38,40]. The separator provides electrical isolation between the two electrodes; however, it is an ion-permeable membrane, giving room for ionic charge transfer between the two sections of the electrolyte. The materials used for the separator usually depend on the electrolyte used and they include polymer and paper for organic electrolytes and ceramic and glass fiber for aqueous electrolytes. More details on the structure and construction of DLCs can be found in Sharma and Bhatti [36], Signorelli et al. [38], and Yoshida et al. [40].

Currently, the two major DLCs are the electrochemical double layer capacitor (EDLC) and the HC. The EDLC, often referred to as a SC or UC, has both its positive and negative electrodes made from carbon. The most common HC is the lithium-ion capacitor (LiC); this is formed from the combination of the intercalation mechanism of a lithium ion battery with the cathode of an EDLC; the anode of the LiC is doped with a lithium ion, hence the name LiC. Other materials used for the electrodes of HCs include potassium-ion and other lithium-containing materials such as $Li_4Ti_5O_{12}$, TiO_2, $LiMn_2O_4$, and $LiFePO_4$ [41]. The other type of DLC is the pseudo capacitor. Contrary to the EDLC and the HC, storage of charge is done faradically through the transfer of charge between the electrode and the electrolyte [42]. This faradic charge storage in pseudo-capacitors presents the potential for higher energy densities than the EDLCs. However, the low cycling stability and huge prohibitive costs have limited the successful adoption of pseudo-capacitors in the market [43].

The performance of energy storages in regards to their specific energy and power densities is usually compared using a graph called the Ragone plot. It consists of two axes, the energy density and power density axis. The different energy storage devices are then plotted on the graph according to their respective characteristics; with this, their performances can be easily compared at a glance. The Ragone plot presented in Figure 2 [44] shows the major differences between the LiC and the EDLC (also known as SC). The LiC has a much higher energy density than the SC, while the SC has a higher power density than the LiC.

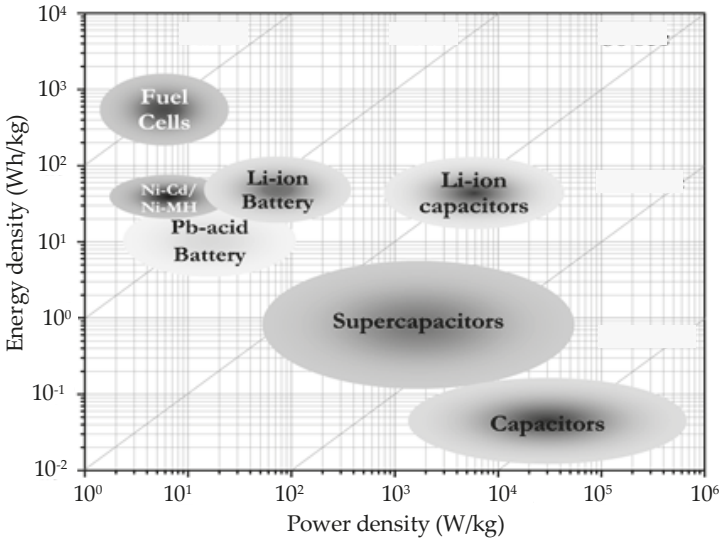

Figure 2. The Ragone plot of some energy storage devices showing their characteristics in regard to their energy and power densities (adapted from [44]).

The applications of DLCs are very wide and cannot be exhaustively discussed, as new applications are being introduced in research year in and year out. Their applications include, but are not limited to, the following: applications in memory backups of computing devices [45], energy storage hybridization in electric vehicles [46–48], applications in static synchronous compensators (STATCOMs) for improved power quality in power distribution systems [36,49,50].

3. Double Layer Capacitor Modelling

Before diving into the world of double layer capacitor modelling, it is important to briefly review some modelling methods of conventional capacitors. This will give a complete perspective when looking at the DLCs, since the basis for the double layer capacitor is the conventional capacitor.

3.1. Conventional Capacitor Modelling

Capacitors are usually modelled as lumped RLC (resistor-inductor-capacitor) networks, with the resistor representing the series resistance or ESR (equivalent series resistance) of the capacitor, the inductor representing the inductance of the capacitor leads and the current path through the capacitor, while the capacitor's value is the rated capacitance of the capacitor being modelled. However, results from recent experiments indicate that the inductance or equivalent series inductance (ESL) in the lumped RLC models is quite inaccurate, and hence can be misleading [51].

Due to this fact, a more distributed model of capacitors is introduced by Sullivan et al. [51] in their research. This distributed model was derived in the form of a standard lumped transmission line model. Figure 3 describes the progression of the derivation of this distributed model from the standard lossless transmission line model in Figure 3a, through to the proposed distributed capacitor model. In the standard lossless lumped transmission line model, each individual capacitor plate pair is modelled as a discrete capacitor and then an inductance is added between these discrete capacitors. The inductance is calculated using Equation (1)

$$L = \mu_o \cdot \left(\frac{xl}{w} \right) \tag{1}$$

where μ_o is the permeability of free space, l is the length of the capacitor that is parallel to the current path, w is the width of the capacitor, and an assumption is made that $w >> x$, where x is the height.

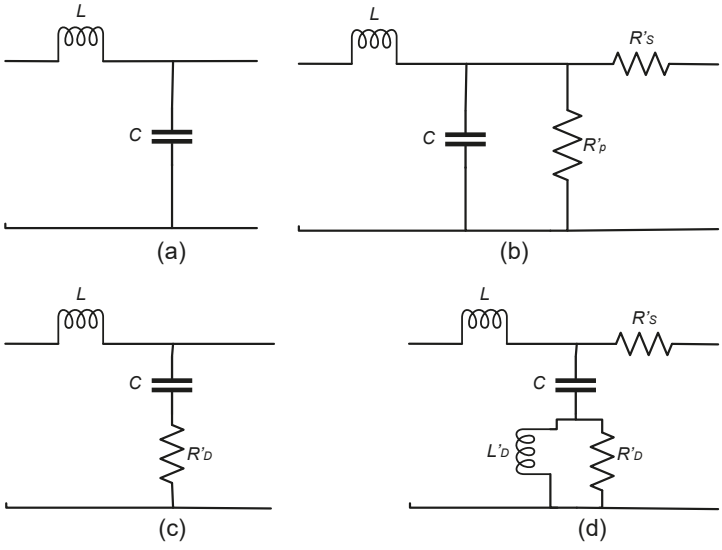

Figure 3. Schematic of (**a**) the standard transmission line model (**b**,**c**) improvements to the transmission line model, and (**d**) the distributed capacitor model formed on the basis of the standard transmission line model.

However, although the standard lossless transmission line is the most basic distributed model of the capacitor, it does not match the behavior of actual capacitors in practical. This obviously is due to the fact that actual capacitors are not lossless. In Figure 3b, two resistors are introduced in the standard lossless transmission line model $R'p$, representing the leakage resistance, and $R's$, which represents the vertical path along the end metallization of the capacitor. Both resistances are very small and are reported to have very little effect on matching the simulated results to the experimental results. The model is further tweaked in Figure 3c by introducing resistor R'_D to model the dielectric losses and the metallization resistance on each plate. It is reported that this model gives a more closely related result in simulation to experiments when compared to the model in Figure 3b. A more improved model was developed and is as shown in Figure 3d. This model is obtained through comparison of the measured and simulated step-response results. In this model, inductor L'_D is placed in parallel to resistor R'_D. This was done to indicate a frequency dependence in the loss effects; this was based on the principle that losses in the ceramic dielectric increase rapidly with frequency.

In the same study, the authors introduced another capacitor model that was based on measurements of the dielectric characteristics in the frequency domain as opposed to just matching the overall step response of the system, as was done in the model presented in Figure 4. Although a great improvement was reportedly achieved by using both models proposed by the authors when compared with the lumped *RLC* model, the distributed models still show a significant difference between the simulated and experimental data. The authors suggest that a more comprehensive model of the eddy current losses could match the actual behavior of the capacitor. The authors report that their models fit better to experimental data when compared to the alternatives, although their models still need to be refined further to fully capture the actual behavior of capacitors. There are two major problems with the models proposed by the authors. Firstly, the models have only been validated for one type of capacitor. Secondly, there is no specific number of lumped sections that is satisfactory to obtain best results; this would make the research quite difficult to replicate in simulation.

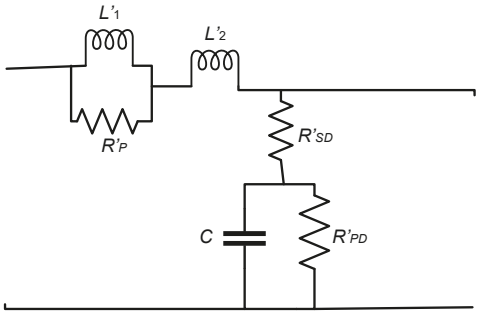

Figure 4. Schematic of the distributed capacitor model based on frequency characterization of the dielectrics.

In another study by Perisse et al. [52], two models were developed for electrolytic capacitors taking into account the temperature and aging of the capacitors. Their motivation was that since in many applications of the electrolytic capacitors, such as transport and aerospace engineering, the degrading characteristics and temperature variations become significant with time, a model taking these degrading characteristics into consideration is very important. Figure 5 presents the two models that were used. The parameter identification was carried out using a genetic algorithm integrated into Matlab®, and this was done also using the frequency data measurements. In Figure 5a, C_1, represents the total capacitance between the anode and the cathode. Resistance R_a is a combination of a number of terms, which include the resistances of the terminals, the tabs, the foils, the impregnated electrolyte paper, the tunnel electrolyte, and the dielectric. R_c is the leakage current, which is dependent on the quality of the dielectric material. R_b was not stated to represent anything but was reported to be essential in obtaining a physical representation of the model, even though it did not have much influence in the range of measurement.

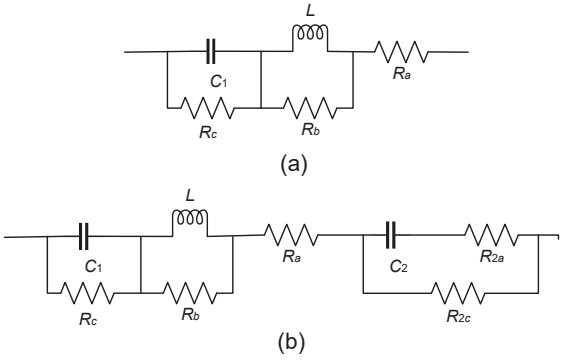

Figure 5. Electrical model of electrolytic capacitors with parameter identification done by applying genetic algorithm on the frequency data. Note that (**b**) is an extended version of (**a**) with the extended circuit parameters allowing room to factor in the effects of temperature.

Capacitor C_2 and resistors R_{2a} and R_{2c} were added in Figure 5b in order to factor in the effect of temperature reduction so as to obtain better results throughout the temperature range, especially for negative temperatures. The exact method of their parameter identification and characterization is detailed in the study by Perisse et al. [52]. It is important to state that although the results reported by the authors are positive, the models have been validated for only electrolytic capacitors, therefore they

cannot be applied to other capacitor types unless further research is carried out to validate the model for other capacitor types.

Looking at these four capacitor models, it can be said that the lumped *RLC* circuit model is still the simplest and most basic model for conventional capacitors, since other more detailed models fall short in their validations and simulations. Now that we have established the background of conventional capacitors, the next few subsections will focus on modelling of DLCs.

3.2. Classical Equivalent Circuit Model

The classical equivalent circuit model of DLCs is the most common, simplest, and probably the most basic model of a double layer capacitor [53]. This model is represented in Figure 6 [25]. It consists of just three parameters: a capacitor (C), a series resistance R, and a parallel resistance (R_p). The three circuit parameters can be obtained from the datasheet of the manufacturers of the devices. R_i is the equivalent series resistance, C is the rated capacitance of the device, and R_p is calculated by dividing the nominal voltage by the leakage current, which are both presented in the datasheets of the manufacturers.

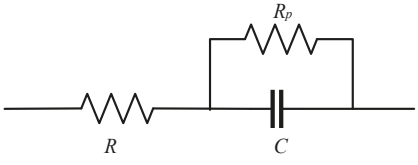

Figure 6. Classical equivalent circuit of a double layer capacitor showing its three basic characteristics: the internal resistance (R), its capacitance (C), and its self-discharge resistance (R_p).

The ease of parameter identification for the classical equivalent circuit model makes it very easy to implement in simulation. The classical equivalent model has been validated to have a closely relatable response to the actual response of a physical model [53,54]. However, in his research, Rodolfo [55] came to the conclusion that the classical equivalent circuit model does not perfectly match the behavior of DLCs as compared to other electrical models. Therefore, for basic simulation studies the classical equivalent circuit model can be used, especially in preliminary design calculations.

Cultura and Salameh [56] suggest that for short duration experiments, the classical equivalent circuit model can be further reduced by removing the leakage resistance, thereby reducing the model to just the equivalent series resistance and the capacitance of the DLC. This is because the leakage resistance is much larger than the series resistance, therefore it has no significant effect on the performance of the model for an analysis lasting for a short duration. Another derivation from the classical equivalent circuit model was done by Nakajo et al. [57]. The authors replaced the capacitance C in the classical equivalent circuit model with a variable capacitor. The capacitance was varied depending on the discharge current through a lookup table. The model was validated with a 200 F Lithium-ion capacitor and the results obtained were reported to be impressively above 98% correlation for both charging and discharging of the DLC.

A slight deviation from the classical equivalent circuit model is the first order circuit model, which is also a derivation of the lumped *RLC* model used for conventional capacitors. Figure 7 shows the schematic representation. The series inductor L is added to represent the equivalent series inductance (ESL) of the capacitor. The ESL is a representation of the inductance of the capacitor leads and the current paths through the capacitor just as it is in conventional capacitors.

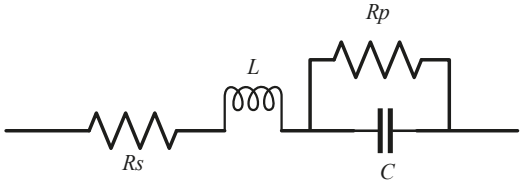

Figure 7. First order circuit model of DLCs, which can be described as a variation of the classical equivalent circuit model, taking into account the inductance of the capacitor leads and the inductance of the current paths in the capacitor.

Another variation of the classical equivalent circuit model is shown in Figure 8. Cultura and Salameh [56] claimed that this model can adequately describe the performance of capacitors in slow discharge applications. This model was used to determine the terminal behavior of a double layer capacitor. The total cell capacitance (C_{cell}) was calculated using (2), which is expressed as the sum of a constant capacitor (C_o) and a variable capacitor (V_c) whose value changes linearly with the cell voltage.

$$C_{cell} = C_o + kV_c \tag{2}$$

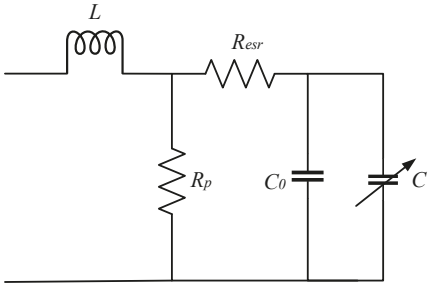

Figure 8. Variation of the classical equivalent circuit model of DLCs taking into account the linear change in cell capacitance of the capacitor, represented by a variable capacitor.

Just as it is in the classical equivalent circuit, R_{esr} is the equivalent series resistance (ESR), which brings about the loss of energy during charging and discharging, R_p accounts for the capacitor self-discharge, and inductance (L) is a result of the capacitor construction, which is the inductance of the capacitor leads and parallel current paths. This model has been validated for a SC bank (more detail is reported in [56]).

3.3. Ladder Circuit Model

Nelms et al. [53] investigated the use of ladder circuits to model DLCs. This investigation was justified by the success achieved from modelling nickel fiber electrodes in electrochemical capacitors in previous research. The ladder circuit model is presented in Figure 9. Part of the ladder circuit looks like the circuit of the classical equivalent circuit model, but the circuit parameters of the ladder circuit were determined from alternating current (AC) impedance measurements and EQUIVCRT (a computer program developed at the University of Twente). This program uses the nonlinear least squares fitting technique as opposed to direct derivation from the datasheets, as is in the case of the classical equivalent circuit. More details of the AC impedance characterization and parameter identification technique used for the ladder circuit model are presented in the study by Nelms et al. [53].

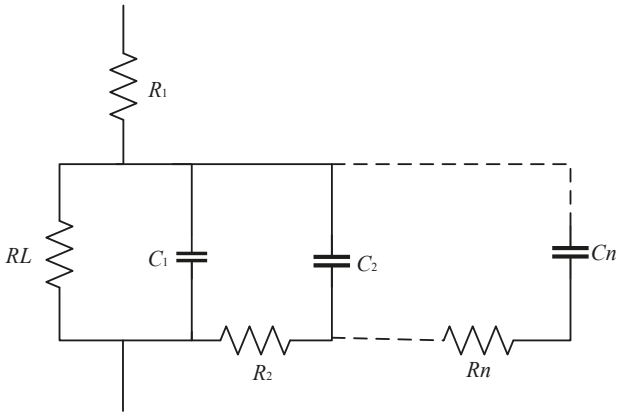

Figure 9. Ladder circuit model of a DLC.

The ladder circuit model was evaluated using two different applications: a pulse load and a slow discharge. The results obtained were further compared with the classical equivalent circuit model. It was discovered that the classical equivalent circuit model better predicted the capacitor voltage under slow discharge than the ladder circuit model. This might have been due to the number of rungs on the ladder circuit, since the authors proposed more resistor-capacitor (RC) branches on the ladder circuit to enhance the ability of the ladder circuit model to better predict the characteristics of the DLCs.

The use of ladder circuits to model DLCs looks promising from the reports in literature. However, there is no fixed number of RC branches that must be used to obtain accurate results in the prediction of the characteristics of DLCs; this makes the use of this model difficult, and secondly, the parameter identification technique is complex. More research is needed to determine the minimum number of RC branches required to accurately predict the electrical characteristics of DLCs.

3.4. Transmission Line Model

A transmission line model also exists for DLCs just as it does for conventional capacitors; this is because the capacitance of the layers shows a non-linear relationship with their surface area, as reported by Cultura and Salameh [56]. This non-linear relationship is primarily due to the porous materials forming the electrodes of the DLC, causing the resistance and capacitance to be distributed and not lumped. Hence the proposal that the theoretical model of a double layer capacitor be treated as a transmission line with voltage dependent distributed capacitance.

The schematic of the transmission line model of DLCs looks very similar to the ladder circuit model previously discussed. Figure 10 represents the theoretical transmission line model of DLCs. The parameter identification is unclear, but it most probably makes theoretical sense, since the conventional capacitors are also modelled using transmission line models.

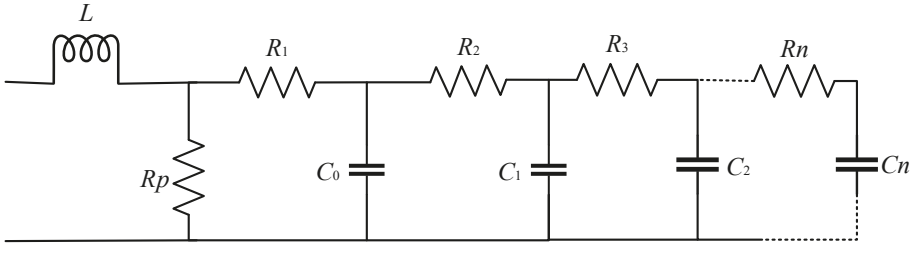

Figure 10. Transmission line model of DLCs.

3.5. Zubieta Model

The Zubieta model is named after Luis Zubieta, a Venezuelan researcher. He proposed what would become the Zubieta model for DLCs [58]. The Zubieta model consists of three RC branches and a parallel leakage resistance, to model its self-discharge property. The Zubieta model is illustrated in Figure 11 [59,60]. The three RC branches of the model represent three different time constants to model the charge and discharge of the DLC for up to 30 min.

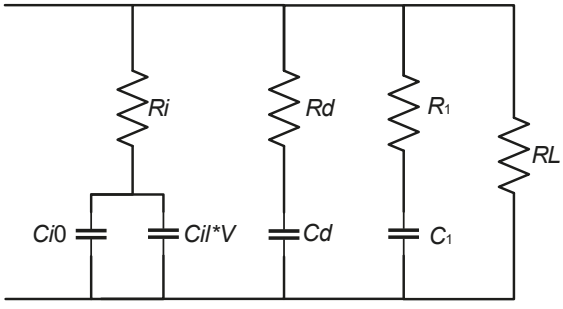

Figure 11. The Zubieta model of DLCs showing the three different RC branches.

The first *RC* branch is modelled as a voltage dependent differential capacitor consisting of a fixed capacitance (*Ci0*) and a voltage dependent capacitor (*Ci1 * V*). This first branch determines the behavior of the DLC in the initial time of operation lasting just a few seconds. The second *RC* branch, parameterized by *Rd* and *Cd*, is referred to as the delayed branch; this branch is responsible for the response of the DLC immediately after the initial time of operation of a few seconds up to 10 min. The third RC branch, with parameters (R_1) and (C_1), is responsible for the behavior of the model for times longer than 10 min.

The parameter identification process is carried out branch by branch starting with the immediate branch. The parameters of the immediate branch are determined by charging an uncharged DLC with a high constant current over a period of about 20 ms. This is under the assumption that all the charge over this period of time is stored in the immediate branch. After the first charging under constant high current for 20 ms, the terminal voltage is measured and *Ri* as described in Figure 3 is calculated by dividing the measured terminal voltage by the high current used to charge the DLC. To obtain the value of *Ci0*, the DLC is further charged under the same constant current until the terminal voltage increases by 50 mV. *Ci*0 is then calculated using (3). To determine *Cil*, the DLC is further charged until the terminal voltage is equal to its rated voltage, then the high constant current source is turned off, a fall time of 20 ms is allowed, and then the terminal voltage is measured and *Cil* is calculated using (4).

$$Ci0 = Ich * \frac{\Delta t}{\Delta V} \tag{3}$$

$$Cil = \frac{2}{v_1} * \left(\frac{Ich * (t1 - 20\text{ ms})}{v_1} \right) - Ci0 \tag{4}$$

where Ich is the constant high current, Δt is the time period it takes to increase the charge of the DLC by 50 mV, and ΔV is 50 mV. v_1 is the terminal voltage at $t1$, while $t1$ is the time it takes the DLC to charge up to its rated voltage during charge plus a further 20 ms after the charging current has been isolated. It was assumed that when the DLC reaches full charge, a charge redistribution occurs and that this redistribution of charge goes into the delayed and the long-term branch, respectively, starting with the delayed branch. The whole parameter identification procedure is a rather complex process and it is outlined in detail by Zubieta and R. Bonert [59,60].

The model was validated for a number of 470 F and 1500 F DLCs to eliminate the probability of manufacturing defects affecting the characterization results. The results reported from the validation show a very close correlation of both simulation and experimental responses. The model was further validated by Negroiu et al. [58] in their research, and they also came to very similar conclusions. They further suggested that the Zubieta model be extended on multiple branches in order to be able to predict the operation for longer than 30 min. However, this would be unnecessary, since DLCs traditionally have enough charge in them to last just a few minutes, except for the simulation of very large DLC banks with massive energy storage abilities.

The Zubieta model has been further validated by Weddel et al. [61] and Diab et al. [62] in different independent studies for different applications and the results are all coherent. It has been introduced in some simulation packages as a DLC block, specifically the Matlab® Simulink® software [63], therefore it can be said that the Zubieta model is very suitable for electrical design simulations and it has come to stay. However, the characterization and parameter identification process of the model is very complex and cannot be carried out without having the physical DLC device handy. This is because of the measurements that need to be taken from the DLC and calculations that are done; these values cannot be found on the datasheets of the manufacturers, thus making it difficult to use the model for simulation.

Since the parameter identification for the Zubieta model can be very challenging, manufacturers of DLCs should be encouraged to carry out the characterization of their products and present the parameters in their datasheets to facilitate easy implementation of the Zubieta model in design and simulations.

3.6. Two-Branch Model

The two-branch model, as its name suggests, consists of two RC branches. This looks very similar to the first two RC branches of the Zubieta model. Figure 12 shows the two-branch model with its two RC branches arranged in parallel. Just like the Zubieta, the first RC branch consists of two different capacitors, but in this model the first branch is responsible for the main energy storage and the second RC branch is responsible for the medium- and long-term response of the DLC [64,65].

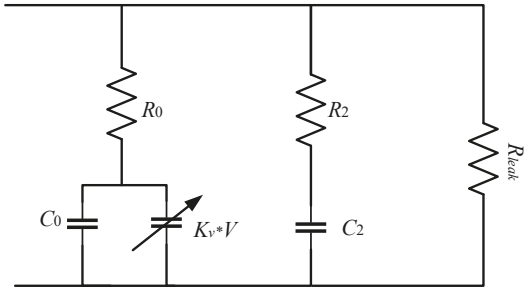

Figure 12. The two-branch model of DLCs showing the configuration of the two RC branches.

The parameter identification of the two-branch model can be done using two different methods as is described in detail in Faranda et al. [64] and Pucci et al. [65]. Although the structure of the two-branch model is very similar to the structure of the Zubieta model, it has very different parameter identification techniques. Faranda et al. [64] claim that the process of parameter identification is more precise, easier, and faster than other models, perhaps including the Zubieta model. This is probably because only five parameters are required as opposed to the seven parameters in the Zubieta model. This claim has yet to be verified.

Pucci et al. [65] used the least-squared method for parameter identification of the two-branch model (this identification method is prescribed in detail in [65]). The authors also claim that the employed parameter identification method is fast, easy, and robust to noise and measurement errors.

The two different research studies that examined the two-branch model sound very promising, but the two-branch model must be compared with the Zubieta model to verify the claims of the propagators of the two-branch method. Again, just like the Zubieta model, since the circuit parameters are determined experimentally this makes it difficult to use the model without having the physical device on hand in order to take the measurements and perform necessary calculations.

3.7. Unique Models

All the models discussed previously focus strictly on predicting the electrical characteristics of the DLCs, particularly the terminal voltage of the capacitor. There are some very complex models that look at other characteristics, such as thermal effects and life cycle characteristics [66–70]. Some of these complex models employ the use of high tech solutions like frequency impedance spectroscopy for their characterization and parameter identification (see, for example, [31,66,71]). These models are unique because most of them do not focus on the electrical characteristics but instead on other characteristics affecting DLCs.

In German et al. (2012) [68] and German et al. (2016) [72], the authors proposed the interpretation of DLC ageing using the multi-pore (MP) model. The focus of their research was strictly to monitor the ageing characteristic of the DLC. Of the two methods currently used to accelerate the ageing of an energy storage system (cycling and floating ageing), they used the multi-pore model to predict the floating ageing of the DLC. The authors also used the constant phase element (CPE) model developed by De Levie [73] to interpret the floating ageing of a DLC. They further validated their approach by comparing the MP model to the CPE model, thus validating their approach. They concluded that the ageing of DLCs is primarily a result of the redox reactions between the reactive parasitic elements present on the surface of the electrode and the electrolyte. In other studies Hwang et al. [74] and Uno and Kukita [75] used accelerated ageing and degradation tests to evaluate and estimate the cycle life of DLCs. Specifically in the study by Hwang et al. [74], the authors compared eight capacitors of the same capacitances but from different manufacturers. This was done to predict the failure time and life time under normal condition using the accelerated degradation test. Their research is particularly interesting because their method could be used in selecting the best alternative when comparing DLCs of the same capacitance across different manufacturers. In the study by Uno and Kukita [75], the authors applied the cycle life prediction model proposed in a study by Uno and Tanaka [76] to predict the cycle life of a DLC and evaluate its performance as an alternative to rechargeable batteries. The authors stated that the cycle life trends obtained in their research correlated effectively. However, no specific values were presented to tell how effective these correlation reports are.

The thermal modelling of DLCs has been presented in various previous literature [66,67,77–80]. In the thermal modelling of DLCs, AC impedance spectroscopy was used for the characterization analysis. In a paper by Funaki [80], the dependence of the voltage of DLCs on temperature during charge and discharge was evaluated, as well as their efficiency. An n-stage RC equivalent circuit was also proposed. The RC circuit looks quite similar to the ladder circuit model; the circuit parameter identification was also done using AC impedance measurements. It was concluded that the temperature dependency of the equivalent series resistance of the DLC can be expressed using a quadratic function of temperature. The number of stages required for the equivalent circuit was also determined to be three, since the frequency characteristics of the DLC were adequately represented with suppressed error. The authors in Guillemet et al. [67] proposed using compact thermal modelling to predict the thermal responses of the DLC under cycling. They further used finite-element method (FEM) simulations to further verify their proposal, and their results are reported to be that the temperature deviations did not exceed 8%. In Omar et al. [71], the characterization of DLCs is done with the hysteresis effect as a major factor. The parameter identification is also done using impedance

spectroscopy, and more detail is presented in the literature. Another very interesting thermal model is the electro-thermal model proposed in Parvini et al. [81]. This model combined the classical equivalent circuit with the reversible and irreversible heat generation in the DLC cell. The parameter identification of the electrical characteristics was carried out using pulse-relaxation data obtained from experiments in the DLC cell. Although the authors report a high accuracy in their model (and the graphs presented suggest so), there are no specific values presented to give a good picture of the level of correlation.

In Akar et al. [23] and Omar et al. [31], the authors used AC impedance spectroscopy to model the DLC in the frequency domain. Firouz et al. [82] used the non-linear least square method with trust-region-reflective algorithm for the identification of parameters. An Nth order RC circuit was also proposed for the modelling in time domain. The authors propose combining both the frequency and time domains in the analysis and characterization of DLCs. Their proposal is hinged on the limitations of implementing the individual domains. Nelms et al. (2001) [83] also used AC impedance spectroscopy in combination with the parameter identification topology described in Nelms et al. 2003 [53] to predict the performance of a DLC. They proposed a model which was referred to as the Debye polarisation cell (DPC). They compared the performance of the DPC to that of the classical equivalent circuit model and found that although the results followed a similar trend, the classical equivalent circuit model better matched the measured data. The only advantage of the DPC over the lumped parameter models was that some of the elements of the DPC could be associated with the chemical reactions in the DLC. However, no correlation results are presented for either the equivalent circuit model or the DPC model, which makes it difficult to evaluate the accuracy of the models.

3.8. Comparison of Models Reviewed

Eight electrical models of DLCs have been reviewed in detail in this review paper, excluding the models for conventional capacitors and the other unique models. Table 1 is a brief comparison of these models. All of the eight models can be used for power electronics and energy storage applications, however, only the classical equivalent circuit and the Zubieta models have been reportedly used in literature.

Table 1. Comparisons of the different electrical DLC models considered.

DLC Model	Parameters Required	Complexity of Parameter Identification	Reported Accuracy (%)	Validation Capacitance (F)
Classical equivalent circuit	3	Very easy (from datasheet)	Not reported	5 and 500
First order circuit model	4	Easy (from datasheet)	Not reported	Not reported
Classical equivalent circuit II	5	Experimental measurements	98	200
Ladder circuit	$\geq$7	AC Impedance	Not reported	50
Transmission line	$\geq$10	Theoretical (AC characterization)	Not reported	140
Zubieta	8	Experimental data	90	470 and 1500
Two-branch	6	Experimental data	97	110, 200, 350, and 600

The classical equivalent circuit model is the simplest model for DLCs, requiring only three parameters as compared to the number of parameters required in the other models reviewed in this paper. Its parameter identification technique is also very simple, since all the parameters required are all presented in the datasheet of the manufacturer, therefore it would be very useful for preliminary design calculations and simulations. However, for a more detailed prediction of the electrical responses of DLCs, a more detailed model is required. Two variations of the classical equivalent circuit models that would probably give a more detailed view of the DLC behavior were discussed, but the inductor value might be difficult to obtain from the datasheet in the case of the first order circuit model while the second variation, which introduced a variable capacitor, needs its parameters determined by experimentation, which can be cumbersome for end users, especially for calculations in conceptual designs.

The ladder circuit model uses a minimum of seven parameters and its characterization and parameter identification is carried out using impedance spectroscopy, which is quite complex. The RC ladder circuit model has not been applied in any project in literature. It is suggested in literature

that the more rungs on the ladder circuit, the more accurate the prediction of the model, however, more work needs to be done to determine the minimum number of rungs required on the ladder to achieve perfect results in the simulations.

The transmission line model is a rather theoretical model, however, it makes sense to have a ladder circuit model for DLCs, since there is a ladder circuit model for conventional capacitors. The transmission line model looks a bit similar to the ladder circuit model, with very few differences. The parameter identification method is not so clear, but most likely AC impedance characterization is also applicable to the transmission line model, since it is used for the ladder circuit model. The transmission line model has not been applied in literature, but it might better describe the behavior of DLCs, since it takes into account the inductance of the leads and the current paths through the capacitor.

The Zubieta model is arguably the most common electrical model for DLCs, consisting of eight parameters, which are determined by a cumbersome experimental process. It has been applied in literature, validated several times, and even adopted by Matlab® Simulink® as block devices for DLCs for simulations; however, since the parameter identification process is experimental, it is difficult to utilize the model without having the physical limitation, which is a huge limitation.

The two-branch model is quite similar to the Zubieta model but consists of two fewer circuit parameters. The parameter identification is also experimental, just like the Zubieta model, but uses different techniques. There are two different identification techniques in literature for the parameters of the two-branch model. These techniques are both shorter than the technique used in the Zubieta model, perhaps because of the reduced number of parameters.

Summarily, looking at the comparison presented in Table 1, the only comparable metric aside from the number of parameters required and the complexity of their identification is the reported accuracy. However, only a few of the authors actually report specific values of accuracy or levels of correlation with the experimental data. Looking at the capacitance of the DLCs reportedly used for validation by the authors, they differ widely across the different models. These differences make it difficult to specifically highlight a DLC model as the best or most accurate for power electronics and energy storage applications. There is need for more research that would compare the electrical circuit models and validate them specifically for the same capacitance value so that the most accurate can be determined. At this stage, it would be improper to point out one of the models as the most effective in predicting the voltage of a DLC. However, it can be stated categorically that the classical equivalent circuit model remains the simplest DLC electrical circuit model, as its parameterization is easy.

4. Conclusions

The aim of this paper was to review the many available electrical models of DLCs for power electronics applications. This was done to bring to light their limitations and advantages and the opportunities for further research into the subject of electrical modeling of DLCs. The different prevalent electrical models of DLCs have been reviewed and their characteristic circuits have been presented. Their limitations and strengths have been discussed, which has allowed us to reach the following conclusions:

1. The classical equivalent circuit models can be used for basic preliminary design calculations, as the circuit parameters are presented in the manufacturers' datasheet.
2. More research is needed to determine the minimum number of RC branches required to obtain accurate results and thereby validate the potency of the ladder circuit model.
3. The transmission line model has the potential to give better results than the ladder circuit model, however, it has not been tested. Therefore, researchers are encouraged to test the transmission line model and compare the results with the ladder circuit model in order to clear the air in this grey area.
4. The two-branch method must be further compared against the Zubieta model to verify the claims of its propagators.

5. Since the Zubieta model has been validated widely and is gaining ground in simulation software like Matlab® Simulink®, DLC manufacturers should be encouraged to characterize their products using the Zubieta model and present the parameters in their datasheets to facilitate easy and accurate design and simulation of the DLCs.

The focus of this paper is the electrical model for DLCs, therefore only the models that satisfy these criteria are reviewed in detail. However, the more complex models, which look at the thermal, ageing, and hysteresis characteristics, are highlighted but not reviewed in detail, since they fall out of the scope of this review. It is anticipated that the key issues raised in this review will stir up a chain of new research into resolving issues around the adoption of the electrical DLC models. Furthermore, this review is a call to action for all the stakeholders in the DLC industry like manufacturers, power electronic designers, engineers, and researchers.

Author Contributions: Conceptualization and Writing—original draft preparation: I.N.J.; Writing—Review and Editing and Supervision: N.G. and R.G.

Funding: This material is based on research/work supported wholly/in part by the National Research Foundation (NRF) of South Africa (Grant Numbers: 112236). The research findings are that of the authors and not that of the NRF.

Conflicts of Interest: The authors declare no conflict of interest.

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A Novel Composite Equalizer Based on an Additional Cell for Series-Connected Lithium-Ion Cells

Xin Lai *, Chun Jiang, Yuejiu Zheng *, Han Gao, Peng Huang and Long Zhou

College of Mechanical Engineering, University of Shanghai for Science and Technology, Shanghai 200093, China; jiangchun621@126.com (C.J.); gaohanmail@gmail.com (H.G.); peng_huang@foxmail.com (P.H.); zhoulong925@126.com (L.Z.)

* Correspondence: laixin@usst.edu.cn (X.L.); yuejiu_zheng@163.com (Y.Z.); Tel.: +86-139-183-94287 (X.L.)

Received: 1 October 2018; Accepted: 20 November 2018; Published: 1 December 2018

Abstract: Cell inconsistency can lead to poor performance and safety hazards. Therefore, cell equalizer is essentially required to prevent the series-connected cells from overcharging, undercharging, and overdischarging. Among current equalization schemes, passive equalizer has a continuously wasting energy with low equalization efficiency, and active equalizer has high cost with complex circuit structure. In this study, a novel composite equalizer based on an additional cell with low complexity is presented. This method combines a passive equalizer and an active equalizer. Firstly, the configuration and circuit of our proposed composite equalizer are introduced, and the equalization principle is analyzed. On this basis, the control strategy and algorithm of the composite equalizer are further proposed. Finally, the composite equalizer is verified through simulation and experiment in various cases. The study results show that this method improves both the consistency level and the available capacity of the battery pack. Moreover, our proposed equalizer can overcome the shortcomings of commonly used equalizer and combining the advantages of different equalizer to maximize the equalization efficiency with a simpler equalizer structure.

Keywords: lithium-ion power battery pack; composite equalizer; active equalization; passive equalization; control strategy and algorithm

1. Introduction

Energy crisis and environmental problem are two major challenges facing humankind in recent years, and energy savings and emission reduction have become real priorities all over the world. New technologies and methods for saving energy and reducing emissions have become an important research focus in modern automobiles [1–5]. In this situation, the development and popularization of battery electric vehicles (BEVs) and hybrid electric vehicles (HEVs) have entered a high-speed period. As energy storage and supply components, batteries directly determine the safety and mileage of electric vehicles (EVs). Therefore, battery and its management system are one of the core technologies of EVs [6–8]. Various power batteries, such as lead acid, nickel-metal hydride (NiMH), and lithium-ion batteries (LIBs) have been used in EVs. Among them, LIBs are widely used due to their high energy density, long cycle life, and high efficiency [4,9–11]. In order to meet high-energy and high-power application requirements for EVs, hundreds or thousands of cells are connected in series and parallel to form battery packs [12–14]. Factors such as the manufacturing process and the actual working environment cause inconsistencies in the performance of these LIBs. The most intuitive manifestation is voltage inconsistency, while the other is internal resistance inconsistency. These inconsistencies cause the actual capacity of the battery packs to be less than the theoretical capacity, which greatly reduces their service life [5,15–17].

In order to reduce cell inconsistency, it is necessary to screen cells before combining them into a battery pack. Cells in the same battery pack should have the same chemical properties and

physical sizes. However, the consistency level among cells is already higher even after screening. Cell inconsistency in a battery pack can lead a cell or some cells to be overcharged, undercharged, or even overdischarged, causing serious security problems [5,16,18]. In order to maximize battery life and utilization, battery equalization technology is widely used to reduce the impact of battery inconsistencies. Therefore, equalization technology is critical for improving battery performance.

There are two main ways to equalize lithium-ion batteries. One is chemical equalization, i.e., to achieve an equalization target through the chemical reaction inside the battery [19]. This method is easy to implement and does not require complex circuit connections, but this method is presently in its infancy. The other is physical equalization, i.e., to achieve an equalization target by means of mechanics or electronics. Physical equalization mainly includes passive and active equalization [20,21]. Passive equalization, also known as energy dissipation equalization, can realize equalization by passing the excess energy of the cell through a bypass resistor. Passive equalization is advantageous in terms of its simple structure and low cost, but is disadvantageous due to its low equalization current and large energy loss [22–24]. However, energy is dissipated in the form of heat by the bypass resistor, which greatly reduces the energy utilization of the whole battery and simultaneously increases the temperature. Due to the demands of controlling the temperature within a certain range, the equalization current is usually low and the equalization time is long. In addition, the temperature difference may worsen the battery inconsistency [25].

Active equalization, also called energy transfer equalization, can realize energy transfer between cells in the battery packs by means of energy storage elements or other driving circuit configurations. Various active equalization configurations are summarized in Refs. [26–28]. The common energy storage elements are capacitors, inductors, and transformers. The advantages of active equalization include low energy loss and high efficiency. However, the disadvantages include complex control algorithms and high cost. In addition to the equalization configuration, the equalization algorithm also has a significant impact on the equalization efficiency improvement. It can be divided into state of charge (SOC)-, capacity-, and voltage-based equalization algorithms [22,29–31]. Generally, the energy transfer between the cells is a function of the voltage difference between cells. As a result, when the voltage difference is low, the equalization speed decreases and cells can remain unbalanced [22,30,32], and the balancing efficiency needs to be further improved [33]. Through the analysis above, we know that both active and passive equalizers have their own advantages and disadvantages.

In this study, a novel composite equalization method based on an additional cell which combines both passive and active equalizations is proposed, according to the characteristics of different equalization methods. The principle, circuit, and control strategy and algorithm are studied, and the effectiveness is verified by simulation in various cases. This method has the advantages of simple structure, low cost, simple control, and high efficiency compared to common passive and active equalization methods. Moreover, an additional cell is used in this method as the energy storage element, which allows energy storage and transfer between the battery and the additional cell. This increases the capacity of the battery pack to a certain degree while also realizing the equalization function.

The remainder of this paper is structured as follows: Section 2 gives a description of the circuit of the composite equalization. Section 3 presents its operation principles and control strategy, respectively. Modeling and simulation analysis are reported in Section 4. The effectiveness of the proposed equalizer is validated by experimental results in Section 5. Finally, conclusions and final remarks are presented in Section 6.

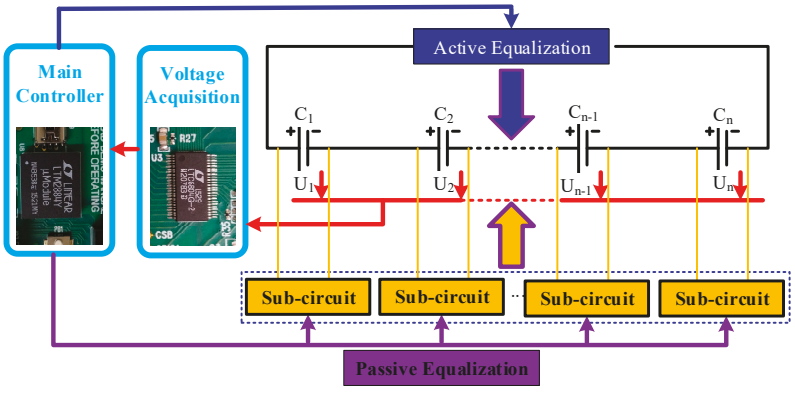
2. Scheme of Composite Equalizer

2.1. Configuration of the Composite Equalization Circuit

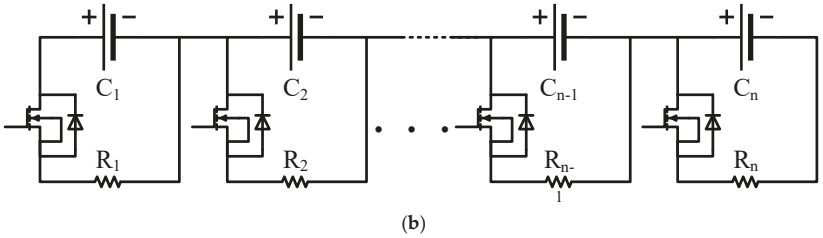
To improve the equalization efficiency, we propose a composite equalization configuration based on an additional cell that combines both passive and active equalization. This method makes full use of the advantages of different equalizations, as shown in Figure 1a. The equalization circuit is

primarily composed of the main controller, the voltage acquisition module, the composite equalization module, and so on.

Recently, the widely used passive equalization method uses a bypass resistor in parallel with the cell to consume the excess energy of the cell, as shown in Figure 1b. The active equalization in this paper uses an additional cell as the energy storage element, thus allowing for energy storage and transfer between the battery and the additional cell. This increases the capacity of the battery pack to a certain degree while also enabling the equalization function. As shown in Figure 1c, the active equalization circuit mainly includes a cell selection circuit, a commutation circuit, a freewheeling circuit, and so on. The cell selection circuit is used to select the cell to be equalized in the battery pack. The function of the commutation circuit is to make the positive and negative polarity of the cell which is to be equalized the same as the additional cell. The circuit includes four parallel branches. The freewheeling circuit consists of diodes, MOSFETs, and an inductor, and is used to buffer the current of the circuit and protect the circuit elements from being damaged when the circuit is switched on or off.

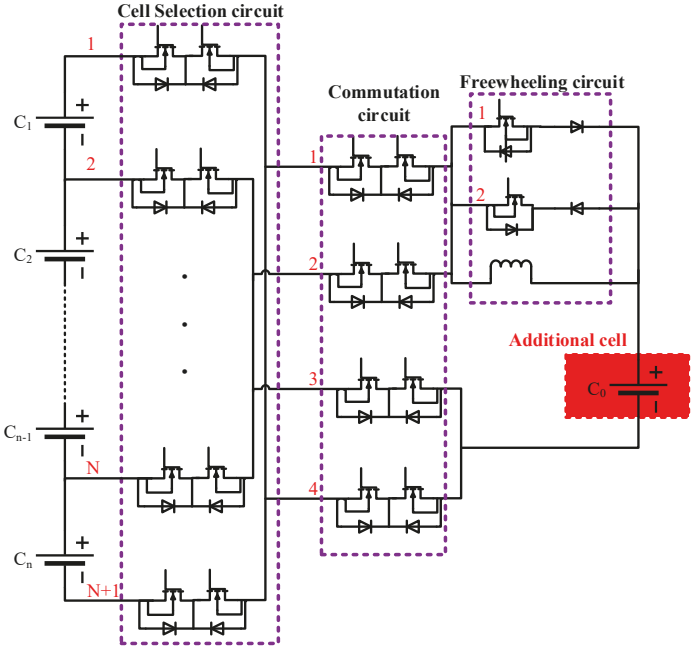


(**a**)



(**b**)

Figure 1. *Cont.*



(**c**)

Figure 1. Configuration and circuit of composite equalization. (**a**) Configuration; (**b**) passive equalization circuit; and (**c**) active equalization circuit.

2.2. Principle of the Composite Equalization Circuit

The basic principle of composite equalization is to choose the best equalization mode according to the relative voltage state between the cell in the battery pack and the additional cell. Equalization modes are generally divided into active and passive equalization modes. The active equalization mode can also be divided into the first and second active equalization modes. The equalization modes are explained separately as follows: (a) First active equalization mode: the high voltage cell charges the additional cell when this mode is in operation. As shown in Figure 2a, it is assumed that C_1 is the cell with the maximum voltage in the battery pack. The corresponding MOSFETs are controlled to turn on, and C_1 then charges the additional cell C_0. (b) Second active equalization mode: the additional cell charges the low voltage cell when this mode is in operation. As shown in Figure 2b, it is assumed that C_2 is the cell with the minimum voltage in the battery pack. The corresponding MOSFETs are controlled to turn on, and the additional cell C_0 then charges C_2. (c) Passive equalization mode: the high voltage cell battery is discharged through the bypass resistor when this mode is in operation. As shown in Figure 2c, it is assumed that C_1 is the cell with the maximum voltage in the battery pack. The corresponding MOSFETs are controlled to turn on and C_1 is then discharged through the bypass resistor. Therefore, through designing the control strategy and algorithm, each of the three equalization modes is activated according to the cell voltage change during the equalization process.

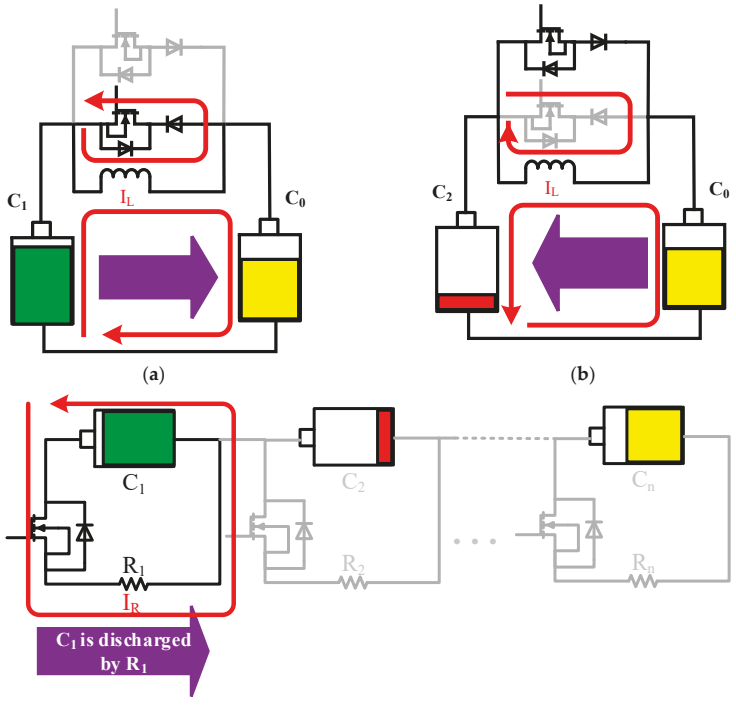


Figure 2. Principle of composite equalization. (**a**) First active equalization mode; (**b**) second active equalization mode; and (**c**) passive equalization mode.

3. Control Strategy and Algorithm

The voltage-based equalization algorithm is adopted in this paper. First, a threshold of voltage range (5 mV in this paper) is chosen. Then the voltages of cells in the battery pack are collected, and the maximum and minimum voltage are selected. If the difference between the maximum and minimum voltage is greater than the threshold, equalization control will be applied to the battery pack, otherwise not.

We first need to determine the critical voltage difference value ΔU between the additional cell and the cell to be equalized in the battery pack. When the active and passive equalization currents are equal, the voltage difference between the cell to be equalized in the battery pack and the additional cell is equal to the critical value ΔU.

It is assumed that the voltage of the cell i is U_i, where i = 1, 2, 3, . . . , n. The maximum voltage is U_{max}, and the minimum voltage is U_{min}. The voltage range between the cells is u. The voltage of the additional cell is U_0. The difference between the maximum voltage and the additional cell voltage is u_1. The difference between the additional cell voltage and the minimum voltage is u_2. The relationship between these parameters can be expressed as follows:

$$U_{max} = \text{Max}\{U_1, U_2, \ldots, U_n\} \quad (1)$$

$$U_{min} = \text{Min}\{U_1, U_2, \ldots, U_n\} \quad (2)$$

$$u = U_{max} - U_{min} \quad (3)$$

$$u_1 = U_{max} - U_0 \quad (4)$$

$$u_2 = U_0 - U_{min} \quad (5)$$

Based on the analysis above, the composite equalization control algorithm designed in this paper is shown in Figure 3a, and can be specifically described as:

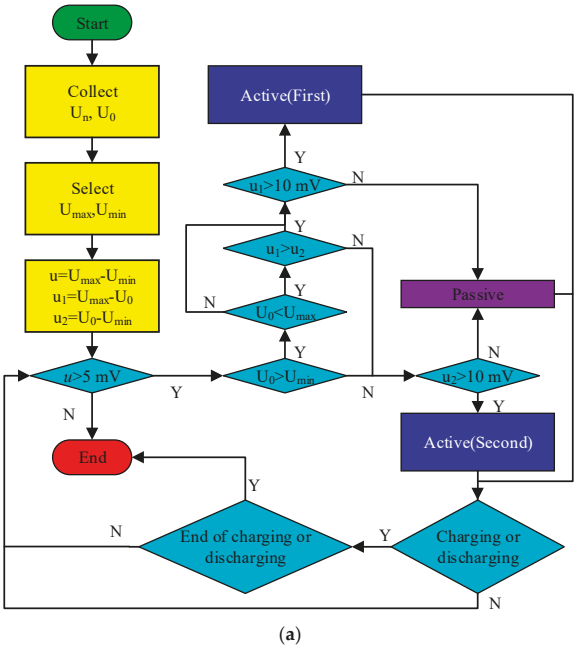
(1) When the voltage U_0 of the additional cell C_0 is detected to be less than the minimum voltage U_{min} in the battery pack and u_1 is greater than ΔU, the first active equalization mode is used. Otherwise, passive equalization is used.

(2) When the voltage U_0 of the additional cell C_0 is detected to be greater than the maximum voltage U_{max} in the battery pack and u_2 is greater than ΔU, the second active equalization mode is used. Otherwise passive equalization is used.

(3) When the voltage U_0 of the additional cell C_0 is between the minimum voltage U_{min} and the maximum voltage U_{max} and u_1 is greater than u_2, return to (1). Otherwise, return to (2).

(4) When the battery pack is charged or discharged (dynamic equalization), equalization will stop once charging or discharging has completed. When the battery pack is not charged or discharged (static equalization), equalization will stop if the difference between the maximum and the minimum voltage in the battery pack is less than the threshold (5 mV in this paper).

The passive equalization control algorithm is shown in Figure 3b. To avoid frequent activation of the switches, the cell's single equalization time T must reach t_0. The active equalization control algorithm is shown in Figure 3c. To avoid frequent activation of the switches, the cell's single equalization time T must reach t_0. The switch of the cell selection circuit is turned off immediately when the active equalization current I_L is greater than 2 A, thus suspending equalization. When the active equalization current I_L is less than 1 A, the switch is turned on to continue equalization. In dynamic equalization, t_0 should not be large; we take 60 s in this paper. In static equalization, t_0 should not be too small; we take 600 s in this paper.



(**a**)

Figure 3. *Cont.*

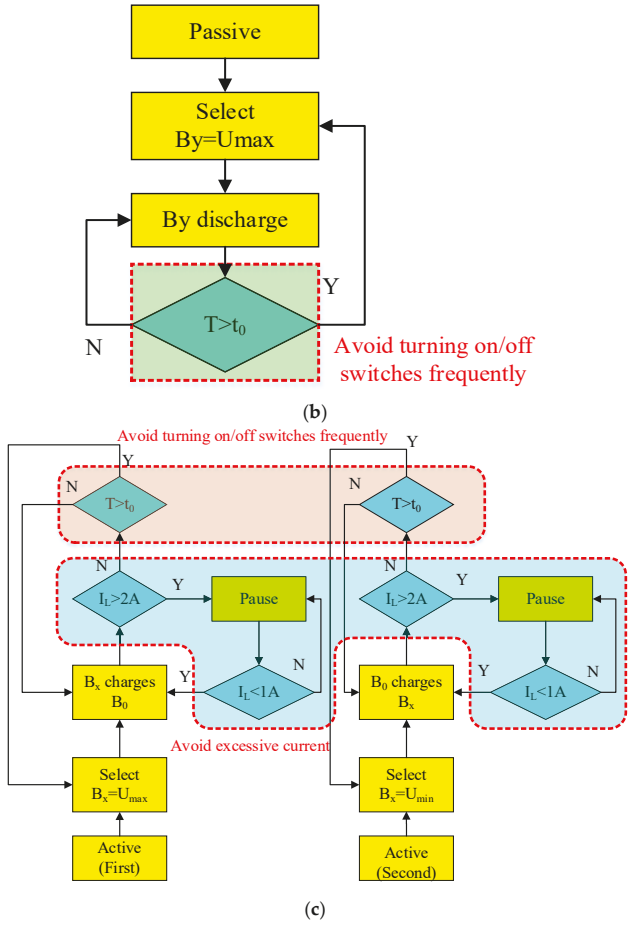


Figure 3. Flow chart of composite equalization control strategy. (**a**) Selection of composite equalization mode; (**b**) passive equalization mode; and (**c**) active equalization mode.

4. Modeling and Simulation Analysis

In this section, we use the Simscape module in MATLAB/Simulink (MathWorks, Natick, MA, USA) to build a physical model of the composite equalization circuit, and we model the equalization control strategy and algorithm in Simulink/Stateflow. The simulation model is shown in Figure 4. Based on the simulation model, the equalization process is simulated in various cases, to verify the effectiveness of the proposed composite equalization.

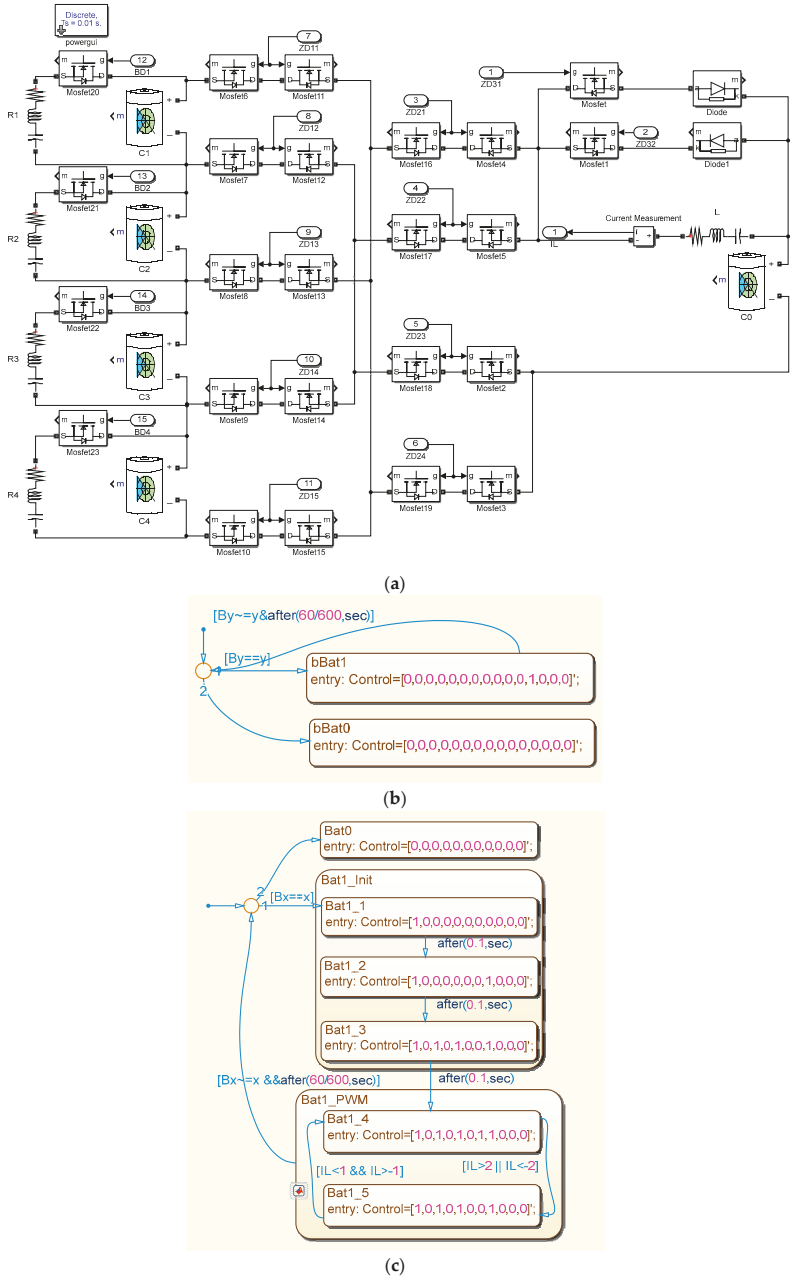


Figure 4. Simulation model of composite equalization. (**a**) Circuit configuration using Simscape in MATLAB; (**b**) passive equalization mode; and (**c**) active equalization mode.

The parameters set in the simulation are as follows: four lithium-ion cells with nominal voltage 3.7 V and rated capacity 24 Ah are connected in series to form a battery pack. The additional cell is also a lithium-ion cell with nominal voltage 3.7 V and rated capacity 24 Ah. The resistance of the

bypass resistor is 30 Ω. According to the control strategy in the last section, we need to determine the size of ΔU. Preliminary simulation results show that the size of passive equalization current is 0.13 A. When the active equalization current reaches 0.13 A, the voltage difference between the additional cell and the cell which is being equalized in the battery pack is about 10 mV, thus the size of ΔU is 10 mV. The equalization process is simulated under three different states named charging, discharging and static to verify the effectiveness of the proposed composite equalization method. Simulation is carried out in MATLAB 2014a on a computer with a 3.1 GHz processor, 4 GB memory, and 64-bit operating system.

4.1. Equalization during the Charging Process

During the entire charging equalization process, there are three different conditions on the relative voltage state between the cell to be equalized in the battery pack and the additional cell, which are described as follows:

(1) The relative voltage state between the cell to be equalized in the battery pack and the additional cell stays constant, and the voltage U_0 of the additional cell is always less than the minimum voltage U_{min}.

(2) The relative voltage state between the cell to be equalized in the battery pack and the additional cell undergoes a dynamic change process. At first, the voltage U_0 of the additional cell is greater than the maximum voltage U_{max}. Then it takes a value between the minimum voltage U_{min} and the maximum voltage U_{max}. Finally, it is less than the minimum voltage U_{min}.

(3) The relative voltage state between the cell to be equalized in the battery pack and the additional cell stays constant, and the voltage U_0 of the additional cell is always greater than the maximum voltage U_{max}.

Assuming that the SOC of C_1 to C_4 are set to 5%, 8%, 11%, and 14%, respectively. Before charging, the SOC of the additional cell is set to 2%, 50%, and 98% under the three conditions above, respectively. A constant current power supply with 8 A of current is used to charge the battery pack. When the voltage of any cell in the battery pack reaches 4.2 V, the constant current power supply will stop charging the battery pack.

In this study, four cases marked as case A, B, C, and D are set to simulate the equalization effect under charging conditions, and the simulation results are shown in Figure 5 and Table 1. As shown in Figure 5, the voltage difference among cells during the charging process without equalization is 43.20 mV, but it decreases to 27.50 mV, 27.70 mV, and 14.20 mV after equalization.

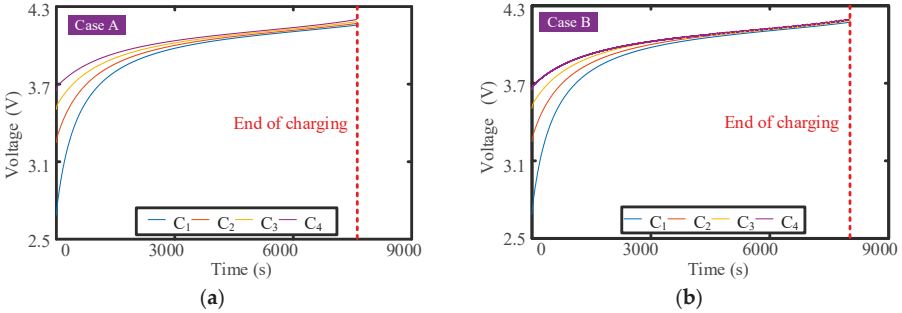


Figure 5. *Cont.*

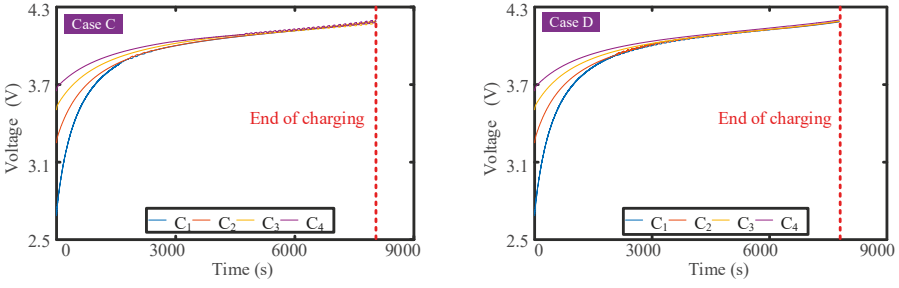


Figure 5. Simulation results of charging equalization. (**a**) Case A: no equalization; (**b**) Case B: SOC (State of Charge) of C_0 = 2%; (**c**) Case C: SOC of C_0 = 50%; and (**d**) Case D: SOC of C_0 = 98%.

Table 1. Charging time comparison.

Case	Charging Time (s)
A	7602
B	8022
C	8044
D	7783

As shown in Table 1, the charging time increases when charging with equalization, indicating that the capacity of the battery pack increases after charging with equalization. Our previous studies [33,34] show the relationship between pack capacity and cell capacities is:

$$C_{pack} = \min(SOC \cdot C) + \min\{(1 - SOC) \cdot C\} \quad (6)$$

where C_{pack} is pack capacity, SOC is the state of charge of the cell, and C is the cell capacity.

The voltage range and the SOC extremum after charging are shown in Table 2. According to Equation (6), as shown in Figure 6, the battery pack capacity under four cases after charging is 21.70 Ah, 22.63 Ah, 23.42 Ah, and 23.04 Ah.

Table 2. Voltage range and SOC (State of Charge) extremum after charging.

Case	Voltage Range (mV)	Maximum of SOC (%)	Minimum of SOC (%)
A	43.20	78.9709	69.4039
B	27.50	78.9935	73.2911
C	27.70	79.1225	76.7093
D	14.20	80.1918	76.2118

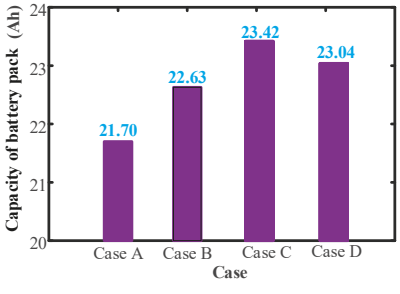


Figure 6. Battery pack capacity after charging.

4.2. Equalization during the Discharging Process

During the entire discharging equalization process, there are three different conditions on the relative voltage state between the cell to be equalized in the battery pack and the additional cell, which are as follows:

(1) The relative voltage state between the cell to be equalized in the battery pack and the additional cell stays constant, and the voltage U_0 of the additional cell is always less than the minimum voltage U_{min}.

(2) The relative voltage state between the cell to be equalized in the battery pack and the additional cell undergoes a dynamic change process. At first, the voltage U_0 of the additional cell is less than the minimum voltage U_{min}. Then, it takes a value between the minimum voltage U_{min} and the maximum voltage U_{max}. Finally, it is greater than the maximum voltage U_{max}.

(3) The relative voltage state between the cell to be equalized in the battery pack and the additional cell stays constant, and the voltage U_0 of the additional cell is always greater than the maximum voltage U_{max}.

Assuming that the SOC of C_1–C_4 is set to 90%, 92%, 94%, and 96%, respectively, before discharging, the SOC of the additional cell is set to 2%, 50%, and 98%, respectively, under the three conditions above. A 2 Ω resistor is used to discharge the battery pack. When the voltage of any cell in the battery pack reaches 2.6 V, the battery pack will stop discharging. The voltage change trajectory of the cells in the battery pack is shown in Figure 7 and the discharging time is shown in Table 3. As shown in Figure 7, the voltage difference among cells during the discharging process without equalization is 789.10 mV, but it decreases to 95.10 mV, 40.30 mV, and 21.80 mV after equalization.

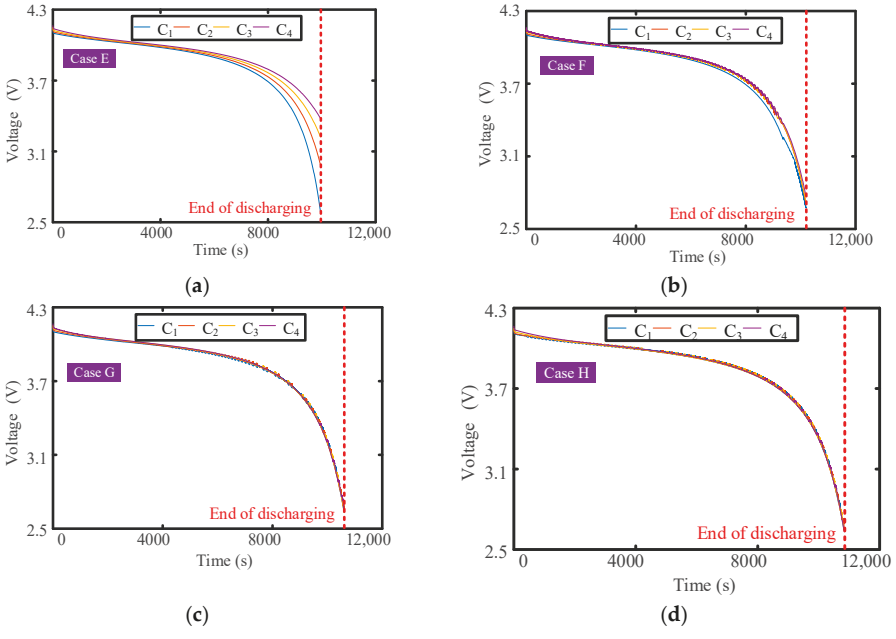


Figure 7. Simulation results of discharging equalization. (**a**) Case E: no equalization; (**b**) Case F: SOC of C_0 = 2%; (**c**) Case G: SOC of C_0 = 50%; and (**d**) Case H: SOC of C_0 = 98%.

Table 3. Discharging time comparison.

Case	Discharging Time (s)
E	9948
F	10,189
G	10,610
H	10,841

The voltage range and the SOC extremum after discharging are shown in Table 4. According to (6), as shown in Figure 8, the battery pack capacity under four cases after discharging is 22.47 Ah, 23.83 Ah, 23.99 Ah, and 23.99 Ah.

Table 4. Voltage range and SOC extremum after discharging.

Case	Voltage Range (mV)	Maximum of SOC (%)	Minimum of SOC (%)
E	789.10	6.3843	0.0063
F	95.10	0.6933	0.0019
G	40.30	0.0477	0.0008
H	21.80	0.0482	0.0046

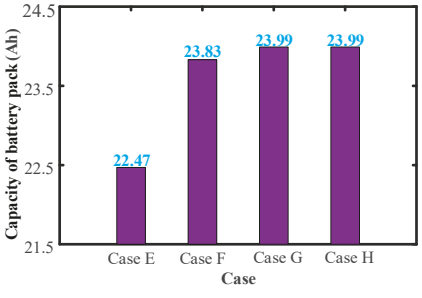


Figure 8. Battery pack capacity after discharging.

4.3. Equalization during the Static Process

During the entire static equalization process, the relative voltage state between the cell to be equalized in the battery pack and the additional cell stays constant. There are three different conditions, which are as follows:

(1) The voltage U_0 of the additional cell is always less than the minimum voltage U_{min}.
(2) The voltage U_0 of the additional cell is always between the minimum voltage U_{min} and the maximum voltage U_{max}.
(3) The voltage U_0 of the additional cell is always greater than the maximum voltage U_{max}.

Assuming that the SOC of C_1–C_4 is set to 46%, 50%, 54%, and 58%, respectively, the SOC of the additional cell is set to 36%, 52%, and 68% under the three conditions above, respectively. Equalization will only begin if the voltage range of the cells in the battery pack is greater than 5 mV. The voltage change trajectory of the cells in the battery pack is shown in Figure 9, and the discharging time is shown in Table 5. As shown in Figure 9, the voltage difference among cells without equalization is 36.60 mV, but it decreases to about 5 mV after equalization.

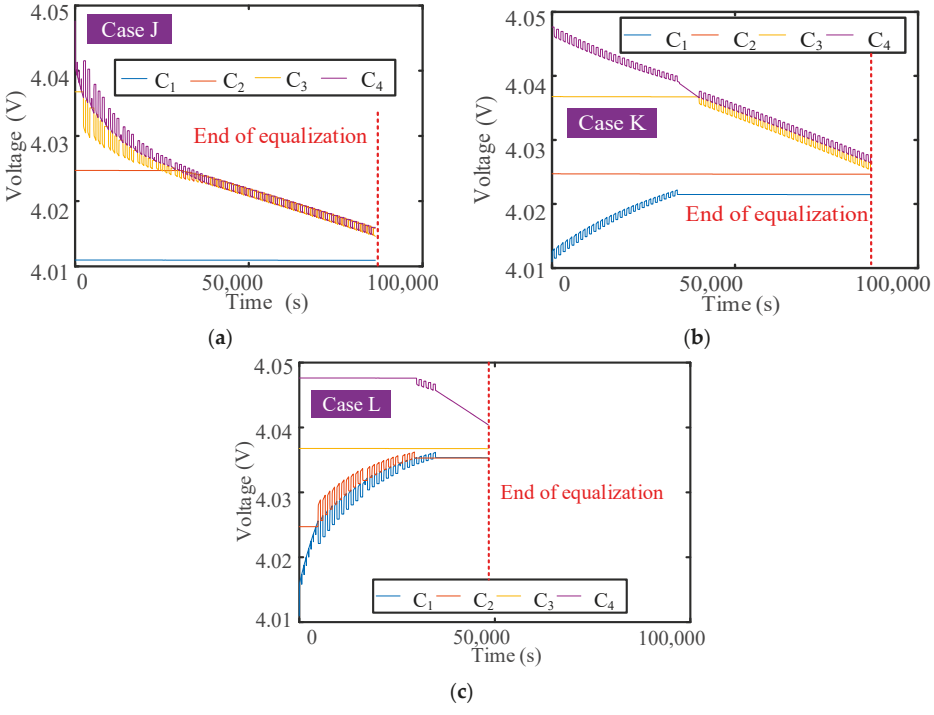


Figure 9. Simulation results of static equalization. (**a**) Case J: SOC of C_0 = 36%; (**b**) Case K: SOC of C_0 = 52%; and (**c**) Case L: SOC of C_0 = 68%.

Table 5. Equalization time comparison.

Case	Equalization Time (s)
I [1]	None
J	86,400
K	86,800
L	48,300

[1] No equalization.

The voltage range and the SOC extremum after static equalization are shown in Table 6. According to (6), as shown in Figure 10, the battery pack capacity under four cases after static equalization is 20.86 Ah, 23.64 Ah, 23.52 Ah, and 23.42 Ah.

Table 6. Voltage range and SOC extremum after static equalization.

Case	Voltage Range (mV)	Maximum of SOC (%)	Minimum of SOC (%)
I [1]	36.60	55.3540	42.5980
J	5.10	44.0755	42.5843
K	5.00	47.7993	45.7882
L	5.10	52.8665	50.5495

[1] No equalization.

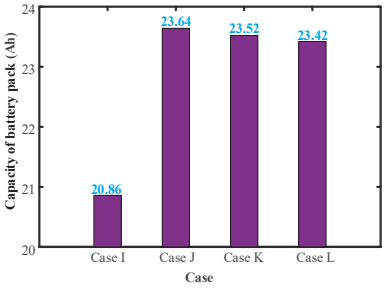


Figure 10. Battery pack capacity (static).

4.4. Comparative Study with Passive and Active Equalization

In this section, the composite equalization is compared to the passive and active equalization introduced in Section 2. We only choose the equalization during the static process in this section. The equalization during other process (charge and discharge) is similar, so there is no detail. Therefore, the initial conditions of cells in this section is consistent with that in Section 4.3. As for the comparison results, the end voltage and capacity of the cells are not very different because the equalization target (5 mV) of different equalizers are the same. In the previous sections, the end voltage and capacity of the cells are used to compare results between no equalization and equalization, so the comparison in this section is mainly through the equalization time. The shorter the equalization time, the better the equalization effect.

The voltage change of the cells in the battery pack during the different equalization methods is shown in Figure 11, and the equalization time of the different equalization methods is listed in Figure 12. It can be seen that the equalization time of the active and passive equalizers is longer than that of the proposed composite equalizer in the case of the additional cell with various SOCs, indicating the proposed method has higher equalization efficiency. Moreover, the equalization efficiency increases with the increase of the SOC of the additional cell.

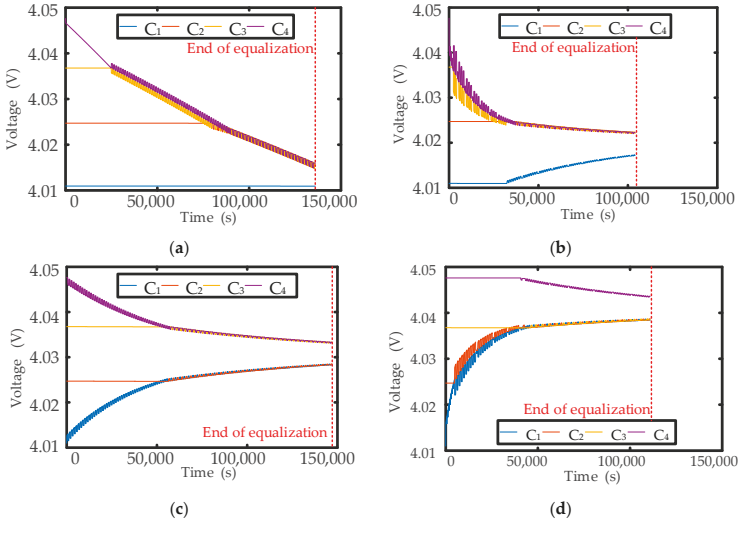


Figure 11. Simulation results of single equalization. (**a**) Passive equalization; (**b**) Active equalization (SOC of C_0 = 36%); (**c**) active equalization (SOC of C_0 = 52%); and (**d**) active equalization (SOC of C_0 = 68%).

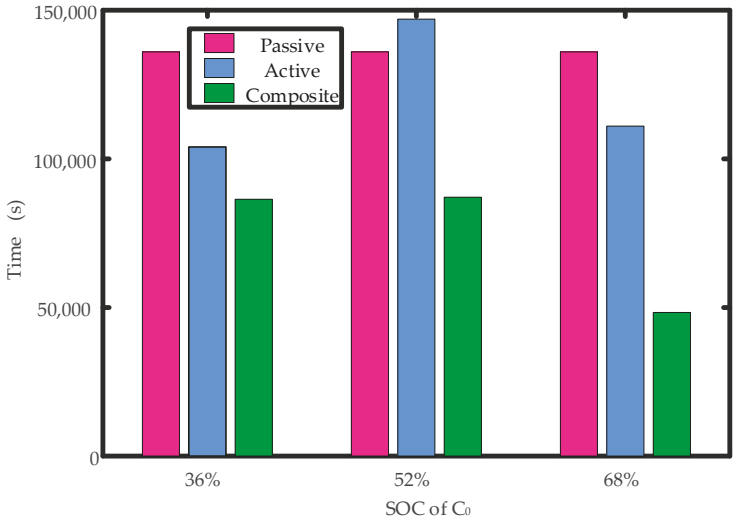


Figure 12. Comparison of simulation time for three different equalization methods.

5. Experiment Verification

To verify the effectiveness of the proposed equalizer, experimental verification is investigated in this section. The composite equalization system is mainly divided into three parts. The first part is the microcontroller unit (MCU) based on XC164CS (Infineon Technologies, Neubiberg, Germany). The function of this part is to receive the voltage information of all single cells in the battery pack, to drive the corresponding relay switch, and to communicate with the host computer. The second part is the cell voltage acquisition circuit based on LTC6804 (Analog Devices, Norwood, MA, USA). The function of this part is to detect and collect all cell voltage information in the battery pack, and then transmit it to the MCU. The third part is the core equalization circuit, including passive and active equalization. The function of this part is to adjust the voltage level of cells in the battery pack so as to keep the voltage level of cells in good consistency.

Figure 13 shows the experimental platform. The equalization circuit is the proposed circuit, and the control algorithm is realized in the controller. The data can be read by the human machine interface, and experimental data is recorded by the personal computer (PC). In this experiment, 12 cells are used as test cells for the equalizer, and a cell is used as additional cell. The parameters of the experimental cells are as follows: nominal capacity is 3200 mAh; nominal voltage is 3.6 V, lower and upper cut-off voltage are 2.5 V and 4.2 V, respectively. In the experiment, each cell has different initial SOC, and the SOC of the additional cell is the highest.

Figure 14 shows the experiment results under static condition. It can be seen that the test cells are charged by additional cell. Except Cell 8, the maximum voltage difference between cells is reduced from 32 mV to 6 mV in 3500 s. Moreover, it is obvious that passive equalizer is running (Cell 8) while passive equalizer is turned on, which greatly improves the equalization efficiency. The maximum voltage difference of all cells is reduced from 72 mV to 18 mV.

It is necessary to point out that the speed of passive equalization is slow (Cell 8), which is caused by the smaller voltage difference between cells, which is caused by the smaller equalization current, which is the disadvantage of passive equalization. However, our proposed composite equalization method combines active and passive equalizers to improve equalization efficiency, and our designed active equalizer based on an additional cell has a simpler structure than the traditional active equalizer.

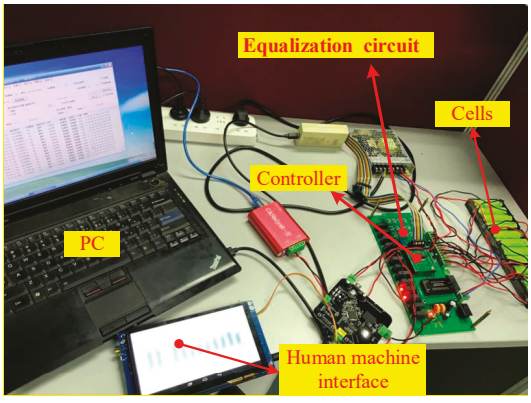


Figure 13. Experimental platform of the proposed equalizer.

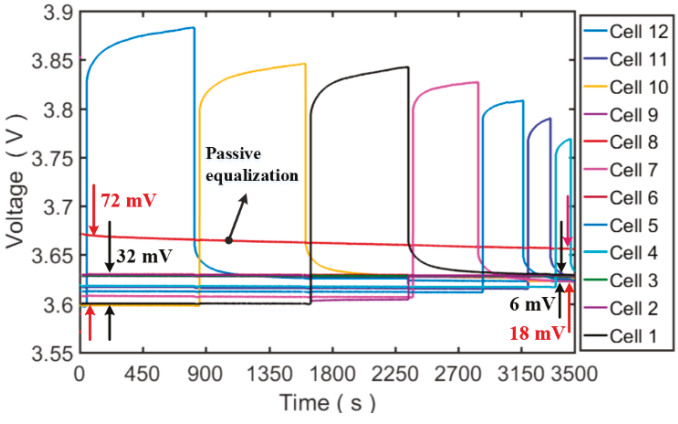


Figure 14. Experimental result under static condition.

6. Conclusions

In order to improve the consistency of cells in lithium-ion powered battery packs for EVs, a composite equalization method based on an additional cell that combines both active and passive equalizers is proposed. The equalization principle, circuit, control strategy and algorithm are studied through simulation and experiment in many cases. The main conclusions of this study are as follows:

(1) A novel composite equalization method is proposed, and its configuration and circuit are designed. The composite equalization includes passive and active equalization parts. These are mutually independent in structure and are mutually coordinated in function. Passive equalization adopts common energy dissipation equalization by using a bypass resistor. Active equalizer adopts non-dissipative equalization by using an additional cell, which has a simpler structure than the traditional active equalizer.

(2) A composite equalization algorithm containing three equalization modes is proposed. The equalization mode can be switched automatically according to the state of the cells. When the voltage difference between the cell to be equalized and the additional cell is large, active equalization will be used. When the voltage difference between the cell to be equalized and the additional cell is small, passive equalization will be used. The algorithm combines the advantages of the different equalization methods.

(3) The Simscape module in MATLAB/Simulink is used to build a physical model of the composite equalization circuit, and the equalization control strategy and algorithm are modeled in Simulink/Stateflow. The simulation results show that the consistency level of the battery pack improved and the available capacity increased. Moreover, the equalization time of the composite equalization during the static equalization process is obviously shortened compared to single equalization.

(4) Experimental results have shown the proposed equalizer demonstrates a good comprehensive performance of active and passive equalizers.

The proposed method is not sufficient tested and verified in a real battery management system for various cases. Further works include: (a) More intensive verification of the proposed method and algorithm in battery packs for various cases; (b) a more advanced equalization algorithm based on composite equalizer; and (c) equalization control of parallel-connected battery based on our proposed method.

Author Contributions: All authors contributed to the paper. Conceptualization: X.L. and Y.Z.; data curation: C.J. and P.H.; investigation: H.G. and X.L.; methodology: X.L. and L.Z.; project administration: X.L. and Y.Z.; software: C.J.; validation: H.G.; writing (original draft): X.L. and C.J.; writing (review and editing): X.L., C.J., and P.H. All the authors read and approved the final manuscript.

Funding: This research was funded by the National Natural Science Foundation of China (NSFC) under the grant number of 51505290 and 51877138.

Conflicts of Interest: The authors declare no conflict of interest.

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An All-Region State-of-Charge Estimator Based on Global Particle Swarm Optimization and Improved Extended Kalman Filter for Lithium-Ion Batteries

Xin Lai *, Wei Yi, Yuejiu Zheng * and Long Zhou

School of Mechanical Engineering, University of Shanghai for Science and Technology, Shanghai 200093, China; 13072182082@163.com (W.Y.); zhoulong925@126.com (L.Z.)

* Correspondence: laixin@usst.edu.cn (X.L.); yuejiu_zheng@163.com (Y.Z.); Tel.: +86-021-5527-5287 (X.L.)

Received: 29 October 2018; Accepted: 12 November 2018; Published: 14 November 2018

Abstract: In this paper, a novel model parameter identification method and a state-of-charge (SOC) estimator for lithium-ion batteries (LIBs) are proposed to improve the global accuracy of SOC estimation in the all SOC range (0–100%). Firstly, a subregion optimization method based on particle swarm optimization is developed to find the optimal model parameters of LIBs in each subregion, and the optimal number of subregions is investigated from the perspective of accuracy and computation time. Then, to solve the problem of a low accuracy of SOC estimation caused by large model error in the low SOC range, an improved extended Kalman filter (IEKF) algorithm with variable noise covariance is proposed. Finally, the effectiveness of the proposed methods are verified by experiments on two kinds of batteries under three working cycles, and case studies show that the proposed IEKF has better accuracy and robustness than the traditional extended Kalman filter (EKF) in the all SOC range.

Keywords: lithium-ion batteries; SOC estimator; parameter identification; particle swarm optimization; improved extended Kalman filter; battery management system

1. Introduction

Concerns about the impact of environmental degradation and the energy crisis have encouraged humans to develop new sustainable energy resources, and energy conversion and storage devices involving lithium batteries (LIBs), lead-acid batteries, nickel-cadmium batteries, fuel cells and supercapacitors, have become research hotspots [1–5]. Currently, LIBs have been regarded as the first choice for electric vehicles (EVs) because of their low self-discharge rate, high energy density, long lifespan and almost zero memory effect [6–9]. To ensure the safe operation of LIBs, an effective battery management system (BMS) was designed to provide monitoring and protection in EV applications [10,11]. One of the major functions of BMS is the real-time estimation of various battery states, such as state-of-charge (SOC), state-of-health [12] and state-of- energy [13]. For a BMS in EVs, one of the most important states is SOC, which indicates the remaining driving range. Therefore, accurate SOC estimation is of great significance to enhance the reliability and safety of EVs. In recent decades, SOC estimation techniques have been extensively reported by a number of researchers [14–16].

1.1. Review of SOC Estimation Approaches

The LIB is a dynamic nonlinear and time-varying system, and the SOC of a LIB cannot be measured directly. Thus, accurate SOC estimation is a cumbersome task [17]. In recent years, many studies have been devoted to developing methodologies for SOC estimation. Traditionally, frequently-used SOC estimation methods can be simply divided into two categories: non-model based methods and model-based methods [15,18]. As a non-model based method, the coulomb counting method is easy to

realize, however it suffers from the error accumulation problem caused by the initial value and current sensor errors [19]. For model-based methods, three key factors for obtaining an accurate SOC can be summarized, namely, a suitable model structure, matched model parameters and a robust estimation algorithm. In other words, the accuracy of the SOC estimation heavily depends on the battery model and estimator algorithm.

Due to a relatively simple mathematical structure and low computation burden, equivalent circuit models (ECMs) have become the most popular models utilized to describe the input/output behavior of LIBs through electrical circuits [20,21]. The commonly used ECMs are based on the RC networks with different orders. Obviously, the model structure and model parameters directly affect the model accuracy. Therefore, a model parameter identification algorithm is very important for improving the model accuracy. In existing studies, a variety of optimization algorithms have been used to identify model parameters of ECMs, such as the genetic algorithm (GA) [10], the particle swarm optimization (PSO) algorithm [22], and the least-squares method [23].

There is no doubt that the estimation algorithm is crucial to the SOC estimation accuracy. In the literature, several SOC estimation algorithms have been presented to improve the accuracy, reliability and robustness of estimation [24,25], such as the coulomb counting method, the open-circuit-voltage (OCV) method, the extended Kalman filter (EKF), fuzzy logic and the support vector machine [26], the proportional-integral (PI) observer [27], the Luenberger observer [28], the sliding mode observer [29] and the non-linear observers, multivariate adaptive regression splines [30], and bi-linear interpolation [31]. As the EKF is an optimum adaptive algorithm based on recursive estimation, it has attracted much attention [32]. However, the operation of the EKF assumes a Gaussian error distribution and the algorithm is inapplicable when the error distribution is non-Gaussian. In addition, as the EKF is based on ECM, the uncertainty of the ECM model parameters should be taken into consideration.

Previous studies have focused on the model parameter identification and the SOC estimation in a fixed range, little attention has been paid to the SOC estimation in the all SOC range (0–100%). In fact, the performance of the LIB in the all-region SOC is different. If the fixed model parameters are used for SOC estimation, the model error and SOC error may be very large. Moreover, Reference [33] confirmed that the model error of ECMs in the low SOC range (<20%) is much greater than that in the high SOC range, resulting in a large SOC estimation error based on the traditional EKF in the low SOC range. Therefore, it is necessary to develop an algorithm that can accurately estimate SOC in the low SOC range. In this study, an all-region model parameters identification method is proposed, and then a SOC estimator based on an improved EKF is developed to improve the accuracy of the SOC estimation in the all SOC range.

1.2. Main Contributions

This paper aims to develop a global parameter identification method and an all-region SOC estimator for the ECM. Specifically, the main contribution of this study is summarized as:

(1) A subregion identification method for model parameter of ECMs in the all-region SOC is proposed to improve the global model accuracy. In this method, the all-region SOC (0–100%) is divided into several subregions, and the parameters in each subregion are identified. Therefore, the model parameter of the all-region is composed of the model parameter of each subregion. Moreover, the optimal number of subregions is investigated to balance the model accuracy and computation time.

(2) An improved EKF-based SOC estimator with varying noise covariance is proposed to improve the accuracy of the SOC estimation in the all SOC range. ECM has a low model accuracy in the low SOC range, resulting in a large SOC estimation error based on the traditional EKF. The effectiveness of the proposed estimator in the all-region SOC is verified by experiments.

(3) Our proposed model parameter identification method and SOC estimator are evaluated by two kinds of batteries under three working cycles.

1.3. Organization of the Paper

The rest of this paper is structured as follows: Section 2 describes the experimental equipment and results. In Section 3, a novel model-parameter identification method in the all SOC range is proposed. Section 4 describes an improved EKF-based SOC estimator. In Section 5, case studies of two kinds of batteries under three working cycles are employed to verify the effectiveness of the presented method and algorithm. Finally, conclusions are summarized in Section 6.

2. Experiment

The schematic of the test bench is shown in Figure 1a. It consists of a battery tester made by DIGATRON (BTS-600) (Digatron Power Electronics, Aachen, Germany), a thermal chamber for environment control and a host computer for operation control and data display/storage. The battery tester can charge/discharge a battery according to the designed program in a software installed on the host computer. The errors of the current and voltage sensors are less than 0.1%. The measured data and control command are transmitted to the host computer through the TCP/IP protocol. The acquired data are used to determine model parameters and verify the proposed SOC estimator.

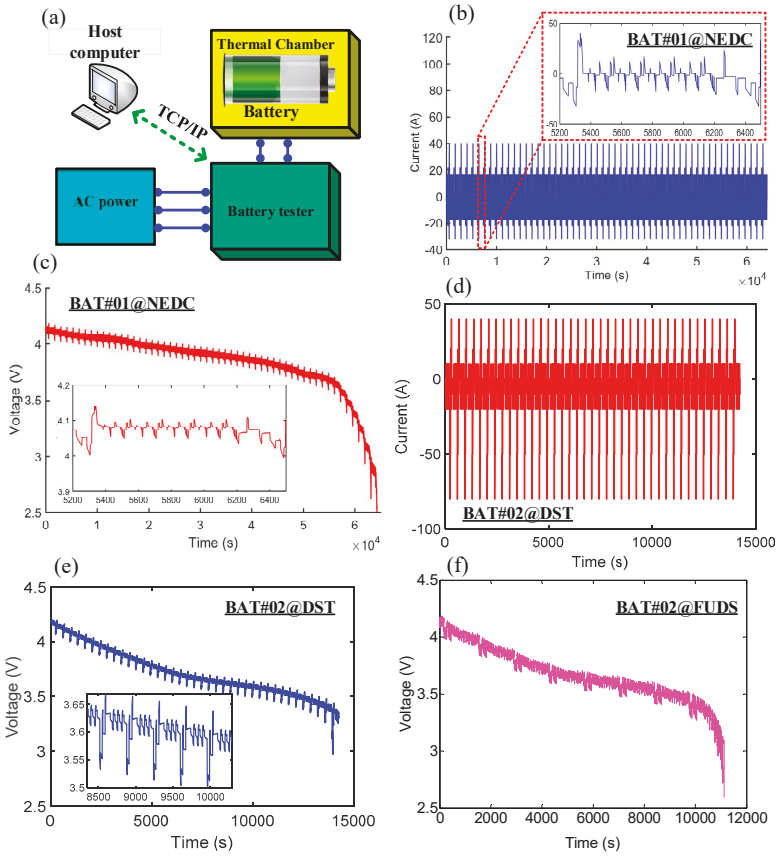


Figure 1. Battery test bench and experimental results under three working cycles. (**a**) Schematic of the test bench; (**b**) Current profile under the new European driving cycle (NEDC); (**c**) Voltage profile under the NEDC; (**d**) Current profile under the dynamic stress test (DST); (**e**) Voltage profile under the DST; (**f**) Voltage profile under the federal urban driving schedule (FUDS).

In order to fully verify the effectiveness of the proposed model identification method and SOC estimator, two types of batteries under three working cycles were selected for experiments. The main parameters of the two batteries are listed in Table 1. The experimental batteries were first fully charged and then discharged to the cut-off voltage under three working cycles, namely the new European driving cycle (NEDC), dynamic stress test (DST) and federal urban driving schedule (FUDS). The current and voltage during discharge were recorded, as shown in Figure 1b–f.

Moreover, the actual capacities and OCV curves of the test LIBs were determined by the standard capacity and hybrid pulse power characterization (HPPC) experiments. These experimental procedures are standard processes, which can be found in References [34,35].

Table 1. Main parameters of experimental battery.

	Nominal Capacity (Ah)	Lower Cut-Off Voltage (V)	Upper Cut-Off Voltage (V)	Maximum Charge Current (A)
BAT#01	32.5	2.5	4.15	65
BAT#02	40	2.8	4.2	100

3. Model and Parameter Identification

3.1. Equivalent Circuit Model

Reference [10] examined eleven ECMs and concluded that the first- and second-order RC models have the best balance of accuracy and reliability. Therefore, the 2RC model is used as the battery model for the parameter identification and SOC estimation in the all SOC range in this paper.

The model structure of 2RC is illustrated in Figure 2. In Figure 2, R_0 is equivalent to the Ohmic resistance, U_{OCV} is the voltage source, R_1 and R_2 are the diffusion resistances, and C_1 and C_2 are diffusion capacitances. The terminal voltages of the two series-connected RC circuits are denoted by U_1 and U_2, the current is denoted by I, and the terminal voltage is denoted by U_L.

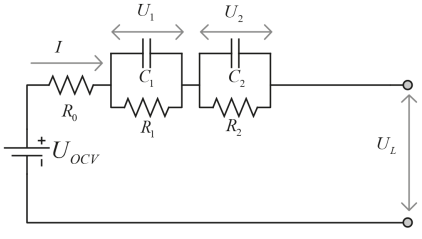


Figure 2. Model structure of 2RC.

Based on the circuit principle, the discretization equations of the 2RC model can be expressed as:

$$\begin{cases} U_L(k) = U_{OCV}(k) + I(k)R_0 + U_1(k) + U_2(k) \\ U_1(k+1) = U_1(k)e^{-\frac{\Delta t}{\tau_1}} + I(k)R_1\left(1 - e^{-\frac{\Delta t}{\tau_1}}\right) \\ U_2(k+1) = U_2(k)e^{-\frac{\Delta t}{\tau_2}} + I(k)R_2\left(1 - e^{-\frac{\Delta t}{\tau_2}}\right) \end{cases} \tag{1}$$

$$R_0 = \begin{cases} R_0^+ & i(k) \geq 0 \\ R_0^- & i(k) < 0 \end{cases} \tag{2}$$

where the subscript k denotes the time step, τ_1 and τ_2 are time constants of the RC network ($\tau_1 = R_1C_1$, $\tau_2 = R_2C_2$), Δt is the sampling period, and R_0^+ and R_0^- are the ohmic resistances during charging and discharging, respectively.

3.2. Model-Parameter Identification Based on Particle Swarm Optimization

To further improve the model accuracy, a suitable model parameter is essential. In the 2RC model, six parameters need to be determined, as is given in:

$$\theta = \left[R_0^+, R_0^-, \tau_1, R_1, \tau_2, R_2\right] \tag{3}$$

In this paper, the PSO algorithm is used to determine these model parameters in the all SOC range. The PSO algorithm is a global random search algorithm based on swarm intelligence, which simulates the migration and clustering behavior of birds in the process of foraging. The basic idea of the PSO is to find the optimal solution through cooperation and information sharing among individuals in the group [6,36–38]. The process of PSO can be briefly introduced as follows. In a D-dimensional search space, there are m particles. The position and velocity of the i-th particle ($1 \leq i \leq m$) can be expressed as $X_i = (X_{i1}, X_{i2}, \ldots, X_{iD})$ and $V_i = (V_{i1}, V_{i2}, \ldots, V_{iD})$, respectively. The best historical position of the i-th particle is expressed as $P_i = (P_{i1}, P_{i2}, \ldots, P_{iD})$, and the best position for all particles is expressed as $P_g = (P_{g1}, P_{g2}, \ldots, P_{gD})$. Then, particles update their speed and position according to the following expressions:

$$V_{iD}^{k+1} = \omega V_{iD}^k + c_1 r_1 \left(P_{iD}^k - X_{iD}^k\right) + c_2 r_2 \left(P_{gD}^k - X_{iD}^k\right) \tag{4}$$

$$X_{iD}^{k+1} = X_{iD}^k + V_{iD}^{k+1} \tag{5}$$

where ω is the inertia factor; k is the current iteration number; c_1 and c_2 are the acceleration constants; r_1 and r_2 are random numbers in range of (0, 1).

The pseudo codes of the PSO algorithm are listed in Algorithm 1. In the PSO, the root-mean-square-error (*RMSE*) between the model voltage and the measured voltage is used to establish the fitness function, which can be expressed as

$$M_{RMSE} = \sqrt{\frac{1}{n}\sum_{k=1}^{n}\left(u_k(\theta) - \hat{u}_k(\theta)\right)^2} \tag{6}$$

where M_{RMSE} represents the *RMSE* of the battery model, u_k represents the model terminal voltage, and $\hat{u}_k$ represents the measured voltage.

Algorithm 1. Pseudo-code of the PSO algorithm.

```
procedure PSO
  for each particle i
        Initialize velocity V_i and position X_i for particle i
        Evaluate particle i and set P_i = X_i
  end for
      gBest = min [21]
  while not stop
      for i = 1 to n
        Update the velocity and position of particle i using Equations (4) and (5)
        Evaluate particle i
            if fit (X_i) < fit (P_i)
          P_i = X_i;
          if fit(Pg) < fit (gBest)
            gBest = Pg;
        end for
   end while
end procedure
```

3.3. All-Region Parameter Identification of ECM

Obviously, the nonlinearity of the external characteristics of the battery is very serious. Therefore, if fixed model parameters are used in the all SOC range, the model error is very large. In other words, the model parameters optimized by PSO in the all SOC range (constant model parameters are obtained) are the global optimum solution, but is not the best solution for each subregion. The reason is that the model parameters should be changed with SOC rather than being invariable. Therefore, a subregion identification method was developed to find the optimal solution of each subregion in this study (variable model parameters are obtained). The optimal solution of each subregion constitutes the best solution of the whole SOC range. In other words, the model with variable parameters has smaller model errors than that with constant parameters in the whole SOC range. The schematic of our proposed method is shown in Figure 3. The battery model used in this method is the 2RC model, which is introduced in detail in Section 3.1.

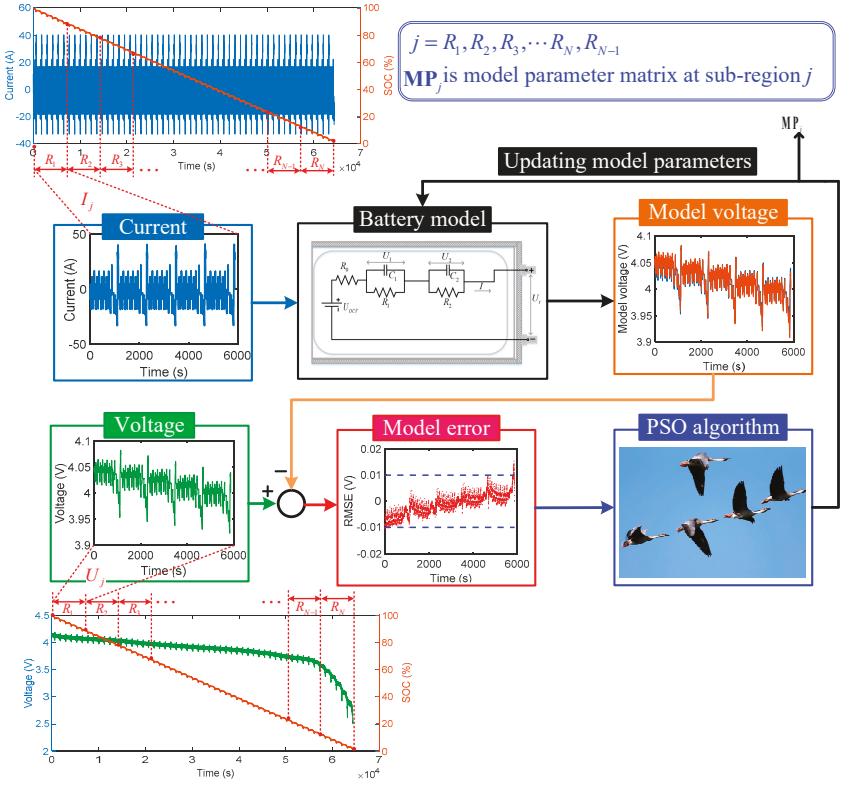


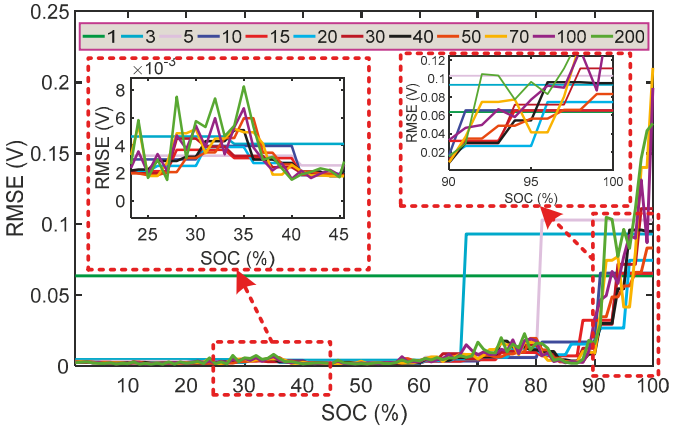
Figure 3. Framework of the parameter identification method of the equivalent circuit models (ECM) in the all state-of-charge (SOC) range.

The basic principle of the proposed method is as follows: the all SOC range (0–100%) is divided into N subregions, and the PSO algorithm is then used to identify the model parameters in each subregion. Therefore, *N* groups of model parameters are thereby obtained to form model parameters for the all SOC range. For the SOC estimation, the model parameters are selected based on the corresponding SOC range. This method of solving the optimal solution in each subregion to form the all-region solution can improve the accuracy of the model and lay a foundation for the accurate estimation of SOC. It should be noted that the real SOC is very difficult to obtain, so it is difficult to

accurately determine the SOC in each subregion, possibly resulting in the model parameters having errors. However, the model parameters are slow-varying and varied little in a small range. Therefore, the small model parameter error has little effect on the SOC estimation error. The flow of our method is as follows: firstly, the current SOC is obtained by the OCV-SOC curve, then the model parameters are obtained by judging the area in which the SOC is located. Finally, the SOC estimation is performed using our proposed estimator. Generally speaking, the SOC value obtained by the OCV-SOC curve may have an error, but the error is not very large. Therefore, the error of the model parameters obtained by our method is very small, and it is reasonable to use the SOC with a small error to query the model parameters.

As shown in Figure 3, the parameter identification process in each subregion is as follows. The input signal is the current, and the output signal of ECM is the model voltage based on the current model parameters. Then, the model error is obtained by comparing model voltage with measured voltage. Finally, model parameters are updated to pursue the minimum model error using PSO. When the optimal model parameters of the current subregion are identified, the optimal model parameters of the next subregion are solved until the model parameters of all regions are identified.

Obviously, the identification results are closely related to the value of the number of subregions (N). In order to investigate the relationship between model error, identification time and N values, we identified the model parameters under different N values. The identification process was run in MATLAB 2014b installed on a PC with 3.1 GHz CPU (Intel, Santa Clara, CA, USA) and 8 GB RAM (Kingston, Fountain Valley, CA, USA). The identification results are shown in Figures 4 and 5. Figure 4a shows the relationship between the *RMSE* and N under NEDC. It can be seen that the model error decreases with an increase in the value of N. However, the model error does not always decrease. When N is greater than 20, the model error will no longer decrease or even increase. Figure 4b shows the identification time under different N values. It can be seen that the identification time decreases with an increase in the value of N. The reason for this phenomenon can be expressed as follows: when N is small, the PSO algorithm takes a long time to find the optimal value in each subregion. When N is large, it is relatively easy for PSO to find the optimal solution. Therefore, the identification time becomes shorter. However, when N is greater than 20, the identification time is no longer reduced.



(**a**)

Figure 4. *Cont.*

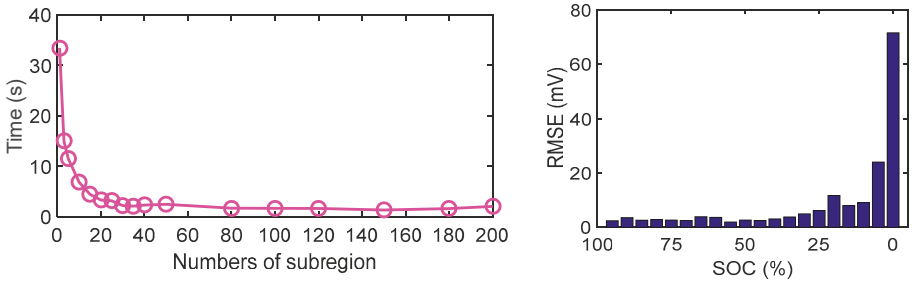


Figure 4. Identification results of BAT#01 under the new European driving cycle (NEDC). (**a**) Root-mean-square-error (*RMSE*) of the equivalent circuit models (ECM) under different *N* values. (**b**) Identification time under different *N* values. (**c**) Distribution of *RMSE* (*N* = 20).

To further clarify the relationship between model errors and the number of subregions, the parameter identification of another battery (BAT#02) under the DST and FUDS working cycles was carried out, and the identification results are shown in Figure 5. In Figure 5, the average *RMSE* is the average value of the *RMSE* of ECMs in the all SOC range. It can be seen that *N* = 20 is the best choice to balance the identification accuracy and the identification time under the DST and FUDS.

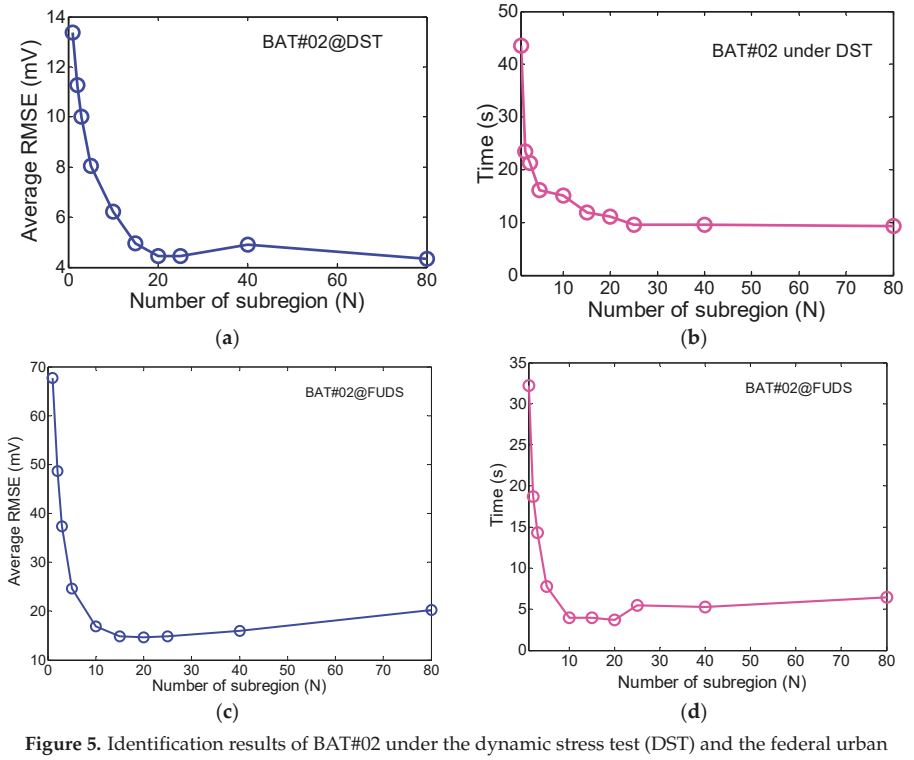


Figure 5. Identification results of BAT#02 under the dynamic stress test (DST) and the federal urban driving schedule (FUDS). (**a**) Relationship between average root-mean-square-error (*RMSE*) and *N* under the DST; (**b**) Relationship between identification time and *N* under the DST; (**c**) Relationship between average *RMSE* and *N* under the FUDS; (**d**) Relationship between identification time and *N* under the FUDS.

Based on the identification results of the above three working cycles, we can conclude that $N = 20$ is the best choice with the highest accuracy and the shortest identification time. Figure 4b shows the distribution of *RMSE* in the all SOC range ($N = 20$). It can be seen that the model has satisfactory accuracy in the high SOC range (20–100%), indicating the effectiveness of the proposed method. Table 2 lists the identification results of model parameters in the all SOC range. Note that the model error in the low SOC range (0–20%) is large, which is caused by the defects of the ECM. Therefore, model errors in the low SOC range need to be considered for an all-region SOC estimator.

Table 2. Identified parameters in all state-of-charge (SOC) range ($N = 20$).

SOC Range (%)	$R_0^+(\Omega)$	$R_0^-(\Omega)$	$R_1(\Omega)$	$\tau_1(s)$	$R_2(\Omega)$	$\tau_2(s)$
0–5	0.00151	0.00150	0.000802	25.96175	5.35×10^{-11}	910.1351
5–10	0.00142	0.00149	0.000144	4.291183	0.00089	36.14319
10–15	0.00128	0.00155	0.000428	7.268605	0.001204	76.50539
15–20	0.00142	0.00162	0.001829	292.5856	0.000979	26.74074
20–25	0.00130	0.00153	0.000559	11.88647	0.002403	149.2718
25–30	0.00136	0.00165	0.000891	29.3174	0.004348	725.8318
30–35	0.00137	0.00167	0.003932	493.7445	0.00058	18.99163
35–40	0.00139	0.00163	0.000674	23.38255	0.001858	363.3004
40–45	0.00130	0.00155	0.000478	12.50162	0.001385	152.1977
45–50	0.00118	0.00161	0.001177	172.2351	0.000491	11.14567
50–55	0.00139	0.00157	0.000675	23.54001	0.001762	262.7994
55–60	0.00143	0.00162	0.003075	609.9358	0.000921	37.09781
60–65	0.00132	0.00174	0.000826	34.21432	0.005307	862.0298
65–70	0.00130	0.00177	0.008134	766.7005	0.00057	18.45616
70–75	0.00144	0.00171	0.011066	934.3178	0.000646	23.98743
75–80	0.00130	0.00177	0.000409	8.049046	0.012025	788.1887
80–85	0.00133	0.00184	0.003062	377.0807	0.000918	32.84381
85–90	0.00169	0.00176	1.93×10^{-11}	307.087	0.016334	1000
90–95	0.00200	0.00168	0.067043	1000	0.003688	999.9995
95–100	0.00200	0.00200	0.082935	1000	0.064369	999.9998

4. An Improved EKF-Based SOC Estimator in the All SOC Range

4.1. EKF-Based SOC Estimator

The EKF is robust against modeling uncertainty, linearization error, and process and measurement noise. Therefore, the EKF is very suitable for the SOC estimation of LIBs. The schematic of the EKF-based SOC estimator is shown in Figure 6.

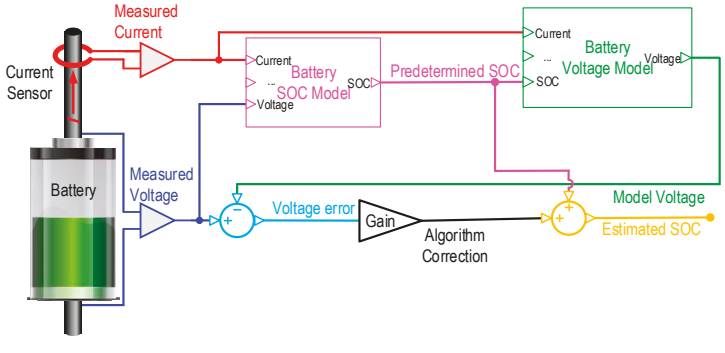


Figure 6. Schematic of the extended Kalman filter (EKF)-based state-of-charge (SOC) estimator.

For the 2RC model, the state variable x can be written as:

$$x = [SOC,\ U_1,\ U_2]^T \tag{7}$$

From Equations (2)–(4), the following expressions can be obtained:

$$f(x_k, u_k) = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \exp(-\Delta t/\tau_1) & 0 \\ 0 & 0 & \exp(-\Delta t/\tau_2) \end{bmatrix} \begin{bmatrix} \mathrm{SOC}_{EKF,k} \\ U_{1,k} \\ U_{2,k} \end{bmatrix} + \begin{bmatrix} -\eta \Delta t/C_n \\ R_1(1-\exp(-\Delta t/\tau_1)) \\ R_2(1-\exp(-\Delta t/\tau_2)) \end{bmatrix} I_k \tag{8}$$

$$g(x_k, u_k) = U_{OCV}(\mathrm{SOC}_{EKF,k}) - I_k R_0 - U_{1,k} - U_{2,k} \tag{9}$$

where Δt is the sample period.

According to References [39,40], the standard EKF equations for the battery system are listed in Algorithm 2. Note that the Kalman gain $\mathbf{L}_k^x$ mainly depends on the comparison between the input noise covariance Σ_w and the output noise covariance Σ_v, thus choosing these two noise covariances properly has a great influence on the accuracy of the SOC estimation.

Algorithm 2. Summary of the extended Kalman filter (EKF)-based state-of-charge (SOC) estimator.

Definitions:

The nonlinear state-space model:

$$\begin{cases} x_{k+1} = f(x_k, u_k) + w_k \\ y_k = g(x_k, u_k) + v_k \end{cases}$$

where x is the system state vector, $f(x_k, u_k)$ is a state transition function and $g(x_k, u_k)$ is a measurement function, w_k is the unmeasured process noise and v_k is the measurement noise.

Initialization:

$\hat{\mathbf{x}}_0^+ = E[\hat{\mathbf{x}}_0]$, $\sum_{x,0}^+ = E\left[\left(\mathbf{x}_0 - \hat{\mathbf{x}}_0^+\right)\left(\mathbf{x}_0 - \hat{\mathbf{x}}_0^+\right)^T\right]$

Computation:

Time update:

$\hat{\mathbf{x}}_k^- = f\left(\hat{\mathbf{x}}_{k-1}^+, u_{k-1}\right) + \mathbf{w}_{k-1}$; $\sum_{x,k}^- = \mathbf{A}_{k-1}\sum_{x,k-1}^+ \mathbf{A}_{k-1}^T + \sum w$.

Measurement update:

Error innovation: $e_k = y_k - \hat{y}_k = y_k - g\left(\hat{\mathbf{x}}_k^-, u_k\right)$.

Estimator gain matrix: $\mathbf{L}_k^x = \sum_{x,k}^- \left(\mathbf{C}_k^x\right)^T \left[\mathbf{C}_k^x \mathbf{X}_k^x \sum_{x,k}^- \left(\mathbf{C}_k^x\right)^T + \sum_v\right]^{-1}$

Measurement update: $\hat{\mathbf{x}}_k^+ = \hat{\mathbf{x}}_k^- + \mathbf{L}_k^x[y_k - \hat{y}_k]$

Error covariance measurement update: $\sum_{x,k}^+ = \left(\mathbf{I} - \mathbf{L}_k^x C_k^x\right)\sum_{x,k}^-$

where $\mathbf{A}_k = \left.\frac{\partial f(x_k,u_k)}{\partial x}\right|_{x=\hat{x}_k^+}$, $\mathbf{C}_k = \left.\frac{\partial g(x_k,u_k)}{\partial x}\right|_{x=\hat{x}_k^-}$

4.2. An Improved EKF-Based SOC Estimator

Section 3.3 indicates that the ECM has low accuracy in the low SOC range. Therefore, the SOC error obtained by the traditional EKF is large. To solve this problem, an improved EKF (IEKF)-based SOC estimator is proposed in this paper. The expression of $\mathbf{L}_k^x$, the relative ratio of Σ_w and Σ_v, determines the performance of the EKF algorithm. Figure 7 shows the SOC and SOC error based on the EKF with different distributions of noise covariance under the NEDC, FUDS and DST working cycles (capacity error is set to 0.5%). The calculation results of the three working cycles show that the SOC estimated value is more inclined to the SOC value obtained by the ampere-hour (AH) method when the Σ_w is smaller and the Σ_v is larger, while the estimated value is more inclined to the SOC estimated value obtained by the normal EKF when the Σ_w is larger and the Σ_v is smaller. As shown in Figure 4a, the model error is very large in the low SOC range, resulting in a large SOC estimation error based on the traditional EKF. At this time, the SOC estimation value obtained by the AH method is more reliable, because the AH method is not affected by the ECM error. Therefore, a smaller Σ_w value

and a larger Σ_v value should be used. When the model error is small, it indicates that the battery is in the high SOC range, and Σ_w and Σ_v should return to the normal value.

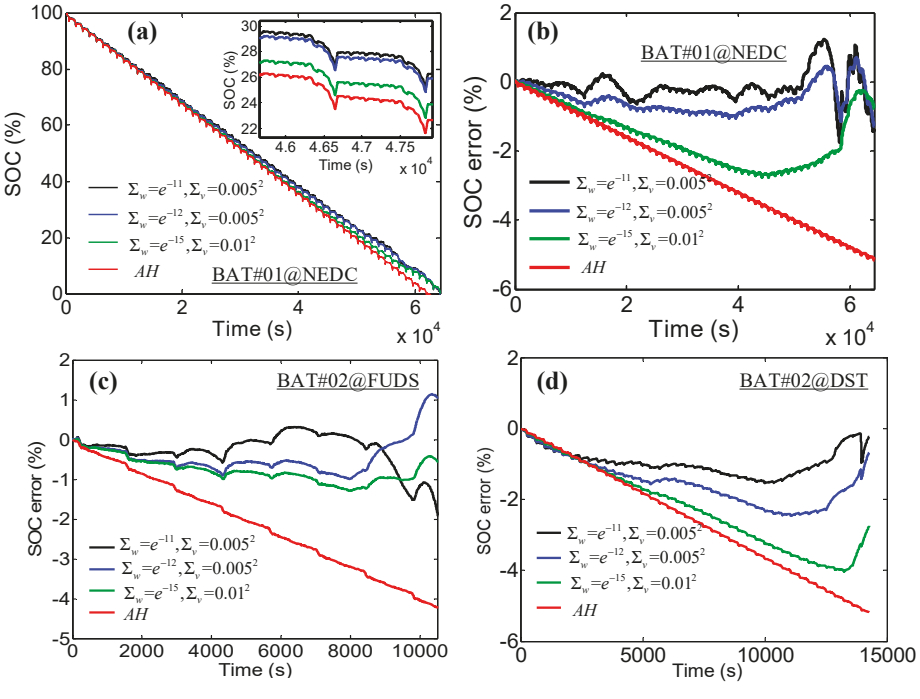


Figure 7. State-of-charge (SOC) and SOC error based on the extended Kalman filter (EKF) with different distributions of noise covariance under three working cycles (capacity error is set to 0.5%). (**a**) SOC of BAT#01 under the new European driving cycle (NEDC); (**b**) SOC error of BAT#01 under NEDC; (**c**) SOC error of BAT#02 under the federal urban driving schedule (FUDS); (**d**) SOC error of BAT#02 under the dynamic stress test (DST).

When the accuracy of the ECM is insufficient in the low SOC range, the IEKF algorithm is more confident in the estimation value using the AH method. Therefore, the accuracy of the AH method directly affects the SOC estimation accuracy in the low SOC range. The error sources of the AH method include capacity error, coulombic efficiency error, measured current error, self-discharge etc. The specific influence of these factors on the AH method is as follows.

(a) Case 1: the capacity error is 5%. Figure 8 shows that the maximum incremental error of the SOC caused by the AH method in this case is 1% in the low SOC range (0−20%).

(b) Case 2: the coulomb efficiency error is 0.1%. Figure 8 shows that the maximum incremental error caused by the AH method in this case is 0.1% in the low SOC range.

(c) Case 3: the drift of the measured current is 100 mA, and the self-discharge is 1 mA. Figure 8 shows that the maximum incremental error in this case is less than 1%.

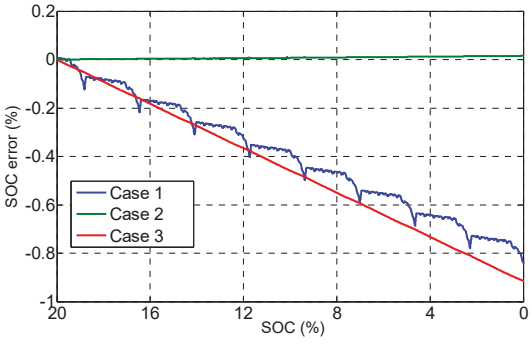


Figure 8. Calculation of the state-of-change (SOC) error source based on the ampere-hour (AH) method.

In summary, the maximum incremental error caused by the AH method cannot exceed 2.0% in the all low SOC range even if the above assumptions are superimposed. Therefore, our proposed method is useful for improving the accuracy of SOC estimation in low SOC range.

However, the exact Kalman noise covariance cannot be directly obtained. In this paper, we take the model error (M_{RMSE}) as the reference signal. The model error is obtained by comparing the measured voltage with the one obtained by the model. From Section 3.3, we can see that the low SOC range is 20% of the all-region SOC. Therefore, the cumulative error caused by the AH method is small, and once the normal EKF algorithm is returned, the initial error can be eliminated. The values of Σ_w and Σ_v are listed in Equation (10). The proposed method improves the SOC estimation accuracy in the all SOC range by adjusting the distribution of noise covariance according to the model error in real time.

$$(\Sigma_w, \Sigma_v) = \begin{cases} (e^{-11}, 0.005^2) & M_{RMSE} \leq 0.003V \\ (e^{-12}, 0.005^2) & 0.003V < M_{RMSE} \leq 0.006V \\ (1e^{-15}, 0.010^2) & 0.006V < M_{RMSE} \leq 0.009V \\ (e^{-50}, 1.000^2) & M_{RMSE} > 0.009V \end{cases} \tag{10}$$

5. Results and Discussion

5.1. Case Studies under NEDC

To verify the effectiveness of the proposed all-region model-parameter identification and SOC estimator, the SOC is estimated under various cases using the experimental data in Section 2. The estimated results are shown in Figure 9. Figure 9a shows the SOC estimation error in ideal conditions. In this paper, the ideal condition means there is no capacity error and sensor measurement error. The results indicate that the proposed IEKF algorithm has much higher accuracy in the low SOC range than the EKF algorithm, and has almost the same accuracy in the high SOC range. Figure 9b shows the SOC error is under 5% of the capacity error, indicates that the IEKF algorithm is better than EKF in the all SOC range. In practical applications, the errors of current sensor and voltage sensor exist. Figure 9c shows the SOC error of two algorithms under a current error of 32.5 mA noise and 32.5 mA drift (0.1% full scale of current sensor). Figure 9d shows the SOC error under a voltage error of 10 mV noise and 5 mV drift. Table 3 lists the *RMSE* of the SOC in the all SOC range. Case studies show that the SOC error obtained by EKF and IEKF is almost the same in the high SOC range (SOC $\geq$ 20%). However, the SOC error obtained by IEKF is obviously smaller than that by EKF in the low SOC range (SOC < 20%). Figure 10 shows the SOC estimation result under NEDC in the all SOC range. It is obvious that the SOC obtained by the IEKF tracks the real SOC better than that obtained by the EKF. Moreover, our proposed IEKF only adjusts the distribution of noise covariance on the basis of the

traditional EKF. Therefore, the computation times of IEKF and EKF are almost the same. Through the above analysis, we can conclude that our proposed IEKF is better than the traditional EKF in the all SOC range.

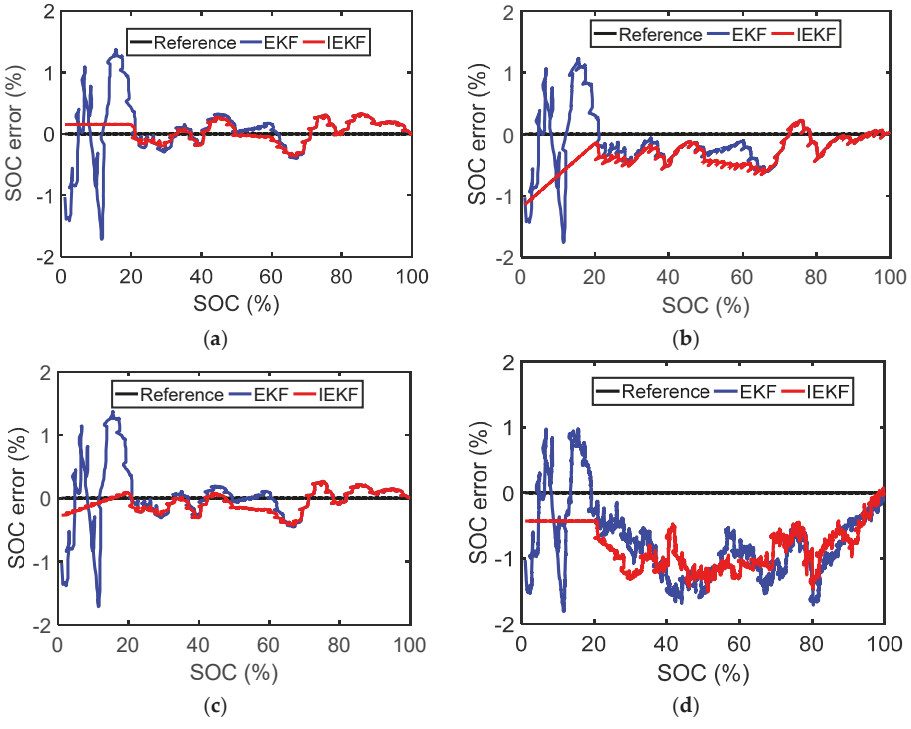


Figure 9. The state-of-change (SOC) estimated error comparison in the all-region SOC under the new European driving cycle (NEDC). (**a**) Case A: SOC error in ideal condition; (**b**) Case B: SOC error under 5% capacity error; (**c**) Case C: SOC error under current error of 32.5 mA noise and 32.5 mA drift; (**d**) Case D: SOC error under voltage error of 10 mV noise and 5 mV drift.

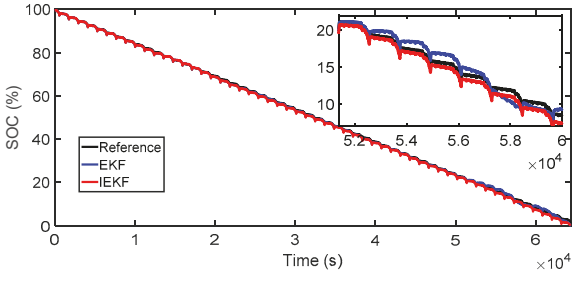


Figure 10. State-of-change (SOC) estimation results under the new European driving cycle (NEDC) in the all-region SOC (capacity error is set to 6%, current error is 50 mA noise and 50 mA drift).

Table 3. Root-mean-square-error (*RMSE*) in the all state-of-change (SOC) range.

Case	EKF	IEKF
Case A	0.43%	0.17%
Case B	0.44%	0.41%
Case C	0.57%	0.44%
Case D	1.47	1.25%

5.2. Additional Validation under the DST and FUDS Working Conditions

In order to further verify the reliability and accuracy of the proposed algorithm, verification on another battery (BAT#02) under the DST and FUDS is performed. The results are shown in Figure 11. It can be seen that the accuracy of our proposed IEKF is higher than that of EKF under the DST and FUDS in the all-region SOC.

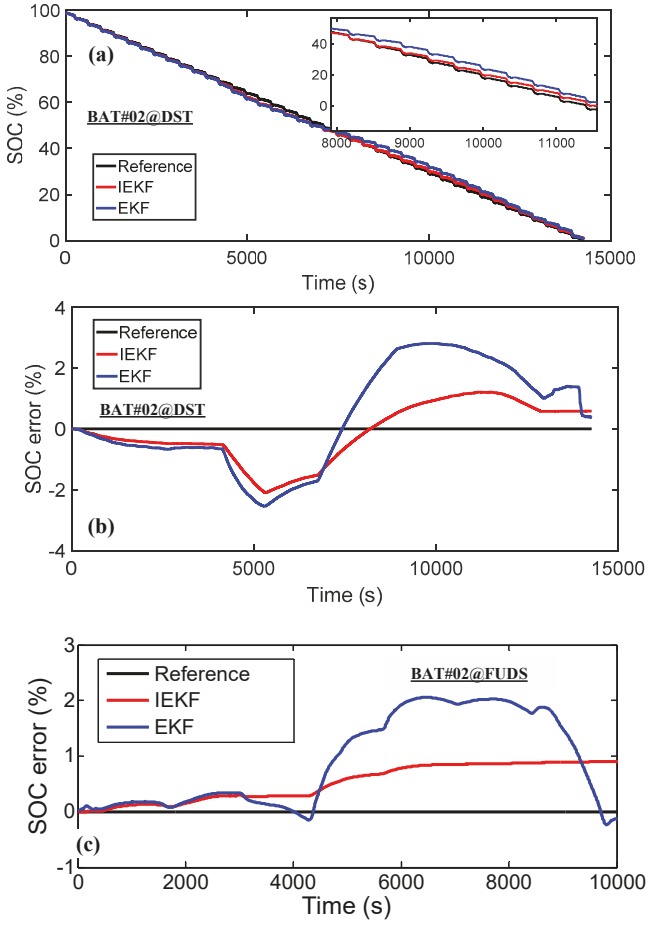


Figure 11. State-of-change (SOC) estimation results of BAT#2 under the dynamic stress test (DST) and the federal urban driving schedule (FUDS) in the all SOC range. (**a**) SOC estimation value under the DST; (**b**) Estimation error under the DST; (**c**) Estimation error under the FUDS.

In conclusion, the effectiveness of the proposed parameter identification method and SOC estimator are verified by case studies under NEDC, DST and FUDS working conditions, and the accuracy and reliability of IEKF are better than traditional EKF in the all SOC range.

6. Conclusions

In this paper, a model parameter identification method was proposed to improve the global model accuracy for the ECM. Then, an improved EKF-based SOC estimator with varying noise covariance was developed to improve the SOC estimation accuracy in the low SOC range, which can solve the problem of a low estimation accuracy of traditional EKF based on the ECM in the low SOC range. The experimental results of two kinds of batteries under the NEDC and DST working cycles show that: (1) the proposed parameter identification method of ECM can achieve global optimum in the all SOC range, and the model error is within 10 mV when the SOC ranges from 100% to 20%. Moreover, the model accuracy does not always improve by increasing the number of subregions (N). Conversely, the model accuracy no longer increases or even decreases when N increases to a certain value. Our investigation shows that $N = 20$ is the best choice with the highest accuracy and the shortest identification time; (2) the SOC estimation error is within $\pm 1\%$ in the all SOC range, indicating that the proposed IEKF has better accuracy and reliability than the traditional EKF.

It should be noted that our proposed method and algorithm are only verified by experiments in the DST and NEDC working cycles. However, the results can provide valuable references for the battery model parameter identification and SOC estimation in real applications. The application of the proposed method and algorithm in real EVs will be our future research work.

Author Contributions: All authors contributed to the paper. Conceptualization, X.L. and Y.Z.; data curation, W.Y. and L.Z.; investigation, X.L.; methodology, X.L.; project administration, X.L. and Y.Z.; software, X.L.; validation, X.L.; writing (original draft), X.L. and W.Y.; writing (review and editing), X.L. and Y.Z.

Funding: This research was funded by the National Natural Science Foundation of China (NSFC) under the grant number of 51505290 and 51507102.

Conflicts of Interest: The authors declare no conflicts of interest.

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electronics

MDPI

Review

SoC Estimation for Lithium-ion Batteries: Review and Future Challenges

Juan Pablo Rivera-Barrera [1,*], Nicolás Muñoz-Galeano [1] and Henry Omar Sarmiento-Maldonado [2]

[1] Research Group in Efficient Energy Management, GIMEL, Universidad de Antioquia, Medellín 050010, Colombia; nicolas.munoz@udea.edu.co

[2] Research Group in Control, Automation and Robotics, ICARO, Politécnico Colombiano Jaime Isaza Cadavid, Medellín 050022, Colombia; hosarmiento@elpoli.edu.co

* Correspondence: jpablo.rivera@udea.edu.co; Tel.: +57-3013753205

Received: 18 October 2017; Accepted: 8 November 2017; Published: 23 November 2017

Abstract: Energy storage emerged as a top concern for the modern cities, and the choice of the lithium-ion chemistry battery technology as an effective solution for storage applications proved to be a highly efficient option. State of charge (SoC) represents the available battery capacity and is one of the most important states that need to be monitored to optimize the performance and extend the lifetime of batteries. This review summarizes the methods for SoC estimation for lithium-ion batteries (LiBs). The SoC estimation methods are presented focusing on the description of the techniques and the elaboration of their weaknesses for the use in on-line battery management systems (BMS) applications. SoC estimation is a challenging task hindered by considerable changes in battery characteristics over its lifetime due to aging and to the distinct nonlinear behavior. This has led scholars to propose different methods that clearly raised the challenge of establishing a relationship between the accuracy and robustness of the methods, and their low complexity to be implemented. This paper publishes an exhaustive review of the works presented during the last five years, where the tendency of the estimation techniques has been oriented toward a mixture of probabilistic techniques and some artificial intelligence.

Keywords: energy storage; lithium-ion battery; battery management system BMS; battery modeling; state of charge SoC

1. Introduction

Two main industrial applications require high technology systems in energy storage: smart grids and electric vehicles (EVs) [1]. LiBs look likely to replace lead acid batteries (PbAB) and become the preferred power supply for EVs due to their advantages of large capacity, long cycle life, and no memory [2]. However, LiBs require special handling to avoid deterioration of battery performance and prevent situations that could result in severe damage or explosions. So, LiBs technology requires careful monitoring and regulation. The SoC is one of the most important states to be tracked in a battery to optimize the performance and extend the lifetime of batteries [3]. SoC is defined as the rate of the available capacity to its maximum capacity when a battery is completely charged, and describes the remaining percentage of battery capacity. The monitoring and regulation of the states of batteries are done by a BMS that uses a battery analytical model and consists of hardware and software for battery management. It includes, among others, algorithms to determine the battery's more critical states. For EV applications, batteries must not only deliver a certain amount of energy to the drive train during operation but also provide power in different road situations. For this reason, it is essential to know the maximum power that can be delivered to and from the battery by charging or discharging, respectively, with SoC being needed for making decisions concerning the operation.

Batteries' operation can be modeled to find and monitor their states, mainly the SoC. The literature reports different approaches [4]. Most of those approaches simultaneously use a model of the battery with an algorithm to estimate the SoC [5–7], while a few others use separate methods [8,9]. It is important to consider that neither models nor methods are able to fulfill the performance required by demanding applications [10]. Therefore, the selection of the appropriate algorithm is up to the designer. To this aim, this paper presents a review of the main proposals in the literature in recent years for SoC estimation. This review can help the designer with choosing the most convenient approach.

This paragraph has as its main goal to show the most recent reviews of SoC estimation. A chapter of a book reported in [11] includes a brief review of SoC estimation techniques. Although this is a 2017 publication, its bibliographical revision for SoC techniques only includes 27 references to websites, journals, transactions, and conference proceedings that were published between 1998 and 2013. A review of SoC estimation for LiBs in electric and hybrid electric vehicles (HEVs) was published in [4]. While 59% of the references cited in this journal correspond to approaches for SoC estimation, the remaining papers refer to the estimation of other states of the battery. The focus of [4] was to present the strengths and weaknesses of the approaches rather than to describe their respective techniques in detail, and of all the references concerning SoC, just 20% correspond to 2013 studies, and 15% to 2012 studies. The remaining 65% of references date to 2011 or earlier. For EVs and HEVs, the trend is now towards the design of intelligent BMS, which involves research into intelligent-adaptive SoC estimation methods [12]. This is because it has been shown that, to get the best results for building a perfect lifetime calendar of the battery, a mix of adaptive systems should be used [13]. In [4], just 18% of SoC-related references correspond to adaptive systems such as fuzzy logic, artificial neural networks, ANN, fuzzy based neural networks, and support vector machines. On the other hand, [4] has not mentioned references to other techniques that have been applied in the last five years related to the use of evolutionary computing such as genetic algorithms and other hybrid methods [10]. In the same way, [14] presents a SoC estimation review for LiBs with only 80 references, 78% of which are from 2013 and earlier. The SoC estimation review presented in [14] is inaccurate when it presents the "Internal Resistant Method" as one of the conventional SoC estimation techniques since this is not now used for SoC estimation due to the difficulty of monitoring the resistance because it changes slightly with a wide range of SoC [15]. The work presented in [14] does not give an explanation of the methodologies proper for each method and in the classification marked "other techniques", all the mentioned references are from 2013 or earlier. The SoC estimation review presented in [16] makes a list of the techniques used until 2014 to estimate SoC, but it is limited to listing techniques; although it cites 81 references, it does not describe methodologies or indicate advantages or disadvantages. Recently, an overview of online implementable SoC estimation methods for LiBs was published in [17]. It only considers those techniques that can be implemented online and is limited to presenting the basic concepts related to Coulomb counting, open circuit voltage, and impedance spectroscopy. Also, it concentrates only on listing model-based methods. The current trend of using artificial intelligence in SoC estimation is only quoted by mentioning artificial neural network-based methods. The research developed in [17] is an overview based on 54 references that briefly describe just five of the SoC estimation methods.

Due to the trend in SoC estimation techniques before 2013 presented in [4], and due to the fact that the trend over the last five years has been towards the inclusion of some probabilistic techniques or artificial intelligence to improve the performance of estimation algorithms, this paper presents an exhaustive review of the SoC estimation methods published since 2013 and gives a description of each of those methods according to a general classification, presenting the main drawbacks. The descriptions of the SoC estimation methods, which may be complex for a designer who is starting out in the field of LiBs states estimation, are presented in a complete but simple way with original diagrams of this review.

According to the searches done in the databases IEEE Xplore digital Library and Science Direct Elsevier's platform, with the search criterion "state of charge estimation in batteries" since 2013, 433 and

270 publications, respectively, have appeared in this field. This review considered only those that present techniques applicable to LiBs and also emphasize SoC estimation methodologies. On the other hand, those references that were limited to using a SoC estimation methodology originally presented in another publication, without contributions, were discarded. So, SoC estimation classification methods in this review are based on 145 references published in the last five years; 57% of those cited references correspond to journals and transactions, 39% to conferences, and the remaining 4% to other sources like magazines, books, theses, and proceedings. The paper is organized as follows: In Section 2 some important definitions related to battery terminology are explained. Section 3 presents an overview of battery modeling techniques. Section 4 is dedicated to presenting the technique used for each method and its classification. Finally, Sections 5 and 6 are dedicated to a discussion of future challenges, and conclusions, respectively.

2. Battery Management Systems (BMS)

A BMS is a device that is built with hardware and software that control the operational conditions of the battery to prolong its life, guaranteeing its safety and providing an accurate estimation of the different states of the battery for the energy management modules. To meet this, a BMS has several features to control and monitor the states of the battery at different battery cell, battery module, and battery pack levels [1].

The capability of a battery to store energy decreases over its lifetime. State of health (SoH) is an indicator of this deterioration. The remaining useful life (RUL) is the remaining time or number of load cycles until the battery reaches its end of life (EoL). A BMS must be not only a protection circuit but also a thorough and accurate device that can predict the SoC, SoH, RUL, capacity, and available power, to increase the efficiency and the safety of the battery. By continuously measuring current, voltage, and temperature in batteries, the aforementioned parameters can be estimated. The estimation of the SoC is key in a BMS, but its online and accurate estimation remains a challenge due to strong nonlinear and complex electrochemical reactions in the battery and because battery characteristics change with aging [18].

The literature reports many different approaches to designing a BMS depending on the functionalities desired for the specific application, but most of them focus on a certain function of BMS, such as SoC estimation [10,19–22], or the balancing process [23–28]. Few studies present research concerning BMS from a global perspective like in [29], which displays an entire BMS design adopting a distributed structure to reach better scalability and portability. As mentioned, for EVs and HEVs the trend is now towards the design of intelligent BMS ,which involves research areas in artificial intelligence applied for the battery state estimation [12]. A predictive and adaptive BMS based on models is especially important for large battery packs for applications such as EVs and grid integration [30–33]. In the work presented in [34], a BMS is designed based on a seventh-order, single particle battery model with electrolyte diffusion and temperature-dependent parameters that take advantage of the response variations of the Li ion cell with temperature, but focus their efforts on SoC estimation.

3. Battery Modeling

A battery model is used to study the relationship between the external characteristics and the internal states of a battery by establishing a mathematical model. In order to use methods for SoC estimation, first a cell model in a discrete-time state-space form is needed [35]:

$$x_{k+1} = A_k x_k + B_k u_k + w_k \tag{1}$$

$$y_k = C_k x_k + D_k u_k + v_k, \tag{2}$$

where $x_k \in R^n$ is the system state vector at discrete-time index k. The vector $u_k \in R^p$ is the measured exogenous system input and a known/deterministic input to the system at time k. $w_k \in R^n$ is the

unmeasured stochastic "process noise" that affects the system state. The system output is $y_k \in R^m$ and is obtained by a linear combination of states and inputs, plus $v_k \in R^m$, which models the measurement noise and affects the measurement of the system output in a memory-less way, but does not affect the system state. If the requirements of the model need to consider the nonlinear components of the system, the model can be expressed as:

$$x_{k+1} = f(x_k, u_k) + w_k \tag{3}$$

$$y_k = g(x_k, u_k) + v_k. \tag{4}$$

These models (Equations (1)–(4)) update its own state and output values based on its input. Equations (1) and (3) are called the "system equation" and capture the evolving system dynamics. System stability, dynamic controllability, and sensitivity to disturbance may all be determined from these two equations. Equations (2) and (4) are called the "measurement equation," while the matrices $A_k \in R^{nxn}, B_k \in R^{nxp}, C_k \in R^{mxn}$ and $D_k \in R^{mxp}$, describe the dynamics of the system and are possibly time-varying depending on the particular battery model technique used. The functions $f(x_k,\ u_k)$ and $g(x_k,\ u_k)$ also describe the dynamics of the system and are nonlinear functions specified by the particular battery model technique used. Every particular battery model technique prescribes estimating parameters that may not be directly measured. Equations (1) and (2) are illustrated in the block diagram of Figure 1, and for the nonlinear case, Equations (3) and (4) are illustrated in the block diagram of Figure 2.

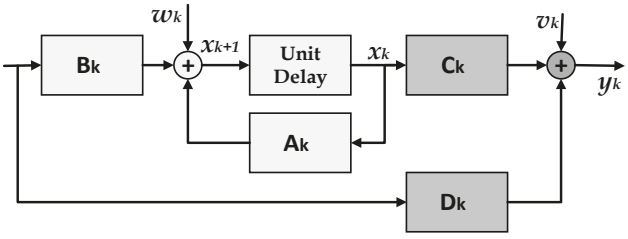

Figure 1. Linear discrete-time system from Equations (1) and (2).

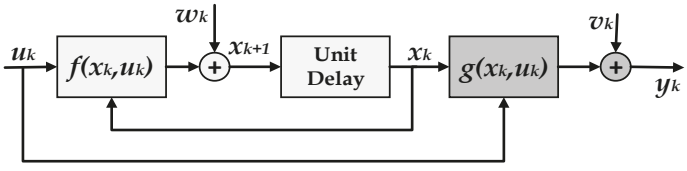

Figure 2. Nonlinear discrete-time system from Equations (3) and (4).

Commonly used battery cell model techniques that fit Equations (1)–(4) are mainly electrochemical and electric circuit models. Electrochemical models are suitable for predicting quantities at both the macroscopic and microscopic level, but these models have high computational complexity, presenting difficulties in obtaining parameters, and the equations can only be solved using specialist software [36]. The equivalent electric circuit model (ECM) based on external dynamic characteristics can simulate the working characteristics of different kinds of batteries, thereby avoiding detailed calculations of internal electrochemical processes. This review shows that ECM is commonly used as a base for SoC estimation, mainly the resistance–capacitance (RC) network-based ECM, which consists of voltage sources, resistors, and capacitors to form a circuit network. ECM and electrochemical models (EChM) will be examined in detail in Section 4.2.1.

As hundreds of single cells are connected in parallel and series to compose a battery pack and provide energy that can meet the requirements of an application like a smart grid or EV, a whole battery pack model is required. The similarity principle cannot be simply implemented from a single cell to the battery pack because of cell inconsistencies and mechanical integrity influences [37]. If cell inconsistencies are considered, describing every individual cell with its unique ECM and parameters is desirable. However, it takes time to experiment on every individual cell to fit a precise ECM, and a complete model for a large number of cells would become quite complex. The approach presented in [37] uses a Thevenin ECM for every single cell in an array of more than 90 series-connected cells, and this model is used to identify the internal resistance of each cell. Similarly, in [38] a Thevenin model that uses two different branches (for charge and discharge) is connected in series n times to represent n cells in a series-connected battery pack. Russu et al. in [38] present the model equations for n cells, and these equations are included as a single system by using Equations (1) and (2)

4. Methods for SoC Estimation

SoC represents the available battery capacity that can be withdrawn from the battery and is used to prevent its over-discharge or over-charge as well as to operate the battery in such a manner that aging effects are reduced. SoC estimation has drawn the attention of many researchers, and many different methods have been proposed [18]. To make a classification of the methods is not an easy task because most approaches point to the combination of two or more methods and the inclusion of different heuristic or deterministic mathematical tools. This review will show that it is common to find a mix of both open circuit voltage (OCV) and coulomb counting (CC) methods. It is common for these combinations to involve a variety of improvements in the initial and online SoC estimation since methods applied separately can suffer from some inaccuracies. For example, [8] combined the algorithm OCV method, a full charge detector/dynamic load observer, and, as the key function, the CC method with robust extended Kalman filter algorithm (REKF). These combinations make it harder to sort out each approach into a specific method classification. However, based on the classification made in [4], and from the published literature on this topic in the last five years, this review proposes two categories (direct and indirect methods), and several subcategories that summarize trends in SoC estimation. Figure 3 displays a summary of these categories with their main drawbacks.

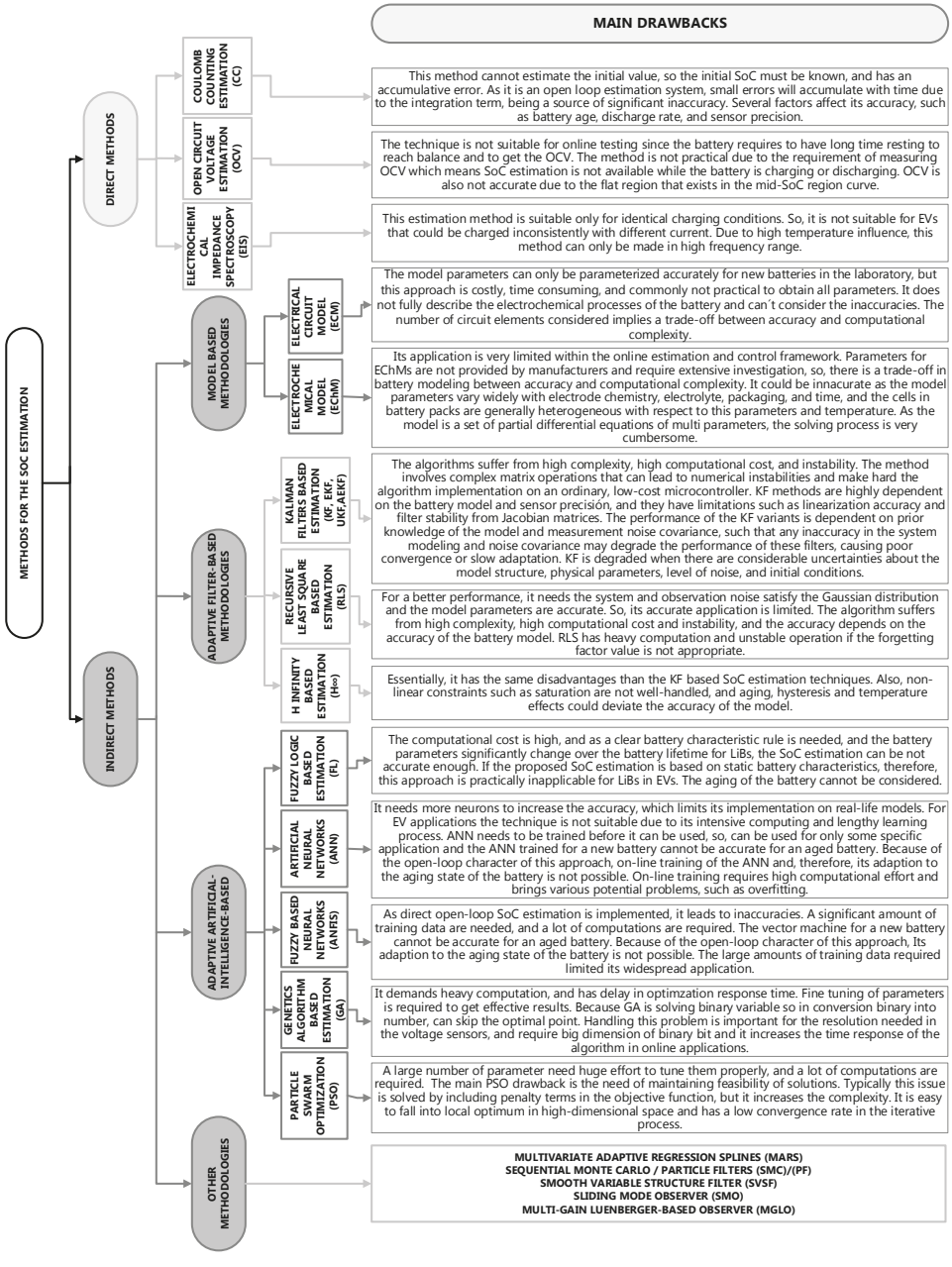

Figure 3. Summary of methods for the SoC estimation and main disadvantages.

4.1. Direct Methods

Direct SoC estimation methods use and measure physical battery properties such as voltage, current, and temperature, and then, by using an equation or relationship, the SoC can be estimated.

4.1.1. Coulomb Counting Estimation (CC)

CC has been standardized in the industry as an SoC estimation method [39]. At present, the CC method (also known as the ampere-hour balancing method), is the most used method for SoC estimation since it is the most accurate technique for short-term calculations. The CC method defines SoC as [8]:

$$SoC(t) = SoC(t_0) + \frac{1}{C_n}\int_{t_0}^{t_0+t} I_{bat}(d\tau) \times 100\%, \quad (5)$$

where $SoC(t_0)$ is the initial SoC, C_n the nominal capacity, and I_{bat} is the charging/discharging current. CC is a simple method, but has problems such as an initial value error and accumulated errors, so it is necessary to take into account the following issues: The measurement of battery current can contain measurement errors and abundant measurement noise. Errors due to noise and the wide range in sensors' resolution or rounding lead to accumulated errors and Equation (5) will gradually lose precision, so supporting algorithms are necessary. The initial SoC may not be known in practice and to define the SoC of a battery is only feasible when the battery system is in thermodynamic equilibrium [40].

CC is calculated by charge and discharge current time integral, and it is necessary to know the initial SoC value. If not known, this is usually assumed. This method is unable to eliminate cumulative error and is sensitive to the initial SoC value. If the initial SoC value is inaccurate, it will affect all estimates and error will accumulate during the whole estimation process. Despite being widely used in recent years, CC is not a method that is usually used as a sole tool for estimating SoC but is commonly used in combination with other techniques. A few publications, like [41], use the CC technique as the only tool to calculate the SoC. This work uses CC as a unique method for the SoC estimation since it incorporates a procedure that allows an on-line adaptive parameter estimation of a source-dependent ECM like will be described in Section 4.2.1.

4.1.2. Open Circuit Voltage-Based Estimation (OCV)

SoC estimation methods commonly impose a characterization of the OCV curve (mainly through a polynomial or a look-up table), as they use either a direct OCV curve inversion method (if the application permits cell steady state voltage measurement), or a cell model-based methods [42]. Making voltage measurements to determine the SoC for the cell allows us to define the relation:

$$SoC = f^{-1}(OCV). \quad (6)$$

In the OCV method, the cell's voltage is continuously measured, and the corresponding SoC is obtained from a table. The method has inherent difficulties in practical applications: the sensors need high resolution to measure voltage accurately, and sufficient time is required for equilibrium. The OCV method can be very accurate, but as it needs a rest time to estimate the SoC, it cannot be used in real time. Also, the OCV–SoC relationship differs among cells and, therefore results in unacceptable error. However, the OCV method is used to calibrate the CC method expressed in Equation (5) [40], in combination with noise-filtering and other adaptive techniques, as is described in Section 4.2.2.

To understand why the OCV–SoC curve cannot be used directly to estimate SoC, we must analyze Figure 4, which was obtained from the experimental data. This figure displays 10 curves obtained under different C-rates charging processes for a $LiNiCoMnO_2$ battery. In the figure, it can be seen that, as the amount of charging current increases in each cycle, the curve shifts upward. This behavior gives to the charging process the following features: (1) When the battery receives a large amount of current, the charging process reaches the upper limit voltage faster than when it receives less current; (2) At the same open OCV, the battery has different SoC values depending on the amount of current it is receiving, with SoC values being larger when the charging process is developed under small values of current. If the behavior of the discharging process were presented, opposite features to the charging process could be seen. This OCV curve is fairly flat over the operational SoC range. Thus, even the

smallest error in the OCV obtained from a battery model can lead to divergence of SoC from the actual value. To compensate for the mentioned shortcomings, the OCV method has to be mixed with other approaches. In [40,43] the SoC has been estimated by inferring the remaining cell voltage from an OCV using the OCV–SoC curve and Equation (6).

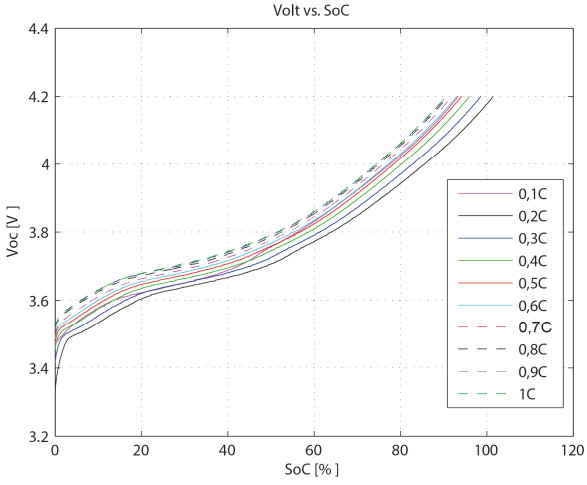

Figure 4. OCV vs. SoC during the charge process at different current values.

The changes of the OCV curve of each cell due to battery aging and performance degradation distort the estimation technique if nothing is done to adjust the curve. Therefore, OCV–SoC curve correction is required and in [42,44] it is implemented by comparing the capacity error with the CC and look-up table methods or by polynomial parametrization for the OCV curve. The OCV method compensates for both parameter and temperature variations in SoC estimation method presented in [20]. In [20] the OCV–SoC characteristic is represented by a controlled sources circuit, where a voltage-controlled source bridges SoC to OCV.

OCV is a common tool for supporting other methods. For example, in [45] a discontinuous discharging method to establish OCV–SoC characterization is used to calculate the internal resistance of the model battery and, in combination with an ECM and an extended Kalman observer, estimates the SoC. In [46,47], it is also used for determining the parameters of an ECM of a cell. The curve is used as part of the circuit model in [48–50] to consider the hysteresis phenomenon, which shows a difference in the equilibrium OCV between the charge and discharge processes of batteries.

4.1.3. Impedance Measurement-Based Estimation

An impedance measurement system is obtained from sinusoidal excitations at different excitation frequencies in which both voltage and current are recorded, and their complex quotient is computed as the cell impedance. The impedance spectroscopy of a battery cell can be approximated with two circles on the Nyquist plane [51]. In recent years, methods based on electrochemical impedance spectroscopy (EIS) have found application for accurate analysis of occurring electrochemical processes and diagnosis of LiBs, as the cell chemistry has a strong effect on the curve of the impedance spectrum [52,53]. An experimental lifetime model that can predict the internal resistance increase at various temperatures and SoC levels was developed and parameterized in [54].

In [52] the battery model is established using a simple ECM whose parameters are determined by the impedance measured data, presented as a Nyquist plot. The measured impedance (at frequencies between 100 mHz and 100 Khz) is decomposed with the help of a phase angle in a real part (x axis)

and an imaginary part (y axis), which are plotted against each other. Once the parameters of the model are known, the SoC can be estimated. A similar process is developed in [55] for finding the internal resistance growth model of the LiB cell. As this method needs a sinusoidal source, it is not suitable for online applications. The research developed in [56] uses an approach of the EIS for the online estimation of a LiB by decomposing the impulse signal used for getting the impulse response of the circuit model into the corresponding Fourier series factors. With this different frequencies sinusoidal signal, an online spectral analysis is made to obtain the impedance. The works presented in [57,58] introduce an EIS approach where the Nyquist plot impedance spectra is divided into high, mid, and low frequency sections. This division allows us to simplify the ECM parameter estimation and then, by using OCV correction and a fractional Kalman filter, estimate SoC.

4.2. Indirect Methods

These methods propose connecting the measured battery signals (voltage, current, and temperature) with the battery SoC employing a battery model. A high-fidelity battery model is required to capture the characteristics of the real-life battery and predict its behavior under a wide variety of conditions. In a BMS algorithm, using the signals as model inputs, the model can be used to calculate the SoC and other states of the battery.

4.2.1. Model-Based Estimation Methods

Model-based estimation techniques have become more common as they surmount the disadvantages of the direct estimation methods. Model-based methods deploy a battery model with advanced algorithms to estimate the states of a battery from its measured parameters such as voltage, current, and temperature. Although there are different approaches presented in the literature for estimating SoC directly using a battery model, this section just reviews electrical and electrochemical models because they are the base for most of the other methods of battery modeling. For example, the model technique displayed in [59] presents the so-called fractional order impedance model, which is inferred by mixing EIS technique and a first-order equivalent circuit model that will be described in the following. To estimate the SoC of a LiB, [59] deduces a fractional order Kalman filter and establishes a battery model that cannot be classified into the next two categories, but it is based on the two techniques presented here.

(1) Electrical Circuit Model-Based Estimation (ECM)

There are three different ECMs of a LiB widely adopted because of their excellent dynamic performance, described in [36]. The first is known as the Thevenin model and is a first-order RC model that consists of a nonlinear voltage source V_{OCV} as a function of SoC, a capacitor to model polarization capacitance and diffusion effects within the battery, C_{P1}, a diffusion resistance, R_{P1}, an internal resistance, R_t, a charge/discharge current, I_b, and a battery terminal voltage, V_t. The second model adds a capacitor in series with the voltage source V_{OCV} to characterize the capacity of store charge of the battery and to describe the changes in the OCV over time. This review calls this second model the first-order ECM. Similarly, the third one is obtained by adding in series an RC network (a parallel R_{P2}/C_{P2}) to simulate concentration and electrochemical polarizations. This review calls this model the second-order ECM. Figure 5 shows the second-order ECM.

An increase in the number of parallel RC networks can enhance the accuracy of dynamic battery response prediction. However, the coupling of SoC and time constants with cycle number and temperature leads to high prediction errors for estimating the SoC [60]. In [36], the discretization equations of each of the three mentioned models are presented and used in combination with an extended Kalman filter (EKF) and the CC estimation method to estimate the SoC. Wang et al. in [36] show that the second-order ECM is the most accurate and has the best dynamic performance, but is also the most complex of these three models. The work presented in [61] makes a comparison between continuous-time and discrete-time equations of the second-order ECM and concludes that discrete-time

identification methods are less robust due to undesired sensitivity issues in transformation of discrete domain parameters. The parameters of the second-order ECM can be calculated with different datasets depending on the scenario where the model is going to be used, like in [62].

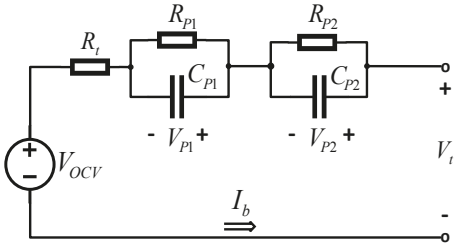

Figure 5. Second-order ECM.

By employing a simple ECM, like the Thevenin ECM, the SoC can be directly calculated by the transformation of the model equations [38,63–65]. The advantage of this approach is its simplicity, which enables easy implementation on a low-cost target microcontroller. In [5], The Thevenin model and second-order ECM were used for SoC estimation and compared with three other enhanced ECMs. The difference between these models is the way the SoC equations are calculated. In this approach, the equation model considers an SoC_{surf} based on electrochemical analysis rather than the average SoC (Equation (5)), to reflect the real-time particle surface concentration. This approach shows better performance in a low SoC range compared with the one that uses the average SoC for the ECM.

A fourth typical ECM originally proposed in [66] is presented in [6]. This model is quite accurate and could significantly increase the battery's nonlinear dynamic behavior identification. The model is shown in Figure 6. The OCV–SoC behavior of the battery is modeled by a self-discharge resistance R_d, a battery storage capacitor C_C, and a current-dependent current source. Likewise, the voltage–current characteristics are modeled as a second-order ECM but replacing the voltage source with a voltage-dependent voltage source to relate SoC to OCV. This ECM and the voltage–current dynamic mathematical equations are presented in [6], where V_{P1} and V_{P2} are the state variables, I_b is the input, and V_t is the output. In [10], by using this ECM, a procedure is developed that performs a real-time comparison between measured and calculated values of the battery voltage, while a PI-based observer is used to provide the SoC actual values. The second-order model has also been used in [60] for predicting SoC over a complete drive cycle in EV applications, but it uses a three time-constant model for modeling the transient behavior of the terminal voltage. For this reason, it uses a third RC network in series with the existing two. This ECM has been used as a part of the electrochemical model presented in [67].

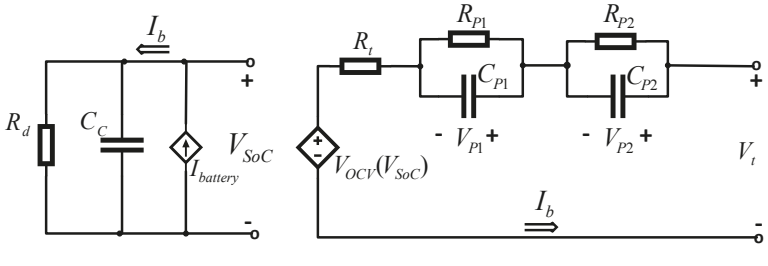

Figure 6. Source-dependent ECM.

In practical, all the parameterization values of the resistances and capacitors depend on the particular operating point of the battery, so they are vary with time, temperature, power demand, SoC, and SoH. In the four mentioned models, the battery SoC is directly incorporated into the model using its relationship with the battery OCV. If the scope of the model is to simulate dynamics slower than 1 s, it is possible to use an ECM like the described Thevenin model [51]. A possible variation is not to incorporate the battery SoC in the equations, but to estimate the battery OCV using the model and then use another technique to estimate the SoC from the OCV, like the approach presented in [68,69]. In [68] an improved Thevenin model that includes the hysteresis phenomenon in its equations is used for obtaining the voltage of the cell and then, by using Equation (5) and a multiple model Kalman filter (KF) in one case, and an autovariance least squares technique in the other, estimates the SoC. In [70], a Thevenin ECM is used to obtain the OCV and then, a linear fitting of a portion of the OCV–SoC curve is used to obtain the SoC. A similar process is followed in [71] to obtain the SoC, but this approach uses a simple ECM that considers just a voltage source and an internal resistance.

SoC estimation methods mix the second-order ECM of a LiB with other techniques such as an improved KF, like in [72,73], or with a kinetic model capable of predicting the circuit characteristics and the nonlinear effects under dynamic loads accurately, like in [74,75] (in these approaches, SoC estimation is replaced with the state of energy, SoE, calculation). However, it was not used in SoC estimation directly; the second-order ECM is coupled with a thermal model by heat generation equations in [76]. As this model gives accurate predictions of the temperature distribution through the cell surface and the voltage behavior under various operating conditions, it could be used in enhanced SoC estimation procedures.

By using second-order ECM plus an EKF and Equation (5), the approach presented in [7] can estimate the SoC and shows that it does not rely on the initial SoC and is immune to parameter errors. The approach displayed in [77] uses the second-order ECM presented in [7] to obtain the voltage circuit using the SoC and current as inputs. Then, another partial least squares battery-based model is used to estimate the same circuit voltage. Both calculations are compared with the terminal voltage of reference and the algorithm selects the model whose output has the minimum difference compared to the measured terminal voltage. This algorithm uses model free adaptive control to calculate ΔI, utilizing the terminal voltage errors; with this enhanced value, the algorithm calculates the SoC correction. Despite the mixed algorithm making the estimation process simple and effective, it increases the computational burden and the fusion mechanism, and the proposed methods with limited samples under various conditions still need further research [77]. In [78] a second-order ECM equation whose parameters are dependent on SoC, or deep of discharge (DoD), charging or discharge rate, and temperature, is used to estimate the SoC, and three different optimization techniques are used to estimate the parameters of the ECM and the feasibility of these techniques are evaluated by the accuracy of the predicted model and the rate of convergence in prediction.

Another ECM different than the conventional four mentioned is presented in [79]. In this approach, the architecture and components of the proposed circuit model capture the diffusion characteristics and the resulting overpotential by way of segment-wise diffusion modeling and based on the chemical mass transport mechanism. An approach that considers a second-order ECM as a base to add a thermal generation and thermal transfer equations is presented in [80] for real-time SoC estimation. In [80], electrical and thermal equations are coupled into a single model, and then an EKF is used for SoC estimation.

(2) Electrochemical Model-Based Estimation (EChM)

Electrochemical models (EChMs) use the equations that describe physicochemical phenomena like diffusion, intercalation, and electrochemical kinetics occurring in a battery. The definition of these equations involves a specialized knowledge of electrochemistry, hence their exploitation in the field of electrical and electronics engineering is not common. These models are typically computationally challenging owing to a system of coupled time-varying partial differential equations. They are known

to be computationally prohibitive, and thus their employment in BMS is hard. For example, a simple EChM like that presented in [81] involves six nonlinear partial differential equations that need a numerical solution. This complexity not only prevents the implementation of monitoring algorithms on low-cost target microcontrollers but also reduces the number of model parameters that can be adapted on-line to the present states of the battery [82]. For this reason, such models are best suited for optimization of the physical and material design aspects of internal electrodes and electrolytes [60]. The review presented in [83] is a brief updated literature revision of approaches using electrochemical models to estimate different states in batteries.

Several publications propose EChMs that could be used for SoC and other battery states estimation but do not present the SoC estimation process [67,83–87]. For example, [84] presents the full equation descriptions and model algorithm of an EChM based on the absolute nodal coordinate formulation approach, and also a brief model order reduction techniques review for EChMs. Most methods that use EChMs develop reduced-order models and use an estimator. The work developed in [88] fully describes a reduced order EChM. The model reduction and observer design process are intimately intertwined; simpler models ease estimation design at the expense of fidelity. Moura et al. in [83] present a state estimation scheme for a reduced EChM by deriving a single-particle model (SPM) with electrolyte. Tran et al. in [87] present equations of a three-parameter SPM and their Matlab simulation.

The approaches presented in [89–92] specifically develop EChMs for SoC estimation. Zou et al. in [89] propose a model composed of four submodels that capture the electrochemical, thermal, electrical, and aging dynamics in a set of partial differential equations. As one of the outputs of the full model is the SoC, it can be directly estimated by solving the system equations. Barlett et al. in [90] present a reduced-order electrochemical model for different Li ion chemistries that are used in dual-nonlinear observers (KF, fixed interval Kalman smoother and particle filter), to estimate the cell SoC and loss of cyclable lithium over time. The research presented in [91] described an EChM where a set of discretized equations are used to estimate the SoC directly, and then SoC is compared with an approach where the EChM is written as a linearly spatially interconnected system. Here, by exploiting the resulting semi-separable structure, the method uses an EKF to optimize the calculations for the SoC estimation. The technique presented in [88] introduces EChM parameters estimation by a noninvasive optimization strategy at any state of battery life. This technique is used in [92] for SoC estimation.

The advantage of EChMs is that they inherently include the dependence of the battery behavior on SoC and temperature, while electrical models must store their parameters as look-up tables for various SoC and temperature combinations. The disadvantage of EChMs is their high complexity. As has been stated, the parameter values of a battery model vary with temperature, so SoC estimation values directly depend on battery thermal behavior. Excessive temperature can greatly accelerate the battery aging process, and even cause a fire or explosion in the battery pack in severe cases. On the other hand, the battery electrical properties, such as usable capacity, internal resistance, and power delivery ability, all depend on the battery's internal temperature [80]. The battery's internal temperature can reach critical a lot quicker than the surface temperature. Thus, the surface temperature measurement alone might be not sufficient to ensure safe battery operation. This is why, for enhanced security and more accurate SoC estimation, the parameter values of the ECMs should be continually updated. This can be achieved with the adaptive methods described below. In EChMs, since they include temperature as one of their variables, this may not be necessary.

Most of the battery degradation literature consists of empirical-based studies with results extracted from experimental tests in laboratories [93]. Ahmadian et al. in [93] present the most prominent degradation models and the effects of degradation factors on LiBs' performance. Bashash et al. in [94] state that there is an exponential relation between calendar aging and SoC. This relationship shows that battery internal resistance increases as SoC increases. Thus, battery degradation increases if it is kept at high SoCs. Also, the average SoC maintained during battery cycling has an influence on the degradation rate, and a higher average SoC leads to faster degradation [93]. So, storing a battery

at full charge may be considered misuse. As the aging of batteries is reflected directly in the model parameters, the parameter values of the models should be continually updated, and the adaptive SoC methods described below can be used try to reach this condition.

4.2.2. Adaptive Filter-Based Estimation Methods

Adaptive techniques combine the direct and model-based methods, and are adaptive and self-designing systems that can automatically adjust to changing systems. Adaptive systems usually use feedback to change the current output according to the varying input [13].

(1) Kalman Filter-Based Estimation

KF theory can be applied by viewing each cell in the battery pack as a dynamic system whose inputs include the current and temperature of the cell and whose output is the terminal voltage. The way KF is used for SoC estimation is based on the explanation of the technique in [95]. As the parameters of Equations (1) and (2) depend on the cell model used, the idea is to include the desired unknown quantities into state vector x_k and the KF will automatically compute the best estimate of its present values. In this case, SoC has to be included as a state in the vector x_k. For deriving the filter equations, w_k and v_k are assumed to be mutually uncorrelated white Gaussian random processes, with zero mean and covariance matrices Σ_w Σ_v with known values $E[w_n w_k^T] = \begin{cases} \Sigma_w & n = k \\ 0 & n \neq k \end{cases}$; and $E[v_n v_k^T] = \begin{cases} \Sigma_v & n = k \\ 0 & n \neq k \end{cases}$.

$E[\cdot]$ is the statistical expectation operator, and T is the matrix transpose. The KF problem is then: Use the observed data $\{u_0, u_1, \ldots, u_k\}$ and $\{y_0, y_1, \ldots, y_k\}$ to find the minimum mean squared error while at the same time estimating $\hat{x}_k$ of the state x_k. So, with w_k and v_k, and an observable system modeled, solve: $\hat{x}_k = \arg\min E[(x_k - \hat{x})^T (x_k - \hat{x}) | u_0, u_1, \ldots, u_k, y_0, y_1, \ldots, y_k]$; with $\hat{x} \in R^n$.

KF gives a set of computationally efficient recursive relationships that involve both an estimate of the state itself, and also the covariance matrix $\Sigma_{\tilde{x},k} = E[\tilde{x}_k \tilde{x}_k^T]$ of the state estimate error $\tilde{x}_k = x_k - \hat{x}_k$. A covariance matrix of the error, $\Sigma_{\tilde{x},k}$, with large singular values indicates a high level of uncertainty in the state estimate, and one with small singular values indicates confidence in the estimate. The KF algorithm is depicted in Figure 7. The algorithm is initialized with the best available information on the state and error covariance: $\hat{x}_0^+ = E[x_0]$; $\Sigma_{\tilde{x},0}^+ = E[(x_0 - \hat{x}_0^+)(x_0 - \hat{x}_0^+)^T]$. Usually these quantities are not known, so initialization can be performed in an ad hoc manner, and the KF will quickly converge to the actual values as it runs. Later, the KF repeatedly performs two steps at each measurement interval: (1) It *predicts* the value of the present state, system output, and error covariance: $\hat{x}_k$, $\hat{y}_k$, $\Sigma_{\tilde{x},k}^-$, respectively. These values are predicted by propagating the system input through the system model dynamics (Equation (2)), assuming the expected process noise w_k of zero: $\hat{x}_k^- = A_{k-1}\hat{x}_{k-1}^+ + B_{k-1}u_{k-1}$; $\Sigma_{\tilde{x},k}^- = A_{k-1}\Sigma_{\tilde{x},k-1}^+ A_{k-1}^T + \Sigma_w$; and $\hat{y}_k = C_k\hat{x}_k^- + D_k u_k$; (2) Using a measurement of the physical system output, it *corrects* the state estimate and error covariance to $\hat{x}_k^+$ and $\Sigma_{\tilde{x},k}^+$: $\hat{x}_k^+ = \hat{x}_k^- + L_k[y_k - \hat{y}_k]$. It can be seen in these equations that the error between the output measurement y_k and the output estimation $\hat{y}_k$ is weighted by Kalman gain vector L_k, which is defined as $L_k = \Sigma_{\tilde{x},k}^- C_k^T [C_k \Sigma_{\tilde{x},k}^- C_k^T + \Sigma_v]^{-1}$. The covariance correction step is $\Sigma_{\tilde{x},k}^+ = (I - L_k C_k)\Sigma_{\tilde{x},k}^-$. The covariance matrix indicates the uncertainty of the state estimate, and it always decreases due to the new information provided by the measurement. The uncertainty value of SoC is reduced by the KF algorithm because the recursive equations are repeatedly evaluated during system operation [96].

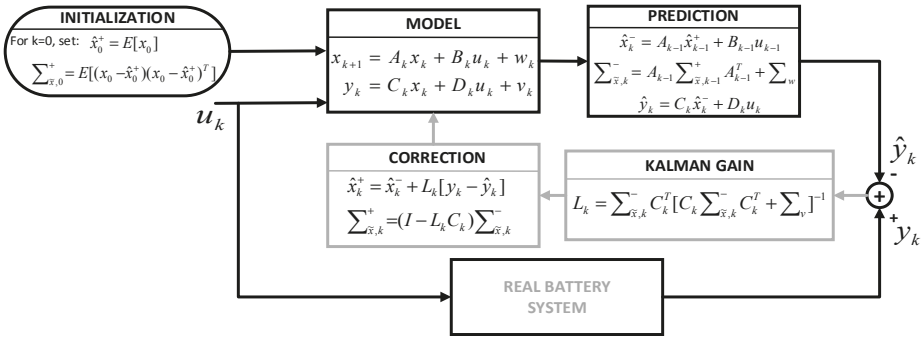

Figure 7. Kalman filter iteration diagram.

Recently, the EKF has attracted increasing attention and become one of the most commonly used methods to estimate the battery SoC even when the initial SoC is unknown [97]. KF is the optimum state estimator for linear systems. If the system is nonlinear, a linearization process can be used at every time step to approximate the nonlinear system with a linear time varying (LTV) system. This LTV system is then utilized in the KF, resulting in an EKF on the real nonlinear system. Using a nonlinear model such as that presented in Equations (3) and (4), and taking into account the same considerations for w_k and v_k, at each time step, $f(x_k, u_k)$ and $g(x_k, u_k)$ are linearized by a first-order Taylor-series expansion. Assuming that $f(x_k, u_k)$ and $g(x_k, u_k)$ are differentiable at all operating points (x_k, u_k): $f(x_k, u_k) \approx f(\hat{x}_k, u_k) + \left.\frac{\partial f(x_k, u_k)}{\partial x_k}\right|_{x_k=\hat{x}_k} (x_k - \hat{x}_k)$; $g(x_k, u_k) \approx g(\hat{x}_k, u_k) + \left.\frac{\partial g(x_k, u_k)}{\partial x_k}\right|_{x_k=\hat{x}_k} (x_k - \hat{x}_k)$. Combining these two equations with Equations (3) and (4), the linearized equations that describe the real system state as a function of itself (known inputs u_k and $\hat{x}_k$, and the unmeasurable noise inputs w_k and v_k), we have: $x_{k+1} \approx \hat{A}_k x_k + f(\hat{x}_k, u_k) - \hat{A}_k \hat{x}_k + w_k$; $y_k \approx \hat{C}_k x_k + g(\hat{x}_k, u_k) - \hat{C}_k \hat{x}_k + v_k$., where $\hat{A}_k = \left.\frac{\partial f(x_k, u_k)}{\partial x_k}\right|_{x_k=\hat{x}_k^+}$, $\hat{C}_k = \left.\frac{\partial g(x_k, u_k)}{\partial x_k}\right|_{x_k=\hat{x}_k^-}$. With this linearization, the EKF iterative algorithm is similar to that presented for the KF and is described in Figure 8.

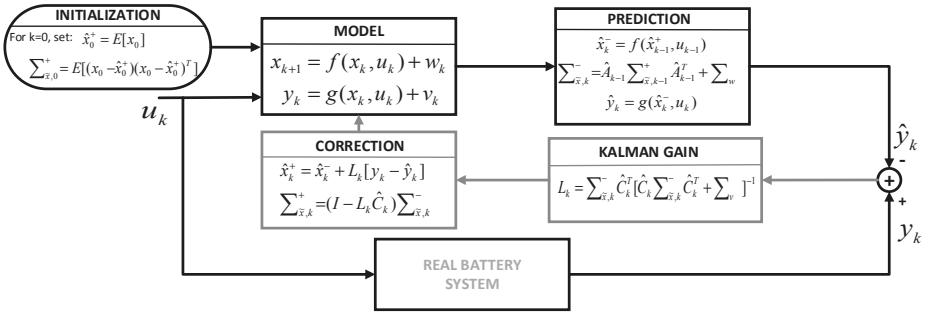

Figure 8. Extended Kalman filter iteration diagram.

The linearization process made in EKF uses the first- or second-order terms of the Taylor series expansion to approximate a nonlinear model, which degrades the SOC estimation accuracy. To overcome this, instead of local linearization, the unscented Kalman filter (UKF) captures the statistical distribution characteristics of a nonlinear system according to a series of sigma points [98]. The UKF based on unscented transform not only does not require the calculation of a Jacobian matrix

but has a higher order of accuracy in the noise statistics estimation than the EKF, such as the mean and error covariance of the state vector of the battery system [97]. Figure 9 shows the UKF algorithm. The sigma points and weighted coefficients calculations, as well as the covariance matrix of the error factors included in the Kalman gain, can be seen in [98,99].

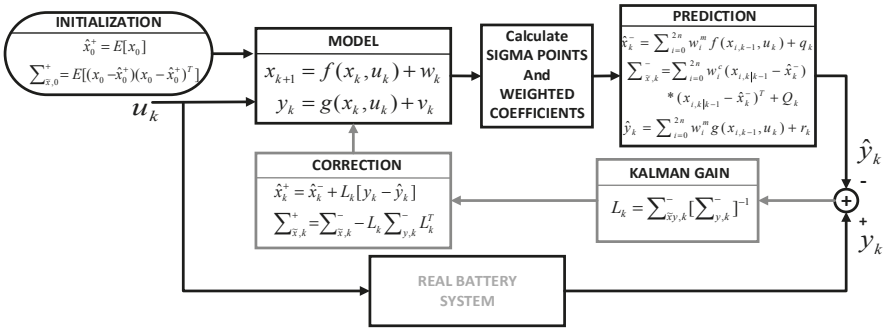

Figure 9. Unscented Kalman filter iteration diagram.

In [100] a KF is introduced to extract an OCV value in a noisy environment, and then to estimate SoC based on the OCV–SoC mapping. As the KF has the observability of the system as a requirement, a virtual-measurement-based method can be implemented to account for a local loss of observability, like is presented in [91]. This approach uses the iterative process of the KF described in Figure 8 for estimating not only SoC but also other battery parameters, like the KF implemented in [96] estimates both SoC and SoH. It is common to find a combination of CC or OCV methods with the KF method to estimate SoC value, as is presented in [58,101].

Some good examples of how to apply and run an EKF algorithm (as depicted in Figure 9) for SoC estimation are presented in [7,21,91,102]. Due to the electrochemical and thermal models of the batteries being highly nonlinear, EKF is used for estimating its parameters, followed by SoC [45,80,90]. The EKF method is also used in combination with CC and/or OCV, as proposed in [11,45,50,103]. The works presented in [47,68,104] use a multiple model approach that uses a bank of EKFs to estimate the SoC of the battery. Each filter represents a particular operational condition of the battery, and is used to enhance the accuracy of the SoC EKF estimation by accounting for the unknown measurement noise covariance. Additionally, any errors in the model can also be compensated for by an increase in the measurement noise covariance. The state estimate is provided through a sum of each filter's estimate weighted by the likelihood of the unknown elements conditioned on the measurement sequence.

KF and EKF work well when the system model and noise statistics are known a priori. Wrong assumptions or changes during operation may lead to a degradation of filter estimates. Fleischer et al. in [8] implement an REKF, which is more robust to uncertainties in the system equation, in the measurement equation, and in the noise covariances. It also provides the estimation error bounds dynamically. This approach uses the same algorithm depicted in Figure 8 but adds a tuning parameter that guarantees that the relation between process/measurement noise and estimation error is lower than this parameter value. Fleischer et al. in [8] use a state space linear circuit model where the output is the OCV, and the SoC is one of the state variables. An improvement to the measurement noise due to a harsh electromagnetic environment, like the present in EVs, is to add a wavelet transform matrix (WTM) that can analyze and denoise the nonstationary current and voltage signals. Zhang et al. in [9] developed a SoC estimation approach that uses this improvement in the measurement noise treatment and, by correcting the covariance matrix error in the depicted EKF, builds an adaptive EKF (AEKF) that can reduce the estimation error when the measurements are passed through WTM.

Another common improvement to the KF algorithm for finding SoC is UKF, which is used in [97,105]. In [105], the equations of an ECM with two RC branches are written in the form of Equations (4) and (5). Here, an adaptive adjustment of the noise covariances is implemented using a technique of covariance matching to estimate the noise statistics in this iterative process adaptively; see the estimation process presented in Figure. It allows for obtaining better accuracy both in battery model parameters estimation and in the battery SoC estimation. This method is known as adaptive UKF (AUKF) and is employed here for online model parameter identification of the ECM at each sampling time. Subsequently, based on the updated model parameters, SoC estimation is conducted using the AUKF method. Since the temperature variation affects the performance of the battery, it is important to compensate for temperature effects to improve the model's predictive capability and SoC estimation. UKF is implemented in [98] to estimate SoC using a modification of ECM (a resistance and a capacitor correction factor), to include the impact of different current rates and SoC on the battery internal resistance, and the impact of different temperatures and current rates on the battery capacity. To deal with the variation of battery parameters due to temperature changes [106,107], we propose a SoC estimation approach and online parameter updating using a dual square root UKF based on unit spherical unscented transform. A relatively simple modification to the depicted UKF is the double UKF algorithm used in [72]. It introduces the use of two UKF filters that work together to calculate the real value of SoC and ohmic resistance to obtain a final SoH value.

(2) Recursive Least Squares-Based Estimation (RLS)

The least squares method calculates system parameter values that minimize the least squares error between the measured output signal and the estimated output signal by assuming that the system is disturbed by white noise. The recursive least squares (RLS) method is used in adaptive filters to find the filter coefficients that allow for obtaining the minimum square of the error signal (defined as the difference between the desired signal and the signal produced at the output of the filter). The RLS algorithm makes this process recursively and updates its estimated parameter values by incorporating new information from every sampling time. RLS with a single fixed forgetting factor is a parameter identification method that is described in Figure 10. In this figure, e_k is the output estimation error, P_k is the covariance matrix of the parameter estimates, λ is the forgetting factor, and K_k is the RLS gain. The forgetting factor allows the algorithm to tune its parameters to a time-varying system. The tuning speed depends on the asymptotic memory length N, which means that information is forgotten with a time constant of N sample intervals [108]: $\lambda = 1 - \frac{1}{N}$. When all information is preserved, the memory length $N = \infty$, which means $\lambda = 1$. When information dies away with a time constant of one sampling interval, the forgetting factor becomes 0.

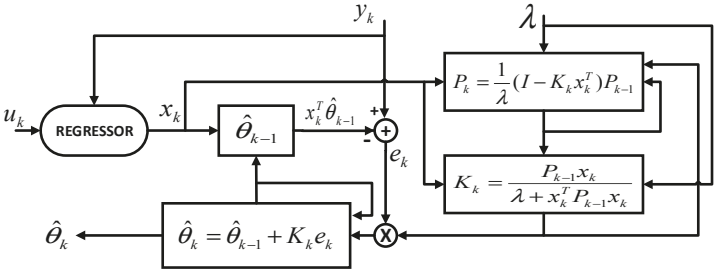

Figure 10. Recursive least squares algorithm.

The approach presented in [109], seeking to solve the problems related to model accuracy, sensor precision, data saturation, and heavy computation in the EKF-based methods [110], uses the RLS method to improve an adaptive EKF to estimate online the SoC and the battery model parameters.

Also, a RLS for estimating the circuit parameters was used in [111,112]. A RLS filter is employed in [112] to dynamically estimate in real time the parameters of a Thevenin ECM. Next, the model parameters are used to estimate the battery's OCV and hence its SoC via the fading KF. Shen et al. in [111] use a single forgetting factor RLS like that presented in Figure to obtain the second-order ECM parameters and an EKF for the final SoC estimation procedure. Rozaqi and Rijanto in [108] present multiple fixed forgetting factors RLS, where OCV and internal resistance of a Thevenin ECM are used as the main parameters to be estimated by the algorithm, and then to estimate SoC. Lotfi et al. in [82] use an observer-based reduced-order EChM to estimate SoC by using an RLS with exponential forgetting parameter identification routine to compensate for the reduced-order model uncertainties. In [82], an RLS algorithm was coupled with a Luenberger-like observer for the estimation of the states of the model.

(3) H Infinity-Based Estimation (H∞)

H infinity (H∞) theory is a powerful tool to restrict the effect of exogenous disturbances on output. The H∞-based method is to guarantee that the norm from the system and measurement noises to the SoC estimation error are less than a given attenuation level, which can still ensure SoC estimation accuracy in the worst cases [113]. The H∞ filter is robust in the presence of parameter uncertainties and modeling errors [114], and its general procedure is displayed in Figure 11.

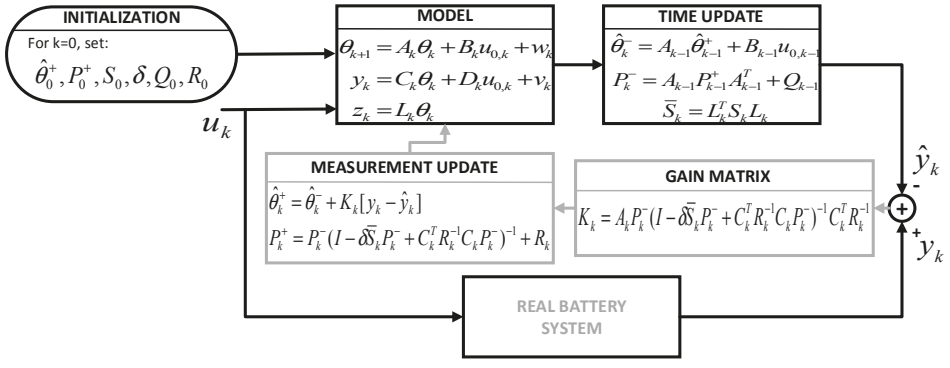

Figure 11. H-infinity filter algorithm.

In Figure, θ_k is the state vector of the model, y_k is the output, and z_k represents the SoC. P is the covariance matrix, δ is the constraint boundary, and S is a user-defined positive definite matrix that will affect the gain matrix. Also L is a user-defined matrix. Q and R are the covariances of the process noise w_k and measurement noise v_k, respectively. Xiong et al. in [114] present a time-saving method to obtain the OCV–SoC relationship through any existing current and voltage measurements by using the H∞ filter in the absence of the time-intensive OCV test. Here, the parameters and OCV of a Thevenin ECM are obtained by using the procedure depicted in Figure, and OCV–SoC relationships are extracted from standardized characterization tests. Then, the method obtains the SoC using another H∞ filter and considering a linearized state space model like that depicted in Figure 2, and establishing the relationship $z_{s,k} = L_{s,k}x_k$.

In the SoC estimation process, the variation of the model parameter under different aging levels and operation conditions is a critical issue that is addressed by using a dual H∞ filter in [115]. This strategy uses a first H∞ filter to overcome the drawback of its sensitivity to their initial noise information, and the second part of the filter is an adaptive H∞ filter that employs a covariance matching approach to estimate SoC. H∞ provides the most consistent estimates concerning different uncertainties, compared with EKF and UKF [116]. However, the variability of the estimation errors is

larger for batteries with a strong correlation between SoC and OCV. Fridholm et al. in [116] describe the H∞ technique by using a Thevenin ECM in two different battery chemistries. Yu et al. in [117] use the H∞ procedure to trace the parameters online according to the working conditions, and utilizes an UKF for the final SoC estimation. The strategy presented in [118] displays the H∞ technique at both cell and pack levels. Lin et al. in [119] propose a multi-model probability fusion SoC estimation using H-infinity algorithm. Here, the H∞ technique is employed to develop online SoC estimators for the Thevenin, second-, and third-order ECMs. Another battery model like the electromotive force model presented in [113] is used, combined with the H∞ algorithm, to estimate SoC.

4.2.3. Adaptive Artificial-Intelligence-Based Techniques Estimation

A short (13 references) review of adaptive techniques including the KF, Artificial Neural Networks (ANNs), and Fuzzy Logic (FL) systems was presented [13].

(1) Fuzzy-Logic-Based Estimation (FL)

FL is a problem-solving methodology that simplifies all the noisy, vague, ambiguous, and imprecise input data by using objective rules to find the real value of the input. The operating principle of a FL technique can be structured into four simple stages [13]: (1) Fuzzification: in this stage the measured system values are converted into linguistic fuzzy sets, and classified into membership functions. Fuzzy sets specify the degree of belonging to each logical set; (2) Fuzzy rule base: a fuzzy rule base is designed using professional experience and system operating method; (3) Inference Engine: through this stage all the fuzzy rules are transformed into fuzzy linguistic outputs; (4) Defuzzification: translates the linguistic fuzzy rules into analog output values.

FL systems can generalize any system using cycle number estimation because in some of the battery tests it will be easier to describe the state of the battery (High, Low) rather than getting a precise number. The approach presented in [120] uses a fuzzy rule-based system to compute the nonlinear gain of a KF that estimates SoC, and a Genetic Algorithm (GA) is used to evolve the definition of the rule base. In [121] a Thevenin ECM in a weighted combination with the CC method is adopted by the fuzzy logic control scheme to obtain a static SoC estimation. Then the dynamic battery SoC is precisely estimated on the basis of static SoC using an ANN.

Fuzzy technique can be used to model a battery with high accuracy and consider the degradation process in the model [122]. This model could be used for other approaches to the SoC estimation process or to improve the performance of other SoC estimation techniques like in [123], which presents an improved fuzzy adaptive KF method, or like in [102], where a fuzzy controller is applied to online adjust the measurement noise variance. Cheng et al. in [102] designed a fuzzy self-adjusting controller where, according to fuzzy inference rules, the error covariance matrix elements of KF are adjusted online and in real time for every step of the KF iterations. In [124], the polarization resistance of the battery model is modeled using fuzzy rules that are a function of both SoC and the current. Despite the fact that this approach does not directly use the FL technique for the SoC estimation process, the model presented can be adapted to this task. Similarly, [125] uses FL by fuzzy self-tuning algorithms to update the model parameters of a second-order ECM that is used with an adaptive UKF to obtain SoC values. Hametner and Jakubek in [126] present a SoC estimation technique based on a purely data-driven model and a nonlinear fuzzy observer that uses KF theory for each local linear state space model. Then, the technique uses linear combinations of the local filters to derive a global filter and estimate SoC.

A dew publications directly calculate SoC from FL [127,128]. Zheng et al. in [128] estimate SoC and cell capacities by comparing cell voltages at the beginning and end of charging. This approach calls the technique the "FL Dissipative Cell Equalization" algorithm. Sheng and Xiao in [127] use a least squares support vector machine by applying fuzzy inference and nonlinear correlation measurement. This allows an improvement in the SoC estimation process due to the effects of the samples with low confidence being reduced.

(2) Artificial Neural Networks-Based Estimation (ANN)

ANN relies on an input layer and output layer consisting of neurons that contain system-specific normalized input and output information. The mathematical junction between the input and the output layer is realized by a hidden layer and its neurons, where the neurons are interconnected as in Figure 12. Every neuron except the inputs consist of a sum of the products of the output O_{pred} of the neurons in the predecessor layer and a particular weight $W_{pred,actual}$ between the neurons of the predecessor and the actual layer [129]: $\varphi_{actual} = \sum_{i=1}^{l} (O_{pred} * W_{pred,actual})$. Those cumulated outputs and weights φ_{actual} are arguments for a sigmoidal activation function $sig(\varphi_{actual})$ to determine an output O_{actual} for every neuron in the actual layer: $O_{actual} = sig_{(\varphi_{actual})} = \frac{1}{1+e^{-\varphi_{actual}}}$. Those outputs are further distributed to the successor neurons in the next layer, whether a hidden or an output layer.

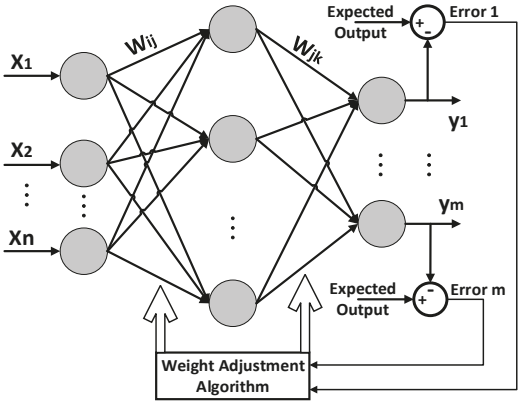

Figure 12. Topology structure of ANN model.

There are two basic architectures of ANNs: feed-forward networks and feedback (recurrent) networks. Meanwhile, there are three main training scenarios for ANNs: supervised, unsupervised, and hybrid. A feed-forward neural network (FFNN) has no feedback and the input signals propagate through the network forward from the input layer to output layer. In the back propagation neural network model (BPNN) feedback and learning take place during the propagation of input patterns from the input neurons to the output neurons. The outputs are compared with the desired target values, and error is produced. Then the weights are adapted to minimize the error. The initial values of weights are assumed to be zero, and the weight between the actual neuron and the output of the predecessor neuron is defined as $W_{pred,actual}$. The weight adaptation equation is given by [130]: $W_{pre,act}(t_n) = W_{pre,ac}(t_{n-1}) - \frac{\alpha E(t_n)}{W_{pre,ac}(t_{n-1})} \Delta W_{pre,ac}(t_{n-1})$, where $0 < \alpha < 1$; $E = \frac{1}{2} * \sum (y_i - O_{actual})^2$; $i = 1 \ldots n$; and y_i is the expected output.

In [129] a BPNN was used for the SoC determination based on frequency domain data. Here, the real and imaginary parts of the measured impedance, plus the frequency of each measurement are used as X1, X2, and X3 inputs of a three-input BPNN like that presented in Figure. The corresponding output layer provides with its neurons the dedicated SoC classes $\{c_i\}$ corresponding to the SoC specific impedance spectra. The neuron with the determined SoC will remain after execution with the binary value one, and all the others will remain with the value zero. Two different architectures of BPNN are used for calculating SoC in [131]. Unlike these traditional BPNNs, [132] does not take into account the equivalent inner resistance of the battery and makes a single improvement to the weight adjustment algorithm of its BPNN that can significantly reduce the SoC estimation error. In [133] a simple radial basis ANN is used just to identify the ECM parameters and then, using SoC as one of the state-space variables and employing EKF, SoC is estimated. In [133] the inputs of the ANN

are SoC and the current and voltage measured, and the output is the OCV. A similar strategy is used in [43,134–136], where, after modeling the battery system by an ANN model and a state space model as presented in Section 3, SoC is calculated using a dual EKF or other adaptive filter-based estimator. Wang et al. in [137] use a four-input, one-output BPNN. Its only output is SoC estimation in an EV. The four inputs are the current at times [k] and [$k-1$], and the voltage at times [k] and [$k-1$]. This method uses an extensive dataset of charging and discharging experimental LiB voltage and current, obtained at different standardized driving conditions, and trains the network offline. The approach reports that the inclusion of previous time points allows the ANN to better understand the relation of current and voltage drops to SoC. Other approaches can estimate online the battery SoC directly from an ANN [6,138–142]. In [138] the inputs for a topology like in Figure are separated depending on the behaviors of a battery while charging, idling, and discharging. Yan and Wang in [142] utilize a simple two-input, one-output, and one hidden layer BPNN structure. Yan and Wang in [142] used as inputs the current and terminal voltage of the battery, and SoC as the output variable.

The main disadvantage of ANN is that it needs more neurons to increase the accuracy, which limits its implementation in real-life models. In addition, each ANN needs to be trained before it can be used and numerous iterations may be required to train it. For this reason, the trained ANN can be used for only one specific application. For example, in a HEV, the input conditions are always changing and simulating these inputs will be hard. On the other hand, ANN is not effective in extrapolation, which limits its ability to calculate the remaining charge time of a battery [13].

(3) Fuzzy-Based Neural Network Estimation

In general, two types of fuzzy-based neural networks are used in the literature for the estimation of SoC: the adaptive neuro-fuzzy inference system (ANFIS) and the local linear model tree [8]. In all cases, direct open-loop SoC estimation is implemented. ANFIS combines the advantages of fuzzy systems and adaptive networks in one hybrid intelligent paradigm. The flexibility and subjectivity of fuzzy inference systems, when added to the optimization strength and learning capability of adaptive networks, give ANFIS its remarkable power of modeling, approximation, nonlinear mapping, and pattern recognition. ANFIS can be used to model cell characteristics [143], to online correct other SoC estimation techniques for reaching high accuracy [144], or to directly obtain the SoC estimated value [145].

An offline model for power systems applications using ANFIS is developed in [143] for SoC estimation in LiBs. In this publication, based on the manufacturer data on LiBs, the ANFIS battery model is trained offline and developed to yield the cell SoC at any given temperature and OCV within the training range. The cell SoC is estimated while the battery is at rest, and the CC approach is adopted at the cell level. The fact that the ANFIS model is based on the data supplied by manufacturer makes this approach inefficient due to most of the manufacturers not supplying battery data. On the other hand, to take into account the cell degradation, it is required to add a mechanism that guarantees accurate SoC estimation over time. Dai et al. in [144] utilize a KF to estimate the SoC by using a second-order ECM. Then, the ANFIS method is used to correct the SoC obtained by KF. Here, the ANFIS technique is comprised of two steps: the first step is the acquirement of the fuzzy inference system knowledge base based on ANFIS using the experimental data offline, and the next step is the online correction of the pack's SoC estimation results. Dai et al. in [144] present the elaboration of the building, training, and optimizing of the ANFIS model. In [145] a Thevenin ECM is used to obtain the OCV. This output voltage is used as an input of an ANFIS system whose output is the SoC. Despite the tests being performed with a NiMH battery, they are applicable to other chemistries.

Another ANFIS application is presented in [8]. It uses a combination of several algorithms to determine the battery state variables. In this approach, among other SoC boundary estimation methods, a robust EKF is implemented for recalibration of the CC method. Then, the method uses ANFIS to estimate the state of available power. Since ANFIS is known to suffer from the curse of dimensionality, the large number of inputs is likely to hinder the estimation performance. Extensive

experimentation is sometimes required to obtain the ANFIS training dataset [143]. The approach of ANFIS estimation is basically the same as that of the direct SoC estimation using ANNs and, therefore, has the same disadvantages.

(4) Genetic Algorithm-Based Estimation (GA)

Genetic Algorithm (GA) is an optimization technique where the variables of interest of the system to be optimized are characterized in the form of strings called chromosomes. In SoC estimation applications, the chromosome is a vector that has as elements the parameters of the battery model used. SoC can be an element of this vector. The algorithm is initiated by creating a random set of chromosomes in the search space followed by an iterative process of selection, crossover, and mutation to find the optimal solution, as depicted in Figure 13. The stop criterion is defined by an objective function that minimizes the error between the voltages defined in the chromosome and the actual measured voltage. This criterion selects the best population in each iteration.

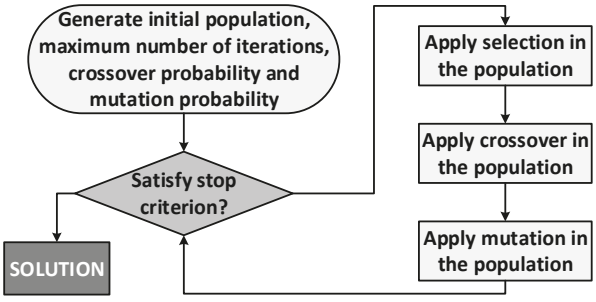

Figure 13. GA algorithm.

GA is used as an optimization technique to estimate different states of the battery. The approaches presented in [59,146] use a GA to identify time constant and other parameters of the battery model (fractional order and EIS-based model [59], and Thevenin ECM [146]). Despite these proposals utilizing a UKF-based SoC and EKF-based SoC estimation, respectively, the model parameter estimation using the GA is crucial, and accounts for the high accuracy of the methods. In [5], a classic GA was used to identify the parameters of five different ECMs and, thus, estimate the SoC. In [78] a GA is used as one of the optimization techniques to estimate the second-order ECM equation parameters that are dependent on SoC, and so to estimate the SoC. The objective of this optimization process was to find the values of polynomial coefficients of parameters equations, which produce a OCV–SoC characteristic that best fits the characteristic curve obtained from the manufacturer's battery data. As the model fitness function is defined as the absolute of the difference between model output and catalog values at each sample point, the absence of battery data supplied by the manufacturer may cause this method to be unsuitable for many applications. Rozaqi and Rijanto in [108] apply a RLS algorithm for battery SoC estimation by using a Thevenin ECM of a LiB. Here OCV and the internal resistance are the parameters to be estimated, and the optimum values of RLS are determined using a GA.

Several variations in GA applications for SoC estimation processes can be found in the literature. One of them is just to use the algorithm to identify the initial SoC, like the procedure presented in [147]. This approach uses a Thevenin ECM, and SoC estimation is finally made by a modified OCV method. Yan and Wang in [142] use a GA for optimizing the weights and thresholds of a one hidden layer BPNN that has SoC as the only output. In [112], OCV is calculated based on a Thevenin ECM, and then, by using it, SoC is estimated through a fading KF where the fading factors that optimize the KF are calculated by the means of a GA.

(5) Particle Swarm Optimization Algorithm-Based Estimation (PSO)

Particle swarm optimization (PSO) is a swarm intelligence-based meta-heuristic optimization technique inspired by intelligent movement depicted by the population of different species. The algorithm consists of a population of particles randomly initialized in the search space. Initially, it produces a random population and then generates the next population based on an objective function. In this process, the PSO algorithm is similar to GA, but PSO does not need reproduction or mutation to produce the next generation. Thus, PSO is faster at finding solutions than GA [148]. The initiated population works collectively through velocity: $v_i^{t+1} = wv_i^t + c_1.rand.(p_{b_i} - x_i^t) + c_2.rand.(g_b - x_i^t)$; and position: $x_i^{t+1} = x_i^t + v_i^{t+1}$; to find the optimal solution [78]. In these equations, w is the inertia weight factor, c_j is an acceleration coefficient, *rand* is a random number between 0 and 1, v_i^t is the velocity of particle i at iteration t, and x_i^t is the current position of particle i at iteration t. Each particle moves iteratively in the solution space with movement depending on global best position (g_b) of the swarm and its personal best solution (p_{b_i}).

In SoC estimation applications the process of iterative update of the position of the particles is continued until the stop criterion is met, and this criterion is given by an objective function that evaluates the relation OCV–SoC in a direct or indirect way like in [78,149], where a PSO method is used to determine the unknown parameters of a second-order ECM to obtain the OCV. Then these approaches estimate SoC using a lookup table. In [150], instead of a lookup table, the CC method is used for estimating SoC. Ismail and Toha in [148] develop the same process but uses a Thevenin ECM. Huachun et al. in [151] calculated the parameters of a Thevenin ECM using a PSO algorithm and, by using a technique called second-order sliding mode observer, estimated SoC. The approach presented in [152] uses the PSO algorithm to estimate the second-order ECM parameters, but SoC is calculated using two different methods: EKF and the smooth variable structure filter (SVSF). The approach presented in [153] uses a version of the second-order ECM where the voltage source is replaced by a SoC-dependent capacitance and an RC parallel network is added as a third time constant. The values of all intrinsic parameters of this ECM are estimated using a PSO algorithm, and instead of assuming any predefined nonlinear relationships between intrinsic parameters and SoC, the PSO algorithm takes the response of all intrinsic parameters, as well as SoC, into account in the parameter estimation without treating SoC as an independent variable. Antón et al. in [154] present a statistical learning technique for SoC estimation called multivariate adaptive regression splines (MARS), whose optimal parameters are calculated using PSO.

4.2.4. Other Estimation Techniques

The methods presented abovecan suffer from one or several drawbacks like sensor drifts and precision, modeling mismatches and lack of model accuracy, data saturation, heavy computation, or specific input information requirements. These aspects are key factors that influence the accuracy of the SoC estimation method, so the authors are still working on innovative proposals to overcome those error sources in the SoC estimation process. Although some approaches do not fit into any of the previously presented categories, it is important to list some of those new proposals in this review.

Statistical learning theory addresses the problem of finding a predictive function based on data. The goal is to learn a general rule that maps input variables to outputs. In [154], the MARS statistical learning method was applied to estimate the SoC of a high-capacity battery cell for a simple data profile (constant-current constant-voltage charge, and constant-current discharge) and a limited range of SoC. The fact that MARS parameters are difficult to estimate generates some limitations in the technique. Another statistical approach is presented in [155], which uses a particle filter (PF) or sequential Monte Carlo (SMC) method for SoC estimation of a LiB battery pack for an EV. SMC is a set of genetic-type particle Monte Carlo methodology to solve filtering problems arising from signal processing and Bayesian statistical inference. The filtering problem consists of estimating the internal states in dynamical systems when partial observations are made; random perturbations are present in the sensors as well as in the dynamical system. This proposal utilizes both Gaussian and non-Gaussian

distributed noise models. PF utilizes particles (weighted random samples) to approximate the posterior distribution sampled by the Monte Carlo method.

Afshari et al. in [152] use a second-order ECM and a smooth variable structure filter (SVSF) to estimate the SoC. The SVSF benefits from the robustness of variable structure systems in which it is guaranteed that the measurement error (innovation sequence) remains norm-bounded. The stability and convergence of the SVSF method are proven in this publication. The filter is formulated in a predictor–corrector form, and its corrective gain is designed to force the states to remain within a subspace of true states. This paper shows that this filter is robust to a wider range of modeling inaccuracies and parametric uncertainties. SVSF is implemented to alleviate the effects of different factors on SoC estimation like inaccuracies in modeling a cell, deviations of a battery's parameters from their nominal values due to aging, unpredictable temperature variations, and measurement and environmental noises. The publication states that the SVSF method is more robust to modeling and for parametric uncertainties, and demonstrates the superiority of the SVSF over the EKF for SoC estimation under uncertain conditions.

Huanchun et al. in [151] propose an approach based on second-order sliding mode observer (SMO) for battery SoC estimation. The PSO technique is utilized to estimate the Thevenin ECM parameters. The estimation technique has a robust tracking capability in SoC estimation with high accuracy for both known and unknown initial SoC, and showed that SoC could be determined with high accuracy based on only the measurements of the battery voltage and current.

Tang et al. in [110] present a multi-gain Luenberger-based (MGL) observer that is robust to modeling inaccuracy and sensor drifts to estimate SoC. The gains of the observer are switched by a classifier, which categorizes the errors between the real voltage measurement and model output into different groups. Correspondingly, different observing strategies are designed for different groups for better SoC estimation robustness and accuracy.

5. Technical Challenges in the SoC Estimation Process

The factors affecting battery SoC are many and complicated. Scholars have proposed many methods to estimate SoC, but these still do not guarantee accuracy and practicability. There are two overall challenges in this field: (1) To enhance the SoC estimation accuracy, robustness, and effectiveness without increasing the complexity of the models and estimation procedures; (2) To simplify the complexity of the estimation process, and therefore facilitate its implementation in low-cost hardware. The solutions for the two challenges are closely related and cannot be disconnected from each other. The goal is to find a trade-off in the SoC estimation procedures between accuracy and computational complexity in compliance with the motto "simple is better." To achieve this, it is necessary to propose strategies to nullify or minimize sources of error in the SoC estimation methodologies.

In this review, the main SoC estimation error sources are: (1) Zero-mean sensing noise is inevitable in practical cases for both current and voltage sensors; (2) Battery modeling error or inaccuracies in the models; (3) The parameters that are assumed such as covariance and noise type, initial SoC, and search spaces in optimization processes; (4) Other unknown error sources that may have been caused by some unknown reasons or the combination of errors noted above. For example, the drifting of the current sensor can cause a large SoC estimation error in the current integral method after a long period of error accumulation; however, the influence is negligible when the time is short.

Now the two main mentioned challenges become more specific: To deal with the probabilistic tendency to model the sensing noise with models closer to the real pehonomena; to find less complex and more accurate battery models that include aging and thermal behavior; to define methodologies to establish initial values; and to identify and characterize other possible error sources. The last three can be solved by overcoming the drawbacks of the battery modeling by including the battery strong nonlinearity, time-varying features, and temperature effects on the behavior. The principal concern in the thermal control of LiBs is the considerable temperature rise that happens during charging and discharging, which may cause thermal runaway. Therefore, understanding the discharge behavior

of a lithium ion battery is very important as well as using correction factors in the models according to temperature variations, or other approaches that guarantee the inclusion of thermal restrictions and also variations of thermal and electric behaviors between cells within a battery pack. A fully efficient battery model can quantitatively characterize battery nonlinearities such as open-circuit voltage, internal resistance, and transient voltage response. Such a model enables designers to gain a thorough understanding of battery behaviors under different operating situations and will allow accurate battery performance prediction and the optimization not only of the safe control of the battery but also the extension of its useful life thanks to the optimum management of all its capacity. This kind of model would simplify and optimize the design of the BMS. The information contained in the current i and voltage v variables are related to microscopic behavior within each battery cell, and they embrace all the internal dynamics of a battery. This review proposes that at a given instant k, i_k, and v_k are the result of the performance of all the internal chemistry of the battery under conditions such as aging, temperature, hysteresis, self-discharge, rates of charge and discharge, and even noise present in the battery as a system (except the noise of the DAQ systems). The challenge is to take these data, extract the information, and build a system free from the constraints and limitations presented by existing methods.

6. Conclusions

This paper critically reviews SoC estimation methodologies presented by scholars in the last five years, presenting the fundamentals and main drawbacks of each method. The approaches that have not been extensively used during recent years have not been cited here. From the review of the different approaches, it can be concluded that the hardest part of obtaining a battery SoC estimation is to build a model that reflects the reality inside the battery, including the impact of temperature dependencies on internal resistance and capacity fading. It can also be concluded that the accuracy of SoC estimation may be affected by factors such as modeling imperfections, parametric uncertainties, sensor inaccuracies, and measurement noise. There are also some other factors that affect the battery performance (and therefore, the estimation method), including self-discharging, aging effects, imbalance between cells, capacity fade, and temperature effects. No matter the method, there must always be a trade-off in battery modeling between accuracy and computational complexity. The literature shows that the aging of LiBs is influenced by temperature, time, SoC, cycle number, charge rate, and depth of discharge. Also, the SoC estimation accuracy is affected by the inclusion or not of these parameters into the battery models. Those SoC estimation techniques that continuously update the model parameters can address the aging phenomenon. The review shows that the temperature makes model parameters vary. So the inclusion of thermal behavior in the model used for SoC estimation is needed for better SoC estimation accuracy.

For real-time EV application, the model has to be as simple as possible, keeping the accuracy of SoC estimation within a reasonable range. ECM is regarded as the most appropriate for online estimation and, based on this type of model the adaptive filter-based and artificial-intelligence-based approaches are presented to estimate the SoC with high precision. However, the lack of physical–chemical explanation for the microscopic movements in the battery is the main drawback of this model. Meanwhile, the electrochemical model, which could illustrate the charge transfer between two electrodes and reveal the electrochemical mechanism, is reported as too complicated to be used for online calculation. From the review, it is clear that adaptive filter-based algorithms are more suitable for EV applications, and those based on artificial intelligence are not suitable for this application due to its intensive computing and/or offline learning process requirements. For solving the optimization problem in filter-based techniques, the trend is to use artificial-intelligence-based optimization techniques because of their simplicity, flexibility, derivation-free mechanism, and local optima avoidance.

As the battery modeling is a fundamental process to establish an accurate SoC estimation algorithm, and due to the battery modeling methods proposed by literature not being accurate enough

under specific conditions and having several restrictions on aging assessment to continually update the models, it is necessary to perform more research in this field. The building of practical battery and the application of the adaptive control technology, the expert system theories, and artificial intelligence in the modeling process are required. It is important to consider that none of the reviewed methods is entirely efficient and reliable, and although it may be complete and accurate for an application under certain conditions, it may be inaccurate for others. Therefore, the selection of the appropriate algorithm is up to the designer, mainly depending on his or her knowledge of the addressed application. To this aim, the information provided earlier can help with choosing the most convenient approach.

Acknowledgments: We would like to thank the Administrative Department of Science, Technology, and Innovation of the Colombian government, COLCIENCIAS, for supporting this work, and the University Politécnico Colombiano Jaime Isaza Cadavid for covering the costs to publish in this journal. The authors also want to thank Universidad de Antioquia for the support of the project CODI 2015-7747.

Author Contributions: All authors contributed to the paper. Nicolás Muñoz-Galeano was the director of the research project; Juan Pablo Rivera-Barrera was responsible for collecting the information and analizing the different methodologies; Henry Omar Sarmiento-Maldonado was the advisor of the project. All authors were responsible for organizing and revising the whole paper and for classifying the different methodologies.

Conflicts of Interest: The authors declare no conflict of interest.

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Small Signal Stability of a Balanced Three-Phase AC Microgrid Using Harmonic Linearization: Parametric-Based Analysis

Atta Ur Rahman *,†, Irtaza Syed and Mukhtar Ullah

Electrical Engineering Department, National University of Computer and Emerging Sciences, Islamabad 44000, Pakistan; irtaza.syed@nu.edu.pk (I.S.); mukhtar.ullah@nu.edu.pk (M.U.)

* Correspondence: atta.rahman@nu.edu.pk; Tel.: +92-334-355-9900

† Current address: Electrical Engineering Department, National University of Computer and Emerging Sciences, Islamabad 44000, Pakistan.

Received: 31 October 2018; Accepted: 17 December 2018; Published: 21 December 2018

Abstract: The growth of power-electronic-based components is inescapable in future distribution grids (DGs). The introduction of these non-linear components poses many challenges, not only in terms of power quality, but also in terms of stability. These challenges become more acute when active loads are behaving as generators and power is flowing in reverse direction. The frequency-domain-based impedance modeling methods are preferred for small signal stability analysis (SSSA) of DGs involving such non-linear components. The harmonic linearization method can be used for impedance estimation, and afterwards, the Nyquist stability criterion can be used for stability analysis. In this paper, a parametric-based stability analysis of grid-connected active loads at the point of common coupling (PCC) is done by changing the parallel clustering distance and size of active loads. The results verify a positive impact on the stability of increasing parallel clustering and distance from the PCC and a negative impact of increasing the size of individual active loads.

Keywords: DC-AC power converters; frequency-domain analysis; impedance-based model; Nyquist stability analysis; small signal stability analysis; harmonic linearization

1. Introduction

Electrical energy is the global source of energy, and every device in the future will eventually switch to the electric source of energy. It is necessary to not only utilize every possible resource of energy, but also make the transmission system as efficient, reliable, and stable as possible. The worldwide integration of renewables and other power electronic (PE)-based resources at distribution grids (DGs) is an effort to meet this ever-increasing energy demand [1–3].

The PE-based components, which are non-linear devices and draw/deliver constant power, have a dominant role in the future DGs [4–7]. It is expected from the PE-based active loads to give support to the grid under the IEEE-1547 grid integration code [8]. These PE-based non-linear devices behave as negative impedances and have a constant power nature, so traditional stability methods are unable to deal with these [9–13]. The growth and clustering of these new PE-based components at or near the point of common coupling (PCC) may lead to the instability of DGs [14–19].

In the frequency domain, the impedance-based modeling methods are used for small signal stability analysis (SSSA), where the impedances are estimated at the PCC to apply the stability criterion. Two frequency domain impedance-based SSSA modeling methods are harmonic linearization (HL) [20–22] and the impedance estimation method used for balanced three-phase system transformation into the synchronous reference frame (SRF) [23–27]. A comparative analysis for different stability analysis techniques is given in Table 1.

Table 1. Comparative analysis of different stability techniques [20,28–33]. SRF, synchronous reference frame.

Model	Disadvantages	Reference
Lyapunov Methods (Time Domain)	A detailed system modeling is required for this method, so it does not work well for complex large systems. Its converter model is unable to capture the harmonic effect.	[28,29,31,33]
Probabilistic Methods (Time Domain)	It requires huge computational effort, so this method is very time consuming. Inaccurate first approximation may lead to faulty conclusions. Not all applied schemes work for complex large systems.	[32]
Phasor Model	It is often not differentiable due to significantly higher dimensions.	[20]
Bifurcation Theory	It is slow in the time domain and more complicated in the frequency domain for a higher order system.	[30]
SRF Method	Limited to only balanced three-phase systems.	[20,33]

In the SRF method, the balanced three-phase shunt current perturbation is used for impedance estimation [24,34–36] with the automated unit as presented in [36,37]. The impedance can be measured in real time with negligible additional cost [21,22,25,38–43] by this method. The limitation of the SRF method is that it can only be used to extract the impedances for balanced three-phase systems. This method is unable to capture harmonic effects. This method does not work for a system that is a combination of single- and a three-phase system. Furthermore, this method cannot be used for such a three-phase system in which one specific phase is heavily loaded as compared to the other phases or for an unbalanced system when a fault or other abnormal conditions occur [20,33]. In these scenarios, the zero-axis component is not zero, so the model cannot be linearized by using the SRF method to extract the impedances [20].

HL can be used without the limitations of SRF and is generally applicable to all kinds of AC systems. It can be used for a balanced three-phase system, a single-phase system, an unbalanced three-phase system having harmonics, and a three-phase system having one phase heavily loaded as compared to the other phases [20,33]. This method decomposes the AC system into linear and time-invariant symmetrical components without cross-coupling between them. Here, HL has many advantages over the other methods.

In this paper, the three-phase harmonic shunt-current-injection technique is used to introduce harmonic current perturbation at the PCC. The resultant harmonic voltage and harmonic current components on the source side and load side respectively are used to estimate the source and load side impedances by using the HL technique.

2. System Modeling Using HL

In this technique, the impedances of the non-linear system are extracted by superimposing a specific harmonic component. Superimposing a specific harmonic component involves two steps: firstly, harmonic perturbation is introduced into the system at the PCC, and secondly, the system response is monitored by using symmetrical components (positive, negative, and zero components).

To estimate the impedances, the perturbation source is switched in at the PCC to inject the perturbations into the system. This perturbation source should have a perturbation magnitude significantly higher than the magnitude level PCC to have an impact at the PCC. Current perturbations are usually preferred because these are used in shunt configuration (as shown in Figure 1) as compared to voltage perturbations used in series configuration [24,34]. There are two basic methods, one based on electronic circuits and the other based on wound rotor induction machines, to switch in shunt current perturbations' source for practical impedance estimation [34]. After injecting the perturbations at the PCC, the corresponding change in the source side and load side parameters (voltages and currents) is measured.

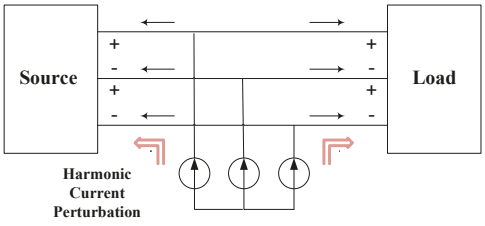


Figure 1. Current perturbation injection in the shunt configuration.

The Nyquist stability criterion (NSC) and/or Bode plot stability criteria are applied after developing the impedance-based model for the stability analysis in the frequency domain. Mostly, NSC is applied to verify the stability of the interconnected systems after extracting the impedances of both sides at the PCC.

The HL technique can deal with the positive and negative components of symmetrical components separately by using the property of linear time-invariant (LTI) systems. The system is stable only if all the components of the sequence domain are stable.

In the HL technique, specific harmonic perturbations are injected at a specific point, usually at the PCC. The old and new values of voltages and currents are measured both at the source side and load side. From the ratio of voltages and currents, the impedances are extracted from both the source and the load side.

This technique estimates the stability of the overall system at the PCC after extracting impedances through symmetrical components by developing a linear model (along a periodically time-varying operation trajectory) of the AC system having non-linear components. This operation trajectory may consist of any single harmonic or a collection of multiple odd harmonics for impedance extraction. The corresponding impedances in the sequence domain are extracted by using the harmonic balance principle [44] and small-signal approximation, assuming that the harmonic perturbation is sufficiently small.

To ensure the power quality and grid stability, it is necessary that the grid interconnection of active loads be carefully examined. The objective of this work is to estimate and establish the pattern of small signal stability (SSS) in relation to the varying sizes, penetration level, and distances of the active loads from the PCC (as shown in Figure 2) to assess the stability of the distribution grid. Figure 2 describes how the size, distance, or penetration is changed for comparative stability analysis.

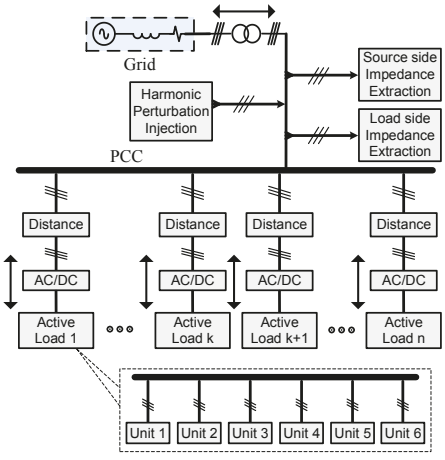


Figure 2. Comparative stability analysis of grid-connected active loads at the point of common coupling (PCC) with changing size, distance, and penetration.

3. Mathematical Modeling of the Impedances at the PCC

By applying the concept of the feedback control system on the simplified power system shown in Figure 3, the transfer function with $V_l(s)$ as output, $V_s(s)$ as input, $Z_1(s)$ as forward gain, and $Z_s(s)$ as reverse gain is given in (1).

$$\frac{[V_l(s)]}{[V_s(s)]} = \frac{1}{1 + [Z_1(s)][Z_s(s)]^{-1}} \tag{1}$$

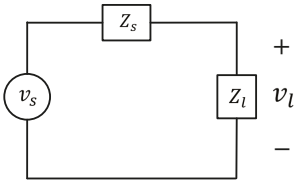


Figure 3. Simplified power system as a feedback control system.

The open loop gain, $L(s)$ can be extracted by rearranging (1) as given in (2).

$$V_l(s) = [1 + [Z_1(s)][Z_s(s)]^{-1}]^{-1}[V_s(s)] \tag{2}$$

The stability can be determined by applying the NSC and only observing the Nyquist contour of the open loop transfer function, as given in (3).

$$L(s) = [Z_1(s)][Z_s(s)]^{-1} \tag{3}$$

The transfer function of this power system can be determined in terms of input voltage V_s and output voltage V_l, as shown in (4), where the term 012 (zero-positive-negative) represents that the quantities are in the HL.

$$\frac{V_{l(012)}(s)}{V_{s(012)}(s)} = \frac{1}{1 + [Z_{l(012)}(s)][Z_{s(012)}(s)]^{-1}} \tag{4}$$

This can be rearranged as given by (5) to extract the open loop gain $L(s)$ to apply the NSC on the open loop gain in (3).

$$V_{l(012)}(s) = \frac{V_{s(012)}(s)}{1 + [Z_{l(012)}(s)][Z_{s(012)}(s)]^{-1}} \tag{5}$$

Since the HL technique uses the symmetrical components for stability analysis, therefore relations are expressed in terms of the symmetrical components.

By increasing the parallel clustering of the active loads, at a specific frequency, the effective value of the load side impedance decreases at the PCC as shown in Figure 4 and as given by (6), where Z_a is the impedance of non-linear active loads connected at the PCC.

$$\frac{1}{Z_a} = \frac{1}{Z_{a1}} + \frac{1}{Z_{a2}} + \frac{1}{Z_{a3}} + \frac{1}{Z_{a4}} + ... + \frac{1}{Z_{an}} \tag{6}$$

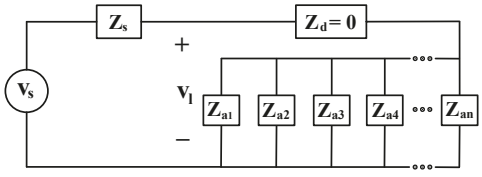


Figure 4. The effect of increasing penetration on load side impedance.

The total load side impedance Z_l can be expressed as given by (7).

$$Z_l = Z_d + Z_a \tag{7}$$

On the other hand, by increasing serial clustering (size) at the PCC, at a specific frequency, the effective value of load side impedance Z_l increases, as shown in Figure 5 and as given by (8).

$$Z_l = Z_{a1} + Z_{a2} + Z_{a3} + Z_{a4} + ... + Z_{an} + Z_d \tag{8}$$

If (8) is compared with (7), it is clear that the value of $Z_a = Z_{a1} + Z_{a2} + Z_{a3} + Z_{a4} + ... + Z_{an}$ is increasing with size while Z_d remains constant.

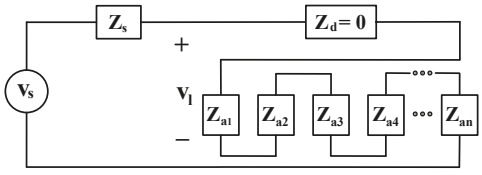


Figure 5. Effect of increasing the size on load side impedance.

Finally, by increasing the distance from the PCC, at a specific frequency, the effective value of the load side impedance Z_l decreases. This is because as the distance increases, the contribution of non-linear active load impedance in total series impedance decreases, as shown in Figure 6 and as given by (9).

$$Z_l = Z_{d1} + Z_{d2} + Z_{d3} + Z_{d4} + ... + Z_{dn} + Z_a \tag{9}$$

If (9) is compared with (7), it is clear that the value of $Z_d = Z_{d1} + Z_{d2} + Z_{d3} + Z_{d4} + ... + Z_{dn}$ is increasing with distance, while Z_a remains constant.

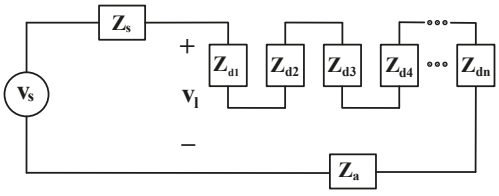


Figure 6. Effect of increasing distance from the PCC on load side impedance.

In the impedance-based method, the perturbations are injected into the distribution system with the perturbation injection point dividing the system into two parts. The part with larger AC sources is called the source side, and the other part is called the load side.

The first step to determine the impedance is to superimpose the harmonic perturbation over the fundamental carrier signal. Then, the second step is to determine the resultant change in the response of that specific harmonic component at the frequency of interest. The fundamental or any other single harmonic, as well as multiple harmonics can be superimposed on the original power wave to extract the impedances. The current perturbations are injected into the system in shunt, as shown in Figure 1. Three-phase AC voltage and current are converted into symmetrical components at the point of injection. The source and load impedances are then extracted using the ratio of voltage and current at the extraction point. The impedance extracted from the ratio of symmetrical components of voltage and currents can be directly used for stability analysis. A typical impedance measurement setup is shown in Figure 7.

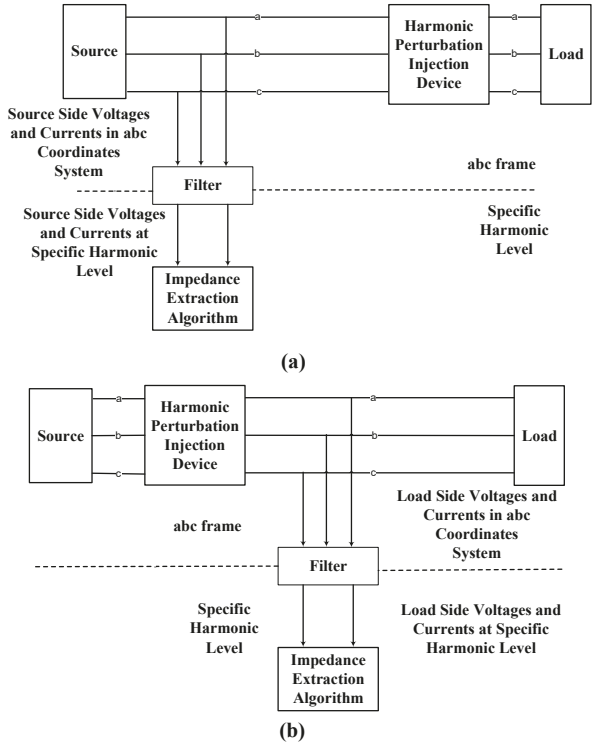


Figure 7. Impedance measurement setup for the (**a**) source side and (**b**) load side.

The load and source side impedance matrix in symmetrical components are given by (10) and (11):

$$\left[Z_{l(012)}\right]_{3\times3} = \begin{bmatrix} Z_{l(00)} & Z_{l(01)} & Z_{l(02)} \\ Z_{l(10)} & Z_{l(11)} & Z_{l(12)} \\ Z_{l(20)} & Z_{l(21)} & Z_{l(22)} \end{bmatrix} \tag{10}$$

$$\left[Z_{s(012)}\right]_{3\times3} = \begin{bmatrix} Z_{s(00)} & Z_{s(01)} & Z_{s(02)} \\ Z_{s(10)} & Z_{s(11)} & Z_{s(12)} \\ Z_{s(20)} & Z_{s(21)} & Z_{s(22)} \end{bmatrix} \tag{11}$$

The relation between voltage and current in symmetrical components on the load side is given by (12) for a balanced three-phase system.

$$\left[V_{l(012)}\right]_{3\times1} = \left[Z_{l(012)}\right]_{3\times3} \left[I_{l(012)}\right]_{3\times1} \tag{12}$$

The perturbations are introduced at the PCC to build nine full equations based on a 3×3 impedance matrix for both the source side and the load side. A single perturbation can generate only three equations (for both the source and load side) [45]. At least three perturbations are introduced to build full 3×3 impedance matrices for the source and the load side. Voltages on the load side in HL after first perturbation are given by (13):

$$\left[V^1_{l(012)}\right]_{3\times1} = \left[Z_{l(012)}\right]_{3\times3} \left[I^1_{l(012)}\right]_{3\times1} \tag{13}$$

The voltages in HL on the load side after the second perturbation are given by (14):

$$\left[V^2_{l(012)}\right]_{3\times1} = \left[Z_{l(012)}\right]_{3\times3} \left[I^2_{l(012)}\right]_{3\times1} \tag{14}$$

The voltages in HL on the load side after the third perturbation are given by (15):

$$\left[V^3_{l(012)}\right]_{3\times1} = \left[Z_{l(012)}\right]_{3\times3} \left[I^3_{l(012)}\right]_{3\times1} \tag{15}$$

Equations (13)–(15) can be written in combined form as (16).

$$\left[V_{l(012)}\right]_{3\times3} = \left[Z_{l(012)}\right]_{3\times3} \left[I_{l(012)}\right]_{3\times3} \tag{16}$$

Rearranging (16) results in (17),

$$\left[Z_{l(012)}\right]_{3\times3} = \left[V_{l(012)}\right]_{3\times3} \left[I_{l(012)}\right]^{-1}_{3\times3} \tag{17}$$

Similarly, for the source side, (17) can be rewritten as (18):

$$\left[Z_{s(012)}\right]_{3\times3} = \left[V_{s(012)}\right]_{3\times3} \left[I_{s(012)}\right]^{-1}_{3\times3} \tag{18}$$

The unknown impedances can be found through simulation or the experiment-based impedance method.

4. Simulation Results

The Simulink model of the grid-connected PV systems (shown in Figure 8) was used for stability analysis.

The detail of the system parameters is tabulated in Table 2. In this model, different PV systems, each having a rating of 100 kW, were integrated with PCC. In this configuration, each unit of the PV system consisted of 100 kW, and the size of the active load may consist of multiple units. To achieve the objective of comparative analysis, it was assumed that all the PV systems were working at the same temperature and receiving the same amount of irradiance. The stability at the PCC was evaluated against three different indices. These three indices were;

1. First, stability was assessed by changing the parallel clustering (penetration) of grid-connected active loads.
2. Then, the stability was evaluated by changing the distance of active loads from the PCC.
3. Afterwards, the stability at the PCC was assessed by changing the serial clustering (size) of active loads.

These parameters were changed one by one, and the corresponding change in load side impedance at the PCC was recorded. Then, NSC was applied on the load side and source side impedance in each of the above cases. The corresponding Nyquist plots were drawn against different specific values of these parameters. The objective was to assess how varying these parameter affected the stability at the PCC.

Table 2. Parameters at the PCC for different penetrations of active loads.

Parameter	Symbol	Value	Symbol	Value
Power Source	P	2500 MVA	V	120 kV
Line Section	$R[r_1]$	[0.1153]	$L[r_1]$	$[1.05 \times 10^{-3}]$
Line Section	$R[r_0]$	[0.413]	$L[r_0]$	$[3.32 \times 10^{-3}]$
Industrial Load	P	30 MW	Q	2 MVar
Residential Load 1	P	2 MW	Q	0
Residential Load 2	P	100 kW	Q	0

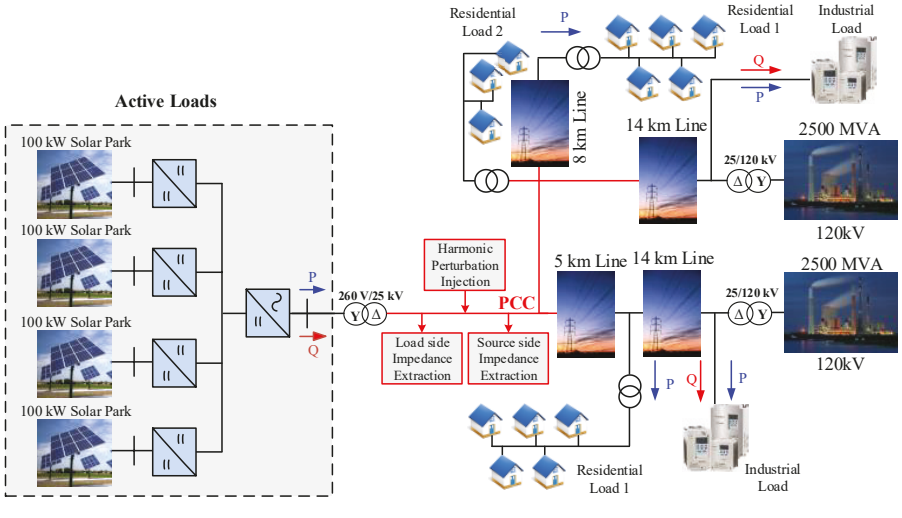
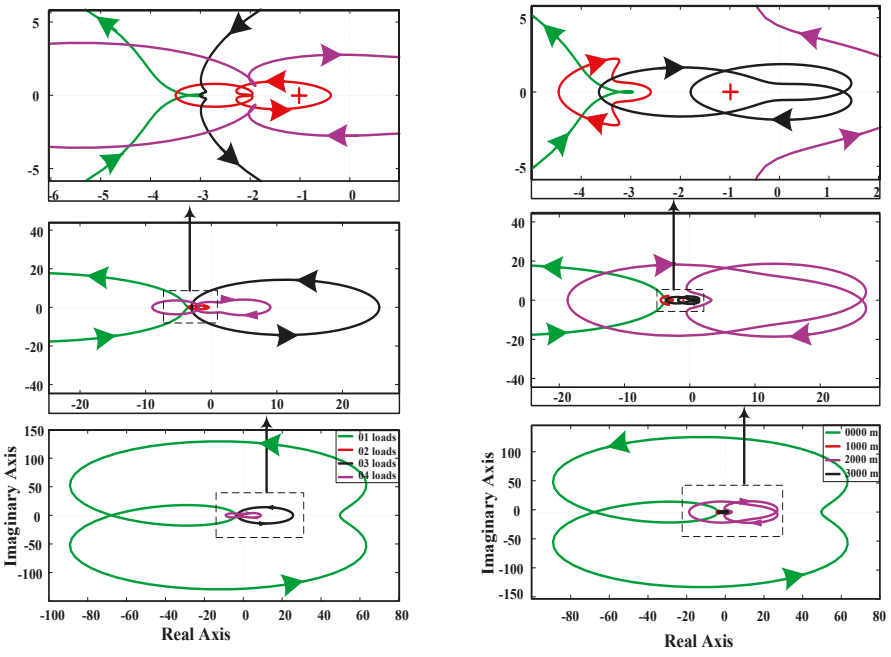


Figure 8. Simulink model of grid-connected active Loads.

The dynamic models of grid-connected active loads were developed and designed in MATLAB Simulink. The block diagram of the grid-connected active loads is shown in Figure 2 where PCC was working at a 25-kV voltage rating. Figure 2 describes how the size, distance, or penetration was changed for comparative stability analysis.

4.1. Effect of Penetration

The first objective was to check the stability pattern at the PCC against various penetrations. The penetration of active loads was varied in a systematic way, and the corresponding change in load side impedance was recorded. The resultant Nyquist plots for different values of parallel clustering by keeping the distance and size constant are shown in a single plot in Figure 9a.



(**a**) Nyquist plot for different penetrations. (**b**) Nyquist plot for different distances from PCC.

Figure 9. Nyquist plot for different penetrations and distances.

It is clear from these plots that as the parallel clustering increased, the anti-clockwise encirclements of -1 vanished. The anti-clockwise encirclements of -1 depicted the total number of closed loop poles in the night half plane, which caused the instability of the system. When the anti-clockwise encirclements of -1 vanished, the system became stable. The microgrid system was designed in such a way that the PCC was working at a stability boundary for different indices. Therefore, as the system indices were changed near the PCC, the system changed from unstable to stable or vice versa. Not all of the Nyquist plot is clearly visible to the naked eye, so the selected parts of the lower Nyquist plots are zoomed-in and shown above for better and clear understanding of the Nyquist plots. The system at the PCC was unstable when only a single active load (of size 700 kW i.e., seven units) was connected at the PCC (distance = 0 km). The Nyquist plot of one active load depicted an anti-clockwise encirclement, as shown in the lower part of Figure 9a. Similarly, the system at the PCC was still unstable when two and three active loads were connected respectively at the PCC in parallel configuration, as shown in the zoomed-in version of Figure 9a. When the parallel clustering reached the four active loads,

keeping size and distance unchanged, the system at the PCC became stable. The stability would further improve by increasing the penetration at the PCC by keeping the distance and size constant.

4.2. Effect of Distance from PCC

To check the effect of the distance of active loads from the PCC to the stability at the PCC, the distance of active load was varied by keeping the penetration and size constant. The objective of selecting a specific penetration and a specific size was to keep the PCC near the stability boundary. The penetration of one active load and the size of seven units (700 kW) were chosen in this case. The load side impedance was recorded by changing the distance from the PCC by keeping the penetration and size constant in all the cases. The NSC was applied on the load and the source side impedances to get the Nyquist plot for different values of distances, as shown in Figure 9b.

The results show that the system was unstable at the PCC when the distance was 0 km because there was a pole in the right half plane (anti-clockwise encirclement of -1). As the distance was increased to 1 km, the anti-clockwise encirclement vanished (as shown in the zoomed-in version of the Nyquist plots), so the system became stable at the PCC. This stability further improved as the distance increased to 2 km and 3 km, respectively, by keeping the size and penetration constant.

4.3. Effect of the Sizes of Active Loads

To check the effect of changing the size of an active load on the stability at the PCC, the size was varied by keeping the distance and penetration constant. A single active load was connected at the PCC in this case, so the distance was 0 km and the penetration was one active load. The load side impedance changed by changing the size. Different Nyquist plots were obtained when NSC was applied on different values of load side impedances and the same value of source side impedance. These Nyquist plots, each corresponding to different sizes of an active load, are shown in Figure 10.

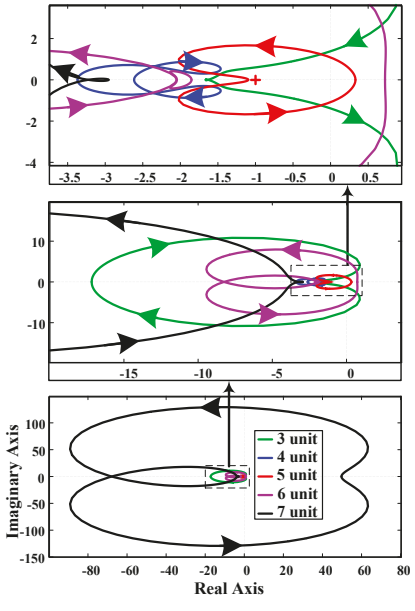


Figure 10. Nyquist plot for different sizes of active loads.

Initially, the system was stable at the PCC, as there were no anti-clockwise encirclements of -1, which depicts that there were no poles in the right half plane. The system remained stable when the

size of active loads was equal to or less than four units (400 kW). As the size of the system reached five units (500 kW), the system became unstable, and there was an anti-clockwise encirclement of −1, which depicts a pole in the right half plane. The stability further deteriorated as the size was increased further.

The summery of the above three cases is given in Table 3. According to this table, when the size was increased by keeping other parameters constant, the stability at the PCC deteriorated. When the distance was increased from the PCC by keeping other parameters constant, the stability at the PCC improved.

When the penetration was increased at the PCC by keeping the distance and size constant, the stability at the PCC improved. The stability behavior at the PCC by changing the size, distance, and penetration is given in Figure 11. Figure 11 depicts the stability region in connection with size, distance, and penetration. Firstly, keeping distance (=0 km) and penetration (=1) constant, the instability boundary for size was six units. As the size decreased, the stability improved. The direction of the arrow shows the stability behavior (from the unstable to stable region and from the stable to more stable region). Secondly, keeping distance (=0 km) and size (=7 units) constant, the instability boundary for penetration was one active load. The direction of the arrow shows the stability behavior, so as the penetration increased, the stability improved further. Finally, keeping size (=7 units) and penetration (=1) constant, the instability boundary for distance was 0 km. As the distance increased, the stability improved further. These results verified that there was a strong relation between these parameters and the stability at the PCC. Changing any other system components, the stability boundary would shift, but the behavior of the stability and the relation to these parameters will remain the same.

Table 3. Effect of different parameters on stability.

Penetration	Distance at PCC	Size	Effect on Stability
Increasing	Constant	Constant	Improve
Constant	Increasing	Constant	Improve
Constant	Constant	Increasing	Deteriorate

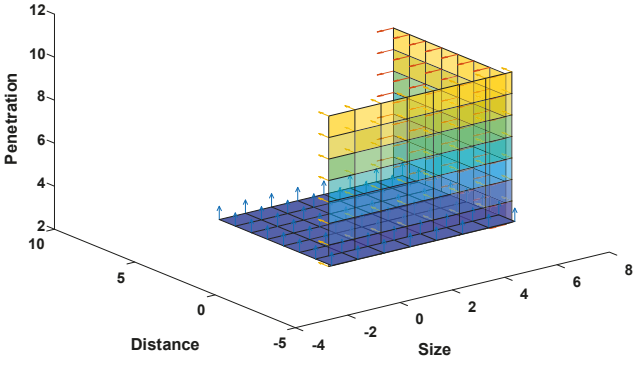


Figure 11. The stability behavior at the PCC for different sizes, distances, and penetrations.

The simulation results presented were near the stability boundary. These results and stability boundaries were only specific for the system designed for simulation. Changing the system would change the stability boundary because impedance would change. However, the relation of different parameters with the Nyquist stability would remain the same.

5. Conclusions

In this paper, the SSSA at the PCC was done by varying one of three parameters (size distance and penetration) and keeping the other two constant. The results show that the stability pattern of NSC changes in a systematic way in response to a systematic change in any of these parameters. The impact of increasing penetration and increasing distance from the PCC was positive on the stability at the PCC, while the impact of increasing the size (while keeping the other parameters constant) was negative on the stability at the PCC. Thus, a change in any of these parameters will play a significant role in deciding the stability at the PCC.

The design and composition, as well as the distance from the PCC of active loads play an important role in the SSS of an AC microgrid. These parameters must be thoroughly assessed before deploying active loads at the PCC.

Author Contributions: Conceptualization, A.U.R. and I.S.; Methodology, A.U.R. and I.S.; Software, A.U.R. and M.U.; Validation, A.U.R. and M.U.; Formal analysis, A.U.R. and I.S.; Investigation, A.U.R.; Writing original draft preparation, A.U.R.; Writing review and editing, I.S. and M.U.; Supervision, I.S.; Project administration, M.U.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

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Energy Management and Switching Control of PHEV Charging Stations in a Hybrid Smart Micro-Grid System

Tariq Kamal [1,2,*], Murat Karabacak [2], Syed Zulqadar Hassan [3], Luis M. Fernández-Ramírez [1], Muhammad Tanveer Riaz [3], Muhammad Abbas Khan [5] and Laiq Khan [6]

1 Research Group in Electrical Technologies for Sustainable and Renewable Energy (PAIDI-TEP-023), Department of Electrical Engineering, University of Cadiz, Higher Polytechnic School of Algeciras, 11202 Algeciras (Cadiz), Spain; luis.fernandez@uca.es

2 Department of Electrical and Electronics Engineering, Sakarya University, 54050 Sakarya, Turkey; muratkarabacak@sakarya.edu.tr

3 State Key Laboratory of Power Transmission Equipment and System Security and New Technology, School of Electrical Engineering, Chongqing University, 400044 Chongqing, China; syedzulqadar.hassan.pk@ieee.org (S.Z.H.); tanveer.riaz@ieee.org (M.T.R.)

4 Department of Electrical Engineering, Lahore University of Management Sciences (LUMS), 54792 Lahore, Pakistan; hussnainriaz8@gmail.com

5 School of Electronics and Information Engineering, Changchun University of Science and Technology, Jilin 130022, China; engineerabbaskhan111@gmail.com

6 Department of Electrical Engineering, COMSATS Institute of Information Technology, 22060 Abbottabad, Pakistan; laiq@ciit.net.pk

* Correspondence: tariq.kamal.pk@ieee.org; Tel.: +90-536-6375731

Received: 30 June 2018; Accepted: 20 August 2018; Published: 22 August 2018

Abstract: In this study, the energy management and switching control of plug-in hybrid electric vehicles (PHEVs) in a hybrid smart micro-grid system was designed. The charging station in this research consists of real market PHEVs of different companies with different sizes. The rate of charging of PHEVs is managed via switching control to receive maximum benefits from renewable energy sources and reduce the consumption of electricity from the grid. To support the optimum utilization of sustainable power, charging time and network stability, seven scenarios were developed for different interaction among the proposed micro-grid system and PHEVs. The proposed hybrid smart micro-grid system consists of three renewable energy sources: photovoltaic (PV) array controlled via an intelligent fuzzy control maximum power point subsystem, a fuel cell stack and a microturbine set controlled by proportional integral differential/proportional integral subsystems. A hybrid energy storage system (super-capacitor, battery storage bank and hydrogen) and residential load are also included in the proposed architecture. The hybrid smart micro-grid system is checked in terms of voltage regulation, frequency deviation and total harmonic distortion (THD). It was found that these are in limits according to the international standards. The simulations verify the feasibility of the proposed system and fulfill the requirement of vehicle-to-grid and grid-to-vehicle operations in a smart grid environment.

Keywords: plug-in hybrid electric vehicles; power management system; renewable energy sources; fuzzy; smart micro-grid

1. Introduction

Due to environmental concerns, depletion of fossil fuels, and advances in battery storage system, PHEVs have received a great amount of attention in the transportation sector [1,2]. These days, the

world is looking towards renewable energy sources such as solar, wind and biomass to produce green energy. This green energy can be utilized by vehicles which are considered the main sources of environmental pollution. For example, 33.7% of greenhouse gas emissions were released by the transportation sector to the environment in 2012 [3]. Similarly, many American Lungs Association projects have stated [4] that the transportation sector is responsible for numerous lung diseases in America. Consequently, transport industries have introduced low emission vehicles such as PHEVs to directly address these problems. Therefore, each year, the purchase of PHEV increases worldwide. In the future, many Electric Vehicles (EVs) will be available in the transportation sector. For example, in 2015, approximately one million PHEVs were on US roads and 425,000 PHEVs were sold [5,6]. Furthermore, the Electric Power Research Institute have concluded that the PHEVs market share may reach up to 62% by 2050 in the US [7]. In the US, there are about 250 million registered vehicles. Using a moderate scenario since 2020, if the US vehicle fleet is 10% PHEVs and each vehicle uses 25 kWh battery capacity, the total 625 GWh would be a potential threat to today's utility.

The first electric vehicle was sold in Turkey in 2012 [8]. The electric vehicle market in Turkey is now growing very rapidly. According to the Ministry of Science, Industry and Technology of Turkey, PHEVs will become the dominant vehicle choice on the road soon in Turkey. The increasing of PHEVs could burden the existing utility, which can result power losses at the customers end. Specifically, uncontrolled charging can cause grid stability problems on the local scale. Pakistan under Rahmat Group company has signed an agreement with two different Chinese companies to introduce EVs in Pakistan [9]. In the initial stage, the companies will introduce electric buses in the transport market, and in the second phase, a factory would be established at the complex in Jamshoro District of Sindh, Pakistan to produce electric cars and two-wheelers. According to the Energy Conservation Center belonging to the Ministry of Water and Power of Pakistan, the transport sector represents 28% of the total energy consumption in Pakistan. In the Pakistan scenario reported on 30 June 2015, the gap between electricity demand and supply was 5201 MW [10]. Currently, Pakistan is suffering from severe energy crisis, where urban and rural areas are not powered by proper electricity for 8–12 h and 18 h per day, respectively. There is a growing risk that the proliferation of EVs will trigger extreme surges in demand in Pakistan. This cannot be ignored, especially in Pakistan, and therefore, it is imperative to design a Charging Station (CS) setup powered from Renewable Energy Sources (RESs) coupled with smart charging strategies.

Generally, vehicles are supposed to stay for at least 5 h per day in workplace [11]. Hence, making electric CS in a given workplace is beneficial, but the result would be some overloading issues particularly at the distribution level. Since the upgrading of transformer is an inflexible and a quite expensive option, this concern needs close concentration. Many authors in the literature have studied the effect of PHEVs charging on the distribution transformer [12–14]. In [12], the authors discussed the impact of PHEVs on distribution networks, but there is no analytical calculation in the paper. In [13], the authors analyzed the concerns due to the integration of PHEV on the residential distribution networks; however, in this study, the number of PHEVs per distribution transformer was limited to two. The authors concluded in [14] that the power management of the EV battery charge profile can help manage the loss of life of the distribution transformer. However, not much work has been done to charge the PHEVs from several RESs in a smart micro-grid.

Although there are a few published papers about CSs for PHEV supplied by PV [15–18], they present certain limitations. For instance, the control of the PV system was not studied in [15–18]. Further, in all these papers, the authors designed the CSs based on the control of DC-link voltage, but the DC-link voltage has its own limitation and the authors did not consider the control of DC-link voltage when it reaches its maximum limit. Similarly, several authors focused on the residential distribution networks [19–21]. In [22,23], the authors described the overall peak demand due to the charging of EVs. They suggested that it should be managed effectively with proper load management. Smart control strategies that can open the paths for PV systems and EVs to integrate with the current power systems are suggested in [24]. The charging of PHEVs from PV system and its co-benefits are discussed in [25]. The study explains that PV provides an auspicious source of mid-day generation power for PHEVs while PHEVs perform as a

dispatchable load. In another paper, the authors showed that high scale integration of EVs in the existing utility would be possible through management and scheduling [26]. The significance of EVs operating as an energy storage source is studied in [27]. There are three types of charging methods for PHEVs/EVs: Alternating Current (AC) level-1, AC level-2 and Direct Current (DC) level-3 charging. DC charging allows boosting the overall efficiency and providing the opportunity of fast charging [28–30]. The same concept is also supported in [31,32]. This sets it up appropriately to mix distributed renewable power generations such as PV, fuel cells, wind and other energy storage devices such as super-capacitor (SC) using the DC distribution bus (bus is an electrical node, which can be in DC or AC, where two or more electrical elements, such as loads, generators, etc., meet). Different DC charging station infrastructures have been presented by many authors [33,34].

The integration of PHEVs in municipal parking deck using smart energy management system is developed in [35]. The energy management system is there to control provision of energy to the vehicle battery chargers through real time monitoring to secure the maximum consumption of available power from sustainable energy and charging time. None of the papers reviewed provide an intelligent control, power electronics interface and power management of PHEVs in smart micro-grid system, where the primary energy source is controlled efficiently. None of those reviewed studies consider the real weather characteristics, but many researchers have developed charging station using virtual generated weather patterns. Moreover, the intelligent control of a renewable energy source is very important for a stable DC bus voltage. For instance, fluctuations in bus voltage cause power imbalance that originate from different sources of disturbances such as sudden change in solar irradiance or temperature, and abrupt change in PHEVs load. Such a power imbalance results an extra energy. The above-mentioned papers do not discuss the control of photovoltaic in their charging station which is essential for maximum efficiency.

This paper intends a proper power management for different PHEV models in a hybrid smart micro-grid system where the required power for the PHEVs charging is smartly managed from solar, hydrogen energy (fuel cell), natural gas (micro-turbine), SC, battery and grid. The operation of the charging algorithm is performed using dynamic power switches of the power converters controlled via proportional integral differential/proportional integral subsystems. The highly intermittent nature of PV in the proposed hybrid smart micro-grid system is addressed by an isolated intelligent fuzzy inference subsystem. The intelligent fuzzy inference subsystem contributes to minimize the stress on the DC bus and ensures quality and regulated output power to CS. If the power sent by the PV is in excess of the requirement of the PHEVs charging, the remaining power will be supplied to charge the battery and then the SC. If still there is an excess power, then it will be used to produce hydrogen for fuel cell or sent to a national grid. Correspondingly, if the net power provided by the PV is less than the demand, the battery and then the SC will be used to deliver the required power provided their SoC > 20%. If the requirement surpasses the power provided by the combination of PV/SC/battery, the difference is provided by the fuel cell. If there is still a need, the difference will be covered by the Micro-turbine (MT), followed by the national grid. In addition, the proposed CS also comprises of a Battery Storage System (BSS) as supplementary power sources to store the power in off peak hours, which can be used in rush hours to charge the PHEVs or provide to the grid.

This work is arranged as follows: Section 2 gives the description of the proposed hybrid smart micro-grid system. The control of the systems components is described in Section 3. The problem formulation of the proposed work is presented in Section 4. Section 5 deals with the proposed power management. Section 6 supports the performance of the proposed system via simulations, followed by a conclusion in Section 7.

2. System Description

Figure 1 shows the proposed system configuration combining PV system, FC system, SC module and battery bank to form a combine DC bus line by four different non-isolated DC-DC converters. The PV system is taken as the primary power source; SC module and battery bank serves as a short-term storage system; and the Solid Oxide Fuel Cell (SOFC) is used as a backup and long-term storage system [36]. The additional power with respect to the load requirement is used for the battery,

SC charging and hydrogen production for later use in the SOFC. The output of the DC bus link is combined through a three-phase main inverter to supply the desired power to the grid if only one source is accessible. On the other hand, the PHEVs/EVs CS, MT, residential load and utility grid are integrated to form an AC bus line. The MT also behaves as a backup to take full advantage of RESs, while the CS acts as either load under the Grid-to-Vehicle (G2V) concept or distributed sources of energy under the Vehicle-to-Grid (V2G) revenue opportunity [37]. The MT interface consists of a rectifier followed by a unidirectional hysteresis current control inverter. A bidirectional inverter is used for power sending and receiving from the CS towards an AC bus link. The CS is designed to charge five PHEVs and BSS. The PHEVs are selected from five different companies. The grid attachment is used to accomplish any charging demand more than the RESs output. The development of all energy sources are according to Table 1 and taken from [38–42].

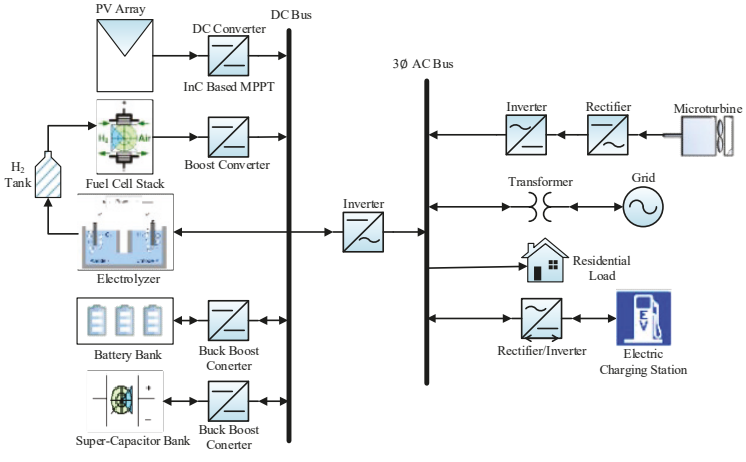

Figure 1. Proposed hybrid smart micro-grid system.

Table 1. RESs and their power converter parameters [36,38,42–44].

PV Array		**Battery**	
Type	SunPower SPR-305-WHT	Type	CINCO FM/BB12100T
Module	305 W @ 1 kW/m^2, 25 °C	Capacity	50 Ah
Number of series/string	13	Single module voltage	12 V
Number of parallel strings	66	No of series connected modules	34
Power Rating	305 × 13 × 66 ≈ 262 kW	Rated Voltage	12 × 34 ≈ 400 V
Supercapacitor		**Fuel Cell Array**	
Type	Maxwell Boost Cap BMOD0165-48.6VUC	Type	Bloom Energy USA ES-5700
Capacitance	165 F	Number of cells in series in the stack	768
Number of series capacitors	50	SOFC Stack	4 kW
Number of parallel capacitors	20	SOFC Array	5 × 10 = 50
No of modules	12	SOFC Array Power Rating	50 × 4 kW = 200 kW
Rated Voltage	12 × 48.6 ≈ 584 V		
Electrolyzer		**Microturbine**	
Type	QualeanQL-85000	Type	Ingersoll Rand MT250
Rated Power	30 kW	Rated Power	200 kVA, 160 kW
Rated Voltage	380 V	Rated Voltage	440 V
Number of Cells in Stack	30	Rated Frequency	50 Hz
Utility Grid		**Main Inverter**	
Phase Voltage	11 kV	Type	Zhejiang, China CHZIRI-2VF
Rated Power	10 MVA	Rated Power	400 kW
Phase Frequency	50 Hz	Rated Voltage	200/540 V

3. Architecture and Control of the Proposed Charging Station

Figure 2 illustrates a detailed structure of the proposed CS, which is located in Pakistan. The major components of CS are the PHEVs, BSS, power converters and the power management controller. A Power Management System (PMS) monitors all the PHEVs and BSS. The algorithm implemented in the PMS senses the State of Charge (SOC), rated charging power of the PHEVs batteries, the peak and off-peak hours, and controls the power flow in the CS, as given in Figure 2. The SoC level provides information about the charging and discharging of the PHEVs/EVs and BSS.

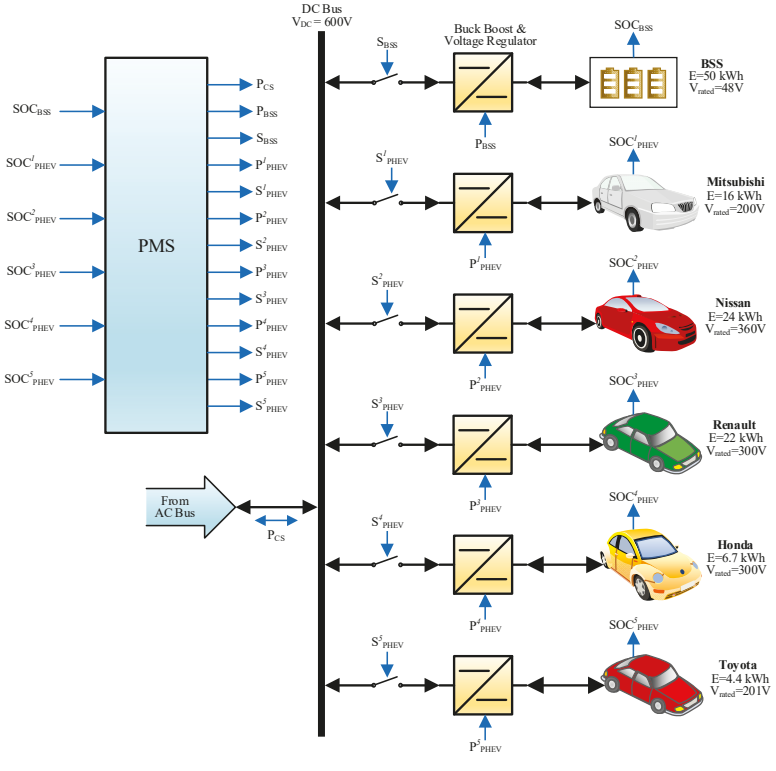

Figure 2. Structure of electric charging station.

The PMS also consists of a Battery Management System (BMS) which prevents the PHEVs and BSS from getting overcharged. The BSS also supports the charging of the PHEVs when there is no power available from the AC bus link. The battery bank in the BSS can be charged from the AC bus link during off peak hours.

Five different types of PHEVs/EVs are considered: Mitsubishi i-MiEV, Kangoo Z.E, Toyota Prius plug-in, Nissan leaf, Honda Accord Hybrid and Renault. Their respective usable battery capacity and charging information is listed in Table 2. Since the PHEVs/EVs are from different automobile manufacturers, their control approach and BSS are based on the charging requirements of each PHEV and BSS. Each PHEV and BSS must have an autonomous buck-boost converter fitted in each charge point in the proposed CS. All the buck-boost converters of the CS are controlled by conventional Proportional Integral Differential (PID) controllers, as shown in Figure 3, and their parameters are given in Table 3.

Table 2. PHEVs technical details [45–49].

Company Name	Vehicle Name	Battery Type	Battery Capacity (kWh)	Range (km)	Charging Rate (kW)		Rated Voltage (V)	Charging Time	
					Slow	Fast		Slow	Fast
Mitsubishi	MiEV	Li-ion	16.0	160	3	50	20	7 h	30 min
Nissan	Leaf	Li-ion	24.0	160	6.6	50	360	4 h	30 min
Renault	Kangoo Z.E.	Li-ion	22.0	170	3	43	300	6 h	30 min
Honda	Civic hybrid	Li-ion	6.7	150	2.2	13.4	300	3 h	30 min
Toyota	Prius	Li-ion	4.4	16	1	8	201	5 h	30 min

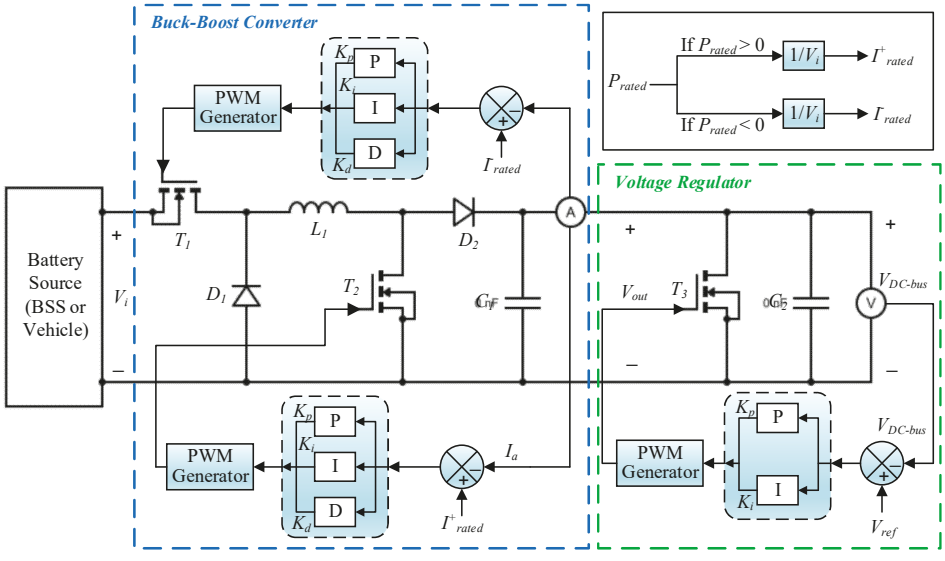

Figure 3. Schematic diagram of a buck boost converter/voltage regulator.

The output of the overall charging station is coupled to the AC bus via a bidirectional inverter-controlled hysteresis current control embedded with PI controllers, as illustrated in Figure 4, whose parameters are shown in Table 1. The PI controllers try to reduce the error to adjust the desired active and the reactive powers. It is assumed that all vehicles have equal market penetration and the analysis is considered for a 24-h cycle for a typical summer day in Pakistan. The proposed architecture is flexible and multiple PHEVs can be charged by increasing the corresponding charging points. Furthermore, the DC-DC boost converter based on the intelligent fuzzy controller is used to exactly track the MPP of the PV, as shown in Figure 5. The intelligent fuzzy controller is modeled using expert knowledge and many inputs. Based on those inputs, the fuzzy rules are defined in the Fuzzy Logic Controller (FLC). A FLC operates in three steps: a fuzzifier to express the crisp value of inputs into their respective fuzzy sets, an inference system to generate appropriate output also in the form of fuzzy sets, and a De-fuzzifier to give the original crisp value through conversion theorems (i.e., center of area). Similarly, a DC-DC boost converter based on PI control is used to control the FC voltage.

Table 3. Buck boost/voltage regulator parameters of the charging station.

Parameter	Representation	Values
CS DC Buck Boost Converter		
Model Type	NCP1136	
V_{rated}	Rated Voltage	10/700 V
C_1	Converter Capacitance	2200 µF
L_1	Converter Inductance	1 mH
K_p, K_i, K_d	PID Gains (T_1)	1.5, 1, 1
K_p, K_i, K_d	Proportional Gain (T_2)	1.5, 1, 1
f	Rated Switching Frequency	10 kHz
CS DC Voltage Regulator		
Model Type	MC33363ADWG	
V_{rated}	Rated Voltage	10/700 V
C_2	Converter Capacitance	4700 µF
K_p	Proportional Gain	0.0005
K_i	Integral Gain	0.15
f	Rated Switching Frequency	10 kHz
CS Converter		
Model Type	Zhejiang, China CHZIRI-2VF	
P_{rated}	Rated Power	220 kW
V_{rated}	Rated Voltage	220/1140 V
f_C	Carrier Frequency	10 kΩ
f_{out}	Frequency of Output Voltage	50 Hz
C_s	Snubber Capacitance	100 kΩ
R_s	Snubber Resistance	10 kΩ
L	Inductance L-Filter	2.6 µH

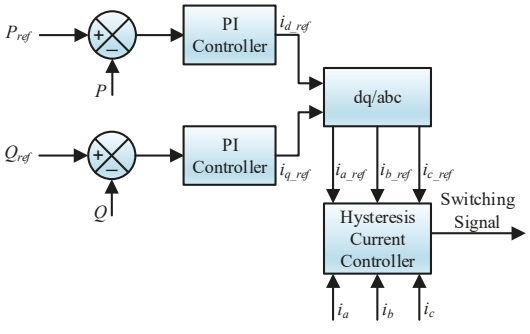

Figure 4. Schematic diagram of charging station converter control.

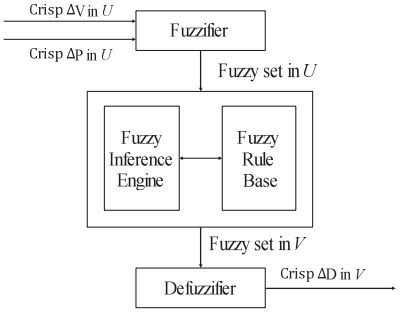

Figure 5. Fuzzy logic controller model.

4. Problem Formulation

In this paper, the objective is to design a decision-making control algorithm for the PHEVs CS by using the available resources (renewable energy, utility grid) for the PHEVs charging, while reducing the stress on the utility grid and satisfying the required demand of all PHEVs and BSS. Equation (1) represents the formulation for the PHEVs CS. According to Equation (1), the actual power level of all vehicles and BSS must reach their reference level within the desired time provided the charging constraints of all PHEVs/EVs and BSS according to Table 2. The power quality and network constraints are according to international standards such as IEC61000 and IEEE 519-2014. Pakistan's LV power network is considered in this work.

$$\begin{aligned} &\bigcup \begin{bmatrix} PHEV_{i=5} \\ BSS \end{bmatrix} \Big|_{t\to\infty} \begin{bmatrix} P_{PHEV_{i=5}}(t) \to P_{PHEV_{i=5\_ref}}(t) \\ P_{BSS}(t) \to P_{BSS\_ref}(t) \end{bmatrix} \\ &\text{s.t :} \\ &\qquad SOC_{i,\min} \le SOC_i(t) \le SOC_{i,\max} \\ &\qquad 0 \le |SOC(t+1) - SOC(t)| \le |\Delta SOC_{i,\max}| \\ &\qquad V_{\min-load\,(rms)} \le V_{load\,(rms)} \le V_{\max-load\,(rms)} \\ &\qquad THD_{\min-v_{load}} \le THD_{v_{st}}, THD_{\min-i_{load}} \le THD_{i_{st}} \\ &\qquad f_{\min-Vfund} < f_{Vload} < f_{\max-Vfund} \end{aligned} \tag{1}$$

where $SOC_{i,\min}$ and $SOC_{i,\max}$ are the user-defined minimum and maximum battery SOCs limits for the ith PHEV/EV. Once SOC_i reaches $SOC_{i,\max}$, the ith battery charger switches to a stand-by mode to avoid the overcharging of the PHEV/EV battery. To prevent large variations in the charging rate over consecutive time slots, the SoC ramp rate is bounded by the constraint $\Delta SOC_{\max}$. $V_{loadrms}$ is the RMS voltage at the customer side; $THD_{v_{st}}$ and $THD_{i_{st}}$ are the acceptable value of total harmonic distortion in voltage and current, respectively; and $f_{\text{min-}vfund}$ and $f_{\text{max-}vfund}$ are the allowable limits in the load voltage frequency deviation.

5. Proposed Power Management System for PHEVS/EVs

There are two main buses: DC and AC bus. The PHEVs/EVs CS is the major part of the AC bus. Therefore, the bidirectional power flow between the CSs and the rest of the system, especially with the grid, occurs via AC bus. The overall PMS consists of seven possible scenarios considered for a 24-h cycle as depicted in Figure 6. Five PHEVS/EVs and BSS are the main actors which take part in the PMS. Before explaining the PMS, one must know the following points which are considered during the simulation.

- For the PHEVs charging, the PMS must to take power from BSS rather than the AC bus.
- Similarly, in the case of discharging of PHEVs, first BSS then the AC bus is used to take power from the PHEVs.
- The PHEV owner will decide how much power he wants to transfer or receive.

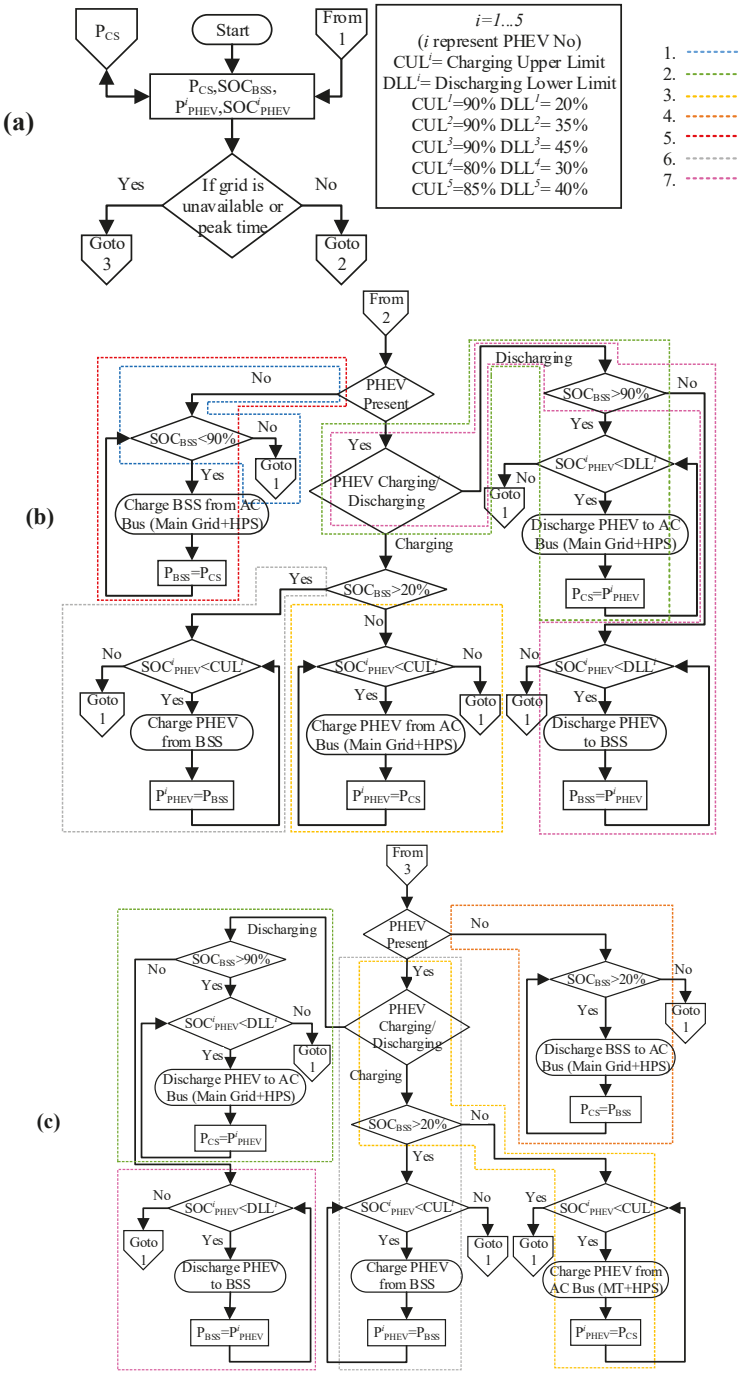

Figure 6. Flow chart of the proposed PMS: (**a**) initial decision stage of the PMS; (**b**) PMS working at off peak hours; and (**c**) PMS working at peak hours.

5.1. Proposed Scenarios for the Charging Station PMS

To develop a proper power management at a CS, several possible scenarios are taken for one complete day depending on the user preference and interest, as shown in Table 4. In a real-time scenario, the power flow between grid and PHEVs depend upon the mutual understanding between them.

Table 4. Possible scenarios.

Scenario	Description
1	No Cars in the CS (Empty CS)
2	Vehicles to AC bus
3	AC bus to Vehicles
4	BSS to AC bus
5	AC bus to BSS
6	BSS to Vehicles
7	Vehicles to BSS

5.1.1. Scenario 1 (No Cars in the CS or Empty CS)

This scenario was considered the normal situation. PHEVs are not present in the CS for charging and BSS is fully charged.

5.1.2. Scenario 2 (Vehicles to AC Bus Line)

This case is the most likely and creates a promising opportunity in the form of V2G or Vehicle-to-Home (V2H). In this scenario, the PMS first checks the availability of the charged PHEVs and the BSS. If the charged PHEVs are available and are programmed to discharge their power and the SoC of BSS is also greater than 90%, then the controller will allow the PHEVs to discharge to the AC bus. This power is further transmitted to the grid or to the load. The owners of the PHEVs will decide how much they discharge their PHEVs, which is automatically accomplished by the controller.

5.1.3. Scenario 3 (AC Bus to Vehicles)

In this situation, the controller first checks the SoC of the BSS. If the BSS is not available for PHEV charging, then the AC bus power is used to charge the PHEVs. It is imperative to show that the maximum power for the AC bus comes from RESs.

5.1.4. Scenario 4 (BSS to AC Bus)

It is also possible that there are no PHEVs in the CS and BSS is charged. The PMS controller will allow the charged BSS to supply its power to the AC bus. Depending upon the choice, the power could be transmitted to the grid or directly to the residential load. Regardless, it will reduce the overall stress on the grid.

5.1.5. Scenario 5 (AC Bus to BSS)

This case is considered for the off-peak time. According to the proposed PMS, if there are no PHEVs and all other loads are satisfied, then the AC bus will supply power to the BSS. The charged BSS will reduce the burden on the grid during peak times.

5.1.6. Scenario 6 (BSS to Vehicles)

Those PHEVs that want to be charged from the BSS are covered in this mode. The proposed PMS will allow the charged BSS to satisfy the required demands of the PHEVs.

5.1.7. Scenario 7 (Vehicles to BSS)

In this case, the controller will allow the PHEV to transfer power to the BSS. All seven scenarios are explained well during simulation.

6. Simulation Results

To evaluate the proposed PMS, simulations were performed in MATLAB/Simulink and the modes of operation are verified. The simulation started at midnight and finished at midnight the next day, on 22 July 2017, in Islamabad, Pakistan. The simulation was performed on an hourly basis for the energy available from the RESs, utility grid and accordingly manages the charging demand of PHEVs/EVs and demand of residential load. The goal was to observe the response of the proposed system over a long period of time including day and night cases. The PHEV/EV battery SOC was used to calculate the charging time and charging energy when the vehicles enter the charging station.

It is important to mention that level 3 (DC fast charging) was used to charge the PHEVs/EVs in this simulation. On fast charging, the vehicle battery takes approximately 30 min to fully charge. The data used for simulation are shown in Table 2. The PV output power obtained by the fuzzy controller is shown in Figure 7. The individual powers available from the PV, SOFC, MT, SC module and the battery bank are shown in Figure 8. The total available power from the different energy sources and the total demand including residential load, CS load and utility grid are shown in Figure 9. To make the discussion simple, the net power available from the PV, SOFC, MT, SC module and the battery bank is represented by P-RESs.

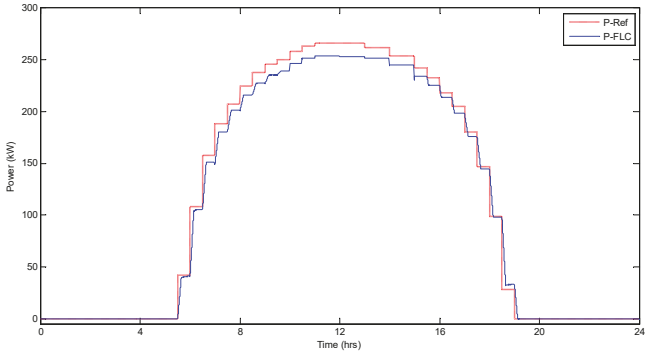

Figure 7. PV output power.

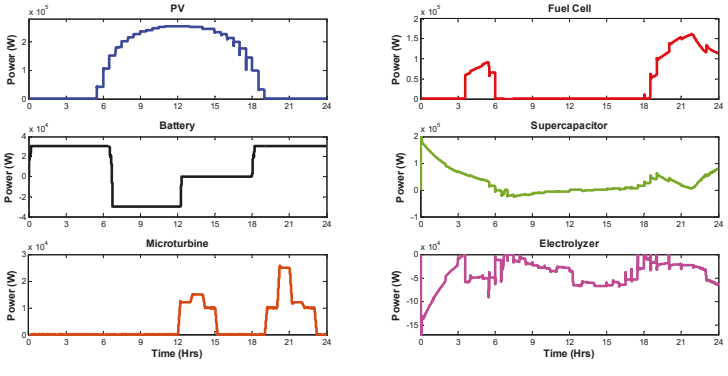

Figure 8. Individual powers of RESs.

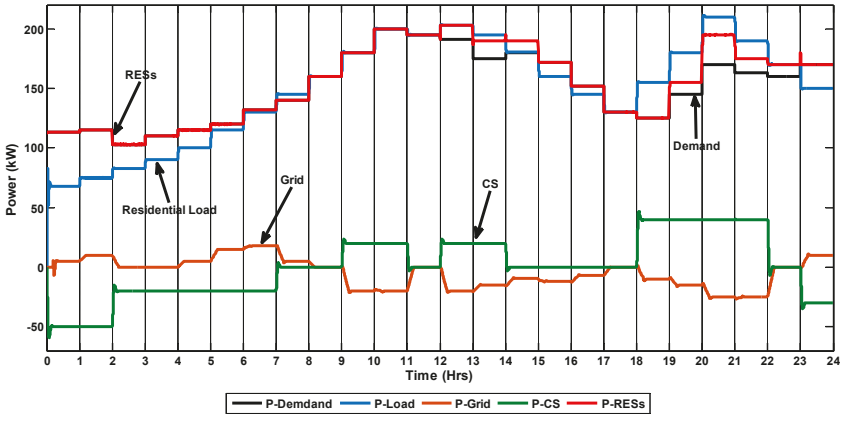

Figure 9. Power of all the energy sources and total demand in the proposed micro-grid.

During t = 0–2 h, it is obvious that the power delivered by the RESs exactly satisfies the total demand. The CS is receiving power from both the RESs and grid, but a higher share of power comes from the RESs, viz., the total demand of the CS in this interval is 100 kW in which the RESs' share is 85 kW, while the utility grid provides 15 kW. In addition, it is noticeable that at this interval there is no PHEVs/EVs present for the charging, therefore the total power received from the AC bus is used to charge the BSS through DC-DC converter and its SOC increases from 40% to 60% (Scenario 5) as shown in Figures 10a and 11. The charged BSS could help to reduce the stress on the grid during the peak times. During t = 2–4 h, the CS need 40 kW power which is completely provided by RESs. This power is utilized to charge the Mitsubishi i-MiEV and Nissan leaf vehicles and their batteries' SoCs go from 50% to 65% and 30% to 90%, respectively (Scenario 3, Figure 10b,c). Most of the vehicles come for charging at night due to the normal or low electricity price which could be used in rush hours under the V2G scheme, e.g., during t = 4–7 h, Toyota Prius plug-in, Honda Accord Hybrid and Renault Kangoo Z.E vehicles are charged from the AC bus. A total of 60 kW power is utilized to charge all these three vehicles. Among 60 kW, the RESs contribute 38 kW, while the grid provides 22 kW.

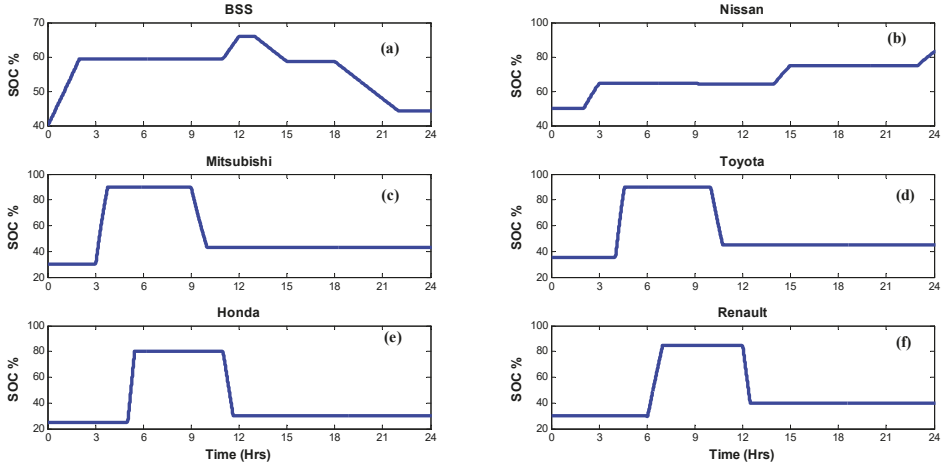

Figure 10. State of charge of the BSS and PHEVs.

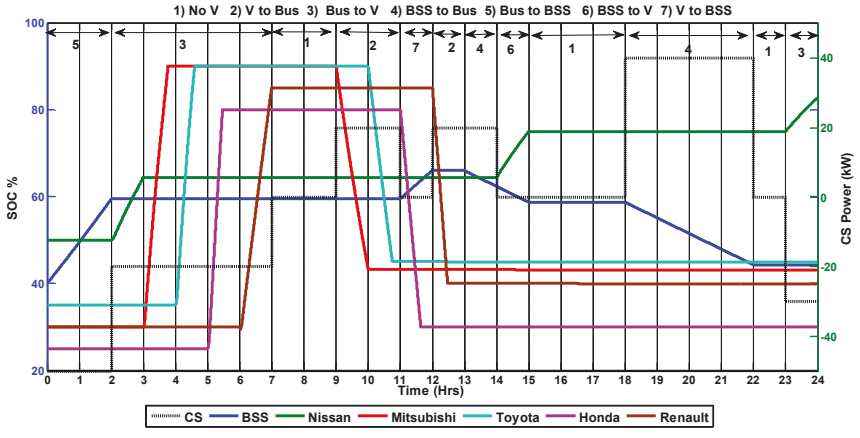

Figure 11. SOC of the BSS/PHEVs and CS power using the proposed PMS.

The charging station demand is zero during t = 7–9 h (Scenario 1), hence, both the RESs and utility grid are used to meet the residential load demand. Some of the discharged PHEVs/EVs wants to discharge under the revenue opportunity scheme during peak times. For example, during t = 9–11 h, Mitsubishi i-MiEV and Toyota Prius plug-in supply 40 kW power combined to the AC bus (Scenario 2), which is then transferred to the grid through the CS inverter, as shown in Figure 10b,c and Figure 11.

Similarly, Renault Kangoo Z.E provides 20 kW to the AC bus during t = 12–13 h, which is completely transferred to the utility grid because the RESs satisfy the residential load, as shown in Figure 9. During t = 13–14 h, the residential demand increases and needs 5 kW. According to the PMS, the required power is provided from the BSS. A total of 20 kW is transferred from the BSS to the AC bus and thus the SoC decreases from 66% to 62% (Scenario 5). Out of 20 kW, the residential load utilizes 5 kW, while the remaining 15 kW is sent to the utility grid via the CS inverter and thus the total demand decreases.

Those PHEVs that want to be charged from the BSS are covered during t = 14–15 h, viz., Nissan leaf has received power from the BSS (Scenario 6) and it increases from 65% to 75%, as shown in Figure 10a,b and Figure 11. In this interval, the RESs first satisfy the residential load demand while the remaining 10 kW power is sent to the utility grid. The demand of the CS is zero during t = 15–18 h, therefore the RESs meet the residential load while the remaining excess power, i.e., 19 kW, is sent to the utility grid. Figure 9 shows that the peak hours occur during t = 18–22 h, viz., the residential load is at peak, the utility grid cannot provide the power due to the rush hours, and the RESs cannot meet the residential load; therefore, the BSS provides 160 kW power to the AC bus. The AC bus then provides 85 kW to the grid while the remaining 75 kW power is utilized to satisfy the residential load demand. Similarly, Scenarios 1 and 3 are repeated during t = 22–23 h and t = 23–24 h, respectively.

The power quality and grid stability parameters such as RMS load voltage, load frequency and net power at AC bus are shown in Figures 12 and 13. The net power on the AC bus is zero, which indicates that the overall system and grid are stable. The RMS load voltage, load frequency deviation and DC bus voltage deviation are in limits according to the IEC61000 and IEEE 519-2014 standards.

The proposed PMS based on FLC is also compared with that based on PID controllers. Figure 14 illustrates the changes in the DC bus voltage obtained by both PMSs. The simulation results show that the proposed FLC (denoted as black) has a faster response, smaller overshoot and maintains better DC bus voltage compared to the standard PID controller (denoted as red).

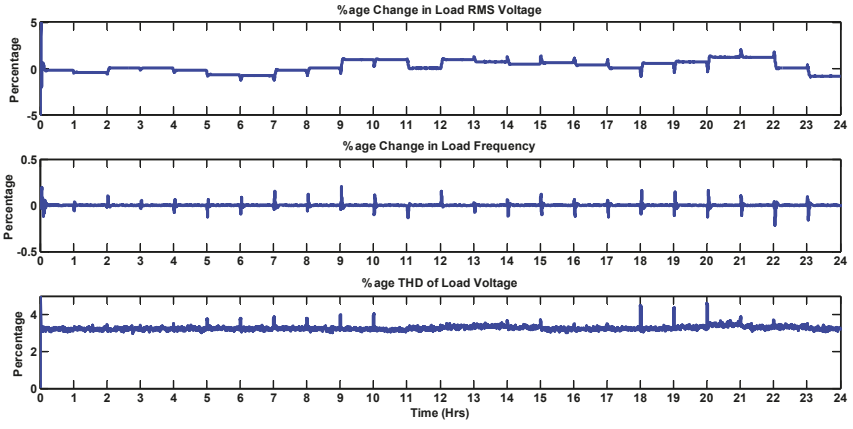

Figure 12. Power quality parameters.

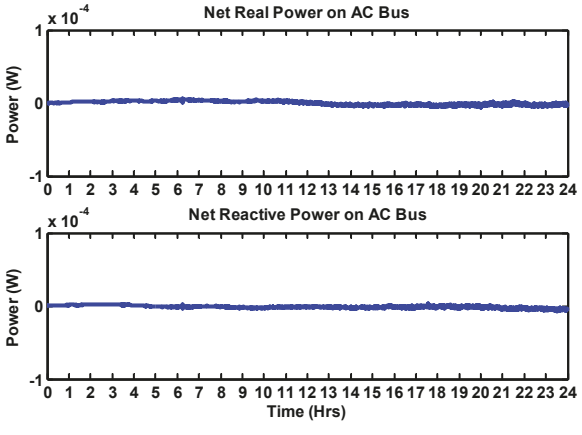

Figure 13. Grid stability parameters.

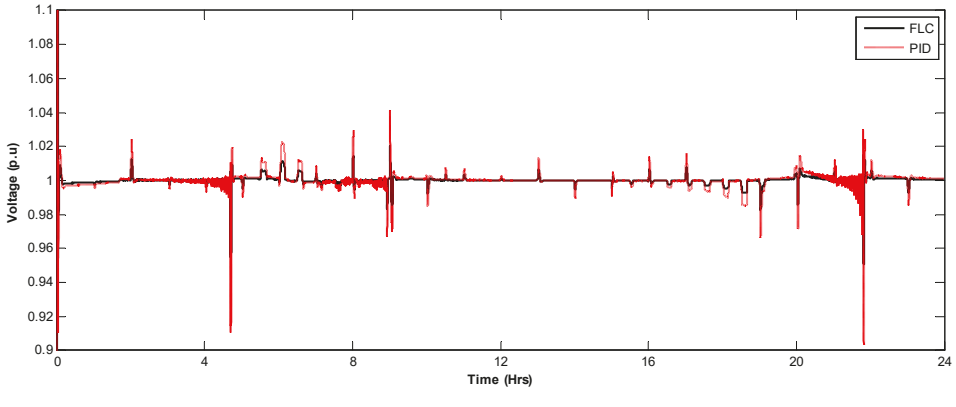

Figure 14. DC bus voltage deviation: PMS based on FLC versus PMS based on PID controllers.

7. Conclusions

Without proper management, the penetration of PHEVs in the transportation sector can cause a burden on the distribution systems, especially when many PHEVs are connected to the grid at peak-hours. To face this concern, the distribution system requires to be improved to carry new loads. The enhancement of conventional grids to smart grids will create a proper management system to control the PHEVs charging and avoid the distribution transformer from being overloaded. To further increase the benefits of PEHVs, it is essential to take power from the RESs for the PHEVs charging. This paper proposes a PHEVs/EVs CS structure using a high share of power from the RESs and proper power management strategies. The proposed PMS managed the PHEVs charging in such a way that their charging does not become a burden on the utility during peak hours. The paper also provides the integration and coordination of different RESs. This paper shows that the PHEV charging demand does not disturb the grid stability and power quality parameters of the proposed system.

Author Contributions: T.K., and L.K. designed the algorithm in this work. S.Z.H., M.H.R., M.T.R. and M.A.K. were responsible for the preparation of required material. M.K. and L.M.F.-R. analyzed the results. All authors contributed at different stages.

Funding: This work was partially funded by the Turkish government under "Türkiye Bursları 2015–2020".

Acknowledgments: Thanks to University of Cadiz, Spain for providing technical support under the framework of the Erasmus program of the European Commission.

Conflicts of Interest: The authors declare no conflict of interest.

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A Variable Speed Pumped Storage System Based on Droop-Fed Vector Control Strategy for Grid Frequency and AC-Bus Voltage Stability

Girmaw Teshager Bitew [1,*], Minxiao Han [1], Sifrash Amogne Mekonnen [2] and Patrobers Simiyu [1]

[1] State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, School of Electrical and Electronics Engineering, North China Electric Power University, Beijing 102206, China; hanminxiao@ncepu.edu.cn (M.H.); simiyupr@yahoo.com (P.S.)

[2] Social Science and Humanity College, Debre Markos University, Debre Markos 269, Ethiopia; gbitew1983@yahoo.com (S.A.M.)

* Correspondence: 1154300005@ncepu.edu.cn; Tel.: +86-155-1026-0077

Received: 7 May 2018; Accepted: 3 July 2018; Published: 7 July 2018

Abstract: Harnessing wind energy is the most rapidly growing amongst renewable energy sources. However, because of its intermittency in nature, wind power results in unfavorable influences on power system control, operation and stability. The voltage sag and flicker and grid frequency fluctuation are significant in this regard. To minimize the effect of wind power fluctuations and other contingencies on the grid frequency and AC-bus voltage, this paper presents a droop-fed vector control strategy based variable speed pumped storage (VSPS) system comprising the doubly fed induction machine. Modelling of the system is undertaken based on a phasor model technique. The case study is made by considering the droop-controlled VSPS plant in a grid containing conventional synchronous machines for hydropower and thermal power plants and an induction machine wind farm. The performance is validated and analyzed using a MATLAB/Simulink platform. The proposed droop-fed control model is compared with the conventional control strategy (without being droop-fed) and tested to wind power fluctuations, start-up transients, load variations and three-phase fault. The results show that the droop-fed vector control strategy of the VSPS plant achieves better dynamic and steady state controlling responses for grid frequency and AC-bus voltage in the power system than the conventional vector control scheme during wind power fluctuations and contingencies.

Keywords: variable speed pumped storage system; droop control; vector control; phasor model technique

1. Introduction

Due to increasing environmental concerns and energy markets, wind power generation has undergone rapid growth. In 2013, the world wind power production capacity was 318 GW and is forecasted to reach 712 GW, 1480 GW, 2089 GW and 2672 GW by 2020, 2030, 2040, and 2050, respectively, in a moderate scenario. China records the fastest growth in this regard [1,2].

Wind energy production is eco-friendly, sustainable, space efficient, incredible domestic potential, has low operational cost, revitalizing to rural economies, etc. However, the major drawback of wind power is its intermittency in nature over time, hence, significant wind power fluctuations can be observed. For a power system even with moderate wind power penetration, the fluctuations should be mitigated, otherwise this may lead to substantial deviations in the grid frequency [3], voltage sag and flicker at the grid buses [4], steady state voltage deviation, even equipment damage and system collapse at large. A study in [5] shows that the variable speed pumped storage (VSPS) system can improve the steady state operations and dynamic stability of the power system. Having dependable

features, the VSPS plant can play a key role in stabilizing the dynamics and transients of the grid affected by wind power fluctuations and other contingencies [6–11].

So far, many works have been done on the control strategies doubly fed induction machine in doubly fed induction machine (DFIM) based applications. Vector control strategy is predominantly taken into account in this regard. According to the references [8,9,12–16], the very common applicable vector control strategies implemented in DFIM are field oriented control (FOC) and direct torque control (DTC).

Based on the concept of the DTC, the direct power control (DPC) strategy is adopted. DPC is applied in an electrical machine field and has been widely studied. In DPC, the control of the real and reactive instantaneous power is independent, direct and simple [17,18]. It is noted that DPC has noble features than FOC particularly in the variable speed application [13,16,19]. Moreover, a comparative study between DPC and FOC strategies for doubly fed induction generator (DFIG) has been conducted in [19] and attempts to assure having lower computational complexity and machine model dependency, direct controllability of active and reactive powers, very good transitory response and lower overall implementation complexity than FOC. DPC is also characterized by its fast dynamic response against parameter variations and it does not utilize a rotor current control loops. In the DPC strategy, the estimations of active and reactive powers are carried out using current measurements, and directly controlled with hysteresis controllers and a switching table [12,14].

On the other hand, DPC has drawbacks compared to the FOC strategy. It has high ripples of active and reactive powers, high switching frequency which presents a high harmonic distortion of the generated currents, and provides warming-up of the silicon switchers [16]. Based on the comparative study in [16], it is hardly to state on the superiority of DPC versus FOC owing to the balance of the merits of them.

Regardless of its types, DPC or FOC, vector control confirms the higher level performance improvements in grid frequency and AC-bus voltage regulation with the implementation of the phasor model technique. However, the study of vector control in DFIM based VSPS application with the implementation of the phasor model technique is limited. The frequency regulator based on DPC implemented in a full-size converter fed synchronous machine was, for example, conducted in [8], but DFIM would be better advantages than synchronous machine in the implementation of VSPS plant for its efficiency and control [20]. The reference [13] also attempts to explore DPC in DFIG based wind power system. The DPC in [11] was also studied for the application of DFIM-based VSPS system with emphasis on converter topology study. Implementing an H-bridge cascaded multilevel converter for VSPS based on a stator voltage FOC strategy has been presented in [9] for suppressing the effect of a wind farm power fluctuations. Moreover, power filtering algorithm solution control approach was proposed in [3] to regulate the deviations of the grid frequency caused by wind power fluctuations. DPC is also studied in [11–16,19] and FOC is in [16,19] as well. The aforementioned works have not considered the phasor model simulation technique as significantly important in the large power system stability and control analysis where simulation time and computational storage are very critical. Since the electromagnetic transients are not of interest, the dynamic simulation time is highly reduced in the phasor model technique because the sinusoidal voltages and currents are replaced with phasors expressed in polar form. Implementing a phasor model in any linear system is also an advantage in that since the studies of a small-signal stability are based on eigenvalue analysis of the linearized power system, the eigenvalue analysis is complemented with dynamic simulations of the non-linear system [21,22]. Nevertheless, when implementing a phasor model technique in the DFIM application, grid frequency controlling is challenging. In the phasor model technique, the grid frequency is fixed to a constant value. It is difficult to develop a phasor locked loop which is used to synthesize the frequency. Thus, the grid frequency control is made through the active power control strategy which is an open loop control scheme for the frequency as shown in Figure 1. As a result, the responses in the grid frequency lack dynamic performances especially during contingencies [23].

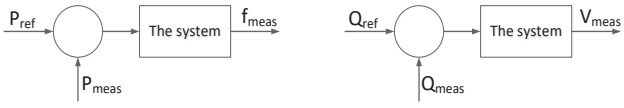


Figure 1. Open-loop frequency and AC-bus voltage control through the power control strategy.

On the other hand, the frequency has a droop characteristic with active power in the converter system. Due to the imposed frequency droop, the converter will respond to the decrement of the frequency by increasing the inverted power or by reducing the rectified power. So, the frequency droop is estimated per unit increment of rectified power to be fed to the closed control system. Since a change in the converter power results in a change in DC voltage level, a frequency decrement will be manifested as decrement in DC voltage level in an AC/DC interface system which in turn results in demanding a power flow compensation [24]. Therefore, this problem can be resolved by incorporating a synchronous machine in the power grid system helping to get the measured and estimated frequency to the VSPS control system since the rotor speed of the synchronous machine is the same as the grid frequency with a proportion factor.

Regarding voltage regulation, the AC voltage can be controlled either by reactive power control or constant voltage control. Considering the reactive power PI control, the steady state deviation of AC voltage can be observed. For a constant voltage control strategy, generating or absorbing reactive power by the VSC converter is distorted during disturbances, hence leading to significant voltage sag and flicker and steady state voltage magnitude deviations. Therefore, combining these strategies together provides droop based power control resulting in fast dynamic control response and minimized error in steady state values. Therefore, droop controllers are to be incorporated as the input of reactive power PI control (outer loop controller) of the conventional vector control strategy.

Hence, this paper presents a droop-fed vector control strategy based VSPS system for the reduction of wind power fluctuation and other contingencies impact on grid frequency and AC-bus voltage to resolve the steady state and dynamic performance problems stated in the aforementioned papers. The converter employed is the three-level neutral point clamped voltage sourced converter (NPC-VSC). Due to its novel features to the VSPS plant, the DFIM is deployed. To validate the performance of the proposed system, a phasor model simulation technique is developed and analyzed in a MATLAB/Simulink platform. The performances of the proposed system are made by comparison with the conventional method. The VSPS grid connected system consisting of hydropower and thermal power with synchronous machine and wind farm with induction generator is presented for a case study. The results show that the proposed VSPS control strategy achieves better performances in the dynamic and steady state responses of the grid frequency and AC voltage than the conventional strategy.

2. Materials and Methods

2.1. Basic Concepts of Droop Vector Control System

2.1.1. The Vector Control

Vector control is strictly defined as a variable frequency drive control method in which the stator currents of a three-phase AC electric motor are identified as two orthogonal components that can be visualized with a vector [25]. One of the two components states the torque and the other magnetic flux of the machine. From the flux and torque references, the drive control system calculates the corresponding current component references. To keep the measured current components at their reference values, typically PI controllers are used. A single-variable scalar (V/f) control will be universally displaced by the vector control strategy due to increase of the microprocessors vector control computational power. It is applicable to both induction and synchronous machines.

The very common applicable control strategies named FOC and DTC are categorized under vector control scheme [8,16]. They are different on the operation principle but their objectives are the same. Both of them aim to control effectively the machine torque and flux, and have been successfully implemented [16]. The FOC controllers move the stator field so that it is perpendicular to the rotating rotor field. The FOC is an attractive control method but it also has a drawback. The precise knowledge of the motor parameters are, for example, mandatory. It is particularly difficult to measure precisely with a varying temperature. The DTC, which is a more robust control scheme, provides for estimating the stator flux and electric torque of the machine from terminal measurements in the stationary reference frame. The DPC strategy adopted based DTC was initially developed in 1998 [26] and implemented to DFIG in 2006 [12]. A DPC is characterized by its fast dynamic response against parameter variations and it does not utilize a rotor current control loops. The DPC also has drawbacks with high ripples of active and reactive powers, high switching frequency of which presents a high harmonic distortion of the generated currents, and provides warming-up of the silicon switchers [16].

2.1.2. The Droop Control

The main concept of droop control is to build an additional VSC-DC link frequency and AC voltage control on top of the state-of-the-art frequency and AC voltage control approach to provide virtual reserve through VSC-DC link systems. In case of the power change due to load or supply variation, the droop characteristics of grid frequency and AC voltage is observed in the VSC-DC link based system performance as is strongly related to change of power.

The frequency control structure given in Figure 2 provides a governor like droop behavior through active power loop. If there are generating units in the power system, the load sharing is determined by the frequency droop of each power generating unit, which is defined as R = $\Delta\omega/\Delta$P. For two power generating units with frequency droops R_1 and R_2, the following relationship is established for the power output ΔP_1 and ΔP_2:

$$\frac{\Delta P_1}{\Delta P_2} = \frac{R_2}{R_1} \tag{1}$$

The power generating unit with smaller frequency droop shares more loads in the power system. Accordingly, the frequency droop of the VSC-DC link with the proposed frequency controller can be expressed as

$$\Delta f = \frac{1}{K_f}(\mathrm{P}_{ref} - \mathrm{P}) \tag{2}$$

where K_f is the droop constant.

Likewise, if two or more alternating-voltage-controlling units are connected to a common bus in the power system, the alternating voltage controls should be coordinated to avoid hunting between the units. The transformer used in the application of VSC is to transform the grid or load bus voltage to a suitable voltage. Nevertheless, the VSC-based system performance is affected due to voltage droops of the transformer [27]. Thus, instead of controlling the alternating voltage of the point-of common-coupling (PCC), the VSC-DC link and the synchronous generator both control voltages between their own terminal/filter-bus voltages and the voltage of the PCC to give a droop characteristic to their alternating-voltage controls. So, the virtual inertia is provided through the reactive power or AC voltage control loop of the VSC system. Since the voltage is strongly related to the reactive power generation or absorption, its droop needs to be compensated via a reactive power control loop as shown Figure 2.

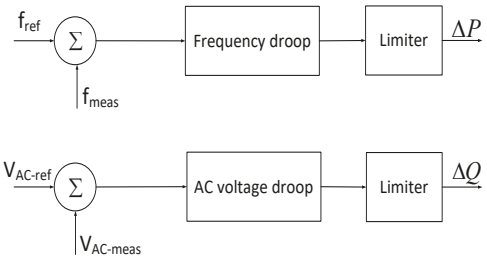


Figure 2. The block diagram of the droop control.

2.2. The Proposed System Modelling

The structure of the proposed system in this paper is illustrated in Figure 3. As shown in the figure, the DFIM of the VSPS is configured in such a way that the rotor is connected with the rotor side NPC-VSCr and the stator is connected with the grid, whereas the grid side NPC-VSCg is connected with the grid through the coupling inductor. Details are explained in [23]. The wind farm is also connected to the grid with the conventional machine. The control structure is hierarchical having inner loops (current PI controllers), outer loops (power PI controllers) and droop controllers (frequency droop controller and AC voltage droop controller).

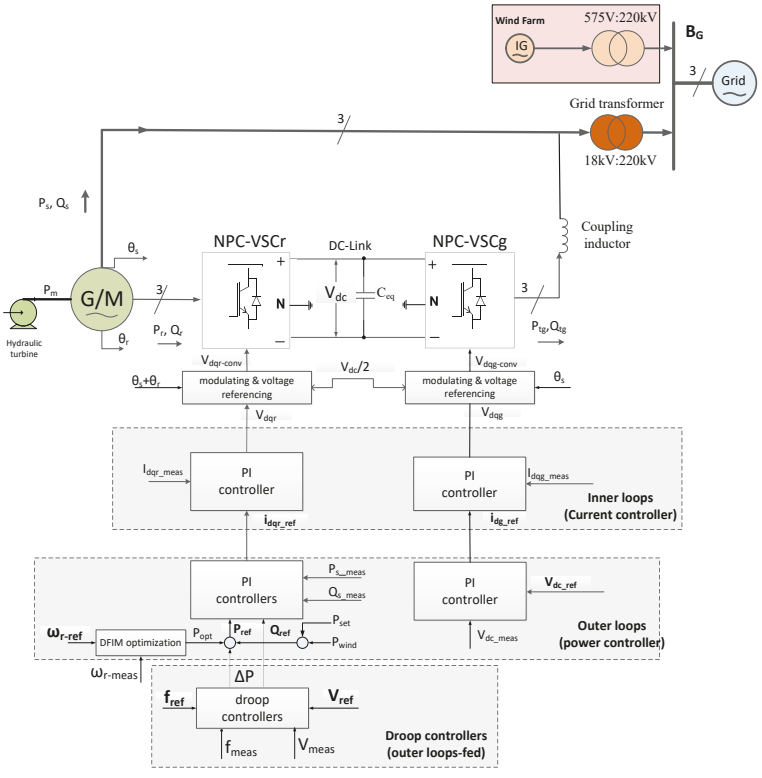


Figure 3. Structure of droop-fed vector control strategy for the NPC-VSC topology of the VSPS-wind-grid integrated system.

2.3. Machine and Converter Modelling

Detailed modelling of the hydraulic-turbine, the DFIM and the NPC-VSC is presented in [23] and the wind farm also in [15] by the same authors. This paper focuses on developing the control strategy of the VSPS in the wind-grid-integrated system for analyzing the dynamic behavior and performance of controlling the grid frequency and AC-bus voltage during the fluctuation of wind energy and other contingencies.

2.4. Control Modelling in MATLAB Platform for Dynamic and Steady State Analysis

Referring to [15,23], we have the stator power equations and the dynamics equations of the induction machine fluxes in (3) and (4) respectively.

$$\begin{aligned} P_s &= 1.5(v_{qs}i_{qs} + v_{ds}i_{ds}) \\ Q_s &= 1.5(v_{qs}i_{ds} - v_{ds}i_{qs}) \end{aligned} \tag{3}$$

$$\begin{aligned} \tfrac{d\Psi_{ds}}{dt} &= V_{ds} - R_s i_{ds} - \omega_s \Psi_{qs} \\ \tfrac{d\Psi_{qs}}{dt} &= V_{qs} - R_s i_{qs} + \omega_s \Psi_{ds} \\ \tfrac{d\Psi_{dr}}{dt} &= V_{dr} - R_r i_{dr} + (\omega_s - \omega_r)\Psi_{qr} \\ \tfrac{d\Psi_{qr}}{dt} &= V_{qr} - R_r i_{qr} - (\omega_s - \omega_r)\Psi_{dr} \end{aligned} \tag{4}$$

Based on the detail works in [23], from (3) and (4), the stator power (P_s, Q_s) is determined and expressed as a function of the rotor dq-axis current.

$$\begin{aligned} P_s &= 1.5V_s(L_m/L_s)i_{qr} \\ Q_s &= 1.5V_s[(\Psi_s/L_s) - (L_m/L_s)i_{dr}] \end{aligned} \tag{5}$$

Equation in (5) implies the independent control of the real power and reactive power in the application of a DFIM-based VSPS system, and equations in (6) have been also derived based on the assumptions taken; a voltage drop across stator resistor being very small compared to the grid voltage and a magnitude of stator flux fairly constant.

$$\begin{aligned} V_{qr} &= R_r i_{qr} + L_r^* \tfrac{di_{qr}}{dt} + (\omega_s - \omega_r)(L_r i_{dr} + L_m i_{ds}) \\ V_{dr} &= R_r i_{dr} + L_r^* \tfrac{di_{dr}}{dt} - (\omega_s - \omega_r)(L_r i_{qr} + L_m i_{qs}) \end{aligned} \tag{6}$$

where $L_r^* = L_r - (L_m^2/L_s)$ and V_{qr} and V_{dr} are feed-forward voltages to the controller.

Thus, the dynamics of the rotor dq-axes currents are controlled by developing the PI control loops from (6) which in turn are used to control the stator active power which is the function of rotor dq-axes current as equated in (5). However, dynamics of i_{dr} and i_{qr} are coupled due to the presence of the terms $L_r(\omega_s - \omega_r)$ in (6). Since the VSC controls the DFIM rotor terminal voltage, as stated in (6), i_{qr} and i_{dr} are to be related to the new control inputs u_{qr} and u_{dr}. To decouple the dynamics, the new control inputs are introduced and is redefined as in (7).

$$\begin{aligned} u_{qr} &= V_{qr} - (\omega_s - \omega_r)(L_r i_{dr} + L_m i_{ds}) \\ u_{dr} &= V_{dr} + (\omega_s - \omega_r)(L_r i_{qr} + L_m i_{qs}) \\ \text{where } u_{dr} &= L_r^* \tfrac{di_{dr}}{dt} + R_r i_{dr} \\ u_{qr} &= L_r^* \tfrac{di_{qr}}{dt} + R_r i_{qr} \end{aligned} \tag{7}$$

On the other hand, in the grid side of NPC-VSCg converter, the PI control of DC voltage in the DC link is deployed for regulating the proper active power exchange between the converter and the grid on the outer loop whereas PI current controller is used on the inner loop. But, reactive power

exchange is usually set to zero [28]. The mathematical model design is made by the equation in (5) denoting the voltage equations across the coupling inductor.

$$\begin{aligned} V_{dg} &= R\mathrm{i}_{dg} + L\frac{di_{dg}}{dt} - \omega_s L i_{qg} + V_{ds} \\ V_{qg} &= R\mathrm{i}_{qg} + L\frac{di_{qg}}{dt} + \omega_s L i_{dg} + V_{qs} \end{aligned} \tag{8}$$

where R and L are the coupling inductor resistance and inductance respectively; and V_{dqg} and V_{dqs} are control inputs and disturbance inputs respectively.

Similarly, i_{qg} and i_{dg} are to be related to the new control inputs u_{qg} and u_{dg} and (9) is redefined as

$$\begin{aligned} u_{dg} &= V_{dg} + \omega_s L i_{qg} - V_{ds} \\ u_{qg} &= V_{qg} - \omega_s L i_{dg} - V_{qs} \\ \text{where } u_{dg} &= L\frac{di_{dg}}{dt} + R i_{dg} \\ u_{qg} &= L\frac{di_{qg}}{dt} + R i_{qg} \end{aligned} \tag{9}$$

Thus, from (7) and (9), the rotor and grid current control loops (inner loops) are developed. Both current controllers are supported by feed forward terms predicting V_{dqr} and V_{dqg}. The dynamics of the DC voltage in the DC link is defined by (10). The converters and DC-link are assumed to be lossless.

$$\frac{dV_{dc}}{dt} = \frac{1}{C} i_{dc} = \frac{1}{CV_{dc}}(\mathrm{P}_r - \mathrm{P}_g) \tag{10}$$

where C and V_{dc} are the DC link capacitance and DC voltage respectively. P_g and P_r are active power flow in the grid and rotor side of the converters respectively.

The power equations of (3) also hold for a grid side power flow and denoted by (11).

$$\begin{aligned} P_{tg} &= 1.5(v_{qg} i_{qg} + v_{dg} i_{dg}) \\ Q_{tg} &= 1.5(v_{qg} i_{dg} - v_{dg} i_{qg}) \end{aligned} \tag{11}$$

2.5. Control of Active and Reactive Power for Rotor Side Converter

Active or reactive power is controlled by the rotor side converter which connects rotor windings and DC link. This converter offers a proper AC excitation for the windings of the rotor that provides the stator windings proper active power.

2.5.1. Active Power Control

Controlling of active power can ensure controlling of system frequency. So as to keep the grid frequency constant, synchronous generators, for example, can have a permanent droop control loop in the turbine control. It is dedicated to adjust the active power balance between the production and the consumption of the system. On the other hand, implementing the primary frequency control in the DFIM-based VSPS unit, which is critically important, controls the active power flow of the system. In this application, a vector control strategy is employed to have fast dynamic response and lets the control system compensate effectively during contingencies. Even if this is a limited control scheme that is placed in the VSPS unit, the significant output that is an adjustable and nearly constant power flow can be seen from the network of the power system as far as the VSPS operates within the specified limits. The power command P_{opt} of the control system of the VSPS is determined from the capacity of the VSPS unit and its efficiency. An external set point, P_{set} which is the input to the power control system, in this regard, should be assumed for the VSPS. The set point depends on the VSPS capacity and the situation of the power grid. The value of this set point is dedicated to optimize the system energy balance and update relatively with slow rate. The main concern is, however, to control the contingencies and regulate the VSPS power for mitigating the impact on the grid stability.

As illustrated in Figure 3, the rotor-side converter control is modelled in two stages. The first stage is power (PQ) control (the outer loop) in that the active/reactive power tracks the respective reference. This loop provides dq-axis reference currents for the second stage (the inner loop). The inner loop is technically a current control offering dq-axis reference voltage for modulation and injected to the converter. PI controllers with limiters are applied in both control stages.

The model design of the active power control of the rotor side converter is presented as follows. Referring to the voltage equations in (4), we have the mathematical equations of (6). From (6), the rotor electrical dynamics model is determined based on the system equations and representing two decoupled, first-order subsystems. It can control i_{dqr} by u_{dqr}, in turn, u_{dqr} can be delivered by corresponding PI compensators. The compensators process the current errors and provides u_{dqr}. The control plants in dq-axis current-control loops are identical. Therefore, the corresponding compensators can also be identical. Thus, the compensator can be a simple proportional-integral (PI) compensator, $K_i(s)$ to enable tracking of a respective reference. The compensator is defined by

$$K_i(s) = \frac{P_i s + I_i}{s} \tag{12}$$

Thus, the loop gain becomes

$$\ell(s) = \left(\frac{P_i}{L_r^*}\right)\frac{s + I_i/P_i}{s + R_r/L_r^*} \tag{13}$$

Due to the plant pole at s = $-R_r/L_r$*, which is fairly close to the origin, the magnitude and the phase of the loop gain start to drop from a relatively low frequency. Thus, the plant pole is first canceled by the compensator zero s = $-I_i/P_i$, and the loop gain assumes the form $\ell = P_i/L_r^*$. Then, based on the plant function, $G_i(s) = 1/(L_r^* s + R_r)$ developed from (7) and considering the compensator $K_i(s)$ in, the closed-loop transfer function becomes;

$$\frac{I_{dqr}(s)}{I_{dqr-ref}(s)} = G_{ic}(s) \approx \frac{1}{\tau^* s + 1} \text{ if } P_i = L_r^*/\tau^* \text{ and } I_i = R_r/\tau^* \tag{14}$$

where P_i and I_i are proportional and integral gains and $\tau^* = L_r^*/R_r$. The gains are determined and tuned based on the control stability theory. The control structure of the inner loop is illustrated in Figure 5a.

From Equation (14), the q-axis rotor current as a function of its own reference value is obtained.

$$I_{qr}(s) = G_{ic}(s) I_{qr-ref}(s) \tag{15}$$

Multiplying both sides of (15) by 1.5 VsLm/Ls, we get

$$1.5 V_s L_m / L_s I_{qr}(s) = G_{ic}(s) 1.5 V_s L_m / L_s I_{qr-ref}(s) \tag{16}$$

Therefore, based on Equation (5), from (16), we can deduce (17).

$$P_s(s) = G_p(s) P_{s-ref}(s) \tag{17}$$

From these relationship, we can have the block diagram of Figure 4.

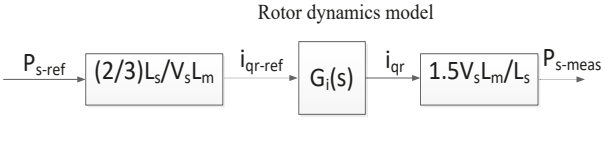


Figure 4. Control block diagram of the vector controlled DFIM for active power control loop.

Thus, plant function $G_p(s)$ is defined by multiplying $G_{ic}(s)$ with 1.5 VsLm/Ls i.e., $G_p(s) = 1.5V_sL_m/L_s(L_r^*s + R_r)$. Accordingly, the closed loop active power control is developed as shown in Figure 5b. The PI control of $K_p(s)$ of Figure 5b processes the error signal e_p and provides the reference current $i_{qr\text{-}ref}$ and defined by;

$$K_p(s) = \frac{P_ps + I_p}{s} \tag{18}$$

where P_p and I_p are proportional and integral gains. The open loop transfer function becomes;

$$G_{po}(s) = \left(K\frac{(P_ps + P_i)(I_ps + I_i)}{L_r^*s^3 + (R_r + I_p)s^2 + I_is}\right) \tag{19}$$

where K = 1.5 VsLm/Ls. We used the symmetrical optimum method to determine the control gains (P_p and I_p) since the open loop transfer function has a pole at the origin. This method optimizes the system's control behavior. Thus, the inner current loop with wider bandwidth of 2.4 Hz than the outer power loop with 1.11 Hz is designed.

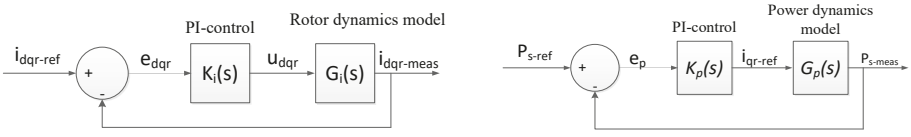


Figure 5. The PI control structure of the NPC-VSCr: (**a**) the current controller (inner loop); (**b**) the active power control (outer loop).

Permanent droop should be included in this control as active power in DFIM is controlled by the converter. In dominant wind farm power production fluctuations, the response of the power system to contingencies is highly improved if a frequency droop control scheme is included in the active power control loop. The power transfer within the DC-link can be modulated by a frequency droop control. It can be modelled as an additional signal that is added to the active power reference P_{ref} in Figure 6.

According to Figure 6, the difference between actual and reference frequency is forwarded to a proportional controller which defines permanent droop. The proportional output is added to the signal of the active power P_{set} and the optimized output power P_{opt} from the induction machine and the sum of them presents the active power reference P_{ref} for the PI active power control in the outer loop.

The optimized power P_{opt} is the very beginning reference power of the VSPS control system which is determined by considering the capacity of the hydraulic turbines of the VSPS plant along with its losses. Since the plant is a variable speed scheme, the control system enables to adjust and regulate the plant when the power variation occurs in the grid. Thus, we can add the power command $\Delta P_{wind} = P_{wind} - P_{set}$ to the VSPS power control unit and to be compensated. P_{wind} is the wind farm power measured which is subject to the fluctuation due to its intermittency. Then, it is designed for the converters to offer frequency support to the grid. This control structure provides a governor-like droop behavior through active power flow. The droop-type control is built based on the concept of power synchronization control in which grid synchronization is achieved regardless of a dedicated synchronization unit [21]. This droop-type control system provides a DC link with frequency droop characteristic. For other power generating units in the grid system, the load sharing is possible.

Hence, with the additional power command ΔP_f due to change of frequency caused by all contingencies to the VSPS active power control system, improvement of the dynamics performance of the power system can be ensured, and (20) is accordingly determined.

$$\Delta P_f = K_f(f_{ref} - f_{grid}) \tag{20}$$

where K_f is the droop constant, f_{ref} is the reference frequency in which 50 Hz applied in this paper, and f_{grid} is the grid frequency measured and estimated from the rotor speed of the synchronous machine in the same grid.

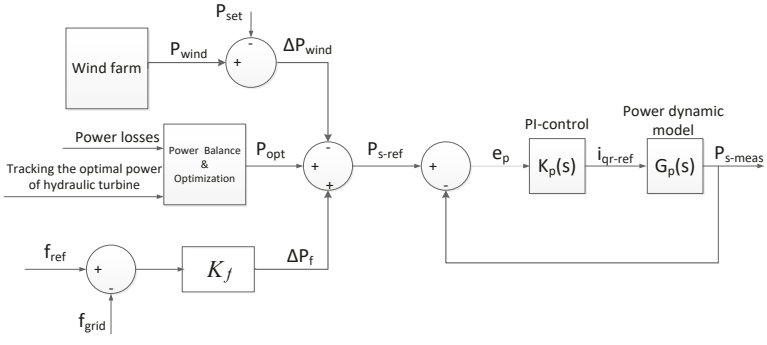


Figure 6. A rotor-side converter of active power control structure.

2.5.2. Reactive Power Control

The same procedures following as in the active power modelling section, the reactive power control system is developed. From the Equations (5), (14) and Figure 5, the model (21) is determined.

$$Q_s(s) = G_q(s)Q_{s-ref}(s) \tag{21}$$

Hence, the dynamic model for the reactive power control of rotor side converter VSC-NPCr is developed, and the PI control of $K_q(s)$ is defined in (22).

$$K_q(s) = \frac{P_q s + I_q}{s} \tag{22}$$

The rotor side converter provides the proper reactive power of stator windings as stated above. Therefore, in order to keep the AC-bus voltage constant, i.e., to adjust the generation and absorption of the reactive power in the converter, additional signal should be included to the reference reactive power. With load compensation, referring Figure 7, for parallel connected voltage control units, the magnitudes of the resulting compensated voltages can be given by

$$\begin{aligned} V_{t-SG} &= e_{SG} + k_{SG}(\mathrm{R}_{SG} + \mathrm{jX}_{SG})\mathrm{i}_{SG} \\ V_{t-vsc} &= e_{vsc} + k_{vsc}(\mathrm{R}_{vsc} + \mathrm{jX}_{vsc})\mathrm{i}_{vsc} \end{aligned} \tag{23}$$

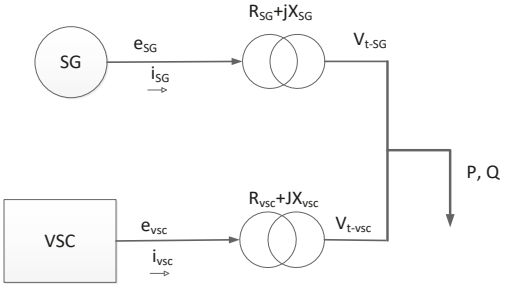


Figure 7. Voltage droop control for parallel connected voltage-control units.

In order to provide appropriate AC voltage in the network, for example, the DFIM reactive power can be properly controlled. This control can be accomplished based on the control structure presented in Figure 8. This figure indicates that the difference between actual AC voltage V_{meas} and reference AC voltage V_{ref} of the AC grid is integrated and added to the reactive power set signal Q_{set} and the sum of both signals presents the reference of the reactive power Q_{ref} for the PI reactive power control on the outer loop of the VSPS control system provided in the rotor side.

From (23), the voltage-reactive power relationship of Equation (24) with the droop constant K_{ac} is derived.

$$\Delta Q_{vsc} = K_{ac}(V_{ref} - V_{meas}) \tag{24}$$

The voltage control structure through the reactive power control loop is illustrated in Figure 8.

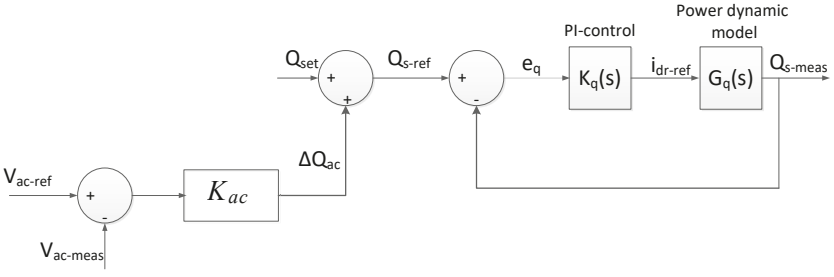


Figure 8. A rotor-side converter of reactive power control structure.

2.6. Control of Active and Reactive Power for Grid Side Converter

The reactive power on the grid side converter is controlled by a PI controller by setting its reference value zero. Whereas the proper active power exchange between the converter and grid is controlled through the PI control of DC voltage in the DC link.

For control design purposes, the d-axis is supposed to be set in phase with the voltage across the resistor. Thus, the d-component of the voltages in d-q coordinates becomes v_{dg} and zero that of v_{qg}. So, the power equations of (11) is deduced by (25).

$$\begin{aligned} P_{tg} &= 1.5 v_{dg} i_{dg} \\ Q_{tg} &= -1.5 v_{dg} i_{qg} \end{aligned} \tag{25}$$

Ignoring the losses and harmonics due to switching in the converter, the real power balance equation on the grid side can be given by:

$$P_{tg} = 1.5 v_{dg} i_{dg} = V_{dc} I_{dc} \tag{26}$$

Equation (26) implies that the DC-bus voltage is likely and independently controlled by controlling the d-axis current i_{dg}.

The objective of the active/reactive power controller of the VSC system is to regulate the active/reactive power exchange between the converter and the AC grid. In this controller, for the sake of mathematical formulation, it is supposed to be the DC side of the VSC is connected to an ideal DC voltage source that dictates the DC-bus voltage as shown in Figure 9.

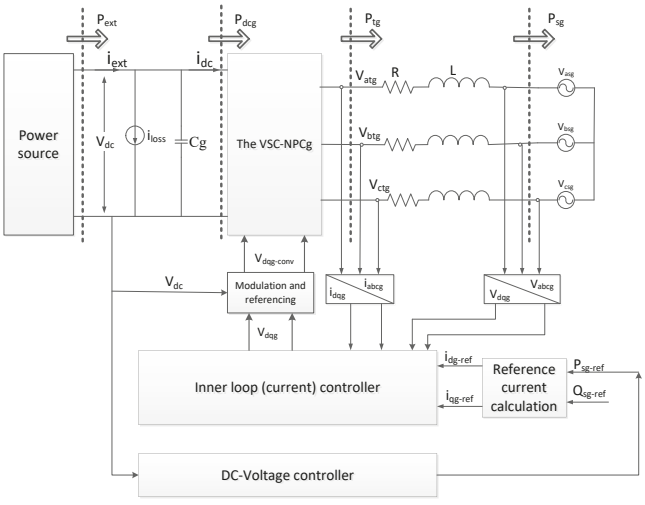


Figure 9. Simplified schematic diagram of the controlled DC-voltage power port of a three-level NPC-VSCg.

According to Figure 9, any power imbalance within the outlined area results in excursions (and potential instability) of the DC-bus voltage since there is no DC voltage source in the VSC system. Thus, the DC-voltage V_{dc} of the grid port requires proper regulation. $P_{ext}(t)$ cannot be controlled by the VSC system since it is typically an exogenous signal. Thus, to ensure the power balance exchange, P_{dcg} must be controlled through the VSC system. Based on Figure 9, the power balance is expressed by (27).

$$P_{ext} - V_{dc}i_{loss} - \frac{d}{dt}(\frac{1}{2}C_g V_{dc}^2) = P_{dcg} = V_{dc}i_{dc} \tag{27}$$

However, for a three-level NPC-VSC, the DC bus effective capacitance is half each of its DC-side capacitors. Ignoring the power losses related to the IGBT resistance r_{on} and substituting for $P_{dcg} = P_{tg}$ and rearranging the resultant, (27) is rewritten as (28).

$$P_{ext} - \underbrace{V_{dc}i_{loss}}_{P_{loss}} - \frac{d}{dt}(\frac{1}{2}C_g V_{dc}^2) = P_{tg} \tag{28}$$

where P_{tg} is the power at the AC-side terminal of the VSC. Equation (28) represents a power balance and describes a dynamic behavior of V_{dc} of a system in which V_{dc}^2 is the output state variable, the P_{tg} is the control input, and P_{ext} and P_{loss} are the exogenous inputs. C_g is the capacitance for smoothing the DC-bus voltage ripples.

Similarly, taking into account the system on the rotor side converter encompassing C_r, the following equation holds.

$$\frac{d}{dt}(\frac{1}{2}C_r V_{dc}^2) = P_{dcr} - \underbrace{V_{dc}i_{lossr}}_{P_{lossr}} - P_{ext} \tag{29}$$

Ignoring the power losses related to the IGBT resistance r_{on}, AC-side terminal power is equal to the machine rotor power $P_r = P_{dcr}$. Adding (28) and (29) together, the Equation (30) is found.

$$\frac{d}{dt}(\frac{1}{2}C_{eq} V_{dc}^2) = -P_{tg} - P_{loss} + P_{dcr} \tag{30}$$

Equation (30) describes a power-balance dynamic equation for the capacitance $C_{eq} = C_r + C_g$, which is subjected to the (relatively small) discharging power $P_{loss} = V_{dc}$ ($i_{lossr} + i_{lossg}$) the (widely variable) charging power P_{dcr}, and the (controllable) discharging power P_{tg}.

Starting with the voltage equation across the coupling inductor from Figure 6, we have

$$L\frac{di}{dt} = -Ri + V_{tg} - V_{sg} \tag{31}$$

The control input P_{tg} is expressed in terms of P_{sg} and Q_{sg} since the VSC system of Figure 9 enables to control P_{sg} and Q_{sg}. Multiplying both sides of (31) by $(3/2)i^*$ (i^* is the conjugate of i), we obtain

$$\frac{3L}{2}\mathrm{Re}\{\frac{di}{dt}i^*\} = -\frac{3}{2}R\hat{i}^2 + \frac{3}{2}\mathrm{Re}\{V_{tg}i^*\} - \frac{3}{2}\mathrm{Re}\{V_{sg}i^*\} \tag{32}$$

Rearranging and solving (30) for $P_{tg} = (3/2)\mathrm{Re}\{V_{tg}i^*\}$ and $P_{sg} = (3/2)\mathrm{Re}\{V_{sg}i^*\}$, we get

$$P_{tg} = P_{sg} + \frac{3}{2}R\hat{i}^2 + \frac{3L}{2}\mathrm{Re}\{\frac{di}{dt}i^*\} \text{ or } P_{tg} = P_{sg} + \frac{3}{2}R\hat{i}^2 + \frac{3L}{4}\frac{d\hat{i}^2}{dt} \tag{33}$$

Practically, R is a small resistance and its absorbed power is negligible compared to P_{tg} and P_{sg}. However, during transients, the power absorbed by the coupling inductor can be significant. So, L must be adequately large to suppress the switching harmonics. Furthermore, since the current controllers in dq-axis frame are fast, i can undergo rapid phase and amplitude changes, during the real/reactive-power command tracking process.

From the power equation, we have

$$P_{sg} + jQ_{sg} = \frac{3}{2}(V_{sg}i^*) \text{ or } P_{sg}^2 + Q_{sg}^2 = \frac{9}{4}\hat{V}_{sg}^2\hat{i}^2 \tag{34}$$

Solving (34) for $\hat{i}^2$ and substituting in (33), Equation (35) is derived

$$P_{tg} \approx P_{sg} + \left(\frac{2L}{3\hat{V}_{sg}^2}\right)P_{sg}\frac{dP_{sg}}{dt} + \left(\frac{2L}{3\hat{V}_{sg}^2}\right)Q_{sg}\frac{dQ_{sg}}{dt} \tag{35}$$

Substituting (35) in (30), Equation (36) holds.

$$\frac{dV_{dc}^2}{dt} = \frac{2}{C_{eq}}\left[-P_{loss} + P_{dcr} - P_{sg} - \left(\left(\frac{2L}{3\hat{V}_{sg}^2}\right)P_{sg}\frac{dP_{sg}}{dt} + \left(\frac{2L}{3\hat{V}_{sg}^2}\right)Q_{sg}\frac{dQ_{sg}}{dt}\right)\right] \tag{36}$$

Equation (36) describes the dynamics of V_{dc}^2; P_{sg} is the control input, Q_{sg} are the disturbance inputs. Thus, to control V_{dc}^2, one can form the control scheme shown in Figure 8, which consists of an inner control loop nested inside an outer loop. The outer loop compares V_{dc}^2 with its reference value, processes the error by a compensator, and delivers $P_{sg\text{-}ref}$ to the inner control loop. The inner control loop is basically the current controller which regulates its reference value calculated from the $P_{sg\text{-}ref}$ of the outer loop controller.

Since the control plant is nonlinear, Equation (36) should be linearized about the steady state real power flow operating points based on [29], and thus, designing $G_{dc}(s)$ accordingly. So, $P_{sg0} = P_{ext} - P_{loss} \approx P_{ext0}$; and (36) is linearized as

$$\frac{d\tilde{V}_{dc}^2}{dt} = \frac{2}{C_{eq}}\left[-\tilde{P}_{ext} - \tilde{P}_{sg} - \left\{\left(\frac{2L}{3\hat{V}_{sg}^2}\right)P_{sg0}\frac{d\tilde{P}_{sg}}{dt} + \left(\frac{2L}{3\hat{V}_{sg}^2}\right)Q_{sg0}\frac{d\tilde{Q}_{sg}}{dt}\right\}\right] \tag{37}$$

where ~denotes small-signal perturbations. The time domain of (37) is transformed into Laplace domain resulting in a control plant transfer function as

$$G_{dc}(s) = \frac{\widetilde{V}_{dc}^2}{\widetilde{P}_{sg}} = -\left(\frac{2}{C_{eq}}\right)\frac{\tau s + 1}{s} \tag{38}$$

where τ is the time constant defined by

$$\tau = \frac{2LP_{sgo}}{3\hat{V}_{sg}^2} \tag{39}$$

where L, P_{sg0} and $\hat{V}_{sg}$ are respectively the coupling inductance, (steady-state) real power flow and grid-side AC voltage magnitude.

As per Equation (39), if P_{ext0} is small, τ is insignificant and the plant is predominantly an integrator since τ is proportional to the real-power flow P_{ext0} (or P_{sg0}). τ brings a phase shift in $G_{dc}(s)$ when P_{ext0} increases. In the inverting operation mode where P_{ext0} is positive, τ is positive and adds to the phase of $G_{dc}(s)$. However, in the rectifying operation mode where P_{ext0} is negative, τ is negative and reduces the phase of $G_{dc}(s)$; a larger absolute value of P_{ext0} results in a smaller phase of $G_{dc}(s)$. Based on (38), the plant zero is $z = -1/\tau$. Therefore, a negative τ corresponds to a zero on the right-half plane, and the controlled DC-voltage VSPS represents a non-minimum-phase system in the rectifying operation mode. Thus, the phase reduction associated with the non-minimum-phase zero has a detrimental impact on the closed-loop stability.

Taking into account of system model linearization, the PI controller parameters are chosen around the operating points. For the model linearization, the point of a reference is obtained by specifying a reference input V_{dc-ref}. The control structure is depicted in Figure 10a.

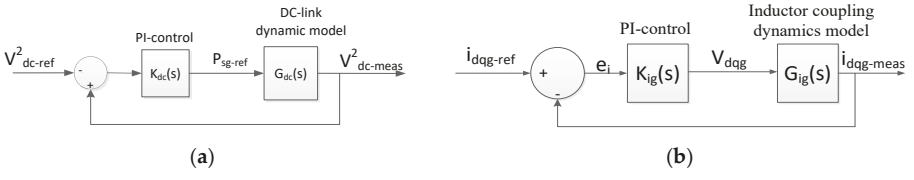


Figure 10. The control structure for grid side converter of NPC-VSC: (**a**) the DC-bus voltage control (outer loop) structure; (**b**) the current control (inner loop) structure.

The compensator $K_{dc}(s)$ is designed to guarantee an adequate stability margin even if the steady state operating point changes. It is designed based on the plant function of (36) in which V_{dc}^2 is impacted by P_{ext} and P_{loss} under the steady state and transient conditions. The feed-forward compensation can reduce the impact of P_{ext}. However, the feed-forward compensation is hardly effective to mitigate the impact of P_{loss} due to uncertainty of the measurement and estimation of P_{loss}. Therefore, $K_{dc}(s)$ must have an integral term (I_{dc}) to eliminate the steady state error of V_{dc}^2 caused by P_{loss}. Because of a presence of an integral term in the control plant and to ensure an adequate phase margin and stability, a proportional term (P_{dc}) must be included in the $K_{dc}(s)$. Hence, the PI compensation $K_{dc}(s)$ of Figure 9a is defined by (40).

$$K_{dc}(s) = \frac{P_{dc}s + I_{dc}}{s} \tag{40}$$

where P_{dc} and I_{dc} are respectively proportional and integral constants of the PI controller.

The control of the inner loops in the grid side converter is designed based on the voltage dynamics equation of (8) by following the same procedure as of the rotor side. The inner loop current controllers which are identical due to identical dynamic model are dedicated to control both active and reactive

power i_{dg} for active power and i_{qg} for reactive power. Hence, PI control structure of the inner loops shown in Figure 10b is developed.

The PI controller compensation $K_{ig}(s)$ and the inductor coupling dynamic model $G_{ig}(s)$ of Figure 9b are derived and given by (41) and (42) respectively.

$$K_{ig}(s) = \frac{P_{ig}s + I_{ig}}{s} \tag{41}$$

$$G_{ig}(s) = \frac{1}{\tau s + 1}; \tau = L/R \tag{42}$$

where P_{ig}, I_{ig}; L and R respectively proportional and integral constants; inductance and resistance of the coupling inductor.

2.7. Measuring and Estimation of the Grid Frequency

The grid frequency can be detected or measured through a phase-locked loop (PLL) which is a nonlinear feedback system that generates an output signal whose phase is related to the phase of an input signal. A basic advantage of PLL is to synthesize the grid frequency in a power system.

In a phasor model, however, the PLL is ignored. In this method, the sinusoidal voltages and currents are replaced by phasor quantities (complex numbers) at the system nominal frequency (50 Hz). As a result, measuring of a frequency for controlling is, in a phasor model technique, critically challenging. As stated above, frequency is regulated in an open loop way through the active power control system and, in turn. the dynamic stability of the frequency during contingencies is not ensured. Therefore, a method to synthesize the frequency is proposed in this paper and presented as follows.

In the basic operation principle of a synchronous machine, the rotating magnetic field of the stator is synchronously moving with the speed of the rotor. The frequency of the power system in which the synchronous machine connected to is the number of cycles per second in an alternating current sine wave of the rotating magnetic field of the stator. Its value is practically 50 Hz or 60 Hz. The frequency and the rotor speed are linearly related in the synchronous machine. It is given as

$$f = \frac{p}{120}n \tag{43}$$

where f, p and n are respectively electrical frequency in Hz, number of poles and rotor speed of the machine in rpm

From (43), it is deduced that the per-unit (pu) values of the frequency and rotor speed are equal, i.e., $f_{pu} = n_{pu}$. Thus, taking the pu values of the rotor speed as the pu values of the frequency is practically acceptable. Therefore, the rotor speed is measured and estimated from the synchronous machine and synthesized into the input of the frequency droop controller of the VSPS plant which contains the doubly fed induction machine.

2.8. Voltage Modulation and Converter Reference Voltage

The self-commutated VSC converter is a fast and controllable converter for AC/DC interface applications. One type of VSC converters is a three-level NPC power converter which contains three arms with each four switching components with antiparallel diodes and two NPC diodes. Since this paper is engaged to validate the performance of the proposed system in accordance with the phasor model technique, the following assumptions are taken: the power losses in the converters are neglected and the switching dynamics can be also neglected because the frequency of a pulse width modulation in NPC-VSC is much greater than the frequency of the grid [30]. Hence, modulated and converter reference voltages of the VSCs in this paper are denoted by the equivalent phasor model equations and obtained accordingly.

The modulated voltages of the rotor-side converter are given in (44).

$$m_{dqr} = \left| (2/\mathrm{V}_{dc})\mathrm{V}_{dqr-ref} * V_{nom}\sqrt{2/3} \right| \tag{44}$$

where V_{dqr_ref}* is the feed-forward voltage in pu value and V_{nom} is the RMS nominal voltage of the VSPS plant. The converter control voltage is defined by

$$V_{dqr-cont} = \left|m_{dqr}\right|\angle(\theta_s + \theta_r + \angle V_{dqr}) \tag{45}$$

where $\angle V_{dqr}$ is an angle obtained from the feed forward voltages.

Similarly, for grid side converter, the modulated and the converter control voltages are obtained and given by the following equations.

$$\begin{aligned} m_{dqg} &= \left|(2/V_{dc})V_{dqg-ref} * V_{nom}\sqrt{2/3}\right| \\ V_{dqr-cont} &= \left|m_{dqg}\right|\angle(\theta_s + \angle V_{dqg}) \end{aligned} \tag{46}$$

where V_{dqg_ref}* is the feed-forward voltage in pu value and $\angle V_{dqg}$ is an angle obtained from the feed forward voltages.

Since the converters reference voltage should be fed in actual value, they are determined by

$$\begin{aligned} V_{dqr-conv} &= (1/2)\sqrt{3/2}(V_{dc}/V_{nom})V_{dqr-cont} \\ V_{dqg-conv} &= (1/2)\sqrt{3/2}(V_{dc}/V_{nom})V_{dqg-cont} \end{aligned} \tag{47}$$

where $V_{dqr\text{-}conv}$ and $V_{dqg\text{-}conv}$ are rotor side and grid side converter reference voltages respectively.

2.9. Case Study and Simulation Model

In this paper, a case-study is undertaken involving a 300 MW DFIM-based VSPS and a power grid system integrated with a wind-farm comprising of seven identical 15 MW wind turbine induction generators. To investigate the impact of wind fluctuations on the grid frequency, a medium power system model consisting of two 200 MVA hydropower plants and one 15 MVA diesel power unit with conventional synchronous generators is established. The phasor model technique in a MATLAB/Simulink platform is applied. For the conventional synchronous machines, the primary voltage regulation method in automatic voltage regulators based on the standard IEEE type I and the primary frequency regulation in turbine governors are used. The simulation network model setup is illustrated in Figure 11 with a single-line diagram.

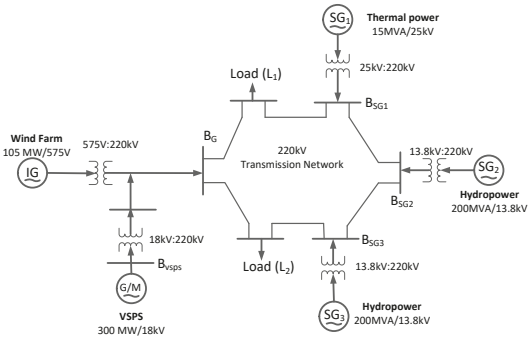


Figure 11. Single-line diagram setup of the VSPS-wind farm-grid integrated system for the case study [15].

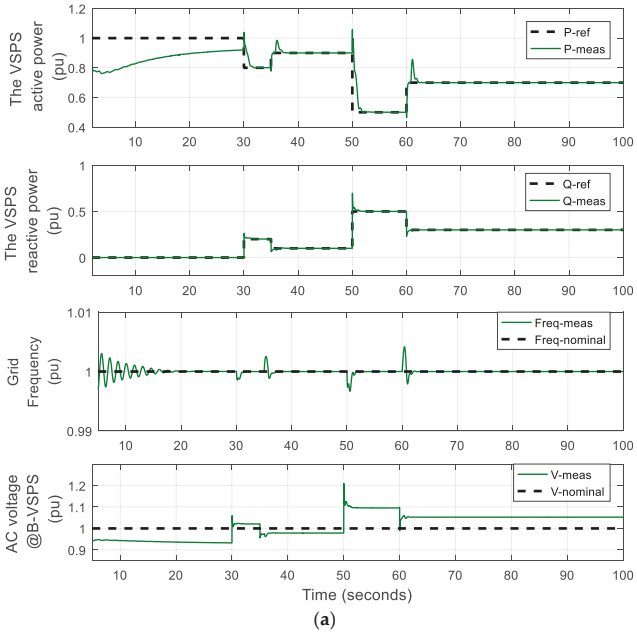
3. Results and Discussions

The control of power in the DFIM based VSPS system is essentially the power control of the VSC fed VSPS system. The results presented in this section demonstrate the dynamics and steady-state

responses of grid frequency and AC-bus voltage control. The performances are made by comparing between the control system with and without the droop control.

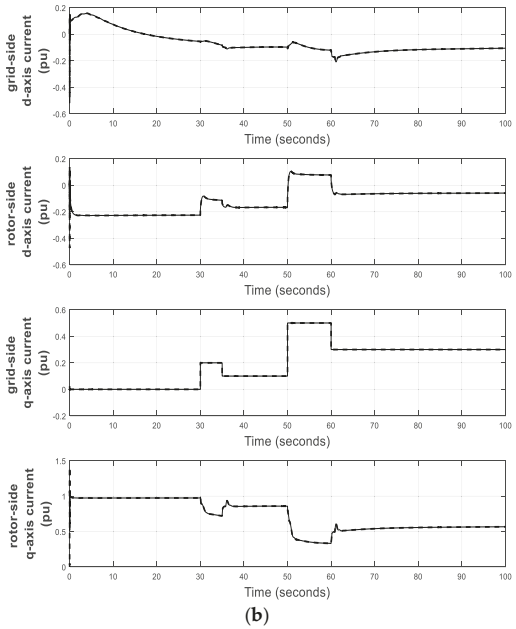
3.1. VSPS Grid-Integrated Network Simulation and Implications for Regulating Grid Frequency and AC-Bus Voltage in Case of Contingencies

The control of power in the DFIM-based VSPS system with a wind farm is essentially the power control of the VSC-fed VSPS system. Figure 12 shows the evolution of the VSPS unit in the proposed network depicted in Figure 11 but excluding the wind farm and with the absence of contingencies. Generally, the reference reactive power is set to zero for a system without droop control over any operating conditions since there is no reactive power exchange between the converter and the grid. However, to show the performance of the control system, the varying active and reactive power instructional signals are given to the control system as a reference value. As shown in Figure 12a, the proposed control system tracks the power fluctuation instructions very well. A small distortion is observed while the instruction signals vary from one value to the other. A 20% overshoot is perceived during the instruction signal switches from lower to higher values. The overshoots in active power have some impact on frequency deviations. The variations in instructional signal of reactive power cause the AC voltage to deviate from its nominal value. The excursions are quickly regulated. Figure 11b shows the response of the inner loop signals when the power fluctuation instructions are imposed on the outer loop system. The response shows perfect tracking of the respective reference signals. Similarly, precise tracking of inner loop control reference signals in the droop and without droop-fed vector control of the VSPS system along with the wind power farm is also shown in Figure 13. But since the droop-fed matters to change the reference values in the dq-rotor currents, the responses between the control system with and without droop-fed in the dq-rotor currents vary. Hence, the results from Figures 12 and 13 imply that the droop-fed vector control strategy based VSPS system can adjust the grid frequency and AC voltage fluctuations caused by wind energy or other contingencies in a power grid integrated system quickly and flexibly. This is verified in the following sections.



(**a**)

Figure 12. *Cont.*



(**b**)

Figure 12. The droop-fed vector control based VSPS system without wind farm: (**a**) tracking of power instructions on outer loop control; (**b**) tracking of inner loop control reference signals.

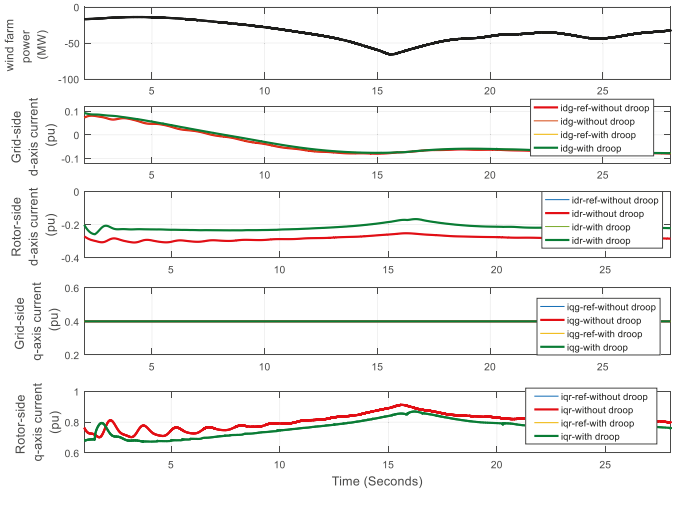


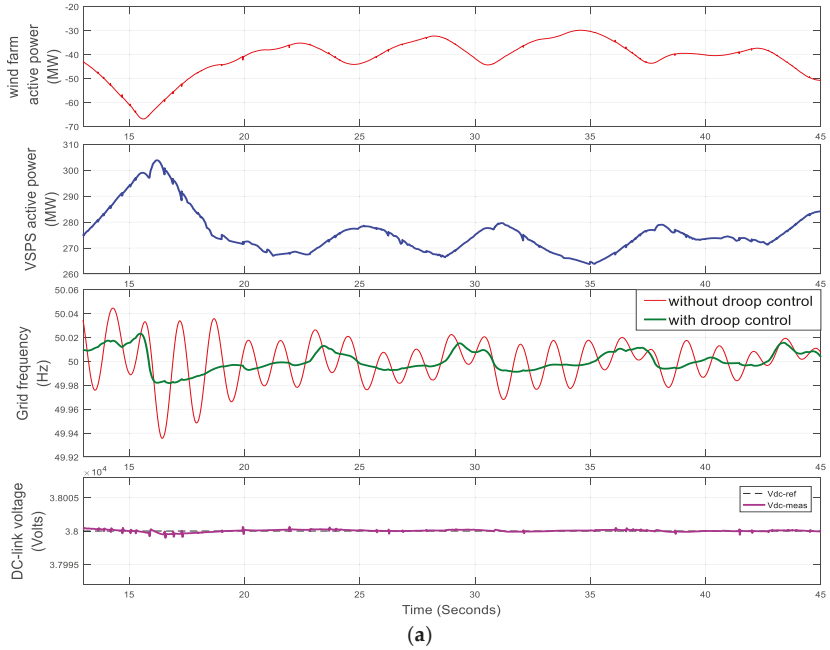
Figure 13. Tracking of inner loop control reference signals in the droop and without droop-fed vector control of the VSPS system along with wind farm.

3.2. Comparison of the Proposed Control Scheme with the Conventional Strategy

3.2.1. Grid Frequency Control and Response

Figure 14a shows the evolution of the network in grid frequency response by comparing the VSPS active power control with and without droop control and the DC-link voltage. While the power

fluctuation of the wind farm occurs in the grid, the VSPS is dedicated to compensate the fluctuations accordingly and smaller deviations in the grid frequency are recorded with droop than without droop control. The waveform of the DC voltage result shows a precise regulated dynamic response and insignificant deviations for wind power fluctuations. The difference in frequency deviations between the two control modes is more significant at a higher wind power fluctuation. It implies that the droop control system is effective for regulating the grid frequency excursions caused by large contingences. Figure 14b shows the evolution of the frequency comparison between these control modes during the start-up transient and when a three-phase fault is imposed at t = 30 s for nine cycles. During the start-up and fault, less excursions in frequency are observed with droop than without droop control. The time taken to dampen the frequency excursions to their nominal value without droop control is much longer than with droop. In this case, the droop control quickly and effectively regulates the frequency dynamics during grid disturbances.



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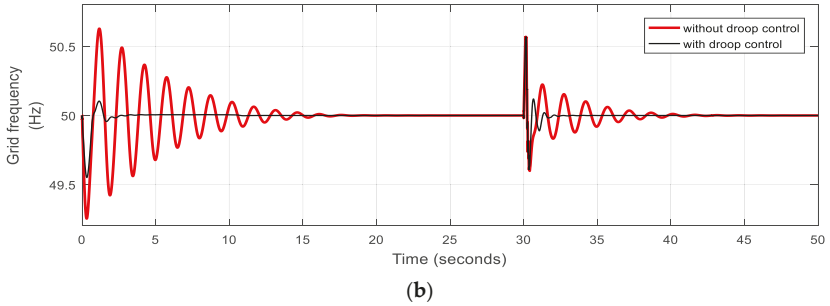

(**b**)

Figure 14. Evolution of the network in grid frequency response comparing the VSPS active power control with and without droop control and the DC link voltage as well: (**a**) while the wind farm power fluctuation exists in the grid; (**b**) during the start-up transient and three phase fault.

3.2.2. AC-Bus Voltage Control and Response

Figure 15 shows the AC-bus voltage regulation and response of the VSPS vector control system with and without being droop-fed. Two cases with different voltage levels are considered; one at the bus terminal of the VSPS plant (B_{vsps}), while the other at bus B_{SG3} in the grid system. In both cases, the AC bus voltage is improved to its nominal value with droop-control than without it. The AC voltage is well regulated as the equivalent reactive power is generated by the induction machine to compensate the voltage droop through the VSC based droop-fed vector control strategy. This verifies the strong known relationship between the reactive power and the AC-bus voltage stated in the load flow equation.

Figure 15 also shows the relationship between wind power fluctuations and AC voltage at buses B_{vsps} and B_{SG3}. When the wind fluctuation is increased, as shown in Figure 15 at t = 15.1 s, there is greater deviation in the AC-bus voltage at both buses in the conventional vector control strategy while it remains the same in the droop-fed control mode. This is because of the direct relationship between the reactive power absorbed from the grid by the induction generator of the wind farm and its active power generation. Therefore, the fluctuation of the active power generation caused by the wind speed variation results in higher absorption of reactive power by the induction generator which leads to AC-bus voltage deviation in the grid. Hence, the VSC based droop control of the VSPS system plays a key role of balancing the generation and absorption of reactive power in the grid at varying active power from the wind farm so as to regulate the AC bus voltage.

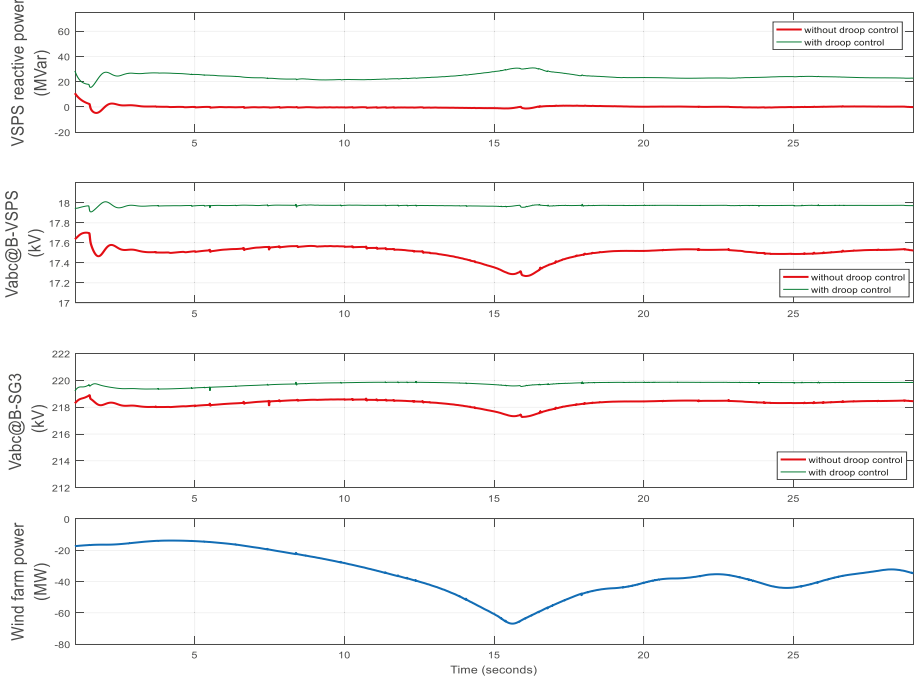

Figure 15. Evolution of the network in AC-bus voltage response of the VSPS control system considered at two buses by comparing the reactive power control with and without droop control while the wind is fluctuating.

3.3. The Frequency and AC Voltage Control and Response During Load Variations

Figure 16 demonstrates the grid frequency and AC bus voltage control and response when 20 MW load is added to the grid at t = 20 s and removed at t = 40 s in order to compare the performances of the

control modes between the droop-feed and without it. In Figure 16a, the evolution is the grid frequency associated with the active power injected at the bus B_{SG3} and the VSPS active power generation while the load is added and removed to and from the grid. The frequency tracks its nominal value very quickly with the droop control than without droop. In the absence of droop control, when the power imbalance occurs, the frequency is very sensitive for deviation and hardly to control timely. The bus power injection is also affected by the frequency fluctuation, but with the droop control, it regulates the power supply/load balance by adjusting the VSPS to increase or decrease its generation accordingly.

Figure 16b simulates the AC bus voltage control associated with the reactive power status of the VSPS plant. When the load is added to the grid, the AC bus voltage decreases more with the control system without droop mode, but in the droop mode, the voltage tracks its nominal value, because of generating more reactive power by the VSPS plant.

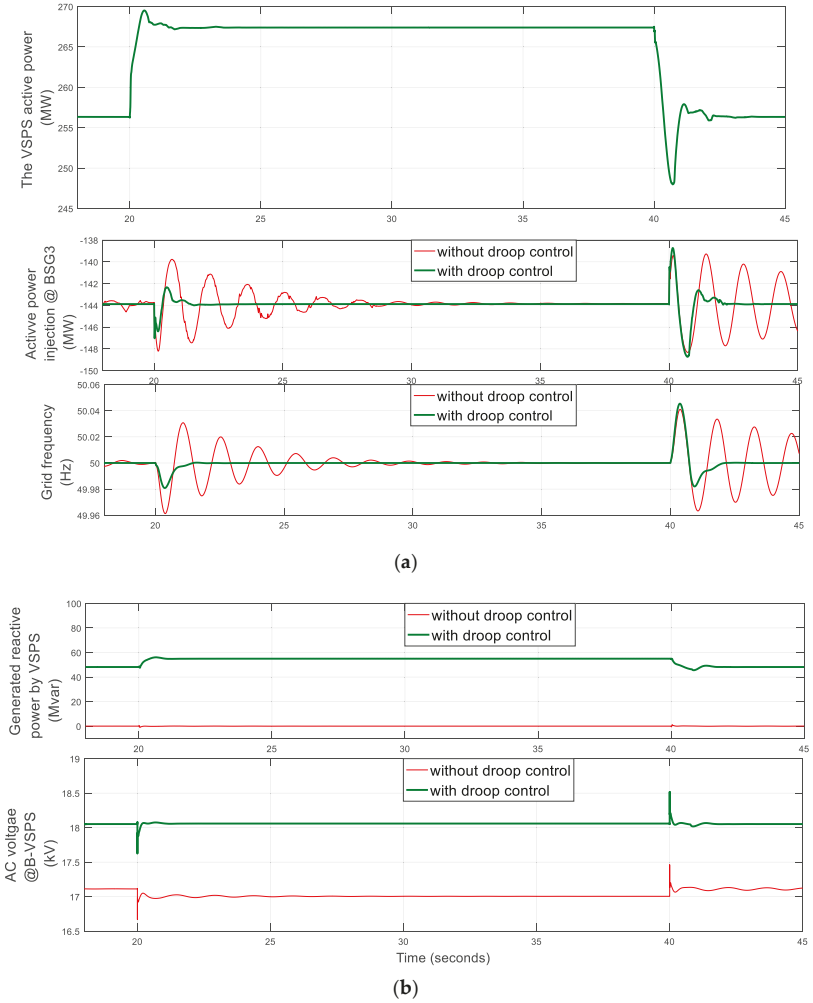

Figure 16. Evolutions of the network in the load variations; (**a**) in frequency control and response associated with active power; (**b**) AC bus voltage control and response associated with reactive power generation by the VSPS.

In general, the droop-fed vector control is quite effective to regulate the grid frequency and AC-bus voltage; in turn, it can help the stability development of the grid which are connected to a renewable energy resources.

4. Conclusions

This paper presents a study on droop-fed vector control strategy-based doubly fed induction machine VSPS system for the reduction of wind power fluctuation impact and other contingencies on grid frequency and AC-bus voltage stability. Mathematical models based on a phasor model technique is presented. A case study of a grid system having five supplies and two loads with seven buses is conducted. The grid includes both synchronous and induction machines. Since the rotor speed rotates synchronously with the rotating magnetic field of the stator of the synchronous machine, the grid frequency is computed from the rotor speed relationship for measuring and estimating to feed the VSPS active power control loop. The performance is validated in a MATLAB/Simulink platform. The results show that the proposed control strategy for the VSPS system achieves better dynamic and steady state controlling responses of grid frequency and AC-bus voltage in the power system than the conventional one while the intermittent wind power, load variations three-phase fault and start-up transients are imposed to the grid with small errors in acceptable ranges in the power grid system.

Author Contributions: Conceptualization, G.T.B. and M.H.; Methodology, G.T.B.; Software, G.T.B.; Validation, G.T.B., M.H. and S.A.M.; Formal Analysis, G.T.B.; Investigation, G.T.B.; Resources, M.H.; Data Curation, G.T.B.; Writing-Original Draft Preparation, G.T.B.; Writing-Review & Editing, M.H., P.S. and S.A.M.; Visualization, G.T.B.; Supervision, M.H.; Project Administration, M.H.; Funding Acquisition, M.H.

Funding: This research received no external funding.

Acknowledgments: This work was supported by the State Key Laboratory of Smart Grid Protection and Control, "111" Project (B08013) of China.

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

The followings are the main parameters of the system used in this paper:

- A VSC DFIM based VSPS plant; turbine rating = 300 MW; rated hydraulic head=165 m; piping area = 11.15 m^2; gate opening at no load = 0.06 pu and at full load = 0.94 pu; base value is taken as a power of 333 MVA and a voltage of 220 kV
    - power capacity = 333 MVA/18 kV, stator resistance and leakage inductance R_s = 0.0086 pu and L_{ls} = 0.152 pu, rotor resistance and leakage inductance R_r = 0.007 pu and L_{lr} = 0.187 pu, magnetization inductance L_m = 300 pu, inertia constant, friction factor, and pairs of poles H(s) = 10.6, f(pu) = 0.02 and p = 12
    - Converter rating = 66 MVA/38 kV DC voltage, the DC-link equivalent capacitance $C_{eq} = 2 \times 10^{-2}$ Farad, the coupling inductor resistance and inductance R = 0.0025 pu and L = 0.25 pu
    - The rotor side controller Current loop gains (P_i = 1.25 and I_i = 15) Active power loop gains (P_p = 1.5 and I_p = 20) Reactive power loop gains (P_q = 0.3 and I_q = 5.5) Frequency droop constant (K_f = 90) AC voltage droop constant (K_{ac} = 60)
    - The grid side controller Current loop gains (P_{ig} = 1.1 and I_{ig} = 9) DC voltage loop gains (P_{dc} = 0.001 and I_{dc} = 0.02)
    - Grid connecting transformer: capacity = 350 MVA, 18 kV/220 kV, winding parameters $R_1 = R_2$ = 0.0025 pu and $L_1 = L_2$ = 0.08 pu; magnetization resistance and inductance $R_m = L_m$ = 500 pu
- Two hydropower plants (synchronous generator): each has a power capacity = 200 MVA, 13.8 kV; and grid connecting transformer capacity = 350 MVA, 13.8 kV/220 kV.

- A diesel power plant (synchronous generator): Power capacity = 15 MVA, 25 kV; grid connecting transformer capacity = 20 MVA, 25 kV/220 kV.
- A wind farm with induction generator: seven turbines 15 MW capacity each, 575 V; and grid connecting transformer capacity 12 MVA, 575 V/220 kV for each wind turbine
- Load = 630 MVA and the system frequency is 50 Hz.

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A Virtual Micro-Islanding-Based Control Paradigm for Renewable Microgrids

Khurram Hashmi [1,*], Muhammad Mansoor Khan [1], Huawei Jiang [2], Muhammad Umair Shahid [1], Salman Habib [1], Muhammad Talib Faiz [1] and Houjun Tang [1]

[1] School of Electronics Information and Electrical Engineering (SEIEE), Shanghai Jiao tong University, No. 800 Dongchuan Road, Shanghai 200240, China; mkhancn@yahoo.com (M.M.K.); muhammadumairshahid@sjtu.edu.cn (M.U.S.); sams560@sjtu.edu.cn (S.H); talib_faiz@sjtu.edu.cn (M.T.F.); hjtang@sjtu.edu.cn (H.T.)

[2] State Grid, Wuxi Power Supply Company, Wuxi 214000, China; jiang.huawei93@outlook.com

* Correspondence: khurram_hashmi@sjtu.edu.cn; Tel.: +86-132-6290-7351

Received: 27 May 2018; Accepted: 28 June 2018; Published: 4 July 2018

Abstract: Improvements in control of renewable energy-based microgrids are a growing area of interest. A hierarchical control structure is popularly implemented to regulate key parameters such as power sharing between generation sources, system frequency and node voltages. A distributed control infrastructure is realized by means of a communication network that spans the micro-distribution grid. Measured and estimated values, as well as corrective signals are transmitted across this network to effect required system regulation. However, intermittent latencies and failures of component communication links may result in power imbalances between generation sources, deviations in node voltages and system frequency. This paper proposes a hierarchical control structure to regulate the operation of an islanded AC microgrid experiencing communication link failures. The proposed strategy aims to virtually sub-divide the microgrid into controllable "islands". Thereafter, active power sharing, frequency and voltage restoration is achieved by competing converter systems through multi-agent consensus. The effectiveness of the proposed methodology has been verified through stability analyses using system wide mathematical small signal models and case study simulations in MATLAB, Simpower systems.

Keywords: microgrid control; distributed control; power system operation and control

1. Introduction

Recent advances in renewable energy technologies have led to a greater penetration of distributed renewable energy resources (DERs) in power distribution networks. However, due to the stochastic nature of renewable energy resources, Distributed Generation Units (DGUs) suffer from voltage deviations, frequency and power flow variations. Micro-grids (MGs) present a viable solution to the renewable energy integration problem. A micro grid is usually composed of a smaller power distribution network, energy sources, energy storages, Electric Vehicles (EV), DGUs, supervisory control and data acquisition devices. The MG behaves as a smaller isolated power system that can operate either as an energized island or in synchrony with the legacy power network. Local control measures are applied within the micro-grid to address voltage, frequency and power flow deviations [1–4].

Power conversion stages of multiple DGUs operate in parallel through the MG distribution network. Proportional sharing of power between various DGUs is required to ensure stable system operation and fair power contribution by each generation source in a microgrid. Droop control methods are employed as a simple decentralized strategy for sharing total load power among DGUs. Active and reactive power fractions proportional to frequency and amplitude respectively, are subtracted from

converter output. This method is commonly referred to as *P-f* and *Q-E* droop method and has been previously used in the control of un-interruptible power supply systems (UPS) [5–10]. Although, the droop methods provide a degree of reliability, there are certain drawbacks associated therewith. *P-f* / *Q-E* droop control works on the principle of reducing frequency and voltage by fractions to achieve power sharing. To keep the system voltage and frequency within a permissible range, a secondary control layer must be implemented to periodically correct these deviations. This can be realized through a centralized hierarchical control; composed of three or more control layers; or a decentralized control strategy where local nodes share information that modifies voltage and frequency references for inner control loops [10–14].

Most centralized control algorithms require a two-way transmission of information between DGUs throughout the system and Microgrid central controllers (MGCC). Such a control structure is often complicated and expensive to implement, in addition to being susceptible to single point of failure (SPOF). Therefore, a decentralized control approach employing consensus algorithms, has emerged as an alternate to centralized control methods [2,15–17]. Consensus-based methods model the frequency and voltage restoration goals as a multi-agent consensus problem; where, each power converter behaves as an agent regulating its voltage and frequency in combination with other agents (nodes), collectively arriving at consensus values for $\boldsymbol{V}$ and $\boldsymbol{f}$. A virtual leader node may provide desired nominal values for controlled parameters to the micro grid controls [2,18,19].

Some researches propose a secondary voltage restoration method based on distributed cooperative control of multi-agent systems [12], wherein individual inverter units are considered as systems having non-linear internal dynamics. Input-Output feedback linearization is used to convert the secondary voltage restoration problem in such units into a second order linear tracker synchronization problem. The authors in [20] explore active power sharing in islanded AC microgrid with secondary control of frequency and voltage restoration. The inverters have been modeled as cooperative multiagent systems such that their frequency and voltage restoration be a synchronization problem. In [21], the authors present a consensus-based distributed secondary restoration control for both frequency and voltage in droop-controlled AC microgrids.

The authors in [22], present a distributed secondary control method for an inverter-based microgrid with uncertain communication links. The method discussed addresses active power flow control and restoration of frequency and voltage to nominal values. In [23], a distributed control strategy for reactive power sharing and voltage restoration in AC microgrids is presented. The strategy discussed uses small signal model of the system and sensitivity analysis to evaluate the relationship between voltage magnitude and reactive power sharing. In [24], authors have proposed a consensus-based distributed voltage control algorithm for islanded inverter-based microgrids with arbitrary meshed electrical topologies. This algorithm is based on weighted average consensus protocol that replaces traditional V-Q droop method.

The authors in [25] present a dynamic consensus algorithm (DCA) for coordinated control with an autonomous current sharing control strategy to balance discharge rate of energy storage systems (ESS) in an islanded AC microgrid. The DCA is used to share information between DG converter units to regulate output power according to ESS capacities and battery state of charge. In [26] authors propose a cooperative distributed control method for AC microgrids that discusses an alternate for the centralized secondary control and the primary-level droop mechanism of each inverter. Voltage, reactive power, and active power regulators are employed to achieve regulation of these parameters.

The work presented in [12,20,21,23,24] assumes a fault-free communication network with no broken or disrupted communication links. The communication digraph used is, therefore, time in-varying. However, the studies presented in [22,25,26] discuss scenarios with faulty communication links. The authors in [25] have represented faulty communications through a dynamically varying digraph.

This work proposes a hybrid, multi-agent consensus-based control strategy to realize power sharing, voltage and frequency regulation for an islanded AC microgrid. The method developed here addresses faults created by faulty communication links through virtually isolating portions of the

network suffering from communication faults and intermittencies. Thereafter, the control parameters are tuned to treat these isolated portions as smaller "virtual micro-grids" within the larger micro-gird. The salient contributions of this work are:

1. Identification of failed communication links.
2. Virtual segmentation of the MG network into smaller controllable islands.
3. Variation in droop and consensus control parameters to achieve power sharing, voltage and frequency restoration during communication faults.
4. Using small signal analysis to study MG system stability under the proposed control scheme.

The rest of the paper is divided as follows: Section 2 gives the microgrid network layout, derives the admittance matrix and fundamental power flow equations. Section 3 describes the hierarchical control paradigm proposed. Section 4 gives details of the communication network layer and basic graph theoretic definitions. Section 5 expounds the virtual sub islanding method used in this work. Section 6 gives small signal system derivation. Section 7 presents the results of stability analysis using eigen evolutions. Section 8 gives case study simulations and results. Section 9 concludes the paper.

2. Network Layout

This section describes the network layout and derives the admittance matrix and fundamental power flow equations. Figure 1 represents a simplified radial type three phase three wire system used in this study and the proposed four level control strategy. Buses 1 through 6 are fed through power electronic converters interfaced with the network using LC filters. The buses 2 through 6 are directly loaded with adjustable power loads whereas bus-1 is not directly loaded. This network can be operated in islanded mode. Table 1 outlines rated system parameters and Table 2 gives bus loads. All distributed renewable generators are represented by equivalent DC sources. Later sections describe the multi-level control methodology in detail.

Table 1. System parameters for microgrid control.

Parameters	Values	Parameters	Values
L_f	1.35 mH	m_p	4.5×10^{-6}
R_f	0.1 Ω	n_q	1×10^{-6}
C_f	25 μF	K_{pf}	0.4
L_c	1.35 mH	K_{if}	0.5
R_c	0.05 Ω	K_{pV}	0.5
R_{line}	0.1 Ω	K_{iV}	0.3
L_{line}	0.5 mH	F	1
f_{nom}	60 Hz	ω_c	60 Hz
V_{nom}	415 $V_{L\text{-}L}$		

Table 2. System loads.

Bus. No.	Directly Connected Bus Load	
	P (p.u.)	Q (p.u.)
1.	0	0
2.	0.3	0.3
3.	0.25	0.25
4.	0.25	0.25
5.	0.25	0.25
6.	0.25	0.25
7.	0	0

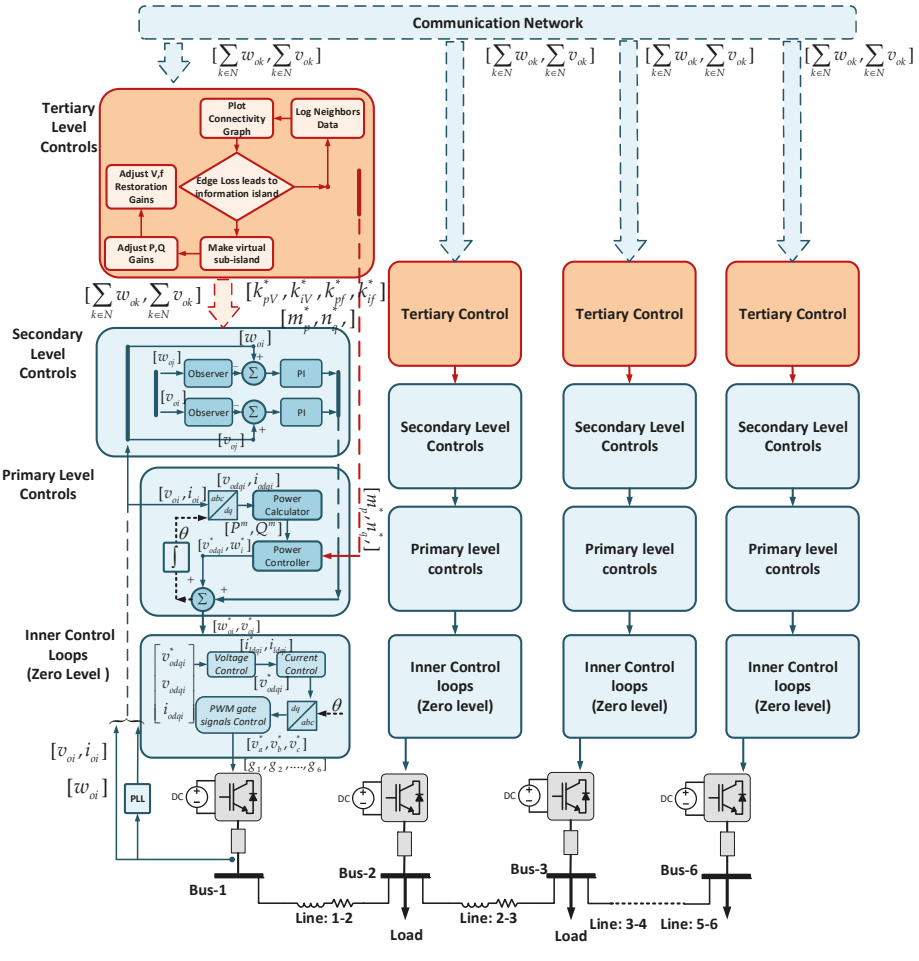


Figure 1. Distribution network and control system layout.

Equation (1) Gives the combined bus admittance matrix of micro network. Equation (2) gives the steady state model of the system.

$$Y_{busMG} = \begin{bmatrix} (Y_{s1}+Y_{17}+Y_{12}) & -Y_{12} & 0 & 0 & 0 & 0 & -Y_{17} \\ -Y_{21} & (Y_{s2}+Y_{23}+Y_{12}) & -Y_{23} & 0 & 0 & 0 & 0 \\ 0 & -Y_{32} & (Y_{s3}+Y_{32}+Y_{34}) & -Y_{34} & 0 & 0 & 0 \\ 0 & 0 & -Y_{43} & (Y_{s4}+Y_{43}+Y_{45}) & -Y_{45} & 0 & 0 \\ 0 & 0 & 0 & -Y_{54} & (Y_{s5}+Y_{54}+Y_{56}) & -Y_{56} & 0 \\ 0 & 0 & 0 & 0 & -Y_{65} & (Y_{s6}+Y_{65}) & 0 \\ -Y_{71} & 0 & 0 & 0 & 0 & 0 & (Y_{71}+Y_{s7}) \end{bmatrix} \quad (1)$$

$$[Y_{busMG}] \bullet \begin{bmatrix} V_1 & V_2 & V_3 & V_4 & V_5 & V_6 & V_7 \end{bmatrix}^T = \begin{bmatrix} I_{s1} & I_{s2} & I_{s3} & I_{s4} & I_{s5} & I_{s6} & I_{s7} \end{bmatrix}^T \quad (2)$$

where $\boldsymbol{Y_{si}}$ represents the inverter (source) LCL coupling admittance; $\boldsymbol{Y_{ij}}$ represents the line admittance between $\boldsymbol{i^{th}}$ and $\boldsymbol{j^{th}}$ busses (nodes); $\boldsymbol{I_{si}}$ represents the current injected into the $\boldsymbol{i^{th}}$ bus. The active and reactive powers injected at each node can be given by (3) and (4).

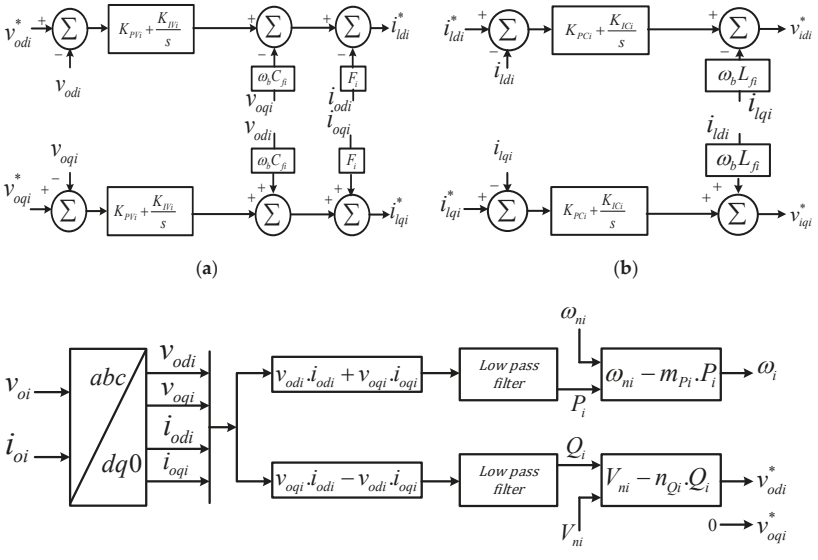
$$P_i = \sum_{n=1}^{N} |Y_{in} V_i V_n| \cdot \cos(\theta_{in} + \delta_n - \delta_i) \tag{3}$$

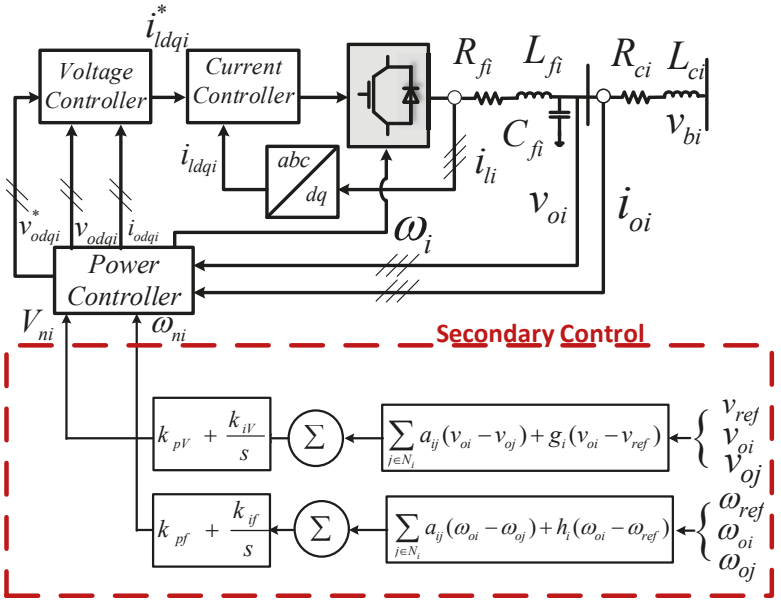
$$Q_i = -\sum_{n=1}^{N} |Y_{in} V_i V_n| \cdot \sin(\theta_{in} + \delta_n - \delta_i) \tag{4}$$

where, $\boldsymbol{Y_{in}}$ is the admittance connected between $\boldsymbol{i^{th}}$and $\boldsymbol{n^{th}}$ bus; $\boldsymbol{V_i}$is the voltage magnitude at $\boldsymbol{i^{th}}$ inverter terminal and $\boldsymbol{V_n}$ is voltage magnitude at the $\boldsymbol{n^{th}}$ bus; θ_{in} is the admittance angle between bus ith and nth bus, δ_n is voltage angle at $\boldsymbol{n^{th}}$ bus whereas δ_i is the voltage angle at $\boldsymbol{i^{th}}$ bus.

3. Hierarchical Control Paradigm

This section elaborates on the hierarchical control structure implemented to regulate the microgrid network. the distributed control paradigm is divided into four layers, as shown in Figure 1. The inner, or zero level controls, consist of current and voltage control loops that regulate basic local dynamics. The primary level controls address power balancing between converter nodes. The secondary level controls serve to correct voltage and frequency deviations created by primary control action. The zero level, primary and secondary controls are further elaborated in Figure 2a–d. This work proposes a tertiary level control, aimed at detecting communication link failures and mitigating their effect by creating smaller virtual sub-islands within the microgrid and regulating their performance by modifying secondary and primary controller parameters. The tertiary controls absorb and process frequency and voltage measurements $\left(\sum_{k\in N} \omega_{ok}, \sum_{k\in N} v_{ok}\right)$, from node neighborhood. Once the status of connectivity of the network has been determined as described in Section 5, updated references for voltage and frequency PI gains in secondary control $K_{pV}{}^*, K_{iV}{}^*, K_{pf}{}^*, K_{if}{}^*$, and droop gains $m_p{}^*, n_p{}^*$ are passed down to secondary and primary levels.





(**d**)

Figure 2. (**a**) Voltage Control loop; (**b**) Current Control loop; (**c**) Primary Control: Power Controller; (**d**) Secondary Control: Voltage and Frequency regulation.

3.1. Zero Level Control loops: Voltage and Current Regulation

Voltage and current control loops in d-q-0 frame form the zero level control loops for each of the power converters as shown in Figure 2a,b. dynamical equations for voltage control loop are given as (5) and (6).

$$\left.\begin{array}{l} \frac{d\phi_{di}}{dt} = \phi'_{di} = u^*_{odi} - u_{odi} \\ \frac{d\phi_{qi}}{dt} = \phi'_{qi} = u^*_{oqi} - u_{oqi} \end{array}\right\} \tag{5}$$

$$\left.\begin{array}{l} i^*_{ldi} = F_i \cdot i_{odi} - \omega_b \cdot C_{fi} \cdot u_{oqi} + K_{PVi}\left(u^*_{odi} - u_{odi}\right) + K_{IVi}\phi_{di} \\ i^*_{lqi} = F_i \cdot i_{oqi} - \omega_b \cdot C_{fi} \cdot u_{odi} + K_{PVi}\left(u^*_{oqi} - u_{oqi}\right) + K_{IVi}\phi_{qi} \end{array}\right\} \tag{6}$$

where, K_{PVi} and K_{IVi} represent the proportional and integral gains of the voltage controller. ϕ_{di} and ϕ_{qi} are auxiliary state variables for the PI controllers. F_i is the feed-forward gain. v_{oqi}, v_{odi}, i_{odi} and i_{oqi} are system measurements as seen in Figure 2d.

Similarly, (7) and (8) represent the dynamical model for current control loop at each node as shown in Figure 2b.

$$\left.\begin{array}{l} \frac{d\varsigma_{di}}{dt} = \varsigma'_{di} = i^*_{ldi} - i_{ldi} \\ \frac{d\varsigma_{qi}}{dt} = \varsigma'_{qi} = i^*_{lqi} - i_{lqi} \end{array}\right\} \tag{7}$$

$$\left.\begin{array}{l} u^*_{idi} = -\omega_b \cdot L_{fi} \cdot i_{lqi} + K_{PCi}\left(i^*_{ldi} - i_{ldi}\right) + K_{ICi}\varsigma_{di} \\ u^*_{iqi} = \omega_b \cdot L_{fi} \cdot i_{ldi} + K_{PCi}\left(i^*_{lqi} - i_{lqi}\right) + K_{ICi}\varsigma_{qi} \end{array}\right\} \tag{8}$$

where, K_{PCi} and K_{ICi} represent the proportional and integral gains of the voltage controller. ς_{di} and ς_{qi} are auxiliary state variables for the PI controllers used. i_{lqi} and i_{ldi} are system measurements as seen in Figure 2d.

3.2. Primary Controls: Power Balancing between Distributed Sources

Power sharing control is based on so called "droop" principle [27], i.e., frequency and voltage are proportionally reduced to achieve active and reactive power sharing respectively as shown in Figure 2c. Equations (9) and (10) represent the droop controller.

$$\omega_i^* = \omega_i - m_{Pi} \cdot (P_i) \tag{9}$$

$$\left.\begin{array}{c} V_{di}^* = V_{di} - n_{Qi} \cdot (Q_i) \\ V_{qi}^* = 0 \\ V_o = \sqrt{V_{di}^{*2} + V_{qi}^{*2}} \end{array}\right\} \tag{10}$$

where, ω_i and V_0 are the nominal references of frequency and voltage for the ith inverter. P_i and Q_i correspond to active and reactive power being injected by the $\boldsymbol{i^{th}}$ power inverter at output terminals. m_{Pi} and n_{Qi} are droop gains that can be calculated as (11).

$$\left\{\begin{array}{l} m_{Pi} = \frac{\Delta\omega}{Pmax} \\ n_{Qi} = \frac{\Delta V}{Qmax} \end{array}\right. \tag{11}$$

where, $\Delta\omega$ and ΔV are the maximum change permissible for converter frequency and voltage respectively. *Pmax* and *Qmax* are the maximum active and reactive power the converter can deliver [12]. Primary control calculates power using two-axis theory. For accurate measurement of the fundamental power component low pass filters are used having cut off frequency of ω_{ci}. The reference frames of all inverters may be converted a common reference frame. The angle difference between $\boldsymbol{i^{th}}$ inverter and common frequency reference frame can be shown as (12)

$$\delta = \int (\omega - \omega_{com}) \cdot dt \tag{12}$$

where, ω_{com} is the MG common system frequency.

3.3. Secondary Controls: Voltage Magnitude and Frequency Restoration

Voltage magnitude and frequency restoration is achieved through multiagent consensus-based secondary control implemented at each node [28]. Figure 2d shows the distributed frequency and voltage restoration control schemes. Frequency regulation method is given by (13).

$$\left.\begin{array}{rl} \delta\omega_i(t) = & k_{pf} e_{\omega i}(t) + k_{if} \int e_{\omega i}(t) \cdot dt \\ e_{\omega i}(t) = \sum\limits_{j \in N_i} & a_{ij}\left(\omega_{oi}(t) - \omega_{oj}(t)\right) \\ & + h_i\left(\omega_{oi}(t) - \omega_{ref}(t)\right) \end{array}\right\} \tag{13}$$

where, ω_{ref} is the nominal reference frequency, ω_{oj} is the measured system frequency sensed at all nodes in the neighborhood of the $\boldsymbol{i^{th}}$ node being considered. k_{pf} and k_{if} are proportional and integral gains as shown in Figure 2d. $\delta\omega_i$ is the frequency correction applied to frequency reference of the $\boldsymbol{i^{th}}$ inverter node. h_i is pinning gain whose value is zero for primary node.

The voltage regulation method is described in (14):

$$\left.\begin{array}{rl} \delta V_i = & k_{pv} e_{vi} + k_{iv} \int e_{vi} dt \\ e_{vi}(t) = \sum\limits_{j \in N_i} & a_{ij}\left(v_{oi}(t) - v_{oj}(t)\right) \\ & + g_i\left(v_{oi}(t) - v_{ref}(t)\right) \end{array}\right\} \tag{14}$$

where, v_{nom} is the nominal reference voltage for the system in p.u., v_{oj} is the system voltage sensed at all converter nodes in the communication neighborhood of the node $\boldsymbol{i}$being considered. k_{pv} and k_{iv} are

proportional and integral gains as shown in Figure 2d. δV_i is the voltage correction applied to voltage reference of the i^{th} inverter node. g_i is pinning gain whose value is zero for primary node.

4. Communication Network

The communication network used to exchange information between DGs can be modelled as a digraph. A digraph is usually expressed as $G_{com} = (V_g\ E_g\ A_g)$ which is composed of a non-empty, finite set of M nodes given by $V_g = \{ v_1\ v_2\ v_3 \ldots\ v_M\}$. The arcs that connect these nodes are given by $E_g \subset V_g \times V_g$. The associated adjacency matrix is given by $A_g = [a_{ij}] \in R^{N\times N}$. In a microgrid, the DGs can be thought of as the nodes of a communication digraph whereas the arcs represent communication links [28].

In this work, it is assumed that the communication network is initially stable and time invariant as represented in Figure 3a. However, communication links are made to break in analysis given in later sections of the paper. Channel noise has been neglected for simplifying calculations. Therefore, the representative digraph is also initially time invariant, i.e., A_g is a constant. An arc from node $\boldsymbol{j}$ to node $\boldsymbol{i}$ is denoted by $(v_j\ ,\ v_i)$, where node $\boldsymbol{j}$ receives information from node $\boldsymbol{i}$. a_{ij} is the weight of the arc connecting v_i to v_j. $a_{ij} > 0$, if $(v_j\ ,\ v_i) \in E_g$, otherwise $a_{ij} = 0$. Node i is called a neighbor of node j, if the arc$(v_j\ ,\ v_i) \in E_g$. Set of nodes neighboring the ith DGU v_i are given by $N_i = \{v_j \in V_g : (v_i\ , v_j) \in E_g\}$. The Laplacian Matrix $L_g = (l_{ij})_{N\times N}$ is defined as $l_{ij} = -a_{ij}$, $i \neq j$ and $l_{ii} = \sum_{j-1}^{N} a_{ij}$ for $i = 1, \ldots,\ N$. Such that $L_{1N} = 0$ with $1_N = (1,\ \ldots, 1)^T \in R^N$. The in-degree matrix can be defined as $D_G^{in} = diag\ \{d_i^{in}\}$, where, $d_i^{in} = \sum\limits_{j\ \in\ N_i} (a_{ji})$and out-degree matrix as $D_G^{out} = diag\ \{d_i^{out}\}$, where $d_i^{out} = \sum_{i\ \in\ N_i}(a_{ji})$. The diagonal pinning gain matrix is given by $G = diag\ \{g_i\}$. The system adjacency, degree and Laplacian matrix are given in Appendix C.

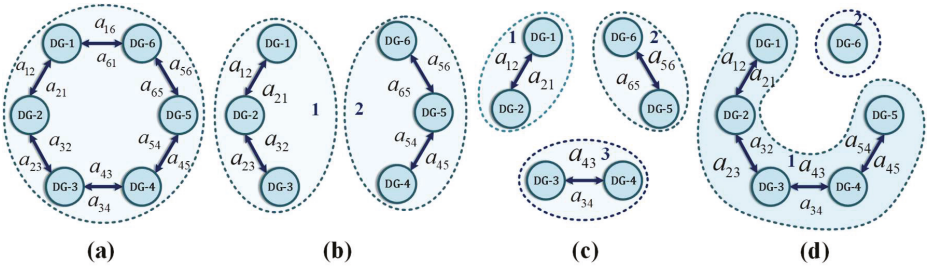


Figure 3. Communication network connectivity: (**a**) Full ring bidirectional connectivity; (**b**) Dual link failure resulting in two symmetrical sub networks; (**c**) Triple link failure resulting in three symmetrical sub networks; (**d**) Dual link failure resulting in two asymmetrical sub-networks.

The multiagent consensus algorithms implemented across the MG system converge over time according to [29]. The global system dynamics can therefore be given as (15) and (16).

$$\dot{x} = -(\boldsymbol{D_g} + \boldsymbol{G_g})x + \boldsymbol{A_g}x = -(\boldsymbol{D_g} + \boldsymbol{G_g} - \boldsymbol{A_g})x + Gx_0 \tag{15}$$

where,

$$\dot{x} = -(\boldsymbol{L_g} + \boldsymbol{G_g})x + G\underline{x}_0 \tag{16}$$

and,

$$\underline{x}_0 = 1x_0 = [x_o \ldots x_0]^T$$

5. Virtual Sub-Islanding: Tertiary Controls

In this section, tertiary controls are presented here that monitor network connectivity. When link breakage is detected the microgrid network is virtually partitioned into sub-networks determined by connectivity of healthy communication links as described in Figure 3b,d. The supervisory consensus gains in the secondary control loop and primary control droop gains are subsequently updated to regulate power sharing and frequency voltage regulation. The following subsections further elaborate these functions.

5.1. Cut Set Enumeration

Cut set enumeration is used to analyze virtual segmentation of the microgrid network into major and minor sub-islands. A cut set of a connected graph or nodes may be defined as set of edges whose removal can disconnect the graph or nodes. Therefore, a cut set divides a graph into exact components and can subsequently be used to denote a partition of the vertices [30,31]. If V_g denotes the vertex of graph G, and if P_g is the subset of vertices in one component of graph G induced by a cut set, then the cut set can be represented by, $(P_g, \overline{P}_g)$, where $\overline{P}_g = V_g - P_g$. The cut set space for a graph with n vertices has dimensions of $(n-1)$.

5.2. Depth First Search Algorithm

The Depth First Search (DFS) algorithm is used to analyze graph connectivity. A graph G_{com} consists of vertices V_g and edges E_g. Initially all vertices are considered as un-visited. The DFS algorithm starts from any vertex of the graph and follows an edge until it reaches next vertex V_g. While choosing an edge to traverse, an edge emanating from an un-visited vertex is always chosen. A set of old vertices V_g with possible unvisited edges are stored in memory [32,33]. The updated Laplacian matrix then can be obtained as $L_g = D_g^{in} - A_g$ [32,34,35].

The following Lemmas elaborate the formation of cut-sets:

Lemma 1. *A vertex cut set for graph $G_{com} = (V_g, E_g)$ is a sub set of V_g, whose removal will result into a disconnected graph. The vertex connectivity of graph G_{com}, represented by $k_0(G_{com})$, is the minimum number of vertices in any of its vertex cut set. Assuming N nodes form a graph, if two sub sets become disconnected from each other, one of these sets of agents/ nodes are considered lost [33]. Since there are two such sets created, the smaller of the two will be considered as lost. We can define a ratio as:*

$$\varnothing(S) = \frac{\varepsilon(S, S^c)}{\min\{card(S), card(S^c)\}} \tag{17}$$

where, $\varepsilon(S, S^c)$ is the number of disconnected nodes, $card(S)$ and $card(S^c)$ are the number of nodes in sub sets.

Cheeger's Inequality [33] states that:

$$\varnothing(S) \geq \lambda_2(G_{com}) \geq \frac{\varnothing(G_{com})^2}{2d_{max}(G_{com})} \tag{18}$$

Lemma 2. *Let graph $G_{com} = [V_g, E_g]$, for each vertex $v \in V_g$ (node) creates a lookup table that contains all vertices w, such that $(v, w) \in E_g$. This lookup table is called adjacency matrix for vertex V_g. A set of lookup tables at each node (vertices) in graph G_{com} is called adjacent structure for graph G_{com}. A graph may have many adjacency structures because every edge around a vertex gives an adjacency structure and every structure leads to a unique arrangement of edges at each vertex.*

The Depth First Search method (DFS) described in Appendix B [32] functions efficiently using the adjacency structure producing set of edges (E_g). DFS algorithm is here labeled depth first index,

$DFI(v)$ for every vertex V_g. Initially the value is equal to zero, whereas on the last iteration, the $DFI(v)$ is the order of last visited vertex V_g. The complexity of the algorithm is $O(\max(n, |E_g|))$. For every $v \in V$, $DFI(v)$ Is called only once after it will be $DFI(v) = 0$. DFS algorithm total time proportional to $|E_g|$.

The proposed method uses each node to maintain a communication link table of all known nodes throughout the micro network. These tables are updated following an exchange of information between neighboring nodes. When one or more communication links fail partially or completely, as shown in Figure 3b–d, the proposed algorithm virtually segments the network into smaller "virtual" sub micro grids. The control parameters for these scenarios are determined by arriving at good tradeoffs between system stability and better performance for each case. Eigen evolutions are used to arrive at these optimized values that are then stored in lookup tables, as shown in Table 3, that updated droop gains (m_p*, n_q*) and consensus gains (K_{pV} *, K_{iV} *, K_{pf} *, K_{if} *) accordingly.

Table 3. Controller parameters for analyzed cases.

Cases	Description	Secondary Consensus Gain			Primary Droop Gain	
1.	Full ring network	Voltage	K_{pV} K_{iV}	0.5 0.1	m_p	1.0×10^{-10}
		Frequency	K_{pf} K_{if}	0.4 0.1	n_q	1.0×10^{-7}
2.	Two symmetrical islands formed	Voltage	K_{pV} K_{iV}	0.7 0.2	m_p	1.0×10^{-5}
		Frequency	K_{pf} K_{if}	0.8 0.2	n_q	1.0×10^{-3}
3.	Three symmetrical islands formed	Voltage	K_{pV} K_{iV}	1.2 0.3	m_p	2.5×10^{-3}
		Frequency	K_{pf} K_{if}	1.5 0.2	n_q	1.0×10^{-3}
4.	Two asymmetrical islands formed	Voltage	K_{pV} K_{iV}	3.0 0.5	m_p	2.0×10^{-4}
		Frequency	K_{pf} K_{if}	2.2 0.5	n_q	1.0×10^{-4}

6. Small Signal Analysis of Microgrid System

To evaluate the performance of a proposed control method, small signal analysis of the MG system is undertaken [29,36]. Large signal dynamical equations are perturbed to obtain small signal model of the entire MG system. This section elaborates the small signal model components used in development and analysis of the control scheme.

6.1. Zero Level Converter Control Model

Small signal model for voltage control are given as in Equations (19)–(22), obtained by perturbing respective dynamical equations around quiescent point at which stability analysis is required [37,38].

$$\Delta\phi_{di} = \phi'_{di} = \Delta v^*_{odi} - \Delta v_{odi} \tag{19}$$

$$\Delta\phi_{qi} = \phi'_{qi} = \Delta v^*_{oqi} - \Delta v_{oqi} \tag{20}$$

$$\Delta i^*_{ldi} = F_i \cdot \Delta i_{odi} - \omega_b \cdot C_{fi} \cdot \Delta v_{oqi} + K_{PVi}(\Delta v^*_{odi} - \Delta v_{odi}) + K_{IVi}\phi_{di} \tag{21}$$

$$\Delta i^*_{lqi} = F_i \cdot \Delta i_{oqi} - \omega_b \cdot C_{fi} \cdot \Delta v_{odi} + K_{PVi}\left(\Delta v^*_{oqi} - \Delta v_{oqi}\right) + K_{IVi}\phi_{qi} \tag{22}$$

where, K_{PVi} and K_{IVi} represent the proportional and integral gains of the voltage controller. $\Delta\phi_{di}$ and $\Delta\phi_{qi}$ are perturbations in auxiliary state variables for the PI controllers. F_i is the feed-forward gain. v_{oqi}, v_{odi}, i_{odi} and i_{oqi} are system measurements as described before.

Similarly, Equations (23)–(26) represent the small signal model for current control loop at each node as shown in Figure 2b.

$$\Delta\varsigma_{di} = \varsigma'_{di} = \Delta i^*_{ldi} - \Delta i_{ldi} \tag{23}$$

$$\Delta\varsigma_{qi} = \varsigma'_{qi} = \Delta i^*_{lqi} - \Delta i_{lqi} \tag{24}$$

$$\Delta v^*_{idi} = -\omega_b \cdot L_{fi} \cdot \Delta i_{lqi} + K_{PCi}(\Delta i^*_{ldi} - \Delta i_{ldi}) + K_{ICi} \cdot \Delta\varsigma_{di} \tag{25}$$

$$\Delta v^*_{iqi} = \omega_b \cdot L_{fi} \cdot + K_{PCi}\left(\Delta i^*_{lqi} - \Delta i_{lqi}\right) + K_{ICi} \cdot \Delta\varsigma_{qi} \tag{26}$$

where, K_{PCi} and K_{ICi} represent the proportional and integral gains of the voltage controller. $\Delta\varsigma_{di}$ and $\Delta\varsigma_{qi}$ are perturbations in auxiliary state variables for the PI controllers used. i_{lqi} and i_{ldi} are system measurements as described before in Section 3.

6.2. Primary Power Sharing Control Model

The linearized small signal model for power controller can be written as Equations (27) and (28). The power controller provides operating frequency for the DGU ($\boldsymbol{\omega_i}$) and reference voltage ($\boldsymbol{v_{odi*}}$ and $\boldsymbol{v_{oqi*}}$) for voltage control loop [12].

$$\dot{\Delta P} = -\omega_{ci}\Delta P_i + \omega_{ci}\left(I_{od}\Delta v_{od} + I_{oq}\Delta v_{oq} + V_{od}\Delta i_{od} + V_{oq}\Delta i_{oq}\right) \tag{27}$$

$$\dot{\Delta Q} = -\omega_{ci}\Delta Q_i + \omega_{ci}\left(I_{oq}\Delta v_{od} - I_{od}\Delta v_{oq} - V_{oq}\Delta i_{od} + V_{od}\Delta i_{oq}\right) \tag{28}$$

where I_{od}, I_{oq}, V_{od} and V_{oq} represent steady state values of i_{od}, i_{oq}, v_{od}, v_{oq} as in Figure 2c,d. ω_{ci} is the cut-off frequency for low pass filters employed in the power calculator.

Small signal model of frequency and voltage control are given by (29) and (30):

$$\left.\begin{array}{c} \Delta\omega = -m_p \cdot \Delta P \\ \Delta v^*_{od} = -n_q \cdot \Delta Q \\ \Delta v^*_{oq} = 0 \end{array}\right\} \tag{29}$$

$$\dot{\Delta\delta} = \Delta\omega - \Delta\omega_{com} = -m_p \cdot \Delta P - \Delta\omega_{com} \tag{30}$$

6.3. Grid-Side Filter Model

The small signal model for the LC output filter can be given by Equations (31)–(36):

$$\dot{\Delta i_{ldi}} = -\frac{R_{fi}}{L_{fi}} \cdot \Delta i_{ldi} + \omega_i \cdot \Delta i_{lqi} + \frac{1}{Lfi} \cdot \Delta v_{idi} - \frac{1}{Lfi} \cdot \Delta v_{odi} + I_{lq} \cdot \Delta\omega \tag{31}$$

$$\dot{\Delta i_{lqi}} = -\frac{R_{fi}}{L_{fi}} \cdot \Delta i_{lqi} - \omega_i \cdot \Delta i_{ldi} + \frac{1}{Lfi} \cdot \Delta v_{iqi} - \frac{1}{Lfi} \cdot \Delta v_{oqi} + \cdot\Delta\omega \tag{32}$$

$$\dot{\Delta v_{odi}} = \omega_i \cdot \Delta v_{oqi} + \frac{1}{Cfi} \cdot \Delta i_{ldi} - \frac{1}{Cfi} \cdot \Delta i_{odi} + V_{oq} \cdot \Delta\omega \tag{33}$$

$$\dot{\Delta v_{oqi}} = \omega_i \cdot \Delta v_{odi} + \frac{1}{Cfi} \cdot \Delta i_{lqi} - \frac{1}{Cfi} \cdot \Delta i_{oqi} - V_{od} \cdot \Delta\omega \tag{34}$$

$$\dot{\Delta i_{odi}} = -\frac{R_{ci}}{L_{ci}} \cdot \Delta i_{odi} + \omega_i \cdot \Delta i_{oqi} + \frac{1}{L_{ci}} \cdot \Delta v_{odi} - \frac{1}{L_{ci}} \cdot \Delta v_{bdi} + I_{oq} \cdot \Delta\omega \tag{35}$$

$$\Delta \dot{i}_{oqi} = -\frac{R_{ci}}{L_{ci}} \cdot \Delta i_{oqi} - \omega_i \cdot \Delta i_{odi} + \frac{1}{L_{ci}} \cdot \Delta v_{oqi} - \frac{1}{L_{ci}} \cdot \Delta v_{bqi} - I_{od} \cdot \Delta\omega \tag{36}$$

The input and output parameters as shown in Figure 2d are transformed to the common reference frame using transformation matrix T_γ as in Equations (37) and (38):

$$[\Delta i_o DQ] = [T_\gamma] \cdot \left[i_{odq} \right] = \begin{bmatrix} \cos(\delta) & -\sin(\delta) \\ \sin(\delta) & \cos(\delta) \end{bmatrix} \cdot \left[\Delta i_{odq} \right] + \begin{bmatrix} -I_{od}\cos(\delta) & -I_{oq}\sin(\delta) \\ I_{od}\sin(\delta) & -I_{oq}\cos(\delta) \end{bmatrix} [\Delta\delta] \tag{37}$$

$$\left[\Delta u_{bdq} \right] = \left[T_\gamma{}^{-1} \right] \cdot [u_{bDQ}] = \begin{bmatrix} \cos(\delta) & \sin(\delta) \\ -\sin(\delta) & \cos(\delta) \end{bmatrix} \cdot [\Delta v_{bDQ}] + \begin{bmatrix} -U_{bD}\sin(\delta) & -U_{bQ}\cos(\delta) \\ -U_{bD}\cos(\delta) & -U_{bQ}\sin(\delta) \end{bmatrix} [\Delta\delta] \tag{38}$$

6.4. Small Signal Model of the i^{th} Inverter

The components described in previous sections can be combined to arrive at a small signal model of i^{th} distributed generation unit. This model can be written in suitable form as:

$$\left[\Delta \dot{x}_{invi} \right] = A_{invi} \cdot [\Delta x_{invi}] + B_{invi} \cdot \left[\Delta u_{bDQi} \right] + B_{iWcom} \cdot [\Delta w_{com}] \tag{39}$$

$$\begin{bmatrix} \Delta w_i \\ \Delta i_{oDQi} \end{bmatrix} = \begin{bmatrix} C_{invwi} \\ C_{invci} \end{bmatrix} \cdot [\Delta x_{invi}] \tag{40}$$

where the state vector is

$$[\Delta x_{inv}] = \begin{bmatrix} \Delta\delta_i \; \Delta P_i \; \Delta Q_i \; \Delta\phi_{di} \; \Delta\phi_{qi} \; \Delta\varsigma_{di} \; \Delta\varsigma_{qi} \; \Delta i_{ldi} \; \Delta i_{lqi} \\ \Delta v_{odi} \; \Delta v_{oqi} \; \Delta i_{odi} \; \Delta i_{oqi} \end{bmatrix}^T \tag{41}$$

The matrices A_{invi}, B_{invi}, B_{iwcom}, C_{inwi}, C_{invci} depend on component values and may be calculated as shown in appendices.

6.5. Combined Model of N Inverters

A combined model for power converters paralleled through the microgrid network is presented as in Equations (42)–(47):

$$\left.\begin{array}{c} [\Delta x_{inv}] = A_{inv} \cdot [\Delta x_{inv}] + B_{inv} \cdot \left[\Delta v_{bDQ} \right] \\ \left[\Delta i_{oDQ} \right] = C_{invc} \cdot \left[\Delta x_{inv} \right] \end{array}\right\} \tag{42}$$

$$[\Delta x_{inv}] = [\Delta x_{inv1} \; \Delta x_{inv2} \ldots \; \Delta x_{invN}]^T \tag{43}$$

$$A_{inv} = \begin{bmatrix} A_{inv1} + B_{1wcom}C_{invw1} & 0 & 0 & 0 \\ 0 & A_{inv2} + B_{2wcom}C_{invw2} & 0 & 0 \\ 0 & 0 & . & 0 \\ 0 & 0 & 0 & A_{invN} + B_{Nwcom}C_{invwN} \end{bmatrix} \tag{44}$$

$$B_{inv} = \begin{bmatrix} B_{inv1} \\ B_{inv2} \\ . \\ B_{invN} \end{bmatrix} \tag{45}$$

$$\left[\Delta v_{bDQ} \right] = \left[\Delta v_{bDQ1} \; \Delta v_{bDQ2} \ldots \Delta v_{bDQN} \right]^T \tag{46}$$

$$C_{inv} = \begin{bmatrix} [C_{invc1}] & 0 & 0 & 0 \\ 0 & [C_{invc2}] & 0 & 0 \\ 0 & 0 & . & 0 \\ 0 & 0 & 0 & [C_{invcN}] \end{bmatrix} \tag{47}$$

6.6. Load and Network Model

A combined model for load and network, derived through Kirchhoff voltage and current laws, can be expressed in terms of line currents and node voltages as in (48) and (49):

$$[\Delta \dot{i}_{lineDQ}] = A_{NET}[\Delta i_{lineDQ}] + B_{1NET}[\Delta u_{bDQ}] + B_{2NET} \cdot \Delta\omega \tag{48}$$

$$[\Delta \dot{i}_{loadDQ}] = A_{LOAD}[\Delta i_{loadDQ}] + B_{1LOAD}[\Delta u_{bDQ}] + B_{2LOAD} \cdot \Delta\omega \tag{49}$$

where, A_{NET}, B_{1NET}, B_{2NET} and A_{LOAD}, B_{1LOAD}, B_{2LOAD} are network and load matrices, respectively, given in Appendix A.

6.7. Micro Grid Model

Finally, we can combine above described component models to express a small signal model for the complete microgrid system (50)–(55). The system used here is composed of s = 6 DGUs, n = 6 lines, p = 5 loads, m = 7 nodes. MATLAB Simulink, and Linear analysis tools (R2018a, product registered to SJTU, Shanghai, China) have been used to analyze this complex system by perturbing dynamical equations of the same.

$$[\Delta v_{bDQ}] = R_N\left(M_{inv}[\Delta i_{oDQ}] + M_{Load}\left[\Delta \dot{i}_{loadDQ}\right] + M_{net}[\Delta \dot{i}_{lineDQ}]\right) \tag{50}$$

$$R_N = \begin{bmatrix} r_N & & \\ & \ddots & \\ & & r_N \end{bmatrix}_{2m \times 2n} \tag{51}$$

$$M_{Load} = \begin{bmatrix} -1 & & \\ & \ddots & \\ & & -1 \end{bmatrix}_{2m \times 2p} \tag{52}$$

$$M_{net} = \begin{bmatrix} -1 & & & \\ 0 & -1 & & \\ 1 & 0 & -1 & \\ & 1 & 0 & -1 \\ & & 1 & 0 \\ & & & 1 \end{bmatrix}_{2m \times 2n} \tag{53}$$

$$M_{inv} = \begin{bmatrix} 1 & & & \\ & 1 & & \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ & & 1 & \\ & & & 1 \end{bmatrix}_{2m \times 2s} \tag{54}$$

$$\begin{bmatrix} \Delta \dot{x}_{inv} \\ \Delta \dot{i}_{lineDQ} \\ \Delta \dot{i}_{loadDQ} \end{bmatrix} = A_{MG} \begin{bmatrix} \Delta x_{inv} \\ \Delta i_{lineDQ} \\ \Delta i_{loadDQ} \end{bmatrix} \tag{55}$$

where, (53) represents the complete small signal model of the MG system used in this study. The system matrix A_{MG} is provided in the appendices.

7. Stability and Sensitivity Analysis

The small signal model of the MG given by Equations (48)–(53) is utilized to plot eigen values of the system under varying control and system parameters. Eigen values or modes are solutions to characteristic equation of the system's linearized state matrix. Sensitivity of the system states to changes in system parameters can be determined by analyzing the system state matrix $A_{MG.}$ A sensitivity factor rp_{ki} gives the measure of association between different state variables and their participation in modes [36,39]. Sensitivity, rp_{ki} of an eigen value λ_i, in relation to the corresponding diagonal element of state matrix a_{kk}, can be given by (56):

$$rp_{ki} = \frac{\partial \lambda_i}{\partial a_{kk}} \tag{56}$$

Eigen evolution traces are plotted to perform stability and sensitivity analyses, ascertain limits for the test MG network under the proposed control scheme. The droop gains of all inverters as well as multiagent consensus gains have been perturbed to arrive at operational limits of the system as given in Table 4. Eigen traces given in Figure 4a–d demonstrate system behavior under varying control gains. Figure 4a shows the movement of eigen values with increase in $\boldsymbol{m_p}$, towards the right half plane. Figure 4b shows the movement of eigen values under influence of increasing proportional consensus gains, (K_{pV}, K_{pf}), towards the right half plane. Figure 4c shows the movement of eigen values under influence of increasing integral consensus gains, (K_{iV}, K_{if}) towards the left half of the plane. Proportional consensus gains (K_{pV}, K_{pf}) tend to force the system towards early convergence, however they push the system stability to its limits. Conversely, integral consensus gains (K_{iV}, K_{if}) tend to stabilize the system. Figure 4d shows the movement of poles under influence of increasing reactive power control gains $\boldsymbol{n_q}$, towards the right half plane. Table 4 gives operational limits of control parameters obtained from the analysis. Overall, the MG system is more sensitive towards variation in reactive power control gains $\boldsymbol{n_q}$ than active power gains $\boldsymbol{m_p}$.

Table 4. Variation range for primary and secondary controller gains.

Sr. No.	Control Parameters		
1.	Droop Gains	Min.	Max.
	m_p	1×10^{-10}	1×10^{-3}
	n_q	1×10^{-7}	1×10^{-3}
2.	Consensus frequency		
	k_{pf}	0.4	2.5
	k_{if}	0.1	0.6
3.	Consensus voltage		
	k_{pV}	0.5	3.5
	k_{iV}	0.1	0.7

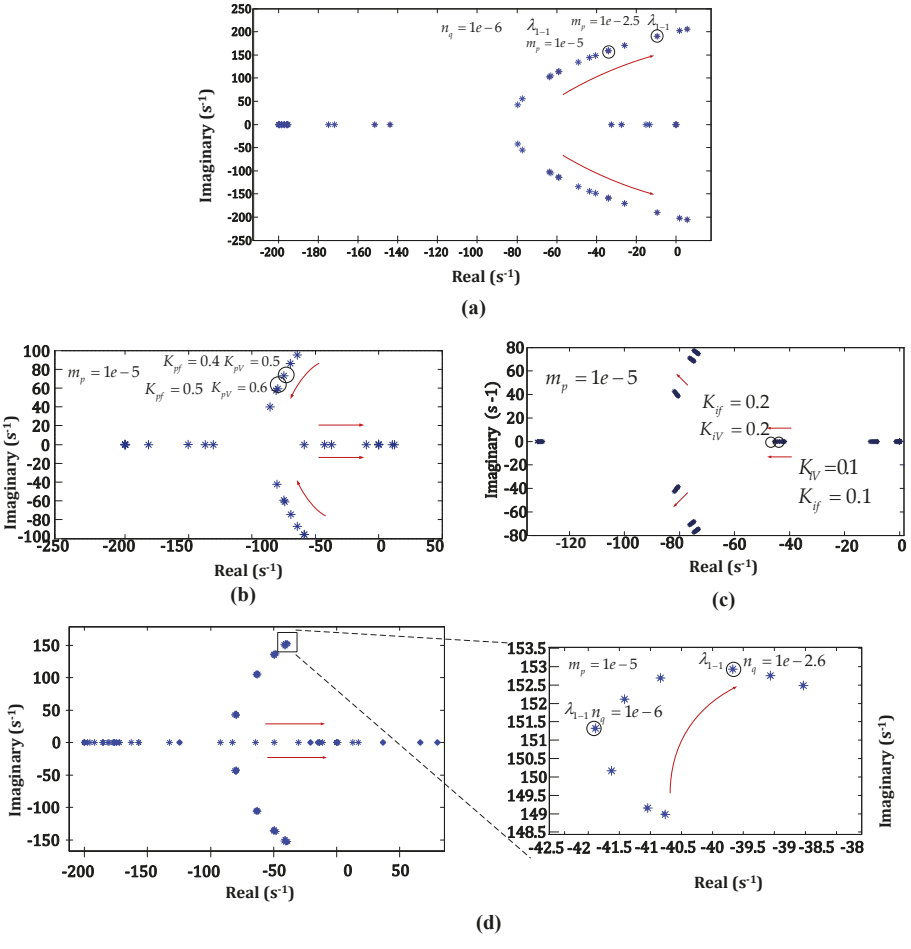


Figure 4. Observing effect of control gain variation on system stability through eigen traces: (**a**) effect of variation in $\mathbf{m_p}$; (**b**) effect of variation in tertiary controller integral gains; (**c**) effect of variation in tertiary controller proportional gains; (**d**) effect of variation in $\mathbf{n_q}$.

8. Evaluation with Case Studies

This section elaborates case study simulations undertaken for scenarios resulting from multiple communication link failures. The proposed algorithm subsequently segments the microgrid network into "virtual sub islands" described as follows. Figure 5a–g gives active power sharing results for each case discussed.

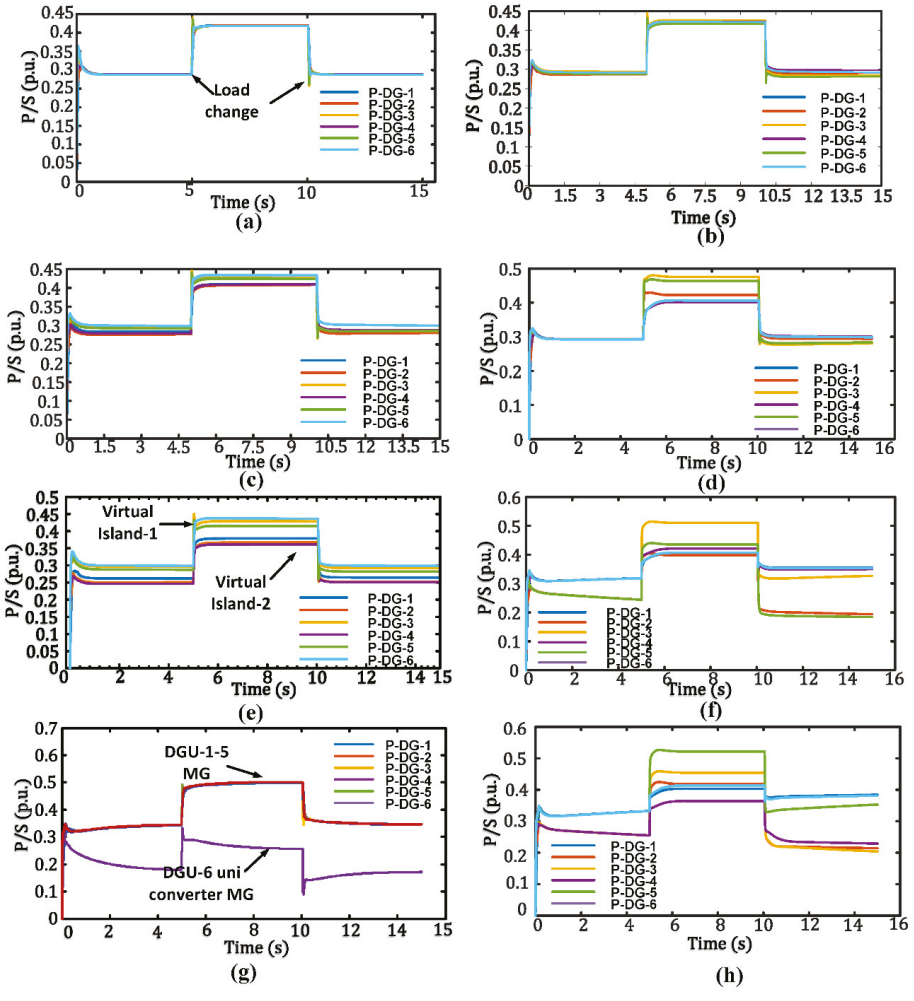


Figure 5. Comparison of active power sharing under proposed control strategy and conventional consensus-based control with varying communication network health: (**a**) Full ring connectivity with proposed control; (**b**) Full ring connectivity with consensus-based control; (**c**) Triple link failure, three sub-islands with proposed control; (**d**) Triple link failure, three sub islands with consensus-based control (**e**) Dual link failure, two sub islands with proposed control (**f**) Dual link failure, two sub islands with conventional consensus-based control (**g**) Dual link failure, two asymmetrical sub islands with proposed control (**h**) Dual link failure, two asymmetrical sub islands with consensus-based control.

8.1. Case-1: Full Ring Sparse Connected Communication Network

In the first scenario considered, the communication network between nodes forms a complete ring digraph as represented in Figure 3a. All nodes receive information from neighboring nodes and, as such, no communication islands are formed. All converter nodes converge to proportional values of active power injection as seen in Figure 5a.

8.2. Case-2: Two Sub Groups with Equal Number of Members

This scenario is based on multiple link failures leading to the segmentation of the microgrid communication network into two virtual islands of approximately equal size. The DGUs 1 through 3 form one communication sub-island whereas DGUs 4 through 6 form another sub-island as shown in Figure 3b. Subsequently, with the aid of proposed controls, active power injected by all nodes falls within two subgroups as can be seen Figure 5c, whereas, in absence thereof, the injected powers diverge, as seen in Figure 5e.

8.3. Case-3: Three or More Sub Groups with Equal Number of Members

This considers a scenario where communication link failures divide the microgrid information network into three or more virtual sub-islands approximately equal in size viz the number of nodes in each. Accordingly, DGUs 1 and 2, 3 and 4, 5 and 6, form three virtual sub islands as shown in Figure 3c. The control algorithms within each sub-island drive the system to achieve proportional power sharing as shown in Figure 5e. Conversely, Figure 5c shows an imbalance in injected active powers when the proposed tertiary controls are absent.

8.4. Case-4: Two Sub Groups with Un-Equal Number of Members

This scenario considers an event wherein one node becomes completely isolated from the other nodes due to multiple communication link failures. The DGUs 1 through 5 correspond to one virtual sub-island. Whereas, the DGU-6 is isolated as an individual converter sub-island as shown in Figure 3d. The results obtained for this can be seen in Figure 5g. It may be observed that tertiary controls enable the power injected to fall within two subgroups accordingly, whereas, in absence thereof, the injected powers diverge.

8.5. Comparison with Previous Conventional Control Strategies

Figure 5 compares the simulation study results obtained for the proposed control strategy with results of conventional consensus-based control and distributed estimation-based methods. The left half of the figure (Figure 5: (a) (c) (e) (g)) shows the results for the proposed method, whereas, those on the right (Figure 5: (b) (d) (f) (h)) are the results of consensus-based control. It can be observed that for all cases presented, the proposed method shows better convergence than previously existing control schemes. Figure 6a,b present results for frequency and voltage restoration with the proposed control strategy, whereas, subfigures (c) and (d) present results of frequency and voltage restoration with consensus-based control under faulted communication links. Table 5 compares the proposed strategy with conventional methods previously discussed under similar testing circumstances following respective details presented. The proposed method shows early convergence under a given condition as compared with others with lesser active power mismatch between DGUs.

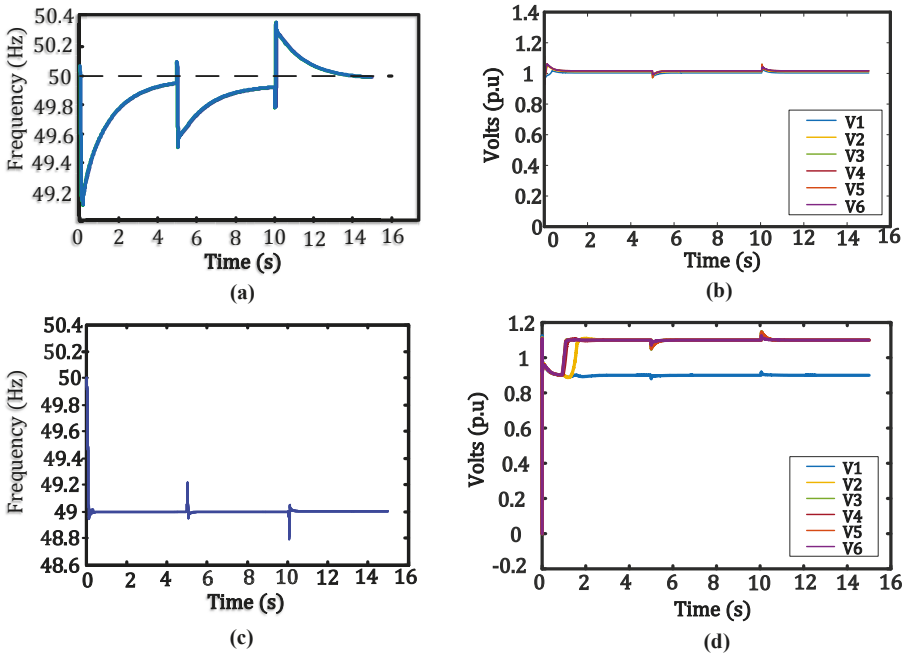


Figure 6. System performance under communication failures: (**a**) Frequency restoration with the proposed control strategy; (**b**) Voltage restoration with the proposed control strategy; (**c**) Frequency restoration with consensus-based control; (**d**) Voltage restoration with consensus-based control.

Table 5. Comparison of the proposed control strategy with existing conventional Strategies.

Sr. No.	Parameters	Proposed Method	Distributed Estimation-Based Methods [22,25,26]	Consensus-Based Methods [12,20,21,23]
1.	Maximum Active power mismatch	0.03 p.u.	0.05 p.u.	0.10 p.u.
2.	Max Voltage variation	0.01 p.u.	0.1 p.u.	0.2 p.u.
3.	Max frequency variation	0.4 Hz (4.0×10^{-5} Hz/VA)	0.2 Hz (2.0×10^{-5} Hz/VA)	1 Hz (1.0×10^{-5} Hz/VA)
4.	Convergence time (frequency)	4 s	10 s	No convergence if links severed
5.	Convergence time (voltage)	1 s	7 s	No convergence if links severed

9. Conclusions

A hierarchical multiagent consensus-based control strategy is proposed to address the coupled objectives of power balancing between generation sources, voltage and frequency restoration in islanded AC microgrids. A sparse communication network spans alongside a system distribution network and provides media for communication of estimated values and corrective signals. The proposed method mitigates system instability and power sharing imbalances when the supervisory communication network is experiencing link failures. The nodes lying inside connected communication neighborhoods form virtual "sub-islands", wherein, power sharing, voltage and frequency regulation

control function with reference to locally available information. To verify the effectiveness of the proposed strategy, mathematical small signal models of individual components are stitched together to form an MG system model. These models are then used to analyze the performance of the said controls using eigen plots with regards to system stability and sensitivity towards variation in control parameters. Case simulation studies for different communication scenarios are undertaken. The two kinds of analyses adopted verify the effectiveness of the proposed control strategy for the given scenarios.

Author Contributions: K.H., M.U.S. and M.M.K. have contributed to the conceptualization behind this work. K.H. has prepared the write up and manuscript. M.U.S. has prepared the algorithms used in this paper, whereas, M.M.K. has helped with small signal modelling and validation. S.H. has helped with the write up, sectionalizing and appropriate referencing. H.J. and M.T.F. have helped with the software and experimental verification. This work had been jointly supervised by M.M.K. and H.T.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A. System Matrices

$$A_{MG} = \begin{bmatrix} A_{inv} + B_{inv}R_N M_{inv} C_{invC} & B_{inv}R_N M_{net} & B_{inv}R_N M_{Load} \\ B_{1net}R_N M_{inv} C_{invC} + B_{2net} C_{inv.\omega} & A_{net} + B_{1net}R_N M_{net} & B_{1Net}R_N M_{Load} \\ B_{1Load}R_N M_{inv} C_{invC} + B_{2Load} C_{inv.\omega} & B_{1Load}R_N M_{net} & A_{Load} + B_{1Load}R_N M_{Load} \end{bmatrix}$$

$$A_{Invi} = \begin{bmatrix} A_{Pi} & 0 & 0 & B_{Pi} \\ B_{V1i}C_{Pvi} & 0 & 0 & B_{V2i} \\ B_{C1i}D_{V1i}C_{Pvi} & B_{C1i}C_{Vi} & 0 & B_{C1i}D_{V2i} + B_{C2i} \\ B_{LCL1i}D_{C1i}D_{V1i}C_{Pvi} + B_{LCL2i}[T_{Vi}^{-1}00] & B_{LCLIi}D_{CIi}C_{Vi} & B_{LCLi}C_{Ci} & A_{LCLi} + B_{LCLIi}(D_{C1i}D_{V2i} + D_{C2i}) \\ B_{LCL3i}C_{Pwi} & & & \end{bmatrix}_{13\times 13}$$

$$A_{net} = \begin{bmatrix} \frac{-R_{line1}}{L_{line1}} & \omega_0 & 0 & 0 & 0 & 0 \\ -\omega_0 & \frac{-R_{line1}}{L_{line1}} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-R_{line2}}{L_{line2}} & \omega_0 & 0 & 0 \\ 0 & 0 & -\omega_0 & \frac{-R_{line2}}{L_{line2}} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-R_{lineN}}{L_{lineN}} & \omega_0 \\ 0 & 0 & 0 & 0 & -\omega_0 & \frac{-R_{lineN}}{L_{lineN}} \end{bmatrix}$$

$$A_{load} = \begin{bmatrix} \frac{-R_{load1}}{L_{load1}} & \omega_0 & 0 & 0 & 0 & 0 \\ -\omega_0 & \frac{-R_{load1}}{L_{load1}} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-R_{load2}}{L_{load2}} & \omega_0 & 0 & 0 \\ 0 & 0 & -\omega_0 & \frac{-R_{load2}}{L_{load2}} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-R_{loadN}}{L_{loadN}} & \omega_0 \\ 0 & 0 & 0 & 0 & -\omega_0 & \frac{-R_{loadN}}{L_{loadN}} \end{bmatrix}$$

$$B_{1net} = \begin{bmatrix} \frac{1}{L_{line1}} & & -\frac{1}{L_{line1}} & & & & & \\ & \frac{1}{L_{line1}} & & -\frac{1}{L_{line1}} & & & & \\ & & & & \ddots & & & \\ & & & & & \frac{1}{L_{lineN}} & & -\frac{1}{L_{lineN}} \\ & & & & & & \frac{1}{L_{lineN}} & & -\frac{1}{L_{lineN}} \end{bmatrix}$$

$$B_{1LOAD} = \begin{bmatrix} \frac{1}{L_{load1}} & & -\frac{1}{L_{load1}} & & & & & & \\ & \frac{1}{L_{load1}} & & -\frac{1}{L_{load1}} & & & & & \\ & & & & \ddots & & & & \\ & & & & & \frac{1}{L_{loadN}} & & -\frac{1}{L_{loadN}} & \\ & & & & & & \frac{1}{L_{loadN}} & & -\frac{1}{L_{loadN}} \end{bmatrix}$$

$$B_{INVi} = \begin{bmatrix} 0 & 0 & 0 & B_{LCL2}T_s^{-1} \end{bmatrix}^T_{2\times 13}$$

$$B_{iwcom} = \begin{bmatrix} B_{Pwcom} & 0 & 0 & 0 \end{bmatrix}^T_{13\times 1}$$

$$C_{INVwi} = \left\{ \begin{array}{c} \begin{bmatrix} C_{pw} & 0 & 0 & 0 \end{bmatrix}_{1\times 13} \; i = 1 \\ \hline \begin{bmatrix} 0 & 0 & 0 & 0 \end{bmatrix}_{1\times 13} \; i \neq 1 \end{array} \right\}$$

$$C_{INVci} = \begin{bmatrix} [T_C \quad 0 \quad 0] & 0 & 0 & [0 \quad 0 \quad T_S] \end{bmatrix}_{2\times 13}$$

where all entries of the matrices A_{MG}, A_{invi}, B_{invi}, B_{iwcom}, C_{INVwi}, C_{INVci} represent sub-matrices describing the system obtained from (5)–(40) after mathematical manipulations.

Appendix B. Algorithm

Algorithm 1: Depth First Search for Graph $G = \{A(v)|v \in V\}$, where $A(v)$ adjacency list for V

Initiate: A graph $G(V, E)$ repressing comm. network topology for the Micro Grid.
Check: the connectivity using DFS and generate look up table.
BEGIN
Integer i;
Routine $DFS(v, u)$; Comment vertex u is the parent vertex for v vertex in the spanning tree constructed
BEGIN
NUMBER (V): = i := $i + 1$;
FOR w is the adjacency list if v DO
BEGIN
IF w is not yet numbered THEN
BEGIN
Construct arc $v \rightarrow w$ in P;
$DFS(w, v)$;
END
ELSE IF NUMBER (w) < NUMBER (v) and $w = u$
THEN construct arc $v- \rightarrow w$ in p;
END;
END;
i := 0;
$DFS(s, 0)$;
END;

Appendix C.

Appendix C.1. Adjacency Matrix

$$A_g = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 1 & 0 \end{bmatrix}$$

Appendix C.2. Degree Matrix

$$D_g = \begin{bmatrix} 2 & 0 & 0 & 0 & 0 & 0 \\ 0 & 2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 2 & 0 \\ 0 & 0 & 0 & 0 & 0 & 2 \end{bmatrix}$$

Appendix C.3. Laplacian Matrix

$$L_g = \begin{bmatrix} 2 & -1 & 0 & 0 & 0 & -1 \\ -1 & 2 & -1 & 0 & 0 & 0 \\ 0 & -1 & 2 & -1 & 0 & 0 \\ 0 & 0 & -1 & 2 & -1 & 0 \\ 0 & 0 & 0 & -1 & 2 & -1 \\ -1 & 0 & 0 & 0 & -1 & 0 \end{bmatrix}$$

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A Control Methodology for Load Sharing System Restoration in Islanded DC Micro Grid with Faulty Communication Links

Muhammad Umair Shahid [1,*], Muhammad Mansoor Khan [1], Khurram Hashmi [1], Salman Habib [1], Huawei Jiang [2] and Houjun Tang [1]

[1] School of Electronics, Information & Electrical Engineering (SEIEE), Smart Grid Research & Development Centre, Shanghai Jiao Tong University, Shanghai 200240, China; mkhancn@yahoo.com (M.M.K.); khurram_hashmi@sjtu.edu.cn (K.H.); iamsuliman@hotmail.com (S.H.); hjtang@sjtu.edu.cn (H.T.)

[2] State Grid Wuxi Power Supply Company, Wuxi 214000, China; jiang.huawei93@outlook.com

* Correspondence: MuhammadUmairShahid@sjtu.edu.cn; Tel.: +86-132-6290-7356

Received: 4 April 2018; Accepted: 31 May 2018; Published: 4 June 2018

Abstract: Communication-based distributed secondary control is extensively used in DC microgrids. Compared to centralized control, it can provide better voltage regulation and load sharing in microgrids. A conventional secondary control technique that converges the system to a common operating point is improved by using the control methodology to detect the communication link failure and stabilize the system operation during communication islanding. Recently, more robust control schemes have been proposed to improve resilience, but communication islanding has not been addressed at the secondary level control for which the system requires additional tertiary control. However, link failure is a possibility in the microgrid, so this paper proposes a control scheme at the secondary level to detect communication islanding. Communication islanding may lead the system to unpredictable behavior, which may cause the system to become unstable and may further lead to a cascading failure. The proposed control scheme sustains the stability and operation of a DC microgrid. Voltage and current observer works in a parallel manner with the proposed secondary control to achieve a correction term for global operating points. The proposed control scheme has been verified through analysis and simulation.

Keywords: DC–DC converters; multi-level control; renewable energy resources control; electrical engineering communications

1. Introduction

Microgrids are small-scale isolated distribution systems which are currently receiving increased attention due to the widespread use of renewable energy resources, energy storage batteries, and the increment of electronics-based loads that use DC current. Therefore, DC microgrids avoid cumbersome DC–AC–DC generation [1–4]. However, the usage of DC microgrids at distribution scale is increasing with the collaboration of various renewable resources due to the higher penetration of electric vehicles [5–7]. DC microgrids reduce the number of conversion units and also overcome the disadvantages of AC power, such as transformers inrush current, phase angle, frequency synchronization, reactive power, and power quality [3,8,9]. Although DC microgrids are emerging and inverter-based AC microgrids are the recent focus of research, many traditional AC loads appear in the system as DC loads when fed through inverter drive systems [8]. When studying the conventional control hierarchy for a legacy power system grid, a hierarchical control system is conventionally adopted for microgrids [10–12]. Multi-level hierarchical control is a tertiary control, which is responsible for the coordination between distributed generated units and the economic

dispatch of the units. Tertiary control adjusts the microgrid voltage for the scheduled exchange of power between the microgrid and the main grid. It adjusts the load sharing and maximum power-sharing, which increases the utilization of renewable energy, suppresses stress, and affects the aging of the microgrids [13–15]. To adjust the voltage set point of the primary controller by the tertiary and secondary controller, a primary controller is implemented locally with the droop mechanism to converge the voltage of the converters [12]. Tertiary and secondary control systems are implemented in a centralized mode in such a way that they are connected with high-speed communication networks. Communication networks used to exchange the reference values for the primary control, and any link failure of the network system may lead the affected unit to malfunction, overstressing other units, and potentially leading the system towards instability and failure [13]. A future extension for link failure in the controllability adds more complexity to the central controller. Distributed control is as an alternative to centralized systems which provides more reliability, easy scalability, and a simpler network for communication [16,17]. Structurally, it is desired to extend the distributed control in secondary and primary control levels; this control provides voltage regulation and better load sharing for DC microgrids [15].

Better load sharing is implemented using communication between converters that assign the loads according to their rated power, which equalizes the per-unit current of all nodes and reduces circulating current and overstressing of all sources [18,19]. Droop control is primarily adopted for load sharing by adding a virtual resistance to every converter. Despite the ease and simplicity in a droop control, it suffers from poor voltage regulation and current sharing. The main reason for this is the virtual impedance and output voltage mismatch between converters, which affects the real power flow between DC power systems [20–22]. Improvement in systems requires a secondary control system that has better voltage regulation and load sharing, which is done over a communication network. Secondary control may be a centralized system exchanging values over a fully connected communication network through directly connected nodes of the microgrid [15,22]. A centralized secondary control measure voltage of the microgrid calculates the restoration value of voltage for the microgrid and feeds the same value to every converter. It assumes that the voltage of every converter is the same for all the nodes in a microgrid, which is not a feasible assumption for a DC microgrid [19].

The conventional DC droop technique is used to linearly reduce the DC output voltage such that current increases, and it has limitations in line resistance in a droop control and DC bus voltage deviation increases. Droop control helps to achieve the independent operation of converters and improves current sharing [13]. The cooperative control of DC microgrids creates a distributed secondary and primary control paradigm. Secondary control adjusts set-points for the overall system, and the primary control regulates individual units employing droop control law. The controller controls the transmission line impedance and communicates with other converters in the form of a sparse technique for current sharing [14]. Using a distributed network, consensus protocol is implemented which eliminates the need for master–slave topology. Voltage regulation at a fixed point and current in per-unit are used in consensus to share the current between nodes. This involves tertiary, secondary, and primary controls. Tertiary controls the power dispatch, secondary sets the point for operation, and primary is a droop control. The controller does not require any prior knowledge of the number of converters, which makes it plug-and-play system [12]. The droop method is widely used for current or load sharing by using the virtual impedance of each converter, which prevents power sources from becoming overstressed [15]. A high droop coefficient improves the load sharing, which results in a cost for degrading voltage regulation. To achieve the required load sharing, the droop coefficient varies in the range of line impedance and line variation [16]. The communication network spans all over the microgrid for centralized control which is embedded in each converter. Node-to-node communication links are required for all sources, and any link failure makes the microgrid operation unstable. The effect of line impedance is also taken into account for the connected graph [20]. Despite improved accuracy because of the fully connected network system, any individual link failure affects the system performance. Appropriately, it is required that the average voltage over the microgrid is

directed at the global voltage set point controlled by the tertiary control, which is called global voltage regulation [21,23]. The efficiency of DC microgrids varies because of the effect of communication delays generated between the nodes to exchange values. This can cause system instability and response to load sharing of nodes [24–26]. In a bi-directional connectivity graph system, when a large amount of data is exchanged, errors in communication may occur that result in deterioration of the system performance [27,28]. Due to the intermittent nature of renewable energy resources, a fast control scheme is required [26]. A new control scheme at the secondary level is proposed with minimum data exchange to overcome the mismatch in operating reference points to in turn reduce the stress and stabilize the system. The proposed control scheme can detect communication link failure and reliable operation of the system by varying the gain for correction terms. The proposed scheme does not require the tertiary-level control which is usually used in conventional consensus-based communication control.

This paper focuses on the improvement of the secondary-level control of DC microgrids. The main features of the proposed distributed cooperative control are as follows:

1. Analysis of two-way cooperation in nodes through a communication graph by making improvements in secondary control, which can detect communication link failure and stabilize the system accordingly.
2. Each converter has a level of intelligence, which uses the proposed scheme to get correction terms and adjust the system more accurately.
3. The proposed control system does not require prior knowledge of the nodes, which gives it plug-and-play capability.
4. A sparse communication network is spanned throughout the microgrid, through which converters can communicate with their neighbors, which is completely different from the centralized control approach.

This manuscript is organized as follows: Section 2 is related to the detection of communication islanding and its impact on the system. An introduction to graph theory is presented in Section 3. Section 4 demonstrates the proposed distributed control. Section 5 presents the case studies and simulation. Finally, the conclusions of the paper are drawn in Section 6.

2. Detection of Communication Islanding and Impact

After link failure, small islands form in the DC microgrid network. The proposed scheme uses a bi-directional sparse network in which every node is connected to its neighboring nodes, as in Figure 1. In normal operation, consensus control will converge the system on global reference points. In case of communication link failure, the proposed secondary control detects and shifts the system control to primary control of the disconnected node, which overcomes the need for tertiary Control. Conventional consensus-based communication control systems use tertiary control in the case of link failure. The advantage of shifting the system to primary control is that it operates on a fixed reference value, without being unstable or generating any stress on the microgrid system. As shown in Figure 2, secondary-level control is modified to detect link failure on the basis of the values which are received from neighbors. If any value is missing or not received, a link failure is detected and the system is shifted to primary control. Otherwise, tertiary control is needed to overtake control of the system in order to remain stable. The flowchart in Figure 3 elaborates this operation. The proposed control method is modified with a logical switch, which removes the requirement for tertiary control by controlling the gain of the correction term on the secondary control of the disconnected node. Proposed Switch technique varies the gain on detecting, as an example if one side communication link failure gain becomes half or both side communication failure then gain becomes zero. The system remains stable and will not generate stress on the disconnected node.

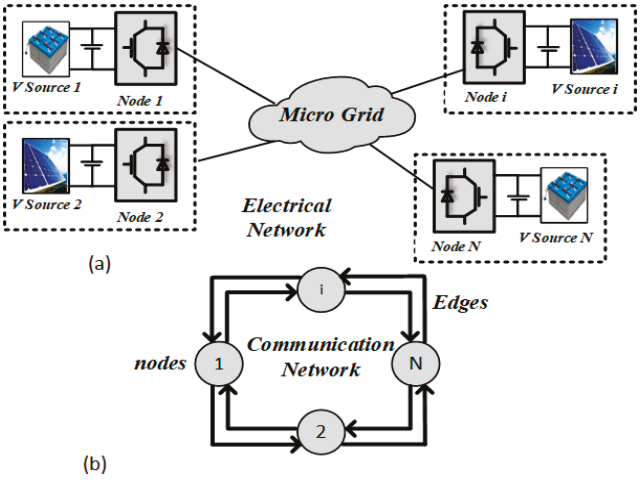

Figure 1. General layout of a micro-grid: (**a**) Power-supplying nodes; (**b**) Communication network spanned among nodes for data exchange.

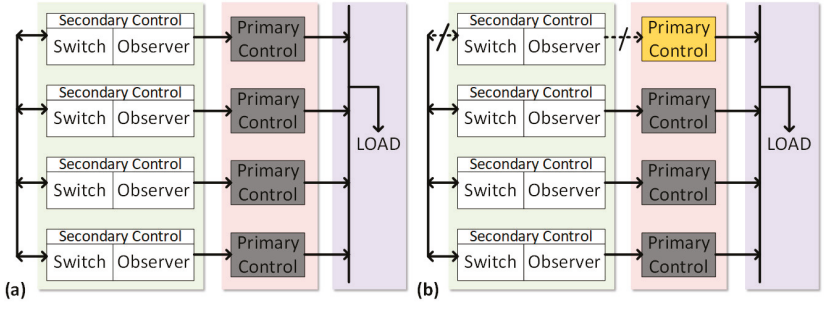

Figure 2. DC micro-grid (MG): (**a**) Regular 4-node DC MG; (**b**) Communication fault 4-node DC MG.

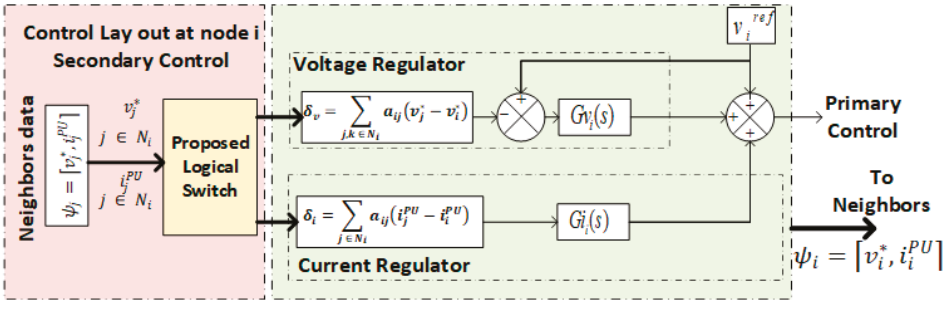

Figure 3. Proposed secondary control for a DC microgrid.

3. Review of Graph Theory

A DC microgrid (MG) system can be represented using graph theory in the form of a graph. The requirement for representing a DC MG using graph theory arises due to the increased number of nodes. So, irrespective of the communication method, the information transfer from one node

to another can be expressed graphically. Graph theory is a well-established field of mathematics which helps to study different scenarios and cases in DC MG systems for the exchange of information flow [27].

A distributed cooperative control can be represented graphically. Figure 1 shows the physical and cyber layers of the DC microgrid. Nodes represent the active sources and edges show the communication links between the nodes. The cyber layer lays the network to achieve global consensus by exchanging information with neighbors, which is an improvement upon conventional consensus systems. By exchanging values with neighbors, every agent sets its reference values according to neighbors information [28]. Thus, cooperative control offers a global consensus, provided with the help of the communication network. So, communication link failure affects the system stability in achieving convergence and generates stress on nodes [12,29].

A bi-directional communication network as in Figure 1b can be represented using graph theory. Such a graph is usually represented mathematically as a set of nodes $V_G = \left[V_1^g, V_2^g, V_3^g \ldots\ldots..V_N^g\right]$ connected through the edges $E_G \subset V_G \times V_G$. This set consists of elements such as $i, j = 1, 2, 3, \ldots\ldots..n$ and $i \neq j$. When an edge exists between nodes v_i and v_j, it is called adjacent and the system creates an adjacent matrix $A_G = |a_{ij}| \in R^{N \times N}$, where N is the number of active source nodes. Adjacency matrix A_G consists of the communication weights, where $a_{ij} > 0$, if $\left(v_j^g, v_i^g\right) \in E_G$ and $a_{ij} = 0$, otherwise. a_{ij} is the coefficient of communication for transferring data from node j to node i. Here the adjacency matrix is considered with a time-invariant function. $N_i = \left\{j \middle| \left(v_j^g, v_i^g\right) \in E_G\right\}$ denotes a set of all neighbors of point i; that is, if $i, j \in N_i$, then v_i^g receives the information from v_j^g. The degree matrix consists of an in-degree matrix and an out-degree matrix. The in-degree matrix $D_G^{in} = diag\left\{d_i^{in}\right\}$ is a diagonal matrix, $d_i^{in} = \sum_{j \in N_i} a_{ji}$. Similarly, with the out-degree matrix $D_G^{out} = diag\left\{d_i^{out}\right\}$, $d_i^{out} = \sum_{i \in N_i} a_{ji}$. A Laplacian matrix is defined as $L_G = D_G^{in} - A_G$, whose eigenvalues adjust the global values for the microgrid. The Laplacian matrix is assumed to be balanced if the in-degree and out-degree matrices of every node are the same (i.e., $D_G^{in} = D_G^{out}$). Essentially, the in-degree matrices have a greater effect on the global dynamics of the node, which is influenced by its neighbors. In a practical system, if the graph is undirected (which means all the links are bi-directional), then the Laplacian matrix is balanced [30–32].

4. Proposed Distributed Control

The global dynamics of voltage regulation and load sharing are the primary uses of the secondary control, which requires proper set points in order for every converter to operate. The proposed distributed control technique has the ability to detect link failure and stabilize the system during communication islanding. Communication link failure affects the system's stability and functioning. The proposed control method is modified with a control switch that can detect the communication link failure, which can be on one side or on both sides and shifts the system to primary droop control. In primary control, the system works on droop and remains stable without using any tertiary-level control. The proposed scheme is shown in Figures 3 and 4, where a node receives reference points from neighbors and in the case of failure will stop secondary control and shift to primary control. A flowchart for the proposed control method is also shown in Figure 5, which explains the proposed control method better. When the information received from a neighbor's system converges to a common reference point, it increases cooperation for load sharing and voltage reference points. Common reference points are consistently updated through a voltage regulator and a current regulator. Node reference voltage can be expressed as [32]:

$$v_i^* = v_i^{ref} + \delta v_i + \delta i_i, \tag{1}$$

where v_i^{ref}, δv_i, and δi_i are the global voltage parameters for constant reference voltages, voltage correction term of ith node, and current correction term for ith node, respectively. Reference points are further tuned in Figure 3 using observers (Voltage and Current) on each node. In the case of any mismatch with the node's reference point, correction terms are generated by the voltage

observer δv_i and the current observer δi_i to converge the system for better load sharing and voltage regulation. The proposed controller has a logical switch with a voltage observer and a current observer. The proposed controller detects communication link failure, whereas the voltage observer on node i senses the voltage across the microgrid to compare voltage with the global reference v_i^{ref} and converge the voltage of node i to clear any mismatch between nodes using the PI (Proportional Integral) controller $Gv_i(s)$. A distributed cooperative observer estimates the voltage and current compared with the neighbor's data for the average microgrid reference, as implemented in Figure 2. It uses the dynamic consensus framework to process the neighbors' exchange data with local data and adjust the voltage regulation for the microgrid. Figure 4 explains the main operation of the voltage observer to take global voltage averages. The voltage observer at node i receives the neighbor voltages $v_j^*(j \in N_i)$, which can be written as [13]:

$$v_i^*(t) = v_i(t) + \int_0^t \sum_{j \in N_i} a_{ij}\left(v_j^*(\tau) - v_i^*(\tau)\right)d\tau. \tag{2}$$

Differentiating can be expressed as Equation (2):

$$\dot{v}_i^* = \dot{v}_i + \sum_{j \in N_i} a_{ij}\left(\dot{v}_j^* - \dot{v}_i^*\right) = \dot{v}_i + \sum_{j \in N_i} a_{ij}\dot{v}_j^* - d_i^{in}\,\dot{v}_i^*. \tag{3}$$

Global observer dynamics can be arranged as:

$$\dot{\overline{v}} = \dot{\mathrm{v}} - \left(D_G^{in} - A_G\right)\overline{v} = \dot{\mathrm{v}} - L\overline{v}. \tag{4}$$

The protocol which is used to update the set point for voltage in the voltage observer is referred to as dynamic consensus. As shown in Equation (4), the local set point (i.e., v_i) is directly input into the estimation algorithm. Thus, any change in voltage at node i's local set point quickly responds to the situation. As a result, the new v_i^* is set in the local system and also sent to the neighbors for the reference of other nodes [33].

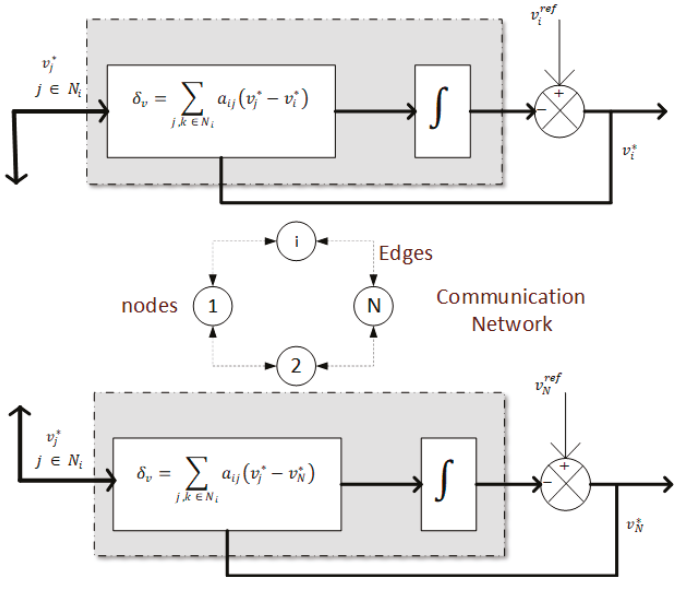

Figure 4. Voltage observer in the proposed secondary control.

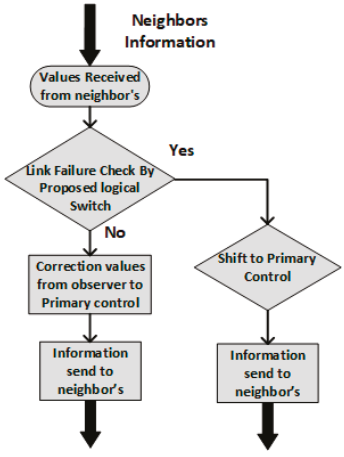

Figure 5. Proposed algorithm flow chart.

The vector for voltages $v = [v_1, v_2, \ldots\ldots, v_N]^T$ carries the measured voltage for each node. Similarly, the correction estimation vector is $v^* = [v_1^*, v_2^*, \ldots\ldots, v_N^*]^T$ and carries all the global voltage set points for all nodes. An equivalent equation for frequency can be expressed as:

$$s\overline{V} - \overline{v}(0) = sV - \mathrm{v}(0) - L\overline{V}. \tag{5}$$

A current regulator of node i checks the current reference value and tries to make a correction term to ensure equal load sharing between each node. Distributed line impedance varies the droop controller performance. As on node i, it compares local per-unit i_i^{PU} current with the neighbors' weighted average current per-unit and finds the correction value for current δ_i [13].

$$\delta_i = \sum_{j,\in N_i} a_{ji}\left(i_j^{PU} - i_i^{PU}\right), \tag{6}$$

where a_{ji} is the weight of the communication link, i_j^{PU} is the current from neighbors, and i_i^{PU} is the current of node i. Thus, if any mismatch between the per-unit current of the converters occurs, the current regulator will generate the correction term and adjust the current into a balanced form.

4.1. Single Converter model

DC MG systems based on multiple DC–DC converters usually have high switching frequency. Therefore, the impact of non-linearity in switching frequencies is averaged out, and owing to this fact the converters are a model based on state average modeling, and consensus control is also approximated as continuous in the time domain. However, when a connection failure occurs, the delay is very large in comparison to the normal delay in a communication network. The small signal model for a Buck converter is shown in (7) [34–36]:

$$\begin{pmatrix} \frac{di}{dt} \\ \frac{dv}{dt} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix} \begin{pmatrix} i \\ v \end{pmatrix} + \begin{pmatrix} \frac{D}{L} \\ 0 \end{pmatrix} V_g. \tag{7}$$

The transfer function for output values:

$$G_{vd} = \frac{v(s)}{d(s)} = \frac{v_g}{LCs^2 + \frac{L}{R}s + 1}, \tag{8}$$

$$G_{id} = \frac{i(s)}{d(s)} = \frac{I + V_o Cs + \frac{V_o}{R}}{LCs^2 + \frac{L}{R}s + 1}. \tag{9}$$

4.2. DC MG System Modeling

Let global reference voltage $v_{ref} = \left[v_1^{ref}, \ldots\ldots\ldots, v_n^{ref}\right]^T$ and actual supplied current $i = [i_1, \ldots\ldots i_n]^T$ vectors. The cooperative control of Figure 3 generates terms δv_1 and δi_i which are also represented as $\boldsymbol{\delta v_2}$ at the primary control signal point [13]. Accordingly,

$$\Delta V^1 = H\left(V_{ref} - \overline{V}\right), \tag{10}$$

$$\Delta V^2 = -cGLI^{PU}. \tag{11}$$

$\Delta v^1 = \left[\delta v_1^1, \ldots\ldots\ldots, \delta v_N^1\right]^T$ and $\Delta v^2 = \left[\delta v_1^2, \ldots\ldots\ldots, \delta v_N^2\right]^T$ are voltage and current correction term vectors. The Laplace transforms of Δv^1 and Δv^2 are ΔV^1 and ΔV^2. $H = diag\{H_i\}$ is the voltage controller matrix and $G = diag\{G_i\}$ is the current controller matrix. I^{PU} is the Laplace transform of i^{PU}, which is the per-unit current vector $i^{PU} = \left[i_1^{PU}, \ldots\ldots i_N^{PU}\right]^T$.

$$I^{PU} = I_{rated}^{-1} I \tag{12}$$

By, substituting (11) in (12),

$$\Delta V^2 = -cGLI_{rated}^{-1} I. \tag{13}$$

The local voltage set point for proposed controller is

$$V^* = V_{ref} + \Delta V^1 + \Delta V^2 - rI, \tag{14}$$

where $v^* = \left[v_1^*, \ldots\ldots\ldots, v_n^*\right]^T$ is the vector of the local voltage set and its Laplace transform is V^*. r is the virtual resistance matrix. Substituting (10) and (13) in (14),

$$V^* = (I_N + H)V_{ref} + H\overline{V} - \left(cGLI_{rated}^{-1} + r\right)I. \tag{15}$$

The dynamic behavior of the converter with a closed loop can be expressed as:

$$V_i = G_i^c(s)V_i^*, \tag{16}$$

where V_i and V_i^* are the voltage and G_i^c is the gain of converter i. The global dynamics of the converter will be

$$V = G_c V^*, \tag{17}$$

where the transfer matrix is $G_c = diag\left\{G_i^c\right\}$. By substituting (15) in (17),

$$V = G_c\left((I_N + H)V_{ref} + H\overline{V} - \left(cGLI_{rated}^{-1} + r\right)I\right). \tag{18}$$

By rearranging (5), we can get

$$\overline{V} = s(sI_N + L)^{-1}V = H_{obs}V. \tag{19}$$

Let us suppose a delay function in the neighbor's reference voltages. All of the delays are equal and periodic for delay value $\boldsymbol{\tau}$.

$$\overline{V} = s(sI_N + L)^{-1}V = H_{obs}V \times e^{s\tau} \tag{20}$$

For some sample of time, this function will be stable. The DC MG admittance matrix $\boldsymbol{Y_{bus}}$ is related to actual supplied current as

$$I = Y_{bus}V. \tag{21}$$

The detail of the distribution grid is contained in an admittance matrix. Therefore, (18) can be expressed as

$$\begin{cases} V = \left(G_c^{-1} + HH_{obs}^{F} \times e^{s\tau} + \left(cGLI_{rated}^{-1} + r\right)Y_{bus}\right)^{-1}(I_N + H)V_{ref}, \\ I = \left((Y_{bus}G_c)^{-1} + HH_{obs}^{F}Y_{bus}^{-1} \times e^{s\tau} + cGLI_{rated}^{-1} + r\right)^{-1}(I_N + H)V_{ref}. \end{cases} \tag{22}$$

Equation (22) describes the global dynamic with proposed controls, the system being linear. Suitable values for different gains can be found, such that poles of the system lie in the left half of the plan and the system will be stable for some open interval of delay $\boldsymbol{\tau}$.

For periodic and synchronized communication, the value of $\boldsymbol{\tau}$ should be small enough such that system can achieve reasonable stability and robustness as targeted by the design specification. At the same time, it should be large enough such that it can be realized by practical means of implementation. It can safely be assumed that small variations in delay will not cause any system instability, as the bandwidth of secondary control, which depends on communication-based control, is quite a bit lower than communication rate. If the delay increases due to some uncertainty in the communication link, then the link can be considered as broken and reliance on such communication is not appropriate, as it can jeopardize system stability. A more generalized limit to this uncertain value of delay can be derived by discretizing the system and extending Lemma 1 of the agreement protocol in the presence of noise [27]. This is expressed as follows: consider the discrete time equation for agreement protocol:

$$z(k+1) = (I - \gamma(k)L(g))z(k). \tag{23}$$

Equation (23) satisfies the following state:

$$\lim_{k\to\infty}\gamma(k) = 0, \sum_{k=1}^{\infty}\gamma(k) = \infty, \textit{ and } \sum_{k=1}^{\infty}\gamma^2(k) < \infty. \tag{24}$$

Lemma 1. *For a connected graph, the system's trajectory (23) convergences to the agreement set A w.p.1 (with probability 1) if the condition in (24) holds and for all* $k \geq 1$, $\gamma(k) \leq 2/\lambda_n(g)$.

For system convergence, a delay $\gamma(k) \leq 2/\lambda_n(g)$ with fixed boundary according to Lemma 1, So the system will converge and remain stable under such boundary that the nodes consider stable and healthy. more than this delay boundary that node consider as failed in communication network.

5. Case Studies and Simulation

A circular bi-directional communication ring was considered for the DC MG experimental setup to check the effectiveness and performance of the proposed control method by performing simulations in MATLAB, as shown in Figure 6. For the considered case study, the DC MG had a four-node radial network in a circular communication structure to support a DC resistive load connected on different nodes. For communication between nodes, an isolated RS232 was used in setup to exchange reference values. In the simulated case study, the effect of communication channel transmission delay was also considered. A detailed switch model was used for power converters to present more realistic results. The full case scenario is illustrated in Figure 6, and detailed node parameters used for the experimental setup are given in Table 1, which shows the communication links and power lines. The circular structure consisted of two-way communication with neighbors, as shown in Figure 7.

Transmission impedance effect was also considered in the experimental setup. As shown in Figures 3 and 6, the proposed control scheme detects link failure between the connected nodes and adjusts the gains according to the link failure, as explained in the flowchart in Figure 5. The detection algorithm is continuously working at every node, and if any link failure occurs, the secondary control quickly responds to the link failures and varies the gains that affect the voltage correction and current correction terms. Considering switch S2 in the experimental setup of the case study, only one node was connected with a load for the worst-case scenario with other nodes sharing the load. Consequently, the system output voltage and current sharing stabilized as shown in Figure 8a,b. The system remained stable, with variations in secondary control gain accordingly. Whenever link failure occurred in the MG as in Figure 7c, the proposed controller at the secondary level detected the link failure and it varied the voltage gain and current correction, as can be seen in Figure 8c,d. It can be seen from Equations (1) and (6) that for the correction term, the equation is dependent on the neighbor's reference values. When a link failure occurs, the reference from the neighbors in the correction equations are constant or zero, which therefore leads to sharp variations in the system correction term as in Figure 8c,d. Figure 9a,b display a conventional system without a link failure detection system that generates a correction term in absence of reference values at the voltage and current correction. This will result in the output voltage following the input voltage due to correction terms as in Figure 8c,d. The graphical representation is shown in Figure 7 for different scenarios. Bi-directional system communication links are assumed to have a balanced Laplacian matrix and adjacency matrix for communication graph weights using a_{ij} to generate correction terms. Figure 7a shows the fully connected balanced Laplacian matrix as shown in Equation (25):

$$L = \begin{pmatrix} 2 & -1 & 0 & -1 \\ -1 & 2 & -1 & 0 \\ 0 & -1 & 2 & -1 \\ -1 & 0 & -1 & 2 \end{pmatrix}. \tag{25}$$

Similarly, Figure 7b shows one communication link failure which changes the Laplacian matrix as shown in Equation (26). On the other hand, if failure of both links occurs, as shown in Figure 7c, then its Laplacian for the remaining system will be as in Equation (27):

$$L = \begin{pmatrix} 1 & -1 & 0 & 0 \\ -1 & 2 & -1 & 0 \\ 0 & -1 & 2 & -1 \\ 0 & 0 & -1 & 1 \end{pmatrix}, \tag{26}$$

$$L = \begin{pmatrix} 1 & -1 & 0 \\ -1 & 2 & -1 \\ 0 & -1 & 1 \end{pmatrix}. \tag{27}$$

During regular connectivity, all four nodes will work normally and exchange values with neighbors for correction terms as shown in Figure 6 and the first case of Figure 7a. With that correction term, the system will converge to a common reference point and share the load in a balanced form. Whereas, if one link failure occurs in any two nodes as in Figure 7b, the Laplacian will be different as in Equation (26), and consensus will work normally, in which it will vary the gain and adjust the system in order to maintain its stability and load sharing. As a result, the system has no effect on regular working of DC MG. If links fail on both sides then one node is communication islanding, whereas all other nodes can exchange information with each other. In that case, the proposed algorithm will maintain stability and load sharing by shifting the islanded node to droop by varying its gain. In contrast, the conventional secondary control would no longer be able to stabilize the system and requires tertiary control to take over the system for normal operation. The usage of the proposed control method helps

in stabilizing the system performance and neutralizing the need for tertiary control in the system. By using a simulation study, comparisons were made between the conventional secondary control with the proposed control as shown in Figures 8 and 9. Two cases were considered in the simulation: one is fully connected and the other is communication islanded, in which both links are assumed to be failed. Initially, the system worked in a fully connected condition, but link failure occurred at 1.5 s, and as in Figure 8, the proposed algorithm maintained system stability and load sharing. In contrast, the regular consensus system became unstable, which affected system performance.

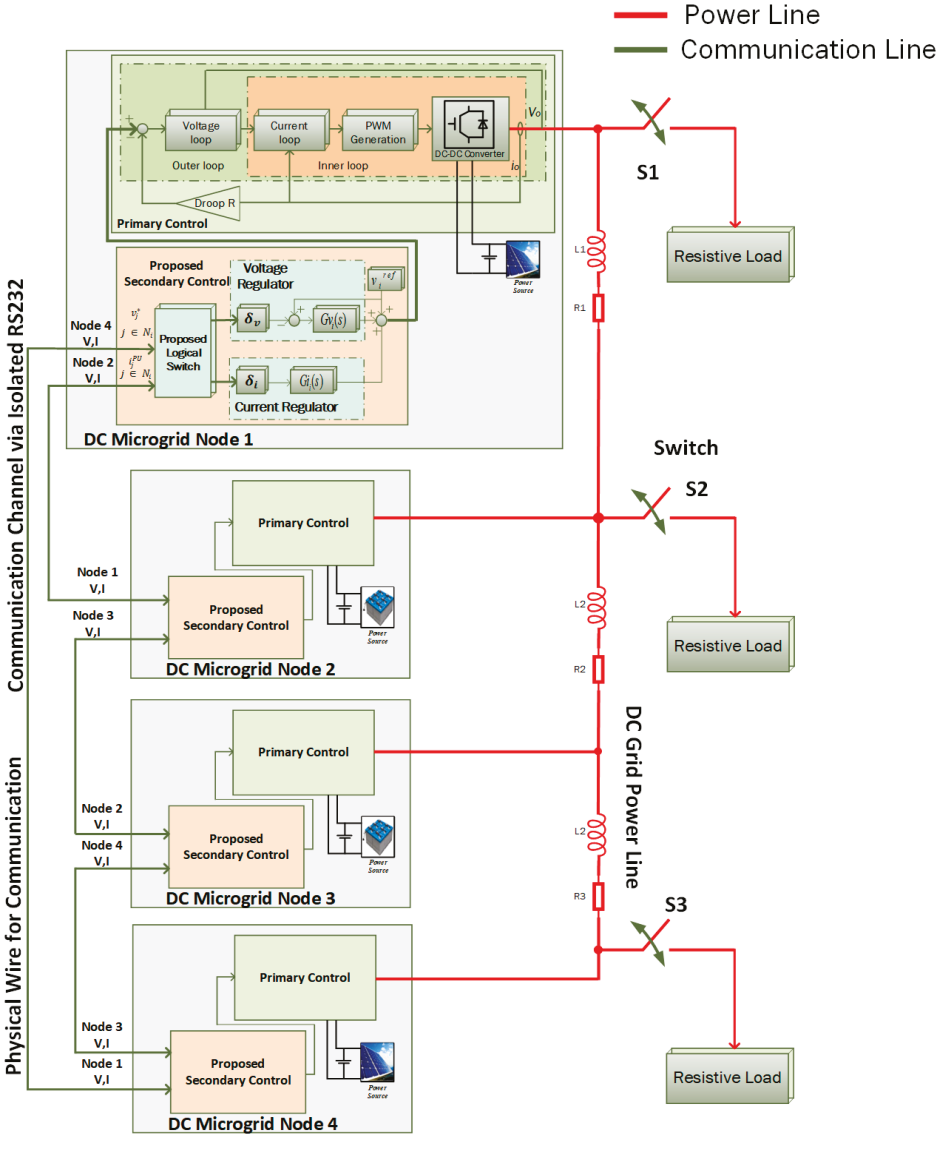

Figure 6. Proposed DC Microgrid experimental setup for case study.

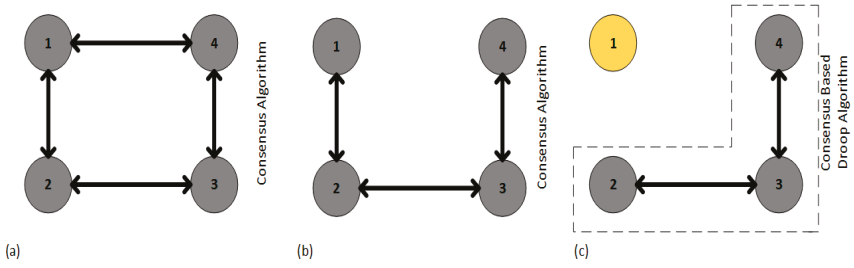

Figure 7. Different scenarios for DC MG.

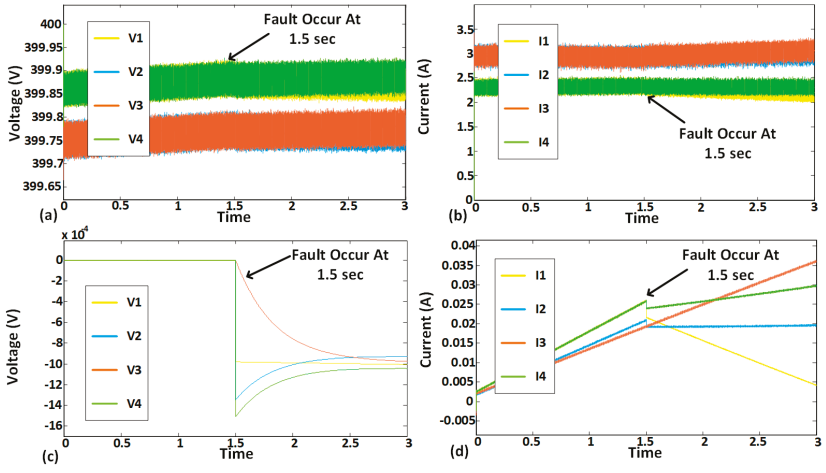

Figure 8. Results of proposed secondary control simulation: (**a**) node voltages; (**b**) node current; (**c**) voltage correction term; (**d**) current correction term.

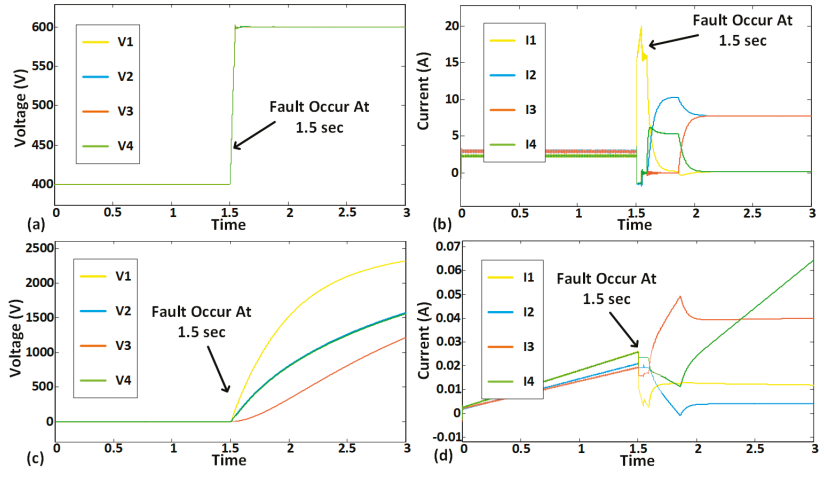

Figure 9. Results of conventional secondary control simulation: (**a**) node voltages; (**b**) node current; (**c**) voltage correction term; (**d**) current correction term.

Table 1. Parameters for single converter node in DC microgrid.

Parameters	Values
Input Voltage	600 V
Output Voltage	400 V
Droop gain (G_{Droop})	0.025
Resistive Load	80 ohm
Line Resistance	0.0005 ohm/m
Line inductance	0.50 µH/m
Line Length	100 m
Switching Frequency	10 kHz
Filter Inductor	1 mH
Filter Capacitor	300 µF
Communication Channel Bandwidth Delay at 20 kHz	0.15 ms
Inner loop	$Kp = 10$ $Ki = 0.05$
Outer loop	$Kp = 40$ $Ki = 0.05$
Voltage Observer	$Kp = 6$ $Ki = 0.1$
Current Observer	$Kp = 0.11$ $Ki = 0.6$

Plug-and-Play Capacity

The proposed system has plug-and-play capability. When one or more nodes' communication links fail at any time, the proposed controls stabilize the system. Communication link failure makes communication islands of varied sizes in the system. The proposed controls work to balance the system in the case of communication islanding. The performance of the DC MG shown in Figures 8 and 9 was satisfactory under such case. A load variation test was also done on the proposed control scheme, and it performed well and balanced the system in time, as in Figure 10.

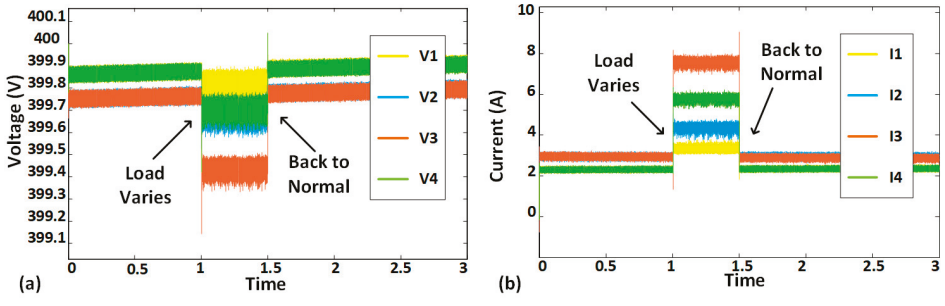

Figure 10. Load variation in the DC microgrid: (**a**) node voltage; (**b**) node current.

6. Conclusions

A distributed control scheme is proposed for a DC microgrid with some level of intelligence to check the communication link failure at the secondary level control. The proposed communication islanding algorithm scheme detects the link failure, and if any failure occurs, the proposed control scheme stabilizes the system and maintains load sharing. After detecting link failure, the proposed control scheme varies the gain of the correction term for the voltage and current observers, which stabilizes the system's operation during communication islanding and achieves a global reference point. This study shows that the proposed secondary control scheme is effective and provides stability to the

system in the case of a communication islanding scenario. The performance of the proposed scheme in communication link failure detection and stabilizing the system operation was tested through MATLAB/Simulink.

Author Contributions: M.U.S. proposed the idea for writing the manuscript. M.M.K. and H.T. suggested the literature and supervised in writing the manuscript. K.H. helped M.U.S. in writing and formatting. S.H. helped in modifying the figures and shared the summary of various credible articles to be included in this manuscript. H.J. helped in system parameters to make the simulation test possible.

Conflicts of Interest: The authors declare no conflict of interest.

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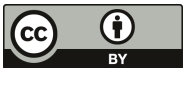

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Article

A Novel Synchronization Technique for Wireless Power Transfer Systems

Xin Liu [1], Nan Jin [2], Xijun Yang [1,*], Tianfeng Wang [1], Khurram Hashmi [1] and Houjun Tang [1]

[1] Key Laboratory of Control of Power Transmission and Transformation Ministry of Education, Shanghai Jiao Tong University, 800 Dongchuan RD., Shanghai 200240, China; Liu_xin@sjtu.edu.cn (X.L.); wangtf1992@163.com (T.W.); khurram_hashmi@sjtu.edu.cn (K.H.); hjtang@sjtu.edu.cn (H.T.)

[2] College of Electric and Information Engineering, Zhengzhou University of Light Industry, Zhengzhou 450002, China; jinnan@zzuli.edu.cn

* Correspondence: yangxijun@sjtu.edu.cn; Tel.: +86-138-1606-6208

Received: 29 September 2018; Accepted: 6 November 2018; Published: 13 November 2018

Abstract: Recently, wireless power transfer (WPT) systems with active receivers have been proposed for conduction loss reduction, bidirectional power transfer and efficiency improvement. However, the synchronization of WPT systems is complex in nature with the selection of high operating frequencies. Without proper synchronization, power oscillations appear and the system can become unstable. In this paper, a detailed analysis of different WPT systems is presented and the essence of the synchronization technique is derived as being composed of two functions: independent frequency locking and reference phase calibration. The voltage across the receiver-side compensation capacitor is divided and utilized for frequency locking, whereas the reference phase calibration is realized through software code. The proposed method is effective and easy to implement, with a lower overall cost due to its simplicity. The technique can work effectively at high frequency and withstand large variations of operating frequency, load and mutual inductance. In addition, it can address the synchronization problem of multiple active receiver WPT systems with and without cross coupling among the receiving coils. Theoretical analysis and experimental results validate the proposed technique.

Keywords: active receivers; frequency locking; reference phase calibration; synchronization; wireless power transfer

1. Introduction

Wireless power transfer (WPT) techniques can realize energy transmission through coupled coils without the need for physical contact between the transmitter and the receiver [1–3]. Considerable efforts are put into the modeling, performance analysis, design and optimization of WPT systems [4–10]. The operating frequencies of WPT systems can range from kHz to MHz. Radio frequency (RF) WPT systems operate at higher frequencies (such as 6.78 MHz and 13.56 MHz) and aim to increase the power transfer capacity [10–12]. Since the frequency is too high for digital signal processors (DSP) to control the transitions in RF WPT systems, diode rectification is widely adopted which brings about high forward voltage losses. Inductive power transfer systems with lower operating frequency (such as 85 kHz) can be used to transmit higher power levels such as in electric vehicle charging scenarios. Although inductive power transfer systems transmit power wirelessly in a shorter distance than RF systems, their overall efficiencies and power levels are higher. To avoid large transmission losses, various methods are investigated to achieve high efficiency. Recently, inductive power transfer systems with active receivers are the focus of study [13–16]. These systems can realize bidirectional power transfer [17–19] and contribute to efficiency improvement [20–22]. An active receiver in Reference [20] contributes to a maximum efficiency rise of 10% compared with traditional diode rectifiers. However,

such systems are complex in nature and some issues remain unresolved, such as the synchronization problem. The transmitter and receiver are contactless, whereas the control signals of the primary and secondary sides are in rigorous sequential relationships [23]. Although, theoretically the controllers can have the same operating frequency, the actual output frequencies may differ due to manufacturing tolerances of the devices. For DSP TMS320F28335 [24], the frequency precisions of regular pulse width modulator (PWM) and high resolution pulse width modulator (HRPWM) at 100 kHz are 0.1% and 0.002%, respectively. The corresponding maximum errors in the frequencies are in the range of 100 Hz and 2 Hz, respectively. Although the frequency deviations are much smaller as compared to the fundamental operating frequency, the WPT system becomes unstable. Without effective synchronization, the phase angles between the primary and secondary resonant voltages will change periodically, which results in power oscillations. Thus, synchronization of the WPT systems with active receivers is necessary and crucial for stable system operation.

Synchronization methods of the WPT systems can be classified into three categories as elaborated in Figure 1. The first method, as shown in Figure 1a, is introducing an external clock such as general packet radio service (GPRS), code division multiple access (CDMA) and Wi-Fi. Such systems can work only in places where the communication signals are available and stable. When the signal transfer path changes, phase error will appear due to changed time delays of different controllers. Thus, this technique cannot be easily applied to systems where the transmitter and receiver spatially move with respect to each other, such as mobile phone and electric vehicle charging scenarios [25]. The second method is, installing real-time clocks on the transmitter and receiver sides as shown in Figure 1b, which can include on-board atomic clocks and precision oscillators. This method is expensive, whereas small frequency discrepancies still exist. Cumulative error occurs during a long-time operation. The third method is, considering the transmitter as a source and synchronizing the receiver using auxiliary devices as shown in Figure 1c. The feasibility and robustness of the third scheme is greater in these methods. In References [17,18,26,27], a sense winding on the secondary side is proposed to capture the magnetic flux generated by the primary resonant current in order for synchronization. A voltage signal on the sense winding can be induced and the phase locking loop (PLL) is used to detect the primary time sequence. However, secondary magnetic flux produces an undesired voltage, which can deteriorate the synchronization performance seriously. A compensation circuit should be added to eliminate the phase error caused by this effect, whereas the circuit parameters depend heavily on the operating conditions. As reported in Reference [17], the phase error can be about 22% when the coupling factor is decreased by 50% and 15% when the primary compensation capacitance is decreased by 20%. In Reference [20], secondary current is sampled by the sensor for synchronization. Except for the cost and frequency bandwidth of the sensors, the phase error caused by the time delay of the devices is corrected by a carefully designed and parameter-sensitive phase-shift circuit. In References [28,29], the real and reactive powers produced by the receiver are utilized to estimate the position of the voltage vector induced by the primary converter. This method requires accurate samplings of secondary high-frequency resonant current and voltage, as well as a complex processing hardware circuit and calculation algorithm. In multiple active receiver applications, the magnetic field becomes more complex, which increases the difficulty in phase compensation. Previous works largely focus on the applications and contributions of multiple active receiver WPT systems [30,31], whereas, synchronization techniques have not been explored due to their complexity.

Since time delay of the synchronization signal can lead to phase errors, it can be inferred that the accuracy of the synchronization technique is closely related to the signal transmission speed. A higher speed, therefore, corresponds to a higher accuracy. Some high speed methods typically use a laser beam for synchronization [32]. However, the authors find that the essence of synchronization is frequency locking which is independent of signal transmission speed. Generally, circuit-based methods are utilized to correct the phase errors caused by the time delay and system parameter variations [17,20]. The authors find that phase calibration can be easily achieved through software code.

This paper provides a clear illustration of the synchronization technique for the WPT systems. Four specific conditions are investigated, namely: Tuned and detuned WPT systems with one active receiver, and multiple active receiver WPT systems with and without cross coupling among receiving coils. Through summarizing the analysis of different systems, the essence of the synchronization technique is deduced and presented. Then, a universal synchronization technique belonging to the third synchronization category is elaborated and verified through experimental results. The salient contributions of this work are:

(1) Presenting a detailed analysis of the synchronization technique and clearly decomposing it into independent frequency locking and reference phase calibration based on mathematical derivations;
(2) Proposing an effective frequency locking circuit that has strong robustness and independence of system parameters;
(3) Achieving reference phase calibration through software code without using additional phase-shift circuits, which advances in easy realization and cost effectiveness;
(4) Realizing the synchronization for WPT systems with multiple active receivers.

This paper is divided into five sections. Section 2 analyzes different WPT systems with active receivers, which contributes to figuring out the essence of the synchronization technique. Based on the analysis, Section 3 presents the proposed hardware circuit and software code, aiming for frequency locking and reference phase calibration, respectively. Section 4 validates the feasibility and effectiveness of the proposed systems through experiments. Section 5 concludes this paper.

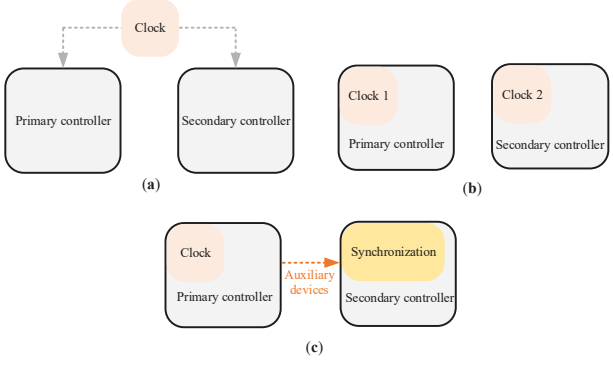


Figure 1. Synchronization methods: (**a**) external clock; (**b**) precision on-board clocks; and (**c**) auxiliary synchronization devices.

2. Synchronization Analysis

2.1. Tuned WPT System with One Active Receiver

The schematic of a WPT system with one active receiver is depicted in Figure 2. $V_{1,dc}$, $V_{2,dc}$, $I_{1,dc}$ and $I_{2,dc}$ are the primary and secondary dc voltages and currents, respectively. $C_{1,dc}$ and $C_{2,dc}$ are the filtering capacitors and $R_{L,2}$ is the load. L_1 and L_2 are the transmitting and receiving coils compensated by C_1 and C_2, respectively. R_1 and R_2 are the coil resistances. Q_1–Q_8 are eight metal-oxide-semiconductor field effect transistors (MOSFETs). v_1 and v_2 are the voltages applied on the resonant network, which contain only the odd frequency components. i_1 and i_2 are the primary and secondary resonant currents. Their fundamental frequency components are denoted as v_{11}, v_{21}, i_{11} and i_{21}, whose root-mean-square (RMS) values are V_{11}, V_{21}, I_{11} and I_{21}, respectively. Due to the band pass filtering effect by the resonant network, the fundamental frequency component contributes most to the transferred power. Therefore, i_{11} and i_{21} are nearly the same as i_1 and i_2, respectively. The typical waveforms of the system are presented in Figure 3, where v_{21} leads i_{21} by φ_2. $2\alpha_1$ and $2\beta_2$ represent

the phase angles of the resonant voltages. In most of the previously published papers related to WPT systems, fundamental harmonic analysis (FHA) and phasor methods are widely adopted [20–22], which can greatly simplify the analysis. In this paper, boldface letters represent the phasors and capital italic letters represent RMS values of the phasors. For example, $\mathbf{V_{11}}$ and V_{11} represent the voltage phasor and RMS value of v_{11}, respectively.

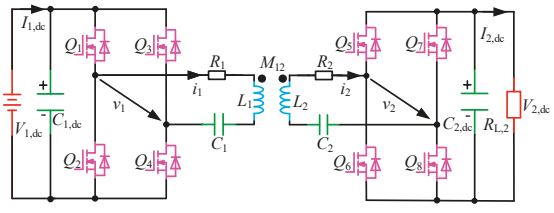


Figure 2. WPT system with one active receiver.

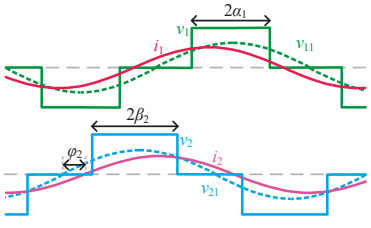


Figure 3. Typical primary and secondary waveforms of a WPT system with one active receiver.

Primary and secondary parameters are identical and the inverting angular frequency ω_1 is $\frac{1}{\sqrt{L_1C_1}}$. Then, Equation (1) is obtained according to primary current loop.

$$\mathbf{V_{11}} = -j\omega_1 M_{12}\mathbf{I_{21}} + \mathbf{I_{11}}R_1 \tag{1}$$

Generally, the voltage across R_1 is much smaller than $\mathbf{V_{11}}$. Therefore, Equation (1) can be simplified into Equation (2).

$$\mathbf{I_{21}} = \frac{\mathbf{V_{11}} - \mathbf{I_{11}}R_1}{-j\omega_1 M_{12}} \approx \frac{\mathbf{V_{11}}}{-j\omega_1 M_{12}} \tag{2}$$

Neglecting the losses of the active bridge, energy conservation equation of the receiver can be derived as

$$V_{21}I_{21}\cos\varphi_2 = V_{2,dc}I_{2,dc}. \tag{3}$$

According to fundamental harmonic analysis, V_{11} and V_{21} can be obtained.

$$V_{11} = \frac{2\sqrt{2}\sin\alpha_1}{\pi}V_{1,dc} \tag{4}$$

$$V_{21} = \frac{2\sqrt{2}\sin\beta_2}{\pi}V_{2,dc} \tag{5}$$

Thus, the expression of $I_{2,dc}$ can be deduced as

$$I_{2,dc} = \frac{8\sin\alpha_1\sin\beta_2\cos\varphi_2}{\pi^2\omega_1 M_{12}}V_{1,dc}. \tag{6}$$

When the primary and secondary controllers operate at different frequencies (f_1 and f_2, respectively), φ_2 is expressed as

$$\varphi_2 = 2\pi(f_1 - f_2)t + \varphi_{2,0}, \tag{7}$$

where $\varphi_{2,0}$ is the initial phase of φ_2. $\varphi_{2,0}$ is determined by controllers, whereas it may be different from the coded phase.

Then, $I_{2,\mathrm{dc}}$ is derived by substituting Equations (7) into (6).

$$I_{2,\mathrm{dc}} = \frac{8V_{1,\mathrm{dc}} \sin\alpha_1 \sin\beta_2}{\pi^2 \omega_1 M_{12}} \cos[2\pi(f_1 - f_2)t + \varphi_{2,0}] \tag{8}$$

When $f_1 = f_2$, $I_{2,\mathrm{dc}}$ is stable. Furthermore, when $\varphi_{2,0} = 0$, $I_{2,\mathrm{dc}}$ reaches peak value which benefits power transfer.

2.2. Detuned WPT System with One Active Receiver

Figure 4 shows the equivalent circuit of an active bridge. Z_2 represents the equivalent impedance of the active bridge on the AC side, which consists of resistive and reactive components. The phase of $\mathbf{I_{21}}$ is denoted by φ_{i_2}. Then, $\mathbf{V_{21}}$ can be expressed as

$$\mathbf{V_{21}} = \frac{2\sqrt{2}\sin\beta_2}{\pi} V_{2,\mathrm{dc}} e^{j(\varphi_2 + \varphi_{i_2})}. \tag{9}$$

Since $I_{2,\mathrm{dc}} = V_{2,\mathrm{dc}}/R_{\mathrm{L},2}$, Equation (3) can be deduced into Equation (10).

$$V_{21} I_{21} \cos\varphi_2 = \frac{{V_{2,\mathrm{dc}}}^2}{R_{\mathrm{L},2}} \tag{10}$$

Therefore, I_{21} can be obtained and $\mathbf{I_{21}}$ can be rewritten as

$$\mathbf{I_{21}} = \frac{\pi V_{2,\mathrm{dc}} e^{j\varphi_{i_2}}}{2\sqrt{2} R_{\mathrm{L},2} \sin\beta_2 \cos\varphi_2}. \tag{11}$$

The expression of Z_2 can be derived as Equation (12) according to Equations (9) and (11), which is related to φ_2.

$$Z_2 = \frac{\mathbf{V_{21}}}{\mathbf{I_{21}}} = \frac{8\sin^2\beta_2 \cos\varphi_2 R_{\mathrm{L},2} e^{j\varphi_2}}{\pi^2} \tag{12}$$

Furthermore, the relationship between $I_{2,\mathrm{dc}}$ and I_{21} can be obtained as Equation (13).

$$I_{2,\mathrm{dc}} = \frac{2\sqrt{2}\sin\beta_2 \cos\varphi_2}{\pi} I_{21} \tag{13}$$

The transmitter can operate at various frequencies and the dual-side parameters can be different in practice, that is, the system can be detuned. The primary and secondary reactance are expressed as Equations (14) and (15).

$$X_1 = \omega_1 L_1 - \frac{1}{\omega_1 C_1} \tag{14}$$

$$X_2 = \omega_1 L_2 - \frac{1}{\omega_1 C_2} \tag{15}$$

Therefore, the dual-side current loops can be derived as follows.

$$\mathbf{V_{11}} = -j\omega_1 M_{12} \mathbf{I_{21}} + {}_{11}(R_1 + jX_1) \tag{16}$$

$$0 = -j\omega_1 M_{12} \mathbf{I_{11}} + \mathbf{I_{21}}(R_2 + jX_2 + Z_2) \tag{17}$$

Then, the secondary current $\mathbf{I_{21}}$ can be deduced as Equation (18).

$$\mathbf{I_{21}} = \frac{j\omega_1 M_{12} \mathbf{V_{11}}}{(R_1 + jX_1)(R_2 + jX_2 + Z_2) + {\omega_1}^2 {M_{12}}^2} \tag{18}$$

By combining Equations (4), (13) and (18), the following equation can be obtained.

$$I_{2,\mathrm{dc}} = \frac{8\omega_1 M_{12} V_{1,\mathrm{dc}} \sin\alpha_1 \sin\beta_2}{\pi^2} \frac{\cos\varphi_2}{|(R_1 + jX_1)(R_2 + jX_2 + Z_2) + {\omega_1}^2 {M_{12}}^2|} \tag{19}$$

Defining the function $g_2(\varphi_2)$ to indicate the influence of φ_2 on $I_{2,\mathrm{dc}}$.

$$g_2(\varphi_2) = \frac{\cos\varphi_2}{|(R_1 + jX_1)(R_2 + jX_2 + Z_2) + {\omega_1}^2 {M_{12}}^2|} \tag{20}$$

By substituting Equations (7) and (20) into Equation (19), $I_{2,\mathrm{dc}}$ can be rewritten as

$$I_{2,\mathrm{dc}} = \frac{8\omega_1 M_{12} V_{1,\mathrm{dc}} \sin\alpha_1 \sin\beta_2}{\pi^2} g_2(2\pi(f_1 - f_2)t + \varphi_{2,0}). \tag{21}$$

The output current is related to the frequency difference of the controllers and the initial phase. Without synchronization, φ_2 changes periodically, resulting in the variation of $g_2(\varphi_2)$. As a result, $I_{2,\mathrm{dc}}$ will oscillate at the frequency of $(f_1 - f_2)$.

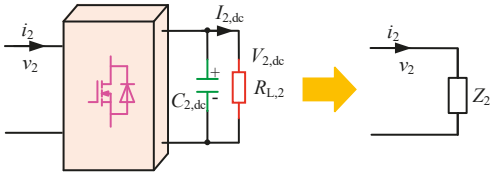


Figure 4. Equivalent circuit of active bridge.

2.3. Multiple Receivers without Cross Coupling

Figure 5 shows a multiple active receiver WPT system without cross coupling among the receiving coils, which has one transmitter and multiple receivers. The transmitting and receiving coils are coupled, whose mutual inductances are denoted as $M_{1\mathrm{i}}$ ($\mathrm{i} \geq 2$). L_i, R_i, C_i, $C_{\mathrm{i,dc}}$ and $R_{\mathrm{L,i}}$ are the coil inductance, coil resistance, compensation capacitor, filtering capacitor and loading resistance of receiver i, respectively. v_i, i_i and $I_{\mathrm{i,dc}}$ are the resonant voltage, resonant current and output dc current, respectively.

The phase difference between $v_{\mathrm{i}1}$ and $i_{\mathrm{i}1}$ (φ_i) can be expressed as

$$\varphi_\mathrm{i} = 2\pi(f_1 - f_\mathrm{i})t + \varphi_{\mathrm{i},0}, \tag{22}$$

where $\varphi_{\mathrm{i},0}$ and f_i are the initial phase of φ_i and the operating frequency of receiver i, respectively.

Equivalent impedance Z_i and reactance X_i given by Equations (23) and (24), can be obtained according to Equations (12) and (14).

$$Z_\mathrm{i} = \frac{8\sin^2\beta_\mathrm{i}\cos\varphi_\mathrm{i} R_{\mathrm{L,i}} e^{j\varphi_\mathrm{i}}}{\pi^2} \tag{23}$$

$$X_\mathrm{i} = \omega_1 L_\mathrm{i} - \frac{1}{\omega_1 C_\mathrm{i}} \tag{24}$$

The source of the system described is the primary resonant voltage. The original electromotive force of each receiver coil is induced by the primary current. Therefore, the resonant current frequencies of the receivers are supposed to be identical to the primary operating frequency. The current loops of the system are given as follows.

$$\mathbf{V_{11}} = -\sum_{k=2}^{n} j\omega_1 M_{1k}\mathbf{I_{k1}} + \mathbf{I_{11}}(R_1 + jX_1) \tag{25}$$

$$0 = -j\omega_1 M_{1i}\mathbf{I_{11}} + \mathbf{I_{i1}}(R_i + jX_i + Z_i) \tag{26}$$

Primary current $\mathbf{I_{11}}$ and the receiver-side resonant current $\mathbf{I_{i1}}$ can be deduced as Equations (27) and (28).

$$\mathbf{I_{11}} = \frac{\mathbf{V_{11}}}{R_1 + jX_1 + \sum_{k=2}^{n} \frac{{\omega_1}^2 {M_{1k}}^2}{R_k + jX_k + Z_k}} \tag{27}$$

$$\mathbf{I_{i1}} = \frac{j\omega_1 M_{1i}\mathbf{V_{11}}}{(R_i + jX_i + Z_i)(R_1 + jX_1 + \sum_{k=2}^{n} \frac{{\omega_1}^2 {M_{1k}}^2}{R_k + jX_k + Z_k})} \tag{28}$$

Thus, $I_{i,dc}$ is derived based on Equation (13).

$$I_{i,dc} = \frac{8\omega_1 M_{1i} V_{1,dc} \sin\alpha_1 \sin\beta_i}{\pi^2} \frac{\cos\varphi_i}{\left|(R_i + jX_i + Z_i)(R_1 + jX_1 + \sum_{k=2}^{n} \frac{{\omega_1}^2 {M_{1k}}^2}{R_k + jX_k + Z_k})\right|} \tag{29}$$

Z_i is related to φ_i. Therefore, function $g_i(\varphi_2, ..., \varphi_n)$ is defined to indicate the influence of φ_i on $I_{i,dc}$.

$$g_i(\varphi_2, ..., \varphi_n) = \frac{\cos\varphi_i}{\left|(R_i + jX_i + Z_i)(R_1 + jX_1 + \sum_{k=2}^{n} \frac{{\omega_1}^2 {M_{1k}}^2}{R_k + jX_k + Z_k})\right|} \tag{30}$$

By substituting Equations (22) and (30) into Equation (29), $I_{i,dc}$ can be rewritten as

$$I_{i,dc} = \frac{8\omega_1 M_{1i} V_{1,dc} \sin\alpha_1 \sin\beta_i}{\pi^2} g_i((2\pi(f_1 - f_2)t + \varphi_{2,0}), ..., (2\pi(f_1 - f_n)t + \varphi_{n,0})). \tag{31}$$

When the cross coupling among the receiving coils is not considered, $I_{i,dc}$ is a function of the operating frequency differences $(f_1 - f_i)$ and the initial phases $(\varphi_{i,0})$.

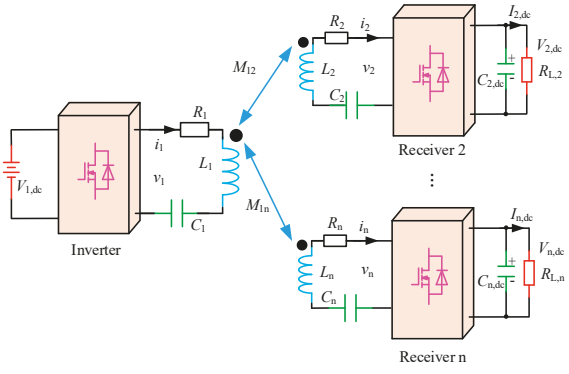


Figure 5. Schematic of a multiple active receiver WPT system without cross coupling.

2.4. Multiple Receivers with Cross Coupling

Figure 6 shows a multiple active receiver WPT system with cross coupling among the receiving coils. The cross coupling mutual inductances are denoted as M_{ij} (i, j $\geq$ 2 and i $\neq$ j). The current loop of receiver i can be deduced as Equation (32).

$$0 = -\sum_{j=1,j\neq i}^{n} j\omega_1 M_{ji}\mathbf{I_{j1}} + \mathbf{I_{i1}}(R_i + jX_i + Z_i),\ i \geq 2 \tag{32}$$

Then, the receiver-side resonant current $\mathbf{I_{i1}}$ can be obtained by:

$$\mathbf{I_{i1}} = \frac{\sum_{j=1,j\neq i}^{n} j\omega_1 M_{ji}\mathbf{I_{j1}}}{R_i + jX_i + Z_i},\ i \geq 2. \tag{33}$$

Thus, the expression of $I_{i,dc}$ is derived.

$$I_{i,dc} = \frac{2\sqrt{2}\sin\beta_i \cos\varphi_i}{\pi} \frac{\left|\sum_{j=1,j\neq i}^{n} j\omega_1 M_{ji}\mathbf{I_{j1}}\right|}{|R_i + jX_i + Z_i|},\ i \geq 2 \tag{34}$$

The equivalent impedance of the receiver and the resonant currents are related to φ_i. Thus, function $g_i(\varphi_2, ..., \varphi_n)$ is defined as follows.

$$g_i(\varphi_2, ..., \varphi_n) = \frac{\left|\sum_{j=1,j\neq i}^{n} j\omega_1 M_{ji}\mathbf{I_{j1}}\right| \cos\varphi_i}{|R_i + jX_i + Z_i|},\ i \geq 2 \tag{35}$$

$I_{i,dc}$ can be rewritten as Equation (36).

$$I_{i,dc} = \frac{2\sqrt{2}\sin\beta_i}{\pi} g_i((2\pi(f_1 - f_2)t + \varphi_{2,0}), ..., (2\pi(f_1 - f_n)t + \varphi_{n,0})) \tag{36}$$

Regardless of their tuned or detuned conditions, having one or multiple active receivers, with or without crossing coupling, the frequency of receiver-side resonant currents should be f_1. It is found that Equations (8), (21), (31) and (36) can be written into a similar expression as shown in Equation (37) where a_i is a constant value under a certain system configuration.

$$I_{i,dc} = a_i g_i((2\pi(f_1 - f_2)t + \varphi_{2,0}), ..., (2\pi(f_1 - f_n)t + \varphi_{n,0})) \tag{37}$$

The synchronization target is to keep $I_{i,dc}$ constant and find the reference phase of the receivers. Thus, the synchronization of the WPT systems can be divided into two independent functions: Ensuring that $f_2 = f_3 = \ldots = f_n = f_1$ and $\varphi_{2,0} = \varphi_{3,0} = \ldots = \varphi_{n,0} = 0°$.

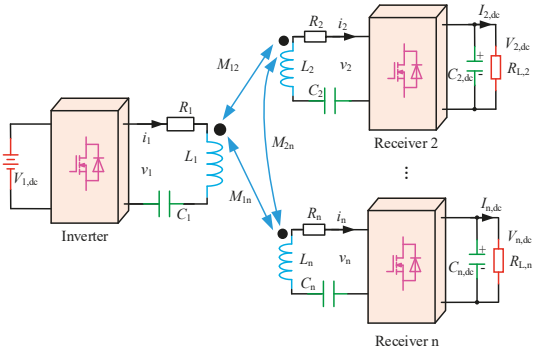


Figure 6. Schematic of a multiple active receiver WPT system with cross coupling.

3. Proposed Synchronization Technique

The synchronization system can be decomposed into independent frequency locking and reference phase calibration as analyzed in Section 2. In this paper, the frequency locking is realized by a proposed hardware circuit and the reference phase calibration is achieved through software code.

3.1. Hardware Circuit

The frequency of receiver-side resonant currents should be f_1. i_i flows through C_i. Thus, the frequency of the voltage across C_i should be equal to f_1 as well. In this paper, the voltage across the compensation capacitor is utilized for frequency locking.

Figure 7 shows the block diagram and detailed schematic of the proposed frequency locking circuit, which produces a zero-crossing synchronization signal. The voltage across C_i is divided over the resistances, which can obtain voltage v_{ci}. The high-side resistance R_h is 2 MΩ and the low-side resistance R_l is 10 kΩ. To ensure that v_{ci} stays within a proper range, the values of the divider resistances should be configured with the power level. A bidirectional Zener diode with 6.8 V reverse breakdown voltage is used to limit the voltage. v_{ci} is sent to the comparator TLV3502 (Texas Instruments, Richardson, TX, USA) which can generate a square wave with the frequency f_1. After passing through the isolator ISO721 (Texas Instruments, Richardson, TX, USA), the frequency locking signal v_{fi} is fed to the synchronization port of DSP such as GPIO6 in TMS320F28335 (Texas Instruments, Richardson, TX, USA). The comparator and the isolator are supplied by an isolated direct-current-to-direct-current (DC/DC) converter ADUM5000 (Analog Devices Inc., Wood, MA, USA). The resonant capacitor voltage is high and is converted into a digital signal immediately. Thus, the frequency locking circuit is insensitive to interferences. In addition, the circuit consists of a comparator, an isolator and an isolated power supply chip, which makes it cost effective and has a low power consumption.

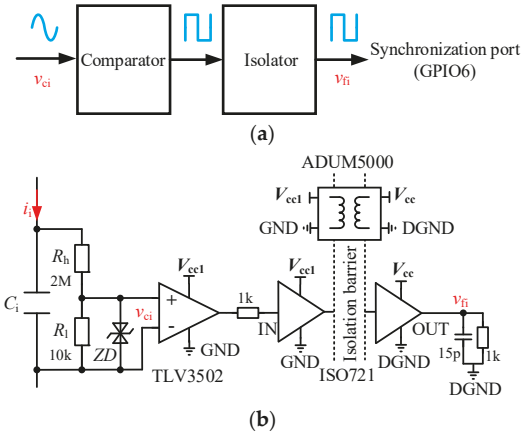


Figure 7. Proposed frequency locking circuit: (**a**) block diagram; and (**b**) detailed schematic.

3.2. Software Code

v_{ci} lags i_i by 90°. However, due to the time delay of the frequency locking and the driver circuits, $\varphi_{i,0}$ in Equation (37) is uncertain and can differ from the coded initial phase. After locking the frequency, the reference phases of the controllers should be calibrated, which is implemented by software code. The coded phase defined in the controller is φ_i' whose initial value is $\varphi_{i,0}'$. The task of reference phase calibration is to change $\varphi_{i,0}'$ to ensure $\varphi_{i,0} = 0$, that is, v_i and i_i are in phase. Figure 8 shows the reference phase calibration process. Firstly, φ_i' is set at $\varphi_{i,0}'$. v_i and i_i are captured by the oscilloscope. Then,

the system is turned on and v_i and i_i phase synchronization is observed. If v_i and i_i are not in phase, traversal algorithm can be executed to change φ_i,' where φ_i' can vary from $\varphi_{i,0}$' to 360° + $\varphi_{i,0}$.' Once v_i and i_i are in phase, the reference phase is locked and $\varphi_{i,0}$' is determined. Since the time delay remains almost unchanged for a certain circuit, the corresponding phase error is independent of the load, the mutual inductance and other system parameters. Furthermore, the reference phase calibration only needs one execution after the system is implemented and it can be completed within several minutes, which makes this synchronization technique easy for wide applications.

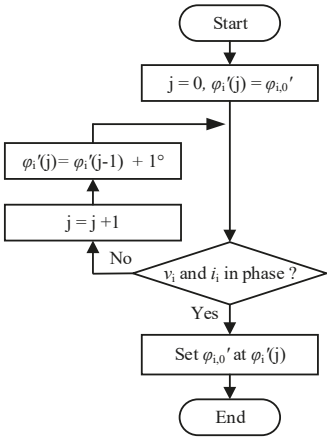


Figure 8. Reference phase calibration process.

The main flowchart of the phase calibration process has been elaborated above, whereas the register configuration details are of great importance as described below. Improper configuration can lead to the system becoming unstable.

There are three counter modes of the enhanced pulse width modulator (EPWM): count-up mode, count-down mode and count-up-down mode. For easy calculation of the register values, the count-up mode is adopted in this work. The frequency locking process in the controller is shown in Figure 9, where TBPRD1 and TBPRDi (i $\geq$ 2) are the time base periods (TBPRD) of the PWM modules of the transmitter-side and receiver-side controllers, respectively. For better understanding, the time delay of the devices is not considered in this analysis. Ideally, time base periods can be the same. However, the actual output frequency will deviate from the preset value due to limited frequency precision. In practice, TBPRDi should be greater than TBPRD1. The receiver-side controller detects the frequency locking signal at first, where the counter should be equivalent to TBPRD1. Then, the counter is reset to 0. This process can ensure the frequency of v_i equal to f_1.

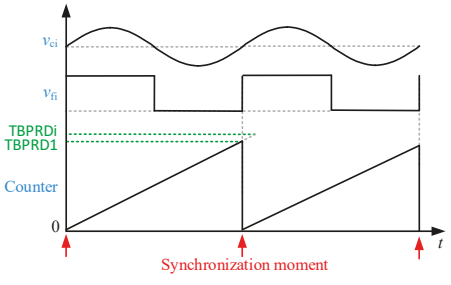


Figure 9. Synchronization process.

Faulty configurations of the reserved registers can lead to two problems. Firstly, as shown in Figure 10a, where TBPRDi is smaller than TBPRD1, the counter operates abnormally. The counter reaches TBPRDi and is reset to 0. When the frequency locking signal appears, the counter is reset to 0 again, resulting in a wrong counting sequence. Therefore, TBPRDi should be greater than TBPRD1. Secondly, as shown in Figure 10b, although the counter operates normally, an erroneous gate drive signal is generated. Comparing values of groups A and B (CMPA and CMPB) are used to generate β_i and φ_i. When CMPB (or CMPA) falls into the range of (TBPRD1, TBPRDi), wrong gate drive signals appear. The counter cannot reach the reserved register value where the control signal is supposed to be toggled. Then, the gate drive signal remains unchanged, which leads to a wrong v_i. Therefore, the maximum CMPA and CMPB should be slightly smaller than TBPRD1, which is denoted as CMP_{max}. The specific value of CMP_{max} should be determined according to the frequency precision of the controllers.

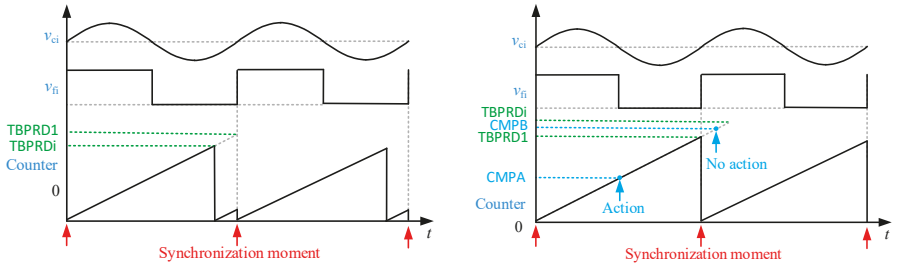


Figure 10. Faulty configuration of reserved registers: (**a**) wrong counting sequence; and (**b**) comparing value beyond the counting range.

Figure 11 shows the detailed synchronization process and corresponding relationships among the reserved register values and the phase angles. The gate drive signals of receiver i are denoted as Q_{4i-3}, Q_{4i-2}, Q_{4i-1} and Q_{4i}, whereas the comparing values of the corresponding controller are denoted as $CMPA_{2i-1}$, $CMPB_{2i-1}$, $CMPA_{2i}$ and $CMPB_{2i}$. The mathematical expressions of the register values are shown in the following equations.

$$CMPA_{2i-1} = \frac{(\varphi_{i,0}{}' - \varphi_i + \beta_i - 90)}{360} CMP_{max} \tag{38}$$

$$CMPB_{2i-1} = \frac{(\varphi_{i,0}{}' - \varphi_i + \beta_i - 270)}{360} CMP_{max} \tag{39}$$

$$CMPA_{2i} = \frac{(\varphi_{i,0}{}' - \varphi_i - \beta_i + 90)}{360} CMP_{max} \tag{40}$$

$$CMPB_{2i} = \frac{(\varphi_{i,0}{}' - \varphi_i - \beta_i - 90)}{360} CMP_{max} \tag{41}$$

Since φ_i and $\varphi_{i,0}{}'$ may range from 0° to 360°, according to Equations (38)–(41), the calculated CMPA and CMPB values may be beyond [0, CMP_{max}]. When these values are negative or greater than CMP_{max}, several times of CMP_{max} should be added or subtracted to ensure them falling in the range.

The task of reference phase calibration process is to change $\varphi_{i,0}{}'$ to track the point where $\varphi_i = 0$. After that, the receiver-side phase angles can be applied for impedance matching or output power regulation [20,21]. Many wireless charging devices require a constant voltage supply. Thus, Figure 12 shows the control flowchart for constant voltage power transfer, where $U_{i,dc}{}^*$ represents the desired voltage. If $U_{i,dc}$ is greater than $U_{i,dc}{}^*$ (i.e., $U_{i,dc} > U_{i,dc}{}^*$), β_i is decreased by 1°. Otherwise, β_i is increased by 1°. This method is effective and easy to implement.

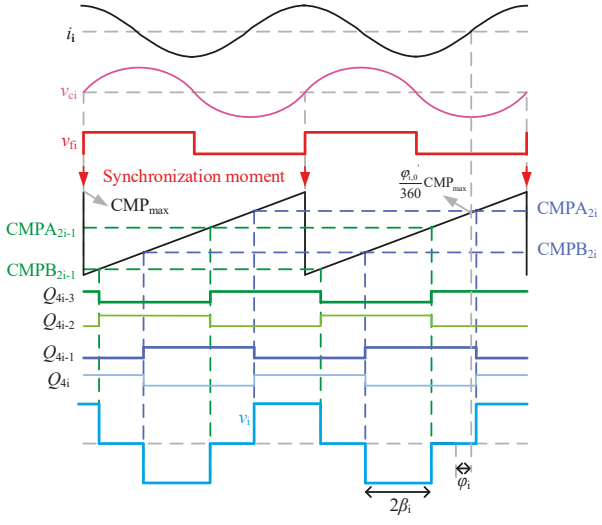


Figure 11. Detailed synchronization process and corresponding relationships among reserved register values and phase angles.

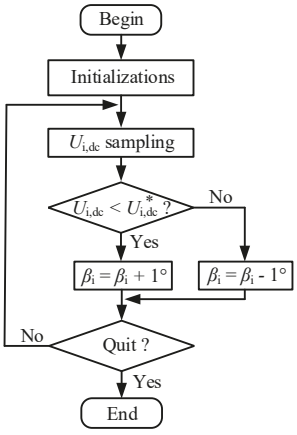


Figure 12. Flowchart of constant voltage power transfer.

3.3. System Layout

The schematic of the proposed WPT system with multiple active receivers is shown in Figure 13. A frequency locking circuit is installed on each receiver side that produces the synchronization signal for each DSP controller.

The prototype system is implemented in the following sequence: Firstly, the coded initial phase is calibrated and then the corresponding reference phase is written into the controllers. Secondly, the primary controller is turned on and the primary active bridge inverts the high frequency voltage. The frequency locking signal is generated, whereas the receiver-side controllers remain on standby and the diode rectification is used by the receivers. Thirdly, the gate drive signals of the receivers are generated. Finally, the phase angles are altered according to power transfer requirements.

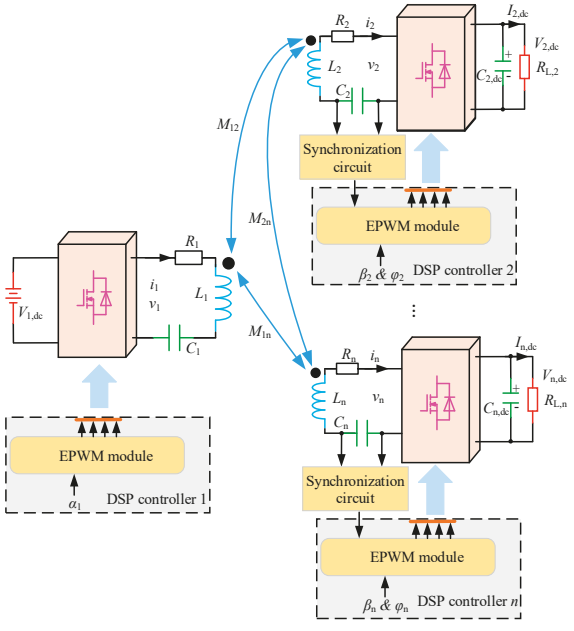


Figure 13. System schematic.

4. Experiment and Discussion

To verify the presented synchronization technique, the system is experimentally studied by using two prototypes: the first WPT system is implemented with one active receiver, whereas, the other with two active receivers. The specific parameters of the prototypes are listed in Table 1. Three independent microcontrollers and six Cree half bridges are used [33]. The coil self-inductances and mutual inductances are measured using inductance, capacitance, and resistance (LCR) meter TH2830 (RIGOL, Suzhou, China). Chroma programmable alternating-current-to-direct-current (AC/DC) electronic load model 63803 (Chroma, Marlborough, MA, USA) is utilized to vary the loading resistance. Tektronix TPS2024B Oscilloscope (Tektronix, Inc., Beaverton, OR, USA) is used to record the experimental waveforms. The experimental video is attached in Supplementary Materials.

Table 1. Key parameters of proposed system.

Symbol	Quantity	Value
L_1	coil inductance of transmitter	61 μH
L_2	coil inductance of receiver 1	61 μH
L_3	coil inductance of receiver 2	81 μH
C_1	primary compensation capacitance	0.05 μF
C_2	compensation capacitance of receiver 1	0.05 μF
C_3	compensation capacitance of receiver 2	0.04 μF

4.1. One active Receiver WPT System

Figure 14 shows the photograph of the WPT system with one active receiver. Figure 14a shows the designed DSP controller which consists of frequency locking circuit, power supply module and DSP TMS320F28335. Figure 14b shows the view of the complete system. Both the coil inductances are 61 μH, which are compensated by 0.05 μF AC capacitors. $V_{1,dc}$ is 50 V. The power transfer distance (d_{12}) is 80 mm with the mutual inductance of 16.7 μH.

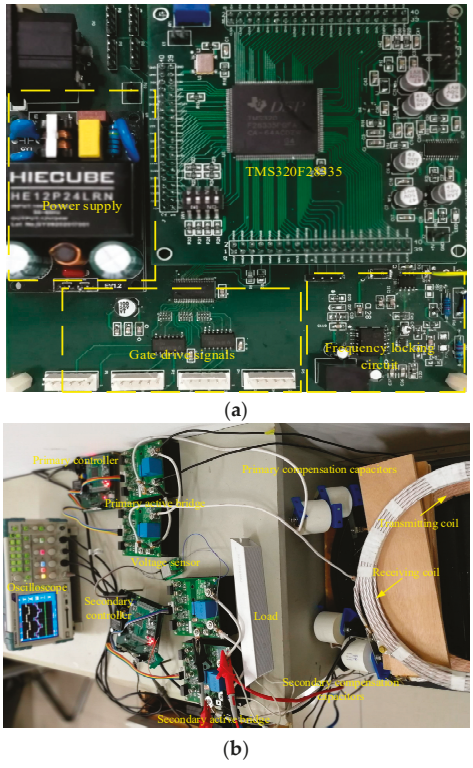


Figure 14. Photograph of WPT system with one active receiver: (**a**) DSP controller; and (**b**) overall system.

According to international standard of wireless electric vehicle charging SAE J2954 [34], the operating frequency of the WPT system ranges from 81. 38 kHz to 90 kHz. The worst possible synchronization scenario is investigated in this paper, that is, when f_1 is 90 kHz. The secondary operating frequency is also set at 90 kHz. Figure 15 shows the experimental result of v_1, v_2, i_2 and $V_{2,\mathrm{dc}}$ without proposed synchronization technique. Both α_1 and β_2 are 45°. $R_{\mathrm{L},2}$ is 50 Ω. The transient process is shown in the upper portion of the figure, whereas the corresponding enlarged details are shown in the lower portion. As evident from the figure, $V_{2,\mathrm{dc}}$ changes periodically at a frequency about 0.6 Hz. Because of the limited frequency precision of the microcontrollers, there exists 0.6 Hz frequency difference between the transmitter and the receiver. Although the frequency difference is small compared to 90 kHz operating frequency, φ_2 ranges from 0° to 360° at 0.6 Hz. Since $I_{2,\mathrm{dc}}$ is a cosine function according to (8), power oscillations appear. When φ_2 lies within a range of (90°, 270°), the power is transferred from the secondary side to the primary side. However, loading resistance is utilized in this experiment, which cannot provide the required power. Therefore, $V_{2,\mathrm{dc}}$ becomes zero during this phase range as shown in the lower part of Figure 15a. When φ_2 lies within a range of (−90°, 90°), the power is transferred to the secondary side and $V_{2,\mathrm{dc}}$ is a cosine function. In simulations, the frequency of the gate drive signal is identical to the preset one, which can be used to verify the above experiment. A simulation in Simulink is implemented and $f_1 - f_2$ is set at 0.6 Hz. The simulated result in Figure 15b agrees well with the experiment, which validates the synchronization analysis. It can be concluded that WPT systems with active receivers cannot function normally without applying synchronization techniques.

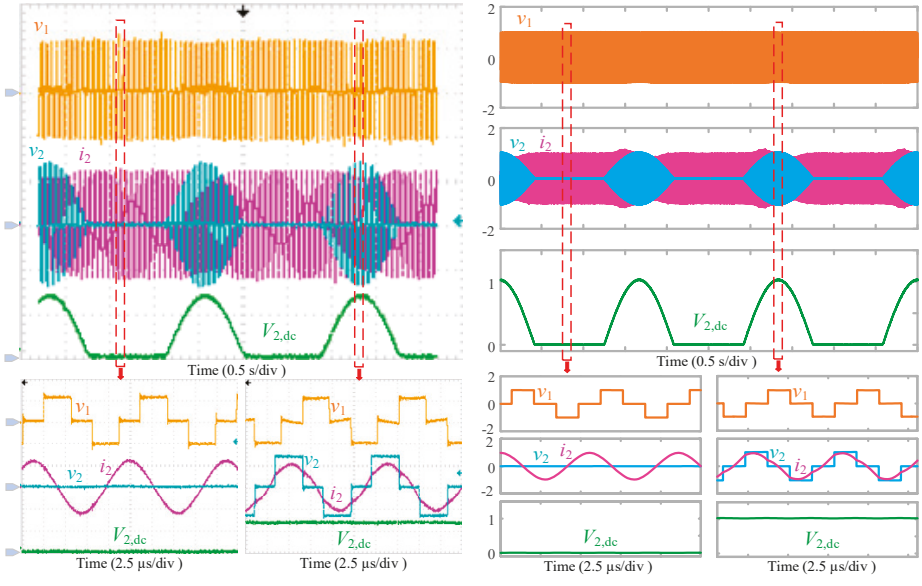


Figure 15. Power oscillations without synchronization: (**a**) experimental; and (**b**) simulated. v_1, 50 V/div; v_2 and $V_{2,dc}$,100 V/div; i_2, 5 A/div.

Figure 16 shows the experimental synchronization results of the proposed technique under various conditions, including v_{f2}, v_2, i_2 and $V_{2,dc}$. Figure 16a shows the typical experimental waveforms of the tuned WPT system. The input voltage, the phase angles and the load remain unchanged. The measured resonant frequency of the system is 91.5 kHz and the transmitter operates at this frequency. As can be seen in Figure 16a, the frequency locking signal v_{f2} is stable and v_2 is in phase with i_2. Figure 16b shows the typical waveforms of the detuned WPT system where the operating frequency is 90 kHz. The proposed synchronization technique performs well in the detuned WPT system. Figure 16c shows the experimental result during mutual inductance variation in the detuned WPT system. d_{12} changes from 120 mm to 80 mm, where the mutual inductance changes from 11.1 µH to 16.7 µH. $V_{2,dc}$ decreases with the increase of mutual inductance. As evident from the enlarged details, the system is stable and v_2 is still in phase with i_2. Figure 16d shows the experimental result during load variation in the detuned WPT system. $R_{L,2}$ changes from 50 Ω to 25 Ω by connecting the electronic load in parallel. Although $V_{2,dc}$ decreases by nearly half, v_2 and i_2 remain in phase.

The proposed synchronization system can work effectively with variations in operating frequency, coil position and load. Then, β_2 can be used to regulate the output power. Figure 17 shows the constant voltage power transfer process. The reference output voltage is set at 100 V. To guarantee the transferred power, $V_{1,dc}$ is increased to 80 V in this experiment. The load changes from 50 Ω to 25 Ω. To better record and observe the transition, β_2 is varied by 1° each 100 millisecond in this experiment. As evident from the figures, β_2 increases with decreasing $R_{L,2}$ to supply more power and $V_{2,dc}$ stabilizes at the desired 100 V within 0.25 s. The setting period can be decreased by reducing the observation time and increasing the increment or decrement to β_2. The received power increases from 200 W to 400 W and the dc-to-dc efficiency increases from 91.5% to 92.3%. For operational convenience, a magnetic core has not been used on the receiver side. The coupling factor can be increased by installing a magnetic core, which can improve the overall efficiency.

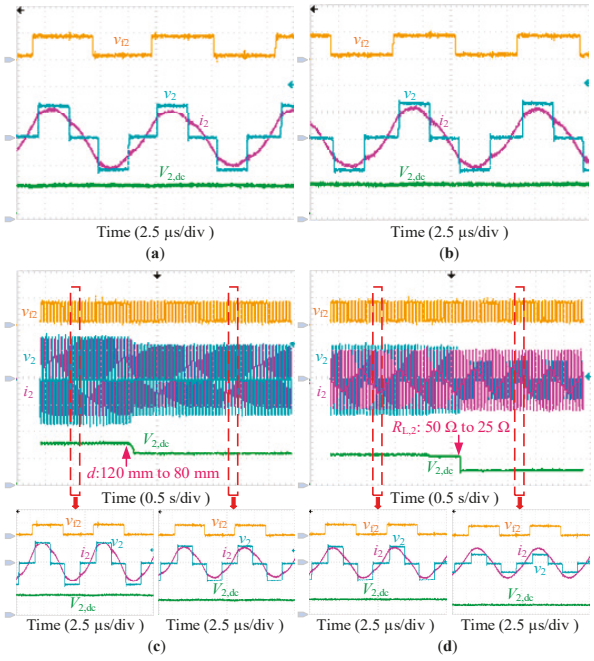


Figure 16. Experimental synchronization results of proposed technique under various conditions: (**a**) tuned WPT system; (**b**) detuned WPT system; (**c**) mutual inductance variation in detuned WPT system; and (**d**) load variation in detuned WPT system. v_{f2}, 5 V/div; v_2 and $V_{2,dc}$, 100 V/div; i_2, 5 A/div.

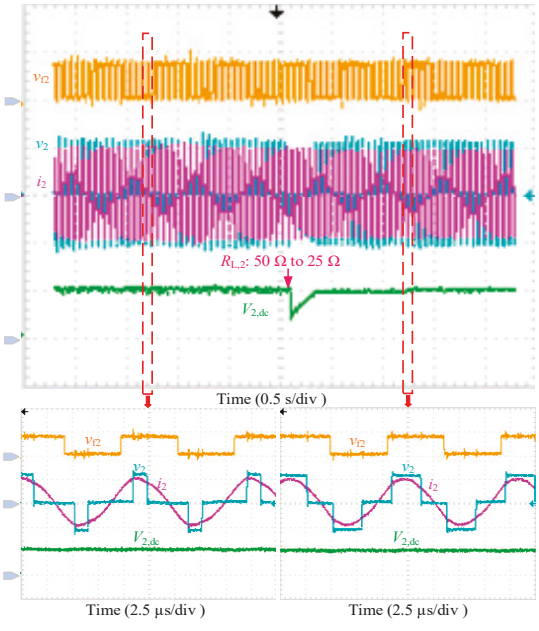
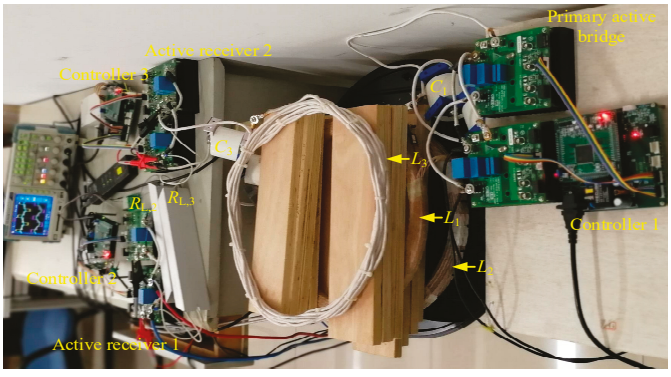


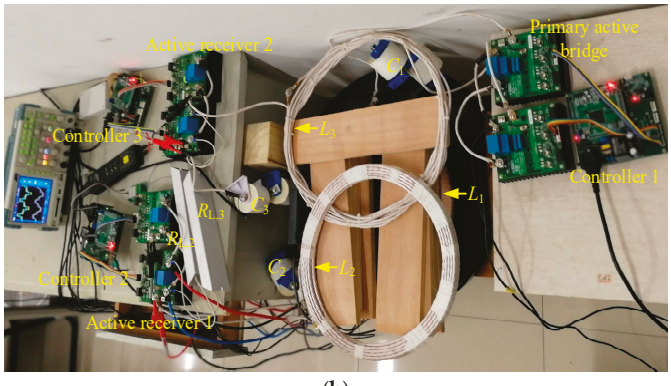
Figure 17. Constant voltage power transfer. v_{f2}, 5 V/div; v_2 and $V_{2,dc}$, 100 V/div; i_2, 10 A/div.

4.2. Multiple Active Receiver Wpt System

Figure 18a,b show the photographs of the multiple active receiver WPT systems without and with cross coupling between receiver-side coils, respectively. $V_{1,dc}$ is 50 V and α_1 is set at 45°. $R_{L,2}$ and $R_{L,3}$ are 50 Ω. L_3 is 81 μH, compensated by 0.04 μF AC capacitor. The calculated resonant frequency of receiver 2 is 88.5 kHz. The systems operates at 90 kHz, that is, the complex detuned condition. To confirm that the receivers can work under different conditions, β_2 is set at 45° and β_3 at 30°. In Figure 18a, the transmitting coil lies in the middle and the cross coupling between the two receiving coils is neglected. Both d_{12} and d_{13} are 80 mm. M_{12} and M_{13} are 21.2 μH and 16.7 μH, respectively. In Figure 18b, the receivers are put on the above. Except for the mutual inductances among the coils, the system parameters remain the same. M_{12}, M_{13} and M_{23} are 8.9 μH, 11.7 μH and 4.8 μH, respectively. The cross coupling mutual inductance between the receiving coils is comparable with the mutual inductances.



(**a**)



(**b**)

Figure 18. Multiple active receiver WPT systems without and with cross coupling between receiver-side coils: (**a**) without cross coupling; and (**b**) with cross coupling.

Figure 19a shows the typical waveforms of the successful synchronization result without crossing coupling, including v_2, i_2, v_3 and i_3. As evident from the figure, v_2 and v_3 are in phase with i_2 and i_3, respectively. The power is transferred to the active receivers successfully. Figure 19b shows the typical waveforms of the system with cross coupling between two receiver-side coils. The synchronization system performs well and the WPT system is stable. These experiments confirm the feasibility of the proposed synchronization technique in multiple active receiver WPT systems.

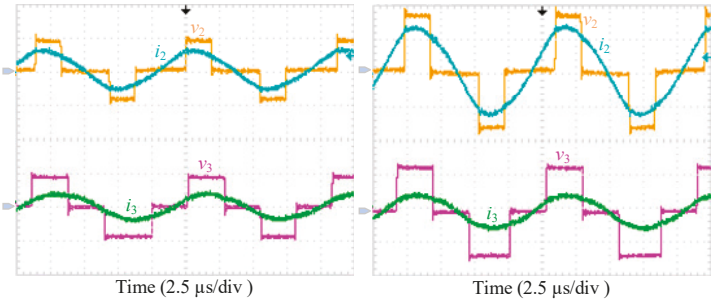


Figure 19. Successful synchronization results of multiple active receiver systems without and with cross coupling between receiver-side coils: (**a**) without cross coupling; and (**b**) with cross coupling. v_2 and v_3, 50 V/div; i_2 and i_3, 5 A/div.

4.3. Discussion

This paper provides a comprehensive synchronization analysis of different WPT systems and decomposes the synchronization system into independent frequency locking and reference phase calibration. Table 2 summarizes the comparisons of different synchronization techniques. The inverter's operating frequency is 20 kHz in References [6,17], 30 kHz in Reference [20] and 85 kHz in Reference [29]. A higher operating frequency can amplify the phase errors observed in Reference [17]. Thus, the synchronization difficulty increases with the increasing frequency. The proposed system can operate at 90 kHz, validating the effectiveness of proposed frequency locking method. In addition, the proposed synchronization technique is independent of system parameters and the phase error can be calibrated in advance. Thus, it can perform well under different conditions such as frequency variation, mutual inductance variation, load variation and so forth. Usually, a critical and parameter-sensitive phase-shift circuit is needed to compensate the phase error caused by time delay. However, it is easier to achieve reference phase calibration by software code, which reduces the complexity and cost of the synchronization circuit. Although the proposed technique is validated through a resistance load, it can be effectively applied to battery charging and bidirectional power transfer systems.

Table 2. Comparisons of different synchronization techniques.

Source	Operating Frequency	Frequency Variation	Mutual Induction Variation	Load Variation	Multiple Receivers	Phase Calibration Method	Complexity
[6]	20 kHz	×	×	√	×	N/A	N/A
[17]	20 kHz	×	√	√	×	Circuit-based	Complex circuit and algorithm
[20]	30 kHz	×	×	√	×	Circuit-based	N/A
[29]	85 kHz	×	√	√	×	Circuit-based	Complex circuit and algorithm
This paper	90 kHz	√	√	√	√	Software Code	Simple circuit and simplified algorithm

5. Conclusions

This paper presents a detailed synchronization analysis of WPT systems with active receivers. The synchronization problem is decomposed into two independent parts: frequency locking and reference phase calibration. Based on the analysis, a novel synchronization technique is proposed where frequency locking is realized through the hardware circuit and reference phase calibration is achieved through software code, which is a great progress for synchronization system design. In experiments, frequency locking can be realized at 90 kHz and reference phase calibration only requires one execution after the system is implemented. The proposed synchronization technique adapts to multiple active

receivers under tuned and detuned conditions. In addition, the synchronization system performs well when key system parameters vary. Constant voltage power transfer can be realized with 92.3% dc-to-dc efficiency at 400 W received power. The feasibility and effectiveness of the proposed synchronization technique have been verified by theoretical analysis and experimental results.

Supplementary Materials: The following are available online at https://zenodo.org/record/1485267#.W-qdtFLFKJ0.

Author Contributions: X.L., H.T. and X.Y. conceptualized the main idea of this research project; X.L. designed and conducted the experiments with the help of T.W.; N.J. and X.Y. checked the results. X.L. wrote the whole paper; N.J. and K.H. reviewed and edited the paper.

Funding: This research was funded by United Foundation of NSFC-Henan, grant number U1604136. The APC was funded by Xijun Yang.

Conflicts of Interest: The authors declare no conflict of interest.

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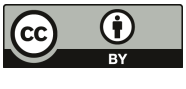

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Article

A Novel Single-switch Phase Controlled Wireless Power Transfer System

Xin Liu [1], Nan Jin [2], Xijun Yang [1], Khurram Hashmi [1], Dianguan Ma [1,*] and Houjun Tang [1]

[1] Key Laboratory of Control of Power Transmission and Transformation Ministry of Education, Shanghai Jiao Tong University, 800 Dongchuan RD., Shanghai 200240, China; Liu_xin@sjtu.edu.cn (X.L.); yangxijun@sjtu.edu.cn (X.Y.); khurram_hashmi@sjtu.edu.cn (K.H.); hjtang@sjtu.edu.cn (H.T.)

[2] College of Electric and Information Engineering, Zhengzhou University of Light Industry, Zhengzhou 450002, China; jinnan@zzuli.edu.cn

* Correspondence: dgma@sjtu.edu.cn; Tel.: +86-138-1758-7820

Received: 6 October 2018; Accepted: 25 October 2018; Published: 29 October 2018

Abstract: Battery charging is a fundamental application of Wireless Power Transfer (WPT) systems that requires effective implementation of Constant Current (CC) and Constant Voltage (CV) power conduction modes. DC-DC converters used in WPT systems utilize large inductors and capacitors that increase the size and volume of the system in addition to causing higher DC losses. This work proposes a novel single-switch active rectifier for phase controlled WPT systems that is smaller in volume and weight as compared to conventional WPT topologies. The proposed method simplifies the control scheme using improved Digital Phase Control (DPC) and Analog Phase Control (APC) to realize the CC and CV power transfer modes. Furthermore, it prevents forward voltage losses in Silicon Carbide (SiC) switches and shoot through states with improved switching patterns. Simulation studies and experimental results are added to verify the effectiveness of the proposed methodology.

Keywords: active rectifiers; single-switch; analog phase control; digital phase control; wireless power transfer

1. Introduction

WPT techniques can realize energy conversion without physical connections. It has gained tremendous attention in both research and industry. Recently, wireless charging is the focus of study. To improve battery life time, the system has special requirements for the charging current and voltage profiles. WPT systems can realize both CC and CV power transfer modes through either primary or secondary side control. However, primary side control requires an additional communication channel [1,2]. It is more simplified and straightforward to directly achieve the CC and CV power transfer modes through secondary side control. Therefore, various DC-DC converters [3–8] are installed on the receiver side for power regulation, including buck converter [4], boost converter [5,9,10], and buck-boost converter [6,11]. Although DC-DC converters have simpler controls, they require additional capacitors and inductors that increase the weight, volume, and cost of the receiver. In addition, more cascaded circuits result in more losses on the DC side. To address these drawbacks, researchers propose active rectifiers on the receiver side. Active rectifiers are initially put forward to reduce the conduction losses of the diode rectifier and transfer the power bi-directionally [12–19]. Recently, Phase Control (PC) method is introduced to regulate resonant currents [20–25], which can further reduce the energy consumed by parasitic resistances.

Active rectifiers proposed for WPT systems can be classified into three categories: (i) full bridge rectifier with four switches; (ii) semi-bridgeless rectifier with two switches; and (iii) single- switch rectifier. Full active bridge rectifiers are used in various applications [12–25]. Four Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) and four isolated driver circuits are installed on

the receiver side. Short circuit may appear in the full bridge topology due to faulty operation. Such a characteristic reduces the reliability of the WPT systems, especially battery charging systems where short circuit can lead to fire and explosion. It is desirable to investigate a more cost-effective and reliable approach to achieve secondary PC. Therefore, researchers in [26–28] develop two-switch rectifiers for WPT systems. In [26,27], a semi-bridgeless topology with two MOSFETs is proposed, where two switches are installed on the lower side of the rectifier. Secondary PC can be achieved as well. In [28], two MOSFETs are in reverse connection and controlled by one signal. Duty ratio control is applied to regulate the power. Furthermore, researchers in [29–36] investigate single-switch rectifiers. In [29], a switch is connected in parallel with a resonant compensation capacitor. Power regulation can be achieved by tuning/detuning through this variable capacitor. However, this method makes the system deviate from optimal resonant point, which may cause an efficiency drop. In [30–32], a switch is connected in series with parallel resonant tank. When the switch is turned off, the receiver transfers the power only in half the period. In addition, it is difficult to obtain a stable DC voltage. In [33], an active switch is inserted into the lower phase leg of a full diode bridge. When the switch is turned on, the resonant tank is shorted in half the period and the power can be regulated by duty ratio control. In [34–36], a boost converter is directly connected after the diode bridge which reduces one filter capacitor.

Active rectifiers with two or four switches can realize PC [12–27], whereas previous single-switch rectifiers can only adopt duty ratio control [29–36]. Although duty ratio control is easier to implement, it can cause resonant current oscillations when the power transfer path is chopped. It requires larger filter capacitors to maintain the desired DC voltage. In addition, single-switch receivers in [29–33] are half-controlled, i.e., their power regulation abilities are restricted, which may fail to meet the CC and CV power transfer requirements.

This paper proposes a novel single-switch phase controlled receiver for WPT systems for the first time. With this method, the secondary side inductor is removed and only a small filter capacitor is added, thereby reducing the size of the receiver and lessening the number of switches used. The salient contributions of this work are:

(1) The proposed methodology reduces the number of active switches and isolated driver circuits as compared to conventional phase controlled receivers.
(2) An APC method is applied to this improved receiver that circumvents synchronization algorithms and additional programming. APC method regulates the power automatically, which reduces the difficulty in design and implementation.
(3) Most previously discussed single-switch methods are half-controlled and use duty ratio variation. In this work, the receiver is fully controlled and has a stronger power regulation ability as compared to conventional single-switch receivers.
(4) The proposed receiver fully utilizes the SiC MOSFET to reduce switching losses while avoiding high forward voltage losses through its intrinsic diode.

This paper is divided as follows: Section 2 shows the proposed single-switch receiver and illustrates its operating modes. Then, it presents the derivations for the CC and CV power transfer modes. Section 3 elaborates the detailed implementation techniques of the proposed DPC and APC methods. In Section 4, simulations and experiments are added to validate the feasibility and effectiveness of the proposed topology and control methods. Finally, Section 5 concludes this paper.

2. Modeling and Analysis

This section presents mathematical modeling and analysis for the proposed WPT system.

2.1. Proposed Topology

A WPT system with the proposed single-switch receiver is shown in Figure 1. U_i and U_o are the DC voltages, whereas v_p and v_s are the primary and secondary resonant voltages. L_p and L_s are the

primary and secondary coil inductances, which are compensated by C_p and C_s, respectively. S_1–S_5 are the SiC MOSFETs, and D_1–D_5 are the diodes. C_i and C_o are the filter capacitors, and R_L is the load. i_1 and i_2 are the currents flowing through S_5 and D_5, respectively. I_i and I_o denote the input and output DC currents.

The typical waveforms of the proposed topology are shown in Figure 2, where 2β presents the phase angle of v_s. According to the current directions and paths, the receiver has six operating modes as depicted in Figure 3.

Mode 1: $i_s > 0$, and S_5 is on. There exist two current loops on the receiver side: L_s–D_1–S_5–D_4–C_s and C_o–R_L. The diode bridge is short-circuited by S_5, and I_o is supplied by C_o. Thus, v_s is zero.

Mode 2: $i_s > 0$, and S_5 is turned off at the beginning of Mode 2. C_o charges, and U_o increases. Thus, the current loop is L_s–D_1–D_5–U_o–D_4–C_s. v_s is basically equal to U_o.

Mode 3: $i_s > 0$, and S_5 is turned on at the beginning of Mode 3. Then, i_s flows through S_5 and v_s becomes zero. U_o is supplied by C_o, and it begins to decrease. The current loops are: L_s–D_1–S_5–D_4–C_s and C_o–R_L.

Mode 4: S_5 remains on and v_s. remains zero, whereas i_s changes its direction. U_o continues to decrease. The current loop of i_s becomes L_s–C_s–D_3–S_5–D_2.

Mode 5: $i_s < 0$, and S_5 is turned off at the beginning of Mode 5. C_o charges via i_s, and U_o begins to increase. The current loop is L_s–C_s–D_3–D_5–U_o–D_2. v_s is basically equal to $-U_o$.

Mode 6: $i_s < 0$, and S_5 is turned on at the beginning of Mode 6. The current loop of i_s becomes L_s–C_s–D_3–S_5–D_2, and U_o is supplied by C_o again.

To minimize switching losses, a SiC MOSFET can be used. Since the forward voltage of the intrinsic diode of the SiC MOSFET is high, a SiC diode is connected in parallel to overcome the high forward voltage loss of the intrinsic diode. However, no current freewheels through S_5 in the proposed receiver, which means the SiC diode is not necessary in this application. Therefore, the proposed receiver can fully utilize the SiC MOSFET to reduce switching losses while avoiding its drawback of high forward voltage losses through its intrinsic diode.

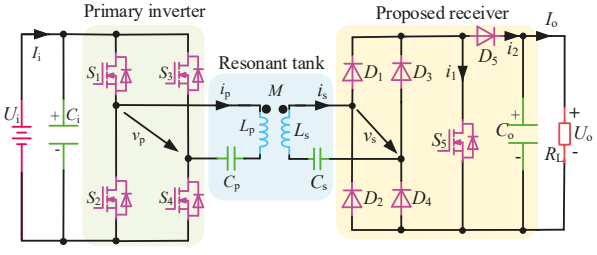

Figure 1. WPT system with proposed single-switch receiver.

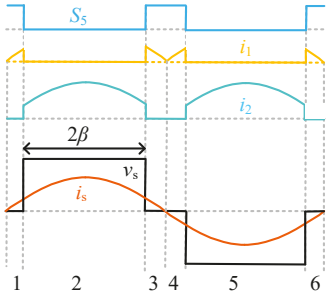

Figure 2. Typical waveforms of proposed receiver. S_5, gate drive signal (blue line); i_1, current flowing through MOSFET (yellow line); i_2, current flowing through D_5 (light green line); i_s, secondary resonant current (orange line); v_s, secondary resonant voltage (black line).

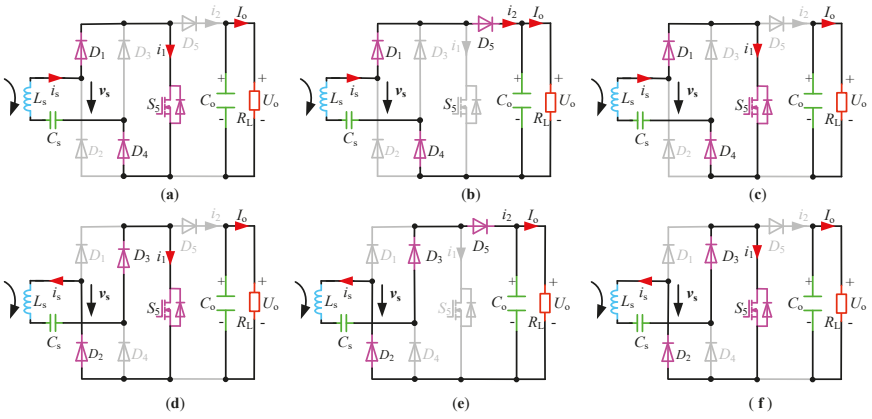

Figure 3. Operating modes of proposed receiver: (**a**) Mode 1; (**b**) Mode 2; (**c**) Mode 3; (**d**) Mode 4; (**e**) Mode 5; and (**f**) Mode 6.

2.2. Power Regulation

The CC and CV power transfer realizations are the basic requirements for battery charging systems. This section presents the theoretical analysis of secondary side control through proposed single-switch phase-controlled receiver.

The system operates at the resonant frequency, that is

$$\omega = \frac{1}{\sqrt{L_p C_p}} = \frac{1}{\sqrt{L_s C_s}} \tag{1}$$

R_p and R_s represent primary and secondary coil resistances, respectively. Then, the following equations are obtained according to Kirchhoff Voltage Law (KVL).

$$v_p = -j\omega M i_s + i_p R_p \tag{2}$$

$$j\omega M i_p = v_s + i_s R_s \tag{3}$$

According to Fourier series and fundamental harmonic analysis [23–25], the root-mean-square value of v_s (V_s) can be denoted as:

$$V_s = \frac{2\sqrt{2}}{\pi} U_o \sin\beta. \tag{4}$$

Without considering the switching losses, the input and output powers of the rectifier are equal.

$$V_s I_s \simeq U_o I_o \tag{5}$$

Then, I_o versus I_s is deduced.

$$I_o \simeq \frac{2\sqrt{2}\sin\beta}{\pi} I_s \tag{6}$$

According to Equation (2), i_s can be rewritten as

$$i_s = \frac{v_p - i_p R_p}{-j\omega M} \simeq \frac{v_p}{-j\omega M} \tag{7}$$

Thus, I_o and U_o can be approximately derived as Equations (8) and (9).

$$I_o \simeq \frac{2\sqrt{2}\sin\beta}{\pi\omega M} V_p \tag{8}$$

$$U_o \simeq \frac{2\sqrt{2}R_L \sin\beta}{\pi\omega M} V_p \tag{9}$$

A larger β means a larger I_o and U_o. Therefore, β can be utilized to achieve the CC and CV power transfer modes.

3. Implementation Methods

This section presents implementation techniques for realizing DPC and APC with the proposed receiver in WPT system.

3.1. Digital Phase Control

The schematic of the DPC system is shown in Figure 4, where two independent Digital Signal Processors (DSPs) are installed. Digital control is widely used for various applications due to its flexibility. Since the controller should be isolated from the main circuit for safety consideration, isolated driver circuits as well as isolated power supplies are installed on primary and secondary sides. Furthermore, isolated current and voltage sensors are required on the receiver side for output electrical information feedback. To avoid power oscillations, the synchronization of secondary receiver is of essential importance. In [24], secondary synchronization is realized by utilizing the resonant voltage across C_s. The synchronization circuit consists of a comparator and an isolator, as shown in Figure 4, where R_h and R_l are the divider resistances. The operating frequency of the receiver-side switches in the full active bridge is equal to the current frequency, whereas it is twice that frequency in the proposed receiver. Thus, the receiver is synchronized once every two periods.

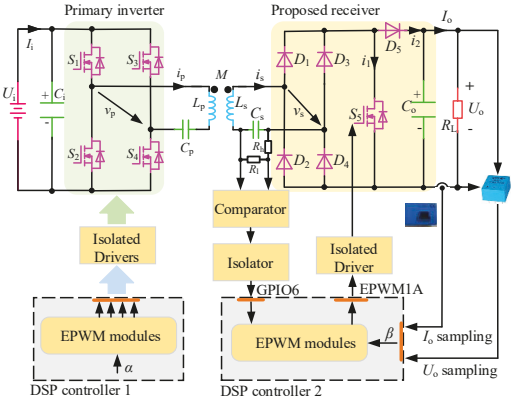

Figure 4. Schematic of DPC system.

Figure 5 shows the typical synchronization waveforms. The comparator turns the divided sinusoidal voltage into a square-wave synchronization signal. After passing a digital isolator, it is sent to the synchronization port of the DSP controller. TBPRD, CMPA, and CMPB are the time base period and comparing values of the reserved registers of the controller, respectively. The 0 and TBPRD shown in Figure 5 are the minimum and maximum values of the counter of the controller, i.e., CMPA and CMPB fall within the range of [0, TBPRD]. When the counter reaches CMPA, S_5 is turned off. When the counter reaches CMPB, S_5 is turned on. The relationships among TBPRD, CMPA, CMPB, and β are shown in Equations (10) and (11).

$$\text{CMPA} = \frac{180 - \beta}{180}\text{TBPRD} \tag{10}$$

$$\text{CMPB} = \frac{\beta}{180}\text{TBPRD} \tag{11}$$

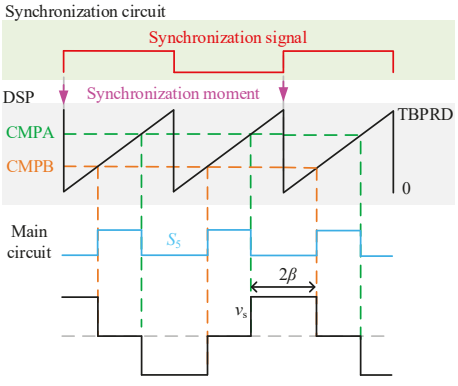

Figure 5. Typical synchronization waveforms.

TBPRD is determined by the inverter frequency, and the comparing values produce the desired β. Afterwards, the corresponding gate drive signal generates v_s in the main circuit.

As analyzed in Section 2, a larger β brings about larger I_o and U_o. Therefore, the output power regulation can be achieved by changing β. The algorithm flowchart of the CC and CV power transfer modes is shown in Figure 6, where I_o^* and U_o^* are the expected current and voltage values. Power transfer mode selection is determined by one bit, referred to as "Mode", which is defined in the controller. The designer can initialize the Mode by setting it at 1 or 0 in the software code. When the Mode is 1, the receiver operates at the CC power transfer mode, otherwise, it operates at the CV power transfer mode. I_o is sampled for the CC power transfer mode, and U_o for the CV power transfer mode. To obtain accurate sampling values, 20 samplings of I_o or U_o are averaged. β ranges from 0° to 90°. When I_o or U_o is smaller than the desired value, β is increased by 0.1°. Otherwise, β is decreased by 0.1°. This control algorithm is simple and effective. The primary controller is turned on and the primary active bridge inverts the high frequency voltage. The frequency locking signal is generated, whereas the receiver-side controllers remain on standby and the diode rectification is used by the receiver at first. When U_o reaches the threshold value, the controller is turned on.

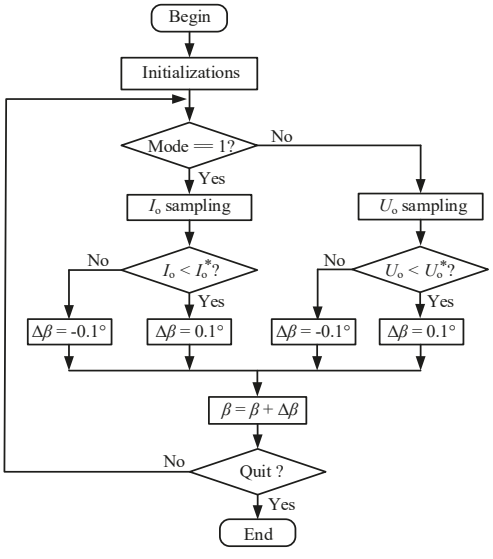

Figure 6. Algorithm flowchart of DPC receiver.

In full active bridge receivers, four gate drive signals should be controlled to generate v_s. However, β is determined by one signal in the proposed receiver, which makes the software code realization easier.

3.2. Analog Phase Control

The DPC method can achieve good control flexibility and performance. However, the receiver requires some auxiliary circuits. To further reduce the complexity and cost of the receiver, a novel APC method is presented as follows.

The schematic of the proposed APC system is shown in Figure 7. R_1 and R_2 are the divider resistances. R_3 and R_9 are the sampling resistances. The voltage across R_3 is fed back for the CC power transfer, and the divided voltage across R_2 for the CV power transfer. Since R_3 is small, and R_4 and R_5 are used to amplify the signal. In APC system, power transfer mode selection is realized by a 2:1 switch. R_1–R_5 should satisfy Equation (12).

$$I_o^* R_3 \frac{R_4 + R_5}{R_4} = U_o^* \frac{R_2}{R_1 + R_2} \tag{12}$$

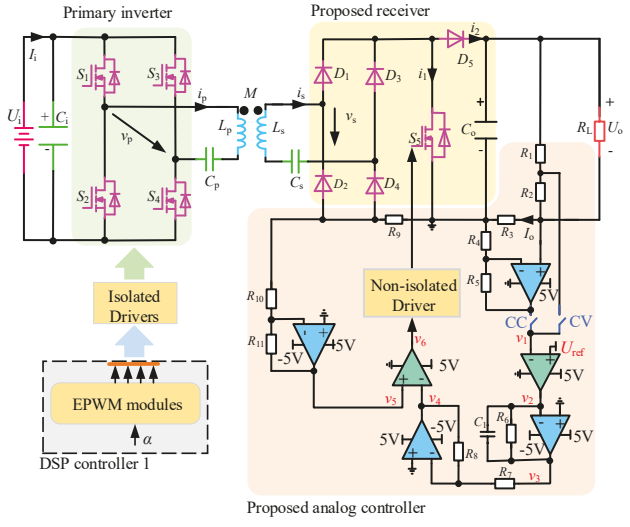

Figure 7. Schematic of APC system.

U_{ref} is a reference voltage. The relationships among U_o^*, I_o^*, and U_{ref} are given in Equations (13) and (14). Different output current and voltage can be achieved by setting U_{ref} and R_1–R_5.

$$I_o^* = \frac{U_{ref} R_4}{R_3(R_4 + R_5)} \tag{13}$$

$$U_o^* = \frac{U_{ref}(R_1 + R_2)}{R_2} \tag{14}$$

R_6 and C_1 act as an integrator. Their values have a great influence on the dynamic and static performances of the system. To better demonstrate this characteristic, time constant τ is defined as Equation (15).

$$\tau = R_6 C_1 \tag{15}$$

A smaller τ brings about a faster dynamic response with a larger overshoot, whereas a larger τ corresponds to a better static performance with a slower dynamic response.

Figure 8 shows the typical waveforms of the APC receiver. When I_o (or U_o) is greater than I_o^* (or U_o^*), v_1 is greater than U_{ref}, and the comparator generates a zero v_2. Otherwise, a positive v_2 is produced. v_3 decreases for a positive v_2 and increases for a zero v_2. Since v_3 is negative, an inverting amplifier is used. The ratio of R_8 versus R_7 can regulate the response characteristic. i_s flows through R_9, and the voltage drop is amplified by R_{10} and R_{11}, which obtains a half-wave voltage v_5. Then, v_4 and v_5 are sent to a comparator, and they can produce the desired control signal. After passing the non-isolated driver circuit, the gate drive signal is fed to the switch. When S_5 is turned on, the receiver is short-circuited, which results in a zero v_s. When S_5 is turned off, v_s becomes U_o or $-U_o$. β is automatically regulated by the feedback signals.

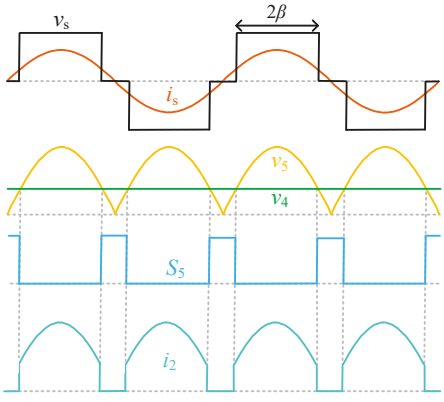

Figure 8. Typical waveforms of APC receiver. i_s, secondary resonant current (orange line); v_s, secondary resonant voltage (black line); v_4, feedback signal (green line); v_5, half-wave signal (yellow line); S_5, gate drive signal (blue line); i_2, current flowing through D_5 (light green line).

The CC and CV power transfer modes can be achieved through the proposed analog controller. Meanwhile, the receiver does not require synchronization techniques and additional programming. Thus, the proposed APC method significantly reduces the difficulty in implementation, the cost, volume, and weight of the receiver.

4. Simulation and Experiment

Results are obtained from simulation studies in PLECS and hardware prototype experiments. Both results are presented and compared to validate the feasibility of the proposed topology and control methods. The main parameters of the WPT system are listed in Table 1. L_p and L_s are 150 μH and 200 μH with a coil distance of 10 cm. The primary and secondary coils are compensated by 23 nF and 17 nF resonant capacitors, respectively. The inverting frequency of the transmitter is 85 kHz. The diodes are MUR3020PT, with a low forward voltage drop of 1 V. SiC MOSFETs are SCT3030KL. Heat sinks are installed on each diode and MOSFET.

Table 1. Main parameters of WPT system.

Symbol	Quantity	Value
L_p	coil inductance of transmitter	150 μH
L_s	coil inductance of receiver	200 μH
C_p	primary compensation capacitance	23 nF
C_s	secondary compensation capacitance	17 nF
f	inverting frequency	85 kHz

4.1. Digital Phase Control

The prototype photograph of the DPC system is shown in Figure 9. Two TMS320F28335 chips are used as the primary and secondary controllers. The transmitter inverts the DC voltage into high frequency resonant voltage v_p. Then, v_s is induced by the magnetic field generated by i_p. Afterwards, secondary resonant current i_s is rectified into DC current I_o by the proposed receiver. Finally, the power is consumed by Chroma programmable AC-DC electronic load model 63803. Current and voltage sensors are installed to sample the feedback signals for power regulation. ACPL-W346 chips are used as the isolated drivers which are supplied by isolated DC-DC converter G1212S-2W.

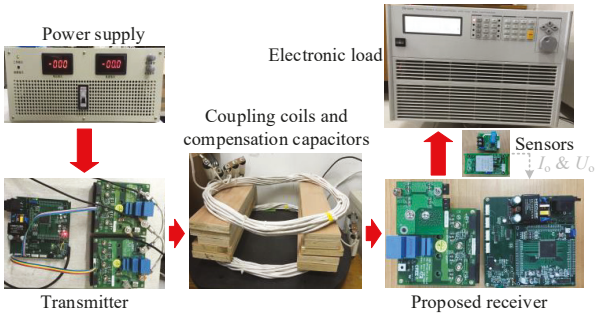

Figure 9. Prototype photograph of DPC system.

Figure 10 shows the typical waveforms of the DPC receiver. To ensure that the signal fed to the comparator stays within a proper range, the values of the divider resistances should be configured with the power level. In this paper, the high-side resistance R_h is 2 MΩ and the low-side resistance R_l is 10 kΩ. The voltage across C_p generates the synchronization signal, and it is fed to GPIO6 of the controller. v_s and i_s are controlled to be in phase. The desired output voltage or current is realized by regulating β.

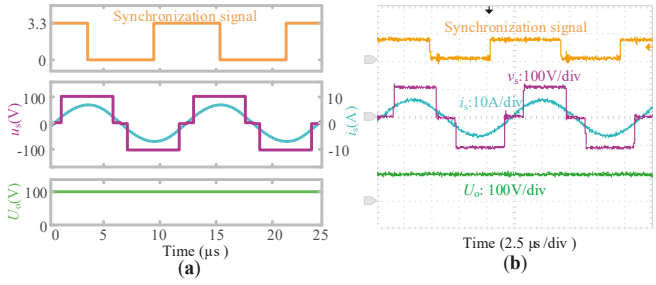

Figure 10. Typical waveforms of DPC receiver: (**a**) simulated; and (**b**) experimental. Synchronization signal (yellow lines); i_s, secondary resonant current (blue lines); v_s, secondary resonant voltage (purple lines); U_o, output voltage (green lines).

Figure 11a,b shows the simulated and experimental CC power transfer results by DPC. The reference current is set at 2 A, and R_L changes from 25 Ω to 50 Ω. When R_L is 25 Ω, the simulated and experimental values of β are 27.8° and 27.4°, respectively. The simulated and experimental output currents are 2.00 A and 1.96 A, which correspond to 83.3% and 80.8% DC-to-DC efficiencies, respectively. When R_L is 50 Ω, the simulated and experimental values of β are 28.6° and 27.5°, respectively. The simulated and experimental output currents are 1.99 A and 1.97 A, with DC-to-DC efficiencies of 90.0% and 86.2%, respectively. I_o keeps unchanged against load variations.

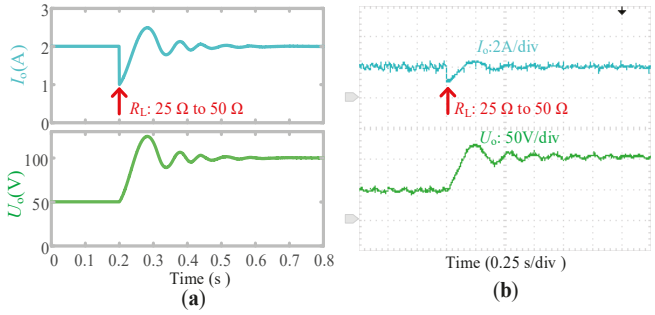

Figure 11. Simulated and experimental CC power transfer results of DPC system: (**a**) simulated; and (**b**) experimental. I_o, output current (blue lines); U_o, output voltage (green lines).

Figure 12a,b shows the simulated and experimental CV power transfer results by DPC. The reference voltage is set at 100 V. When R_L is 25 Ω, the simulated and experimental values of β are 73.9° and 73.5°, which produce 100.0 V and 101.2 V output voltages, respectively. The simulated and experimental efficiencies are 93.1% and 91.4%, respectively. When R_L is 50 Ω, the simulated and experimental values of β become 27.7° and 28.1°, respectively. The corresponding output voltages are 99.5 V and 100.5 V, with DC-to-DC efficiencies of 90.0% and 85.8%, respectively. During load variations, U_o remains at the desired level by regulating β accordingly.

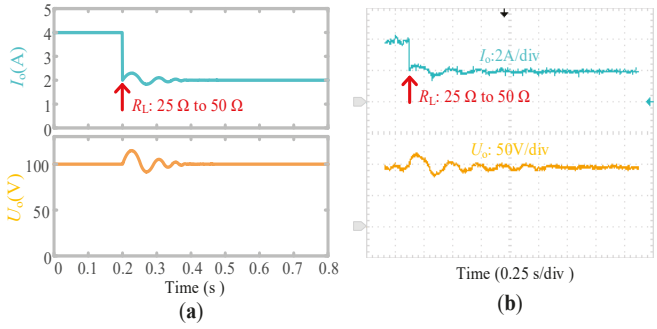

Figure 12. Simulated and experimental CV power transfer results of DPC system: (**a**) simulated; and (**b**) experimental. I_o, output current (blue lines); U_o, output voltage (yellow lines).

4.2. Analog Phase Control

A photograph of the APC receiver is shown in Figure 13. U_{ref} is set at 2.5 V. The divider resistances R_1 and R_2 are 91 kΩ and 2.2 kΩ, respectively. The sampling resistances R_3 and R_9 are 10 mΩ. R_4 and R_5 are 0.5 kΩ (1 kΩ//1 kΩ) and 62 kΩ, respectively. The ratios of R_7 versus R_8 and R_{11} versus R_{10} are 1 and 22, which ensures v_4 and v_5 falling within proper ranges. TLV3502 and THS4062 are used as the comparator and the operational amplifier, respectively. The configurations of the simulations are identical to the experimental prototype.

Figure 14 shows the logical waveforms of the APC receiver, including v_4, v_5, v_6, and v_s. Regulation circuits are installed on the main circuit. v_4 and v_5 are sent to TLV3502 which generates the control signal. When v_5 is smaller than v_4, v_6 becomes high level, and S_5 is turned on. Otherwise, v_6 becomes low level, and S_5 is turned off. Small oscillations appear in v_6, which should be interferences caused by the switching processes. When I_o or U_o is smaller than the expected value, v_4 decreases which brings about a larger β. Otherwise, v_4 increases, and a smaller β is produced.

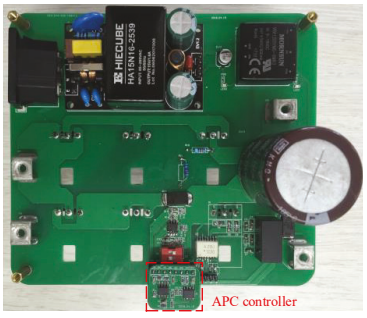

Figure 13. Photograph of APC receiver.

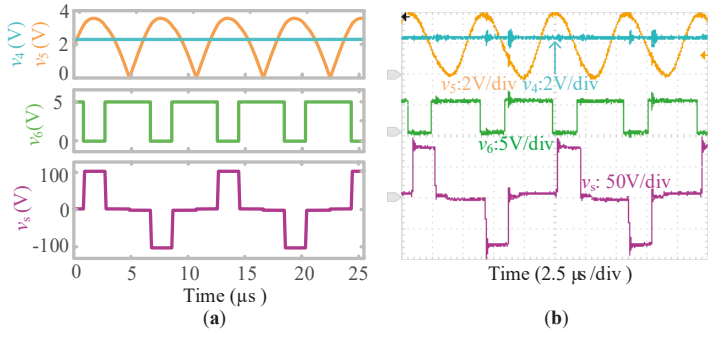

Figure 14. Logical waveforms of APC receiver: (**a**) simulated; and (**b**) experimental. v_4, feedback signal (blue lines); v_5, half-wave signal (yellow lines); v_6, control signal (green lines); v_s, secondary resonant voltage (purple lines).

Figure 15 shows the typical waveforms of the APC receiver. In simulations, v_s is in phase with i_s. However, in experiments, it takes some time for the signal to go through the operational amplifier, the comparator, the DSP, and the driver circuit. This time delay results in v_s lagging i_s by some degrees. High performance devices can reduce this time delay.

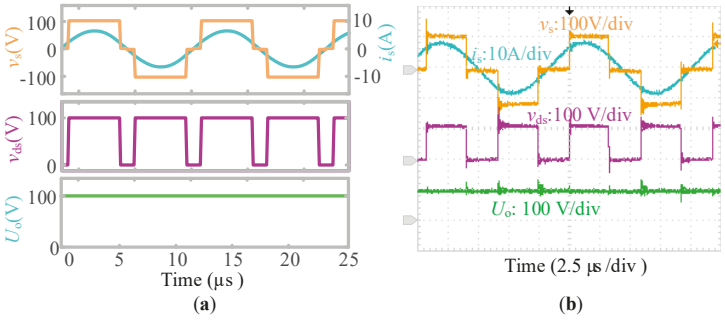

Figure 15. Typical waveforms of APC receiver: (**a**) simulated; and (**b**) experimental. I_s: secondary resonant current (blue lines); v_s, secondary resonant voltage (yellow lines); v_{ds}, voltage across S_5 (purple lines); U_o, output voltage (green lines).

Figure 16a,b shows the simulated and experimental results of the CC power transfer by APC. When R_L is 25 Ω, the simulated and experimental output currents are 1.99 A and 1.98 A, respectively.

The simulated and experimental DC-to-DC efficiencies are 82.5% and 78.2%. When R_L is 50 Ω, the simulated and experimental output currents are 1.99 A and 1.94 A, which correspond to 89.5% and 85.2% DC-to-DC efficiencies, respectively. In the CC mode, I_o maintains at the desired 2 A against load variations.

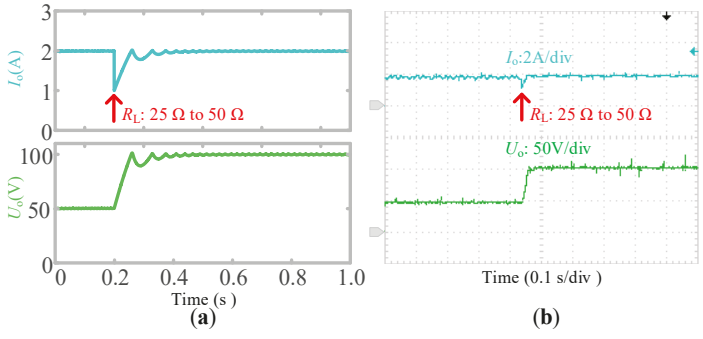

Figure 16. Simulated and experimental CC power transfer results of APC system: (**a**) simulated; and (**b**) experimental. I_o, output current (blue lines); U_o, output voltage (green lines).

Figure 17a,b shows the simulated and experimental results of the CV power transfer by APC. The reference voltage is set at 100 V. When R_L is 25 Ω, the simulated and experimental output voltages are 99.7 V and 103.7 V, whose DC-to-DC efficiencies are 92.2% and 88.9%, respectively. When R_L is 50 Ω, the simulated and experimental output voltages are 99.5 V and 104.6 V, respectively. The overall simulated and experimental efficiencies are 89.4% and 84.7%, respectively. In the CV mode, U_o remains unchanged against load variations.

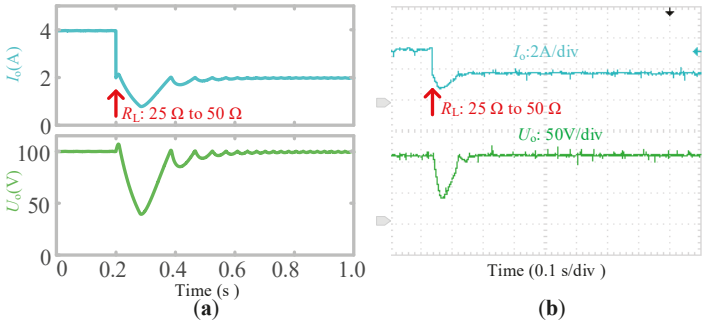

Figure 17. Simulated and experimental CV power transfer results of APC system: (**a**) simulated; and (**b**) experimental. I_o, output current (blue lines); U_o, output voltage (green lines).

Since simulations are closer to an ideal system than experiments, their efficiencies are higher than experimental ones. However, the dynamic and static performance are generally the same, which verifies the feasibility of the APC system.

4.3. Comparisons between Proposed Methods

Figure 18 shows the photograph of the two proposed controllers. The DPC controller is 9.0 cm × 9.0 cm × 2.7 cm, whereas the APC controller is only 2.4 cm × 2.0 cm × 0.3 cm. The analog controller is much smaller than the digital one. The volume, weight, and cost of the analog receiver can be significantly reduced.

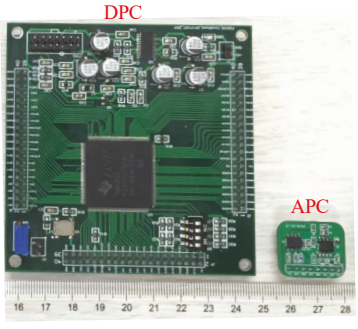

Figure 18. Photograph of two proposed controllers.

Although both the DPC and APC methods can realize the CC and CV power transfer modes, they differ in some aspects. Table 2 compares the differences of the two proposed methods. The DPC system is more complex: it requires a DSP controller, isolated power supplies and driver circuits, current and voltage sensors, and the synchronization circuit. However, the DPC system can eliminate the time delay caused by the regulation circuit and avoid additional power losses of the sampling and divider resistances in the APC receiver. The highest measured experimental efficiency of the APC system is 89.4%, whereas it is 91.4% in the DPC system. Thus, the DPC receiver contributes to a higher performance compared to the APC receiver. Furthermore, it is easier to change the received power through the software code as in the DPC system than changing the regulation resistances as in the APC system, i.e., the DPC system has a greater flexibility than the APC system. Conversely, the APC receiver is simpler since it does not require synchronization algorithms and dedicated programming. In addition, it needs fewer auxiliary devices, i.e., isolated power supplies and expensive sensors are not needed, as well as has a smaller printed circuit board layout. This makes the analog receiver lighter, more cost-effective, and compact.

Table 2. Comparisons between DPC and APC.

Methods	DPC	APC
Complexity	High	Low
Performance	Very High	Good
Flexibility	Very High	Good
Cost	High	Low
Weight	Heavy	Light
Volume	Large	Small

4.4. Comparisons among Different Topologies of WPT Receivers

Comparisons among different WPT receivers are presented in Table 3, and the advantages of the proposed topology and control methods are demonstrated below.

Table 3. Comparisons among different receivers for WPT systems.

Topologies	Capacitors	Inductors	Digital Controllers	Switches	Control Methods	Power Regulation Ability
DC-DC converters [3–8]	2	1	1	1	Duty ratio control	Full-controlled
Full bridge [12–25]	1	0	1	4	Phase control	Full-controlled
Semi-bridgeless [26,27]	1	0	1	2	Phase control	Full-controlled
Reported single-switch receivers [29–33]	1	0	1	1	Duty ratio control	Half-controlled
Proposed receiver	1	0	0 or 1	1	Phase control	Full-controlled

Compared to DC-DC converters used in the WPT systems, the proposed receiver advances in two aspects. Firstly, fewer capacitors and no inductors are required in the proposed receiver. It can reduce the volume and weight of the receiver. Secondly, AC-DC and DC-DC conversions are achieved simultaneously by the proposed receiver. Fewer cascaded circuits, therefore, bring about a higher overall efficiency.

Compared to full bridge and semi-bridgeless topologies, the proposed receiver advances in two aspects: Firstly, the proposed receiver is more cost-effective since the number of SiC MOSFETs and driver circuits used in the proposed receiver have been reduced by 75% as compared to full bridge topology, and 50% as compared to semi-bridgeless topology. In addition, a SiC diode, aiming to reduce high forward voltage, is not needed in the proposed receiver. Therefore, the cost reduction can be significant. Secondly, the proposed receiver has a higher reliability. Dead time is required to avoid short circuit in full bridge applications, whereas the proposed receiver gets rid of short circuit due to the reverse blocking of the diode.

Most reported single-switch receivers are half-controlled, which may fail to achieve the CC and CV power transfer modes. Furthermore, the receivers require a large capacitor to stabilize the output voltage due to the usage of duty ratio control. However, the proposed receiver is full-controlled and has a strong power regulation ability. Owing to the utilization of PC, a small filter capacitor is needed in the proposed receiver.

5. Conclusions

This paper presents a novel single-switch phase controlled active rectifier as receiver for WPT systems. Improved DPC and APC methods are proposed based on the receiver topology to achieve effective CC and CV power transfer modes. The proposed method prevents forward voltage losses in SiC switches and accidental shoot through states with improved switching patterns. The system is easy to implement, has a lower cost, smaller volume, lighter weight, and a higher reliability than conventional phase controlled receivers. Detailed analyses of the operating modes and implementation techniques are presented. Simulated and experimental results of a 400-W WPT system are included which show more than 91% overall efficiency and thereby demonstrate the feasibility of the proposed system.

Author Contributions: X.L., H.T., and X.Y. conceptualized the main idea of this research project; X.L. designed and conducted the experiments; N.J. and D.M. checked the results; X.L. wrote the whole paper; and N.J., D.M. and K.H. reviewed and edited the paper.

Funding: This research was funded by United Foundation of NSFC-Henan, grant number U1604136. The APC was funded by Houjun Tang.

Conflicts of Interest: The authors declare no conflict of interest.

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Wireless Power Transfer for Battery Powering System

Tianfeng Wang [1], Xin Liu [1], Nan Jin [2], Houjun Tang [1], Xijun Yang [1,*] and Muhammad Ali [1]

[1] School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai 200240, China; wangtf1992@sjtu.edu.cn (T.W.); Liu_xin@sjtu.edu.cn (X.L.); hjtang@sjtu.edu.cn (H.T.); engrmak.ee@sjtu.edu.cn (M.A.)

[2] College of Electric and Information Engineering, Zhengzhou University of Light Industry, Zhengzhou 450002, China; jinnan@zzuli.edu.cn

* Correspondence: yangxijun@sjtu.edu.cn; Tel.: +86-021-34204604

Received: 18 August 2018; Accepted: 5 September 2018; Published: 7 September 2018

Abstract: The LCL topology (formed by an LC tank with a transmitting coil) is extensively utilized in wireless power transfer (WPT) systems with the features of a constant resonant current and ability to disconnect load abruptly. However, it requires high input voltage, which limits its utilization in battery powering scenarios (12~24 V). A current-fed inverter (CFI) is applied to the LCL-S (a compensation capacitor in series with the receiving coil) WPT systems to boost the input voltage, thereby getting a higher resonant current in the transmitting side (Tx). To facilitate the voltage regulation in the receiving side (Rx), a semi-active bridge (SAB) is introduced into the system, which further boosts the output voltage by a lower frequency switching at different duty ratios. Rigorous mathematical analysis of the proposed system is carried out and design guidelines are subsequently derived. Moreover, a power loss reduction is realized by zero voltage switch (ZVS) of the four switches in the Tx which are deduced and presented. Simulations and experiments are added to verify the proposed system. Consequently, a 93.3% system efficiency (DC-to-DC efficiency) is obtained using the proposed topology. Optimization techniques for a higher efficiency are included in this study.

Keywords: current-fed inverter; LCL-S topology; semi-active bridge; soft switching; voltage boost; wireless power transfer

1. Introduction

Nowadays, wireless power transfer (WPT) technology is a leading research field due to the wide spread electronic devices that can benefit from this technology. For instance, electric vehicles can get rid of electrical hazards caused by wire snapping and reduce on-board battery burden by dynamic charging [1–3]. Medical implants benefit from the increased power supply without the penalty of a greater bulk [4,5]. In addition, a WPT charger can power multiple loads simultaneously without lots of wires and complex connections. Accordingly, it can be predicted that WPT will be a good assistant of, or an alternative to the plug-in power transfer in various voltage rate systems. The advantages and prospects have already ignited a hot interest all over the world, and related studies are burgeoning.

In WPT systems, the compensation topologies are very crucial for high efficiency and power rates by reducing and even cancelling leakage inductance. Research on compensation topologies and their features are continually carried out and new ideas have been investigated and put forward as well [6–9]. Many research works rely on four basic topologies, namely series-series (SS), series-parallel (SP), parallel-parallel (PP), and parallel-series (PS) [10]. However, to meet special or practical requirements, such as constant current/voltage output [7,11] and the endurance of load tripping, hybrid compensation approaches like LC and LCC [12,13] have been put forward. Although, the hybrid topologies introduce more passive components into the system and may add power loss and system bulk, their benefits overweight the shortcoming for demand and security reasons. Among

these topologies, the LCL topology, formed by an LC tank with a transmitting coil, is regarded as an ideal network used in the transmitting side (Tx), due to its ability to maintain the transmitting current constant and independent of the reflected impedance of the receivers [11,14]. Thus, the induced voltage in every receiving side (Rx) is steady. Moreover, if the disconnection happens in the four basic topologies, urgent protection would be needed, or the circuit is over-current burned. The LCL topology can endure unexpected load disconnection, so it is rather promising in practice. Accordingly, the LCL topology is applied in the Tx in this literature due to these features.

Nevertheless, this topology requires a large input voltage or small receiving coil inductance to augment the transmitting current and induce a high voltage in the Rx. Decreasing the coil inductance will lead to a small mutual inductance and a voltage decreasing in the Rx. Hence, enlarging the input voltage is recommended. The input voltage is 400 V in Ref. [9], and the input voltage of the Evatran products is 220 V. Otherwise, the output voltage can be small, only 5 V in Ref. [11] due to the small input of 26 V. For some power sources, such as photovoltaic panels and batteries, the voltage rating of each cell is very low. The output voltage of a solar cell module is around 12~24 V, and the nominal voltage of a lead-acid battery with six cells is only 12 V. Simply increasing the number of panels and cells in series can surge the system bulk, pressure and insulation requirement, thereby being impractical for solar system applications, wearable devices, and other portable equipment. In addition, the WPT technology may be adopted as an aid for safety and reliability in some internal sub-systems, where only low-voltage sources can be provided.

To extend the WPT technology and LCL topology to battery powering system and wirelessly power the loads within the 12~24 V input range, front-end boost circuits are in great need. Inserting the traditional boost circuits before the inverter is a good solution and also generally used. High efficiency of the boost circuits can be obtained due to the maturity of boost techniques. However, lots of components (an active switch, a power diode, a comparably large inductor, and a capacitor) and auxiliary circuits (control circuits and drivers) are needed. In contrast, the Z-source/quasi-Z-source networks boost the output voltage by shorting the end-rear bridge, which can be realized by the full bridge inverter itself and the extra control circuits are not required [15]. Nevertheless, two inductors and two capacitors are added so the losses caused by these components increase inevitably and the system may incur maloperations caused by the resonant networks [16–18]. On the other hand, large inductances are required in the Z-source network to suppress the ripples and prevent the discontinuous current mode [19]. Hence these two mentioned circuits will increase the bulk of the power system, which may cause difficulty in carrying or assembling.

To realize a high conversion gain and a compact size with a simpler topology, a current-fed inverter (CFI) is a good alternative in WPT systems. The CFI only contains a full bridge inverter and two identical front-end inductors so that the power conversion stages are reduced with an improvement in reliability [20,21]. Compared with the voltage source inverter (VSI) in series with a boost circuit, the CFI has a simpler circuit and easier control method. The control and response rates are also improved due to the compact stages. Compared with the Z-source inverter (ZSI), the CFI has less components and reduces the total harmonic distortion (THD) of the input current. Moreover, the switches in the CFI can operate ZVS from inductive impedance to capacitive impedance and the top-side switches can be turned OFF softly in some scenarios.

Conventionally, there are two kinds of schemes to regulate the output voltage. One scheme is to apply a diode rectifier in the Rx but conduct the optimal charge control in the Tx (the source voltage level shift, the duty ratio adjustment, etc.). This scheme predigests the Rx complexity but needs frequent and quick communications. Another scheme is to control the Rx by itself, which lowers the communication demand. Two circuits have already been proposed: inserting the buck-boost converter connected in series with the rectifier [22] or replacing the rectifier with an active bridge [23]. The former involves a large inductor and more control circuits. The latterrequires a complicated controller and complex auxiliary circuits with increasing receiving volume, which is not as compact as mobile devices require. Considering the trade-off between the size and communication complexity,

an active switch replaces one diode of the rectifier and regulates the load voltage in this literature. This semi-active bridge (SAB) can regulate the output by being operated at a variable frequency and duty ratio. Specially, the SAB can boost the output, which can obtain higher voltage than the diode rectifier. Different from the switches in an active bridge that must operate at a high and precise resonant frequency, the switch in SAB can conduct at a lower frequency. Additionally, the complex control protocols and negotiation required by the active bridge [24] are not necessary for the SAB.

The paper is structured as follows: Section 2 depicts the proposed circuit diagram of the WPT system, followed by its operating principle. The capability of soft switching is also elaborated upon. Section 3 models the proposed system with mathematical analyses of the system parameters. Guidelines are provided on the configurations of the inductors, coils, and loads. In Section 4, simulations are implemented, and results are presented and compared. To further support and verify the theoretical analysis and simulation accuracy, a prototype is developed and experimental results are provided in Section 5. A 93.3% system efficiency (DC-to-DC efficiency) is achieved, and the output voltage is within twice to four times that of the input. Optimization techniques for higher efficiency are included. Finally, Section 6 concludes the paper.

2. Proposed Topology

2.1. System Composition

A block diagram of the proposed topology with one receiver is demonstrated in Figure 1. In the Tx, the CFI contains a clamp capacitor C_o, two identical front-end inductors (L_1 and L_2), and four switches (Q_1, Q_{1a}, Q_2, and Q_{2a}), which can be regarded as an assembly of two boost converters [20,21]. A combination of the switching pattern and the inductors implement the boost function, and the amplitude of the output voltage is equal to the capacitor voltage V_C across C_o. For the resonant network, the LCL topology and series compensation topology is employed in the Tx and Rx, respectively. As for the Rx, the SAB supersedes the rectifier, where a bottom side diode is replaced by a controllable switch Q_s.

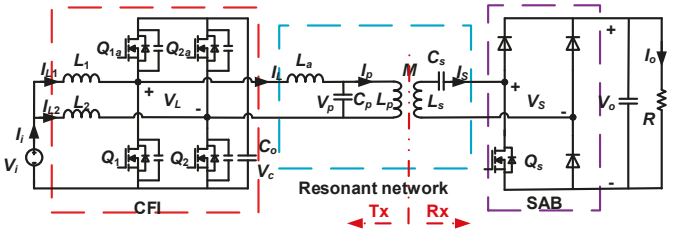

Figure 1. Proposed circuit diagram of WPT systems with one receiver.

In this paper, bold italic letters symbolize the phasors and the italic letters symbolize the real numbers or RMS values. In Figure 1, L_p and C_p represent the Tx coil inductance and its compensation capacitance. L_s and C_s represent the Rx coil inductance and its compensation capacitance. L_a and M represent the compensation inductance and mutual inductance. V_i and I_i are the input voltage and input current from the source. $\boldsymbol{V}_L$ and $\boldsymbol{I}_L$ are the output voltage and current of the CFI. $\boldsymbol{V}_p$ and $\boldsymbol{I}_p$ are the voltage across and the current through Tx coil. $\boldsymbol{V}_s$ and $\boldsymbol{I}_s$ are the input voltage of the SAB and the resonant current in the resonant tank.

2.2. Operation Patterns in Tx

Theoretically, four states exist in the full bridge. However, if the top-side switches are both ON, the charging circuits for L_1 and L_2 are broken and the voltage-boost function cannot be accomplished. Thus, three states are conducted in the CFI. Defining the duty ratio of Q_1 and Q_2 as d_s, d_s should be

above 0.5 to prevent Q_{1a} and Q_{2a} being both ON. The unequal PWM control [25] is adopted in this paper and the corresponding waveforms are depicted in Figure 2a. The four switches all conduct at a resonant frequency f_s. When Q_{1a} and Q_2 are ON, V_L is positive, L_1 is discharged but L_2 is charged, as shown in Figure 2b. When Q_{2a} and Q_1 are ON, V_L is negative, L_1 is charged but L_2 is discharged, as shown in Figure 2d. When the bottom-side switches are ON, V_L is zero, both L_1 and L_2 are charged, as shown in Figure 2c,e.

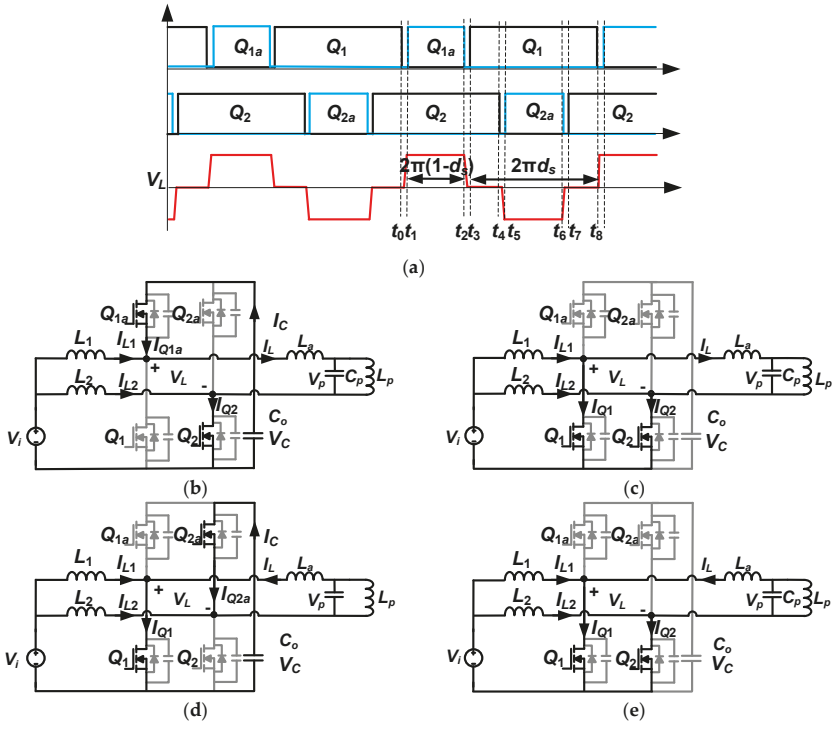

Figure 2. (**a**) Typical operation patterns of the CFI, (**b**) t_1~t_2; (**c**) t_3~t_4; (**d**) t_5~t_6; (**e**) t_7~t_8.

The current stress of each switches is estimated as

$$\begin{cases} I_{Q1a\max} = I_{Lm} - I_{L1\min} \\ I_{Q1\max} = I_{Lm} + I_{L1\max} \\ I_{Q2a\max} = I_{Lm} - I_{L2\min} \\ I_{Q2\max} = I_{Lm} + I_{L2\max} \end{cases}. \tag{1}$$

As can be seen, the bottom-side switches suffer higher stresses than the top-side switches. According to the boost converter properties [26], the peak-to-peak current ripple and the maximum value of the inductor currents in Discontinuous Conduction Mode (DCM) are larger than those in Continuous Conduction Mode (CCM) under the same load conditions. Due to the rear-end resonant current, L_1 and L_2 will not enter DCM but quasi-CCM, where the currents through the inductors reverse their direction and the inductors are charged by the resonant network. The current ripple in quasi-CCM is large and the switches will suffer large stresses, according to Equation (1). Consequently, the CFI in this paper is recommended to operate in CCM to decrease the current stresses of the bottom switches. Thus, the two front-end inductors L_1 and L_2 should be well designed.

2.3. Operation Patterns in Rx

In the receiving side, Q_s operates at frequency f_{Qs}. The ratio of f_s and f_{Qs} is denoted as n (>1), and the duty ratio of Q_s is denoted as d_{Qs}. Parts of the waveforms and the corresponding patterns are illustrated in Figure 3. The direction of the dark arrow of $\boldsymbol{I}_s$ is chosen as a reference direction and the red dotted lines denote the actual current paths. When Q_s is turned OFF, it functions as a common diode. The duty ratio of Q_s is 0.5 and the corresponding waveforms of $\boldsymbol{V}_s$, $\boldsymbol{I}_s$, $\boldsymbol{I}_p$ are presented in Figure 3a. $\boldsymbol{I}_s$ flows as shown in Figure 3b,c, where $\boldsymbol{V}_s$ is positive and negative, respectively. When Q_s is turned ON, the anode of D_1 is directly connected with the anode of D_3 as shown in Figure 3d,e. When $\boldsymbol{I}_s$ is positive, as shown in Figure 3d, it flows straight from one end of the compensation capacitor to the end of the Tx coil, that is, the load R is cut off from the resonant source and $\boldsymbol{V}_s$ drops to zero. When $\boldsymbol{I}_s$ is negative, as shown in Figure 3e, however, it flows through D_2 and powers the parallel capacitor and the load. At that time, $\boldsymbol{V}_s$ is negative as shown in Figure 3a. Therefore, $\boldsymbol{I}_s$ resonates at f_s, while the frequency of its envelope line is f_{Qs}. On the other hand, the amplitude of $\boldsymbol{I}_p$ can be deemed as a constant value, although the equivalent load changes frequently as mentioned. Hence, the Rx can achieve a stable induced voltage ignoring the rapid change of the equivalent impedance, which is also the reason for choosing the LCL topology as the SAB and LCL complement each other.

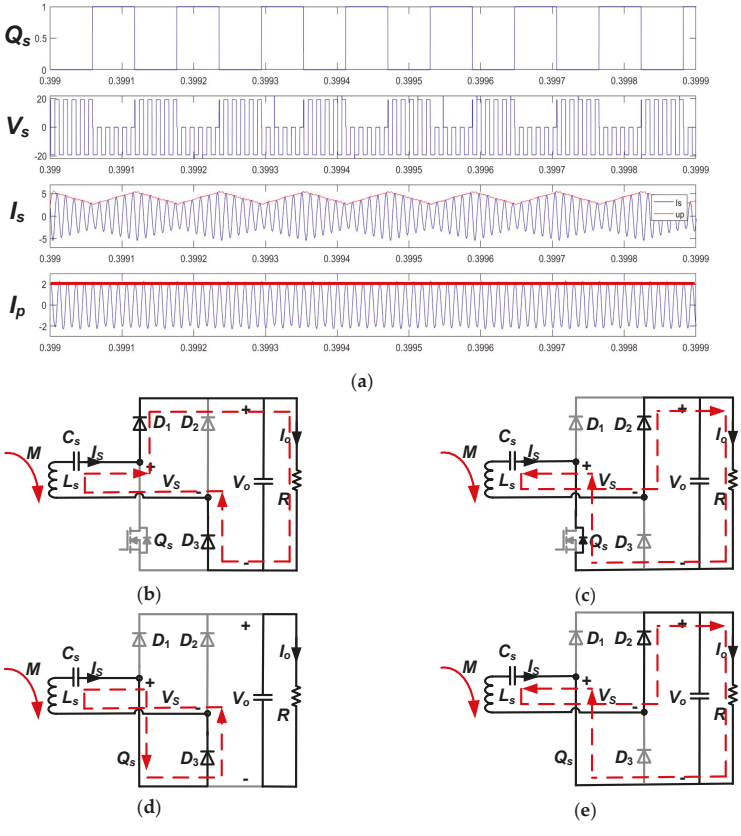

Figure 3. Typical waveforms and operation patterns of the SAB (**a**) waveforms of the SAB (**b**) current path when Q_s is OFF and $\boldsymbol{I}_s$ is positive (**c**) current path when Q_s is OFF and $\boldsymbol{I}_s$ is negative (**d**) current path when Q_s is ON and $\boldsymbol{I}_s$ is positive (**e**) current path when Q_s is ON and $\boldsymbol{I}_s$ is negative.

2.4. Soft-Switching Capability

In the Tx, the soft-switching operation is accomplished by the CFI and the clamp capacitor C_o. Q_1 and Q_{1a} are chosen to illustrate the soft-switching process. The analysis of Q_2 and Q_{2a} is fundamentally the same as the analysis of Q_1 and Q_{1a} due to the topology symmetry. The current paths are depicted in Figure 4.

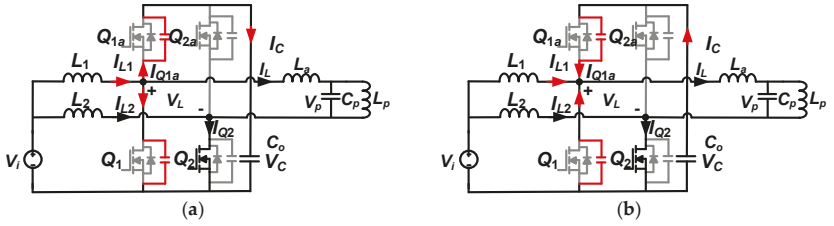

Figure 4. Current paths for CFI conducting ZVS (**a**) state before Q_{1a} is on t_0~t_1; (**b**) state before Q_1 is on t_2~t_3.

Figure 4a shows the state before Q_{1a} is ON, where $\boldsymbol{I}_{L1}$ reaches its maximum value. The difference between $\boldsymbol{I}_{L1}$ and $\boldsymbol{I}_L$ is positive. The current difference charges the parallel capacitor of Q_{1a}, C_{Q1a}, and discharges the parallel capacitor of Q_1, C_{Q1}. Figure 4b shows the state before Q_1 is ON, where $\boldsymbol{I}_{L1}$ reaches its minimum value. At that time, the difference between $\boldsymbol{I}_{L1}$ and $\boldsymbol{I}_L$ is negative. Then, C_o also provides current to charge C_{Q1} and discharge C_{Q1a}. Hence, ZVS of Q_{1a} and Q_1 are achieved.

To turn OFF the top-side switches softly [27], $\boldsymbol{I}_{L1}$ should be a bit larger than $\boldsymbol{I}_L$ before Q_{1a} is OFF so that $\boldsymbol{I}_{Q1a}$ will reverse direction from Figure 5a to Figure 5b. Then, when Q_{1a} is turned OFF, the freewheeling current can flow through the parallel diode, providing a condition for the soft-switching OFF [27].

In comparison with the VSI, the inductors in the CFI can provide the current directly for soft switching, thereof getting rid of the rear-end resonant current limitation. Accordingly, the soft switching can be more likely accomplished.

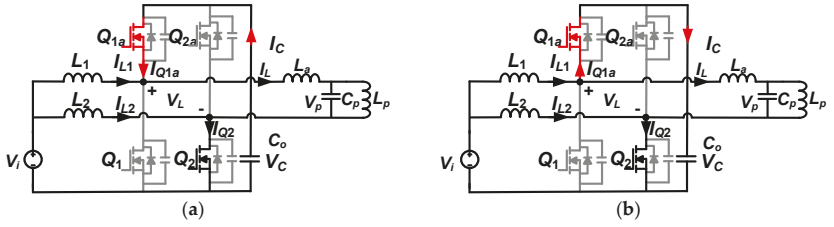

Figure 5. Current paths before turning OFF Q_{1a} (**a**) preclude to the hard OFF; (**b**) preclude to the soft OFF.

To guarantee the inductors working in CCM and the minimum value of $\boldsymbol{I}_{L1}$ larger than $\boldsymbol{I}_L$, the inductance should be large, accompanied with the increase of the internal resistance and power loss caused by the inductors. Thus, the inductance should be set at a reasonable value.

In the Rx, the soft-switching operation [27] can also be realized by Q_s being turned ON/OFF when the current and the voltage are negative. If Q_s is turned OFF when $\boldsymbol{I}_s$ is positive and $\boldsymbol{V}_s$ is zero, the current path will suddenly change from Figure 3d to Figure 3b, leading to a surge of $\boldsymbol{V}_s$ and the hard-switching OFF Q_s. Additionally, if Q_s is turned ON when $\boldsymbol{I}_s$ and $\boldsymbol{V}_s$ are positive, the current path will suddenly change from Figure 3b to Figure 3d, leading to a plunge of $\boldsymbol{V}_s$ and the hard-switching ON of Q_s. The distortion waveform of $\boldsymbol{V}_s$ is demonstrated in Figure 6b. However, if Q_s is turned

ON/OFF when I_s is negative, the current pattern switches between Figure 3c and Figure 3e. As can be seen, the voltage output in Figure 6c is ideal and the soft-switching operation is also achieved. To prevent this distortion, Q_s should be turned ON when I_s is negative, which can be achieved alone in the Rx. In contrast, the dual active bridge (DAB) strictly demands the synchronization [28], otherwise, the system becomes unstable and power oscillations occur.

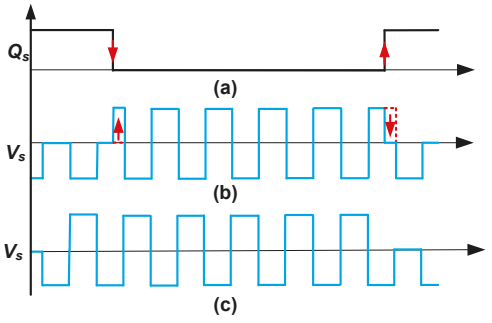

Figure 6. Difference of V_s caused by the switch time (**a**) Q_s switch time; (**b**) distortion of V_s; (**c**) ideal waveform of V_s.

3. Mathematical Modeling and Configuration

3.1. Equivalent Circuit Model

To model and analyze the proposed system, an equivalent circuit is established as shown in Figure 7. Z_p, Z_{sref}, and R_{ac} denote the Tx equivalent impedance, the reflected impedance from the Rx and the equivalent ac resistance calculated in a receiving switching period, respectively. Z_{pt}, Z_{sreft}, and R_{act} denote the three impedances calculated in a resonant period. r_p and r_s denote the inner resistances of the Tx coil and the Rx coil. Besides, L_a is designed to be identical to L_p. Considering the power losses, inner resistance of L_a is represented by r_{La}. In addition, r_L denotes the inner resistance of L_1 and L_2. The Tx switching frequency and the resonant frequency are both equalized to f_s.

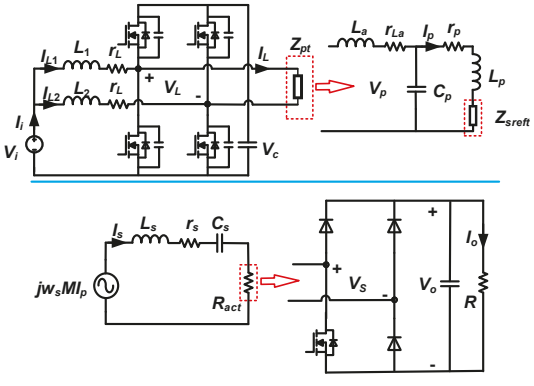

Figure 7. Equivalent circuit diagram.

Thus, Z_{pt} is resistant and deduced as:

$$Z_{pt} = j\omega_s L_a + r_{La} + \frac{(j\omega_s L_p + Z_{sreft} + r_p)\frac{1}{j\omega_s C_p}}{j\omega_s L_p + Z_{sreft} + r_p + \frac{1}{j\omega_s C_p}} = \frac{(\omega_s L_p)^2}{Z_{sreft} + r_p} + r_{La} \approx \frac{(\omega_s L_p)^2}{Z_{sreft} + r_p}, \quad (2)$$

where, Z_{sreft} is equal to

$$Z_{sreft} = \frac{(\omega_s M)^2}{R_{act} + r_s}. \tag{3}$$

Based on the boost model, the amplitude of the square wave $\boldsymbol{V}_L$ is derived as:

$$V_{Lm} = V_C = \frac{V_i}{1 - d_s}. \tag{4}$$

Thus, the RMS value of the fundamental harmonic of $\boldsymbol{V}_L$ is deduced as:

$$V_{L1} = 2\sqrt{2} V_i \frac{\sin \pi d_s}{\pi(1 - d_s)}. \tag{5}$$

Then, the output current of CFI in a resonant period is:

$$I_L = \frac{V_{L1}}{Z_{pt}} = \frac{2\sqrt{2} V \sin \pi d_s}{\pi(1 - d_s)(\omega_s L_p)^2} \left[\frac{(\omega_s M)^2}{R_{act} + r_s} + r_p \right]. \tag{6}$$

Obviously, $\boldsymbol{I}_L$ is load-dependent and its RMS value $\boldsymbol{I}_L$ will decrease with the augment of R_{act}. However, the RMS value of branch current $\boldsymbol{I}_p$ is calculated as:

$$I_p = \frac{V_{L1} \cdot (Z_{sreft} + r_p)}{(\omega_s L_p)^2} \frac{\frac{1}{j\omega_s C_p}}{\frac{1}{j\omega_s C_p} + j\omega_s L_p + Z_{sreft} + r_p} = \frac{V_{L1}}{j\omega_s L_p}, \tag{7}$$

which signifies that $\boldsymbol{I}_p$ is independent of the Rx characteristics but proportional to the input voltage. Accordingly, high input voltage $\boldsymbol{V}_L$ is recommended to maintain a large resonant current. According to the mutual inductance theory, the induced voltage $\boldsymbol{V}_s$ in the Rx keeps steady if $\boldsymbol{I}_p$ is constant.

In the Rx, the model can be presented as:

$$j\omega_s M I_p = \left[j\omega_s L_s + r_s + \frac{1}{j\omega_s C_s} + R_{act} \right] I_s = [r_s + R_{act}] I_s, \tag{8}$$

which implies that the induced voltage and the receiving current are in-phase.

3.2. Equivalent Resistance of SAB

To analyze the impact of duty ratio d_{Qs} and receiving switching frequency f_{Qs} (=f_s/n) on R_{ac}, R_{act}, and output voltage V_o, the harmonic approximation method and extended describing function are utilized. Assuming that the induced voltage $v(t)$, receiving current $i_{sL}(t)$, and compensation capacitor voltage $v_{sC}(t)$ can be approximated by fundamental terms and the former two are in same phase due to the resistive impedance, it has

$$\begin{cases} v(t) = \omega_s M I_{pm} \sin \omega_s t \\ i_{sL}(t) = i_{sLs}(t) \sin \omega_s t \\ v_{sC}(t) = v_{sCc}(t) \cos \omega_s t \end{cases}, \tag{9}$$

where, the envelope terms are slowly time varying at f_s/n.

By utilizing the extended describing method, $\boldsymbol{V}_s$ whose waveform is depicted in Figure 3a, can be approximated as

$$v_s(t) \approx f_s(n, d_{Qs}, V_o) \sin \omega_s t. \tag{10}$$

The extended describing function f_s (n, d_{Qs}, V_o) can be calculated by Fourier expansions and given as

$$f_s(n, d_{Qs}, V_o) = -\frac{d_{Qs}}{2}V_o + \sum_{k=1}^{\infty}\left[a_k \cos k\frac{\omega_s}{n}t + b_k \sin k\frac{\omega_s}{n}t\right], \tag{11}$$

where the coefficients are

$$\begin{cases} a_k = \frac{V_o}{\pi k}\left[\sum\limits_{i=1}^{2n-2d_{Qs}n}(-1)^i \sin k\varphi\big|_{\pi(i-1)/n}^{\pi i/n} - \sum\limits_{i=n-d_{Qs}n}^{n-1}\sin k\varphi\big|_{2\pi i/n}^{\pi(2i+1)/n}\right] \\ b_k = \frac{V_o}{\pi k}\left[\sum\limits_{i=1}^{2n-2d_{Qs}n}(-1)^{i-1}\cos k\varphi\big|_{\pi(i-1)/n}^{\pi i/n} + \sum\limits_{i=n-d_{Qs}n}^{n-1}\cos k\varphi\big|_{2\pi i/n}^{\pi(2i+1)/n}\right] \end{cases}. \tag{12}$$

However, it is difficult to get an analytical solution on the relationship between f_s, d_{Qs}, V_o, and R_{ac}, since the switching frequency is below the resonant frequency and the equivalent impedance in each resonant period is different from others, which is totally contrary to the small-signal model condition [29]. Nevertheless, a trend estimation can be conducted by analyzing the extreme cases. Since the SAB disconnects the load OFF and ON, it can be assumed that when the load is OFF, the equivalent impedance R_{ac} decreases. To validate this assumption and estimate the relation between d_{Qs} and R_{ac}, two extreme cases (d_{Qs} = 0 and d_{Qs} = 1) are considered. The corresponding waveforms are presented in Figure 8.

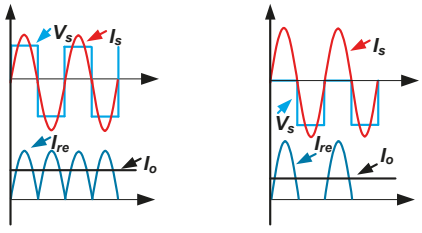

Figure 8. Typical waveforms of the Rx under different duty ratios (**a**) d_{Qs} = 0; (**b**) d_{Qs} = 1.

When Q_s stays OFF, that is d_{Qs} = 0, the SAB works as a diode rectifier. The typical waveforms are depicted in Figure 8a, where I_{re} represents the output current of the SAB. Thus, the equivalent ac resistance reaches the maximum as given in [30]:

$$\begin{cases} R_{act} = R_{ac} \\ R_{ac\max} = \frac{8R}{\pi^2} \end{cases}. \tag{13}$$

However, when Q_s stays ON, that is d_{Qs} = 1, the anode of D_1 is directly connected with the anode of D_3, waveforms change to Figure 8b and the ac load accordingly, is

$$\begin{cases} R_{act} = R_{ac} \\ R_{ac\max} = \frac{2\sqrt{2}R}{\pi^2} \end{cases}. \tag{14}$$

It can be found that R_{ac} decreases when d_{Qs} increases. Besides, on basis of Equation (6), it can be drawn that the input current $\boldsymbol{I}_L$ and input power will rise as d_{Qs} increases, and the dc output V_o boost as well due to the energy principles. Thus, the voltage boost function is accomplished.

Assuming that the power loss caused by SAB can be ignored, the power fetched from the Tx is equal to the load power, that is,

$$\frac{V_o^2}{R} = I_p^2 \frac{(\omega_s M)^2}{R_{act} + r_s} \frac{R_{act}}{R_{act} + r_s}. \tag{15}$$

Hence, by substituting Equations (5), (7), (13) and (14) into Equation (15), the range of the output voltage is estimated as:

$$\frac{2\sqrt{2}\pi MR}{L_p(8R + \pi^2 r_s)} \frac{\sin \pi d_s}{(1 - d_s)} V_i \le V_o \le \frac{2^{0.75}\pi MR}{L_p(2\sqrt{2}R + \pi^2 r_s)} \frac{\sin \pi d_s}{(1 - d_s)} V_i, \tag{16}$$

which shows the dc load can acquire a wide range of output. Besides, the output voltage V_o can be higher than the input voltage V_i with proper configurations.

3.3. Soft-Switching Design in Tx

The power fetched from the CFI P_L during a resonant period is deduced, with Equations (5) and (6), as:

$$P_L = \frac{8V_i^2}{(\omega_s L_p)^2} \frac{\sin^2 \pi d_s}{\pi^2 (1-d_s)^2} \left[\frac{(\omega_s M)^2}{R_{act} + r_s} + r_p \right] \ge \frac{8V_i^2}{(\omega_s L_p)^2} \frac{\sin^2 \pi d_s}{\pi^2 (1-d_s)^2} \left[\frac{(\omega_s M)^2}{R_{acmax} + r_s} + r_p \right] = P_{Lmin}. \tag{17}$$

Assuming that the magnitude of power loss caused by the switches, L_1, L_2, and C_o can be ignored as compared to that of P_L, P_L is therefore equal to the DC input power P_i, which can be presented as:

$$P_i = \frac{1}{2} V_i \left[2I_{imin} + \frac{V_i}{L}(2d_s - 1)T_s \right], \tag{18}$$

where, $L = L_1 = L_2$, I_{imin} is the minimum value of the DC input current, illustrated in Figure 9, and can be calculated as

$$I_{imin} = 2I_{L1min} + \frac{V_i T_s}{2L}. \tag{19}$$

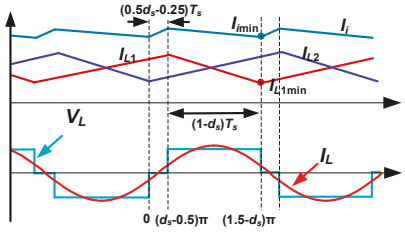

Figure 9. Typical waveforms of the CFI.

Accordingly, $\boldsymbol{I}_{L1min}$ can be calculated with Equations (17)–(19) as:

$$I_{L1min} = \frac{4V_i \sin^2 \pi d_s}{\pi^2 (1 - d_s)^2 Z_{pt}} - \frac{V_i T_s}{2L} d_s. \tag{20}$$

To prevent the system from quasi-CCM, $\boldsymbol{I}_{L1min}$ should be above zero. To make $\boldsymbol{I}_{L1min} > 0$, L can be deduced from Equation (20) with Equation (2) as:

$$L > \frac{T_s d_s}{8 \frac{\sin^2 \pi d_s}{\pi^2 (1-d_s)^2}} \frac{(\omega_s L_p)^2}{\frac{(\omega_s M)^2}{R_{act} + r_s} + r_p}. \tag{21}$$

On the other hand, to complete the soft-switching OFF Q_{1a}, it demands

$$I_{L1\min} > I_L|_{\varphi=1.5\pi-\pi d_s}. \tag{22}$$

Defining Q as the loaded quality factor of the Tx, Q can be calculated as:

$$Q = \frac{Z_{sreft}}{\omega_s L_p} = \frac{\omega_s k^2 L_s}{(R_{act} + r_s)}, \tag{23}$$

where k denotes the coupling coefficient.

When Q is large, the output current of CFI is sinusoidal as presented in Figure 9. To complete soft-switching OFF Q_{1a}, Equation (22) is written as:

$$I_{L1\min} > \sqrt{2} I_L \sin\left(\frac{3}{2}\pi - \pi d_s\right), \tag{24}$$

that is, L is deduced from Equation (24) as:

$$L > \frac{T_s d_s}{8 \frac{\sin \pi d_s}{\pi(1-d_s)} \left[\frac{\sin \pi d_s}{\pi(1-d_s)} + \cos \pi d_s\right]} \frac{(\omega_s L_p)^2}{\frac{(\omega_s M)^2}{R_{act}+r_s} + r_p}. \tag{25}$$

Since d_s is above 0.5, the right of Equation (21) is larger than that of Equation (25) and reaches its maximum when d_s is 0.5. Hence, the inductance should meet the requirement as:

$$L > \frac{\pi^2}{64 f_s} \frac{(\omega_s L_p)^2}{\frac{(\omega_s M)^2}{R_{act}+r_s} + r_p}. \tag{26}$$

Nevertheless, considering the inner resistances and power losses of the two inductors at high input current, L cannot increase blindly otherwise the system efficiency will degrade.

However, when Q is small (i.e., $Q < 1$ according to the MATLAB and PLECS simulation), $\boldsymbol{I}_L$ distorts and $\boldsymbol{I}_{Q1a}$ can never reverse direction no matter how large L is, thereby failing soft-switching OFF Q_{1a} and Q_{2a}. In practice, the inner resistances of the coils will surge significantly with the increase of the coil inductance. On the other hand, the LCL topology requires rigorous manufacturing technique to reduce the coil resistance since the losses of the coil resistors in LCL topology far outweigh that in series compensation topology. Accordingly, L_p and M are usually small, which inevitably results in a small Q and distortion of $\boldsymbol{I}_L$. Simply increasing L_s can reduce the receiving efficiency due to the enlarged coil resistance, leading to the system efficiency decreasing as well. Thus, there is a trade-off between the soft-switching OFF and system efficiency.

3.4. Optimal Load

To evaluate the system efficiency variation caused by the change of the equivalent impedance, the optimal load is calculated. Given that the power loss caused by the CFI is hard to theoretically calculated, the transmitting efficiency η, defined as the ratio of the CFI output power to the equivalent ac power, is presented to calculate the optimal load for the CFI and approximate the system efficiency. η can be written with Equations (3), (5)–(7) as:

$$\eta = \frac{I_p^2 Z_{sreft}}{V_{L1} I_L} = (\omega_s M)^2 \frac{R_{act}}{r_p {R_{act}}^2 + (\omega_s M)^2 R_{act} + 2 r_s r_p R_{act} + (\omega_s M)^2 r_s + r_s^2 r_p}. \tag{27}$$

The derivative of Equation (27) is calculated as:

$$\frac{d\eta}{dt} = (\omega_s M)^2 \frac{-r_p {R_{act}}^2 + (\omega_s M)^2 r_s + r_s^2 r_p}{\left[r_p {R_{act}}^2 + (\omega_s M)^2 R_{act} + 2 r_s r_p R_{act} + (\omega_s M)^2 r_s + r_s^2 r_p\right]^2}. \quad (28)$$

To obtain the highest η, Equation (28) should be equal to zero, that is,

$$R_{act} = \sqrt{\frac{(\omega_s M)^2 r_s}{r_p} + r_s^2}. \quad (29)$$

To maintain a large output voltage, L_s is deliberately designed much larger than L_p, whereas, r_s is 75 times r_p in this paper. Hence, Equation (29) can be simplified as:

$$R_{act} = \omega_s M \sqrt{r_s / r_p}. \quad (30)$$

By substituting Equation (30) into Equation (23), Equation (23) is rewritten as:

$$Q = k \sqrt{\frac{L_s}{r_s} \frac{r_p}{L_p}}. \quad (31)$$

If R_{act} is set as the optimal value, and Equation (31) is above 1, the soft-switching OFF Q_{1a} and Q_{2a} can be achieved.

4. Simulation and Verification

To validate the analysis and the aforementioned assumptions, simulations are implemented. According to Equation (7), the Tx coil inductance L_p is set as a small value, 15.5 μH, to obtain a large current and small resistance 8 mΩ as well. The coil-to-coil gap is fixed at 10 cm and the coupling coefficient k is 0.2. Since the receiving coil adopt the series compensation topology, the coil inductance is designed to a large value and set as a large value as 274.7 μH but followed by a large resistance, 0.3 Ω. To obtain high efficiency based on Equations (27) and (29), the dc load is set as 52 Ω according to Equation (13). It is worth noting that efficiency will drop when Q_s turns ON, because R_{act} will gradually deviate from the optimum. The forward voltage drop of the diode V_F is 0.6 V and the on resistance of the MOSFET is 80 mΩ. The configurations are listed in Table 1.

Table 1. Model Parameters.

Parameter	Value	Parameter	Value
Load R	52 Ω	Input voltage E_V	24 V
Transmitting switching frequency f_s	85 kHz	Mutual inductance M	18 μH
Transmitting inductance L_p	15.5 μH	Transmitting inner resistance r_p	8 mΩ
Receiving inductance L_s	274.7 μH	Receiving inner resistance r_s	0.3 Ω
Compensation inductance L_a	15.5 μH	Compensation inner resistance r_{La}	0.04 Ω
DC inductance L_1 & L_2	51 μH	DC inner resistance r_L	0.2 Ω
Transmitting capacitance C_p	222 nF	Receiving capacitance C_s	12.8 nF
Clamp capacitance C_o	470 μF	Transmitting duty ratio d_S	0.7
Forward voltage drop of diode V_F	0.6 V	On resistance of MOSFET R_{on}	80 mΩ

4.1. Soft-Switching Realization

When Q_s operates at different duty ratios, the equivalent ac impedance varies. Thus, the variation range of the loaded quality factor is [0.14, 0.40] calculated by Equation (23). The range of the minimum of the front-end inductance L is calculated as [38.6 μH, 107.4 μH] by Equation (21). When the SAB works as a common diode rectifier, the minimum of L surges to 107.4 μH, which also means a bulky

size and large inner resistance. Although the large inductors prevent circulating current, the saved power can hardly compensate the losses caused by the inner resistance, and hence L is configured a medium value as 51 μH with 0.2 Ω. Then, after Q_s operates, the circulating current will be eliminated. Simulations are fulfilled at different d_{Qs}. The simulation waveforms of Q_{1a} and $\boldsymbol{I}_{L1}$ are depicted in Figure 10. Figure 10a illustrates the waveforms where R is 52 Ω and Q_s stays OFF. The whole system efficiency is 94.5%. Figure 10b illustrates the waveforms where R is 52 Ω and Q_s operates as 8500 Hz with d_{Qs} = 0.5. The efficiency is 94.1%. Figure 10c demonstrates the waveforms where R is 52 Ω and Q_s stays ON. The efficiency is 90.8%. Figure 10d demonstrates the waveforms where R is 20 Ω and Q_s stays ON.

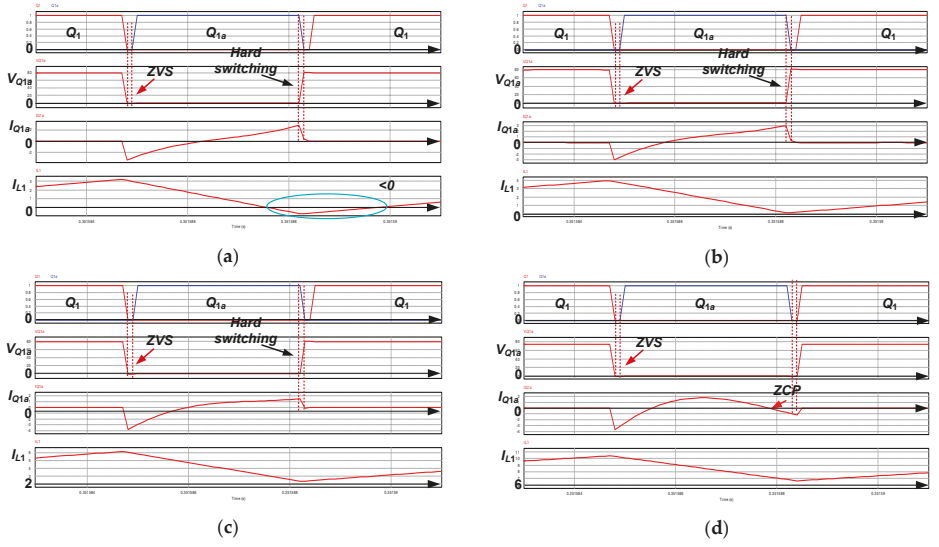

Figure 10. Typical waveforms of Q_{1a} and $\boldsymbol{I}_{L1}$ with a same L but different d_{Qs}: (**a**) R = 52 Ω, d_{Qs} = 0, η = 94.5%; (**b**) R = 52 Ω, d_{Qs} = 0.5, η = 94.1%; (**c**) R = 52 Ω, d_{Qs} = 1, η = 90.8%; (**d**) R = 20 Ω, d_{Qs} = 1.

As Figure 10 shows, before Q_{1a} is ON, the voltage across Q_{1a}, $\boldsymbol{V}_{Q1a}$, has already reached zero. Hence, ZVS is accomplished in above mentioned four cases. However, when R is 52 Ω and Q is below 1, Q_{1a} is hard-switching OFF. Additionally, when R_{ac} is small, the theoretical minimum of L is above 51 μH so that the quasi-CCM occurs, and $\boldsymbol{I}_{L1}$ is below zero for a period of time, which means L_1 is charged by the resonant network and a circulation current exists in L_1 and L_2. When R_{ac} augments, the value 51 μH satisfies Equation (21) and the circulating current is eliminated as illustrated in Figure 10b,c. Two conclusions can be drawn. Firstly, the deviation of the optimal load will reduce the efficiency comparing Figure 10b with Figure 10c. Secondly, the elimination of the circulation current can increase the efficiency as can be observed by comparing Figure 10b with Figure 10a,c. Besides, when the load decreases and Q increases above 1, a zero-cross point (ZCP) occurs before Q_{1a} is OFF and $\boldsymbol{I}_{Q1a}$ reverses its direction as Figure 5b demonstrates. Then $\boldsymbol{I}_{Q1a}$ can flow through the parallel diode for freewheeling rather than be forced to abruptly discontinue, which achieves the soft-switching OFF Q_{1a} as analyzed.

4.2. Equivalent Resistance of SAB and Variation Trend

In Section 3, the equivalent resistance of SAB R_{act} is regarded as a pure resistance according to the analysis on full-wave rectifier [30] and half-wave rectifier. To validate this assumption, we have Q_s working at 8500 Hz with d_{Qs} = 0.5. Waveforms of $\boldsymbol{I}_p$, $\boldsymbol{I}_s$, and $\boldsymbol{V}_s$ are presented in Figure 11. The purple dotted lines show that $\boldsymbol{I}_p$ lags 90° behind $\boldsymbol{I}_s$ so $j\omega_s M\boldsymbol{I}_p$ is in phase with $\boldsymbol{I}_s$ which conforms to Equation

(8). Moreover, the dark dotted lines show that the fundamental voltage $\boldsymbol{V}_s$ and $\boldsymbol{I}_s$ are also in phase. These phases verify a purely resistive equivalent impedance.

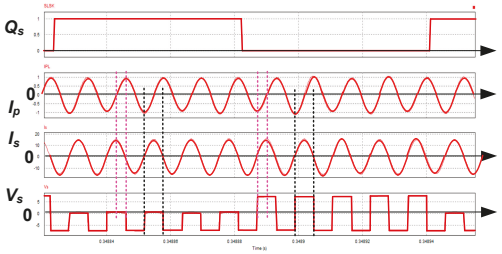

Figure 11. Phase differences in the Tx.

To further evaluate the impact of frequency ratio n and duty ratio d_{Qs} on the system, the simulation results of the output dc voltage, transferred power, and efficiency under different conditions are depicted and compared in Figure 12. Q_s works at three frequencies, 8500 Hz (i.e., n = 10), 17,000 Hz (i.e., n = 5), and 42,500 Hz (i.e., n = 2).

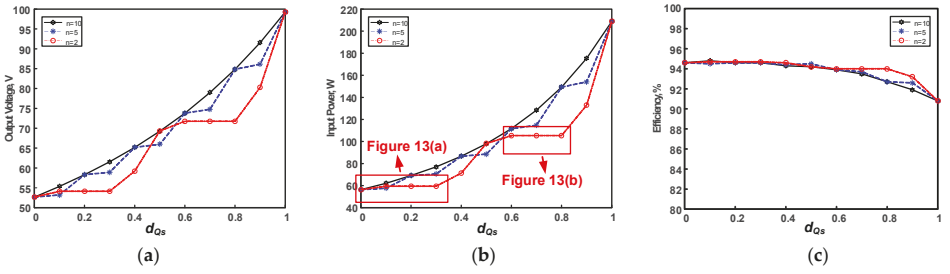

Figure 12. System performance under different frequencies and duty ratios (**a**) output voltage (**b**) input power (**c**) efficiency.

From Figure 12a, it is observable that the output voltage grows with the increase of d_{Qs}, which verifies the voltage boost function as claimed and also reflects the rise of R_{ac} according to Equation (15). Besides, the increase of input power can prove the negative correlation between R_{act} and $\boldsymbol{I}_L$ as already presented in Equation (6). In addition, it can be observed that the system has the same input power and output voltage once the product of n and d_{Qs} is integral and d_{Qs} stays the same. The integer of $n{\cdot}d_{Qs}$ means that a switching-ON period of Q_s contains an integral multiple of the resonant period, as does the switching-OFF period. On the other hand, an identical d_{Qs} means an identical proportion of the on-load time and idle time as presented in Figure 6. Accordingly, the equivalent ac load remains the same. If the switching-ON period of Q_s does not contain an integral multiple of the resonant period, the output voltage and input power may rise disproportionately as the blue line and the red line show. This phenomenon occurs because the effective proportions of the on-load time and idle time does not change. The examples in Figure 13 should suffice to demonstrate the stated where $n{\cdot}d_{Qs} \leq 0.5$ or $0.5 \leq n{\cdot}(1 - d_{Qs}) \leq 1$.

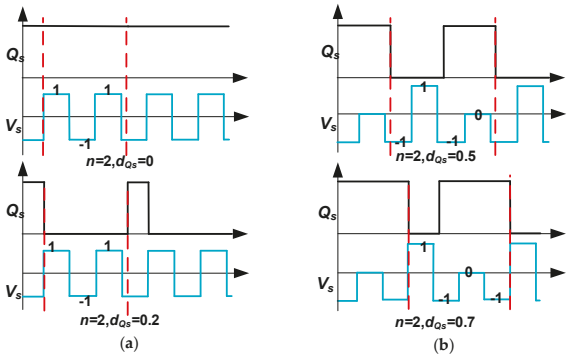

Figure 13. Impact of n and d_{Qs} on the equivalent impedance when $n \cdot d_{Qs}$ is small (**a**) $n \cdot d_{Qs} \leq 0.5$ (**b**) $0.5 \leq n \cdot (1 - d_{Qs}) \leq 1$.

Therefore, a large frequency ratio, i.e., a low operation of the receiving side, allows the power to grow in a linear fashion. However, if Q_s works at a low frequency, the ripple of the output voltage gets large, which may be unbearable for battery charging. For instance, the system output voltages, input powers, and efficiencies are totally identical when Q_s operates at 8500 Hz and 4250 Hz, theoretically. Nevertheless, the ripples at 4250 Hz operation are three times those at 8500 Hz. Thus, there is a trade-off between the system variation linearity and the output ripples considering the practical application. It is worth noting that the switching loss of the MOSFETs is not considered in the simulation, which will rise with the increase of the operating frequency. In this paper, Q_s conducts at 8500 Hz as recommended.

5. Experimental Result and Discussions

To validate and evaluate the aforementioned analyses and simulations, a practical prototype was established and tested. Figure 14 shows the laboratory prototype and its component configurations have been already tabulated in Table 1 in Section 4. However, the actual value of the load was 51.2 Ω and the switching frequencies of the Tx and the Rx were 86 kHz and 8600 Hz, respectively. The DSP TMS320F28335 (San Jose, CA, USA) was used as the digital controller in this system. MPP (Ni-Fe-Mo) cores were chosen for L_1, L_2, and L_a for lower loss. The coil diameter is 37 cm and the coil-to-coil gap is set as 10 cm. The inductances are measured by a Keysight E4980AL (Santa Rosa, CA, USA) LCR meter under 86 kHz.

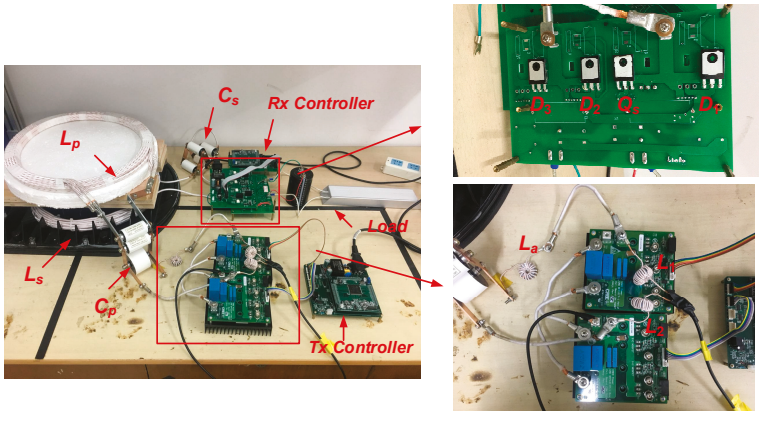

Figure 14. Prototype of the proposed system.

5.1. Soft-Switching Realization

All the four switches on the transmitter can perform ZVS under wide power variation as analyzed. The dead time is set as 2% of the resonant period. The waveforms of the four switches in three cases (Q_s stays OFF, d_{Qs} = 0.5, and Q_s stays ON) are presented in Figure 15. The input power is the smallest when Q_s keeps OFF, and the output current $\boldsymbol{I}_L$ distorts as claimed in Section 3 and is presented in Figure 15b. Nevertheless, ZVS of the four switches are achieved successfully as presented in Figure 15a. After Q_s operates, both the input power and the loaded quality factor rise. When d_{Qs} = 0.5, $\boldsymbol{I}_L$ is different from each other in every resonant period but $\boldsymbol{I}_{L1}$ keeps periodic variation. Hence, the current $\boldsymbol{I}_{L1}$-$\boldsymbol{I}_L$ provided for ZVS keeps changing in Figure 15d. However, ZVS of the top-side switches is still realized and ZVS of the bottom-side is also achieved most of the time as illustrated in Figure 15c. When Q_s stays on, $\boldsymbol{I}_L$ approximates to sine. As can been seen, all the switches can conduct ZVS as presented in Figure 15e. However, the soft switching-OFF for the top side switches is not achieved. The red lines in Figure 15b,d,f denote the result of $\boldsymbol{I}_{L1}$ minus $\boldsymbol{I}_L$, and the waveforms, when Q_{1a} is going to be turned OFF, are emphasized by the ellipse. At that time, the result $\triangle I$ being negative denotes that there is a current flowing from the source electrode of Q_{1a} to its drain electrode. Therefore, the hard-switching OFF is inevitable.

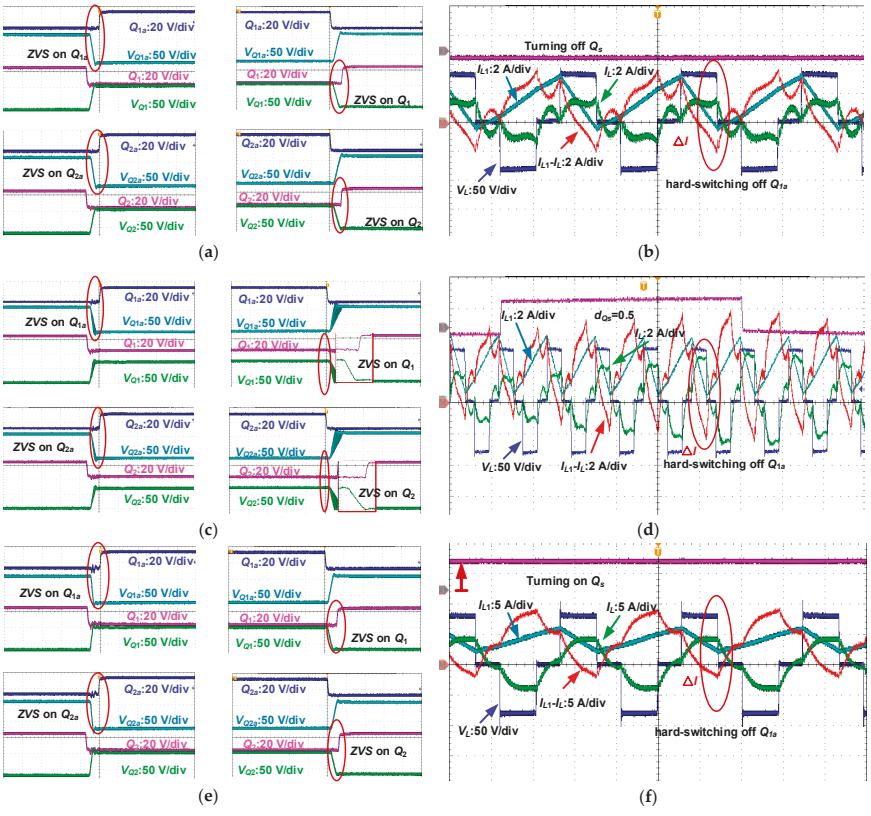

Figure 15. ZVS waveforms under different cases: (**a**) ZVS of four switches when d_{Qs} = 0; (**b**) current waveforms when d_{Qs} = 0; (**c**) ZVS of four switches when d_{Qs} = 0.5; (**d**) current waveforms when d_{Qs} = 0.5 (**e**) ZVS of four switches when d_{Qs} = 1; (**f**) current waveforms when d_{Qs} = 1.

On the Rx, soft switching of Q_s can also be achieved. Figure 16a,b demonstrate the waveforms of $\boldsymbol{V}_s$ and $\boldsymbol{V}_{Qs}$ at different d_{Qs} conditions. It can be observed that if Q_s is turned ON/OFF when $\boldsymbol{V}_s$ is negative and $\boldsymbol{V}_{Qs}$ is zero as illustrated in Figure 3c,e, voltage distortion does not occur. Nevertheless, in practice, $n \cdot d_{Qs}$ is not always an integer, thereby resulting in three switching situations: Q_s hard switching ON, Q_s hard switching OFF, and Q_s hard switching ON/OFF. To estimate the hard-switching impact, d_{Qs} is set as 0.4, and n is set as 10. Then Q_s works in soft-switching ON/OFF case as shown in Figure 16c and hard-switching ON/OFF as shown in Figure 16d. When $\boldsymbol{V}_s$ and $\boldsymbol{V}_{Qs}$ are positive, Q_s is turned ON. The current path switches from Figure 3b to Figure 3d compulsively, leading to a distortion denoted by the ellipse 1 in Figure 16d. When $\boldsymbol{V}_s$ and $\boldsymbol{V}_{Qs}$ are positive, Q_s is turned OFF. The current path switches from Figure 3d to Figure 3b compulsively, leading to a distortion denoted by the ellipse 2 in Figure 16d. It is found that when the input power is 103.2 W, the former efficiency is 93.3%, a little higher than the latter efficiency of 92.7%, saving switching loss of 0.5 W.

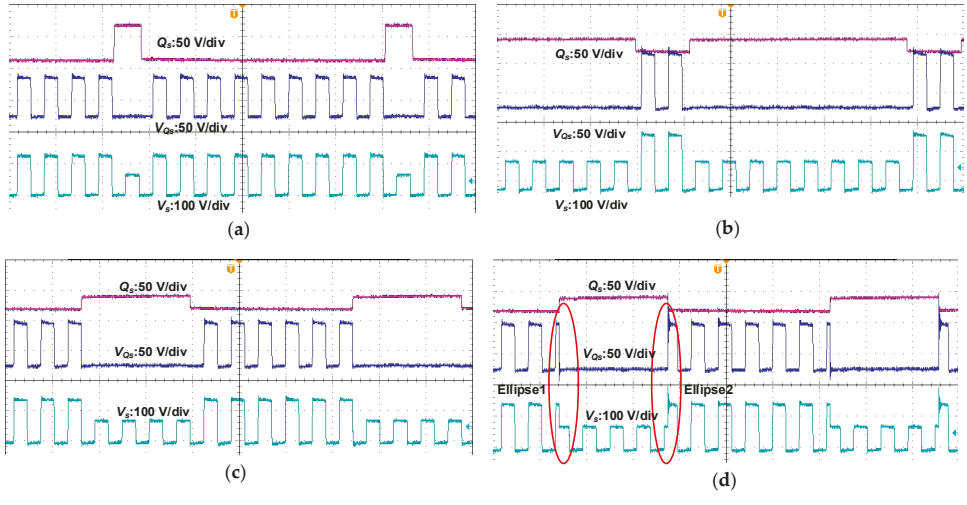

Figure 16. Waveforms of $\boldsymbol{V}_s$ and $\boldsymbol{V}_{Qs}$ with different d_{Qs}: (**a**) $d_{Qs} = 0.1$ (**b**) $d_{Qs} = 0.8$ (**c**) $d_{Qs} = 0.4$ (**d**) $d_{Qs} = 0.4$ but hard switching.

Additionally, $\boldsymbol{I}_{L1}$ is observed to analyze the impact of the equivalent load and the front-end inductance. At first, the value of L_1 and L_2 is set as 51 μH. When Q_s stays OFF, both the input power and the equivalent impedance are small. The inductance, 51 μH, is much less than the proposed value, 107 μH. Part of $\boldsymbol{I}_{L1}$ is below zero as depicted in Figure 17a, thereby showing a circulating current exists in L_1 and L_2. However, with the increase of the equivalent impedance, the value of 51 μH meets the requirements. Hence, the circulating current is eliminated and $\boldsymbol{I}_{L1}$ is always above zero as presented in Figure 17b,c.

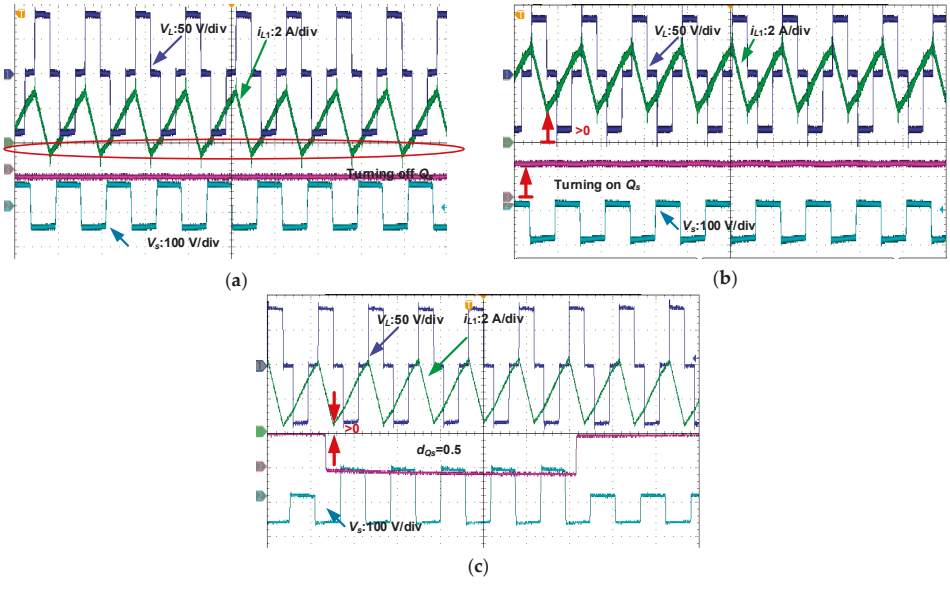

Figure 17. Waveforms of $\boldsymbol{I}_{L1}$, $\boldsymbol{V}_p$, and $\boldsymbol{V}_s$: L_1 is 51 µH but the equivalent impedance R_{act} changes (**a**) Q_s stays OFF, R_{act} reaches the maximum, part of $\boldsymbol{I}_{L1}$ is below zero; (**b**) Q_s stays ON, R_{act} reaches the minimum, $\boldsymbol{I}_{L1}$ is above zero; (**c**) Q_s operates with d_{Qs} = 0.5, $\boldsymbol{I}_{L1}$ is above zero.

5.2. Efficiency and Loss Estimation

Figure 18 demonstrates the system efficiency and the loss estimation. The blue dashed line presents the simulation result and the dark line presents the experimental result. Figure 18a shows that a higher output voltage more than the input voltage 24 V, is accomplished and boosted further after Q_s working. The results support the calculation of Equation (16). The experimental output voltage at the beginning is the same as the simulation but deviates from the theoretical value with the increasing of d_{Qs} and system operation power. Besides, the input power of the experiment is a little higher than that of the simulation power when d_{Qs} is below 0.5, whereas this situation reverses after d_{Qs} becomes above 0.5. This difference is mainly caused by the modelling of the SAB in the simulations. At first, the practical forward voltage drop is not invariably 0.6 V but increase from 0.6 V to 0.8 V. The deterioration of the voltage drop can be regarded as the increase of R_{act}, thereby decreasing the practical input power according to Equation (17). In addition, the input current surging from 2.8 A to 8.7 A and the temperature rise may result in the parameter drift and the difference presented in Figure 18. High efficiency is achieved over the variation of d_{Qs} as depicted in Figure 18c. Although the efficiency drops with d_{Qs} rising, 88% efficiency is sustained. In general, the results of the established simulation and experimental prototype are accordant and validate the proposed topology and methods. High efficiency can still be obtained though three inductors are added into the WPT system.

Based on the data presented in Figure 18a,b, the power losses can be calculated. When Q_s stays OFF, the power loss is 5.31 W, where the losses caused by the rectifier (0.6 V drop) and the inner resistance of the front-end inductors L_1 and L_2 (0.2 Ω) are obvious and make the main percentage as presented in Figure 18d, where d_{Qs} is 0. After Q_s operates and the power transfer rate rises, the loss ratio of the front-end inductors and the Rx coil increases as shown in Figure 18d where d_{Qs} is 1. Hence, there are two ways to improve the system efficiency. One is decreasing the high-frequency resistance by optimizing the inductors and determining a proper value according to Equations (21) and (25). Another method is reducing the receiver coil resistance with optimal coil manufacturing. Otherwise the output rate reduces according to Equations (16) and (17).

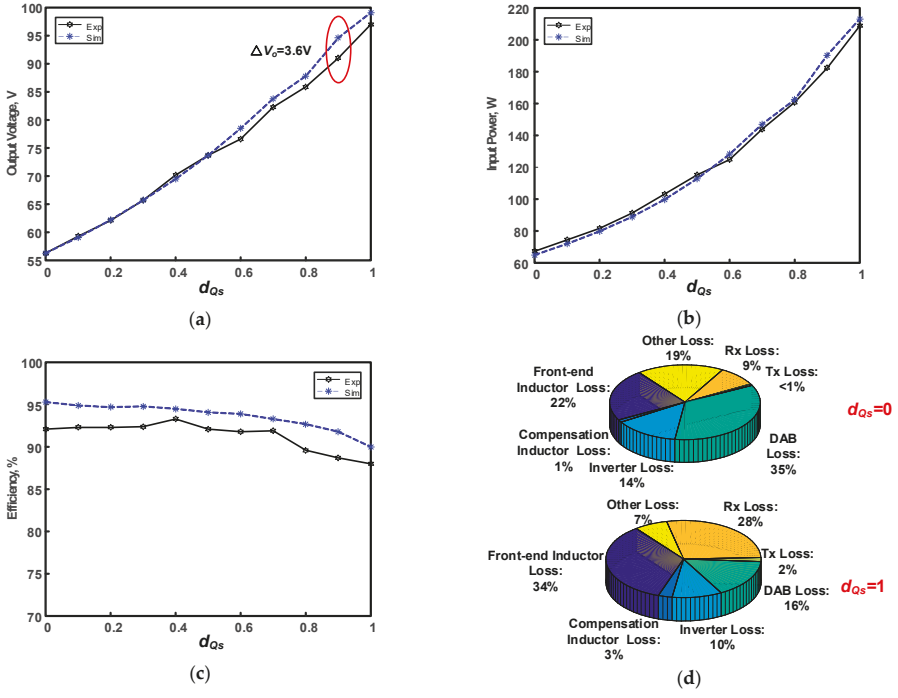

Figure 18. Efficiency and power loss comparison (**a**) V_o vs. d_{Qs}; (**b**) P_i vs. d_{Qs}; (**c**) η vs. d_{Qs}; (**d**) loss analysis of extreme working cases.

5.3. Load Tripping

To further present the advantage of LCL topology to the load tripping as aforementioned, experiments are added for validation. For convenience, the Tx coil will be artificially removed to imitate the load tripping scenario. Figure 19 shows the variation of $\boldsymbol{I}_L$ and $\boldsymbol{I}_P$. Over the working time, $\boldsymbol{I}_P$ stays constant even though the load is off, which is in accordance with the analysis of Equation (7). However, $\boldsymbol{I}_L$ varies when the load is off and on. $\boldsymbol{I}_L$ becomes small when the load is off, but becomes large again when the load is reconnected. Moreover, it can be seen that the whole system remains safe all the time.

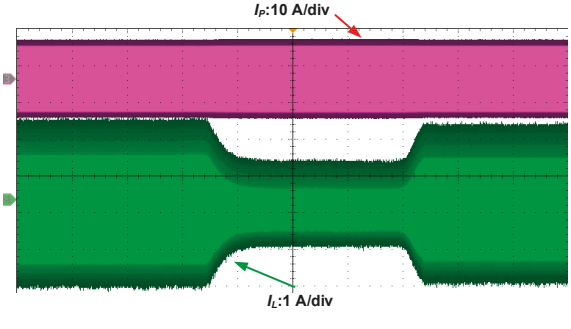

Figure 19. Waveforms of $\boldsymbol{I}_L$ and $\boldsymbol{I}_P$ when load tripping occurs.

6. Conclusions

The LCL topology is regarded as an ideal network used in the WPT systems due to its constant resonant current in the Tx coil and independence of the reflected impedance of the receivers. However, this topology requires a large source voltage to generate transmitting current and induced voltage of receivers, which limits its application in the low voltage scenarios, such as 12~24 V. This paper applied a CFI into WPT systems to boost the voltage for LCL. ZVS of the switches were accomplished under wide range of power rates and also under serious current distortion. The ability of the CFI to turn OFF the top-side switches softly was also deduced and presented in this paper.

On the receiving side, a SAB was proposed and applied to regulate and boost the output voltage and the system power. The SAB allows a lower frequency and reduces the communication requirement compared with the DAB synchronization. Higher output voltage and wide variation range were accomplished.

Guidelines on the parameter design of the front-end inductance, coils and optimal load were elaborately presented. Although more inductors were added into the system, a peak efficiency of 93.3% was obtained and the lowest efficiency was maintained at 88% with proper configuration. Both simulations and experimental results are conducted to verify the aforementioned analysis. Furthermore, optimization methods for efficiency improvement is included in this study.

Author Contributions: H.T., X.Y., and T.W. conceptualized the main idea of this research project; T.W. designed and conducted the experiments with the help of M.A. and X.L.; T.W., X.L., and N.J. checked and analyzed the results. T.W. wrote the whole paper; M.A. reviewed and edited the paper.

Funding: This work was funded by United Foundation of NSFC-Henan (U1604136).

Conflicts of Interest: The authors declare no conflict of interest.

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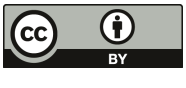

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Article

Simulation Model of a 2-kW IPT Charger with Phase-Shift Control: Validation through the Tuning of the Coupling Factor

Javier Vázquez [1]*, Pedro Roncero-Sánchez [1] and Alfonso Parreño Torres [2]

[1] Institute of Energy Research and Industrial Applications, University of Castilla-La Mancha, Campus Universitario S/N, 13071 Ciudad Real, Spain; Pedro.Roncero@uclm.es
[2] Institute of Industrial Development, Castilla-La Mancha Science and Technology Park, Paseo de la Innovación 1, 02006 Albacete, Spain; Alfonso.Parreno@pctclm.com
* Correspondence: Javier.Vazquez@uclm.es; Tel.: +34-926-295300

Received: 5 September 2018; Accepted: 14 October 2018; Published: 16 October 2018

Abstract: When applied to road vehicle electrification, inductive power transfer (IPT) technology has the potential to boost the transition from combustion engines to electric motors powered by a battery pack. This work focuses on the validation of a PSpice circuit model developed as a replica of a 2-kW IPT prototype with series-series compensation operating at 18.65 kHz. The laboratory prototype has the three stages commonly found in an IPT system: an inverter, controlled by the phase-shift technique, a coil coupling and a load. Simulations were run with the circuit model for three different distances between the two coils of the inductive coupling, all of which are of interest for practical chargers: 125, 150 and 175 mm. The validation approach was based on tuning the magnetic coupling factor for each distance and a set of ten load resistances, until the best match between the simulated and the experimental peak currents supplied by the inverter was found in each case. The coupling factors obtained from the simulation work are in good agreement with their experimental counterparts for the three distances, provided the duty cycle of the inverter output voltage is not too small. The circuit model developed is, therefore, able to reproduce the behavior of the laboratory prototype with sufficient accuracy over a wide range of distances between coils and loading conditions.

Keywords: electric vehicle; wireless power transfer; inductive coupling; coupling factor; phase-shift control; series-series compensation; PSpice

1. Introduction

The applications of wireless power transfer (WPT) technology, which is the contactless transmission of power by an electromagnetic field and was pioneered by Nikola Tesla over a century ago, cover an increasingly wider range of electrical goods. Some examples are cell phones, medical implants, engine telemetry, home electronic appliances, such as electric toothbrushes or some of the robot vacuum cleaners that have recently appeared, and electric vehicles (EV) [1,2]. Magnetic coupling WPT, which is a special case of non-radiative (or near-field) transmission [1,3], is suitable for power transfer over the moderate distances that are typical in EV wireless charging. For longer distances, the transmission of energy necessarily involves electromagnetic radiation. This has, in recent years, become a mature area of expertise, as evidenced by the large number of scientific papers and patent applications in the field, which began to increase considerably in 2008 and have continued to do so [4].

The electricity storage technology utilized to power an EV is, to date, arguably a major deterrent to those drivers who might be willing to make the transition from a combustion engine vehicle to a

pure EV, in the context of increasing environmental awareness. Unfortunately all battery technologies, even those currently regarded as the most advanced for use with EVs, as is the case of lithium-ion batteries [5], still lack competitiveness owing to a limited life time, a high cost, long recharging cycles and low energy density [6]. Their energy density is much lower than that of fossil fuels, which severely limits the autonomy of EVs as regards traveling long distances. While the battery performance affects all EVs equally, regardless of their charging technology (either conductive or wireless), the lack of a charging cable is an attractive feature that could promote the deployment of wireless solutions in the near future.

Charging by means of magnetic coupling WPT can be either static or dynamic. During static charging, the EV remains stationary while the battery is charged, as opposed to dynamic charging, when the EV is in motion on an energized track consisting of a sequence of road-embedded coils to which a current is supplied in synchronism with the position of the vehicle [7]. The dynamic charging exacerbates the challenges, but in turn avoids the need for a high capacity battery [8].

The core of a typical inductive power transfer (IPT) EV charger consists of a pair of looselycoupled coils. The transmitting coil, which is placed on the primary side, is driven by an alternating signal source and transfers energy to the receiving coil on the secondary side by guiding some of the magnetic flux that is generated across the air gap between both windings, just like a transformer does, by using the principle of electromagnetic induction [3]. Owing to the weakness of the magnetic coupling, a fraction of the magnetic flux generated by the primary coil fails to reach the secondary coil, giving rise to a leakage flux, which is represented by leakage inductances. The strength of the coupling, characterized by the coupling factor k, is low in IPT systems.

It is common practice to add compensation capacitors to both sides of the magnetic coupling, connected either in series or in parallel with the respective coils and designed in such a way that the transmitter and the receiver resonate at the same frequency. The resulting topologies are labeled SS, SP, PS and PP [9,10], where S stands for series and P for parallel. When the system is driven at the resonance frequency, the compensation capacitor on the transmitter side minimizes the reactive power provided by the power supply, whereas the compensation capacitor at the receiver maximizes the power transfer [11]. This resonant scheme has also been denominated as RIPT (resonant inductive power transfer) [12] or ICPT (inductively coupled power transfer) [8] in order to distinguish it from the initial non-resonant IPT scheme; in practice, however, researchers tend to use the abbreviation IPT to refer to the resonant topology, and this term is currently in widespread use.

Although each of the four basic compensation topologies have their own pros and cons, a comparative analysis in terms of efficiency, power transfer and other relevant criteria concludes that the current-source-type SS and SP compensation schemes are superior to the others [13]. One of the outstanding advantages of the SS topology for EV charging, which is not shared by any of the other three, is that the compensation capacitor on the transmitter side is independent of both the coupling factor and the load [9,14,15]. Despite some of the inherent problems of the SS topology, such as high voltages across the compensation capacitors or a drastic increase in the primary current if the secondary side is left open-circuited unintentionally [14,16], the SS topology is a usual choice when designing IPT-based EV chargers [10,14,17–23]. It should be pointed out, however, that IPT chargers cannot currently compete with conductive chargers in terms of efficiency: while conductive chargers achieve an overall efficiency of above 90%, IPT chargers fall below that figure. Reported values obtained under optimal operation conditions range from 84% to 88% [14,18,20,24]. Moreover, a mismatch in the coil alignment or an increase in the air gap contribute to a decrease in the overall efficiency.

In a practical IPT charger, the strength of the magnetic coupling is sometimes boosted with the use of ferrite cores placed on both sides of the coupling [6,18–20,25]. The stray magnetic field can be shielded with an aluminum plate placed on the receiving side and attached to the chassis of the EV [6,18,25]. The SAE-J2954 standard [26], which was released as a guideline in 2013 and issued in 2016, replaces the previous recommendation practice SAE-J1773 for EV inductively-coupled charging and establishes a nominal operating frequency for the driving signal of 85 kHz. This moderate frequency

makes magnetic coupling WPT no different from IPT [6]. Some prototypes that adhere to SAE-J2954 have recently been demonstrated [18,20,27]. It should be pointed out that SAE-J2954 was issued as a recommended practice, whose technical specifications, including the nominal frequency of operation, are pending re-evaluation after 2018.

This paper presents work whose objective is to validate a PSpice simulation model that was built as a replica of a 2-kW SS-compensated IPT prototype and which was tested experimentally in a previous work for three distances between coils that fall in the range of the expected ground clearance of light-duty EVs [14]. The validation procedure consisted of comparing the coupling factors provided by the model with their experimental counterparts for the same three air gaps and ten loading conditions for each of them. The proposed approach, based on the tuning of the coupling factor, can be readily adapted to simulate the behavior of IPT prototypes other than the one discussed in this work, including those featuring ferrite cores, which are more difficult to characterize by purely analytical methods. The simulation model can, therefore, be regarded as a practical design tool capable of providing reliable information during the development process of an IPT system. Section 2 begins with a brief analysis of the circuit of a general IPT system with SS compensation, which provides the minimum theoretical framework required to verify whether the results are in agreement. The laboratory prototype on which the simulation model is based is described in Section 3. Section 4 focuses on how the coupling factors for the air gaps under study were determined in an experimental manner using measurements carried out only in the inductive coupling stage. Section 5 contains a thorough stage-by-stage description of the circuit model developed. The definitive k factors obtained with the model are the result of a tuning process that seeks the best match between the experimental and the simulated peak amplitudes of the current waveforms supplied by the inverter. The corresponding results, which lead to the validation of the model, are analyzed in Section 6. A comparative study between the experimental and the simulated current waveforms, on which the tuning procedure is based, follows in Section 7. The conclusions are summarized in Section 8.

2. Circuit Analysis of an IPT System

The general scheme of an IPT system comprises three stages: a primary section, supplied by a grid, followed by a compensated inductive coupling with a primary and a secondary coil and finally by a secondary section that charges a battery. The primary coil is driven by an alternating signal supplied by a full-bridge inverter located in the primary section. The voltage induced across the secondary coil is, in turn, rectified and conditioned prior to feeding the battery, sometimes with the insertion of a DC/DC converter or simply with a filter capacitor. The battery is usually replaced in laboratory prototypes with a variable resistor R that reflects its state of charge (SOC) at a given time of the charging process [1]. Figure 1 depicts the three stages particularized for the SS-compensated IPT prototype used in this work.

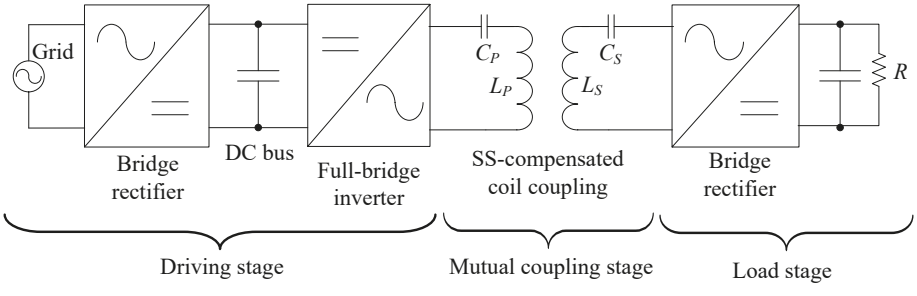

Figure 1. Constructed IPT prototype: general scheme. S, series.

A simplified equivalent circuit of the entire IPT prototype is shown in Figure 2. The circuit, which models the mutual coupling stage by means of a T-network, can be analyzed via a fundamental harmonic approximation (FHA) owing to the presence of a sinusoidal voltage source $v_P(t)$ that represents the fundamental component of the voltage that drives the primary coil generated by the inverter. FHA is a widely-used approach in the context of IPT systems that simplifies the analysis without compromising the accuracy, since the harmonic content of the resonant currents is usually low owing to the high quality factors of the resonant tanks [18].

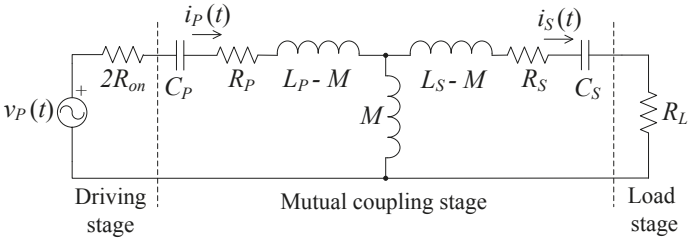

Figure 2. IPT prototype: equivalent circuit.

The conduction resistance of any of the four inverter switches is modeled with R_{on}. Since two switches are closed at any given time when an AC output is synthesized from a DC input, the circuit model includes the resistance $2R_{on}$ in series with the driving voltage. The resistance R_P results from the sum of two contributions located in the primary section and connected in series: the stray series resistance of the primary coil, R_{L_P}, and the stray series resistance of the primary capacitance, R_{C_P}. The resistance R_S is, in turn, the sum of the stray series resistances of the secondary coil, R_{L_S}, and that of the secondary capacitance, R_{C_S}. R_L accounts for the equivalent resistance of the rectifier stage and the battery. M represents the mutual inductance between the two coils, which relates to k and to the primary and secondary self-inductances L_P and L_S through the following expression:

$$M = k\sqrt{L_P L_S} \tag{1}$$

Leakage inductances on the primary and the secondary sides, L_{Pk} and L_{Sk}, can be expressed as a function of either k or M and the primary to secondary turns ratio $r = N_P/N_S$:

$$L_{Pk} = (1-k)L_P = L_P - rM \tag{2}$$

$$L_{Sk} = (1-k)L_S = L_S - M/r \tag{3}$$

Note that the inductances L_P–M and L_S–M that appear in the T-model coincide with L_{Pk} and L_{Sk} only if r = 1. Expressions (1), (2) and (3) show that IPT systems, for which k is necessarily low, have non-negligible leakage inductances.

In the phasor domain, the impedance seen from the primary side, Z_P, can be written as:

$$Z_P = \frac{\overline{V_P}}{\overline{I_P}} = 2R_{on} + R_P + j(X_{L_P} + X_{C_P}) + Z_R \tag{4}$$

where Z_R is the reflected impedance, which depends on circuit elements present on the secondary side:

$$Z_R = \frac{\omega^2 M^2 [R_S + R_L - j(X_{L_S} + X_{C_S})]}{(R_S + R_L)^2 + (X_{L_S} + X_{C_S})^2} \tag{5}$$

Since the primary and secondary resonant circuits are designed to resonate at the same frequency, the common resonance frequency is given by:

$$\omega_r = \frac{1}{\sqrt{L_S C_S}} = \frac{1}{\sqrt{L_P C_P}} \tag{6}$$

When the circuit is driven at the resonance frequency, both the reactances on the primary side, X_{L_P} and X_{C_P}, and those on the secondary side, X_{L_S} and X_{C_S}, cancel each other out. Z_P is thus simplified to an expression without imaginary part, where V_P and I_P represent the peak amplitudes of their corresponding voltage and current phasors:

$$Z_P(\omega_r) = \frac{V_P}{I_P} = 2R_{on} + R_P + \frac{\omega_r^2 M^2}{R_S + R_L} \tag{7}$$

On the other hand, the power delivered to the load stage, represented by R_L, is [17,18,21]:

$$P_L = \frac{(\omega_r M V_{P\text{rms}})^2 R_L}{[(R_L + R_S)R_P + \omega_r^2 M^2]^2} \tag{8}$$

Finally, the efficiency of the mutual coupling stage can be calculated as follows: [14,17]:

$$\eta_{\text{IPT}} = \frac{R_L}{R_L + R_S + \frac{R_P(R_L+R_S)^2}{\omega_r^2 M^2}} \tag{9}$$

3. Laboratory Prototype

Figure 3 shows the three stages of the constructed prototype in a single image, along with the control electronics and the instrumentation utilized, all of which are described below.

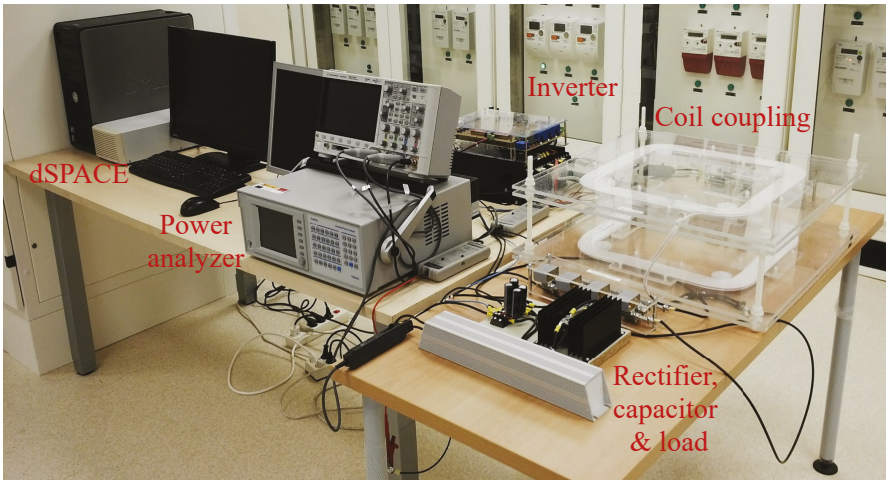

Figure 3. Laboratory prototype with control electronics and instrumentation.

3.1. Driving Stage

The driving stage, which was fed from a single-phase 230 V/50 Hz outlet of the power grid, features an AC/DC converter that provides a stable DC bus voltage V_{DC}, followed by an H-bridge inverter based on IGBT switches. The driving function was implemented using two legs of a modular three-phase inverter connected to the grid, purchased from Semikron Electronics S.L., Barcelona, Spain. It includes a bridge rectifier (ref. SK95D12), an IGBT module (ref. SK30GB128) and some additional electronics. Figure 4 depicts a simplified circuit diagram of the driving stage.

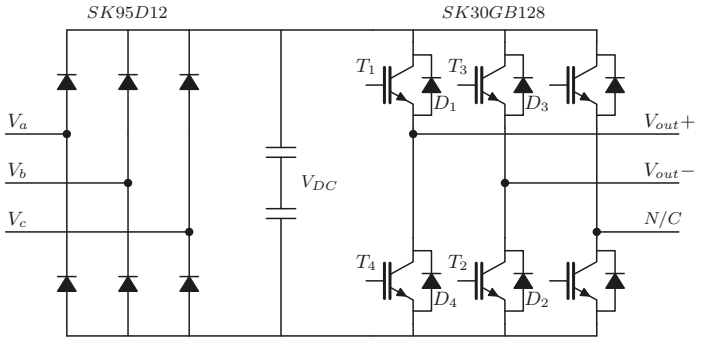

Figure 4. Driving stage: circuit diagram.

The bridge rectifier is characterized by a reverse voltage of 1200 V and a current of 95 A, whereas the IGBT switches support a collector-emitter voltage of 1200 V and a collector current of 25 A (all maximum ratings). Each of the two capacitors in Figure 4 results from a parallel arrangement of four capacitors rated at 680 µF and 400 V. The equivalent capacitance of the eight capacitors amounts thus to 1360 µF and is rated at 800 V. The features of the driving stage were expanded by means of a customized PCB attached to the top of the inverter: this includes a fiber optic interface to allow communication with a dSPACE control platform, a measurement unit of both the inverter leg currents and the DC bus voltage, and a module to protect against overcurrents.

Although the H-bridge inverter is a single-phase two-level voltage-source converter (VSC), its switching scheme is such that it does not produce a square wave output voltage, but rather a controlled one with intervals in which the output is both zero and $+V_{DC}$ and $-V_{DC}$. This controlled output with three output levels, whose duty cycle can be adjusted, is characteristic of a phase-shift control scheme. The inverter output voltage can be set to zero periodically during the so-called interval of zero voltage, whose duration can be regulated in the full range from 0 rad to 2π rad throughout each period. It is characterized by the zero-voltage angle α, which varies from 0 rad to $\pi/2$ rad. As can be seen in Figure 5, the trigger pulses V_{T1} and V_{T4}, which are applied to their respective IGBT gates located on the left leg of the inverter, are complementary. The same applies to the trigger pulses on the right leg, V_{T2} and V_{T3}. The four pulses have a duty cycle of 50%. The synchronization scheme results in a phase shift δ_{2-1} between the pulses V_{T2} and V_{T1}, on the one hand, and a second phase shift δ_{3-4} between V_{T3} and V_{T4}, on the other. Both of them are equal to 2α, whereas the interval of zero voltage is 4α throughout a period.

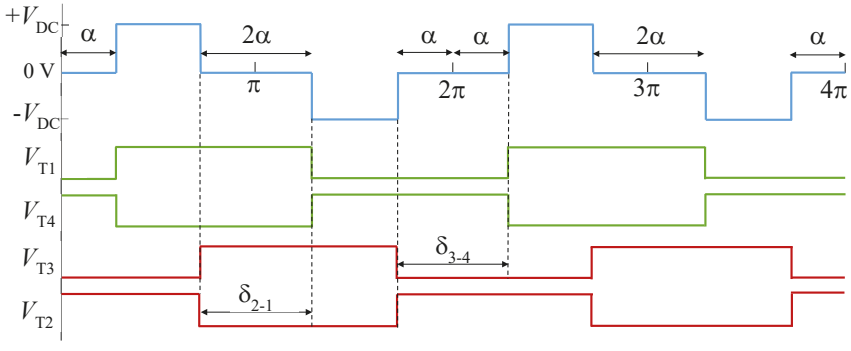

Figure 5. Phase-shift control scheme showing the displacement angles δ_{2-1} and δ_{3-4} that determine the interval of zero voltage in the inverter output voltage.

The amplitude of each harmonic that is present in the inverter output voltage waveform can be controlled by varying α, as stated in (10) [28].

$$V_n = \frac{4V_{DC}}{n\pi}\cos(n\alpha) \tag{10}$$

The inverter output rms voltage V_{rms} is, moreover, dependent on α [28]:

$$V_{\text{rms}} = V_{DC}\sqrt{1 - \frac{2\alpha}{\pi}} \tag{11}$$

The rms current supplied by the inverter to the primary coil can consequently be set to a given target value by simply selecting the appropriate angle α. An analog voltage, which is proportional to the α required, was generated by using a dSPACE 1103 (dSPACE GmbH, Paderborn, Germany) control platform. That voltage was, in turn, read by the IC UCC3895 (Texas Instruments, Dallas, TX, USA), a phase-shift PWM controller that generated the switching scheme shown in Figure 3 and is required to synchronize the trigger pulses V_{T1} to V_{T4}. The resulting inverter output voltage had a frequency of 18.65 kHz. Examples of IPT systems with an SS compensation topology featuring a phase-shift control scheme are those described in [14,20,29].

3.2. Inductive Coupling Stage with SS Compensation

Both circular and square coils have been reported in the construction of IPT prototypes. Considering that the mutual inductance M between square coils is $(4/\pi)^2$ times larger than between circular ones when the corresponding circumference is inscribed in the square [30], square rather than circular coils were chosen to design the coupling stage. The two coils, which were wound using Litz wire with a section of 6.28 mm^2, have 22 turns each with 11 turns piled up on top of the other 11, as Figure 6 illustrates.

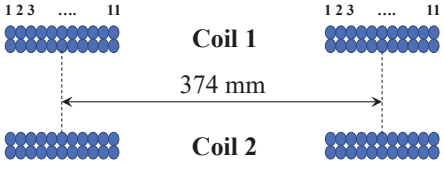

Figure 6. Constructed coils: cross-section.

Mechanical stability was achieved by sandwiching each coil between two methacrylate plates. The air gap between the coils can be manually adjusted to the desired value by means of nylon screws placed at the corners of the holding plates. The four screws also contribute to keeping the coils perfectly aligned and parallel to each other.

Each of the two compensation capacitances resulted from an arrangement composed of four branches connected in parallel and two polypropylene film capacitors connected in series per branch, with a nominal capacitance of 100 nF per capacitor (ref. MMKP386 F1230 manufactured by Vishay, Malvern, PA, USA). This arrangement is necessary to support the high voltages developed across the capacitors when the prototype operates at the resonance frequency.

3.3. Load Stage

The load stage comprises a high voltage rectifier followed by a capacitor arrangement with which to reduce the ripple current, which is in turn connected to a combination of power resistors.

The bridge rectifier was constructed by connecting two semiconductor modules (ref. STTH6006TV, ST Microelectronics, Geneva, Switzerland) . Each module includes two ultrafast diodes characterized by a peak reverse voltage of 600 V and an average forward current of 30 A (absolute ratings).

The filter capacitance was the result of combining four electrolytic capacitors in an arrangement composed of two branches connected in parallel with two capacitors connected in series per branch. Each capacitor is rated at 220 μF and 450 V, with a capacitance tolerance of ±20%.

The power resistors utilized were of a wirewound type rated at 800 W. Ten different ohmic values, from 2.5 to 40 Ω, were available from series and parallel combinations of resistors with a nominal resistance of 10 Ω.

3.4. Prototype Testing and Performance Figures

Tests were conducted for three air gaps between coils (125, 150 and 175 mm), which will henceforth be referred to as g_x, where x is the corresponding gap. The rms primary current, $I_{P\text{rms}}$, was kept at approximately 10 A via individual adjustments of the angle α for each air gap g_x and resistance R being tested. Controlling the current in the primary coil allows the series-compensated secondary side to resemble a voltage source [9].

The load power P_L depends strongly on both g_x and R. For g_{125}, the air gap for which the magnetic coupling is the strongest of all three, P_L reached 2 kW when R was 5 Ω (higher loads led to lower transferred powers). On the other hand, if the three air gaps are considered altogether, P_L was always above 1 kW for R = 5 Ω and below 500 W for R = 30 Ω. The overall efficiency, computed from grid supply to load, was 82.5% for the intermediate case of g_{150}. However, if only the coil coupling stage is taken into account, it exceeded 90%. Further details regarding the prototype performance can be found in [14]. It should be noted that, according to (9) , the efficiency of an SS-compensated inductive coupling stage depends, among other parameters, on the resonance frequency ω_r and the mutual inductance M, and an increase in either of them causes an increase in the efficiency. Figure 7 plots η_{IPT} calculated with (9) for the three air gaps and two different resonance frequencies (18.65 kHz and 85 kHz), with the load resistance R_L ranging from 2.5 Ω to 40 Ω. As can be seen, when the frequency is 18.65 kHz, η_{IPT} is above 90% only under certain operation conditions, in agreement with the efficiency figures found experimentally. However, for the case of 85 kHz, η_{IPT} represents a significant improvement, exceeding 95% for most of the loads and air gaps. Unfortunately, the desired increase in η_{IPT} that arises as a consequence of an increase in either M or ω_r is accompanied necessarily by a reduction in the power delivered to the load, as follows from (8). Consequently, an IPT system working at a relatively low frequency of operation, as in the case discussed in this work, is characterized by moderate efficiency figures that are compensated by an enhanced power transfer capability.

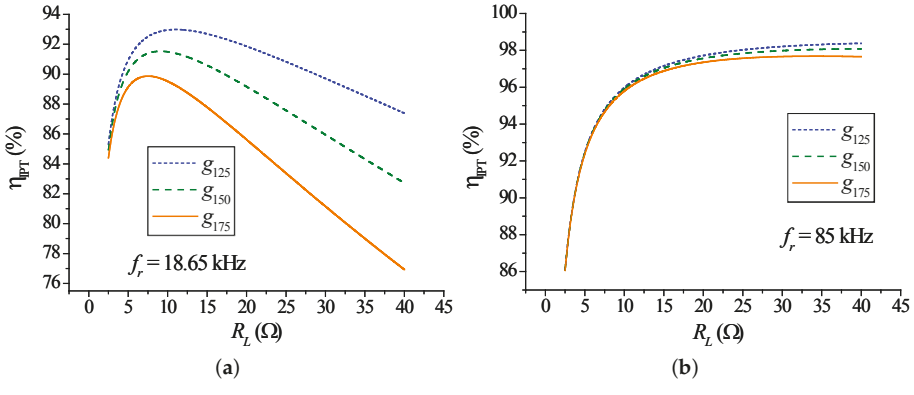

Figure 7. η_{IPT} versus R_L for two different frequencies of operation: (**a**) 18.65 kHz; (**b**) 85 kHz.

4. Experimental Determination of the Coupling Factor

A reliable figure for the coupling factor between two coupled coils can be obtained experimentally by applying the voltage ratio method, which consists of measuring the peak amplitude of the voltage waveform at each winding in open circuit conditions when a sinusoidal driving voltage is applied to the other winding [31]. The method, therefore, requires four voltage measurements for a given air gap between coils: the driving voltages at the primary and secondary windings, denoted by V_{dP} and V_{dS}, and the corresponding open circuit voltages, represented by V_{ocP} and V_{ocS}. Since the accuracy is improved if measurements are taken at a frequency at which the quality factor Q of the coils is high [31], the selected frequency of the driving voltage was 20 kHz. The experimental coupling factor obeys the following expression:

$$k_{\text{exp}} = \sqrt{\frac{V_{ocP}}{V_{dS}} \frac{V_{ocS}}{V_{dP}}} \tag{12}$$

Considering that, for a given amplitude of the voltage applied to the driving coil, the voltage across the open-circuited coil decreases as the air gap increases, the presence of noise on the voltage signals can compromise the accuracy of the measurements, especially in the case of large air gaps. Small driving amplitudes were, therefore, avoided. In order to verify whether or not there is a threshold for the driving amplitude below which the k values obtained lack accuracy, four sets of measurements were taken for each air gap, during which the driving amplitudes V_d were set to values of around 5, 10, 15 and 20 V. The resulting k values are represented in Figure 8.

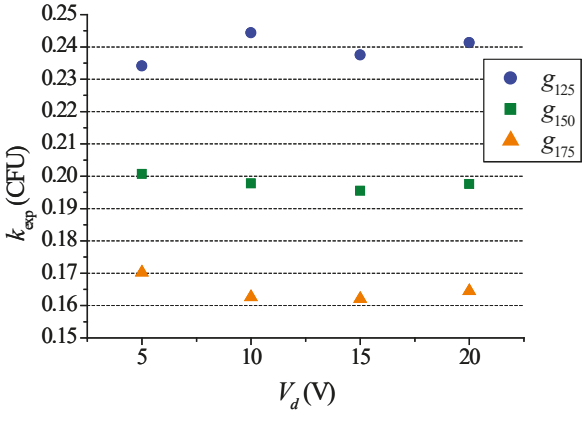

Figure 8. Determination of k_{exp} for four driving voltage amplitudes.

As can be seen, the method is able to distinguish among the three cases under study satisfactorily for every V_d. However, there is a noticeable upward deviation of the k factor obtained for g_{175} when V_d is 5 V with respect to the values that result from the other three amplitudes, which are not that different from each other. A similar deviation for 5 V, although more moderate, occurs for g_{150}. The same occurs with g_{125}, this time with a downward deviation. This analysis suggests that the driving voltage threshold sought is located somewhere between 5 and 10 V and measurements at 5 V were consequently ruled out. Although the remaining sets of measurements taken at 10, 15 and 20 V gave rise to similar k factors, the 20-V set can be regarded as the most reliable of all as its signal-to-noise ratio is the largest. The k values obtained with that set are represented in Table 1 and will be used as targets to be compared with the corresponding values resulting from the simulations.

Table 1. Coupling factors obtained experimentally (V_d = 20 V).

Air gap (mm)	125	150	175
k_{exp}	0.241	0.198	0.164

5. Circuit Model for Simulation

A preliminary version of the circuit model presented in this work was utilized to estimate k for the single case of g_{125} without prior knowledge of the corresponding experimental k factor to be used as a reliable reference for validation purposes [32]. This estimate of k relied on a successive approximation technique that, in turn, relied on experimental measurements of the primary peak currents for three loads (5, 10 and 20 Ω). It was not necessary to follow that approximate method here, since the experimental k values for the three air gaps were now available.

A schematic representation of the PSpice simulation model is shown in Figure 9. It has been improved when compared to the initial version, as a number of changes were made in both the inverter and the load stages. While the inverter topology remains the same, some of its parameters model the real device with more accuracy in the current version. With regard to the load stage, the refinements involve all the parts: the bridge rectifier model, the filter capacitor and the resistive load. A description of the three stages present in the circuit model follows below.

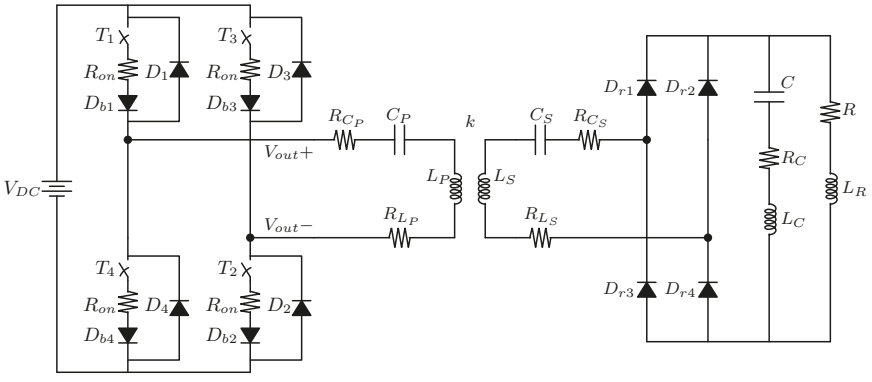

Figure 9. IPT prototype: circuit model.

5.1. Full-Bridge Inverter Stage

The four IGBTs were replaced with voltage-controlled switches denominated as T_1 to T_4. As IGBTs carry the current in one direction and block it in the opposite one, diodes D_{b1} to D_{b4} were added to provide the blocking functionality. Considering that the switches must carry both positive and negative currents when inductive loads are driven, all switches are equipped with reverse-parallel feedback diodes D_1 to D_4 that carry the negative current during a certain time interval throughout each period.

The switch model includes a non-zero on-resistance R_{on} equal to 48 mΩ corresponding to the IGBT module SK30GB128 (Semikron S.L., Barcelona, Spain), as reported in the manufacturer's datasheet under the name r_{CE} (typical value). The DC bus voltage V_{DC} was calculated by adding the voltage drop across the switches to the amplitude of the inverter output voltage experimental waveforms. The model parameters of the blocking diodes placed in series with the switches were purposely chosen to obtain a negligible drop in voltage across the diodes. The series resistance R_s was, therefore, set to zero and the emission coefficient n was set to 0.001. n is an empirical constant, also termed as the ideality factor, that appears in the exponential $i - v$ relationship of a diode. Reducing n makes the turn-on voltage of the diode $i - v$ characteristic to approach 0 V; however, convergence problems may arise if

n is made too small. In real diodes, n depends on both the material and the physical construction of the device [33]. Table 2 summarizes a selection of some key circuit parameters for the switch and for the two diode models present in the inverter. Other diode parameters not shown in the table adopt the default values of the PSpice Dbreak diode model.

Table 2. Inverter model: selected circuit parameters.

Switches T_1 to T_4			
$R_{on}(\Omega)$	$R_{off}(\Omega)$	$V_{on}(\mathrm{V})$	$V_{off}(\mathrm{V})$
0.048	1×10^6	1	0
Diodes D_{b1} to D_{b4}		**Diodes D_1 to D_4**	
$R_s(\Omega)$	n	$R_s(\Omega)$	n
0	0.001	0.1	1

5.2. Compensated Coil Coupling Stage

The inductive coupling was modeled with a PSpice device able to couple two or more coils through the corresponding coupling factors between each coil pair. The self-inductances of the primary and secondary coils, L_P and L_S, were measured using a 4294A precision impedance analyzer (by Agilent), with which the corresponding series stray resistances of the two coils, R_{L_P} and R_{L_S}, were also obtained. The two compensation capacitor arrangements were similarly measured in order to obtain both their capacitances C_P and C_S and their series stray resistances R_{C_P} and R_{C_S}, all of which are listed in Table 3.

Table 3. Compensated coil coupling model: circuit parameters.

Primary Side		**Secondary Side**	
C_P	186.9 nF	C_S	187.0 nF
R_{C_P}	32 mΩ	R_{C_S}	35 mΩ
L_P	393 µH	L_S	389 µH
R_{L_P}	369 mΩ	R_{L_S}	367 mΩ

5.3. Load Stage

The PSpice model files for the voltage rectifier STTH6006TV1 (STMicroelectronics, Geneva, Switzerland), which are available for download on the manufacturer's website, were added to the PSpice libraries. With regard to the filter capacitor arrangement, its equivalent circuit was simplified to a series RLC combination, as electrolytic capacitors form an RLC resonant circuit with a low Q [34]. Owing to the low Q, a measurement of impedance magnitude and phase versus frequency using an impedance analyzer revealed a broad impedance minimum centered around 90 kHz rather than the sharp resonance typical of resonators with a high Q, along with a slow change in the phase rather than an abrupt transition (ideally, from -90° to $+90^\circ$ at the resonance frequency). The frequency range chosen to obtain the equivalent RLC circuit covers four decades, from 50 Hz to 500 kHz, with the objective of capturing the most significant features of the frequency response on both sides of the resonance that are necessary for the impedance analyzer to calculate reliable model parameters. With regard to the power resistor, it was initially modeled with an $RL||C$ network, which is typical for wirewound resistors, as is the case here. However, in standard resistors of this type, the capacitance is so low that it is normally ignored, since resonance effects are virtually non-existent [34]. The model adopted was, therefore, a series RL combination. Owing to the construction of wirebound resistors, their equivalent series inductance is not negligible. In the present case, it amounts to 39.20 µH for one of the 10 Ω resistors used in the prototype. Note that if no ripple were present across the load resistor, the equivalent inductance would not play any role and it could, therefore, be safely removed from the resistor model. Since some ripple remained unfiltered on the rectified voltage signal despite the presence of the filter capacitor, the stray inductance L_R present in the power resistor was added to the model. Table 4. shows the corresponding circuit parameters.

Table 4. Load stage: circuit parameters.

Filter Capacitor		Load Resistor	
C	187.80 µF	R	10.21 Ω
R_C	718 mΩ	L_R	39.20 µH
L_C	325 nH		

6. Model Validation

Six input parameters had to be confirmed prior to running a simulation: the DC bus voltage V_{DC}, the switching frequency f, the zero-voltage angle α, the load resistance R with its series stray inductance L_R, and the coupling factor k. Simulations for each air gap were run with ten different load resistances, whose nominal values were 2.5, 5, 7.5, 10, 15, 20, 25, 30, 35 and 40 Ω. All possible combinations of different loads and air gaps led to a total of thirty angles α with which to keep $I_{P\text{rms}}$ controlled at around 10 A. Several k values were tentatively tried for all combinations of g_x and R until the best match between the experimental and the simulated primary peak currents was found, using three decimal digits for k. Following this iterative procedure for every combination of g_x and R yielded a set of ten k values for each air gap. The results, which are compared with the experimental k values in Table 1, are shown in Figure 10.

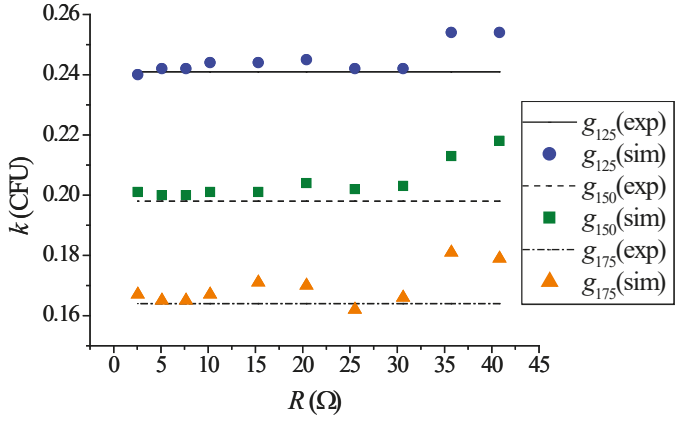

Figure 10. Coupling factors for the three air gaps and ten loads. Experimental and simulated data are represented by straight lines and discrete points, respectively.

Upon inspecting Figure 10, it is apparent that the model is capable of discriminating well among the three air gaps, although deviations from the expected k values are especially noticeable for the loads of 35 and 40 Ω. As a result of the phase-shift control action, α adopts new values as the whole range of loads is swept. Figure 11 shows that α converges to 90° as R increases, regardless of g_x. This increase in α with R makes the rms voltage at the inverter output drop in order to keep the primary current controlled for every load, as follows from (7) and (11). In practice, after a new load was connected, α was adjusted manually from the dSPACE platform until the monitored $I_{P\text{rms}}$ was as close as possible to 10 A.

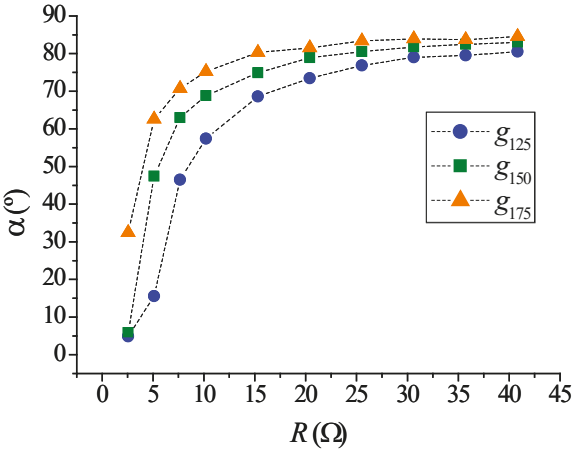

Figure 11. Convergence of α with *R*.

As a consequence of this gradual convergence process, the rate at which α changes has a non-linear dependence with *R*: a given increment in *R* makes α undergo a significant increase in the area of small loads; however, the same increment causes only a moderate increase in α for large loads. Although this holds for the three g_x, the effect becomes more pronounced as the air gap increases. Note that the cosine function in (10) accounts for the non-linear behavior observed.

The deviations from the experimental *k* factors, expressed in coupling factor units (CFU), are plotted in Figure 12 in the form of absolute errors. They reach a maximum of 7×10^{-3} CFU with the exception of the two cases mentioned previously, in which they grow remarkably larger. Overall, the area of low *R* (up to 10 Ω) behaves best, as the deviations are 3×10^{-3} CFU or less for the three g_x. It should be noted that the absolute errors found for g_{125} are the smallest for the ten loads, ranging from 1×10^{-3} to 4×10^{-3} CFU with the exception, once again, of the two largest load resistances.

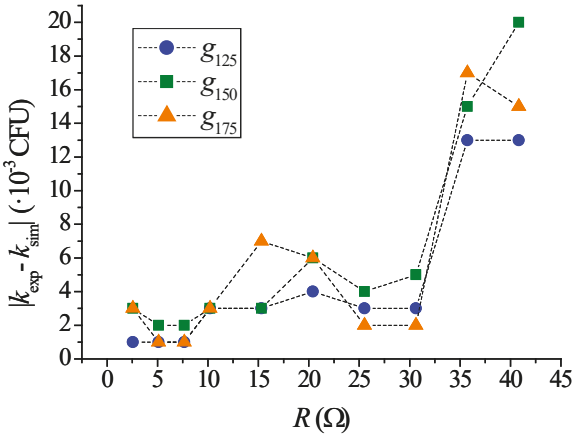

Figure 12. Absolute errors obtained in the determination of *k* with the circuit model.

The accuracy of every single model parameter contributes to the reliability of the circuit model, even in the case of those parameters that, in principle, play a minor role. This is the case of R_{on}: if, for a given g_x and *R*, R_{on} decreases from its actual value of 48 mΩ to 1 mΩ (that is, the inverter switches are

modeled as virtually ideal devices), the primary peak current increases according to (7), which in some cases alters the k obtained with the circuit model. Taking for example g_{150}, the increase in the primary current caused by that drop in R_{on} does not suffice to modify k for R = 2.5 Ω. However, in the case of R = 40 Ω, k undergoes an increase of 2×10^{-3} CFU, which would add to the corresponding absolute error, making the deviation from the experimental k even larger.

As stated previously, an increase in R translates into small increases in α in the area of high loads. This has important implications with regard to the sensitivity of the system and its capability to accurately determine k, since a small change in α when the prototype is loaded with a large R leads to significant variations in the peak primary current. It is, therefore, of interest to test the model response under small variations in α that may occur owing to a measurement error, as α results from time measurements of the experimental waveforms of the inverter output voltage.

Assuming that α was obtained with an error of ±0.25°, and plotting k against R for g_{125} for illustration purposes, it is apparent that k undergoes an increasingly larger shift from the k factors obtained with α as R increases. As can be seen in Figure 13, the error has little or no influence on k within the low load range. However, from 10 Ω onward, the shifts grow larger and larger both above and below the initial k values, reaching a maximum of 4×10^{-3} CFU for 40 Ω (k = 0.250 for α+0.25° and k = 0.258 for α−0.25°). If a small measurement error in the determination of α is taken into account, the capability of the system to deliver reliable figures for k consequently worsens as R increases. This may contribute to justifying the deviations found in the determination of k for the two largest loads.

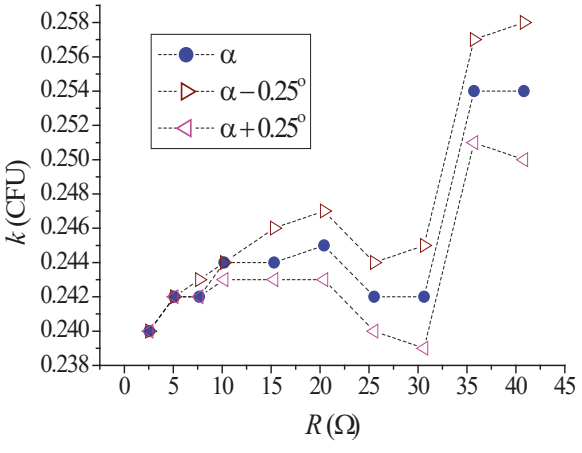

Figure 13. Influence on k of a ±0.25° error in the determination of α for g_{125}.

7. Waveform Analysis

Both experimental and simulated waveforms are shown in Figure 14 for comparison purposes. The inverter output voltages and currents are represented by blue and pink lines, respectively. A selection of three representative cases was chosen (specifically, those corresponding to 2.5, 10 and 40 Ω for the intermediate air gap g_{150}). Note that the duty cycle of the inverter output voltage is very low for 40 Ω, one of the two cases in which the circuit model behaves worst.

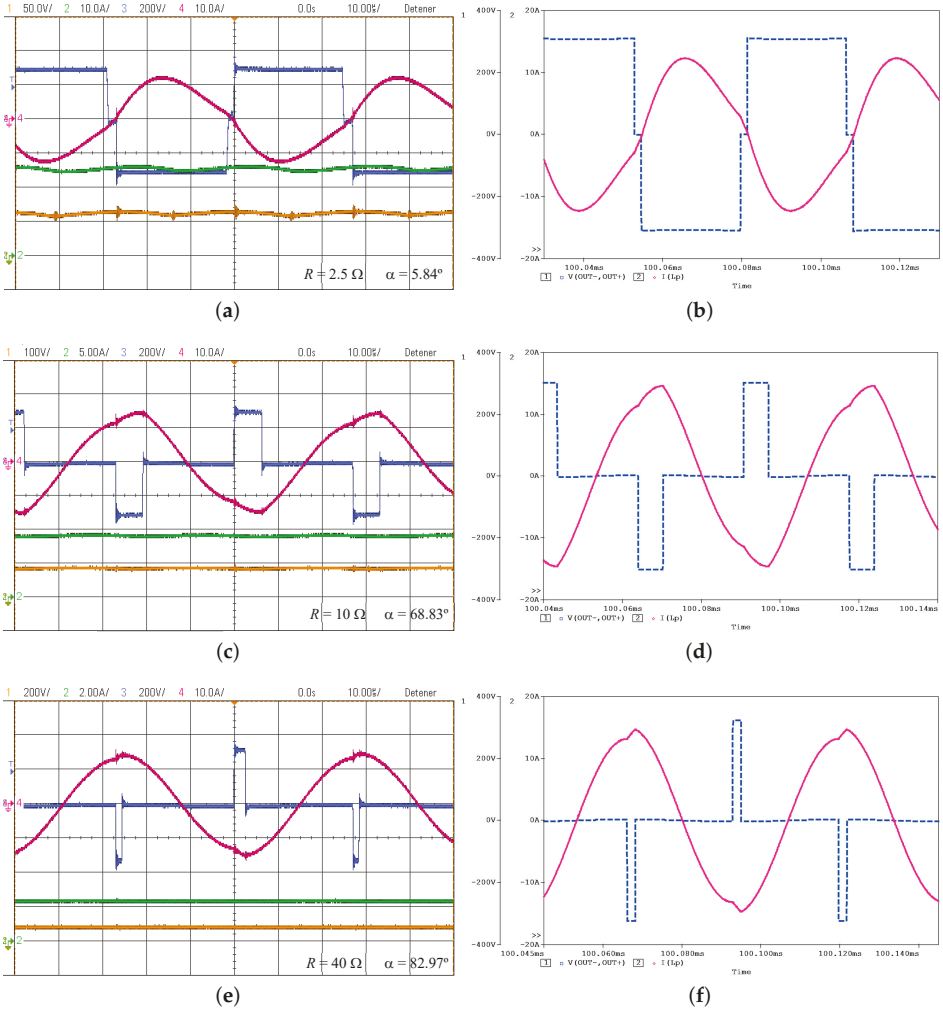

Figure 14. Selected inverter output voltage and current waveforms for g_{150}. (**a**,**c**,**e**) experimental prototype; (**b**,**d**,**f**) PSpice simulation.

A comparison of the shapes and amplitudes of the two sets of waveforms makes it possible to conclude that the simulated waveforms are very similar to their experimental counterparts. Moreover, the shape of the current waveforms is quite sinusoidal in all cases, which confirms the validity of the FHA approximation adopted before analyzing the equivalent circuit of the IPT prototype. The low harmonic content of the primary current waveforms can be understood in terms of the band-pass filtering process introduced by the resonant circuit on the primary side of the coupling. Alternatively, it can be regarded as a consequence of dealing with loosely coupled coils, which are characterized by a low k. Recall that leakage inductances are, according to (2) and (3), relatively large in the circuit model of a weak inductive coupling: a large leakage inductance effectively filters out most of the harmonic content of the current waveform, leading to the observed sinusoidal-like waveforms. Furthermore, the larger the air gap is, the larger the leakage inductance becomes, and more frequencies are consequently rejected from the spectrum of the current waveform. This effect is illustrated in

Figure 15, which represents the total harmonic distortion (THD) versus R. As can be seen, the harmonic content decreases as g_x increases, which is easier to verify for those loads in which α is similar for the three g_x (all of them, with the exception of the three smaller ones). In the case of small loads (up to 10 Ω), the plot does not show the effect clearly since, for a given load, the corresponding three angles α are quite different depending on g_x. Finally, it should be pointed out that no correlation was found between the harmonic content and the deviations in k depicted in Figure 12. In fact, the THD is especially low for the two largest loads, for which the model behaves worst. It is not, therefore, possible to claim that the two estimates of k with the largest absolute errors occur as a consequence of a high harmonic content in the corresponding current waveforms.

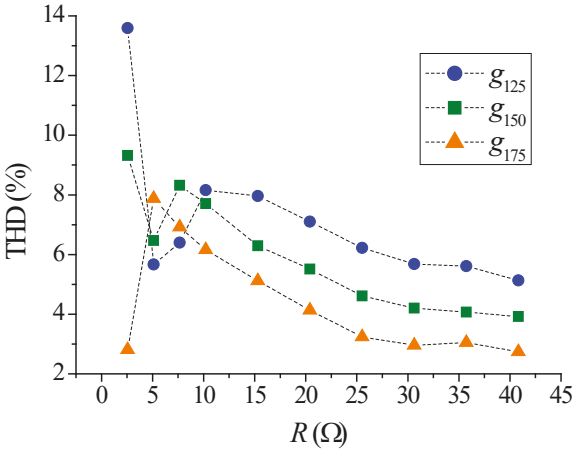

Figure 15. THD versus R.

8. Conclusions

A PSpice circuit model, developed as a replica of a 2-kW IPT charger operating at 18.65 kHz and controlled with the phase-shift technique, has been tested and validated for three air gaps of practical interest in the case of light-duty EVs: 125, 150 and 175 mm. The validation procedure was based on determining the existing deviations between the coupling factors obtained experimentally for every air gap and those delivered by the simulation model for a set of ten load resistances, ranging from 2.5 Ω to 40 Ω. The results show that the deviations are within reasonable limits (below 7×10^{-3} CFU) for the three air gaps and all the loads tested with the exception of the two largest, for which the duty cycle of the inverter output voltage is especially low and accuracy is, therefore, compromised. The best agreement was found in the lower range of load resistances (up to 10 Ω), in which deviations lie between 1×10^{-3} CFU and 3×10^{-3} CFU. Consequently, the overall performance of the simulation model is satisfactory, although there is evidence of a certain threshold level for the load resistance (or, equivalently, for the zero-voltage angle α) above which the reliability of the simulation model declines. Setting the threshold at the nominal resistance of 35 Ω, the corresponding α angles are 79.54°, 82.46° and 83.68° for the air gaps of 125, 150 and 175 mm, respectively. Since one of the six input parameters of the circuit model is the switching frequency, the PSpice circuit developed can be readily adapted to simulate the behavior of prototypes that comply with the SAE-J2954 standard issued for EV wireless charging, which establishes a nominal switching frequency of 85 kHz.

Author Contributions: Conceptualization, J.V. Data curation, J.V., P.R. and A.P. Formal analysis, J.V. Funding acquisition, P.R. Investigation, J.V., P.R. and A.P. Methodology, J.V. Project administration, P.R. Software, J.V. and P.R. Supervision, P.R. Validation, J.V. and P.R. Writing, original draft, J.V. Writing, review and editing, P.R. and A.P.

Funding: This work has been supported by the Ministry of Economy and Competitiveness of Spain, and by the European Regional Development Fund under the research project ENE2015-71417-R (MINECO/FEDER, UE).

Acknowledgments: The authors thank the anonymous referees for their valuable suggestions and comments, which have led to the present amended version of the original manuscript.

Conflicts of Interest: The authors declare no conflict of interest. The founding sponsors had no role in the design of the study; in the collection, analyses or interpretation of data; in the writing of the manuscript; nor in the decision to publish the results.

Abbreviations

The following abbreviations are used in this manuscript:

CFU	Coupling factor unit
EV	Electric vehicle
FHA	Fundamental harmonic approximation
IC	Integrated circuit
ICPT	Inductively-coupled power transfer
IGBT	Insulated-gate bipolar junction transistor
IPT	Inductive power transfer
PCB	Printed circuit board
PWM	Pulse-width modulation
RIPT	Resonant inductive power transfer
SOC	State of charge
SS	Series-series
THD	Total harmonic distortion
VSC	Voltage-source converter
WPT	Wireless power transfer

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Correction

Correction: Vázquez, J. et al. Simulation Model of a 2-kW IPT Charger with Phase-Shift Control: Validation through the Tuning of the Coupling Factor. *Electronics* 2018, 7, 255

Javier Vázquez [1,*], Pedro Roncero-Sánchez [1] and Alfonso Parreño Torres [2]

[1] Institute of Energy Research and Industrial Applications, University of Castilla-La Mancha, Campus Universitario S/N, 13071 Ciudad Real, Spain; Pedro.Roncero@uclm.es
[2] Institute of Industrial Development, Castilla-La Mancha Science and Technology Park, Paseo de la Innovación 1, 02006 Albacete, Spain; Alfonso.Parreno@pctclm.com
* Correspondence: Javier.Vazquez@uclm.es

Received: 28 November 2018; Accepted: 30 November 2018; Published: 3 December 2018

The authors wish to make the following correction to our published paper [1].

There is a misprint in Equation (3) of the published paper, which expresses the leakage inductance on the secondary side, denoted by L_{Sk}, in terms of the secondary self-inductance L_S, the mutual inductance M and the turns ratio r. The term r/M is incorrect and should be replaced with M/r.

In summary, on page 4, Equation (3) should be changed from

$$L_{Sk} = (1-k)\,L_S = L_S - \frac{r}{M} \tag{1}$$

to the following correct version:

$$L_{Sk} = (1-k)\,L_S = L_S - \frac{M}{r} \tag{2}$$

The authors would like to apologize for any inconvenience caused to the readers by these changes. The change does not affect the scientific results. The manuscript will be updated and the original will remain online on the article webpage, with a reference to this Correction.

References

1. Vázquez, J.; Roncero-Sánchez, P.; Torres, A.P. Simulation Model of a 2-kW IPT Charger with Phase-Shift Control: Validation through the Tuning of the Coupling Factor. *Electronics* **2018**, *7*, 255. [CrossRef]

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Review

Magnetically Coupled Resonance WPT: Review of Compensation Topologies, Resonator Structures with Misalignment, and EMI Diagnostics

Mohamad Abou Houran, Xu Yang and Wenjie Chen *

School of Electrical Engineering, Xi'an Jiaotong University, Xi'an 710049, China;
eng.horan@yahoo.com (M.A.H.); yangxu@xjtu.edu.cn (X.Y.)
* Correspondence: cwj@xjtu.edu.cn; Tel.: +86-29-82665223

Received: 11 September 2018; Accepted: 22 October 2018; Published: 2 November 2018

Abstract: Magnetically coupled resonance wireless power transfer systems (MCR WPT) have been developed in recent years. There are several key benefits of such systems, including dispensing with power cords, being able to charge multiple devices simultaneously, and having a wide power range. Hence, WPT systems have been used to supply the power for many applications, such as electric vehicles (EVs), implantable medical devices (IMDs), consumer electronics, etc. The literature has reported numerous topologies, many structures with misalignment effects, and various standards related to WPT systems; they are usually confusing and difficult to follow. To provide a clearer picture, this paper aims to provide comprehensive classifications for the recent contributions to the current state of MCR WPT. This paper sets a benchmark in order to provide a deep comparison between different WPT systems according to different criteria: (1) compensation topologies; (2) resonator structures with misalignment effects; and, (3) electromagnetic field (EMF) diagnostics and electromagnetic field interference (EMI), including the WPT-related standards and EMI and EMF reduction methods. Finally, WPT systems are arranged according to the application type. In addition, a WPT case study is proposed, an algorithm design is given, and experiments are conducted to validate the results obtained by simulations.

Keywords: compensation topology; electromagnetic field (EMF); electromagnetic field interference (EMI); misalignment; resonator structure; wireless power transfer (WPT); WPT standards

1. Introduction

Wireless power transfer (WPT) is a promising technology due to its advantages of being cordless, safe during charging, and its ability to operate in a wet and harsh environment [1]. It has gained global acceptance, and is used to supply the power for many applications in several fields, such as electric vehicles (EVs) [2–14], online electric vehicles (OLEVs) [15–17], plug-in hybrid electric vehicle (PHEVs) [18], superconducting magnetic levitation trains (maglev) [19], implantable medical devices (IMDs) [20–31], and consumer electronics [32–34]. In addition, it has been used in the charging systems of autonomous underwater vehicles (AUVs) [35], the rotary of a gas turbine [36], and Internet of Things (IoT) applications [37–39].

According to the energy transfer mechanism, the WPT technology can be divided into two categories. The first is far-field wireless transmission, which is also called electromagnetic radiation WPT. It includes microwave power transfer (MPT) [40–42], laser power transfer (LPT) [43–45], and solar power satellites (SPS) [46,47].

The second is near-field WPT (Figure 1), which can, in turn, be classified into two groups. Firstly, there is inductive power transfer, including the inductive coupled power transfer (ICPT or IPT), and magnetically coupled resonance wireless power transfer (MCR WPT); as shown in Figure 1a, Tx is

the transmitting coil and *Rx* is the receiving coil. Secondly, there is capacitive power transfer (CPT), as displayed in Figure 1b. Some IPT systems have presented high power transmission efficiency (PTE) of larger than 90% for transmission distances of several centimeters; however, for longer distances, efficiency will drop significantly [48–63]. Nevertheless, authors have presented an innovative IPT system to transfer power a distance of 5 m using dipole coils [64]. Most of the presented CPT systems are designed for low-power applications, including USB devices, lamps, and small robots [8,65–73], where the transmitting distance is limited to the millimeter range. High efficiency is provided by MCR WPT for a longer transferring distance [23,34,74–82].

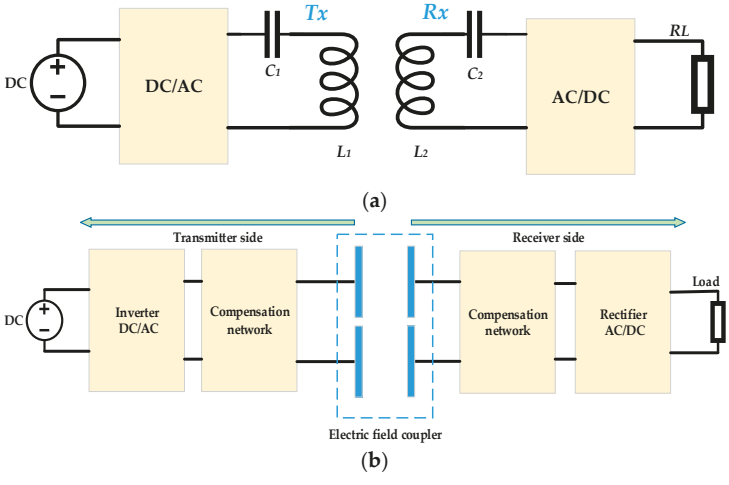


Figure 1. Near-field wireless power transfer (WPT): (**a**) Structure of inductive power transfer (IPT)/magnetically coupled wireless power transfer (MCR WPT); (**b**) Structure of capacitive power transfer (CPT).

Due to its importance and rapid development, WPT has been widely used over the last few years, offering a practical technique to transfer power wirelessly in many applications on a commercial scale. Many studies have been conducted in this area, and the literature has reported much research related to several aspects of MCR WPT, which is usually confusing and difficult to follow. To give a clear picture, this paper aims to review the recent contributions to the current state of MCR WPT systems. This paper sets a benchmark in order to provide comprehensive classifications with a deep comparison between different WPT systems according to different criteria. They are as follows:

1. Compensation topologies: Basic and hybrid compensation topologies are reported, and some commonly used topologies are compared based on application type.
2. Research work related to the resonator structure is discussed as follows:

    - Coil geometry is discussed in detail, including many resonator shapes, such as planar coils, three-dimensional (3D) structures, cavity structures, and coils with cores, etc., which are compared based on set criteria.
    - The differences between single-phase WPT and three-phase WPT systems are highlighted, and some three-phase WPT projects are reported.
    - Multi-coil systems, which are capable of charging multiple devices simultaneously, such as LEDs, are addressed.
    - Operating frequency effects on the design of coil structure.
    - Inductance of several resonator structures.

- Misalignment study: Several misalignment types are displayed and compared based on their resonator structure and effects, in addition to their advantages and disadvantages.

3. Electromagnetic field interference (EMI) diagnostics, including WPT-related standards and guidelines. In addition, EMI and EMF reduction methods are reported and compared. Moreover, advantages and disadvantages of these methods are addressed.
4. Basic applications of WPT systems are given. Next, a WPT case study is proposed. In the proposed winding method, a bio-inspired joint made of two spherical structures is given. The algorithm design is provided, and experiments are conducted to validate the obtained results by simulation and optimization.

The paper is organized as follows. In Section 2, a benchmark is set to present the major categorizations of the WPT system. Section 3 discusses compensation topologies in detail. Section 4 classifies and reviews many resonator structures in detail. The misalignment study is presented in Section 5. WPT-related standards, electromagnetic field (EMF) mitigation methods, and EMI mitigation methods are given in Section 6. In Section 7, WPT applications are illustrated, an optimized design of a WPT system is given, and a case study is proposed and discussed. Finally, the conclusion and further areas for research are provided in Section 8.

2. Benchmark of the Research Work

In this paper, a benchmark is proposed (Figure 2) that provides various categorizations of research works related to WPT. The benchmark classifies major research areas relating to WPT, which include compensation topology, resonator structure, misalignment study, EMI and EMF diagnostics, frequency-splitting issue, impedance matching, control strategy, and WPT optimization. In this paper, a number of these issues related to WPT systems are discussed in detail. Other issues, such as impedance matching (which will be discussed in brief in Section 3) and control methods [83,84], will not be discussed for the sake of brevity.

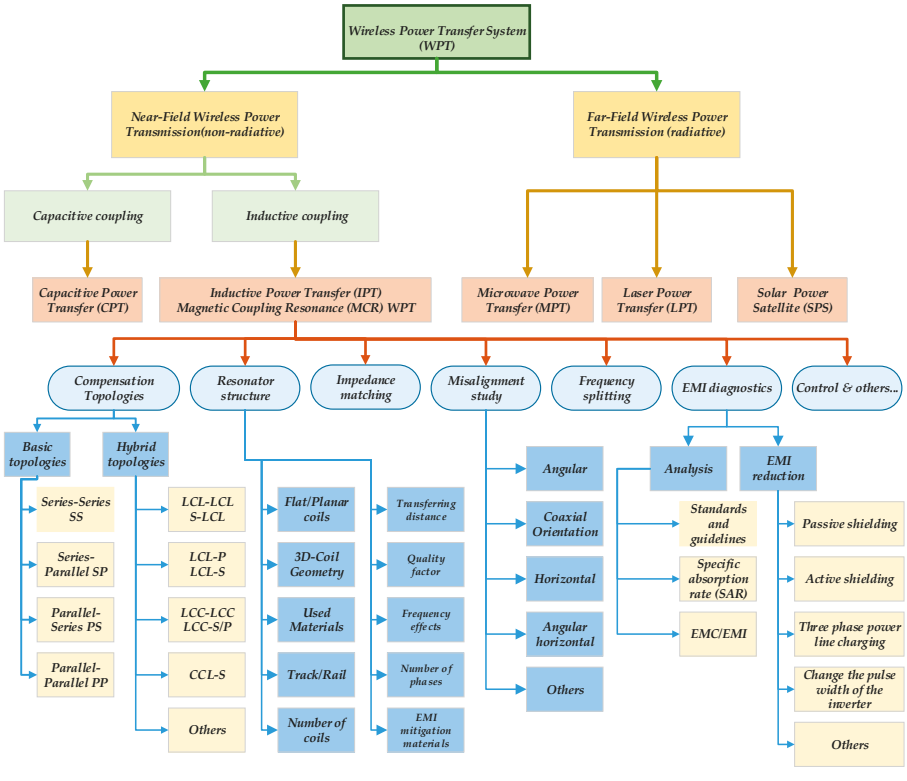


Figure 2. WPT classifications and major research areas.

3. Compensation Topologies

There are some requirements for compensation, which are as follows. (1) The compensation capacitor resonates with the primary and/or secondary inductance in order to provide reactive power, which is required for the inductances to generate an adequate magnetic field. Therefore, the basic function for the compensation of a primary coil is to minimize the volt-ampere (VA) rating of the power supply. In the secondary coil, compensation cancels the inductance to maximize the power transfer capability [85]. (2) Constant-voltage/constant-current output (CVO/CCO). (3) The maximum efficiency of a WPT system can be determined by two parameters, the coupling coefficient and quality factor [54]. (4) Bifurcation resistance, which refers to a condition where the frequency realizes a zero phase angle (ZPA) [57,85].

3.1. Basic and Hybrid Compensation Topologies

Figure 3 shows the classifications of the compensation topology. They include two groups. The first is of the four basic topologies, and the second comprises hybrid topologies, which are combinations of series and parallel topologies.

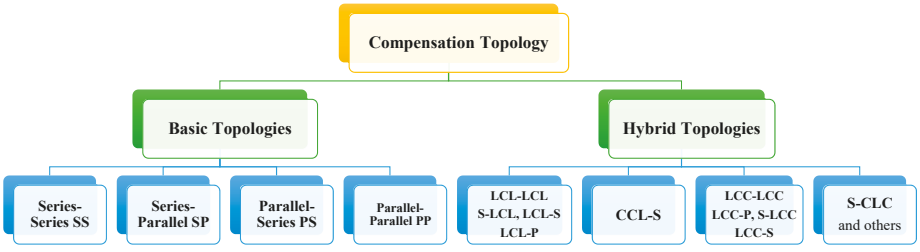


Figure 3. Classifications of the compensation topology.

Many compensation topologies have been reported. As illustrated in Figure 4, there are four basic compensation topologies: series-series (SS) [3,86–90], series-parallel (SP) [91], parallel-series (PS) [1], and parallel-parallel (PP) [92]. In Figure 4, k is the coupling coefficient, M is the mutual inductance, U_g is the input voltage on the primary side, U_2 is the load voltage, and R_L is the load. L_1, L_2, C_1, and C_2 are the self-inductances and external compensation capacitors of the primary and secondary coils, respectively. R_1 and R_2 are the resistances of the primary and secondary coils, respectively. On the other hand, hybrid compensation topologies are investigated, such as LCC-P and LCL-P are reported in [93], where LCC and LCL are on the transmitting side, and parallel (P) is on the receiving side. Moreover, S-CLC [94], CCL-S [95], LCL-S [96], and LCC-LCC [18,97–99] are discussed. Double-sided LCC-compensated WPT (multi-LCC on the transmitter side) is presented in [100], and LCL-LCL is given in [101]. Some commonly used hybrid topologies in the research work are displayed in Figure 5. L_p and L_S are the primary and secondary inductances, respectively.

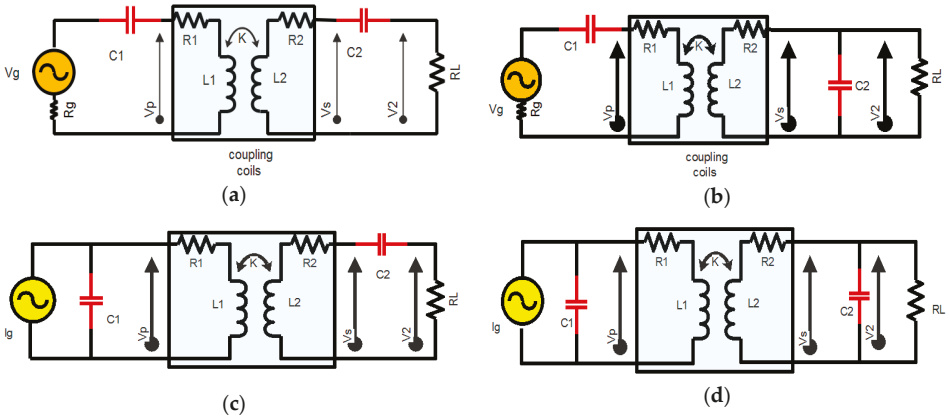


Figure 4. The basic topologies: (**a**) Series-Series (SS); (**b**) Series-Parallel (SP); (**c**) Parallel-Series (PS); (**d**) Parallel-Parallel (PP).

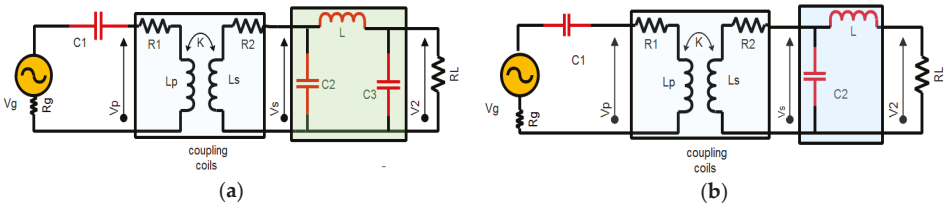


Figure 5. *Cont.*

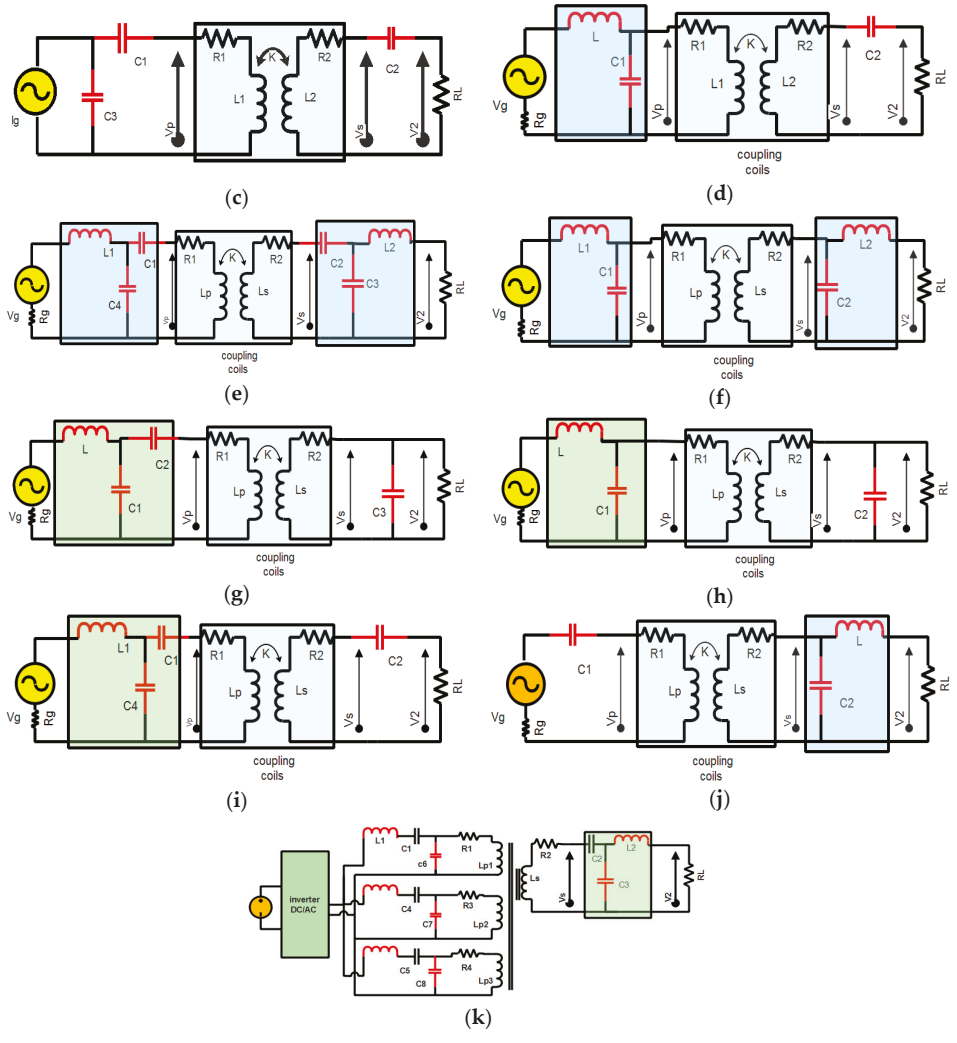


Figure 5. Hybrid compensation topologies: (**a**) S-CLC; (**b**) S-LCL; (**c**) CCL-S; (**d**) LCL-S; (**e**) LCC-LCC; (**f**) LCL-LCL; (**g**) LCC-P; (**h**) LCL-P; (**i**) LCC-S; (**j**) S-LCL; (**k**) Double-Sided LCC.

3.2. Review of Different WPT Systems Based on Topology and Application Type

Table 1 gives a comparison between different WPT systems based on the compensation topologies and application type (electric vehicles). The systems are easily compared considering some criteria, such as transferred power, frequency, resonators' dimensions, and transferring distance. In this table, f_0 is the resonant frequency, k is the coupling coefficient, and R_L is the load value. In addition, N_1 and N_2 are the number of turns for primary coils and secondary coils, respectively. D_1 and D_2 are the length (or diameter) and width (or diameter) of the transmitter and receiver coils, respectively. Finally, P_{out} is the output power and V_{out} is the output voltage. Table 2 reviews the WPT systems that are used in dynamic charging for EVs application.

Table 1. Review of different WPT systems based on topology and application type (such as electric vehicles, or EVs). EMI: electromagnetic field interference.

Reference and Topology	$f_0/k/R_L$ (kHz, Ω)	P_{out}, V_{out}	Efficiency	Resonators				Note
				N_1 Turn N_2 Turn	D_1 mm Length, Diameter mm	D_2 mm width, Diameter mm	Gap mm	
[14] SS/LCC-LCC	$f_0 = 85$ $k = 0.135$ $R_L = 2, 3, 5$	1 kW 50 V	95% for SS, and 93% for LCC	10 8	500 diameter	400 diameter	200	Based on EMI, LCC-LCC topology is considered more robust to EMI exposure.
[89] SS/LCC-LCC	$f_0 = 79$	7.7 kW max. 270~405 V	For LCC: 96%	-	800	600	200	The LCC-LCC topology has higher efficiency when the mutual inductance is at minimum.
[101] SS/LCL-LCL	$f_0 = 85$ $k = 0.1$ $R_L = 10$	3.3 kW	93.1% for SS, 89.5% for LCC	20 × 3 layers 17 × 2 layers	550 × 400 mm^2	240 × 240 mm^2	100	Compared to SS topology, the LCL-LCL type has a high power factor.
[98] LCC-LCC	$f_0 = 79$ $k = 0.18$~0.32 $R_L = 10$~200	7.5 kW 450 V	96%	1	800	600	200	Resonant frequency f_0 is independent of the coupling coefficient and load conditions.
[99] LCC-LCC	$f_0 = 95$ $k = 0.14$–0.30	5.6 kW 300~450 V	95.36%	-	600 200	600 200	150	The extra integration-induced couplings give more space for magnetic cores.
[87] LCC-LCC	$f_0 = 85$ $k = 0.153$ $R_L = 49.95$	3.3 kW 405.7 V	92.6%	18 16	600	300	150	Energy storage has no relation to topology type, but only with transferred power level and coupling coefficient.
[97] LCC-LCC	$f_0 = 85$ $k = 0.1877$	3 kW 300 V	95.5%	-	600 × 450 × 4 mm^3 640 × 496 × 8 mm^3 711.2 × 558.8 × 2 mm^3	400 × 300 × 4 mm^3 480 × 352 × 8 mm^3 508 × 406 × 2 mm^3	150	The compensated resonator design helps to eliminate or reduce the extra-coupling effects to a tiny level.

Table 2. Review of WPT systems that are used in dynamic charging for EVs and plug-in hybrid electric vehicles (PHEVs).

Reference and Topology	$f_0/k/R_L$ (kHz, Ω)	P_{out}, V_{out}	Efficiency	Coils' Dimensions and Number of Turns	Gap mm	Note
[96] LCL-S LCC-S	f_0 = 140 k = 0.18–0.32	Nominal power: 1 kW 80~90 V	Similar: LCC and LCL: 93%	Coil radius is 163 mm	100	The topology gives more robust power transfer character against the variation of k.
[100] Double-sided LCC	f_0 = 85 k = 0.13	1.4 kW 150 V	89.78%	9 turns for each transmitter, *Tx* coil 6× (388 mm×400 mm), and for *Rx*: 485 mm×400 mm	150	This paper presented a continuous dynamic WPT system, which reduces the power pulsations.
[102] LCL	f_0 = 85 k = 3.7–5.4%	5 kW	-	The secondary: 0.35 m × 0.7 m N87 ferrite material (each 93 mm × 28 mm × 16 mm).	240	The system is designed to supply power along the whole length of the track by activating only one primary pad.
[103] SS	f_0 = 85 k = 0.4	20 kW	80%	Transmitter dimensions are 10 cm × 75 cm, number of turns: nine Receiver: 25 cm × 20 cm, number of turns: 12.	100	Downscale prototype operating at 85 kHz ± 2.5 kHz.
[104] SP	f_0 = 23 R_L = 2	2 kW	-	Coils diameter: 330 mm. Turns: seven turns for transmitter coil and five turns for receiver coil.	100	This paper presented technical aspects of in-motion WPTs for charging EVs and PHEVs.
[105] SS	f_0 = 85	-	97.6% pads length ratio is 1:1	Coil external width: 58 mm Coil inner width 38 Wire diameter 5 mm Number of turns: 8 turns.	200	Investigated the pad shape: influence of the variation of the ratio between *Tx* and *Rx* lengths with respect to the behavior of the coupling.

In PS-compensated WPT, the reactive current of the current-fed resonating converter circulates inside the parallel resonant tank without going through the switching system. Therefore, the current rating of the switching devices is reduced, and the conduction loss is reduced for a given power level. This topology has a high voltage stress on the inverter switches, especially for high power loads, and it becomes worse when the coupling coefficient is low. CCL-S is an example of hybrid topologies; as shown in Figure 5c, it has an extra series capacitor on the primary side, which leads to a lower switching loss compared to the parallel LC-S. Parallel LC-compensated WPT is preferred for low voltage gain applications. However, for higher voltage gain, CCL is preferred. S-CLC topology, which is shown in Figure 5a, provides an easier achievement of ZPA. In Figure 5k, the double-sided LCC-compensated topology was illustrated, and a continuous dynamic WPT charging system was introduced.

The output current and output voltage of SS, S-LCL, S-CLC, and SP compensation topologies are inversely proportional to the mutual inductance, and the output power is inversely proportional to the square of the mutual inductance. Regarding double-sided LCL, as well as double-sided LCC, LCL-S, LCL-P, PS, and PP compensation topologies, the output current and output voltage are proportional to the mutual inductance, and the output power is proportional to the square of the mutual inductance. Based on that, the design method of these topologies can be determined. Consider two cases. The first is an SS-compensated WPT system, which is designed to transfer a nominal power at the maximum mutual inductance, and means perfectly aligned coils. At the maximum mutual inductance, the input voltage and efficiency of the SS topology will be higher, and the current will be lower. The second is an LCC-compensated WPT system, which is designed at the minimum mutual inductance, and means a maximum misalignment between resonators.

Finally, at high-frequency circuits, there arises an impedance matching problem, where the circuit components gain a non-resistive aspect. To achieve maximum power transfer efficiency, the circuit must be impedance matched to minimize these effects [106,107]. Some impedance-matching methods were proposed, such as employing the impedance inverter only at the receiver side [108], and using a dual-band resistance compression network (RCN) as a matching network [109].

4. The Resonator Structure

Figure 6 shows the research work related to the resonator structure (geometry) including several categories, such as planar coil, 3D structures, tracks/rail, coils with cores, and the type of used materials, etc. In addition, the suitable application type for each structure is given, and the frequency ranges for some of these geometries are provided.

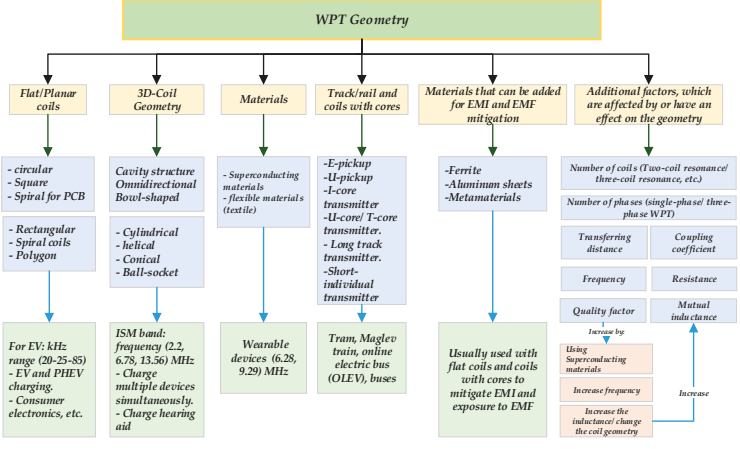


Figure 6. Classifications of resonator structure.

4.1. Shape of the Resonator

Different studies have been investigated based on the shape of resonators. They are classified as follows:

- Flat/planar-shaped coils, such as rectangular-shaped structure [89,98,110,111], octagonal resonator [101], and a double D coil (DD) [112]. In addition, defected ground structure (DGS) is presented in [113,114]. DGS means a "defect" has been integrated on the ground plane of a microwave planar circuit; this DGS technique is adopted to improve various parameters of a microwave circuit, such as low gain and narrow bandwidth [115]. Moreover, circular coils [116,117] and square coils [99,118,119] are discussed. There are planar printed spiral coils (PSC) [120–123] as well, the WPT system in the printed circuit board (PCB) [124–127], pancake coils [128], and planar shielded-loop resonators [129].
- Three-dimensional (3D) geometries are investigated, such as for instance, bowl-shaped transmitter coils [28], which are used for charging hearing aids, cylindrical coils [80], helix loop resonators [130–133], and conical coils [134]. In [135,136], the three-dimensional resonant cavity is presented, which offers a good way of charging multiple devices simultaneously. An orthogonal winding is discussed in [137], and a cylindrical cavity is given in [138]. In [139–142], the authors proposed an omnidirectional WPT system, and in [143], the authors discussed a ball joint structure.
- Coils' materials are discussed, for example, a receiver coil made of aluminum is used in [125]. In [144], the authors proposed a helical-type coil made of superconductors in order to increase the quality factor of the coils. In [145], the authors applied an MCR WPT system (planar textile resonators, or PTRs) to wearable consumer electronics by using flexible materials.
- Coils with cores are given, such as dipole-type coils [64], which presented a WPT prototype that is capable of transferring the power up to a 5-m distance. For charging vehicles, buses, trams, and trains, long-track transmitter and short-individual tracks are used [16,17,90]. Moreover, E-core and U-core types are discussed [94,146].

Other structures were presented, for example, multiple-input multiple-output structures (MIMO) [147,148], a wirelessly powered cage system [149], transparent electrode resonators [150], domino-resonator systems [151–153], and dual-layer nested structures [154]. Moreover, the three-phase system [16,35,155] found its way to the wireless charging technology through some real applications. Finally, an L-shape transmitter was discussed in [156].

Most of the resonators are coreless, which means no iron losses (hysteresis loss, eddy current). However, the quality factor, and thus the efficiency, will be low. To overcome this problem, there are three options. The first is increasing the mutual inductance by changing the geometry or increasing the number of turns and adding ferrites. However, in some cases, ferrite cannot be added due to cost and space limitations. The second is increasing the frequency, but it could be limited by the switching speed of the semiconductors, and it might cause more switching losses. The third is using multi-transmitter WPT systems, but resonant inverters with different power rates are required.

Table 3 presents projects related to the defected ground structure (DGS). The defected ground structure (DGS) can operate at high frequencies, for example, the spiral-strips DGS operates at 50 MHz, which provides a high-quality factor and introduces a structure that mitigates the problem of a low self-inductance that is given by H-shaped DGS. Compared to H-shaped DGS, the semi-H-shaped DGS shows a better efficiency and greater transferring distance even if they have the same size. In Table 4, the three-dimensional resonant structures are reported and compared. Cylindrical, helical, and cavity structures are used to provide power for some applications, such as hearing aids, LEDs, and toys.

Table 5 displays studies related to flat structure, in which the power transferring distance is almost twice the radius/width of the coil, and the power range is within several watts to several dozen watts of power. Table 6 gives two cases of WPT systems using coils with cores. Several core types are used, especially in EV charging applications. Table 7 reports research works on domino resonator systems for low-power applications.

Table 3. Research works related to defected ground structure (DGS).

WPT System	Resonator Parameters						f_0/k	Efficiency	Note
	Resonator Structure	Size of the Coils/Number of the Coils	N_1/N_2 Ratio	D_1 mm	D_2 mm	Gap mm			
[113]	H-shaped DGS Semi-H-shaped DGS	Symmetrical, two-coil resonance structure	1	20 21	20 21	13 25	300 kHz/k = 0.025	68%/73%	Semi H-shaped DGS resonator is more robust to the coaxial orientation misalignment.
[114]	Spiral-strips DGS	Symmetrical Asymmetrical	1	50 × 50 mm^2 50 × 50 mm^2	50 × 50 mm^2 50 × 30 mm^2	50 40	50 MHz	84%/78%	Spiral-strips DGS provides a better quality factor other than H-shaped or semi-H-shaped DGS.

Table 4. Research work related to three-dimensional (3D) structure.

WPT System	Resonators				f_0, R_L P_{out}, V_{out}, Efficiency %	Note
	Resonator Structure	Size of the Coils/Number of Coils	Coils' Dimensions and Number of Turns	Gap		
[80]	Structures: cylindrical for *Tx*, *Rx1*, and planar rectangular for *Rx2*.	Asymmetrical/four-coil resonator structure	The diameter of *Tx* is 350 mm, the thickness is 0.35 mm, and the width is 29 mm besides a one-turn driving coil. The radius of *Rx1*: 80 mm, the height: 50 mm, besides a seven-turn coil that was used as the output coil. The area of *Rx2* is 20.5 × 20 mm^2, and the thickness is 0.35 mm.	150 mm *Tx1* 200 mm *Tx2*	7 MHz LED loads 80%	*Tx* is simply printed on the internal or external cover, or inserted in the clothes.
[132]	Helical coils	Symmetrical/three-c resonator structure	The radius is 0.325 m, the pitch is 0.05 m, and the number of turns is N = 5, d_{12} = 6 m	2–4 m	10 MHz 90%	Compared with a single-transmitter WPT system, a higher power transfer efficiency (PTE) was achieved stably for the angular aligned and the angular misaligned.
[29]	3D structure/Bowl-shaj transmitter coil and spiral helical receiver coils	Asymmetrical/three resonator structure	The *Tx* bowl-shaped, which is a combination of both a spiral coil (s) and a conical-shaped coil (c) with a big diameter of 58 mm, a thickness of 9.1 mm, and turns: *NS* = *Nc* = 7 turns. The volume of the receiver coils Rx (spiral s1+ helical h) is 10.5 × 6.5 × 2.46 mm^3 with *Ns*1 = *Nh* = 8 turns	Within 3D cavity	6.78 MHz 2.5 to 4.3 V 60%	The proposed system can uniformly charge a pouch-type LIB of a hearing aid in spite of its position or arrangement.
3D structure: WPT systems operating at higher frequencies:						
[131]	3D structure/Helical coils	Symmetrical/systen with Relay resonator	Symmetrical relay resonator with multi load transfer and number of turns is 12	-	193 MHz 0.1~2.0 Ω Several dozen watts of power, 30~40%	The WPT system transfers the same power to multiple loads over a range of distances.
[136]	The *Tx* is a cavity resonator and the *Rx* is a square coil	Asymmetrical/mult structure	The dimensions of the cavity resonator are a = 1.52 m, b = 1.42 m, and d = 1.83 m. *Rx* square coil has one turn 7.62 cm. (multi receivers)	91 cm	191.65 MHz 50-Ω 8-W LED 50%	The system is able to deliver power to many devices simultaneously, such as LEDs and toys in a box.
[138]	3D structure/Cylindric cavity resonator	Asymmetrical/two- structure	The radius of the *Tx* coil is 30 cm, and the height is 25.4 cm; the volume of the cavity is 0.072 m^3. The radius of *Rx* is 2.5 mm, and the volume of the receiver coil is 13.75 mm^3.	10 cm	375.32 MHz 50 Ω 33%	PTE of the optimal impedance-matching (IM) system can achieve 33.88%, which is four times the 7.68% that can be achieved without an optimal IM system.

Table 5. Research work related to flat structures for low-power applications.

WPT System	Resonator Parameters				$f_0/k/R_L$	P_{out}, Efficiency %	Note
	Resonator Structure	Coils/Number of the Coils	Coils' Dimensions and Number of Turns	Gap			
[116]	Flat structure/Circular coils (44-mm inner diameter)	Symmetrical/three resonance structure	Two 76-mm diameter circular coils and a source coil with 36-mm diameter.	62 mm	684 kHz 20 Ω	12.9 W 43% At 40 mm	The maximum efficiency of the three-coil system shows a significant advantage over that of the two-coil system.
[117]	Flat structure/Circular spiral coils	Asymmetrical/four resonance structure	Six turns for each coil. Outer diameter for *Tx* is 590 mm; for *Rx*, it is 280 mm, and the drive loop diameter is 280 mm	700 m	7.65 MHz $k = 0.1376$	12 W Laptop 50%	Presented a WPT that maximizes the quality factor of the coils; by proper loading of the drive and load loops, efficiency will be better.
[122]	Double-layer printed spiral coil PSC (square spiral coil)	Symmetrical/four resonance structure	Double-layered for each layer: 3.875 turns. Width: 288 mm, Substrate: 300 mm × 300 mm	500 mm	4.03 MHz	150 W 50%	The printed spiral coil (PSC) has high precision, high stability, easy to design, and manufacture.

Table 6. Research work related to coil with cores structure.

WPT System	Resonators				$f_0/k/R_L$	P_{out}, V_{out}, Efficiency %	Note
	Resonator Structure	Size of the Coils/Number of Coils	Coils' Dimensions and Number of Turns	Gap			
[64]	Coil with a core/Dipoles with cores	Symmetrical/two-coil resonance structure	Number of turns for *Rx*: 22. Number of turns for *Tx*: 86. The length of the core is 3 m, and the length of the coil is 1 m.	3 m 4 m 5 m	20 kHz *k*: (0.68%,0.39%, 0.26%) 40 Ω	1403 W 29% 471 W 16% 209 W 8%	Coils with ferrite cores will minimize parasitic effects. The optimum-stepped core structure can reduce the core loss.
For roadway-powered moving electric vehicles (high power)							
[146]	Coil with a core/Resonator with EE, UU core-type	Asymmetrical/multi-coil structure	Power line modules in addition to UU, EE cores. Pick up coils for EE: five coils total, center: 64 turns, left and right: 28 turns each.	26 cm	20 kHz	100 kW 620 V 80%	The implementation cost of the power receiver unit/kW was about $89/kW.

Table 7. Domino resonator systems.

WPT System	Resonator parameters		f_0/R_L	P_{out}, Efficiency %	Note
	Resonator Structure	Coils' Dimensions and Number of Turns			
[151,152]	Symmetrical/circular coils/domino structure/	The WPT has eight resonators, which have a radius of path r of 300/235 mm for three-resonator and four-resonator systems, respectively. The number of turns is 11.	520 kHz (11.57~16.94) Ω	14 W, 70.68~83%	The optimized operating frequency of this system is not the resonant frequency of the resonators.

The circular, spiral circular, square, and rectangular geometries are widely used due to their simple design and low manufacturing cost. To give a clearer picture of the circular and rectangular coils, new classifications (concluded from the above-mentioned tables) are presented in Tables 8 and 9, respectively. Comparing the size of the coils, the transferring distance, and the operating frequency, the systems will show approximate results.

Table 8. Research work on circular structures.

Case	1	2	3	4	6
A/S/iC	A/2C	S/2C	S/2C	A/2C	S/2C
Topology	SS	LCL-S LCC-S	SP	LCC-LCC	SS
Size D_1/D_2 mm	500/400	226/226	500/500	600/300	220/220
Gap mm	200	100	200	150	240
Frequency	85 kHz	140 kHz	20 kHz	85 kHz	200 kHz
Efficiency	95%	93%	93%	92.6%	85%

Note: A: asymmetrical system; S: symmetrical system; C: coil; i: number of coils.

Table 9. Research work on rectangular structures.

Case	1	2	4
A/S	S	A	S
Topology	LCC-LCC	LCC-LCC	S-SP
Size mm^2	800 × 600	600 × 450 400 × 300	500 × 600
Gap mm	200	150	100
Frequency kHz	79	85	40
Efficiency	96%	95.5%	95.2%

In EV charging application and due to space limitations, some structures, such as the helix, omnidirectional, cavity, or conical, cannot be used. However, the resonators are designed as spiral or planar coils. These geometries are printable and easy to implement at a low cost. Moreover, the dynamic charging systems are used, and according to the track length, they can be divided into two categories. The first is the long-track transmitter, which can charge multiple vehicles simultaneously. This system is simple and has a low number of components. The online electric vehicle (OLEV) with a maximum charging power up to 100 kW is one example. However, this design has a low efficiency of 74%. The second is the short-individual transmitter, where the length of the transmitter is usually within 1 m. In this system, each transmitter has a compensation circuit. Therefore, multiple short transmitters are arranged in an array to make a tracking lane, and the transmitters can be excited based on the location of the receiver. This structure is considered flexible, but requires a large number of circuit components and converters.

There are other architectures used in EVs; for example, in [104], the Oak Ridge National Laboratory (ORNL) presented an in-motion charging system for EVs/PHEVs, which transfers the power to a moving receiver coil as it passes over two transmitting coils connected in series. In this system, the coil design depends on jacketed Litz cable coils over a structure of soft ferrite. The Research Centre for Energy Resources and Consumption (CIRCE) in Spain proposed a receiver, which is longer than the transmitter [157]. In [105], the influence of the difference of the ratio between the receiver length and the transmitter length is investigated. The structure is a couple of unipolar square-shaped pads made of a copper coil, and a metallic plate, which represents the floor of the vehicle chassis, was placed 25 cm above the transmitter. In [158], the authors presented an overview of the current studies related to automotive applications, such as Korea Advanced Institute of Science and Technology (KAIST) projects on an OLEV bus, HalolPT, which developed IPT solutions in a power range of 3.3–20 kW, and WiTricity (MIT), which proposed a 3.3-kW system that has been proven. In addition, Plugless Power is a 3.3-kW IPT stationary charger, which was developed by Evatran and Bosch.

Based on the number of phases, WPT systems can be divided into two sections: single-phase systems and three-phase systems. The three-phase WPT systems that operate at symmetrical conditions and similar phase currents have two essential benefits compared to the single-phase systems: they have higher power level and better far-field EMC performance due to the three magnetic fields' superposition. In addition, they have very small power ripples on the DC output [159]. The three-phase WPT system found its way to some practical applications, for example, in [16], authors proposed a three-phase WPT system, which has six overlaid power lines and ended in two Y-points; each power line is symmetrical from its center, as a result, it can reduce the leakage magnetic field. In [35], the authors proposed a three-phase WPT, which can be used in recharging AUVs. A continuous charging system without onboard batteries was proposed [49]. In this system, charging the batteries along roadways is not required. Therefore, there was no need for complicated pickup structures. For heavy-duty applications, a tuning approach for the three-phase WPT with a long track is presented [160]. There are some high power three-phase WPT systems in operation, such as the Brunswick and Berlin buses with a maximum power of 200 kW based on Bombardier PRIMOVE technology.

4.2. Size and Number of the Resonators

Comparing the transmitter and receiver coils according to their size, they can be either symmetrical or asymmetrical. The first one is the symmetrical coils, where the transmitter and the receiver coils have the same size [94,110,117]. However, in the asymmetrical coils, the transmitter and receiver coils have a different size [80,118,136]. WPT systems can be categorized according to the number of coils, as shown in Figure 7, where they can be classified as follows: two-coil structure (2C) [64,113], three-coil structure (3C) [116,132], four-coil structure (4C) [119,122], and multi-coil structure (MC) [136,151,152]. The strongly coupled magnetic resonance (SCMR), which is a 4C system, is classified into four systems [161]: a standard SCMR system, a conformal SCMR (CSCMR system), a 3D SCMR, and a hybrid SCMR (HSCMR). Generally, the two-coil system saves more space than the other systems. However, the three-coil or four-coil systems allow transferring higher power for a longer distance.

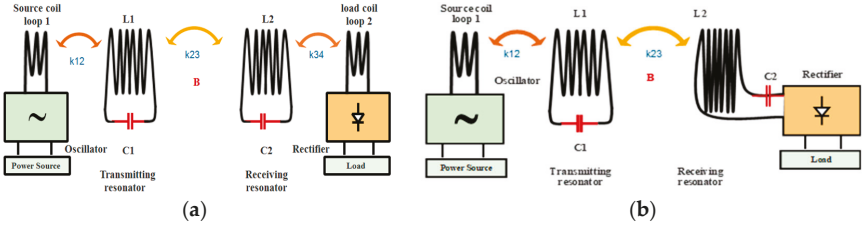


Figure 7. MCR WPT structure based on the number of the coils: (**a**) Four-coil MCR WPT; (**b**) Three-coil MCR WPT.

The multi-coil system is capable of charging multiple devices simultaneously. A WPT system that consists of a single transmitter and multiple receivers is investigated [32], and considered the influence of load and mutual inductance (the position of receivers) on the efficiency. A multi-coil transmitter array is employed to boost the power gain, which in turn allowed the application of very small receivers at a quite far distance [77]. A power transfer from a single source coil to multiple receivers through MCR WPT was demonstrated [162]. In addition, a WPT system based on the resonant cavity is proposed [136], and provided an efficient power delivery to many receivers simultaneously in an enclosed 3D volume of space (charging multiple toys that are placed randomly in a box or charging multiple LEDs). WPT systems based on the resonant cavity have the potential to enable a wide variety of new applications in many medical and industrial fields. However, this system has a problem in distributing the power uniformly to many receivers, especially in wearable devices or IMDs. To overcome this issue, a selective technique for smart power delivery to multiple receivers

is presented [163]. The method allows transferring the power to one receiver coil among multiple receivers by separating the resonant frequencies of the receivers, and isolating the cross-coupling effects between the coils.

4.3. Loop Inductance

Table 10 provides the self-inductance formula for some resonator shapes, such as square, rectangular, circular, and so on [164,165]. Table 11 gives layout dependent factors (x_i) for on-chip spiral inductors, such as square, hexagonal, octagonal, and circular [124].

Table 10. The inductance of different coreless loops.

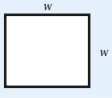
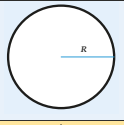
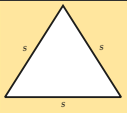
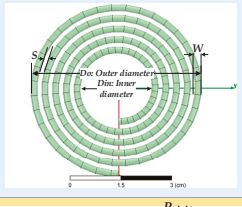
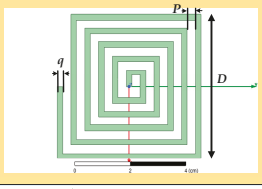
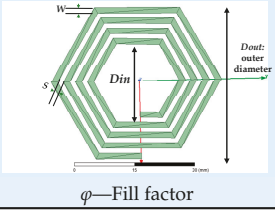
Resonator Type	Inductance	Comments
Straight conductor	$\frac{\mu_0}{2\pi}\left[\left(\ln\frac{2l}{a}\right)-\frac{3}{4}\right]$	l: Length, a: radius of the conductor.
Square loop	$2N^2\frac{\mu_0\mu_r w}{\pi}\left[\left(\ln\frac{w}{a}\right)-0.774\right]$ Where N: The number of turns.	μ_r: Relative permeability. 
Rectangular loop	$N^2\frac{\mu_0\mu_r w}{\pi}\left[\begin{array}{r}-2(w+h)+2\sqrt{h^2+w^2}\\ h\ln\left(\frac{h+\sqrt{h^2+w^2}}{w}\right)-w\ln\left(\\ h\ln\left(\frac{2h}{a}\right)+w\ln\end{array}\right.$	
Circular	$N^2\mu_0\mu_r R\left[\ln\left(\frac{8R}{a}\right)-2.0\right]$ R: radius	
Equilateral triangle	$N^2\frac{3\mu_0\mu_r s}{2\pi}\left[\ln\left(\frac{s}{a}\right)-1.405\right]$	
Pancake coil (flat spiral coil)	$\left(N^2A^2\right)/(30A-11D_{in})$ where: $A=(D_{in}+N(w+s))/2$ W: the wire diameter. S: the separation between two turns.	
Square spiral coil	$27.10^{-10}\left(\frac{D^{8/3}}{P^{5/3}}\right)\left(1+R^{-1}\right)^{5/3}$ where $R=P/q$ q: thickness, P: the separation between turns.	
On-chip inductor spiral loops *L*-(nH) [124]	$N^2\frac{x_1 D_{ave}\mu_0}{2}\left[\ln\left(\frac{x_2}{\varphi}\right)+x_3.\varphi+x_4.\varphi^2\right]$ where: $D_{ave}=(d_{out}+d_{in})/2$ $\varphi=(d_{out}-d_{in})/(d_{out}+d_{in})$ x_i—Factors from (layout depending, it is given in Table 11)	 φ—Fill factor

Table 11. Layout dependent factors.

Layout	x_1	x_2	x_3	x_4
Square	1.27	2.07	0.18	0.13
Hexagonal	1.09	2.23	0	0.17
Octagonal	1.07	2.29	0	0.19
Circular	1	2.46	0	0.2

Coil design is a basic step in WPT systems, since it determines the level of power transfer, efficiency, and the overall performance [104]. Therefore, the inductance is considered one of the most significant factors in the WPT system. The inductance depends on the coil geometry, which includes the size of the resonator, cross-sectional area, length, and number of turns, in addition to the separation between turns and thickness or width of copper.

4.4. Operating Frequency Effects on the Design of Coil Structure

An ideal inductor can be modeled as an inductance with no resistance, capacitance, or energy dissipation. On the other hand, for real inductors, as shown in Figure 8, the above-mentioned components are inevitable. The wire has a resistance (R_{ac}) and losses in the core materials. In addition, there are parasitic capacitances (C_{self}) caused by the electric field between the turns. The parasitic capacitance with the self-inductance can determine the self-resonant frequency (SRF) of the coil. At high frequencies, the effect of these factors will be obvious, and the AC resistance value will increase due to the skin effect. Therefore, the quality factor of the coils will drop. Due to high frequency, the current will be concentrated near the surface of the copper conductor, and as a result, the power loss will increase and cannot be ignored [166].

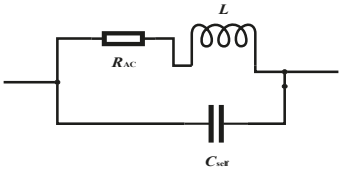


Figure 8. Equivalent circuit of the real inductor.

The inductance and skin effect are given as follows [162]: $R = r.N/d\sigma\delta$, $\delta = 1/\sqrt{\pi\sigma\mu f}$ (m), respectively. In the previous equations, r is the radius of the coil, d is the radius of the wire, and σ is the conductivity; for copper, $\sigma = 5.8 \times 10^7$ (S/m) and $\mu_0 = 4\pi \times 10^{-7}$ (H/m). Figure 9 presents a copper conductor with a 0.5-mm radius. When the frequency increases, the skin effect will be clearer. In order to reduce the AC resistance and power losses, Litz wires (multi-strand wires) are used to wind the coils. Based on the operating frequency range, the required diameter, and the number of wire gauge of the Litz wire can be determined [146]. In addition, superconducting materials were used to decrease the resistance and achieve a high-quality factor [144].

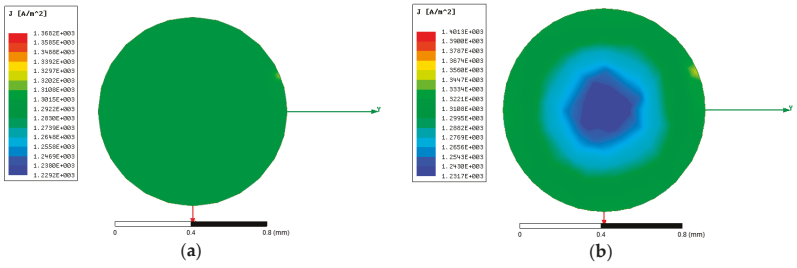
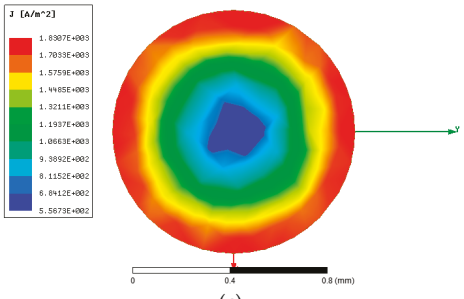


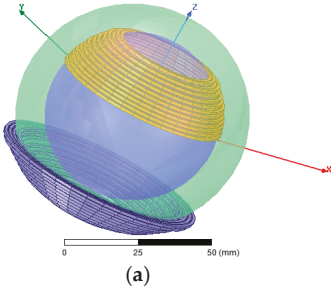
Figure 9. *Cont.*



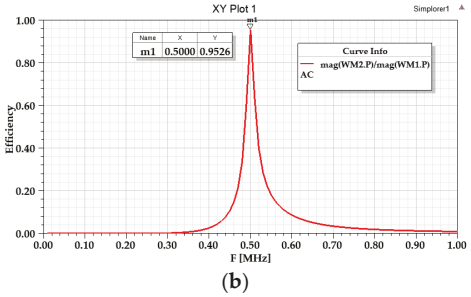
(**c**)

Figure 9. Skin effect (done by ANSYS Electronics 19.0.0; Canonsburg, PA, USA; 2018): (**a**) 60 Hz; (**b**) 20 kHz; (**c**) 85 kHz.

Finally, the frequency-splitting issue is a key point of an MCR WPT system. When moving the resonators toward each other gradually, the coupling between them becomes stronger, and if they are close enough, the resonant frequency will change. As a result, the transferred power drops sharply [167]. To clarify this case, Figure 10 shows two spherical structures for a WPT system, where the transmitting coil *Tx* is in blue, and the receiving coil *Rx* is in orange (the spherical joint structure for a WPT will be discussed in the seventh section). The coil windings are wound in different ways. In Figure 10a, *Tx* and *Rx* are located opposite to each other, and the coupling coefficient will be $k = 0.089$. Figure 10b displays the efficiency at the resonant frequency (500 kHz). In Figure 10c, *Tx* and *Rx* coils are wound in the same direction as the hemispherical structures. As a result, this model will have a short transferring distance, and the coupling coefficient will be high $k = 0.54$. Figure 10d illustrates the efficiency at the resonant frequency (500 kHz).



(**a**)



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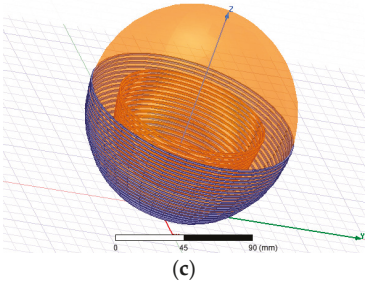
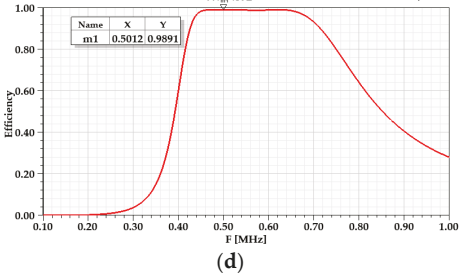


(**c**)



(**d**)

Figure 10. Efficiency at the resonant frequency (500 kHz) for two spherical structures. (**a**,**b**) $k = 0.089$; (**c**,**d**) $k = 0.54$.

To deal with the frequency-splitting issue and power transfer degradation, several methods are presented, such as an adaptive frequency tracking method, which changes the frequency in the strongly coupled region [168]. Instead, the frequency-splitting issue is suppressed by switchable configurations, such as for example, a switchable capacitor array [169], alternative multiple loops [170,171], and various load resistances [172].

5. Misalignment Study

In order to get a higher power transfer efficiency (PTE), the alignment between the WPT resonators should be perfect. However, the coils are usually misaligned [119]. There are several types of misalignment between the coils, which include the following. (1) In lateral (horizontal) misalignment, the coils are located in parallel planes, but they are offset by distance Δx. (2) In angular misalignment, the receiver coil is moved by an angle ϑ while the centers of the transmitter and receiver coils are well aligned [173]. (3) In vertical variation, the receiving coil moves vertically. (4) In planar misalignment, *Tx* and *Rx* are in parallel, and *Rx* rotates around the center point, but keeps the same transferring distance. (5) In angular azimuth misalignment, the transmitter is fixed, and the receiver rotates around the *z*-axis in the *x*-*y* plane from $\varphi = 0^\circ$ to $\varphi = 360^\circ$. (6) In angular elevation misalignment, the receiver rotates around the *x*-axis in the *y*-*z* plane from $\theta = 0^\circ$ to $\theta = 360^\circ$, and the transmitter is fixed [161].

Figure 11 displays different types of misalignment. This figure has shown a circular resonator to present misalignment types. However, the same misalignments apply to other structures as well, such as rectangular, square, and hexagon.

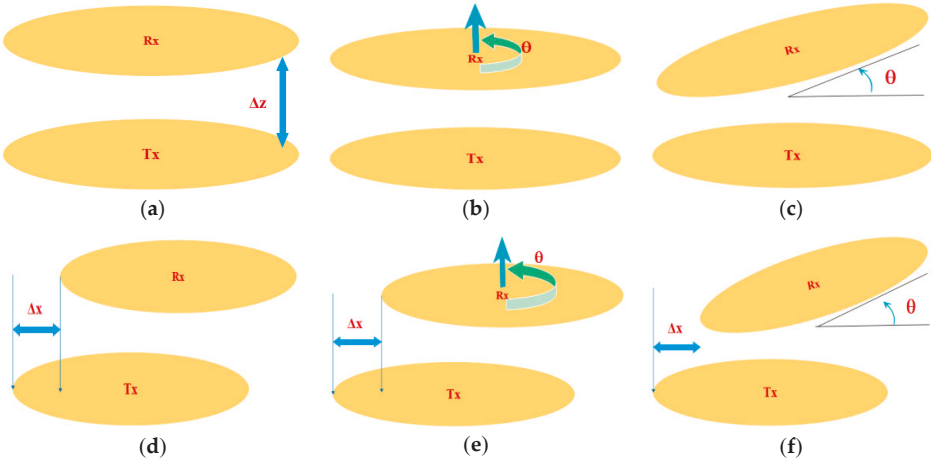


Figure 11. Types of misalignments: (**a**) Vertical variation; (**b**) Planar; (**c**) Angular; (**d**) Lateral (horizontal); (**e**) Planar and horizontal; (**f**) Angular horizontal.

Table 12 compares between different misalignments considering the coil structure and misalignment effect; some notes related to each type are given in comments.

The misalignment differs randomly under different situations and different application types. As a result, several parameters may change during the process, such as the mutual inductance, the efficiency, and output power. During the EV's charging, if there is imperfect parking, the transmitter and receiver coils will be misaligned. The transmitter coil is fixed on/under the ground, and the receiver is mounted on the bottom of the vehicle. In IMDs applications, if the patient breathes, the air gap of the WPT will change. Therefore, it is important to predict the misalignment tolerance of the WPT system in different applications. In addition, the system needs good controllability and optimization to deal with its parameter variations.

Table 12. Misalignment types: a review. SCMR: strongly coupled magnetic resonance. HSCMR: hybrid SCMR. CSCMR: conformal SCMR.

Case	The Resonator Structure	Misalignment Type	The Effect of Misalignments	Comments
[173]	Circular spiral coil	Lateral/Angular	The values of output voltage decrease with the misalignment.	According to the test, even if the lateral and angular misalignments happen. The efficiency at a 5 cm distance is up to 50%.
[161]	Circular	Lateral/Angular azimuth/Angular elevation	The proposed structures: 3D SCMR, HSCMR, and CSCMR are less sensitive to the misalignments than the standard SCMR system.	The system achieves an efficiency of 40% for the entire range of 360° in case of the angular misalignment.
[1]	Helical	Lateral/Angular general (angular horizontal)	$M = x(\Delta, \alpha)$. N^2: M is the mutual inductance, which increases linearly depending on the square of the coil turns.	x (Δ, α) is a variable coefficient that depends on the lateral misalignment Δ, and the angular misalignment α. The average value of the slope is (0−10 cm, 0~50°).
[99]	Double D (DD) bipolar pads	Horizontal	The efficiency is higher than 90%, even at a large misalignment in the x-direction.	For EV application, the x-misalignment is door-to-door, and the y-misalignment is front to rear.
[95]	UU type	Horizontal/Vertical	The self-inductance of the pads changes slowly with the misalignment of the coils, but the mutual inductance changes fast.	The current-fed compensation topology is a practical solution for WPT.
[132]	Helical coils	Angular	Compared to the single-transmitter WPT system, the proposed system gives a higher power transfer efficiency during the angular aligned and in case of the angular misaligned.	The paper proposed a multiple-transmitter WPT, which provides a power transfer diversity.
[113]	H-shaped DGS and semi-H-shaped	Horizontal shift/Coaxial orientation	Compared to H-shaped DGS, the semi-H-shaped DGS is more robust to misalignments.	These features boost the usage of the semi-H-shaped DGS in WPT applications.
[117]	Circular spiral coil	Angular	The case of a fixed frequency undergoes the same trend of process from the over coupled to critically coupled, and then under coupled system.	The receiver unit is placed on the axis at a fixed transferring distance of 50 cm.
[110]	Rectangular	Forward direction	Compared with SP-compensated WPT, the S/SP-compensated WPT is more robust to the misalignment.	The range of the output voltage of the SP-compensated WPT is almost double that of the S/SP-compensated WPT,

6. EMI and EMF Diagnostics in the WPT System

The electromagnetic spectrum includes two sectors. They are as follows. The first is the non-ionizing area, which means the energy of the waves is too low to ionize tissues. The second is the ionizing radiation area. MCR WPT products use electromagnetic waves within the non-ionizing area of the electromagnetic spectrum.

6.1. WPT-Related Standards, Including the Safety Issues

Regarding safety issues linked to WPT usage, there are two serious issues. The first is that long-term exposures to time-varying EMFs can harm the human body. Therefore, the International Commission on Non-Ionizing Radiation Protection (ICNIRP), expert groups, and the World Health Organization (WHO) have documented and issued some guidelines to ensure the safety of the human body. The second is a wide range of harmonics generated by inverters, which in turn create EMI issues on the other electronic devices' operations. Therefore, it is important to suppress EMF and EMI in the WPT system [174].

Based on the obvious risks that are caused by using the WPT charging systems, it is necessary to regulate the usage of the WPT systems. Therefore, many recommendations, standards, and guidelines

were issued. Table 13 provides a comprehensive review of WPT-related standards and guidelines that were issued by different international organization around the world. For example, in order to protect against any known health effects, the ICNIRP has published guidelines for maximum exposure limits. They consist of the publications from 1998 (0 Hz–300 GHz) and 2010 (0 Hz–100 kHz).

Table 14 presents the near-field WPT systems, including the frequency and power ranges under study in non-ISM bands for Japan and South Korea.

It is inevitable for the electrical circuits and the human body that are close to the WPT system to be under the influence of EMI emissions or exposure to EMFs. Therefore, it is essential to regulate the deployment of the WPT system to ensure the safety of the consumers and electrical components. The standards differ from one country to another. Therefore, the WPT system can be categorized based on the frequency, power, transferring distance, and application type. As a result, the WPT system is handled as normal equipment that follows specific restrictions, or it is considered an important case that follows tighter restrictions.

Table 13. Comprehensive review of WPT-related standards and guidelines. EMF: electromagnetic field, EU: European Union, ICPT: inductive coupled power transfer, USA: United States.

Standards	Substandard	Country	Frequency/Power	Application/Comments
Federal Communications Commission (FCC)	KDB 680106 Part 15B and part 18	USA	Above 9 kHz are considered intentional radiators.	Radio frequency (RF) exposure wireless charging apps (wireless chargers, inductive chargers, and wireless charging pads).
Society of Automotive Engineers (SAE)	SAE J2954/J2836/6™ J2847/6-J2931/6		J2954™ EVs and PHEVs use 85 kHz band.	Wireless charging task force, specific use cases, and specific protocols.
The International Special Committee on Radiofrequency	CISPR SC-B	International	From 9 kHz upwards, CISPR 11 range is 150 kHz up to 1 GHz	Household appliances, ignition systems, and fluorescent lamps.
	CISPR 11:2015			Power electronics in the industrial, scientific and medical frequency band (ISM band): RF equipment used in WPT.
International Electrotechnical Commission (IEC)	IEC 61980-1:2015, IEC 62827-2:2017, IEC PAS 63095-1:2017(E)		For IEC PAS 63095-1:2017(E) baseline power profiles are (≤5 W) and extended power profile is (≤15 W).	▪ IEC 61980-1:2015: General requirements for EV WPT. ▪ IEC 62827-1:2016: justifies various functions of WPT system. ▪ IEC 62827-2:2017: Control management of multiple-device WPT. ▪ IEC PAS 63095-1:2017(E): Qi WPT and interface definitions.
International Organization for Standardization (ISO)	ISO PAS 19363, 2017-1-1, (ISO/NP 19363 under development)		Close synchronization with IEC 61980 and SAE J2954.	▪ Magnetic field WPT, safety, and interoperability requirements.
International Commission on Non-Ionizing Radiation Protection (ICNIRP)	ICNIRP 1998 ICNIRP 2009 ICNIRP 2010		EM Field: (1 Hz–100 kHz)/2010 (1 Hz–300 kHz) 1998.	▪ Guideline for limiting the exposure to electric fields and magnetic fields, which vary by time. ▪ ICNIRP 2010 replaces the low-frequency part of the 1998 guidelines.
European Telecommunication Standards Institute (ETSI)	ETSI EN 303 417 V1.1.0 (2017-9).	EU	For WPT systems that use frequency other than RF beam, and it has investigated ranges: [19–21 kHz, 59–61 kHz, 79–90 kHz, 100–300 kHz, and 6765–6795 kHz].	Harmonized standard, which covers the essential requirements of article 3.2 of Directive 2014/53/EU.
China Communication Standard Association (CCSA)	CCSA TC9	China	Part1: General; part2: Tightly coupled (ICPT); and part3: Resonance wireless power transfer (MCR WPT).	EMF evaluation methods for WPT and EMC limit and measurements.
	YD/T 2654-2013			Requirements and test methods of EMC of WPT equipment.

Table 13. *Cont.*

Standards	Substandard	Country	Frequency/Power	Application/Comments
Association of Radio Industries and Businesses (ARIB); Broadband Wireless Forum (BWF)	ARIB STD-T113 (2015)	Japan	6.78 MHz-band MCR WPT for mobile, 400 kHz–band for CPT. EV/PHEV WPT spectrum: (42 kHz~48 kHz, 52 kHz~58 kHz, 79~90 kHz, and 140.91~148.5 kHz). Power: 3 kW and 7.7 kW.	Study for WPT spectrum for all the applications and technologies. ▪ CPT system. ▪ MCR WPT using 6.78 MHz for mobile and portable devices. ▪ Magnetic induction WPT for home appliances and office equipment. ▪ WPT for EV/PHEV.
	BWF TR-02 Edition 1.0/2016		100 kHz, 100–500 kHz, and 6.78 MHz.	▪ Assessment on EMI due to WPT systems.
Telecommunication Technology Association (TTA)	TTAR-06.162 (19/11/2015)	Korea	For EV in 2011, OLEV (19 kHz~21 kHz and 59 kHz~61 kHz).Normal Power: 100 kW.Frequency: 13.56 MHz band is used for 3D glasses WPT.	▪ Efficiency measuring methods for WPT and heavy duty EVs. ▪ MCR WPT (magnetic resonance). ▪ WPT (magnetic induction).
Alliance for Wireless Power (A4WP)	A4WP standards	Established in 2012 (Samsung, Qualcomm and others)	6.78 MHz for power transfer and 2.4 GHz for the control signals.	▪ Magnetic resonance WPT. ▪ A4WP and PMA have merged to form industry-leading organization for wireless charging standards.
Wireless Power Consortium Qi (WPC)	Qi standards Version 1.0.Version 1.1.	Industry group, since 2008	Range: 110 kHz–205 kHz.Low power in the range of (0–5) W. Medium power is up to 120 W.	▪ Details and specifics about the Qi WPC standards. ▪ ICPT system. ▪ Used in cell phone, music players, Bluetooth, etc.
Power Matters Alliance (PMA)	PMA standard	Founded by Procter, Gamble and Powermat in	277 kHz–357 kHz and up to 5–10 W.	▪ Magnetic induction technique. ▪ Mobile device ecosystem.
Additional standards for electromagnetic compatibility EMC, immunity tests and measurements: Radiated and conducted emissions—CISPR 11. Compliance testing of wireless power transfer products ASNI C63.30. Radiated EM immunity—ISO 11451-2:2015-06 (E).				

Table 14. Current and ongoing study frequency and power range for WPT in Japan and Korea. PCs: personal computers.

WPT System	Country	Frequency Range under Consideration	Power Range under Considerations	Application
Inductive coupling (IPT): low power	Already in Japan, Korea	Japan: 110 kHz–205 kHz. Korea:100 kHz–205 kHz.	-	Mobile devices, portable devices, consumer electronics (CE), and industrial fields.
Inductive coupling (IPT): high power	Japan	Japan: 20.05 kHz–38 kHz, 42 kHz–58 kHz, and 62 kHz–100 kHz.	Japan: Several watts up to 1.5 kW.	Home appliances operating with high power, and office equipment.
Magnetically coupling resonant (MCR WPT)	Japan, Korea	Japan and Korea in the range of: (6.765–6.795) MHz.	Japan: Up to 100 W. Korea: Unlimited in-band emission limit	Mobile devices, tablets, note-PCs, and home appliances, which operate with low power.
Capacitive coupling (CPT)	Japan	Japan: 425 kHz–524 kHz.	Japan: Up to 100 W	Portable devices, tablets, and home appliances.

6.2. EMF and EMI Mitigation Methods

Some WPT charging applications have a large air gap, such as EVs, where it can reach 10–30 cm. This creates high levels of a stray field in the coils' vicinities, thus arises an issue regarding the exposure to magnetic fields for people who approach the vehicle or passengers during the charging process [175]. In [175], the authors presented a pulsed magnetic fields methodology (developed according to the requirements of the International Commission on Non-Ionizing Radiation Protection (ICNIRP) guidelines), the results for the assessment applied to a 20-kW IPT system for dynamic charging of EV at the frequency of 85 kHz. The charging is performed by using several independent transmitters (each one: 1.5 m long and 0.5 m wide). When the vehicle is above them, they will be activated. In this direction, the authors investigated the human exposure to the EMFs by using a computational modeling applied to a 7-kW WPT charging system at the frequency of 85 kHz [176]. In [177], two-step scaled frequency finite-difference time-domain (SF-FDTD) methods are used to calculate the internally induced electric fields in the human body.

EMF safety can be achieved through the magnetic field level reduction in the near-field area. Therefore, several reduction methods were presented, such as using ferrite materials [14], metallic materials (aluminum) [178,179], and metamaterials (MM) [180–183]. Changing the pulse width of the inverter to decrease the harmonics of the leakage electric field was presented [184]. In [185], the authors presented three active methods that include the independent self-EMF cancelation (ISEC), the 3-dB dominant EMF cancel method (3DEC), and the linkage-free EMF cancel method (LFEC). In addition, the authors have reported other techniques, such as separating pickup rectifiers and magnetic mirror methods. In [7], the authors presented a resonant reactive shield with one coil and a capacitor. In [186], a resonant reactive shield with two coils and four capacitors was discussed. Figure 12 illustrates the above-mentioned EMF mitigation methods. On the other hand, some EMI mitigation methods are reported, for example, the spread spectrum clock technology (SSC) [187]. In [174], the authors investigated an isolation inductor scheme to reduce EMI in an automotive tightly coupled handheld resonant charging system. Moreover, EMI can be suppressed by optimizing the rise and fall times of the output voltage in high-frequency soft-switching converters [188].

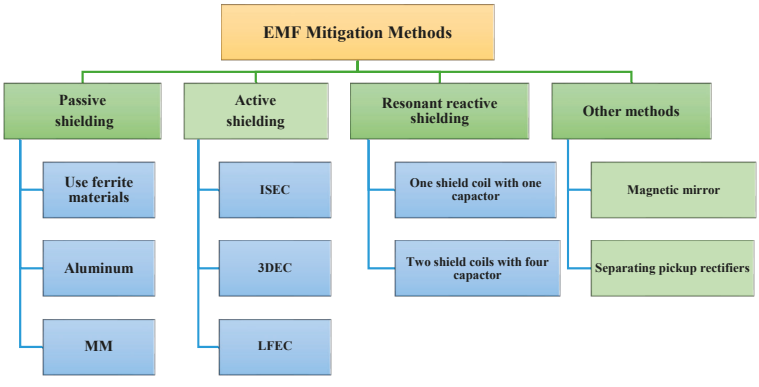


Figure 12. EMF mitigation methods.

Table 15 compares between different EMI and EMF mitigation methods, in addition to their advantages and disadvantages.

Table 15. EMF and EMI reduction methods: advantages and disadvantages. 3DEC: 3-dB dominant EMF cancel method, ISEC: independent self-EMF cancelation, LFEC: linkage-free EMF cancel method.

Case	Reduction Method	Advantages	Disadvantages	Notes
[14]	Using ferrite bars	Ferrite acts as a partial magnetic core for coupled coils, and it improves the system performance.	Ferrite bars experience hysteresis losses and have extra costs. In addition, some applications do not have enough space.	LCC-compensated topology is more effective than SS-compensated topology, and it produces a lower magnetic field in the near-field area.
[178]	Ferrimagnetic material	It can confine and guide the magnetic flux by providing a path close to magnetic field sources.	Using the ferrimagnetic material could be limited for some applications due to its cost, occupied space, and weight.	The EMF noise that is produced by CSPR topology is higher and worse than that of the CSSR noise. CSPR means constant current source CCO, series resonance for *Tx*, parallel resonance for *Rx*, and a resistive load (R). CSSR: constant current source
	Metallic shielding (Aluminum), same case in [179]	The metallic shielding induces eddy currents, which result in magnetic fields cancelation. Therefore, the total magnetic field near the material is reduced.	Ferrite and metallic shields block a wide band of electromagnetic spectrum. Consequently, they have a lower power transfer efficiency, in addition to the thermal stress caused by eddy currents.	
[180]	Near-field metamaterial zero-permeability shield	It does not cause significant extra losses, and it blocks the near-field radiation only at an exact frequency.	If the metamaterial is not placed between the coils, it will work as a shield, so it does not enhance the coupling.	The selective frequency technique blocks specific frequencies and allows other fields to pass. Consequently, this method could be used for human safety.
[16]	Three-phase power line to reduce the leakage EMF	The current circulates in two wires for each phase. Therefore, the side and center parts of the power lines cancel each other.	The three-phase system has a higher input current compared to the single-phase system.	This system uses six overlaid power lines (three in the center and three to the side); they are ended to two y-connections.
[185]	Active shielding: ISEC / 3DEC / LFEC	It generates counter magnetic fields from the EMF cancel coil. In addition, it is suitable for high-power application, such as EVs, PHEVs, and road-powered type EVs.	Requires extra components, extra coils, and a power supply.	The linear time-invariant steady-state system, which means that the cores are unsaturated and the circuit parameters are constant.
[7,186, 189]	Reactive resonant (with one or two shielding coils)	The cancelation magnetic field is generated from the original magnetic field noise. Therefore, it does not require any power source.	Requires shielding coils and capacitors.	The shielding coils are connected to each other so that the primary shield coil can supply enough shield current for the second shield coil. Consequently, the leakage magnetic field is reduced.
EMI mitigation methods				
[187]	Spread spectrum clock technology (SSC)	This method reduces the current spectrum, and as a result, the EMI is suppressed.	It requires a power supply, which occupies more space and weight. In addition, it is not simple to design.	Triangular modulation; the peak deviation ±1% and the modulation frequency is 156.25 Hz.
[174]	The isolation inductor scheme to reduce EMI	The magnitude of the input impedance is increased at higher frequencies. At the resonant frequency, no change at the magnitude of the input impedance.	DC–DC and coil-to-coil efficiencies are decreased due to the coil and core losses of the isolation inductor.	Isolation inductors of *Tx* and *Rx* are made of shell-type ferrite cores' coils.

7. WPT Applications: An Optimized Case Study

Figure 13 summarizes many applications of a WPT charging system, and shows that the WPT became an important part of some basic fields. First, in transportation, wireless power transfer for electric vehicles is a promising technology. Secondly, in the implantable medical devices (IMDs), it gives a convenient, reliable, and safe way to supply the power wirelessly without any pain to patients. Thirdly, in the field of consumer electronic applications, WPT is used in LED TVs, charging portable devices, such as cell phones, tablets, and other smart building appliances, where the WPT technology reflects the development of this kind of buildings. Moreover, the WPT system is used in IoT applications. Finally, WPT systems are used in LED lights, underwater detection, military defense systems, space applications, etc.

Figure 13. WPT applications.

To give a clear picture about the design method for a certain application, a 3D structured WPT that transfers the power wirelessly in a robotic application is proposed. The system is a bio-inspired joint for the WPT system. The joint consists of a movable spherical structure that rotates inside a big sphere using a mechanical stud (0°–85°). The transmitter coil (Tx) is wound on a hemispherical structure, as shown in Figure 14a, or wound on a spherical structure (with a slot), as shown in Figure 14c. In this case, the mechanical stud can rotate the small sphere up to 45°. The receiver coil (Rx) is wound on the small sphere structure. α is the displacement angle (degrees) between the vertical axes of the joint structures.

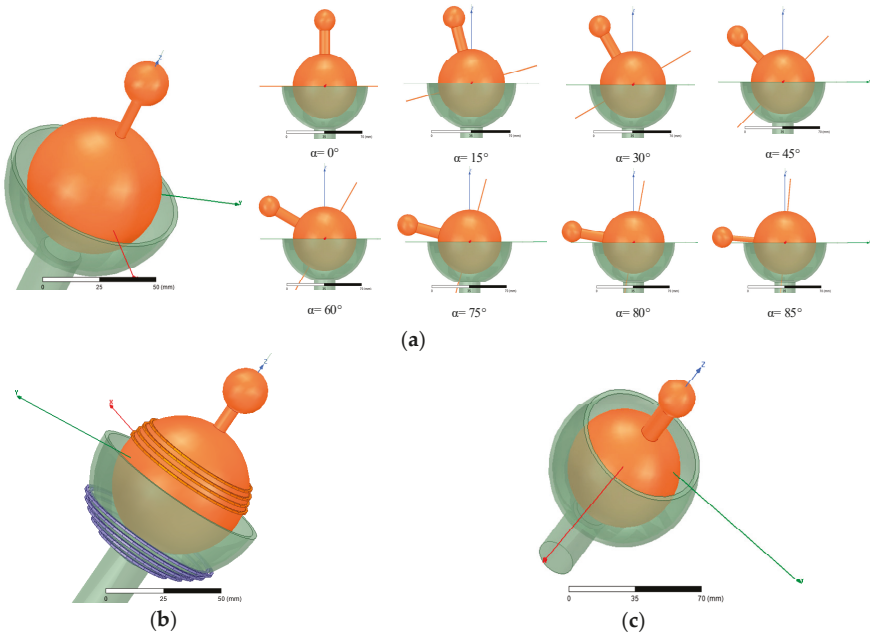


Figure 14. Joint-WPT: (**a**) Displacement angle (0°–85°); (**b**) An example of winding *Tx* and *Rx* coils; (**c**) Spherical model (0°–45°).

To design the WPT system, Figure 15 is illustrated. Considering the transferred power, frequency, structure, and other parameters, the purpose of the WPT system should be determined. The application type has two types of constraints, which include the structure and electrical constraints. The structure constraints include the size, volume, and gap. The electrical constraints comprise the compensation topology and its parameters, the required power to be transferred, and the operating frequency. On the other hand, several variables are parameterized to optimize the WPT, such as for example, the mutual inductance M, the output power, and the efficiency. WPT optimization is achieved by simulation and calculation, and experiments are put forward to validate the obtained results. Other factors can be considered during the design, such as suitable EMI and EMF mitigation methods (based on the application type).

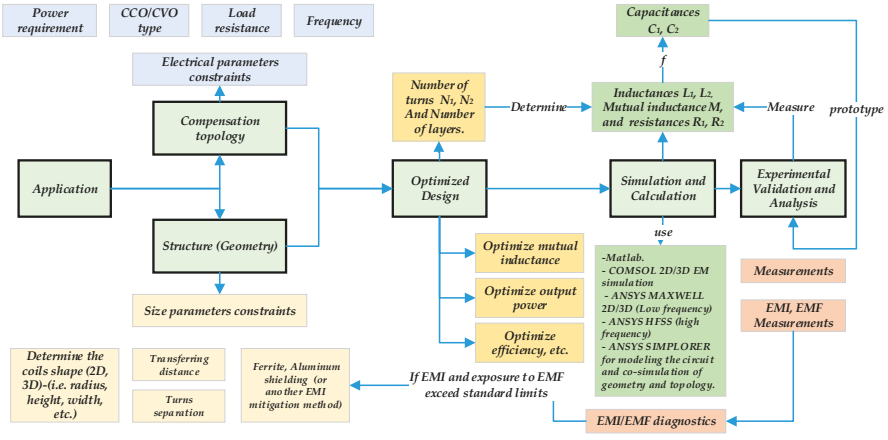


Figure 15. Schematic represents the design process of a WPT system.

7.1. Optimization Method

The power transfer efficiency (PTE) is a key design factor of the WPT system while operating over the resonance frequency. PTE optimization depends on the mutual inductance (M). M is proportional to the square root of the transmitter and receiver inductances L_1 and L_2, respectively. Therefore, the WPT system is optimized by changing the shape of the winding coils to maximize the mutual inductance (SS-compensated WPT) and reduce its fluctuation during the angular displacement. Several variables are considered to parameterize the coils, such as the number of turns, space between turns, and variation in the z-axis position.

Figure 16 presents the joint-WPT system in the y-z plane. The transmitter coil has N_1 turns, and the receiver coil has N_2 turns. r_i is the radius of each horizontal turn of the transmitter coil at a zi (z-position). rj is the radius of each horizontal turn of the receiver coil at zj (z-position). The radius of the transmitter coil is already given by r_s = 3.85 cm, and the radius of the receiver coil is given by r_b = 2.85 cm.

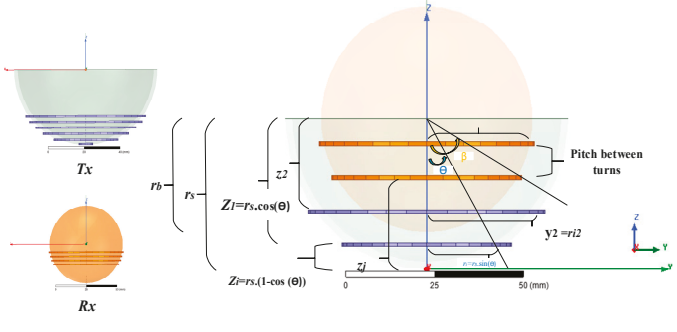


Figure 16. Joint WPT in the y-z plane with several variables to parameterize the coils.

The algorithm design is written as follows:

1. The size constraints: $0 \leq z_i \leq r_s$; the turns cover the whole space of the hemisphere of the transmitter structure, which means: $0 \leq \theta \leq (\pi/2)$. On the other hand, $10 \leq z_j \leq 2\, r_b$; the turns cover the whole space of the small sphere, which means: $0 \leq \beta \leq (\pi)$. The pitch between turns is set to P = 0.5 mm.

2. Initialize z_i, β, and θ as 0. Initialize z_j = 10 mm (start z-position for Rx), $N_1 = 0$, $N_2 = 0$, $m = 0$, and $n = 0$.
3. Enter the radius of the transmitter coil r_s = 38.5 mm, the radius of the receiver coil r_b = 28.5 mm, and the pitch between turns P.
4. Enter β and θ. // Measured in radian.
5. Count: $\theta = \theta + (1/36)\ \pi$, $\beta = \beta + (1/36)\ \pi$, $N_1 = N_1 + 1$, $N_2 = N_2 + 1$, $z_{im} = z_{im} + P$, and $z_{jn} = z_{jn} + P$, n addition to $m = m + 1$ and $n = n + 1$. // Increment angles to determine the z-position and r for each turn of the transmitter and receiver coils. ($(1/36)\ \pi$ is the assumed step). Increment N_1 and N_2 to find the number of turns for both coils. Move the turns in the z-direction with the pitch between coils equal to 0.5 mm. The number of turns can be calculated by $N_1 = z_{im}/P$ and $N_2 = z_{jm}/P$.
6. Calculate $r_{im} = r_s \sin(\theta)$, $r_{jn} = r_b \sin(\beta)$, $z_{im} = r_s\ (1 - \cos(\theta))$, and $z_{jn} = r_b\ (1 - \cos(\beta))$. // mm (based on angles).
7. Calculate L_1 and L_2: the self-inductances of the transmitter coil and receiver coil, respectively. Calculate and maximize the mutual inductance M and the coefficient coupling k, and determine the required capacitors C_1, C_2. // In order to maximize the mutual inductance, the inductances will be adjusted based on the number of turns and the space between turns (pitch). The transferring distance between Tx and Rx will determine the coupling coefficient, which should be less than a certain value k_s.
8. With the available values of the frequency and coil resistance, calculate the quality factor, transferred power, and efficiency.
9. Sweep the frequency and mutual inductance to maximize the efficiency and transferred power.
10. Is $k < k_s$, if yes, go to 11, or else go to step 13. The coupling coefficient should stay within a certain range to avoid cases with very low values or cases with very high coupling between Tx and Rx.
11. Is $\theta < \pi/2$, if yes, go to step 12, or else go to step 13.
12. Is $\beta < \pi$, if yes, go to step 3, or else proceed to step 13.
13. End.

Figure 17 illustrates a flowchart that represents the algorithm design.

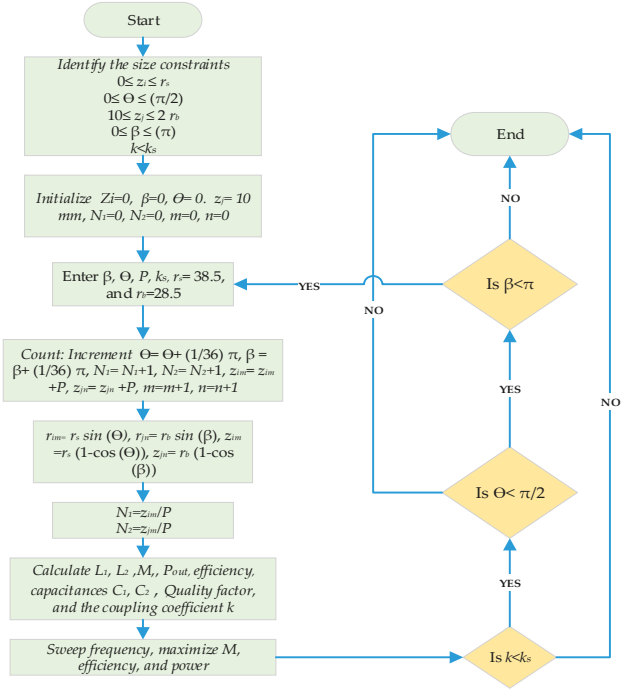


Figure 17. Flowchart represents the algorithm design of the joint WPT.

7.2. Simulations

The simulation of the joint WPT system is conducted by ANSYS electronics 19.0.0, USA, 2018. The optimization process has resulted in cases with high coupling coefficient values and others with low values. As shown in Figure 18, two cases are considered. The first is the hemisphere winding with a high coupling coefficient (k = 0.54). The second is the optimized model with k = 0.089. The obtained parameters are given in Table 16.

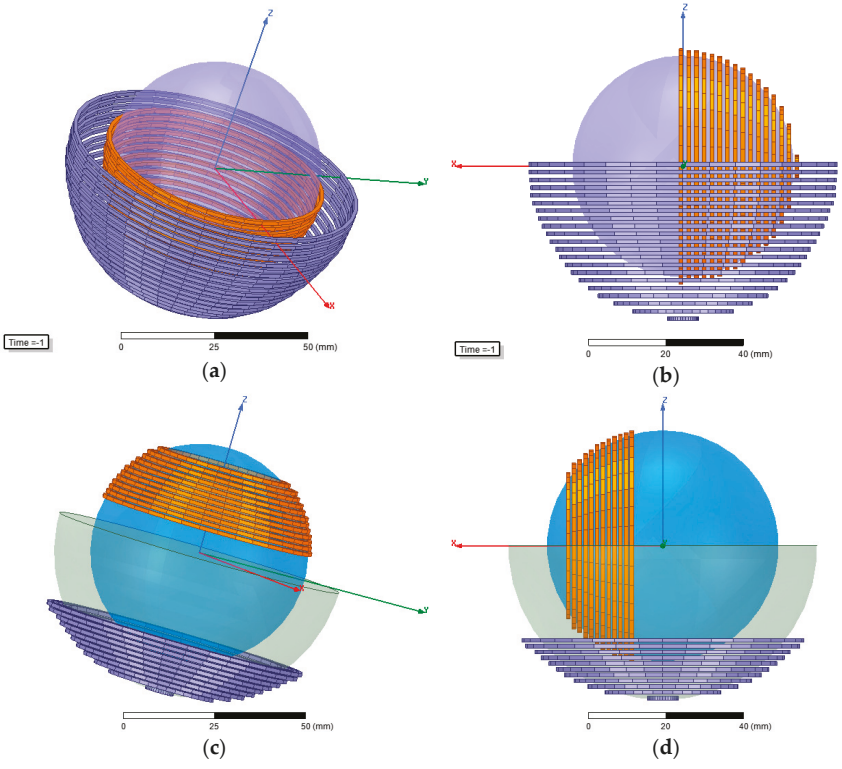
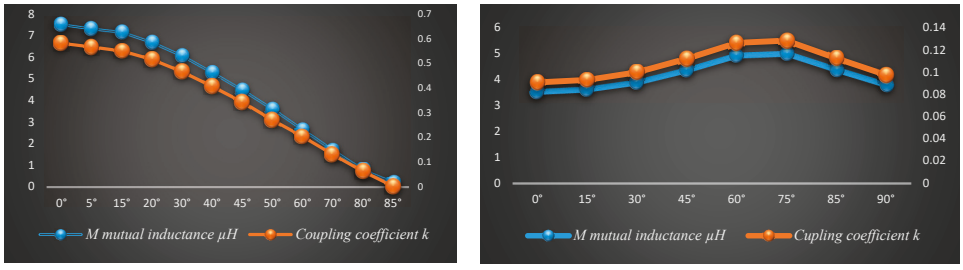


Figure 18. Two case studies: (**a**) Hemisphere winding at 0°; (**b**) Hemisphere winding at 90°; (**c**) Optimized design at 0°; (**d**) Optimized design at 90°.

Table 16. Parameters of case studies.

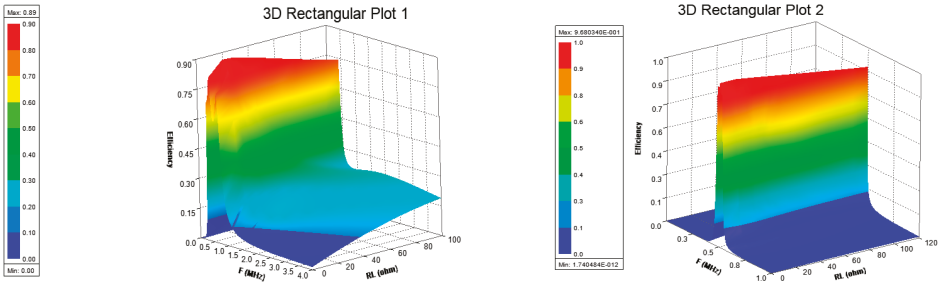
WPT	f_0	N_1/N_2	L_1/L_2 (μH)	Resistances: R_1, R_2 (Ω)	Mutual Inductance M	Coupling Coefficient k	C_1/C_2 (nF)
Hemisphere (a)	500 kHz	21/16	21.14/7.8156	0.23/0.13	7.478 μH	0.54	4.79/12.96
Optimized model (b)		34/22	50.699/31.83	0.19/0.1	3.6117 μH	0.089	2/3.18

Figure 19 shows that the mutual inductance and coupling coefficient for the hemisphere-winding drop rapidly with the angular misalignment, which can, in turn, lead to low efficiency. However, with the optimized solution, the fluctuation of M and k is reduced, and the performance of the WPT system is improved. Therefore, the receiver can rotate inside the transmitter from zero degrees (perfectly aligned coils) up to 90 degrees (practically 85°) while keeping high efficiency. Figure 20 shows the relation between the efficiency, load, and resonant frequency. For the hemispherical winding at a load of R_L = 20 Ω, the efficiency was up to 96% at $\alpha = 0°$. However, at $\alpha = 85°$, the efficiency dropped to lower than 10%. On the other hand, for the optimized WPT with the same load, the efficiency was up to 95.75% at $\alpha = 0°$ and 96% at $\alpha = 85°$ (the mutual inductance at 85° is higher than that at 0°).



(**a**) (**b**)

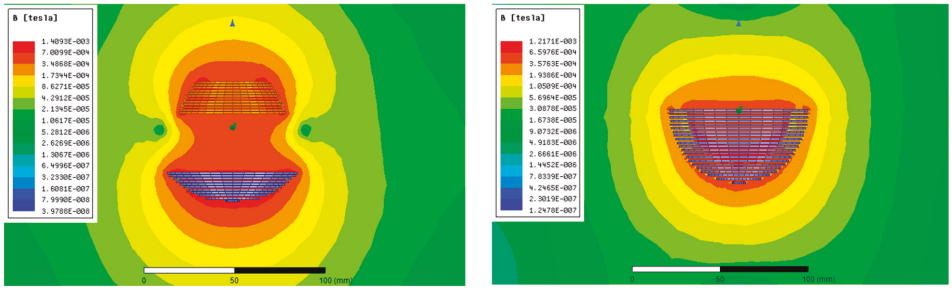
Figure 19. The mutual inductance and coupling coefficient: (**a**) Hemisphere winding; (**b**) Optimized design.



(**a**) (**b**)

Figure 20. WPT efficiency: (**a**) Hemisphere winding; (**b**) Optimized design.

Figure 21 presents the magnetic field density for the optimized and hemisphere models. The magnetic field density is given by B = μH, where H is the magnetic field strength (intensity) measured by (A/m). In Figure 21a, at $\alpha = 0°$, the yellow area (within 12-cm diameter) shows that B is around 86 μT, which is higher than the allowed level by ICNIRP 2010 (should not exceed 27 μT). In Figure 21b, the magnetic field density is concentrated in the close area around the coils. These cases require attention if the WPT is deployed close to the human body or other sensitive circuits. EMI and EMF mitigation methods can be selected based on the cost, weight, and size constraints of the joint. For instant, choosing ferrites is not a good choice, since it will put more pressure on the robotic arm. Based on the simulation results, a thin light sheet of aluminum can reduce the magnetic field density around the joint WPT to a safe level.



(**a**) (**b**)

Figure 21. The magnetic field density (B vector/cross section): (**a**) Optimized design; (**b**) Hemisphere winding.

7.3. Experiments of the Proposed WPT and Measurements

The WPT system is fabricated to validate the calculated and simulated results. Figure 22 presents the experimental setup, where a multi-strand Litz wire was used to wind the coils. Radio frequency (RF) Mica-type capacitors CDE (CD15FA102JO3F) and a half-bridge inverter were used. The system is SS-compensated WPT, and the experiments included two models, as presented in Table 16.

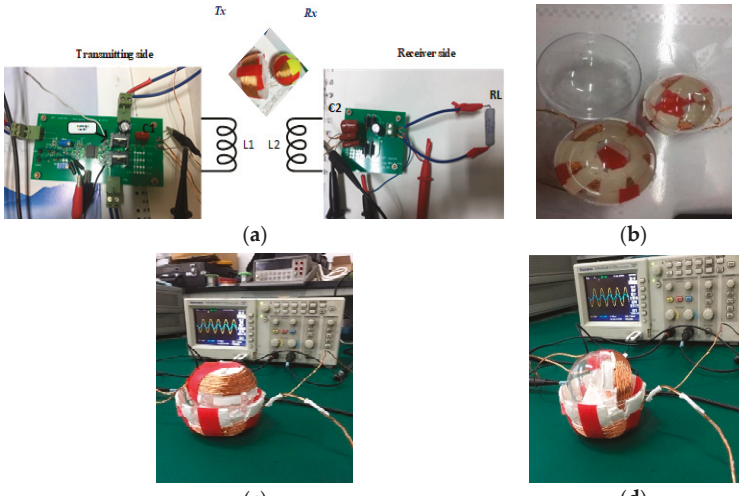


Figure 22. Experimental setup: (**a**) Circuits; (**b**) Hemisphere windings; (**c**) Optimized design at $\alpha = 0°$; (**d**) Optimized design at $\alpha = 90°$.

Figure 23 shows the input and output voltages at the resonant frequency (496 kHz) for the hemisphere-winding in Figure 23a, and the optimized model in Figure 23b.

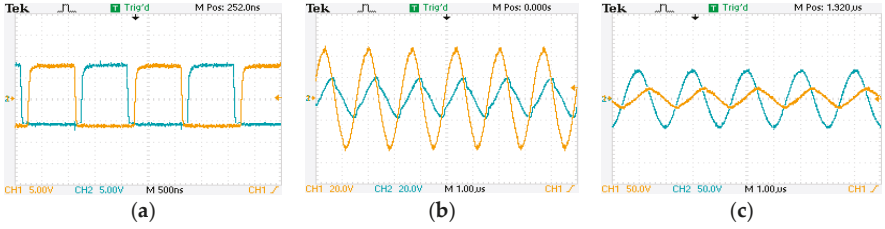


Figure 23. (**a**) Pulse-width modulation (PWM) signal; (**b**) Input/output voltages for the hemisphere case; (**c**) Input/output voltages for the optimized model.

The angular misalignment effects on the input and output voltages are given in Figures 24 and 25. In this structure, the receiver coil can rotate up to 85°. At $\alpha = 85°$, for the hemisphere-winding, the output voltage will drop to values close to zero. However, for the optimized model, even at $\alpha = 85°$, the output voltage keeps a high value.

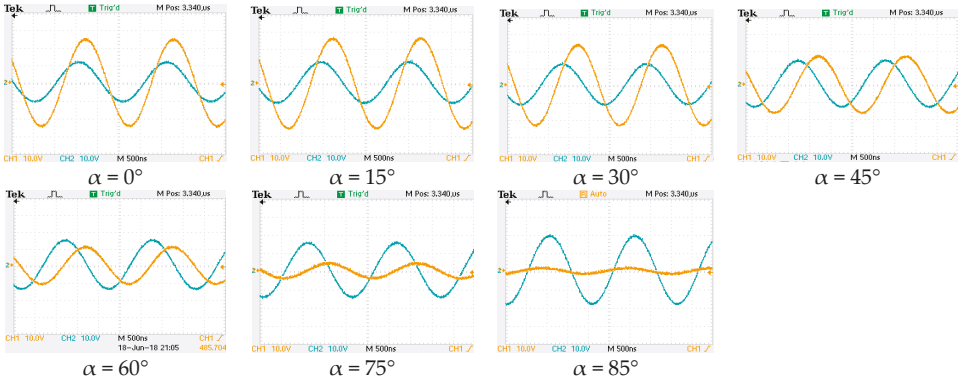


Figure 24. Input (blue) and output (orange) coil-to-coil voltages for the hemisphere winding.

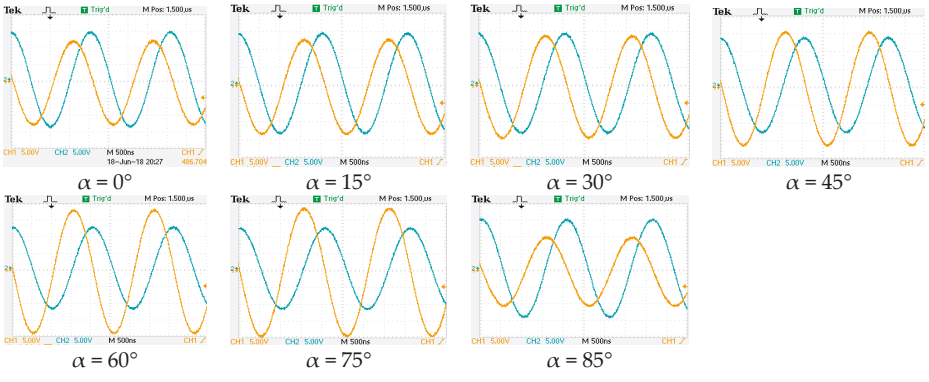


Figure 25. Input (blue) and output (orange) coil-to-coil voltages for the optimized model.

7.4. Cost Assessment of WPT Systems

The cost assessment of the WPT system can be done by considering the number of required components, such as inverter switches, diodes, Litz wires, resistors, capacitances, etc. In general, compared to hybrid topologies, the SS, SP, PS, and PP compensation topologies require fewer components. At kHz-range frequencies, high output power could be needed, and the power converters are added. As a result, the total cost is increased, such as EV charging applications that operate at 20 kHz and 85 kHz. At high frequencies, the output power could be very low, and the system does not require additional components such as IMDs that use the ISM band (2.2 MHz and 6.78 MHz).

8. Conclusions and Future Research

This paper has comprehensively reviewed the recent progress of the MCR WPT system including several aspects, such as compensation topologies, resonator structures, and misalignment analysis. In addition, EMI and EMF diagnostics were discussed, and the WPT-related standards were reviewed. Moreover, several EMI and EMF mitigation methods were reported and compared. Furthermore, a wide range of WPT applications was presented. Finally, a WPT case study was proposed. In the proposed winding method, a bio-inspired joint made of two spherical structures was given. The design process and algorithm design were provided, and experiments were conducted to validate the obtained results by simulation.

As shown in Figure 26, to work toward an optimum design of WPT, there are some factors that have an impact on the design process and thus should be considered during the design and

manufacturing process. The application type is determined by considering the size or volume, the transferring distance, the required power to be transferred, and the operating frequency. After that, inductances, resistances, quality factors, and mutual inductance are obtained. Choosing a proper compensation topology is another basic step. Other factors are considered, such as suitable EMI and EMF mitigation methods. Therefore, a good combination of the above-mentioned factors has to be considered. Even though many studies have been investigated, research related to new topologies, novel structures, new materials, and mitigation methods, in addition to system stability under misalignments, impedance matching, control strategy, and cost-effective assessment should be done.

Figure 26. Influencing factors in order to get an optimal WPT.

Author Contributions: M.A.H. conducted the review and wrote the manuscript. X.Y. and W.C. Guided and contributed in discussions and supervision.

Funding: This research received no external funding.

Acknowledgments: The authors would like to thank the anonymous reviewers for their constructive comments.

Conflicts of Interest: The authors declare no conflict of interest.

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MDPI
St. Alban-Anlage 66
4052 Basel
Switzerland
Tel. +41 61 683 77 34
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ISBN 978-3-03921-021-3