

Advanced Thin Film Materials for Photovoltaic Applications

Edited by I. M. Dharmadasa Printed Edition of the Special Issue Published in *Coatings*



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Editor

I. M. Dharmadasa

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About the Editor

I. M. Dharmadasa, Ph.D., is the Head of the Electronic Materials & Sensors Group at the Materials and Engineering Research Institute at Sheffield Hallam University in the UK. He has four decades of experience in both industry (BP Research—Sunbury) and academia. His research focuses on the development of next generation, low-cost and high-efficiency solar cells using electroplated semiconductors. These solar cells based on CdS/CdTe currently show 15% efficient lab scale solar cells, and his efforts are focused on developing graded bandgap multi-layer solar cells. Prof. Dharmadasa has published over 250 articles, six patents, and two books on "Advances in Thin Film Solar Cells" and "Graded Bandgap Multi-Layer Solar Cells". In this process, he has successfully supervised 28 PhDs, 14 years of postdoctoral research and examined 32 doctoral candidates. He is also actively involved in the promotion of clean energy for the sustainable development and reduction of poverty. He has designed, piloted, monitored for several years and is now replicating the "Solar Village" project. He referees for over 12 journals and is one of the editors for two learned journals in his research field. He currently serves as an assessor/panel member for The European Commission and the Commonwealth Scholarship Commission.





Special Issue: "Advanced Thin Film Materials for Photovoltaic Applications"

I. M. Dharmadasa

Editorial

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Abstract: Photovoltaic (PV) technology is rapidly entering the energy market, providing clean energy for sustainable development in society, reducing air pollution. In order to accelerate the use of PV solar energy, both an improvement in conversion efficiency and reduction in manufacturing cost should be carried out continuously in the future. This can be achieved by the use of advanced thin film materials produced by low-cost growth techniques in novel device architectures. This effort intends to provide the latest research results on thin film photovoltaic solar energy materials in one place. This Special Issue presents the growth and characterisation of several PV solar energy materials using low-cost techniques to utilise in new device structures after optimisation. This will therefore provide specialists in the field with useful references and new insights into the subject. It is hoped that this common platform will serve as a stepping-stone for further development of this highly important field.

Keywords: thin films; perovskite; SnS/SnS₂; CdS/CdTe; CIGS; silicon; electroplating of semiconductors; photovoltaics

In the past, photovoltaic device development was mainly based on simple p-n homo- or heterojunction type structures. However, these devices utilise only a fraction of the solar spectrum, and the rest is lost during the PV process. In order to harvest all photons from UV, Visible and IR regions, and add the contributions from "impurity PV effect" and "impact ionisation", graded bandgap multi-layer devices were designed [1]. These designs were experimentally tested using well known semiconductors (GaAs/AlGaAs), and their validity was proven by achieving $V_{oc} \sim 1.175$ V and FF ~ 0.86 [2]. After this validation, the new device architectures were fabricated using low-cost electroplated materials, and has achieved 15.3% efficiency to date. A monograph has been published [3] on this subject and the search for low-cost, advanced thin film materials is essential for the development of next-generation PV devices based on graded band-gap multi-layer solar cells.

This Special Issue consists of ten fully refereed scientific publications: seven open access articles [4–10] and three open access review articles [11–13]. The seven articles provide information on perovskite, SnS/SnS₂, CdTe, CIGS, silicon and transparent conducting oxide (SnO₂) materials used in solar cell development. One of these articles is a featured paper on electrodeposition of CdTe [7]. Out of the three review articles, one summarises the CdTe_(1-x)Se_x thin films in solar cell applications [11]. The second review focuses on the encapsulation of organic and perovskite solar cells [12]. The third paper is a feature review of the electroplating of semiconductor materials for applications in large area electronic devices [13].

Among the research articles, Nishi et al. [4] present their latest work on $CH_3NH_3PbI_3$ perovskite material deposited under normal atmospheric conditions. These authors present devices with efficiencies ~14.3% and a stability up to four weeks, with the efficiency reducing only to 13.4%. This work shows the improvement in stability in the right direction. The next article by Gedi et al. [5] presents the results of eco-friendly SnS and SnS₂ thin films' growth and characterisation using

chemical solution process. They report uniform and well-adhered layers with band gaps of 1.28 and 2.92 eV values, suitable for PV applications. Opyrchal et al. [6] report the photoluminescence study on the effect of Cu on the front side illumination of CdTe/CdS solar cells. The work focuses on the PL transitions close to the bandgap of CdTe. Ojo and Dharmadasa [7] present the results of electroplated CdTe material grown for use in CdS/CdTe solar cells. This article focuses on a case study of the temperature-dependent properties of electroplated CdTe thin films. Lorbada et al. [8], in their research article, provides a deep insight into the electronic properties of CIGS modules with monolithic interconnects. Chen et al. [9] present their results on enhancement of the potential-induced degradation resistance of crystalline silicon solar cells via anti-reflection coatings deposited by industrial PECVD method. The last research article by Ren et al. [10] presents the use of spin-coated SnO₂ thin films to cover cracks in the TiO₂ hole blocking layer used in perovskite solar cells. This process has improved the conversion efficiency of their solar cell structure.

The first review article by Lingg et al. [11] describes the properties of $CdTe_{(1-x)}Se_x$ thin films used in solar cell applications. First Solar Company has achieved ~22% efficient CdS/CdTe-based devices by incorporating Se in the CdTe layer. Hence, this comprehensive review is useful for researchers in this field to learn the properties of $CdTe_{(1-x)}Se_x$ alloy. The addition of Se in front of the solar cell creates a graded bandgap structure, enhancing the device performance. The second review paper by Uddin et al. [12] on the encapsulation of organic and perovskite solar cells is really important in order to improve the stability and lifetime of these types of solar cells. Although the highest thin film solar cell efficiencies of ~23% are reported for perovskite solar cells, their instability is a real concern at present. Hence, this encapsulation work is timely and useful for the researchers in this area. The last paper by Ojo and Dharmadasa [13] is a review paper on low-cost and high quality materials growth technique. This paper describes the electroplating of semiconductor materials for applications in large-area electronics such as PV solar panels and display devices. This will be an ideal paper for new researchers who intend to enter this area of research activities.

Finally, I would like to express my appreciation to all of the contributors to this Special Issue. They have positively responded to this call and their contributions are highly appreciated. Thanks are also due to the Coatings administration team for their efficient and excellent service, and for producing this professional publication.

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Photovoltaic Characteristics of CH₃NH₃PbI₃ Perovskite Solar Cells Added with Ethylammonium Bromide and Formamidinium Iodide

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Abstract: Photovoltaic characteristics of solar cell devices in which ethylammonium (EA) and formamidinium (FA) were added to CH₃NH₃PbI₃ perovskite photoactive layers were investigated. The thin films for the devices were deposited by an ordinary spin-coating technique in ambient air, and the X-ray diffraction analysis revealed changes of the lattice constants, crystallite sizes and crystal orientations. By adding FA and EA, surface defects of the perovskite layer decreased, and the photoelectric parameters were improved. In addition, the highly (100) crystal orientations and device stabilities were improved by the EA and FA addition.

Keywords: perovskite solar cells; ethlammonium; formamidinium; microstructure

1. Introduction

Organic-inorganic perovskite solar cells provide photoelectric conversion in wide wavelength ranges and exhibit excellent photovoltaic properties [1–6]. Since the film of CH₃NH₃PbI₃ (MAPbI₃) can be formed by a spin-coating method, there is an advantage that the production process is easy and low cost. In spite of these merits, there is a serious problem that the stability is extremely low. In order to solve this problem, research and development of devices with higher power conversion efficiency and stability using formamidinium (FA) [7–13], guanidinium [14,15] or alkali metal [16–21] doped perovskites for the methylammonium (MA) site have been conducted.

There also exists research and development of devices with ethylammonium (EA) added to perovskites [22–26]. EA has a larger ionic radius (2.74 Å) than that of MA (2.17 Å), and the addition of EA can be expected to improve stability from the viewpoint of calculations [25,27] and tolerance factor [1]. In addition, there is a report that the thermal stability and crystallinity are higher than those of MA, and the addition of EA to the perovskites showed a surface coating with fewer defects and improves the stability of the device [23,28]. However, it should be noted that excessive addition of EA leads to phase separation, a decrease in crystallinity, and precipitation of PbI₂ as an impurity [29,30].

The purpose of this study is to examine the microstructures and photovoltaic characteristics of FA and EA co-added CH₃NH₃PbI₃ perovskite solar cells. The stability of a MAPbI₃ perovskite structure might be predicted by calculating the tolerance factor (*t*-factor) [31–35], which is given by $t = \frac{r_{MA}+r_1}{\sqrt{2}(r_{Pb}+r_1)}$, where *r* is an ionic radius [36]. When the *t*-factor is in the range of 0.81–1.1, perovskite structures could be formed [35]. If the *t*-factor is adjusted to 1.0, perovskite structures with cubic symmetry could be realized. The ionic radii of MA⁺, FA⁺, EA⁺, Pb²⁺, I⁻, Br⁻, and Cl⁻ are 2.17, 2.53, 2.74, 1.19, 2.20, 1.96, and 1.81 Å, respectively [35,36]. By adding FA⁺ and EA⁺ with larger ionic radii than MA⁺, *t*-factor gets closer to 1, and the stability is expected to be improved. In addition, EA addition is expected to promote the crystal growth and improve the stability of the device [23,28], and there are few reports on



simultaneous addition of FA and EA to the perovskite layer. The effects of the simultaneous addition to the perovskite compounds were analyzed by microstructural and photovoltaic characterization.

2. Materials and Methods

A cross-section and deposition process of the present perovskite solar cells is summarized and shown in Figure 1. A fluorine-doped tin oxide (FTO, Nippon Sheet Glass Company, Ltd., Tokyo, Japan) substrate was dipped and washed in an ultrasonic washing machine using acetone twice and methanol once, and cleaned with flowing N₂. The 0.15 and 0.30 M precursor solutions of TiO₂ were prepared from 0.055 and 0.11 mL titanium disopropoxide bis (acetyl acetonate) (Sigma Aldrich, Tokyo, Japan) and 1-btanol (1.0 mL, Nacalai Tesque, Kyoto, Japan). The solutions were cast on the transparent FTO, and spin-coated at 3000 rpm for 30 s and heat-treated at 125 °C for 5 min [37–39]. The processes with 0.30 M precursor solutions were repeated twice. In order to form a dense electron transport TiO₂, the deposited samples were annealed at 550 °C for 30 min. The mesoporous TiO₂ layer was deposited with TiO₂ nanoparticles (P-25, Aerosil, Tokyo, Japan) and polyethylene glycol (Nacalai Tesque, Kyoto, Japan) in ultrapure water. The solution was blended with acethylacetone (20 µL, Fujifilm Wako Pure Chemical Corporation, Osaka, Japan) and triton-X-1001 (10 µL, Sigma Aldrich, Tokyo, Japan) for 30 min, and allowed to stand for 24 h to remove bubbles from the mixed solution. The prepared TiO₂ mixed solution was spin-coated at 5000 rpm for 30 s and annealed at 550 °C for 30 min, and a mesoporous TiO₂ layer was formed.

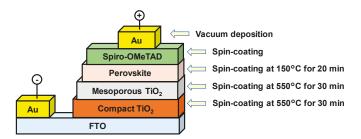


Figure 1. Cross-section of the cell and process conditions.

The perovskite precursor solutions were prepared as mixed solutions of methylamine hydroiodide CH_3NH_3I (MAI, 2.4 M, Tokyo Chemical Industry, Tokyo, Japan) and PbCl₂ (0.8 M, Sigma Aldrich, Tokyo, Japan) in *N*,*N*-dimethylformamide (DMF) (0.5 mL, Sigma Aldrich, Tokyo, Japan) at 60 °C for 24 h. This is used as a standard cell, and the amount of MAI was reduced by adding formamidine hydroiodide $CH(NH_2)_2I$ (FAI, Tokyo Chemical Industry, Tokyo, Japan), ethylamine hydrobromide $CH_3CH_2NH_3Br$ (EABr, Tokyo Chemical Industry, Tokyo, Japan), and ethylamine hydrochloride $CH_3CH_2NH_3CI$ (EACl, Tokyo Chemical Industry, Tokyo, Japan). Detailed compositions of the perovskite compounds are listed in Table 1, together with the *t*-factors. The perovskite precursor solutions were spin-coated at 2000 rpm for 60 s and applied an air-blowing method during spin-coating [40,41]. The device was annealed at 150 °C for 20 min in the ambient air.

The hole-transport layer was deposited by spin-coating. A chlorobenzene solution (0.5 mL) of 2,2',7,7'-tetrakis-(*N*,*N*-di-p-methoxyphenylamine)-9,9'-spirobifluorene (spiro-OMeTAD, Fujifilm Wako Pure Chemical, Corporation, Osaka, Japan, 36.1 mg) was prepared by mixing it for 12 h. An acetonitrile solution (0.5 mL) of lithium bis (trifluoromethylsulfonyl) imide (Li-TFSI, Tokyo Chemical Industry, Tokyo, Japan) was also prepared by mixing it for 12 h. A mixture solution of the spiro-OMeTAD solution with 4-tertbutylpridine (14.4 μ L, Sigma Aldrich, Tokyo, Japan) and Li-TFSI solution (8.8 μ L) was prepared by mixing it at 70 °C for 30 min. The spiro-OMeTAD layer was deposited by spin-coating at 4000 rpm for 30 s. After that, gold (Au) thin film electrodes were deposited as electrodes by vacuum evaporation. As investigated in the previous works [42–44], layer thicknesses of the compact TiO₂,

mesoporous TiO_2 + perovskite, spiro-OMeTAD, and Au layers were roughly estimated to be 40, 600, 50, and 200 nm, respectively.

Composition of Perovskite	EABr (%)	FAI (%)	t-Factor
MAPbI ₃	0	0	0.912
MA _{0.9} FA _{0.1} PbI ₃	0	10	0.919
MA _{0.8} FA _{0.2} PbI ₃	0	20	0.927
MA _{0.5} FA _{0.5} PbI ₃	0	50	0.949
MA _{0.8} FA _{0.1} EA _{0.1} PbI _{2.7} Br _{0.3}	10	10	0.933
MA _{0.75} FA _{0.2} EA _{0.05} PbI _{2.85} Br _{0.15}	5	20	0.933
MA _{0.7} FA _{0.2} EA _{0.1} PbI _{2.7} Br _{0.3}	10	20	0.940
MA _{0.6} FA _{0.2} EA _{0.2} PbI _{2.4} Br _{0.6}	20	20	0.954
MA _{0.75} FA _{0.2} EA _{0.05} PbI _{2.85} Cl _{0.15}	5	20	0.934
MA _{0.7} FA _{0.2} EA _{0.1} PbI _{2.7} Cl _{0.3}	10	20	0.941

Table 1. Compositions and calculated *t*-factors of the present perovskite compounds.

The light-induced current density voltage (*J*–*V*) curves of the fabricated devices were obtained by using air mass 1.5 illuminator (San-ei Electric XES-301S, 100 mW·cm⁻²) and a current-voltage apparatus (B2901A, Keysight, Santa Rosa, CA, USA). In addition, the external quantum efficiencies of the devices were obtained (QE-R, Enli Technology, Kaohsiung, Taiwan). Optical microscopy (Eclipse E600, Nikon, Tokyo, Japan) and X-ray diffraction (D2 PHASER, Bruker, Billerica, MA, USA) measurements were performed to analyze the surface morphologies and nanoscopic structures.

3. Results and Discussion

J–*V* curves collected in the light condition for the fabricated perovskite solar cells are displayed in Figure 2. Table 2 shows summarized parameters of the fabricated solar cells. A conversion efficiency (η) of the standard cell is 6.72%. The *J*_{SC}, *V*_{OC} and η were improved from 19.2 mA·cm⁻², 0.687 V and 6.72% to 21.5 mA·cm⁻², 0.922 V and 14.25% by addition of FA 20% at the MA site. When EA 10% and FA 10% were added simultaneously, the *J*_{SC}, *V*_{OC} and η increased 19.9 mA cm⁻², 0.946 V and 12.43%. Addition of EACl was also effective for the improvement of the device properties. Further addition of EA and FA would decrease the device performance.

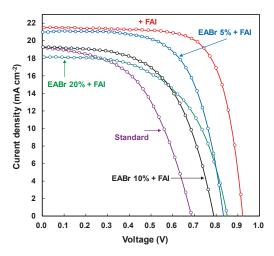


Figure 2. J–V characteristics collected in light condition for the fabricated solar cells.

Device	J _{SC} (mA·cm ^{−2})	V _{OC} (V)	FF	$R_{\rm S}$ ($\Omega \cdot \rm cm^2$)	$R_{\rm Sh}$ ($\Omega \cdot \rm cm^2$)	η (%)	η _{ave} (%)
Standard	19.2	0.687	0.509	8.8	337	6.72	6.35
+FAI 10%	21.8	0.816	0.574	6.2	1663	10.24	8.04
+FAI 20%	21.5	0.922	0.719	3.4	4839	14.25	13.66
+FAI 50%	15.7	0.926	0.712	4.7	13,545	10.36	10.31
EABr 10% + FAI 10%	19.9	0.946	0.660	6.1	4667	12.43	12.23
EABr 5% + FAI 20%	21.0	0.834	0.648	5.6	4952	11.33	10.63
EABr 10% + FAI 20%	19.3	0.789	0.572	5.7	1015	8.47	8.70
EABr 20% + FAI 20%	18.1	0.851	0.562	4.8	2340	8.68	8.27
EACl 5% + FAI 20%	20.4	0.879	0.618	6.4	1879	11.06	10.63
EACl 10% + FAI 20%	20.2	0.933	0.647	5.2	66,637	12.21	11.64

Table 2. Measured parameters of the cells fabricated in this study. J_{SC} : short-circuit current density. V_{OC} : open-circuit voltage. FF: fill factor. R_{S} : series resistance. R_{Sh} : shunt resistance. η : conversion efficiency. η_{ave} : averaged efficiency of three cells.

Figure 3 is the *J*–*V* curves of the fabricated photovoltaic cells after 4 weeks in ambient air, and the estimated parameters are shown in Table 3. The conversion efficiency of the standard cell was lowered to 5.69%. Co-addition of small amount of EA and FA to MAPbI₃ provided higher stability compared with the standard cells, as shown in Figure 4.

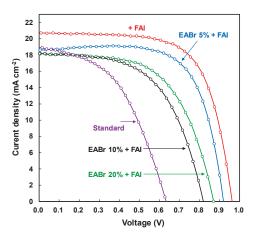


Figure 3. *J*–*V* characteristics collected in light condition for the fabricated solar cells after 4 weeks in ambient air without encapsulation.

Table 3. Measured photovoltaic parameters of the fabricated cells after 4 weeks.

Device	J _{SC} (mA·cm ⁻²)	V _{OC} (V)	FF	$R_{\rm S}$ ($\Omega \cdot {\rm cm}^2$)	$R_{\rm Sh}$ ($\Omega \cdot { m cm}^2$)	η (%)	η _{ave} (%)
Standard	19.0	0.633	0.474	8.9	212	5.69	5.25
+FAI 10%	17.3	0.925	0.615	8.7	5123	9.85	9.30
+FAI 20%	20.7	0.961	0.675	4.6	2455	13.43	13.30
+FAI 50%	14.8	0.964	0.684	6.0	75,968	9.74	8.99
EABr 10% + FAI 10%	17.3	0.925	0.615	8.7	5123	9.85	9.30
EABr 5% + FAI 20%	18.6	0.919	0.699	5.2	19,971	11.93	11.41
EABr 10% + FAI 20%	18.2	0.819	0.564	7.6	1129	8.39	6.86
EABr 20% + FAI 20%	18.2	0.870	0.585	6.6	946	9.26	8.77
EACl 5% + FAI 20%	17.3	0.900	0.682	5.1	4097	10.62	9.98
EACl 10% + FAI 20%	17.0	0.932	0.664	5.8	5407	10.54	9.49

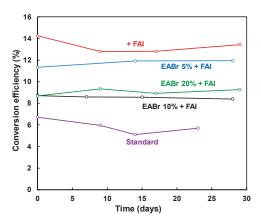


Figure 4. Stability measurements of the fabricated perovskite devices.

Optical microscopy images of the perovskites through spiro-OMeTAD are shown Figure 5. By adding EA and FA, surface defects of the perovskite layer decreased. Obtaining a perovskite layer with few defects enables efficient charge separation and charge extraction, which is thought to have led to improved device performance. In addition, defects in the perovskite layer are a cause of charge recombination, and it is considered that suppression of the defect has led to improvement in stability.

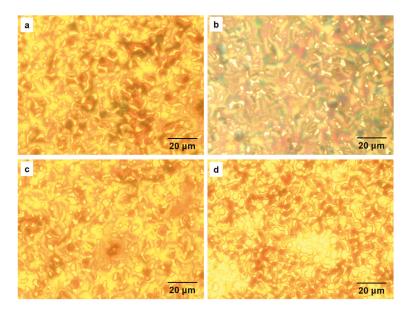


Figure 5. Optical microscopy images of cells with the compositions of (**a**) FAI 20%, (**b**) EABr 5% + FAI 20%, (**c**) EABr 10% + FAI 20%, and (**d**) EABr 20% + FAI 20%.

External quantum efficiency (EQE) spectra of the fabricated photovoltaic cells are shown in Figure 6. The band gap energies (E_g) were estimated from EQE spectra around 800 nm by linear fitting using band gap calculator software (Enli Technology, QE-R), and the measured band gap energies of the perovskite compounds increased from 1.54 to 1.57 eV by adding EA. The E_g value of the 20% EABr-added perovskite crystals was wider than that of the 20% FAI-added perovskite. The EQE values

of the EABr-added device was lower between 350 and 750 nm than that of the FAI-added device, which led to a decrease of the J_{SC} values.

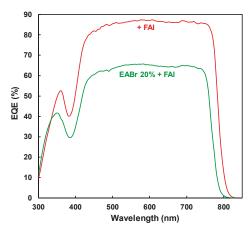


Figure 6. External quantum efficiency spectra of the fabricated solar cells.

X-ray diffraction (XRD) patterns of the fabricated cells added with EABr and FAI are shown in Figure 7a. Increases of (100) and (200) diffraction reflections are observed by adding FAI or EABr. In addition, only (100) and (200) peaks are observed, which indicates that the cells exhibited highly oriented (100) perovskite crystals by the air-blowing method [40].

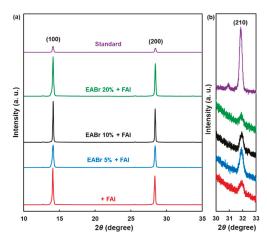


Figure 7. (a) X-ray diffraction (XRD) pattern of the present solar cells and (b) enlarged pattern of (a).

Microstructural parameters of the present perovskite compounds are listed in Table 4. The lattice constants of the FAI-added perovskites were higher compared with the standard MAPbI₃ material, whereas those of the EABr and FAI co-added perovskite decreased. Crystallite sizes were estimated from the (200) reflections, and they increased by the addition of FAI and EABr. The I_{100}/I_{210} intensity ratios of (100) reflections (I_{100}) to (210) reflections (I_{210}) were measured from the XRD data in Figure 7a,b, and the results are shown in Table 4. If the CH₃NH₃PbI₃ cubic perovskite particles are randomly oriented, then the I_{100}/I_{210} value should be 2.08 [35]. For the standard cell prepared in the present study, the I_{100}/I_{210} is 48, which means the (100) crystal surfaces of the cubic structures are strongly

aligned in the solar cell. By the addition of FAI to the perovskite compounds, I_{100}/I_{210} was increased to 1694, and the I_{100}/I_{210} increased further to 1939 by adding EABr. This is 40 times higher than the I_{100}/I_{210} of the standard perovskite device.

Perovskites	Lattice Constant a (Å)	Crystallite Size D ₂₀₀ (Å)	Orientation I ₁₀₀ /I ₂₁₀
Standard	6.274(1)	479	48
+FAI 20%	6.286(1)	647	1694
EABr 5% + FAI 20%	6.281(0)	528	460
EABr 10% + FAI 20%	6.283(1)	1506	1155
EABr 20% + FAI 20%	6.280(2)	830	1939

Table 4. Microstructural parameters for the perovskite crystals. Preferred crystal orientations were indicated with ratios of 100 diffraction intensities (I_{100}) to 210 diffraction intensities (I_{210}).

A schematic model showing molecular structures (MA, FA, and EA) and the lattice structure of the FAI and EABr added perovskites is shown in Figure 8a,b, respectively. The lattice constant *a* of 6.315 Å for a perovskite single crystal [35,45] is greater compared with the *a* of the perovskite compound in a cell configuration [46,47]. If the perovskite particles were synthesized and deposited on the mesoporous TiO₂ layer, some of the CH₃NH₂ molecules might be desorbed. Then, MA vacancies could be formed, and the lattice constant (6.274 Å) of MAPbI₃ is smaller than that of single crystal, as listed in Table 4. When FAI was added to the standard MAPbI₃, the FA would occupy the defects and MA sites, and the lattice constant increased to 6.286 Å, as shown in Figure 8b and Table 4. As the size of Br⁻ is fairly small compare with that of I⁻, *a* values of the EABr-added crystals decreased to 6.280 Å compared with FAI-added perovskite crystals, as indicated by arrows in Figure 8b. Combination of the present EA/FA with other molecules [15,48] and alkali metals [21,49] might also be effective for the stabilization of the perovskite compounds.

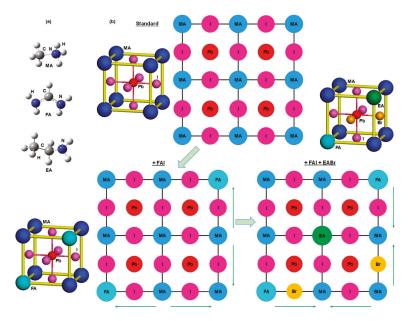


Figure 8. Structures of (**a**) methylammonium (MA), formamidinium (FA), ethylammonium (EA) and (**b**) the present perovskite compounds.

4. Conclusions

Solar cells using perovskite in the photoactive layer were produced by using spin-coating technique in ordinary air, and the influence on photovoltaic characteristics by adding EA and FA to the perovskite phase was investigated. From the results of J-V characteristics, the addition of EA and FA improved V_{OC} and FF, leading to an improvement in photoelectric conversion efficiency. Devices with EA and FA added maintained photoelectric conversion efficiencies even after 4 weeks compared to that of the standard device. Optical microscope results showed surface improvement, and X-ray diffraction results showed FA and EA substitution at MA position of the perovskite. By substituting FA and EA, which have larger ionic radii than MA, the perovskite structures would have more stable cubic structures with higher stability.

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Effect of Thioacetamide Concentration on the Preparation of Single-Phase SnS and SnS₂ Thin Films for Optoelectronic Applications

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Abstract: Eco-friendly tin sulfide (SnS) thin films were deposited by chemical solution process using varying concentrations of a sulfur precursor (thioacetamide, 0.50–0.75 M). Optimized thioacetamide concentrations of 0.6 and 0.7 M were obtained for the preparation of single-phase SnS and SnS₂ films for photovoltaic absorbers and buffers, respectively. The as-deposited SnS and SnS₂ thin films were uniform and pinhole-free without any major cracks and satisfactorily adhered to the substrate; they appeared in dark-brown and orange colors, respectively. Thin-film studies (compositional, structural, optical, and electrical) revealed that the as-prepared SnS and SnS₂ films were polycrystalline in nature; exhibited orthorhombic and hexagonal crystal structures with (111) and (001) peaks as the preferred orientation; had optimal band gaps of 1.28 and 2.92 eV; and exhibited p- and n-type electrical conductivity, respectively. This study presents a step towards the growth of SnS and SnS₂ binary compounds for a clean and economical power source.

Keywords: tin monosulfide; tin disulfide; chemical solution process; absorber; buffer; solar cells; renewable energy

1. Introduction

In recent years, inorganic semiconductors have been employed to generate clean energy in various optoelectronic and electrochemical fields, mainly because of their high stability under atmospheric conditions [1–5]. Among these, groups IV–VI tin-based binary sulfides such as tin monosulfide (SnS) and tin disulfide (SnS₂) have drawn much attention because of their abundance, low cost, non-toxicity, high catalytic activity, material diversity, structural multiformity, and excellent electrical conductivity [6]. SnS crystallizes in an orthorhombic structure with the Pnma space group [7] and exhibits excellent optoelectrical properties such as a strong absorption coefficient (> 10⁵ cm⁻¹) with direct optical band gap energy ranging from 1.16 to 1.79 eV [8,9] and p-type conductivity with a carrier concentration of the order of 10^{11} – 10^{18} cm⁻³ [10], which are suitable for thin-film photovoltaic absorbers. In addition, maintenance of stoichiometry is simpler compared with the other conventional light absorbers [11–15]. Another tin-based binary sulfide, SnS₂, adopts a hexagonal-layered structure with the P3ml space group, similar to the structure of the CdI₂ system [16]. Moreover, SnS₂ has a relatively high optical band gap in the range of 2.04–3.30 eV [17] with direct transitions and exhibits n-type conductivity. These promising characteristics make SnS a suitable absorber candidate material



for thin-film solar cells [1]; moreover, SnS is presumably expected to be a better alternative to the already developed technologies such as Cu(In,Ga)Se₂ (23.35%) [18] and CdTe (22.1%) [19], which are limited by their toxicity, scarcity, and exorbitant cost. Similarly, the favorable electronic characteristics, excellent structural flexibility, wider spectral response, and better thermal stability of SnS₂ make it a competitive nontoxic substitute for the conventional CdS [14] and Zn(O,S) [20] buffers in thin-film solar cells [2]. Furthermore, both SnS and SnS₂ have also been applied in photodetectors [21,22], photocatalysis [23], water splitting [24], gas sensors [25,26], biosensors [27], field-effect transistors [28,29], lithium-sodium ion batteries [30,31], thermoelectrics [32], electrochemical capacitors [33], and supercapacitors [34].

Various approaches including physical and chemical techniques have been explored to deposit both SnS and SnS₂ thin films. Among these techniques, the chemical solution process (CSP) or chemical bath deposition (CBD) offers more inexpensive and flexible depositions. The preparation of single-phase SnS and SnS₂ films by CSP depends on the release and reaction rate of sulfur ions in the reaction solution, which can be controlled by the selection of a suitable sulfur precursor at a concentration, which affects not only the formation of the phase but also the growth rate, thickness, and other physical properties of the product films. Therefore, optimizing the concentration of the sulfur precursor is highly preferable to obtain high-quality SnS and SnS₂ films for the desired applications. Previous research suggests that thioacetamide (TA) and sodium thiosulfate have been mainly used as sulfur precursors since 1987 (Figure 1). Of these, thioacetamide is more preferable because it works under both acidic and alkaline bath conditions.

Therefore, a set of SnS thin films were deposited by CSP using varying thioacetamide concentrations, while the other growth parameters were maintained constant. The influence of thioacetamide concentration on the growth and physical properties of the thin films are discussed in the subsequent sections. Thus, its concentration was optimized for the preparation of pure SnS and SnS₂ films for wide applications.

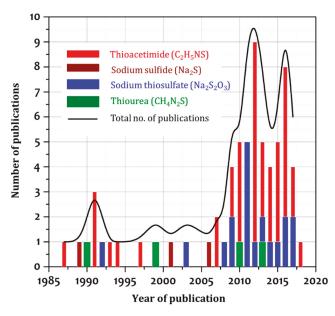


Figure 1. The number of chemical bath deposition (CBD) SnS reports on the usage of different sulfur precursors from 1980 to the present.

2. Experimental Section

The deposition procedure for SnS and SnS₂ films by CSP is schematically presented in Figure 2, and the process has been described in detail in our previous reports [35,36]. Analytical-grade tin chloride (SnCl₂.2H₂O, 0.1 M) and tartaric acid (C₄H₆O₆, 1.2 M) were used as a tin source and complexing agent, respectively, and 10 mL of thioacetamide (C₂H₅NS, 0.50-0.75 M) was used as the source material for the S ions. The as-prepared thin films were cleaned using deionized (DI) water and dried in a vacuum oven. By the following equations, the kinetics of SnS and SnS₂ films can be understood.

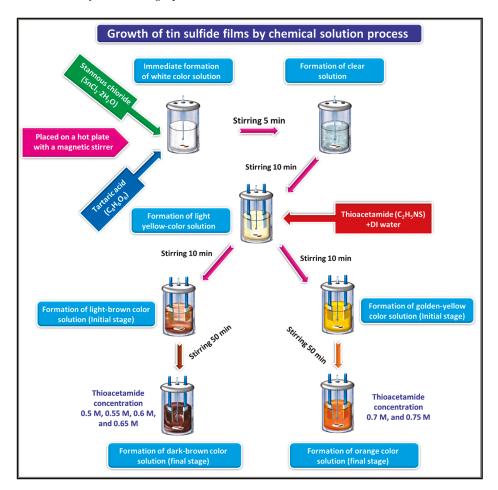


Figure 2. Schematic representation of the growth of tin sulfide films.

In an aqueous tin chloride solution, the complexation of tartaric acid is

$$\operatorname{SnCl}_2 \cdot 2\operatorname{H}_2\operatorname{O} + \operatorname{L} \Leftrightarrow \operatorname{Sn}(\operatorname{C}_4\operatorname{H}_6\operatorname{O}_6)^{2+} + 2\operatorname{Cl}^- + 2\operatorname{H}_2\operatorname{O}_6$$

The free Sn^{2+} ions are slowly released by the dissociation of tin tartrate ions ($Sn(C_4H_6O_6)^{2+}$) in a controlled way, as below:

$$\operatorname{Sn}(\operatorname{C}_4\operatorname{H}_6\operatorname{O}_6)^{2+} \rightleftharpoons \operatorname{Sn}^{2+} + \operatorname{C}_4\operatorname{H}_6\operatorname{O}_6.$$

The hydrolysis of thioacetamide can produce S²⁻ ions by

$$\begin{split} CH_3CSNH_2 + H_2O \rightleftharpoons CH_3CONH_2 + H_2S, \\ H_2S + H_2O \rightleftharpoons H_3O^+ + HS^-, \\ HS^- \rightleftharpoons H^+ + S^{2-}, \\ HS^- + OH^- \rightleftharpoons H_2O + S^{2-}. \end{split}$$

When the thioacetamide concentration is changed, multiphase or other single-phase films can be formed by the following reactions:

$$\operatorname{Sn}^{2+} + \operatorname{S}^{2-} \to \operatorname{SnS},$$

 $\operatorname{3SnS} + \operatorname{S} \to \operatorname{SnS} + \operatorname{Sn}_2\operatorname{S}_3,$
 $\operatorname{Sn}_2\operatorname{S}_3 + \operatorname{S} \to \operatorname{2SnS}_2,$

The compositional, structural, optical, and electrical characteristics of the as-deposited films were analyzed using an X-ray photoelectron spectrometer (Waltham, MA, USA) (XPS: A VG Multilab 2000; Al K α radiation = 1486.6 eV), X-ray diffractometer (Almelo, Overijssel, Netherlands) (XRD: PANalytical X'Pert PRO MPD, Malvern Panalytical with Cu K α radiation, λ = 1.5406 Å), UV-Vis-NIR spectrometer (Santa Clara, CA, USA) (Aglient), and Hall measurement system (Anyang-city, Gyeonggi-do, South Korea) (ECOPIA HMS-3000VER), respectively.

3. Results and Discussion

All the deposited tin sulfide films were confirmed to be satisfactorily adherent. The films appeared in dark-brown and orange shades at TA concentration ranges of 0.50–0.65 M and 0.70–0.75 M, respectively. The effect of TA concentration on the elemental composition and chemical states of elements was investigated by XPS. The XPS survey spectrum indicated that the deposited films were mainly composed of the Sn 3d doublet along with the S 2p peaks, representing the existence of the elements Sn and S. A high-resolution scan of the Sn 3d and S 2p peaks is shown in Figure 3a,b, respectively.

The Sn 3d doublet in the films grown with lower TA concentrations (0.5–0.6 M) showed two strong peaks at about 485.6 and 494.1 eV that were related to Sn $3d_{5/2}$ and Sn $3d_{3/2}$, respectively, which are the characteristics of Sn^{2+} in SnS. The Sn $3d_{5/2}$ and Sn $3d_{3/2}$ peaks were observed to expand at a TA concentration of 0.65 M, and the deconvolution of these peaks reveals the existence of two humps in each peak, linked to the elevated intensity for Sn^{2+} and low intensity for Sn^{4+} , indicating the coexistence of secondary Sn₂S₃ along with SnS. As the TA concentration was increased further (0.7 M), the spectra showed the binding energies for Sn $3d_{5/2}$ and Sn $3d_{3/2}$ as 486.7 (487.2) and 494.9 (495.1) eV, respectively [37,38], revealing the presence of Sn⁴⁺ produced in the SnS₂ phase. Beyond this concentration (0.75 M), the deconvolution of the broadened Sn 3d doublets suggests the presence of low intense Sn^{2+} and high intense Sn^{4+} , confirming the formation of the Sn_2S_3 secondary phase along with SnS₂. The high-resolution XPS spectrum of S 2p for the as-prepared films exhibited single peaks related to $S^{2-}-Sn^{2+}$ (161.3 eV) and $S-Sn^{4+}$ (162.3 eV) bonds at TA concentrations of 0.5–0.6 and 0.7 M, which are characteristic of single-phase SnS and SnS₂ films, respectively [35]. The remaining core-level S 2p spectra (for TA = 0.65 and 0.75 M) showed two deconvoluted peaks related to the binding energies of both $S^{2-}-Sn^{2+}$ (161.3 eV) and $S-Sn^{4+}$ (162.3 eV) bonding, suggesting the presence of the Sn_2S_3 secondary phase. The Sn/S atomic ratio varied between 1.12 to 0.53 with the change in TA concentration. The lower Sn/S atomic ratio indicated that S is more dominant at higher TA values. This excess of sulfur probably led to the formation of the binary phases, SnS₂ and Sn₂S₃ along with the SnS phase, which were further observed in the XRD studies. The film grown at TA concentrations of 0.6 M and 0.7 M exhibited Sn/S atomic ratios of 0.98 and 0.51, indicating that the films have a clear stoichiometry for the formation of the pure SnS and SnS₂ phases, respectively.

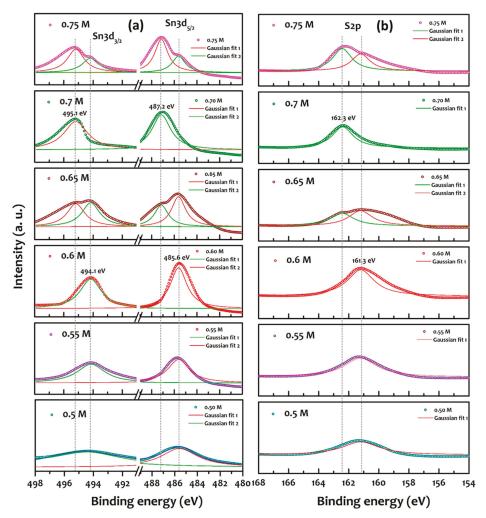


Figure 3. High-resolution X-ray photoelectron spectrometer (XPS) scan of (a) Sn 3d and (b) S 2p core levels.

In general, the structural properties of the thin films were observed to be highly influenced by the compositional variations in the film. In this study, the structural behavior of SnS films grown using different TA concentrations was analyzed using XRD. The diffraction patterns (Figure 4) confirmed the polycrystalline nature of the as-prepared films; some of these showed various binary phases, depending upon the TA concentration: the films deposited in the TA concentration range of 0.5-0.6 M exhibited a strong peak at $2\theta = 31.6^{\circ}$, which is related to the (111) plane, along with other minor peaks at around $2\theta = 27.1^{\circ}$, 38.8° , and 51.1° , which were assigned to the diffraction from the (101), (131), and (112) planes of orthorhombic SnS (JCPDS Card No. 39-0354) [39], respectively. Moreover, the crystalline state improved with an increase in the TA concentration. As the TA concentration was increased to 0.55 M, the film exhibited additional planes of (130) and (260) related to the Sn₂S₃ binary phase (JCPDS Card No. 14-0619) [40]; as the TA concentration was further increased to 0.7 M, the film exhibited different diffraction planes of hexagonal SnS₂ (JCPDS Card No. 23-0677) [41] with (001) reflection at 15.02° as the preferred orientation; and beyond this TA concentration (0.75 M), the film

additionally exhibited (130), (260), and (540) planes of the secondary Sn_2S_3 phase along with SnS_2 . Therefore, the films deposited under TA concentrations of 0.6 and 0.7 M exhibited good crystalline and pure orthorhombic SnS (111) and hexagonal SnS₂ (001) phases, respectively. Thus, these results are observed to agree well with the XPS observations.

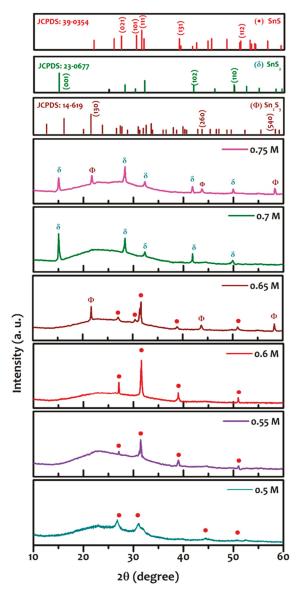


Figure 4. XRD patterns of the films deposited at different TA concentrations.

The average crystallite size, D, of the deposited films was estimated using the Debye–Scherrer formula [42] using the strong (1 1 1) and (0 0 1) peaks of the deposited films with a TA concentration in the range of 0.5-0.65 M and 0.7-0.75 M, respectively. It was found that the crystal size varied from

15 to 29 nm with the change of TA concentration from 0.5 to 0.65 M. In addition, a D of 26 nm was obtained for the film deposited at a concentration of 0.7 M, and it was decreased to 24 nm for a further increase in TA concentration to 0.75 M. Therefore, the D of the SnS (TA = 0.6 M) and SnS₂ (0.7 M) films was obtained as 29 nm and 26 nm, respectively. The surface morphology and surface average grain size of both SnS (TA = 0.6 M) and SnS₂ (0.7 M) films were obtained from SEM images (Figure 5). Both the films showed compact morphology without pin-holes and cracks. The SnS film showed almost elliptical-shaped grains with an average grain size of ~295 nm, whereas the SnS₂ film showed shuttle-shaped grains of nearly 272 nm in size.

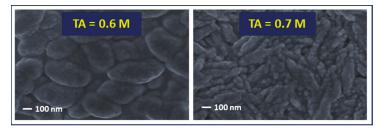


Figure 5. SEM surface images of both SnS and SnS₂ films deposited at thioacetamide (TA) concentrations of 0.6 and 0.7 M, respectively.

The optical studies of the films deposited at different TA concentrations were carried out using the UV-Vis-NIR photo spectrometer. The films deposited at TA concentrations in the range of 0.5–0.6 and 0.7 M exhibited a sharp absorption edge in the absorption spectra, whereas at TA concentrations of 0.65 and 0.75 M, the films exhibited a nonlinear fall in the absorption edge, indicating the potential presence of the secondary phase of Sn₂S₃ along with either the SnS or SnS₂ phase. The band gap of the prepared films was estimated from the Tauc plots $((\alpha h \nu)^2 vs. h \nu)$ [43], as shown in Figure 6. The films deposited at concentrations of 0.6 and 0.7 M are observed to exhibit band gaps of 1.28 and 2.92 eV, respectively, corresponding to the energy gaps of the SnS and SnS₂ phases. Furthermore, the films prepared at a 0.65 M concentration exhibited two different values of band gap—specifically, ~0.94 and ~1.34 eV—that are attributed to the presence of the Sn₂S₃ secondary phase along with SnS; on the other hand, at a concentration of 0.75 M, the films exhibited band gaps of ~1.11 and ~2.53 eV, corresponding to the presence of the Sn₂S₃ secondary phase and SnS₂ phase, respectively.

Figure 7 shows the variation of the refractive index (n) and extinction coefficient (k) as a function of the TA concentration. The evaluated n value is observed to first increase and then decrease with increasing TA concentrations up to 2 M, whereas the calculated k value exhibits a reverse variation trend. The films grown at TA concentrations of 0.6 and 0.7 M exhibit n values of 3.24 and 2.63 and k values of 0.13 and 0.61, respectively. The obtained n and k values in the present study are in good agreement with the reported values [2,44].

Electrical parameters such as conductivity type, resistivity, mobility, and carrier density of the films deposited at various TA concentrations were determined using Hall effect studies. The positive sign of the Hall coefficient for the films prepared at TA concentrations in the range of 0.50–0.65 M indicates p-type electrical conductivity, whereas the negative sign for the films deposited at TA concentrations of 0.7 and 0.75 M suggests n-type electrical conductivity. Furthermore, the films deposited at concentrations of 0.6 and 0.7 M exhibited carrier densities of 4.1×10^{15} and 7.2×10^{19} cm⁻³; mobilities of 62.3 and 32.4 cm²V⁻¹s⁻¹; and resistivities of 29.2 and 17.4 Ω -cm, respectively, which are related to the SnS and SnS₂ phases. These results are in agreement with the reported data [45,46].

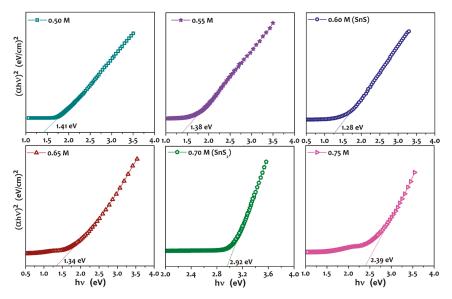


Figure 6. Tauc's plots of the films deposited at different TA concentrations.

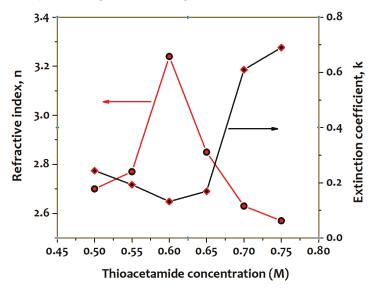


Figure 7. Variation of n and k with TA concentrations.

4. Conclusions

In this study, SnS thin films were prepared using chemical solution process by varying the concentration of TA (0.5–0.75 M), while the other growth parameters were maintained constant. The films prepared at TA concentrations of 0.6 and 0.7 M exhibited Sn/S atomic ratios of 0.98 and 0.51, confirming the formation of single SnS and SnS₂ phases, respectively. The XRD studies showed that all deposited films were polycrystalline in nature and exhibited various binary phases depending upon the TA concentration. The films deposited at a TA concentration of 0.6 M exhibited a pure orthorhombic SnS phase, whereas those at 0.7 M concentration exhibited a completely hexagonal SnS₂

phase. In addition, they showed the direct optical band gap of 1.28 and 2.92 eV with p- and n-type conductivities, which confirmed the suitability of these films not only for application as solar absorbers and buffers, respectively, but also for other applications.

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Article PL Study on the Effect of Cu on the Front Side Luminescence of CdTe/CdS Solar Cells

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Abstract: The effect of Cu on highly efficient CdTe thin solid film cells with a glass/TCO/CdS/CdTe structure subjected to CdCl₂ treatment was investigated by low-temperature photoluminescence (PL). The PL of the CdS/CdTe junction in samples without Cu deposition revealed a large shift in the bound exciton position due to the formation of $CdS_{x}Te_{1-x}$ alloys with E_{g} (alloy) \cong 1.557 eV at the interface region. After Cu deposition on the CdTe layer and subsequent heat treatment, a neutral acceptor-bound exciton (A^{0}_{Cu} ,X) line at 1.59 eV and two additional band-edge peaks at 1.54 and 1.56 eV were observed, indicating an increase in the energy gap value in the vicinity of the CdTe/CdS interface to that characteristic of bulk CdTe. These results may suggest the disappearance of the intermixing phase at the CdTe/CdS interface due to the presence of Cu atoms in the junction area and the interaction of the Cu with sulfur atoms. Furthermore, an increase in the intensity of CdS-related peaks in Cu-doped samples was observed, implying that Cu atoms were incorporated into CdS after heat treatment.

Keywords: photovoltaic; CdTe; CdS; solar cell; luminescence; spectroscopy

1. Introduction

The low-temperature photoluminescence (PL) of CdTe single crystals has been intensively studied in the past [1,2]. It is very well known that the typical low-temperature spectrum of undoped single-crystal CdTe consists of bands assigned to the recombination of free excitons (FX), bound excitons (AX or DX), free-to-bound transitions (FB), and donor–acceptor pair (DAP) transitions. Fewer low-temperature PL studies have been conducted for polycrystalline CdTe, which has been established as a very promising photovoltaic material for thin film solar cells [3,4]. A typical CdTe solar cell consisting of a CdS/CdTe layer grown on a SnO₂/glass substrate is based on recombination within an n-CdS/p-CdTe heterojunction. Despite a 9.7% lattice mismatch occurring between the hexagonal CdS and the cubic CdTe, high-efficiency devices result from this junction, probably due to interdiffusion at the CdS/CdTe interface [5–8]. The S may passivate the grain boundaries and relieve the lattice mismatch between CdS and CdTe, thereby reducing recombination and improving device performance.

It is very well known that the post-deposition $CdCl_2$ annealing step is required to make reasonably efficient CdTe solar cells. It has been suggested that the $CdCl_2$ treatment enlarges grains, causes recrystallization, and enhances the diffusion of S from CdS into CdTe at the interface [2,7]. Additionally, the presence of chlorine dopants creates new recombination centers that may affect the recombination processes of photogenerated electron–hole pairs. It has been reported that the $CdCl_2$ treatment introduces two very important chlorine related defects, such as chlorine substituting on a tellurium site (Cl_{Te}) donor center and a V_{Cd} - Cl_{Te} (A) acceptor center that can be identified in the PL spectrum [1,5,9,10].

It was found recently that further improvement of CdTe solar cell can be achieved by Cu doping [11–16]. Cu enters the CdTe interstitially forming a shallow donor, Cu_i centers and gives rise to deep acceptor Cu_{Cd} centers via substitution [12–15].

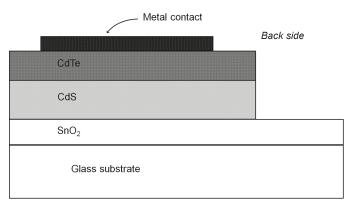
In this paper, results of studies on the effect of Cu doping on the low-temperature front side PL of CdS/CdTe solar cells will be presented.

2. Experimental Design

2.1. Film Deposition and Cell Fabrication

Cadmium telluride solar cells were fabricated in the superstrate configuration with the structure: glass/TCO/n⁺-CdS/p-CdTe/graphite/metal back contact in our laboratory (CNBM Center). Commercially available soda-lime glass coated with SnO₂:F/HRT was used as a substrate for the depositions. CdS (~80 nm in thickness) was deposited by chemical bath deposition (CBD) at 88 °C using cadmium chloride, thiourea, ammonium acetate, and ammonia, followed by annealing at 400 °C. CdTe (6–10 µm in thickness) was deposited by close-spaced sublimation (CSS) at $T_s = 600$ °C using graphite susceptors in 10–15 Torr He/O₂. The CdTe was then soaked in CdCl₂/methanol at 80 °C, followed by a furnace anneal under controlled conditions (380 °C, He/O₂, 300 Torr) in order to improve the CdTe structure and minority carrier lifetime. To form the back contact, a nitric-phosphoric (NP) acid etch was used to remove the surface oxide, and a very thin layer of Cu was evaporated. The efficiency of the cells examined in this work was in the range of 10%–11%. The overall process is described in [17].

A schematic of a typical CdS/CdTe solar cell is shown in Figure 1.



Front side

Figure 1. The glass substrate represents the front side of a solar cell and the CdTe layer represents the backside of a solar cell. The glass substrate, SnO₂, and CdS layers are transparent to a 658 nm line that is absorbed only by the CdTe film at the interface (junction luminescence).

2.2. Photoluminescence Measurements

The PL spectra were measured for undoped and Cu-doped CdTe/CdS cells produced from the CdTe source with a purity of 99.999% (5N) or 99.9999% (7N) and illuminated by monochromatic light directed onto the backside or front side of the solar cell structure. All measurements were performed on CdCl₂-treated cell structures, but before the deposition of the back contact.

For the backside PL, the measurements were taken by illuminating the CdTe/CdS cells with a 658 nm line generated by a red laser diode (LPM658, Newport, Irvine, CA, USA). For the front side luminescence, in addition to red excitation, a blue line with a wavelength of 405 nm (laser diode LQA405-8SE, Newport, Irvine, CA, USA) was also used. In Cu-doped samples, Cu was introduced to the cell through diffusion at 400 °C from a layer of pure metal deposited on the CdTe after chlorine treatment. The thickness of the copper layer was 10 nm. All of the samples used for PL measurements were placed in a closed-cycle cryostat with a controlled temperature ranging from 10 to 300 K. Spectra

were recorded using a grated monochromator coupled to a cooled photomultiplier tube (R106999, Hamamatsu, Tokyo, Japan).

3. Experimental Results and Discussion

3.1. Optical Characterization of the CdS/CdTe Solar Cells

In Figure 2, the results of the backside PL excited by 658 nm light are shown for two different CdS/CdTe samples. One sample was a solar cell grown in the NREL laboratory (Golden, Colorado, USA) and kindly supplied to us for testing. The second sample was grown in the CNBM Center using the same methodology used to generate solar cell devices with an efficiency of about 11%. As can be seen in Figure 2, the spectra obtained from both samples were similar. The presence of an excitonic band with a maximum at 1.59 eV indicated good-quality CdTe polycrystalline films in both samples. In both samples, defect-related peaks observed at around 1.44 eV were recorded. The defect-related peaks were assigned to DAP transitions between the Cl_{Te} donor centers and the A acceptor centers [1,10]. The origin of the peaks between 1.55 and 1.50 eV in both samples is still under discussion. A similar emission behavior was reported by other authors [1,10] who assigned bands in this region to DAP transitions (1.56 eV) and free electron–acceptor (e, A^0) transitions (1.54 eV).

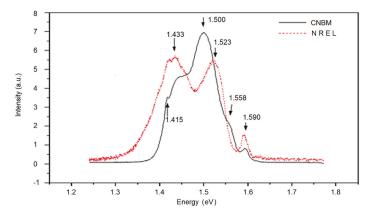


Figure 2. Backside luminescence (10 K) of CdS/CdTe solar cells grown in the NREL laboratory and CNBM New Energy Materials Research Center, respectively.

3.2. Front Side Luminescence of CdS/CdTe Structure Excited by a 658 nm (1.88 eV) Line

For front side luminescence, solar cells were illuminated from the front side of the device consisting of glass covered by TCO and a CdS window transparent to excitation light of 658 nm. However, the excitation light was strongly absorbed by the CdTe layer. Due to the high absorption, the generation of free electron–hole pairs and their subsequent separation or recombination occurred exclusively in a very narrow layer of the CdTe adjacent to the CdS/CdTe interface. Front side PL, called junction luminescence, gives us direct information about processes occurring in this area.

3.2.1. Front Side Luminescence of an Undoped CdS/CdTe

Figure 3 shows the PL spectrum obtained for the undoped CdS/CdTe structure excited from the junction side through the glass. The backside PL spectrum obtained for the same sample is shown for comparison. The junction PL of undoped CdS/CdTe structures has been reported by several investigators [10,11,18,19] and results similar to ours were obtained. The front side spectrum consists of two peaks at 1.53 and 1.43 eV; the high-energy peak at 1.59 eV detected in the backside spectrum is not present. There are two possible explanations for this observation. One possibility is to assume

that the origin of the 1.53 eV peak in the junction PL and the 1.59 eV peak in the backside PL is the same, namely that they are both due to bound-exciton emission. The 73 MeV shift in the exciton peak towards a lower energy for the junction region can be attributed to the reduction of the bandgap due to the formation of the $CdS_{x}Te_{1-x}$ alloy at the interface described in [7–10]. The shift found in this paper is similar to that found in [19,20].

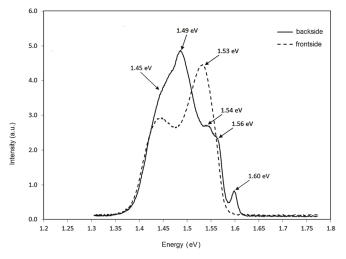


Figure 3. Photoluminescence (PL) spectra (10 K) from undoped CdS/CdTe solar cells excited from the backside (full line) and front side (dotted line) of the cell.

The alternative explanation is to assume that the excitonic band at 1.59 eV is depressed due to a high density in defects at the interface and that the 1.53 eV peak is equivalent to the broad free-to-bound peak around 1.56 eV detected in the same sample excited from the back. However, the analysis of the temperature dependence of the intensity of the 1.53 eV peak presented in the next section strongly favors the assertion of an excitonic origin of this peak.

3.2.2. Temperature Dependence of the 1.53 eV Peak

In order to further clarify the origin of the 1.53 eV peak found in the junction PL of the undoped sample, additional measurements of PL as a function of temperature were conducted. The analysis of the temperature dependence of the intensity of the 1.53 eV transition presented in Figure 4 shows a good fit with a two activation-energy model:

$$\frac{I(T)}{I(0)} = \frac{1}{1 + C_1 e^{\frac{-E_1}{kT}} + C_2 e^{\frac{-E_2}{kT}}}$$
(1)

proposed by Bimberg et al. [20] for the temperature decay of bound excitons. The activation energies E_1 and E_2 in this equation represent the electron–hole binding energy and the binding energy of the exciton to the impurity, respectively.

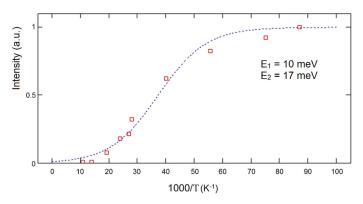


Figure 4. Temperature dependence of the PL intensity of the 1.53 transition in undoped cells along with the two-activation energy fit.

The binding energy of 10 meV is in good agreement with the binding energy of the free exciton [1], and it is reasonable to assume that the 17 meV point represents the binding energy of the exciton to the unidentified acceptor or the chlorine donor. The exciton position of 1.53 eV and the two binding energies, 0.01 and 0.017 eV, can be used to calculate the energy gap for CdS_xTe_{1-x} alloy [1]:

$$E_{\rm g} (\text{alloy}) = 1.53 + 0.01 + 0.017 = 1.557 \,\text{eV}$$
 (2)

Following the work of Ohata [21] and Pal [22], the composition of such alloy can be predicted using a simple quadratic equation:

$$E_{g(CdSxTe1-x)} = kx^{2} + (E_{g(CdS)} - E_{g(CdTe)} - k)x + E_{g(CdTe)}$$
(3)

Assuming k = 1.7 eV from [21] and substituting a 10 K bandgap for CdS ($E_{g (CdS)} = 2.59 \text{ e}$) and for that of CdTe ($E_{g (CdTe)} = 1.61 \text{ eV}$), the value $x \approx 0.08$ can be obtained.

3.2.3. Effect of Cu on the Front Side Luminescence of CdS/CdTe Solar Cells

The effect of Cu on the solar cell structure was studied by measuring the front side PL from a sample with a 10 nm Cu layer deposited on the CdTe side of the cell that was subjected to chlorine treatment, as described previously. After Cu deposition, the cell was annealed for 10 min at 400 °C. As can be seen from the Figure 5, in addition to peaks at 1.43 and 1.53 eV observed in the undoped samples, two new peaks at 1.595 and 1.56 eV were recorded in the Cu-doped samples. The following conclusions can be drawn from the comparison of the spectra taken for doped and undoped samples:

- The PL results show that Cu was present in the vicinity of the junction as a result of its migration from the backside of the solar cell during the post deposition annealing.
- The presence of peaks at maximums of 1.59 and 1.56 eV (absent in copper-free cells) indicated that the composition of the CdTeS alloy at the interface was dramatically changed due to Cu diffusion into the junction area. It has already been established [23,24] that the peak at 1.59 eV in Cu-doped CdTe corresponds to Cu_{Cd}-bound exciton.
- The position of the exciton peak can be used to estimate the value of the energy gap in the CdTe layer adjacent to the CdTe/CdS interface using the following relation: $h\omega_{\text{bound exciton}} = E_g E_B$. The value of E_g obtained from the junction luminescence of Cu-doped sample is essentially identical to the $E_g = 1.605$ of bulk CdTe in 10 K [25]. This indicates that the formation of the CdSTe alloy observed in undoped solar cells is suppressed by the presence of copper in the junction area.

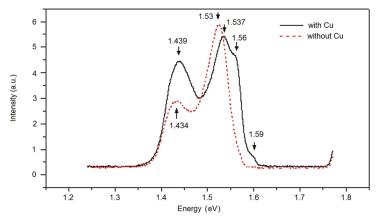


Figure 5. Front side luminescence of Cu-doped (full line) and undoped (dotted line) CdS/CdTe solar cells taken at 10 K.

It is worth noting that a similar effect has not been found in previously reported studies [11,18,19] of front side luminescence of Cu-doped CdTe/CdS solar cells. This may suggest that the Cu did not reach the junction area in those samples.

3.3. Front Side Luminescence of CdS/CdTe Structure Excited by a 405 nm (3.06 eV) Line

3.3.1. Front Side Luminescence of an Undoped CdS/CdTe Structure

Contrary to red light, blue light is strongly absorbed by the CdS layer. Therefore, it is reasonable to assume that the PL shown in Figure 6 is related mainly to emission from the CdS layer. In a high energy range, four peaks with maximal emission at 2.34, 1.92, 1.79 eV and a weak emission at 1.65 eV were recorded. Despite the extensive literature on the luminescence of polycrystalline thin film CdS, the interpretation of the observed PL bands may not be easy. The low-temperature PL strongly depends on the type of deposition and the post-deposition treatment [26,27]. According to the literature data [26], it is reasonable to assume that the emission at around 2.34 eV can be attributed to the excitons bound to substitutional Te atoms on the sulfur lattice site while the two bands at 1.79 and 1.65 eV may be due to a DAP transition involving Te complexes in the CdS. The peak at 1.92 eV had a similar position to what has been called a red band, ascribed to V_{Cd} - V_s defects [26].

In the low energy range, two strong peaks at 1.51 and 1.41 eV were detected. The origin of those peaks is not clear. They may be related to an emission from CdTe as the position of those peaks are similar to that recorded for the front side PL excited by red light. On the other hand, similar peaks were found in polycrystalline CdS grown on glass or TCO by chemical bath deposition [26], and were ascribed to the transition of electrons trapped in surface states to the valence band.

3.3.2. Effect of Cu on the Front Side Luminescence of CdS/CdTe Solar Cells

The effect of Cu doping on CdS luminescence has never been studied before. As can be seen from Figure 6, the intensity of all four high energy peaks increased significantly due to Cu doping but no peak shift was observed. This can be understood assuming that the Cu passes through the interface and diffuses into the CdS film, where it reacts with native CdS defects in such way that the number of nonradiative recombination events decreases. The decrease in the intensity of the peaks at 1.51 and 1.41 eV in doped samples suggests that those peaks are related to the CdS lattice rather than to the CdTe. The reduction of the intensity of the peaks can be ascribed to the reduction in the number of surface defects in the Cu-doped sample.

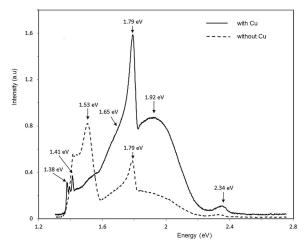


Figure 6. Front side luminescence (10 K) from Cu-doped (solid line) and undoped (dotted line) CdS/CdTe solar cells excited by the 405 nm line.

4. Conclusions

Low-temperature junction PL has been used to study the effect of Cu deposited on CdTe on the electronic structure of CdTe/CdS solar cells grown in our laboratory.

In undoped cells, good evidence for the interdiffusion of sulfur and bandgap reduction was found in CdTe/CdS solar cells subjected to CdCl₂ treatment. The energy gap of 1.557 eV was calculated and the composition of the interface alloy was estimated to be $x \approx 0.08$.

In Cu-doped samples, the junction PL data provides evidence that Cu diffuses into the junction area, forming Cu_{Cd} centers. The most interesting result of this work is the fact that the energy bandgap of CdTe at the interface restores its original value of about 1.60 eV. This allows us to suggest that the presence of Cu in the junction area hinders the interdiffusion of sulfur through the interface. If so, the effect of sulfur diffusion on the cell performance should be reexamined.

Finally, this is the first time that CU has been documented to diffuse through the interface into the CdS layer, changing the character of the recombination processes in the CdS.

Author Contributions: Conceptualization, H.O. and D.C.; Methodology, H.O.; Validation, H.O.; Formal Analysis, H.O. and D.C.; Investigation, D.C.; resources, Z.C.; Data Curation, H.O.; Writing—Original Draft Preparation, H.O.; Writing—Review and Editing, H.O., D.C. and Z.C.; Visualization, D.C. and H.O.; Supervision, K.C.; Project Administration, H.O. and K.C.; Funding Acquisition, K.C.

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Conflicts of Interest: The authors declare no conflict of interest.

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Article

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Factors Affecting Electroplated Semiconductor Material Properties: The Case Study of Deposition Temperature on Cadmium Telluride

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Abstract: Electrodeposition of cadmium telluride (CdTe) on fluorine doped tin oxide (FTO) using two electrode configurations was successfully achieved with the main focus on the growth temperature. The electroplating temperatures explored ranged between 55 and 85 $^\circ C$ for aqueous electrolytes containing 1.5 M cadmium nitrate tetrahydrate (Cd(NO₃)₂·4H₂O) and 0.002 M tellurium oxide (TeO₂). The ensuing CdTe thin-films were characterized using X-ray diffraction (XRD), UV-Vis spectrophotometry, scanning electron microscopy (SEM), energy dispersive X-ray (EDX), and photoelectrochemical (PEC) cell measurements. The electroplated CdTe thin-films exhibit a dominant (111) CdTe cubic structure, while the crystallite size increases with the increase in the electroplating temperature. The dislocation density and the number of crystallites per unit area decrease with increasing growth temperature. The optical characterization depicts that the CdTe samples show comparable absorbance and a resulting bandgap of 1.51 ± 0.03 eV for as-deposited CdTe layers. A marginal increase in the bandgap and reduction in the absorption edge slope towards lower deposition temperatures were also revealed. The annealed CdTe thin-films showed improvement in the energy bandgap as it tends towards 1.45 eV while retaining the aforementioned absorption edge slope trend. Scanning electron microscopy shows that the underlying FTO layers are well covered with increasing grain size observable relative to the increase in the deposition temperature. The energy dispersive X-ray analyses show an alteration in the Te/Cd relative to the deposition temperature. Higher Te ratio with respect to Cd was revealed at deposition temperature lower than 85 °C. The photoelectrochemical cell study shows that both *p*- and *n*-type CdTe can be electroplated and that deposition temperatures below 85 °C at 1400 mV results in p-type CdTe layers.

Keywords: electrodeposition; CdTe film; two-electrode configuration; thin films; electroplating temperature

1. Introduction

Electrodeposition has emerged as a one of the versatile and cost-effective growth techniques of metal, metalloid, and semiconductor materials [1]. With emphasis on semiconductor growth, the use of either two- or three- electrode electroplating technique has been effective in the growth of high-performance semiconductor materials [2]. Aside from the the electroplating configuration, challenging factors affecting the reproducibility of electroplated materials include the solutes incorporated and solvent utilized, electrolytic bath ionic concentrations, solution aging (electroplating age), the stabilities of both growth pH and deposition temperature, and the deposition current density [3]. Provided these factors are optimized, high-quality semiconductor materials such as cadmium telluride (CdTe) thin-films can be grown and incorporated for different applications. CdTe

is one of the II-VI semiconductor materials that has been grown using several techniques including electroplating [4,5] and has been extensively researched owing to its properties [6]. Due to the direct bandgap of CdTe at room temperature (~1.45 eV), it is capable of absorbing a substantial fraction of the electromagnetic spectrum under AM1.5 conditions. This characteristic has been explored in the photovoltaic (PV) community in achieving high-efficiency CdTe-based solar cells [7]. The recent hike in the conversion efficiency from 16.5% in 2004 [8] to 22.1% in 2016 [9] as reported in the literature is mainly due to the eradication of defects within the crystal lattice or traps within the bandgap in addition to improved crystallinity, passivation of the grain boundaries which is due to better understanding of both material and device issues. Therefore, it is fundamental to strive towards process optimization amongst others. Under both two and three- electrode electrodeposition configurations, different deposition temperatures have been utilized by independent researchers [10–16] without a unifying examination of the effect of electroplating temperature in aqueous solution. Although, limiting factors such as the operating temperature of reference electrode (of about 70 °C) is to be considered for the three-electrode configurations. Therefore, this publication examines the effect of temperature of the electrolyte on the structural, optical, morphological compositional properties and electronic properties of electrodeposited CdTe layers grown from an aqueous solution containing tellurium dioxide (TeO₂) and cadmium nitrate Cd(NO₃)₂ as the respective precursors of Te and Cd.

2. Materials and Methods

2.1. Thin-Film Synthesis

Cadmium telluride thin-films were electrodeposited from a solution containing 1.5 M cadmium nitrate tetrahydrate ($Cd(NO_3)_2$ ·4H₂O) and 0.002 M tellurium oxide (TeO₂). The respective precursors for Cd and Te were dissolved in 400 mL of deionized (DI) water contained in a polypropylene beaker using the set up depicted in Figure 1. The resulting aqueous solution will be referred to as CdTe-bath henceforth in this report. Using these precursor concentrations and electrolytic cell set up, four electrolytic baths were created. To achieve a transparent and homogenous solution, the baths were stirred for about 300 min.

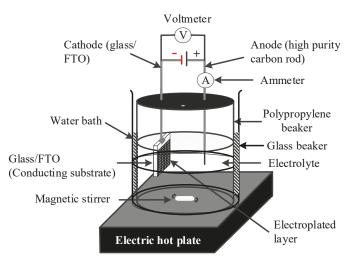


Figure 1. Typical two-electrode electrodeposition configuration.

Prior to electroplating, the pH and the magnetic stirring rate of the bath were maintained at 2.00 ± 0.02 and ~ 300 rpm. The adjustment of the pH is achieved by either using nitric (HNO₃) acid to lower the pH value or ammonium hydroxide (NH₄OH)—an alkaline to increase the pH value.

The deposition temperature is set at 55, 65, 75, and 85 °C for respective electrolytic baths, while the deposition voltage is kept constant at 1400 mV for all the CdTe layers. The 1400 mV cathodic growth voltage is based on prior optimization of CdTe thin-films grown from a pure $Cd(NO_3)_2$ electrolyte as described in the literature [17]. The deposition temperature lower or higher than this range were not reported due to low adhesion of the ED-CdTe thin-film and the formation of water bubbles on the g/FTO substrate due to the close proximity of the deposition temperature to the boiling point of water.

The glass/fluorine-doped tin oxide (g/FTO) substrates utilized as the working electrode were cut into strips with a dimension of $3 \times 2 \text{ cm}^2$. The g/FTO strips were washed using soap water in an ultrasonic bath, alcohol, rinse thoroughly in DI water and dried using nitrogen gas [18]. After the thin-film layer deposition, the $3 \times 2 \text{ cm}^2$ strips were cut into two halves of $3 \times 1 \text{ cm}^2$. One half is left as-deposited (AD) while the other is cadmium chloride treated (CCT) to improve the material and electronic properties of the CdTe layers as it used in the CdTe-based photovoltaic device-ready process. The CCT treatment was performed by adding a few drops of aqueous solution containing 0.1 M CdCl₂ in 20 mL of DI water to the CdTe surface. The full coverage of the CdTe layers with the CdCl₂ solution was achieved by spreading the solution using solution-damped cotton bud. The CdTe layers were allowed to air-dry and annealed afterwards in air at 400 °C for 20 min. The CCT-CdTe layers were allowed to cool in the air before both the AD and the CCT layers were rinsed to eliminate the loosely adhered particles of CdTe, Cd, and Te from the surfaces of the thin-film and dried in the presence of nitrogen gas.

It is necessary to note that cyclic voltammetry as shown in Figure 2 of the CdTe-bath was performed at electrolytic bath conditions when bath temperature, pH, and stirring rate were set at 85 °C, 2.00 ± 0.02 and ~300 rpm. The voltammogram is the current-voltage (I-V) curve of the CdTe-bath to determine the optimal cathodic voltage region for the deposition of CdTe.

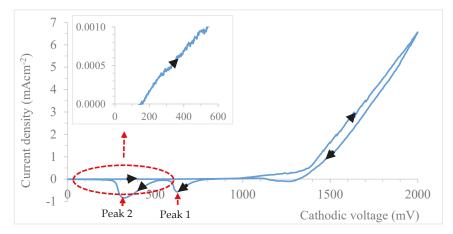


Figure 2. Typical cyclic voltammogram of an aqueous electrolyte at 85 °C containing 1.5 M $Cd(NO_3)_2$ ·4H₂O and 0.0002 M TeO₂ in 400 mL of DI water.

Tellurium is deposited first because it is more positive as compared to cadmium with respective standard reduction potential value of +593 mV and -403 mV with respect to standard H₂ electrode. From the inset of Figure 2, Te starts depositing at a cathodic voltage of ~170 mV and above, while Cd starts deposition at 1000 mV. Details of the optimization process have been documented by the author's group in the literature [12,17].

2.2. Thin-Film Characterization

The electroplated layer characterisation were performed using equipment made available by the Materials and Engineering Research Institute (MERI) research institute, Sheffield Hallam University (SHU), UK.

The structural characterization was carried out using Philips PW 3710 X'pert diffractometer (Almelo, Netherlands) mounted with 1.5406 Å wavelength Cu-K α monochromator. The X-ray diffraction system is also equipped with X'Pert High Score which aided with phase identification, dominant diffraction and for the estimation of the crystallite sizes. For the experiments presented in this work, thin-films were scanned between the range of $2\theta = 20^{\circ}-70^{\circ}$. Using the Scherrer formula as shown in Equation (1), the crystallite size *D* was estimated. Where β denotes the full-width-at-half-maximum (FWHM) of the diffraction intensity in radians, θ denotes the Bragg angle, λ denotes the X-rays wavelength (which is 1.5406 Å for Cu-K α monochromator) and *K* is the shape constant. For spherical geometry, *K* is taken as 0.94.

$$D = \frac{K\lambda}{\beta\cos\theta} \tag{1}$$

The dislocation density, δ , which defines the length of dislocation lines per unit volume of crystal in the thin-film is calculated using Equation (2) as reported in the literature [19]

$$\delta = \frac{1}{D^2} \tag{2}$$

The estimation of the number of crystallites per unit area in the thin-film, N, was done using Equation (3) as documented in [19,20].

$$N = \frac{t}{D^3} \tag{3}$$

The film thickness was measured using a UBM 1080 Microfocus optical profilometer (UBM Messtechnik, Koln, Germany) and mathematically estimated using Faraday's law of electrolysis (see Equation (4)), where *T* is the film thickness, *J* is the average current density during deposition, *M* is the molar mass of CdTe ($M_{CdTe} = 240.01 \text{ gmol}^{-1}$), *t* is the duration of deposition, *n* is the number of electrons transferred for deposition of 1 molecule of CdTe (n = 6), and *F* is the constant defined by Faraday as 96,485 Cmol⁻¹, and ϱ is the density of CdTe.

$$T = \frac{JMt}{n\rho F} \tag{4}$$

The optical absorbance data of the electroplated thin-films were taking within the range of 200 to 800 nm using Cary50 Scan UV-visible spectrophotometer (Agilent Technologies, Santa Clara, CA, USA). From the absorbance data accumulated within the specified wavelength range, the bandgap was estimated using the Tauc's formula illustrated in Equation (5) via the graph of $(\alpha hv)^2$ versus (*hv*). Where the coefficient of absorption is represented by α , the bandgap energy is represented by E_g , the Planck's constant is represented by *h*, the incident photon frequency is represented by *v*, the proportionality constant which depends on the refractive index of the sample under investigation is represented by *k*, and *m* equals 0.5 for a direct bandgap semiconductor. The extrapolation of the straight line portion of the Tauc's plot (at $(\alpha hv)^2 = 0)$ gives the bandgap energy.

$$\alpha = \frac{k(hv - E_g)^m}{hv}$$
(5)

The examination of the thin film's surface morphology and composition was performed in vacuum condition using FEI Nova200 NanoSEM (Electron Nanoscopy Instrument, Lincoln, NE, USA) fitted with energy dispersive X-ray (EDX) detector. The confirmation of the electrical conduction type is done using photoelectrochemical (PEC) cell measurements by the formation of a junction

between the solid (g/FTO/CdTe) and liquid (an aqueous solution of $0.1 \text{ M Na}_2\text{S}_2\text{O}_3$ in 20 mL DI water). The comprehensive detail of the PEC set up is incorporated in [18].

3. Result and Discussion

Material Characterization: In order to validate the results in this Section, all the stated values correspond to the average of three replica samples investigated under the same conditions.

3.1. X-Ray Diffraction (XRD) Analysis

For this set of experiments, the thicknesses of the CdTe layers electrodeposited at a different temperature from CdTe-baths was maintained at ~1µm under as-deposited conditions using factors such as deposition time, stirring rate amongst others. Figure 3a,b illustrate the typical XRD patterns of CdTe thin-films electrodeposited at different growth temperatures under as-deposited (AD) and cadmium chloride treated (CCT) conditions respectively. While Table 1; Table 2 are the respective summaries of the X-ray diffraction analysis for cubic (111) CdTe diffraction for AD and CCT-CdTe layers and the comparative analysis of the dislocation density and number of crystallites per unit area of the CdTe thin-films electroplated at a different temperature. Under both the AD and CCT conditions, the CdTe layers show diffraction patterns with a preferential and strong (111) phase of the cubic structure of CdTe at $2\theta = \sim 24.0^{\circ}$ (see Figure 3a,b). Diffractions with the underlying g/FTO substrate were observable at $2\theta = \sim 20.6^{\circ}$, $\sim 33.8^{\circ}$, $\sim 37.9^{\circ}$, $\sim 51.6^{\circ}$, $\sim 60.7^{\circ}$ and $\sim 65.6^{\circ}$. This is in addition to the cadmium tellurate (Cd_xTeO_y) diffraction observed at $2\theta = 23.0^{\circ}$. With respect to the AD-CdTe layers shown in Figure 3a and Table 1, an increase in the deposition temperature resulted in an increase in the cubic (111) CdTe diffraction intensity, peak sharpness, and crystallite size as evident by the 65.8 nm observed at 85 °C. This indicates an enhancement in the crystallinity and a reduction in the lattice defects of the CdTe-layers at high deposition temperature. This observation can also be said of the CCT-CdTe layers with the highest cubic (111) CdTe intensity at 85 °C (see Figure 3b and Table 1).

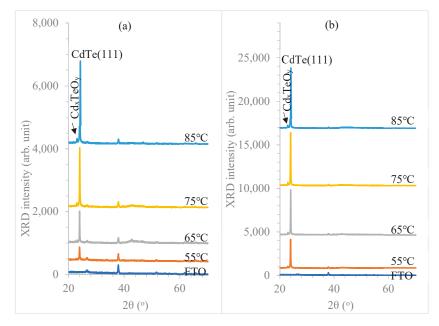


Figure 3. XRD patterns of CdTe thin-films electroplated at different temperatures under (**a**) as-deposited (AD) and (**b**) cadmium chloride treated (CCT) conditions.

With emphasis on the CdTe (111)C preferred orientation, a drastic improvement in the intensity of the diffraction after CCT treatment and crystallite size was observed notwithstanding the CdTe-bath deposition temperature. Interestingly, a reduction in the dislocation density and the number of crystallites per unit area was observed with an increase in the deposition temperature, while further improvements were observed even after CCT (see Table 2 and Figure 4). This observations might be as a result of the recrystallization of the polycrystalline CdTe thin-films during treatment which results to the improvement in the Cd/Te stoichiometry by the sublimation of surplus elements or the formation of CdTe by the reaction between surplus elemental Te and Cd from CdCl₂ treatment [4,21]. It should be noted that no matter the deposition technique, Te –precipitation is one of the main challenges in the deposition of CdTe [22,23]

Deposition Temperature (±2 °C)	20 (°)	Lattice Spacing (Å)	FWHM (°)	Crystallite Size D (nm)	Dislocation Density δ ₁ ×10 ¹¹ (Lines·cm ⁻²)	Number of Crystallites per Unit Area N ₁ ×10 ¹² (cm ⁻²)
			AD)		
55	23.9	3.73	0.227	37.4	7.15	1.91
65	23.8	3.74	0.195	43.5	5.28	1.21
75	23.9	3.72	0.162	52.4	3.64	0.69
85	24.0	3.70	0.129	65.8	2.31	0.35
			CC	Г		
55	23.9	3.714	0.162	52.4	3.64	0.69
65	24.0	3.708	0.129	65.8	2.31	0.35
75	24.0	3.713	0.129	65.8	2.31	0.35
85	24.0	3.715	0.129	65.8	2.31	0.35

Table 1. Summary of the X-ray diffraction analysis for cubic (111) CdTe diffraction for AD and CCT-CdTe layers.

Improvement in the crystallinity of CdTe after post-growth treatment in the presence of chlorine due to factors such as grain growth, recrystallization amongst others is generally accepted by the scientific community [24,25]. The stagnation observed in the crystallite size at 65.8 nm might be as a result of the limitation of the XRD machine utilized and/or that of the Scherrer's formula utilized in the measurement and analysis of CdTe thin-films respectively [26,27].

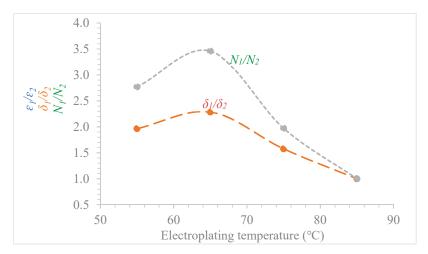


Figure 4. Comparative analysis of the dislocation density and number of crystallites per unit area of the CdTe films electroplated at different cathodic voltages.

Deposition Temperature (±2 $^{\circ}$ C)	δ_1/δ_2	N1/N2
55	1.96	2.77
65	2.29	3.46
75	1.58	1.97
85	1.00	1.00

Table 2. Comparative analysis of the dislocation density and number of crystallites per unit area of the CdTe films electroplated at different temperature under AD and CCT conditions.

The obtained XRD diffraction data from the CdTe thin film structural analysis is in agreement with the 01-075-2086 reference file of the Joint Committee on Powder Diffraction Standards (JCPDS) for cubic CdTe layers.

3.2. Thickness Measurement

For this experiment, the deposition duration was maintained at 180 min for each of the electroplated CdTe at different deposition temperatures. Figure 5 shows the graphical plot of both the estimated and the measured thicknesses including the average deposition current density of the CdTe layers against the deposition temperature. For the estimated thickness using the Faraday's equation (see Equation (4)), the rise in the thickness of electrodeposited CdTe with increasing deposition temperature was solely due to the corresponding increase in the average current density of deposition. In addition, increase in the solubility of solvents and the catalyses, the reactions are also as a result of an increase in the electroplating temperature [28]. Correspondingly, this divulges an increase in the deposition current density and hence, a rapid growth rate of constituent elements or compounds.

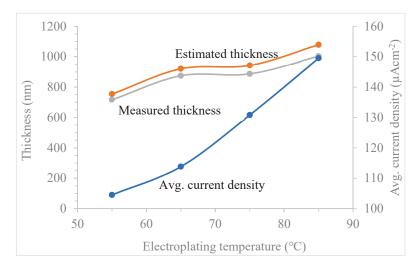


Figure 5. A plot of the estimated and measured thicknesses (as-deposited) and the average current density during electroplating against the electroplating temperature for CdTe layers grown for 180 min.

The observed deviation of the estimated thickness and the measured thickness is due to the assumption made by Faraday's law of electrolysis that all the electronic charges flowing through the electrolytic cell partake in the growth of the electroplated materials. The assumption did not consider the electronic charges associated with the breakdown of water into its constituent ions and the additional chemical reactions on both the cathode and anode. Therefore, the estimated thickness using Faraday's formula served as the upper limit of the thickness. As observed in Figure 5, a greater deviation between the measured and the estimated thickness was observed for the CdTe layers grown

at 85 $^{\circ}\text{C}$ due to the favourable impact of higher temperature to molecular and ionic activity within the electrolyte.

3.3. Optical Properties Analysis

Figure 6a,b shows the Tauc's plot of $(\alpha hv)^2$ against (hv) for CdTe thin-films electrodeposited at different temperatures under both AD and CCT conditions respectively. Table 3 and Figure 7 summarizes the observed bandgap energy and the absorption edge of the investigated CdTe thin-films. Under the as-deposited condition, the observed bandgaps range is within the generally acceptable range of 1.51 ± 0.03 eV for CdTe layers [29]. This follows a trend in which the highest bandgap of 1.54 eV was recorded at 55 °C and the lowest bandgap of 1.48 eV was observed at 85 °C. It is generally accepted in the photovoltaic community that the optimal bandgap 1.45 eV is required to achieve the highest efficiency of a one-bandgap p-n junction photovoltaic device.

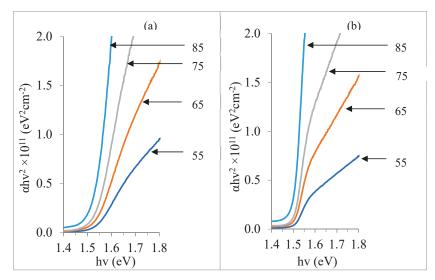
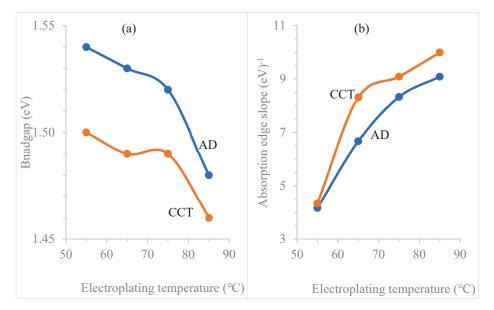


Figure 6. Optical absorption spectra for electroplated CdTe thin-films electroplated at different deposition temperature under (a) AD and (b) CCT conditions.

 Table 3. The optical bandgap and absorption edge slope of CdTe layers electroplated from electrolytes at different temperatures.

Electroplating	Bandgap (eV)		Absorbance Edge Slope (eV ⁻¹)		
Temperature (°C)	AD	CCT	AD	CCT	
55	1.54	1.50	4.17	4.34	
65	1.53	1.49	6.67	8.33	
75	1.52	1.49	8.33	9.09	
85	1.48	1.46	9.09	10.00	

A shift towards 1.45 eV bandgap was observed after post-growth treatment –CCT as shown in Figure 6b, Figure 7 and Table 3. This observation should be as a result of the improvement in the material and electronic properties of CdTe [24,25]. Further to this, a shift in the absorption edge slope was also observable, with the highest edge slope observed at 85 °C under both AD and CCT conditions. It is known that the sharpness of the absorption edge slope indicates lesser impurity energy levels and defects in the thin-films under investigation [30–33]. This observation suggests that more



stoichiometric CdTe layers are deposited at 85 $^{\circ}$ C and a further improvement is achievable after CCT. This observation is in agreement with the summation made in Section 3.1.

Figure 7. (a) A plot of optical bandgap of CdTe electroplated from electrolytes at different deposition temperature and (b) is the absorption edge slope of the CdTe layers under both AD and CCT conditions against deposition temperature.

3.4. Morphological Properties Analysis

Figure 8a–d shows the SEM images of CCT-CdTe thin-films electrodeposited at different growth temperatures ranging from 55 to 85 °C. The CdTe thin-films deposited at all the explored deposition temperatures show excellent coverage of the underlying g/FTO substrate. The purported good coverage is due to the good quality of the CdTe layers deposited based on the electrodeposition parameters such as the cathodic voltage, stirring rate, pH amongst other factors prior to CCT. While the retention of the complete coverage after CCT is owing to the enhancements in the CdTe micro-structure as a result of the recrystallization, sublimation of superfluous elements, grain growth and the formation of CdTe via a chemical reaction between excess Cd from CdCl₂ and precipitated Te in the layer. In AD-CdTe, cauliflower-like clusters consisting of numerous crystals are often observed with sizes ranging between \sim 30 and 65 nm [17]. Upon CCT, these crystals merge into grains due to their large surface to volume ratio. This is a key feature of nano-materials and helps in the formation of large grains. The CCT-CdTe grains are much larger with grains sizes ranging between \sim 200 and 6000 nm.

Based on topological observation, a gradual increase in the grain size with increasing deposition temperature was noted with the largest grain size of 6 μ m and lower grain boundary density observed for the 85 °C bath. This observation indicates that although CCT facilitates grain growth in CdTe, high deposition temperature favours grain growth. It is relevant at this point to compare the noted trend of the grain size in Figure 8 with the deductions made based on the number of crystallites per unit area N_1 in Section 3.1. It is at this point important to note that the calculated crystallite size using the Scherrer formula in XRD analysis does not translate to the sizes of grains observed in the SEM micrograph. However, grains can be formed from a single or multiple crystallites.

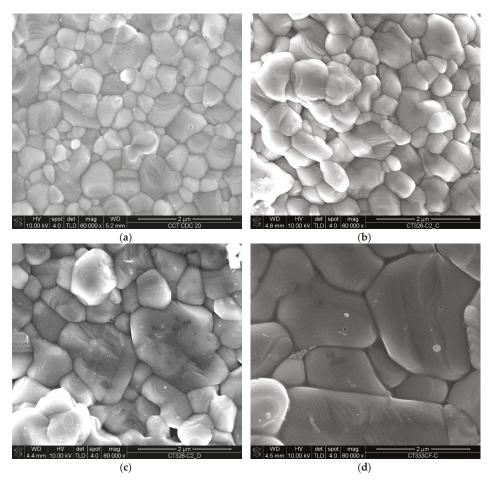


Figure 8. Typical 2-dimensional SEM micrographs for CdCl₂ treated CdTe samples grown from electrolyte at different electroplating temperature between 55 and 85 °C. (**a**) 55 °C CCT-CdTe; (**b**) 65°C CCT-CdTe; (**c**) 75 °C CCT-CdTe; (**d**) 85 °C CCT-CdTe.

3.5. Compositional Measurement

Figure 9 shows the typical EDX spectra for AD and CCT-CdTe grain at 85 °C and the plot of the atomic composition ratio of Te to Cd in electroplated CdTe layers under both AD and CCT conditions against the electroplating temperature. Aside from Te and Cd elements, other elements such as O, F, Sn, Si were also randomly observed owing to layer oxidation and/or the underlying g/FTO substrate. With emphasis on the as-deposited CdTe layers as shown in Figure 9, the compositional ratio of Te/Cd is less than 1 for the CdTe thin-film deposited at 85 °C. The CdTe thin-films grown at deposition temperature 75 °C and below show comparative Te-richness.

It can be recalled from the succinct discussion on the cyclic voltammogram in Section 2.1 and Figure 2 that with the increasing deposition potential, electroplated layers go through the stages of Te deposition, Te-rich CdTe deposition, near stoichiometric CdTe deposition and Cd-rich CdTe depositions based on the redox potential of Cd and Te. The observed effect of deposition temperature even when it is performed at the same deposition potential seems to give a similar effect by a continued shift in the cyclic voltammetric graph to the right with decreasing deposition temperature. This argument is valid

due to the catalytic effect of heat in reaction and in the mobility of ions constituted in the electrolyte especially Cd with comparatively lower redox potential. This is one of the possible reasons for the Cd or Te richness of the deposited CdTe layer at the same cathodic voltage at the exploring temperature of 85 °C and between 55 and 85 °C, respectively. After CCT, a shift towards stoichiometry in the atomic composition ratio of the CdTe layers was observed (see Figure 9). This might be influenced by the reaction between Cd from CdCl₂ with unreacted Te and/or the sublimation of excess elemental Cd and Te from the layer. For photovoltaic applications, the richness of Cd in CdTe used as an absorber layer has been documented in the literature to produce a comparatively higher efficiency [34–37]. A stoichiometry of 50/50 Te to Cd atomic composition was observed for the 85 °C CdTe after CCT signify comparatively higher crystallinity. This observation is in agreement with the high crystallinity level observed at 85 °C.

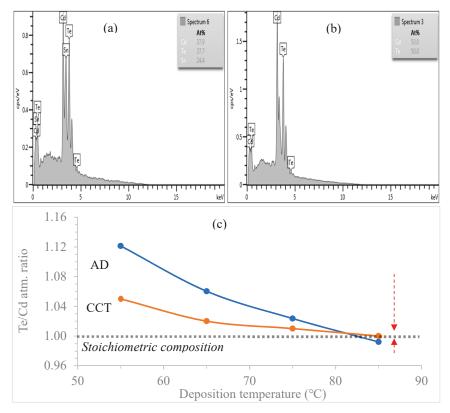


Figure 9. EDX spectra of CdTe grown from the 85 °C electrolyte under (**a**) AD, (**b**) CCT conditions (**c**) is the graphical summary of Te/Cd atomic composition ratio against electroplating temperature of CdTe for both AD and CCT samples.

3.6. Photoelectrochemical (PEC) Cell Measurement

Figure 10 shows the PEC cell measurements of the CdTe layers electroplated from electrolytes at different deposition temperature against electroplating temperature under both AD and CCT conditions. An all-round technique such as the Hall effect measurement was not used because of the effect of the highly conductive FTO underlying substrate. The obtained data cannot be isolated only for CdTe from the measurement.

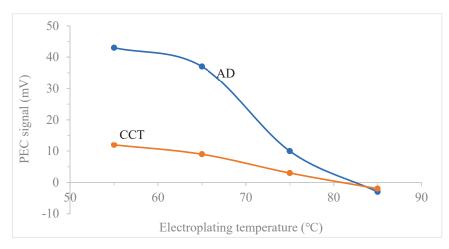


Figure 10. A plot of PEC signal of CdTe electroplated from electrolytes at different deposition temperatures against electroplating temperature under both AD and CCT conditions.

As depicted in Figure 10, the electrical conduction type of the as-deposited CdTe layers grown at 85 °C is *n*-type while the ones grown at between 55 and 75 °C, are *p*-type. A similar observation is also made of the CdTe layers after CCT with a shift from the *n*-type layers towards p-type electrical conductivity and vice versa, while the initial conduction types were retained. The observed PEC signal shift after CCT is an attribute of recrystallization amongst factors that have been well document [24,25]. It is captivating that the observed PEC trend is somewhat similar to that of the EDX spectra summary in Figure 9c. This is because one of the predominant factors determining the electrical conduction type is the atomic compositional ratio of the constituent elements, with Te-richness in CdTe resulting in p-type and Cd-richness resulting in *n*-type conduction type [18,34,35]. Other factors include the heat treatment parameters (such as duration, temperature), preliminary atomic composition of Cd and Te, the concentration of CdCl₂ or other dopants utilized in treatment, the structure of the defects in the material, and the initial conductivity type of the material [10,17,24,38].

4. Conclusions

The effect of deposition temperature in a two-electrode electrodeposition configuration was explored and the ensued CdTe thin-films were methodically characterized and presented. The structural, optical, morphological, compositional, and electronic properties of the CdTe relative to their deposition temperature were studied. All the electroplated thin-films grown at a different deposition temperature of the electrolyte show polycrystalline cubic structure of the material with a preferred orientation along the (111) plane. The dislocation density for the as-deposited CdTe was observed to be 7.15×10^{11} lines·cm⁻² for the CdTe deposited at 55 °C and 2.31×10^{11} lines·cm⁻² for the grown CdTe at 85 °C, which was respectively reduced to 3.64 and 2.31 lines cm^{-2} . The number of crystallites per unit area N was found to reduce from 1.91×10^{12} to 0.35×10^{12} cm⁻² with increased deposition temperature from 55 to 85 °C. The N was found to reduce to 0.69×10^{12} to 0.35×10^{12} cm⁻² with increased deposition temperature from 55 to 85 °C after CCT. This is an indication that the crystallite sizes increases after annealing. This was evident with the crystallite sizes of the as-deposited films ranging from 37.4 to 65.8 nm with increased deposition temperature from 55 to 85 °C to 52.4 to 65.8 nm after post-growth CCT. The optical property investigation reveals that, the deposited layers possess bandgaps ranging between 1.51 ± 0.03 eV under as-deposited condition and 1.48 ± 0.02 eV after CCT. Prominently, the sharpness of the optical absorption edge slope reduces with the reduction in the deposition temperature. Morphologically, all the electrodeposited layers show full underlying layer coverage.

Comparatively, larger grains after CCT were observed for layers grown at 85 °C. The compositional analysis reveals the presence of Cd and Te in the deposited thin-film. A atomic ratio for Cd:Te of 1:1 was recorded for CdTe layers grown at an electroplating temperature of 85 °C. Additionally, an increase in the atomic concentration of Te with the reduction of the electroplating temperature for the explore deposition temperature range of 85 to 55 °C was noted. The PEC measurements show that the CdTe layers grown at 85 °C is *n*-type under both AD and CCT conditions, while p-type conduction type CdTe layers ensued for the layers grown at deposition temperature of 75 °C and below. These results underline the importance of the deposition temperature in the electrodeposition and the capability of two-electrode electrode position configuration. Aside from the elimination of possible contaminants from the reference electrode in this configuration, the 2-electrode system also provides the leeway of electroplating at higher temperatures to improve the material and electronic gualities of PV materials.

Author Contributions: The individual contributions to this publication include the conceptualization, A.A.O.; methodology, A.A.O.; validation, A.A.O. and I.M.D.; formal analysis, A.A.O.; investigation, A.A.O.; resources, A.A.O. and I.M.D.; data curation, A.A.O.; writing—original draft preparation, A.A.O.; writing—review and editing, A.A.O.; visualization, I.M.D.; supervision, I.M.D.; project administration, I.M.D.

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Conflicts of Interest: The authors declare no conflict of interest.

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Article

A Deep Insight into the Electronic Properties of CIGS Modules with Monolithic Interconnects Based on 2D Simulations with TCAD

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Abstract: The aim of this work is to provide an insight into the impact of the P1 shunt on the performance of ZnO/CdS/Cu(In,Ga)Se₂/Mo modules with monolithic interconnects. The P1 scribe is a pattern that separates the back contact of two adjacent cells and is filled with Cu(In,Ga)Se₂ (CIGS). This scribe introduces a shunt that can affect significantly the behavior of the device, especially under weak light conditions. Based on 2D numerical simulations performed with TCAD, we postulate a mechanism that affects the current flow through the P1 shunt. This mechanism is similar to that of a junction field effect transistor device with a p-type channel, in which the current flow can be modulated by varying the thickness of the channel and the doping concentration. The results of these simulations suggest that expanding the space charge region (SCR) into P1 reduces the shunt conductance in this path significantly, thus decreasing the current flow through it. The presented simulations demonstrate that two fabrication parameters have a direct influence on the extension of the SCR, which are the thickness of the absorber layer and its acceptor concentration.

Keywords: Cu(In,Ga)Se₂; mini-module; numerical simulation; P1 shunt; space charge region (SCR); TCAD; transistor effect

1. Introduction

The prospects of copper indium gallium diselenide-based solar cells (CIGS) as an alternative to traditional silicon solutions are growing with each efficiency achievement. Three devices are distinguished regarding their respective efficiencies, which are lab-scale, mini-modules, and modules. Regarding lab-scale devices, ZSW reported an efficiency of 22.6% [1], meanwhile Solar Frontier reported the world record with an efficiency of 22.9% [2]. In the case of mini-module devices, 18.7% efficiency was reported by Solibro [3]. Finally, TSMC reported an efficiency of 16.5% for a full-size module in reference [4].

According to reference [5], improving the efficiency of lab scale cells could show the potential for improvement of large area interconnected devices. Optimization of ZnO window layers, absorbers and CIGS/CdS interfaces are found to be a key for the improvement of laboratory size devices [5]. On the other hand, according to reference [4], taking into consideration the dead areas of interconnects could also reduce power losses and improve module efficiency.

In this work, we present simulations of the dead area in interconnected devices with varied fabrication parameters to study their impact on the dark *JV*-characteristic. We will also show experimental results to compare them with the simulations. Furthermore, based on these simulations

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and experimental results we will explain a mechanism that plays an important role in the JV-characteristic of the device.

Thin film CIGS devices consist of five functional layers [6,7]. The monolithic interconnects between two devices are introduced through three scribes [7,8]. This structure is known to induce some efficiency losses due to shunts and dead areas [8,9]. In this work we investigate the shunt associated with the P1 scribe between adjacent molybdenum contacts. It has a direct impact on the *JV*-characteristic of the device, as demonstrated in reference [8], and is related both to the resistivity of the material and the width of the scribe. The scribe width can be adjusted easily to increase the resistance between both molybdenum contacts and reduce the P1 shunt; however, it also increases the dead area, and according to reference [8] there is a superior limit in which the efficiency starts to decrease. The schematic given in Figure 1 represents the target structure for simulation, adapted from [7] but simplified for the scope of this work.

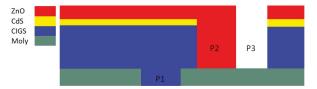


Figure 1. Schematic of Cu(In,Ga)Se₂ (CIGS) device with ZnO/CdS/CIGS/Moly and P1, P2, P3 scribes.

The mechanism discussed in this contribution is closely related to the working principle of a junction field effect transistor device (JFET), similar to the simplified p-type channel model with three layers presented in reference [10]. On top of the JFET device there is an n-type semiconductor layer with a gate contact placed over it. Under this layer there is a p-type semiconductor, which corresponds to the channel, being the main current path. The model exhibits two lateral contacts, the source, and the drain.

A space charge region (SCR) is created in the region near the p–n junction. The width of this SCR can be controlled by applying a bias to the gate or adjusting the values of acceptor (N_A) and donor (N_D) concentrations for the p-type and n-type semiconductor layers, respectively. A negative bias applied to the gate will increase the width of the SCR, whereas a positive bias will reduce it. The applied bias modulates the width of the SCR at the expense of the channel; thus, the current level in the channel is adjusted.

In the case of CIGS devices with monolithic interconnects the situation is similar. The top n-type semiconductor is ZnO/CdS. The intermediate p-type CIGS layer, including the P1 scribe, corresponds to the channel, which is placed between both molybdenum contacts. These contacts correspond to the source and the drain in the previous model. There is also a SCR in the junction between the ZnO/CdS n-type and the CIGS p-type semiconductor.

Numerical simulation is a powerful tool to investigate and optimize CIGS in different contexts. In reference [11], 2D simulation models of CIGS devices with monolithic interconnects are presented. The impact of different parameter variations, including the width of the P1 scribe and the value of N_A on the performance ratio and low light behavior are also studied in reference [11]. Another contribution that deals with 2D numerical simulations of CIGS devices is reference [12], in which passivation of the CIGS/CdS interface is studied, although the presented model does not include the interconnect. The numerical optimization of the width of the point-contact used for passivation of the CIGS/CdS interface is possible according to reference [12].

Numerical simulations can also be used to study new materials for CIGS devices. In reference [13], bandgap gradient optimization of CIGS devices with ZnS buffer layer was performed. The main result presented in reference [13] is how the bandgap gradient in CIGS affects the carrier transportation, and in turn the device performance.

Finally, simulation is the most efficient method for device optimization before production. The work presented in reference [14] shows how the thickness of the CIGS and ZnO layers can be adjusted to increase the efficiency of CIGS thin-film devices.

Our contribution shows how these numerical simulation tools could be used to propose new models that explain the behavior of large area CIGS solar cells.

2. Materials and Methods

Simulations—Our first model, which is presented in Figure 2, replicates an element of a module with a monolithic interconnect, including a P1 and P2 scribe. The P3 scribe is not included in our model as it does not add any significant contribution to the discussed mechanism. The simulation is performed using Sentaurus TCAD (Synopsys, Mountain View, CA, USA) [15], which solves the Poisson and continuity equation sets for both electrons and holes [16,17]. The electronic and physical properties, as well as the physical dimensions of the device are presented in Table 1, which includes the geometry of the P1 and P2 scribes and total dead area. The temperature for all simulations is set at 300 K.

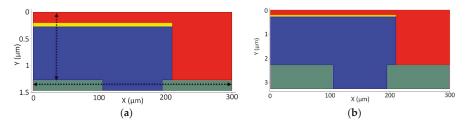


Figure 2. (a) Device structure with reduced CIGS and molybdenum thickness (1 and 0.2 μ m, respectively), the vertical and horizontal lines indicate the positions of the vertical and horizontal cuts of 2D results, respectively; (b) device structure with extended CIGS and molybdenum thickness (2 and 1 μ m, respectively).

Layer	N _D (cm ⁻³)	$N_{\rm A}$ (cm ⁻³)	X (eV)	μ _e (cm²/V·s)	μ_h (cm ² /V·s)	E_g (eV)	Thickness (µm)	Scribe	Width (µm)
ZnO	10 ²⁰	-	4.6	50	20	3.5	0.2	P1	90
CdS	10^{17}	-	4.4	50	20	2.5	0.05	P2	90
CIGS	-	$10^{14} - 10^{16}$	4.6	50	20	1.2	1.00-2.00	Dead area	200
Moly	-	-	-	-	-	-	0.20 - 1.0	Total	300

Table 1. Key parameters of the functional layers with the dimensions of scribes and dead area.

The parameters presented in Table 1 are in the same range as those seen in the literature [11,12]. The values of the electron and hole mobilities (μ_e and μ_h , respectively) could be considered overestimated, although in the contributions presented previously [12,13], the values of the mobilities for both carrier types are even higher ($\mu_e = 100$ and $\mu_h = 25 \text{ cm}^2/\text{V}\cdot\text{s}$).

Figure 3 introduces a second model that is relevant for the scope of this work. The aim of this simulation is to verify whether the presence of the space charge region (SCR) has an impact on the current flowing between anode and cathode through the P1-shunt. As such, the presented model has only a CIGS layer over the patterned (P1 scribe) molybdenum layer presented previously. Without the ZnO/CdS n-type semiconductor layers there is no junction, therefore the SCR is eliminated.

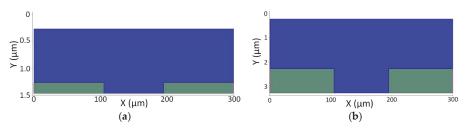


Figure 3. Device structure without ZnO/CdS layers. (a) CIGS and molybdenum thickness of 1 and 0.2 μ m, respectively; (b) CIGS and molybdenum thickness of 2 and 1 μ m, respectively.

Experimental procedure—We performed experiments on a real CIGS sample with monolithic interconnect to compare these results with the simulations of the models presented in Figures 2 and 3. The elimination of the ZnO/CdS layers was achieved through chemical etching with HCl (5% concentration) applied for 5 min. There is a previous publication related to the effect of the SCR on the conductivity of devices before and after etching presented in reference [18], although in this particular case, the experiment also involved dark annealing before the CdS layer was removed.

In our case, we measured the dark *JV*-curve of the CIGS sample at room temperature (25 °C) before and after etching without applying any other treatments to compare these results with the simulations. Our sample was produced in a pilot line with a co-evaporation process, a laser scribing for P1 and a mechanical patterning for P2 and P3, similar to reference [19]. Mechanical patterning of P2 and P3 is known to create fewer smooth trenches compared to laser ablation [20]. However, scribing P2 and P3 by nanosecond laser ablation is not recommended, as it might also damage the back contact [21]. According to reference [21], structuring of P2 and P3 scribes can be performed with picosecond laser ablation.

Alternative procedures for printing interconnect scribes in the device are presented in reference [22], in which P1, P2, and P3 are scribed with a femtosecond laser pulse after all the layers are deposited. P1 is filled then with a dielectric material and a metal on top of it to keep the electric continuity in the transparent contact oxide layer (TCO). On the other hand, P2 is filled with a metal to connect the TCO with the back contact of the next cell. Different materials for the filling were discussed in reference [22], including their impact on the electric behavior of the device. The method presented in reference [22] is expected to reduce the total dead area of one cell from 500 to 100 μ m.

Previous research on thermally induced metastabilities provided a relation between the degradation of the electric characteristics in CIGS devices and their decrease in doping based on the results of capacitance profiling techniques; some of these can be found in references [23]. However, other works suggest that these accelerated ageing treatments induce other collateral effects such as enhancing the Schottky barrier between molybdenum and CIGS [24]. Thus, these treatments are not considered to study the transistor effect presented in this contribution.

3. Results

3.1. Results of the Simulations

Figure 2 presents the structure used for the first simulation, which is performed at 300 K. The results of this simulation are presented in Figure 4, with the *JV*-curve in the dark for varied N_A values in the CIGS bulk. A nonlinear decrease of reverse current density with decreasing N_A according to Figure 4b was observed. From the curves of Figure 4a it can also be deduced that the forward bias required to open the current path through the p–n junction decreases with N_A . This bias could be related to the built-in voltage (V_{bi}) of the device [16], which is the height of the barrier due to the SCR.

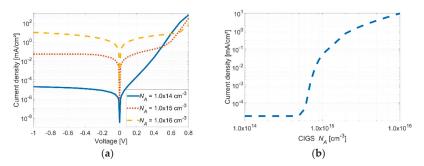


Figure 4. (a) Semilog *JV*-curve of the structure for varied values of N_A ; (b) Current density at 1 V reverse bias for varied values of N_A .

Another interesting result that could be extracted from Figure 4a is the existence of a non-symmetric behavior between the forward and reverse bias regions for $N_A = 10^{14} \text{ cm}^{-3}$. This can be explained by the fact that for lower values of N_A , the non-linear diode behavior of the device starts to dominate over the linear one at lower positive biases compared to the case of higher CIGS dopings.

Figure 5 shows a 2D plot of the simulated current density. This result gives another hint regarding the transistor effect created by the SCR and the conductance through P1. If N_A in CIGS decreases, the SCR extends into P1 and reduces the available space in the channel for the current flowing through it. To the contrary, when N_A increases, the SCR shrinks to the junction, widening the channel.

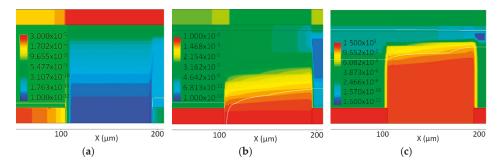


Figure 5. 2D representation of the current density flowing through the P1-shunt under a reverse bias of 1 V between anode and cathode for CIGS with: (a) $N_{\rm A} = 10^{14}$ cm⁻³; (b) CIGS $N_{\rm A} = 10^{15}$ cm⁻³; (c) $N_{\rm A} = 10^{16}$ cm⁻³. The color scale of each plot is in (mA/cm²).

As mentioned above, V_{bi} is reduced when N_A decreases. It is possible to explain this behavior with the electric field inside the device across the p–n junction, [16]. In Figure 6a, a vertical cut of the vertical component of the electric field over the anode (see Figure 2a) for the extreme values of N_A is presented. The electric field in the case of $N_A = 10^{16}$ cm⁻³ has a higher value at the CdS/CIGS interface than in the case of $N_A = 10^{14}$ cm⁻³. On the other hand, for $N_A = 10^{14}$ cm⁻³, the electric field in the CIGS bulk is constant, indicating full carrier depletion down to the contact, while in the case of $N_A = 10^{16}$ cm⁻³, the electric field in the CIGS bulk reduces linearly to 0, in support of the existence a quasi-neutral region with flat bands.

Further evidence of the effect of the SCR in the device is the absence of free carriers in the CIGS layer. These results belong to the simulation of the structure presented in Figure 2. In Figure 6b there is a representation of a horizontal cut between both contacts with the value of the free hole concentration. These curves correspond to values of $N_A = 10^{14} \text{ cm}^{-3}$ and $N_A = 10^{16} \text{ cm}^{-3}$. With lower N_A , the concentration of free holes in P1 is also reduced, but not with a linear dependency on N_A .

In the case of $N_A = 10^{14} \text{ cm}^{-3}$, the concentration of free holes in P1 is 12 orders of magnitude lower than the value of N_A , while in the case of $N_A = 10^{16} \text{ cm}^{-3}$, the free hole density is in the same order of magnitude with the value of N_A . This absence of free holes means that the hole current density between both contacts will also be reduced in the same proportion when a reverse bias is applied.

The thickness of the CIGS layer is another key parameter for the behavior of the device, as mentioned previously. The SCR extends into the CIGS layer, and if the width of the channel is sufficiently reduced, it is possible to close the path of the current through the P1 region. In Figure 7a we present a comparison between the current density for a 2 and a 1-µm thick CIGS layer. A particular emphasis on the current density in the P1-shunt for the device with a 2-µm thick CIGS layer $N_{\rm A} = 10^{15}$ cm⁻³ is presented in Figure 7b.

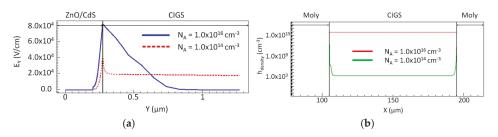


Figure 6. (a) Vertical cut (see Figure 2a) of the *Y*-component of the electric field (E_y) with $N_A = 10^{16}$ cm⁻³ and 10^{14} cm⁻³ under a bias between anode and cathode of 0 V; (b) Horizontal cut (see Figure 2a) of the free hole density between both molybdenum contacts for $N_A = 10^{16}$ and 10^{14} cm⁻³.

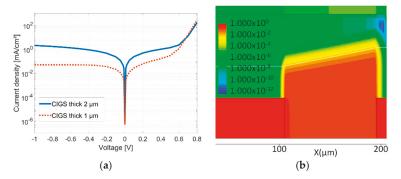


Figure 7. (a) *JV*-curve in the dark for the structures with 2 and 1 μ m CIGS layer thickness, respectively and $N_A = 10^{15} \text{ cm}^{-3}$; (b) 2D plot of the current density flowing through P1 in the structure with 2 μ m CIGS and 1 μ m molybdenum thicknesses under reverse bias of 1 V, the color scale is in mA/cm².

If we compare the results presented in Figure 7b with those of Figure 5b, the SCR does not reach the bottom of P1 when the CIGS layer is thicker. In the structure with CIGS thickness of 1 μ m, the SCR partially closes the path through P1, reducing the current density in reverse bias.

Figure 3a presents the structure of the second simulation with only CIGS/molybdenum layers, the latter divided by the P1 scribe. The temperature of the simulation was set at 300 K. A comparison between the *JV*-curves for different values of N_A in CIGS can be seen in Figure 8a, whereas a curve of the variation of the current in reverse bias for values of N_A between 10^{14} and 10^{16} cm⁻³ is shown in Figure 8b, where the current density increases linearly with the value of N_A .

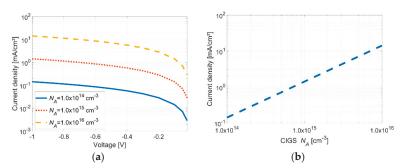


Figure 8. (a) Dark *JV*-curves of the device without ZnO/CdS for values of N_A between 10^{14} cm⁻³ to 10^{16} cm⁻³; (b) Current density vs. N_A under a reverse bias of 1 V between both contacts.

3.2. Experimental Results

It is possible to provide some evidence regarding the effect of the SCR in the reverse current of real devices. As mentioned before, if the ZnO/CdS layers are removed from the device via HCl etching, it will be possible to measure the *JV*-curve without the impact of the SCR. The results of the *JV*-measurement at 25 °C are shown in Figure 9, compared to simulation results from the models presented in Figures 2b and 3b.

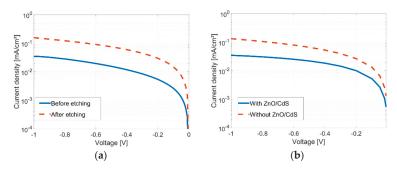


Figure 9. (a) *JV*-curve in reverse bias of the device before and after etching the ZnO/CdS layers; (b) Simulated *JV*-curves in reverse bias of the structures presented in Figure 2b (with ZnO/CdS layers) and Figure 3b (with no ZnO/CdS layer) with $N_A = 3 \times 10^{14} \text{ cm}^{-3}$. Electron and hole mobilities are reduced to 0.25 and 0.5 cm²/V·s, respectively, to fit the experimental curves.

Both the experimental and simulated results show a similar behavior. When the ZnO/CdS layer was removed, the current density flowing between both contacts increased. As mentioned above, the simulation results relate this effect to the elimination of the SCR created due to the doping gradient between the n-type and p-type semiconductors. The semiconductor parameters of the CIGS sample used in the experiment are unknown, although it is possible to adjust the simulation parameters until a good compromise with experimental results is reached as indicated in Figure 9. A necessary reduction of hole and electron mobilities in order to fit experimental findings might be justified by the fact that the shunt path across P1 involves a lateral current transport across potential barriers due to grain boundaries, in agreement with [25]. The columnar nature of the grains leads to expect a higher number of grain boundaries in the horizontal direction (along the *x*-axis) compared to the vertical one (along the *y*-axis).

4. Discussion

The results of our work suggest a mechanism similar to the JFET simplified model presented in reference [9]. In our case, the equivalence of source and drain are both molybdenum contacts, and P1 is the channel. ZnO and CdS are part of the n-type gate material, which is directly connected to the drain. If a forward bias is applied, the current flows through the p–n junction instead of through the channel. Increasing or reducing the doping gradient between the p and n-type semiconductor layers affects the SCR in the device, and if this region is wide enough to close the channel, the P1 shunt conductance will be reduced.

This behavior is presented in Figure 4a, as the reverse current bias was significantly reduced when N_A in CIGS is decreased below 10^{15} cm⁻³. Figure 4b provides further evidence of this transistor-like behavior, as the reverse bias current does not have a linear dependence with the applied bias. In fact, the reverse bias current is constant for values of N_A lower than 5×10^{14} cm⁻³, as the SCR closes the path of the current through P1. If we increase this value, the current density in reverse bias increases exponentially as the SCR thickness is reduced and the path through P1 opens. After a certain value of N_A in CIGS, in this case 10^{15} cm⁻³, the current density in reverse bias increases almost linearly. These results are in agreement with those presented in reference [11], in which decreasing the value of N_A below 10^{15} cm⁻³ is shown to have no impact on the shunt resistance of the device. It is interesting to mention that a gallium gradient, which is present in highly efficient CIGS devices with bandgap grading [26], can also play a role in the transistor-like behavior. A depth-dependent gallium distribution may induce a doping gradient [27], which to certain extent could affect the width of the SCR, and therefore the transistor effect might not be present. For sake of simplicity in the modelling, this effect has not been considered in our simulations, but could be regarded as a topic for further work.

The decrease of V_{bi} is a side-effect of manipulating the value of N_A . It should be considered carefully as it will also affect other parameters such as the open circuit voltage, the maximum power point, the fill factor and the efficiency. A good compromise between N_A and CIGS thickness is required to decrease the P1 shunt while reducing the impact on these parameters.

Removing the ZnO/CdS layer provides further evidence of the impact of the SCR in the P1 shunt and the reverse current density of the device. In this situation, the SCR is not present, and the reverse current density depends only on N_A ; thus, the transistor effect is not present in the behavior of the device. In Figure 8b, the reverse current density increases proportional to N_A ; in contrast with the results presented in Figure 4b. This increase in the reverse bias current is also presented in reference [18], in which the elimination of the SCR is considered to be the main reason behind this behavior.

This elimination of the transistor-like behavior is made plausible in the experimental results and the simulation of Figure 9. Etching away the ZnO/CdS layer increases the reverse current density. This increase may vary depending on the width of the SCR and the thickness of the CIGS layer. The results of our simulations are in agreement with experimental findings.

5. Conclusions

Based on 2D simulation results of CIGS cells with monolithic interconnects we proposed a mechanism that affects the P1 shunt, and consequently, the Ohmic behavior of the device. As has been discussed in this contribution, this mechanism has similarities with the behavior of a p-type JFET transistor device. According to this model, CIGS in P1 is the p-type channel in the device. As has been shown in the simulations, varying the thickness and the doping of CIGS, the width of the channel can be modulated, and therefore the current flowing in P1. Reducing N_A extends the SCR into the P1 interconnect. This means that the channel width is narrowed leading to a decreased shunt conductance. Experimental evidence was also provided to support the validity of the simulations. *JV*-measurements before and after etching the ZnO/CdS layer showed that when the n-type semiconductor was removed, the SCR and the transistor behavior were eliminated. The simulation results of a model with and without the ZnO/CdS layers support qualitatively the proposed mechanism.

Author Contributions: Conceptualization, R.V.L. and T.W.; Methology, R.V.L. and T.W.; Project Administration, T.W.; Supervision, D.F.M. and T.W.; Investigation, R.V.L.; Writing—Original Draft, R.V.L.; Writing—Review and Editing, T.W., T.L., D.M. and D.F.M.

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Conflicts of Interest: The authors declare no conflict of interest.

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Enhancement for Potential-Induced Degradation Resistance of Crystalline Silicon Solar Cells via Anti-Reflection Coating by Industrial PECVD Methods

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Abstract: The issue of potential-induced degradation (PID) has gained more concerns due to causing the catastrophic failures in photovoltaic (PV) modules. One of the approaches to diminish PID is to modify the anti-reflection coating (ARC) layer upon the front surface of crystalline silicon solar cells. Here, we focus on the modification of ARC films to realize PID-free step-by-step through three delicate experiments. Firstly, the ARC films deposited by direct plasma enhanced chemical vapor deposition (PECVD) and by indirect PECVD were investigated. The results showed that the efficiency degradation of solar cells by indirect PECVD method is up to -33.82%, which is out of the IEC 62804 standard and is significantly more severe than by the direct PECVD method (-0.82%). Next, the performance of PID-resist for the solar cell via indirect PECVD was improved significantly (PID reduced from -31.82% to -2.79%) by a pre-oxidation step, which not only meets the standard but also has higher throughput than direct PECVD. Lastly, we applied a novel PECVD technology, called the pulsed-plasma (PP) PECVD method, to deal with the PID issue. The results of the HF-etching rate test and FTIR measurement indicated the films deposited by PP PECVD have higher potential against PID in consideration of less oxygen content in this film. That demonstrated the film properties were changed by applied a new control of freedom, i.e., PP method. In addition, the 96 h PID result of the integrated PP method was only -2.07%, which was comparable to that of the integrated traditional CP method. In summary, we proposed three effective or potential approaches to eliminate the PID issue, and all approaches satisfied the IEC 62804 standard of less than 5% power loss in PV modules.

Keywords: anti-reflection coating; potential-induced degradation; solar cell; plasma enhanced chemical vapor deposition

1. Introduction

Photovoltaic (PV) has been recognized as the most competitive renewable energy among various renewable technologies according to its diverse applications and is a candidate of next generation large-volume power plants. For instance, Águas et al. [1] applied the PV for building-integrated photovoltaics (BIPV) application; Águas et al. [2] also fabricated thin film solar cells on cellulose paper for flexible, wearable application; and most of all was for large-scale power plants. According to the statistic reports of International Energy Agency (IEA), it pointed out that the cumulative installed



capacity of solar installations was almost 303 GW at the end of 2016 [3]. Based on the demand for long-term and safe operation, the reliabilities of PV modules gain more attention. In Figure 1, we depicted the components of crystalline silicon module under negative bias. Solar cells were held in between the front glass cover and the rear backsheet. The glass was used for light transmission and module protection; the backsheet was implemented for the reflection of incident lights shined at the gap between individual solar cells and for the reflection of residual lights that penetrate the solar cells. In general, the lifetime of PV modules was designed over 25 years. However, several kinds of issues resulted in irreversible degradation of PV modules, in which one of the most catastrophic failures was noted as potential-induced degradation (PID).

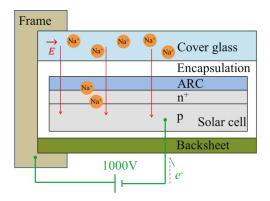


Figure 1. The structure of a crystalline Si PV module was introduced. In this diagram, the solar cells are negative-biased and the shunting model via sodium ions (Na⁺) is depicted.

PID was firstly reported for both crystalline silicon modules and amorphous silicon thin film modules by the Jet Propulsion Laboratory in 1985, but it was observed by SunPower Corp. until 2005 and coined by Pingel et al. in 2010 [4,5]. PID is ascribed to a high electric potential difference across a PV module inducing a leakage current flowing through the solar cells, which results in reversible or irreversible power conversion efficiency degradation. The schematic diagram is shown in Figure 1. Currently, 1000 V is applied in a PV power system to minimize the electric power transportation loss by serially connected PV modules. Nevertheless, the PID of PV modules is significantly enhanced under a high bias. For p-type Si-based solar cells, the most remarkable type of PID mechanism is "potential induced shunting" (PID-s). PID-s describes a degradation ascribed to both sodium ions and solar cells under a negative-biased condition. Sodium ions (Na⁺), coming from soda-lime glass, are drifted through the anti-refractive coating (ARC) layer, and then accumulate at the ARC/Si interface or in the stacking faults. Finally, the shunting paths are formed, and then the p-n junction is damaged.

Several promising strategies to approach PID-resistant PV systems have been proposed for cell, module-, or system-levels [6,7]. On the cell-level, modifying the ARC layer by elevating its refractive index (RI) has well been demonstrated to alleviate the PID-s issue [5,7–10]. In the factory of c-Si solar cells, various plasma enhanced chemical vapor deposition (PECVD) methods provide the ARC layers for solar cells, including direct, remoter, continuous-plasma (CP) and pulsed-plasma (PP) types. From the literature, it was reported that increasing the RI of the ARC layer improves its electric conductivity which can prevent positive charges accumulating in the surface and Na⁺ drifted by electric field. However, if the RI of the ARC layer deviates from the theoretically optimal value (i.e., the square-root of the RI of silicon), the light trapping performance of ARC degrades. Hence, there is a trade-off between PID-resistant ability and power conversion efficiency (PCE). In addition, Mishina et al. [11] pointed out that the film quality of the ARC has a great impact on PID-resistant ability. They showed that the ARC films deposited by the novel direct PECVD performed better PID-resistance than the one deposited by remoter PECVD, even without scarifying the PCE (i.e., keeping the conventional RI value). However, direct PECVD, in comparison with remoter PECVD, has relatively low throughput and gains additional running costs in commercialized applications. Beside the modification of ARC films, a thin oxide film between the ARC and Si substrate has been proven as another efficient solution for PID-resistant solar cells [7,12,13]. Furthermore, Nagel et al. demonstrated that the cells with this thin thermal oxide layer gained a 0.2% increase in PCE, which is ascribed to the improvement of surface passivation in the front surface [12].

Recently, a novel PECVD method, PP modulated PECVD, is commonly used for modifying SiN_x films by controlling the ion bombardment and film nucleation process [14–17]. Contrary to continuous-plasma PECVD, the manipulation of pulsed-plasma PECVD is by using a frequency modulated glow discharge during deposition, and then modifying the film qualities. After ionization, the lifetimes between free radicals remain different, and then the clusters during the film synthesization have been designated by controlling the duty cycle and periods. The duty cycle is the ratio of conducting glow discharge to the periods, as shown in the schematic diagram in Figure 2. In the scenario of low frequency modulated radio frequency (RF) discharge (40 Hz) in Watanabe et al.'s study [18], lifetimes of SiH_n (n = 0–2) radicals were shorter than 10 ms (these were estimated to be below 3 ms); whereas the lifetime of SiH₃ was longer than 20 ms. Regarding the achievement of film quality modification by PP PECVD, Watanabe et al. also pointed out the film mainly composed of SiH₃ shows fewer dangling bonds and reduced powder particle in size during deposition [18]. In addition, Viera et al. reported a high purity and controllable nanostructure achieved by the PP method [19], and Byungwhan Kim et al. pointed out that the films made by the PP method present denser and smoother surface roughness [20].

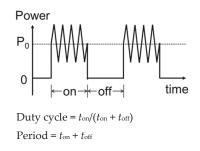


Figure 2. Time modulated RF source and the definition of duty cycle and of period.

The PID issue has been addressed for years. Current PV power plants have enrolled different kinds of cutting edge technologies to solve uprising PID concern. For instance, other types of solar cells (PERC and HIT) with inherent high voltage output are becoming mainstream, and 1500 V power system are replacing traditional 1000 V power systems [10,21]. In consideration of even stricter PID-resistant demands, improved or novel PID-resistant solutions are necessary in the future. In this work, we firstly proposed a PP PECVD technology to deal with the PID issue. Besides, the comparisons of the ARC films deposited by direct and indirect PECVD, and the enhancement of the PID-resistant ability by the additional interface oxide layer were investigated.

2. Materials and Methods

In this work, three closely related experiments were designed to approach PID-free c-Si solar cells. The cell structure is depicted in Figure 1. First, we compared PID-resistant abilities between different kinds of commercially available PECVD, namely direct PECVD (Shimadzu Corporation, Kyoto, Japan) and indirect PECVD (OTB SOLAR DEPX 2400). For the direct PECVD system, the electrodes are placed across the specimens, and the reactant gases are ionized nearby the specimens. Besides, the electric field across the electrodes can boost the moment of ions and thus these energetic ions bombard the

deposited film during deposition. Contrary to direct PECVD, the gaseous ions are generated separately from the substrates and sent to target locations through an inlet for the indirect PECVD. Secondly, in consideration of the relatively higher throughput of the OTB system, we introduced a thin oxide layer at the interface of the ARC film and Si to solve the PID issue. For these two experiments, we used 6-inch multi-crystalline silicon (mc-Si) solar cells with traditional Al back surface field (BSF), and these specimens were tested by the standard PID testing procedure. Moreover, we investigated the SiN_x films deposited by PP and CP PECVD (Otb Solar Depx 2400 by Roth & Rau, Hohenstein-Ernstthal, Germany). In common, there are two approaches to modulate the glow discharge for realizing the PP method by either controlled inlet gas or controlled bias. The latter one was employed in this work. The deposition parameters of RF frequency, modulated frequency, and duty cycle are 13.56 MHz, 80 Hz and 50%, respectively. For the PID test, we replaced the conventional mc-Si solar cells by the PERC-type mono-crystalline silicon (c-Si) solar cells which had a thin oxide layer located at the interface of the ARC and Si as well. For the characterizations of these films, we also conducted a dilute HF etching test. The dilute HF-etching rate has been pointed out as a good indicator of the film quality against PID [11]. A total of eight specimens with an RI value of 2.06 deposited by the CP and PP method were dipped in 3.85 vol % HF solution at room temperature. Fourier transform infrared (FTIR) spectra were conducted for the chemical composition of SiN_x films.

Based on the instruction of standard reliability test of PID, IEC-62804-1 [22], we followed and even tested a more severe testing condition to clarify the significance of experimental variables. All specimens in this experiment were carried out by the same PID testing procedures as following:

- Four solar cells were laminated in one module but disconnected from each other as shown in Figure 3.
- (2) The electric performances and electroluminescence (EL) images of the PV modules were recorded before PID testing.
- (3) Aluminum foils with deionized water wetted were attached upon the front glasses of modules, and then connected with the positive terminal of a high-voltage power source.
- (4) On the other hand, the negative terminal of this high-voltage power source was connected to the shunted cathodes and anodes of solar cells.
- (5) PV modules were processed in a climate chamber for 48/96 h, at 85 °C, with 85% relative humidity, and -1000 V bias.
- (6) After PID treatment, the measurements referred to in Step 2 were repeated.

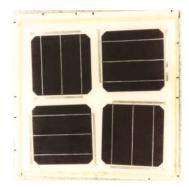


Figure 3. The photo of the (PID) test module with four cells packaged separately.

The equation for characterizing PID is listed as Equation (1):

$$PID(\%) = \frac{\left(P_{mpp,AF} - P_{mpp,BF}\right)}{P_{mpp,BF}}$$
(1)

where $P_{mpp,AF}$ is the maximum output power under standard testing conditions after PID treatment, and $P_{mpp,BF}$ is the one before PID treatment. Under the IEC 62804 standard, modules with less than 5% power loss and without induced major defects could be recognized as PID resistance [23,24].

3. Results and Discussion

3.1. PID-Resistant Approach via Film-Quality Modification

The PID-resistance of two film deposition methods was compared in this experiment, i.e., direct and indirect PECVD. The detail comparison of our equipment of these two approaches and the corresponding results are listed in Table 1. After performing the PID test, the results for mc-Si solar cells with SiN_x films deposited by the direct and indirect PECVD are presented in Table 2, showing the EL images before and after the PID test and power conversion efficiency loss. For the EL images, before PID treatment, both kinds of cells perform uniform illumination under forward bias. The EL image of the cells via indirect PECVD is relatively less uniform than via direct PECVD, which is ascribed to the inherent less gas inlets in indirect PECVD equipment. After the PID test, the apparent dark areas (marked by a red oval) were observed for the EL image of the cells via indirect PECVD, but barely seen for the direct PECVD. It indicates the more severe power conversion efficiency loss for the cell via indirect PECVD. The power conversion efficiency loss of the cell via the indirect PECVD method is up to -33.82%, significantly more severe than the one via the direct PECVD method (-0.82%). The highlighted areas in the red circles in Table 2 are located between two bus bars. This phenomenon can be interpreted by the PID-shunt model [7], where Na⁺ ions are firstly accumulated on the surface of the ARC driven by the applied negative bias, and are then drifted through the ARC layer, and finally shunt the p-n junction dramatically.

Features	Direct PECVD	Indirect PECVD
RF system	Direct plasma	Remote plasma
Pressure control	Pressure control (APC valve)	Pump speed control (pump frequency)
Pressure	67 Pa	23–25 Pa
Deposition rate	Low speed	High speed
Process time	120 s	18 s
Temperature control	Set temperature	Set heater power
Process temperature	450 °C	450 °Ĉ
Gas flow ratio (SiH4:NH3)	1:3	1:3
Film thickness	85 nm	85 nm
Refractive index	2.10	2.10

Table 1. The comparison of direct and indirect PECVD and the controlled film thickness and refractive index of specimens.

Comparing the two deposition methods, the SiN_x films deposited by direct PECVD are denser, more compact, and more conformal, but had more surface damages due to ions bombardment. Therefore, we deduce that the denser SiN_x film made by direct PECVD can resist Na^+ penetration due to less pin holes and smaller clusters during deposition. However, its lower productivity is a concern from the point-of-view of industrial applications [11,16,25,26].

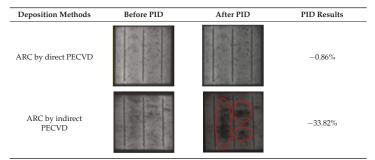


Table 2. The PID testing results and EL images for the solar cells with SiN_x films deposited by the direct and indirect PECVD.

3.2. PID-Resistant Approach via Pre-Oxidation Treatment

Although Si solar cells via indirect PECVD is associated with severe PID concern, we note the advantages of ultrahigh deposition rate (5 nm/s), which has high throughput for mass production [26]. A pre-oxidation step before ARC films by indirect PECVD was introduced to improve PID-resistance ability. Therefore, a thin oxide layer (SiO₂ or SiO_x N_{μ}) was formed between ARC and Si substrate by using a furnace with an atmosphere of O₂ and N₂ and with the setting temperature of 800 °C. The thickness of this oxide layer was around 2 to 5 nm confirmed by ellipsometer. In this section, the specimens with and without this interface oxide layer were produced. The PID testing results are presented in Table 3. The PID effect was dramatically improved and was down to -2.79% by inserting an oxide layer, which well fulfills the IEC 62804 standard of power loss less than -5%. The root cause about the role of the oxide layer was explained by Naumann et al. [27], and the extensive research about the role of oxide layer in the recovery process of PID was reported by Lausch et al. [28]. Volker Naumann pointed out two facts by investigating the cross section of the solar cell after PID treatment by TEM and EDX mapping. (1) Na was accumulated at the c-Si stacking fault resulting in the creation of a shunting path. (2) The results of O mapping identified the position of the interface oxide layer, and, moreover, the Na was also "trapped" and scatteringly distributed in the oxide layer. Lausch et al. further proved that this oxide layer may assist the Na to diffuse out from c-Si stacking fault when performing a PID recover experiment. In addition, the oxide layer served as a barrier against Na drift into the silicon base. In short, the PID-resistant ability can be improved by a factor of 10 in this experiment by introducing a thin oxide layer between Si and SiN_x films in the case of indirect PECVD which can fit the high-throughput requirement of the fabrication of Si solar cells.

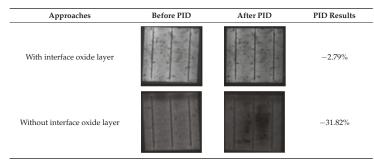


Table 3. The PID testing results and EL images for the solar cells with or without an interface oxide layer between the ARC and Si substrate on indirect PECVD.

3.3. A Novel PID-Resistant Approach via SiN_x Film Deposited by PP PECVD

Recently, PP PECVD is becoming the mainstream technique for the fabrication of c-Si solar cells. This novel method has some remarkable advantages, including higher throughput, no additional process step, being easier to control the film quality, and so on. Hence, we firstly proposed a novel study to improve the PID-resistance of SiN_x films by PP PECVD. In addition, regarding higher PID-resistant demands for modern solar cells, we evaluated the PID-resistance of 6-inch c-Si PERC-type solar cells. For the characterization of these films, we conducted a dilute HF etching test, FTIR measurement, and PID test for SiN_x films deposited by CP and PP methods.

The etched film thickness for different etching duration is presented in Figure 4. The film thicknesses of origin, and after 3, 6, and 9 min etched, were measured by ellipsometer, and the discrepancies were calculated. The HF-etching rates were deduced by linear fitting. The HF-etching rate of SiN_x film deposited by PP PECVD is 2.5 nm/min, 2.6 times lower than the one by CP PECVD. Mishina et al. [11] pointed out that the mechanism of HF etching is associated with the SiN_x dissociations via oxygen assistance, i.e., higher oxygen density in the SiN_x film leads to a larger HF-etching rate. In addition, the SiN_x film with lower HF etching rate (lower oxygen density) is related to high PID-resistance [11]. The root cause is that the oxygen contained in SiN_x may be in the form of SiN₂O or SiO₂, and subsequently, the SiO₂ dissolved in the molten salt (Na⁺) will form a liquid sodium silicate (Na₂O·(SiO₂)) [11,29,30]. The oxygen-assisted corrosion of the SiN_x film in molten salt would create a shunting path and then worsens the original PID-resistance of the ARC film. Accordingly, since our ARC films made by the PP method contain less oxygen atoms than by the CP method, we derived the SiN_x film bade by the PP method to perform better PID-resistance.

FTIR measurement was employed to characterize the chemical composition discrepancies between the films deposited by CP and by PP methods, and the results are shown in Figure 5. The absorbance at 850 cm^{-1} was designated as the asymmetric stretching vibration mode of Si–N bonding [31]; the absorbance at 2160 cm⁻¹ was designated as the in phase stretching vibration mode of Si-rich Si-H bonds [32]. Compared to the peak of Si–N stretching mode of the SiN_x film deposited by the PP method located at 831.2 cm⁻¹, the one deposited by the CP method is at 881 cm⁻¹. Shinichi Kobayashi reported that the large blue shift of the Si-N stretching mode is ascribed to oxidation because of the net change of electronegativity around the Si–N bonds due to the increase in the Si–O bond density [33]. The blue-shifted peak of Si–N mode indicates that the CP method-deposited SiN_x film contains inherently higher oxygen, which agrees with the result of the dilute HF etching test. These results also suggest that the PP method can diminish the oxygen content in SiN_x as well as can increase the PID-resistant ability. The absorbance peak at 3350 cm⁻¹ is designated as N-H bonds [34], and these N-H bonds present almost identical for the films deposited both PP and CP methods. In addition, Si-N and Si–H peak magnitudes of the PP method-deposited SiN_x film are significantly less than that of the CP method-deposited SiN_x film. These results indicate that our PP method-deposited SiN_x film is either relatively thinner or has a smaller RI value (or less Si content) than that of the CP method-deposited one. Ideally, to compare the PID-resistant ability of SiN_x films deposited by CP and PP methods, it should have the same thickness and Si content. Therefore, these observed either thinner or lower Si content films might lead us under evaluate the anti-PID ability of the PP method SiN_x film because Na⁺ can easier penetrate into thinner and accumulate on lower conductivity SiN_x films. Nevertheless, we succeeded in the modification of the SiN_x property of film thickness, silicon content, or oxygen content by introducing the PP method as an additional control of freedom.

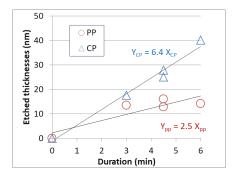


Figure 4. Etched thicknesses of SiN_x films deposited by PP and CP PECVD in 3.85 vol % HF solution. The film thicknesses were measured by ellipsometer. Each specimen was recorded at five locations and the variations may come from the non-uniform etching rate in whole wafers and from the measuring uncertainties.

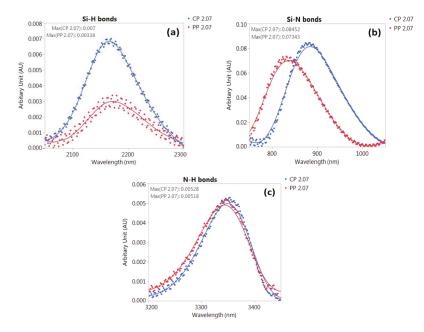


Figure 5. IR absorbance of (a) Si–H, (b) Si–N, and (c) N–H bonds by Fourier transform infrared (FTIR) characterizations for the SiN_x films deposited by the CP and PP methods. The smooth curves are provided as a guide to the eye for indicating the absorbance peaks.

Finally, not only the 48- but also 96-h PID treatments for c-Si PERC-type solar cells, in which there were four and two pieces respectively, were performed and are shown in Figure 6. Simultaneously, EL images are shown in Table 4. PID results revealed that both groups of samples fit the requirement of IEC 62804 specification, i.e., power conversion efficiency loss of the cells after PID test is under 5%. It was noticeable that the PP group for 48-h testing had shown the largest error bar. This is because we retained all data and one of them seemed to be an outlier (-1.07%, -1.09%, -1.23%, -3.30%). As the duration of PID test increases, the power conversion efficiency loss gets higher.

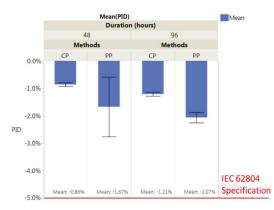


Figure 6. Distributions of 48/96 h PID testing results for the solar cells with CP and PP deposited anti-reflection coating. The red line represents the IEC 62804 specification (-5.0%).

Table 4. The 48/96 h PID testing results and EL images for the solar cells with CP and PP deposited anti-reflection coating.

Approaches	Before PID	After 48 h	After 96 h
CP method		PID -0.8%	PID -1.2%
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PP method		PID -1.2%	PID -2.2%
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The PID-resistant ability of the PP group was slightly lower than the one of the CP group. Since the oxide layer between the ARC film and Si plays an important role in the resistance of PID, the weighting of the PID-resistance ability via the PP modulated PECVD is reduced. Another reason is that the realistic deposition condition of the PP modulated PECVD is slightly away from our expectation. We thought that we had controlled the same RI value (2.07) for both groups and controlled comparable film thicknesses (of 78.6 nm (CP) and 77.9 nm (PP) by single wavelength ellipsometer at 632.8 nm). However, by taking an empirical relation of refractive index with the stoichiometry from Dauwe [35] or complemented to low-pressure PECVD from Lelièvre et al. as below [36]:

$$n = 1.22 + 0.61 \frac{[\text{Si}]}{[\text{N}]} \tag{2}$$

The empirical RI can be estimated through chemical stoichiometry of Si and N. Hence, according to our FTIR results, the film deposited by PP PECVD contains a lower Si concentration, and thus has a lower RI value than the CP method-deposited SiN_x film. Therefore, the extracted RI value by

single wavelength ellipsometer might not be that accurate, and influences this delicate experiment at the beginning.

To the best of our knowledge, we may be the first team studying PID-resistant ability through the pulsed-plasma indirect PECVD method. This additional control of freedom was realized in adjusting film properties, which was confirmed by the mentioned dilute HF etching test and FTIR measurement. The PID results of the PP method are qualified for the generalized criteria of less than -5%, and has potentially achieved lower power loss if fine-tuning the SiN_x film towards a higher RI value. In summary, we demonstrated the ARC of solar cells deposited by the PP method has advantages for higher PID demands.

4. Conclusions

The comparison of PID-resistance for the SiN_x films deposited by the direct and indirect PECVD was evaluated. After the PID test, the power conversion efficiency loss of the cell via indirect PECVD method was -33.82%, however, the loss of the cell via direct PECVD method was only -0.82%. Direct PECVD provides dense SiN_x films for increasing the PID-resistant ability. By taking the main advantage of the extremely high throughput of inline-type indirect PECVD, we demonstrated that the anti-PID ability can be much improved from -31.82% to -2.79% by introducing a thin oxide layer between indirect PECVD-deposited SiN_x film and Si through a simple pre-oxidation step. The oxide layer prevents sodium ions from accumulating at the silicon stacking faults and diminishes the possible shunting path.

Regarding to the uprising PID concern, we introduced a novel PP PECVD method for ARC deposition on PERC-type solar cells. The films made by the PP PECVD method were investigated by dilute HF etching and FTIR, and the corresponding cells were tested by PID treatments. The HF-etching rate of PP deposited SiN_x film is 2.5 nm/min, which is 2.6 times lower than that of CP deposited SiN_x film. A lower HF-etching rate indicates that the films made by the PP method contain less oxygen atoms and prevent chemical decomposition ascribed to oxidation of Na. The FTIR results consistently showed the lower oxygen content of the PP deposited SiN_x film and revealed that the PP deposited SiN_x films are thinner or have a smaller refractive index if compared to the CP deposited ones. As a result, we demonstrated the PID results of the cells with PP deposited SiN_x film were comparable to the ones with CP deposited SiN_x film, and the degradations of all cells satisfied the general criteria of the IEC 62804 specification. In addition, the involvement of pulsed plasma exhibits an extra degree of freedom to tune the film properties. Moreover, we expect the PP deposited SiN_x films, with further optimal film thickness and RI, would perform more aggressive PID-resistance than the conventional CP deposited ones.

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Conflicts of Interest: The authors declare no conflict of interest.

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Facile Solution Spin-Coating SnO₂ Thin Film Covering Cracks of TiO₂ Hole Blocking Layer for Perovskite Solar Cells

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Abstract: The hole blocking layer plays an important role in suppressing recombination of holes and electrons between the perovskite layer and fluorine-doped tin oxide (FTO). Morphological defects, such as cracks, at the compact TiO₂ hole blocking layer due to rough FTO surface seriously affect performance of perovskite solar cells (PSCs). Herein, we employ a simple spin-coating SnO₂ thin film solution to cover cracks of TiO₂ hole blocking layer for PSCs. The experiment results indicate that the TiO₂/SnO₂ complementary composite hole blocking layer could eliminate the serious electrical current leakage existing inside the device, extremely reducing interface defects and hysteresis. Furthermore, a high efficiency of 13.52% was achieved for the device, which is the highest efficiency ever recorded in PSCs with spongy carbon film deposited on a separated FTO-substrate as composite counter electrode under one sun illumination.

Keywords: perovskite solar cell; hole blocking layer; solution spin-coating; TiO₂/SnO₂ layer

1. Introduction

Currently, perovskite solar cells (PSCs) have been recognized as the most promising alternatives to conventional silicon solar cells due to high conversion efficiency, low manufacturing cost, and simple process [1–7]. As for typical planar heterojunction PSCs composed of working electrode (cathode)/hole blocking layer/perovskite layer/electron blocking layer/counter electrode (anode), the hole blocking layer plays an important role in extracting electrons from the perovskite layer and, as well as, suppressing recombination of holes and electrons between the perovskite layer and FTO [8–11]. A uniform, pinhole-free and well electrically conductive hole blocking layer is highly demanded for well performed planar heterojunction PSCs [8,12]. Liao et al. found that the pinholes on the surface of the single SnO₂ hole blocking layer coating on the rough FTO substrate were still hard to eliminate. Therefore, radio-frequency magnetron sputtering TiO₂ fully covered the surface of the FTO electrode, thus passivating the FTO surface defects and reducing the recombination, finally utilizing TiO_2/SnO_2 bilayer as hole blocking layer to improve device performance [8,13]. Furthermore, TiO₂ compact layer has commonly been used as the hole blocking layer in the planar heterojunction PSCs. Since the spin-coating process formed a highly irregular thick TiO₂ layer on top of the rough FTO layer, the pinholes appeared on the surface of the TiO₂ hole blocking layer, so that the perovskite light-absorber layer directly contacted the FTO layer, resulting in recombination of holes and electrons between the perovskite light-absorber layer and FTO layer. Though uniform and pinhole-free compact TiO₂ layers were prepared using atomic layer deposition to improve device performance, the atomic

layer deposition method had the disadvantage of including a low crystallinity of thin film due to the low deposition temperature [14]. However, Choi et al. mitigated the influence of the morphological defects (such as an irregular film thickness and poor physical contact between the TiO₂ and the FTO layers) at the TiO₂ interface due to a rough FTO by implementing a TiO₂ hole blocking layer based on the anodization method [15]. Though the research by Choi et al. mitigated the influence of the morphological defects, the preparation technology was very complicated. Up to now, several research groups have developed carbon counter electrodes to reduce the costs of perovskite devices [16–18]. In our research group, previously, the PSC based on sponge carbon/FTO composite counter electrode obtained the power conversion efficiency of 10.7% [19].

In this work, we employ TiO₂/SnO₂ complementary composite layer prepared by facile solution spin-coating SnO₂ on compact TiO₂-coated rough FTO as the hole blocking layer for planar heterojunction PSCs to solve morphological defects, such as cracks, at the compact TiO_2 hole blocking layer due to rough FTO surface. However, due to TiO_2 hole blocking layer has relative lower electron mobility, leading to unbalanced carrier transport in the device, thus regular planar structure PSC usually has a strong hysteresis behavior [20]. Meanwhile, SnO₂ is currently recognized as the promising hole blocking layer substitution for the conventional TiO₂ due to high electron mobility, low conduction band minimum, and low-temperature preparation [20–25]. Grätzel et al. and co-workers reported planar PSCs with efficiencies close to 21% using a simple, solution-processed technological approach for depositing SnO₂ layers [26]. Thereby, we obtained the modified hole blocking layer thin film without cracks through solution spin-coating SnO₂ on compact TiO₂-coated rough FTO at 3000 rpm. Correspondingly, this TiO₂/SnO₂ thin film and component optimization of perovskite precursor solution contributed to the formation of high-quality perovskite thin films (such as high crystallinity, large grain size, low defect density, and good flatness). Notably, the largest size of individual perovskite grain reached 2.67 μ m. Therefore, PSC based on the TiO₂/SnO₂ complementary composite hole blocking layer achieved high power conversion efficiencies (PCE) of 13.52% in size of 0.2 cm² under absolute ambient condition, which is the highest efficiency ever recorded in PSCs with such spongy carbon/FTO composite counter electrode. These improvements indicate that the TiO_2/SnO_2 complementary composite hole blocking layer could eliminate the serious electrical current leakage existing inside the device and reduce interface defects.

2. Materials and Methods

2.1. Materials

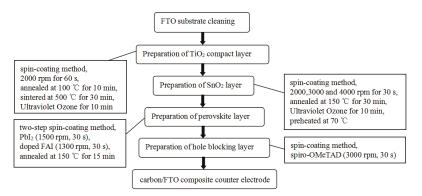
Fluorine-doped SnO₂ (FTO) substrates were obtained from Yingkou Opv Tech New Energy Co., Ltd. (Yingkou, China, 7–8 Ω /square, 2.2 mm in thickness, 1.5 \times 1.5 cm² in specification). N,N-dimethylformamide (DMF) and dimethyl sulfoxide (DMSO) were purchased from Sa'en Chemical Technology (Shanghai, China) Co., Ltd. Acidic titanium dioxide solution (bl-TiO₂) was purchased from Shanghai MaterWin New Materials Co., Ltd. (Shanghai, China, product code of MTW-CL-H-002, commodity name of HH-TiO_x, colorless and transparent in appearance, 99.98% in purity). The SnO₂ colloid precursor (Cas No. 18282-10-5) was obtained from Alfa Aesar (Shanghai, China, tin (IV) oxide, 15% in H₂O colloidal dispersion). Before use, the particles were diluted by deionized water to 3%. Lead(II) Iodide (PbI2, Cas No. 10101-63-0, yellow crystalline powder in appearance, purity >99.99%), Methylammonium iodide (CH₃NH₃I, MAI, Cas No. 14965-49-2, white powder in appearance, purity >99.5%), Formamidinium Iodide (HC(NH₂)₂I, FAI, Cas No. 879643-71-7, white powder in appearance, purity \geq 99.5%), Methylammonium Bromide (CH₃NH₃Br, MABr, Cas No. 6876-37-5, white powder in appearance, purity \geq 99.5%), Methylammonium Chloride (CH₃NH₃Cl, MACl, Cas No. 593-51-1, white powder in appearance, purity ≥99.5%), and commercial 2,2',7,7'-tetrakis-(*N*,*N*-dip-methoxyphenylamine)-9,9'-spirobifluorene solution (Spiro-OMeTAD, Cas No. 207739-72-8, yellow powder in appearance, purity \geq 99.5%) were purchased from Xi'an Polymer Light Technology Corp. (Xi'an, China).

2.2. Device Fabrication

The surface treatment of the FTO for complete coverage before deposition of any film which affect severely the film deposition and properties. Malviya et al. demonstrated that rigorous cleaning process yielded clean FTO surface, and rigorous cleaning of the substrates prior to the hematite deposition was crucial for achieving highly reproducible results [27]. In order to ensure the quality of the subsequent film deposition, we thoroughly cleaned the FTO glass substrate before proceeding to the next step. FTO substrate was firstly wiped using a mixed solution of detergent and deionized water. The resultant FTO substrates were ultrasonically cleaned with glass water (deionized water: acetone: 2-propanol = 1:1:1) and ethanol for 20 min, separately. The FTO glasses were dried with dryer for 30 min and then cleaned with ultraviolet ozone for 10 min. Compact TiO₂ layer was deposited on the cleaned FTO substrate by spin-coating an acidic titanium dioxide solution at 2000 rpm for 60 s. The substrate was annealed on a hotplate at 100 $^{\circ}$ C for 10 min, and then sintered in muffle furnace at 500 °C for 30 min. For TiO₂/SnO₂ complementary composite hole blocking layer based devices, due to the hydrophobicity of the TiO₂ thin film layer and the complete aqueous solution of the SnO₂ precursor solution, the FTO/TiO₂ substrates were firstly cleaned by ultraviolet ozone for 10 min in order to form a hydrophilic group on the surface of the film. Then the SnO₂ functional layer was prepared by spin-coating 3 wt % SnO₂ precursor solution on the compact TiO₂-coated FTO substrate for 30 s at 2000, 3000, and 4000 rpm, respectively [23]. Subsequently, the FTO/TiO₂/SnO₂ based substrates were dried on a hotplate at 150 °C for 30 min, and then cleaned by ultraviolet ozone for 10 min again to improve its hydrophilicity.

The perovskite thin film was deposited by a two-step spin-coating method [19]. Firstly, the prepared $FTO/TiO_2/SnO_2$ substrates were preheated on a hotplate at 70 °C. The precursor solution of PbI₂ was prepared by dissolving 0.5993 g PbI₂ powder in 1 mL mixture of DMF/DMSO (0.95:0.05 of volume ratio), and then spin-coated on the preheated $FTO/TiO_2/SnO_2$ substrates at 1500 rpm for 30 s. After that, the doped FAI precursor solution was prepared by mixing 60 mg FAI and 6 mg MABr and 6 mg MACl in 1 mL isopropanol, and then spin-coated on the PbI₂ layer at 1300 rpm for 30 s. In order to obtain a high-quality perovskite light-absorber layer, the spin-coated substrates were annealed on a hotplate at 150 °C for 15 min under ambient condition. The electron blocking layer was deposited on top of the perovskite layer by 3000 rpm for 30 s using Spiro-OMeTAD solution.

Finally, some cleaned FTO glasses were used as substrates to collect soot of a burning candle as spongy carbon counter electrodes. The spongy carbon/FTO composite counter electrode was then pressed on the Spiro-OMeTAD layers of uncompleted devices. The whole process is carried out in air condition with a relative humidity of 10%–20% at room temperature. The entire preparation process was described in Scheme 1.



Scheme 1. The entire process of the device fabrication.

2.3. Characterization

X-ray diffraction (XRD) data from samples of perovskite films deposited on FTO/TiO₂/SnO₂ substrates were collected using an X-ray diffractometer (D8 Focus, Bruker, Dresden, Germany). The morphology of the perovskite films were measured using a scanning electron microscope (SEM) (SIGMA, Zeiss, Jena, Germany). The photo-current density–voltage (J–V) characteristics were measured under simulated standard air-mass AM 1.5 sunlight with using a solar simulator (Sol 3A, Oriel, Newport, RI, USA). All the measurements of the PSCs were performed under ambient atmosphere at room temperature without encapsulation.

3. Results and Discussion

Figure 1 shows the top-view SEM images of the bare FTO glass substrate (Figure 1a) and 3D roughness reconstruction of bare FTO glass (Figure 1f). As we can see, the surface of the bare FTO is very rough which corresponds to Sa (arithmetic-mean-height) of 74 nm. Many cracks (marked with a red square in Figure 1b) are observed on the surface of TiO_2 thin film. Figure 1c is the enlarged SEM surface image of the red square (in Figure 1b), however, the bottom FTO can be seen through the cracks, which will cause a large number of photocarriers to be recombination and seriously affect the performance of the PSC device. As shown in the cross-sectional SEM image (Figure 1d), the poor uniformity of TiO₂ thin film and the obvious fracture (marked with a red circle in Figure 1d) which was due to surface roughness of FTO, reveals that the bare FTO surface was exposed and could form direct contact with the perovskite layer, resulting in serious recombination of holes and electrons between the perovskite layer and FTO, in agreement with the results obtained with top-view SEM images (Figure 1b,c). The cross-sectional SEM image of bare FTO layer is shown in Figure 1e, we can find that the surface of bare FTO layer was very rough due to the presence of sharp peaks. Even some peaks and valleys reached a height of ~200 nm. However, as can be seen from Figure 1d, the spin-coating process formed a highly irregular thick TiO₂ layer due to overfilling the valleys on the rough FTO surface with TiO₂. The average thickness of single-layer TiO₂ compact layer was ~100 nm, which indicated some FTO peaks higher than 100 nm could not be covered, leading to the appearance of cracks in single-layer TiO₂ thin films. This is consistent with the observation from SEM images (Figure 1b,c) of the hole blocking layer thin films prepared with single-layer TiO2 compact layer deposited on rough FTO substrates. The PSC devices based on single-layer TiO_2 hole blocking layer and double-layer TiO_2 hole blocking layer are named as device R1 and device R2, respectively. Table 1 shows the summary of J–V characteristics of device R1 and device R2 from reverse scan. As we can see, device R1 achieved low power conversion efficiency of 4.63% due to the presence of cracks. Compared with the device R1, the performance of the device R2 was improved. Huang et al. reported a facile dip-coating route to sequentially prepare a dense sol-gel-derived titanium dioxide (TiO₂) hole blocking layer and a smooth organolead halide perovskite film for pseudo-planar heterojunction perovskite solar cells [28]. Masood et al. used a scalable and low-cost dip coating method to prepare uniform and ultra-thin (5-50 nm) compact TiO₂ films on FTO glass substrates [29]. Though the dip-coating process does not require any complicated equipment and greatly minimizes the waste of source materials, enabling fast and easy production of uniform thin films, the method is not the same as our spin coating process.

Table 1. Summary of J–V characteristics of device R1 and device R2 from reverse scan.

Devices	N^{a}	$J_{\rm sc}$ ^b (mA/cm ²)	$V_{\rm oc}$ ^c (V)	FF d	PCE ^e (%)
R1	1	13.13	0.86	41.09	4.63
R2	2	18.26	0.97	54.70	9.66

Notes: ^a Number of TiO₂ spin-coating layers; ^b Short-circuit photocurrent density; ^c Open-circuit voltage; ^d Fill factor; ^e Power conversion efficiency.

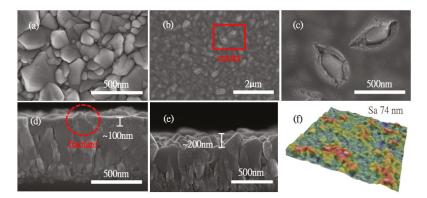


Figure 1. SEM images: (**a**) Top-view SEM image of bare FTO glass; (**b**,**c**) Top-view SEM image of TiO₂ film; (**d**) Cross-sectional SEM image of TiO₂ film; (**e**) Cross-sectional SEM image of bare FTO glass; (**f**) Top-view SEM image of 3D roughness reconstruction of bare FTO glass.

Figure 2 presents the top-view SEM images of SnO2 thin films deposited on compact TiO2-coated rough FTO for 30 s at 2000 rpm (Figure 2a,b), 3000 rpm (Figure 2c,d), and 4000 rpm (Figure 2e,f), respectively. As shown in Figure 2a,b, the cracks on the surface of the TiO_2/SnO_2 thin film were obviously filled with SnO₂ crystal grains. Due to the rotational speed being too low, a thick SnO₂ thin film formed. Thus, many cracks appeared on the surface of the SnO₂ thin film. Jiang et al. demonstrated a dense, pinhole-free film formed by spin coating SnO₂ nanoparticles solution onto glass/Indium-Tin Oxide (ITO) substrate at 3000 rpm [23]. However, in our experiment, as shown in Figure 2c,d, modified TiO₂/SnO₂ thin film without visible cracks through solution spin-coating SnO₂ on compact TiO₂-coated rough FTO at 3000 rpm formed, and is flat, uniform, and dense, which indicates the TiO_2/SnO_2 complementary composite hole blocking layer is able to fully cover the rough surface of the FTO electrode. Choi et al. demonstrated the TiO₂ film was so too thin that pinholes were observed in the TiO₂ layer, and electrons in the FTO layer easily recombined with holes due to the lack of hole blocking [15]. However, in our experiment, as the rotating speed increased to 4000 rpm, the bare FTO was exposed from a few large cracks in Figure 2e,f, which indicated that the thickness of the functional layer of SnO₂ was thinner due to the excessive spin-coating speed, and coverage of FTO/TiO₂ based substrate is incomplete. This result suggests that the direct contact between bare FTO and the perovskite light-absorber layer can cause the recombination of holes and electrons, leading to the degradation of device performance. It is consistent with the results obtained with summary of photovoltaic parameters with the J–V characteristics from reverse scan of the PSC devices based on TiO₂/SnO₂ complementary composite hole blocking layer.

However, the reasons for formation of cracks are different under high speed (4000 rpm) and low speed (2000 rpm), presented in detail in Figure 3. Figure 3 presents schematics for formation process of SnO_2 thin films at different rotational speed. Compared with situations of other rotational speed, the SnO_2 thin film from 2000 rpm was thicker, and the total amount of solution in the film was more. The solvent volatilization rate is lower during the spin coating process of 30 s, so that the solution film of SnO_2 was formed. During the annealing process of the solution film at 150 °C for 30 min, the solvent evaporated and the solution film contracted in the thickness direction, resulting in the exposure of the sharp peak of substrate, thus forming the cracks, as shown as Figure 3, corresponding to the SEM images (Figure 2a,b).

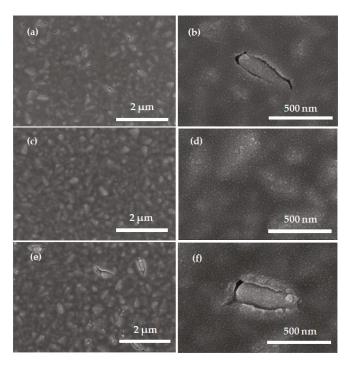


Figure 2. Top-view SEM images of SnO₂ thin films deposited on compact TiO₂-coated rough FTO at different spin-coating speeds for 30 s: (**a**,**b**) 2000 rpm; (**c**,**d**) 3000 rpm; (**e**,**f**) 4000 rpm.

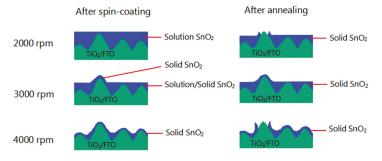


Figure 3. Schematics for formation of SnO₂ thin films at different rotational speed.

For the SnO_2 film from 3000 rpm, the solvent volatilized rate was more than the situation of SnO_2 film from 2000 rpm during the spin coating of 30 s, and the film itself was relatively thinner, thus forming a semi-solid/semi-liquid film after finishing the spin coating. In particular, the SnO_2 film at the location of the sharp peak of substrate almost became solid, thus preserving the shape at the location of the sharp peak, as shown as Figure 3, corresponding to the SEM images (Figure 2c,d).

In the process of spin-coating at 4000 rpm, the solvent volatilization was very fast, and the whole SnO_2 film was very thin and the total amount of solvent was very little, so the solid SnO_2 film had been formed after 30 s spin coating. It is worth noting that at the position of the sharp peak of substrate, the SnO_2 film was so thin that the ability to withstand strain of the film was very weak, resulting in a crack after annealing at 150 °C, as shown as Figure 3, corresponding to the SEM images (Figure 2e,f).

In addition, the film from spin coating at high speed was thinner than the one at low speed, and the film from spin coating at high speed was rougher than the one at low speed. Light trapping is a technique to improve optical absorption in the active layer of a solar cell. The rough surface can act as a light trapping structure to enhance the absorption perovskite solar cell [30–33]. However, the feature size here (<74 nm) is far less than the effective trapping sizes mentioned by previous research groups (~300 nm [30], ~6 μ m [31] and ~800 nm [32]), so that the TiO₂/SnO₂ thin film with lower roughness is not the main reason for the efficiency drop.

Figure 4 presents the cross-sectional SEM images of the TiO_2/SnO_2 complementary composite hole blocking layer with SnO_2 spin-coated on compact TiO_2 -coated FTO at 3000 rpm, which indicated the formation of modified TiO_2/SnO_2 film without visible breakages. As shown in Figure 4a, the entire film of TiO_2/SnO_2 complementary composite hole blocking layer was uniform in thickness and completely covered. Compared with single-layer TiO_2 hole blocking layer thin film, the SnO_2 thin film spin-coated on compact TiO_2 -coated rough FTO exhibited a flatter surface. Notably, as shown in Figure 4b, the TiO_2/SnO_2 complementary composite hole blocking layer also has good coverage at the protrusions of the underlying substrate and no breakage or large bulging in the protrusions could be observed. This is consistent with the observation from top-view SEM images of SnO_2 films deposited on compact TiO_2 -coated rough FTO at 3000 rpm (Figure 2c,d).

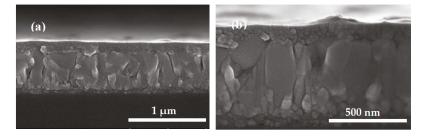


Figure 4. Cross-sectional SEM images of the TiO₂/SnO₂ complementary composite hole blocking layer with SnO₂ spin-coated on compact TiO₂-coated rough FTO at 3000 rpm: (**a**) Smaller magnification; (**b**) Larger magnification.

Figure 5 shows schematic illustration for the solution spin-coating process of TiO_2/SnO_2 complementary composite hole blocking layer. As we can see, the surface of the bare FTO was very rough due to the presence of sharp peaks (Figure 5a), corresponding to the SEM image (Figure 1e). As shown in Figure 5b, the spin-coating process formed a highly irregular thick TiO_2 layer due to overfilling the valleys on the rough FTO surface with TiO_2 , resulting in many cracks appearing on the surface of TiO_2 , and the bare FTO surface was exposed, corresponding to the SEM images (Figure 1b–d). However, as can be seen from Figure 5c, the cracks were absent from the surface of SnO_2 thin film deposited on compact TiO_2 -coated rough FTO at 3000 rpm and the SnO_2 thin film fully covered the surface of the FTO electrode, corresponding to the SEM images (Figure 2c,d). Meanwhile, the SnO_2 thin film is flat, uniform, and dense, corresponding to the SEM images (Figure 4). This result suggests that the modified TiO_2/SnO_2 complementary composite hole blocking layer is beneficial to suppressing recombination of holes and electrons between the perovskite layer and FTO and enhances the performance of devices.

XRD data of the SnO₂ thin film deposited on FTO/TiO₂ substrate were collected in Figure 6. Each of the marked peak positions in the figure (Figure 6) corresponded to the (110), (101), (200), (211), (310), (301) crystal planes of the SnO₂ crystal, which was in consistent with the results of the previous report [23] about XRD pattern of the SnO₂ material, indicating SnO₂ thin film composite counter electrodes had been successfully deposited on the FTO/TiO₂ substrate.

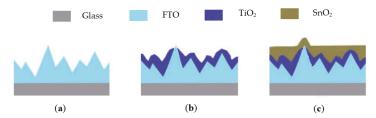


Figure 5. Schematic illustration for the solution spin-coating process of TiO_2/SnO_2 complementary composite hole blocking layer: (**a**) The bare FTO substrate; (**b**) TiO_2 thin film deposited on rough FTO substrate; (**c**) SnO_2 thin film deposited on compact TiO_2 -coated rough FTO at 3000 rpm.

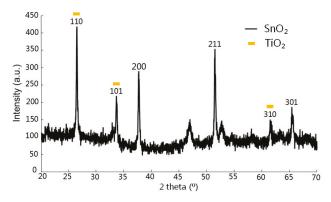


Figure 6. XRD pattern of SnO₂ thin film deposited on FTO/TiO₂ substrate.

Figure 7 presents top-view SEM images (Figure 7a,b) and cross-sectional SEM image (Figure 7c) of perovskite thin films deposited on TiO₂/SnO₂ of solution spin-coating SnO₂ on compact TiO₂-coated rough FTO at 3000 rpm, respectively. From Figure 7a,b, it can be seen that the entire perovskite film was high-quality and quite uniform free of cracks. However, high-quality perovskite film is essential for the performance of planar PSCs, as it can avoid the direct contact of hole blocking layer and electron blocking layer [20]. It is worth noting that the individual grain size of perovskite crystals was especially large, and the largest grain size reached a rare 2.67 μ m. Furthermore, due to the passivation of the doping, the grain boundary was too smooth, which reduced defects of grain boundaries in the perovskite film to a great extent. From the cross-sectional SEM image (Figure 7c), it can be found that the entire perovskite film was composed of single layer of large grains and uniformly dense, which is coincident with the morphology of the film on the top-view SEM images (Figure 7a,b).

Figure 8 displays the XRD pattern of the perovskite thin film deposited on $FTO/TiO_2/SnO_2$ substrate in the case of spin-coating SnO_2 at 3000 rpm. Obviously, the XRD pattern presents strong and sharp (101) and (200) diffraction peaks at 14.02° and 28.32° , demonstrating the good crystallinity of perovskite film, which is consistent with the SEM results (Figure 7) of the large-grain-size perovskite film. The perovskite grains of good crystallinity effectively enhance the efficiency of injection of photo-carriers of the perovskite light-absorber layer into the hole blocking layer and electron blocking layer, thereby further improving the overall performance of the PSC device.

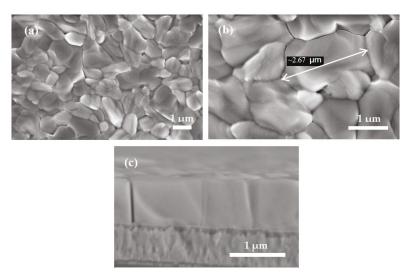


Figure 7. SEM images: (a,b) Top-view SEM images of FTO/TiO_2/SnO_2/perovskite; (c) Cross-sectional SEM image of FTO/TiO_2/SnO_2/perovskite.

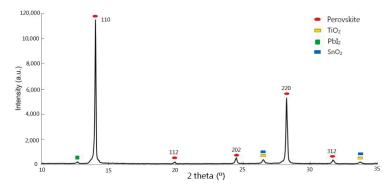


Figure 8. XRD pattern of the perovskite thin film deposited on $FTO/TiO_2/SnO_2$ substrate in the case of spin-coating SnO_2 at 3000 rpm.

Figure 9 shows energy bandgap diagram for TiO_2/SnO_2 based PSC, the shift of conduction band is not the main reason for the efficiency drop [34].

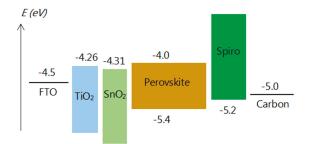


Figure 9. Energy bandgap diagram for TiO₂/SnO₂ based perovskite solar cells.

Figure 10 shows the *J*–*V* curves from reverse scan (RS) and forward scan (FS) for the PSC devices based on TiO_2/SnO_2 complementary composite hole blocking layer under different SnO_2 spin-coating speeds, measured under simulated sunlight with intensity of 100 mW cm⁻² (AM 1.5 G). Obviously, when the SnO_2 spin-coating speed was 3000 rpm, the RS and FS curves of the device basically coincided and the hysteresis phenomenon basically disappeared, which matches the thin film morphology seen from the top-view SEM images (Figure 7a,b). When the SnO_2 spin-coating speeds were 2000 and 4000 rpm, a SnO_2 functional layer that was wither too thick or too thin could not match well with the TiO_2 compact layer to form modified TiO_2/SnO_2 complementary composite hole blocking layer. This led directly to a drop in the optoelectronic performance of the device. The presence of cracks also caused serious electrical current leakage existing inside the device, resulting the PSC devices under these two processes having different degrees of hysteresis.

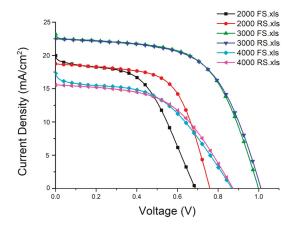


Figure 10. The *J*–*V* curves from reverse scan (RS) and forward scan (FS) for the PSC devices based on TiO_2/SnO_2 complementary composite hole blocking layer under different SnO_2 spin-coating speeds, measured under simulated sunlight with intensity of 100 mW cm⁻² (AM 1.5 G).

Table 2 shows summary of J-V characteristics from RS of the PSC devices based on TiO₂/SnO₂ complementary composite hole blocking layer under different SnO₂ spin-coating speeds. The best cell based on TiO₂/SnO₂ complementary composite hole blocking layer under the SnO₂ spin-coating speed of 3000 rpm obtained a PEC of 13.52% corresponding to a J_{sc} of 22.48 mA cm⁻², a V_{oc} of 1.01 V and a FF of 59.51. Although this efficiency is not the highest in PSCs, it is the highest efficiency ever recorded in PSCs with such spongy carbon/FTO composite counter electrode, and furthermore, the preparation techniques of high-quality perovskite thin films and the cheap spongy carbon/FTO composite counter electrode under absolute ambient condition are beneficial for large-scale applications and commercialization. At the same time, since the problem of the defect at the interface between the hole blocking layer and the perovskite light-absorber layer was solved, the hysteresis phenomenon of the entire device was well solved.

Table 2. Summary of J-V characteristics from reverse scan of the PSC devices based on TiO₂/SnO₂ complementary composite hole blocking layer under different SnO₂ spin-coating speeds.

RSSC ^a (rpm)	$J_{\rm sc}$ ^b (mA/cm ²)	$V_{\rm oc}$ ^c (V)	FF ^d	PCE ^e (%)
2000	18.74	0.76	61.95	8.81
3000	22.48	1.01	59.51	13.52
4000	15.56	0.87	52.22	7.10

Notes: ^a Rotating speed of spin-coating SnO₂; ^b Short-circuit photocurrent density; ^c Open-circuit voltage; ^d Fill factor; ^e Power conversion efficiency.

4. Conclusions

In summary, we optimized a rotational speed of spin-coating SnO_2 at 3000 rpm to cover the cracks of compact TiO₂-coated on rough FTO. Using composite layered TiO₂/SnO₂ can reduce hysteresis behavior due to an effectively suppressed recombination of holes and electrons between the perovskite layer and FTO. Meanwhile, as a result, we achieved high-quality perovskite thin films and high efficiency of 13.52% for devices with spongy carbon/FTO composite counter electrode. This work highlights the preparation process of modified hole blocking layer in PSC and has a certain reference significance for perovskite based opto-electronic devices.

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Conflicts of Interest: The authors declare no conflicts of interest.

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Review



Review of $CdTe_{1-x}Se_x$ Thin Films in Solar Cell Applications

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Abstract: Recent improvements in CdTe thin film solar cells have been achieved by using $CdTe_{1-x}Se_x$ as a part of the absorber layer. This review summarizes the published literature concerning the material properties of $CdTe_{1-x}Se_x$ and its application in current thin film CdTe photovoltaics. One of the important properties of $CdTe_{1-x}Se_x$ is its band gap bowing, which facilitates a lowering of the CdTe band gap towards the optimum band gap for highest theoretical efficiency. In practice, a $CdTe_{1-x}Se_x$ gradient is introduced to the front of CdTe, which induces a band gap gradient and allows for the fabrication of solar cells with enhanced short-circuit current while maintaining a high open-circuit voltage. In some device structures, the addition of $CdTe_{1-x}Se_x$ also allows for a reduction in CdS thickness or its complete elimination, reducing parasitic absorption of low wavelength photons.

Keywords: CdTe; CdSe; CdTe_{1-x}Se_x; photovoltaics; solar cells; review

1. Introduction

With a global drive towards renewable energies, photovoltaics is an increasing part of global energy supply. CdTe is the leading technology amongst thin film solar cells for cost effective solar electricity production, due to its high photovoltaic conversion efficiency, long-term performance stability, low fabrication costs and short energy-payback time [1]. The current efficiency record for CdTe cells is 22.1%, held by First Solar [2,3].

In state-of-the-art CdTe solar cells, the J_{SC} is already close to its theoretical limit [4]. According to the Shockley–Queisser thermodynamic limit to solar cell efficiency, the optimum band gap for maximum theoretical solar cell efficiency under AM 1.5 G is 1.34 eV [5,6]; the band gap of CdTe is slightly too wide at 1.5 eV [4]. Strategies to shift the band gap of the CdTe absorber towards the theoretical optimum can help to further increase photocurrent and, consequently, the efficiency. CdTe_{1-x}Se_x is a promising material for this purpose, as its band gap can be shifted down to 1.4 eV [7,8] by appropriately adjusting the composition. First Solar's world record cell efficiency was improved from 19.5% to 22.1% using an absorber with a lower band gap than CdTe, the CdTe_{1-x}Se_x alloy [9–11].

With an absorber material that has an adjustable band gap, the band gap profile through the absorber layer can be engineered by applying a compositional grading. Different research groups have been investigating the use of a $CdTe_{1-x}Se_x$ layer towards the front of a CdTe absorber layer, resulting in champion devices with improved J_{SC} due to higher absorption in the low-band gap front layer, while maintaining the V_{OC} from the bulk CdTe [8,12–17].

For traditional CdS/CdTe solar cells, a CdCl₂ treatment, generally consisting of deposition of CdCl₂ on the absorber and subsequent heating, is needed to recrystallize the absorber layer, resulting in increased CdTe grain size and intermixing of CdS and CdTe as well as modifications in electronic properties leading to enhancement in photovoltaic conversion efficiency [18]. If a CdSe or CdTe_{1-x}Se_x layer is inserted in between CdS and CdTe, interdiffusion during CdCl₂ treatment results in a CdTe_{1-x}Se_x

layer. Because $CdTe_{1-x}Se_x$ has no miscibility gap, a continuous composition gradient is formed, with an associated band gap gradient [15,19], allowing for absorption of high-wavelength photons. Several research groups have also found that, with the use of a $CdTe_{1-x}Se_x$ front layer, the CdS window layer thickness can be reduced, or the CdS layer can even be omitted completely, reducing parasitic absorption in the short-wavelength region and further increasing J_{SC} [8,14,20]. A thick CdS layer is generally required to avoid direct contact between the transparent conducting oxide (TCO) and the CdTe absorber, but a $CdTe_{1-x}Se_x$ absorber seems to be less sensitive to this issue. Further improvement was achieved by replacing CdS with MgZnO, which has a more favorable band alignment with both CdTe and $CdTe_{1-x}Se_x$ than CdS, and which is more transparent in the short-wavelength region [15,21,22]. Additionally, passivation of defects due to Se has been reported to be responsible for the higher carrier lifetimes in CdTe_{1-x}Se_x compared to CdTe [19,23].

CdTe technology has shifted in recent years from a traditional CdS/CdTe structure to a device structure that utilizes a $CdTe_{1-x}Se_x$ layer and a band gap gradient, but no CdS layer, in order to achieve high currents and voltages. In this review paper we discuss the steps of this transformation, from the first introduction of a $CdTe_{1-x}Se_x$ layer to the complete replacement of the CdS layer by MgZnO and $CdTe_{1-x}Se_x$. We discuss the material properties of $CdTe_{1-x}Se_x$ and their dependence on composition and the application of this material in thin-film solar cells.

2. Growth of CdTe_{1-x}Se_x Thin Films and Material Properties

In this section, we will discuss the deposition of $CdTe_{1-x}Se_x$ films and their structural, optical and electronic properties.

 $CdTe_{1-x}Se_x$ is a solid solution without a miscibility gap; the alloy is stable over the complete composition range $0 \le x \le 1$. Thin films of desired composition can be grown with a variety of methods, such as high-vacuum evaporation of the elements [24] or the alloy $CdTe_{1-x}Se_x$ [25,26], co-evaporation of CdTe and CdSe [8,27], close space sublimation of the alloy $CdTe_{1-x}Se_x$ [23,28] or co-sublimation of the components CdTe and CdSe [29], molecular beam epitaxy [30,31], hot wall deposition [32], electron beam deposition [7,33], or electrodeposition [34,35]. The properties of grown layers depend on the deposition method and the conditions used.

In solar cells, the main methods used for $CdTe_{1-x}Se_x$ formation are high-vacuum evaporation [8] or radio frequency sputtering [14,16,20] of a CdSe layer next to a CdTe layer, with interdiffusion during $CdCl_2$ treatment, or close space sublimation of a $CdTe_{1-x}Se_x$ layer next to a CdTe layer [15], which also interdiffuse during $CdCl_2$ treatment. Close space sublimation is performed at higher temperatures than high-vacuum deposition or sputtering, and in CdTe it results in very large grains. The lower deposition temperature of high-vacuum evaporation results in smaller as-deposited grains. However, recrystallization during $CdCl_2$ treatment results in overall comparable grain sizes between different deposition methods [36]. The properties of $CdTe_{1-x}Se_x$ are therefore expected to depend on deposition parameters as well as $CdCl_2$ treatment conditions.

2.1. Crystal Structure

CdTe crystallizes in the cubic zinc blende structure, while CdSe crystallizes in the hexagonal wurzite structure. The two structures are closely related; each Cd²⁺ ion is surrounded by a tetrahedron of four Se²⁻ and/or Te²⁻ ions. In the solid solution CdTe_{1-x}Se_x, both the zinc blende and the wurzite structure have been reported [16,34,37–39]. For $0.2 \le x \le 0.5$, cubic zinc blende is the low-temperature structure, with a transition to hexagonal wurzite at temperatures above 800 °C. This transition temperature decreases with increasing *x*, and at *x* = 0.6 the hexagonal wurzite structure is formed at 600 °C [16,37]. With appropriate deposition parameters, mainly dependent on substrate temperature, the entire composition range of CdTe_{1-x}Se_x can be fabricated in the zinc blende structure. In this structure, the lattice constant *a* decreases with increasing *x*, following Vegard's law, due to the smaller size of Se²⁻ compared to Te²⁻ [7,33,40,41]. The wurzite structure can occur at room temperature for *x* = 0.3 and higher, sometimes mixed with the zinc blende structure [34,38,39]. In solar cell applications,

the zinc blende structure is desired, as it is photoactive, i.e., it can convert light into photovoltaic current, while the wurzite structure is not photoactive [16].

2.2. Optical Properties

 $CdTe_{1-x}Se_x$ has a direct band gap with a pronounced bowing behavior. Figure 1 shows reported band gaps of $CdTe_{1-x}Se_x$ thin films measured with different methods, as well as one band gap bowing derived from first-principles DFT calculations, all showing a similar bowing behavior trend. The bowing parameter *b* can be extracted from experimental data with a second-degree polynomial fit. The band gap of any composition *x* can then be calculated using Equation (1) [42]:

$$E_G(x) = x \cdot E_G^{CdSe} + (1-x) \cdot E_G^{CdTe} - b \cdot x \cdot (1-x)$$
(1)

Band gap bowing parameters from bulk and thin-film $CdTe_{1-x}Se_x$, fabricated by different methods and using different measurement techniques, are listed in Table 1. The published bowing parameter values cover a range of 0.56–0.97, and they all agree on the composition of the band gap minimum at $0.3 \le x \le 0.4$, independent of fabrication method. The bowing only marginally depends on the crystal structure [39]. The band gap determination using photoluminescence and cathodoluminescence seem to yield bowing parameters slightly higher than transmittance/reflectance measurements, but they are still in good agreement [31].

Theoretical calculations using different methods are also shown in Table 1, and they seem to be in good agreement with experimental data [42–44]. The band gap minima in all experiments and calculations are around 1.4 eV, confirming that $CdTe_{1-x}Se_x$ is a good candidate for band-gap engineering in CdTe solar cells for the purpose of increasing J_{SC} .

In $CdTe_{1-x}Se_x$, the valence band edge is dominated by Se and Te p-orbitals, and the conduction band edge is dominated by Cd s- and p-states. Therefore, the anion substitution would be expected to primarily affect the valence band edge [43,45]. However, first-principles calculations show that the bowing of the band gap is caused by the bowing of both band edges due to strong intra-band coupling in both the valence and the conduction band [44].

The refractive index of $CdTe_{1-x}Se_x$ is almost constant over a large range of wavelengths, as well as with changes in composition and film thickness. Use of a $CdTe_{1-x}Se_x$ layer is therefore not expected to change the overall reflectance of a solar cell, and the introduction of a $CdTe_{1-x}Se_x$ gradient does not introduce a gradient in the refractive index [7,25,32].

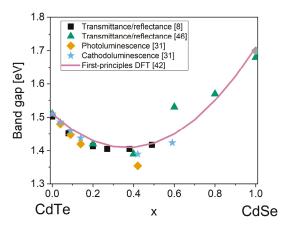


Figure 1. Band gap bowing of $CdTe_{1-x}Se_x$ measured by different methods [8,31,46] and calculated from first-principles DFT [42].

Source	Deposition	Band Gap Determination	Crystal Structure	x Range	Bowing Parameter	x of Band Gap Minimum	Band Gap Minimum
[39]	Sintering of mixed CdTe and CdSe powders	Transmittance/reflectance	zinc blende	0-0.6	0.74	0.35	1.38
[39]	Sintering of mixed CdTe and CdSe powders	Transmittance/reflectance	wurzite	0.4–1	0.68	0.33	1.4
[8]	Co-evaporation of CdTe and CdSe	Transmittance/reflectance	zinc blende	0-0.5	0.78	0.37	1.39
[7]	Electron-beam evaporation	Transmittance/reflectance	zinc blende	0–1	0.567	0.37	1.44
[46]	Thermal evaporation of mixed CdTe and CdSe powders	Transmittance/reflectance	zinc blende	0–1	0.571	0.35	1.44
[31]	Molecular beam epitaxy on Si	Photoluminescence	zinc blende	0–1	0.97	0.40	1.35
[31]	Molecular beam epitaxy on Si	Cathodoluminescence	zinc blende	0–1	0.82	0.38	1.39
[42]	-	First-principles DFT calculations	zinc blende	0–1	0.75	0.40	1.41
[43]	-	sp ³ s* tight-binding method calculations	zinc blende	0–1	0.904	0.39	1.37
[44]	-	First-principle hybrid-functional calculations	zinc blende	0–1	0.725	0.39	1.43

Table 1. Band gap bowing parameters of layers and powders synthesized with different methods.

2.3. Electronic Properties

The electronic properties of $CdTe_{1-x}Se_x$ have not been studied extensively. As-deposited $CdTe_{1-x}Se_x$ is an n-type semiconductor with carrier densities between 10^{13} cm⁻³ (CdTe) and 10^{18} cm⁻³ (CdSe) [40]. The Hall mobility increases by less than an order of magnitude between CdTe and CdSe. Both carrier density and mobility are dependent on deposition temperature, with higher values at higher deposition temperatures due to increased grain size and possibly a reduction in structural defects [26,40]. In solar cell processing, the CdTe_{1-x}Se_x layer is subjected to a CdCl₂ treatment, during which it recrystallizes. In CdTe, the recrystallization results in larger grains, reduced structural defects, and reduced recombination [18,47]. A similar effect is expected for CdTe_{1-x}Se_x. In absorbers consisting of a CdTe_{1-x}Se_x layer in front of CdTe, recrystallization during CdCl₂ treatment has been shown to be responsible for a reduction in stacking faults, combined with interdiffusion of the CdTe_{1-x}Se_x and CdTe layers [19,28].

In solar cells that use $CdTe_{1-x}Se_x$ as part of the absorber layer, dopants are generally added to the whole $CdTe_{1-x}Se_x/CdTe$ stack and permeate the $CdTe_{1-x}Se_x$ layer via diffusion. A commonly used extrinsic dopant is copper, which forms deep acceptors as Cu on a Cd site (Cu_{Cd}) [48,49]. First-principles calculations indicate that the formation energy of this acceptor defect exhibits a bowing, with lower formation energies in the $CdTe_{1-x}Se_x$ solid solution than in either parent compound [44]. In the mixed alloy, the bonding Te orbitals are partially replaced with Se orbitals, which have a lower energy. The electronic effects of this change in bonding orbitals are one reason for the bowing behavior. Another reason is the smaller lattice constant with increasing *x* leading to reduced compressive strain when Cd is replaced by the much smaller Cu [44]. The reduced formation energy indicates better dopability of $CdTe_{1-x}Se_x$ with copper compared to CdTe. However, Hall effect measurements of $CdTe_{1-x}Se_x$ with $0 \le x \le 0.2$, deposited by high-vacuum evaporation and subjected to a $CdCl_2$ treatment, revealed that the achievable doping concentration is lower in Se-containing samples, with more than an order of magnitude difference between CdTe and x = 0.2 [8]. A possible explanation is that compensating donors, such as copper on interstitial sites (Cu_i), are formed as well, and that the formation energy of

these defects is also dependent on *x*. If the electronic and/or structural effects of $CdTe_{1-x}Se_x$ alloying facilitate the formation of compensating donors more than the formation of acceptor defects, the result is a limit to the achievable hole density [8,49,50].

The photoluminescence decay of $CdTe_{1-x}Se_x$ measured by time-resolved photoluminescence (TRPL) is generally dominated by surface recombination, resulting in short apparent lifetimes [23,51]. In order to get a reliable measure for the bulk minority carrier lifetime, the surface has to be passivated, e.g., using Al₂O₃, which provides field-effect passivation [52]. Another approach is two-photon excitation (2PE) TRPL, which allows for lifetime measurements at a selected depth of the absorber [51,53]. In CdTe_{1-x}Se_x layers (x = 0.2, deposited by close space sublimation and subjected to CdCl₂ treatment) with both surfaces passivated by sputtered Al_2O_3 , lifetimes of up to 430 ns were measured, an order of magnitude higher than lifetimes in similarly passivated CdTe [23]. The reason seems to be that Se passivates a deep defect in the bulk of the absorber, even at low concentrations [19]. This is also correlated with longer diffusion length in material with higher x [13,19]. Two-photon excitation TRPL measurements performed on an interdiffused $CdTe_{1-x}Se_x/CdTe$ absorber (close space sublimation, CdCl₂ treated, resulting maximum Se content $x \approx 0.16$) have shown lifetimes of around an order of magnitude higher in the Se-rich front layer compared to the CdTe back layer. This lifetime difference within a single absorber was linked to reduced recombination at the grain boundaries in the Se-containing region [51,53]. Se therefore, at least up to $x \approx 0.2$, seems to provide both passivation of a bulk defect and of the grain boundaries, resulting in an overall increased lifetime. Further studies are needed to accurately determine the lifetime dependence with x, and to determine the steepness of the lifetime gradient in an interdiffused $CdTe_{1-x}Se_x/CdTe$ absorber.

The various deposition methods used for CdSe or $CdTe_{1-x}Se_x$ apply a variety of substrate temperatures and deposition rates. We expect that the reported properties of $CdTe_{1-x}Se_x$ may depend on deposition method as well as on the parameters of the CdCl₂ treatment, but further investigations are needed to determine the extent.

3. $CdTe_{1-x}Se_x$ in Solar Cells

In recent years, $CdTe_{1-x}Se_x$ has been used as a layer at the front of a predominantly CdTe absorber layer (see Figure 2), either deposited as CdSe or as $CdTe_{1-x}Se_x$, which interdiffuse with CdTe during CdCl₂ treatment to form a continuous composition gradient. This results in an absorber layer with a low band gap, increasing the J_{SC} , and it allows for a reduction in CdS thickness, both in superstrate and substrate configuration. As a further step, Munshi et al. [15] replaced the CdS with MgZnO for the highest device efficiencies. Schematics of the different device configurations in which $CdTe_{1-x}Se_x$ layers have been used are shown in Figure 2, from $CdS/CdTe_{1-x}Se_x/CdTe$ (Figure 2b), to $CdTe_{1-x}Se_x/CdTe$ (Figure 2c), to $MgZnO/CdTe_{1-x}Se_x/CdTe$ (Figure 2d). As an alternative to the conventional superstrate configuration, a device in substrate configuration (Figure 2e) is discussed as well.

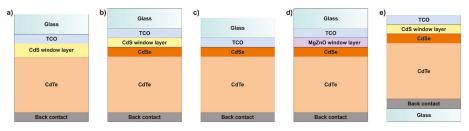


Figure 2. Schematics of deposited layers for solar cells (intermixing not depicted, thicknesses not to scale) for (**a**) a conventional CdTe device, (**b**) a device with a CdSe layer between CdTe and CdS [20]; (**c**) a device with CdSe replacing CdS [14,16]; (**d**) a device with MgZnO and CdSe replacing CdS [15]; and (**e**) a device in substrate configuration with a CdSe layer between CdTe and CdS [8].

The best reported devices for each of the different structures in Figure 2 are listed in Table 2, as well as the CdTe_{1-x}Se_x-containing record device by First Solar. By removing the CdS layer, a small increase in J_{SC} and FF has been shown, due to reduced parasitic absorption of CdS, at the cost of some losses in V_{OC} , due to interface recombination at the TCO/CdTe_{1-x}Se_x interface [20]. With a MgZnO window layer, all device parameters could be improved: high J_{SC} due to the absence of parasitic absorption in the window layer, and high V_{OC} and FF due to a good band alignment between MgZnO and CdTe_{1-x}Se_x, resulting in a power conversion efficiency of 19.1% [15]. For the substrate configuration device, while the FF is comparable to superstrate devices, the V_{OC} and J_{SC} are lower. The loss in V_{OC} may be due to interface recombination at the CdS/CdTe_{1-x}Se_x interface; the loss in J_{SC} due to parasitic absorption in the remaining CdS layer [8]. The world record device from First Solar surpasses all other devices in terms of V_{OC} and J_{SC} , and only the MgZnO/CdTe_{1-x}Se_x device can exceed its FF. The exact structure and therefore the reasons for this outstanding performance are not public knowledge, but the high J_{SC} and V_{OC} indicate the use of MgZnO or a similar window layer [3,9,10].

Table 2. *J-V* parameters of the best $CdTe_{1-x}Se_x$ -containing devices for each configuration shown in Figure 2.

Source	Device Structure	V _{OC} [mV]	Jsc [mA/cm ²]	FF [%]	Efficiency [%]
Paudel and Yan [20]	Figure 2b	806	27.2	64.1	14.1
Paudel and Yan [20]	Figure 2c	771	27.5	69.4	14.7
Munshi et al. [15]	Figure 2d	854	28.4	79.1	19.1
Lingg et al. [8]	Figure 2e	710	25.6	67	12.2
First Solar [3,9,10]	unknown	887.2	31.69	78.5	22.1

In the following section, we will first discuss the deposition methods used to form a $CdTe_{1-x}Se_x/CdTe$ solar cell absorber, and in subsequent subsections we will discuss the details of how $CdTe_{1-x}Se_x$ has been used to improve performance in devices with different configurations.

3.1. Formation of a $CdTe_{1-x}Se_x$ Layer during Device Processing

Different deposition methods have been used to form a $CdTe_{1-x}Se_x$ layer. In conventional superstrate configuration, CdSe can be deposited by high-vacuum evaporation [27], magnetron sputtering [14,16,47], or pulsed laser deposition [54], with $CdTe_{1-x}Se_x$ formation during $CdCl_2$ treatment. An alternative is close-space sublimation (CSS) of a $CdTe_{1-x}Se_x$ layer [15,19,29]. The CdSe or $CdTe_{1-x}Se_x$ layer is followed by deposition of CdTe, $CdCl_2$ and doping treatments, and back contact deposition.

For devices in substrate configuration, a CdSe layer is deposited onto CdTe, followed by CdCl₂ and doping treatments and window layer/front contact deposition (see Figure 2e) [8].

In all of these device structures, the absorber and window layer are recrystallized and the $CdSe/CdTe_{1-x}Se_x$ interdiffuse with the CdTe during $CdCl_2$ treatment. In an as-deposited $CdTe_{1-x}Se_x$ and CdTe absorber, a large number of small grains towards the front ($CdTe_{1-x}Se_x$) and increasing grain size towards the back are observed, but after the $CdCl_2$ treatment, the grains are uniform in size and no distinct boundary is visible between $CdTe_{1-x}Se_x$ and CdTe [28]. Scanning transmission electron microscopy (STEM)/energy-dispersive x-ray spectroscopy (EDS) mapping reveals interdiffusion of $CdTe_{1-x}Se_x$ and CdTe, with Se diffusing more than a µm into the CdTe layer [15,28]. Secondary ion mass spectrometry (SIMS) reveals accumulation of Se at grain boundaries in the CdTe layer, and a relative loss of Se at grain boundaries in the $CdTe_{1-x}Se_x$ layer, which is a strong indication for a combination of fast diffusion of Se along the grain boundaries and slow diffusion into the grains [19].

Any photons with energies above the CdTe band gap ($\geq 1.5 \text{ eV}$) are absorbed in the CdTe_{1-x}Se_x layer or in the CdTe absorber underneath. CdTe_{1-x}Se_x has a lower band gap than CdTe (down to 1.4 eV), and it therefore absorbs photons that cannot be absorbed by CdTe. To maximize J_{SC} gain, the CdTe_{1-x}Se_x layer has to be sufficiently thick to absorb the majority of these photons with energies

below the CdTe band gap. If it is formed from CdSe, the composition of the $CdTe_{1-x}Se_x$ layer after interdiffusion depends on the thickness of the deposited CdSe layer as well as on the annealing conditions. Yan et al. found that for CdSe layers up to 100 nm thick, the interdiffusion is sufficient to result in a completely photoactive zinc blende absorber with compositions of $x \le 0.65$. For thicker layers, a non-photoactive wurzite layer with x > 0.65 remains at the front of the absorber, which is undesirable because of parasitic absorption. With this method, it is difficult to achieve a thick photoactive layer for full absorption without formation of a non-photoactive layer [16,20,47]. Forming the CdTe_{1-x}Se_x layer by depositing CdTe_{1-x}Se_x with $x \le 0.65$ instead of CdSe allows for a higher overall Se content in the absorber because the risk of forming a non-photoactive wurzite layer is minimized, and thick photoactive low-band gap layers can be formed [15].

The interdiffusion of $CdTe_{1-x}Se_x$ and CdTe creates a compositional gradient, which is expected to be correlated to the gradient in the material properties of $CdTe_{1-x}Se_x$, such as band gap, lattice constant, charge carrier concentration, and minority carrier lifetime. In particular, Fiducia et al. [19] reported gradients in both band gap and diffusion length (determined from cathodoluminescence measurements) that are directly correlated with the Se concentration gradient in a $CdTe_{1-x}Se_x/CdTe$ device.

3.2. Overview of Device Performances with $CdTe_{1-x}Se_x$

Different research groups have had varying success in improving device performance using CdSe. Published device parameters are listed in Table 3, where the parameters are compared with reference devices without CdSe. Generally, the J_{SC} could be improved by the reduced band gap and by reducing or removing the CdS layer. V_{OC} losses are partially due to the reduced band gap. Further V_{OC} losses together with fill factor losses have been mostly attributed to interface recombination, but they were not further investigated. The highest V_{OC} was achieved by use of a MgZnO window layer instead of CdS. The deposition methods are also listed as they may have an influence on the material properties and device performance. The different approaches and results are discussed in the following subsections.

Source	Device Structure		J _{SC} [mA/cm ²]	FF [%]	Efficiency [%]
	CdSe (100 nm, RFS)/CdTe (CSS)	770	27	60.2	12.6
Poplawsky et al. [16]	CdS (130 nm, RFS)/CdTe (CSS)	810	23.8	75.4	14.5
	difference with CdSe	-40	+3.2	-15.2	-1.9
	CdSe (100 nm, RFS)/CdTe (CSS)	690	26.9	64.8	12.1
Mia et al. [14]	CdS (140 nm, RFS)/CdTe (CSS)	847	24.7	70	14.6
	difference with CdSe	-157	+2.2	-5.2	-2.5
	CdSe (100 nm RFS)/CdTe (CSS)	771	27.5	69.4	14.7
	CdS (15 nm, RFS)/CdSe (100 nm, RFS)/CdTe (CSS)	806	27.2	64.1	14.1
Paudel and Yan [20]	CdS (130 nm, RFS)/CdTe (CSS)	811	24.2	75.5	14.8
	difference only CdSe	-40	+3.3	-6.1	-0.1
	difference mixed CdS/CdSe	-5	+3	-11.4	-0.7
	CdS (30 nm)/CdSe (60 nm)/CdTe (all HVE, substrate config.)	710	25.6	67	12.2
pLingg et al. [8]	CdS (120 nm)/CdTe (all HVE, substrate config.)	830	18.5	69.4	10.5
	difference with CdSe	-120	+7.1	-2.4	+1.7
Munchi et al. [15]	MgZnO (RFS)/CdTe _{0.8} Se _{0.2} (800 nm, CSS)/CdTe (CSS)	854	28.4	79.1	19.1
Munshi et al. [15]	MgZnO (RFS)/CdTe (CSS)	860	26.3	78.9	17.9
	difference with CdSe	-6	+2.1	+0.2	+1.2
	CdTe _{1-x} Se _x /CdTe *	887.2	31.69	78.5	22.1
First Solar [3,9,10]	CdS/CdTe *	875.9	30.25	79.4	21
	difference with CdSe	+11.3	+1.44	-0.9	+1.1

Table 3. *J-V* parameters of devices containing CdSe compared with non-CdSe devices. Deposition methods are abbreviated as RFS (radio frequency sputtering), CSS (close space sublimation), and HVE (high vacuum evaporation).

* The exact device structures and methods of deposition used in the First Solar record devices are not public knowledge.

3.3. CdSe/CdTe Devices without a Window Layer

The performance of devices where the CdS window layer is completely substituted by a CdSe layer (Figure 2c) depends strongly on the thickness of the CdSe layer. Up to 100 nm thick CdSe layers completely interdiffuse with the CdTe during CdCl₂ treatment, forming photoactive zinc blende $CdTe_{1-x}Se_x$. This results in increased J_{SC} compared to CdS/CdTe devices (see Figure 3) on the one hand because of increased absorption in the long-wavelength region due to a reduced band gap of the absorber, and on the other hand because the absorbing CdS layer is eliminated (see Figure 4). The overall efficiency however is still reduced because of losses in V_{OC} and FF.

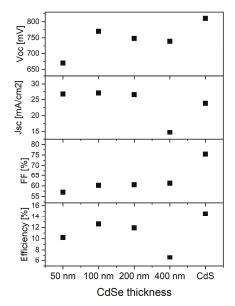


Figure 3. Performance of CdSe/CdTe solar cells with different CdSe thicknesses (values taken from Poplawsky et al. [16]).

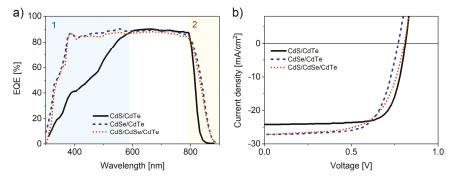


Figure 4. External quantum efficiency (EQE) (**a**) and *J*-*V* (**b**) curves of solar cells with different window layers (adapted from [20]).

With thicker CdSe layers, the interdiffusion is not complete, and the J_{SC} is reduced due to parasitic absorption in residual non-photoactive wurzite $CdTe_{1-x}Se_x$ with high Se content (x > 0.65). With optimized CdSe thickness, the J_{SC} can be increased by more than 3 mA/cm², however, this is not

sufficient to offset the losses in V_{OC} , which are attributed to high interface recombination at the direct contact between $\text{CdTe}_{1-x}\text{Se}_x$ and TCO [16,20].

The TCO used in CdTe and $CdTe_{1-x}Se_x/CdTe$ devices is usually a bilayer of a low-resistivity material, such as SnO₂:F (FTO), and a high-resistivity material, such as SnO₂. The highly resistive transparent (HRT) layer is used to prevent direct contact between the absorber and the FTO in the case of incomplete CdS coverage [55]. Baines et al. [12] investigated different oxides as HRT layers for CdTe_{1-x}Se_x absorbers and found SnO₂ to be the best. It reduces V_{OC} losses that occur from direct contact of CdTe_{1-x}Se_x with FTO, but the interface recombination is still higher than with a CdS layer [12,20]. In fact, the devices listed in Table 3 all use a SnO₂ HRT layer.

With electron-beam induced current (EBIC) measurements the position of the junction can be determined: for up to 100 nm CdSe, the junction is located at the $CdTe_{1-x}Se_x/TCO$ interface. This reveals that the $CdTe_{1-x}Se_x$ does not act as a window layer, but as part of the p-side of the junction. For thicker CdSe layers, the junction is shifted into the $CdTe_{1-x}Se_x$ layer, to the interface between photoactive and non-photoactive $CdTe_{1-x}Se_x$ [16]. The V_{OC} and J_{SC} decrease for thicker layers, confirming that the presence of the non-photoactive wurzite $CdTe_{1-x}Se_x$ is not beneficial for the device performance. Deposition methods and parameters therefore have to be chosen to minimize the formation of non-photoactive $CdTe_{1-x}Se_x$.

3.4. CdSe/CdTe Devices with a CdS Window Layer

With a combined CdS/CdSe window layer (Figure 2b), device performance can be increased by combining the upsides of both layers while minimizing the drawbacks (see Table 3). By reducing the CdS thickness from 130 nm in a CdS/CdTe device to 15 nm in a CdS/CdSe/CdTe device, the parasitic absorption in the short-wavelength region is minimized (region 1 in Figure 4a) and the J_{SC} is increased. Further J_{SC} increase is due to a shift in band gap with CdTe_{1-x}Se_x (region 2 in Figure 4a). The J_{SC} is therefore very similar to a CdSe/CdTe device, while the V_{OC} is improved with the CdS layer in between the CdTe_{1-x}Se_x and the TCO, which reduces the interface recombination (see Figure 4b) [20,54].

A CdS/CdSe/CdTe structure also works in substrate configuration solar cells (Figure 2e). Substrate configuration CdTe solar cells require a thick CdS layer in order to mitigate the formation of pinholes. With a CdTe_{1-x}Se_x layer between CdTe and CdS, the CdS layer thickness can be reduced from 120 to 30 nm with only small losses in V_{OC} and with a 7.1 mA/cm² increase in J_{SC} due to the reduction in CdS thickness and the reduction in band gap, resulting in an overall improvement in efficiency (see Table 3) [8].

3.5. CdTe_{1-x}Se_x/CdTe Devices with a MgZnO Window Layer

Recent high-efficiency CdTe devices have been achieved by replacing the CdS window layer with MgZnO (see Table 3) [15,22]. MgZnO has a band gap of 3.7 eV, higher than CdS, thereby reducing parasitic absorption, and it has a better band alignment with CdTe than TCO/CdS, reducing interface recombination and allowing for a higher V_{OC} [21,22]. However, introduction of a MgZnO window layer into a device structure can be problematic. The MgZnO/CdTe interface is sensitive to barriers originating from oxides, e.g., MgO, that can be formed during deposition. To obtain high-efficiency MgZnO/CdTe devices, deposition parameters, such as temperature and oxygen partial pressure during deposition, and CdCl₂ treatment, have to be carefully optimized [56].

Further improvement was achieved by using a $CdTe_{1-x}Se_x$ layer at the front of the CdTe absorber. With an 800 nm thick $CdTe_{1-x}Se_x$ layer in front of a CdTe absorber, Munshi et al. showed an improvement in device efficiency from 17.9% for a MgZnO/CdTe device to 19.1% in a MgZnO/CdTe_{1-x}Se_x/CdTe device (see Table 3) [15]. They improved the J_{SC} by 2.1 mA/cm² while retaining the high V_{OC} (see Figure 5a). As the device contains no CdS, the EQE in the short-wavelength region is improved (region 1 in Figure 5a).

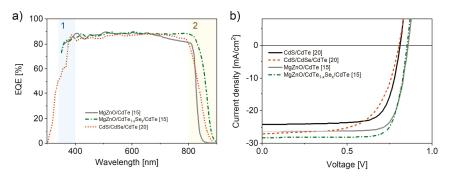


Figure 5. EQE (a) and *J-V* (b) curves of MgZnO/CdTe and MgZnO/CdTe_{1-x}Se_x/CdTe devices (adapted from [15]) compared with a CdS/CdSe/CdTe device (adapted from [20]).

The benefit of depositing $CdTe_{1-x}Se_x$ instead of CdSe in front of CdTe is the low possibility that non-photoactive wurzite $CdTe_{1-x}Se_x$ is formed. As a consequence, higher amounts of Se can be introduced to the device for better fine-tuning of the band gap gradient [29]. This results in a thicker photoactive low-band gap $CdTe_{1-x}Se_x$ layer in the finished device. The low-band gap region appears sufficiently thick to absorb most photons with energies below the band gap of CdTe, down to about 1.42 eV, as evidenced by the shift in absorption edge in the EQE curve in region 2 in Figure 5a. The difference in absorption between the thick photoactive layer achieved with $CdTe_{1-x}Se_x$ deposition and the thin photoactive layer achieved with CdSe deposition can be seen in the steepness of the EQE curve in region 2 in Figure 5a. The conclusion can be drawn that for maximized J_{SC} gain from $CdTe_{1-x}Se_x$, deposition of a $CdTe_{1-x}Se_x$ layer instead of a CdSe layer is necessary.

The high V_{OC} in the MgZnO/CdTe_{1-x}Se_x/CdTe device was in part attributed to a high lifetime of 22 ns measured by TRPL, four times higher than in the MgZnO/CdTe device, due to improved interface quality between MgZnO and CdTe_{1-x}Se_x, and also due to the passivation of a recombination center by Se [13,15,19]. The MgZnO/CdTe_{1-x}Se_x/CdTe device has a much higher V_{OC} than the CdS/CdTe_{1-x}Se_x/CdTe devices. This indicates that the V_{OC} in these structures is limited by the TCO/CdS/CdTe_{1-x}Se_x interfaces, but further investigations into the V_{OC} and FF loss of CdTe_{1-x}Se_x/CdTe devices is needed to confirm this.

Figure 6 compares the EQE curve of the high-efficiency MgZnO/CdTe_{1-x}Se_x/CdTe device with the record device from First Solar. The First Solar device uses a CdTe_{1-x}Se_x layer and some kind of buffer layer instead of CdS [11]. It has a higher V_{OC} and higher J_{SC} than the MgZnO/CdTe_{1-x}Se_x/CdTe device (see Table 3) [3,11]. The increase in J_{SC} is primarily due to a very good absorption at high wavelengths (region 2 in Figure 6). The very straight absorption edge indicates the presence of a sufficiently thick CdTe_{1-x}Se_x layer with a band gap of 1.4 eV for complete absorption of photons in this region. Some further improvement of J_{SC} is achieved by an overall higher EQE, probably due to an antireflection coating. In the short-wavelength region (region 1 in Figure 6), the curves are very similar. This is an indication that First Solar must have used MgZnO or a similar material as a buffer layer, eliminating the influence of parasitic absorption. The increase in V_{OC} might be due to better interface engineering and therefore reduced recombination, but without more information on the First Solar device structure no conclusions can be drawn.

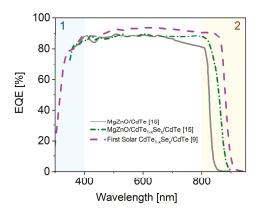


Figure 6. EQE curves of Munshi et al. (adapted from [15]) and the First Solar record device (adapted from [9]).

4. Conclusions

 $CdTe_{1-x}Se_x$ has been successfully introduced into CdTe devices by several different groups. It has been shown that a band gap gradient can be achieved by several different techniques and deposition methods. For better control and a higher limit to the amount of Se put into the devices, use of a $CdTe_{1-x}Se_x$ layer is preferable to a CdSe layer in order to avoid formation of non-photoactive wurzite CdTeSe. In devices with a $CdTe_{1-x}Se_x$ layer at the front of the CdTe absorber, the reduced band gap and possibility of reduced CdS window layer thickness result in increased short-circuit current. The open circuit voltage can be maintained at the level of CdTe devices due to Se passivating a recombination center in the absorber. The best reported devices use a MgZnO window layer instead of CdS, which provides a better band alignment with the absorber and eliminates parasitic absorption from the window layer.

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Encapsulation of Organic and Perovskite Solar Cells: A Review

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Abstract: Photovoltaic is one of the promising renewable sources of power to meet the future challenge of energy need. Organic and perovskite thin film solar cells are an emerging cost-effective photovoltaic technology because of low-cost manufacturing processing and their light weight. The main barrier of commercial use of organic and perovskite solar cells is the poor stability of devices. Encapsulation of these photovoltaic devices is one of the best ways to address this stability issue and enhance the device lifetime by employing materials and structures that possess high barrier performance for oxygen and moisture. The aim of this review paper is to find different encapsulation materials and techniques for perovskite and organic solar cells according to the present understanding of reliability issues. It discusses the available encapsulate materials and their utility in limiting chemical, such as water vapour and oxygen penetration. It also covers the mechanisms of mechanical degradation within the individual layers and solar cell as a whole, and possible obstacles to their application in both organic and perovskite solar cells. The contemporary understanding of these degradation mechanisms, their interplay, and their initiating factors (both internal and external) are also discussed.

Keywords: organic solar cells; perovskite solar cells; encapsulation; stability

1. Introduction

Organic photovoltaic (OPV) and Perovskite solar cell (PSC) are promising emerging photovoltaics thin film technology. Light harvester metal-halide perovskite materials, such as methyl-ammonium lead iodide (CH₃NH₃PbI₃), have exhibited small exciton binding energy, high optical cross-section, superior ambipolar charge transport, tuneable band gaps, and low-cost fabrication [1]. The CH₃NH₃PbI₃ PSCs and OPV devices can be solution-processed, which is suitable for roll-to-roll manufacturing processes for inexpensive largescale commercialization. The power conversion efficiency (PCE) of OPV devices have overpassed 14% for single junction and 17% for tandem devices to date with the development of low band-gap organic materials and device processing technology [2–5]. The achievement of the highest PCE of PSCs over 23.3% has shown promising future directions for using in large-scale production, together with traditional silicon solar cells [6]. Low-temperature (<150 °C) and solution-processed ZnO based electron transport layer (ETL) is one of the most promising materials for large scale roll-to-roll fabrication of perovskite and organic solar cells, owing to its almost identical electron affinity (4.2 eV) of TiO2. Arafat et al. have already demonstrated aluminium (Al) doped ZnO (AZO) ETL of PSC with cell efficiency over 18% [7]. Currently, the poor stability of OPV and perovskite solar cells is a barrier for the commercialisation [8]. It is believed that oxygen and moisture are the external main reason for degradation of organic and PSCs, as shown in Figure 1 [9]. All the internal possible degradation mechanisms in PSCs can be controlled by careful interface engineering, such as a good choice of cathode and anode interlayer materials, ion-hybridizations in perovskite layer, etc.

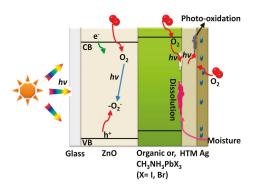


Figure 1. Schematic diagram of an organic/Perovskite solar cell (PSC) solar cell structure. The electron-hole pair recombination, moisture dissolution of perovskite material and photo-oxidation processes at the interface between hole transport materials (HTM) and metal electrode are shown. Adapted with permission from [9]. Copyright 2018 Royal Society of Chemistry.

Encapsulation of organic and perovskite solar cells can play an effective role in improving the stability of both devices. The encapsulation layer can act as a barrier layer by restricting the diffusion of oxygen and moisture through this encapsulation material, resulting in the protection of the cathode interface and the active layer from deterioration as shown in Figure 2. Encapsulation materials should have high barrier performance for oxygen and moisture. The encapsulation material layer structure is a critical factor to overcome these issues and enhance the device stability [10].

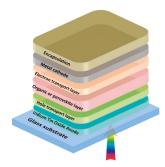


Figure 2. A schematic diagram of an organic or perovskite solar cells structure with an encapsulation layer.

The encapsulation material needs to possess good process ability, low water absorptivity, and permeability. Encapsulation materials should have relatively higher dielectric constant, light transmission, and resistance to ultraviolet (UV) degradation and thermal oxidation. They also require excellent chemical inertness, adhesion, and mechanical strength [11,12]. Oxygen transmission rate (OTR) and water vapour transmission rate (WVTR) are the steady state rates at which oxygen and water vapour gas can penetrate through a film that affects the encapsulation layer. A schematic diagram of organic and/or perovskite solar cells device is shown in Figure 2 with an encapsulation layer. This encapsulation layer material should have the following (Table 1) required properties to protect the device from the oxygen and water vapour effects. A list of specifications of requirements of encapsulation materials is listed in Table 1.

Characteristics	Specification of Requirement
WVTR	10^{-3} - 10^{-6} g·m ⁻² ·day ⁻¹
OTR	10^{-3} - 10^{-5} cm ³ ·m ⁻² ·day ⁻¹ ·atm ⁻¹
Glass transition temperature (T_g)	<-40 °C (during the winter in deserts)
Total light transmission	>90% of incident light
Water absorption	<0.5 wt % (20 °C/100% RH)
Tensile modulus	<20.7 mPa (>3000 psi) at 25 °C

UV absorption degradation

Hydrolysis

Table 1. Specifications and requirements for encapsulating materials for the protection of organic and perovskite devices from the oxygen and moisture. Reprinted with permission from [12]. Copyright 2016 John Wiley & Sons, Inc.

To determine the value of OTR, it is necessary to use a colorimetric sensor [13,14]. The OTR was calculated by measuring the amount of oxygen during a certain period at a constant rate that it passed through the cathode. By knowing the value of OTR and WVTR it is possible to determine how good is the encapsulated materials performance for the protection of perovskite and OPVs devices from degradation through their lifetime and performance. The effective WVTR can be determined by monitoring the temporal rate of change of the cathode (metal) electrical conductance. If it is assumed that the diffusivity of water vapour and oxygen obeys Fick's law (diffusivity is independent of concentration), then the WVTR or OTR can be described as [15]:

WVTR(t) =
$$\frac{DC_{\rm s}}{l} \left[1 + 2 \sum_{n=1}^{n} (-1)^n e^{\frac{[-Dn^2 \pi l]}{l^2}} \right]$$
 (1)

None (>350 nm)

None (80 °C, 100% RH)

where *D* is the diffusivity, C_s is the surface saturation concentrations, *t* is the time, and *l* is the film thickness. Normally, *D* increases with increasing temperature. WVTR and OTR is also a function of temperature.

The good performance encapsulation materials should have a value larger than 10^{-6} g·m⁻²·day⁻¹ for WVTR (Table 1) to protect the OPV and PSCs devices [16]. As an example, an OPV device with a structure ITO/ZnO/P3HT:PCBM/PEDOT:PSS/Al was encapsulated using ZnO and UV resin with a large WVTR value of 5.0×10^{-1} g·m⁻²·day⁻¹ [17]. In Ref. [18], the WVTR value was found as big as of 100 g·m⁻²·day⁻¹ for an encapsulated OPV (ITO/PEDOT:PSS/P3HT:PC₇₁BM/Ca/Al) with an epoxy resin. On the other hand, in Ref. [17] OPVs cells under the configuration ITO/DMD/Cs₂CO₃/P3HT:PCBM/MoO₃/Al were encapsulated using polyvinyl butyral (PVB), ethylene vinyl acetate (EVA), and thermoplastic poly-urethane (TPU) with a WVTR value of 60, 40, and 150 g·m⁻²·day⁻¹, respectively, and with an OTR value in the range of $10^{-2}-10^2$ cm³·m⁻²·day⁻¹. In this current work, the WVTR and OTR values were not calculated due to different experimental details.

The most common type of an encapsulation method refers to thin film layers encapsulated on top of OPV and perovskite devices using atomic layer deposition (ALD) [19,20]. ALD is particularly suitable for organic and flexible electronics. However, the ALD technique is expensive. Other methods are roll lamination systems encapsulating the OPV devices between two sheets uniting them with an adhesive [21], the other method is based on heat sealing, a process that basically consists of supplying thermal energy on outside of package to soften/melt the sealants [14] and using a glass substrate that is to be sealed with thermosetting epoxy, it could not be effectively applied to flexible devices [22].

Many works have been done for the advancement of good quality encapsulation technologies to stop the migration of environmental oxygen and moisture into device layers. The device lifetime and stability can be improved with high barrier performance encapsulation materials and structures for providing sufficient durability for commercial application. The encapsulation materials with high optical transmission and high dielectric constant need to possess good processing ability. Mechanical strength, good adhesion, and chemical inertness are also required for a suitable encapsulation material. It is also expected to have low water-absorptivity and permeability and relatively high resistance to UV degradation and thermal oxidation [23]. Organic materials with a good combination of these properties are most commonly used as the encapsulate for the improvement of acceptable device durability [24]. When compared to their inorganic counterparts, the organic encapsulation materials have demonstrated notable advantages, such as the flexible synthesis of the organic molecules by varying their energy levels, molecular weight, and solubility [25]. Organic encapsulation materials are also expendable and they have lesser impact on the environment [26]. Hence, organic materials are the best suitable candidate for the encapsulation of flexible organic and perovskite devices.

2. Degradation Mechanism of OPV and Perovskite Solar Cells

The degradation of organic and perovskite devices can be divided into two mechanisms: intrinsic and extrinsic. Both of these mechanisms are related to mass-transport processes. The metal electrode/active layer interfaces play major roles in the degradation of both devices [27]. Under normal environmental conditions, the relatively high sensitivity of organic and perovskite materials towards oxygen and moisture decrease the device reliability and lifetime.

2.1. Degradation of OPV Devices

Intrinsic degradation: It is due to changes in the structures of the interfaces between layers of the stacking materials, owing to internal modification of the materials used. The key issue is stability, which is limiting the practical applications of OPV devices. The lifetime of OPV devices is now over many thousands of hours. These improvements of lifetime have been achieved with the application of device architecture optimizations and different interface materials, especially after the investigation of hole conductor layers incorporating carbon electrodes. This is promised stable, low cost, and easy device fabrication methods.

Extrinsic Stability: It is affected by the infiltration of air, e.g., oxygen and water. Such degradation from external factors can escalate by light irradiation. There are some organic materials and metal electrodes can also be degraded by oxygen and water. Oxygen or moisture can be trapped during the fabrication processes or they could diffuse into the cell structure during device lifetime. Due to the following factors, oxygen strongly influences the extrinsic stability in some OPV devices [28]: (i) fullerene molecules are hydrophobic and does not react with water; (ii) the exposure to oxygen in air has negative impact on the electron-transport properties of fullerene; and (iii) oxygen forms surface dipoles and increases the metal work-functions. The abovementioned properties yield in the deterioration of the performance of conventional OPVs; however, they might initially enhance the performance of inverted OPV [11]. The chemical degradation processes are the degradation of the metallic electrodes, degradation of the transparent electrode, intermediate hole extraction layers, and/or even the chosen method to synthesize the materials [29,30]. Although it is well-known that oxygen is typically a p-type dopant in semiconductors, the oxygen vacancies act as electron donors [31]. The electronic properties of semiconducting p-type layers might be improved briefly upon exposure to oxygen [32]. To overcome this issue, researchers have developed inverted OPV devices [33,34]. In a humid environment, the oxide layer can double in thickness, and hence block charge-tunnelling. Unlike the abovementioned positive/negative effects of oxygen, there is hardly any positive impact of water on OPV devices that has ever been suggested. Encapsulation delays the process of degradation, but the currently available materials used for encapsulation. The overall device degradation is not stopped, even by a complex encapsulation schemes, such as a sealed glass container or a high vacuum chamber are employed, because the processes involving water and oxygen are efficiently alleviated. The physical and chemical characteristics of the constituent materials are a complex phenomenon. Several processes may take place simultaneously in both physical and chemical characteristics [35].

2.2. Degradation of Perovskite Devices

There are several issues that are related to the degradation of PSCs, such as interface and device instability. These must be addressed to achieve good reproducibility with high conversion efficiencies and long lifetimes of PSCs. A comprehensive understanding of these issues in PSCs is required to achieve stability breakthroughs for practical commercial applications. For the PCE improvement, the stability of PSCs has to be improved for successful small- and large-scale applications.

The degradation of PSCs can occur as a result of intrinsic and extrinsic stability, such as thermal instability (intrinsic stability) and susceptibility of the perovskite material to ambient conditions (e.g., oxygen and humidity). Degradation can occur by other device structure components, such as the degradation of the ETL (TiO₂ or ZnO) at the interface upon light irradiation and the lack of stability of the hole-transport material [36,37]. The stability of perovskite thin films and PSCs has been widely studied [38–40], which includes the degradation of the perovskite material upon exposure to illumination, humidity, or increased temperature [41–44]. Different schemes have been investigated to enhance the stability of PSCs, such as replacing the mesoporous layer [45], modifying the composition or deposition process of perovskite material [46–49], using various charge-transport materials [50–55] and carbon-based electrodes [46], and interfacial layers and/or surface treatments [56–59]. In most of the researches on stability, the stability tests were reported after the devices being stored in the ambient or dark with measurements of the device performance at regular intervals [52,54,55,60]. The report on encouraging stability of the perovskite devices, such as 0.3% PCE drop in one month, often involves storing them under dark in a low-humidity desiccator [39].

However, it is now well established that PSCs are very susceptible to high humidity. The degradation is notably quicker under high humidity conditions [61,62], and it is much faster under continuous illumination than degradation involving storage in the dark [56,62]. Even the degradation under ambient illumination is significantly faster when compared to dark storage [63]. Since there is no standard testing protocol for reporting stability test results, it is strenuous to draw comparisons directly between test results from different publications. For example, Zhu et al. performed stability tests under constant illumination over a short time period in an N₂ glovebox to prevent the intrusion of humidity [62]. Thermal stability has been reported without exposure to illumination or humidity, or a combination of thermal stress and illumination [64]. In some studies, a white light-emitting diode (LED) was used for the illumination, not a solar simulator [50]. The stability can be over-estimated under illumination, owing to the absence of strong UV component in the emission spectrum. The degradation of the perovskite film is reportedly slower under illumination when a UV filter is used in order to eliminate the UV component from the simulated sunlight illumination [43]. Some works have applied several stress factors at the same time during the tests. The factors include constant illumination, ambient humidity of +50%, and increased temperature [65]. Moreover, the moderately humid environment has been used to obtain outdoor testing results [66].

Multiple stability tests have been performed on cells under low ambient humidity without encapsulation, typically under dark conditions [38,46–49], with very few exceptions [50,57,67]. After several hours, devices without encapsulation generally displayed severe degradation under continuous illumination whilst encapsulated devices showed a relatively longer lifetime [39]. In comparison to fully encapsulated devices with a protected edge, partially encapsulated devices showed a shorter lifespan [46]. This signifies the importance of complete encapsulation in order to enhance extend the lifetime of OPV and perovskite devices. However, the comprehensive comparison between different encapsulation techniques for PSCs is still rare [65]. A careful and complicated encapsulation system, developed by employing the combination of a desiccant material and UV epoxy resin, exhibited significantly improved stability. However, the device performance quickly decreased to <50% of the initial efficiency within 10 h under constant illumination and at an ambient humidity of 80% and cell temperature of 85 °C [65]. The absence of standardized testing conditions and studies regarding the effect of encapsulation on the device stability is hampering the advancements of stable organic and perovskite cells. Various encapsulation methods have been investigated for common perovskite

devices that include planar TiO_2 on fluorine doped tin oxide (FTO) glass, methylammonium lead iodide (MAPbI₃) as the active layer, and tetrakis[*N*,*N*-di(4-methoxyphenyl) amino]-9,9'-spirobifluorene (spiro-OMeTAD) as the hole transport layer (HTL) [43]. The international summit on OPV stability (ISOS) was followed for the organic solar cell testing (ISOS-L-2 and ISOS-O-1) [68].

2.2.1. Thermal and Photo Stability

It is found that the photo-stability of perovskite materials is a serious problem for the application of PSCs. The perovskite material begins to decompose into PbI₃ at temperature 140 °C [69], and even at temperature 85 °C when it is heated in nitrogen for 24 h [41]. The slight heating of perovskite materials improved the performance of devices due to the formation of a small amount of PbI₃ which passivate the perovskite. The device performance may be recovered if it is stored in the dark for a short time. Poor photo-stability of perovskite materials could be raised from the local phase change under an elevated temperature when exposed to light. The dual ion hybridization by compositional material engineering at two sites (A and X) simultaneously can solve the perovskite materials stability. The existing ionic components within the perovskite crystal structure would be partially substituted by analogous ions of similar electronic properties, which would passivate the vulnerable sites present within the structure and thereby eliminating the degradation pathways efficiently from the inside-out. For example—the existing monovalent (A-site) organic cation would be partially substituted by metal (Caesium, Cs^+) ions. It has been experimentally proved that heat rather than moisture was the main cause of PSC degradation [70]. The key stability of PSC is to prevent the escape of volatile decomposition products from the perovskite solar cell materials. Polyisobutylene (PIB) encapsulation is one of the promising low cost and low application temperature packaging solutions for PSCs.

2.2.2. Ion Movement

Ion migration in the perovskite materials is another critical issue for the PSCs [71]. The ions (anion or cation) in the halide perovskite materials can move under bias voltage or thermal drift, causing device instability. A schematic diagram of different ion/defects movements in perovskite device structure is shown in Figure 3.

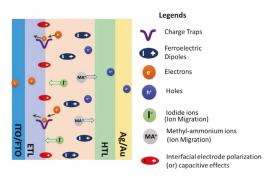


Figure 3. Schematic diagram shows the various ion/defects movements in perovskite device structure that could possibly lead to hysteresis phenomenon during current-voltage characteristic measurements. The exact nature of each ion-movement processes and its degree of influence on hysteresis varies with respect to the device structure and materials involved. Reprinted with permission from [71]. 2018 Solar Energy Materials and Solar Cells.

This defects/ion migration, such as iodine vacancies across the interface, can induce interfacial degradation. This defect migration affects device operational mechanisms and finally cause device failure during operation [9,72].

2.2.3. Electrode Degradation

The interfacial stability of PSCs is also critical for the overall device stability. Recently, it has been found that reactions between iodine-based decomposition products, such as HI from perovskite materials, and traditional metal electrode materials, such as Al or Ag, can lead to the formation of AlI₃ or AgI, respectively [55]. The formation of AlI₃ or AgI compound escalates perovskite decomposition when the material is exposed in an ambient environment (Figure 3) [55]. One way of enhancing the device stability is to insulate the perovskite material from the electrode (Ag/Al). The dispersal of halide ions in PSCs through the charge transport layers could exert a negative impact on the long-term stability of cells.

2.2.4. Charge Transport Layers Degradation

The reasons behind poor device stability of PSCs are due to either the perovskite materials or charge transport layer interfaces. Organic semiconductor layers in the PSC structure that are used as charge transport layers (ETL and HTL) are prone to both oxidization and water absorption that can reduce the device stability. For example, an n-type fullerene, PCBM was used as an efficient ETL in an inverted structure PSC [73]. The authors found that the PCBM went through changes in terms of chemical states or band structure in ambient air, which was a major contributing factor to the device degradation [73]. A p-type organic semiconductor, PEDOT:PSS, is generally used in the inverted structure as the HTL. PEDOT:PSS has high water absorptivity and acidic properties causing etching of the transparent conductive electrode, such as ITO. The hygroscopic and acidic nature of PEDOT:PSS accelerates device degradation [55,74]. Lithium (Li) doped Spiro-OMeTAD salt is also hygroscopic and can diffuse water into the light absorbing perovskite layer causing device failure [75]. Several investigations suggested that oxygen de-absorption from TiO_2 surface (degradation of TiO_2 layer), while light soaking leads to failure of devices [45]. Multiple techniques have been employed for the improvement of the device stability [7,74]. Idigoras et al. [76] deposited thin polymer layer by the remote plasma vacuum deposition of adamantine powder for the encapsulation of perovskite solar cells. They observed that the deterioration of device performance was significantly delayed because of the encapsulation layer.

Bella et al. [77] investigated the stability of PSCs by encapsulation of photochemical resistance as well as moisture tolerance, a fluoro-polymeric light-curable coating on the back contact side. The use of the fluoro-polymeric layer on top of the PSC has the prospect of preventing the oxygen and moisture migration between the top back contact and the perovskite layer due to the hydrophobicity of the coating. The fluoro-polymeric UV-coating possesses a cross-linked nature that can lower the free volume when compared to the traditional non–cross-linked, polymeric systems. Hence, it is expected to improve the long-term stability of PSCs [78]. Figure 4 displays the test results of device stability in terms of PCEs under various atmospheric conditions and photochemical external stresses during 180-days (4320 h). Moreover, those encapsulated devices were tested in outdoor conditions for a time of >3 months (i.e., 2160 h). Successful tolerance toward heavy rain, soil, and dust were observed on the external surface made of glass. In real outdoor conditions, the fluorinated luminescent down shifting layer with low-surface energy helps to clean the front electrode easily.

Uncoated and front-coated devices were studied for an overall period of six months in the aging test. The devices were stored in a glove box filled with Ar for the first three months. The devices were continuously illuminated for 8 h every day with a UV optical fibre with light intensity 5 mW·cm⁻². 5% contribution from the UV light source (280–400 nm) helped to simulate the solar spectral irradiance on Earth (AM1.5G, 1000 W·m⁻²). In the forced UV aging test (Figure 4), the uncoated devices (black curve) had a reduction of 30% in their initial efficiency after one week of UV exposure and stopped working after one month. All of the five front-coated cells (red curve) retained 98% of their initial PCE, even after three months and demonstrated excellent stability under the same conditions.

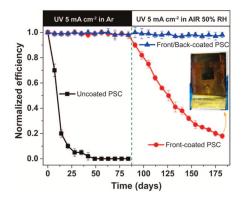


Figure 4. The aging test results on the three series of PSCs: (i) uncoated, (ii) front-coated with a luminescent fluorinated coating, and (iii) front/back-coated (front coating with the luminescent fluorophore and back contact coating with a moisture resistant fluoro-polymeric layer). The cells were stored in an Ar environment during the first three months of the test period. They were kept in the air with RH = 50% for the next three months. During the whole testing period, the PSCs were exposed to continuous UV illumination. The device power conversion efficiency (PCE) was recorded once a week. The inset shows a photograph of a front-coated solar cell at the end of the test. Reprinted with permission from [77]. Copyright 2018 American Association for the Advancement of Science.

By simple visual inspection, the effects of degradation were easily detectable. The progressive yellowing was observed in the mixed-perovskite layer upon 50% RH exposure. The back-contact side was coated with a fluoropolymeric light-curable coating in the front/back-coated devices for stabilizing the devices with enhanced photochemical resistance and moisture tolerance. A similar method was used in the luminescent downshifting experiment for back-coated PSCs. It is hypothesized that the use of highly hydrophobic fluoropolymeric layer on the PSC top can prevent water permeation from the top back contact to the perovskite layer. In addition, the fluoro-polymeric UV-coating possesses a cross-linked nature, leading to lower free volume when compared to the traditional non-cross-linked, polymeric systems. Hence, the coating is expected to improve the long-term stability of PSCs [79]. The aging test results of the front/back-coated PSCs (blue curve), i.e., devices with a luminescent coating on front and a moisture-resistant coating on the back contact, is shown in Figure 4. Even under the combined effects of photochemical and environmental stresses, all the five devices retained exceptional stability of 98%.

The front/back-coated PSCs showed longer lifetime stability retaining most of their initial efficiency the ageing test due to the following reasons:

- securing the perovskite material from UV irradiation and converting it into visible photons;
- shielding devices from oxygen and moisture, hence blocking the hydrolytic behaviour of the perovskite material;
- maintaining clean front electrode clean by the self-cleaning characteristics of this fluorinated polymer. Similar results were also observed for outdoor tests performed.

The non-homogeneous deposition of the coating layers on the front/back side of the device can cause slow hydrolysis of the active perovskite layer. To test the homogeneity of the deposited coating layer, Bella et al. [77] dipped the devices with front/back coatings into the water for about a day. No change in photovoltaic performance was observed in the front/back-coated devices, even after one day of immersion in water.

3. Encapsulation Requirements

To ensure satisfactory encapsulation (Table 1), the permeation of WVTR and OTR needs to be two-three orders of magnitude lower than the bare substrate. Silicon-based dielectric films, deposited by PECVD, have reportedly demonstrated excellent transparent, single-layer barrier performance [80]. However, on polymer substrates it is very difficult to obtain permeation levels that are 1000 times lower by a single layer barrier. The increase in single-layer barrier thickness results in an OTR value that is on-zero asymptotic and is governed by the defects in the barrier layer. Such defects are typically generated from the intrinsic or extrinsic roughness of surface [81]. Hence, the performance of single-layer, encapsulated gas barriers is controlled by the nano-meter size structural defects. In theoretical calculations, the total permeation rate is much higher due to a large number of small pin-holes than that from few but larger defects in the same total pin-hole area [82]. The lateral diffusion of gas is more crucial when the defect diameters are smaller than the substrate thickness. The multilayered deposition of inorganic materials can slightly enhance the performance of the encapsulation barrier. The deposition of organic-inorganic multilayers films to obtain increased barrier performance is the most common practice [83]. However, there are several challenges in the way of utilization and development of thin-film encapsulation. To face these challenges, a variety of materials have been developed to improve the device lifetimes, such as titanium oxide (TiO_x). Using thin films as barriers for device encapsulation is not sufficient for the protection of organic and perovskite devices. The use of glass plates as encapsulation is the simplest and best example for the protection of oxygen and moister. Glass encapsulation can supply the required oxygen and moisture protection in the organic and perovskite solar cells for commercial application. However, glass encapsulation cannot apply on inflexible devices. It has also been shown that a thin layer of SiO_xC_y acts as a barrier for oxygen and moisture. Unfortunately, the PECVD process is required for the deposition of this encapsulation film, which is expensive and uses complicated vacuum systems. This is also not suitable to deposit on a flexible substrate as a barrier of oxygen and moister transmission. Although there are other encapsulating materials, they cannot fulfil the barrier requirements for organic and perovskite solar cells. In this review paper, we have presented different encapsulation materials used in various approaches and integrated with organic and perovskite devices. In Table 2, we have summarized some of the polymer materials with their WVTR values for the organic and perovskite solar cells. Recently, using the RF plasma polymerization technique linalyl acetate [84,85] and terpinene-4-ol thin films has been deposited for the encapsulation of devices. On the basis of surface and optical properties, these polymer based thin films can be potential encapsulating layers for organic and perovskite solar cells [86,87].

Materials for Encapsulation

The encapsulation materials should have high a dielectric breakdown that matches the refractive index with other layers and high volume resistivity. Materials should be low cost, dimensionally stability, and easy to deposit. WVTR and OTR represent the steady state rates at which water vapour and oxygen gas, respectively, penetrate through the encapsulating film that affects the encapsulation layer. Glass transition temperature (T_g) for organic encapsulation material is another important property, which is dependent on the chain flexibility. The polymer mechanically varies from being rigid and brittle and becomes tough and leathery. The maximum exposure temperatures on encapsulation material and the effect on the mechanical behaviour of the material should be known. The light transmission through the encapsulation materials is also important to measure to understand how it will affect the device performance. The encapsulation material requirements are also to define the UV absorption degradation, hydrolysis, and some other aspects. A list of suitable polymer encapsulation materials and their specifications for the roll-to-roll fabrication of devices are given below.

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Materials	Encapsulation Type	Water Vapour Transmission Rate (WVTR) (g·m ⁻² ·day ⁻¹)	Comments	References
Ethylene vinyl acetate (EVA)	Single layer encapsulation	40	Light transmission of 91%. Suitable for resisting weather and long-term reliability under light exposure. It is suitable for encapsulation of organic and perovskite solar modules.	[88,89]
Europium doped EVA: Eu ³⁺	Single layer encapsulation	40	Absorption bang gap is 310 nm (4 eV). Suitable for PV module encapsulation. Eu $^{3+}$ doped EVA layers can induce photon down-shifting with wavelengths <460 nm.	[06]
Ethylene methyl acrylate (EMA)	Single layer encapsulation	Not mentioned	EMA is suitable for chemical resistance, thermally stability, adherence to different substrates and excellent mechanical behaviour at low temperature. It is suitable for encapsulation of perovskite and organic devices.	[23,91]
Polyvinyl butyral (PVB)	Single layer encapsulation	60	PVB has high optical transparency, good heat resistance, good adherence to solar cells, glass, and other plastics, increased bond durability, and compatible with module components. PVB is already used as encapsulation layer for thin film solar cells.	[14]
Thermoplastic polyurethane (TPU)	Single layer encapsulation	150	TPU film is better than EVA film for encapsulation since it is flexible to bond with relatively hard materials. These films can be processed in normal atmospheric pressure without cross-linking and emissions.	[92,93]
UV-cured epoxy	Single layer encapsulation	16	Epoxy film is good for encapsulation. It is optically transparent, thermally conductive, weather resistance, high temperature resistance, good adhesive properties on glass and plastic.	[20]
Polyisobutylene (PIB)	Single layer encapsulation	0.001-0.0001	PIB is a synthetic rubber. It can encapsulate organic and perovskite solar cells.	[70]
Cyclized perfluoro-polymer (CytopTM)	Single layer encapsulation	Not mentioned	Conventional thin-film deposition techniques e.g., spin coating can be used to deposit this polymer. It is transparent and amorphous. This material is good for weather resistant, good for oxygen/water-vapor shielding for testing organic device lifetime.	[94]
Organic-inorganic hybrid materials ORMOCERs (ORM)	Single layer encapsulation	0.01	It is organic and inorganic components modified ceramics or ORM. It has good chemical resistance, highly transparent, anti-soling, of fiftusion- inhibition. OTR is <0.01 cm ³ m ⁻² day ⁻¹ . These properties are necessary for the encapsulation of organic and perovskite solar cells.	[95,96]
ORMOSIL aero-gel thin film	Single layer encapsulation	Not mentioned	It is mechanically and thermally stable and highly transparent. ORMOSIL materials are flexibility and stability at atmospheric conditions. ORMOSIL has variable organic group that can modify the chemical and physical surface properties.	[97,98]
Other organic materials	Single layer encapsulation	Not mentioned	Encapsulation tested of 10 polymers were poly(vinyl methyl ketone) (PVMK), poly(methyl methacrylate) (PVMMA), poly(vinyliene chloride-co-vinyl chloride) (PVDC-co-PVC), poly (vinylidene fluoride)(PVDF), polycycylonitide (PAN), poly(vinylatenol) (PVA), poly(vinylphenol) (PVF), poly(methyl vinyl ether) (PAN), polystyrene (FS) and poly(vinyl chloride) (PVC). An encapsulation approach with these 10 low-polarity polymer is demonstrated to block water/moisture and prevent encapsulation-induced degradation.	[001'66]
Luminescent downshifting fluoro-polymeric coating such as PTFE (polytetrafluoroethylene), PFA (perfluoraelkoxy), FEP (fluorinated ethylene-propylene), etc.	Single layer encapsulation	Not mentioned	It is very good as an encapsulating material for organic and perovskite solar cells to improve the device stability for the out-door application. Fluoropolymers are excellent for chemical and thermal resistance. Their surfaces are non-reactive with all chemicals and solvents.	[101]

4. Discussion

Thin-film encapsulation is a vital technology that is required for the application and commercialization of perovskite and organic solar cells. An effective encapsulation is crucial to prevent the permeation of moister and oxygen to achieve the desired reliability and device lifetime. More progress is needed to develop encapsulating materials for devices with specific requirements. The processing conditions of EVA exposure time and damp heat affect its adhesion strength. Transport of moister and oxygen through local pinholes become an issue for achieving ultrahigh barriers encapsulation that is hard to be avoided. New encapsulation materials need to be developed to fulfil the encapsulation requirements and achieve ultrahigh encapsulation barriers. Furthermore, the encapsulation processing temperature of thin film should be within the temperature range that is suitable for the organic polymer substrate materials. Usually, low-temperature PECVD processed inorganic encapsulation thin films are not suitable for the encapsulation barrier, since these films suffer from intrinsic defects. Water vapour and oxygen can easily diffuse through these defects. For high performance encapsulation barriers, these intrinsic defects should be reduced or passivated. Inorganic and organic alternating multilayer films can be one solution to reduce and avoid intrinsic pinholes. The defects in the inorganic layers can be passivated by an organic film and do not channel continuously through the multilayer structure. A steady state permeation rate of moister and oxygen can be maintained by the multilayer encapsulation barrier structures. A transient rate of encapsulation barrier can be maintained over a specific time-period that might exceed the desired lifetime of encapsulated devices. Typically, the permeation rate in the transient region is lower than the permeation rate in the steady state. It is suggested that the barrier performance characterization from the initial transient period will provide an underestimation of the total permeation rate for long-term applications. As a result, the barrier performance in multilayer structures should be characterized separately, such as the steady-state and transient permeation rates. This should be used for the calculation of lag time to avoid overestimation of expected device lifetimes or barrier performance during both storage and application. Moreover, the deposition of high quality inorganic encapsulation layer with vacuum deposition processes is expensive and low through put.

Since there are alternative deposition processes using different deposition chambers for organic and inorganic layers, multilayer barrier structures are expensive. If inorganic layers can be deposited from the solution precursors, it can be a promising solution to this problem, making it possible to deposit inorganic and organic multilayer barriers employing similar deposition techniques. Hence, totally solution process should be developed for low cost, high barrier materials for perovskite and OPV encapsulation. Optimization of the individual film dimension can be useful multilayer encapsulation structures. Before adapting these technologies, the quality of films should also be improved. The reliability and continuous yield of encapsulation processes must be explored to reduce the processing steps and time. Since perovskite and organic solar cells are very susceptible to moisture, it is crucial to use a low-diffusivity edge seal material.

Graphene is a carbon-based one-dimensional material with excellent electronic and mechanical properties offering limitless opportunities in device engineering. In line with this, graphene can be used as a bi-functional electrode that will serve as a highly conductive charge collection electrode as well as an encapsulant for the underlying organic or perovskite layers. This carbon-graphene based encapsulation technology is sought to be a viable approach for large scale commercialization and deployment of organic and perovskite solar cells technology.

5. Conclusions

Effective thin film encapsulation is crucial to prevent the permeation of water vapour and oxygen for achieving the stability and desired life times of organic and perovskite solar cells. The problem of achieving a thin layer encapsulation barrier is transport-dependent permeation through localized pin-holes that is strenuous to control. New materials and technology are required to satisfy the requirements of encapsulation to prevent the permeation of moisture and oxygen for the reliability and stability of devices. The encapsulation processing temperature of thin film should be within the temperature range suitable for the organic and polymer substrate materials. Multilayer polymer films of encapsulation can be a solution to block the pinholes in the films to stop the permeation of water vapour and oxygen. However, the barrier performance of multilayer structures encapsulation consists of a steady state permeation rate as well as a transient rate over a specified time. These rates of encapsulation barrier can exceed the desired lifetime of encapsulated devices. The barrier performance in multilayer structures should be characterized separately by the steady-state and transient permeation rates over a specified time-period. Multilayer thin film encapsulation structures deposited under vacuum will be exorbitant, owing to alternative deposition of layers in separate deposition chambers. Solution process deposition can be a promising alternative for low-cost barrier materials for thin film multilayers encapsulation. Subsequently, multilayers can be deposited with a similar deposition process to obtain low-cost barrier materials. Film quality should be improved before adopting the multilayer encapsulation technologies. Encapsulation layers with high quality are significant to improve the device lifetimes.

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Electroplating of Semiconductor Materials for Applications in Large Area Electronics: A Review

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Abstract: The attributes of electroplating as a low-cost, simple, scalable, and manufacturable semiconductor deposition technique for the fabrication of large-area and nanotechnology-based device applications are discussed. These strengths of electrodeposition are buttressed experimentally using techniques such as X-ray diffraction, ultraviolet-visible spectroscopy, scanning electron microscopy, atomic force microscopy, energy-dispersive X-ray spectroscopy, and photoelectrochemical cell studies. Based on the results of structural, morphological, compositional, optical, and electronic properties evaluated, it is evident that electroplating possesses the capabilities of producing high-quality semiconductors usable for producing excellent devices. In this paper we will describe the progress of electroplating techniques mainly for the deposition of semiconductor thin film materials and their treatment processes, and fabrication of solar cells.

Keywords: electroplating; semiconductors; large-area electronics; characterisation; solar cells

1. Introduction

Electroplating has been well explored over the years especially for the purification, extraction, protection, and coating of semiconductors, metals, and metalloids in the industrial sector [1] to achieve diverse characteristic properties. The use of the electroplating technique in the deposition of semiconductor materials dates back to the 1970s [2–4], with the deposition of semiconductors from the II-VI group. The ascendance of the electrodeposition of semiconductor material led to the growth and fabrication of CdS/CdTe-based solar cell devices within a decade afterwards [5]. The fabrication of thin-film solar cells with photovoltaic conversion efficiency of ~10% was the stimulus for an intense global research into electrodeposited semiconductor compounds. The research also spanned into the electrodeposition of II-VI semiconductor materials such as ZnTe [6], ZnSe [6], ZnS [7], ZnO [8], etc., and spread into semiconductor material compounds in the binary (III-V, IV-VI), ternary (CuInSe₂) [9,10], and quaternary (Cu₂ZnSnS₄, CuInGaSe₂) groups [11]. The electroplating of elemental semiconductors and other wide bandgap nitrides has also been captured in the literature. This communication critically appraises the strengths, weaknesses, potentials, and the state-of-the-art electroplating technique in the fabrication of large-area electronics and other macro-electronic devices such as photovoltaic (PV) solar panels and display devices.

2. An Overview of Electrodeposition Technique

Electrodeposition is the process of depositing elemental or compound metals or semiconductors on a conducting substrate by passing an electric current through an ionic electrolyte in which metal or semiconductor ions are present [12]. The passage of current is required due to the inability of the chemical reaction resulting in the deposition of the solid material on the conducting substrate to proceed on its own as a result of positive free energy change ΔG of the reaction. Electrodeposition can be categorised based on power supply source, working electrode, and electrode configuration (as shown in Figure 1), but the basic deposition mechanism and setup remains similar. The basic deposition mechanism entails the flow of electrons from the power supply to the cathode. The positively charged cations are attracted towards the cathode and negatively charged anions to the anode. The cations or anions are neutralised electrically by gaining electrons (through reduction process) or losing electrons (through oxidation process) and being deposited on the working electrode (WE), respectively [12].

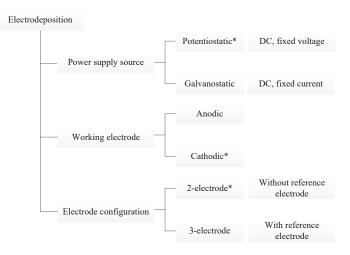


Figure 1. The main categories of electrodeposition technique.

The typical electrodeposition (ED) setup of a two-electrode (2E) configuration, as shown in Figure 2a, consists of a deposition container (beaker), deposition electrolyte, magnetic stirrer, hotplate, power supply, a working electrode, a counter electrode, and an optional reference electrode (RE) in the case of a three-electrode (3E) configuration (see Figure 2b). The use of a potentiostatic power source was due to the effect of deposition voltage on the atomic percentage composition of elements in the electrodeposited layer, which is one of the factors determining the conductivity type [13,14]. Cathodic deposition is mainly utilized due to its ability to produce stoichiometric thin-films with good adherence to the substrate as compared to anodic deposition [15]. Conversely, the galvanostatic electrodeposition is controlled and measured by maintaining constant current density through an electrolytic cell disregarding the changes in the resistance due to the deposited electroplated layer.

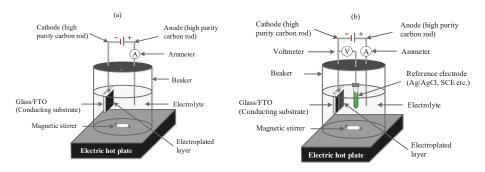


Figure 2. Typical (a) two-electrode and (b) three-electrode electrodeposition setups.

The 2E configuration, as shown in Figure 2a, was utilised due to its industrial applicability, process simplification, and also to eliminate possible Ag^+ - and K^+ -ion doping [16,17], which may emerge from the Ag/AgCl or saturated calomel electrode (SCE) reference electrodes (see Figure 2b). Taking the electrodeposition of n-CdS and n-CdTe layers which are respectively utilised as the main window and absorber layers in this work into perspective, both K^+ and Ag^+ from group I of the periodic table are considered as p-type dopants. Therefore, any leakage of K^+ and Ag^+ into the electrolytic bath may result in compensation leading to the growth of highly resistive material which has a detrimental effect on the efficiency of fabricated solar cells. This has been experimentally shown and reported in the literature [16].

The two-electrode electrodeposition configurations are not without challenges, with the main challenge being the fluctuation or drop in the potential measured across the cathode and the anode during deposition. This is due to the alteration in resistivity of the substrate with increasing semiconductor layer thickness and the change in the ionic concentration of the electrolyte. For the three-electrode configuration, the potential difference is measured across the working and the reference electrodes, while the measured current is between the working and the counter electrodes. In general, other factors such as the pH of the electrolyte [18], applied deposition potential [13,14], deposition temperature [19], stirring rate [20], deposition current density, duration of deposition and thickness [21], underlying substrate [22], and concentration of ions in the deposition electrolyte [18] affects the electrodeposition process and the properties of the deposited layers. Recent publications have demonstrated the similarities between electrodeposited semiconductors using three-electrode and two-electrode electroplating configurations [23,24]. The electrodeposition of both elements and compounds is governed by Faraday's laws of electrodeposition as mathematically depicted in Equation (1).

$$T = \left(\frac{1}{nF}\right) \left(\frac{itM}{\varrho A}\right) = \left(\frac{JtM}{nF\varrho}\right) \tag{1}$$

where *T* is the thickness (cm), *J* is current density (A cm⁻²), *t* is the deposition time (s), *M* is the molecular mass (g mol⁻¹), *n* is the number of electrons transferred in the chemical reaction for the formation of 1 mole of substance in g cm⁻³, *F* is Faraday's constant (96,485 C mol⁻¹), and ρ is the density (g cm⁻³). It should be noted that Faraday's law of electrolysis assumes that all electronic charges passing through the electrolyte contribute to the deposition of deposited material layer without any consideration of the resistance losses in the system and electronic charge contribution to the decomposition of solvent into its constituent ions [25].

3. Factors Influencing Electrodeposition

3.1. Solutes, Solvents, and Deposition Electrolytes

The effects of the incorporated solute and solvent utilised are of importance in electrodeposition. Taking the electrodeposition of CdS into consideration, sodium-(Na)-based precursor (Na₂S₂O₃) has been often utilised [26,27]. Although sodium (Na) ions are not electrodeposited at low cathodic voltages, the incorporation of Na in CdS films is achievable through adsorption, absorption or chemical reactions as a result of increased Na accumulation in the electrolytic bath. It should be noted that Na is a p-type dopant in CdS [28] resulting in increasing electrical resistivity of subsequent CdS layers due to Na accumulation. Further to this, the Na-based precursor (Na₂S₂O₃) is also associated with the precipitation of sulphur during the electroplating. Recent understanding has shown that the replacement of the well-established sulphur precursor with thiourea (NH₂CSNH₂) (which is more associated with chemical bath deposition (CBD) technique) results in the reduction/elimination of sulphur precipitate [29,30].

The choice of solvent to be utilised also possesses as an important factor in electroplating as demonstrated by the deposition of CdTe from ethylene glycol ($C_2H_6O_2$) electrolyte containing cadmium iodide (CdI₂) [31]. Using aqueous solution as solute, Cd-I complexes such as CdI⁺, CdI₂,

 CdI_3^- , and CdI_4^{2-} are formed in aqueous solution [32,33] debarring the deposition of Cd and the co-deposition of CdTe. It is noteworthy that CdTe from other Cd precursors have been explored and reported in the literature [34,35]. Therefore, the choice of solute and solvent for electroplating purposes is a factor to reckon with in addition to a number of other factors inherent in the electrodeposition process to achieve superior qualities of electroplated semiconductor materials. This understanding has been accrued for over two decades of exploration, and careful examination of grown semiconductors at Solar Energy Group within Sheffield Hallam University (SHU), in addition to the literature. A large number of semiconductors explored in SHU and documented in the literature [9,29,36–47] is summarised in Table 1.

Material Electroplated	E_{g} (eV)	Precursors Used for Electroplating	Precursors Used for Electroplating Comments	
CuInSe ₂	~1.00	CuSO ₄ for Cu ions, In ₂ (SO ₄) ₃ for In ions and H ₂ SeO ₃ for Se ions	Ability to grow both p- and n-type material	[9]
CdTe	1.45	$CdSO_4$ or $Cd(NO_3)_2$ or $CdCl_2$ for Cd ions and TeO_2 for Te ions	Ability to grow both p- and n-type CdTe using Cd-sulphate, nitrate, and chloride precursors	[40,41]
CuInGaSe ₂	1.00-1.70	$CuSO_4$ for Cu ions, $In_2(SO_4)_3$ for In ions, $Ga_2(SO_4)_3$ for Ga ions and H_2SeO_3 for Se ions	Ability to grow both p- and n-type material	[42]
CdSe	1.90	$CdCl_2$ for Cd ions and SeO_2 for Se ions	-	[43]
InSe	1.90	InCl ₃ for In ions and SeO ₂ for Se ions	-	[44]
GaSe	2.00	$Ga_2(SO_4)_2$ for Ga ions and SeO_2 for Se ions	-	-
ZnTe	1.90-2.60	ZnSO ₄ for Zn ions and TeO ₂ for Te ions	Ability to grow both p- and n-type material	[45]
CdS	2.42	CdCl ₂ for Cd ions and Na ₂ S ₂ O ₃ , NH ₄ S ₂ O ₃ or NH ₂ CSNH ₂ for S	Conductivity type is always n-type	[29,46,47]
CdMnTe	1.57-2.50	CdSO ₄ for Cd ions, MnSO ₄ for Mn ions and TeO ₂ for Te ions	-	-
ZnSe	2.70	$\rm ZnSO_4$ for Zn ions and $\rm SeO_2$ for Se ions	Ability to grow both p- and n-type material	[36]
ZnO	3.30	Zn(NO ₃) ₂ for Zn ions	-	[37]
ZnS	3.75	$ZnSO_4$ for Zn and $(NH_4)_2S_2O_3$ for S ions	Ability to grow both p- and n-type material	[38]
Polyaniline (PAni)	-	C ₆ H ₅ NH ₂ and H ₂ SO ₄	To use as a pinhole plugging layer	[39]

Table 1. Summary of explored electronic materials to date at authors' research group using electroplating from aqueous solutions.

3.2. Electrolytic Bath pH Value

The composition of an electrolytic bath naturally determines the pH of the bath. Basically, the acidity (pH < 7.00) of an electrolyte can be increased by the introduction of an acid. The hydrogen ions (H⁺) from the dissociated acid reacts with water in aqueous solution to form hydronium ions (H₃O⁺). On the other hand, the alkalinity of a solution increases (pH > 7.00) with the reduction in the H₃O⁺ concentration. This is caused by the reaction of dissociated hydroxide ions (OH⁻) from introduced alkaline with H⁺ ions from water dissociation to form water (H₂O) rather than hydronium ions. It is well documented that elemental and compound deposition responds to this chemical dynamic mainly in wet deposition techniques such as chemical bath deposition (CBD) [48] and electrodeposition techniques [49]. With emphasis on electrodeposition, the effect of pH on the bath and the deposited layers vary from selective deposition/etching of element [50], alteration of the characteristic properties of the deposited layers [51,52], elemental/compound precipitation [53],

and increase in the deposition current density [54]. Furthermore, the effect of pH on the dissociation of common solvent such as water is also well documented in the literature [55], with the notion that an increase in the acidity of an electroplating bath results in the increase in the concentration of dissociated ions in the aqueous solution [55]. Due to the increased ionic concentration, the deposition current density increases until it stabilises or continues to increase, depending on the composition of the solution.

3.3. Deposition Temperature

It is a known fact that an increase in the temperature of a matter increases the motion of the molecules inside it. As such, the electrolytic bath temperature increases solubility of the solvent, catalyses the reactions, energizes the ions, and increases the transport number, which results in an increase in the deposition current density and rate of deposition of constituent elements or compounds. Further to this, the work performed on electrodeposition depicted that an increase in the crystallinity of as-deposited semiconductor material is achievable at higher growth temperature [3,56]. For electroplated semiconductor materials from aqueous solution, there is a limitation on the growth temperature due to the boiling temperature of water at 100 °C under standard atmospheric pressure, while the electroplating from other electrolytic baths can go as high as 160 °C [31]. Deposition of materials at higher temperature provides energy required for ions/atoms to move around and deposit in a regular crystalline pattern.

3.4. Deposition Current Density

With regards to Faraday's law of electrodeposition, the deposition current density is directly related to the thickness of the deposited layer. Thus, the deposition current density is dependent on factors effecting the energizing of the inherent ions in the electrolyte such as stirring rate, bath temperature, concentration of constituent [57], and electrical conductivity of the substrate amongst other constraints. While a gradual alteration in the deposition current density is expected depending on the electrical conductivity of the electroplated layers.

With respect to semiconductor materials such as CdTe, the literature depicts the effect of current density on the morphological, compositional and the structural properties of the deposited layer [58,59]. Based on the deposition configuration, it can be inferred that the deposition current density of three-electrode configuration and two-electrode deposition configuration vary. CdTe with optimal characteristic properties deposited from a three-electrode deposition is known to lie between \sim (0.3–0.6) mA cm⁻² [57,60]. While two-electrode electrodeposition has been documented to produce CdTe layers with an optimal characteristic property of ~(0.15–0.18) mA cm⁻² [61]. Under potentiostatic mode, Basol (1988) clarified that the deposition current density for CdTe electroplating depends on the tellurium concentration in the electrolyte [57]. The incorporation of excessive Te can alter the composition of the deposited CdTe, conduction type to p-CdTe due to Te-richness [62], and reduce adhesion on the underlying substrate. Reduction in the adhesion of CdTe may also occur due to the deficiency of Te concentration in the electrolytic bath. In either condition (excess or deficiency of Te concentration in the electrolyte), the crystallinity, morphology, and adhesion of the ensued CdTe layer suffer. In addition, current density during co-deposition of competing ions such as Ga^{3+} and Fe^{2+} in the electroplating of Fe-Ga alloys is a determinant of the Fe:Ga elemental composition ratio of the resultant alloy [63].

3.5. Duration of Deposition and Thickness

Electroplating of materials with main emphasis on semiconductor commences by the nucleation of the most electropositive element on the points on the conducting substrates with the highest electric field. Therefore, it can be categorically stated that the nucleation and nucleation modes of semiconductor material is conductive substrate dependent [1,22,64]. Consequential to the surface roughness of the underlying working electrode such as glass/fluorine-doped tin oxide (g/FTO),

the highest electric field is experienced at the peaks of the rough surfaces. The nucleation of the electroplated material spreads out through to the lowest valley from the initiation rough surface peaks resulting into columnar nature of the deposited layers [14]. The potency of this mechanism is highly influential at the initial stages of deposition due to unevenness of the deposited layer thickness characterised by pin-holes, voids, gaps, and high dislocation density within the semiconductor material [21]. This characteristic property is detrimental when a thin semiconductor layer with a thickness of <100 nm is required [21].

4. Strengths and Weaknesses of Electrodeposition

4.1. Strengths of Electrodeposition

4.1.1. Electrolytic Bath Life Longevity and Self -Purification

At the start of an electrolytic bath, electro-purification of the bath is highly essential to reduce and eliminate the impurity level, which is mostly incorporated in the precursors amongst other impurity sources. It should be noted that even with a high purity precursor with 99.999% purity, it can carry an impurity level of 10 ppm. Purification is essential due to the effect of impurities even in ppm levels [65] on the characteristic properties of electroplated semiconductor materials. It should be noted that electro-purification of a bath must be performed using similar deposition parameters (such as bath temperature, pH, stirring rate, etc.) to the semiconductor deposition. The electro-purification potential utilised should be lower than the deposition potential range of the required elements established using cyclic voltammetry. Based on this characteristic property of electroplating technique, the more layers deposited, the purer the electrolyte and the electroplated semiconductor gets due to the gradual reduction of background impurities and improved material property. This property not only increases the purity of the electrolyte and the deposited semiconductor, but also increases the longevity of the bath as compared to the batch process of chemical bath deposition (CBD) technique.

To further mitigate other sources of impurities, a fraction of researchers choose two-electrode over the three-electrode configuration to avoid possible impurities from the reference electrode. While the usage of Teflon-ware (polypropylene beaker) is necessitated to house the electrolyte due to possible leaching of elemental sodium and other dopants from glass-wares [66] into acidic electrolytes.

4.1.2. Ease of Doping Intrinsic and Extrinsic

With the effective purification of the electrolyte, intrinsic doping has been demonstrated in the literature for binary [38,67], ternary [68], and quaternary [69,70] semiconductor materials by changing the deposition voltage. Taking an example of a I–III–VI₂ semiconductor materials such as CuInGaSe₂, the stoichiometric semiconductor layer consists of 25% of the group I element, 25% of the group III elements, and 50% of group VI element. Due to the positive reduction potential of Cu ($E_0 = 0.52$ V), at low deposition voltages, high elemental composition of Cu (group I) is incorporated in the semiconductor resulting into *p*-type conduction type. But an increase in the cathodic voltage increases the elemental composition resulting in an *n*-type semiconductor material, as in the case of CuInSe2 (see Figure 3a). While at intermediate voltages, the material exhibits insulating or intrinsic properties. This electrical characteristic property, as demonstrated in the literature [68–70], signifies the ability of growth of *p*-, *i*-, and *n*-type materials from the same bath by cathodic voltage variation (see Figure 3b).

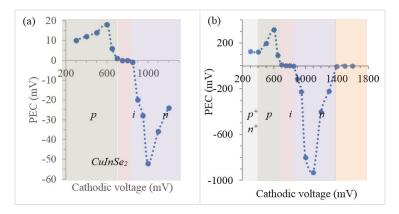


Figure 3. Photoelectrochemical (PEC) cell measurement signal for (**a**) CuInSe₂ and (**b**) CuInGaSe₂ with increasing cathodic voltages. Note the ability to grow p⁺, p, i, n, and n⁺ materials from the same electrolyte, simply by varying the deposition voltage. Reproduced from [68,70] with permission; Copyright 2004 Sheffield Hallam University.

The effect of cathodic voltage on the elemental composition of binary semiconductors has also been demonstrated and documented in the literature [14,62]. The effect of alteration in the growth voltage on the elemental composition of electroplated materials even for as low as 1 mV step has been documented [29] (see Figure 4).

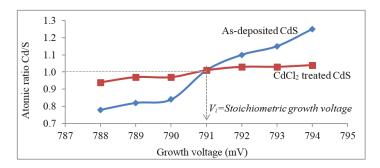


Figure 4. Atomic composition ratios of Cd to S in as-deposited and CdCl₂ treated CdS thin films at different deposition cathodic voltages.

The ease of intrinsic doping and the effect of extrinsic doping of electroplated semiconductor materials have been well established in the literature [65,71]. Due to the simplicity of ED, doping at the ppm level is made possible [65,71,72].

4.1.3. Bandgap Engineering Capability

The control or alteration of the bandgap of materials (with emphasis on semiconductor) is easily achievable in electrodeposition techniques. Typically, this can be achieved by controlling the atomic composition of the elemental component of the semiconductor material. Intrinsically, electrodeposition has the ability to change the composition of growing material by a simple alteration of the cathodic voltage [38,68–70]. An ensuing alteration in the bandgap of grown semiconductor material due to change in the growth cathodic voltage has been documented in the literature [42]. It is well known that an increase in the atomic concentration of Ga in CuInGaSe₂ by increasing the cathodic voltage increases

the bandgap of CuInGaSe₂. While a reduction in the cathodic voltage of the CuInGaSe₂ results in the reduction of bandgap due to the richness of Cu [42] (see Figure 5). This ability provides the ease of bandgap engineering of semiconductor material such as CuInGaSe₂ between ~1.00 and 2.20 eV. Extrinsically, this observation has also been documented for electroplated binary semiconductor materials such as CdTe doped with Ga [65] amongst others. The bandgap of the resulting doped semiconductor directly affected the incorporated dopant even at the parts per million level [65,71].

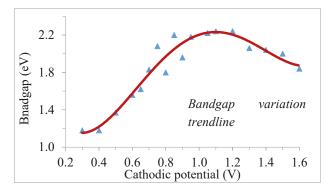


Figure 5. Energy bandgap variation for CuInGaSe₂ as a function of the cathodic voltage.

4.1.4. Low Cost and Simplicity

There are over 14 different and well-established techniques to grow thin-film semiconductor materials [73] which can be broadly categorised under physical or chemical deposition. Physical deposition refers to the technologies in which material is released from a source and deposited on a substrate using thermodynamic, electromechanical or mechanical processes [1,74]. Chemical deposition techniques are accomplished by the utilisation of precursors either in their liquid or gaseous state to produce a chemical reaction on the surface of a substrate, leaving behind chemically deposited thin-film coatings on the substrate. Electrodeposition falls under chemical deposition techniques which can be carried out in an uncontrolled environment and without a vacuum system. The setup for electroplating which is mainly constituted of a computerized potentiostat and hotplate/magnetic stirrer with a cost implication of less than £5000 as compared to other techniques such as the well-established metallorganic chemical vapour deposition (MOCVD) or close space sublimation (CSS) system with a high initial cost implication of about £1 million for a laboratory setup. In addition, these systems have limitations as concerning the materials that can be grown. Furthermore, the relatively low heat energy required during growth and post-growth treatment makes electroplating a more energy-economic deposition technique as compared to a large number of other techniques. More importantly, grown semiconductor layers using cost-effective electroplating techniques are comparable to semiconductor layers grown using highly expensive techniques [29,75], and they all require post-deposition treatments [76,77].

4.1.5. Scalability and Manufacturability

The scalability and manufacturability of electroplating has been demonstrated on an industrial scale by British Petroleum (BP) Solar in the 1980s and 1990s [78,79]. BP Solar manufactured CdTe-based solar cells with a solar panel area ~1 m² with a conversion efficiency of ~10% [78,79]. As compared to the laboratory scale setup as shown in Figure 2, scaling up requires a larger tank to contain the electrolyte and multi-plate cathode attached to multiple conducting substrates. The use of larger tanks and multi-plate cathode increases the throughput of deposited layers and an added advantage of electroplating on intricate shapes and designs.

4.2. Weaknesses of Electrodeposition

One of the main disadvantages of electrodeposition includes comparatively low rates of deposition and the need for a conducting substrate as the working electrode in the electroplating setup. Due to this requirement, using conventional characterisation techniques such as the Hall effect to determine the electrical properties of the deposited layers on FTO, for example, will not be possible due to the underlying conducting layer.

4.2.1. Instability of Current Density during Deposition

The control of the electrodeposition process due to the alteration of current density with increasing deposition layer thickness is a challenge (under potentiostatic condition). The electroplating of materials with electrical conductivity levels lower than the primary substrate results in the reduction of current density with a direct relationship with the thickness of the deposited material [80]. This observation is common for both 2E and 3E electroplating configurations, but the applied voltage can vary slightly in 2E configuration.

4.2.2. Control and Regulation of Ions within the Electrolytic Bath

The chemical concentration of ionic species in an electrolytic bath is defined during bath creation, but the control, regulation and measurement of ionic concentration within the electrolytic bath during electroplating remains a challenge. This is as a result of the depletion in the ionic concentration and the inability to gauge/measure the concentration change during and after initial deposition, therefore replenishing the bath with the appropriate chemical concentration becomes difficult and thereby reducing reproducibility tendencies of electroplated layers.

4.2.3. Formation of Solution-Based Complexes

There is a possibility for the formation of complexes within the electrolyte which might be debarring the deposition of an element and/or the co-deposition of a compound [32,33]. This is the case for the deposition of CdTe from aqueous solution containing CdI₂ as the Cd-precursor. The literature shows that due to the formation of Cd-I complexes in aqueous solution, only p-CdTe layers due to Te-richness is possible [32,33]. Unnecessary precipitation removes chemicals from the electrolyte, changing the elemental concentration in the bath.

4.2.4. Extrinsic Doping of Electrolytic Bath by the Electrodes

Control of purity throughout the electrolytic bath lifespan if an electrolytic bath is essential. It is well known that the purity of an electrolytic bath increases with the deposition aging of the bath but there is a tendency of an influx of impurity which might be due to etching, corrosion or dissolution of the electrode. For electrodeposition setup using carbon electrode, there has been observation of increased carbon concentration in deposited semiconductor layers. The incorporation of carbon into the electrolytic bath is due to the deterioration of the anode utilised in the electrolytic cell setup.

4.2.5. Non-Uniformity of Electrodeposited Semiconductor Layers

Due to the unevenness of the underlying conducting substrate such as transparent conducting oxide (TCO), the highest electric field is experienced at the peaks of the rough conducting substrate surfaces. Nucleation starts at the peaks and spreads out through to the lowest valley resulting into layers with columnar nature [14].

4.2.6. Post-Growth Treatment

It is well documented that electrodeposited layers with an emphasis on semiconductors often require post-deposition treatment to further improve their structural, morphological, compositional, and optical properties [81–83]. It is, although, arguable that other semiconductor deposition techniques

such as [77], MOCVD [84], and CSS [85] also require such treatments, as it is evident in the performances of the applications utilised for References [81–83].

Asides semiconductors, other issues such as the influence of different process conditions on mechanical properties of electroplated materials and the control of the integrity of the electroplated layers as it relates to further processing have also been the raised [86,87], but not discussed in this communication.

5. All-Electroplated Photovoltaic Devices

The comparability of the structural, morphological, compositional, optical, and other material properties has been well documented in the literature [29,42,68,88]. Electrodeposited cadmium telluride (CdTe) and copper indium gallium selenide (CIGS) are amongst the commonly used absorber layers in all-electrodeposited photovoltaic applications [57,89]. The versatility of the technique in the growth of all-electrodeposited configurations has been well documented [13,90–92]. The band diagrams of possible n-p and n-n⁺ large Schottky barrier junctions are shown in Figure 6 fabricated using CdS/CdTe configuration. The full characterisation process of both the CdS and CdTe are documented in the literature [40,46]. The electronic properties of the fabricated photovoltaic cells obtained using current–voltage (I–V) and capacitance–voltage (C–V) techniques are summarised in Table 2.

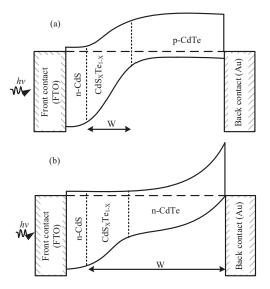


Figure 6. Energy band diagrams representing (a) glass/FTO/n-CdS/p-CdTe/Au and (b) glass/FTO/n-CdS/n-CdTe/Au device configurations.

Parameters			Values		
CdTe Growth Voltage (mV)	1340	1360	1370	1380	1400
	<i>I–V</i> un	der dark condi	tion		
$R_{\rm sh}\left(\Omega\right)$	1016	>10 ⁵	>10 ⁵	>10 ⁵	>10 ⁵
$R_{\rm s}$ (k Ω)	0.21	0.80	0.50	1.43	1.50
log (RF)	0.4	3.5	3.9	3.3	3.0
$I_{\rm o}$ (A)	$2.5 imes 10^{-5}$	$3.9 imes 10^{-9}$	$1.0 imes 10^{-9}$	$3.2 imes 10^{-9}$	$5.0 imes 10^{-9}$
n	>2.00	1.95	1.86	1.58	1.86
$\Phi_{\rm b}~({\rm eV})$	>0.52	>0.76	>0.81	>0.77	>0.77
	<i>I–V</i> under AM	[1.5 illuminatio	n condition		
I _{sc} (mA)	0.53	0.62	0.65	0.82	0.57
$J_{\rm sc}$ (mA cm ⁻²)	16.88	19.75	20.70	26.11	18.15
$V_{\rm oc}$ (V)	0.23	0.49	0.72	0.60	0.57
Fill factor	0.31	0.46	0.50	0.45	0.48
Efficiency (%)	1.20	4.45	7.50	7.05	4.97
C–V under dark condition					
$\sigma imes 10^{-4} \ (\Omega \ \mathrm{cm}^{-1})$	1.41		2.85		6.03
$N_{\rm A}$ or $N_{\rm D}$ (cm ⁻³)	$7.74 imes 10^{16}$		$3.10 imes 10^{14}$		$9.10 imes10^{14}$
μ (cm ² V ⁻¹ s ⁻¹)	0.01	-	5.74	_	4.14
C _o (pF)	1630		330		370
W (nm)	187.6		926.7		826.5

Table 2. Summary of device parameters obtained from *I*–*V* (both under illuminated and dark conditions) and *C*–*V* (dark condition) for simple CdS/CdTe-based solar cells grown at different growth voltages in the vicinity of V_i = 1370 mV.

It is well known that intrinsic CdS is n-type and remains *n*-type due to the inherent defect as a result of the presence of S vacancies and Cd interstitials in the crystal lattice of the deposited CdS layers [93]. The devices are fabricated by incorporating CdTe deposited at the vicinity of the transition voltage (V_i) from p-type to n-type CdTe or vice versa. Electroplated CdTe can either be p-type (when Te rich) or n-type (when Cd rich) material under as-deposited condition. Retention or transition of electrical conduction type is possible after cadmium chloride treatment. It is noteworthy that the conversion of the electrical conduction type after post-growth treatment may be attributed to the doping effect as a result of the heat treatment temperature, duration of treatment, initial atomic composition of Cd and Te, the concentration of CdCl₂ utilised in treatment, defect structure present in the starting CdTe layer, and the material's initial conductivity type as documented in the literature [40,41,94]. Therefore depending on the final electrical conduction type, the possible device configurations are possible, and the analysis of device results must be performed with extreme care.

Table 2 summarises the results of CdS/CdTe solar cells made with CdTe layers grown in the vicinity of V_i = 1370 mV. Below the V_i , the CdTe layers are p-type and therefore the devices made are p-n junctions (see Figure 6a). Above the V_i , the CdTe layers are n-type and hence the device structures are n-n⁺ Schottky barrier (see Figure 6b). As shown in Table 2, the devices fabricated with n-CdTe performs better than those made with p-CdTe layers.

CdTe-based devices assuming p-CdTe in CdS/CdTe devices has been documented in the literature [27,95]. But based on recent observations, the incorporation of Cd-rich CdTe absorber layers produce high efficiencies. These effects have been independently observed and reported [96,97] and mainly attributed to the reduced defects in Cd-rich CdTe (the layers are deposited using physical deposition processes).

Using mainly n-CdTe absorber layers, few devices incorporating all-electrodeposited from the SHU group have been documented in the literature and summarised in Table 3.

	Configuration					
Properties	g/FTO/n-CdS/ n-CdTe/Au (Two-Layer Device)	g/FTO/n-CdS/ n-CdTe/p-CdTe/ Au (Three-Layer Device)	g/FTO/n-CdS/ n-CdTe/p-CdTe/ Cu-Au (Three-Layer Device)	Glass/FTO/n-ZnS/ n-CdS/n-CdTe/Au (Three-Layer Device)		
	I-	-V under dark conditio	on			
$ \frac{R_{\rm sh}(\Omega)}{R_{\rm s}({\rm k}\Omega)} $ log (RF)	>10 ⁵ 0.50 3.9	$>7.2 \times 10^5$ 0.50 4.1	10 ⁶ 0.92 3.5	>10 ⁵ 0.47 4.8		
I_{o} (A) n Φ_{b} (eV)	1.0×10^{-9} 1.86 >0.81	$1.0 imes 10^{-9}$ 1.86 >0.80	3.16×10^{-9} 1.68 >0.80	$1.0 imes 10^{-9}$ 1.60 >0.82		
	<i>I–V</i> unde	r 1.5 AM illumination	condition			
$I_{sc} (mA)$ $J_{sc} (mA cm^{-2})$ $V_{oc} (V)$ Fill factor Efficiency (%)	0.65 20.70 0.72 0.50 7.50	1.06 33.80 0.73 0.62 15.3	1.85 58.9 0.64 0.50 18.5	1.07 34.08 0.73 0.57 14.18		
	C-	-V under dark conditi	on			
$\sigma imes 10^{-4} (\Omega \ cm)^{-1}$	2.85	_	-	8.82		
$N_{\rm D}-N_{\rm A} ({\rm cm}^{-3}) \\ \mu ({\rm cm}^2 {\rm V}^{-1} {\rm s}^{-1}) \\ C_{\rm o} ({\rm pF}) \\ W ({\rm nm})$	$\begin{array}{c} 3.10 \times 10^{14} \\ 5.74 \\ 330 \\ 926.7 \end{array}$	6.67×10^{14} - 395 -	1.82×10^{14} - 160 -	$7.79 \times 10^{14} \\ 7.07 \\ 280 \\ 1092.2$		

Table 3. Summary of device parameters obtained from *I–V* (both under illuminated and dark conditions) and *C–V* (dark condition) for glass/FTO/n-CdS/n-CdTe/Au and glass/FTO/n-ZnS/n-CdS/n-CdTe/Au solar cells.

6. Conclusions

This work describes electroplating as a robust material deposition technique with wide applications ranging from surface protection to large-area electronics and nano-technology while focusing on semiconductor deposition. The manuscript also reviews the pros and cons of electroplating techniques. The effect of growth parameters such as temperature, pH, stirring rate, precursor, solvent and cathodic voltage, and post-growth heat treatments of the deposited were iterated. The capability of electroplated material to be comparable and possibly superior to semiconductor materials grown using other cash intensive techniques are also highlighted with experimental evidence. Electroplated materials can be applicable in large-area devices such as photovoltaic solar panels and large-area display panels in which intricate shapes are required. Bandgap grading, alteration of elemental composition, and different conductivity type are also possible intrinsically with a change in the cathodic voltage. Other advantages such as columnar growth of nanorods which are tightly packed and normal to the substrate could trigger many new applications in the nanotechnology area.

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