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Design and Control of Power Converters 2019

Edited by
Manuel Arias

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Special Issue Editor

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About the Special Issue Editor

Manuel Arias received an M.Sc. degree in electrical engineering from the University of Oviedo, Spain in 2005 and a Ph.D. degree from the same university in 2010. In 2007 he joined the University of Oviedo as an Assistant Professor and since 2016 he has been an Associate Professor at the same university. His research interests include ac–dc and dc–dc converters, battery-cell equalizers, and LED lighting.

Preface to ”Design and Control of Power Converters 2019”

In terms of research, power electronics is one of the most prolific fields in the world of electronics. One of the main reasons for this is its relevance for present-day society, which is increasingly concerned with energy-saving and greener energy production. This scenario constitutes a powerful catalyst for research, not only boosting the amount of interesting ideas, solutions, and studies, but also the number of topics that emerge under the umbrella of power electronics. This can be seen in the fact that well-established research topics as varied as renewable energies, battery management,
and electric traction coexist—or even merge—with more recent topics such as LED lighting or micro- and nano-grids. Moreover, these topics can be considered as established when compared to others like wide-band-gap devices and electric vehicles, where research is still incipient.

In all of the aforementioned topics, in addition to others, the “design and control of power converters” plays a key role. In this book, representative papers that focus on well-established topics, as well as more recent ones, can be found. This mixture will unquestionably foster new ideas for readers and will help researchers detect solutions that can be migrated from one topic to another, making this book a relevant milestone for any power electronics engineer.

Manuel Arias
Special Issue Editor

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Article

Computer-Aided Design of Digital Compensators for DC/DC Power Converters

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Abstract: Digital control of high-frequency power converters has been used extensively in recent years, providing flexibility, enhancing integration, and allowing for smart control strategies. The core of standard digital control is the discrete linear compensator, which can be calculated in the frequency domain using well-known methods based on the frequency response requirements (crossover frequency, f_c, and phase margin, PM). However, for a given compensator topology, it is not possible to fulfill all combinations of crossover frequency and phase margin, due to the frequency response of the controlled plant and the limitations of the compensator. This paper studies the performance space (f_c, PM) that includes the set of achievable crossover frequencies and phase margin requirements for a combination of converter topology, compensator topology, and sensors, taking into account the effects of digital implementation, such as delays and limit cycling. Regarding limit cycling, two different conditions have been considered, which are related to the design of the digital compensator: a limited compensator integral gain, and a minimum gain margin. This approach can be easily implemented by a computer to speed up the calculations. The performance space provides significant insight into the control design, and can be used to compare compensator designs, select the simplest compensator topology to achieve a given requirement, determine the dynamic limitations of a given configuration, and analyze the effects of delays in the performance of the control loop. Moreover, a figure of merit is proposed to compare the dynamic performance of the different designs. The main goal is to provide a tool that identifies the most suitable compensator design in terms of the dynamic performance, the complexity of the implementation, and the computational resources. The proposed procedure to design the compensator has been validated in the laboratory using an actual DC/DC converter and a digital hardware controller. The tests also validate the theoretical performance space and the most suitable compensator design for a given dynamic specification.

Keywords: power converters; digital control; design space; frequency domain

1. Introduction

Digital controllers have conquered new areas where analog control was predominant, such as high-frequency DC/DC converters. Features such as special operation modes [1,2], complex control and modulation strategies [3], self-identification [4], autotuning [5–7], communications [8], compensator flexibility, and technology integration [9–11] are the added values provided by digital control.

Digital control of high-frequency converters has been approached using different control techniques. State feedback techniques have been used in [12–14], allowing for the arbitrary placement of the closed loop poles. Full state feedback (inductor current and output voltage) is used in [12] to implement the control law, providing improved performance in a boost converter acting as a power factor corrector. In [13,14], state feedback is applied to multiphase power converters to

ensure current-sharing. These techniques are suitable for keeping different quantities in control, typically current and voltage. Therefore, they can be considered as an alternative in multiple loop control structures.

Reference [15] proposes a time-domain design method. The digital compensator is derived from specified rise time and overshoot. In [16], the compensator is designed based on the Internal Model Control design method used in motor control. In [17], complex zero compensation is used to improve transient response. In [18], the root locus method is applied to the calculation of a digital controller for a multiphase buck converter.

Frequency domain techniques are very popular when designing analog linear compensators for DC/DC converters [19]. The compensator is calculated by determining the frequency response of the plant and the dynamic requirements regarding their crossover frequency (f_c) and phase margin (PM). A classical design approach, such as the K-factor method [20] ensures that the magnitude of the open-loop gain is 0 dB at the crossover frequency, and the phase of the open-loop gain provides the required phase margin at that frequency. These design techniques can also be applied to digital linear compensators, considering the discrete nature of the compensator and its implementation, which implies additional factors concerning the analog approach, such as sampling frequency, time delays, and quantization issues. However, the designed controller may not fulfill the expected specifications due to the limitations of the design method itself and the digital implementation—that is, there are $(f_c,\ PM)$ combinations which are impossible to reach.

In [21], an autotuning system, illustrated with a buck converter, automatically calculated digital PI (proportional-integral), PD (proportional-derivative), and PID (proportional integral derivative) compensators. The $(f_c,\ PM)$ requirements and the knowledge of the converter dynamics issued from the autotuning system were the basis for the compensator calculation, but this design approach does not consider in detail the attainability of f_c and PM requirements. In [22], the digital compensator was calculated directly in the z domain, taking a given value of f_c and PM as target performance, without a previous analysis of which of their values could be reached with the proposed compensator type. In [23], the compensator calculation was integrated into the design and optimization process. The design space of the power converter was analyzed considering that the controller was a digital PID, including saturation effects. Different design spaces were proposed, with each one for a particular $(f_c,\ PM)$ specification.

In all the cited cases, the compensator was calculated from the desired values of $(f_c,\ PM)$ and the rest of the bandwidth was ignored. Thus, due to the frequency response of the system, the open-loop gain may cross 0 dB at frequencies different to the crossover frequency, yielding a design that does not meet the dynamic specifications and which could even be unstable. Because of this limitation, each design must be checked after its calculations. If the design does not meet the requirements, it is difficult to decide whether to modify the dynamic specifications, change the topology of the compensator, or modify the sensor.

Thus, it is very interesting and useful for the designer to know the limited set of possible achievable dynamic specifications for a combination of a power converter, compensator, and sensor. This set determines the performance space of the controller regarding the achievable crossover frequency, f_c, and phase margin, PM.

References [24,25] present studies of the design space of analog compensators. However, there are issues related to digital implementation that have an impact on the calculation of the design space and require further investigation, such as sampling frequency, time delays, and limit cycling [26,27]. The consideration of these effects involves additional boundaries and substantially modifies the aspect of the performance space.

This paper proposes a design tool integrating frequency-based design techniques to: (a) determine all the possible solutions without establishing, a priori, the design target $(f_c,\ PM)$; (b) assess the influence of different parameters of the compensator on the dynamic performance of the system;

(c) determine the simplest compensator design regarding the dynamic performance for a given dynamic specification, the complexity of the implementation and the computational resources.

This work presents the algorithms to calculate this new performance space and analyze their impact on the controller design. The graphical representation of the performance space in the axis $(f_c,\ PM)$ can provide the designer with a deep insight on the influence of design parameters through sensitivity analysis. The contribution of this paper regarding prior work is the exhaustive analysis of the digital compensator design (especially in the case of PID); consideration of the limit cycling conditions; and experimental validation.

Section 2 deals with the proposed approach to designing the digital compensator, the description of the limit cycling conditions, and the proposal of a criterion to compare the performance of compensators that provide the same crossover frequency and phase margin. The performance space is introduced in Section 3, defined as a set of feasible and stable designs characterized by their dynamic performance regarding $(f_c,\ PM)$. Section 4 presents the experimental validation of the proposal. Section 5 summarizes the conclusions of the work.

2. Elements for the Calculation of the Digital Compensator

2.1. Model of the System in the Frequency Domain

There are different approaches to calculating a digital linear compensator to control a power converter. One of them is based on the calculation of a continuous compensator that fulfills the dynamic requirements [28,29]. This continuous compensator is discretized by means of conventional methods, such as bilinear or Tustin transformation, to obtain the discrete compensator. This approach provides robustness to the design and confidence for analog designers. However, in some cases, the resulting controller is more complex than required because it includes additional poles that are not necessary for the digital controller (e.g., high-frequency poles are not required since the controlled quantity is sampled at the switching frequency).

A second approach is based on calculating the exact model of the converter in the discrete domain, obtaining its z transfer function [30,31]. This alternative allows for the direct calculation of the discrete compensator using conventional design techniques for discrete control systems. However, this modeling technique is less extended among the conventional design procedures.

The approach used in this work is based on the frequency response of every block, with its continuous or discrete nature being independent and the frequency range limited to half the switching frequency. Although this is an approximation, it works well, as described in later sections, and provides flexibility to the designer. The elements of the block diagram (Figure 1) are as follows:

- The discrete compensator $C(\omega)$ is the element to be calculated. Its frequency response is calculated by the direct substitution of z by $e^{j\omega\tau_{samp}}$, where τ_{samp} is the sampling period. Despite the sampling period τ_{samp} and switching period τ not necessarily being equal, in this work, they are considered the same for the sake of simplicity ($\tau_{samp} = \tau$);
- Switching power converter $G_{vd}(\omega)$. The more accurate approach to obtaining the frequency response of the power converter (plant) is exact discrete modeling [30,31]. However, good results can also be obtained by using averaged modeling techniques [19,32] or experimental measurements. If a continuous averaged model is used, the small alias approach should be ensured. In the case of exact discrete modeling or experimental results, the effect of a large ripple is inherently considered;
- Time delay τ_{delay}. All time delays are lumped in a single block despite their origin: modulator [32], analog to digital converter (ADC) and computation. This approximation is valid in most cases. More detailed descriptions could consider the time delay block split in several parts, but this approach is numerically equivalent to the consideration of a single block;
- Static gains of modulator (G_{PWM0}) and analog to digital converter (G_{ADC0});
- Sensor transfer function $G_S(\omega)$.

The key transfer function to calculate the compensator is the uncompensated loop transfer function T_U given in Equation (1), where $\omega < \pi/\tau$. The open-loop transfer function T is defined in Equation (2).

$$T_U(\omega) = G_{PWM0} \cdot e^{-j\omega \cdot \tau_{delay}} G_{ADC0} G_{vd}(\omega) G_S(\omega) \tag{1}$$

$$T(\omega) = T_U(\omega) C(\omega) \tag{2}$$

2.2. Compensator Calculation

The calculation of the compensator is based on the specified phase margin and crossover frequency in Equations (3) and (4). Therefore, there are two constraints: the first concerning the definition of the cross-over frequency, f_c, since the magnitude of the compensated transfer function has to be equal to 1 at f_c Equation (3); and the second concerning the definition of phase margin, PM Equation (4).

$$|T_U(\omega) \cdot C(\omega)| = 1 = 0\ dB\ if\ \omega = \omega_c = 2\pi \cdot f_c \tag{3}$$

$$arg(T_U(\omega_c) \cdot C(\omega_c)) = -\pi + PM \tag{4}$$

Without loss of generality, two different compensator types are considered: PI (5) and PID (6).

$$C_{PI}(z) = K \frac{\left(z - e^{-2\pi \cdot f_z \cdot \tau}\right)}{(z-1)} = K \frac{(z - r_z)}{(z-1)} \tag{5}$$

$$C_{PID}(z) = K \frac{\left(z - e^{-2\pi \cdot f_{z1} \cdot \tau}\right)\left(z - e^{-2\pi \cdot f_{z2} \cdot \tau}\right)}{(z-1)z} = K \frac{(z - r_{z1})(z - r_{z2})}{(z-1)z} \tag{6}$$

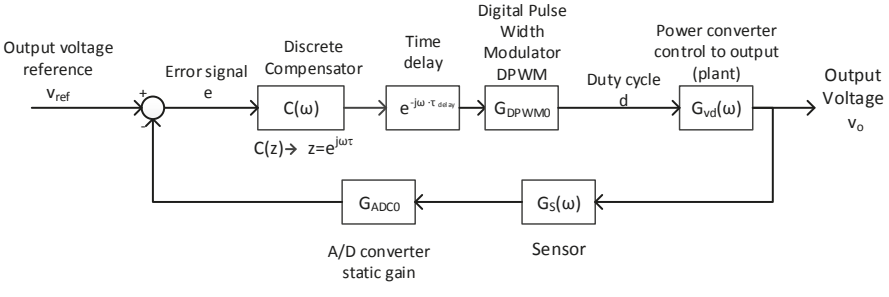


Figure 1. Block diagram of a switched power converter with digital control.

As previously explained, the compensator is calculated from the frequency response of the different blocks of the system. The frequency response of the compensator depends on the topology (PI or PID) and can be calculated by Equations (7) or (8).

$$C_{PI}(\omega) = C_{PI}(z)|_{z=e^{j\omega\tau}} \tag{7}$$

$$C_{\mathrm{PID}}(\omega) = C_{\mathrm{PID}}(z)|_{z=e^{j\omega\tau}} \tag{8}$$

In the proposed form, the PI regulator has only two parameters (K and f_z) that can be determined using the constraints (3) and (4). In the case of PI and PID, if the value of f_z issued from calculations is negative or complex, the solution must be discarded since it yields zeros outside the unit circle or complex coefficients in the difference equation, respectively.

However, the PID compensator has three parameters (K, f_{z1} and f_{z2}), while there are only two constraints from dynamic requirements (f_c and PM). Therefore, an additional constraint must be

established to calculate the compensator. In this work, two possibilities are considered as an additional constraint to determine the coefficients of a PID compensator:

- PID1: the ratio between the frequency of one of the zeros f_{z2} and the crossover frequency f_c is given by the designer, as expressed in Equation (9). This approach is a generalization of the proposed calculation criterion given in [33]. In this case, it is possible to derive an analytical expression of the compensator design parameters K and f_{z1} as a function of the uncompensated transfer function value at f_c, PM, and K_1, as depicted in Equations (14)–(16).

$$\frac{f_{z2}}{f_c} = K_1 \tag{9}$$

- PID2: the ratio between the frequency of both zeros is given by the designer, as expressed in Equation (10). When this ratio is equal to one, both zeros are located at the same frequency, and there are analytical expressions to calculate the compensator parameters Equations (17)–(19). However, for other values of K_2, it is not possible to derive analytical expressions to calculate the parameters directly, because the resulting equation is transcendental. Therefore, numerical methods are required to solve the nonlinear resulting expressions.

$$\frac{f_{z2}}{f_{z1}} = K_2 \tag{10}$$

In the following paragraphs, the equations to calculate each of the proposed compensators are summarized. Thus, the expressions for the calculation of proportional-integral (PI) compensator are Equations (11)–(13). Equation (11) is the transfer function, Equation (12) is the difference equation and Equation (13) is the zero location.

$$C_{PI}(z) = \frac{d(z)}{e(z)} = K\frac{(z - r_z)}{(z-1)} = K\frac{\left(1 - r_z z^{-1}\right)}{\left(1 - z^{-1}\right)} \tag{11}$$

$$d[n] = d[n-1] + K{\cdot}e[n] - K{\cdot}r_z{\cdot}e[n-1] \tag{12}$$

$$r_z = \cos(\omega_c \tau) - \frac{\sin(\omega_c \tau)}{\tan\left(PM - \pi - arg(T_U(j\omega_c)) + \operatorname{atan}\left(\frac{\sin(\omega_c \tau)}{\cos(\omega_c \tau)-1}\right)\right)} \tag{13}$$

where:

$$r_z = e^{-2\pi f_z \tau}; K = \frac{1}{\frac{\left|e^{j\omega_c \cdot \tau} - e^{-2\pi f_z \tau}\right|}{\left|e^{j\omega_c \tau} - 1\right|}\left|T_U(\omega_c)\right|}$$

Expressions for the calculation of proportional-integral-derivative PID1 compensator are Equations (14)–(16). The transfer function is Equation (14), the difference equation is Equation (15) and Equation (16) provides the location of zero 1 (note that the frequency of the other zero is determined by the value of K_1).

$$C_{PID1}(z) = \frac{d(z)}{e(z)} = K\frac{(z - r_{z1})(z - r_{z2})}{(z-1)z} = K\frac{\left(1 - r_{z1} z^{-1}\right)\left(1 - r_{z2} z^{-1}\right)}{\left(1 - z^{-1}\right)} \tag{14}$$

$$d[n] = d[n-1] + K{\cdot}e[n] - K(r_{z1} + r_{z2}){\cdot}e[n-1] + K(r_{z1}{\cdot}r_{z2}){\cdot}e[n-2] \tag{15}$$

$$r_{z1} = \frac{B{\cdot}D - A + (C - B{\cdot}E){\cdot}K_z}{(B{\cdot}E - C - B{\cdot}K_z)} \tag{16}$$

where:

$$A = \sin(2\omega_c \tau);\ B = \tan\left(PM - \pi + \arg\left(e^{j\omega_c \tau} - 1\right) + \omega_c \tau - \arg(T_U(\omega_c))\right); C = \sin(\omega_c \tau);$$

$$D = \cos(2\omega_c\tau);\ E = \cos(\omega_c\tau);\quad K_z = e^{-\omega_c K_1\tau}; r_{z1} = e^{-2\pi f_{z1}\tau}; r_{z2} = e^{-2\pi f_{z2}\tau}$$

$$K = \frac{1}{\frac{\left|e^{j\omega_c\cdot\tau} - e^{-2\pi f_{z1}\tau}\right|\cdot\left|e^{j\omega_c\cdot\tau} - e^{-2\pi f_{z2}\tau}\right|}{\left|e^{j\omega_c\tau} - 1\right|\cdot\left|e^{j\omega_c\tau}\right|}|T_U(\omega_c)|}$$

Finally, expressions for the calculation of PID2 compensator are Equations (17)–(19). The transfer function if Equation (17), the difference equation is Equation (18). Equation (19) is applicable when both zeros are located at the same frequency ($K_2 = 1$).

$$C_{PID2}(z) = \frac{d(z)}{e(z)} = K\frac{(z - r_{z1})(z - r_{z2})}{(z-1)z} = K\frac{\left(1 - r_{z1}z^{-1}\right)\left(1 - r_{z2}z^{-1}\right)}{\left(1 - z^{-1}\right)} \tag{17}$$

$$d[n] = d[n-1] + K\cdot e[n] - K(r_{z1} + r_{z2})\cdot e[n-1] + K(r_{z1}\cdot r_{z2})\cdot e[n-2] \tag{18}$$

$$r_z = \cos(\omega_c\tau) - \frac{\sin(\omega_c\tau)}{\tan\left(\frac{1}{2}\left(PM - \pi - arg(T_U(j\omega_c)) + \text{atan}\left(\frac{\sin(\omega_c\tau)}{\cos(\omega_c\tau)-1}\right) + \omega_c\tau\right)\right)} \tag{19}$$

where:

$$r_z = r_{z1} = r_{z2} = e^{-2\pi f_z\tau}; \qquad K = \frac{1}{\frac{\left|e^{j\omega_c\cdot\tau} - e^{-2\pi f_z\tau}\right|^2}{\left|e^{j\omega_c\tau} - 1\right|\cdot\left|e^{j\omega_c\tau}\right|}|T_U(\omega_c)|}$$

In the case of PID2 compensator with two zeros at different frequency ($r_{z1} \neq r_{z2}$), a numerical approach is used to find the frequency of the zeroes.

2.3. Analysis of the Calculated Compensators

The expressions (11)–(19) provide the compensator parameters to meet the requirements of gain and phase only at the crossover frequency. However, as mentioned in the introduction, because of the frequency response of the plant, the behavior of the open-loop gain at other frequencies can render the solution unstable or not feasible, or even result in a different dynamic performance than expected. Thus, it is interesting to analyze these possibilities considering the whole bandwidth of the loop transfer function.

Five combinations of crossover frequency and phase margin have been considered to analyze the different possibilities. The resulting linear compensators yield the open-loop gain transfer functions illustrated in Figure 2. The plant considered in the calculations is a buck converter (input voltage Vin = 12 V, output voltage Vo = 3 V; output inductance $L_O = 1 \times 10^{-6}$ H; output capacitance $C_O = 47 \times 10^{-6}$ F; output power Po = 10 W; switching frequency fsw = 1000×10^3 Hz; total time delay td = (1/fsw) × 0.5). In the plots, the continuous line represents the theoretical frequency response, while the crosses correspond to the frequency response obtained from time-domain simulations using the discrete compensator performing and ACsweep with the commercial simulator PSIM.

Case 1 (target $f_c = 84$ kHz, target $PM = 45^\circ$) is a feasible solution, since the magnitude of the open-loop gain crosses 0 dB only once, the phase crosses -180° only when the magnitude is lower than 0 dB, and the obtained zero frequency is real and positive.

Case 2 (target $f_c = 79$ kHz, target $PM = 15^\circ$) is a conditionally stable solution, because the phase is lower than -180° at frequencies where the magnitude of the open-loop gain is higher than 0 dB. The point -1 is outside the Nyquist contour, but a decrease in the gain of the system could make the system unstable. Thus, this solution is discarded despite the resulting system not being formally unstable, and the crossover frequency and phase margin should not be included inside the performance space.

Case 3 (target $f_c = 20$ kHz, target $PM = 75^\circ$) is unstable because the phase is lower than -180° when the magnitude is higher than 0 dB. Therefore, this solution must be discarded.

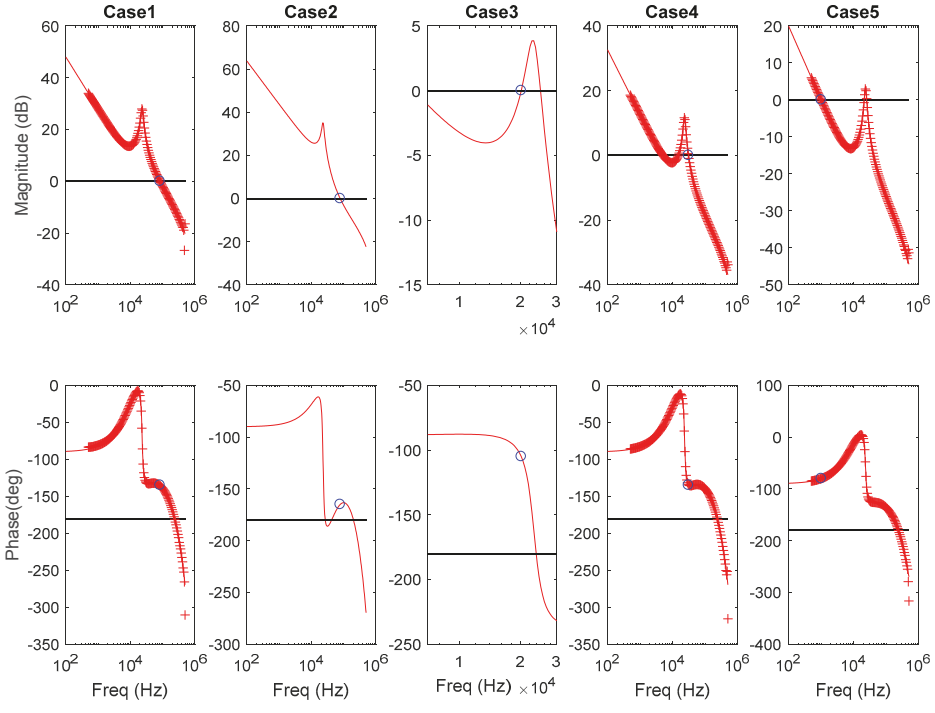


Figure 2. Open-loop transfer function for different combinations of crossover frequency and phase margin. Solid line: theoretical freq. response; crossed line: freq. response from the time-domain simulation with a PSIM simulator.

Case 4 (target $f_c = 20$ kHz, target $PM = 75^\circ$) is stable, but the effective crossover frequency is lower than expected due to the two crossings through 0 dB that appear approximately at 5 kHz and 15 kHz. The result is that the settling time of the system does not correspond with the target crossover frequency, and the system is slower than expected. Thus, with this design procedure and digital compensator, it is not possible to achieve the specified combination of crossover frequency and phase margin. This combination should be considered out of the performance space.

Case 5 (target $f_c = 1$ kHz, target $PM = 100^\circ$) is stable, but the effective crossover frequency is higher than expected. This means that the dynamic response of the system does not match the requirements. Moreover, the effective phase margin is lower. Therefore, this solution is also discarded.

The main conclusion of this analysis is that there are combinations of dynamic specifications that yield designs which should be considered out of the performance space. Reasons to discard the resulting designs are as follows:

- The magnitude of the resulting open-loop gain crosses 0 dB more than once: the solution is discarded since the effective phase margin is different than expected. Thus, the resulting design does not fulfill the dynamic specifications;
- The phase of the resulting open-loop gain crosses -180° with a magnitude greater than 0 dB: the solution is discarded because it is unstable or conditionally stable.

2.4. Limit Cycling Conditions

One of the characteristics of digitally controlled power converters is the limit cycles that can appear under different conditions. This issue is still a subject of research, especially in the case of

transient conditions; but in the literature, different conditions have been established to avoid limit cycling [26]. Some of them are related to the relative resolution between the PWM (pulse width modulator) and the ADC. These are out of the scope of this work, since they do not depend on the compensator calculation, but rather their hardware implementation. However, there are other two conditions related to the design of the linear compensator.

The first condition [26,27] is related to the compensator integral gain K_i, defined in Equation (20). The expressions of the integral gain K_i for PI and PID compensators are given in Equations (21) and (22) respectively.

$$K_i = \lim_{z \to 1}(z-1)C(z) \tag{20}$$

$$K_i = K \cdot (1 - r_z) \tag{21}$$

$$K_i = K(1 - r_{z1})(1 - r_{z2}) \tag{22}$$

This integral gain K_i must be limited in order for a single unit impulse of the error signal to produce a step change in the controlled quantity (e.g., output voltage). This condition is expressed in Equation (23). Theoretically, the parameter a is equal to 1, but in practice a, safety factor is considered, which can typically be $a = 0.5$.

$$0 < T_U(\omega = 0) \cdot K_i < a \tag{23}$$

Once the digital compensator is calculated, it is easy to check if it meets Equation (23) to determine whether the solution should be discarded and considered out of the performance space. However, when analyzing Equations (21) and (22), interesting trends can be identified. In a PI compensator, as K and r_z are directly determined by the constraints imposed by f_c and PM, the only possibility to avoid limit cycling is to change (f_c, PM); that is, to modify the dynamic requirements. On the other hand, in the case of a PID compensator (topologies PID1 and PID2), the additional degree of freedom can be used to avoid limit cycling without changing the f_c and PM requirements, but by changing the parameters of K_1 or K_2 in Equations (9) and (10).

This effect is illustrated in Figure 3. The plots show the value of $T_U(\omega = 0) \cdot K_i$ depending on the parameters K_1 or K_2 and for a given combination of f_c and PM. When K_1 or K_2 are small enough, the plotted product is lower than $a = 1$, so a limit cycling condition is avoided. The conclusion is that by decreasing the frequency of one of the PID zeros, the gain of the system at low frequency is limited enough to avoid the integral gain limit cycling. However, one zero at low frequency can result in a poor low frequency response, as will be shown in the next section. Therefore, a trade-off must be found.

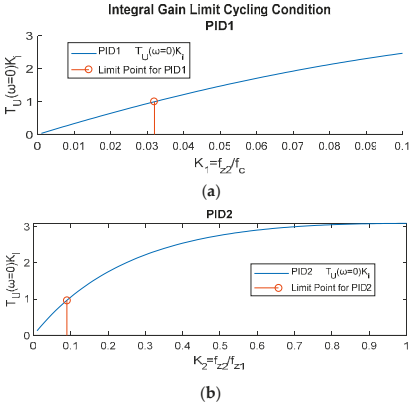


Figure 3. Analysis of the integral gain limit cycling condition for the PID1 (**a**) and PID2 (**b**) compensators.

The second limit cycling condition refers to the requirement of a minimum gain margin, GM, to avoid limit cycling due to the sampling effect in Equation (24), where the parameter α is the security margin.

$$GM > 4.2 \text{ dB} - 20 \cdot \log(\alpha) \tag{24}$$

This condition depends essentially on the crossover frequency f_c. When a high f_c is desired, close to the Nyquist frequency, the gain margin is limited, since the slope of T is limited for a PID compensator beyond f_c. Thus, changing the value of the PID parameter has a very slight effect on the GM, since beyond f_c, the value of T is very similar even if there are significant differences for low frequencies, as illustrated in the open-loop gain displayed in Figure 4a.

2.5. Difference among Solutions with the Same Crossover Frequency and Phase Margin

According to the previous section, for a given f_c and PM, there is only one possible design if all the parameters are fixed: the type of compensator, sampling frequency, parameters K_1 or K_2, and so forth. Following the previously described criteria, it is possible to determine which designs are included in the performance space and which are not. However, it would be interesting to provide a method to compare the different solutions and indicate the best one in terms of the complexity of the implementation, the computational resources, and so forth. Thus, a PI compensator is preferred to a PID for the same crossover frequency and phase margin, since the difference equation has fewer coefficients (expressions (11)–(19)). The compensator with a lower sampling period is preferred, since its implementation needs fewer digital resources.

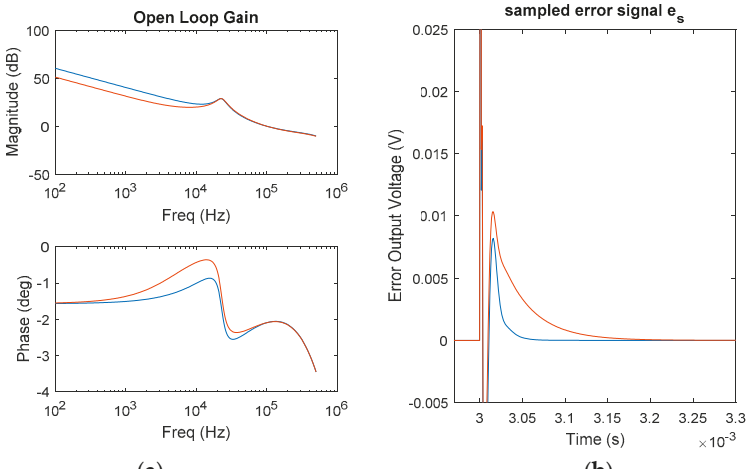


Figure 4. (**a**) Open-loop gain T, corresponding to two different designs of PID2 with the same $(f_c,\ PM)$ and different parameter values of K_2; (**b**) error signal in the time domain when a step in the reference voltage is applied.

However, for the PID compensator, there are different possible designs, since an additional design constraint is used either in PID1 and PID2. Therefore, a performance index should be established to choose between compensators with the same architecture and different parameters.

Figure 4 illustrates this issue. Two different PID2 compensators with different values of K_2 have been calculated. Both achieve the same f_c and PM, but their frequency response is different in the rest of the bandwidth (Figure 4a). The difference in magnitude is approximately 9 dB in the range of 100–1000 Hz for this illustration example. Thus, the transient response for a reference step is also different. When evaluating the error output voltage signal in the time domain—that is, the difference

between the output voltage reference (reference signal) and the actual output voltage (measured controlled signal) in Figure 4b, the design with a lower magnitude in the range of 100–1000 Hz exhibits a longer settling time.

To compare different designs with the same f_c and PM as those appearing in Figure 4, the performance index L is defined in Equation (25). This index is the norm of the difference between the closed loop transfer function of the system $CL(f_k)$ compared with the ideal one, which is equal to 1 at any frequency; f_k is the k-th element of the frequency vector, considering that the proposed design approach is numerical. $CL(f_k)$ is obtained from the open-loop transfer function $T(f_k)$. A weighting factor $\frac{1}{f_k}$ is included to give more importance to the low frequency response. The factor $\frac{f_k - f_{k-1}}{f_{max} - f_{min}}$ is considered to take the non-linear spacing in the frequency vector into account.

$$L = \sqrt{\sum_{k=1}^{N} \left| (CL(f_k) - 1) \cdot \frac{1}{f_k} \right|^2 \cdot \frac{f_k - f_{k-1}}{f_{max} - f_{min}}} = \sqrt{\sum_{k=1}^{N} \left| \left(\frac{T(f_k)}{1 + T(f_k)} - 1 \right) \cdot \frac{1}{f_k} \right|^2 \cdot \frac{f_k - f_{k-1}}{f_{max} - f_{min}}} \quad (25)$$

The ideal value of this index is $L = 0$, which means that the closed-loop transfer function is equal to 1. Comparing two different solutions—that is, two different compensators, the best solution corresponds to the minimum value of index L. It is difficult to find an exact relationship between the proposed index L and the conventional time domain indexes. However, in all tested cases, a higher value of L means a higher error in the time domain, as illustrated in Figure 5, where six different PID designs for the same $(f_c,\ PM)$ are compared. The parameters changing from one design to a different one are K_1 and K_2, as defined in Equations (9) and (10) respectively—that is, the separation between zeros of the compensator. Designs A have higher values of K_1 and K_2 than designs B, and both have higher values of K_1 and K_2 than designs C. In Figure 5a, the frequency response for the different designs is shown. In this particular case, designs PID2B and PID1B are very similar (for example, PID2B is 0.08 dB greater than PID1B at 400 Hz). In Figure 5b, the RMS (root mean square) value of the error signal in the time domain is plotted for the six designs, considering an output voltage reference step and normalizing the values to the lowest RMS value. In Figure 5c, the value of the proposed L index normalizing the value to the lower L index value is shown. Although there is no linear relationship between the time-domain error RMS value and L index value, the lower the L index value, the lower the error RMS value.

Time-response performance indexes are an extended tool to compare compensator performance [34]. However, since the presented design approach is based on the frequency domain, it is desirable to establish a performance index based on the frequency response to quickly compare different compensator performances. Note that if the design method requires the comparison of many solutions, saving computational resource is important.

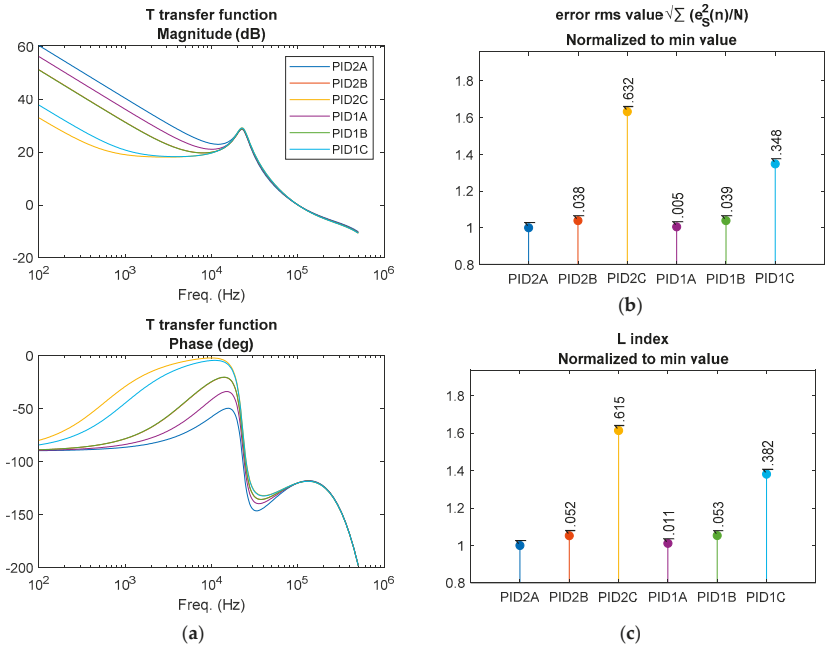


Figure 5. Comparison of solutions with the same (f_c, PM) pair corresponding to different compensator types and parameters. (**a**) Open-loop transfer function; (**b**) RMS value of the error signal obtained from the simulation; (**c**) L index obtained from the open-loop transfer function.

3. Determination of the Performance Space (f_c, PM)

The previous section introduced the frequency-based model of the system, the calculation of different compensator topologies, the criteria to determine whether the designs fulfill the dynamic requirements, and an index to compare compensators that provide the same dynamic specifications $(f_c,\ PM)$.

However, significant advantages can be obtained if the proposed calculation procedure is automated and applied to find a performance space in such a way that all the possible combinations of $(f_c,\ PM)$ that can be fulfilled are found. Thus, the performance space is graphically represented in a plot with frequency units in the horizontal axis and phase units in the vertical axis. In [25], this plot is called a solution map. In this paper, the design space is the set of parameters of the compensator that have to be calculated to obtain given results regarding $(f_c,\ PM)$—that is, to obtain a given performance. Those parameters of the compensator are, finally, the coefficients of the difference Equations (12), (15) and (18), and the performance is the pair $(f_c,\ PM)$. In the following paragraphs, an example illustrates the generation of the performance space $(f_c,\ PM)$ and the influence of different factors, such as the type of compensator and limit cycling conditions. The specifications of the power converter used as our example are as follows: buck topology, input voltage Vin = 12 V, output voltage Vo = 3; output inductance $L_O = 1 \times 10^{-6}$ H; output capacitance $C_O = 47 \times 10^{-6}$ F; capacitor equivalent series resistance $R_{ESRC} = 20 \times 10^{-3}$ Ω; output power Po = 10 W; switching frequency fsw = 1000×10^3 Hz; total time delay td = $(1/fsw) \times 0.5$.

In Figure 6a, the uncompensated open-loop transfer function T_u defined in Equation (1) is shown, including time delays, static gains, and the converter-transfer function (Figure 1). In Figure 6b, the described performance space for the example buck converter and a PID1 compensator is plotted. Limit cycling conditions are not involved in these first calculations. Every point represents a combination

of f_c and PM, and the valid combinations are grouped into different areas, considering the different possibilities discussed in Section 2.3:

- The white area corresponds to solutions with non-real or negative frequencies;
- The pink area is the set of solutions which are unstable or conditionally stable. This area is particularly large at high frequencies;
- The blue area is the set of valid solutions that corresponds to feasible stable designs with the same f_c and PM as plotted in the performance space.

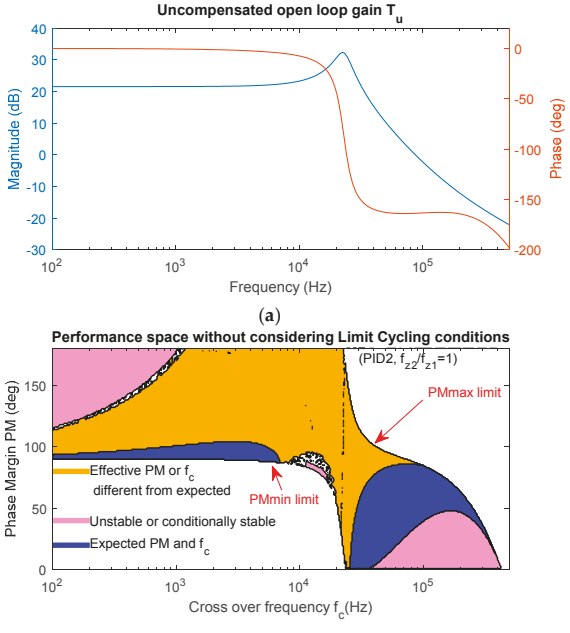


Figure 6. (**a**) Bode plot of the uncompensated transfer function, Tu; (**b**) performance space for a PID1 compensator, without considering limit cycling conditions.

The chosen plant, in this case, exhibits a relatively high Q—that is, the resonance peak is around 10 dB above the low frequency magnitude of the G_{vd} transfer function. This fact is relevant to producing pairs $(f_c,\ PM)$ corresponding to cases 2, 3, 4, and 5 in Figure 2.

The algorithm to calculate the performance space is described in the flowchart of Figure 7. It has been elaborated using the theoretical basis provided in Section 2. The maximum PM that can be achieved (PMmax limit in Figure 6b) can be theoretically calculated as the phase of the uncompensated open-loop transfer function T_U, plus the maximum phase boost that the compensator can provide. On the other hand, there is a limit at low frequencies for the PM (PMmin limit in Figure 6b), determined by the phase of the uncompensated open-loop transfer function T_U and the minimum phase provided by the compensator (-90 degree in any case). These two boundaries are relevant to reduce the calculations and shorten the calculation time of the performance space [35]. Once the initial limits of PM have been established, a double sweep is carried out. For each frequency, the value of PM is initialized and the validity conditions are checked, including those described in Section 2.2, 0 and 0. If they are met, the value of PM is increased, and the validity conditions are checked again.

Once a non-valid solution is achieved for a given frequency value, the PM loop is interrupted, and the algorithm goes to the next frequency value.

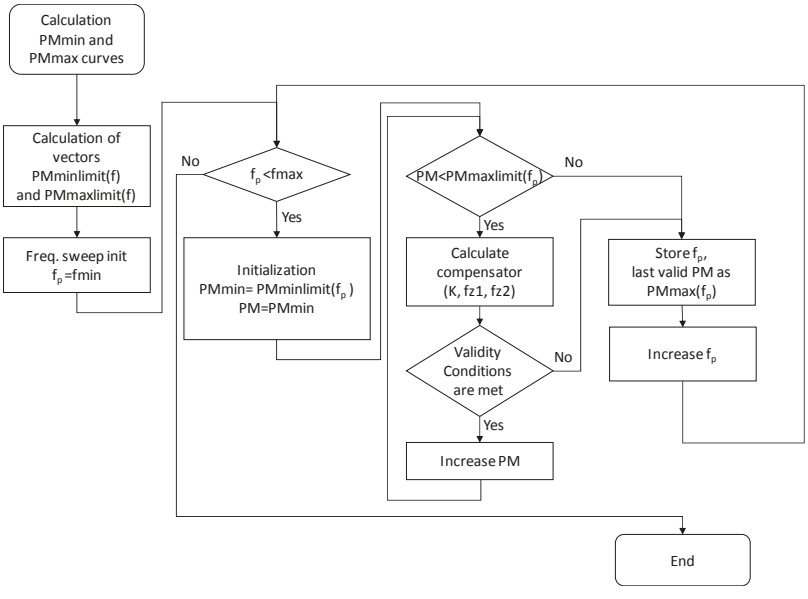


Figure 7. Flowchart of the procedure to calculate the limits of the performance space $(f_c,\ PM)$.

The flowchart in Figure 7 describes the procedure to calculate the limits of the performance space. Moreover, it can be also used to plot the complete performance space $(f_c,\ PM)$ if PMminlimit(f) and PMmaxlimit(f) are set to the minimum and maximum PM values, respectively, and the validity conditions do not interrupt the loop but are used to classify the solutions.

The most valuable contribution of this algorithm is the ability to analyze all possible designs very quickly and compare different compensator types or the influence of design parameters. The following discussion illustrates this added value.

Limit cycling conditions are analyzed in Figure 8 in the case of PID compensators. Different types of compensators and design parameters (ratio of zero frequency, K_1, and K_2) are considered by running the algorithm of Figure 7 once per compensator type and design parameter K_1 or K_2. Note that limit cycling conditions, as described in Section 2.4, can be easily included in the calculations.

The area limited by the red line in Figure 8 corresponds to the pairs $(f_c,\ PM)$ that do not meet the integral gain limit cycling condition. This area is smaller, as the separation between the zero frequencies increases (ratio f_{z2}/f_{z1} for PID2 and ratio f_{z2}/f_c for PID1 decrease). The area limited by the green line in the plots of Figure 8 is the set of solutions that do not meet the limit cycling condition referring to the gain margin. This condition is more related to the frequency itself than to the type of compensator or the value of its design parameter. No significant gains are obtained when the frequencies of the zeros are very different.

Merged results for the PID1 and PID2 compensators are shown in Figure 9. Areas limited by red or green lines in Figure 8 are now discarded designs due to the existence of limit cycles. The area limited by the blue line is the performance space free of limit cycling. In the case of PID2, there is a remarkable difference when the frequency of the zeros changes: the lower the ratio f_{z2}/f_{z1}, the wider the allowable performance space. The integral gain limit cycling condition has, in this case, the strongest influence on the allowable designs. PID1 exhibits similar behavior, although the differences are slightly less significant. Both PID1 and PID2 provide similar results when the ratios f_{z2}/f_{z1} or

f_{z2}/f_c are very small (0.01 in this case). This fact could be used as a criterion to minimize the possibility of a limit cycle, using a high separation between the frequencies of the zeros (low values of f_{z2}/f_{z1}, and f_{z2}/f_c). However, the response of the system at low frequencies can be degraded, as depicted in Section 2.5 and as it is confirmed in the experimental measurements. A trade-off should be achieved between the reduction of the area with limit cycling due to integral gain and the degradation of the low-frequency response.

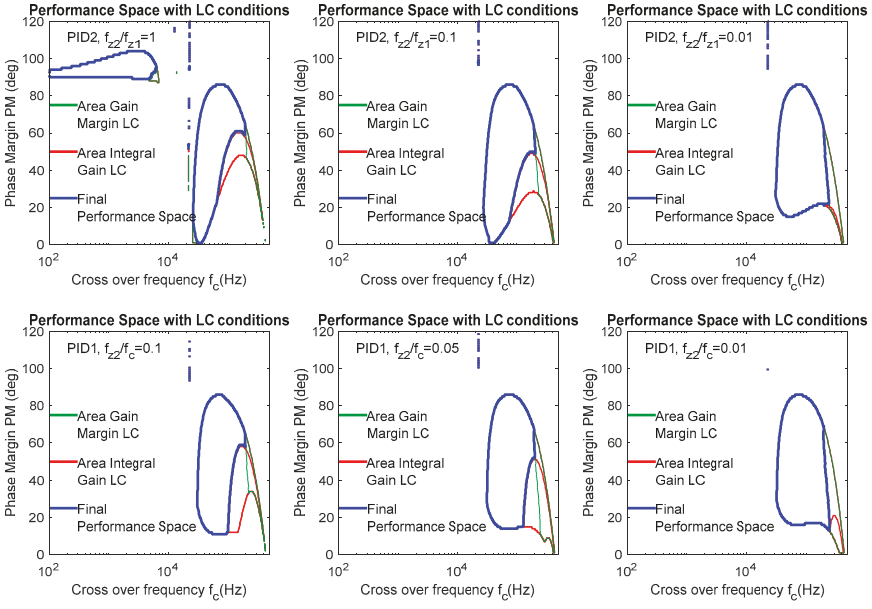


Figure 8. Performance space for PID compensators, remarking areas discarded due to the limit cycling (LC) conditions.

Figure 10 illustrates the limit cycling. Time-domain simulations with a PSIM simulator have been carried out. The ADC and the DPWM (digital PWM) are quantized, but the DPWM has a much higher resolution than the ADC. Therefore, limit cycling concerning the relative resolution of ADC and DPWM [27] is avoided. Small steps in the output voltage reference are introduced to force transient intervals. After those periods, the system enters into a steady state. If there are still oscillations in the output voltage, there is a limit cycle. As predicted by the performance space of Figure 9, two of the six analyzed designs (PID2 $f_{z2}/f_{z1} = 1$ and PID1 $f_{z2}/f_c = 0.1$) are outside the performance space in the area corresponding to limit cycling conditions. The other designs do not suffer from limit cycling, agreeing with Figure 9. Limit cycling failures occur in the case of the lower zero-frequency separation, confirming the trends identified in the previous paragraphs.

A final performance space has been calculated and plotted in Figure 11. This plot summarizes the best possible design for every dynamic requirement $(f_c,\ PM)$. Note that all considered compensator topologies cover some area in the performance space.

The first criterion to select the best solution is simplicity: PI is preferred to PID because of the reduced number of coefficients, Equations (12), (15) and (18). The second criterion is the value of index L, as defined in Section 2.5—that is, in the case of PID compensators achieving a feasible design for a given specified $(f_c,\ PM)$, the preferred solution is the one with the lower index L.

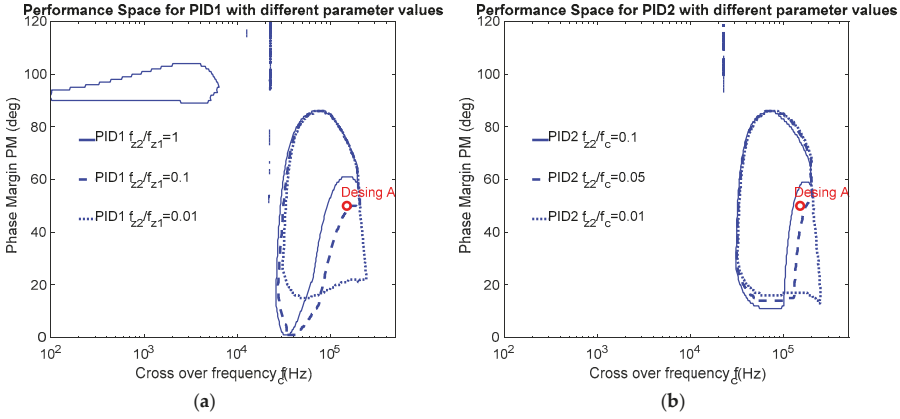


Figure 9. Performance space for the two different PID compensators, considering different values of the design parameter for each of them: (**a**) PID1; (**b**) PID2.

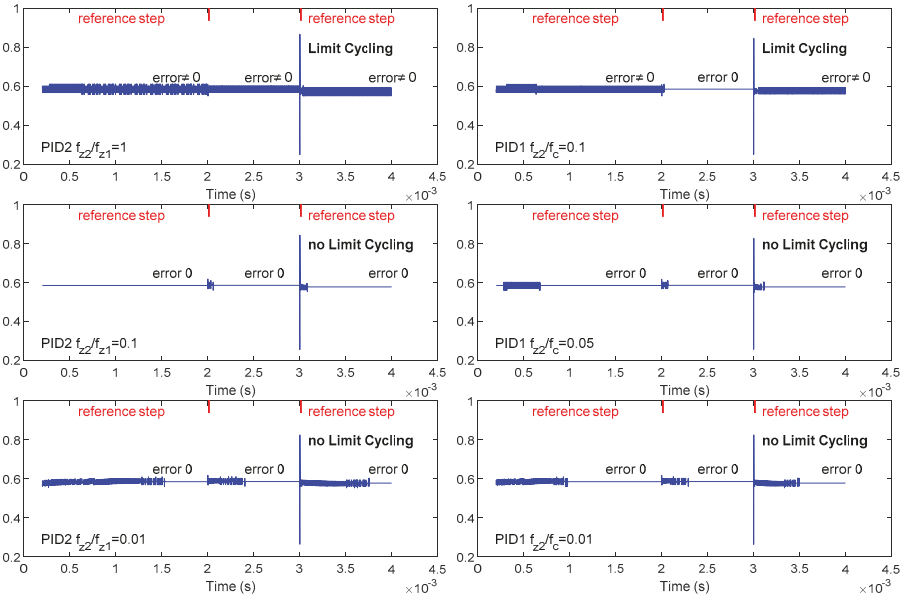


Figure 10. Time response to reference steps for different compensators corresponding to design A (Figure 8). A limit cycle exists for PID1 $f_{z2}/f_{z1} = 1$ and PID2 $f_{z2}/f_c = 0.1$, as predicted by the performance space.

Analyzing this example, the PI is obviously the best solution for a low-frequency requirement. Even if the PID can provide low values of f_c, the PI has a simpler implementation that implies less calculation in the difference equation. Designs using the PI compensator beyond the resonance frequency of the plant are limited to low values of *PM*, which in practice have no significant interest.

The preferred option for values of f_c beyond the resonance frequency is the PID2 with two zeros at the same frequency. The limitation due to the integral gain limit cycling condition can be overcome using either PID2 or PID1, with higher separation between zero frequencies.

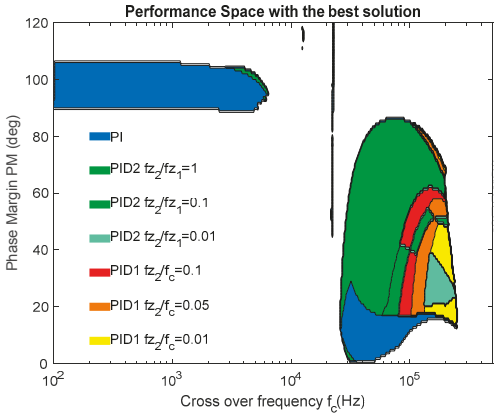


Figure 11. Performance space considering seven different compensators and selecting the best possible solution among them for each point of the performance space (f_c, PM).

All results presented in this section have been obtained by implementing in Matlab the algorithm to generate the performance space (Figure 7). Apart from the comparison of different compensators, the same procedure can be used to perform a sensitivity analysis of other parameters, such as time delays and sampling frequency [35].

4. Experimental Validation

An actual prototype has been built and tested in the laboratory to validate the proposed design procedure, the models, and the assumptions considered in this work. The digital controller has been implemented in a Zybo board, including a Xilinx Zynq-7010 device. An external ADC was used (ADS7476A), limiting the resolution to 10 bits. The specification of the power converter is as follows: input voltage Vin = 8 V, output voltage Vo = 4 V; output inductance $L_O = 76 \times 10^{-6}$ H; output capacitance $C_O = 100 \times 10^{-6}$ F; load resistance Ro = 10 Ω; switching frequency fsw = 100×10^3 Hz. The transfer function of the power converter G_{vd} (Figure 1) has not been calculated, but was measured with a frequency response analyzer. Therefore, all parasitic components (inductor and capacitor series resistances, MOSFET conduction resistance, etc.) are considered in the compensator calculation. The uncompensated loop gain T_u is shown in Figure 12, as well as the performance space, without considering the limit cycling conditions. There are some differences with the performance space presented in Figure 6b due to the differences in the uncompensated open-loop transfer function:

- The total time delay produces a significant phase loss beyond the resonance frequency of the uncompensated open loon gain, limiting the feasible solutions at high frequency (PMmax limit). This phase loss is compensated partially by the effect of the equivalent series resistance of the output capacitor;
- The Q factor is lower, and so in the performance space, there are possible solutions at crossover frequencies close to the resonance frequency.

The combination of the performance spaces for the different type of compensators and different design parameters is shown in Figure 13. In this case, PI ad PID2 with $f_{z2}/f_{z1} = 1$ are the compensator topologies that cover the major part of the area of possible designs. The PID1 topology provides possible designs at high f_c and low PM, where the PID2 with $f_{z2}/f_{z1} = 1$ does not meet the limit cycling condition regarding the integral gain.

The resulting open-loop gain has been measured in the actual prototype for three dynamic specifications, named as design point 1, 2, and 3, detailed in Figure 13. For each design point, both PID1 and PID2 have been designed with $f_{z2}/f_c = 0.1$ and $f_{z2}/f_{z1} = 1$, respectively. Measurements

and theoretical predictions are plotted in Figure 14, which match very well, especially near the crossover frequency. Another interesting comparison between PID1 and PID2 is the magnitude of the open-loop gain for the same design point. Bellow the cross-frequency in each case, PID2 reaches a higher magnitude than PID1, which means a lower L index. That is why, in the performance space plotted in Figure 13, PID2 is a better solution than PID1 for the three illustrated design points. This result is also illustrated in the time-domain waveforms appearing in Figure 15. The output voltage has been measured when a voltage reference step is applied. In the left plot, the six different possibilities for design-point 3 are shown. Although the same crossover frequency and phase margin are selected for the compared waveforms, the system exhibits a different time-response due to the zero location, as shown in previous sections. PID2 with $f_{z2}/f_{z1}= 1$ is the fastest response, matching with the choice to plot the performance space in Figure 13. In the right side of Figure 15, the time-response for design-point 1 for a single compensator is shown to illustrate that, despite the high cross-over frequency, no limit cycles are produced after the transitions, as predicted by the theory.

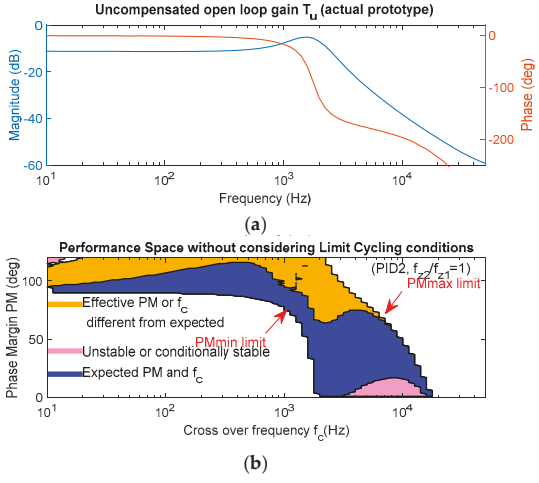


Figure 12. (**a**) The actual prototype's uncompensated open loop gain; (**b**) performance space without considering limit cycling conditions.

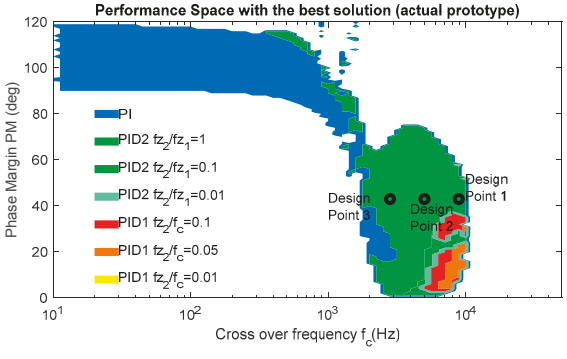


Figure 13. Performance space for the actual prototype with the best solution for each point.

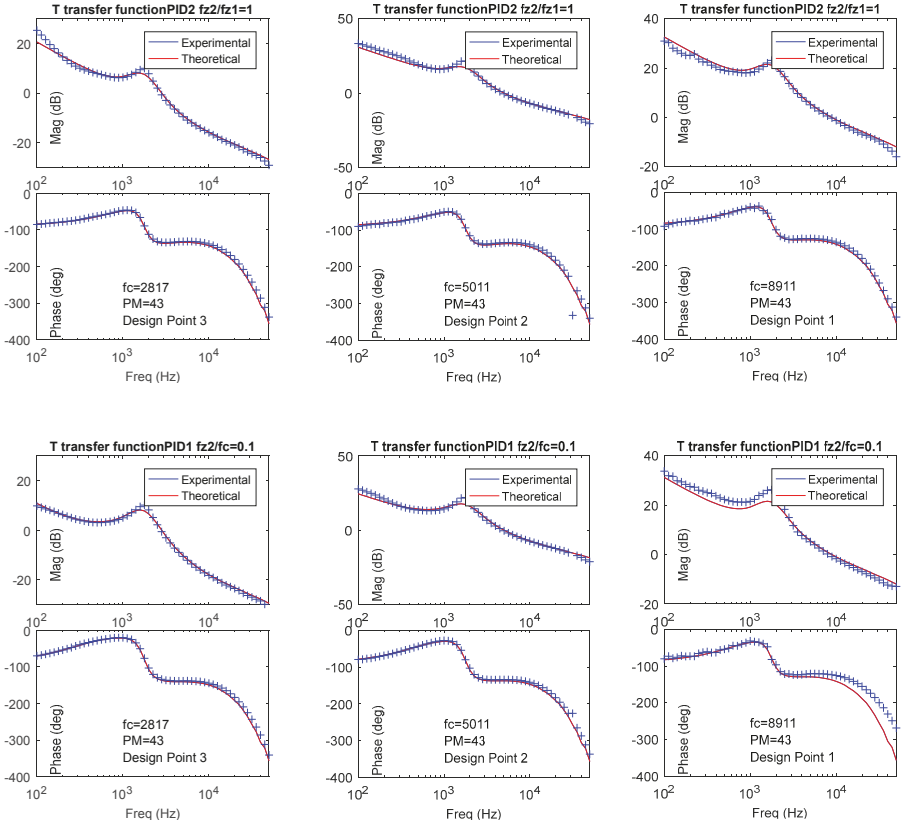
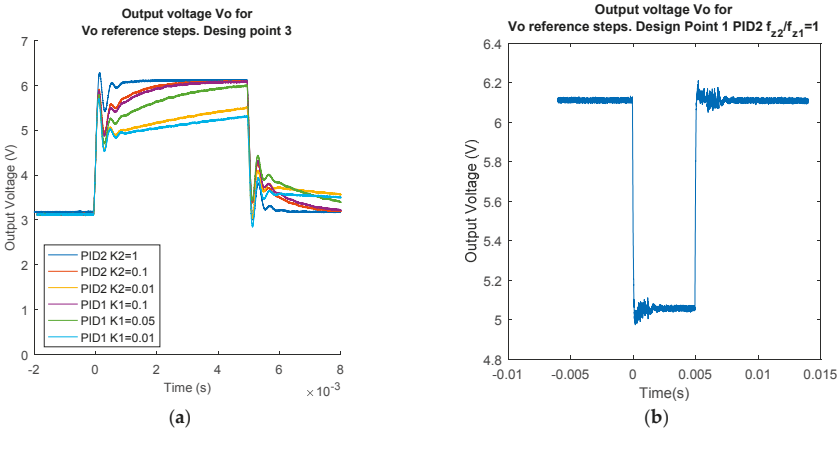


Figure 14. Comparison between the experimental measurements and the theoretical predictions for different PID compensators, considering the three design points in Figure 13.



(**a**) (**b**)

Figure 15. Experimental time-domain waveforms when there is a step in the voltage reference. (**a**) Step response for different designs with f_c = 2817 Hz, PM = 43° (Design point 3); (**b**) step response for design-point 1, using 9 bits in the ADC (note that there is no limit cycling).

5. Conclusions

A frequency-based design approach for the calculation of a digital compensator for DC/DC power-switching converters has been presented. It is based on the analytical calculation of the coefficients of the compensator from the dynamic specifications phase margin, PM, and cross-over frequency, f_c, considering the sampling frequency, delay effects, and limit cycling conditions. The approach is focused on the identification of the dynamic specifications that in fact can be achieved, and its graphical representation on a $(f_c,\ PM)$ axis. Designs that are not feasible, do not fulfill the requirements, are unstable, or do not meet the limit cycling conditions, are excluded from the performance space.

The design procedure has been automatized. A simple algorithm can generate all feasible designs and plot the performance space. It allows for the identification of the dynamic limitations of a given power converter with a given compensator topology. The most important benefit provided by this approach is the ability to perform a quick and straightforward comparison of compensator topologies or sensitivity analysis of a specific parameter, ensuring the feasibility of the proposed designs.

Three compensator topologies have been considered in the calculations: PI and PID, with two different criteria to establish the frequency of the two zeros (PID1 and PID2). The design procedure has been applied in a particular example, considering seven different compensator types and choosing the more suitable design for each point $(f_c,\ PM)$ using a proposed figure of merit calculated from the frequency response.

The described analysis based on the performance space also allows for determination of the simplest compensator design in terms of the dynamic performance, the complexity of the implementation, and the computational resources. In the analyzed example, PI is the best option for low-frequency dynamic requirements. In general, the option covering a larger area in the performance space is PID with two zeros at the same frequency. However, this performance space can be limited by the integral limit cycling condition. Other PID designs with separated zeros can overcome this limitation, but the time response should be assessed. The experimental results of a lab prototype agree with the theoretical predictions.

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Conflicts of Interest: The authors declare no conflict of interest.

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Disturbance Rejection Control Method for Isolated Three-Port Converter with Virtual Damping

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Abstract: The high-power density and capability of three-port converters (TPCs) in generating demanded power synchronously using flexible control strategy make them potential candidates for renewable energy applications to enhance efficiency and power density. The control performance of isolated TPCs can be degraded due to the coupling and interaction of power transmission among different ports, variations of model parameters caused by the changes of the operation point and resonant peak of LC circuit. To address these issues, a linear active disturbance rejection control (LADRC) system is developed in this paper for controlling the utilized TPC. A virtual damping based method is proposed to increase damping ratio of current control subsystem of TPC which is beneficial in further improving dynamic control performance. The simulation and experimental results show that compared to the traditional frequency control strategy, the control performance of isolated TPC can be improved by using the proposed method.

Keywords: three-port converter; linear active disturbance rejection control; virtual damping; linear extended state observer

1. Introduction

The demand for three-port converters (TPCs) in renewable energy generation systems is increasing due to the compact structure of these converters and their ability to handle demanded power synchronously [1–5]. The TPCs not only facilitate multifunctional and multidirectional regulation for electrical power transmission but also provide flexibility in power control and power density enhancement in power conversion systems [6–10].

In an isolated three-port converter, the three windings of an isolated transformer share the same magnetic core, therefore there are unavoidable couplings of power transmission among the three ports of TPC. Decoupling control methods with proper decoupling factors are usually employed in three-port converters to achieve two single-input single-output (SISO) subsystems [11–14]. A classical frequency control theory is usually utilized to design controllers for each port respectively. Since the small signal models employed to design the controllers are produced by linearization of the nonlinear model of TPC at a steady-state operating point, the decoupling and dynamic performances of TPC control system can be degraded significantly by the variation of the operating point. Particularly, since the small signal models of TPC depend on a specific operating point, in a transient state process, a heavy change of the operating point parameters may affect decoupling of different ports and dynamic performance of the control system. Generally, the three-port converter is a multiple-input

multiple-output (MIMO) system, several phase-shifting angles and equivalent duty cycles can be used as control signals, and several voltages and currents of different ports can be assigned as the output signals. A linear quadratic regulator (LQR) based method is applied in ref. [15] to develop a multivariable controller for a three-port converter. Though the LQR method seems capable of achieving performance balance of different ports, it has relatively high sensitivity to the accuracy of system parameters. The parameters of the control models will vary with the change in operating point as these small signal based models used in the control system design are derived at a specific steady state operating point. Also, the design of the parameters of the time domain based LQR method is relatively complex compared to the frequency domain design method.

The LADRC method was first proposed by Zhiqiang Gao, and it has advantages of tolerating changes in model parameters and possesses an inherent decoupling ability that is useful for control system design [16]. In the LADRC method, the influences of model parameter deviations and external interferences can all be regarded as a generalized disturbance [17]. Therefore, the linear extended state observer (LESO) [18,19] can be used to estimate the state variables and generalized disturbance, and the observed signals are used to synthesize control signal in the control system. Compared to conventional PI controller, the LADRC method is shown to enhance the dynamic performance of the control system in [20].

In order to improve the dynamic control performance of an isolated three-port converter in this study, the LADRC method is employed to decrease negative impact of reactions among different ports, and obtain high control performance under load change conditions.

The rest of the paper is organized as follows. In Section 2, the topology, modulation method, power delivery relationship, and control-oriented small signal models are presented. The design of a LADRC based control system for a three-port converter by utilizing its current and voltage control small signal models, and the proposed virtual damping method to suppress the resonant peak in the current control subsystem are given in Section 3. Also, in this section, the principle and the design procedure of decoupling control are briefly illustrated for comparison purposes. The simulation and experiment results are presented in Section 4. Finally, the conclusion is provided in Section 5.

2. Topology and Modeling of TPC

The circuit topology of an isolated TPC is presented in Figure 1a. In this figure, a DC power supply (e.g., it can be a fuel cell or a photovoltaic cell) is set in Port 1, and the power supply, v_{d1} is connected in series with an inductor L_{d1}, and r_e represents the equivalent series resistance (ESR) of L_{d1}. There is 180° phase shift between leg A and leg B, and the duty cycles of all switches in Port 1 are set to be 50% and the drive signals of the switches on the same leg are complementary. The Port 2 and Port 3 are connected with load and energy storage (ES) respectively and their switching patterns are as same as the switching mode of Port 1. A simplified equivalent Δ-connected circuit of the TPC by transferring the related parameters of Port 2 and Port 3 to Port 1 is given in Figure 1b. If the voltage between the middle points of leg A and leg B, v_1 is defined as a reference, the phase shifts of v_2 and v_3 relative to v_1 are denoted as φ_{12} and φ_{13} respectively, and they are shown in Figure 1c. Moreover, L_1, L_2, and L_3 are equivalent series inductances (including winding leakage inductance and additional inductance) of the three transformer windings. The expressions of L_{12}, L_{13}, and L_{23} of the Δ-connected circuit shown in Figure 1b are defined by (1).

$$\begin{cases} L_{12} = L_1 + L_2' + L_1 L_2'/L_3' \\ L_{23} = L_2' + L_3' + L_2' L_3'/L_1 \\ L_{13} = L_3' + L_1 + L_1 L_3'/L_2' \end{cases} \tag{1}$$

L_2' and L_3' are expressed by (2).

$$L_2' = \frac{N_1^2 L_2}{N_2^2}, L_3' = \frac{N_1^2 L_3}{N_3^2} \tag{2}$$

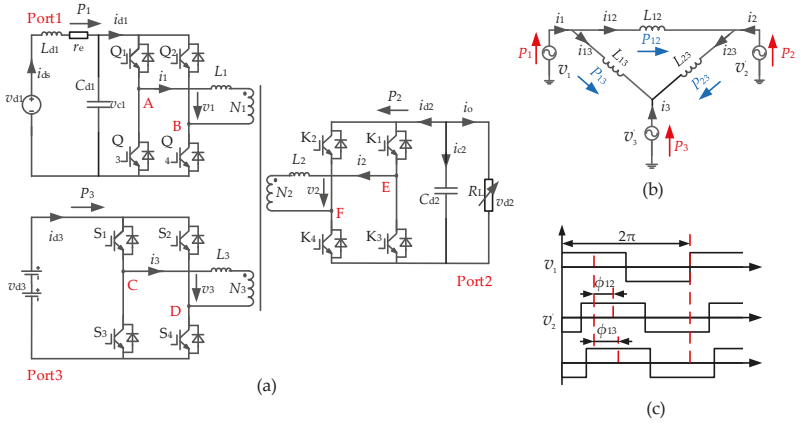

Figure 1. The isolated three-port converter: (**a**) topology; (**b**) equivalent Δ-connected circuit; (**c**) modulation scheme.

In each switching cycle, the total power transmitted between any two ports is approximated to its fundamental component. Therefore, the Fourier expansion based fundamental component analysis method is employed for theoretical analysis in this study. By utilizing the equivalent Δ-connection circuit in Figure 1b, the power equations of each port can be written as in (3).

$$\begin{cases} P_1 = P_{12} + P_{13} \\ P_2 = -P_{12} + P_{23} \\ P_3 = -P_{13} - P_{23} \end{cases}, \ (P_1 + P_2 + P_3 = 0) \tag{3}$$

where

$$\begin{cases} P_{12} = \frac{8N_1}{\pi^2 N_2 \omega_s L_{12}} V_{d1} V_{d2} \sin\varphi_{12} \\ P_{13} = \frac{8N_1}{\pi^2 N_3 \omega_s L_{13}} V_{d1} V_{d3} \sin\varphi_{13} \\ P_{23} = \frac{8N_1^2}{\pi^2 N_2 N_3 \omega_s L_{23}} V_{d2} V_{d3} \sin(\varphi_{13} - \varphi_{12}) \end{cases} \tag{4}$$

In (4), V_{d1}, V_{d2}, and V_{d3} are the rated amplitudes of v_1, v_2, and v_3, N_1, N_2, and N_3 are the transformer winding turns of respective ports, and ω_s is the switching angular frequency. Since the summation of P_1, P_2 and P_3 is kept at zero as shown in (3), that means the power of one port can be determined using the powers of the other two ports. From this point of view, the energy storage port is usually taken as an energy buffer that can be charged or discharged determined by the power delivery and load conditions of Port 1 and Port 2 respectively. According to (3) and (4), the power of Port 1 and Port 2 can be formulated as (5) and (6) respectively.

$$P_1 = \frac{8N_1 V_{d1} V_{d2}}{\pi^2 N_2 \omega_s L_{12}} \sin\varphi_{12} + P_1 = \frac{8N_1 V_{d1} V_{d3}}{\pi^2 N_3 \omega_s L_{13}} \sin\varphi_{13} \tag{5}$$

$$P_2 = -\frac{8N_1 V_{d1} V_{d2} \sin\varphi_{12}}{\pi^2 N_2 \omega_s L_{12}} + \frac{8N_1 V_{d2} V_{d3} \sin(\varphi_{13} - \varphi_{12})}{\pi^2 N_2 N_3 \omega_s L_{23}} \tag{6}$$

Therefore, the corresponding average currents in each switching cycle can be derived as (7) and (8) respectively.

$$\bar{i}_{d1} = \frac{P_1}{V_{d1}} = P_1 = \frac{8N_1 V_{d2}}{\pi^2 N_2 \omega_s L_{12}} \sin\varphi_{12} + \frac{8N_1 V_{d3}}{\pi^2 N_3 \omega_s L_{13}} \sin\varphi_{13} \tag{7}$$

$$\bar{i}_{d2} = \frac{P_2}{V_{d2}} = -\frac{8N_1 V_{d1} \sin\varphi_{12}}{\pi^2 N_2 \omega_s L_{12}} + \frac{8N_1^2 V_{d3} \sin(\varphi_{13} - \varphi_{12})}{\pi^2 N_2 N_3 \omega_s L_{23}} \tag{8}$$

By applying partial differential operation in (7) and (8) respectively, (9) can be obtained for a steady-state operating point A (φ_{120}, φ_{130}).

$$\begin{cases} G_{11} = \left.\frac{\partial \bar{i}_{d2}}{\partial \varphi_{12}}\right|_A = -\frac{8N_1V_{d1}\cos\varphi_{120}}{\pi^2N_2N_3\omega_sL_{12}} - \frac{8N_1^2V_{d3}\cos(\varphi_{130}-\varphi_{120})}{\pi^2N_2N_3\omega_sL_{23}} \\ G_{12} = \left.\frac{\partial \bar{i}_{d2}}{\partial \varphi_{13}}\right|_A = \frac{8N_1^2V_{d3}}{\pi^2N_2N_3\omega_sL_{23}}\cos(\varphi_{130}-\varphi_{120}) \\ G_{21} = \left.\frac{\partial \bar{i}_{d1}}{\partial \varphi_{12}}\right|_A = \frac{8N_1V_{d2}}{\pi^2N_2\omega_sL_{12}}\cos\varphi_{120} \\ G_{22} = \left.\frac{\partial \bar{i}_{d1}}{\partial \varphi_{13}}\right|_A = \frac{8N_1V_{d3}}{\pi^2N_3\omega_sL_{13}}\cos\varphi_{130} \end{cases} \tag{9}$$

Consequently, (9) can be simplified as (10).

$$\begin{bmatrix} \widetilde{i}_{d2} \\ \widetilde{i}_{d1} \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} \widetilde{\varphi}_{12} \\ \widetilde{\varphi}_{13} \end{bmatrix} = \boldsymbol{G_A} \begin{bmatrix}]\widetilde{\varphi}_{12} \\ \widetilde{\varphi}_{13} \end{bmatrix} \tag{10}$$

As shown in (9), besides the circuit parameters, the value of any matrix element in $\boldsymbol{G_A}$, G_{xy} (x = 1, 2 and y = 1, 2) is determined by the steady-state parameters (φ_{120} and φ_{130}). And it can be also seen from (10) that there are couplings between $\widetilde{i}_{d1}$ and $\widetilde{i}_{d2}$ caused by G_{21} and G_{12}.

The small signal linearization model of the three-port converter can be derived as in (11) by applying KCL and KVL laws in Figure 1.

$$\begin{cases} C_{d2}\frac{d\widetilde{v}_{d2}}{dt} = -\frac{\widetilde{v}_{d2}}{R_L} - G_{11}\widetilde{\varphi}_{12} - G_{12}\widetilde{\varphi}_{13} \\ L_{d1}\frac{d\widetilde{i}_{ds}}{dt} = \widetilde{v}_{d1} - \widetilde{v}_{c1} - r_e\widetilde{i}_{ds} \\ C_{d1}\frac{d\widetilde{v}_{c1}}{dt} = \widetilde{i}_{ds} - G_{21}\widetilde{\varphi}_{12} - G_{22}\widetilde{\varphi}_{13} \end{cases} \tag{11}$$

3. Control Strategy for TPC

3.1. Decoupling Control for TPC

Assuming the matrix, $\boldsymbol{G_A}$ given in (10) can be simplified to a diagonal matrix given in (12) by introducing a decoupling matrix $\boldsymbol{H}$ defined in (13).

$$\begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} = \begin{bmatrix} G_{11} & 0 \\ 0 & G_{22} \end{bmatrix} \tag{12}$$

$$\boldsymbol{H} = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} = \begin{bmatrix} \frac{G_{11}G_{22}}{G_{11}G_{22}-G_{12}G_{21}} & \frac{-G_{12}G_{22}}{G_{11}G_{22}-G_{12}G_{21}} \\ \frac{-G_{11}G_{21}}{G_{11}G_{22}-G_{12}G_{21}} & \frac{G_{11}G_{22}}{G_{11}G_{22}-G_{12}G_{21}} \end{bmatrix} \tag{13}$$

The decoupling control block diagram is presented in Figure 2. In this figure, G_v and G_c represent the voltage controller and current controller respectively, which can be synthesized by using Bode plot based design method in frequency domain. In Figure 2, the open loop transfer functions of the voltage and current control subsystems are $G_{vo} = G_{11}G_1$ and $G_{co} = G_{22}G_2$ respectively, the transfer functions of G_1 and G_2 are given in (14). The resonant angular frequency of G_2 is $\omega_n = 1/\sqrt{L_{d1}C_{d1}}$.

$$\begin{cases} G_1(s) = \frac{R_L}{R_LC_{d2}s+1} \\ G_2(s) = \frac{1}{L_{d1}C_{d1}s^2+r_eC_{d1}s+1} \end{cases} \tag{14}$$

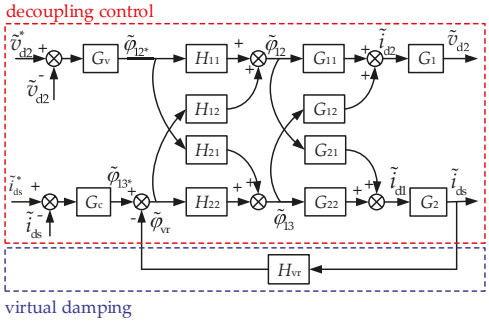

Figure 2. Decoupling control scheme of a three-port converter.

3.2. Virtual Damping Method

For Port 1 in Figure 1, L_{d1} and C_{d1} are utilized to constitute an LC filter to limit the amplitude of the double-switching frequency component of i_{ds} and reduce the negative impact of high-frequency ripple current on the power source (e.g., a fuel cell). However, this might cause performance degradation or an instability issue in current control subsystem due to the high resonant peak and a very weak damping ratio introduced by a pure LC circuit ($r_e = 0$) or with a very small value of r_e shown in (14). Though the resonant phenomenon can be addressed by decreasing the current control bandwidth, the dynamic performance cannot be guaranteed.

The block diagram of the current control subsystem, $G_{co} = G_{22}G_2$ is presented in Figure 3 according to (11). The transfer function, H_{vr} in Figure 2 is a compensation function that is proposed to implement virtual damping in this paper. The expression of H_{vr} is shown in Figure 3. In this figure, r_v is the desired virtual resistor. If the output of H_{vr}, which is $\tilde{\varphi}_{vr}$, is moved from the point A to the point B, then, H_{vr} in Figure 3 is changed to $r_v/(s/\omega_p + 1)$, and it makes H_{vr} a rational fraction. ω_p is used to attenuate the high frequency noise, and if the value of ω_p is high enough, then, $r_v/(s/\omega_p + 1) \approx r_v$ becomes a resistor connected in series with r_e, and the damping ratio of G_2 becomes $(r_s + r_v)/2 \times \sqrt{C_{d1}/L_{d1}}$ with the introduction of r_v as a virtual resistor. In practical applications, the sampled i_{ds} is passed through H_{vr}, and then added to the output of the current controller to obtain the final phase shift between Port 1 and Port 3, and the value of ω_p can be selected between ω_s and $\omega_s/2$.

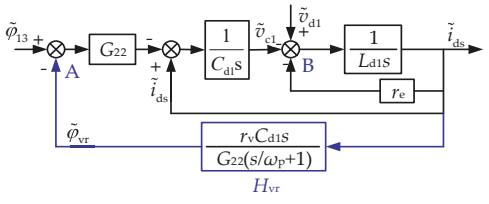

Figure 3. Schematic diagram of virtual damping implementation.

3.3. LADRC for TPC

The small signal model shown in (11) can be transformed into two subsystems to implement the LADRC based control method. The two differential equations for current control subsystem and voltage control subsystem are given by (15) and (16) respectively.

$$\ddot{\tilde{i}}_{ds} = -\frac{1}{C_{d1}L_{d1}}\tilde{i}_{ds} - \frac{r_e}{L_{d1}}\dot{\tilde{i}}_{ds} + \frac{G_{22}}{C_{d1}L_{d1}}\tilde{\varphi}_{12} + \frac{1}{L_{d1}}\dot{\tilde{v}}_{d1} + \left(\frac{G_{21}}{C_{d1}L_{d1}} - b_c\right)\tilde{\varphi}_{13} + b_c\tilde{\varphi}_{13} = f_c + b_c\tilde{\varphi}_{13} \quad (15)$$

$$\dot{\tilde{v}}_{d2} = -\frac{1}{R_L C_{d2}}\tilde{v}_{d2} - \frac{G_{12}}{C_{d2}}\tilde{\varphi}_{13} + \left(-\frac{G_{11}}{C_{d2}} - b_v\right)\tilde{\varphi}_{12} + b_v\tilde{\varphi}_{12} = f_v + b_v\tilde{\varphi}_{12} \quad (16)$$

In (15) and (16), $\widetilde{v}_{d2}$ and $\widetilde{i}_{ds}$ are taken as the output variables of the two subsystems, $\widetilde{\varphi}_{13}$ and $\widetilde{\varphi}_{12}$ are the control signals of the current control subsystem and the voltage control subsystem respectively.

$\widetilde{\varphi}_{13}$ is considered as an external disturbance of voltage control subsystem, while $\widetilde{\varphi}_{12}$ is considered as an external disturbance of the current control subsystem. Furthermore, f_c and f_v are used to represent the generalized disturbances that are associated with both inner and outer variable elements of the two subsystems (e.g., coupling, load, and operating point related parameter changes, etc.). In practical situations, the generalized disturbances, f_c and f_v are usually unknown and cannot be directly measured. Therefore, LESO is adopted to evaluate the generalized disturbances and relevant state variables in the LADRC method.

As for the current control subsystem, $\boldsymbol{x}_c = \left[\widetilde{i}_{ds} \;\; \dot{\widetilde{i}}_{ds} \;\; f_c\right]^T$ is selected as the state vector, the augmented state space model is formulated by (17)

$$\begin{cases} \dot{\boldsymbol{x}}_c = \boldsymbol{A}_c\boldsymbol{x}_c + \boldsymbol{B}_c\widetilde{\varphi}_{13} + \boldsymbol{E}_c\dot{f}_c \\ \widetilde{i}_{ds} = \boldsymbol{C}_c\boldsymbol{x}_c \end{cases} \tag{17}$$

where

$$\begin{cases} \boldsymbol{A}_c = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 0 \end{bmatrix} \\ \boldsymbol{B}_c^T = \begin{bmatrix} 0 & b_c & 0 \end{bmatrix} \\ \boldsymbol{E}_c^T = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \\ \boldsymbol{C}_c = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix} \end{cases} \tag{18}$$

The LESO of current control subsystem is constructed by (19).

$$\begin{cases} \dot{\boldsymbol{z}}_c = [\boldsymbol{A}_c - \boldsymbol{L}_c\boldsymbol{C}_c]\boldsymbol{z}_c + [\;\boldsymbol{B}_c \quad \boldsymbol{L}_{c}]w_c \\ \boldsymbol{y}_c = \boldsymbol{z}_c \end{cases} \tag{19}$$

where $\boldsymbol{y}_c = \boldsymbol{z}_c = \begin{bmatrix} z_{c1} & z_{c2} & z_{c3} \end{bmatrix}^T$ is the observed vector of $\boldsymbol{x}_c$. $w_c = \begin{bmatrix} \widetilde{\varphi}_{13} & \widetilde{i}_{ds} \end{bmatrix}^T$ and $\boldsymbol{L}_c$ given in (20) is the observer gain that can be designed using the pole placement method [17].

$$\boldsymbol{L}_c = \begin{bmatrix} 3\omega_{oc} & 3\omega_{oc}^2 & \omega_{oc}^3 \end{bmatrix}^T \tag{20}$$

where ω_{oc} is the equivalent bandwidth of the observer.

It should be noted that the disturbance caused by the resonance of $L_{d1}C_{d1}$ circuit is included in the generalized disturbance, f_c, therefore, the value of ω_{oc} should be at least twice as large as ω_n, that means $\omega_{oc}/\omega_n \geq 2$ should be satisfied to make the LESO obtain accurate value of f_c, otherwise, the control performance might be significantly degraded.

Similarly, the LESO used for voltage control subsystem is presented in (21).

$$\begin{cases} \dot{\boldsymbol{z}}_v = [\boldsymbol{A}_v - \boldsymbol{L}_v\boldsymbol{C}_v]z_v + [\;\boldsymbol{B}_v \quad L_{v}]w_v \\ \boldsymbol{y}_v = \boldsymbol{z}_v \end{cases} \tag{21}$$

In (21), $\boldsymbol{w}_v = \begin{bmatrix} \widetilde{\varphi}_{12} & \widetilde{\mathrm{v}}_{\mathrm{d2}} \end{bmatrix}$. $\boldsymbol{y}_{\mathrm{v}} = \boldsymbol{z}_{\mathrm{v}} = \begin{bmatrix} z_{\mathrm{v1}} & z_{\mathrm{v2}} \end{bmatrix}^{\mathrm{T}}$ is the output vector of (21) that corresponds to $\boldsymbol{x}_v = \begin{bmatrix} \widetilde{v}_{\mathrm{d2}} & f_{\mathrm{v}} \end{bmatrix}^{\mathrm{T}}$. And the coefficient matrix in (21) are given in (22).

$$\begin{cases} \boldsymbol{A}_{\mathrm{v}} = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \\ \boldsymbol{B}_{\mathrm{v}}^{T} = \begin{bmatrix} b_{\mathrm{v}} & 0 \end{bmatrix} \\ \boldsymbol{E}_{\mathrm{v}}^{T} = \begin{bmatrix} 0 & 1 \end{bmatrix} \\ \boldsymbol{C}_{\mathrm{v}} = \begin{bmatrix} 1 & 0 \end{bmatrix} \end{cases} \tag{22}$$

The corresponding gain vector of the voltage LESO, $\boldsymbol{L}_{\mathrm{v}}$ is shown in (23).

$$\boldsymbol{L}_{\mathrm{v}} = \begin{bmatrix} 2\omega_{\mathrm{ov}} & {\omega_{\mathrm{ov}}}^2 \end{bmatrix}^{\mathrm{T}} \tag{23}$$

Assuming f_{c} and f_{v} can be observed accurately ($z_{\mathrm{c3}} = f_{\mathrm{c}}$, $z_{\mathrm{v2}} = f_{\mathrm{v}}$), and if $\widetilde{\varphi}_{13}$ and $\widetilde{\varphi}_{12}$ in (15) and (16) can be expressed as (24).

$$\begin{cases} \widetilde{\varphi}_{13} = \frac{(u_{\mathrm{c}} - z_{\mathrm{c3}})}{b_{\mathrm{c}}} = \frac{(u_{\mathrm{c}} - f_{\mathrm{c}})}{b_{\mathrm{c}}} \\ \widetilde{\varphi}_{12} = \frac{(u_{\mathrm{v}} - z_{\mathrm{v2}})}{b_{\mathrm{v}}} = \frac{(u_{\mathrm{v}} - f_{\mathrm{v}})}{b_{\mathrm{v}}} \end{cases} \tag{24}$$

The current and voltage control subsystems will be simplified to two simple cascaded integrators systems shown in (25).

$$\begin{cases} \dddot{\widetilde{i}}_{\mathrm{ds}} = u_{\mathrm{c}} \\ \dot{\widetilde{v}}_{\mathrm{d2}} = u_{\mathrm{v}} \end{cases} \tag{25}$$

The current and voltage control signals, u_{c} and u_{v}, for this cascaded integrator system can be proposed as (26).

$$\begin{cases} u_{\mathrm{c}} = k_{\mathrm{pc}}(u_{\mathrm{rc}} - z_{\mathrm{c1}}) - k_{\mathrm{dc}} z_{\mathrm{c2}} \\ u_{\mathrm{v}} = k_{\mathrm{pv}}(u_{\mathrm{rv}} - z_{\mathrm{v1}}) \end{cases} \tag{26}$$

where k_{pc}, k_{pv}, and k_{dc} are controller parameters, and u_{rc} and u_{rv} are current and voltage reference signals, respectively. In (26), it can be seen that u_{c} and u_{v} represent equivalent PD (proportional-derivative) and P (proportional) controllers respectively. The closed-loop transfer functions of the current and voltage control subsystem can be formulated as (27) and (28) which are obtained by substituting the two equations in (26) into the two equations of (25) respectively.

$$G_{\mathrm{cL}} = \frac{k_{\mathrm{pc}}}{s^2 + k_{\mathrm{dc}} s + k_{\mathrm{pc}}},\ (k_{\mathrm{pc}} = \omega_{\mathrm{c}}^2,\ k_{\mathrm{dc}} = 2\xi\omega_{\mathrm{c}}) \tag{27}$$

$$G_{\mathrm{vL}} = \frac{k_{\mathrm{pv}}}{\mathrm{s} + k_{\mathrm{pv}}},\ (k_{\mathrm{pv}} = \omega_{\mathrm{v}}) \tag{28}$$

In (27) and (28), ω_{c} and ω_{v} represent equivalent control bandwidths of the two closed-loop control subsystems with LADRC method, and ξ is the equivalent damping of the current control subsystem, which should be designed to guarantee smooth current change in transient state process (there is no intense oscillations in dynamic process). It can be seen from (27) and (28) that steady state errors are eliminated in the current and voltage closed-loop control systems (when $s = 0$, unity gain is obtained in (27) and (28) respectively) by utilizing (26) as control law. Furthermore, the closed-loop control performances of the two subsystems are completely determined by the designed controller parameters (k_{pc}, k_{pd} and k_{pv}) regardless of the changes of model parameters. This is a prominent characteristic of the LADRC method. (ω_{c}, ω_{oc}) and (ω_{v}, ω_{ov}) are the adjustable LADRC parameters in current and

voltage control subsystems, respectively. Since LADRC method is observer based, the bandwidth of the observer should be kept sufficiently larger than the bandwidth of the control system to realize effective compensation. Therefore, the two ratios, $\alpha_c = \omega_{oc}/\omega_c$ and $\alpha_v = \omega_{ov}/\omega_v$ should be larger than two at least in practical applications to get accurate observed values [21], otherwise, the control performance might not be guaranteed.

4. Simulation and Experimental Results

4.1. Simulation Results

In order to verify the theoretical analysis and design results of the proposed method, a simulation model of the isolated TPC is developed by using MATLAB/Simulink, and the main parameters of the simulation model are listed in Table 1.

Table 1. Parameters of The Simulation Model.

Symbol	Name	Value
v_{d1}	DC input voltage	24 V
v_{d2}	Output voltage	36 V
v_{d3}	Battery voltage	24 V
L_{d1}	Input filter inductor	100 μH
r_e	Input filter inductor ESR	0.1 Ω
C_{d1}	Input filter capacitor	1200 μF
C_{d2}	Output filter capacitor	1000 μF
R_L	Load resistor	45 Ω/22 Ω
f_s	Switching frequency	20 kHz

The steady-state operating point A (0.620, 0.379) is selected which corresponds to R_L = 45 Ω, v_{d2} = 36 V and i_{ds} = 1.3 A, and an extra 0.2 Ω virtual resistor is introduced. The open loop transfer functions of the two subsystems are obtained by substituting the parameters listed in Table 1 into G_{co} and G_{vo}, respectively. The controllers G_c and G_v, given by (29), are designed for the decoupled current and voltage subsystems respectively by using the frequency domain design method.

$$\begin{cases} G_c = \frac{500}{1\times10^{-4}s^2+s} \\ G_v = \frac{0.2813s+6.25}{1\times10^{-8}s^3+2\times10^{-4}s^2+s} \end{cases} \tag{29}$$

The Bode plots of the two subsystems with and without correction are shown in Figures 4a and 4b, respectively.

As can be seen in Figure 4a, the crossover frequency of the corrected current control subsystem with r_v = 0.2 (the curve B) is about 71 Hz, the phase margin is about 81°, and the gain margin is about 7 dB. The crossover frequency of the corrected voltage control subsystem is about 75 Hz, the phase margin is about 85°, and the gain margin is about 33 dB. As a comparison, if r_v = 0.2 is cancelled, the corrected current control subsystem (the curve C) will be unstable, since the resonant peak (the corresponding angular frequency is ω_n = 2887 rad/s) of the curve C will intersect with 0 dB axis under this condition.

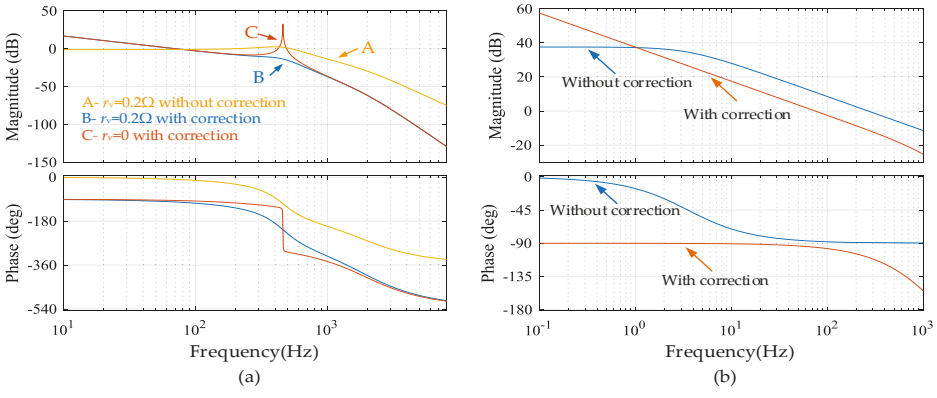

Figure 4. The bode plots of subsystems by using traditional frequency control method: (**a**) i_{ds} subsystem; (**b**) v_{d2} subsystem.

For the control systems with LADRC method, the equivalent control bandwidths of the current and voltage subsystems are the same, $\omega_c = \omega_v = 450$ rad/s (about 72 Hz) which are close to the designed crossover frequencies using the traditional frequency domain method. The observer bandwidths of the current and voltage subsystems are $\omega_{oc} = 4147$ rad/s (about 660 Hz), and $\omega_{ov} = 2000$ rad/s (about 318 Hz) respectively. The simulation results are shown in Figure 5.

Figure 5a shows simulation results of v_{d2} and i_{ds} with traditional frequency control under a step load change condition. As can be seen in Figure 5a, there is an obvious voltage drop (from 36 V to 35.2 V) at 0.5 s when the load is suddenly changed from 29 W to 52 W that resulted in transient fluctuations in i_{ds} (changed from 1.3 A to 1.25 A). When the load is suddenly reduced at 0.7s from 52 W to 29 W, current i_{ds} transiently increases from 1.3 A to 1.37 A, while v_{d2} increases to about 36.8 V, and then decreases gradually to its rated value after 100 ms.

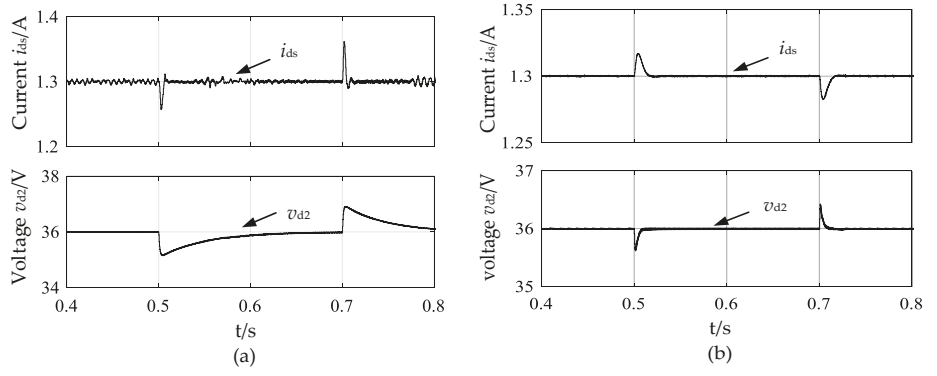

Figure 5. The simulation results of the system: (**a**) with traditional frequency control method; (**b**) with the LADRC method.

The simulation results of the system with the LADRC method and r_v = 0.2 Ω are shown in Figure 5b. In this figure, it can be seen that for the same load change, v_{d2} drops from 36 V to 35.6 V at 0.5 s when the load increased, and it increases from 36 V to 36.4 V at 0.7 s when the load decreases. However, current is changed slightly with respect to the load change. For instance, the current drops from 1.3 A to 1.28 A when the load reduced and it increases from 1.3 A to 1.32 A when the load is increased. By comparing the result shown in Figure 5, it can be seen that the amplitude of i_{ds}

fluctuation in the system controlled with LADRC is lower than that of the system controlled with the traditional frequency control method. Also, the transient recovery time of v_{d2} is much shorter than that of the system with the traditional frequency control. These results imply that the information of the load change observed by LESO is effectively utilized in the control system.

4.2. Experimental Validation and Analysis

In order to further verify the effectiveness of the proposed method, an experimental platform was developed as shown in Figure 6. The circuit parameters and load change conditions of the experimental system are similar to the simulation model. The experimental results are shown in Figures 7–11.

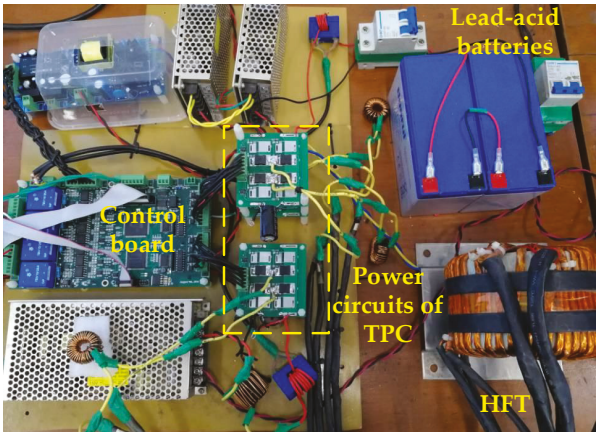

Figure 6. Hardware experiment circuit of the three-port converter.

Figure 7 shows the experimental results, i_{ds}, v_{d2}, Δv_{d2} (fluctuation of v_{d2}) and i_o achieved for the developed converter controlled with the traditional frequency control method. The results of i_{ds} and Δv_{d2} (v_{d2} was controlled to 36 V) for a sudden load increase are shown in Figure 7a. As shown in this figure, there is about 0.24 A drop in i_{ds} and 0.8 V drop in v_{d2} when the load is suddenly changed from 29 W to 52 W. Figure 7b shows the current and voltage changes with respect to sudden load drop where the current and voltage are increased by about 0.24 A and 0.9 V respectively.

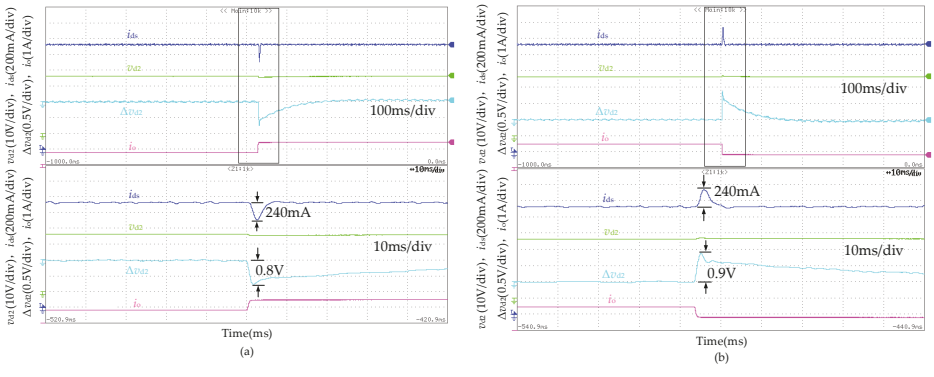

Figure 7. The experiment results of i_{ds}, v_{d2}, Δv_{d2} and i_o with the traditional frequency control method and r_v = 0.2 Ω: (**a**) sudden load increase; (**b**) sudden load decrease.

The effect of the proposed virtual resistor method on i_{ds} control is conducted by removing and re-adding the virtual resistor with the same current controller used in Figure 7. The experimental results are shown in Figure 8a, it can be seen that there are serious oscillations in i_{ds} (the current control subsystem is unstable in this case as indicated by the curve C in Figure 4 and voltage ripples (Δv_{d2}) of v_{d2} are also increased with the same oscillation frequency of i_{ds}. While the virtual resistor scheme is re-performed, the oscillation of i_{ds} can be suppressed soon, and the amplitude of voltage ripple in v_{d2} becomes lower.

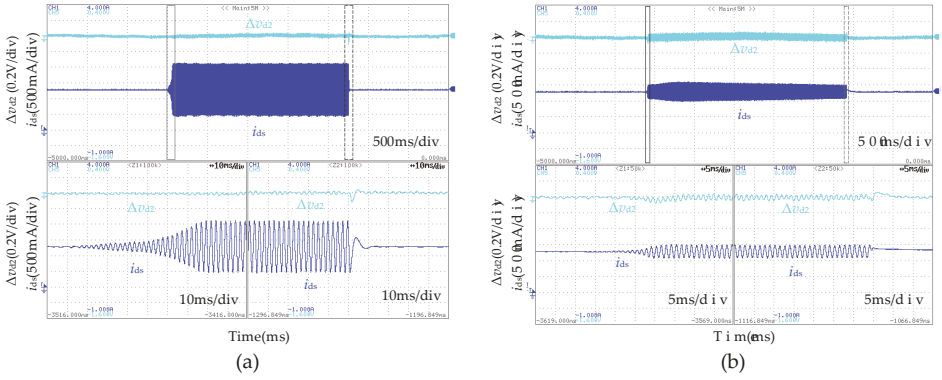

Figure 8. The experimental results with and without r_v = 0.2 Ω virtual resistor (ω_n = 2887 rad/s): (**a**) traditional frequency control; (**b**) LADRC.

The experimental results of i_{ds}, v_{d2}, Δv_{d2} and i_o with the LADRC method and r_v = 0.2 Ω are shown in Figure 9. As shown in Figure 9a, when the same load increment (23 W) is experienced small changes are observed in i_{ds} (changes from 1.3 A to 1.35 A) and v_{d2} (changes from 36 V to 35.6 V) because of the coupling between current and voltage subsystems. As shown in Figure 9b, for a sudden load reduction, i_{ds} is changed from 1.3 A to 1.25 A, and v_{d2} is increased for about 0.5 V. Also, as illustrated in Figure 9, the fluctuations of i_{ds} and v_{d2} in the transient process with the LADRC method are lower than those with the traditional frequency control method as shown in Figure 7, and the voltage transient recovery time with the LADRC method is much shorter than that with the traditional frequency control. These results indicate that the control system with the LADRC has better decoupling performance and adaptability to the operating point changes compared to the control system with the traditional frequency control.

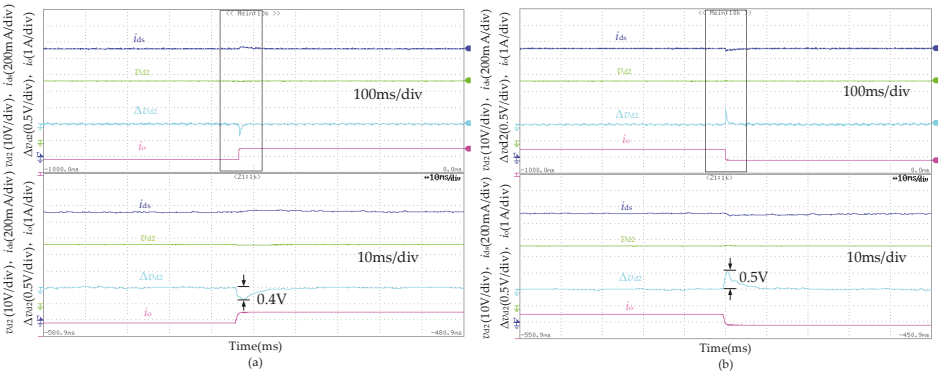

Figure 9. The experimental results of i_{ds}, v_{d2}, Δv_{d2} and i_o with LADRC method, ω_n = 2887 rad/s and r_v = 0.2 Ω: (**a**) sudden load increase; (**b**) sudden load decrease.

The experimental result with and without 0.2 Ω virtual resistor with LADRC method and ω_n = 2887 rad/s is presented in Figure 8b. As shown in this figure, there are obvious current oscillations in i_{ds} when r_v = 0.2 Ω is removed, since the observer bandwidth (ω_{oc} = 4147 rad/s) is not sufficiently higher than the resonant angular frequency of $L_{d1}C_{d1}$ circuit ($\omega_{oc}/\omega_n \approx 1.43 < 2$). And it is similar to the case shown in Figure 8a, the current oscillations can be attenuated effectively if the virtual resistor method is reused.

For comparison study, the resonant angular frequency of $G_2(s)$ in (14) is reduced to ω_n = 1521 rad/s (by setting L_{d1} = 160 μH and C_{d1} = 2700 μF), then there is no oscillations in i_{ds} as shown in Figure 10, that means i_{ds} can be controlled well since the ratio of ω_{oc}/ω_n is about 2.73 which is larger than two in this case, it means that the impact caused by the resonance of $L_{d1}C_{d1}$ circuit can be much accurately observed by the LESO.

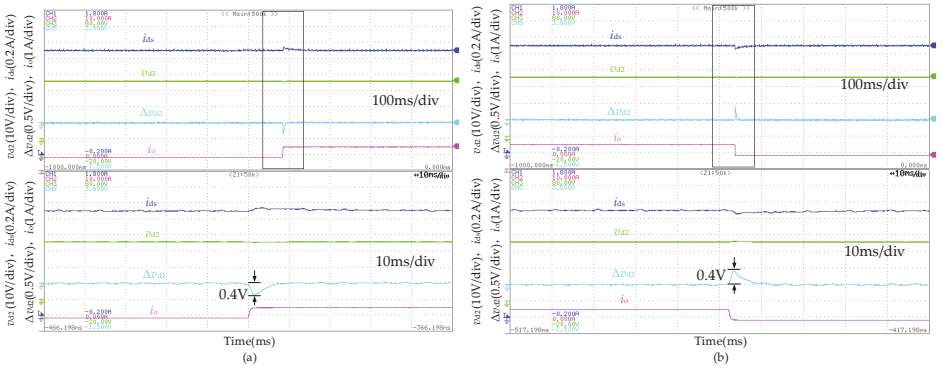

Figure 10. The experimental results of i_{ds}, v_{d2}, Δv_{d2} and i_o with LADRC method, ω_n = 1521 rad/s and r_v = 0 Ω: (**a**) sudden load increase; (**b**) sudden load decrease.

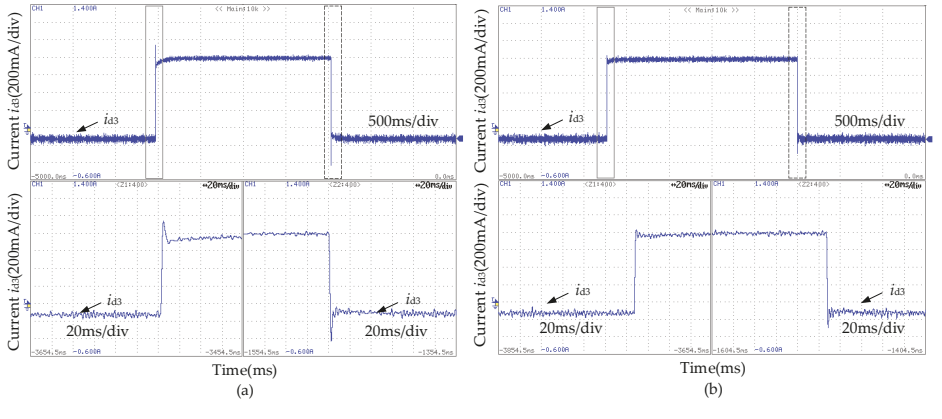

Figure 11. The experimental results of battery current i_{d3}: (**a**) traditional frequency control; (**b**) LADRC.

The battery current i_{d3} for the traditional frequency control and LADRC are shown in Figures 11a and 11b, respectively. In Figure 11, it can be seen that not only the overshoot of i_{d3} with the LADRC is relatively lower, but also the transient recovery time of i_{d3} is shorter than that obtained using the traditional frequency control. This indicates the LADRC method can provide better dynamic balance in the power delivery process. The results shown in Figure 11 have some internal relations with the experimental results presented in Figures 7 and 9. For instance, compared to Figure 11b with LADRC

method applied, the battery overshoot current, i_{d3} shown in Figure 11a is larger when traditional frequency control method is applied. Larger overshoot current causes significant drop in i_{ds} shown in Figure 7a, whereas smaller overshoot of i_{d3} shown in Figure 11b with LADRC resulted in much smaller overshoot in i_{ds} shown in Figure 9a.

5. Conclusions

The model parameter variation caused by the operating point changes and couplings between different ports during power delivery in an isolated three-port converter has a negative impact on the converter control performance. In this study, the LADRC method is employed to control the three-port converter. In the LADRC method, the possible model parameter uncertainties, load changes and the negative impact of LC circuit resonance are all expressed as a generalized disturbance that is considered as a state variable and observed by the LESO which is utilized to synthesize the control signal. In this method, the bandwidth of the LESO is sufficiently higher than the equivalent control bandwidth and the resonant frequency of LC circuit that guarantee the system dynamics and generalized disturbance can be accurately observed. Therefore, the desired closed-loop control performance that is independent of parameters changes and external disturbances can be obtained. And a virtual resistor based method is proposed to increase damping ratio of the current control subsystem of TPC which is beneficial to further improve current control performance using LADRC method. The simulation and experimental results revealed that the proposed method is robust against model parameter changes and external disturbances. Therefore, the dynamic control performance of the three-port converter can be improved significantly.

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Decoupled Current Controller Based on Reduced Order Generalized Integrator for Three-Phase Grid-Connected VSCs in Distributed System

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Abstract: Grid-connected voltage source converters (GC-VSCs) are used for interfacing the distributed power generation system (DPGS) to the utility grid. Performance of the current loop is a critical issue for these GC-VSCs. Recently, reduced order generalized integrator (ROGI)-based current controller is proposed, such that AC reference signal of positive or negative sequences can be separately tracked without steady-state error, which has the advantage of less computational burden. However, the cross-coupling within the ROGI-based current controller would deteriorate the transient response of the current loop. In this paper, a ROGI-based decoupled current controller is proposed to eliminate the coupling between α-axis and β-axis. Thus, the faster dynamic response performance can be achieved while maintaining the merits of ROGI-based current controller. An optimal gain parameter design method for the proposed current controller is presented to improve the stability and dynamic response speed of current loop. Simulation and experiments were performed in MATLAB/Simulink and TMS320C28346 DSP-based laboratory prototype respectively, which validated the proposed theoretical approach.

Keywords: decoupling; reduced order generalized integrator (ROGI); optimal gain; distributed power generation system (DPGS); grid-connected voltage source converters (GC-VSCs)

1. Introduction

In recent years, distributed power generation system (DPGS) has attracted increasing attention with the aggravation of global energy shortage and environmental issues [1–5]. A typical DPGS is shown in Figure 1; due to the intermittence of renewable energy sources (RESs) such as PV systems and wind turbines, energy storage systems (ESSs) based on battery and supercapacitor are used to suppress power fluctuations, which improves the reliability and quality of power supply. Moreover, integrating the electric energy generated by RESs into the power grid is an important way to improve power generation efficiency. As the typical power electronic interfaces between DPGS and power grid, GC-VSCs have been intensively studied [6,7]. In the grid-connected mode, the voltage and frequency at the point of common coupling are dictated by strong power grid, the GC-VSC is controlled to behave as current-controlled converter. Active and reactive power regulation are performed by changing the grid-connected output current [8,9]. Therefore, accurate and fast control of the grid-connected current is one of the most critical technologies, which directly affects the power quality [8–13].

Various research has focused on current control of GC-VSCs [4,6–12,14–25], among which the most widely studied control method is PI controller [17,19,23,26], which effectively guarantees excellent tracking of AC reference signals and fast dynamic response speed, since AC signals become DC signals

through Park transformation and PI controller could produce infinite gain for DC signals [16,17,26]. Nevertheless, d-axis and q-axis current cross-coupling, resulting from the Park transformation, is proportional to the interested control frequency. Actually, the modulation and sampling delay tend to aggravate the coupling and even deteriorate stability of the current loop [17,26]. In addition, resonant controllers are widely used in current loop regulation of GC-VSCs. Proportional-resonant (PR) and vector proportional-integral (VPI) controllers are, respectively, equivalent to conventional PI and complex-vectors PI (cPI) regulators, which are implemented in a positive and negative sequence SRF simultaneously [17]. It assures perfectly tracking AC reference signals without steady-state errors for both sequences [5–7,9,12,14,15,18]. However, the negative-sequence term (i.e., $-j\omega_e$) of conjugated poles introduces two times control frequency fluctuation, bringing slower dynamic response and more severe cross-coupling [16,26]. Moreover, computational burden increases when multiple order harmonics need to be tracked simultaneously [21,22].

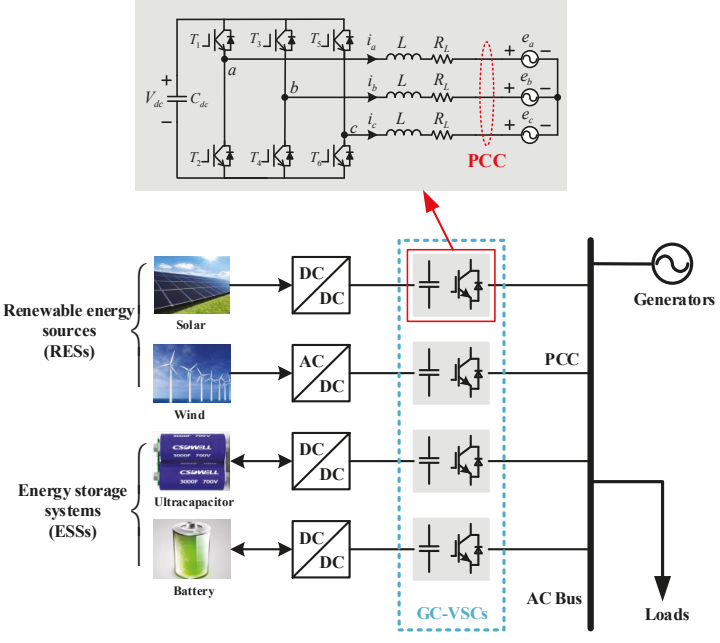


Figure 1. The configuration of a distributed power generation system.

To overcome the disadvantage of the above controllers, some improved methods are proposed. The method of state-feedback decoupling is proposed in [16], which effectively reduces the axes cross-coupling and broadens the bandwidth of current loop. Nevertheless, the decoupling effectiveness could be affected by the time delay and the accuracy of parameter estimation. The alternative decoupling method based on cPI controller is less influenced by these two factors [17]. Thus, a better stability and a faster dynamic response speed of the current loop are achieved. However, the implementation of the aforementioned control algorithms is in SRF and the rotating frame transformation increases the computational burden and complexity. Simultaneously, the error of transformation calculation would emerge if the PLL is not sufficiently accurate [7,9,26]. Overall, a regulator with zero steady-state error in the stationary frame would have some certain advantages in terms of implementation [9–12]. ROGI-based current controller, which is named as PCI controller in [11,12], is proposed with the advantage of less computational burden and improving the bandwidth of harmonics control [21,25]. However, the cross-coupling within the ROGI-based current controller

would deteriorate the transient response of the current loop. In addition, the stability of the current loop will decrease when the control frequency is relatively high [23].

In this paper, a ROGI-based decoupled current controller is proposed, which is capable of suppressing the cross-coupling and improving the dynamic response speed, while possessing the advantage of low computation burden and being convenient to implement. An optimal gain method for parameter tuning is also presented to maximize the stability of the current loop.

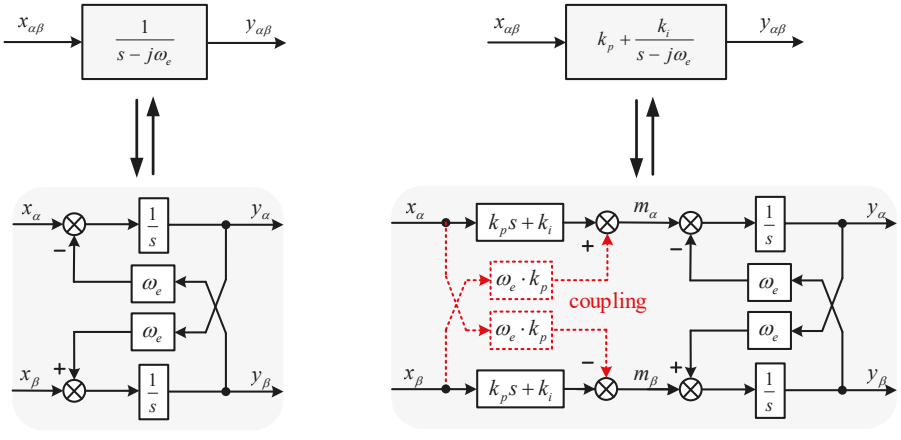
The paper is organized as follows. Coupling of ROGI-based current controller is analyzed in Section 2. Section 3 introduces the proposed ROGI-based decoupled current controller. Specially, the performance of the proposed controller is analyzed through closed-loop frequency response and mathematical derivation, and the optimal parameter design using the root locus is presented. The simulation and experimental results are provided to validate the theoretical approach in Section 4. Finally, Section 5 summarizes the work.

2. Coupling Analysis of ROGI-Based Current Controller

The ROGI is proposed in [21], its transfer function in the s-domain can be expressed as

$$G_{ROGI}(s) = \frac{1}{s \mp j\omega_e} \tag{1}$$

where ω_e is the fundamental frequency and "$-/+$" denotes the positive/negative sequence. The implementation principle of ROGI is shown in Figure 2a.



(**a**) ROGI. (**b**) ROGI-based current controller (PCI).

Figure 2. Implementation principle of ROGI and ROGI-based current controller.

A novel proportional complex integral (PCI) is derived from the principle that zero steady-state error can be achieved if the open-loop gain is infinity at the control frequency [10]. Thus, it can be written by,

$$G_{PCI}(s) = k_p + \frac{k_i}{s - j\omega_e} \tag{2}$$

where k_p is the proportional gain and k_i is the integral gain. It is known from Equation (2) that the PCI controller is equivalent to ROGI-based current controller in [10,21]. For convenience, the PCI controller represents the ROGI-based current controller in this paper. The implementation principle of PCI is shown in Figure 2b, where it can be seen that PCI controller includes two $k_p \cdot \omega_e$ coupling branches,

which will deteriorate the transient response of the current loop. Besides, the coupling aggravates as the control frequency increases.

Figure 3 shows the diagram of PCI-based current closed-loop for GC-VSCs. $G_d^s(s) = e^{-sT_d}$ represents the digital control delay, which consists of one and a half sampling time delay [19], $T_d = 1.5T_s$ (T_s is the sampling cycle). For a more intuitive sense of the coupling, α-axis and β-axis current response with PCI controller is presented in Figure 4 when a step change occurs in reference current. The reference current $i^*_{\alpha\beta}$ decreases from $10 \cdot e^{j\omega_e t}$ to 0 at $t = 0.04s$, where $i^*_\alpha = \mathrm{Re}\{i^*_{\alpha\beta}\} = 10{\cdot}\cos(\omega_e t)$ and $i^*_\beta = \mathrm{Im}\{i^*_{\alpha\beta}\} = 10{\cdot}\sin(\omega_e t)$. In Figure 4a,b, it can be seen that reference current changes in α-axis affects β-axis current, and vice versa. In addition, the coupling will increase with the rising of the control frequency.

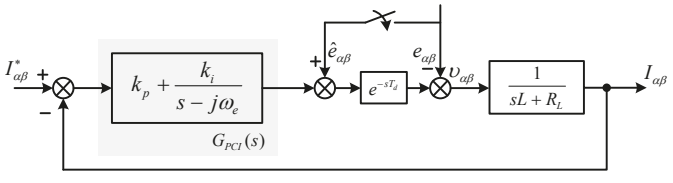
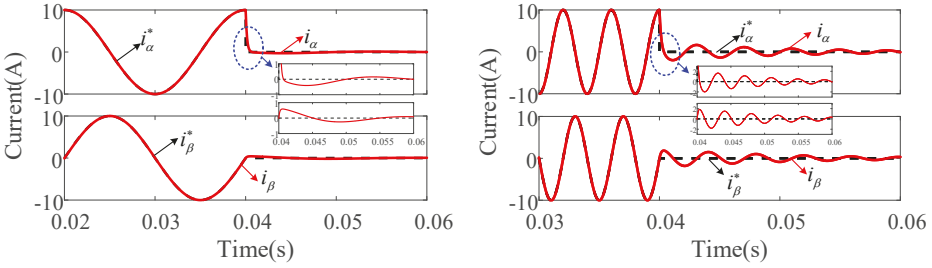


Figure 3. The diagram of PCI-based current closed-loop for GC-VSCs.



(**a**) $\omega_e = 2{\cdot}50{\cdot}\pi$ rad/s (**b**) $\omega_e = 2{\cdot}250{\cdot}\pi$ rad/s.

Figure 4. α-axis and β-axis current response with PCI controller.

3. The Proposed ROGI-Based Decoupled Current Controller

To suppress the axes-coupling in the PCI-based current loop. an effective decoupling method with ROGI-based decoupled current controller is proposed, which improves dynamic response performance of the current loop. For convenience, the proposed ROGI-based decoupled current controller is referred to as the D-PCI controller in the following section.

3.1. Structure of the D-PCI Controller

As shown in Figure 2b and the analysis of coupling, the key to effective decoupling is to remove the cross-coupling term $k_p \cdot \omega_e$. Thus, the structure of the proposed D-PCI current controller is shown in Figure 5. Thus, the transfer function of D-PCI can be expressed as

$$G_{D-PCI}(s) = k_p + \frac{k_i + j\omega_e k_p}{s - j\omega_e} \tag{3}$$

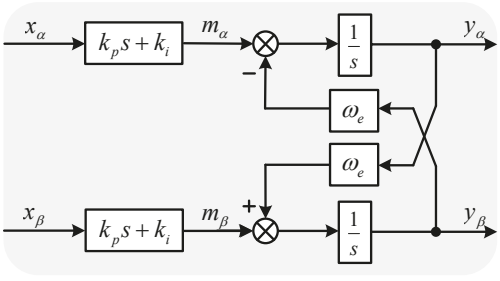


Figure 5. Structure of the proposed D-PCI current controller.

Based on Equations (2) and (3), the Bode plot of PCI and D-PCI controllers tuned at $\omega_e = 2{\cdot}\pi{\cdot}50$ rad/s (i.e., fundamental excitation frequency is 50 Hz) is shown in Figure 6. It can be seen that both PCI and D-PCI controllers achieve infinite gain at fundamental excitation frequency, which means that precise AC reference signal tracking can be realized. Moreover, D-PCI controller has superior performance in suppressing DC reference signal. The magnitude for D-PCI controller is −6.5 dB, while PCI controller is 27 dB.

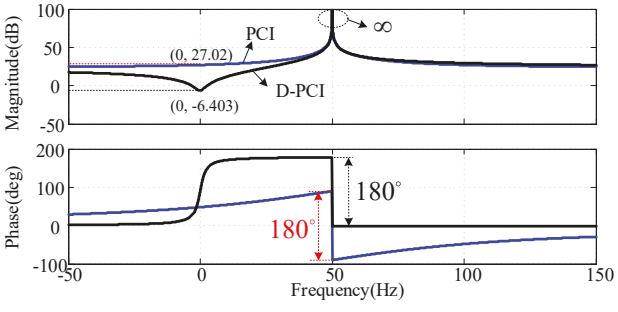
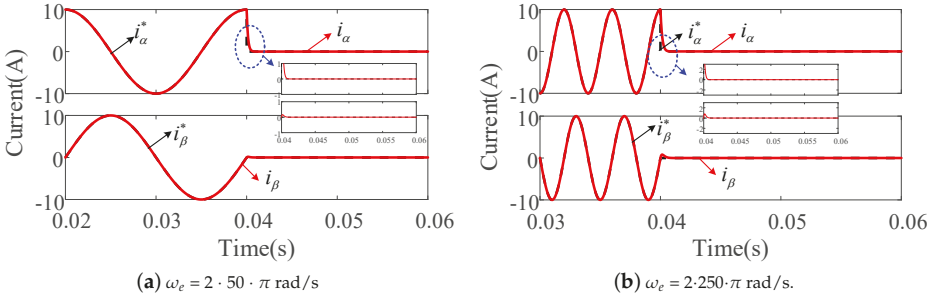


Figure 6. Bode plot of PCI and D-PCI controllers tuned at $\omega_e = 2 \cdot \pi \cdot 50$ rad/s.

Replacing the PCI with D-PCI in Figure 3, α-axis and β-axis current response with D-PCI controller is presented in Figure 7 when a step change occurs in reference current. In Figure 7a,b, it can be seen that, regardless of the control frequency, there is almost no coupling between the current of α-axis and β-axis.



(a) $\omega_e = 2 \cdot 50 \cdot \pi$ rad/s **(b)** $\omega_e = 2{\cdot}250{\cdot}\pi$ rad/s.

Figure 7. α-axis and β-axes current response with D-PCI controller.

3.2. Performance Analysis of the D-PCI Controller

From Figure 3 and Equation (3), the output current $I_{\alpha\beta}$ can be derived as

$$I_{\alpha\beta}(s) = \frac{e^{-sT_d}\cdot(k_p s+k_i)}{(sL+R_L)(s-j\omega_e)+e^{-sT_d}\cdot(k_p s+k_i)} I^*_{\alpha\beta}(s) - \frac{s-j\omega_e}{(sL+R_L)(s-j\omega_e)+e^{-sT_d}\cdot(k_p s+k_i)} e_{\alpha\beta}(s) \tag{4}$$

where

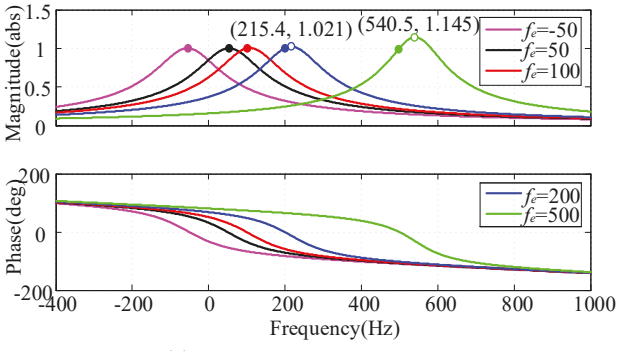
$$G^s_{CL}(s) = \frac{(k_p s+k_i)\cdot e^{-sT_d}}{(s-j\omega_e)(sL+R_L)+(k_p s+k_i)\cdot e^{-sT_d}} \tag{5}$$

is the transfer function between $I_{\alpha\beta}(s)$ and $I^*_{\alpha\beta}(s)$, and

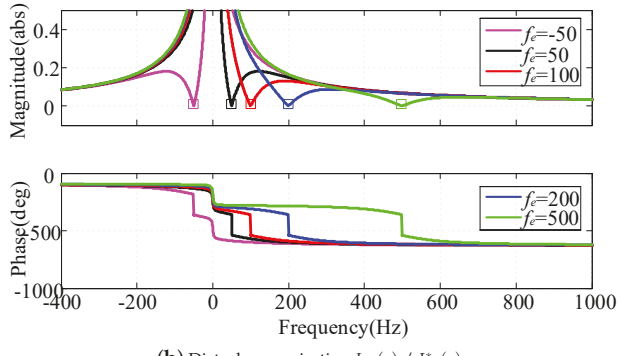
$$G^s_{DL}(s) = -\frac{s-j\omega_e}{(sL+R_L)(s-j\omega_e)+e^{-sT_d}\cdot(k_p s+k_i)} \tag{6}$$

is the transfer function between $I_{\alpha\beta}(s)$ and $e_{\alpha\beta}(s)$.

If the frequency of $I^*_{\alpha\beta}(s)$ (reference input signal) and $e_{\alpha\beta}(s)$ (disturbance signal) is equal to ω_e, i.e., $s = j\omega_e$, then $G^s_{CL}(j\omega_e) = 1$ and $G^s_{DL}(j\omega_e) = 0$. It means that D-PCI controller can realize tracking of AC reference signals and suppress AC disturbance signals. Both closed-loop frequency response and mathematical derivation would be used to evaluate the steady-state tracking performance.



(a) Reference tracking $I_{\alpha\beta}(s)$ / $I^*_{\alpha\beta}(s)$.



(b) Disturbance rejection $I_{\alpha\beta}(s)$ / $I^*_{\alpha\beta}(s)$.

Figure 8. Bode plot of closed-loop current control based on D-PCI controller.

According to Equations (5) and (6), the closed-loop frequency response curves at different control frequencies are shown in Figure 8. The following conclusions can be drawn:

(1) Since the controller provides infinite gain at the interested control frequency (−50 Hz, 50 Hz, 100 Hz, 200 Hz and 500 Hz), unity gain and 0° phase lag output current can be achieved, i.e., $I_{\alpha\beta}(s)/I^*_{\alpha\beta}(s) = 1\angle 0°$, the steady-state error is zero, as shown by "•" in Figure 8a.

(2) As shown by "○" in Figure 8a, a closed-loop anomalous peak (amplification phenomenon of output current) appears near the control frequency, and, as the control frequency increases, the peak value becomes larger, e.g., no obvious amplification appears at 50 Hz or 100 Hz, while the peak value is 1.02 (1.145) times of the unity gain at 215 Hz (540 Hz). It means that the closed-loop anomalous peak will aggravate the transient oscillation and increase the adjustment time and overshoot with the abrupt change of reference signal. Besides, if phase lock angle is inaccurate, the steady-state output current would be amplified.

(3) As shown in Figure 8b, the disturbance signal at the interested control frequency is completely suppressed, i.e., the magnitude is zero (as shown by "□").

The delay compensation method is used to suppress the closed-loop anomalous peak, and Figure 9 shows the closed-loop frequency response after delay compensation. It can be seen that the unity gain and 0° phase lag output current are achieved at the interested control frequencies, and the closed-loop anomalous peak is completely excluded, as shown by "•" in Figure 9.

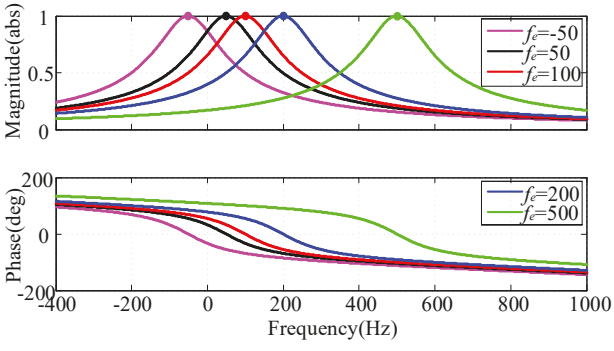


Figure 9. Bode plot of current closed-loop with delay compensation with D-PCI controller.

From the analysis of delay compensation above, the influence of time delay can be ignored. According to the internal model control (IMC) method [13], to cancel the pole of $G^s_{PL}(s)$ by a matching zero in D-PCI controller, $k_i/k_p = R_L/L$ should be satisfied. Hence, Equation (5) can be simplified into Equation (7)

$$G^s_{CL}(s) = \frac{K}{s - j\omega_e + K} \tag{7}$$

where $K = k_p/L$ is the only degree of freedom of the D-PCI controller. Thus, the reference current $i^*_{\alpha\beta}(t)$ can be expressed by

$$i^*_{\alpha\beta}(t) = I_m \cdot \cos(\omega_e t) + jI_m \cdot \sin(\omega_e t) \tag{8}$$

the output current $i_{\alpha\beta}(s)$ is equal to

$$I_{\alpha\beta}(s) = G^s_{CL}(s) \cdot I^*_{\alpha\beta}(s) = \frac{I_m}{s - j\omega_e} - \frac{I_m}{s - j\omega_e + K} \tag{9}$$

in the time domain, Equation (9) can be written as

$$i_{\alpha\beta}(t) = I_m \cdot (\cos\omega_e t - e^{-Kt}) + jI_m \cdot (\sin\omega_e t - e^{-Kt}) \tag{10}$$

if $t \to \infty$ in (10), then

$$\lim_{t\to\infty} i_{\alpha\beta}(t) = I_m \cdot \cos\omega_e t + jI_m \cdot \sin\omega_e t = i^*_{\alpha\beta}(t) \tag{11}$$

It can be seen that D-PCI controller can be used to track ac reference signal without steady-state error, and, with the increase of open-loop gain K, the dynamic response becomes faster. The design of the parameter K is introduced in the next section.

3.3. Parameter Tuning for the D-PCI Controller

In this section, a parameter design method based on root locus is presented. By comprehensive analysis of the IMC method, and as shown in Figure 3, the open-loop transfer function is simplified to

$$G_{OL}^{s}(s) = \frac{(k_p s + k_i) \cdot G_d^s(s)}{(s - j\omega_e)(sL + R_L)} = \frac{K \cdot G_d^s(s)}{(s - j\omega_e)} \tag{12}$$

Taking the following parameters as an example, both the switching and sampling frequency are set to 10 kHz: $L = 5$ mH, $R_L = 0.5\ \Omega$ and $\omega_e = 100\pi$ rad/s. Figure 10 shows the root locus of current loop based on D-PCI controller and Figure 10b is a closer view of the dotted line frame in Figure 10a.

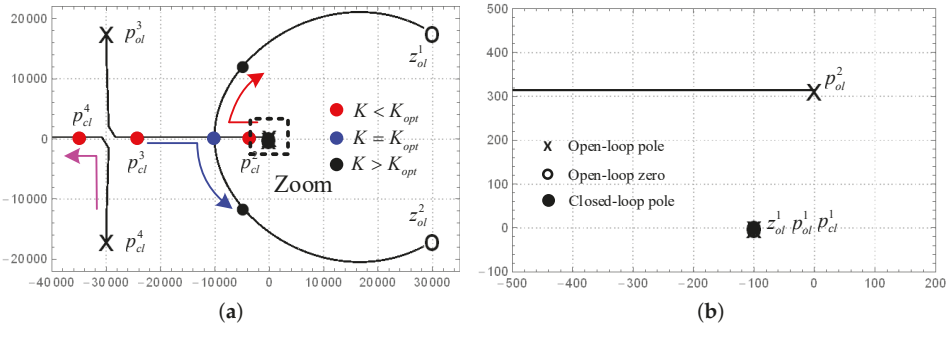


Figure 10. Root locus of current loop based on D-PCI controller: (**a**) general view; and (**b**) closer view of the dotted line frame.

The decay rate $\sigma = \mathrm{Re}(p_{cl})$ and the damping ratio $\xi = \sigma / |p_{cl}|$ are two important indicators to evaluate the system performance. As shown by the closer view in Figure 10b, the open-loop zero z_{ol}^1 and closed-loop pole p_{ol}^1 overlap with each other, while the effect of p_{ol}^1 on system stability and dynamic response is negligible. When K is low ($K < K_{opt}$), p_{cl}^3 and p_{cl}^4 are far away from imaginary axis ($\mathrm{Re}(p_{cl}^2) \ll \mathrm{Re}\{(p_{cl}^3),(p_{cl}^4)\}$), p_{cl}^2 becomes the dominant closed-loop pole, the system is in an overdamped state. By increasing K until p_{cl}^2 and p_{cl}^3 overlap (this gain value of K is defined as K_{opt}), the system switches to a state of critical damping ($\xi \approx 1$), as shown by "•" in Figure 10a, and the maximal stability and the fastest dynamic response are obtained simultaneously. If K is increased further, the system becomes underdamped and overshoot occurs in the transient response. At the same time, the stability decreases because p_{cl}^2 and p_{cl}^3 are closer to the imaginary axis. Consequently, K_{opt} is an optimal choice in terms of stability and dynamic response.

Figure 11 shows the time-domain simulation of output current with different gains of K when an abrupt change happens in the reference current. It can be observed that simulation results are consistent with theoretical analysis based on root locus. Overshoot occurs in the current transient response (when $K > K_{opt}$) due to the underdamped characteristics. If $K < K_{opt}$, the excessive damping ratio limits the dynamic performance (although the overshoot is suppressed). When $K = K_{opt}$, there is no overshoot during the transient response. Simulation results are summarized in Table 1, where it can be seen that $K = K_{opt}$ is a best choice if overshot and transient response are considered simultaneously.

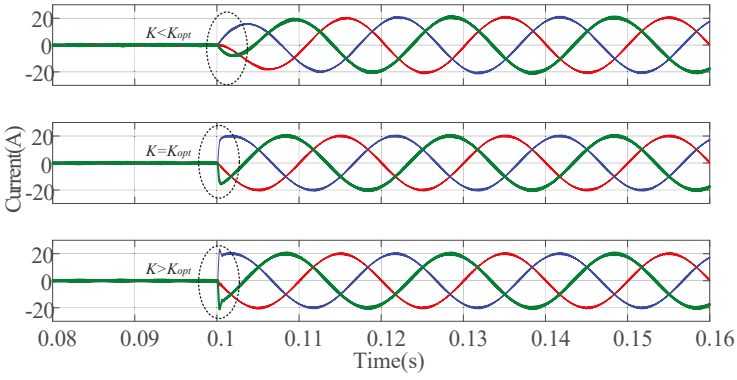


Figure 11. Output current response with different gains of K when an abrupt change happens in the reference current.

Table 1. Evaluation for different value of K

Gain (K)	Damping Ratio ξ	Overshoot	Response Speed
$K < K_{opt}$	$\xi > 1$	no	slow
$K = K_{opt}$	$\xi = 1$	no	fast
$K > K_{opt}$	$\xi < 1$	have	fast

4. Simulation and Experimental Results

To verify the control performance of the proposed D-PCI controller, simulation and experimental results are presented in this section. The main parameters for simulation and experiment are summarized in Table 2.

Table 2. Simulation and experimental setup parameters.

Symbol	Parameters	Value	Unit
V_s	Phase-to-phase voltage	380	V
f	Grid frequency	50	Hz
U_{dc}	DC-link voltage	700	V
L	Inductance of the L filter	5	mH
R_L	Equivalent resistance of the L filter	0.05	Ω
C_{dc}	Capacitor of DC-link	4000	uF
$R(P)$	Active power Load	50(10)	Ω(kW)
I_q^*(Q)	Reactive power Load	21.5(10)	A(kvar)
f_{sw}	Switching frequency	10	kHz
f_s	Sampling frequency	10	kHz
BW	Bandwidth of the current loop	600	Hz
k_{ip}	Proportional gain of the current loop	12.3	/
k_{ii}	Integral gain of the current loop	123	/
k_{vp}	Proportional gain of the voltage loop	0.5	/
k_{vi}	Integral gain of the voltage loop	29.87	/

Figure 12 shows the double closed-loop control scheme of GC-VSC. The outer loop, which has slower dynamics, regulates the DC-link voltage. The inner loop is used to track the reference current, which is the output of the outer loop. In this study, the DC-link voltage was set to 700 V. Comparisons between the proposed and PCI controller were performed in terms of steady-state error and dynamic response.

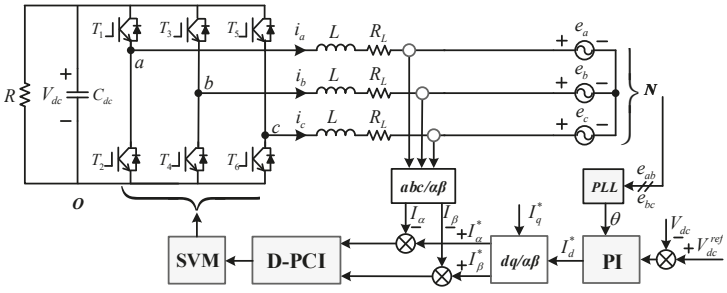


Figure 12. The double closed-loop control scheme of GC-VSC.

4.1. Simulation Results

Figure 13 shows the simulation results of the proposed control strategy. As shown in Figure 13a, the simulation process consisted of several critical time points with load changes, which were used to test the steady-state and dynamic response of the proposed control strategy. Figure 13b–d shows the closer views of Zoom1, Zoom2 and Zoom3 in Figure 13a.

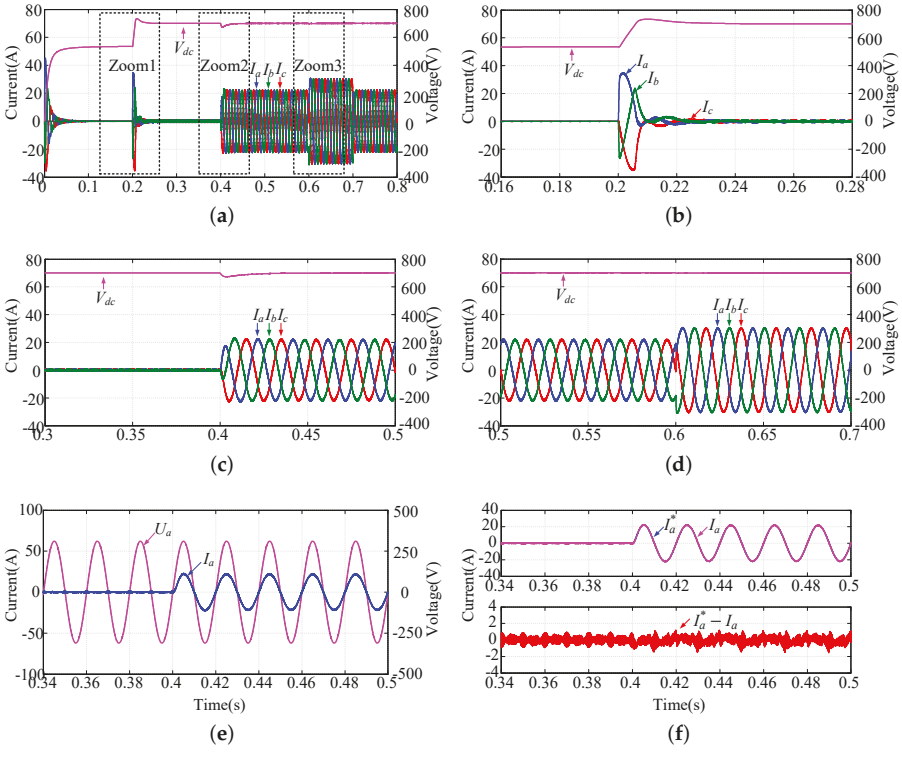


Figure 13. Simulation results of the proposed control strategy: (**a**) general view of the DC-link capacitor voltage and three-phase grid current; (**b**) three-phase grid current when the GC-VSC operates in the state of PWM rectifier; (**c**) three-phase grid current when 10 kW active power is applied; (**d**) three-phase grid current when 10 kvar reactive power is added; (**e**) grid voltage and current of phase A when unity power control is implemented; and (**f**) reference current, actual current and current error of phase A when load changes.

In Figure 13b, it can be seen that the DC-link voltage is regulated to 700 V when the GC-VSC operates in the state of PWM rectifier, which can be replaced by a DC power supply.

Figure 13c shows the transient response of three-phase grid current when 10 kW active power load is applied. It can be seen that the stability of the grid current is achieved after 10 ms. Actually, the dynamic regulation time is less than 10 ms, since the DC-link voltage drop extends the settling time. The excellent dynamic response performance can be further validated by the results in Figure 13d, when 10 kvar reactive power load is added. There is almost no transient regulation process for grid current. In fact, since the reactive power is not consumed, the DC-link voltage does not drop significantly. Moreover, as shown in Figure 13c,d, negligible overshoot is obtained when using the parameter design method in Section 3.

Figure 13e represents the grid voltage and current of phase A with the unit power factor control method. The phase is exactly the same in steady state, which reflects the tracking ability of the D-PCI controller. As shown in Figure 13f, the curves (reference current I_a^* and actual I_a) come closest to coinciding in shape even if a sudden change occurs at 0.4 s, and the current error fluctuates around zero. It shows that the D-PCI controller has the ability to track AC reference signals with zero steady-state error and fast dynamic response.

Figure 14 represents the simulation results with PCI controller. The parameters are consistent with the D-PCI-based control strategy. In Figures 13c and 14a, it can be seen that the dynamic response of D-PCI is faster than PCI, and the excellent performance can be further observed in Figures 13f and 14b. The PCI-based grid current tracks its reference with zero steady-state error after about 30 ms while it takes about 15 ms for the proposed control strategy.

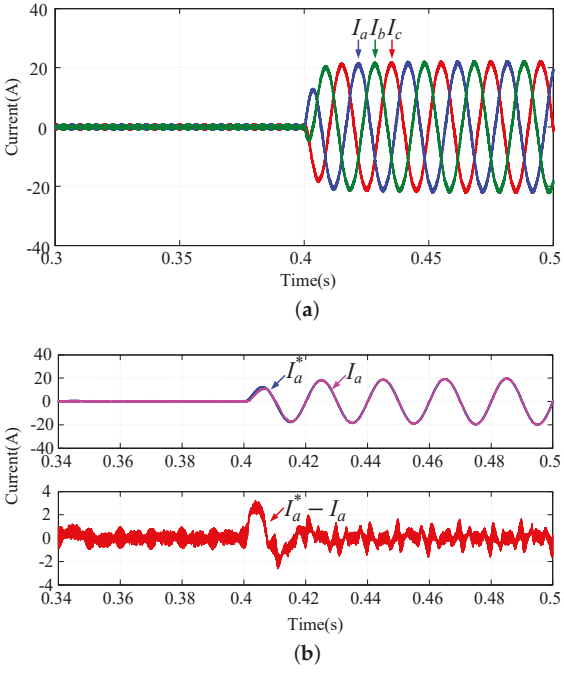


Figure 14. Simulation results of the PCI-based control strategy: (**a**) three-phase grid current when 10 kW active power is applied; and (**b**) reference current, actual current and current error of phase A when load changes.

4.2. Experimental Results

To further support the theoretical analysis and simulation results, the experimental setup of GC-VSC was built in the laboratory, as shown in Figure 15. The parameters in experimental setup were the same as in simulation ones, which are listed in Table 1. Active power load consists of two parallel 100 Ω/10 kW resistors. The real-time algorithm was implemented in the hardware controller, based on TMS320C28346 DSP and EP3C16Q240 FPGA, whose output PWM signals are connected to converter by optical fiber. Experimental waveforms were captured by Yokogawa DL850 oscilloscope. Specifically, the hardware controller lacked of digital-to-analog converter and, since the reference current was a digital variable, it could not be directly measured by the oscilloscope. Therefore, real-time data were acquired by saving memory in Code Composer Studio (Ver.5.5.0) and the waveforms (Figures 16f and 17b) were plotted in MATLAB.

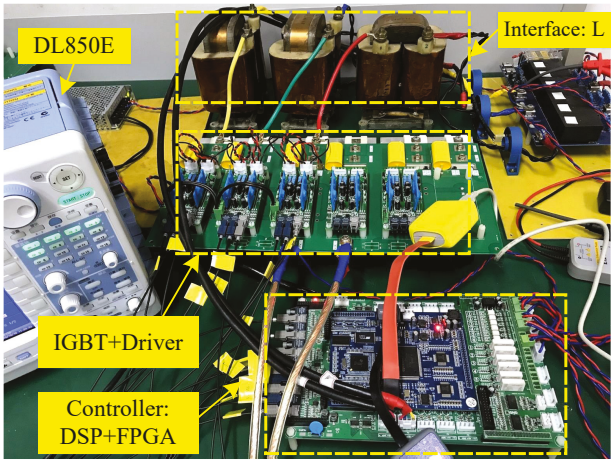


Figure 15. Experimental setup of the GC-VSC.

Figures 16 and 17 show the experimental results of the proposed and PCI-based control strategy, which correspond to the simulation results in Figures 13 and 14, respectively. It can be observed that the experimental and simulation results match to a great extent. The slight difference is the distortion of grid current, which can be mainly attributed to harmonics contained in the grid voltage.

Figure 16 shows that the excellent stability and fast dynamic response of the proposed D-PCI-based control strategy can be obtained even though the GC-VSC experiences different load variation. The superiority can be further verified by the comparative experiments. From the results in Figures 16f and 17b, the following can be concluded: (1) the current error of both strategies tends to zero, which means that tracking of ac reference signal with zero steady-state error can be realized from both methods; and (2) the proposed strategy has faster dynamic response, as the error current of the PCI-based strategy restores to zero after about 30 ms while there is almost no dynamic process for the proposed control strategy.

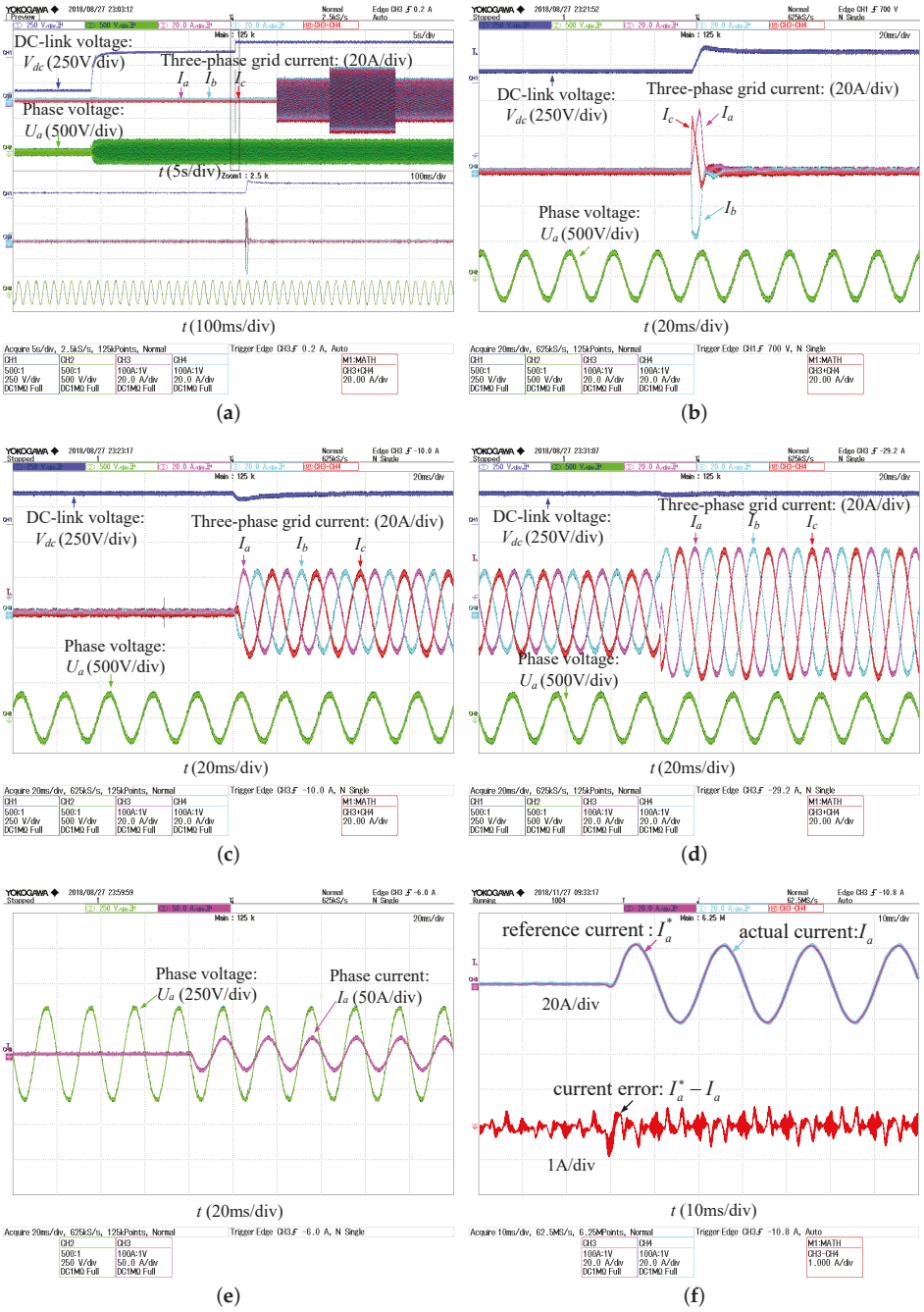
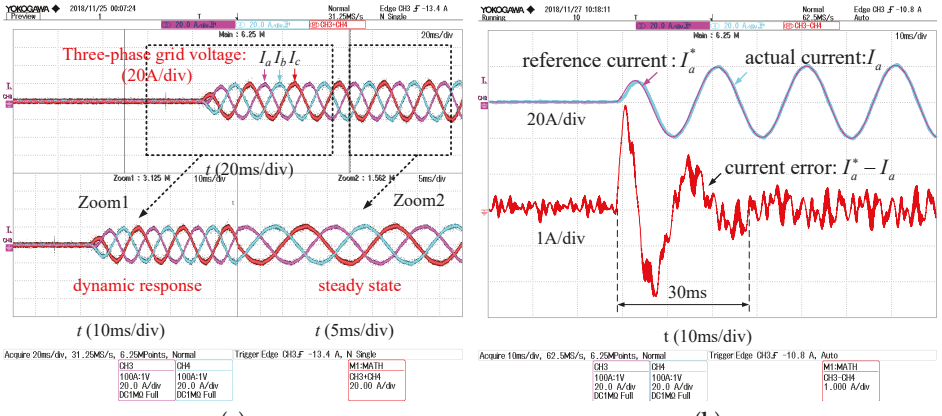


Figure 16. Experimental results of the proposed control strategy: (**a**) general view of the DC-link capacitor voltage and three-phase grid current; (**b**) three-phase grid current when the GC-VSC operates in the state of PWM rectifier; (**c**) three-phase grid current when 10 kW active power is applied; (**d**) three-phase grid current when 10 kvar reactive power is added; (**e**) grid voltage and current of phase A when unity power control is implemented; and (**f**) reference current, actual current and current error of phase A when load changes.



(**a**) (**b**)

Figure 17. Experimental results of the PCI-based control strategy: (**a**) three-phase grid current when 10 kvar reactive power is applied; and (**b**) reference current, actual current and current error of phase A when load changes.

5. Conclusions

To attenuate the impact of axes cross-coupling caused by PCI controller, a novel D-PCI controller-based decoupling method in the stationary frame is proposed to track sinusoidal reference signals with zero steady-state error and achieve fast dynamic response. Moreover, an optimal gain method for parameter tuning is presented for enhancing the stability of the current loop. Comparing with PCI, the proposed D-PCI controller can obtain faster dynamic response, as well as better stability performance. Comparative simulations were performed and experimental results between the proposed and PCI controller were compared, which validated the superiority of the proposed D-PCI controller.

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Nonsingular Terminal Sliding Mode Control Based on Binary Particle Swarm Optimization for DC–AC Converters

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Abstract: This paper proposes an improved feedback algorithm by binary particle swarm optimization (BPSO)-based nonsingular terminal sliding mode control (NTSMC) for DC–AC converters. The NTSMC can create limited system state convergence time and allow singularity avoidance. The BPSO is capable of finding the global best solution in real-world application, thus optimizing NTSMC parameters during digital implementation. The association of NTSMC and BPSO extends the design of classical terminal sliding mode to converge to non-singular points more quickly and introduce optimal methodology to avoid falling into local extremum and low convergence precision. Simulation results show that the improved technique can achieve low total harmonic distortion (THD) and fast transients with both plant parameter variations and sudden step load changes. Experimental results of a DC–AC converter prototype controlled by an algorithm based on digital signal processing have been shown to confirm mathematical analysis and enhanced performance under transient and steady-state load conditions. Since the improved DC–AC converter system has significant advantages in tracking accuracy and solution quality over classical terminal sliding mode DC–AC converter systems, this paper will be applicable to designers of relevant robust control and optimal control technique.

Keywords: binary particle swarm optimization (BPSO); nonsingular terminal sliding mode control (NTSMC); global best solution; total harmonic distortion (THD); DC–AC converter

1. Introduction

DC–AC converters have been widely applied in renewable energy systems, such as solar photovoltaic (PV) energy systems, wind turbine generator systems and fuel cell power generation systems. For example, a solar PV energy system can convert sunlight into usable electrical energy. The simplified solar PV systems include PV panels, DC–DC converters, DC–AC converters and loads. Such system can be designed to yield maximum power delivered to the load. There are two power conversion stages in this structure, so it can be considered a two-stage system. The DC–DC converter is used to handle maximum power point tracking (MPPT) and regulate the DC load voltage. At the same time as the grid connection occurs, the power is generated by the PV panel and converted to AC power by the DC–AC converter. Furthermore, the operation of DC–AC conversion and maximum power point tracking (MPPT) can be combined into a single-stage system using only one DC–AC converter. In various power converter topologies for renewable energy applications, inductor capacitor (LC) filter DC–AC converters are often used as an interface between renewable energy and the grid. The converter DC link is connected to the PV panel either directly or through an intermediate DC–DC power conversion stage. The LC low-pass filter eliminates higher harmonics in the converter's pulse width

modulation (PWM) output, enabling pure sine. Therefore, even under plant parametric variations and external load disturbances, the requirements of high-performance DC–AC converters must involve fast dynamic response and low total harmonic distortion (THD) of the output voltage. In order to meet these requirements, a proportional plus integral (PI) controller is frequently used; nevertheless, the controller may not be able to withstand severe disturbances, thereby degrading the performance of the system [1,2]. In order to obtain better tracking accuracy, the different control schemes are discussed in the research literature [3–7].

The repetitive control related to the H-infinity concept is proposed for the inductor-capacitor-inductor (LCL) grid-tied inverter to achieve near-zero steady-state error and reduce harmonic distortion of the output voltage caused by the nonlinear load. However, this method requires a complex control algorithm [3]. A simpler fractional repetitive method is developed for the voltage control of the microgrid to suppress the generation of harmonics. Although the structure is simple and exhibits a rapid dynamic response when the load suddenly changes, the steady-state response is not significantly improved [4]. A deadbeat control based on predictive model is proposed to control the grid-connected inverter. The proposed inverter with nonlinear load shows good steady state, but this method depends largely on the accuracy of the parameters. The transient performance is somewhat mediocre [5]. The improved direct deadbeat voltage control is applied to the closed-loop regulation of an island AC microgrid. This method is sensitive to changes in plant parameters, and even if the system exhibits a fast dynamic response, it may lead to non-zero steady-state errors [6]. Since the problem of parameter uncertainty and external disturbance can be reduced, it is recommended to combine mu-synthesis with the H-infinity method for island microgrid control; however, the mu-synthesis algorithm complicates the digital implementation and the resulting waveform has visible distortion, especially in strong nonlinear cases [7].

Sliding mode control (SMC) has inherent robustness to system uncertainty and is used as an effective technique in many different engineering fields [8–10]. The SMC system theory and its related sliding surfaces have been widely used in control design for the past 40 years, and the application fields are increasing (power system control, aerospace design problems, robot manipulator control) [11–14]. The primary purpose of the sliding behavior in the SMC direction allows the system state to tend to a predetermined desired hyperplane, i.e., a sliding surface or slip manifold defined in the state space. Once the state trajectory hits the sliding surface, it enters the sliding mode and stays there; after that, the system can achieve its control objectives and can suppress internal parameter changes and external load disturbances [15–18]. Of course, the controller of the DC–AC converter is also universally designed by SMC [19–21]. For the single-phase inverter, a fixed switching frequency sliding mode is proposed; the control design adopts the traditional sliding surface, which causes the output voltage distortion under non-linear load [19]. In order to retrieve the incomplete system dynamics of the grid-connected inverter, a sliding surface based on multi-resonance is designed. Although it can enhance the performance of steady state and transient, this algorithm is time-consuming calculation [20]. The improved SMC shows the ability to suppress uncertainty interference for voltage regulation in the microgrid, but it has complex hardware design and significant jitter [21]. As mentioned above, these classical SMC methods have problems with non-time-limited convergence and jitter.

In the case of a path tracking system, the invariant characteristics exhibited by the classical SMC are only maintained during the sliding phase, and the tracking trajectory may be affected by external load disturbances or changes in internal parameters of the arrival phase. Previous research efforts have attempted to reduce tracking errors and speed up arrival times. The observer can shorten the arrival time, but it uses a traditional reduced-order design, resulting in large jitter, which is not desirable in dynamic systems [22]. In order to eliminate the phase of arrival, a time varying sliding surface given by the constraint of zero error under initial conditions is applied to a rotary actuator system. However, it does not conform to the general situation because the initial conditions can be arbitrarily assigned in the actual system [23]. An indirect sliding mode power control method was developed to control

the grid-connected power converter. Although this method allows the system to slide to the sliding surface in a suitable short time, there is a phenomenon of jitter around the sliding surface [24].

In recent years, an interesting series of SMC controllers, named nonsingular terminal sliding mode (NTSMC) has allowed finite time convergence, and overcome the singularity problem [25]. The NTSMC has been well applied in various fields [26,27]. Although the NTSMC can drive the system state to converge to the origin within a limited time while still retaining the robustness of the classical SMC, it has a jitter problem [28]. From a practical point of view, system parameter changes, external load disturbances, and unmodeled dynamics are difficult to know. If the system uncertainty limit is large or small, the jitter or steady-state error may occur, and the existence and invariance of the sliding mode cannot be guaranteed. Many studies have used adaptive control methods to tackle the effect of the jitter caused by boundary uncertainty. Such solutions effectively reduce the jitter and steady-state error, enhancing both transient and steady-state behavior [29–38]. In addition, the NTSMC has the difficulty in choosing optimal controller parameters particularly in face of large variations of model parameters and load changes.

In the upcoming era of artificial intelligence, the BPSO method has been widely applied in solving optimization problems due to its simplicity, fast execution and high-quality solution [39–43]. For this reason, the BPSO is used to find the optimal values of the NTSMC parameters, therefore significantly improving the control performance and avoiding the tedious trial and error tuning. This improved technique provides another option and potential recommendation as opposed to not adding optimal methodology in the classical terminal sliding mode or SMC. Although the final performance results of the improved system are not superior to the recent THD results of the previous work, it does improve the TSMC method and produces a systematic optimal tuning for the determination of the controller parameters. It may be noted that the association of the presented NTSMC and BPSO results in a closed loop feedback DC–AC converter system that has low THD under steady state load and a fast response under transient load. Finally, the efficacy of the improved technique is verified by the implementation of a digital signal processing (DSP)-based DC–AC converter system, and the improved system is also evaluated by MATLAB/Simulink software.

2. Modeling of DC–AC Converter

Figure 1 depicts a commonly used DC–AC converter consisting of a full-bridge switching element with MOSFETs (metal-oxide-semiconductor field-effect transistors), an LC filter and a resistive load. The DC bus voltage V_s is expressed by the output voltage v_c, and the load R is represented by the output current i_o. In the case of a situation $x_1 = v_c$ and $x_2 = \dot{v}_c$ defined as a state variable, the state equation of the system can be written as

$$\dot{x} = Ax + Bu \tag{1}$$

where $x = \begin{bmatrix} x_1 & x_2 \end{bmatrix}^T$, $A = \begin{bmatrix} 0 & 1 \\ 1/LC & 1/RC \end{bmatrix}$, $B = \begin{bmatrix} 0 & K_{PWM}/LC \end{bmatrix}^T$, and u is the control signal. When the switching frequency is much higher than the fundamental frequency of the AC output, it can be considered as the proportional gain K_{PWM} of the PWM full-bridge switching element and is consistent with $V_s/\hat{v}_{tr}$; $\hat{v}_{tr}$ represents the amplitude of the triangular wave v_{tr} in the PWM. According to (1), the output voltage v_c must follow a sinusoidal reference voltage v_r. Therefore, the tracking request $v_c(t) \to v_r(t)$ as $t \to \infty$ is maintained and the design problem of the DC–AC converter will be the trajectory tracking control problem. The tracking errors $e = \begin{bmatrix} e_1 & e_2 \end{bmatrix}^T$ is defined as

$$e = x - x_r \tag{2}$$

where $x_r = \begin{bmatrix} v_r & \dot{v}_r \end{bmatrix}^T$.

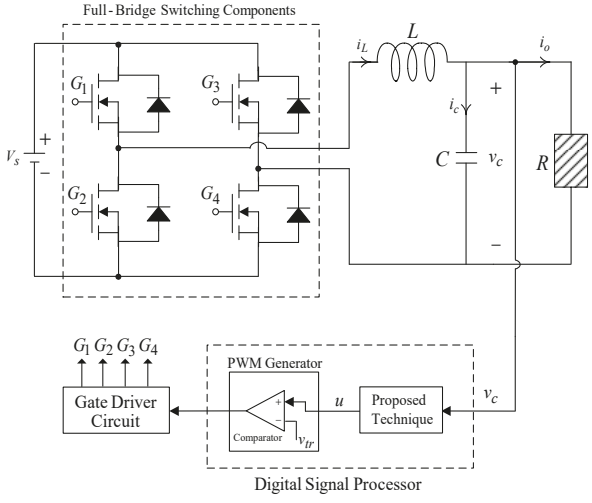

Figure 1. Structure of DC–AC converter.

It can be seen from (1) and (2) that the error state equation of the DC–AC converter can be expressed as

$$\begin{cases} \dot{e}_1 = e_2 \\ \dot{e}_2 = -\frac{1}{LC}e_1 - \frac{1}{RC}e_2 + \frac{K_{PWM}}{LC}u - N \end{cases} \tag{3}$$

where $N = \frac{1}{LC}v_r + \frac{1}{RC}\dot{v}_r + \ddot{v}_r$ is the disturbance.

From (3), the control signal u must be designed so well that the tracking error e can converge to zero. In fact, the NTSMC is a fine control method with nonsingular fast convergence characteristics. The system (3) using NTSMC will achieve fast finite time convergence, strong robustness and infinite stability. However, when the load on a DC–AC converter is a large step change or uncertainty or even a severe nonlinear environment, a global optimization algorithm for the systematic and optimal choice of NTSMC parameter values is becoming more important. Based on such a motivation, and the practical application of artificial intelligence method is rapidly becoming a hot topic in engineering and science, it is a good idea to introduce an optimal methodology in the NTSMC design, providing an alternative reference for researchers. Therefore, NTSMC with BPSO method is proposed to improve the transience and steady-state behaviors of the classical TSMC to provide more accurate tracking. A DC–AC converter using this improved control design can produce a higher performance AC output voltage.

3. Proposed Control Technique

3.1. Problem Statement

First, a brief summary of the problem statement for a nonlinear system using the classical TSMC, is summarized and an improved technique is then designed. Consider the second-order uncertain nonlinear dynamic systems below:

$$\begin{aligned} \dot{x}_1 &= x_2 \\ \dot{x}_2 &= f(x) + g(x) + b(x)u \end{aligned} \tag{4}$$

where the system state is $x = \begin{bmatrix} x_1 & x_2 \end{bmatrix}^T$, $f(x)$ and $b(x)$ stands for a smooth nonlinear function x, $g(x)$ denotes parameter uncertainty and external disturbance and u represents the control input.

To achieve finite time convergence of the system state, the following first-order terminal sliding variable can be defined as

$$s = x_2 + \mu x_1^{\gamma} \tag{5}$$

where $\mu > 0$ is the design constants and $0 < \gamma = \gamma_1/\gamma_2 < 1$ (γ_1 and γ_2 are positive odd integers).

An SMC law $u = u^+(x)$, $u^-(x)$ for $s > 0$, $s < 0$ can be used, which is expressed as driving s to the sliding mode $s = 0$ for a limited time. Therefore, system dynamics can be controlled by the following differential equations:

$$x_2 + \mu x_1^{\gamma} = \dot{x}_1 + \mu x_1^{\gamma} = 0 \tag{6}$$

The limited time t_s from the initial state $x_1(0)$ to zero can be determined by

$$t_s = \frac{\left|x_1(0)\right|^{1-\gamma}}{\mu(1-\gamma)} \tag{7}$$

This indicates the convergence of the two system states x_1 and x_2 the convergence of zero in a finite time in the NTSMC manifold. Considering the Jacobian matrix J, the system state converges to zero gain in a finite time around the equilibrium $x_1 = 0$.

$$J = \frac{\partial \dot{x}_1}{\partial x_1} = -\frac{\mu\gamma}{{x_1}^{(1-\gamma)/\gamma}} \tag{8}$$

From (8), we can obtain the eigenvalues of the first-order approximation matrix as follows.

$$J \to -\infty \text{ when } x_1 \to 0 \tag{9}$$

It is inferred that the eigenvalue has a tendency of negative infinity at the equilibrium point, that is, the speed of the system trajectory to the equilibrium becomes infinite, resulting in limited time accessibility.

Thus, for error dynamics (3), the finite-time terminal sliding function can be expressed as

$$s = \dot{e}_1 + \mu e_1^{\gamma} \tag{10}$$

Using the (10), the $s = 0$ and e_1 arrive within a limited time. The control law can be designed to ensure that TSM occurs as follows.

$$u = u_e + u_s \tag{11}$$

with

$$u_e(t) = b^{-1}[a_1 e_1 + a_2 e_2 - \mu(\gamma e_1^{\gamma-1} \cdot e_2)] \tag{12}$$

$$u_s(t) = -b^{-1}[K \operatorname{sgn}(s)]\ , K > \left|N(t)\right| \tag{13}$$

where $a_1 = 1/LC$, $a_2 = 1/RC$, $b = K_{PWM}/LC$, and u_e called the equivalent control component, control undisturbed plants, such that $s = 0$ and $\dot{s} = 0$. The named sliding control component suppresses system uncertainty. Therefore, the state trajectory will reach the sliding mode $s = 0$ and perform a limited system state convergence time. However, it is worth noting that there are the following problems in the equivalent control component: (i) If $e_2 \neq 0$ when $e_1 = 0$ and $0 < \gamma < 1$, the $u_e(t)$ with $e_1^{\gamma-1} e_2$ may result in a singularity. This singularity causes the control law to produce an unbounded control signal, resulting in an unstable closed loop system. (ii) An imaginary number $e_1^{\gamma-1}$ can be generated in a given situation $0 < \gamma < 1$.

3.2. Control Design

To overcome the singularity problem, the (10) is reconstructed into

$$s = e_1 + \frac{1}{\lambda} e_2^{\frac{q}{p}} \tag{14}$$

where $\lambda > 0$ and p, q are positive odd numbers ($p < q < 2p$). Then, a sliding-mode reaching equation $\dot{s} = -\eta_1 s - \eta_2 |s|^{1-\gamma} \mathrm{sgn}(s)$ is employed. The control law can be expressed as

$$u(t) = u_{nft}(t) + u_s(t) \tag{15}$$

with

$$u_{nft}(t) = b^{-1}[a_1 e_1 + a_2 e_2 - \lambda \frac{p}{q} e_2^{2-\frac{q}{p}}] \tag{16}$$

$$u_s = -b^{-1}\Big[\eta_1 s + \eta_2 |s|^{1-\gamma} \mathrm{sgn}(s)\Big],\ \eta_1,\ \eta_2 > 0,\ 0 < \gamma < 1 \tag{17}$$

where there is no negative index equivalent control u_{nft}, which results in non-singularity, and u_s represents the sliding control for compensating the influence of the disturbance. Therefore, the system state will be forced to arrive $s = 0$ and converge in a limited time.

Proof. Choose Lyapunov candidate as

$$V = \frac{1}{2} s^2 \tag{18}$$

Along the dynamic system trajectory (3) and the control law (15), and use (14), the time derivative V is given as

$$\begin{aligned} \dot{V} &= s\dot{s} \\ &= s\left(\dot{e}_1 + \tfrac{1}{\lambda}\tfrac{q}{p} e_2^{\frac{q}{p}-1} \dot{e}_2\right) \\ &\le -s\left(\tfrac{1}{\lambda}\tfrac{q}{p} e_2^{\frac{q}{p}-1} (\eta_1 s + \eta_2 |s|^{1-\gamma}) \mathrm{sgn}(s)\right) \end{aligned} \tag{19}$$

Since $e_2^{q/p-1} > 0$, $\dot{V} \le 0$, the surface of the NTSMC in (19) is allowed to converge to equilibrium in a limited time. Once $s = e_1 + \lambda^{-1} e_2^{q/p}$, the state of system (3) will also converge to equilibrium within a finite time. However, the load may be a large load disturbance that provides inaccurate tracking performance in the system (3), i.e., the output voltage of the DC–AC converter is not exactly equal to the desired sinusoidal waveform. It is thus important to find out the optimal values of the NTSMC parameters in the (15) to maintain satisfactory performance of the DC–AC converter. To avoid tedious, time-consuming trial-and-error calculations, and obtain global best solutions, the BPSO method is employed to get the optimal value of NTSMC parameters. Finally, the combination of the DC–AC converter in (3) with BPSO method and NTSMC is asymptotically stable, and then achieves finite-time convergence to zero of tracking errors. The BPSO algorithm can be used illustrated in (20) and (21). The (20) and (21) show the evolution models of a particle. The speed and position of each particle can be renovated while flying toward aim.

$$v_i^{t+1} = \sigma_0 v_i^t + \sigma_1 k_1 (\chi_i^{pb} - \chi_i) + \sigma_2 k_2 (\chi_i^{gb} - \chi_i) \tag{20}$$

$$\chi_i^{t+1} = \begin{cases} 0\ , \text{ if rand} \ge Sig(v_i^{t+1}) \\ 1\ , \text{ if rand} < Sig(v_i^{t+1}) \end{cases} \tag{21}$$

where σ_0, σ_1 and σ_2 denote variables, and k_1, k_2 indicate random numbers, v_i is present flying speed, χ_i stands for present position, χ_i^{pb} is local best position, χ_i^{gb} represents global best position, and Sig symbolizes sigmoid function that converts the particle velocity into the probability $1/1 + e^{-v_i^{t+1}}$. □

4. Simulation and Experimental Results

In order to test the performance and robustness of the improved technique, the simulation and experimental results of the improved technique were compared to those obtained using the classical TSMC. The system parameters are as follows: The system parameter are listed as follows: $V_s = 200$ V,

$v_c = 110\ V_{rms}$, $f_o = 60$ Hz, $v_r(t) = \sqrt{2} \cdot 110 \cdot \sin(2\pi \cdot 60 \cdot t)$, $f_s = 15$ kHz, $L = 0.12$ mH, $C = 2\ \mu$F, rated load $= 12\ \Omega$. Under the abrupt load change from no load to 12 ohm, the simulated results obtained using the improved technique and classical TSMC are shown in Figures 2 and 3, respectively. Compared to classical TSMC, the improved technique exhibits a slight voltage drop and allows for fast output voltage recovery to verify its limited time accessibility. Due to the optimal tuning of the BPSO, after an instantaneous voltage dip (7 V_{rms}), the output voltage with the improved technique can be restored to the sinusoidal reference voltage, but the classical TSMC results in a large voltage dip (22 V_{rms}). Figure 4 shows that the improved technique can allow random variations in filter parameters L and C from 10% to 200% and 10% to 200% of the nominal value under a 12 ohm resistive load, respectively; however, the classical TSMC shown in Figure 5 yields the significant oscillations and leads to a descent in system robustness. Table 1 shows the simulated comparison of the voltage drop and %THD of the output voltage for step load and LC variation. A prototype of the DC–AC converter depicted as Figure 6 is constructed. Figure 7 illustrates the experimental waveform obtained using the improved technique under the step load from no load to 12 ohm at a 90 degree firing angle.

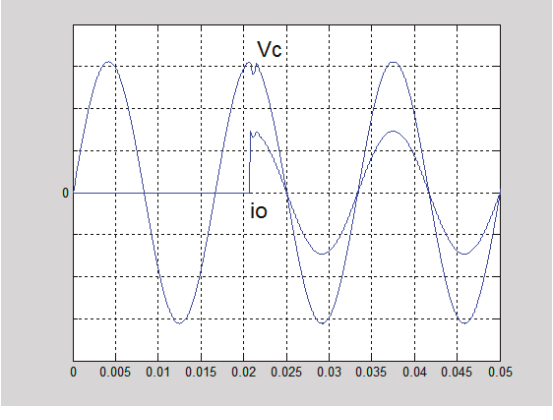

Figure 2. Simulated waveforms under step load change (load suddenly turn on) for the improved technique (50 V/div; 10 A/div).

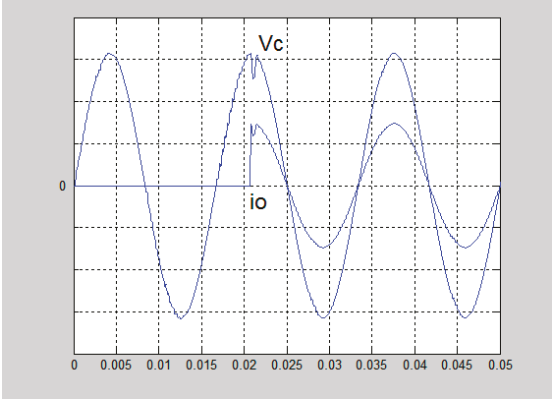

Figure 3. Simulated waveforms under step load change (load suddenly turn on) for the classical TSMC (50 V/div; 10 A/div).

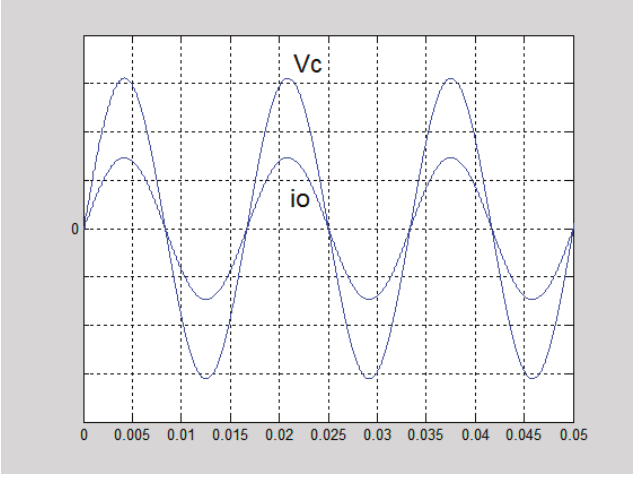

Figure 4. Simulated waveform under LC (inductor capacitor) variation for the improved technique (50 V/div; 10 A/div).

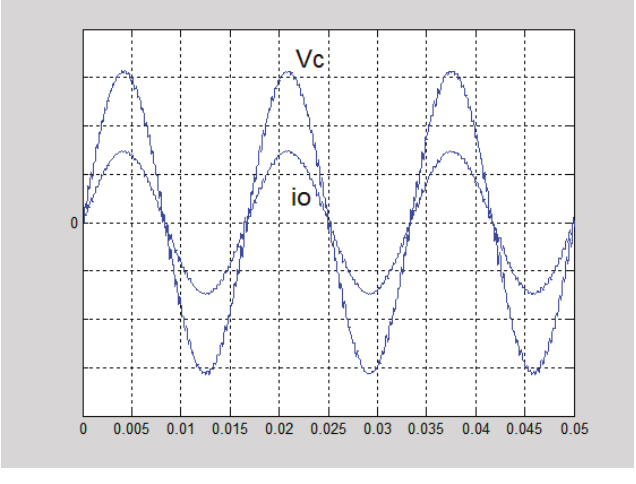

Figure 5. Simulated waveforms under LC variation for the classical terminal sliding mode control (TSMC) (50 V/div; 10 A/div).

Table 1. Simulated output-voltage slump and %THD under step loading and LC variation.

	Simulations	
Improved technique	Step loading (Voltage Slump) LC variation (%THD)	7 V_{rms} 0.23%
Classical TSMC	Step loading (Voltage Slump) LC variation (%THD)	22 V_{rms} 15.98%

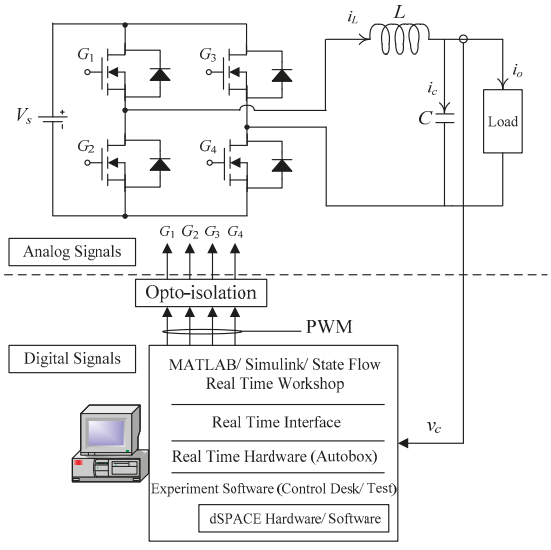

Figure 6. Improved algorithm for DSP (digital signal processing)-based implementation.

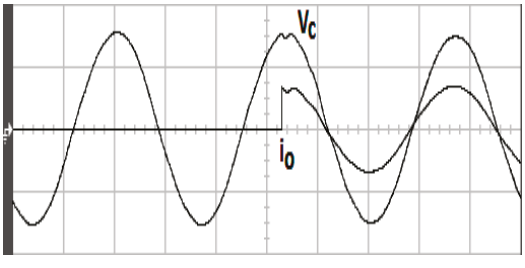

Figure 7. Experimental waveforms under step loading from no load to full load with the improved technique (100 V/div; 20 A/div; 5 ms/div).

After the fast transient response with a voltage slump, the voltage waveform still keeps high tracking precision. Reversely, the experimental waveform obtained using the classical TSMC plotted in Figure 8 appears a large voltage slump and has a slow recovery time. In other words, the output voltage of the improved system due to the action of the BPSO can reach the 110 V_{rms} reference sine wave after the 8 V_{rms} small voltage slump, but the output-voltage slump with the classical TSMC is close to 36 V_{rms}, yielding an unsatisfactory performance in transience. The experimental system performance under the value of filter parameter (L and C) be assumed to undergo a random variation, i.e., 10% ~ 200% of nominal value at a 12 ohm resistive load, is investigated. As can be seen, the output-voltage of the Figure 9 obtained using the improved technique provides the robust ability of greater parameter variation tolerance. However, it is worth noting that a long-time distortion with the sensitivity at the beginning of the waveform exists in the output-voltage with the classical TSMC as shown in Figure 10. Table 2 lists the experimental output-voltage slump and THD values under step load and LC variation.

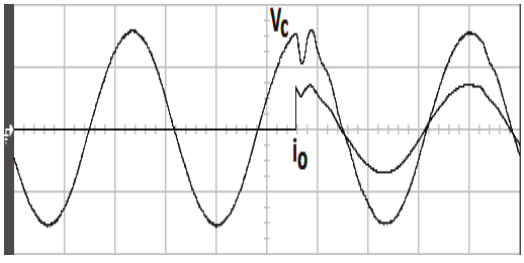

Figure 8. Experimental waveforms under step loading from no load to full load with the classical TSMC (100 V/div; 20 A/div; 5 ms/div).

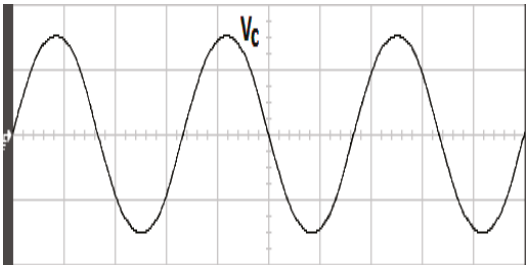

Figure 9. Experimental output-voltage under LC variation with the improved technique (100 V/div; 5 ms/div).

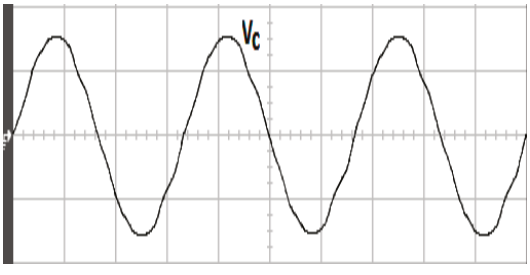

Figure 10. Experimental output-voltage under LC variation with the classical TSMC (100 V/div; 5 ms/div).

Table 2. Experimental output-voltage slump and %THD under step loading and LC variation.

Experiments		
Improved technique	Step loading (Voltage Slump) LC variation (%THD)	8 V_{rms} 0.41%
Classical TSMC	Step loading (Voltage Slump) LC variation (%THD)	36 V_{rms} 11.43%

5. Discussion and Future Research

The improved technique has been proposed for reducing jitter, steady-state error attenuation and greater interference rejection resulting in good system performance. However, in order to advance future research, we have reviewed a large amount of literature on sliding modes, especially in high-order SMC (HOSMC) and adaptive SMC [30–33,38]. The adaptive SMC not only reduces the jitter and steady-state error but also avoids nominal knowledge requirement of the system. The HOSMC

method [44,45] reported on a topic of recent interest in SMC theory. For example, in the rth-order HOSMC, the derivative of the $(r-1)$th control input becomes continuous, and both the sliding plane and its high-order derivative need to be zero. Therefore, the HOSMC retains the original features of the traditional SMC while producing less jitter and better convergence accuracy. The HOSMC method has been used to control DC–AC converter related systems [46–49]. The grid-connected wind energy conversion system is designed by multiple input multiple output HOSMC, so it can adjust active and reactive power, and even develop a switching control scheme based on voltage grid measurement. This approach yields attractive benefits such as robust robustness to system uncertainty, reduced jitter, and finite time convergence of system states to sliding surfaces [46]. A reverse-threshold HOSMC strategy is proposed for grid-connected distributed generation (DG) units. It provides excellent regulation of the inverter output current and provides a perfect sinusoidal balanced current for the grid, resulting in a distributed generator system with good performance against model uncertainties, parameter variations and unmodeled dynamics as well as external disturbances [47]. HOSM observers are effectively introduced into the control design of single-phase DC–AC inverter systems to suppress multiple sources of interference/uncertainty, including parametric perturbations, complex nonlinear dynamics, and external disturbances. Based on the Lyapunov function criterion, the stability of the whole system and the effectiveness of the high-order sliding mode observer are rigorously proved [48]. In addition, an improved HOSM observer is proposed for use in a proton exchange membrane fuel cell system based on excess oxygen ratio, which provides an observation of unmeasurable system conditions. Even under the influence of measurement noise, modeling error, parameter uncertainty and strong external interference, the method still has good robustness and fast convergence, and has limited time stability [49]. As mentioned above, HOSMC produces high-order derivative constraints on the sliding surface while preserving the main advantages of traditional SMC; it is undeniable that HOSMC eliminates jitter effects and produces more accurate control performance. Therefore, HOSMC will promote further research in this area of the DC–AC converter.

6. Conclusions

In this paper, a BPSO optimized NTSMC for a DC–AC converter is described that is capable of producing low THD and fast transients. The importance of the NTSMC is limited system state convergence time and no singularities. Also, the parameters of the NTSMC should be chosen well to obtain optimal performance. These parameters are traditionally determined by a trial and error method, which is very tedious, laborious to implement, and time-consuming. Therefore, the BPSO is used to optimize the NTSMC parameters, yielding better transient and steady-state response. The Lyapunov method is used to analyze the stability of the improved technique. The finite time accessibility of the sliding surface, the asymptotic stability of the closed-loop system and the finite time convergence of the tracking error are proved. Therefore, we believe that the improved technique will contribute to the control design of future artificial intelligence related systems. Simulations and experiments have been developed on prototypes of DC–AC converters using DSP to verify the applicability of the improved technique.

Author Contributions: E.-C.C. conceived, investigated and designed the circuit, and developed the methodology. C.-A.C. and L.-S.Y. prepared software resources, set up simulation software, and E.-C.C. performed circuit simulations. E.-C.C. carried out DC–AC converter prototype, and measured as well as analyzed experimental results. E.-C.C. wrote the paper and revised it for submission.

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Conflicts of Interest: The authors declare no conflicts of interest regarding the publication of this article.

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Flatness-Based Control for the Maximum Power Point Tracking in a Photovoltaic System

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Abstract: Solar energy harvesting using Photovoltaic (PV) systems is one of the most popular sources of renewable energy, however the main drawback of PV systems is their low conversion efficiency. An optimal system operation requires an efficient tracking of the Maximum Power Point (MPP), which represents the maximum energy that can be extracted from the PV panel. This paper presents a novel control approach for the Maximum Power Point Tracking (MPPT) based on the differential flatness property of the Boost converter, which is one of the most used converters in PV systems. The underlying idea of the proposed control approach is to use the classical flatness-based trajectory tracking control where a reference voltage will be defined in terms of the maximum power provided by the PV panel. The effectiveness of the proposed controller is assessed through numerical simulations and experimental tests. The results show that the controller based on differential flatness is capable of converging in less than 0.15 s and, compared with other MPPT techniques, such as Incremental Conductance and Perturb and Observe, it improves the response against sudden changes in load or weather conditions, reducing the ringing in the output of the system. Based on the results, it can be inferred that the new flatness-based controller represents an alternative to improve the MPPT in PV systems, especially when they are subject to sudden load or weather changes.

Keywords: MPPT; differential flatness; nonlinear control

1. Introduction

For many years fossil fuels have been the primary source of energy in the world, however these resources are finite. The threat of climate change due to global warming (caused in part by the burning of fossil fuels) has prompted the search for renewable energy sources such as the sun and the wind. Solar energy is a sustainable, environmentally friendly, and cost-efficient source of energy available around the world, and for this reason solar technologies using photovoltaic (PV) systems have penetrated the electric power production market, with the additional advantages of working quietly and with low maintenance cost. Nonetheless, as it has been remarked by [1], the increment in the use of PV devices in power systems has generated new challenges, such as those related with control strategies looking to provide good, even optimal, operating conditions of the PV systems. Moreover, the control strategies need to cope with the fact that the performance of PV systems depends on solar

irradiance, ambient temperature, and load impedance [2]. As in [1], the approach proposed in this paper is implemented in the open programming environment MATLAB®/Simulink®; nevertheless, the focused problem is the application of a novel control strategy (flatness-based) for the MPPT in PV systems. As mentioned in [3], it is evident that PV components will be essential elements in power electrical systems, where their inclusion considers the MPPT control problem as a strategy that is part of one of the two most important approaches highlighted in literature that corresponds to "the installation and operation of an energy storage system (ESS), while keeping the PVs in the maximum power point tracking (MPPT)..." [3]. To the best knowledge of the authors, no flatness-based control strategies have been reported to cope with the MPPT problem in PV systems. This paper proposes the use of a control strategy based on the differential flatness properties of the PV system model to tackle the MPPT task.

The main drawback of PV systems is their low conversion efficiency. For an optimal operation, it is required for the system to operate at the Maximum Power Point (MPP), which represents the maximum energy that can be extracted from the PV panel. To reach this condition, it is necessary to use Maximum Power Point Tracking (MPPT) systems. A major challenge in PV systems is to handle their non-linear characteristics of current-voltage *I*-*V* relation that generate a unique MPP in the power-voltage relation *P*-*V* [4]. The MPPT process becomes complicated due to the fact that the *P*-*V* relation varies with weather conditions. MPPT methods not only allow an increase in the power delivered by PV systems to the load, but they also give rise to a longer operating life of the system [5].

MPPT algorithms are designed so that the PV system adapts to weather changes in such a way that optimal power is delivered. Typically, these algorithms are integrated into electronic power converter systems where their duty cycle is controlled to deliver the maximum available power to the load [6,7]. Several methods to solve the problem of MPPT have been reported in the literature. Among them are the Perturb and Observe (P&O) method, the Incremental Conductance (IncCond) algorithm, fuzzy logic-based methods, neural networks techniques, and the sliding mode control. The P&O and IncCond are the most popular algorithms to track the MPP [8–13].

The P&O method is inexpensive and relatively simple; its operation is based on periodic measures of the voltage and current of the PV system to calculate the MPP. However, its main disadvantage is that it delivers an oscillatory power around the MPP. Besides, since it is unable to detect if the power variation is caused by weather effects or by inherent perturbations of the algorithm, the P&O method may fail in the presence of abrupt changes of temperature and solar irradiance [14].

The IncCond method is based on the fact that the slope of the *P*-*V* curve of a PV system is zero when the MPP is reached, positive to the left of the MPP and negative to its right. Based on that, the method calculates the MPP by comparing the instantaneous conductance with the incremental conductance to modify the required reference voltage. The main disadvantage of the IncCond method is that the response of the system to reach the MPP under certain conditions can be slow. However, the IncCond technique exhibits less oscillatory behavior around the MPP compared to the P&O method [15].

Fuzzy logic-based methods have demonstrated fast convergence and high performance under varying weather conditions [16–23]. These methods do not require a mathematical model and are able to handle the system nonlinearities. However, the main disadvantage of these controllers is that their effectiveness depends on the error calculation and on the definitions of their base rules for the fuzzy inference mechanism. These definitions must be done by a human expert and the effectiveness of the control relies on them.

Neural network-based algorithms require proper training strategies to effectively track the MPP [24–26]. It is worth mentioning that neural networks must be retrained to be applied to different PV systems since they may have different specifications. Besides this, since the system parameters can be modified over time, it is necessary to periodically train a neural network to ensure its effectiveness. Furthermore, according to [27,28], the implementation of fuzzy logic and neural network algorithms may be complex.

The sliding mode control technique sends an on-off signal to control the operation of the power converter to reach the MPP of the PV system. The commutation function is computed based on the fact that the derivative of the power with respect to the voltage is positive to the left of the MPP, negative to its right, and zero at the MPP. Conventional sliding mode control techniques have limitations such as variable operating frequency and the presence of nonzero steady state error [29].

The use of flatness-based control strategies in the area of power electrical systems has been explored in the last decade, where some works have reported the use of flatness-based controllers for power converters. For instance, authors in [30] use a recursive approach were differential flatness properties are used to synthesize a controller that guarantees closed-loop asymptotic stability of a power converter connected to a DC motor. Two flatness-based controllers are proposed in [31] for a Boost inverter (two DC-DC Boost converters connected in differential mode to a grid) in order to control, individually, each of the two output voltages of the Boost converters. A flatness-based control approach is provided in [32] to achieve the maximum power that is captured by a wind generator driving a permanent magnet synchronous generator whose mathematical model is flat and is connected to a battery bank using an AC-DC converter. A differential flatness-based controller is proposed in [33] to improve the stability of the converters used in a distributed PV-energy storage DC generation system under the presence of parameter disturbances, while an extremum seeking algorithm guarantees the tracking of the MPP under irradiance disturbances. Authors in [30–33] validate their flatness-based control strategies through numerical simulations. Nevertheless, as it has been remarked previously, differential flatness-based methods have not been investigated to deal with the MPPT problem in PV systems.

The main contribution of this paper concerns the use of a novel control strategy to perform the tracking task of the MPP in PV systems. A new methodology that exploits the differential flatness property of the Boost converter allows deriving a MPPT controller for a stand-alone PV system constituted by a PV panel and a Boost power converter with resistive load. The strategy is based on the trajectory tracking flatness-based control approach where a reference voltage is defined in terms of the maximum power provided by the PV panel. Like the mentioned works that have used a flatness approach [30–33], the performance of the control law reported in this paper is validated through numerical simulations. Nevertheless, this paper also reports experimental tests confirming the controller performance.

The proposed approach is shown to be capable of operating under changing conditions of solar irradiance, temperature, and load, even when the variations are abrupt. This is an important feature that an efficient MPPT must have since the presence of clouds or trees, for instance, may degrade the performances of certain controllers. The robustness against load variations (normally related in practice to energy consumption demands) is an important aspect disregarded in most of the existing control techniques. This paper presents also a comparative analysis that shows the benefits of the proposed controller compared to the two most popular methods for the MPPT: P&O and IncCond. The flatness-based controller gives rise to an improved system response regarding the power behavior: before reaching the MPP, less oscillations are shown with the proposed control in contrast to the IncCond, and, once reaching the MPP, unlike the P&O method, no oscillations are exhibited.

This paper is organized as follows: Section 2 presents the mathematical model of the PV system that is used in this study. Section 3 details the design of the differential flatness-based controller to track the MPP. Section 4 presents the numerical simulations to evaluate the effectiveness of the controller under variations of solar irradiance, temperature and load. Besides, a comparative analysis shows the benefits of the proposed controller compared to the P&O and IncCond methods. In Section 5, the performance of the proposed control approach is validated through experimental tests conducted in a prototype of the system. Finally, Section 6 gives some concluding remarks.

2. Photovoltaic System Model

The block diagram of the PV system under consideration is shown in Figure 1. The energy source of the PV system is constituted by a photovoltaic module, the Boost converter acts as interface between the solar panel and the load, and the MPPT controller allows reaching the available maximum power. Notice that the current I_{PV} and the voltage V_{PV} provided by the PV module are used as inputs to the Boost converter and to the MPPT controller which is also fed with the output voltage v of the converter. The average control signal u_{av} generated by the MPPT controller is sent to the converter.

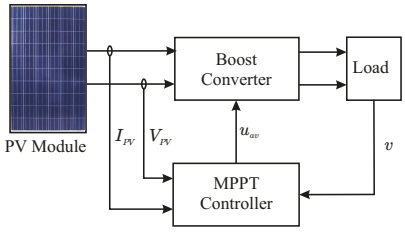


Figure 1. Photovoltaic (PV) system under a Maximum Power Point Tracking (MPPT) controller.

2.1. PV Module Model

A PV module, also known as solar panel, consists of a set of solar cells that are connected in series or in parallel depending on the application for which the PV module is built. If the solar cells are connected in series, the voltage of the PV module is increased while the current keeps constant. Conversely, if a parallel connection is considered, the PV module current is increased while the voltage remains constant.

The equivalent circuit that represents a solar cell is constituted by an energy source that represents the energy generated by the incidence of solar irradiance G which delivers the photogenerated current I_{ph}. This circuit also considers a diode connected in parallel with the energy source, a series resistance R_s that represents the internal resistance to the current flow of the cell and a shunt resistance R_{sh} representing the leakage current (see Figure 2).

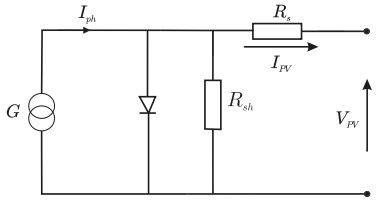


Figure 2. Equivalent circuit of a PV cell.

The equivalent circuit of a PV cell is mathematically described by Equations (1)–(3), where it is assumed that $R_s << R_{sh}$ [34].

$$I_{PV} = I_{ph} - I_o \left[\exp\left(\frac{q\,(V_{PV} + R_s I_{PV})}{K T_c A} \right) - 1 \right] \tag{1}$$

In Equation (1), I_{PV} and V_{PV} denote the output current and voltage of the PV cell, respectively, I_{ph} is the current photogenerated by the solar cell, I_o is the reverse saturation current of the diode, q is the electron charge (1.602×10^{-19} C), R_s is the internal resistance to the current flow of the cell, K is the Boltzmann constant (1.381×10^{-23} J/K), T_c is the temperature of the cell, and A is the diode ideality factor.

The photogenerated current I_{ph} is determined by:

$$I_{ph} = \frac{S}{S_{ref}} \left[I_{SC} + \mu_{SC} \left(T_c - T_{ref} \right) \right] \tag{2}$$

where S is the solar irradiance, S_{ref} is the solar irradiance under reference conditions (1000 W/m^2), I_{SC} is the short-circuit current, μ_{SC} is the coefficient of short-circuit current, and T_{ref} is the reference temperature of the photovoltaic cell [35]. The reverse saturation current I_o is determined by:

$$I_o = I_{o,ref} \left(\frac{T_c}{T_{ref}} \right)^3 \exp \left[\frac{qE_G \left(\frac{1}{T_{ref}} - \frac{1}{T_c} \right)}{AK} \right] \tag{3}$$

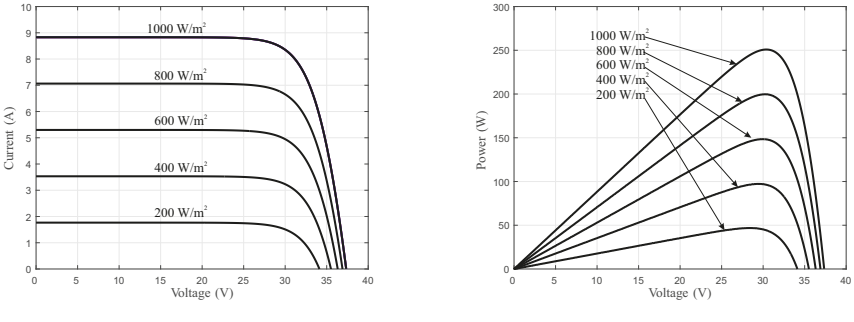
where E_G is the semiconductor energy band used in the solar cell and $I_{o,ref}$ represents the reference reverse saturation current given by:

$$I_{o,ref} = \frac{I_{SC}}{\exp \left(\frac{V_{OC}}{N_s K T_c A} \right) - 1} \tag{4}$$

where N_s is the number of cells connected in series and V_{OC} is the open circuit voltage [35]. In view of Equation (1), the current provided by a PV module is given by:

$$I_{PV} = N_p I_{ph} - N_p I_o \left[\exp \left(\frac{q \left(\frac{V_{PV}}{N_s} + \frac{R_s I_{PV}}{N_p} \right)}{K T_c A} \right) - 1 \right] \tag{5}$$

where N_p is the number of cells connected in parallel [36]. The characteristics of the PV module Renesola Virtus II JC250M-24/Bb, used in this research work, are plotted in Figures 3a,b and 4. Figure 3a shows the *I-V* curves for different values of solar irradiance considering a constant temperature of 25 °C, Figure 3b shows the *P-V* curves for different values of solar irradiance considering a constant temperature of 25 °C, and Figure 4 shows the *I-V* curves considering different temperature values and a solar irradiance of 1000 W/m^2. Notice that the voltage is most likely to be influenced by temperature variations, and the current by solar irradiance changes. As illustrated in Figures 3a,b and 4, high solar irradiance values increase the current, and high temperatures reduce the output voltage of a PV panel. Then, the power conversion capability can be affected under conditions of high temperature and low solar irradiance.



(**a**) *I-V* curves. (**b**) *P-V* curves.

Figure 3. Curves of the PV panel Virtus II JC250M-24/Bb under different irradiance levels and a constant temperature of 25 °C.

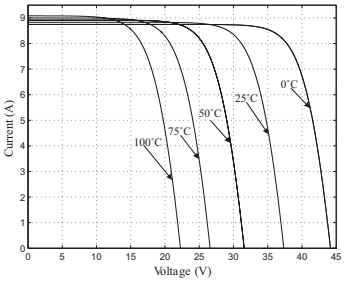


Figure 4. *I-V* curves of the PV panel Virtus II JC250M-24/Bb under different temperature levels and a constant irradiance of 1000 W/m^2.

2.2. Boost Converter Model

A Boost converter is a DC-DC power converter that increases the voltage from its input source to its output. Figure 5 shows the electronic diagram of a Boost power converter in which the input source is the voltage supplied by a photovoltaic panel. This circuit is constituted by a capacitance C, a load resistance R, and an inductance L. The current across the inductor is denoted by i and the output at the capacitor terminals by v. Note that i is assumed to be equal to the PV current I_{PV}.

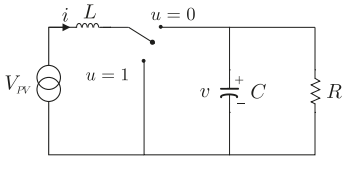


Figure 5. Block diagram of a Boost converter.

Note that the Boost converter includes a switching function u that commutes between two operation modes. When $u = 1$ there is no connection between the voltage source V_{PV} and the system load R. In this case, the system dynamics is described by Equations (6).

$$\begin{aligned} \frac{dv}{dt} &= -\frac{v}{RC} \\ \frac{di}{dt} &= \frac{V_{PV}}{L} \end{aligned} \tag{6}$$

When $u = 0$, there is energy transmission between the power supply and the load, then the system dynamics is described by Equations (7).

$$\begin{aligned} \frac{dv}{dt} &= \frac{i}{C} - \frac{v}{RC} \\ \frac{di}{dt} &= -\frac{v}{L} + \frac{V_{PV}}{L} \end{aligned} \tag{7}$$

Equations (6) and (7) can be unified into the bilinear system defined by Equations (8),

$$\begin{aligned} \frac{dv}{dt} &= \frac{i}{C}(1-u) - \frac{v}{RC} \\ \frac{di}{dt} &= -\frac{v}{L}(1-u) + \frac{V_{PV}}{L} \end{aligned} \tag{8}$$

where i is the inductor current, v is the output voltage, and V_{PV} is the power supply voltage. The control input u represents the switch position function which takes a binary value $u \in \{0,1\}$.

In order to design a control law for the Boost converter, an *average model* must be defined. The *average model* of the Boost converter is represented by the same Equations (8), but the control variable u is redefined as a sufficiently smooth function u_{av} taking values in the real interval [0, 1]. Then, the model given in Equations (8) is referred to as *average model* replacing the switched control input $u \in \{0, 1\}$ by the average control input $u_{av} \in [0, 1]$.

The steady state value of the current $\bar{i}$, for constant values of the input, can be obtained in a parameterized form in terms of the corresponding output voltage equilibrium value $\bar{v}$ as follows:

$$\bar{i} = \frac{\bar{v}^2}{RV_{PV}} \tag{9}$$

3. Flatness-Based Control Design

In nonlinear systems theory, the flatness property is due to the ability of dynamic systems to support an accurate linearization through endogenous feedback. A system that satisfies the flatness property is named a differentially flat system. The main attribute of flat systems is that state and input variables can be expressed directly (without the integration of a differential equation) in terms of a particular set of variables called flat outputs (or linearizing outputs) and a finite number of their derivatives [37]. This section presents the main contribution of this paper which is the development of a controller based on the differential flatness property of the Boost converter for the MPPT of a PV system.

The flatness property of the Boost converter has been established in [38]. A flat output F can be determined by the total energy stored in the system, that is

$$F = \frac{1}{2}\left(Li^2 + Cv^2\right) \tag{10}$$

Using Equations (8), the differential parametrization of the states and the input of the Boost converter are obtained as follows:

$$i = -\frac{RCV_{PV}}{2L} + \beta \tag{11}$$

$$v = \sqrt{\frac{2}{C}F - \frac{L}{C}\left(-\frac{RCV_{PV}}{2L} + \beta\right)} \tag{12}$$

$$u_{av} = 1 - \frac{i\dot{V}_{PV} + \frac{1}{L}V_{PV}^2 + \frac{2}{R^2C}v^2 - \ddot{F}}{\left(\frac{1}{L}V_{PV} + \frac{2}{RC}i\right)v} \tag{13}$$

$$\beta = \frac{1}{2}\sqrt{\left(\frac{RCV_{PV}}{L}\right)^2 + \frac{4}{L}\left(RC\dot{F} + 2F\right)} \tag{14}$$

The derivation of Equations (11)–(14) is presented in Appendix A. Note that the model defined by Equations (8) is represented by the differential parameterization given by Equations (11)–(14) stated in terms of the flat output F and its time derivatives $\dot{F}$ and $\ddot{F}$. In Equation (13), $\dot{V}_{PV}$ is the time derivative of the output voltage of the PV cell.

The underlying idea of the proposed control approach for the MPPT is to use the classical flatness-based trajectory tracking control but instead of predefine a reference path, a reference voltage v^* will be obtained from the maximum power provided by the PV panel. From this reference voltage, using Equation (10), a reference flat output F^* is constructed. The controller is designed to track the reference signal F^* with a guaranteed convergence of the error to zero. As shown below, this ensures an efficient tracking of the MPP.

The control design is explained as follows. To obtain the reference voltage corresponding to the maximum power provided by the PV panel, the power delivered by the Boost converter P_C must match the power supplied by the PV panel P_{PV}, i.e,

$$P_C = P_{PV} \tag{15}$$

Note that, for a pure resistive load, P_C can be written in terms of the output voltage v and the load resistance R, and P_{PV} can be expressed in terms of I_{PV} and V_{PV}, as shown in Equation (16).

$$P_C = \frac{v^2}{R}, \qquad P_{PV} = V_{PV} I_{PV} \tag{16}$$

Then, in view of Equations (15) and (16), the reference voltage v^* that the controller must take into account to guarantee the tracking of the MPP is given by,

$$v^* = \sqrt{V_{PV} I_{PV} R} \tag{17}$$

In order to steer the converter output voltage v to the reference voltage v^* defined in Equation (17), the control must force the flat output F to follow the reference flat output F^* calculated as:

$$F^* = \frac{1}{2}\left(L\left(\frac{v^{*2}}{R V_{PV}} \right)^2 + C v^{*2} \right) \tag{18}$$

In order to establish the closed-loop dynamics, in Equation (13), the highest order derivative of the flat output is replaced by an auxiliary input $\mu_{aux} = \ddot{F}$. Regarding the tracking problem under consideration, the error is defined as $e = F - F^*$. To guarantee stable closed-loop error dynamics, the auxiliary input μ_{aux} can be defined as:

$$\mu_{aux} = \ddot{F}^* - \beta_1(\dot{F} - \dot{F}^*) - \beta_0(F - F^*) \tag{19}$$

with $\beta_0 > 0$ and $\beta_1 > 0$ are constant gains to be determined. Equation (19) allows one to define the error dynamics as:

$$\ddot{e} + \beta_1 \dot{e} + \beta_0 e = 0 \tag{20}$$

which is associated with the characteristic polynomial,

$$p(s) = s^2 + \beta_1 s + \beta_0 \tag{21}$$

For the sake of convenience, the characteristic polynomial can be written in terms of the damping factor ζ and the natural frequency ω_n as follows,

$$p(s) = s^2 + 2\zeta\omega_n s + \omega_n^2 \tag{22}$$

where $\omega_n > 0$ and $\zeta > 0$. Notice that β_1 and β_0 are determined by

$$\beta_1 = 2\zeta\omega_n, \qquad \beta_0 = \omega_n^2 \tag{23}$$

The error will asymptotically converge to zero if the gains of the feedback tracking controller are chosen such that the roots of the characteristic polynomial defined in Equation (21) lie in the left half complex plane. The constants β_1 and β_0 must be chosen accordingly. In view of the parametrization of the control input given in Equation (13) and the auxiliary input dynamics defined in Equation (19),

the flatness-based controller that ensures the tracking of the MPP with an asymptotic convergence of the error to zero is given by

$$u_{av} = 1 - \frac{i^* \dot{V}_{PV} + \frac{1}{L} V_{PV}^2 + \frac{2}{R^2 C} (v^*)^2 - \mu_{aux}}{\left(\frac{1}{L} V_{PV} + \frac{2}{RC} i^* \right) v^*} \tag{24}$$

where i^* is obtained from Equation (11) where β is given in terms of F^* and $\dot{F}^*$. As it was previously described, the switching function of the Boost converter is able to take binary values, then, the average control law defined in Equation (24) cannot be directly implemented. As usual practice in this scenario, a Pulse Width Modulation (PWM) has been used for which the average control u_{av} acts as a modulation signal. Figure 6 presents a schematic diagram illustrating the control system implementation.

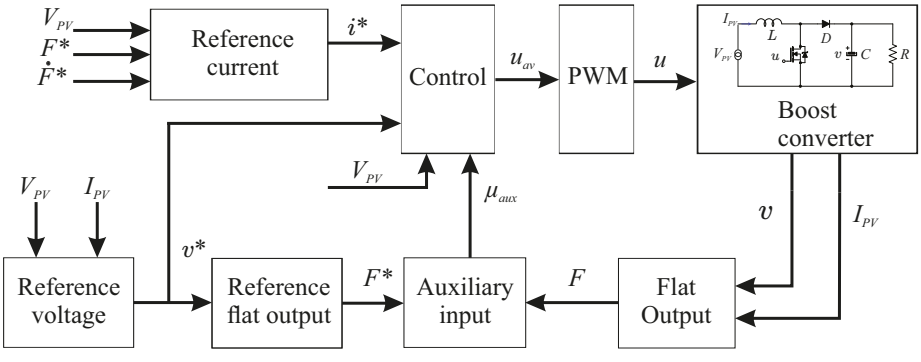


Figure 6. MPPT system block diagram.

4. Simulation Results

In this section the performance of the proposed control approach is evaluated through numerical simulations. The PV system consisting of a photovoltaic module, a Boost converter, a load resistance, and the flatness-based controller is implemented in the MATLAB®/Simulink®environment (R2015a, The MathWorks, Inc, Natick, MA, USA). Table 1 shows the characteristics of the Virtus II photovoltaic module (JC250M-24/Bb, ReneSola, Shanghai, China) used for this experimental setting.

Table 1. Virtus II Electrical characteristics.

Parameters	Value
Maximum Power (P_{MAX})	250 W
Current at Maximum Power (I_{MP})	8.31 A
Voltage at Maximum Power (V_{MP})	30.1 V
Short-Circuit Current (I_{SC})	8.83 A
Open-Circuit Voltage (V_{OC})	37.4 V

Table 2 presents the parameters of the Boost power converter and the proposed values of the natural frequency and the damping factor for the flatness-based controller. Notice that with the proposed values of damping ζ and natural frequency ω_n, the controller gains are β_0 = 90,000 and $\beta_1 = 60$. Then, the roots of the characteristic polynomial given in Equation (21) are $s_1 = -30 + 2.985\text{j}$ and $s_2 = -30 - 2.985\text{j}$. Since the roots lie on the left side of the complex plane, the stability of the error dynamics is ensured, i.e., the error $e = F - F^*$ asymptotically converges to zero as $t \to \infty$.

Table 2. Boost converter parameters.

Parameters	Value
Capacitance C	470 μF
Resistance R	12 Ω
PWM operation frequency	45 kHz
Inductance L	10 mH
Natural frequency ω_n	300
Damping factor ζ	0.1

Through simulations, the robustness of the differential flatness-based controller under variations of the solar irradiance, temperature and load is evaluated. To develop such evaluation, four study cases were considered:

Case 1. At 1.1 s, the solar irradiance is increased from 500 W/m^2 to 1000 W/m^2 within a time interval of 0.1 s. A constant temperature of 25 °C is considered (see Figure 7c).

Case 2. At 0.8 s, the temperature is increased from 15 °C to 25 °C within a time interval of 0.1 s. A constant solar irradiance of 800 W/m^2 is considered (see Figure 8c).

Case 3. Considering a constant temperature of 25 °C, at 0.6 s, the solar irradiance is decreased from 1000 W/m^2 to 500 W/m^2 within a time interval of 0.5 s. Then, at 1.2 s, the solar irradiance is increased from 500 W/m^2 to 1000 W/m^2 within a time interval of 0.5 s. In a different time instant (at 2 s), the temperature increases from 25 °C to 40 °C within a time interval of 0.1 s (see Figure 9c).

Case 4. A solar irradiance of 1000 W/m^2 and a temperature of 25 °C are kept constant while the load instantly decreases from 12 Ω to 6 Ω at 0.5 s (see Figure 10c).

In the first three cases, a constant load of 12 Ω is considered.

Note that the proposed time scales are short (tests were performed within time intervals less than 3 s). This aims at demonstrating the strength of the proposed approach for the MPPT, i.e., to evaluate the performance of the flatness-based control law against sudden variations of weather conditions. Clearly, if the controller is efficient in tracking the MPP in spite of the abrupt changes considered in the study cases described above, it will also have a satisfactory performance under realistic operating conditions involving smoother variations of solar irradiance and of temperature, occurring within longer time intervals.

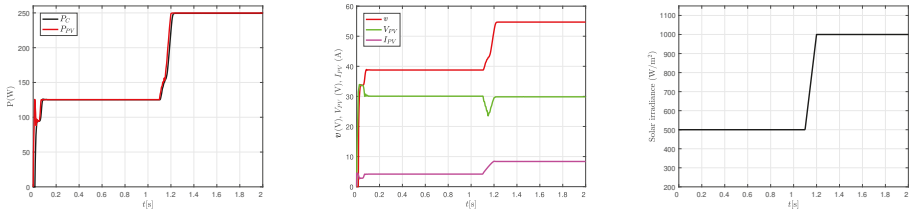
Figures 7–10 illustrate the performance of the proposed control approach under the conditions stated above. Table 3 presents the theoretical maximum power for the different values of temperature and solar irradiance considered in the four study cases. It is important to mention that, theoretically, load variations do not affect the maximum power.

Table 3. Theoretical maximum power.

Solar Radiation (W/m^2)	Temperature (°C)	P_{MAX} (W)
500	25	125
510	23	118
800	25	200
800	15	210
900	45	203
1000	25	250
1000	40	232

The trajectories generated under the conditions described in **Case 1** are depicted in Figure 7. The output power of the Boost converter and the power delivered by the PV panel are shown in Figure 7a. The output voltage of the converter and the current and voltage of the PV panel are presented in Figure 7b. Figure 7c shows the variation of the solar irradiance. Note that the theoretical values of the maximum power for a constant temperature of 25 °C are reached: 125 W for a solar irradiance of 500 W/m^2, and 250 W for 1000 W/m^2. Observe that, as expected, during the time period

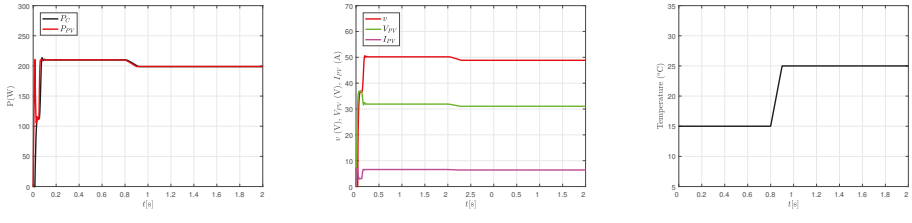
in which the solar irradiance increase takes place (from 1.1 s to 1.2 s), an increment of the current of the PV panel occurs. However, the voltage V_{PV} is kept at a constant value (except for the variation observed within the time lapse in which the solar irradiance variation occurs).



(**a**) (**b**) (**c**)

Figure 7. Simulation results under a variation of solar irradiance (under a constant temperature of 25 °C). Case 1. (**a**) Power of the PV panel (P_{PV}) and output power of the converter (P_C); (**b**) Voltage of the converter (v), voltage and current of the PV panel (V_{PV}, I_{PV}); (**c**) Solar irradiance variation.

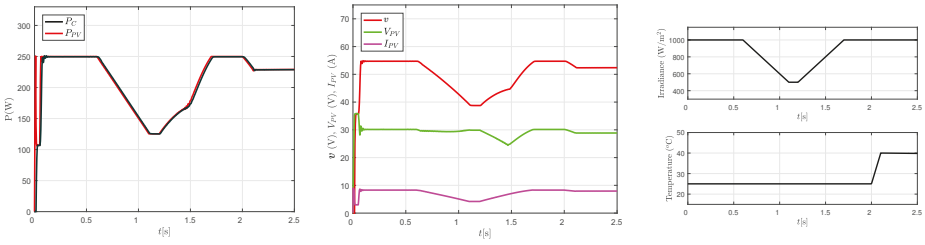
The system response obtained by considering the conditions stated in **Case 2** is illustrated in Figure 8. Figure 8a depicts the Boost converter output power as well as the power delivered by the PV panel. Figure 8b shows the output voltage of the converter and the current and voltage provided by the PV panel. The variation of temperature is presented in Figure 8c. In this case, an increase of temperature occurs from 0.8 s to 0.9 s. In this period of time, the power values are decreased from 210 W/m^2 to 200 W/m^2. These values are in accordance with the theoretical maximum power that can be achieved (see Table 3). As expected, the current of the PV module remains constant and the value of V_{PV} decreases.



(**a**) (**b**) (**c**)

Figure 8. Simulation results under a variation of temperature (under a constant solar irradiance of 800 W/m^2). Case 2. (**a**) Power of the PV panel (P_{PV}) and output power of the converter (P_C); (**b**) Voltage of the converter (v), voltage and current of the PV panel (V_{PV}, I_{PV}); (**c**) Temperature variation.

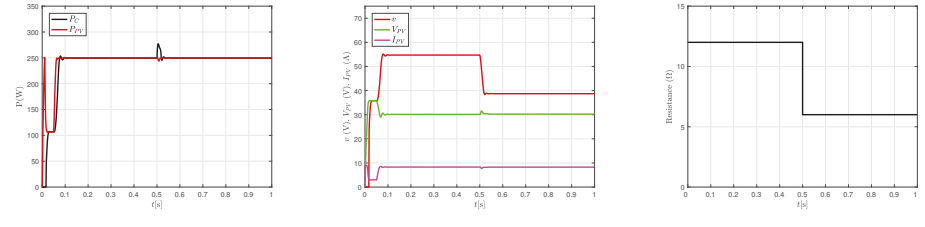
The controller performance under the conditions described in **Case 3** is illustrated in Figure 9. Figure 9a presents the output power of the Boost converter and the power delivered by the PV panel. Figure 9b shows the trajectories of the converter output voltage as well as the voltage and current values delivered by the PV panel. Figure 9c illustrates the solar irradiance and temperature variations. It is obvious that when a decrease of solar irradiance occurs, the power provided by the PV panel P_{PV} and the current I_{PV} also decrease meanwhile the voltage V_{PV} does not vary significantly. Conversely, when solar irradiance increases, the power provided by the PV panel P_{PV} and the current I_{PV} are also incremented meanwhile the voltage V_{PV} undergoes variations but after a short period of time it reaches the previous value again. The temperature increase leads to a slight reduction of the voltage V_{PV} and a decrease of the power P_{PV} meanwhile the current I_{PV} remains almost unchanged. Notice that in all cases the theoretical maximum value of the power provided by the PV panel is achieved (see Table 3).



(**a**) (**b**) (**c**)

Figure 9. Simulation results under solar irradiance and temperature variations. Case 3. (**a**) Power of the PV panel (P_{PV}) and output power of the converter (P_C); (**b**) Voltage of the converter (v), voltage and current of the PV panel (V_{PV}, I_{PV}); (**c**) Solar irradiance and temperature variations.

The controller performance under the conditions described in **Case 4** is illustrated in Figure 10. Figure 10a shows the output power of the Boost converter and the power delivered by the PV panel. Figure 10b shows the trajectories of the converter output voltage as well as the voltage and current values delivered by the PV panel. Figure 10c illustrates the load variation. Note that the load is diminished at 0.5 s leading to minor variations of the signals coming from the PV panel P_{PV}, I_{PV}, and V_{PV}. However, the output voltage of the Boost converter v is significantly decreased. It is noteworthy that variations of the load do not prevent the proposed algorithm from successfully tracking the maximum power.



(**a**) (**b**) (**c**)

Figure 10. Simulation results under a load variation. Case 4. (**a**) Power of the PV panel (P_{PV}) and output power of the converter (P_C); (**b**) Voltage of the converter (v), voltage and current of the PV panel (V_{PV}, I_{PV}); (**c**) Load variation.

Simulation results highlight the performance of the proposed control approach. **Case 1** is defined to demonstrate the robustness of the control law against solar irradiance abrupt changes; **Case 2** aims to show the controller performance under a sudden variation of temperature; **Case 3** allows evaluating the performance of the controller under abrupt variations of solar irradiance and temperature; finally, **Case 4** considers the transit from a lightly loaded system to a heavily loaded one.

Simulation results show that the proposed control scheme is robust against variations of external conditions and that the corresponding values of maximum power are reached in all cases. From Figures 7–10, it can be noticed that the control action takes about 0.1 s to be reflected in the system trajectories and that the system reaches the steady state in a very short period of time regardless the variation of weather conditions and load. This stabilization time can be considered acceptable since most of the PV applications do not require a faster response.

As can be seen, the sudden variations of temperature, solar irradiance and load do not degrade the performance of the flatness-based controller. It can be concluded that the flatness-based controller is effective in maintaining the output power of the PV panel at the corresponding optimum values. Furthermore, it is robust against variations of external conditions and operates under low or high temperatures.

Comparative Analysis

In order to determine the benefits that the proposed control scheme offers in contrast to the most popular MPPT techniques: Perturb and Observe (P&O) and Incremental Conductance (IncCond), numerical simulations were performed. Under the conditions stated in **Case 3**, the conventional P&O method (see for instance [12]) and the IncCond with integral regulator (IncCond+IR) algorithm proposed in [39] were evaluated. Figure 11 shows the performance of these three techniques; $P_{P\&O}$ corresponds to the power obtained with the P&O method, P_{FBC} is the power obtained with the flatness-based control technique proposed in this paper, and $P_{IncCond+IR}$ is the power obtained with the IncCond+IR algorithm.

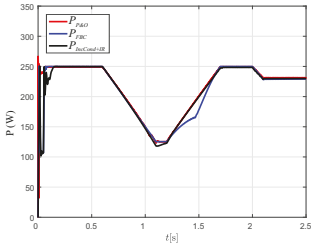
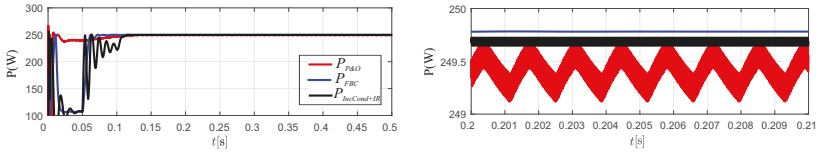


Figure 11. Comparison of three techniques for the MPPT. Simulation results under conditions stated in **Case 3**. Red line: power obtained with the Perturb and Observe (P&O) method. Blue line: power obtained with the flatness-based controller. Black line: power obtained with the IncCond+IR algorithm.

Note that within the time interval where the solar irradiance increase occurs (between 1.2 s and 1.7 s), the response produced with the flatness-based approach differs from the ones produced with the other techniques. However, the theoretical power is reached when the solar irradiance is set at 1000 W/m^2.

At first glance, it might seem that the three methods have almost the same performance, however, a zoom of Figure 11 shows that, although the time to reach the MPP is almost equal (about 0.13 s), the response obtained with the IncCond+IR method exhibits oscillations of significant magnitude before reaching the MPP (see Figure 12a), and that, as expected, the response produced with the P&O technique presents small amplitude oscillations around the MPP (see Figure 12b).



(**a**) (**b**)

Figure 12. Zoom of Figure 11. (**a**) Zoom of Figure 11 between 0 and 0.5 s; (**b**) Zoom of Figure 11 between 0.2 and 0.21 s.

In view of the simulation results, it can be concluded that one important advantage of the proposed approach is that less oscillations are produced before reaching the MPP compared to the IncCond+IR method. Furthermore, the flatness-based method does not give rise to oscillations around the MPP, like the ones observed for the P&O technique.

Another disadvantage of the P&O technique is that its accuracy depends on the perturbation size: if it is small, the method takes more time to reach the MPP, if it is big, the amplitude of the oscillations around the MPP increases [26]. This does not occur with the proposed flatness-based method.

5. Experimental Results

Experimental results obtained with a PV panel Virtus II model JC250M-24/Bb show the performance of the flatness-based controller under realistic scenarios. For the implementation of this MPPT controller, a Boost power converter is designed to operate in continuous mode at a switching frequency of 45 kHz; the parameter values used in the experimental set up are shown in Table 2.

The MPPT flatness-based control algorithm was implemented with the Simulink Real-Time® software (R2015a, The MathWorks, Inc, Natick, MA, USA) using a Humusoft® MF 624 multifunction I/O card (MF624, Humusoft Ltd., Prague, Czechia) that is installed on a computer with an Intel® Core™ processor (i7-2600, 3.40 GHz, Intel, Santa Clara, CA, USA) and 8GB RAM memory (DDR3 1333 MHz, Hynix, Incheon, Korea). The complete scheme operates at a fixed sampling frequency of 10 kHz. A PWM generator set to a frequency of 45 kHz is employed. Four analog inputs are used to sense the current I_{PV} and voltage V_{PV} of the PV panel, the output voltage of the converter v, and the current through the load resistor i_R, which allows monitoring possible variations of the load. The control system can be described as follows. The input signals I_{PV} and V_{PV} are acquired by sensors S22P (current) and AMC1100 (voltage) respectively. The average control signal u_{av} adjusts the duty cycle of the PWM generator which activates the MOSFET 19NF20 through the optocoupler circuit IX3180. The auxiliary input μ_{aux} defined in Equation (19) is generated with the use of the reference signal F^* (derived from the output voltage reference) and the flat output F. The Vantage Pro2^{TM} weather station is used to measure solar radiation; it is remotely connected with an indicator console. The experimental configuration diagram, the nominal values of the components, and the information of electronic devices and sensors are shown in Figure 13.

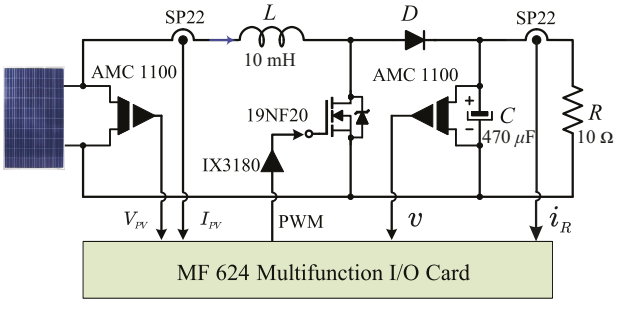
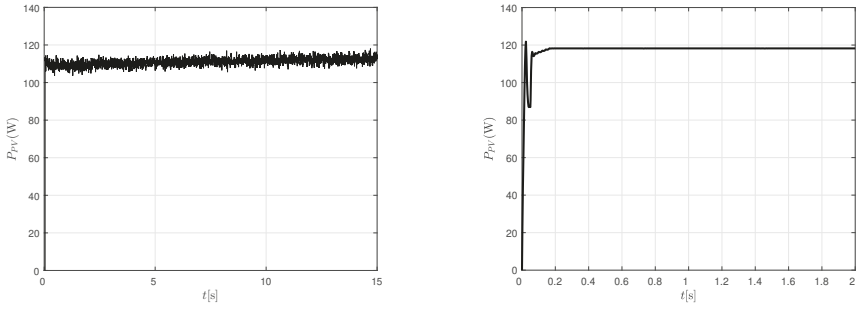


Figure 13. General scheme of a experimental setup of MPPT.

It is important to mention that the true MPP is unknown during a real-time test under natural sunlight. This is because the temperature cannot be accurately measured since PV panels have a multicell distribution and an insulated laminated structure [40].

During the development of experiments, temperature differences of more than 5 °C were found in different sections of the PV panel. Higher temperatures were identified near to the edges of the PV panel due to the heating generated by its laminated structure. To cope with this, approximate values of the panel temperature were calculated from the average of the measured temperatures. Based on these values, the corresponding values of the theoretical maximum power were obtained.

The first experimental test was carried out when a solar irradiance of 510 W/m^2 was measured and an average temperature of 35 °C was calculated. Figure 14 shows the closed-loop response of the system under these conditions. Figure 14a corresponds to the experimental result and Figure 14b to the simulation response.

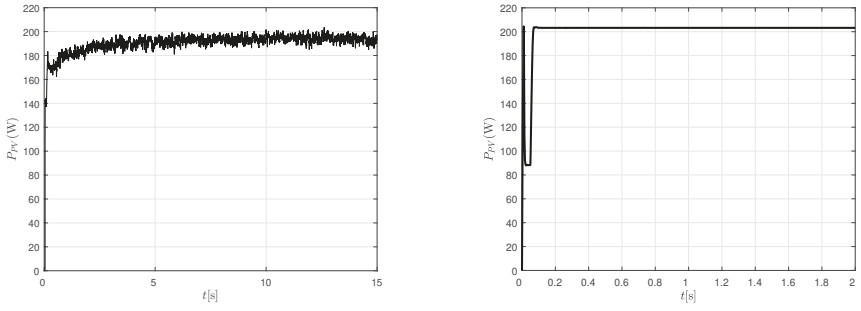


(**a**) Experimental result. (**b**) Simulation result.

Figure 14. System response under a solar irradiance of 510 W/m^2 and an average temperature of 35 °C. Power of the PV panel (P_{PV}).

The second test was conducted under a solar irradiance of 900 W/m^2 and an average temperature of 45 °C. The system response is shown in Figure 15. Figure 15a corresponds to the experimental result and Figure 15b to the simulation response.

Notice that, in simulation, the theoretical maximum powers are reached (118 W for the first case, 203 W for the second one, see Table 3), meanwhile the powers obtained with the experimental tests are below these values (around 110 W for the first case, around 190 W for the second one). As explained before, these differences between the power values are due to the fact that it is impossible to estimate precisely the true MPP value based on the weather conditions because of the complexity of module lamination and measurement accuracy [40]. Besides, there are power losses in the connection cable between the photovoltaic module and the converter that should be considered. In [41], it is shown that the theoretical MPP values can be either higher or lower than the practical measured tracking values. Despite this, from Figures 14a and 15a it can be inferred that the flatness-based controller allows delivering all the available power to the load.



(**a**) Experimental result. (**b**) Simulation result.

Figure 15. System response under a solar irradiance of 900 W/m^2 and an average temperature of 45 °C. Power of the PV panel (P_{PV}).

6. Conclusions

In this paper a novel control strategy for the MPPT was presented. The differential flatness-based property of the Boost converter is exploited to design a controller that allows an effective tracking of the MPP. Numerical simulations were performed in MATLAB® /Simulink® to assess the effectiveness of the flatness-based control law against sudden variations of weather conditions and load considered

in four study cases. For all of them, the theoretical maximum power was reached; it can be concluded that the sudden variations of temperature, solar irradiance, and load do not degrade the performance of the proposed MPPT technique. Furthermore, it was shown that the flatness-based technique has some advantages compared to the P&O method and to the IncCond algorithm related to the PV system response. Simulation results show that the oscillatory behavior around the MPP is avoided with the proposed approach.

Experimental tests were conducted in a prototype of the system consisting of a PV panel Virtus II JC250M-24/Bb. It was noticed that, during the real-time tests, the temperature is not uniform on the PV panel surface. Differences of more than 5 °C were found in different sections of the PV panel. As a result, the theoretical MPP is unknown. Despite this, from the experimental results, it can be inferred that the flatness-based controller allows delivering all the available power from the PV panel to the load. In fact, the power experimentally obtained is close to the theoretical maximum power calculated from average values of the panel temperature.

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Appendix A

This section presents the parametrization of the states and control input of the Boost converter model derived from the flat output. Consider the flat output given by

$$F = \frac{1}{2}\left(Li^2 + Cv^2\right) \tag{A1}$$

Its time derivative is:

$$\dot{F} = Li\frac{di}{dt} + Cv\frac{dv}{dt} \tag{A2}$$

substituting the system dynamics defined by Equations (8) yields,

$$\begin{aligned} \dot{F} &= i[-v\mathbf{u} + V_{PV}] + v[i\mathbf{u} - \frac{v}{R}] \\ \dot{F} &= iV_{PV} - \frac{v^2}{R} \end{aligned} \tag{A3}$$

where:

$$\mathbf{u} = 1 - u_{av} \tag{A4}$$

The parametrization of i is obtained by substituting v^2 (that can be derived from Equation (A3)) into Equation (A1),

$$i = -\frac{RCV_{PV}}{2L} + \beta \tag{A5}$$

where:

$$\beta = \frac{1}{2}\sqrt{\left(\frac{RCV_{PV}}{L}\right)^2 + \frac{4}{L}\left(RC\dot{F} + 2F\right)} \tag{A6}$$

From Equation (A1), one obtains:

$$v = \sqrt{\frac{2F - Li^2}{C}} \tag{A7}$$

substituting Equation (A5) into Equation (A7) yields the parametrization of v, which is obtained as follows:

$$v = \sqrt{\frac{2}{C}F - \frac{L}{C}\left(-\frac{RCV_{PV}}{2L} + \beta\right)^2} \tag{A8}$$

The second derivative of F is:

$$\ddot{F} = i\dot{V}_{PV} + V_{PV}\frac{di}{dt} - \frac{2v}{R}\frac{dv}{dt} \tag{A9}$$

Substituting the system dynamics defined by Equations (8) into Equation (A9) yields the parametrization of the average control as follows:

$$u_{av} = 1 - \frac{i\dot{V}_{PV} + \frac{1}{L}V_{PV}^2 + \frac{2}{R^2C}v^2 - \ddot{F}}{\left(\frac{1}{L}V_{PV} + \frac{2}{RC}i\right)v} \tag{A10}$$

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A New Adaptive Approach to Control Circulating and Output Current of Modular Multilevel Converter

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Abstract: This paper addresses the output current and circulating current control of the modular multi-level converter (MMC). The challenging task of MMCs is the control of output current and circulating current. Existing control structures for output and circulating current achieve control objectives with comparatively complex controllers and the designed parameters for the controller is also difficult. In this paper, an adaptive proportional integral (API) controller is designed to control the output current and the circulating current. The output current is regulated in $\alpha\beta$ axes while the circulating current is regulated in the *abc* stationary frame to enhance MMC performance. The output and circulating current control results using an API controller are compared with the conventional proportional resonant (PR) controller in terms of transient response, stability, optimal performance, and reference tracking for results verification. The API control architecture significantly improve transient response, stability, and have excellent reference tracking capability. Moreover, it controls output current and converges the circulating current to a desired value. The control structure is designed for a three-phase MMC system, simulated and analyzed in MATLAB-Simulink.

Keywords: circulating current; fuzzy; proportional integral; proportional resonant; MMC

1. Introduction

The MMC is becoming an increasingly attractive, competitive, and highly applied technology for medium and high voltage power applications due to its advantages, such as low harmonics, modular structure, simple scaling, loss reduction in switches, and satisfactory fault management [1–3]. Currently, MMCs have been expanded to many applications [4] such as motor drivers [5], solar/wind power systems [6–8], energy transmission and distribution systems [9], and static synchronous compensators (STATCOM) [10]. Recently published literature related to MMC targeted current control, voltage control, loss analysis and modulation, dynamic and steady-state models, modeling, and simulation methods [11–16].

The first structure of the MMC was presented in [17]. Currently, many configurations and control designed approaches have been introduced by many researchers for the control objectives, such as balancing and averaging of SM capacitor voltage, circulating current ripples injection or suppression, and output voltage regulation [18–22]. Figure 1 shows the configuration of a three-phase six arm MMC.

Every arm of the MMC is equipped with a series connected sub module (SM) configuration. The SM, consists of two switches connected with a capacitor, is also depicted in Figure 1.

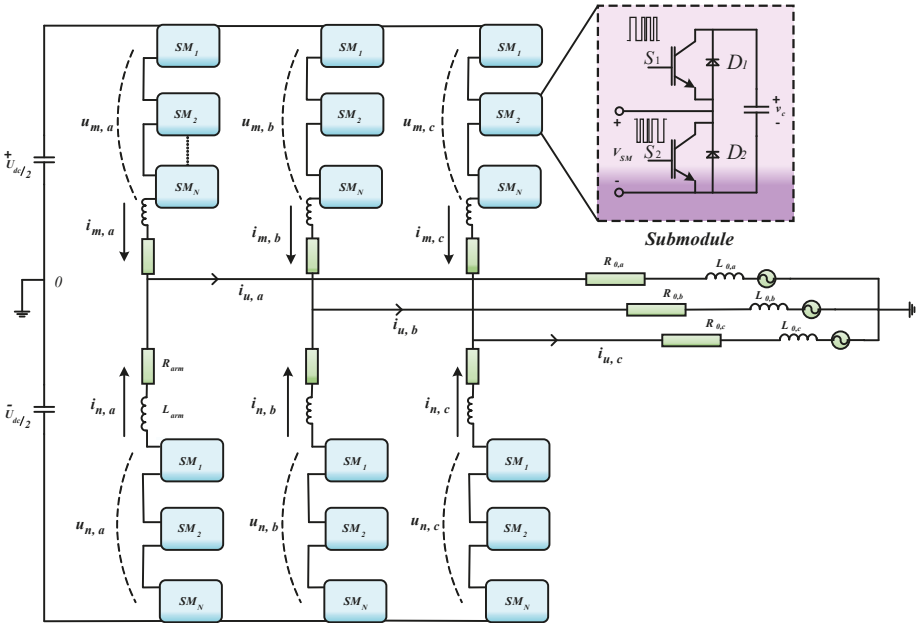


Figure 1. General MMC 3 phase structure.

For the optimal performance of MMC, the control system plays a vital role. The output current is controlled to transfer the power to AC grid while the circulating current does not affect the output of the converter. However, uncontrolled circulating current results in higher losses. The circulating current problem in each arm of MMC arises due to potential differences in every SM arm and DC link. Reference [23] studied the effects of arm inductance and SM capacitance on the magnitude of circulating current. Increases in arm inductance decrease the circulating current, but the circulating currents are not eliminated. The negative sequence component of circulating current rotates at twice line frequency. A control scheme is proposed in [24] by translating the a-b-c sequence components into *dq* rotational frame. But this control structure has a limitation because the circulating current also have positive and zero sequence components along with negative sequence components.

The most common control approach was introduced by Hagiwara and Akagi in [25]. The control method is used to regulate the output current and internal dynamics, i.e., circulating current and internal energy. However, the ripples in circulating current could not be eliminated effectively by this control method. Over the past few years, many control schemes for circulating current were proposed such as *dq* or rotating frame control for the suppression of 2nd order harmonics [26–28], resonant controllers to eliminate harmonics in unbalanced circumstances [29] and to eliminate integral harmonics in circulating currents plug in repetitive controllers are used [30,31]. But the above-mentioned control method is complicated in structure and the controllers are difficult to tune for system stability and performance.

Some researchers have proposed control methods for controlling both circulating current and output current. A PR control strategy is used to control an output current to get the desired output power. The output current is 1st harmonic frequency sinusoid [32]. Since after all PR control strategy gives an infinite gain at the resonant frequency, any small frequency changes may point to an enormous tracking error from the reference signal. A PI controller in [24] is used to control circulating current

and a PR controller is also proposed to suppress the circulating current in [33]. However, the design and tuning parameters of the controllers mentioned above may be complicated as obtaining excellent control operation and stability may be a difficult task.

This paper covers two main issues of the MMC—circulating current control and output current control during normal grid condition. An adaptive PI controller has been used to control both the circulating and output current control in *dq* and *abc* stationary frames. Compared to other control methods, the API control scheme has many advantages such as good tracking, transient response, optimal stability performance, wide range operation capability, and adequate control for the MMC during normal grid condition.

The sections of this paper are organized as Section 2, which describes the operation and modeling of the MMC. Section 3 deals with the control structure design for output and circulating current. The results are discussed in Section 4. While the conclusion is detailed in Section 5.

2. Operation and System Mathematical Modeling

Every SM of an MMC has a capacitor and half bridge connected switches, which gives output voltage according to switch ON or OFF position as depicted in Figure 2.

2.1. Switching Operation of the MMC

The insertion or bypassing of N-SM will give, $(M+1)$ levels of output waveform at every phase of the MMC. Where N represents No of SM and M represents the levels of output wave form. The switching operation of a single phase MMC is illustrated in Figure 2, using a single line schematic diagram.

A DC voltage "U_{dc}" is applied at the input of the MMC. The switches are operating in reciprocal fashion in each SM relying on the position ON or OFF. The solid line shows the capacitor is inserted and the dim line shows a capacitor is bypassed in every SM. The insertion and bypassing of the capacitor will define different levels of voltage at its terminal shown in Figure 2. The capacitor state that is inserted or bypassed are summarized in Table 1.

Table 1. Capacitor states.

Scenario	Capacitors States in the Upper Arm	Capacitors States in the Lower Arm	Output Voltage
1	All capacitors are inserted	All capacitor bypassed	$-\frac{U_{dc}}{2}$
2	One capacitor bypassed and three capacitors inserted	One capacitor inserted and three capacitors bypassed	$-\frac{U_{dc}}{4}$
3	Two capacitors bypassed and two capacitors inserted	Two capacitors inserted and two capacitors bypassed	0
4	Three capacitors bypassed and one capacitor inserted	Three capacitors inserted and one capacitor bypassed	$\frac{U_{dc}}{4}$
5	Four capacitors bypassed and zero capacitors inserted	Four capacitors inserted and zero capacitors bypassed	$\frac{U_{dc}}{2}$

2.2. System Mathematical Modeling

The mathematical modeling of the MMC is derived from a single-phase equivalent circuit as shown in Figure 3.

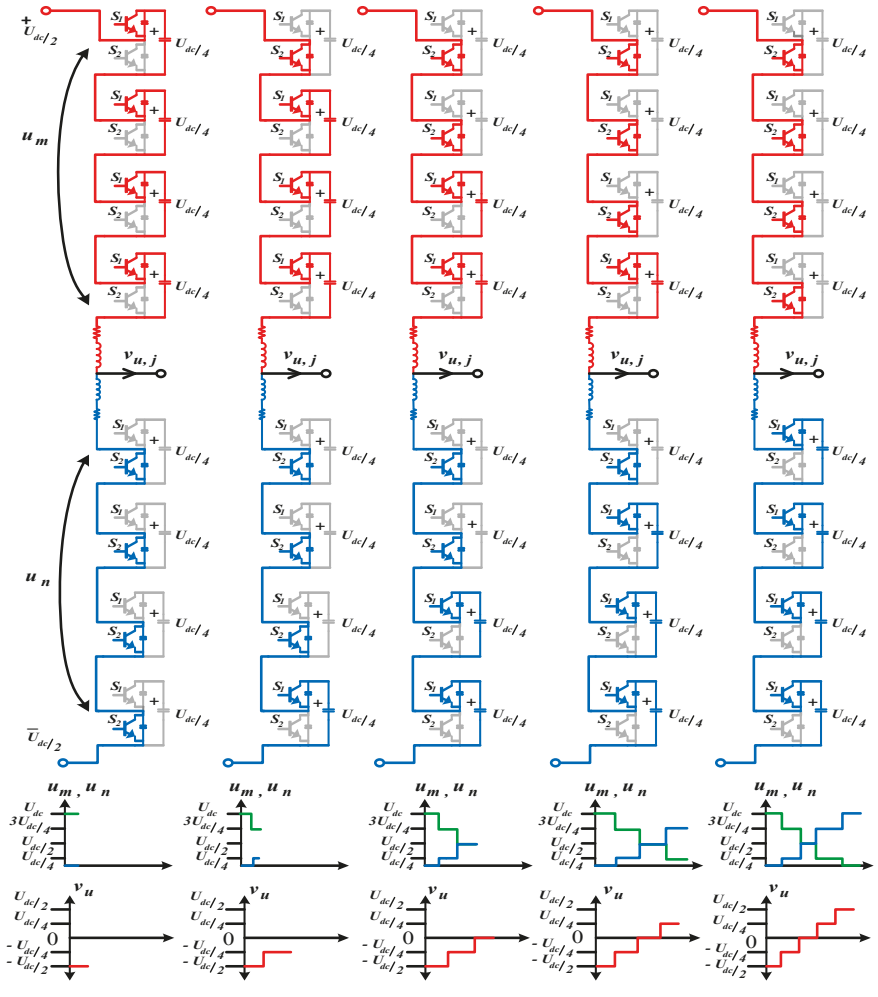


Figure 2. Switching operation of the single phase MMC.

By applying the Kirchhoff loop law, the relations for the arm voltages, output current, and circulating current of the converter are obtained as follow [34]. Where $j \in \{a, b, c\}$

$$-\frac{U_{dc}}{2} + u_{m,j} + R_{arm} i_{m,j} + L_{arm} \frac{di_{m,j}}{dt} + v_{u,j} = 0 \tag{1}$$

$$\frac{U_{dc}}{2} - u_{n,j} - L_{arm} \frac{di_{n,j}}{dt} - R_{arm} i_{n,j} + v_{u,j} = 0 \tag{2}$$

where L_{arm} and R_{arm} denote arm inductance and arm resistance respectively. U_{dc} represent the entire DC bus terminal voltage. $v_{u,j}$ represent output voltage of converter at point Z. $u_{m,j}$ and $u_{n,j}$ represents submodule arm voltages. The upper arm is represented by subscript m while a lower arm is represented by subscript n. Different currents of the MMC are given as

$$i_{m,j} = i_{diff,j} + \frac{i_{u,j}}{2} \tag{3}$$

$$i_{n,j} = i_{diff,j} - \frac{i_{u,j}}{2} \tag{4}$$

$$i_{u,j} = i_{m,j} - i_{n,j} \tag{5}$$

$$i_{diff,j} = \frac{1}{2}\left(i_{m,j} + i_{n,j}\right) \tag{6}$$

where $i_{m,j}$ and $i_{n,j}$ represents the upper arm current and lower arm current. $i_{u,j}$ represent the output current. $i_{diff,j}$ represents an internal circulating current. Adding and subtracting (1) and (2) we obtain the following relation.

$$v_{u,j} = \underbrace{\left(\frac{u_{n,j} - u_{m,j}}{2}\right)}_{e_{v,j}} - \frac{R_{arm}}{2} i_{u,j} - \frac{L_{arm}}{2}\frac{di_{u,j}}{dt} \tag{7}$$

$$v_{diff,j} = \frac{U_{dc}}{2} - R_{arm} i_{diff,j} - \frac{L_{arm} di_{diff,j}}{dt} \tag{8}$$

The $e_{v,j}$ is internal voltage in (7), while $v_{diff,j}$ in (8) is the internal unbalanced voltage of an MMC, and the internal $i_{diff,j}$ over phase $j \in \{a, b, c\}$ can be express as

$$i_{diff,j} = \frac{i_{m,j} + i_{n,j}}{2} = \frac{I_{dc}}{3} + i_{cir,j} \tag{9}$$

where I_{dc} is the dc link current and supposed to be distributed equally in all phases. As a result, the circulating current described in (6) contains 1/3 of the DC link current $\frac{I_{dc}}{3}$ and $i_{cir,j}$ is the AC component of circulating current. The dynamics of an MMC are characterized in Equations (7) and (8). By evaluating Equation (7), the output current $i_{u,j}$ can be controlled by $e_{v,j}$. Similarly, by evaluating Equation (8), the internal circulating current $i_{diff,j}$ can be controlled by $v_{diff,j}$. Furthermore, the capacitor SM internal dynamics with regards to arm voltages and currents are expressed as

$$\frac{C}{N}\frac{dv^{\Sigma}_{cm,j}}{dt} = n^{i}_{m,j} i_{m,j} \tag{10}$$

$$\frac{C}{N}\frac{dv^{\Sigma}_{cn,j}}{dt} = n^{i}_{n,j} i_{n,j} \tag{11}$$

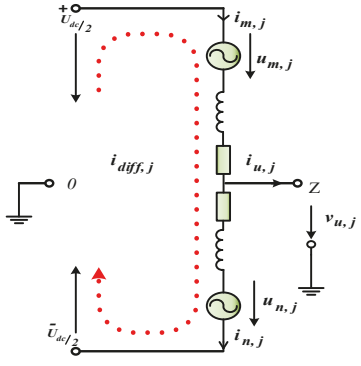


Figure 3. Single phase equivalent circuit.

The capacitance of an SM capacitor is expressed by C, the number of SM in each half arm is represented by N, while capacitor sum voltages in upper and lower arms are represented by $v^{\Sigma}_{cm,j}$ and $v^{\Sigma}_{cn,j}$. Insertion indices of upper and lower arms are represented by $n^{i}_{m,j}$ and $n^{i}_{n,j}$. Insertion indices $n^{i}_{m,j}$

and $n^i_{n,j}$ equal to one means the SM capacitor is inserted while insertion indices $n^i_{m,j}$ and $n^i_{n,j}$ equal to zero means the SM capacitor is bypassed in corresponding arms. As stated by Equations (8) and (9), the reference calculated for the arm voltages can be expressed as

$$u_{m,j\_ref} = \frac{U_{dc}}{2} - e_{v,j} - v_{diff,j} + R_{arm} i_{diff,j} + \frac{L_{arm} di_{diff,j}}{dt} \tag{12}$$

$$u_{n,j\_ref} = \frac{U_{dc}}{2} + e_{v,j} - v_{diff,j} + R_{arm} i_{diff,j} + \frac{L_{arm} di_{diff,j}}{dt} \tag{13}$$

In (13) the $e_{v,j}$ is calculated from the internal loop current controllers [35], while $v_{diff,j}$ is calculated from the circulating current eliminating controller, which can be used to minimize the three-phase circulating current in an MMC. It can be concluded from Equations (1), (2), (12), and (13) that $i_{u,j}$ and $i_{diff,j}$ could be controlled by manipulating $e_{v,j}$ and $v_{diff,j}$, respectively.

3. Control Scheme of the MMC

3.1. Adaptive PI Controller Design

The adaptive PI is a hybrid controller in which fuzzy logic (FL) is used to update the gains of PI for a wide range of operation. The FL makes the processing operation of a PI controller easy in a non-linear system where the system is ill-defined and mathematically poorly designed. The FL pre-processes the controller input (I/P) signal and PI post-process error signal to get the desired output response from the plant.

3.1.1. Fuzzy Controller Architecture

In the real world, problems related to a control system are largely complex, particularly when implementation problems are considered. The promising aspect of the fuzzy logic controller (FLC) is that they incorporate expert knowledge instead of entirely depending upon the exact mathematical model. Moreover, heuristics and intuition knowledge are also incorporated into the control system. Thus, FLC is suitable in applications, where models are ill-defined, not reliable enough, and complex. Essentially, the FLC is an artificial decision maker who works in a closed-loop fashion in real-time as shown in Figure 4. It collects plant O/P information $y(t)$, matches it with the reference I/P $x(t)$, and decides what the plant I/P $v(t)$ would be to assure performance objectives. The FLC is mainly composed of four main phases: rule-base, inference mechanism, fuzzification, and de-fuzzification.

1. The "rule-base" which contains the information of controlling output variables are created in FLC, in the shape of IF-THEN rules, with condition and conclusion.
2. The rules are evaluated in the inference mechanism according to the error. During inference mechanism, it is concluded which control rules are appropriate at the current situation. Moreover, the choice of I/P to the plant are also enabled in this phase.
3. During the fuzzification, a "crisp" (which are real numbers, not fuzzy sets) or actual time information are collected and reshaped to a fuzzy set using fuzzy expressive terms, expressive variables, and membership functions. Moreover, I/P is modified and interpreted which are then compared with the rules defined in the rule-base.
4. The defuzzification transforms the fuzzy outcomes obtained by inference mechanism to real-time or crisp output utilizing membership functions. There are several available methods for defuzzification, i.e., mean of maximum, center of minimum, and center of gravity [36,37].

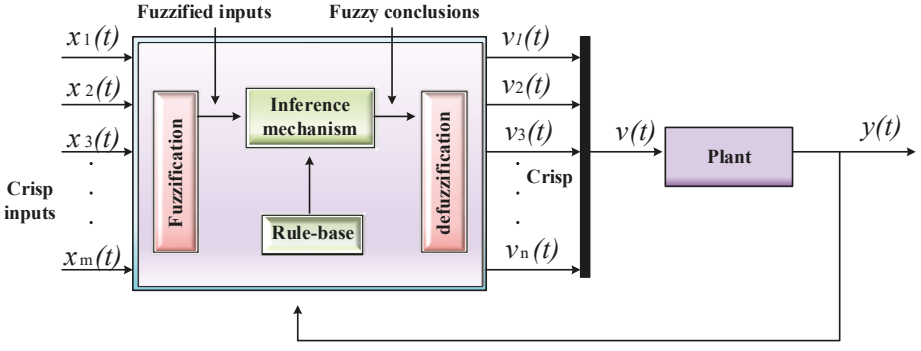


Figure 4. Fuzzy controller architecture to controlled plant.

3.1.2. Fuzzy PI Controller

The PI controller has tuning gains parameter k_p and k_i, respectively. The desired performance of PI control structure is improved by updating the gains, according to error $u(t)$. The adaptability is attained by employing fuzzy rules, as given below and graphically illustrated in Figure 5.

- If error $|u(t)|$ is zero, then proportional gain k_p is large and integral gain k_i is small
- If error $|u(t)|$ is small, then proportional gain k_p is large and integral gain k_i is zero.
- If error $|u(t)|$ is large, then proportional gain k_p is large and integral gain k_i is large.

The "crisp inputs" in the form circulating current and output current are fuzzified and shaped to a fuzzy set using membership function. The fuzzy set is evaluated in the rules-base with condition and conclusion, and concludes which rules are appropriate at the current time. The defuzzification process involves the conversion of the fuzzy outcomes to circulating and output voltages utilizing the membership function. The fuzzy rule selected from the set is defuzzified by using the center of gravity method. While the Gaussian membership function (GMF) is used for fuzzification, the GMF uses two variables, variance σ_i or standard deviation and center d_i as:

$$\mu(x) = \exp\left(-0.5\left(\frac{x_i - d_i}{\sigma_i}\right)^2\right) \tag{14}$$

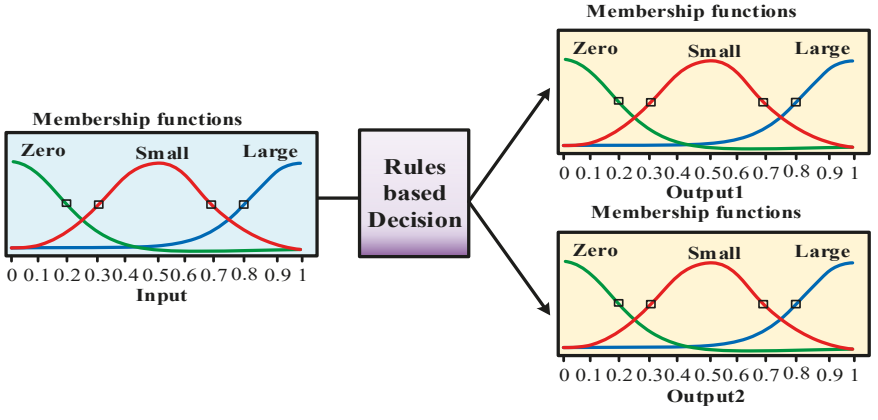


Figure 5. Output–input membership functions.

The defuzzified output of fuzzy is fed as a gain $(K_p,\ K_i)$ to PI. Thus, the PI controller for controlling the $i_{u,j}$ is mathematically defined as:

$$e^*_{v\alpha\beta}(PI) = K_p u(t) + K_i \int u(t)dt \tag{15}$$

The PI controller for controlling the $i_{diff,j}$ is mathematically defined as:

$$v^*_{diff,j}(PI) = K_p u(t) + K_i \int u(t)dt \tag{16}$$

Whereas $u(t)$ is controller input, $e^*_{v\alpha\beta}$ and $v^*_{diff,j}$, controller outputs, k_p and k_i are controller gains respectively. However, the gain's parameters of a conventional PI controller are constant in (15) and (16), which needs adaptation according to system load disturbance, parameter uncertainties, electrical faults, and load variations. To achieve adaptation, the designed controller use $u(t)$ signal as an input for self-tuning of gain parameters, i.e., k_p and k_i, respectively. Fuzzy IF-THEN rules are made as presented in Table 2. Based on these rules, a decision is performed by the inference engine. The defuzzified output is obtained by the center of gravity method for U_1 and U_2.

Table 2. IF-THEN rules employed for gain adaptation.

Input Membership Functions			**IF-THEN Rules**		**Output Membership Functions**	
S.No	Linguistic Terms	Range	If Input $\|u(t)\|$	Then Output (k_p, k_i)	Linguistic Terms	Range
(1)	Zero	[0, 0.2]	Zero	Zero. Large	Zero	[0, 0.2]
(2)	Small	[0.3, 0.7]	Small	Large. Small	Small	[0.3, 0.7]
(3)	Large	[0.8, 1.0]	Large	Large. Large	Large	[0.8, 1.0]

During fuzzification, the error signal, $u(t)$, information is collected and converted/fuzzified to fuzzy set using fuzzy linguistic terms and membership functions and compared with the IF-THEN rules defined in the rule-base. The rules are analyzed in the inference mechanism that decides the firing of the dominant rule. The fuzzy outcomes in the shape of U_1 and U_2 are obtained during defuzzification using the center of gravity method and update the gain parameters K_1 and K_2, respectively. The rules employed in rule-base can be graphically illustrated in Figure 6a–c and shows the various scenarios in which U_1 and U_2 are actually computed by the fuzzy controller based on the absolute error. The line indices which corresponds to inputs can be moved to adjust gains k_p and k_i, as shown in Figure 6a–c.

So, the adaptation of (15) using the API controller for controlling $i_{u,j}$ is mathematically defined as

$$e^*_{v\alpha\beta}(API) = U_1 K_1 u(t) + U_2 K_2 \int u(t)dt \tag{17}$$

The adaptation of (16) using the API controller for controlling $i_{diff,j}$ is mathematically defined as

$$v^*_{diff,j}(API) = U_1 K_1 u(t) + U_2 K_2 \int u(t)dt \tag{18}$$

Whereas U_1 and U_2 are the fuzzy controller output for the gains k_p and k_i respectively. While K_1 and K_2 are used for the representation of updated gains k_p and k_i as shown in Figure 7.

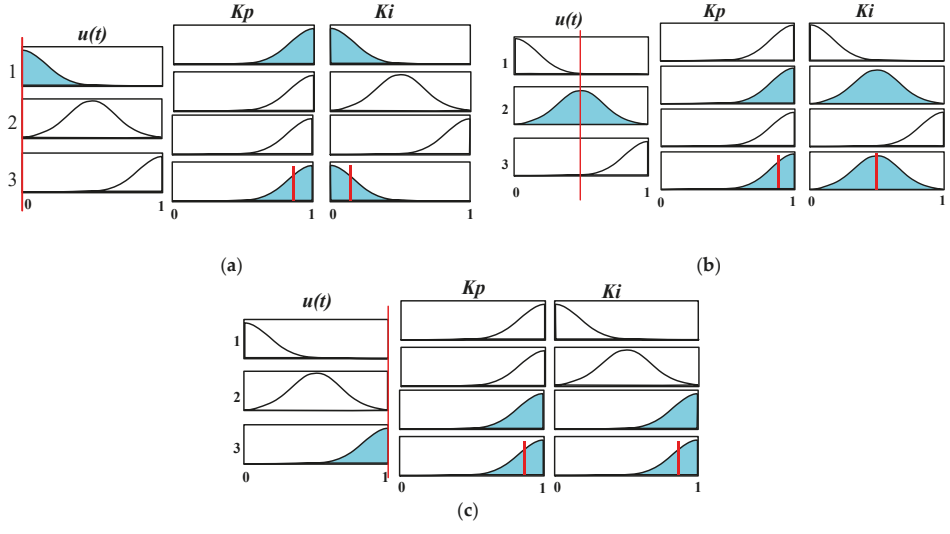


Figure 6. Adaptation of gain values where the: (**a**) error is zero, (**b**) error is small, and (**c**) error is large.

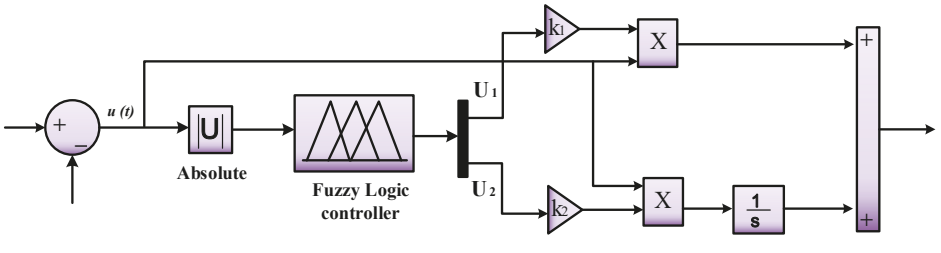


Figure 7. Control structure for error tracking.

3.2. Circulating Current Control

The $i_{diff,j}$ can be regulated by $v_{diff,j}$, therefore, a control scheme is needed to regulate $v_{diff,j}$ for controlling $i_{diff,j}$ to overcome the converter losses. The variable $v_{diff,j}$ is obtained through (8). A feedforward part is added to compensate the voltage drop. Filtering of U_{dc} is not required due to the lower number of harmonics in DC voltage compared to AC voltage. The control law we obtain

$$v^*_{diff,j} = \frac{U_{dc}}{2} - Ri_{diff} - \left(U_1K_1u(t) + U_2K_2\int u(t)dt\right)\left(i^*_{diff,j} - i_{diff,j}\right) \tag{19}$$

The reference is forced to get the desired value of circulating current, i.e., P/MU_{dc}. The control structure using the API controller is shown in Figure 8.

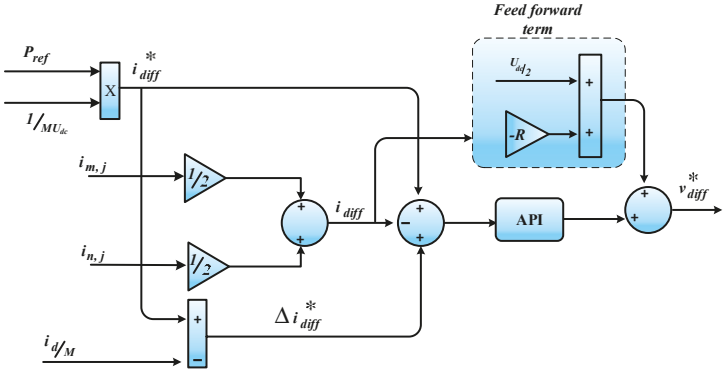


Figure 8. Circulating current control.

3.3. Output Current Control

The output current can be regulated according to the following equation.

$$v_{u,j} = e_{v,j} - \frac{R_{arm}}{2} i_{u,j} - \frac{L_{arm}}{2} \frac{di_{u,j}}{dt} \tag{20}$$

By evaluating (20), $e_{v,j}$ is the variable which can be regulated to control the output current $i_{u,j}$. The Equation (20) can be rewritten as

$$\begin{bmatrix} e_{v,a} \\ e_{v,b} \\ e_{v,c} \end{bmatrix} = \frac{1}{2(sL_{arm} + R_{arm})} \begin{bmatrix} i_{u,a} \\ i_{u,b} \\ i_{u,c} \end{bmatrix} + \begin{bmatrix} v_{u,a} \\ v_{u,b} \\ v_{u,c} \end{bmatrix} \tag{21}$$

Using the Clarke transformation Equation (20) can be transformed into $\alpha\beta$ axis from *a*-*b*-*c* frame $\left(T_{abc \Rightarrow \alpha\beta}\right)$.

$$T_{abc \Rightarrow \alpha\beta} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \sqrt{\frac{1}{2}} & \sqrt{\frac{1}{2}} & \sqrt{\frac{1}{2}} \end{bmatrix} \tag{22}$$

For a three-phase balance system Equation (21) can be written

$$\begin{bmatrix} e_{v,\alpha} \\ e_{v,\beta} \end{bmatrix} = \frac{1}{2(sL_{arm} + R_{arm})} \begin{bmatrix} i_{u,\alpha} \\ i_{u,\beta} \end{bmatrix} + \begin{bmatrix} v_{u,\alpha} \\ v_{u,\beta} \end{bmatrix} \tag{23}$$

In control engineering usage $v_{u,\alpha\beta}$ is load disturbance which will vary inversely according to short circuit ratio [32]. Since $v_{u,\alpha\beta}$ is measurable by introducing a feedforward term, the dynamics can be improved. The control law obtained

$$e^*_{v,j} = \left(U_1 K_1 u(t) + U_2 K_2 \int u(t)dt\right)\left(i^*_{u,j} - i_{u,j}\right) + v_{u,\alpha\beta} + i_{u,\alpha\beta}\frac{R}{2} \tag{24}$$

where $(i^*_{u,j} - i_{u,j})$ error control and the reference for voltage is computed using Equation (24), to control the output current. The output current control structure is shown in Figure 9.

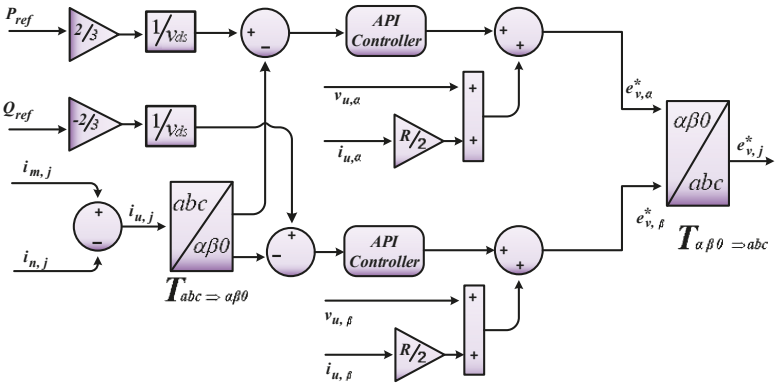


Figure 9. Output Current control.

The overall control scheme for controlling the circulating current and output current is shown in Figure 10.

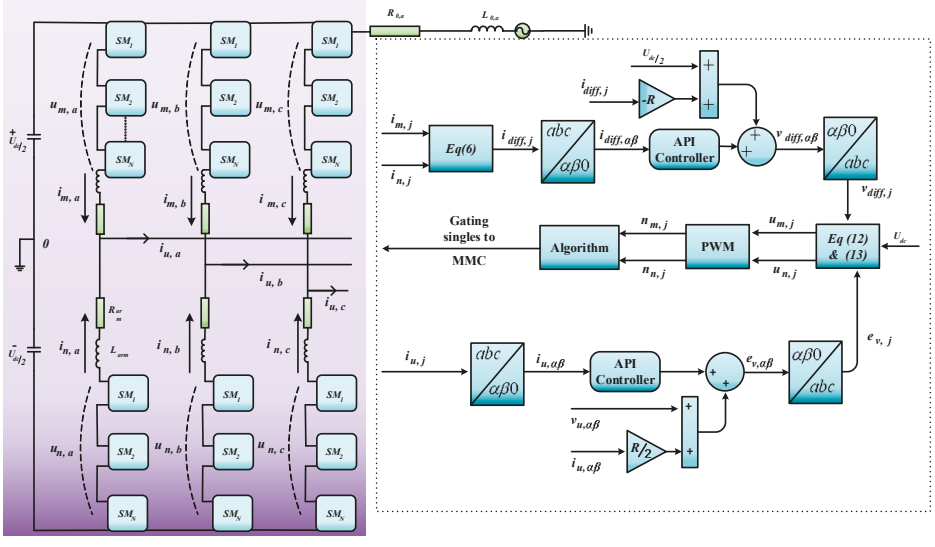
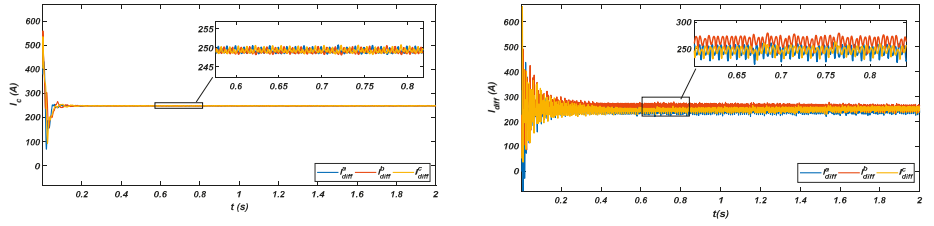


Figure 10. Overall control design for output and circulating currents.

4. Results and Discussions

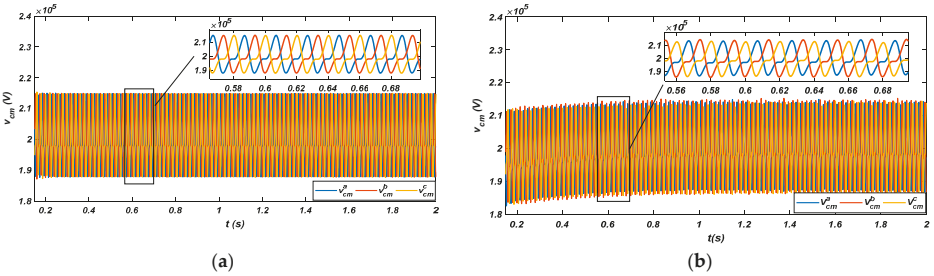
A control design architecture for a three-phase MMC model has been implemented with the help of MATLAB-Simulink (2017a, Natick, Massachusetts, MA, USA). The time for simulation is considered as 2 s. For better understanding, all the results are magnified. A comparative analysis of the results between the proposed API controller and a conventional PR controller has been made. The capacitor sum voltage and circulating current are the variables which need to be controlled, to reduce MMC losses. Ideally, the circulating current value i_{diff} should converge to DC input power, i.e., $\left(i_{diff} = \frac{P}{MU_{dc}}\right)$. The results of circulating current in Figure 11a,b is compared using the API and a PR controller. For a better understanding, the results are magnified for time t = 0.6 s to t = 0.8 s using the magnification tool. The API controller result shows that the circulating current value is converging to the desired value, i.e., 250 A with no oscillations during 0.2 s, showing good result compared to

the PR controller. While in the case of PR controller the circulating current value is not converging to the desired value i.e., 250 A and also shows oscillations up to 0.2 s. Which means that the circulating current is not converged properly. It is also noted that circulating current one phase is exceeding the desired value, i.e., 250 A throughout the simulation as depicted in Figure 11b. The capacitor sum voltage average value should converge to DC link voltage mean value, i.e., $\frac{U_{dc}}{2}$ to get a balance distribution of capacitor sum voltage over desired SM. The capacitor sum voltage of both an upper and a lower arm using the API and a PR controller are analyzed in Figures 12a,b and 13a,b. For a better explanation, the results are magnified for time t = 0.58 s to t = 0.68 s using the magnification tool. The API controller display proper convergence of capacitor sum voltage to a desired DC link mean value for both upper and lower arm. All phase voltages are balanced in magnitude, which shows the balance distribution of capacitor sum voltage for the required SM in both upper and lower arm. As opposed to the API controller, the capacitor sum voltage of both upper and lower arms using the PR controller showed an imbalance in magnitude and created a trajectory path from 0.2 s to 0.8 s, which meant that the capacitor sum value was not totally converged to the desired DC link mean value for a balanced distribution of capacitor voltage in the required SM.



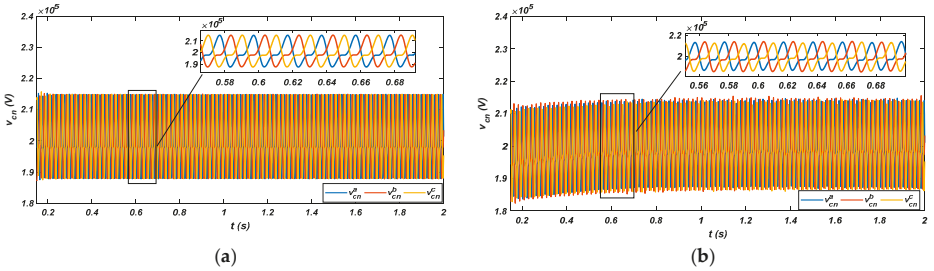
(**a**) (**b**)

Figure 11. (**a**) Circulating current using the API controller; (**b**) circulating current using the PR controller.



(**a**) (**b**)

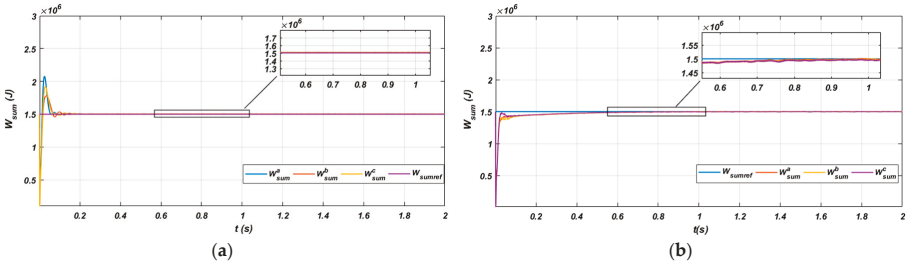
Figure 12. (**a**) Capacitor voltage of an upper arm using the API controller; (**b**) capacitor voltage of an upper arm using the PR controller.



(**a**) (**b**)

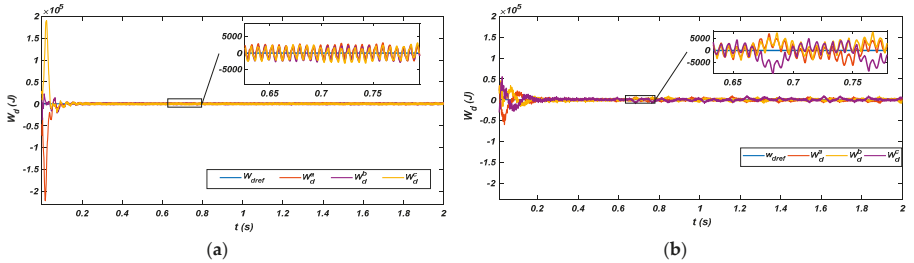
Figure 13. (**a**) Capacitor voltage of a lower arm using the API controller; (**b**) capacitor voltage of a lower arm using the PR controller.

The dynamics of sum energy for both controllers are shown in Figure 14a,b. For better analysis, the results are magnified for time t = 0.6 s to t = 1 s using the magnification tool. At the start, the API controller shows overreaction. The rules defined in the rule-base are called and the decision is carried out to fire the dominant rule. The API controller takes only 0.024 s to clear transient, and the reference is completely tracked at 0.75 s completely without further overshoot, undershoot, steady state error, and ripples. However, in the case of the PR controller, the reference is completely tracked at 1 s. Moreover, the API controller shows a fast and robust response during the transient state. While the sum energy using a PR controller shows slower, oscillatory, and steady-state error. Which means that the PR controller response is slower than the proposed API controller. The energy difference mean value should be regulated correctly and converged to the zero reference value properly. The energy difference dynamics of the MMC for both controllers are shown in Figure 15a,b. For the result analysis, the results are magnified using the magnification tool for t = 0.65 s to t = 0.8 s. At the start, the proposed API controller shows an overreaction for 0.012 s, because the gains parameters are not updated. The rules defined in the rule-base are recalled and update the gain parameters of the PI controller. Once the parameters are updated, the proposed controller start tracking the reference without any further overshoot and converges the delta energy properly to the desired mean value. However, in the PR controller, the delta energy mean value is not converged properly, or showing disturbance, during time interval 0.65 s to 0.8 s. Moreover, the energy difference of both controllers is nearly close to zero. However, the API controller shows perfectly close convergence to zero and oscillating between positive and negative values giving an average value of zero, which means that the energy difference is regulated correctly and converged to zero reference value properly. In comparison to the API, the PR controller in the zoomed window shows that the desired value is showing some disturbance from 0.6 s to 0.8 s, which means that value is not converging to zero correctly during the mentioned time frame or showing a steady state error.



(**a**) (**b**)

Figure 14. (**a**) Sum energy of arms using the API controller; (**b**) sum energy of arms using the PR controller.

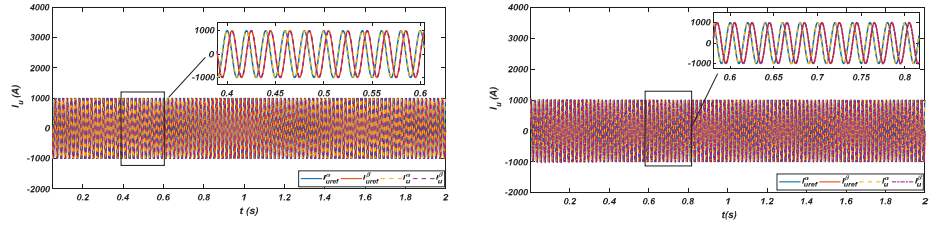


(**a**) (**b**)

Figure 15. (**a**) Energy difference of arms using the API controller; (**b**) energy difference of arms using the PR controller.

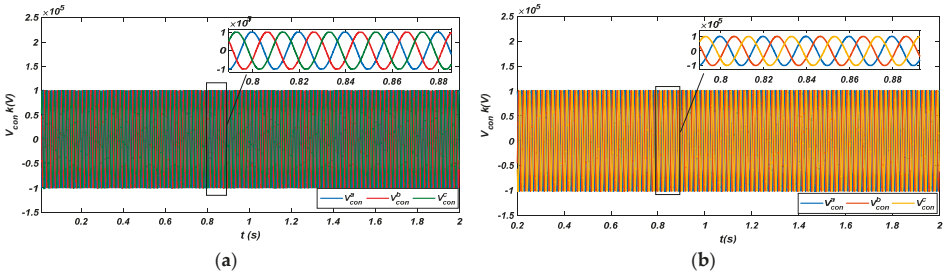
The output current is transformed in the αβ axis for both controllers shown in Figure 16a,b. For the explanation of results, the results are magnified using the magnification tool for t = 0.6 s to

t = 0.8 s. For both controllers, the comparison is made on the basis of the performance indices, reference tracking, and transient and steady-state response. The API controller shows better performance indices, reference tracking, and transient and steady-state response compared to the PR controller. The performance indices are summarized in Table A2 of Appendix A, while converter and grid output phase voltages are shown in Figures 17a,b and 18a,b for both controllers. For an explanation of the results, they are magnified using the magnification tool for t = 0.8 s to t = 0.88 s.



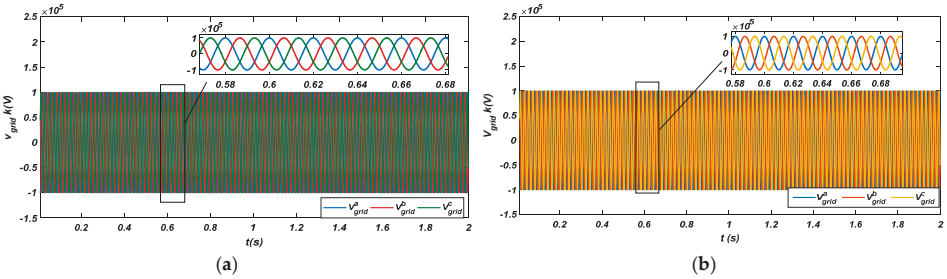
(**a**) (**b**)

Figure 16. (**a**) Output current using the API controller; (**b**) output current using the PR controller.



(**a**) (**b**)

Figure 17. (**a**) Converter phase voltages using the API controller; (**b**) converter phase volatges using the PR controller.



(**a**) (**b**)

Figure 18. (**a**) Grid phase voltage using the API controller; (**b**) grid voltage using the PR controller.

The control structure designed with the API controller is compared with conventional PR controller. The comparative analysis of a conventional PR and proposed API controller for controlling the output and circulating currents shows that the designed controller can track the references. The designed controller is also capable of converging the circulating current to the desired value. With the proposed control structure, the designed controller can converge the DC link voltage mean value to $\frac{U_{dc}}{2}$ for the balance distribution of the capacitor sum voltage in the desired SM. The energy difference in both arms is well regulated by the proposed controller. The proposed API controller shows an improved transient response compared to the PR controller.

5. Conclusions and Future Work

This paper presents a control structure for controlling the circulating current and output current of the MMC during normal grid conditions. The control structure is implemented with an API controller. The control designed structure enables reference tracking, controlled circulating current, output current, the convergence of sum and delta energies to proper values. For validation of the proposed control structure, the results of the designed API controller are compared with a conventional PR control for verification.

MATLAB-Simulink results for both PR and API controllers shows that the API controller has a superior performance over the PR controller. The API controller can converge the circulating current to the desired value. The proposed API controller also shows improved transient response compared to the PR controller. In addition, the controller assures the reference tracking for sum energy and delta energy during the transient and steady response ensuring a stable three-phase output voltage. Moreover, the optimal performance achieved for the MMC parameters using the API controller are shown in Table A1 of Appendix A.

However, the designed control structure for circulating current and output current will be validated using FPGA or DSP TMS3200F28xx Kits (Texas Instruments, Dallas, TX, USA), Intel 8Xc196KC microcontroller (Intel corporation, Santa Clara, CA, USA) and dSPACE Digital Signal Controllers boards (DS1104, dSPACE Inc, Michigan, MI, USA). Feedback linearization and optimal control strategies will be designed and compared with conventionally tuned PR control structure.

Author Contributions: H.J.K., M.I., and W.U. conceptualized the main idea of this paper. M.I. implemented the mathematical equations, simulation verification, and the analyses. The paper was written by M.I. and reviewed by W.U., K.Z., S.U.I., I.K., and H.J.K. All authors were involved in formulating the final version of this paper. Furthermore, the work was supervised by H.J.K.

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Appendix A

Table A1. Converter parameters.

Parameters	Values	Symbols	Units
D.C voltage	200	U_{dc}	kV
Grid voltage	100	v_u	kV
Output current	1	i_u	kA
Frequency	50	f	Hz
No of SM	12	N	-
Inductance	50	L_{arm}	mH
Resistance	1.57	R_{arm}	Ω
Capacitance	0.45	C	mF

Table A2. Performance indices evaluation.

Performance Indices Elevation For	API Controller			PR Controller		
	[1]ISE	[2]IAE	[3]IATE	ISE	IAE	ITAE
Circulating current	3.714	0.2237	0.1834	1696	23.47	14.63
	3.665	0.2105	0.1836	2247	25.46	14.47
	3.694	0.2200	0.1832	2483	25.31	25.31
Output current	400.56	5.968	2.915	1022	13.5	8.913
	20.86	5.658	2.997	50.5	13.1	9.009

[1]ISE: Integral Square Error, [2]IAE: Integral Absolute Error, [3]ITAE: Integral of time Absolute Error.

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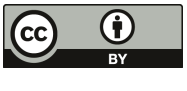

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Direct Digital Design of PIDF Controllers with ComPlex Zeros for DC-DC Buck Converters

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Abstract: This paper presents a new direct digital design method for discrete proportional integral derivative PID + filter (PIDF) controllers employed in DC-DC buck converters. The considered controller structure results in a proper transfer function which has the advantage of being directly implementable by a microcontroller algorithm. Secondly, it can be written as an Infinite Impulse Response (IIR) digital filter. Thirdly, the further degree of freedom introduced by the low pass filter of the transfer function can be used to satisfy additional specifications. A new design procedure is proposed, which consists of the conjunction of the pole-zero cancellation method with an analytical design control methodology based on inversion formulae. These two methods are employed to reduce the negative effects introduced by the complex poles in the transfer function of the buck converter while exactly satisfying steady-state specifications on the tracking error and frequency domain requirements on the phase margin and on the gain crossover frequency. The proposed approach allows the designer to assign a closed-loop bandwidth without constraints imposed by the resonance frequency of the buck converter. The response under step variation of the reference value, and the disturbance rejection capability of the proposed control technique under load variations are also evaluated in real-time implementation by using the Arduino DUE board, and compared with other methods.

Keywords: buck converter; inversion formulae; phase margin; gain crossover frequency

1. Introduction

Many industrial applications need the transformation of a constant DC voltage source to a constant value even under load variation, such as photovoltaic systems, mobile power supply equipment, DC supply systems, etc. The buck converter is one of the most widely utilized DC-DC converters, because of its simplicity, high efficiency, and low cost, see e.g., [1], and therefore each improvement has potentially a major economic and commercial impact. However, the presence of its nonlinear characteristics in the switching behavior and the saturation of the duty cycle render the output voltage control a challenging task. Numerous control strategies have been proposed for the voltage regulation of the buck converter. Each of them has advantages and disadvantages, and the selection of the most appropriate one depends mainly on the design task at hand. A brief review of the main digital control techniques can be found in [2]. Among these, the non-linear sliding mode control, which leads to fast transient response under load variation and high robustness, is worth mentioning [3,4]. However, the control performance is reduced by the introduction of high frequency oscillations around the sliding surface, the so-called chattering. Another practical alternative for the voltage regulation of the buck converter is the fuzzy logic control. This non-linear adaptive technique provides a robust performance under parameter variations and load disturbances, and can operate

with noise and disturbance of different natures. However, these controllers are traditionally designed by trial-and-error, and this, combined with the rich architecture of the controller, constitutes a major drawback in carrying out stability and performance analysis, as well as transfer function and small signal analysis [5]. By contrast, classical linear proportional integral/proportional integral derivtive (PI/PID) control techniques are widely used by industrial practitioners for their simplicity in the design and implementation, and still by far play a major role. In fact, PID control is often taken as a benchmark for comparison with new strategies since it provides a good compromise among various types of performance indices, including voltage tracking and disturbance rejection, while guaranteeing a satisfactory robustness to small variations of the parameters of the buck converter [1]. Many PID-based strategies have also been combined with non-linear techniques to improve the closed-loop performance [2,3,6–10]. However, in the vast majority of the cases, the PID controller is designed in the continuous-time and then, for its practical implementation, it is converted to the discrete-time, see [10–12].

A common approach to the control feedback design involving PID controllers is to consider the ideal (improper) PID transfer function, which is non-causal. By contrast, the discretization of the ideal PID controller results in a casual, thus feasible, discrete transfer function. This explains why, in this context, the discretization appears to be critical. Indeed, frequency domain specifications assigned in the continuous-time domain can be affected by large undesired variations due to the discretization of the controller. Another critical issue in the design of PID controllers for the buck converter is caused by the presence of a resonance peak in the transfer function of the process. In fact, the resonance usually constrains the assignability of the closed-loop bandwidth, which has to be either well below the resonance frequency, or well above. The former solution is usually discarded since, for obvious reasons, it leads to poor performance. However, the latter is typically associated to a very large bandwidth, which is likely to induce severe saturation in the control variable.

This paper presents a new direct design technique for the discrete PID + filter (PIDF) controllers with complex conjugate zeros. Our method hinges on the classical pole-zero cancellation method [10] combined with the so-called discrete "inversion formulae" [13–18]. In the aforementioned design procedure, two parameters of the PIDF controller are used to achieve pole/zero compensation, as in [10], and the remaining two degrees of freedom are used to exactly meet specifications on the phase margin and gain crossover frequency with the use of the inversion formulae. The design approach based on these formulae was first presented for lead, lag and PID controllers in [13–18]. In this paper we introduce a new set of inversion formulae for the design of the time constant of the discrete PIDF controller.

Thanks to the closed-form design of the filter, which guarantees sufficiently large stability margins even in the presence of uncertainty, our method ensures a satisfactory performance in a neighborhood of the operating point.

The approach based on the inversion formulae results in a proper discrete PIDF controller which is directly implementable on a microcontroller, and which exactly satisfies the design requirements in the discrete domain. Thus, unlike the other techniques described above, the specifications are guaranteed to remain exactly satisfied even when considering the discrete implementation of the controller. Note that we avoid indirect tuning procedures and the inherent trial-and-error nature of graphical tuning techniques based on Bode, Nyquist and Nichols plots.

The procedure presented here is analytical in nature, and can be carried out in finite terms via simple equations which are dependent upon the sampling time of the analog-to-digital converter.

The structure of the discrete PIDF controller is obtained from a continuous-time PIDF [19] transfer function through the matched pole-zero mapping discretization method [20]. In this way, the cancelation results in a discrete transfer function, and therefore the controller can be directly designed in the z-domain.

Simulations and comparisons with other methods show the effectiveness of this new control strategy, which can accommodate plant uncertainties and also, importantly, load variations.

The proposed method has been first simulated in MATLAB Simulink® and then tested in a real-time digital implementation using the Atmel SAM3X8E microcontroller based on the ARM® Cortex® -M3 processor on an Arduino Due board. The experimental results have been analyzed and compared with classical PID control solutions.

The paper is organized as follows. The digital control schemes and discrete buck converter model are described in Section 2. In Section 3, we propose the discrete PIDF controller with complex conjugate zeros. The control problem and the proposed design solution are presented in Section 4. We describe the simulated and experimental results of the proposed DC-DC buck converter control and the performance comparison with other methods in Section 5. Conclusions and remarks will end the paper.

2. Digital Control Schemes and Discrete Buck Converter Model

The DC-DC buck converter is a step-down switching converter extensively described, e.g., in [21]. The block scheme of the digital voltage mode control and the buck converter circuit considered in this paper are shown in Figure 1. It is assumed that the converter operates in continuous-conduction mode (CCM).

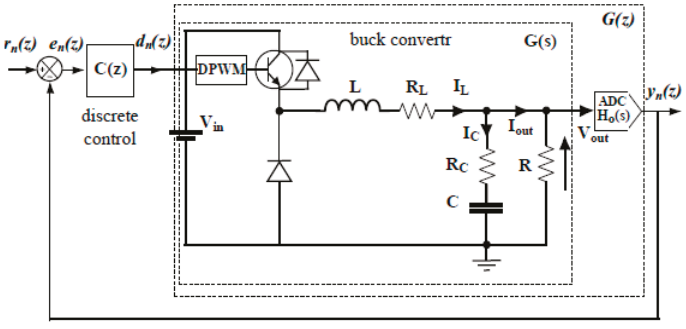


Figure 1. Switching DC-DC converter with digital voltage-mode control.

In the buck converter scheme, V_{out} is the output voltage, V_{in} is the input voltage, L is the filter inductance, C is the filter capacitance, R is the load resistance, R_L and R_C denote, respectively, the parasitic series resistances of the inductor and capacitor. Moreover, $r_n(z)$ represents the reference digital signal, while $y_n(z)$ denotes the sampled output of the process. The sampled signal is obtained by the analog-to-digital converter (ADC) with sampling period T_s. The tracking error signal $e_n(z) = r_n(z) - y_n(z)$ is processed by a discrete-time compensator $C(z)$ to generate the control signal $d_n(z)$. The Digital Pulse Width Modulator (DPWM) converts $d_n(z)$ into the corresponding analog duty cycle with values between 0 and 1 according to the desired ratio of V_{out}/V_{in}, and modulates the PWM signal to drive the buck converter switch.

The transfer function of the discrete plant model $G(z)$ is the Z-transform of the product of the continuous-time converter transfer function $G(s)$ and the transfer function of the zero-order hold:

$$H_0(s) = \frac{1 - e^{-sT_s}}{s}$$

with sampling period T_s:

$$G(z) = Z[H_0(s)G(s)]. \quad (1)$$

Notice that in the hardware device the output voltage of the buck converter is driven into the admissible range of the ADC input voltage by a constant sensor gain H; the resulting output signal of the ADC is then multiplied by the factor $1/H$ to be compared with the reference value r_n. In (1) the

factors $H \cdot (1/H) = 1$ have been simplified and omitted. According to the buck converter averaged model and Equation (2) of [21], the transfer function of the buck converter:

$$G(s) = \frac{V_{out}(s)}{d(s)} = V_{in} \frac{\left(1 + \frac{s}{\omega_o}\right)}{\left(1 + \frac{2\xi}{\omega_n} s + \frac{s^2}{{\omega_n}^2}\right)} \tag{2}$$

is a second-order low-pass filter, with a left-half complex plane zero introduced by the equivalent series resistance of the filter capacitance.

The mathematical averaged model is obtained by the following input/state/output equations, where the diode and transistor conduction losses have been neglected [22].

$$\underbrace{\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_C}{dt} \end{bmatrix}}_{\dot{x}(t)} = \underbrace{\begin{bmatrix} \frac{-R_L}{L} - \frac{RR_C}{L(R+R_C)} & \frac{-R}{L(R+R_C)} \\ \frac{R}{C(R+R_C)} & \frac{-1}{C(R+R_C)} \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} i_L \\ V_C \end{bmatrix}}_{x(t)} + \underbrace{\begin{bmatrix} \frac{V_{in}}{L} \\ 0 \end{bmatrix}}_{B} d(t),$$

$$V_{out}(t) = \underbrace{\begin{bmatrix} \frac{RR_C}{R+R_C} & \frac{R}{R+R_C} \end{bmatrix}}_{C} \underbrace{\begin{bmatrix} i_L \\ V_C \end{bmatrix}}_{x(t)},$$

where:

$$\omega_n = \frac{1}{\sqrt{LC\frac{R+R_C}{R+R_L}}},\ \omega_o = \frac{1}{R_C C},\ \xi = \frac{\omega_n}{2}\left(R_C C + \frac{RR_L C + L}{(R+R_L)}\right). \tag{3}$$

The discrete model of the buck converter is:

$$G(z) = V_{in} \frac{(1 - a - bc)z + e^{-2\xi\omega_n T_s} - a + bc}{z^2 - 2az + e^{-2\xi\omega_n T_s}}, \tag{4}$$

where:

$$a = e^{-\xi\omega_n T_s} \cos\left(\omega_n T_s \sqrt{1 - \xi^2}\right), \tag{5}$$

$$b = e^{-\xi\omega_n T_s} \sin\left(\omega_n T_s \sqrt{1 - \xi^2}\right), \tag{6}$$

$$c = \frac{\xi\omega_o - \omega_n}{\omega_o \sqrt{1 - \xi^2}}, \tag{7}$$

and it can be obtained by applying the definition of the Z-transform to the series plants $H_0(s)G(s)H$. Notice that $G(z)$ is characterized the following two complex conjugate poles:

$$z_{1,2} = e^{(-\xi \pm j\sqrt{1-\xi^2})\omega_n T_s}.$$

Indeed, from (1) it follows that:

$$G(z) = Z\left[\frac{1 - e^{-T_s s}}{s} G(s)\right] = \left(1 - z^{-1}\right) Z\left[\frac{G(s)}{s}\right] = \frac{V_{in}{\omega_n}^2}{\omega_0}\left(1 - z^{-1}\right) Z[R(s)],$$

where:

$$R(s) = \frac{s + \omega_o}{s(s^2 + 2\xi\omega_n s + {\omega_n}^2)}. \tag{8}$$

Expanding $R(s)$ into partial fractions we have:

$$\begin{aligned} R(s) &= \frac{\omega_o}{{\omega_n}^2}\frac{1}{s} - \frac{\omega_o}{{\omega_n}^2}\frac{(s+\xi\omega_n)+\left(\xi\omega_n-\frac{{\omega_n}^2}{\omega_o}\right)}{s^2+2\xi\omega_n s+{\omega_n}^2} \\ &= \frac{\omega_o}{{\omega_n}^2}\frac{1}{s} - \frac{\omega_o}{{\omega_n}^2}\frac{(s+\xi\omega_n)}{(s+\xi\omega_n)^2+{\omega_n}^2\left(1-\xi^2\right)} \\ &= -\frac{\xi\omega_o-\omega_n}{{\omega_n}^2\sqrt{1-\xi^2}}\frac{\omega_n\sqrt{1-\xi^2}}{(s+\xi\omega_n)^2+{\omega_n}^2\left(1-\xi^2\right)}. \end{aligned}$$

Applying the standard manipulation theorems of the Z-transform to $R(s)$ we have:

$$\begin{aligned} R(z) &= \frac{\omega_o}{{\omega_n}^2}\frac{z}{z-1} - \frac{\omega_o}{{\omega_n}^2}\frac{z^2-e^{-\xi\omega_n T_s}\cos(\omega_n T_s\sqrt{1-\xi^2})z}{z^2-2e^{-\xi\omega_n T_s}\cos(\omega_n T_s\sqrt{1-\xi^2})z+e^{-2\xi\omega_n T_s}} \\ &\quad -\frac{\xi\omega_o-\omega_n}{{\omega_n}^2\sqrt{1-\xi^2}}\frac{e^{-\xi\omega_n T_s}\sin(\omega_n T_s\sqrt{1-\xi^2})z}{z^2-2e^{-\xi\omega_n T_s}\cos(\omega_n T_s\sqrt{1-\xi^2})z+e^{-2\xi\omega_n T_s}}. \end{aligned}$$

It follows that (8) can be written as:

$$G(z) = V_{in} - V_{in}\frac{(z-e^{-\xi\omega_n T_s}\cos(\omega_n T_s\sqrt{1-\xi^2}))(z-1)}{z^2-2e^{-\xi\omega_n T_s}\cos(\omega_n T_s\sqrt{1-\xi^2})z+e^{-2\xi\omega_n T_s}}$$

$$-V_{in}\frac{\xi\omega_o-\omega_n}{{\omega_o}^2\sqrt{1-\xi^2}}\frac{e^{-\xi\omega_n T_s}\sin(\omega_n T_s\sqrt{1-\xi^2})z}{z^2-2e^{-\xi\omega_n T_s}\cos(\omega_n T_s\sqrt{1-\xi^2})z+e^{-2\xi\omega_n T_s}},$$

which can be rewritten as in (4) using (5)–(7).

3. The Proposed Discrete PIDF Controller with Complex Conjugate Zeros

The controller presented in this paper is a discrete PIDF controller, described by the following transfer function:

$$C(z) = \widetilde{K}_i\frac{z^2-2\delta_d\omega_d z+{\omega_d}^2}{(z-1)\left(z-\frac{\omega_n}{\beta_d}\right)}. \tag{9}$$

when:

$$\omega_d = e^{-\frac{\delta}{\tau}T_s},\ \delta_d = \cos\left(\frac{T_s}{\tau}\sqrt{1-\delta^2}\right),\ \beta_d = e^{(\beta-\delta)\frac{T_s}{\tau}},$$
$$\widetilde{K}_i = 2k_i\tau\beta\frac{1+e^{-\frac{\beta T_s}{\tau}}}{1+2e^{-\frac{\delta}{\tau}T_s}\cos\left(\frac{T_s}{\tau}\sqrt{1-\delta^2}\right)+e^{-\frac{2\delta}{\tau}T_s}},$$

the controller (9) represents the discrete pole-zero mapping transformation with the sampling period T_s of the following continuous-time PIDF controller:

$$C(s) = K_i\frac{1+2\delta\tau s+(\tau s)^2}{s\left(1+\frac{\tau}{\beta}s\right)}. \tag{10}$$

Here K_i is the integral gain, δ is the damping ratio and $1/\tau$ is the natural frequency of the controller zeros, and:

$$\beta = \frac{K_\infty}{\tau K_i}$$

is a parameter that depends on the high frequency controller gain, which is defined as:

$$K_\infty = \lim_{s\to\infty} C(s).$$

The PIDF controller (10) is equivalent to the classical parallel PIDF controller:

$$C(s) = K_p\left(1 + \frac{1}{sT_i} + \frac{sT_d}{1+sT_f}\right). \tag{11}$$

In fact, equivalent parameters for (11) can be obtained from δ, β, K_i, τ by equating (10) and (11): the resulting proportional gain, and the integral, the derivative and the filter time constants are shown in the following Equation (12):

$$K_p = K_i\frac{\tau}{\beta}(2\delta\beta - 1),\ T_i = \frac{\tau}{\beta}(2\delta\beta - 1),\ T_d = \frac{\tau}{\beta}\left(\frac{\beta^2}{2\delta\beta - 1} - 1\right),\ T_f = \frac{\tau}{\beta}. \tag{12}$$

Notice that when β > 1 and δ ≥ 1 the PIDF controller (10) reduces to a series PID controller, when 0 < β < 1 the PIDF controller has complex conjugate zeros, and when β = 1 and δ = 1 the PIDF controller becomes a PI controller, see [19].

Interestingly, the controller (9) can be written as a digital biquadratic filter:

$$C(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}, \tag{13}$$

where:

$$b_0 = \widetilde{K}_i,\ b_1 = -2\widetilde{K}_i\delta_d\omega_d,\ b_2 = \widetilde{K}_i{\omega_d}^2,$$
$$a_1 = -\left(\frac{\omega_d}{\beta_d} + 1\right),\ a_2 = \frac{\omega_d}{\beta_d},$$

which has the clear advantage of being directly implementable on a microcontroller by using the difference equation:

$$d[n] = \sum_{i=0}^{2} b_i e[n-i] - \sum_{j=1}^{2} a_j d[n-j]. \tag{14}$$

4. The Design Problem and the Proposed Design Solution

For control design purposes, the control system scheme can be simplified as in Figure 2, where $G(z)$ and $C(z)$ are given by (1) and (9), respectively, while $L(z)$ denotes the loop gain transfer function $L(z) = C(z)G(z)$.

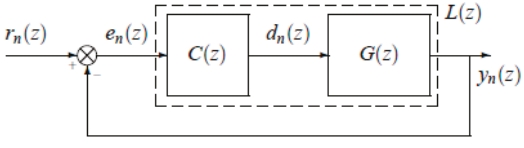


Figure 2. Block scheme of the digital control system.

4.1. Pole/Zero Compensation Method

The PIDF controller (9) introduces a pair of complex conjugate zeros, which can be placed to achieve pole/zero compensation. The PIDF parameters can be selected as follows:

$$\omega_d = e^{-\xi\omega_n T_s},\ \delta_d = \cos\left(\omega_n T_s\sqrt{1-\xi^2}\right), \tag{15}$$

where ξ and ω_n are the parameters of the buck converter described in (3). In this way, the transfer function of the controller can be factorized into two parts. The zeros and the integrator:

$$\frac{z^2 - 2\delta_d\omega_d z + {\omega_d}^2}{z-1} \tag{16}$$

are completely determined by the zero/pole cancellation. The remaining factor is:

$$\widetilde{C}(z) = \frac{\widetilde{K}_i}{z - \frac{\omega_d}{\beta_d}} \tag{17}$$

and it comprises the parameters that are yet to be assigned. Thus, we can consider a new control problem where the controller is $\widetilde{C}(z)$, while the former factor is part of the plant, whose transfer function then becomes:

$$\widetilde{G}(z) = G(z)\frac{z^2 - 2\delta_d\omega_d z + {\omega_d}^2}{z-1}.$$

4.2. Discrete Inversion Formulae Method

The design method based on the so-called "inversion formulae" consists in a set of closed-form expressions that deliver the parameters of the controller to exactly satisfy specifications on the gain crossover frequency ω_g, phase margin Φ_m and/or gain margin G_m. In most cases, these specifications are satisfied if the frequency response associated with the loop gain transfer function:

$$L(e^{\mathrm{j}\omega T_s}) = C(e^{\mathrm{j}\omega Ts})\, G(e^{\mathrm{j}\omega T_s})$$

at frequency ω_g satisfies:

$$\left|L(e^{\mathrm{j}\omega_g T_s})\right| = 1,\ \angle L(e^{\mathrm{j}\omega_g T_s}) = \Phi_m + \pi\,. \tag{18}$$

In other words, the design method based on the inversion formulae is a way of constraining the loop gain polar plot to cross a specific point of the complex plane. In practice, in the vast majority of the situations that are interesting in practice this goal alone is sufficient to guarantee that the specifications on the phase (or gain) margin and crossover frequency are met, see [15] for further details.

The classical feedback design problem is to find a controller $C(z)$ that satisfies the steady-state a zero position error specification, and such that the gain crossover frequency and the phase margin of the loop gain transfer function $L(z)$ are, respectively, ω_g and Φ_m.

The first step of the design method consists in guaranteeing that the steady-state requirement is met. In most situations, the pole at $z = 1$ of the controller is sufficient to automatically satisfy the steady-state requirements. However, in some cases, the number of poles at $z = 1$ of the plant and the single pole at $z = 1$of the controller are not sufficient to meet the desired static requirements, and the factor $\widetilde{K}_i$ in (9) must be chosen accordingly. For example, this is the case of a type-0 plant as the considered buck converter when the steady-state specifications not only require zero position error, but also that the velocity error (i.e., the tracking error in the response of a ramp) be equal to (or smaller than) a given non-zero constant. In the considered case specifications on the steady-state error do not lead to constraints in the value of the integral constant. Let $L(z) = \widetilde{C}(z)\widetilde{G}(z)$ be the loop gain transfer function. We define:

$$M_g \stackrel{def}{=} M(\omega_g) = 1/\left|\widetilde{G}(e^{j\omega_g T_s})\right|, \tag{19}$$

$$\varphi_g \stackrel{def}{=} \varphi(\omega_g) = \Phi_m - \pi - \angle\widetilde{G}(e^{j\omega_g T_s}). \tag{20}$$

The solvability of the feedback design problem amounts to solving the complex equation:

$$L(e^{\mathrm{j}\omega_g T_s}) = e^{\mathrm{j}(\Phi_m - \pi)}$$

in the unknowns $\widetilde{K}_i > 0$ and $\beta_d > 0$. The closed-form solution to this problem is given in the following theorem:

Theorem 1. *The values of $\widetilde{K}_i$ and β_d that solve the control problem are given by the following expressions:*

$$\beta_d = \frac{\omega_d}{\frac{\sin(\omega_g T_s)}{\tan(\varphi_g)} + \cos(\omega_g T_s)}, \tag{21}$$

$$\widetilde{K}_i = -M_g \sin(\varphi_g) \sin(\omega_g T_s) \left(1 + \frac{1}{\tan^2(\varphi_g)}\right). \tag{22}$$

Proof. From (18), the controller (17) has to be designed in such a way that:

$$\widetilde{C}(e^{j\omega_g T_s}) = M_g e^{j\varphi_g} = M_g(\cos\varphi_g + j\sin\varphi_g), \tag{23}$$

holds. The frequency response of (17) for $\omega = \omega_g$ can be written in Cartesian form as:

$$\widetilde{C}(e^{j\omega_g T_s}) = \frac{\widetilde{K}_i}{e^{j\omega_g T_s} - \frac{\omega_d}{\beta_d}}. \tag{24}$$

Equating (24) and (23) directly leads to (21) and (22). □

Remark 1. *It is easy to verify that the parameters β_d and $\widetilde{K}_i$ in (21) and in (22) are positive if and only if:*

$$\tan(\omega_g T_s) > -\tan(\varphi_g) \tag{25}$$

and one of the following conditions holds:

$$\begin{aligned}
&\bullet \omega_g \in \left[0, \tfrac{\pi}{2T_s}\right] && \textit{and} && \varphi_g \in \left[\pi, \tfrac{3}{2}\pi\right],\\
&\bullet \omega_g \in \left[\tfrac{\pi}{2T_s}, \tfrac{\pi}{T_s}\right] && \textit{and} && \varphi_g \in \left[\tfrac{3}{2}\pi, 2\pi\right],\\
&\bullet \omega_g \in \left[\tfrac{\pi}{T_s}, \tfrac{3\pi}{2T_s}\right] && \textit{and} && \varphi_g \in \left[\tfrac{\pi}{2}, \pi\right],\\
&\bullet \omega_g \in \left[\tfrac{3\pi}{2T_s}, \tfrac{2\pi}{T_s}\right] && \textit{and} && \varphi_g \in \left[0, \tfrac{\pi}{2}\right],
\end{aligned}$$

or:

$$\tan(\omega_g T_s) < -\tan(\varphi_g) \tag{26}$$

and one of the following conditions holds:

$$\begin{aligned}
&\bullet \omega_g \in \left[0, \tfrac{\pi}{2T_s}\right] && \textit{and} && \varphi_g \in \left[\tfrac{3}{2}\pi, 2\pi\right],\\
&\bullet \omega_g \in \left[\tfrac{\pi}{2T_s}, \tfrac{\pi}{T_s}\right] && \textit{and} && \varphi_g \in \left[\pi, \tfrac{3}{2}\pi\right],\\
&\bullet \omega_g \in \left[\tfrac{\pi}{T_s}, \tfrac{3\pi}{2T_s}\right] && \textit{and} && \varphi_g \in \left[0, \tfrac{\pi}{2}\right],\\
&\bullet \omega_g \in \left[\tfrac{3\pi}{2T_s}, \tfrac{2\pi}{T_s}\right] && \textit{and} && \varphi_g \in \left[\tfrac{\pi}{2}, \pi\right].
\end{aligned}$$

Note that, if one of the previous conditions fails, the required frequency-domain constraints are infeasible. In other words, the devised inversion formulae provide a solution whenever a feasible solution exists.

It is worth stressing that the proposed approach is based on closed-form expressions that deliver a discrete-time PIDF controller that satisfies exactly the design specification. This is clearly a major advantage since the imposed stability margin is guaranteed, and it is not subject to variations induced by the discretization method.

5. Design of the Buck Converter

5.1. Design Problem

The aim of this section is to apply the proposed designed procedure to the buck converter circuit with the parameters given in Table 1. The steady state requirement is zero position error, while the phase margin and the gain crossover frequency of the open loop frequency response are required to be equal to $\Phi_m = 85^\circ$ and $\omega_g = 1600$ rad/s, respectively.

Table 1. Circuit parameters of the buck converter.

Parameter	Symbol	Value	Units
Input voltage	V_{in}	20	V
Reference voltage	V_{ref}	12	V
Filter Capacitance	C	100	μF
Filter Inductance	L	680	μH
Load resistance	R	20	Ω
ESR of capacitor	R_C	170	$m\Omega$
ESR of inductor	R_L	173	$m\Omega$

5.2. Proposed Solution Using Discrete-Time PIDF Controller

The discrete plant (4) of the buck converter with the parameters given in Table 1 and with sampling period T_s equal to 5×10^{-5} s is:

$$G(z) = \frac{0.603\ z + 0.1122}{z^2 - 1.916z + 0.9513}. \tag{27}$$

The same result can be obtained using the zero-order-hold discretization method on the transfer function of the continuous time averaged model (2):

$$G(s) = \frac{V_{out}(s)}{d(s)} = \frac{5001s + 2.942 \times 10^8}{s^2 + 998.1s + 1.471 \times 10^7}. \tag{28}$$

The steady-state requirements are automatically satisfied by the pole at $z = 1$ of the discrete PIDF controller. Its zeros can be designed to cancel the complex poles of $G(z)$ at $0.96 \pm j\ 0.18$ by selecting $\delta_d = 0.982$ and $\omega_d = 0.97$ rad/s in (9). It follows that:

$$\widetilde{G}(z) = \frac{0.603\ z + 0.1122}{z - 1}. \tag{29}$$

The complex value $\widetilde{G}(e^{\,j\omega_g T_s}) = 8.94\ e^{\,j\,1.54}$ determines the gain $M_g = 1/8.94 = 0.11$ that the controller has to introduce at frequency ω_g, and the phase $\varphi_g = 85^\circ + 180^\circ + 88.4^\circ = 353.4^\circ$ of the controller at ω_g needed to satisfy the design specification on the phase margin. The parameters of the PIDF controller (9) that solves the problem are $\beta_d = 3.22$, $\widetilde{K}_i = 0.078$, and follow directly from (21–22). The resulting PIDF transfer function is:

$$C(z) = \frac{0.0781z^2 - 0.1496z + 0.0743}{z^2 - 1.303z + 0.3033}, \tag{30}$$

which can also be rewritten as:

$$C(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}, \tag{31}$$

with $a_1 = -1.303$, $a_2 = 0.3033$, $b_0 = 0.0781$, $b_1 = -0.1496$, $b_2 = 0.0743$. Applying this discrete controller, the design requirements are exactly satisfied, as one can observe by the Nyquist and Bode plots of the open loop frequency response $L(e^{\,j\omega T_s})$ shown in red in Figures 3 and 4. The step response of the

controlled system is plotted in red in Figure 5 showing the effectiveness of the control in the time domain. Notice that selecting a different value of the sampling time T_s causes the complex conjugate poles of the discrete plant to shift in the complex plane. In this case, new values of δ_d and ω_d can be computed according to (9) as functions of T_s to exactly cancel the shifted poles.

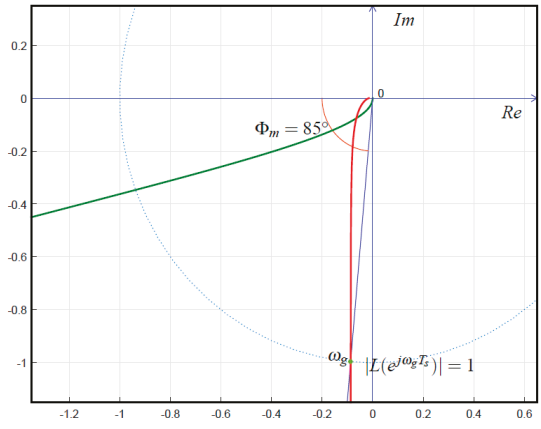


Figure 3. The Nyquist plot of the frequency response of the buck converter (green), and of the open loop frequency response with the discrete-time inversion formulae (red).

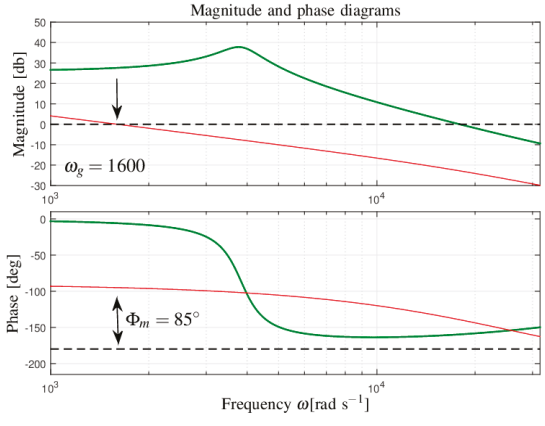


Figure 4. Bode diagrams of the frequency response of the buck converter (green), and of the open loop frequency response with the discrete-time inversion formulae (red).

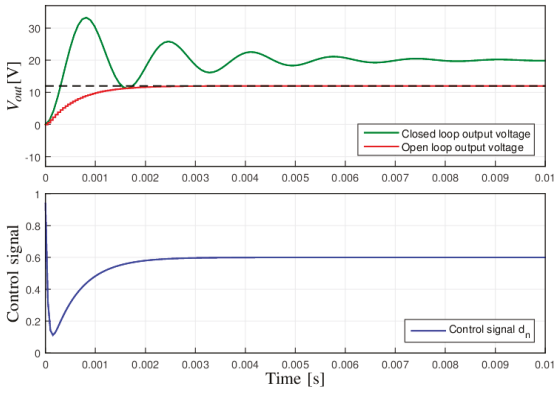


Figure 5. Open-loop step response (green), closed-loop step response (red) and the corresponding control variable (blue).

5.3. Simulation and Experimental Results

The proposed control system for the buck converter regulation has been extensively simulated in MATLAB-Simulink® using the model shown in Figure 6. As a first step, the PIDF controller has been tested introducing the discrete transfer function block contained in the Simulink® library. Then, this block has been substituted with the Infinite Impulse Response (IIR) digital filter shown in Figure 7, which has the advantage to be directly implementable by a microcontroller algorithm.

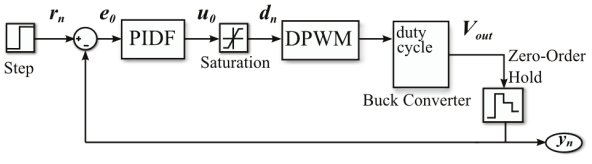


Figure 6. MATLAB-Simulink® model of the buck converter and control system.

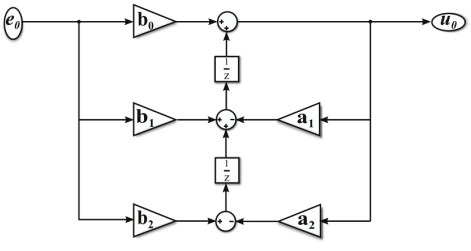


Figure 7. Discrete-time PIDF controller model: biquad cascade IIR filters using a direct form II transposed structure.

The control signal d_n, the inductor current and the output voltage of the converter and inductor under step reference variations from 0 V to 12 V are shown in Figure 8 from which the smoothness and monotonicity of the response achieved with our method can be clearly observed, as well as the notching effect of the complex conjugate zeros, which is well-visible in the first part of the transient response of the control signal. It is also worth noting that the simulated response and the experimental one exhibit a very good matching, demonstrating that our model is effectively descriptive of the real-world buck converter.

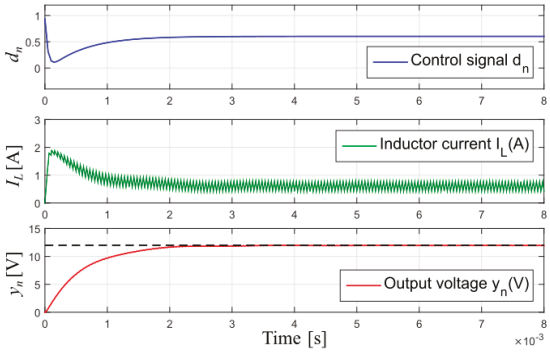


Figure 8. Simulated control signal, inductor current and output voltage under step variation of the reference value from 0 V to 12 V using the proposed control method.

An experimental hardware device has been built to verify the proposed method for the DC-DC buck converter. It is composed by the buck converter and an Arduino Due development board, based on a 32-bit Atmel SAM3X8E ARM® Cortex® M3 CPU, see Figure 9. The main components of the buck converter circuit have been selected as shown in Table 1.

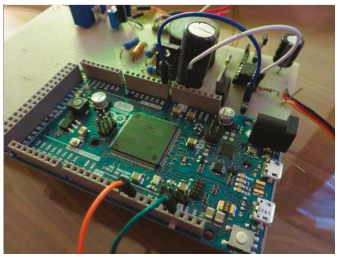


Figure 9. Physical realization of the buck converter.

An interrupt routine is generated every $T_s = 5 \times 10^{-5}$ s. This routine starts the ADC conversion of the output signal of the converter and computes the duty cycle of the PWM control signal. Figure 10 represents the difference Equation (14) of the PIDF controller using the Direct-Form II Transposed structure of a Biquad Cascade IIR Filter shown in Figure 7.

```
//·PIDF·control·algorithm
//·implemented·in·Arduino·board
u0·=·b0·*·e0·+·q1;

q1·=·b1·*·e0·-·a1·*·u0·+·q2;
q2·=·b2·*·e0·-·a2·*·u0;
```

Figure 10. The Biquad Cascade IIR Filter algorithm.

The output voltage of the converter and inductor current I_L under step reference variations from 0 V to 12 V are shown in Figure 11. The measure of I_L has been obtained using the analog transducer LEM 6−*NP* with a 5V supply and a galvanic isolation between the primary and the secondary circuit. The experimental results confirm the behavior already observed in the simulations: the output voltage reaches the desired value in a monotonic fashion, and the inductor current remains always well below

the saturation value. A zoom of the inductor current sensor output in steady-state condition is shown in Figure 12 from which the regularity of the PWM duty cycle when the system has reached the new steady-state can be observed. This is a consequence of the selected bandwidth, which is large enough to obtain a fast set point tracking, but narrow enough to avoid the amplification of high frequency noise and discontinuities due to the PWM behavior. Note that assigning such bandwidth without cancelling the complex conjugate poles would result in large oscillations due to the presence of the resonance peak in the closed-loop system.

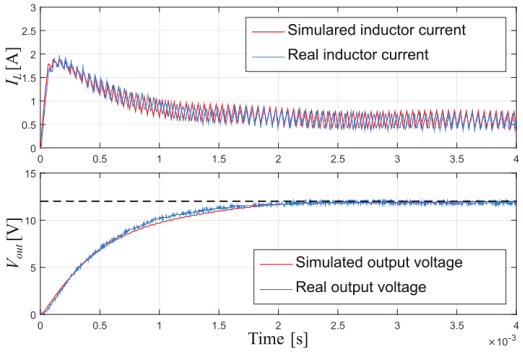


Figure 11. Experimental result using PIDF and the proposed method: inductor current sensor output and converter output signal under reference step variation from 0 V to 12 V.

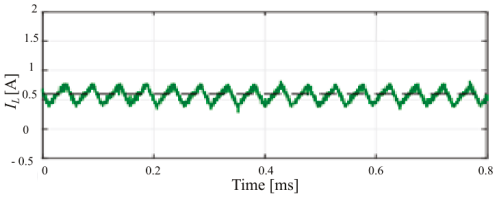


Figure 12. Experimental result using PIDF: zoom of the inductor current sensor output in steady-state condition.

5.4. Comparison with Other Methods

There are various design techniques for determining the parameters of a PID controller when the mathematical model of the plant is explicitly available. For a comparison with the proposed design method, three classical PID tuning techniques have been considered, see Table 2.

Table 2. PID parameters.

Control	K_p	K_i	K_d
IMC-Chien	0.033	958.7	6.519×10^{-5}
Pole placement	0.55	247.1,	7.353×10^{-5}
Pole-zero cancellation	0.02	294.7	2.004×10^{-5}

The first controller has been obtained using the Internal Model Control IMC-Chien method described in [23], and by neglecting the capacitor and inductor resistances in (2). The second has been obtained by placing one zero of the PID controller an octave below the cut-off frequency, approximately at 480 rad/s, while the other zero has been placed at 7×10^3 rad/s, see [12]. The third controller has been obtained by selecting the PID zeros to approximately cancel the complex conjugate poles of the converter at the cut-off frequency and a phase margin equal to 95°, see [10]. The considered

continuous-time PID controllers have been simulated via the Simulink® PID(*s*) block which implements a PID controller in the form:

$$C_{PID}(s) = K_p + \frac{K_i}{s} + K_d \frac{N}{1 + N/s}. \quad (32)$$

The MATLAB-Simulink® PID(*s*) model uses a lowpass filter in the derivative term to obtain a proper transfer function. The default value of the coefficient N in the filter is set at 100. Using this value in (32), all the considered PID controls generate large oscillations during the step response transient. These oscillations are considerably reduced by setting the coefficient N of the filter to the value N = 200,000. It is clear that the time constant of the filter is a critical component in the design of a PID controller and that a systematic design method should be taken into account. Accordingly, in our method, the time constant of the filter is selected to achieve the desired closed-loop system performance, and it is not designed by using trial-and-error, empiric or rule-of-thumb methods.

For the practical implementation of the controller on the Arduino board, the continuous-time PID controllers are converted to the discrete-time by using the backward Euler's integration method, as suggested in [10]. The discrete control algorithm will therefore implement the causal difference equation:

$$d[n] = K_p e(n) + K_i T_s \sum_{i=0}^{n} e(n) + \frac{K_d}{T_s}[e(n) - e(n-1)].$$

Moreover, an anti-windup filter based on the conditional integration method (see [24] for details) has been implemented in order to minimize the detrimental effect of the large saturation resulting from the techniques listed in Table 3.

Table 3. Phase margin variations from continuous to discrete-time control using backward Euler's discretization method.

PID Control	Phase Margin		
	Continuous-Time	Discrete-Time	
		N = 100,000	N = 200,000
IMC-Chien	90°	47.5°	50.5°
Pole placement	98.6°	26.3°	29.5°
Pole-zero cancellation	95.7°	65.2°	67.6°

The simulated step responses of these three methods in the continuous-time are shown in Figure 13. The simulated step response using the IMC-Chien method is very fast, with a settling time of 0.2 ms. However, the peak of the resulting control signal is approximately 80.

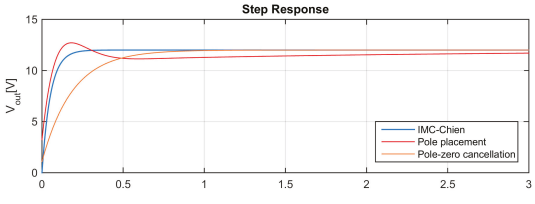


Figure 13. *Cont.*

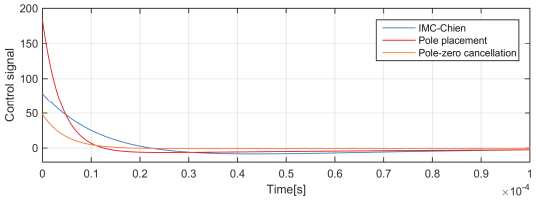


Figure 13. Simulated step responses using IMC-Chien method, the pole placement method and pole-zero control method in the continuous-time case: output voltages and control signals.

On the other hand, the saturation of the duty cycle range [0,1] leads to an oscillatory behavior in the experimental output voltage, see Figure 14b. In fact, the resulting settling time is 20 times greater than the one obtained in the simulated test. Moreover, a steady-state ripple in the output voltage and in the inductor current is present because of the excessively aggressive tuning.

The simulated continuous-time step response using the pole placement method exhibits a rise time of 8.1×10^{-5} s, a settling time of 4.2 ms, and an overshoot equal to 6%. As in the previous case, the control signal reaches a very high value, in this case with a peak of nearly 180. The converter signals obtained using this control method in the experimental hardware device are shown in Figure 14c. The main drawback of this type of control is the large steady-state ripple in the output voltage, see [10]. This is due to an excessively large closed-loop bandwidth that results in an aggressive control action which tries to compensate the high frequency noise. The saturation of the duty cycle in the range [0,1] leads to an ON-OFF behavior in the hardware device and high power dissipation both during the transient response and in the maintenance of the steady-state. Note also that the voltage ripple is unsuitable for most sensitive electronic equipment and the resulting current may cause heating and damage of capacitors over time, see [25].

The simulated continuous-time step response using the pole-zero cancellation method has a rise time of 4.1×10^{-4} s, a settling time of 0.7 ms. The peak of the control signal is 48, which is considerably lower than the ones obtained with the previously described techniques, but still orders of magnitude above the saturation level. The corresponding experimental results are shown in Figure 14d. Notice that the steady-state output ripple is not present using this type of control because of the less aggressive tuning of the parameters, which also results in a lower peak of the control variable. However, the non-linear saturation of the control signal is not considered in (2). As a consequence, the zeros of the controller only partially compensate the oscillatory effects of the buck converter poles in the transient period. It follows that the settling time rises to 4 ms in practice, and the experimental output voltage exhibits an oscillatory behavior with an overshoot of 20–30%.

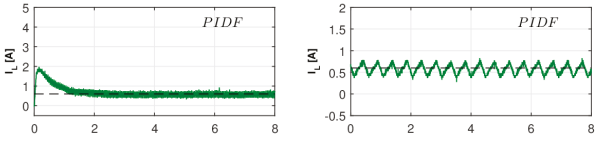


Figure 14. *Cont.*

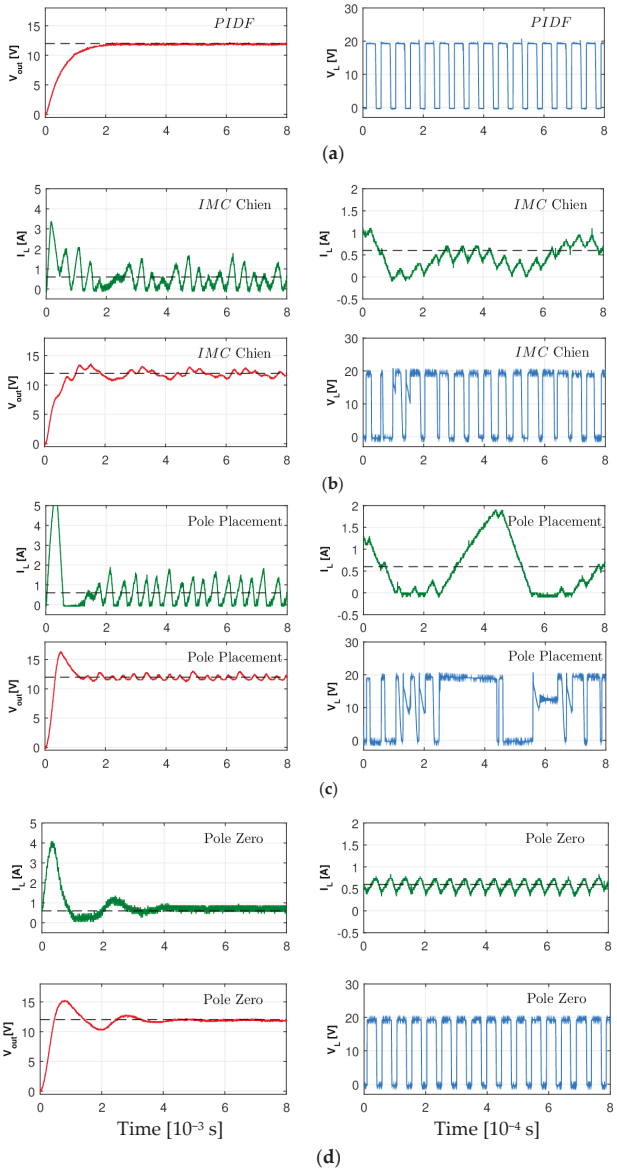


Figure 14. Inductor current and output voltage under step variation of reference value from 0 V to 12 V and zoom of inductor current and inductor current at steady-state using: (**a**) Inversion Formulae, (**b**) IMC-Chien, (**c**) Pole Placement, and (**d**) Pole Zero methods.

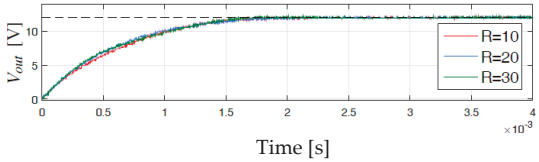
Compared to all the considered methods, the proposed control procedure leads to a good matching between simulated and experimental results, due to the design which is carried out directly in discrete-time via closed-form formulae. As such, the phase margin that we obtain with the discrete PIDF controller is exactly the design one. On the contrary, other approaches are based on the design of the controller in the discrete domain, and eventually, on the discretization of the obtained continuous controller. However, this results in a discrete controller that often delivers a phase margin considerably different from the one that

would have ideally been obtained in the continuous time, see Table 2, where the phase margins obtained from the considered methods and a discrete PID of the following form are presented:

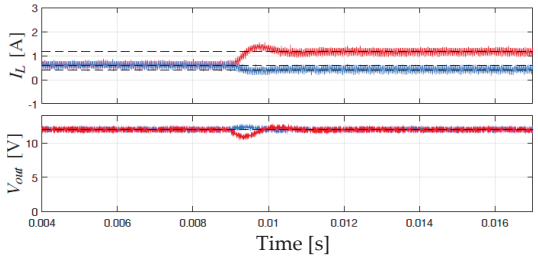
$$PID = K_p + K_i T_s \frac{z}{z-1} + K_d \frac{N}{1 + N T_s \frac{z}{z-1}}.$$

5.5. The Proposed Control under Output Load and Converter Parameters Variations

For the widespread diffusion of a control technique in practical applications, robustness to parameter variation and model uncertainty is clearly a key feature. For this reason, we study the behavior of the output voltage under different load resistance variations. Experimental results of the step load testing under different output loads (10 Ω, 20 Ω and 30 Ω) are shown in Figure 15a. Notice that the output voltage presents an almost overlapping behavior in the three considered cases, confirming that the control is not affected by load variation in the range ±50% of the nominal value, see Table 1. Other experimental results on load variations from 20 Ω to 10 Ω and from 20 Ω to 30 Ω in steady-state condition are shown in Figure 15b. Notice that the proposed control system promptly stabilizes the voltage output with negligible undershoot and overshoot, thus providing a good performance in the case of load variations. Moreover, the set-point step response remains virtually the same irrespectively of the load resistance.



(**a**)



(**b**)

Figure 15. (**a**) Step responses under different output loads (10 Ω, 20 Ω and 30 Ω), (**b**) inductor current and output voltage under load variation from 20 Ω to 30 Ω (blue), and from 20 Ω to 10 Ω (red).

While load variations are due to normal operations of the buck converter, other parameters of the circuit of the converter, such as the inductance and capacitance, may vary as well as a result of the uncertainties affecting the production of the electrical components. In particular, the resonance frequency is directly related to the inductance and capacitance. In fact, since $R>>R_C$ and $R>>R_L$, in practice we have:

$$\omega_n \cong \frac{1}{\sqrt{LC}}.$$

Therefore, the inductor current and the output voltage under variations of the capacitor and inductor in the buck converter are also studied, and the results are shown in Figures 16 and 17. The proposed system delivers a good robust performance under parameter variations, and a monotonic response is obtained with all the considered combinations.

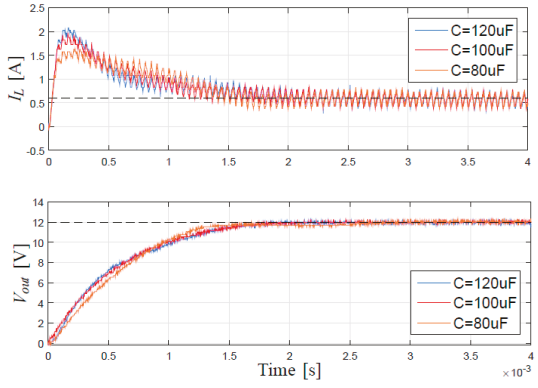


Figure 16. Step responses with the proposed design procedure when the model value of the capacitor is 100 µF−20%, 100 µF+20%.

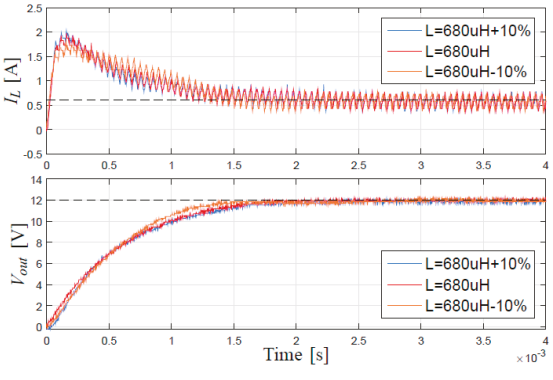


Figure 17. Step responses with the proposed design procedure when the model value of the inductor is set to 680 µH−10% and 680 µH+10%.

6. Conclusions

A new design framework for the control of buck converters has been presented in this paper. The proposed methodology is based on the discrete PIDF controller, and hinges on a direct design procedure that can be easily implemented in any non-specific platform. Indeed, the proposed methodology delivers a closed-form solution to meet suitable phase margin and gain crossover frequency values without a simulation environment. Moreover, the proposed design procedure and the discrete control algorithm are simple, they require small tuning times and they can be implemented by inexpensive microcontrollers.

Numerical and experimental verifications confirm that the proposed method goes well beyond the well-known zero/pole cancellation strategy and other control methods available in the literature. Indeed, the proposed approach enables the designer to assign an arbitrary bandwidth, which is therefore no longer constrained by the resonant peak. This aspect leads to a double benefit. On the one hand, this method avoids an excessively large bandwidth, which would result in noise/ripple amplification and ultimately in an increase in power consumption and a decrease in the component life. On the other hand, this method avoids the discretization problem that derives from discretizing a controller which assigns a bandwidth that is too large with respect to the sampling period. This, in particular, avoids detrimental effects on the stability margin due to the discretization. Moreover, experimental results confirm that the selection of large phase margin with the direct proposed method delivers a good system performance under load variations and plant uncertainties.

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Abbreviations

The following abbreviations and symbols are used in this manuscript:

ADC	Analog-to-digital converter
CCM	Continuous-conduction mode
DC	Direct current
DC-DC	Direct current to direct current
DPWM	Digital pulse width modulator
ESR	Equivalent series resistance
IIR	Infinite impulse response (digital filter)
IMC	Internal model control
PI	Proportional-integral (controller)
PID	Proportional-integral-derivative (controller)
PIDF	PID + filter
PWM	Pulse width modulation
List of Symbols	
a_i, b_i	PIDF coefficients
C	Buck converter capacitance
$C(s)$, $C(z)$	Continuous and discrete-time controller transfer function
D	Control signal
E	Tracking error
$G(s)$, $G(z)$	Continuous and discrete-time plant model
G_m	Gain margin
H	Constant sensor gain
$H_0(s)$	Zero-order hold transfer function
i_L	Buck converter inductor current
K_d	Controller derivative gain
K_i	Controller integral gain
K_∞	High frequency controller gain
K_p	Controller proportional gain
L	Buck converter inductance
$L(s)$, $L(z)$	Continuous and discrete-time loop gain transfer function
N	Filter coefficient
R	Output load resistance
R_C	ESR of buck converter capacitor
R_L	ESR of buck converter inductor
r_n	Reference digital signal
T_d	Derivative time constant of the controller
T_f	Filter time constant of the controller
T_i	Integral time constant of the controller
T_s	Sampling period
u_0	Output signal of IIR filter
V_C	Buck converter capacitor voltage
V_{in}	Buck converter input voltage
V_{out}	Buck converter output voltage
V_{ref}	Reference voltage
y_n	Sampled output of the process

δ	Damping ratio of the controller zeros
Φ_m	Phase margin
ξ	Buck converter damping ratio
ω_g	Gain crossover frequency
ω_n	Buck converter natural frequency
$1/\tau$	Natural frequency of the controller zeros

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Comparison of Novel Approaches to the Predictive Control of a DC-DC Boost Converter, Based on Heuristics

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Abstract: This paper introduces novel approaches to the predictive control of a DC-DC boost converter and a comparison of the controllers built that consider all of the current objectives and minimize the complexity of the online processing. The primary concern is given to the applicability of the inclined methods for systems that are physically small but considered physically fast processes. Although the performed methodologies are simulated and applied to a DC-DC boost converter, they can have broader applicability for different switched affine systems as a subgroup of the hybrid systems. The introduced methods present an alternative way of building the process model based on the fuzzy identification that contributes to the final objective: the applicability of the predictive methods for fast processes.

Keywords: switched affine systems; hybrid systems; fuzzy identification; fuzzy modeling; two degrees of freedom; fuzzy model predictive control

1. Introduction

Predictive control has strict conjunction with the rendering of a proper mathematical model that will be used to determine a successor step of our control algorithm. Subsequently, the modeling paradigm must become the core issue in projecting the predictive control algorithm of the cyber-physical and the physical processes in general. Even though the process is purely natural, meaning it is a naturally continuous system, influenced by the control algorithm, it will undoubtedly evolve into the Hybrid System (HS). That is why this study points out the results from the aspects of HS controls in the field of Switched Affine Systems (SAS). Nowadays, the majority of power electronics uses a kind of Pulse Energy Conversion or Converters (PEC) in rendering the power sources or control signals. Consequently, these systems are in the group of SAS.

In this study, an alternative approach to modeling a DC-DC boost converter has been provided, and our SAS example is taken into consideration as a good representative of the aforementioned field. A renaissance of the HS theory occurred in 1990s. Simultaneously, the emerging of heuristic control principles happened: neural networks and fuzzy control. The findings of those two mostly separately developed fields will be integrated into the new approaches of the model-based predictive control of SAS. It is necessary to highlight that from the corner of the HS theory, the PEC is analytically definable and well posed [1]. From the aspects of applicability, we promote the transformation of HS to the purely continuous, although this principle is found to be incomplete by the HS theory [1]. This is mainly disproven by the inapplicability of the particular HS approaches to fast physical processes. Therein, the assumption that each particular physical process can be presented by Discrete Hybrid Automata (DHA) does not hold. In referring to the qualitative mathematical theory [2], and the need in DHA to synchronize all of the dynamic events, one faces the problem of multiple dynamics that cannot

be unified simply. In previous work [3,4], the modeling was put into the focus and given possible solutions from the physical aspects of the system. First, in [3], the main problem is transferred to the idea of infinity horizon principle. It is comparable with the Model Predictive Control (MPC) infinite horizon, but it should not be mistaken for it. Second, in [4], the problem is grasped with an idea of two dynamics and unified into one by fuzzy logic (FL).

Some previous academic work have provided remarkable results in applying the advanced control algorithms for the relatively simple example of SAS: a DC-DC boost converter [5–13]. As a result, this article underlines the complexity of the controls of the DC-DC boost converter. This complexity has to be known in order to form a more solid basis for understanding the necessity for the advanced control algorithm. The assigned objectives in the control of DC-DC boost converters are the main complexity issue. Consequently, in this study, the standard objectives have been provided, as well as additionally extended with the objective of the applicability issue. The objectives are:

- Robustness to the wide system's parameter changes [PCR]
- Short response period and similar to all different operating points [SR]
- Optimality related to constraints [OPT]
- Stability [S]
- Minimization of the nonlinear phenomena for the selected robustness [NFM]
- Applicability to the systems with fast refresh rate. [A]

The above-mentioned has to determine the reason for finding a new and advanced approach that can integrate all of the objectives, even though established and notable approaches already exist [5,7,11]. Those methodologies are successful in newer releases [14,15], but are still a continuation in a way similarly improving the main and present issues, the processing complexity, and the system discontinuity. The originators of the modeling principles in their releases [5,6,16] direct the modeling to the direction of identification, because of the compelling interest in minimizing the processing complexity. We see that there is still a possibility to improve the well-articulated problems of system discontinuity and processing complexity by reducing the prediction horizon [17], which is the fundamental stability pillar of the MPC in general. Also, generally for the HS, it is essential to bear in mind that distributing or decoupling the modeling complexity into the several and less complex HS models might be the solution, i.e., current, voltage and feedback; however, then the synchronization of those models to the one and overall DHA should not be endangered [1]. Considering that the main fundament of this study is the presentation of Identification-Based (IDB) modeling and a comparison of those modeling-based control algorithms, Figure 1 presents it in a broader view. In contrast to typical and basic model representatives in HS [1], i.e., Piece Wise Affine (PWA) models, Linear Complementarity (LC) models, Extended Linear Complementarity models (ELC), Mixed Logical Dynamical (MLD), and Max-Min-Plus-Scaling (MMPS), the Identification-Based (IDB) modeling represents a new group of models rendered by different identification approaches and algorithms that partly identify the uncertainties in HS models or completely, as in the example of this study. Additionally, and to achieve the selected objectives, the new approach will contain the model-based predictive control strategy reformulated to accommodate the above-mentioned nonlinear system's dynamics problem. As a continuation of previous work [3,4], this study will concentrate more on the comparison of controllers that are rendered by the novel methodologies in seeking more advanced control solutions. Additionally, the subsequent discussion has to contribute to a better understanding of the novelty in the predictive controls that can be widely exploited. Originally, the main goal was to provide a more compact and applicable solution for the DC-DC boost converter that can be integrated into different, more complex, and practical problems. The main complexity is here grasped in the system's model structure and performed offline. The lifted modeling accuracy that is gained by the identification of a constructed process on the site can help in distinguishing and diagnosing other process problems, as discussed in [18]. In contrast, it can block the nonlinearities produced by the semiconductors realistically, and not be injected by the trivial nonlinear switching functions, but still

be compact in forming the overall model for the more complex examples in [19,20]. It will be all based on assumptions that the system states are measurable and the switching period T_s is fixed. Subsequently, Section 2 provides a discussion of the distinctive problems in the modeling of SAS that contributes to the complexity and places the novel solution into the methodology frames that are of crucial importance for the understanding of latter compared controllers. Section 3 presents the successfully applied methods and comparison of the achieved results, and Section 4 contains the short conclusion.

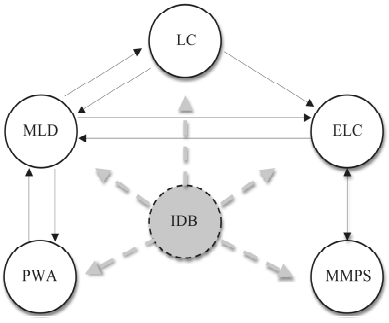


Figure 1. Established types of hybrid models and novel modeling in a Hybrid System (HS).

2. Novel Modeling Paradigm and Predictive Control of a DC-DC Boost Converter, Minimization of Online Processing

Predictive control must be the main strategy in achieving the robustness and optimality of the final control algorithm of a DC-DC boost converter. Optimality in the controls of the DC-DC boost converter must be seen through the system's constraints. The main constraints are the voltage source $E(t)$, the inductor current $i_L(t)$ and duty cycle $d(t)$. In Figure 2, a principal electronic circuit of a DC-DC boost converter is presented, and assigning the mentioned circuit constraints additionally including the converter's voltage set point s, the output voltage v_o, the load current i_R and the capacitor's voltage v_c.

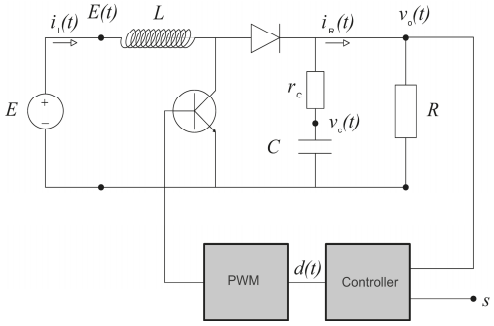


Figure 2. DC-DC boost converter circuit diagram.

To predict a successor control signal of a new control algorithm, a process model has to be known, as well as measured or observed antecedent data. In our case the process model is a mathematical model of the system presented in Figure 2. Mostly, and as already mentioned, in the broader literature of DC-DC boost converters, several different models are known. Based on the authors' opinions and knowledge about this particular system, the following distinctive and established methodologies are available:

- Small and large signal modeling [12,13]

- Poincaré mapping in discontinuous conduction mode (DCM) [7]
- HS based modeling; Mixed Logical Dynamical and Linear Complementarity [11,21,22].

Those modeling principles address most of the modeling problems of a DC-DC boost converter, but from the control theory point of view and applicability, there is room for improvement. It is unlikely that the answer or a predefined block that precisely models our natural process could be found in the modern computer toolboxes. Looking from the simulation side and finally from the control side, different natural processes can be similar. Furthermore, the modeling formalisms are prone to upgrades. A good example is HS formalisms and their development [1]. In the high refresh-rate systems, and before developing the control algorithm, the awareness about proven anomalies that can produce a significant impact on our control algorithm must be present. In the example of a DC-DC boost converter, we highlight the three most distinctive ones:

- Anomalies caused by the system nature [1,2]
- Anomalies caused by the modeling formalisms [23,24]
- Anomalies caused by the control algorithm itself [2,7].

A DC-DC boost converter is a cyber-physical process, which by its nature has a controllable switching process that automatically groups it in SAS as a subgroup of HS. If the switching event would be a time-wise insignificantly short in comparison with the discretization, or if the switching event is just occasionally appearing, then the importance might be minimized or simply distinguished by one bit of information. Otherwise, the significance of that event has to be reconsidered. The pulse width modulation (PWM) of our example is exactly the core issue in the control of a DC-DC boost converter, and subsequently, it has to be viewed through the mentioned existence of the possible anomalies.

The switching event over the semiconductors is burdened with the sticking and grazing effects over the switching manifolds [2]. For the selected physical system, these anomalies are considered natural.

In an application in which we use the HS formalisms, we must be aware of the typical anomalies as "Live lock" and "Zeno" effect [1,2,23,24].

Conclusively, when the control algorithm is in operation, the awareness of the nonlinearity phenomena recognized in bifurcations and chaos come into focus and must be treated by the control algorithm itself.

An elevation of the grade of modeling accuracy, in order to avoid previously mentioned anomalies, raises the complexity of the model and consequently the control algorithm, but it is of great importance in the stability of predictive control. Additionally, at the same time, it minimizes the nonlinearity phenomena. The mentioned complex view on modeling and the contemporary minimization of the limited time of processing bring this discussion to an alternative solution that integrates and conciliates two from the first sight disputable extremes. In our previous work [3,4], as the answer on demanding tasks, the fuzzy logic-based control algorithms successfully provide the possible solution for expressed complexity, and these will be compared here, including the two additional MPC controllers that are not yet presented, but are based on the same modeling principle. The fuzzy logic is not used traditionally [9,10,25] in a way to formulate the nonlinear gain interpolation, but differently to approximate the complex system model and answer positively to all of the objectives that have been collected together. The modeling benefits that are basically derived from the fuzzy system identification are threefold.

First, apart from the HS structure, in this way the system can be interpreted as a purely continuous system; in the worst-case scenario, it maintains the same grade of accuracy as the HS modeling approach.

Second, it provides the final model that is a more compact solution and minimizes the online processing burden of the control algorithm.

Third, in practical solutions, and because it is based on identification, this modeling principle provides the physical characteristics of the electronic circuits in real operation, which overcomes all possible theoretical miscalculations at once.

To understand the novelty of subsequently compared control algorithms, and to frame the modeling methodologies to the unique approach in studies of a DC-DC boost converter, we highlight the main idea. The most distinct characteristic of the new control algorithms is found in the non-analytical but heuristically-based modeling of a DC-DC boost converter. The source models are Takagi-Sugeno (T-S) fuzzy models derived from the mathematically transferred and normed space of measured system states [3,4]. Thus, naturally, the process of measuring, or in the simulation environment the numerical integration, transfers the originally and analytically two-dimensional state space problem of the DC-DC boost converter states $\boldsymbol{x}_a = [v_c \; i_L]^T$ in the six-dimensional $\overline{\boldsymbol{x}} = [\overline{v}_o \; \overline{i}_L \; \overline{E} \; \overline{R} \; d \; t]^T$ normed vector space $(V, \|\cdot\|)$. The newly formed and augmented pseudo-Banach space is derived from the Lebesgue 2 norming of the process variables $\|\cdot\|$, which is expressed by

$$\|x_i\|_{L^p} = \frac{1}{t}\left(\int |x_i|^p dt\right)^{\frac{1}{p}} = \overline{x}_i, \; for \; p = 2 \; and \; i \in [1, 4]. \tag{1}$$

In the above-developed space, the new methodologies perform a different grey box fuzzy identification process to derive the final fuzzy model of a DC-DC boost converter.

The physical process constraints due to the electrical components that were used in the electric circuit presented in Figure 2 will be the main experimental foundation in forming the Fuzzy Universes of Discourses $\mathbf{X_i}$ and $\mathbf{Y}$, of regression vectors and the scaled duty cycle for each particular identification process subsequently explained. In Expression (2), the universes are formed from the excited DHA simulation model of a DC-DC boost converter to provide the necessary robustness, including the discontinuous conduction mode (DCM) and the continuous conduction mode (CCM) of a DC-DC boost converter:

$$\begin{aligned}
&\overline{v}_o = x_1 \in \mathbf{X}_1 = [0 \; V, \; 700 \; V] \\
&\overline{i}_L = x_2 \in \mathbf{X}_2 = [0 \; A, \; 1030 \; A] \\
&E = x_3 \in \mathbf{X}_3 = [10 \; V, \; 16 \; V] \\
&R = \frac{\overline{v}_o}{\overline{i}_R} = x_4 \in \mathbf{X}_4 = [10 \; \Omega, \; 32 \; \Omega] \\
&d_u = y \in \mathbf{Y} = [0.015 \cdot d, \; 0.985 \cdot d] = [0.65, \; 0.0.1].
\end{aligned} \tag{2}$$

2.1. Fuzzy Model Structure of the Two Degrees of Freedom Controller, the Prediction and Processing Minimization

Baždarić et al. in [3] demonstrated the FL identification powerful tool in reconstructing all of the system's possible steady states. It is done in the wide range of operating points that are defined by altering different process parameters in combinations and providing the expected real and extreme system conditions.

In the five-dimensional normed space (excluding the time) $(V^{(-1)}, \|\cdot\|)$, the modeling provides a fuzzy model, which is expressed by Equation (3):

$$\begin{aligned}
\boldsymbol{x}_{\boldsymbol{d_4}} &= [\overline{v}_o \; \overline{i}_L \; E \; R]^T \Leftrightarrow \boldsymbol{x} \\
f(\boldsymbol{x}|\boldsymbol{\theta}) &= \frac{\sum_{j=1}^{b} (a_{j,0} + a_{j,1}x_1 + \ldots + a_{j,4}x_4)\mu_{Hj}(\boldsymbol{x})}{\sum_{j=1}^{b} \mu_{Hj}(\boldsymbol{x})} \\
d_{FEM} &= \mathbf{F}(\boldsymbol{x}_{\boldsymbol{d_4}}) = f(\boldsymbol{x}|\boldsymbol{\theta})
\end{aligned} \tag{3}$$

that relates the system states and process parameters. In Equation (3), the $a_{j,0}$ is the member (real number) of the fuzzy model parameter matrix $\boldsymbol{\theta}$ in the j^{th} row and the first column, while the μ_{Hj} denotes specially j^{th} c-clustering defined membership function from the b number of clusters [3]. Four measured variables of the regression vector $\boldsymbol{x}$ will give information about the process parameters'

change. Instantly and from the previous offline identification process, the fuzzy model relates a linear contribution of inputs, as the T-S consequence functions (3), to the infinity horizon steady duty cycle d_{FEM}.

The model in Equation (3) is a basis for the predictive control of a DC-DC boost converter. As a derived model, Equation (3) is not a dynamic system model, it is used in [3] in the feed-forward line of the optimized PI controller. The resulting control law is

$$\begin{array}{c} d_u(t) = \frac{1}{T_a}\int d_{FEM}(kT_s)dt + d_{PI}(t) \quad T_a - \textit{current constraint based tuning parameter} \\ d_{FEM}(k) = \mathbf{F}(\boldsymbol{x_{d_4}}(k)) = \mathbf{F}(s(k), \mathrm{I}_L, E(k), \frac{\overline{v}_o(k)}{\overline{i}_R(k)}) \end{array} \tag{4}$$

where d_{PI} denotes the output from the PI controller. The control signal d_u is a scaled duty cycle $d(t)$ for the used PWM. The I_L in Equation (4) is the infinity horizon prediction of the steady-state inductor current $\bar{i}_L$, corresponding to the load current $\bar{i}_R$ and the model based reconstructed efficiency ratio.

The control law will guarantee as fast as possible response of a DC-DC boost converter in finding the steady state for a new possible operating point, mostly limited only by the maximum inductor current. As the new predicted steady state is just an approximation with the projected maximum process/model error, the optimized PI controller will be in function to compensate the steady state error. Here, the optimized PI controller's main function is to regulate the process operation near the operating point, where this type of linear controller was found to be the most effective. The posed control solution agrees with all the previously mentioned objectives and forms the Two Degrees of Freedom controller. Thus, the controller predicts the new steady duty cycle instantly and based on the measured process parameters. The fuzzy model $d_{FEM}(k) = \mathbf{F}(\boldsymbol{x_{d_4}}(k))$ is an explicit model as the solution of Equation (3) and does not need calculation of the inverse matrix to fulfill the controller's prediction. It is a Fuzzy Model-Based predictive control that can be compared with the MPC in a sense of infinity horizon prediction [3]. This feature drastically minimizes the controller's processing time.

2.2. Fuzzy Model Structure of the Fuzzy Model Predictive Control (FMPC) Controllers and their Processing Minimization

Furthermore, Baždarić et al. in [4] demonstrated the FL identification powerful tool in reconstructing the system's dynamic model. In the similarly developed normed space $(V, \|\cdot\|)$ as the one in [3], but now 6-dimensional, including the time, the FL identification and modeling will provide the alternative to the analytically derived model of a DC-DC converter. Slightly different than in Equations (2) and (3), the derived fuzzy model will be constructed from the aspects that $\overline{v}_o$ is the output and d_u is an input with the corresponding universes. Moved from the HS theory, but also from the traditional "averaged switched model", this fuzzy model renders all benefits of the alternative modeling as mentioned earlier.

As stated in [4], the fuzzy model $\boldsymbol{F}(\boldsymbol{\varphi}_k)$ is expressed by

$$\begin{array}{c} y_m(k+1) = \boldsymbol{F}(\boldsymbol{\varphi}_k) = \boldsymbol{\beta}(\boldsymbol{\varphi}_2(k))\boldsymbol{\theta}_1\boldsymbol{\varphi}_1(k)^T \\ \boldsymbol{\varphi}_1(k) = [\overline{v}_o(k) \quad \overline{v}_o(k-1) \quad \bar{i}_L(k) \quad d_u(k) \quad 1] \\ \boldsymbol{\varphi}_2(k) = [\overline{E}(k) \quad \overline{v}_o(k)/\bar{i}_R(k) \quad \bar{i}_L(k)]. \end{array} \tag{5}$$

In the Equations (5) the $\boldsymbol{\varphi}_1(k)$ denotes a first-grade and $\boldsymbol{\varphi}_2(k)$ a second-grade regression vector. Furthermore, $\boldsymbol{\theta}_1$ denotes the parameter matrix of the 1st-grade identification, and $\boldsymbol{\beta}(\boldsymbol{\varphi}_2(k)) \in \mathrm{R}^p$ (p-number of fuzzy rules) is the vector of normalized degrees of fulfillment [4]. The mentioned vector is the compact expression of the T-S Fuzzy System that consists of Gaussian membership function in the process of fuzzification, the product as the conjunction function in the premise and the center-average defuzzification. The new type of Fuzzy Model that is now expressing the DC-DC boost converter is a T-S fuzzy nonlinear interpolation of p-linear models identified in the first-grade of identification and further forming the T-S consequence functions. The novelty is that the linear models in the different operating points are not analytically driven, and those are devised by the Least-Squares

(LS) identification process in the wider neighborhood of the operating point. Furthermore, this type of approach minimizes the number of rules in the fuzzy rule base and additionally smoothes the nonlinear interpolation [4]. Equation (6) presents the final state space expression of the DC-DC boost converter, where the matrixes $\boldsymbol{A}_{m_i}$, $\boldsymbol{B}_{m_i}$, $\boldsymbol{R}_{m_i}$ are the LS identified matrixes in the neighborhood of the i-th operating point and $w(k)$ is the unit step function that is used to integrate the identification process error.

$$\begin{gathered} \boldsymbol{x_m}(k+1) = \sum_{i=1}^{p} [\boldsymbol{A}_{m_i}\boldsymbol{x}_m(k) + \boldsymbol{B}_{m_i}d_u(k) + \boldsymbol{R}_{m_i}w(k)]\beta_i(\boldsymbol{\varphi}_2(k)) \\ \beta_i(\boldsymbol{\varphi}_2(k) \in [0,1] \quad \sum_{i=1}^{p} \beta_i(\boldsymbol{\varphi}_2(k) = 1 \quad i = 1,\ldots,p \quad \boldsymbol{x_m} = [\overline{v}_o(k)\ \overline{v}_o(k-1)]^T \end{gathered} \tag{6}$$

As the typical and compared MPC controllers have the time variable inner models (kT_s), the state space form evolves in a more compact form, as provided in Model (7):

$$\begin{gathered} \boldsymbol{A}_{m_k} = \begin{bmatrix} a_{m1_k} & a_{m2_k} \\ 1 & 0 \end{bmatrix} \quad \boldsymbol{B}_{m_k} = \begin{bmatrix} a_{m4_k} \\ 0 \end{bmatrix} \\ \boldsymbol{R}_{m_k} = \begin{bmatrix} a_{m3_k} i_L(k) + a_{m5_k} \\ 0 \end{bmatrix} \\ \boldsymbol{C}_{m_k} = [1 \quad 0] \quad \boldsymbol{D}_{m_k} = 0 \\ \mathbf{x}_m(k+1) = \boldsymbol{A}_{m_k}\mathbf{x}_m(k) + \boldsymbol{B}_{m_k}d_u(k) + \boldsymbol{R}_{m_k}\boldsymbol{w}(k) \\ y_m(k) = \boldsymbol{C}_{m_k}\mathbf{x}_m(k) + \boldsymbol{D}_{m_k}y_m(k) = \boldsymbol{C}_{m_k}\mathbf{x}_m(k). \end{gathered} \tag{7}$$

Herein, $\boldsymbol{a}_m(k) = [a_{m1}(k)a_{m2}(k)a_{m3}(k)a_{m4}(k)a_{m5}(k)] = \boldsymbol{\beta}(\boldsymbol{\varphi}_2(k))\boldsymbol{\theta}_1$ denotes the compact vector of the fuzzy model coefficients at the time k. Those coefficients are profiling our novel FMPC algorithms in the controls of a DC-DC boost converter. As Section 3 compared FMPCs that, after the modeling part, are built typically (reference model, preceding horizon principle and filtering) [26,27], the control laws will be omitted. Here, we present the cost functions $J(k)$ and the suppression factor λ that have been used to form the compared MPC algorithms:

- Fuzzy Dynamic Matrix Control (FDMC)

$$J(k) = \sum_{j=1}^{N_u} q_j(y_m(k+j|k) - r(k+j|k))^2 + \sum_{j=0}^{N_u-1} \lambda_{j+1}(k)\Delta u(k+j|k)^2. \tag{8}$$

- Fuzzy Generalized Predictive Control (FGPC)

$$\begin{gathered} \boldsymbol{J}(k) = \sum_{j=1}^{N_u} \boldsymbol{x_J}^T(k+j|k)\boldsymbol{\Gamma}(j)\boldsymbol{x_J}(k+j|k) \\ \boldsymbol{x_J}(k) = \begin{bmatrix} \boldsymbol{x_{J1}}(k) \\ \boldsymbol{x_{J2}}(k) \end{bmatrix} = \begin{bmatrix} \boldsymbol{y}_p(k+1) - r(k+1) \\ \lambda\Delta u(k) \end{bmatrix} \end{gathered} \tag{9}$$

- Fuzzy Predictive Functional Control (FPFC)

$$J(\boldsymbol{u},k) = \sum_{j=1}^{n_H} (r(k+H_j|k) - y_m(k+H_j|k))^2 + \sum_{j=1}^{n_H} \lambda_j{}^2(k)\boldsymbol{u}(k+j-1|k)^T\boldsymbol{u}(k+j-1|k). \tag{10}$$

During the control horizon N_u, the FDMC cost function (8) minimizes the error between the model-based prediction y_m and first-order reference model r, which is additionally weighted by the state weighting factor q. The control signal u (8) is suppressed by the suppression factor λ. In Equation (9), we see the augmented model state vector $\boldsymbol{x}_J$ which contains the filtered output from

the second order filter $\boldsymbol{y}_p$ [22] and no state weighing factor. The FPFC cost function in Equation (10) is different and additionally minimizes the computation burden, as it calculates for n_H a number of coincidence points H during the control horizon and minimizes the vector of the control signals for those points $\boldsymbol{u}$ [4,21,22]. It is important to add that the suppression factor λ, when comparing FMPCs, is the inner model-based adaptive and time variable factor $\lambda(k) = a_{SUPP} \cdot y_m(k+1) \cdot u(k)^{-1}$, where a_{SUPP} denotes the tuning coefficient [4].

To demonstrate a minimization of the online processing done in [4] by the state space dimension reduction, the model state space matrixes that are presented in the MLD model in [28] are provided:

$$
\begin{gathered}
A = \begin{bmatrix} A_{d_3} & 0_{2x1} & 0_{2x2} \\ 0_{2x2} & 0_{2x1} & 0_{2x2} \\ 0_{1x2} & 1 & 0_{1x2} \end{bmatrix} \\
B_2 = \begin{bmatrix} 0_{2x1} & B_{d_2} - B_{d_3} & B_{d_1} - B_{d_3} & B_{d_4} - B_{d_3} \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \\
B_3 = \begin{bmatrix} I_{2x2} & I_{2x2} & I_{2x2} & 0_{2x1} \\ 0_{3x2} & 0_{3x2} & 0_{3x2} & 0_{3x1} \end{bmatrix} \quad B_1 = 0_{5x1} \\
C = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \end{bmatrix} \\
D_1 = 0 \quad D_2 = 0_{1x4} \quad D_3 = 0_{1x7} \\
x(k+1) = Ax(k) + B_1 u(k) + B_2 \delta(k) + B_3 z(k) \\
y(k) = Cx(k) + D_1 u(k) + D_2 \delta(k) + D_3 z(k) \\
E_2 \delta(k) + E_3 z(k) \leq E_1 u(k) + E_4 x(k) + E_5.
\end{gathered}
\tag{11}
$$

The state-space equations in Model (11) present the final solution in the MLD approach, which consists of the characteristic state space matrixes A, B, C, D, where the A, B are derived from the intermediate matrixes A_{d_i}, B_{d_i} as the result of discretization processes during the T_s time. Thus, in Model (11), the state vector $\boldsymbol{x}$ consists of the inductor current and output voltage, the input is provided by δ as the five-dimensional vector of logic variables, and $\boldsymbol{z}$ is the MLD seven-dimensional auxiliary variables' vector. The matrixes E_i form the set of selected inequalities as the subject to the optimization [28].

It is obvious that in the examples in which we use the Model Predictive Control (MPC), a dimension of the state space model matrixes (A in Model (11) and $\boldsymbol{A}_{m_k}$ in Model (7)) has the extreme impact on the online processing time. Thus, $\boldsymbol{A}_{m_k} \in R^{2x2}$ in comparison with the $A \in R^{5x5}$ simplifies the final model predictive state matrix. For the n horizon prediction, the model predictive state matrix is $A_{m_p} \in R^{n \cdot n_r \; x \; n_c}$, if the n_r and n_c are the number of rows and columns, respectively, of the original model state matrix.

3. Simulation Results of the Novel Control Methods and Their Comparison

Although in this study a Discrete Hybrid Automata (DHA) and the equivalent model of a DC-DC boost converter are considered to be the online processing time complex, it is a recommended basis for forming the simulation model of the MATLAB/SIMULINK platform [29]. For the novel control methods, it is a source in exploring the identification methodologies and later application to the physical processes. Thus, the developed methods will be simulated and applied to the DHA-developed simulation model. A minimum discretization or the sampling time in modeling the PWM, and switching events of the semiconductors, is set to 1 μs while a DC-DC boost converter model sampling time T_s is 333 μs. The simulation process was not done in real time; we left enough time to process the DHA simulation model itself together with the developed control algorithms. To provide a meaningful comparison, we use the test parameters or system events that are applied in [3]. The selection of the operating points and the process parameter change have to prove the

robustness of the control algorithms driven from the minimum borders of a DCM to the maximum borders of the CCM of a DC-DC boost converter. In this comparison, we will also present the MPC-developed methods that were not found to be sufficiently compact, and their processing time was short enough to be applied in the physical experiment of [4]. Subsequently, the Fuzzy Generalized Predictive Control (FGPC) algorithm, the Fuzzy Dynamic Matrix Control (FDMC), the Fuzzy Predictive Functional Control (FPFC), the optimized PI control, and finally the Two Degrees of Freedom (TDOF) control will be tested for the same combination of the system parameters' change, and their dynamics and steady states will be subsequently compared.

The simulation block diagrams of discussing control algorithms can be found in [3,4]. The FMPC methods are based on the same internal model (7) as described in Section 2.2 and [4]. Furthermore, a TDOF control methodology is described in Section 2.1 and [3], and an optimized PI controller as the reference to all of the comparisons is described in both articles. The latter control solution is intentionally chosen to simplify any of the following comparisons, as its construction is based purely on the standard toolbox of the used simulation platform [29] and optimized by the Integral of the Time Weighted Absolute Error (ITAE) criterion.

In Figure 3a, the response of the most favored predictive control solution FPFC is presented. It comes from the online processing time span and aggressiveness in the transition time. The online processing time is again proportionally related to the number of the prediction points, but in the nature of this MPC method, it is the reduction of coinciding points by the implementation of basis functions [26]. Furthermore, in the figure, there is the curve of the inductor current function that demonstrates a controller's controlled manner of the most critical constraint of the DC-DC boost converter. Separately from Figure 3a, Figure 3b presents the manipulated or controlling parameter that is a duty cycle of a DC-DC boost converter.

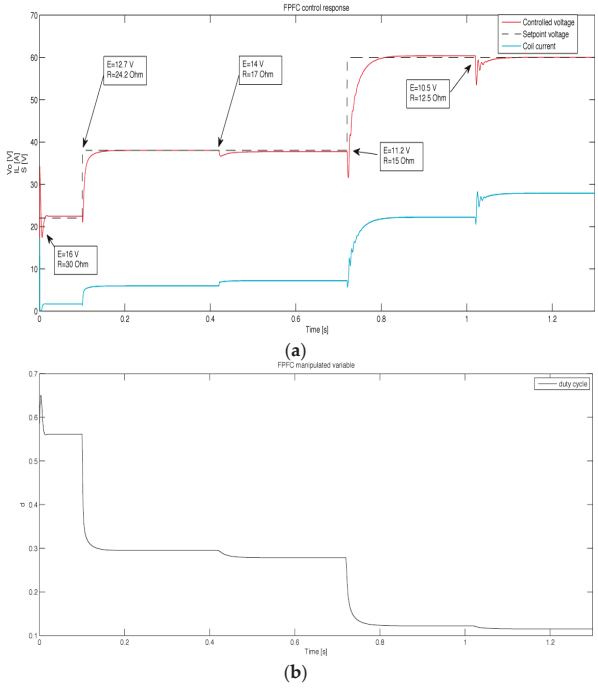


Figure 3. Simulation results: (**a**) Controlled variable by the Fuzzy Predictive Functional Control (FPFC) controller v_o ($MSRE = 0.0023$ for 129601 samples related to the reference) and coil current i_L; (**b**) Manipulated variable from the FPFC controller (duty cycle) $d_u = [0.01,\ 0.66]$ *range* $98.5 \div 1.5\%$.

In the sequel, the result of the simulation process for the FGPC, FDMC, the optimized PI, and the TDOF method is presented in Figures 4–7 respectively.

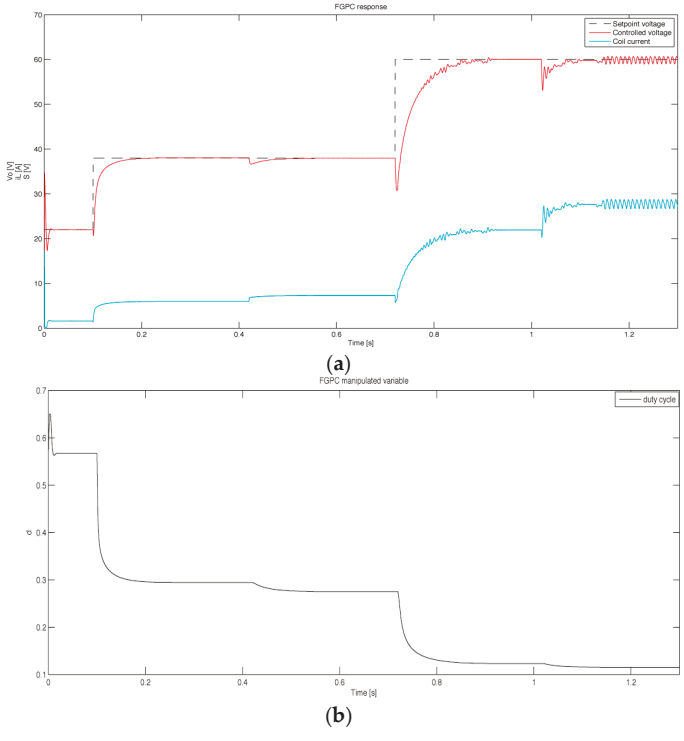


Figure 4. Simulation results: (**a**) Controlled variable by the Fuzzy Generalized Predictive Control (FGPC) controller v_o ($MSRE = 0.0044$ for 129601 samples related to the reference) and coil current i_L; (**b**) Manipulated variable from the FGPC controller (duty cycle) $d_u = [0.01,\ 0.66]$ $range$ $98.5 \div 1.5\%$.

In Figure 4, the FGPC responses are significantly slower and have a slightly worse mean square relative error (MSRE) in comparison with the FPFC. We see that even the second-order filter integrated into the prediction model and filtering the model output did not significantly improve the steady state stability, but it reduces the aggressiveness in the response. The small, steady-state chattering in the last two changes of system parameters assign the border of the controller's robustness. It is well-suppressed by the adaptive controller's control signal suppression factor. Similarly, the FDMC simulation in Figure 6 presents the slightly faster response in the transitions and a worse MSRE, but in Section 2, it is explained that it has less of a processing time burden due to the absence of the model output filter.

From the results, the similarities related to the aggressiveness in the transitions and the accuracy in the steady-state of the applied FMPC methods are noticeable. The best performance is experienced with the FPFC in Figure 3, and other methods can be compared to that reference. Closer to the performance of the FPFC is the FDMC. The FGPC has been found to be a bit coarser in the steady state, but on some occasions, such as a system start, it is faster in the response. As expected, the optimized PI controller in Figure 6 is slower in transitions, especially for the operating points far from the center of the performed optimization for the time periods in which the lower system gains have been experienced.

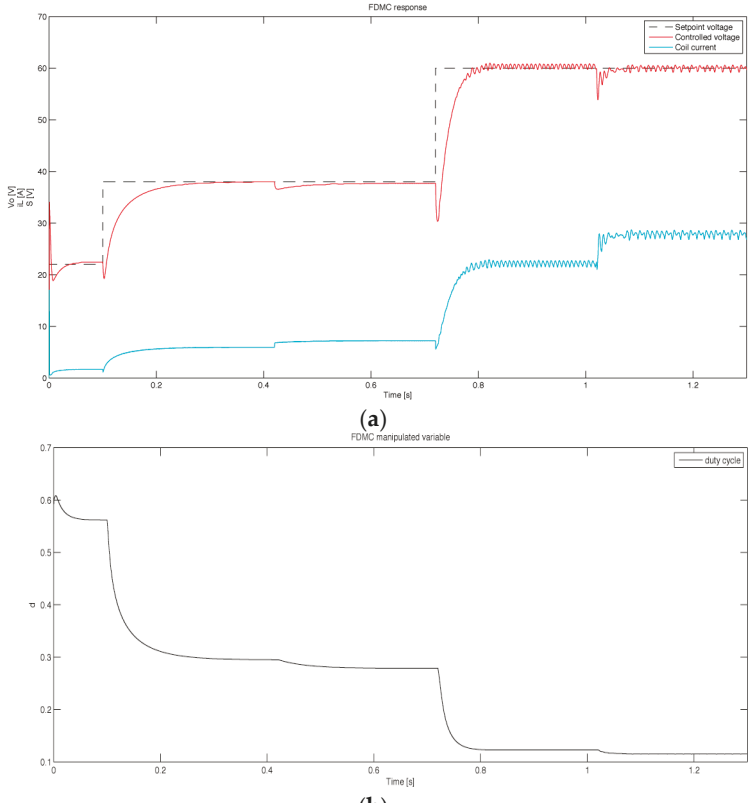


Figure 5. Simulation results: (**a**) Controlled variable by the Fuzzy Dynamic Matrix Control (FDMC) controller v_o ($MSRE = 0.0062$ for 129601 samples related to the reference) and coil current i_L; (**b**) Manipulated variable from the FDMC controller (duty cycle) $d_u = [0.01,\ 0.66]$ $range$ $98.5 \div 1.5\%$.

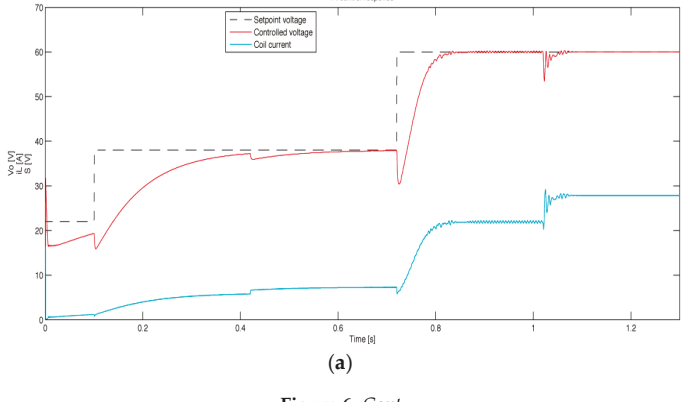
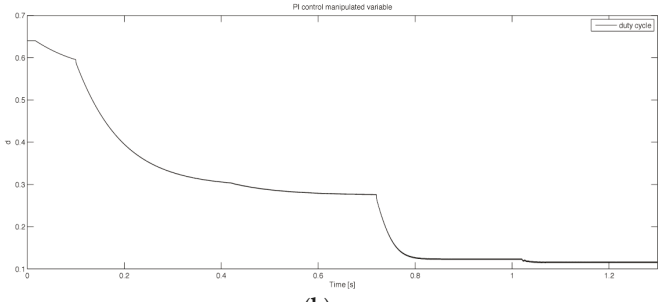
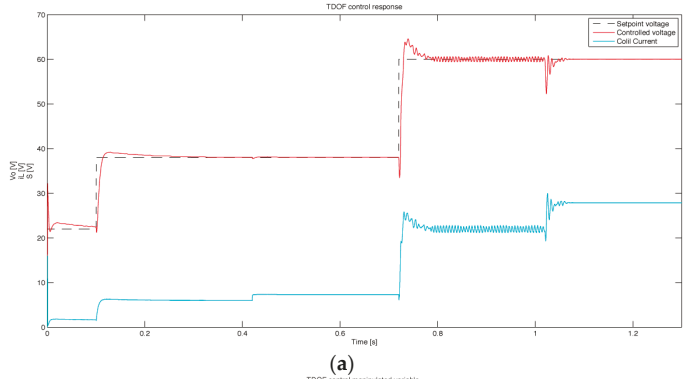


Figure 6. *Cont.*

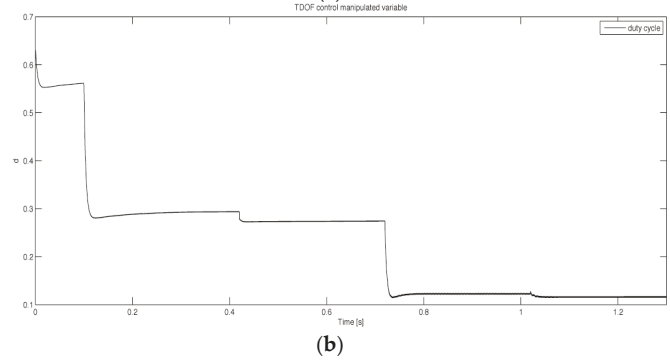


(**b**)

Figure 6. Simulation results: (**a**) Controlled variable by the Optimized PI controller v_o ($MSRE = 0.0220$ for 129601 samples related to the reference) and coil current i_L; (**b**) Manipulated variable from the optimized PI controller (duty cycle) $d_u = [0.01,\ 0.66]$ *range* 98.5 ÷ 1.5%.



(**a**)



(**b**)

Figure 7. Simulation results: (**a**) Controlled variable by the Two Degrees of Freedom (TDOF) controller v_o ($MSRE = 0.0015$ for 129601 samples related to the reference) and coil current i_L; (**b**) Manipulated variable from the TDOF controller (duty cycle) $d_u = [0.01,\ 0.66]$ *range* 98.5 ÷ 1.5%.

Different from the aforementioned, the TDOF methodology that is presented in Figure 7 performs as the fastest in transitions, but during that particular time, the control algorithm cannot attenuate the gradient of change, and on some occasions, it violates the reference point. This scenario is initiated by the error of the identified steady state, which is filtered out by the receding horizon strategy in other FMPCs. In contrast, the TDOF algorithm will certainly demand significantly less processor time of execution. From that point of view, the optimized PI controller will use the shortest time of execution,

but it is not the robust solution, and in some occasions, it cannot reach the reference value before another is selected (see Figure 6).

Figure 8 presents all methods together and additionally simplifies the comparison.

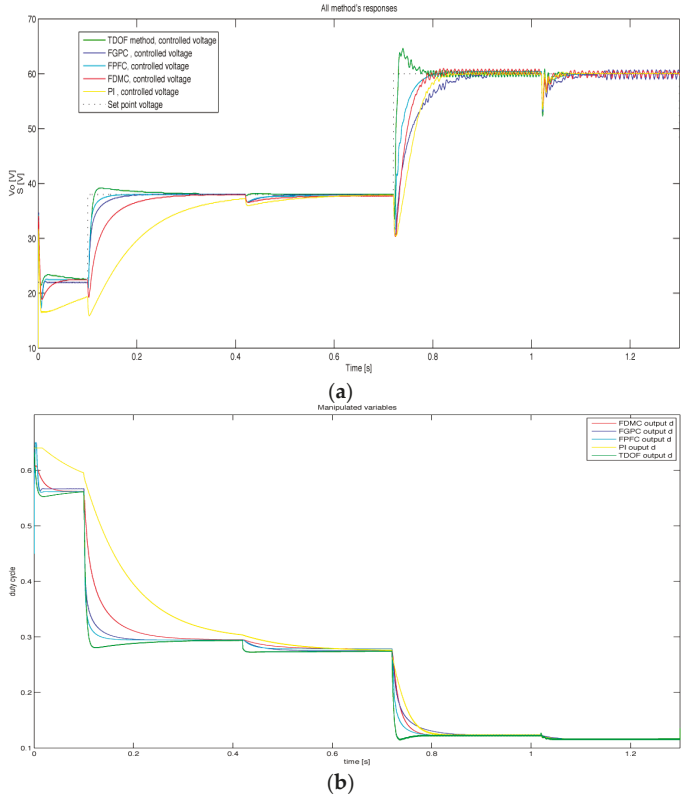


Figure 8. Simulation results: (**a**) Controlled variable v_o compared for all methods; (**b**) Manipulated variable d_u compared for all methods.

The overall comparison is quantified by the time of response and the MSRE that can be seen in Table 1.

Table 1. Comparison of the performances for the applied controllers based on 129601 samples of simulation for the 1.3 s of the simulation duration.

Controller	MSRE	$_{r}t_a$ [s] [1]	t_{st} [s] [2]
FPFC	0.0023	0.0038	0.0110
TDOF	0.0015	0.0099	0.0728
FDMC	0.0062	0.0207	0.0256
FGPC	0.0044	0.0331	0.0103
Opt_PI	0.0220	0.0429 [3]	NA [4]

[1] $_{r}t_a$ is an averaged response time while the controller reaches 0.03 of the relative error to the reference, excluding the start time; [2] t_{st} is the controllers' start time; [3] the time valid only for two comparable responses, [4] NA- non-applicable.

The above successful results led to the selection of the FPFC method as the most favored and comprehensive solution to be applied in the experimental test of the real DC-DC boost converter. Table 2 presents the controller's scores related to the assigned objectives in Section 1.

Table 2. The table of achieved objectives stated in Section 1.

Controller	PCR	SR	OPT	S	NFM	A
FPFC	Y	Y	SO	ES	Y	A
TDOF	Y	Y	ITAEO	ES	Y	A
FDMC	Y	M	SO	ES	Y	M
FGPC	Y	M	SO	ES	Y	M
Opt_PI	N	NA	ITAEO	ES	N	A

Y-yes, N-no, NA-non-applicable, M-moderate, SO-suboptimal, ITAEO-ITAE criterion optimality, ES-experimental stability, A-applicable.

Referring [4], our experimental results prove the assigned objectives mentioned in the Introduction and in Section 2 for the FPFC as the controller with the highest score.

4. Conclusions

The primary objective of this article was the new control methodology in the direction of implementing the most recently developed strategies for systems that are physically small, but complex in their behavior. That task required the fundamental decomposition of the problem and the learning of the most basic system's behavior. Differently from here, most of the known methods performed on this particular problem employ the analytical methodology in forming the model-based solution [5]. In this study, the model is identified with fuzzy logic. Additionally to widely known objectives, the developed modeling allows the forming of control solutions that conciliate the method's complexity with applicability to the physical processes.

The novel controllers presented are developed with the intention of reducing the online processing complexity. This intention guides the development of two different control methodologies. Both of the control methodologies utilize model-based predictive control. In the case of TDOF control, the problem was decomposed in a way to compensate for the main drawback of the numerically optimized linear controller, which is recognized for its robustness for a wider range of the process parameters' change.

The transition period in TDOF methodology is fast, but it sometimes overshoots the reference point, depending on the positivity of the system/model error at that operating point. To synthesize the solution that is considered to be a dynamic model-based prediction, and to rectify the overshoots, a fuzzy model-based MPC solution is derived. In this study, it is shown that for the reasonable longer processing time, the FMPC successfully follows the aggressiveness of the TDOF controller and the contemporary reference model. Furthermore, the modern predictive control methodology here presented has suboptimal control over the complete transition period and the smooth, steady state of the system. Therefore, in general, the presented FMPCs provide the MPC methodologies that apply to the fast response systems.

Further research will go in the direction of implementing these methodologies into the more complex SAS, as well as continuing to implement the qualitative mathematical theory in designing and exploring the new control methodologies.

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Analysis and Control of Electrolytic Capacitor-Less LED Driver Based on Harmonic Injection Technique

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Abstract: AC-DC LED drivers may have a lifespan shorter than the lifespan of LED chips if electrolytic capacitors are used in their construction. Using film capacitors solves this problem but, as their capacitance is considerably lower, the low-frequency ripple will increase. Solving this problem by limiting the output ripple to safe values is possible by distorting the input current using harmonic injection technique, as long as these harmonics still complies with Power Factor Regulations (Energy Star). This harmonic injection alleviates the requirements imposed to the output capacitor in order to limit the low-frequency ripple in the output. This idea is based on the fact that LEDs can be driven by pulsating current with a limited Peak-To-Average Ratio (PTAR) without affecting their performance. By considering the accurate model of LEDs, instead of the typical equivalent resistance, this paper presents an improved and more reliable calculation of the intended harmonic injection. Wherein, its orders and values can be determined for each input/output voltage to obtain the specified PTAR and Power Factor (PF). Also, this harmonic injection can be simply implemented using a single feedback loop, its control circuit has features of wide bandwidth, simple, single-loop and lower cost. A 21W AC-DC buck converter is built to validate the proposed circuit and the derived mathematical model and it complies with IEC61000 3-2 class D standard.

Keywords: pulsating output current; light emitting diode (LED); peak to average ratio (PTAR); power factor correction; harmonic injection; modelling; feedback loop control

1. Introduction

LED technology has several merits over conventional lamps such as: high-efficiency, very long lifespan (approximately 100,000 h [1]), lower power consumption, low maintenance cost and instantaneous switch-on [2,3]. Besides, the LEDs are environmentally friendly. Regarding their efficiency, CREE claimed to be the first company to break the 300 lumens per watt barriers (still being the highest level achieved) [4]. Moreover, lighting consumes 20% of the electrical energy in the industrial countries pushing forward the replacement of conventional lighting with LED lighting.

The critical part that defines the LED lamp lifespan is the driver. One-stage AC-DC LED drivers normally use a bulky electrolytic capacitor to balance power between the pulsating input and the constant output, minimizing the double line frequency current ripple [5]. This capacitor limits the lifespan of the LED lamp to its own lifespan, typically between 1000 and 10,000 h, considerably lower than the lifespan of LEDs [6]. In addition, the lifespan of the E-Caps follows the 10-degree-law that states that it decreases by a factor of 2 for each +10 °C temperature increase. Even assuming

this, operation at 85 °C only pushes its lifespan to 20,000 h. Consequently, eliminating the E-Cap is mandatory and many research efforts have been made in this direction.

Wound and soft winding film capacitors can be used instead of E-Caps due to their long lifespan [7]. However, their energy density is low and that increases the output voltage and the output current ripple of the LED driver. This causes a depraved effect on the LED chip. The light perceived by humans' eyes is proportional to its average value because the light ripple is filtered as long as its frequency is higher than a few hundreds of hertz. Nonetheless, increasing LED peak current (as a consequence of the ripple) results in a change in the chromaticity coordinates, color correlated temperature (CCT), color rendering index (CRI), flux and efficacy degradation, so LED light is perceived as bluish-white [8,9].

Several studies proposed different topologies and control circuits to enable using low-density capacitors with limited LED peak current under a defined ratio called PTAR. The most effective way is harmonic injection technique. The idea is to inject predefined harmonics into the input current to limit the PTAR of the output LED current while observing PF regulations. Figure 1a–c shows different harmonics combinations for the LED current [10,11] with the result of a lower PTAR if those harmonics are wisely selected. First, Figure 1a shows the double line frequency output current in dashed line and the third harmonic order in dashed-dot line. The combination result is shown as a solid line and, as can be seen, its PTAR is lower than in the case of the first harmonic. Second, Figure 1b shows the double line frequency output current combined with the fifth harmonics. In this case, the resulting PTAR is higher than in the case of the first harmonic alone. Finally, Figure 1c shows the double line frequency output current combined with the third harmonics and the fifth harmonics. In this case, the PTAR is the lowest of the three cases. As more harmonic orders are injected, the combination has lower PTAR. However, it is very important to define the amplitudes that lead to the lowest PTAR while keeping the input PF within the regulation limits.

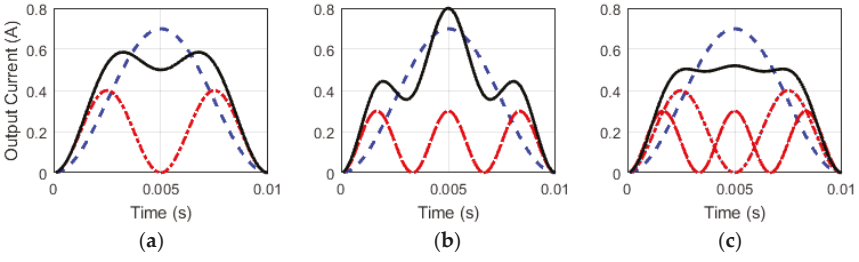


Figure 1. Different cases of the output current waveforms and its circuit diagram under harmonic injection [10,11]. (**a**) Combination of double and third line harmonics orders; (**b**) Combination of double and fifth line harmonics orders; (**c**) Combination of double, third and fifth line harmonics orders.

In [12], a two-stage LED driver is introduced. The first stage is a high frequency boost converter that operates at discontinuous conduction mode (DCM) as a pre-regulator PF correction (PFC) and injecting the 3rd harmonics into the input current. The second stage is a Flyback converter for regulating the LEDs current. The design replaced the storage E-Cap with film one; however, three 47-μF capacitors connected in parallel are still needed.

More harmonics are injected in the input current in [10,11]. The developed circuit is a single stage AC-DC Flyback converter. It has only a 0.47-μF film capacitor in its output. However, the model analysis introduced in [10] was based only on a resistive load model without considering the accurate LED chip model. As a consequence, the theoretical analysis and the experimental results were not well matched. Practical results show a PTAR of 1.43 for the output LED current instead of the designed one of only 1.34. Also, the presented controller included a feedforward loop with a multiplier and a divider that increase the complexity and the cost. In [13], limiting the PTAR of the LED current is achieved by using two loops, feedback and feedforward. Results recorded a PTAR of less than 1.34 by injecting more

harmonics orders. Again, the LED model consists of the equivalent resistor, which results in inaccuracy. In [14,15] a feedforward circuit was proposed to generate a distorted sinusoidal reference signal that contains the required injected harmonics to limit the PTAR. The implemented circuit included one microcontroller in the current loop with two voltage sensors and one current sensor in addition to the multiplier circuit. It uses a look-up table with a normalized value to generate the reference signal for the duty cycle. Moreover, injecting only the third harmonic resulted in a higher PTAR compared to the previous approaches. Similar results can be found in [16], wherein a feedforward loop for harmonic injection in addition to PLL, multiplier and divider circuits are used. A similar strategy was proposed in [17], which reduces the electrolytic output capacitor to almost 24.2% by using an Active Ripple Compensation (ARC). In [18] the same methodology was used to reduce the electrolytic capacitance by 46.3% by using a different ARC technique.

Harmonics injection is not only method to eliminate the E-cap. Ripple cancelation method can be also used to maintain the same purpose. This technique is based on adding a bidirectional converter connected in parallel or series to the output capacitor in order to cancel the double line frequency of the current ripple produced from decreasing the output capacitance as shown in Figure 2 [19]. By controlling the bidirectional converter to absorb the double line harmonics, the output inductor L_o and output capacitor C_o are used only to filter the high frequency harmonics in the output current [20,21]. Consequently, E-cap is eliminated and can be replaced with small capacitance.

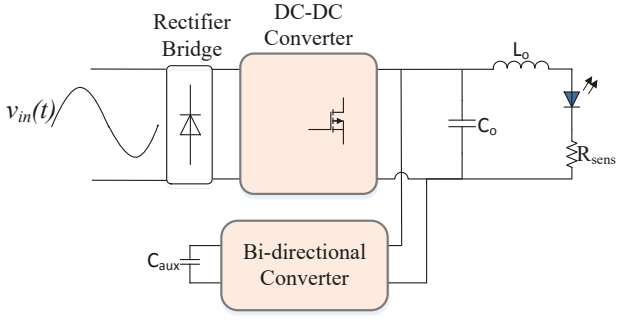


Figure 2. Parallel type of ripple cancellation circuit diagram [19].

Thus, many of these methods are using double stage with more than two semiconductors switches. Cost-wise is still not considered in this technique by using many components counts and using complex control circuits as well.

In [22], a boost converter was used as a pre-regulator to act as a PFC and it was cascaded with LLC resonant converter. Wherein, the frequency modulation technique is used in the control circuit. The behavior of the control circuit acts to vary the frequency when the line voltage changes. It generates the highest frequency at the peak of the line voltage. Therefore, the output current peak is expected to decrease. This kind of technique is suffering from many components counts in power stage and the implementation of the complex controller circuit.

Ripple cancellation technique can maintain the lowest LED current peak. However, the main disadvantage is using an extra converter to absorb the low frequency ripple current and using extra capacitor as shown in Figure 2. Therefore, it increases the component counts and circuit complexity.

Passive LED driver is considered one of the E-cap less topologies. In [23,24], four different passive LED driver topologies were proposed. The first type used valley-fill circuit to keep a high PF. It used a high inductance value of 1.47 H at the input, another bulky inductor value of 1.9 H at the output stage and two output capacitors in the valley fill circuit with a value of 20 µF polypropylene capacitors. The second type was done by making a modification in the valley-fill circuit. It has the same structure of the first type, in addition to the two output polypropylene capacitors in the valley-fill circuit with

a value of 20 µF. The third type was proposed without using the valley-fill circuit. This circuit was considered the most cost-effective one among all passive LED driver types as it used less component counts than the previous two types. The fourth type used a bulky inductor for the input stage with the same value of the first type. Also, it used a coupled inductor and one capacitor to filter the output current ripples.

Passive LED drive is only considered a cost-effective solution in a high-power application where size and cost of this passive elements are not considerable. Wherein, the usage of the bulky inductor instead of the bulky electrolytic capacitor increases the LED driver footprint.

In conclusion, prior researches have the following limitations:

- Using additional control loop circuit to inject harmonics increases the component count. Consequently, the LED lamp cost will increase, limiting its penetration to the market, especially in the case of single-stage solution.
- The best practical result is a PTAR of 1.43 in nominal conditions which is still a high value.
- Using an inaccurate model of the LED chip (i.e., replacing it by a simple resistor), leads to a deviation between the practical results and mathematical ones.

This paper introduces a step forward to modify the harmonic injection techniques to be simpler and more economic through using just one feedback loop, that can achieve the target PTAR and PF by means of using an accurate model for LED chip.

2. Modelling of E-Cap-Less Converter for LED Applications

AC-DC buck converter operating in DCM without electrolytic capacitor is the simplest topology for implementing an AC-DC LED driver because high PF can be achieved with the converter operating as a resistor emulator. Figure 3 shows the LED driver circuit of the converter under study. The LED is modeled as a series branch of three components: a small dynamic resistor r_e, a DC source representing the knee voltage V_{knee} and an ideal diode. Although this is the standard model of a diode, it has not been normally used in AC-DC LED driver design in favor of just the typical and simple equivalent resistance. As will be shown, more accurate results will be obtained in the implementation of the harmonic injection technique for reducing the PTAR if the complex model is considered.

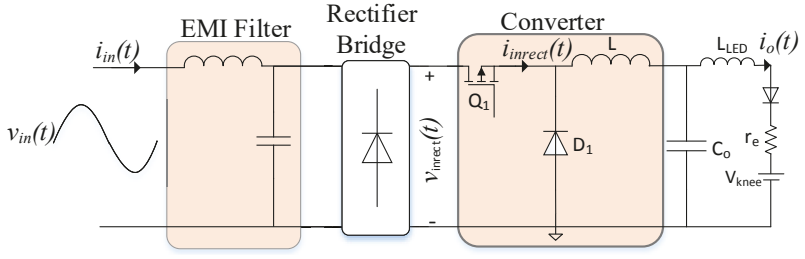


Figure 3. AC-DC E-Cap-less buck converter.

To simplify the analysis of the converter operation, elements such as diode D_1, MOSFET (switch Q_1), capacitor C_o, and inductor L are considered ideal. The buck converter operates with an input voltage equal to a rectified line voltage (whose pulsation is $2\omega_L$). The input current follows the input voltage as long as the input voltage is higher than the output one, defined by the required LED forward voltage (V_f). Figure 4a shows the rectified input voltage, inductor current and output current which starts increasing at T_c and reaches zero again at T_e. Their values can be expressed as follows:

$$T_c = \frac{\left|\sin^{-1}\left(\frac{V_o}{V_{inp}}\right)\right|}{\omega_L} = \frac{\left|\sin^{-1}(M)\right|}{\omega_L}, \quad (1)$$

$$T_e = \frac{T_L}{2} - T_c. \tag{2}$$

where V_{inp} is the peak value of the input voltage, V_o is the output voltage (LED voltage), M is the conversion ratio of the converter and T_L is the period of the input voltage. It should be mentioned that the output voltage is assumed to be constant to simplify the calculation.

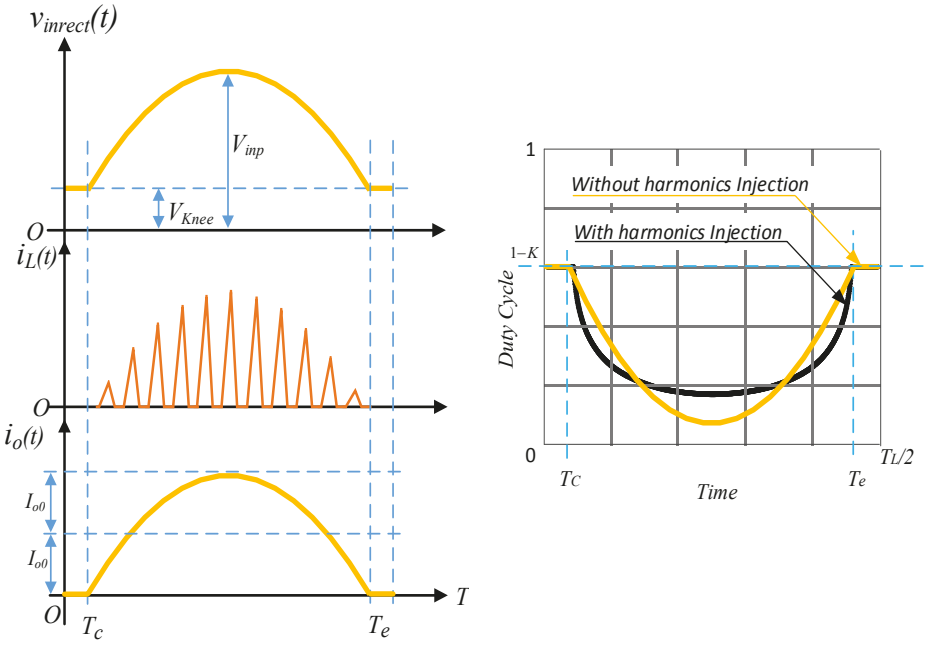


Figure 4. LED driver based buck converter for E-Cap less waveforms with and without harmonics injections. (**a**) Sketch for the rectified input voltage ($v_{inrect}(t)$) and inductor current (i_L) without harmonics injection. (**b**) The Duty cycle shape with and without harmonics injection.

2.1. Period 1: ($T_c \leq t \leq T_e$)

For period 1, the rectified voltage can be expressed as:

$$v_{inrect}(t) = V_{inp}|\sin(\omega_L t)|. \tag{3}$$

By referring to Figure 3, the inductor voltage during the on state of Q_1 can be expressed as:

$$v_L = L\frac{di_L}{dt} = v_{inrect}(t) - V_o. \tag{4}$$

The instantaneous peak inductor current, as shown in Figure 4a, is equal to Δi_L as the converter operates at DCM, and can be expressed as:

$$i_{PK}(t) = \frac{v_{inrect}(t) - V_o}{LF_s}d(t). \tag{5}$$

where $d(t)$ is constant in each switching period, and F_s is the switching frequency.

Also, the maximum peak inductor current over the line cycle can be calculated at the peak line input voltage V_{inp} as:

$$I_{PK} = \frac{V_{inp} - V_o}{LF_s} D_m. \tag{6}$$

where D_m is the maximum duty cycle.

The instantaneous input current, averaged over each switching period, can be expressed as:

$$i_{inrect}(t) = \frac{1}{2} i_{PK}(t) d(t) = \frac{v_{inrect}(t) - V_o}{2LF_s} d(t)^2. \tag{7}$$

where $i_{inrect}(t)$ is the instantaneous rectified current averaged over the switching period.

By ignoring the converter losses, the instantaneous input and output power are equal (over a switching period):

$$p_o(t) = p_{in}(t), \tag{8}$$

$$V_o i_o(t) = v_{inrect}(t) i_{inrect}(t). \tag{9}$$

where $p_o(t)$ is the output power and $p_{in}(t)$ is the input power. By referring to (7) and substituting it into (9) the expression for the output current can be expressed as:

$$i_o\ (t) = \frac{v_{inrect}(t) - V_o}{\frac{2LF_s V_o}{d^2}} v_{inrect}(t). \tag{10}$$

From (10), the instantaneous duty can be expressed as:

$$d(t) = \sqrt{\frac{2LF_s V_o i_o(t)}{v_{inrect}(t)(v_{inrect}(t) - V_o)}}. \tag{11}$$

Referring to (11), the duty cycle in DCM depends on the power stage inductance L, switching frequency F_s, output current $i_o(t)$, the input voltage $v_{inrect}(t)$ and the output voltage V_o.

2.2. Period 2: ($0 \leq t < T_c$ and $T_e < t \leq T_L/2$)

As explained in the section above, Equation (11) represents the derived control duty cycle for the system under study during the main conduction period ($T_c \leq t \leq T_e$). Here the duty cycle equation for the remaining part of the period will be derived.

The converter operates in DCM, where the conversion ratio M can be given as:

$$Conversion\ ratio\ (M) = \frac{2}{1 + \sqrt{1 + \frac{4k}{d^2}}}. \tag{12}$$

where $k = \frac{2L}{RT_s}$ and R is the equivalent load seen by the converter.

By replacing M by d in (12) to obtain the boundary between the DCM and CCM, so the duty cycle equals $1 - K$.

Combing period 1 and 2, using (11) and (12), the duty cycle is derived over the full range as:

$$d(t) = \begin{cases} 1 - K & 0 \leq t < T_c \\ \sqrt{\frac{2LF_S V_o i_o(t)}{v_{inrect}(t)(v_{inrect}(t) - V_o)}} & T_c \leq t \leq T_e \\ 1 - K & T_e < t \leq \frac{T_L}{2} \end{cases} \tag{13}$$

3. Modeling of Proposed E-Cap Less Converter under Harmonic Injection

Harmonic injection will be used to limit the PTAR of the output current. Equation (13) gives the duty cycle of the LED system under study. It is clear that the duty cycle is a function of the instantaneous output LED current and the input rectified voltage. If the output LED current is considered a dc value, the duty cycle shape will be as sketched in Figure 4b with orange line. This results in a PTAR of 2 for pure restive loads and even higher for real LEDs. Injecting harmonics into the current will imply modifying the duty cycle shape as shechted in Figure 4b with black line. In this section, a detailed study for the required harmonic injection components to limit the PTAR while keeping the target PF will be presented.

3.1. LED Output/Input Currents' Harmonics Relations

Figure 4a shows that the LED current during the positive half-line cycle can be expressed as:

$$i_o(t) = \begin{cases} 0 & 0 \le t < T_c \\ I_{o0} - \sum\limits_{n=1}^{\infty} I_{o(2n)} \cos 2n\omega_L t & T_c \le t \le T_e \\ 0 & T_e < t \le T_L/2 \end{cases} \tag{14}$$

where I_{o0} is the DC component, $I_{o(2n)}$ is the peak value of the harmonic component with order n. It is worth to note that if $n = 1$, this refers to conventional system without harmonic injection.

$I_{o(2n)}$ is a function of the conversion ratio M, resulting from the integration over the period $T_c \le t \le T_e$, where T_c is a function of M as derived in (1). Therefore, from (3), (7), (9) and (14) the input current can be derived as:

$$i_{in}(t) = \frac{V_o}{V_{inp}\sin(\omega_L t)} \left(I_{o0} - \sum_{n=1}^{\infty} I_{o(2n)} \cos 2n\omega_L t \right). \tag{15}$$

Using a trigonometric expansion and Chebyshev polynomials to simplify the input current equation [25]:

$$i_{in}(t) = \frac{2\,V_o}{V_{inp}} \left\{ I_{o0}\sin\omega_L t + \sum_{n=1}^{\infty} \left(\left((I_{o0} - \sum_{x=1}^{n} I_{o(2x)} \right) \sin(2n+1)\omega_L t \right) \right\} \tag{16}$$

The Fourier series expansion of the input current is a sum of sinusoidal waveforms with different amplitudes and different frequencies:

$$i_{in}(t) = \sum_{n=1}^{\infty} I_{i(2n-1)} \sin(2n-1)\omega_L t. \tag{17}$$

where $I_{i(2n-1)}$ is the peak value for the nth order harmonic component. By comparing (16) and (17), the relation between the input and output currents harmonics can be obtained:

$$I_{i(2n-1)} = 2\frac{V_o}{V_{inp}} \left(I_{o0} - \sum_{x=2}^{n} I_{o(2(n-1))} \right). \tag{18}$$

3.2. Designed Operating Regions under Target PF and PTAR

From (14), there are multiple combinations of harmonics that can be injected to limit the PTAR while keeping the same PF and the same LED average current (I_{o0}). Therefore, a MATLAB script to sweep all possible combinations for the output current harmonics can be used. The target are those harmonic combinations that lead to minimum PTAR while keeping a PF greater than 0.9.

PF consists of two factors, distortion and displacement. In this case, the displacement factor is considered unity due to the converter operation in DCM. The distortion factor is then the significant one [26]:

$$PF = \frac{I_1}{\sqrt{{I_1}^2 + {I_3}^2 + {I_5}^2 + \ldots}}. \tag{19}$$

Substituting (18) into (19) to determine PF expression as a function of the LED current harmonics:

$$PF = \frac{I_{o0}}{\sqrt{I_{o0}^2 + \sum_{n=1}^{\infty}\left(I_{o0} - \sum_{x=1}^{n} I_{o(2x)}\right)^2}}. \tag{20}$$

The PTAR can be derived from (14) by normalizing the LED current with the DC component. Therefore, the PTAR value will be the peak value of the periodic signal, which can be expressed as:

$$PTAR = Max\left(1 - \sum_{n=1}^{\infty} \mathrm{I}^*_{o(2n)} \cos 2n\omega_L t\right). \tag{21}$$

Regarding the MATLAB script, there are a many harmonics values which can be combined to implement the LED current considering the boundaries given in Equations (20) and (21), which determine the relation between the PTAR, the PF and the conversion ratio M. Therefore, the MATLAB script increases the amplitude of each harmonic component (I_2, I_4, I_6, etc.) and calculates the PTAR and the PF in each case. Valid combinations are those that satisfy the constraint of 0.9 as minimum PF value. Among them, the optimum one will be that with the lowest value of PTAR. Five cases are presented here. Case I is a double the frequency ($2\omega_L$). Case II is a combination of harmonics from the second ($2\omega_L$) to the fourth order ($4\omega_L$). Case III is a combination of harmonics from the second ($2\omega_L$) to the sixth order ($6\omega_L$). Case IV is a combination of harmonics from the second ($2\omega_L$) to the eighth order ($8\omega_L$). Finally, Case V is a combination from the second ($2\omega_L$) to the tenth order ($10\omega_L$).

The proposed analysis follows the flow chart presented in Figure 5. Adding more harmonics decreases the PTAR but also the PF. It is worth mentioning that the cases with higher harmonic orders (above tenth order) have been tested, but they are not considered here as they have a significant impact on PTAR but have a low PF (lower than 0.9) for any harmonic combination.

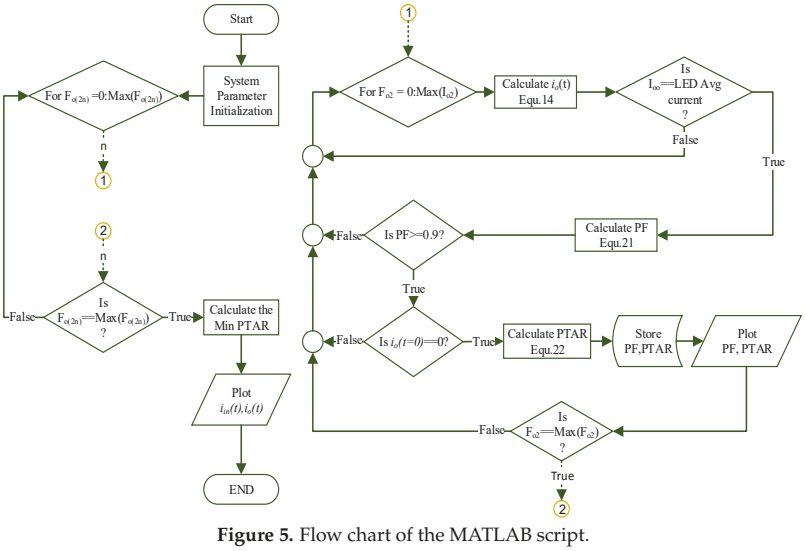


Figure 5. Flow chart of the MATLAB script.

It is in this script where using the real model of the LED rather than the typical equivalent resistance makes the conversion ratio to have a significant impact on PTAR and PF. Figure 6 shows the PTAR under Case V as a function of M while keeping the PF equals to 0.9. It should be mentioned that each point of the graph is obtained by the MATLAB script, which means that the minimum PTAR is shown. As illustrated in this graph, for a PTAR of less than 1.43, the accepted conversion ratio is limited to 0.2. This explain the mismatch in the results obtained by [10,11], where 1.43 was obtained experimentally, while 1.34 was targeted in the theoretical model. Also, this result clarifies the limitation of the conversion ratio in harmonic injection techniques. Using curve fitting, a relation between the PTAR and the conversion ratio M is found:

$$PTAR = -373.3M^4 + 265.3\ M^3 - 59.47\ M^2 + 5.677\ M + 1.142. \tag{22}$$

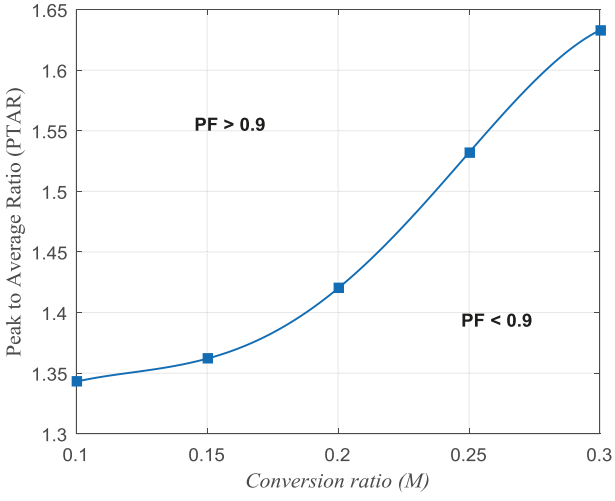


Figure 6. Curve fitted for different values for conversion ratio (M) and Peak to Average Ratio (PTAR).

4. Proposed Control Circuit and Simple Implementation

Taking the benefits described in the previous section, the control loop that reshapes the required LED current will be derived in this section using a straightforward control block. The harmonic combinations obtained from the MATLAB script for the output LED current. The duty cycle can be expressed as a Fourier series expansion using the curve fitting as:

$$d(t) = D_0 - \sum_{n=1}^{\infty} D_{(2n)} \cos 2n\omega_L t. \tag{23}$$

The duty cycle defined in (23) can be obtained by means of the proposed feedforward loop, which allows the chosen harmonic components to pass through. This reshapes the input and output currents as desired. Figure 7 shows the proposed closed-loop control for the LED driver. As can be seen, only a single feedback loop is implemented. The loop compensator, taking advantage of the previously explained harmonic injections optimization, should adjust the duty cycle according to the harmonics obtained from the MATLAB script.

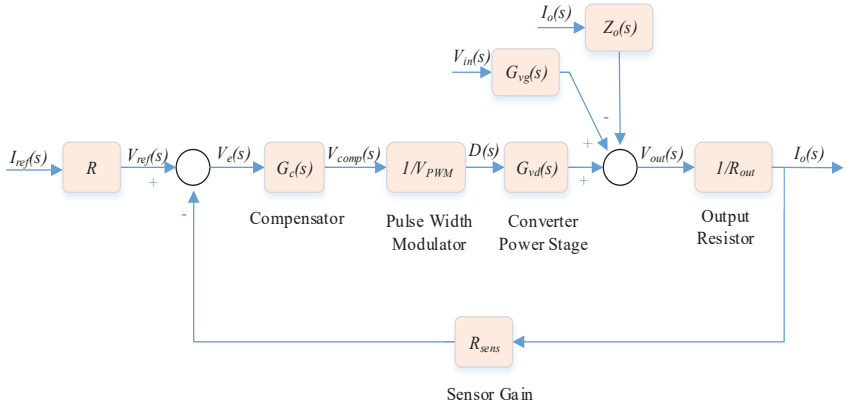


Figure 7. Closed system block configuration of DCM converter.

The loop compensator gain can be computed by dividing each order value of duty cycle harmonics, (24) by the output LED current harmonics, (14). The gain plot of the compensator output can be expressed in logarithmic scale as:

$$G_c = \frac{V_{comp}}{V_e} = \frac{V_{comp}}{V_{ref} - \mathrm{R_{sens}} i_o} = \frac{V_{PWM} D(s)}{V_{ref} - \mathrm{R_{sens}} I_o(s)}. \quad (24)$$

The results obtained with (25) states that this proposed reshaping block (compensation) is based on the division of the duty cycle by the output LED current harmonics.

5. Case Study

To validate the derived mathematical model and the proposed control, a case study will be analyzed in this section. The system parameters will be as follows:

- Nominal input voltage $V_{in} = 220$ VAC $\pm 10\%$.
- Line frequency $f_L = 50$ Hz.
- Output voltage $V_o = 60$ V.
- Average output power $p_o = 21$ W.
- Output current $I_O = 350$ mA.
- Switching frequency $f_s = 100$ kHz.
- Input filter capacitor $C_{in} = 47$ nF.
- Input filter inductor $L_{in} = 560$ µH.
- Output filter capacitor $C_{out} = 0.47$ µF.
- Output filter inductor $L = 270$ µH.
- Series inductor with LED $L_{LED} = 100$ µH.

It should be noted that the extra series inductor with LED is used to act as a low pass filter to attenuate the switching frequency harmonics and preventing it to flow through the LED chips.

5.1. Determination of the Targeted Injected Harmonics' Order Values

Firstly, using (23), the PTAR is determined for the selected conversion ratio M (in this case $M = 0.27$) For $V_{in} = 220\text{VAC} \pm 10\%$ (198 V, 220 V, 244 V) and 60 V output voltage, the PTAR is found to be 1.44, 1.41, and 1.38, respectively. It is important to highlight the advantage of this model where the designer can decide from the beginning of the design process if this resulting PTAR is acceptable or not and if another acceptable conversion ratio M has to be chosen.

Secondly, the MATLAB script is used to calculate the values of the required harmonics to be injected in the output current so that the predefined PTAR is obtained and the PF regulations are observed. Figure 8 shows the output LED current for different harmonic combination cases, as explained in the previous section. It can be shown that the peak value of the output current decreases gradually as the injected harmonic orders increases, while having the same LED current average. Figure 9 shows the input current under the same conditions. Table 1 illustrates the PTAR and the PF for each case. It is clear that Case V (with harmonics up to the tenth order) is the best one as the lowest PTAR is obtained for nominal input voltage (220 V).

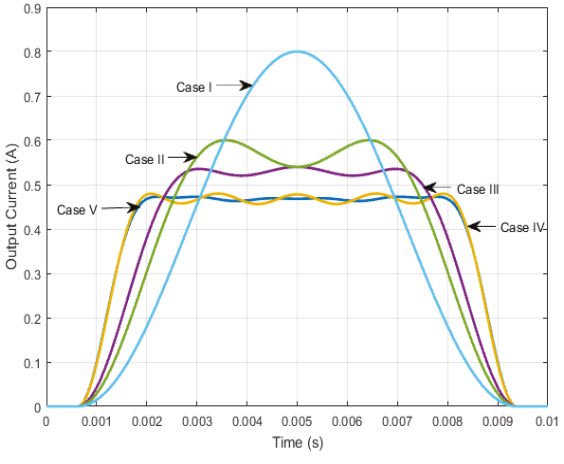


Figure 8. The LED current waveforms under different harmonics order combinations at $220V_{in}$.

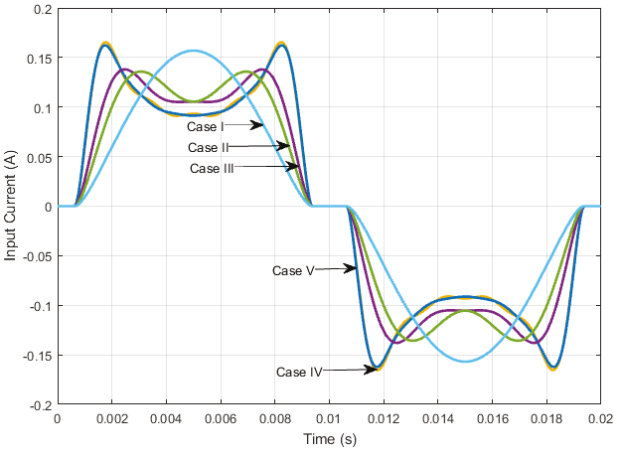


Figure 9. The input current waveform under different harmonics order combinations at $220V_{in}$.

Table 1. PTAR and PF values at different cases, V_{in} = 220 V.

Harmonics	Case I	Case II	Case III	Case IV	Case V
PF	0.983	0.979	0.963	0.9163	0.90
PTAR	2.28	1.713	1.541	1.431	1.41

5.2. Design Control Values for Single Multifunction Block (SMFB)

Once the LED current harmonics are obtained from MATLAB script, their values can be substituted in (14) in order to have the output LED current with its injected harmonic. Then, this output LED current is substituted into the duty cycle Equation (13). The resulting duty cycle is drawn and then the curve fitted as shown in Figure 10. Through this curve fitting, the Fourier components of the duty cycle waveform are obtained. Using (24), the results for the obtained gain, from the division of the duty cycle harmonics to the output LED harmonics, is plotted and fitted in Figure 11a.

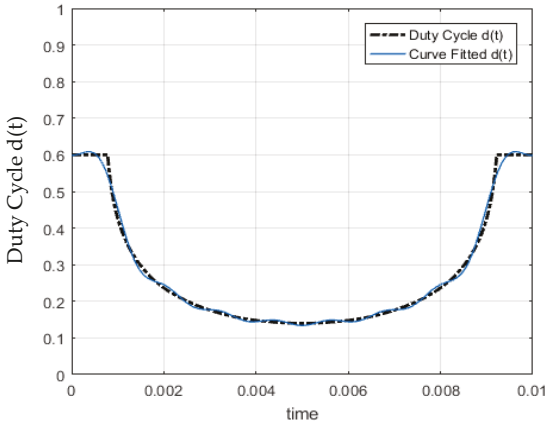
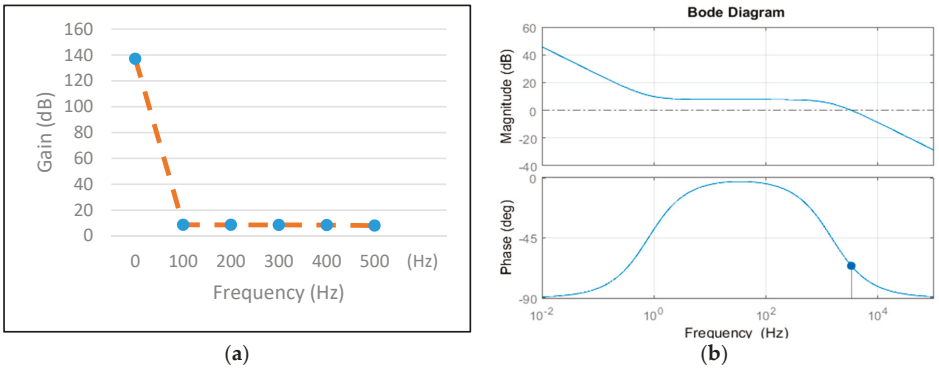


Figure 10. Duty cycle curve fitting.

It is possible to study the required features for this reshape SMFB with the results shown in Figure 11a. The required gain for the loop compensator is almost flat during the frequency range of 100 Hz–500 Hz, which is the frequency range for harmonic injection. As this analysis is concerned with the frequency range of the harmonic injection, it does not discuss the frequency range above this 500 Hz. However, this can follow regular design rules (i.e., having a low-pass filter with bandwidth in the range of one tenth of the switching frequency).



(**a**) (**b**)

Figure 11. (**a**) Model of the bode plot. (**b**) Bode diagram of the system transformation function.

A simple implementation for this proposed SMFB can be an integrator and a pole before the double line frequency, in addition to an extra pole below one tenth of the switching frequency to filter undesired harmonics component. One critical point is that the required phase should be zero

within the 100 Hz–500 Hz range to keep the line current and line voltage in phase (displacement PF requirement).

To summarize, the compensator parameters for this system can be summarized as:

1. Integrator for regulation purpose.
2. One zero at a frequency lower than one tenth of twice the line frequency to flat the gain and keep the phase angle to zero.
3. One pole between the last injected harmonic (>500 Hz, in this case) and one tenth of the switching frequency to filter undesired high frequency harmonics.

The transfer function of the described system can be presented as:

$$G_c = \frac{K\left(1+\frac{s}{W_z}\right)}{s\left(1+\frac{s}{W_p}\right)} = \frac{C_1R_2s+1}{C_1C_2R_1R_2s^2+(C_1R_1+C_2R_2)s}. \quad (25)$$

Figure 11b shows the described system bode plot with the integrator, one zero at one hertz, and one pole at 4 kHz. One advantage of the proposed system is that it has a higher bandwidth, which introduces better dynamics than conventional systems with usually 10 Hz bandwidth.

The SMFB functions are summarized in Figure 12 regulation for the LED average current, duty cycle reshaping, harmonics injection and output current reshaping.

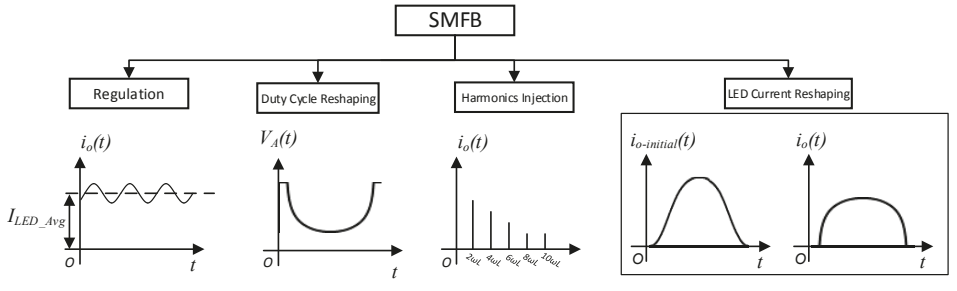


Figure 12. Single Multifunction Block (SMFB) functions.

6. Simulation & Experimental Results

To validate the proposed idea, simulation and experimentation are carried out. Figure 13a describes the circuit diagram used in both simulation and practice. It consists of the EMI filter, the rectifier bridge, and the buck converter. The buck converter switch is AOT22N50 500 V, 22 A N-Channel MOSFET and the diode is ES1J which is 1 A, 200 V Surface Mount Super-Fast Rectifier. The converter has a small output film capacitor to increase the lifetime of the LED driver. Small series resistor Surface Mount R_{sems} = 0.5 Ω 1% 0.5 W is inserted to sense the output current for the control circuit.

The compensator is a Type II, as shown in Figure 13b Due to the simplicity of the control circuit, a generic PWM controller can be used, the UC3825a IC from Texas Instrument with a few surface mount technology (SMT) components. The compensator capacitors and resistors can be calculated using (25). Table 2 shows the compensator values.

Table 2. The compensator value.

Component	R1	R2	C1	C2
Value	100 k Ω	200 k Ω	1 uF	220 pF

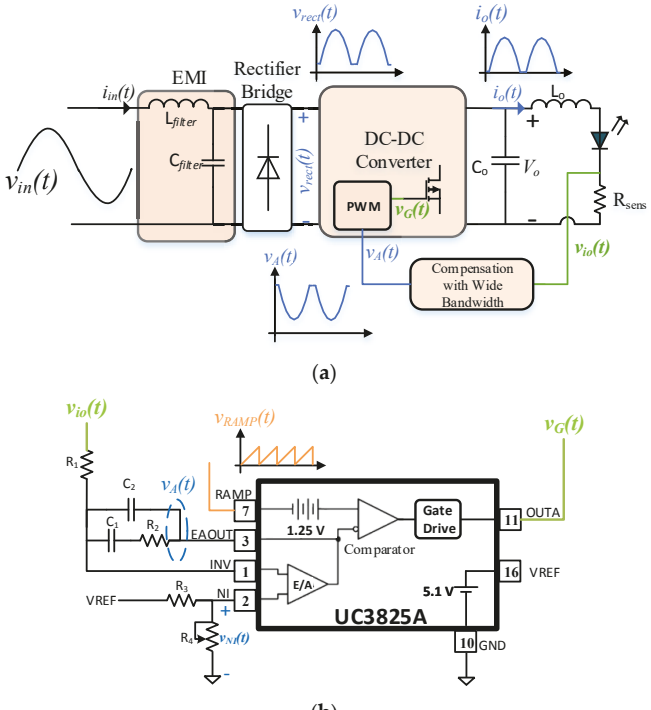


Figure 13. (**a**) Proposed circuit forharmonics injection. (**b**) Compensator circuit diagram for E-Cap less converter.

Figure 14 shows the simulation results obtained with PSIM (left column) as well as the experimental measurements on the prototype (right column). All the figures present the input voltage v_{in}, input current i_{in}, output voltage V_o and output current i_o in AC-DC electrolytic-capacitor-less buck converter. As shown, different line voltages were tested. Figure 14a,b show the results for V_{in} = 198 VAC which implies a conversion ratio of M = 0.21. The recorded PF is 0.9 and the PTAR is 1.43. Similarly, the system under study is tested for V_{in} = 220 VAC (nominal value), which represents M = 0.19, and its results are shown in Figure 14c,d. The recorded PF is 0.9 and the PTAR is 1.41. For V_{in} = 244 VAC, the results are shown in Figure 14e,f. The recorded PF is 0.9 and the PTAR is 1.39 (M = 0.17). Also, no phase shift happens between input current and line voltage as shown in the figures.

As discussed in introduction about the finding in [10], the circuit aimed to inject 3rd and 5th harmonics into the input current to eliminate the E-Cap. This was proposed using complex control technique which increase the component counts and leads to increase the LED driver technology as shown in Table 3 in compare to the proposed single-feedback loop in this paper. In addition, the mathematical model in [2] showed that the PTAR is 1.34, however the experimental results have a mismatch where a PTAR of 1.43 is reported. On the other hand, the proposed mathematical model in this paper has a good correlation with experimental results as shown in Figure 15. This graph shows different values for the PTAR and conversion ratio M under simulation, experimental and mathematical model.

Table 3. comparison between the proposed circuit and [10].

Circuit	PTAR Mathematical	PTAR Experimental	Control Circuit Component Count			No. Control Loops
			Op-Amp	Multiplier	Divider	
[10]	1.34	1.43	4	1	1	2
Proposed	1.41	1.41	2	-	-	1

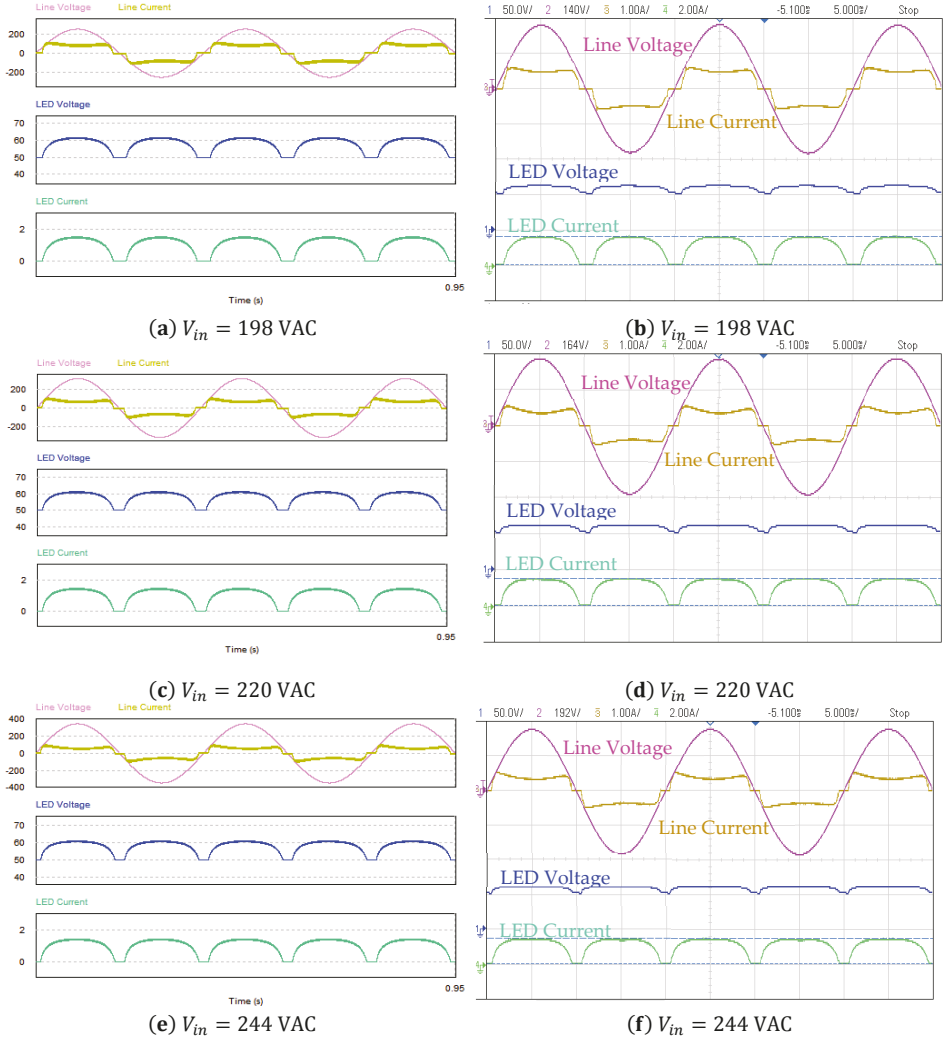


Figure 14. Simulation and prototype waveform results of input voltage v_{in}, input current i_{in}, LED output voltage V_o and output LED current i_o in buck converter.

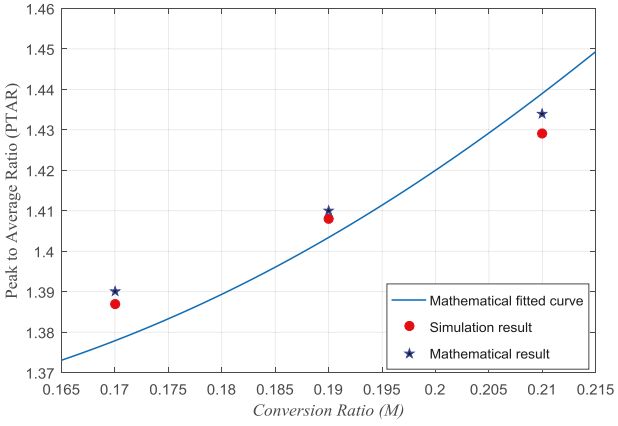


Figure 15. Obtained PTAR at different values for conversion ratio (*M*) from mathematical model, practical and simulation.

An AC-DC power converter should be complied with EN 61000-3-2 standard. This standard for limiting the harmonics current level of the electronics equipment which is injected by different loads back to the grid. Figure 16 shows a comparison between the input current values for the proposed circuit and the maximum values for EN 61000-3-2 Class D standard. This class should be complied for the lighting equipment with an input power smaller or equal than 25 W. The figure verifies that the proposed circuit is compliance with EN 61000-3-2 standard [27].

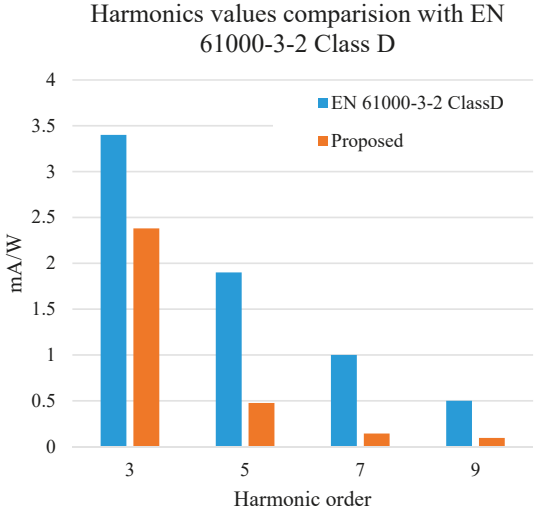


Figure 16. Comparison between the proposed Input current values and maximum level for EN 61000-3-2 Class D standard.

The proposed solution has the features of single feedback loop with low component counts for E-cap less LED solution under limited PTAR, by its turn lower cost solution. Within test, there was no record for visible flicker. However, flicker issue requires more investigation due to the increase in the LED current modulation percentage [28].

7. Conclusions

This paper has proposed the use of the complete LED model instead of the simple equivalent resistance. Its relevance and influence on the design, on the PF and on the PTAR are explored. The proposed model is derived under harmonic injection technique and it determines the required harmonic to limit the LED current PTAR and keep the input PF higher than 0.9. Based on the derived model, a reshape control block is proposed and implemented using a second-order compensator with a single feedback loop. This circuitry can be applied to different converters topologies such as Flyback converter. Results show a good agreement between simulation and experimentation. Results conclude that there is a specified range for the conversion ratio so the target PTAR can be achieved with while complying with ENERGY STAR and EN 61000-3-2 Class D standard.

Author Contributions: M.N. conceived and designed the experiments, performed the experiments, analyzed the data, and wrote the paper. M.O. define the concept, review results, supervision and manage the project. M.A. review results, revised and edited the manuscript. E.M.A., E.-S.H. co-supervised the work.

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Power and Voltage Control for Single-Phase Cascaded H-Bridge Multilevel Converters under Unbalanced Loads

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Abstract: The conventional control method for a single-phase cascaded H-bridge (CHB) multilevel converter is vector (dq) control; however, dq control requires complicated calculations and additional time delays. This paper presents a novel power control strategy for the CHB multilevel converter. A power-based dc-link voltage balance control is also proposed for unbalanced load conditions. The new control method is designed in a virtual $\alpha\beta$ stationary reference frame without coordinate transformation or phase-locked loop (PLL) to avoid the potential issues related to computational complexity. Because only imaginary voltage construction is needed in the proposed control method, the time delay from conventional imaginary current construction can be eliminated. The proposed method can obtain a sinusoidal grid current waveform with unity power factor. Compared with the conventional dq control method, the power control strategy possesses the advantage of a fast dynamic response. The stability of the closed-loop system with the dc-link voltage balance controller is evaluated. Simulation and experimental results are presented to verify the accuracy of the proposed power and voltage control method.

Keywords: cascaded H-bridge (CHB); dc-link voltage balance control; multilevel converter; power control; single-phase system

1. Introduction

Multilevel converters have gained increasing attention as of late. Commonly used multilevel converters include cascaded H-bridge (CHB), flying capacitor, and neutral-point-clamped converters [1]. Among these, the CHB converter has advantages of simple implementation, high reliability, and low harmonics [2], hence, it has been widely researched in academia and industry, particularly in relation to static synchronous compensators [3], solid-state transformers [4], and active power filters [5].

Many control schemes have been proposed to enable the pulse width modulation (PWM) converter to achieve a high power factor and near-sinusoidal grid current [6]. These strategies can be broadly classified into two categories: direct power control (DPC) and direct current control (DCC).

DPC was originally proposed by Ohnishi [7], whose method directly controls the active and reactive power of the PWM converter using three-phase instantaneous power theory. Compared with DCC, DPC has advantages of simple structure, fast dynamic response, high efficiency, and wide applicability [8]. Currently, many advanced DPC strategies have been proposed, such as predictive DPC (P-DPC) [9], deadbeat DPC [10], and slide-mode DPC [11]. In the single-phase PWM converter system, instantaneous power estimation is more complicated than in the three-phase system, which limits the development of DPC schemes in single-phase systems [12].

DCC methods have been frequently used with the PWM converter. The most commonly used DCC method utilizes vector control theory (dq control) [13–16]. Coordination transformation is needed in dq control to change the ac signals into dc signals [17]. The grid voltage phase angle is essential in the coordinate transformation; therefore, a phase-locked loop (PLL) is employed to synchronize the output voltage with the grid voltage vector [18]. To accurately obtain the information on the grid voltage including the amplitude and phase angle, some advanced PLLs have been proposed, such as hybrid filtering technique-based PLL [19], grid sequence separator PLL [20], frequency-fixed SOGI-based PLL [21], and repetitive learning-based PLL [22]. However, the computational complexity of coordinate transformation and PLL increases the calculation burden of the embedded processor like the digital signal processor (DSP) [23]. Therefore, the development of a convenient control method without PLL or coordination transformation is appealing. Recently proposed control methods of the CHB converter are based on model-predictive control (MPC) [24,25]. However, three major problems arise in the MPC scheme used for the CHB converter. First, the calculation burden persists in the MPC method because the number of switching states increases exponentially as more H-bridges are added [26]. The second one is the MPC system sensitiveness problem like sensitive to the parameter [27]. The third problem is that under unbalanced load conditions, the MPC strategy cannot provide a proper control function [28].

It is exceedingly difficult to implement the dq control scheme in the single-phase CHB converter system; imaginary orthogonal current and voltage signals must be created for coordinate transformation ($\alpha\beta$ to dq) because only one physical axis is accessible [29]. In dq control, the imaginary orthogonal current signal is essential in acquiring the dc current signals i_d and i_q for the inner current loop [30]. Thus, an imaginary current construction module is required to produce the imaginary orthogonal current signal [31]. Although the performance of conventional imaginary current construction under the steady state is mostly acceptable, the time delay tends to slow down the system dynamic response and result in further distortion [32,33].

The control scheme performance of the CHB converter in the single-phase system depends on two key factors: sinusoidal grid current waveform with unity power factor and balanced dc-link voltages [34,35]. Therefore, the CHB multilevel converters need a control method to balance the dc-link voltages, especially when the dc-side loads are unbalanced. In [36,37], the dc-link voltages were controlled using individual capacitor voltage controllers. In [38], the presented voltage balance control method uses a weighting factor to adjust the dc-link voltages. In [39], two voltage-balancing techniques were presented, allowing for much more efficient regulation of dc-link voltages. However, these voltage balanced control methods are all based on ac voltage reference duty cycle regulation; a power-based dc-link voltage balance controller has not been analyzed in detail.

In the conventional dq control strategy, the current calculation is complicated and additional time delay is required. For optimization purposes, a power control method without coordinate transformation, PLL or conventional imaginary current construction is introduced and applied to control the single-phase CHB multilevel converter system. Moreover, a power-based dc-link voltage balance control scheme is presented to make the proposed power control strategy available under unbalanced load conditions. This power and voltage control method can achieve a sinusoidal grid current waveform and balanced dc-link voltages. Several experimental tests were conducted to compare dynamic responses of the presented control scheme with those of the classical dq control method. The proposed voltage balance controller is verified as well.

The remainder of this paper is organized as follows: in Section 2, principles of the proposed control scheme and dc-link voltage balance controller are discussed, and the stability of the closed-loop system with the dc-link voltage balance controller is evaluated. Section 3 presents the simulation results. Experimental results are addressed in Section 4. The proposed control method is discussed in Section 5. Finally, relevant conclusions are drawn in Section 6.

2. Control Method Principles

2.1. Model of the Cascaded H-Bridge Multilevel Converter

Figure 1 presents the topology of a two-cell CHB system in which u_s is the grid voltage, i_{sa} is the grid current, u_c is the ac side voltage, L and R_L denote the filter inductor and line resistance, respectively,. u_{dc1} and u_{dc2} represent the dc-link voltages of the first and second H-bridge, and u_{dc_sum} is the total dc-link voltage ($u_{dc1} + u_{dc2}$). R_1 and R_2 are the resistive loads connected to the dc side of each H-bridge.

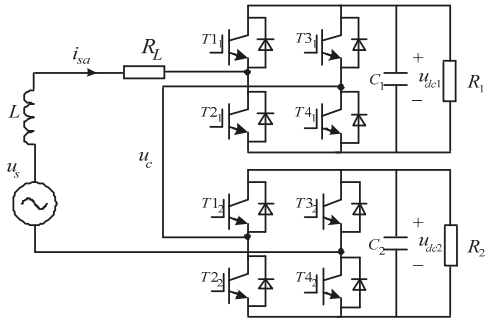

Figure 1. Two-cell single-phase CHB converter.

The mathematical model of the CHB converter is as follows:

$$\begin{cases} L\frac{di_{sa}}{dt} = u_s - u_c - R_L i_{sa} \\ u_{dc\_sum} = u_{dc1} + u_{dc2} \end{cases} \quad (1)$$

To simplify analysis of system stability, according to Equation (1), a small-signal model of the stationary reference frame ($\alpha\beta$ frame) was built, as illustrated in Figure 2. Here, $u_{s\alpha}$ equals u_s, and $u_{s\beta}$ is the orthogonal signal of u_s; $\tilde{u}_{s\alpha}$ and $\tilde{u}_{s\beta}$ represent the small-signal ac variation of $u_{s\alpha}$ and $u_{s\beta}$; $\tilde{u}_{dc1}$ and $\tilde{u}_{dc2}$ denote the small-signal ac variation of u_{dc1} and u_{dc2}; $i_{s\alpha}$ equals i_{sa}, and $i_{s\beta}$ is the orthogonal signal of i_{sa}; $\tilde{i}_{s\alpha}$ and $\tilde{i}_{s\beta}$ represent the small-signal ac variation of $i_{s\alpha}$ and $i_{s\beta}$; $I_{s\alpha}$ and $I_{s\beta}$ stand for the quiescent operating point of $i_{s\alpha}$ and $i_{s\beta}$; $D_{\alpha1}$, $D_{\alpha2}$, $D_{\beta1}$, and $D_{\beta2}$ are the duty cycles of the first and second H-bridge; and $\tilde{d}_{\alpha1}$, $\tilde{d}_{\alpha2}$, $\tilde{d}_{\beta1}$, and $\tilde{d}_{\beta2}$ represent the small-signal ac variation of $D_{\alpha2}$, $D_{\beta1}$, and $D_{\beta2}$.

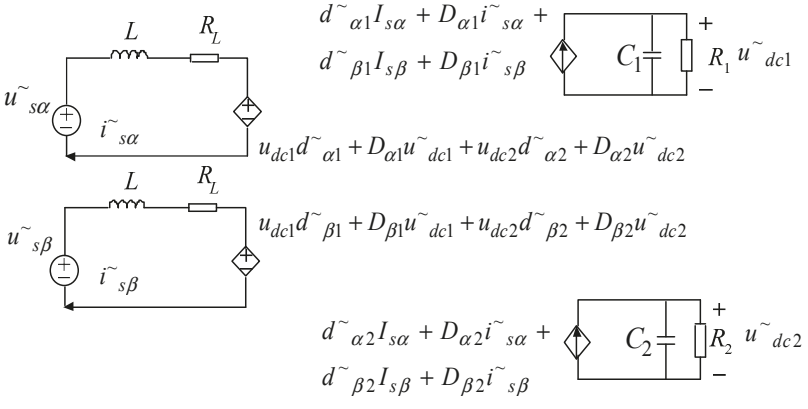

Figure 2. Small-signal model of two-cell single-phase CHB converter in $\alpha\beta$ frame coordination.

2.2. Principle of the Proposed Power Control Method

The main function of CHB multilevel converter is to obtain active power and reactive power from the grid to satisfy load needs. For the CHB converter, the essence of controlling the grid current as well as the dc-link voltage is control of the input and output power. By rapidly and effectively controlling the active and reactive power, the converter can achieve strong dynamic and static characteristics.

In the three-phase CHB converter system, the active power p and reactive power q can be described as:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} u_{s\alpha} & u_{s\beta} \\ u^*_{s\alpha} & u^*_{s\beta} \end{bmatrix} \begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \end{bmatrix} \tag{2}$$

where $u^*_{s\alpha} = u_{s\beta}$, $u^*_{s\beta} = -u_{s\alpha}$.

Only one phase physical variable is available in the single-phase CHB converter system; a second-order generalized integrator (SOGI) block is needed to introduce the imaginary signal. The virtual $\alpha\beta$ stationary reference frame is depicted in Figure 3, the α-axis coincides with the a-axis, and the β-axis is orthogonal to the α-axis.

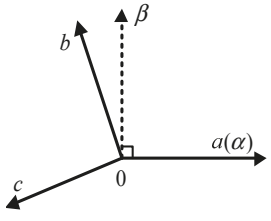

Figure 3. Schematic diagram of virtual $\alpha\beta$ coordinate axis.

In the single-phase CHB converter system, p and q can be described as follows:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \frac{1}{3}\begin{bmatrix} u_{s\alpha} & u_{s\beta} \\ u^*_{s\alpha} & u^*_{s\beta} \end{bmatrix} \begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \end{bmatrix} \tag{3}$$

p^* and q^* are defined as the active power and reactive power reference, respectively; $i^*_{s\alpha}$ and $i^*_{s\beta}$ represent the current reference.

Equations (4) and (5) are shown as follows according to Equation (3), and the coefficient calculation of the proposed power control is shown in Equation (6):

$$\begin{bmatrix} i^*_{s\alpha} \\ i^*_{s\beta} \end{bmatrix} = \frac{3}{u_{s\alpha} * u^*_{s\beta} - u^*_{s\alpha} * u_{s\beta}} \begin{bmatrix} u^*_{s\beta} & -u_{s\beta} \\ -u^*_{s\alpha} & u_{s\alpha} \end{bmatrix} \begin{bmatrix} p^* \\ q^* \end{bmatrix} \tag{4}$$

$$\begin{bmatrix} i^*_{s\alpha} \\ i^*_{s\beta} \end{bmatrix} = \begin{bmatrix} \frac{3u^*_{s\beta}}{u_{s\alpha}*u^*_{s\beta}-u^*_{s\alpha}*u_{s\beta}} p^* + \frac{-3u_{s\beta}}{u_{s\alpha}*u^*_{s\beta}-u^*_{s\alpha}*u_{s\beta}} q^* \\ \frac{-3u^*_{s\alpha}}{u_{s\alpha}*u^*_{s\beta}-u^*_{s\alpha}*u_{s\beta}} p^* + \frac{3u_{s\alpha}}{u_{s\alpha}*u^*_{s\beta}-u^*_{s\alpha}*u_{s\beta}} q^* \end{bmatrix} \tag{5}$$

$$\begin{cases} k_1 = \frac{3u^*_{s\beta}}{u_{s\alpha}*u^*_{s\beta}-u^*_{s\alpha}*u_{s\beta}} \\ k_2 = \frac{-3u_{s\beta}}{u_{s\alpha}*u^*_{s\beta}-u^*_{s\alpha}*u_{s\beta}} \end{cases} \tag{6}$$

If the grid voltage is sinusoidal, then the result of $u_{s\alpha} * u^*_{s\beta} + u^*_{s\alpha} * u^*_{s\beta}$ is constant; p^* is controlled by the outer power loop; q^* is constant because it is given directly; therefore the frequency and phase of the current references $i_{s\alpha}$ and $i_{s\beta}$ are consistent with the instantaneous grid voltage, and the real-time tracking can be achieved. Notably, only $i^*_{s\alpha}$ is used as the current reference, because the CHB multilevel converter is used on a single-phase system.

2.3. Presentation of Proposed Dc-Link Balance Controller

Figure 4 presents the conventional dc-link voltage balance controller. In this approach, the duty cycles of each ac voltage reference u^*_{a1} and u^*_{a2} are modified separately to keep the voltages balanced, and the scheme is suitable for the *dq* method. A power-based dc-link voltage balance controller adjusting the ac current reference duty cycle is introduced in this paper to regulate the individual H-bridge dc-link voltage.

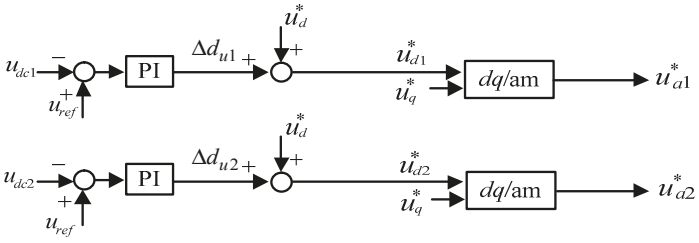

Figure 4. Conventional voltage balance controller [37].

If the dc-link voltage of each H-bridge is unbalanced (mainly via load imbalance), then the power of these H-bridges becomes uneven. To keep the dc-link voltage balanced, the uneven power should be extracted from the grid. Δd_{p1} and Δd_{p2} are used as the compensation values to eliminate uneven power. Δd_{p1} and Δd_{p2} are calculated by the voltage balance controller:

$$\begin{cases} \Delta d_{p1} = (K_p + \frac{K_i}{s})(u_{ref} - u_{dc1}) \cdot u_{dc1} \\ \Delta d_{p2} = (K_p + \frac{K_i}{s})(u_{ref} - u_{dc2}) \cdot u_{dc2} \end{cases} \tag{7}$$

where K_p and K_i represent the proportional and integral coefficient of the proportional-integral (PI) controller, respectively, and u_{ref} is the voltage reference of every H-bridge cell.

The presented voltage balance controller is shown in Figure 5, which modifies the duty cycles of each ac current reference i^*_{sa1} and i^*_{sa2} individually to reduce the dc voltage imbalance. The current reference for each H-bridge can be calculated according to Equations (8)–(10):

$$\begin{cases} i^*_{s\alpha 1} = \Delta d_{i^*sa1} + i^*_{s\alpha} \\ i^*_{s\alpha 2} = \Delta d_{i^*sa2} + i^*_{s\alpha} \end{cases} \tag{8}$$

$$\begin{cases} i^*_{s\alpha 1} = \Delta d_{p1}(k_1 + k_2) + p^*k_1 + q^*k_2 \\ i^*_{s\alpha 2} = \Delta d_{p2}(k_1 + k_2) + p^*k_1 + q^*k_2 \end{cases} \tag{9}$$

$$\begin{cases} i^*_{s\alpha 1} = k_1(\Delta d_{p1} + p^*) + k_2(\Delta d_{p1} + q^*) \\ i^*_{s\alpha 2} = k_1(\Delta d_{p2} + p^*) + k_2(\Delta d_{p2} + q^*) \end{cases} \tag{10}$$

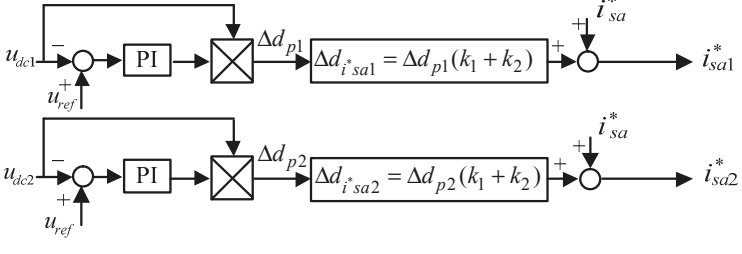

Figure 5. Proposed voltage balance controller.

2.4. Proposed Power Control of the Cascaded H-Bridge Multilevel Converter

The overall control topology of the proposed control method is depicted in Figure 6. The main idea of the proposed control is to obtain command signals in the orthogonal $\alpha\beta$ frame; as such, the dc-link voltages can be balanced.

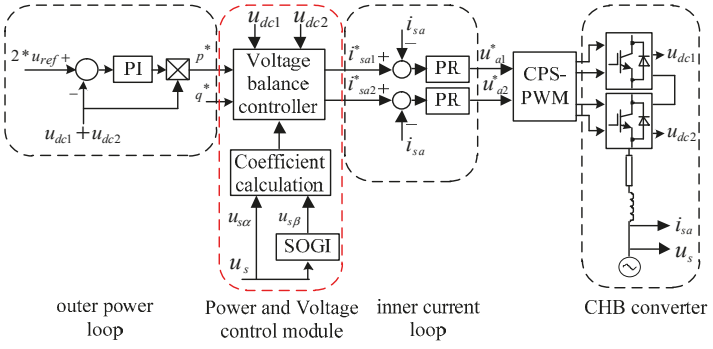

Figure 6. Proposed power and voltage control of CHB converter.

The control system is formed as a double closed-loop control structure using the inner current loop and the outer power loop.

The inner current loop is implemented in the orthogonal $\alpha\beta$ frame. Compared with classical single-phase dq schemes, the current calculation of the proposed control method is simpler because no coordinate transformation, PLL, or conventional imaginary current construction is needed. However, the current references i^*_{sa1} and i^*_{sa2} are ac variables. To track the current references with zero error in the stationary frame and achieve high tracking accuracy when the grid frequency fluctuates, rather than relying on conventional PI controllers or a repetitive controller [40], proportional-plus-resonant (PR) controllers are utilized in the current loop.

As for the outer power loop, a PI controller is used to adjust the total dc-link voltage u_{dc_sum} ($u_{dc1} + u_{dc2}$). The active power p^* is generated by multiplying the output of the PI controller by the total dc-link voltage u_{dc_sum}. Reactive power reference q^* is given directly.

The detailed control topology of the power and voltage control module is shown in Figure 7. Current reference i^*_{sa1} of the first H-bridge and i^*_{sa2} of the second H-bridge are acquired through the dc-link voltage balance control block; these current references are controlled independently. Deviation values between the grid current i_{sa} and the current references are input into the PR regulators separately, and the modulation voltage signals u^*_{a1} and u^*_{a2} are generated for the first and second H-bridge. Carrier phase-shifted PWM (CPS-PWM) technology is adopted to generate five-level voltage, achieving multi-level modulation. Furthermore, if the reactive power reference q^* is set to zero, then a unity power factor can be achieved.

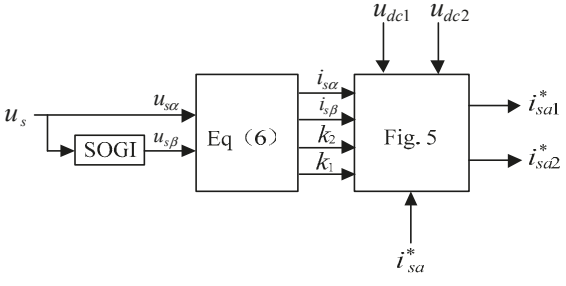

Figure 7. Power and voltage control module.

2.5. Stability Analysis of the Power and Voltage Control Scheme

Assume that the parameters of the H-bridges are identical, such that the dc-link voltage $u_{dc1} = u_{dc2} = u_{dc}$. The double-loop control diagram presented in Figure 6 can thus be transformed as illustrated in Figure 8. In Figure 8, G_V is the voltage gain of CHB, G_{PIV} is the voltage PI regulator, K is the conversion coefficient between p^* and i^*_{sa}, G_{qPR} is the current PR regulator, G_{TPWM} is the transfer function of the PWM modulator, G_{IV} is the transfer function of the voltage to output current i^*_{sa}, and G_{VI} is the transfer function of the current to output voltage u_{dc}. G_{IV} and G_{VI} can be deduced from the small-signal model shown in Figure 2.

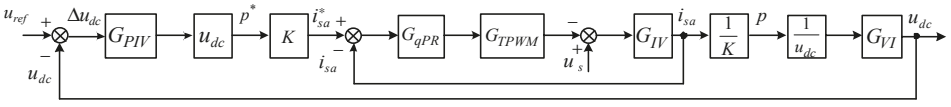

Figure 8. Basic double-loop controller structure diagram of the proposed power control.

The closed-loop transfer function can be expressed as follows:

$$G_V = \frac{G_{PIV}G_{qPR}G_{TPWM}G_{IV}G_{VI}}{1 + G_{PIV}G_{qPR}G_{TPWM}G_{IV}G_{VI}} \tag{11}$$

One bridge of the CHB converter can be simplified according to Figure 9 per Thevenin law. However, the dc-link voltage unbalance problem in CHB remains under the unbalanced load condition; therefore the voltage balance control module should be added. Figure 10 shows the Thevenin equivalent circuit with the dc-link voltage balance module, where Z_1 is the load impedance, Z_{io} is the impedance between the input and output of CHB, M is the gain of the voltage balance control module, G_1 is the conversion coefficient of power to voltage, and i_{out} is the output current. In this case $G_1 = 1/(G_{PIV} * u_{dc})$.

Taking the first H-bridge as an example:

$$G_1[p^* + (u_{ref} - u_{dc1})M]G_V = Z_{io}\frac{u_{dc1}}{Z_1} + u_{dc1} \tag{12}$$

$$u_{dc1} = \frac{G_V G_1}{Z_{io}/Z_1 + 1 + G_V G_1 M}p^* + \frac{G_V G_1 M}{Z_{io}/Z_1 + 1 + G_V G_1 M}u_{ref} \tag{13}$$

Because $Z_1 >> Z_{io}$, GG_1M represents the gain in the basic double-loop controller with the dc-link voltage balance module from Equation (13); the Bode plot is shown in Figure 11. The amplitude margin is 12.7 dB, the cut-off frequency is 272 Hz, the phase margin is 105°, and the cross-over frequency is 78 Hz. All roots of (Z_{io}/Z_1 + 1 + GG_1M) are on the left half-complex plane, ensuring stability of the system with the voltage balance control module.

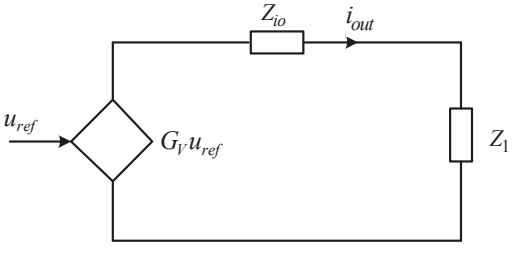

Figure 9. Thevenin equivalent circuit of the basic double-loop.

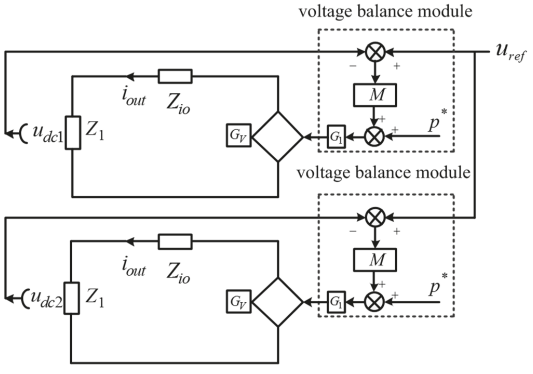

Figure 10. Thevenin equivalent circuit with the voltage balance module controller.

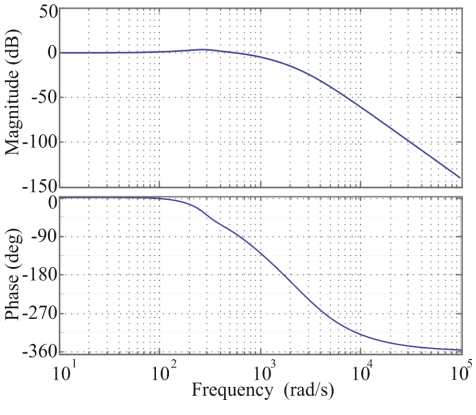

Figure 11. Bode plot of the basic double-loop controller with the dc-link voltage balance module.

3. Simulation Results

The CHB converter system shown in Figure 1 was modelled in the MATLAB/Simulink R2015a (MATLAB/Simulink R2015a, MathWorks, Natick, MA, USA) software environment to verify the power and voltage control scheme. The main system parameters used for simulation are shown in Table 1.

Table 1. Parameters Used For Simulation.

Parameter	Symbol	Simulation Value
Grid voltage *rms* value	u_s	220 V
Grid frequency	f_g	50 Hz
Input inductance	L	3.0 mH
dc-link total voltage	U_{dc}	400 V
dc-link capacitance	C_1, C_2	4700 μF
dc-link load resistance	R_1, R_2	10 Ω, 15 Ω
Switching frequency	f_{sw}	10 kHz
Inner current loop control parameters	P, R, w_c	0.5, 100, 6.28
Outer power loop control parameters	P, I	0.1, 8

3.1. Proposed Power Control Scheme Simulation

Figures 12–14 show the simulation results with unbalanced loads, where $R_1 = 10\ \Omega$ and $R_2 = 15\ \Omega$. Figure 12a displays the grid voltage and grid current waveform in the steady state, revealing that the unity power factor was achieved.

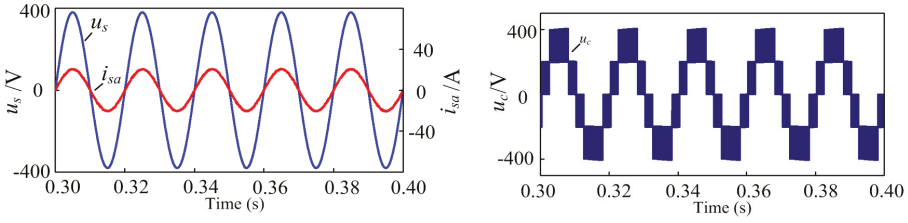

Figure 12. Simulation waveforms of CHB converter in steady state: (**a**) Grid voltage and grid current; (**b**) Five-level voltage staircase waveform.

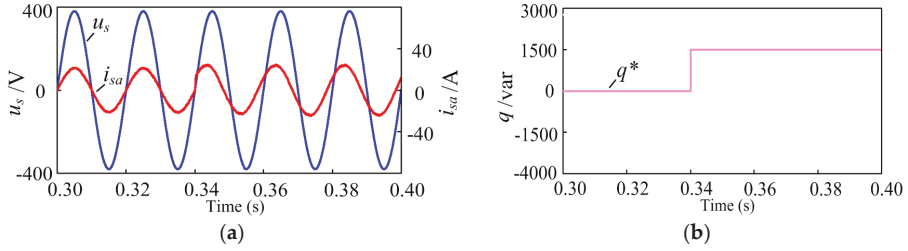

Figure 13. q^* changed from 0 var to 1500 var: (**a**) Dynamic response of the grid current; (**b**) Dynamic response of the reactive power.

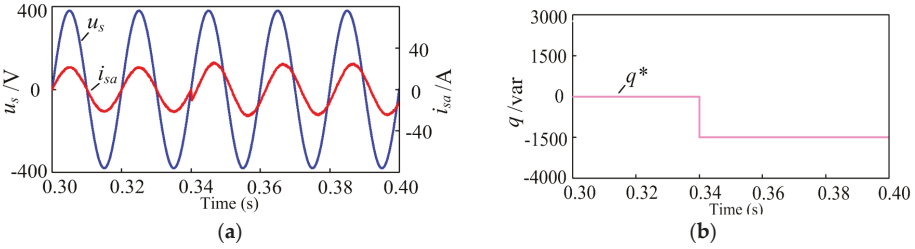

Figure 14. q^* changed from 0 var to −1500 var: (**a**) Dynamic response of the grid current; (**b**) Dynamic response of the reactive power.

Figure 12b shows the ac side five-level staircase voltage. Dynamic responses of the proposed method under sudden reactive power change conditions are shown in Figures 13 and 14. In these, the active power reference p^* is governed by the outer power loop, and the reactive power reference q^* is changed from 0 to −1500 var and 0 to 1500 var at 0.34 s.

3.2. Power-Based Voltage Balance Control Simulation

In this simulation, the initial loads of two H-bridges were 15 Ω resistors. At 1.0 s, the resistor of the first H-bridge declined to 10 Ω. Two distinct cases were considered. In Figure 15a, the voltage balance control module was not utilized, and the dc-link voltages became different after the load change. The second H-bridge, whose resistor was unchanged, demonstrated higher dc-link voltage

than the first H-bridge. Figure 15b shows the dc-link voltages with the voltage balance control method. Using the proposed voltage balance control module, the dc-link voltages returned to the initial value (200 V).

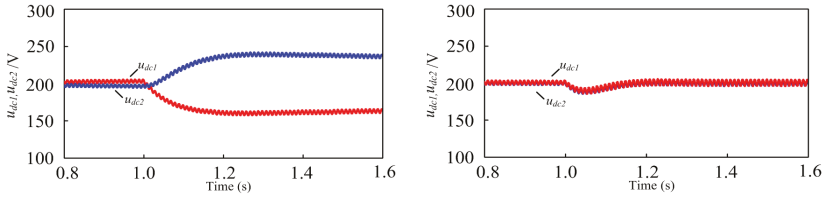

Figure 15. Simulated response of dc-link voltages when load changed: (**a**) Without voltage balance control; (**b**) With voltage balance control.

4. Experimental Results

4.1. Experimental Prototype

A single-phase five-level CHB converter experimental platform was adopted to validate the presented power and voltage control scheme, as shown in Figure 16.

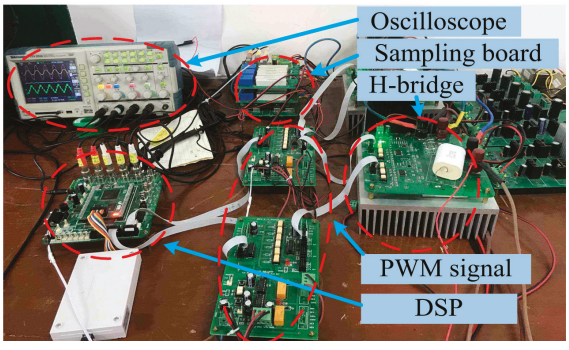

Figure 16. Platform of the experiments.

Two H-bridge converters with serially connected inputs formed the ac side of the experimental setup. The dc output of each converter fed the loads. The converter was interfaced to the grid through a coupling transformer and a voltage regulator to ensure safety during the experiments. The secondary-side voltage of the regulator was set to 80 V (rms), while the dc-link voltage references u_{dc1} and u_{dc2} were set to 50 V. The grid voltage, grid current, ac side voltage, and dc-link voltages were measured using the outer high-performance hall sensors. A TMS320F28377D DSP processor board was utilized to implement the control algorithm. Measured voltage and current signals were fed back to the DSP processor board employing a built-in, 16-bit analog-digital conversion module. The power factor and total harmonic distortion (THD) of the grid current were measured via a Fluke 435 power quality analyzer.

4.2. Steady State

Figure 17 depicts the experimental waveforms of the grid voltage u_s (200 V/division), the grid current i_{sa} (20 A/division), the dc-link voltage of the first H-bridge u_{dc1} (20 V/division), and the ac side voltage u_c (100 V/division) for the proposed scheme in the steady state, where loads R_1 and R_2 in Figure 1 are 10 Ω and 15 Ω, separately. When the reactive power reference q^* was set to zero, the grid

current was in phase with the grid voltage, so the unity power factor was achieved. The THD of the grid current in the steady state was 4.3%, indicated in Figure 18. Moreover, this method was found to compensate for the reactive power: CHB converters can generate or absorb reactive power to the power grid when the reactive power reference is positive or negative. In Figure 19, the grid current was leading the grid voltage; thus, the CHB converter was generating reactive power to the system. In Figure 20, the grid current was lagging the voltage, and the CHB converter was absorbing reactive power from the system.

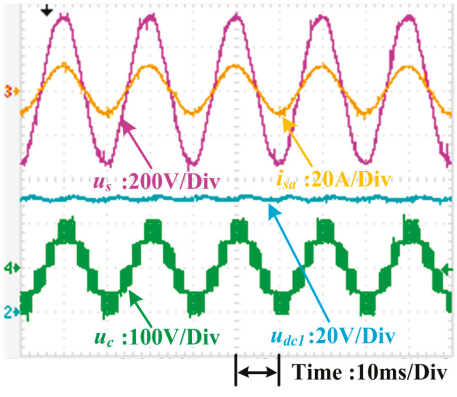

Figure 17. Experimental waveforms of CHB converter in steady state.

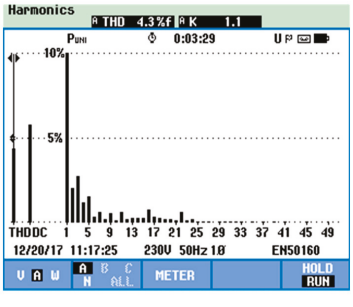

Figure 18. THD of grid current in steady state.

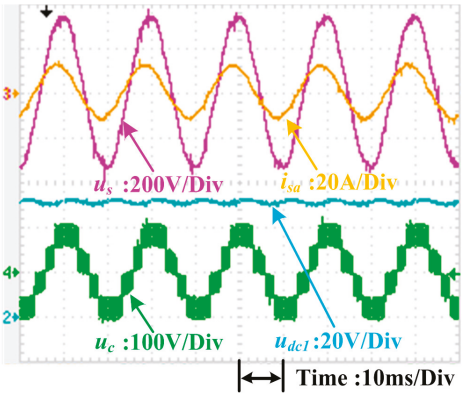

Figure 19. Experimental grid currents of CHB capacitive mode.

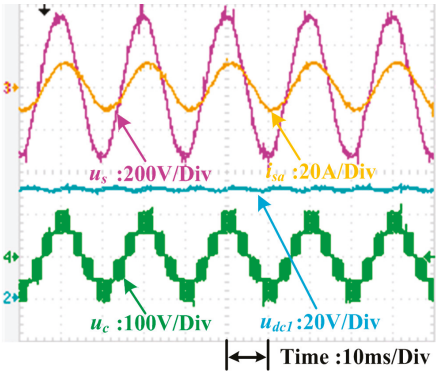

Figure 20. Experimental grid currents of CHB inductive mode.

4.3. Dynamic Response Compared with dq Control

Currently, the most popular control method for the single-phase CHB converter is *dq* control. Several experiments were carried out to compare conventional *dq* control with the proposed control method. These experiments tested the dynamic responses of the systems under sudden power change conditions. In these tests, the total dc-link voltage u_{dc_sum} was kept at 100 V, and the system was connected to two resistive loads where R_1 is 10 Ω and R_2 is 15 Ω, respectively. The dynamic of the d-axis current i^*_d in the *dq* control was managed by the outer voltage loop, and active power p^* in the proposed scheme was controlled by the outer power loop. Therefore, only step changes in the reactive current reference i^*_q in the *dq* control and reactive power reference q^* in the proposed control were applied to evaluate the dynamic control performance of each. Differences in the dynamic performance of the *dq* control scheme and the proposed control method are illustrated in Figures 21–28.

The total dc-link voltage u_{dc_sum} is 100 V; i^*_q and q^* are given directly in each control method. Reactive power reference q^* equals u_{dc_sum} * i^*_q (100 * i^*_q). For instance, when the step change of i^*_q is 5 A, the step change of q^* equals 100 * i^*_q (500 var); when the step change of i^*_q is −5 A, the step change of q^* equals 100 * i^*_q (−500 var).

As shown, the transient responses of the proposed power control method (less than 1 ms) were faster than the *dq* control method (more than 5 ms). In the *dq* control method, a time delay of 1/4 in the fundamental period arose from classical imaginary current construction.

Grid current and five-level staircase voltage continuous distortions also appeared in the *dq* control method due to conventional imaginary current construction.

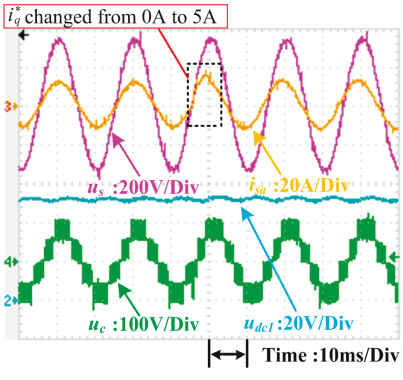

Figure 21. i^*_q changed from 0 A to 5 A (*dq* control method).

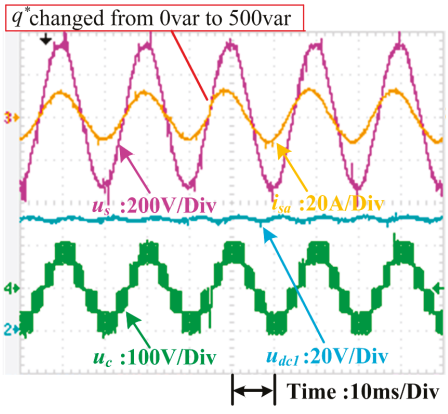

Figure 22. q^* changed from 0 var to 500 var (proposed control method).

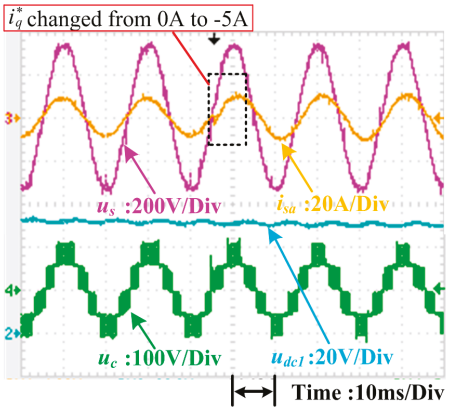

Figure 23. i^*_q changed from 0 A to −5 A (dq control method).

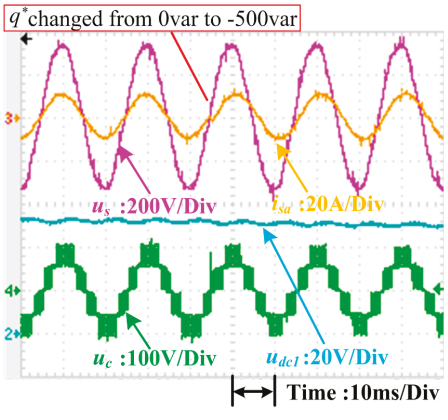

Figure 24. q^* changed from 0 var to −500 var (proposed control method).

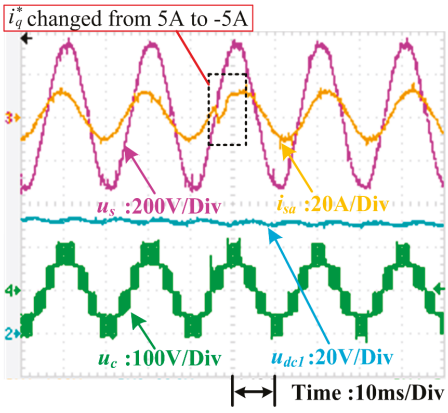

Figure 25. i^*_q changed from 5 A to −5 A (*dq* control method).

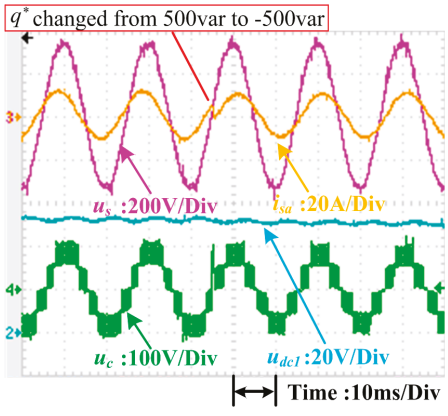

Figure 26. q^* changed from 500 var to −500 var (proposed control method).

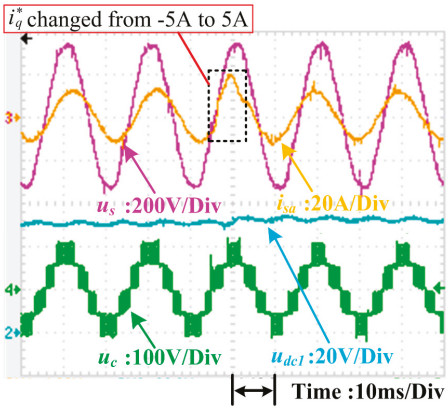

Figure 27. i^*_q changed from −5 A to 5 A (*dq* control method).

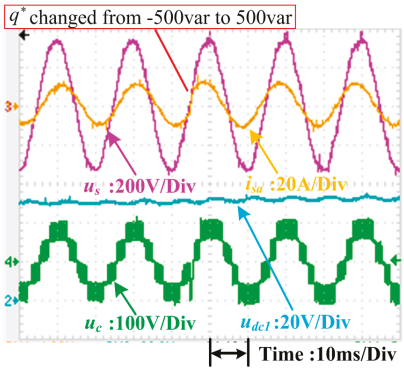

Figure 28. q^* changed from −500 var to 500 var (proposed control method).

4.4. Voltage Balance Control

Besides grid current control, balance control of the dc-link voltages is another important issue. A dc-link voltage balance control method based on power was adopted to render the proposed power control strategy applicable to the CHB converter under unbalanced load conditions.

Unbalanced load experimental tests were conducted to verify the voltage-balancing performance of the presented scheme. In these experiments, the load resistor of the first H-bridge R_1 was stepped from 15 Ω to 10 Ω whereas that of the second H-bridge R_2 was maintained at 15 Ω. In Figure 29a, when the load resistors were changed, the dc-link voltage of the first H-bridge u_{dc1} (10 V/division) declined from 50 V to 45 V, and that of the second H-bridge u_{dc2} (10 V/division) increased from 50 V to 55 V. Figure 29b shows that when the voltage balance controller was adopted, the dc-link voltages could be controlled to 50 V when the load resistors were changed. Thus, the accuracy of the presented dc-link voltage balance control method was confirmed.

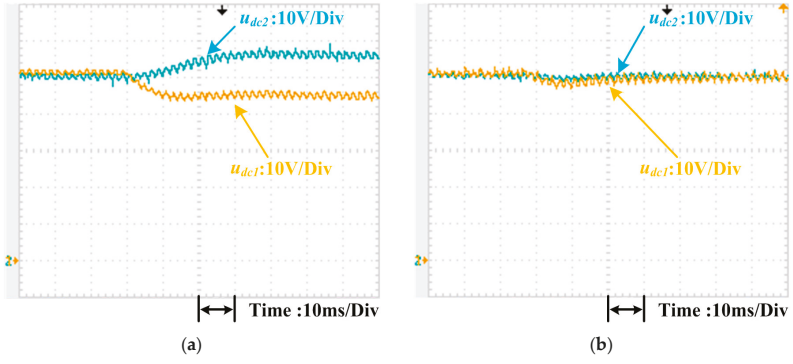

Figure 29. Experimental response of dc-link voltages when load changed: (**a**) Without voltage balance controller, (**b**) With voltage balance controller.

5. Discussion

The proposed power and voltage control method offers many advantages including no coordinate transformation, PLL, or conventional imaginary current construction. Moreover, it was found to exhibit faster transient responses and lower distortions compared with the conventional *dq* control method, as illustrated in Figures 21–28.

The natural frame control scheme presented in [23] also shows the advantages of no coordinate transformation, PLL, or conventional imaginary current construction. Differ from the natural frame

control scheme, the proposed scheme connects power control with current control through the instantaneous power theory. Besides, the proposed voltage balance control module is based on power, in which the power compensation values are used to eliminate the uneven power in active power p and reactive power q.

Even so, this control strategy has some limitations: First, although classical imaginary current construction is not necessary, the creation of an imaginary voltage component cannot be avoided. Therefore, an algorithm can be developed to reduce the time delay caused by imaginary voltage construction. Second, only the steady grid voltage condition was considered here, although abnormal operating states (e.g., grid voltage distortion) exist; thus, the control method should be optimized to make it applicable to such states.

6. Conclusions

A power control method is introduced for the single-phase CHB multilevel converter in this paper. A power-based dc-link voltage balance control module is also presented to eliminate the different dc-link voltages caused by the unbalanced loads.

The proposed power and voltage control method is designed in a virtual $\alpha\beta$ stationary reference frame without coordinate transformation or phase-locked loop. So, the complicated calculation issue can be avoided. What is more, conventional imaginary current construction is not necessary. Problems like time delay can also be avoided. The inner loop current calculation is simplified compared with the conventional dq control scheme. Stability of the proposed control scheme can be guaranteed through the analysis based on small-signal model.

Simulation and experimental results were presented to verify the effectiveness of the proposed control method. In the steady state, the proposed method can obtain the sinusoidal grid current and unity power factor under unbalanced load conditions. Upon comparing the dynamic response of the presented control strategy with that of the dq control scheme, the conducted experiments indicate that the salient feature of the proposed scheme is as follows: the proposed scheme maintains a fast dynamic response advantage over the conventional dq control method. This approach has been shown to be useful for the single-phase CHB multilevel converter system. The proposed control scheme can also be utilized with other multilevel converter systems.

Author Contributions: The individual contribution of each co-author with regards to the reported research and writing of the paper is as follows. D.Y. conceived the idea, L.Y. carried out the experiments and analyzed the data, and all authors wrote the paper.

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Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

CHB	Cascaded H-bridge
PWM	Pulse Width Modulation
DPC	Direct Power Control
DCC	Direct Current Control
P-DPC	Predictive DPC
PLL	Phase-Locked Loop
DSP	Digital Signal Processor
MPC	Model-Predictive Control
SOGI	Second-Order Generalized Integrator
PI	Proportional-Integral
PR	Proportional-plus-Resonant
CPS-PWM	Carrier, Phase-Shifted PWM
THD	Total Harmonic Distortion

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MPPT and SPPT Control for PV-Connected Inverters Using Digital Adaptive Hysteresis Current Control

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Abstract: Most PV systems are usually controlled by a Maximum Power Point Tracking (MPPT) algorithm to maximize the generated electrical power. However, the maximum power is often unstable and depends on the solar irradiance and temperature. This makes it difficult to control the power grid supply-demand balance due to fluctuations caused by the increase of renewable and variable PV systems. This paper proposes a new control algorithm for a PV-connected inverter called Specified Power Point Tracking (SPPT) control in addition to the conventional Maximum Power Point Tracking (MPPT) control. The PV system is controlled to generate the maximum power or a specified power depending on the electricity transactions comes from the electricity trading system. A high-speed FPGA-based digital adaptive hysteresis current control method, which has fast and stable response and simple structure comparing with the popular Sine-triangle Pulse Width Modulation (SPWM) method, is proposed to implement the MPPT and SPPT control. The adaptive hysteresis current band is calculated adaptively to improve a disadvantage of the classical fixed band hysteresis current control on the varying switching frequency. A reference current used in the adaptive hysteresis current control is calculated such that the output power of the PV-connected inverter is maximized in the MPPT control or is maintained at a given value in the SPPT control. The experimental and simulation results show that the PV-connected inverter under the proposed control algorithm generates the desired power almost exactly and yields stable and fast response despite the varying irradiance.

Keywords: PV-connected inverter; MPPT; SPPT; adaptive hysteresis current control

1. Introduction

Nowadays, renewable energy has become a solution to address the energy security concerns and emission standards of most countries. Photovoltaic (PV) energy systems have gained tremendous attention as one of the most promising renewable energy sources due to their advantages on the power scalability, simple installation, and low operating cost [1]. In most PV systems, the PV arrays are usually controlled by a Maximum Power Point Tracking (MPPT) algorithm to maximize the generated electrical power [2]. However, the Maximum Power Point (MPP) of the PV panel is unstable and varies with solar irradiance and temperature. This may cause problems such as voltage rise and protection problems in the utility grid [3]. Furthermore, it is difficult to control the supply-demand balance with the current power grid architecture due to fluctuations caused by the increase of renewable and variable energy generations like PV systems [4,5].

In Japan, at the end of August 2014, 1,368,749 PV projects with the total power of 69.4 GW had been approved. At that time, Kyushu Electric Power Company had approved PV generators with a capacity of 17.76 GW, which surpassed its maximum demand in summer (15.2 GW). The power company was unable to accept more PV energy and had to suspend responses to applications for grid connection

contracts for new PV projects. After that, the same issue has been raised with other power companies in Japan, such as Hokkaido Electric Power (HEPCO), Tohoku Electric Power, Shikoku Electric Power, and Okinawa Electric Power [6]. There is still a limit for the current power grid to accept the increasing PV generators.

In order to maintain the reliability of the current power grid while accepting more and more penetration of renewable energy, such as PV, a new power system concept called digital grid has been proposed [7]. The digital grid enhances the current grid by dividing a large-scale synchronized power system into some smaller size power systems called digital grid cell. The digital grid cells connect together, to the current grid, and other distributed generations via a digital grid router (DGR). In this work, in order to reduce the effect of the demand-supply balance problem caused by the PV generators in the digital grid system, we propose a control algorithm for the PV-connected inverter called Specified Power Point Tracking (SPPT) control in addition to the conventional MPPT control. The control of the PV generator is decided based on the electricity transactions that the DGR receives from the electricity trading system.

Three major classes of current control techniques have been developed over the last few decades: predictive dead-beat, sine-triangle pulse width modulation (SPWM), and hysteresis current control [8]. While the predictive dead-beat control technique tends to give accurate responses, it is complicated for implementation and its accuracy depends on the accuracy of the predictive model [9]. The asynchronous SPWM is the most popular technique and is being used in most MPPT control algorithms in PV systems, such as perturb and observe (P&O), or incremental conductance (InC) [10,11], however, it requires complicated proportional-integral (PI) regulators with undesirable delays. On the other hand, the hysteresis current control has simple structure, fast response, and independent of the inverter system parameters [12]. Because a low sampling frequency may lead to a large ripple current overshoot from the hysteresis current band, a digital hysteresis current control usually requires AD converters with sufficiently high sampling frequency to contain the ripple current within the band accurately [13]. A high sampling frequency at MHz level may be difficult for implementation on conventional microcontrollers and digital signal processors (DSPs), however, such high sampling frequency is beyond the scope of the field programmable gate array (FPGA), which can execute calculations stably at a high frequency and is becoming more and more popular in many electronics applications [14,15].

The basic implementation of hysteresis current control bases on the switching signal derived by comparing the actual current and the tolerance band of the reference current. In classical hysteresis current control, the hysteresis current band is fixed to a certain value, which makes the switching frequency vary to contain the current within the band. This leads to unwanted heavy interference among the phases in the three-phase system. In order to solve this problem, an adaptive hysteresis current control technique has been developed and applied to control the grid-connected and stand-alone multi-functional inverter of the DGR [16,17]. In this study, we propose the novel SPPT control in addition to the conventional MPPT for the PV-connected multi-functional inverter, and a method to implement the control algorithms by a high-speed FPGA-based digital adaptive hysteresis current control.

This paper is organized as follows: Section 2 introduces the concepts of digital grid and digital grid router. The digital adaptive hysteresis current control technique is presented in Section 3. Section 4 presents the MPPT and SPPT control algorithm for the PV-connected inverter using the adaptive hysteresis current control. In Section 5, the experimental and simulation results are shown to illustrate the performances of the proposed method. Conclusions are given in Section 6.

2. Digital Grid Router

The main concept of the digital grid is dividing a large synchronous grid into smaller segmented grid cells, which connect together, to the current grid, and other distributed generations via the DGR as shown in Figure 1 [18]. The DGR controls power flow of the equipment within a cell based on the

trading results receiving from the electricity trading system. The DGR also plays a role of a shock absorber so that intermittent renewable energy sources in digital grid cells will not affect the main grid. It can be used to support the stability of the main grid via energy storage such as batteries. The DGR is composed of multi-functional inverters connected to a common DC bus as shown in Figure 2. Each inverter may connect to a grid, load, PV panel, battery, or a DC sub-grid.

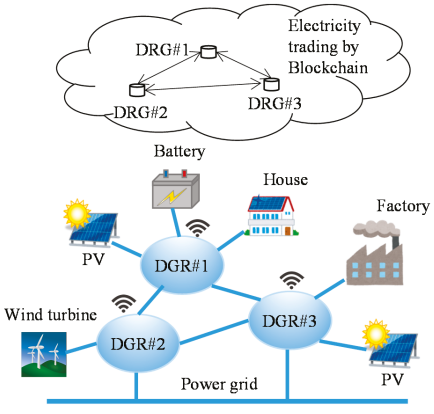

Figure 1. Digital grid system with electricity trading using block-chain.

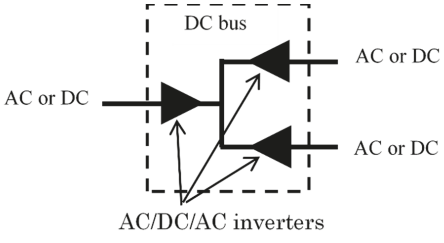

Figure 2. Structure of the digital grid router.

The electricity trading within the digital grid bases on the demand and the supply ability in each digital grid cell, whose states are sent to the trading system on the cloud by a communication network. The smart-contracts using block-chain technology enable the electricity transactions to be operated automatically with the trading algorithm likes Zaraba method [19] in stock markets. This power grid system is expected to produce a free-electricity market between decentralized grids and enable the power grid to be adaptive to the instability due to peak-demand cutting and demand-response matching issues.

3. Adaptive Hysteresis Current Control

Consider a single-phase half-bridge inverter circuit as shown in Figure 3. The inverter has two constant and balanced DC sources, each of which has a value of V_{dc}. Parameters L, L_g, and C.

Represent the hysteresis inductance, output inductance, and capacitance of the ripple current filter, respectively. Let the output current i_o of the inverter be controlled by switch devices S_1 and S_2 to track a given reference current i_{ref} The adaptive hysteresis current control is employed as shown below [16].

Define the current error $\Delta i(t)$ as:

$$\Delta i(t) = i_L(t) - i_{ref}(t), \tag{1}$$

where $i_L(t)$ and $i_{ref}(t)$ are the hysteresis current and the reference currents at the instant t. Consider an instant t_0, when the hysteresis current i_L starts to cross the lower hysteresis band, and the switch S_1 is switched on. Assume that the switch S_1 is switched on during $[t_0,\ t_1)$, and is switched off during $[t_1,\ t_2)$ intervals as shown in Figure 4.

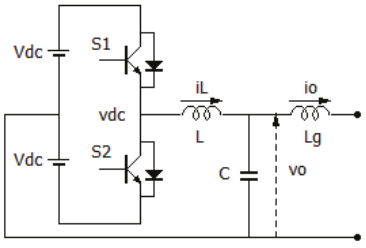

Figure 3. Single-phase half-bridge inverter circuit.

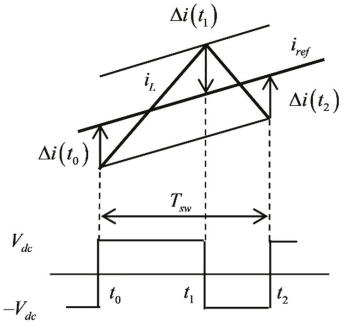

Figure 4. Adaptive hysteresis current band.

A dynamic equation for the hysteresis current can be written as:

$$L\frac{di_L(t)}{dt} = v_{dc}(t) - v_o(t), \tag{2}$$

for $t_0 \le t \le t_2$, where v_o is the instantaneous output voltage and $v_{dc}(t)$ is the inverter input DC voltage elaborated as:

$$v_{dc}(t) = \begin{cases} V_{dc} & if\ S_1\ is\ On \\ -V_{dc} & if\ S_1\ is\ Off \end{cases}. \tag{3}$$

Define the slopes of the hysteresis current in the on and off switching periods by $\dot{I}_{on}$ and $\dot{I}_{off}$ respectively. By assuming that the output voltage v_o is slowly varying during the switching modulation period $[t_0,\ t_2]$, the hysteresis current slopes can be expressed by:

$$s_{on} = \frac{di_L(t)}{dt} = \frac{V_{dc} - v_o(t_0)}{L} \tag{4}$$

for $t \in [t_0,\ t_1)$, and:

$$s_{off} = \frac{di_L(t)}{dt} = \frac{-V_{dc} - v_o(t_0)}{L} \tag{5}$$

for $t \in [t_1,\ t_2)$.

The current errors at t_1 and t_2 are given by:

$$\begin{aligned}\Delta i(t_1) =& i_L(t_1) - i_{ref}(t_1)\\ =& i_{ref}(t_0) + \Delta i(t_0) + s_{on}T_{on} - i_{ref}(t_1)\end{aligned} \tag{6}$$

$$\begin{aligned}\Delta i(t_2) =& i_L(t_2) - i_{ref}(t_2)\\ =& i_{ref}(t_0) + \Delta i(t_0) + \Big(s_{on}T_{on} + s_{off}T_{off}\Big) - i_{ref}(t_2)\end{aligned} \tag{7}$$

where:

$$T_{on} = t_1 - t_0, \tag{8}$$

$$T_{off} = t_2 - t_1. \tag{9}$$

The reference current $i_{ref}(t)$ is slowly varying during the modulation period, such that it can be approximated as:

$$i_{ref}(t_1) = i_{ref}(t_0) + di_{ref}(t_0)T_{on}, \tag{10}$$

$$i_{ref}(t_2) = i_{ref}(t_0) + di_{ref}(t_0)\Big(T_{on} + T_{off}\Big), \tag{11}$$

where $di_{ref}(t_0)$ is derivative of the reference current $i_{ref}(t)$ with respect to t at $t = t_0$.

Substituting Equations (10) and (11) into Equations (6) and (7), we can write the current errors $\Delta i(t_1)$, and $\Delta i(t_2)$ as:

$$\Delta i(t_1) = \Delta i(t_0) + s'_{on}T_{on}, \tag{12}$$

$$\begin{aligned}\Delta i(t_2) =& \Delta i(t_0) + s'_{on}T_{on} + s'_{off}T_{off}\\ =& \Delta i(t_1) + s'_{off}T_{off}\end{aligned}, \tag{13}$$

where s'_{on}, s'_{off} are given as:

$$s'_{on} = s_{on} - di_{ref}(t_0) = \frac{V_{dc} - v_o(t_0)}{L} - di_{ref}(t_0), \tag{14}$$

$$s'_{off} = s_{off} - di_{ref}(t_0) = \frac{-V_{dc} - v_o(t_0)}{L} - di_{ref}(t_0). \tag{15}$$

Let f_{sw} is a desired constant switching frequency. In the adaptive hysteresis current control method, the hysteresis current band $\Delta i_b(t_0)$ is derived by using the following conditions:

$$\Delta i(t_1) - \Delta i(t_0) = 2\Delta i_b(t_0), \tag{16}$$

$$\Delta i(t_2) - \Delta i(t_1) = -2\Delta i_b(t_0), \tag{17}$$

$$T_{on} + T_{off} = T_{sw}, \tag{18}$$

where $T_{sw} = 1/f_{sw}$. Substituting Equations (16)–(18) into Equations (12) and (13), we can derive the hysteresis current band as:

$$\Delta i_b(t_0) = \frac{1}{2f_{sw}}\frac{s_{on}s_{off}}{s_{off} - s_{on}}. \tag{19}$$

By substituting Equations (14) and (15) into Equation (19), the hysteresis current band in Equation (19) can also be written in the form of:

$$\Delta i_b(t_0) = \frac{1}{4Lf_{sw}V_{dc}}\left\{{V_{dc}}^2 - \Big[v_o(t_0) + Ldi_{ref}(t_0)\Big]^2\right\}. \tag{20}$$

For a digital control system, where the measured voltage and current is sampled by analog/digital converters, the hysteresis current band under zero-order-holds (ZOHs) can be written by:

$$\Delta i_b(t) = \frac{1}{4Lf_{sw}V_{dc}}\left\{{V_{dc}}^2 - \left[v_o(kT_{sp}) + Ldi_{ref}(kT_{sp})\right]^2\right\}, \tag{21}$$

where $kT \leq t < (k+1)T$ and T is a sampling interval.

4. Hysteresis Current Control for PV-Connected Inverter

Consider a half-bridge inverter circuit with a PV panel connected between the output and the negative voltage of the inverter as shown in Figure 5. The voltage of the PV panel can be calculated from the output voltage v_o of the inverter as:

$$V = v_o + V_{dc}. \tag{22}$$

The algorithms for MPPT and SPPT controls are described below.

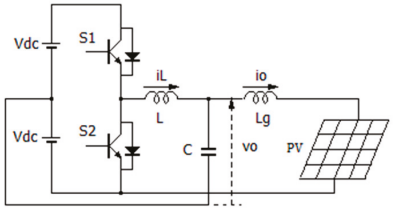

Figure 5. PV connected inverter circuit.

4.1. Algorithm for MPPT Control

Figure 6 shows voltage-current and voltage-power characteristic curves of the PV panel. The maximum power point (MPP) can be determined by a point, at which the derivative of output power P with respect to the voltage V is zero, i.e.:

$$\frac{dP}{dV} = 0. \tag{23}$$

Consider a digital control system, where the measured voltage and current are sampled by analog/digital converters with a sampling interval T. Let sampled-values of the voltage and current of the PV at a sampled instant kT are V_k and I_k. Then, the power P_k at instant kT is calculated as:

$$P_k = V_k I_k. \tag{24}$$

The derivative of the power with respect to the voltage at instant kT for the sampled-value can be written by:

$$\left.\frac{dP}{dV}\right|_k = \frac{\Delta P_k}{\Delta V_k} = \frac{P_k - P_{k-1}}{V_k - V_{k-1}}. \tag{25}$$

The algorithm for hysteresis current control tracking the MPP is as below:

1 : **if** $\frac{\Delta P_k}{\Delta V_k} = 0$
2 : $\quad i_{ref\_k} = i_{ref\_k-1}$
3 : **else**
4 : $\quad$ **if** $\frac{\Delta P}{\Delta V} > 0$
5 : $\quad\quad i_{ref\_k} = i_{ref\_k-1} + \delta i$
6 : $\quad$ **else**
7 : $\quad\quad i_{ref\_k} = i_{ref\_k-1} - \delta i$

where $\delta i > 0$ is a step-size of the reference current. It should be noted that due to the definition for direction of the output current from the inverter as shown in Figure 5, the reference current in this case takes only negative value.

The MPP divides the characteristics of the PV panel into two areas: positive power derivative dP/dV and negative power derivative dP/dV as shown in Figure 6. When the state of the PV panel is in the positive power derivative area, the reference current is decreased. On the contrary, when the state of the PV panel is in the negative power derivative area, the reference current is increased by a step-size δi. This process is continued until the state of the PV arrives the MPP. At the MPP, the reference current is unchanged. While the reference current is changed by the definite step-size δi, the output power of the PV panel may not identify to the MPP exactly. In order to avoid an oscillation of the reference current at the steady stay around the MPP, the MPP can be replaced by a maximum power bandwidth. Then, the MPPT algorithm can be revised as below.

$$
\begin{aligned}
&1: \textbf{if } \left|\frac{\Delta P_k}{\Delta V_k}\right| \leq \delta P_M \\
&2: \quad i_{ref\_k} = i_{ref\_k-1} \\
&3: \textbf{else} \\
&4: \quad \textbf{if } \frac{\Delta P}{\Delta V} > \delta P_M \\
&5: \quad\quad i_{ref\_k} = i_{ref\_k-1} + \delta i \\
&6: \quad \textbf{else} \\
&7: \quad\quad i_{ref\_k} = i_{ref\_k-1} - \delta i
\end{aligned}
$$

where $\delta P > 0$ is the bandwidth of the MPP.

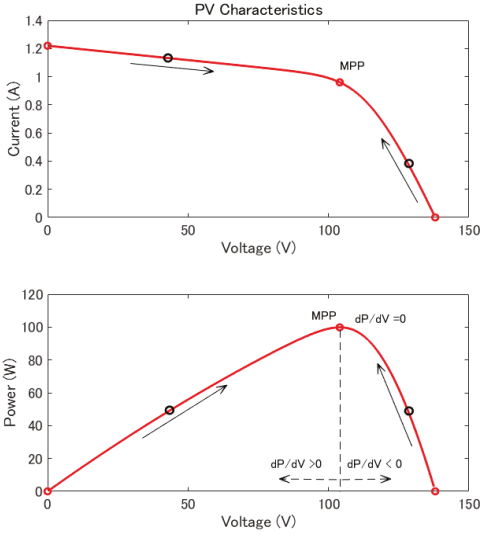

Figure 6. Characteristic PV and MPPT control curves.

4.2. Algorithm for SPPT Control

Let the PV-connected inverter is controlled to generate a given specified power P_s, which is assumed to be less than the generable maximum power. There are two points on the characteristic curves of the PV panel can generate the given power P_s as shown in Figure 7.

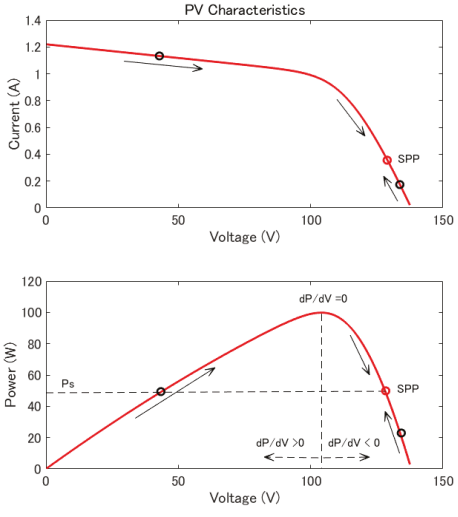

Figure 7. Characteristic PV and SPPT control curves.

However, in order to reduce the power loss, the point in the positive power derivative area, which has smaller current, is preferred. The algorithm tracking the specified power point (SPP) is as below:

$$
\begin{aligned}
&1: \textbf{if } P_k = P_s \\
&2: \quad i_{ref\_k} = i_{ref\_k-1} \\
&3: \textbf{else} \\
&4: \quad \textbf{if } (_k < P_s)P \cap \left(\tfrac{\Delta P}{\Delta V} < 0\right) \\
&5: \quad\quad i_{ref\_k} = i_{ref\_k-1} - \delta i \\
&6: \quad \textbf{else} \\
&7: \quad\quad i_{ref\_k} = i_{ref\_k-1} + \delta i
\end{aligned}
$$

The reference current is unchanged when the output power equals to the given power P_s. When the output power is less than the given power P_s and the state of the PV panel is in the negative power derivative area of the SPP, the reference current is increased. In the other cases, the reference current is decreased by the step-size δi. This process is continued until the state of the PV panel arrives the SPP. By the same way of the MPPT control, in order to avoid an oscillation of the reference current at the steady state around the SPP, the SPP can be replaced by a specified power bandwidth. Then, the SPPT algorithm can be revised as below:

$$
\begin{aligned}
&1: \textbf{if } |P_k - P_s| \leq \delta P_S \\
&2: \quad i_{ref\_k} = i_{ref\_k-1} \\
&3: \textbf{else} \\
&4: \quad \textbf{if } (P_k < P_s - \delta P_S) \cap \left(\tfrac{\Delta P}{\Delta V} < 0\right) \\
&5: \quad\quad i_{ref\_k} = i_{ref\_k-1} - \delta i \\
&6: \quad \textbf{else} \\
&7: \quad\quad i_{ref\_k} = i_{ref\_k-1} + \delta i
\end{aligned}
$$

where $\delta P_S > 0$ is the specified power bandwidth.

5. Experimental Results

5.1. Grid-Connected PV System

Consider a DGR composed of two multi-functional inverters with a common DC bus, which is composed of electrolytic capacitors C_1 and C_2 as shown in Figure 8. The first inverter connects to a PV panel and another one connects to an AC power grid. The grid-connected inverter is controlled to maintain the voltages of capacitors C_1 and C_2 at a given constant value V_{dc_ref}. The PV-connected inverter sends the power generated by the PV panel to the common DC bus, and the grid-connected inverter sends that power from the common DC bus to the grid.

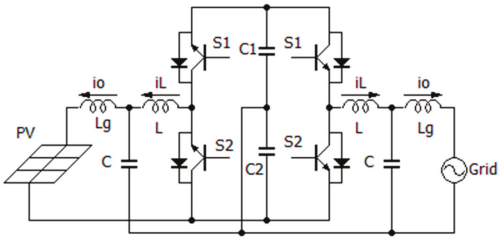

Figure 8. Grid-connected PV panel circuit.

Let v_1 and v_2 are the voltages of capacitors C_1 and C_2. The grid has a voltage of v_g. In this work, the grid-connected inverter is controlled by using the adaptive hysteresis current control presented in session 3 with the reference current is calculated as [18]:

$$i_{ref}(kT) = -k_t\Big(2V_{dc\_ref} - (v_1(kT) + v_2(kT))\Big)\frac{v_g(kT)}{\sqrt{2}V_g} + k_b(v_1(kT) - v_2(kT)), \tag{26}$$

where k_t, $k_b > 0$ are the control gains, which tune the speed of the response, V_g is an effective value of the grid voltage v_g.

5.2. Simple Model for PV Panel

Due to space constraints of the laboratory, a simple electrical circuit composing of a DC power source and a variable resistor as shown in Figure 9 is used to emulate the PV panel. The voltage-current and voltage-power characteristics of this PV model are as below.

The output power P of this PV model is calculated as:

$$P = VI. \tag{27}$$

Using Kirchhoff's rule for the circuit shown by Figure 9, we have:

$$V_{DC} = V + RI. \tag{28}$$

Substituting Equation (28) into Equation (27), we can write the output power P as:

$$P = \frac{1}{R}V(V_{DC} - V). \tag{29}$$

The voltage-current and voltage-power characteristic curves of the PV model given by Equations (28) and (29) can be figured by Figure 10. The maximum power point can be determined as:

$$V_{\max} = \frac{V_{DC}}{2}, \tag{30}$$

$$I_{\max} = \frac{V_{DC}}{2R}, \tag{31}$$

$$P_{\max} = \frac{{V_{DC}}^2}{4R}. \tag{32}$$

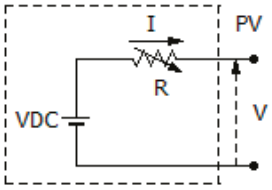

Figure 9. Electrical model for PV panel.

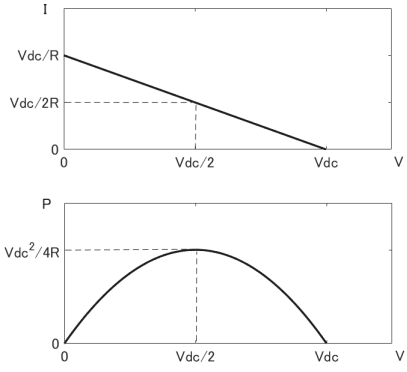

Figure 10. Voltage-current and voltage-power characteristic curves of the PV model.

In Figure 10, it can be seen that the value of the variable resistor R may change the voltage-power and voltage-current characteristics of the PV model. Thus, the variable resistor R can be used to emulate the variation of the solar irradiance. Although the PV model showed in Figure 9 emulates only the basic voltage-current and voltage-power characteristics of the PV panel, it is efficient for the purpose of evaluating the MPPT and SPPT algorithms for the PV control.

5.3. Experimental Results

The proposed control algorithm for the PV-connected inverter has been assessed by using a prototype of the DGR, which is composed of two multi-functional inverters connected by the circuit shown in Figure 8. The experimental setup is shown by Figure 11. Each inverter has a rated power of 300 W. The circuit parameters of the inverters are given by: L = 2.2 mH, L_g = 1.1 mH, and C = 6.8 μF. The reference voltage of the DC bus V_{dc_ref} is set at 175 V. The analog/digital converter (ADC) has the sampling frequency of 4 MHz. The switching transistors in the inverter circuit are IGBT devices with the dead-time at 1.5 μ sec. The constant switching frequency in the adaptive hysteresis current control is at 20 kHz. The control algorithm is implemented on a FPGA board, which has a clock frequency of 160 MHz. The grid has an AC voltage of 100 V and frequency of 50 Hz. The DC power source of the PV model V_{DC} in Figure 10 is at 250 V. The step-size δi of the reference current is at 0.1 A.

Table 1 shows experimental result data for the MPPT control with various solar irradiances, which is emulated by the variable resistor in the PV model. The output power of the PV-connected inverter matches with the maximum power of the PV model calculated using Equation (32) almost exactly.

Table 2 shows experimental result for the same system controlled by SPPT algorithm with the specified power of $P_s = 150$ W. The output power of the inverter is kept at the specified power P_s regardless to the variation of the solar irradiance. Figure 12 shows the voltage and current responses of the grid-connected and PV-connected inverters controlled by the MPPT algorithm with the solar irradiance emulating resistor R at 80 W. Figure 13 shows the responses of the same inverter controlled by the SPPT algorithm. In all the tested cases including that for different value of R, the PV-connected inverter generates a power, which exactly matches the desired power. The grid-connected inverter sends the power generated from the PV-connected inverter to the grid and keeps the voltage of the common DC bus at constant. The voltage and current responses of the both inverters are stable for all tested cases.

Table 1. Experimental result data for MPPT control.

Resistor R [Ω]	Measured Current I [A]	Measured Voltage V [V]	Measured Power P [W]	Calculated Power P [W]
100	1.19	131	155	156
80	1.38	140	194	195
60	1.87	136	254	260

Table 2. Experimental result data for SPPT control.

Resistor R [Ω]	Measured Current I [A]	Measured Voltage V [V]	Measured Power P [W]	Specified Power P_s [W]
100	0.9	161	145	
80	0.76	191	144	150
60	0.72	208	148	

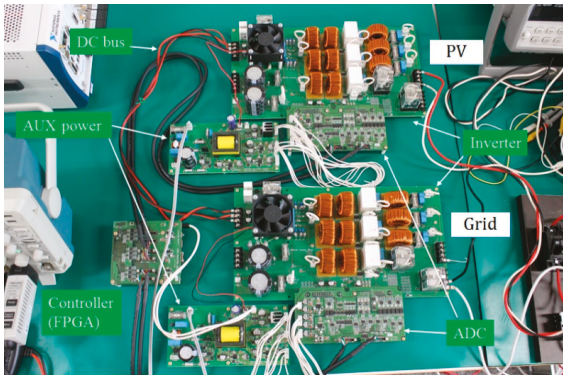

Figure 11. Experimental DGR circuit.

Figures 14 and 15 show the responses of the inverters with the MPPT control when the solar irradiance emulating resistor R changes from 60 W to 100 W and contrarily from 100 W to 60 W, respectively. The experimental results show that the proposed control algorithm yields responses, which are stable and adapt to the variation of the solar irradiance quickly.

Simulations have been carried out to compare the proposed MPPT algorithm using adaptive hysteresis current control with other common MPPT algorithms based on SPWM technique by using

Matlab-Simulink. Figures 16–19 shown the responses of the PV panel for the proposed MPPT, the perturb and observe (P&O) [20], and the incremental conductance (InC) [21], and fractional open-circuit voltage (FOCV) [22] algorithms, respectively. While the P&O and the InC algorithms yield unstable responses with oscillations when the irradiance changes, the proposed and FOCV algorithms give smooth and fast responses without oscillation. However, the proposed algorithm is simpler than the FOCV algorithm, which is based on complicated calculations using a PI regulator.

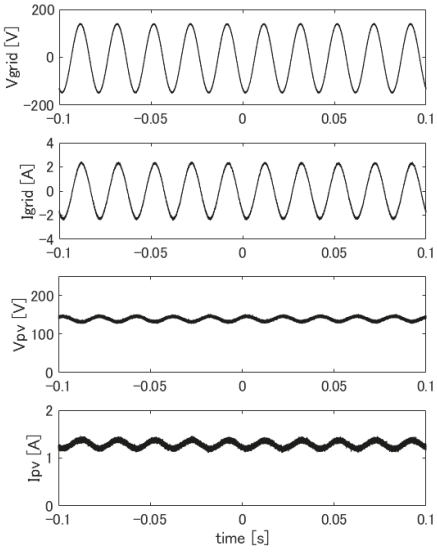

Figure 12. Responses of grid-connected and PV-connected inverters under MPPT control with $R = 80\ \Omega$.

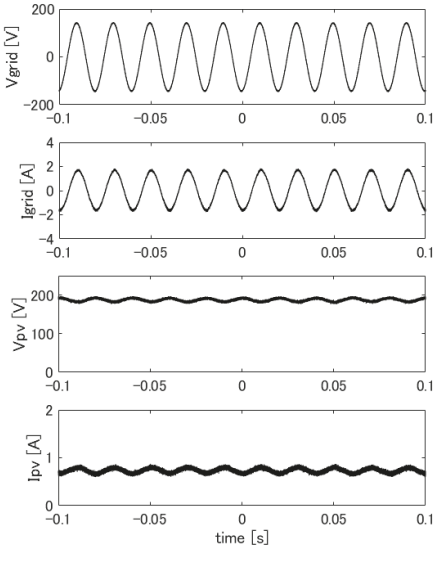

Figure 13. Responses of grid-connected and PV-connected inverters under SPPT control with $R = 80\ \Omega$.

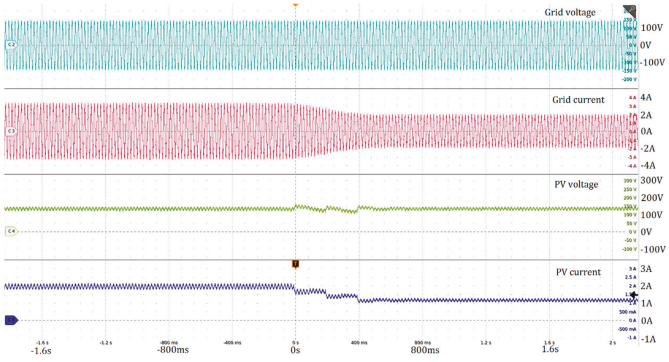

Figure 14. Responses of grid-connected and PV-connected inverters under MPPT control when the resistor *R* changes from 60 W to 100 W.

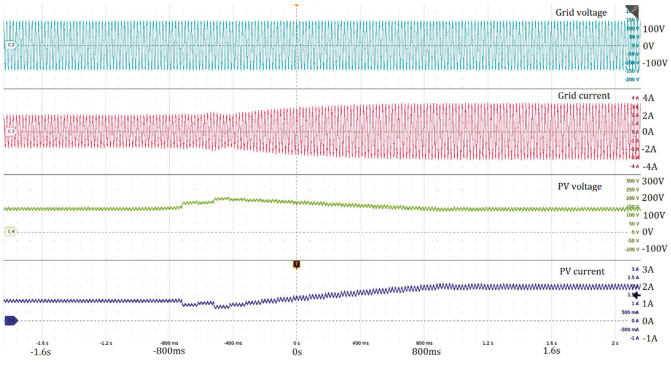

Figure 15. Responses of grid-connected and PV-connected inverters under MPPT control when the resistor *R* changes from 100 W to 60 W.

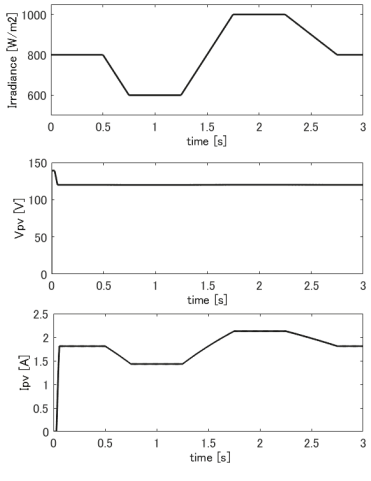

Figure 16. Responses of the proposed MPPT control with the varying irradiance.

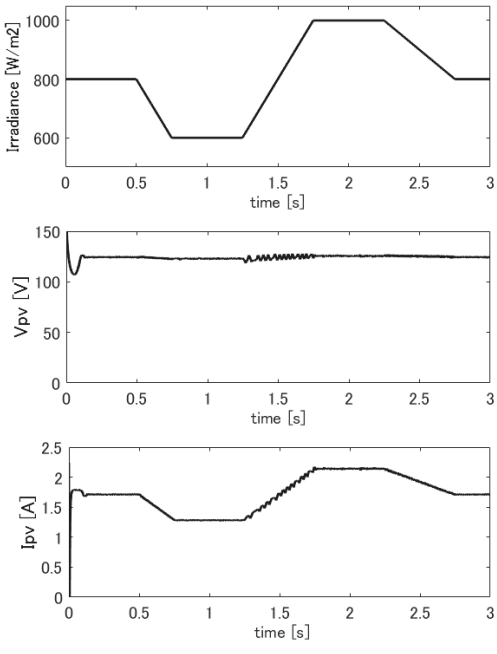

Figure 17. Responses of the P&O control with the varying irradiance.

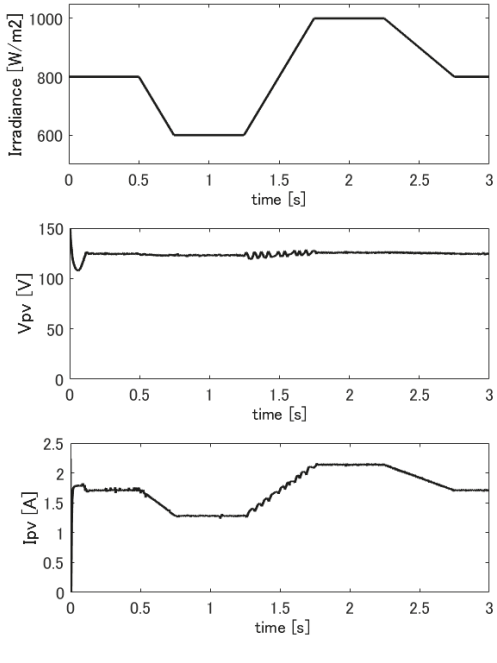

Figure 18. Responses of the InC control with the varying irradiance.

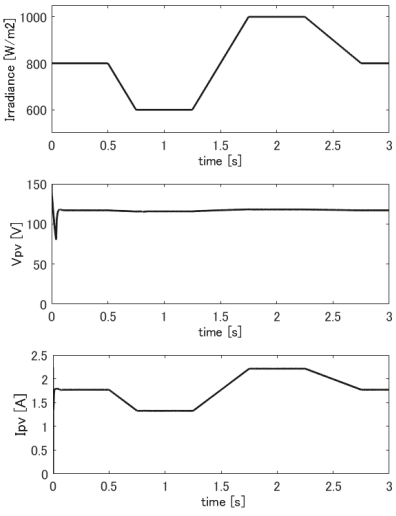

Figure 19. Responses of the FOCV control with the varying irradiance.

6. Conclusions

A new control algorithm for PV-connected inverters called Specified Power Point Tracking (SPPT) control has been proposed in addition to the conventional MPPT control. The PV system is controlled to generate the maximum power or a specified power depending on the electricity transactions. The control algorithm is based on high-speed FPGA-based digital adaptive hysteresis current control, which has a fast and stable response, and a simple structure compared with the conventional sine-triangle PWM method and can improve the disadvantages of the classical fixed band hysteresis current control on the varying switching frequency. The reference current is calculated such that the output power is maximized in the MPPT control or is maintained at a given value in the SPPT control. The hysteresis current control enables us to use the same multi-functional inverter hardware connecting to the PV, the grid, or the load in stand-alone system just by changing the calculation for the reference current. The experimental results show that the PV-connected inverter under the proposed control algorithm generates the desired power almost exactly with stable and fast response despite the varying solar irradiance. The simulation results show that the proposed MPPT control algorithm give better performance than the common MPPT algorithms such as P&O, InC, and FOCV. The proposed MPPT and SPPT control algorithm enables us to control of the PV system based on the electricity transactions receives from the electricity trading system. This operation method is expected to contribute to the improvement of the demand-supply balance problem, which is inhibiting the vast employment of renewable energy.

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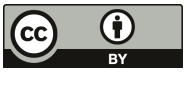

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Design of Current Programmed Switching Converters Using Sliding-Mode Control Theory

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Abstract: This paper presents a comprehensive approach to analyze and design the voltage and current loops of switching DC-DC converters by using sliding-mode control theory. The approach is interchangeably applied to switching converters under current-programmed control with both fixed and variable frequency modulation. An ideal sliding-mode dynamics model is then obtained together with its circuit schematic representation that can be used for designing the output voltage compensator, as well as to predict the large signal behavior such as during start-up and under large disturbances. Simulations and experimental measurements illustrate the theoretical approach for two different examples of switching converters.

Keywords: switching converters; sliding-mode control; current-mode control; hysteresis control

1. Introduction

Switched mode power converters are widely used for power processing in different applications such as in portable devices, solid-state lighting drivers and technologies for renewable energy production. With the aim of either regulating an output variable to a desired reference or balancing the values of different variables, a control strategy is needed [1–3].

One of the key factors affecting the response of these systems is the control mode used. Conventional Voltage Mode Control (VMC) is a simple single feedback loop with only the output voltage as a control variable. However, its first generation version features poor response against load changes [2]. Current Mode Control (CMC), also known in the literature as current-programmed control [4], utilizes the inductor current as an additional control variable, which improves the transient response [2] at the expense of extra cost and more complex controller design. CMC of power converters is nowadays an extensive design practice due to its intrinsic advantages and the existence of an important number of dedicated commercial chips that facilitate its implementation. CMC offers superior performances over conventional VMC in both parallel operation of power converters [5] and voltage regulation of non-minimum phase switching conversion structures [6]. In the first case, current sharing among the different converters of the parallel ensemble is a relatively simple task for both static and dynamic sharing [5], while in the second case, CMC is the best solution for an indirect output voltage regulation [7].

A usual way of controlling switching converters consist of imposing the duration during which a switch is maintained closed or open. In CMC, the control strategy must impose switching instants for the switches by comparing the inductor current with a desired reference. Under fixed switching frequency operation, there are three main types of CMC strategies, namely peak CMC, valley CMC and average CMC. The peak and valley cases are dual, i.e., the internal control loop forces respectively the maximum and the minimum value of the current to track the reference given by the voltage control

loop. Average control, in turn, uses the current average value in a switching cycle to track the reference supplied by the outer loop. Although most commercial ICs of CMC are based on the peak-current control principle due to its simplicity of implementation, the existence of sub-harmonic oscillations for duty cycles bigger than 50% makes necessary the use of a compensating ramp, which constitutes the main drawback of this technique.

From the seminal paper of Deisch [8] until now, more than three decades have elapsed during which a great number of researchers have contributed to building a solid representation of the dynamic behavior of the internal loop by means of either continuous or discrete-time models, or a combination of both. Dozens of papers were reported on this topic during the 1980s, the most representative being [4,9]. Some important contributions to this topic were published in the early 1990s [10–12] until the subject reached enough maturity to be treated as a chapter in some recent text books [2].

In the last decade, a renewed interest has emerged in variable frequency CMC strategies such as constant ON-time CMC [13], which, at the expense of a variable switching frequency operation, offers high efficiency under light load operation and precludes the existence of sub-harmonic oscillations in most cases. A detailed analysis of the dynamic behavior of this control technique can be found in [14], where the main difference with respect to peak CMC is investigated in the buck converter by means of an equivalent circuit consisting of the output load and the LC output filter, which is supplied by two current sources with a resistor and a capacitor in parallel.

Variable switching frequency would also result from the insertion of a hysteretic comparator instead of the Pulse Width Modulator (PWM) with constant switching frequency in the case of current programming, or instead of the PWM with constant ON-time duration in the case of constant ON-time CMC.

The voltage regulation of DC-DC switching converters using hysteretic control, also called free running or bang-bang controlled converters, goes back in time to the early years of modern power electronics when conditions for stable limit cycles in a buck switching regulator were first established [15,16].

Recently, hysteretic controllers were used in Voltage Regulator Module (VRM) applications that require current control with fast response [17–19], and some commercial chips are already available [20].

Traditionally, hysteresis-based control systems have been analyzed by means of frequency domain techniques like the descriptive function or Tsypkin's method [21–23].

On the other hand, Sliding-Mode Control (SMC) theory is a time-domain analytical technique that predicts with high precision the dynamic behavior of a Variable Structure System (VSS) [24,25]. Power converters can be classified as VSSs, and SMC is the natural way to regulate their outputs and deal with their dynamical behavior because the generation of chattering, which is intrinsic to the use of SMC, is also inherent to the nature of power converters operation. In other words, the sliding chattering becomes converter ripple, which is a physical manifestation of the way a converter absorbs energy from the input source, storing it usually in an inductor and then transferring it to an output load.

There are two main results in the SMC theory applicable to switching converters. The first one is the fact that for single input systems, a suitable Lyapunov function $V(x) = \frac{1}{2}\sigma^2(x)$ exists, where $\sigma(x)$ is the switching function. If the switching feedback gains are chosen so that $\dot{V} = \sigma\dot{\sigma} < 0$ in the domain of attraction, then the state trajectory converges to the surface $\sigma = 0$ and is restricted to it for all subsequent time. The second one provides the ideal sliding-mode dynamics on the switching surface. In this case, Filippov's method [26] and the equivalent control approach yield identical sliding equations when applied to systems that are linear with respect to the control input [27].

These techniques have been used in [28] considering feedback switching conditions of the form $\sigma = x_j - K = 0$, expressed in terms of a suitable state variable x_j that is desired to be regulated at a suitable level K. They have been employed in output voltage regulation of DC-DC switching converters in early works such as in [29–33] and also in some recent contributions to this field such as [34–38]. In [39], SMC theory has been applied to control paralleled inverters of the buck type and

in [40,41]. In [42,43], it has been used in the analysis of interleaved boost converters with hysteretic control in a ring configuration. In [44], sliding mode control theory was used to synthesize canonical elements for power processing such as in impedance matching in PV systems and in power factor correction. These techniques were also combined with other robust control methods such as fuzzy logic [45] and H_∞ [46] for designing these systems.

In the field of switching converters, two different kinds of studies using SMC theory exist in the literature. The one that uses this theory to design the switching decision and to analyze the ideal sliding dynamics and that ultimately uses a hysteretic loop to limit the switching frequency [7]. Other works use this theory to derive the equivalent control, and this is used finally to implement a PWM control [32,33]. Actually, with this strategy, all the advantages of SMC are not maintained. Small-signal analysis of sliding mode-controlled switching converters, based on hysteresis modulation, were reported in [47], where Bode plot and root locus analysis were used to reveal the effect of the parameters on the system behavior.

In this paper, on the basis of the equivalent control method, a procedure to design the control loop of DC-DC power converters operating in CMC with both variable and fixed frequency modulation strategies is proposed. The controller employs one switching function of the form $\sigma = i_r - i_L$, where i_L is a converter current and i_r is the output of an outer compensating network that processes the output voltage error. The paper comprehensively explains the dynamics of switching converters regardless of their modulation strategies. In particular, it will be demonstrated that under sliding mode conditions, the behavior of the switching converters under all the control strategies tend to the same dynamics known as the ideal sliding mode dynamics when the switching period tends to zero. The advantages, limitations and drawbacks of each strategy in a practical implementation are also discussed. It is worth noting that in this paper, it is not pretended to control switching converters using sliding mode control that ultimately end-up in a variable frequency implementation of the modulator, but the dynamics of these systems under both constant and variable frequency modulation schemes are explained by using sliding mode control theory, while providing circuit equivalent models that can be used for designing these systems by utilizing conventional frequency-domain methods.

The rest of the paper is organized as follows. The description of the behavior of current-programmed DC-DC converters is presented in Section 2 in the light of sliding mode control theory. A small-signal model is used to design the voltage loop by means of linear techniques in the frequency domain, as well as simulation results on two practical examples of switching converters in Section 3. The examples consist of a boost converter under fixed and variable frequency operation and a buck converter with current-mode hysteretic control and high bandwidth voltage regulation. An experimental validation of the results corresponding to the buck converter is given in Section 4. The application of the approach to single-loop ripple-based voltage mode control is discussed in Section 5. Finally, the conclusions of this work are summarized in Section 6.

2. Sliding-Mode Control of Switching Converters Based on Two-Loop Current Mode Control

In CCM operation, a switching converter is described by a piecewise linear state-space model that can be written in the following form:

$$\dot{x}(t) = \begin{cases} A_1 x(t) + B_1 w(t) & u = 1 \\ A_2 x(t) + B_2 w(t) & u = 0 \end{cases} \tag{1}$$

where u is a binary signal that can take the values of zero or one. It is assumed that the switching is instantaneous. $x(t)$ is the vector of state variables, and $w(t)$ is the vector of independent sources. Equation (1) can be expressed as follows:

$$\dot{x}(t) = [A_1 x(t) + B_1 w(t)]u + [A_2 x(t) + B_2 w(t)](1 - u). \tag{2}$$

Conventionally, the output variable y is a linear combination of the state variables. However, the approach is also applicable to the case with a nonlinear switching surface as in high-order boundary control schemes [48]. Hereinafter, let the linear combination of state variables $y(t) = c^\intercal x(t)$ be the output to be controlled, where c is a suitable vector to select the output $y(t)$ from the state variables $x(t)$. The derivative of the controlled output $y(t)$ is of the form:

$$\dot{y} = (m_1(x,t) + m_2(x,t))u - m_2(x,t) \tag{3}$$

where $m_1(x,t)$ and $m_2(x,t)$ are the rising and falling slopes of the signal $y(t)$ that can be expressed as follows:

$$m_1(x,t) = \quad c^\intercal[A_1 x(t) + B_1 w(t)] \tag{4}$$
$$m_2(x,t) = \quad -c^\intercal[A_2 x(t) + B_2 w(t)]. \tag{5}$$

Our interest is in situations where y can be controlled in sliding mode, so that it follows the reference smooth function $r(t)$ (continuous and differentiable). The switching function can be expressed as follows:

$$\sigma(x,t) = r(t) - y \tag{6}$$

along with the following control law (Figure 1):

$$u = \begin{cases} 1 & \text{if} \quad \sigma > 0 \\ 0 & \text{if} \quad \sigma < 0. \end{cases} \tag{7}$$

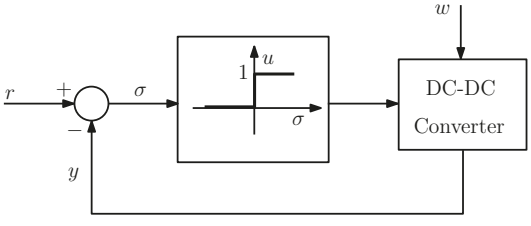

Figure 1. Simplified diagram of a DC-DC converter under Current Mode Control (CMC).

For the existence of a sliding regime on the time-variant surface Σ defined by $\{x|\sigma(x,t) = 0\}$, the sliding condition $\sigma\dot{\sigma} < 0$ must be fulfilled, which is equivalent to:

$$\dot{\sigma}_{\sigma>0} < 0 \tag{8}$$
$$\dot{\sigma}_{\sigma<0} > 0. \tag{9}$$

According to (3), the derivative $\dot{\sigma}$ of the switching function σ can be expressed as follows:

$$\dot{\sigma}(x,t) = \dot{r}(t) - ((m_1(x,t) + m_2(x,t))u - m_2(x,t)). \tag{10}$$

By using (7), the sliding conditions (8) and (9) are:

$$\dot{\sigma}_{\sigma>0} = \dot{r}(t) - m_1(x,t) < 0 \tag{11}$$
$$\dot{\sigma}_{\sigma<0} = \dot{r}(t) + m_2(x,t) > 0 \tag{12}$$

or in compact form:

$$-m_2(x,t) < \dot{r}(t) < m_1(x,t) \tag{13}$$

Equation (13) implies that the rate of change of the signal r must be lower than the absolute values of the slopes $m_1(x,t)$ and $m_2(x,t)$ of the control signal y. This is easily met if the bandwidth of the outer loop is much lower than the switching frequency, as is the case in any practical design. Therefore, under this condition, the trajectory of the system (2) with the control decision (7) will reach the sliding surface Σ in finite time and stay on it in sliding mode [27].

To maintain the trajectory in this regime, it is necessary to switch continuously at infinite frequency in the ideal case. This is not an acceptable behavior for DC-DC switching converters, which are designed to operate in a specific switching frequency range. Operating at higher frequencies, the converter efficiency decreases, and the instantaneous switching model (2) is no longer valid. This problem is solved by introducing a boundary layer around Σ and replacing the switching decision (7) by:

$$u = \begin{cases} 1 & \text{if} \quad \sigma > +\Delta \\ 0 & \text{if} \quad \sigma < -\Delta \end{cases} \tag{14}$$

where $\Delta > 0$. With this control law, the switching frequency in sliding-mode will be finite. In turn, the sliding motion will not occur strictly on the surface Σ, but in a neighborhood that meets the condition $|\sigma| \leq \Delta$. This means that a certain switching ripple will exist in the output to be controlled and other state variables as a penalty of a bounded switching frequency. This is a natural way of exchanging the energy between the reactive components of the converter.

The ideal sliding-mode dynamics is the behavior of the system (2) in the sliding regime with a control of the form (14) and in the limit case when Δ tends to zero. In order to find the ideal sliding-mode equations, the equivalent control method [27] is used. A necessary condition for the existence of an equivalent control u_{eq} and therefore to apply this method is that u appears explicitly on the right side of (10), i.e.,

$$m_1(x,t) + m_2(x,t) \neq 0. \tag{15}$$

Remark 1. *The previous condition is largely related to the fact that the relative degree of the converter u-to-σ loop is equal to one. The fast response characterizing CMC is due to this fact. The relative degree of a switched system is the number of differentiations one needs to perform on the switching function σ to make the input explicitly appear in its derivative, i.e., the minimum n that satisfies the following equation:*

$$\frac{\partial}{\partial u}\frac{\mathrm{d}^n \sigma(x,t)}{\mathrm{d}t^n} \neq 0 \tag{16}$$

Remark 2. *At high frequencies, if the relative degree is one, the system behaves as an integrator, which converts the square-wave signal u to a triangular signal σ.*

Remark 3. *It should be noted that apart from the widely-used hysteresis comparison, any other strategy to limit the switching frequency can be used without invading the sliding motion. Other possible strategies to limit the switching frequency are time delays, filtering and clocked switching.*

In all the cases, if (15) is accomplished, the equation $\dot{\sigma} = 0$ can be solved with respect to u to obtain the equivalent leading to the following expression:

$$u_{eq}(x,t) = \frac{\dot{r}(t) + m_2(x,t)}{m_1(x,t) + m_2(x,t)}. \tag{17}$$

The equivalent control caused by any modulation scheme such as the variable frequency hysteretic modulation and constant switching-frequency peak/valley control methods are the same since the equivalent control corresponds to the ideal sliding dynamics with theoretically infinite switching frequency or to the averaged dynamics of the converter under the switching constraints' imposed previous modulation strategies. The order of the averaged dynamics or the ideal sliding dynamics

is reduced due to the relationship imposed between the state variables by the switching constraint. From (17), if $m_1(x,t) + m_2(x,t) \neq 0$, the equivalent control u_{eq} will exist, and according to (13), its value will be comprised between zero and one. The ideal sliding-mode dynamics is obtained by substituting u in (2) by u_{eq} given by (17) and introducing the order reduction due to the constraint $\sigma = 0$. In DC-DC converters, the ideal sliding-mode dynamics should have an asymptotically-stable equilibrium point.

Note that u is undetermined when $|\sigma| \leq \Delta$; therefore, there is a plurality of controls compatible with (14) [49]. For example, in the hysteretic control (Figure 2a), from the moment that the condition $|\sigma| < \Delta$ is fulfilled, a switching occurs whenever $|\sigma| = \Delta$. Other examples are constant-switching-frequency controls [50], such as peak (Figure 2b) and valley (Figure 2c) current, in which time-driven switching occurs periodically, while event-driven switching occurs whenever $|\sigma| = \Delta$. DC-DC switching converters typically have a periodic behavior in steady-state with two switchings per period. In the limit as Δ tends to zero, the periodic solution tends to the equilibrium point of the ideal sliding-mode dynamics.

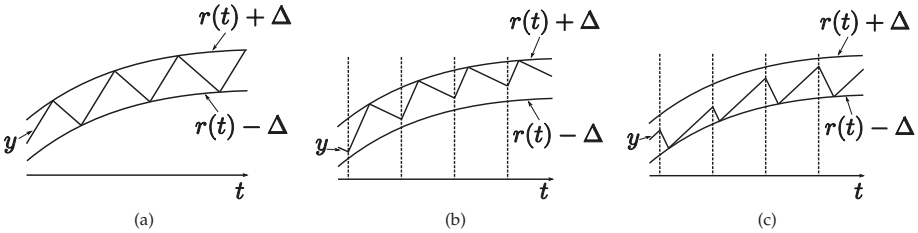

Figure 2. Evolution of the controlled output and its reference in sliding-mode for three types of control implementing (14). (**a**) Hysteresis control. (**b**) Peak control at constant switching frequency. (**c**) Valley control at constant switching frequency.

The DC-DC converter with sliding-mode current control is a system, the control input of which is the current reference $r(t)$. To regulate the output voltage of the converter, a second slower control loop that dictates $r(t)$ from the voltage error must be added. The examples considered in the next section show how to design such a controller using the ideal sliding-mode dynamics model.

3. Practical Examples

3.1. Example 1: A Boost Converter under Fixed and Variable Frequency CMC

Let us consider the boost converter depicted in Figure 3a. The state variables are the inductor current i_L and the capacitor voltage v_o. The independent sources correspond to the input voltage $v_g(t)$ and the current $i_d(t)$, which models load variations. For this example, (2) becomes as follows:

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} = \frac{v_g(t)}{L} - \frac{v_o(1-u)}{L} \tag{18}$$

$$\frac{\mathrm{d}v_o}{\mathrm{d}t} = \frac{i_L(1-u)}{C} - \frac{v_o}{RC} + \frac{i_d(t)}{C}. \tag{19}$$

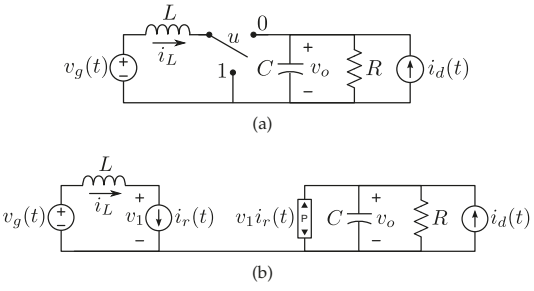

Figure 3. Schematic circuit diagram of (**a**) a Boost converter and (**b**) its ideal sliding-mode dynamics model under CMC.

Let $i_r(t)$ be the current reference. Using the switching function $\sigma = i_r(t) - i_L$ together with the control law (7), the sliding condition (13) leads to the following inequality:

$$\frac{v_g(t) - v_o}{L} < \frac{\mathrm{d}i_r(t)}{\mathrm{d}t} < \frac{v_g(t)}{L}. \tag{20}$$

When $i_r(t)$ is constant, (20) becomes $0 < v_g(t) < v_o$. In this case, starting from zero initial conditions, as soon as v_o reaches $v_g(t)$, the sliding condition is fulfilled, and after a finite time, the system trajectory is constrained in the sliding manifold defined by the constraint $i_r - i_L = 0$. When $i_r(t)$ is time varying or state-dependent, according to (17), the equivalent control for this example becomes as follows:

$$u_{eq} = \frac{L\frac{\mathrm{d}i_r(t)}{\mathrm{d}t} + v_o - v_g(t)}{v_o}. \tag{21}$$

After substituting u by u_{eq} in (18) and (19) and using $\sigma = 0$ ($i_L = i_r(t)$), the system order is reduced, and the following ideal sliding-mode dynamics is obtained:

$$i_L = i_r(t) \tag{22}$$

$$\frac{\mathrm{d}v_o}{\mathrm{d}t} = \frac{i_r(t)\left[v_g(t) - L\frac{\mathrm{d}i_r(t)}{\mathrm{d}t}\right]}{Cv_o} - \frac{v_o}{RC} + \frac{i_d(t)}{C}. \tag{23}$$

Expression (23) also establishes a power balance between the input port and the output port of the boost converter provided that $i_L = i_r$. These equations can be represented by means of an equivalent circuit using a power source [51] to model the nonlinear term (Figure 3b). The ideal sliding-mode dynamics (23), with the following constant inputs:

$$i_r(t) = I_r, \;\; v_g(t) = V_g, \;\; i_d(t) = 0, \tag{24}$$

has the following equilibrium point:

$$v_o{}^* = V_r = \sqrt{I_r R V_g} \tag{25}$$

which is asymptotically stable, as can be demonstrated by means of the Lyapunov function $V(v_o) = (1/2)(v_o - V_r)^2$ [52].

Note that $v_o{}^*$ depends on both the line voltage and the supplied load resistance. That is why a regulation of the voltage v_o is needed when disturbances in $i_d(t)$ and $v_g(t)$ take place. The regulation can be accomplished by adding another external voltage loop and making the current reference i_r be the output of this loop.

Figure 4 shows a double-loop control scheme, which is proposed for output voltage regulation. The voltage controller consists of three cascaded stages. Namely, a Proportional-Integral (PI) block to process the error, a limiter to avoid the current reference overpassing an admissible level and a low-pass filter to ensure the smoothness of $i_r(t)$. The current controller is of the type (14) with $\Delta = I_\Delta$. The transfer function of the voltage controller in the linear region has the following form:

$$G_c(s) = K_p\left(1 + \frac{\omega_I}{s}\right)\frac{1}{1 + s/\omega_h}. \tag{26}$$

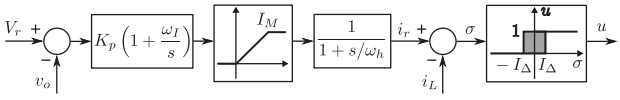

Figure 4. Control scheme with a double loop voltage regulation.

To design $G_c(s)$, a small-signal model of the ideal sliding-mode dynamics will be used. Linearizing (23) around (24) and (25) leads to the following equation for the small-signal variables represented by a "hat" ($\hat{}$) over the letter:

$$\frac{\mathrm{d}\hat{v}_o}{\mathrm{d}t} = -\frac{2}{CR}\hat{v}_o + \frac{V_g}{CV_r}\hat{i}_r(t) - \frac{LV_r}{CRV_g}\frac{\mathrm{d}\hat{i}_r(t)}{\mathrm{d}t} + \frac{V_r}{CRV_g}\hat{v}_g(t) + \frac{1}{C}\hat{i}_d(t). \tag{27}$$

Applying the Laplace transform to (27) yields the following model in terms of transfer functions:

$$\hat{V}_o(s) = G_{vir}(s)\hat{I}_r(s) + G_{vvg}(s)\hat{V}_g(s) + G_{vid}(s)\hat{I}_d(s) \tag{28}$$

where:

$$G_{vir}(s) = \frac{\hat{V}(s)}{\hat{I}_r(s)} = \frac{RV_g}{2V_r}\frac{1 - s/\omega_z}{1 + s/\omega_p} \tag{29}$$

$$G_{vvg}(s) = \frac{\hat{V}V(s)}{\hat{V}_gV(s)} = \frac{V_r}{2V_g}\frac{1}{1 + s/\omega_p} \tag{30}$$

$$G_{vid}(s) = \frac{\hat{V}V(s)}{\hat{I}_dV(s)} = \frac{R}{2}\frac{1}{1 + s/\omega_p} \tag{31}$$

$$\omega_z = \frac{RV_g{}^2}{LV_r{}^2};\ \omega_p = \frac{2}{RC}. \tag{32}$$

The loop gain is $T(s) = G_c(s)G_{vir}(s)$, and the closed-loop output impedance is given by $Z_o(s) = G_{vid}(s)/(1 + T(s))$. Besides, the closed-loop input to output transfer function is expressed as $G_{vvg}(s)/(1 + T(s))$. The coefficients of $G_c(s)$ are chosen to ensure that the frequency response of the total loop gain exhibits a high value of the modulus and a sufficient stability margin. The higher the value of $|T(j\omega)|$, the better will be the disturbance rejection, but for a poor relative stability, there can be a range of frequencies very sensitive to disturbances. In the boost converter, the right half-plane zero of $G_{vir}(s)$ (29) imposes an upper bound on the achievable bandwidth [53].

Let us consider an example of a boost converter with the following set of parameter values: $L = 30\,\mu\text{H}$, $C = 100\,\mu\text{F}$, $R = 10\,\Omega$, $V_g = 10\,\text{V}$ and $V_r = 30\,\text{V}$. Two cases of CMC will be considered, i.e., valley CMC at constant switching frequency (Figure 2c) with $I_\Delta = 2.5\,\text{A}$ and $f_s = 50\,\text{kHz}$ and hysteresis CMC (Figure 2a) with $I_\Delta = 2.22\,\text{A}$, which in the steady-state exhibits the same switching frequency of 50 kHz. In Figure 5, the frequency response from the theoretical expression of $G_{vir}(j\omega)$ is compared to the simulated corresponding frequency response of the two mentioned CMC controllers. The simulated frequency response was obtained using the power electronics simulator software

PSIM©, which has a specific feature to get different types of frequency responses, basically input, output and closed loop gains. The AC sweep module manages the frequency sweep (amplitude, initial frequency, final frequency, number of points) as in a frequency response analyzer.

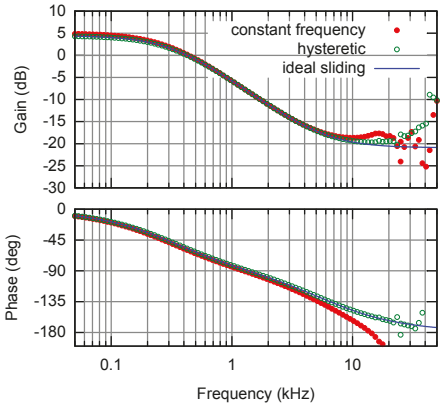

Figure 5. Theoretical and simulated frequency responses from the current reference to output voltage in a boost converter.

A good agreement among the three frequency responses can be clearly observed at low frequencies until approximately 5 kHz ($f_s/10$). The right half-plane zero is located at 6 kHz. Therefore, the control bandwidth will be placed within the region wherein the three responses almost coincide, and the design based on the ideal sliding-mode dynamics model will be valid for the other two cases.

It can be verified in a Bode diagram of $T(j\omega)$ that choosing $\omega_h = \omega_z = 37\,\text{krad/s}$, $\omega_I = 1.2\,\text{krad/s}$ and $K_p = 3.7\,\text{A/V}$, the crossover frequency at 0 dB is $f_c = 2\,\text{kHz}$, the phase margin is 57° and the gain margin is 10 dB at 6 kHz. The Bode diagrams obtained by simulation for the two cases with finite switching frequency show similar results to the ideal case, not only in the loop gain (Figure 6), but also in the output impedance (Figure 7). The closed-loop converter response to a step change in $i_d(t)$ is shown in Figure 8, where the simulated ideal sliding-mode dynamics based on the circuit of Figure 3b is compared to the two previous cases of finite switching frequency. The concordance of the three responses is in agreement with the frequency results depicted in Figure 7.

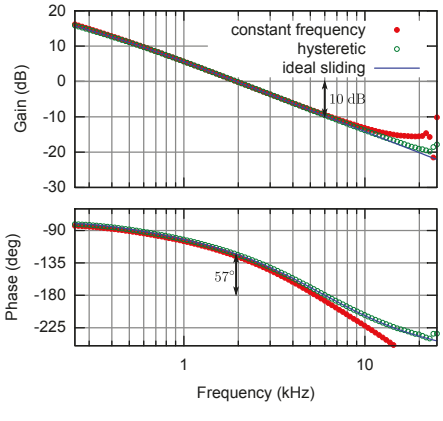

Figure 6. Theoretical and simulated loop gain Bode plots in a boost converter.

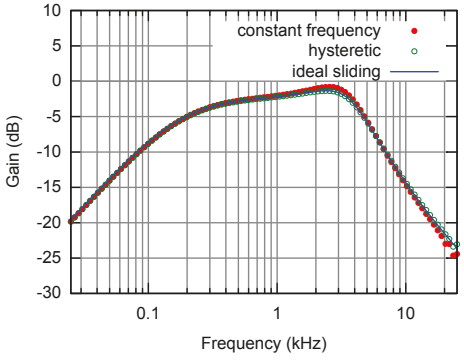

Figure 7. Theoretical and simulated closed-loop output impedance in a boost converter.

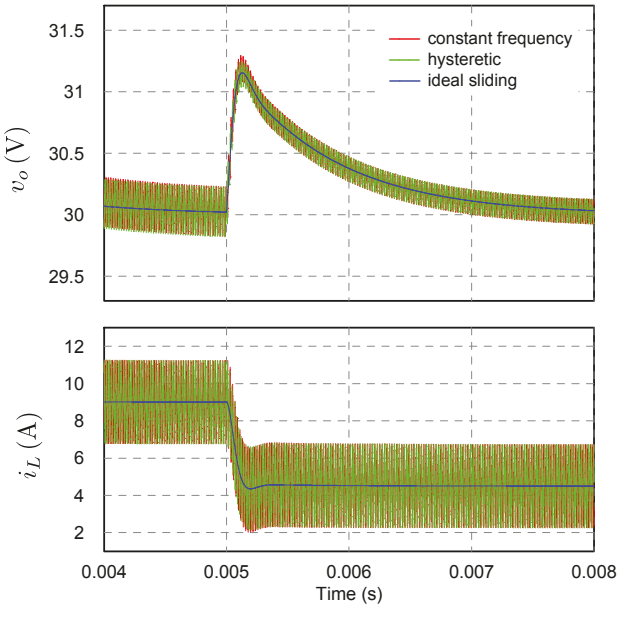

Figure 8. Response of the state variables v_o and i_L of the boost converter in closed-loop to a step change of 1.5 A in $i_d(t)$. Comparison of the ideal sliding-mode dynamics with that corresponding to two different types of control methods at finite switching frequency.

Let us analyze now the time-domain closed-loop converter response from zero initial conditions and without the presence of any disturbance. Figure 9 depicts the case of valley CMC at constant switching frequency. The case of hysteresis control is very similar. It is worth mentioning that the inductor current must be limited in the transient-state. The current control ensures that the inequality $|i_r(t) - i_L| \leq I_\Delta$ is satisfied in sliding mode. The limiter of the voltage controller guarantees that $i_r(t) < I_M$, so that, in the sliding regime, the inductor current satisfies at any instant the inequality $i_L < I_{max}$ where $I_{max} = I_M + I_\Delta$. In this example, the inductor current must reach at least the value ${V_r}^2/(RV_g) = 9$ A, which corresponds to the equilibrium point. The maximum current was fixed to $I_{max} = 15$ A, so that $I_M = 12.78$ A in the case of hysteresis CMC and $I_M = 12.5$ A in the case of valley

CMC. In both cases, the same regions in the response can be observed. Initially $v_o = 0$ V, so that the sliding condition (20) is not accomplished, and the trajectory goes away from the switching manifold defined by $\sigma = 0$ while i_L is increasing. Since the voltage error is positive, $i_r(t)$ also increases until its saturation. This ensures that in some instant, the inequality $i_L > i_r(t) + I_\Delta$ will be satisfied so that $u = 0$ and v_o will be also increasing. When v_o overpasses V_g, the sliding condition is fulfilled, the trajectory alters course and later enters in sliding mode as predicted by the theory. In this regime and with $i_r(t)$ saturated, v_o tends asymptotically towards an equilibrium point in which $v_o{}^* > V_r$. Once v_o surpasses V_r, the voltage controller enters in the linear region, and the trajectory tends towards the desired equilibrium point. An anti-windup system in the integrator can improve this start-up transient by reducing the voltage overshooting, although in this example, it has not been included. Moreover, the converter structure can be modified to avoid the initial current peak [7].

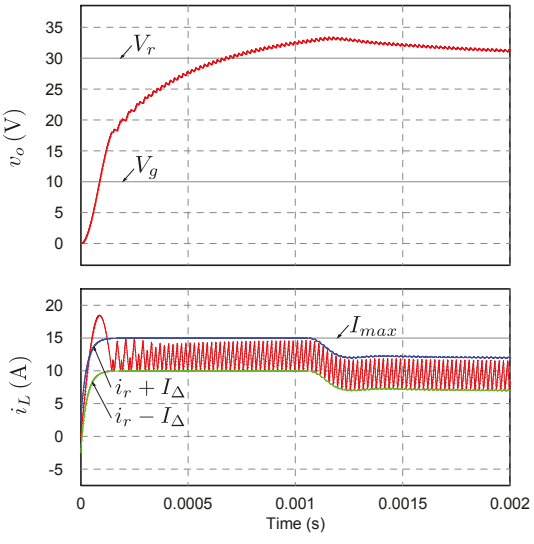

Figure 9. Boost converter response from zero initial conditions using a valley current control at constant switching frequency and voltage regulation.

3.2. Example 2: Buck Converter under Fixed and Variable Frequency CMC

Let us consider the buck converter depicted in Figure 10a, the state equations of which are:

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} = \frac{v_g(t)u - v_o}{L} \tag{33}$$

$$\frac{\mathrm{d}v_o}{\mathrm{d}t} = \frac{i_L}{C} - \frac{v_o}{RC} + \frac{i_d(t)}{C} \tag{34}$$

$$i_g = i_L u \tag{35}$$

$$i_o = \frac{v_o}{R} - i_d(t). \tag{36}$$

Using the switching function $\sigma = i_r(t) - i_L$ and the control law (7), the sliding condition (13) for this converter becomes:

$$-\frac{v_o}{L} < \frac{\mathrm{d}i_r(t)}{\mathrm{d}t} < \frac{v_g(t) - v_o}{L}. \tag{37}$$

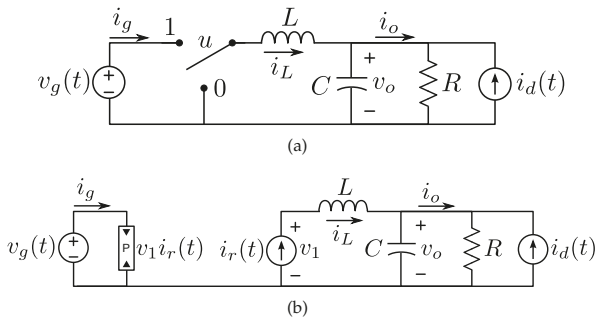

Figure 10. Schematic circuit diagram of (**a**) a Buck converter and (**b**) its ideal sliding-mode dynamics model under CMC.

Inequalities (37) are fulfilled for $i_r(t)$ constant provided that $0 < v_o < v_g(t)$, which are the normal operating conditions of a buck converter. For this converter, the sliding motion is guaranteed from the start-up even with zero initial conditions. The ideal sliding-mode dynamics, obtained by means of the equivalent control method, is the following:

$$i_L = i_r(t) \tag{38}$$

$$\frac{\mathrm{d}v_o}{\mathrm{d}t} = \frac{i_r(t)}{C} - \frac{v_o}{RC} + \frac{i_d(t)}{C} \tag{39}$$

$$i_g = \frac{i_r(t)\left[v_o + L\frac{\mathrm{d}i_r(t)}{\mathrm{d}t}\right]}{v_g(t)} \tag{40}$$

$$i_o = \frac{v_o}{R} - i_d(t) \tag{41}$$

and it can be represented by the circuit illustrated in Figure 10b. The equilibrium point for constant inputs (24), ${v_o}^* = V_r = I_r R$ is asymptotically stable. Linearizing the ideal sliding-mode dynamics around the equilibrium point yields a small-signal model, which is used to design the voltage controller or to analyze the system stability when an input filter is added.

The voltage loop consists of the current reference $\hat{I}_r(s)$ to the output voltage $\hat{V}_o(s)$ transfer function, $G_{vir}(s)$, i.e.,

$$G_{vir}(s) = \frac{R}{1 + sRC}, \tag{42}$$

and the same controller (26) employed in the previous example. In this converter, $G_{vir}(s)$ is a minimum phase transfer function. In the ideal case, the loop gain and the control bandwidth can be made boundlessly high without affecting the system stability. For instance, if a particular value of ω_c is chosen and the coefficients of $G_c(s)$ are calculated according to the following criteria:

$$\omega_c \gg 1/(RC); \;\; K_p = C\omega_c; \;\; \omega_I = \omega_c/4; \;\; \omega_h = 4\omega_c, \tag{43}$$

then ω_c will be the crossover frequency at 0 dB of the loop gain, the phase margin will be higher than 60° and the gain margin will be infinite.

However, the sliding condition (37) is a constraint that must be respected. For example, let us assume that the system is in equilibrium and that a step disturbance of amplitude I_d in current $i_d(t)$ is applied at $t = 0$. If the controller has been designed according to (43), the slope of $i_r(t)$ during the transient-state will be maximal at $t = 0.55/\omega_c$ approximately, reaching a value of:

$$\left.\frac{\mathrm{d}i_r(t)}{\mathrm{d}t}\right|_{t=0.55/\omega_c} \approx -0.8\,\omega_c I_d \tag{44}$$

and therefore, the conditions to keep the sliding mode with this disturbance are:

$$-V_r < -0.8\,\omega_c I_d L < V_g - V_r. \tag{45}$$

Hence, if the bandwidth is too large, small disturbances could provoke very fast variations of $i_r(t)$, violating (37). Moreover, in the case of finite switching frequency, the distortion of the frequency response near the switching frequency degrades the phase margin and limits in turn the control bandwidth. As was observed in Figure 5, the phase decrease is higher in the case of constant switching frequency than in the case of hysteresis, and therefore, a larger bandwidth can be achieved by means of the hysteretic control.

4. Experimental Results

A prototype of the buck converter with hysteretic CMC has been constructed for the set of parameter values $L = 3.3\,\mu\text{H}$, $C = 350\,\mu\text{F}$, $R = 1\,\Omega$, $V_g = 15\,\text{V}$ and $V_r = 5\,\text{V}$. The switching frequency has been tuned to 100 kHz in the equilibrium point. The gain of the current sensor was $R_s = 44\,\text{mV/A}$, and the coefficients of the voltage controller have been calculated according to (43) with $\omega_c = 2\pi \cdot 40\,\text{krad/s}$. A picture of the the experimental setup is shown in Figure 11, and the schematic diagram is depicted in Figure 12. While in the numerical simulations, we used the scheme depicted in Figure 4 in which the saturation block is inserted between the PI compensator and the low-pass filter, our experimental measurements were obtained from a system under the control scheme of Figure 12 in which the saturation block acted after the low-pass filter. From an implementation point of view, it is much simpler to use Figure 12 rather than Figure 4. It is clear that if no saturation takes place, both schemes are equivalent, and this is the case of all the small signal responses (time and frequency domains) presented in the paper. A small difference may arise however under large signal responses such as for instance during the transient. Moreover, it is worth noting that this saturation block was added to limit the current reference during start-up, and this can be accomplished by the scheme of Figure 4, as well as by the one shown at the bottom of Figure 12.

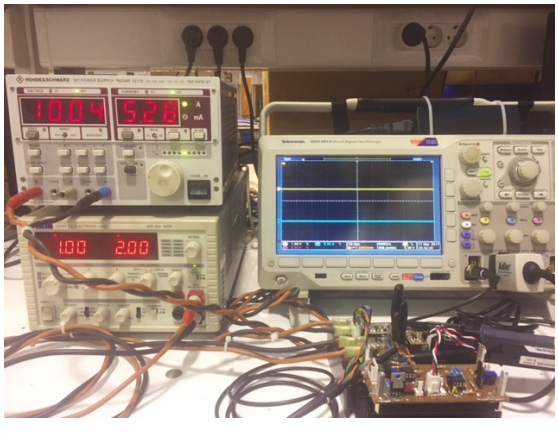

Figure 11. The experimental setup used to validate the theoretical and the simulation results corresponding to the buck converter under two-loop hysteretic CMC.

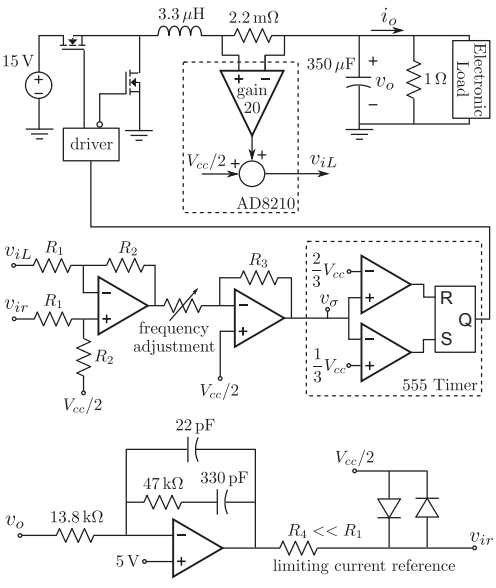

Figure 12. Schematic circuit diagram of the buck converter with hysteretic CMC and output voltage regulation.

The frequency response of the system being the input $\hat{v}_{ir}$ and the output $\hat{v}_o$, in the case of an open voltage loop, has been obtained experimentally, and it is depicted in Figure 13 with the Bode diagram of $G_{vir}(s)/R_s$. The experimental frequency response in Figure 13 was obtained by using the Venable 3120 FRA. In this particular case, the analog control circuit is the one in Figure 12; with the voltage loop opened, the FRA provides the voltage reference v_{ir}, which is composed of a sinusoidal variable frequency reference and a DC component to polarize the system around the desired steady-state operating point. Closed loop gains in Figure 14 were obtained in closed loop using also the Venable 3120 FRA; in this case, a wideband medium frequency injection transformer model Bode Box 200-002 and two probes to obtain differential measurements are connected to the R4-100 Ω resistor.

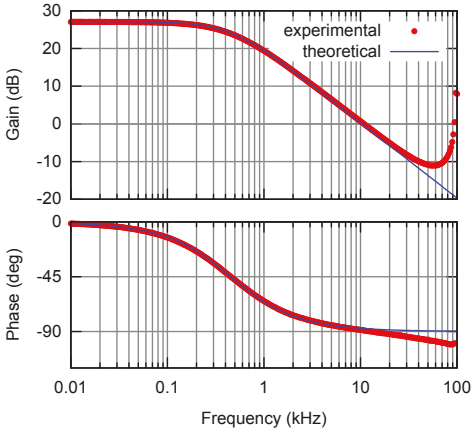

Figure 13. Theoretical and experimental frequency responses from current reference $\hat{v}_{ir}$ to output voltage $\hat{v}_o$ in the buck converter of Figure 12.

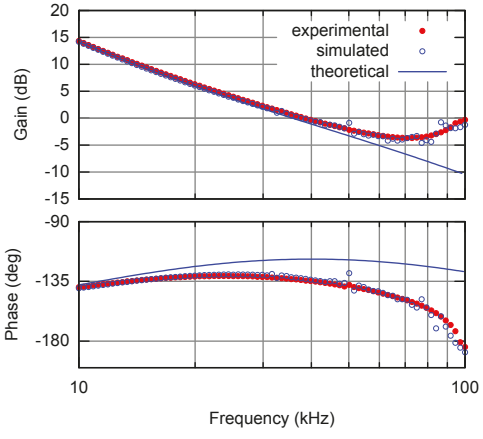

Figure 14. Theoretical, simulated and experimental Bode diagrams of the voltage loop gain in the buck converter.

It can be observed that the model based on the ideal sliding-mode dynamics is valid up to almost one half of the switching frequency. The loop gain has been also measured, and it is shown in Figure 14 with the Bode diagram of $G_c(s)G_{vir}(s)/R_s$ and with the frequency response obtained by numerical simulation of the switched model. It can be observed that the experimental closed-loop bandwidth (ω_c) hardly deviated from the theoretical one, but the phase margin was reduced from 60°–45° due to non-ideal high frequency effects. To match the simulation with the experimental results at high frequency, it was necessary to include in the simulation a dynamic model of the current sensor (a low-pass second-order filter with a cutoff frequency of 450 kHz and a damping ratio of 0.7) and pure delays for both control logic circuits and switching elements (300 ns in total). Figures 15 and 16 show respectively the experimental and simulated response of the converter to a load variation of step type that satisfies the condition (45) by including these non-ideal effects. Note that signal v_σ representing the switching function is not totally within the hysteresis band due to propagation delays and to the dynamics of the current sensor.

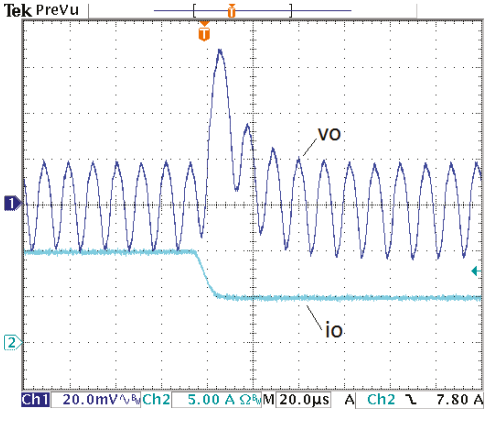

Figure 15. Experimental output voltage response to a load current step in the buck converter from 10 A–5 A.

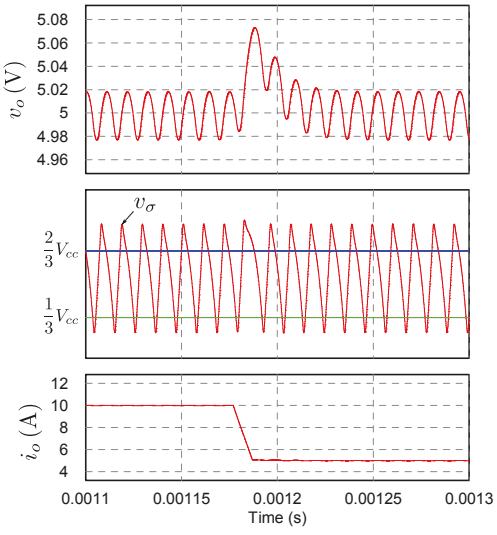

Figure 16. Simulated response to a load current step in the buck converter from 10 A–5 A corresponding to Figure 15.

Remark 4. *The analysis of the same converter with fixed frequency V^2 control and enhanced V^2I_L control [54–56], the V^2I_C [57] and the V^1 control concept [58] can be done following the same procedures with a little effort.*

5. Discussion: Extension to Single-Loop Ripple-Based VMC Strategies

Although the CMC of power converters is nowadays an extensive design practice due to its intrinsic advantages and the existence of an important number of dedicated commercial chips that facilitate its implementation, different ripple-based VMC schemes, that use the parasitic output voltage ripple instead of the inductor current as an additional feedback signal have been also proposed to improve the load transient response of switching converters. For instance, conventional hysteretic voltage mode controllers use the output voltage ripple as the control signal, and a hysteretic comparator is used to generate the square wave for the switch drivers. This is the case of hysteretic voltage regulator modules [59], the V^2 and the enhanced V^2I_L control strategies [54–56] and also the case of the V^2I_C [57] and its equivalent scheme known as the V^1 control concept [58]. Except the V^2I_L control scheme, in all these control strategies, the inductor current is used indirectly in the feedback, and the system works as desired only with a non-ideal output capacitor characterized by a high Equivalent Series Resistance (ESR). Although it is conventionally claimed that hysteretic controllers show faster response than traditional fixed frequency PWM controllers, this happens only with relatively large ESR, and similar responses can be obtained with both modulations if a similar ESR is used. In fact, this ESR introduces indirectly inductor current feedback, and this is the main reason for making the response faster. The enhanced V^2I_L ripple-based control [56] and the I^2 control [60] directly introduce this current feedback. Other approaches for introducing current feedback indirectly in the controller are the so-called raster control surfaces in [61], the use of the capacitor current as in [62] and the introduction of the derivative term of the error signal as in [63].

Although the interest for hysteretic controllers seems a recent practice, due to its immediate application in Voltage Regulation Modules (VRMs) [17,19] and the existence of some commercial chips [20], its use in the voltage regulation of DC-DC switching converters goes back in time to the early years of modern power electronics when conditions for stable limit cycles in a buck switching

regulator were first established [15,16]. Other control schemes that can be placed into the same category are boundary control [48,64] and synergetic control [65] strategies.

All the previous strategies can be implemented either with the variable frequency modulation strategy or a fixed frequency modulation scheme. Variable frequency would result from the use of a hysteretic comparator. It would be also the case for constant ON-time and constant OFF-time strategies. Fixed frequency operation will result from peak CMC (or VMC), valley CMC (or VMC) and average CMC (or VMC) using a latch and a clock signal in the modulator. The same theory can be applied interchangeably to all the previous strategies.

6. Conclusions

A two-loop control design technique for DC-DC switching converters has been presented. The double loop consists of an inner current loop in sliding-mode and an outer voltage regulation loop that includes a limiter of the current reference.

When the sliding condition is accomplished, the converter enters in sliding mode after a finite time, and the current tracks its reference. The ideal sliding-mode dynamics describes the system behavior, and a small-signal model around the equilibrium point is used to design the voltage regulation loop by means of the frequency response method.

It has to be pointed out that sliding-mode control theory does not specify the nature of the switching law when $|\sigma| < \Delta$. Hence, hysteresis control and constant switching frequency control have been compared for a boost converter. The frequency response in both cases almost coincides with the theoretical prediction of the ideal sliding-mode dynamics at low frequencies, the hysteresis control response being much more similar to the ideal case near the switching frequency region. However, in the example reported here for the boost converter, the most limiting factor in the regulation bandwidth is the right half-plane zero, and for that reason, the closed-loop response in both cases is very similar to the ideal one.

In the example of the buck converter, an expression of the sliding condition in terms of both voltage regulation bandwidth and load disturbance amplitude has been derived. A bandwidth of the voltage loop near one half the switching frequency has been obtained using a hysteretic current mode controller. In the same example, it has been found that the actual dynamic behavior of the current sensor and the delay of both switching and control logic circuits can have an appreciable influence upon the phase margin of the voltage loop.

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Suppression Research Regarding Low-Frequency Oscillation in the Vehicle-Grid Coupling System Using Model-Based Predictive Current Control

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Abstract: Recently, low-frequency oscillation (LFO) has occurred many times in high-speed railways and has led to traction blockades. Some of the literature has found that the stability of the vehicle-grid coupling system could be improved by optimizing the control strategy of the traction line-side converter (LSC) to some extent. In this paper, a model-based predictive current control (MBPCC) approach based on continuous control set in the *dq* reference frame for the traction LSC for electric multiple units (EMUs) is proposed. First, the mathematical predictive model of one traction LSC is deduced by discretizing the state equation on the alternating current (AC) side. Then, the optimal control variables are calculated by solving the performance function, which involves the difference between the predicted and reference value of the current, as well as the variations of the control voltage. Finally, combined with bipolar sinusoidal pulse width modulation (SPWM), the whole control algorithm based on MBPCC is formed. The simulation models of EMUs' dual traction LSCs are built in MATLAB/SIMULINK to verify the superior dynamic and static performance, by comparing them with traditional transient direct current control (TDCC). A whole dSPACE semi-physical platform is established to demonstrate the feasibility and effectiveness of MBPCC in real applications. In addition, the simulations of multi-EMUs accessed in the vehicle-grid coupling system are carried out to verify the suppressing effect on LFO. Finally, to find the impact of external parameters (the equivalent leakage inductance of vehicle transformer, the distance to the power supply, and load resistance) on MBPCC's performance, the sensitivity analysis of these parameters is performed. Results indicate that these three parameters have a tiny impact on the proposed method but a significant influence on the performance of TDCC. Both oscillation pattern and oscillation peak under TDCC can be easily influenced when these parameters change.

Keywords: vehicle-grid coupling system; low frequency oscillation; traction line-side converter (LSC); model-based predictive current control (MBPCC); dSPACE semi-physical verification

1. Introduction

With the rapid development of high-speed railway, alternating current (AC)–direct current (DC)–AC drive electric multiple units (EMUs) and electric locomotives are increasingly put into operation. Meanwhile, low-frequency oscillation (LFO) accidents have happened in many countries, such as Norway, Germany, Switzerland, the United States, and France [1–4]. Since 2008, the phenomenon has frequently occurred in China's high-speed railway depots. The LFO in railway is characterized by the amplitude fluctuation of grid-side voltage, current, and DC-side voltage, and happens when the multiple vehicles are concentrated in one power supply district and get power from a traction network [5]. With the larger voltage oscillation peak of the traction network,

the protection logic operation of the line-side converter (LSC) would be triggered and result in the traction blockade, transformer breakdown, even an arrestor explosion [5,6].

Some testing, modeling, and simulation studies have been conducted to explore the mechanism of LFO. In [7], the phenomenon of LFO reappeared, and the stability of the traction LSC was analyzed by the adjustment of proportional integral (PI) controller parameters. Authors in [8] investigated the LFO and proposed an advanced multivariable control concept to avoid occurring stability problems. Based on the eigenvalues analysis, a detailed modeling plan was presented to investigate the mechanism of LFO [9]. A forbidden region-based criterion was performed to analyze of the critical condition of LFO [10]. In [11], a small-signal frequency domain model of LSC in a *dq* reference frame was established, and the impact of controller parameters on the stability of the vehicle-grid coupling system was discussed. According to these studies, the vehicle-grid coupling system can be defined as a dynamic stability problem of a large-scale multi-converter system under specific conditions. Many scholars working with renewable energy plants are dedicated to improving the modeling process of large systems to improve their stability and work efficiency, which can provide a good reference for high-speed railway [12–16]. The oscillation damping methods in railways could be categorized into two types [17]. One is the improvement of the traction network—for example, reducing the equivalent impedance of the traction network or adding power oscillation damping link. The other is modification of the vehicle and control, including decreasing of the number of vehicles, adjusting of the control parameters, and optimizing the control strategy.

Transient direct current control (TDCC) is a traditional control strategy in the traction LSC of China Railway high-speed 3 (CRH3) EMUs, which is a linear combination of error proportion and integral. Its integral feedback can inhibit the constant disturbance, while makes the closed-loop system unresponsive, and prone to oscillation and controlling quantity saturation. Though the integral link can reduce the static errors to a large extent, a tracking static error between the reference value and the actual value is inevitable in TDCC. This will adversely affect the control performance, such as the distortion of input electric parameters. In particular, when the number of EMUs accessed in traction network increases, the distortion will be exacerbated, and may directly lead to LFO.

The most common predictive control methods are generally divided into some types, namely deadbeat control, hysteresis-based control, trajectory-based control, continuous-control-set model predictive control (MPC), and finite-control-set MPC [18]. MPC was originally employed in a process industry that could easily handle multivariable cases, system constraints, and nonlinearities [19], and some studies have verified its good performance by applying it in the power electronics converters in renewable energy systems [20], cascaded H-Bridge Inverters [21], and so on. At present, MPC is regarded as one of the most promising control strategies, is starting to be applied to converters. In combination with predictive selection of a voltage-vector's sequence, predictive direct power control (PDPC) of three-phase converters was proposed, and the effective voltage vector sequence was selected for next sampling period [22]. Based on a finite set of controls, the model PDPC was also proposed, in order to directly control the active and reactive power by forecasting possible future behaviors [23–26]. In [27], the generalized predictive control of three-phase rectifiers developed in the *dq* frame is introduced.

So far, to solve the LFO in a high-speed railway system, the way of adopting the MPC strategy, based on continuous control set in the traction single-phase LSC, has not yet been tried. In addition, the control performance analysis of the proposed method in a vehicle-grid coupling system is also lacking at present. In this paper, which aims to optimize the control performance in EMUs' traction LSCs and handle the LFO in vehicle-grid coupling system, a model-based predictive current control (MBPCC) strategy based on a continuous control set is presented for EMUs' traction LSC control. Simulation results in MATLAB (R2016b, The MathWorks Incorporated, Natick, MA, USA) and experimental data in the dSPACE semi-physical platform demonstrate the effectiveness and superiority of the proposed method. Furthermore, the suppression effect on the LFO is proved in the simulation when multi-vehicles are accessed in the reduced-order model of the traction network.

The paper is organized as follows. In Section 2, the mathematical model of MBPCC based on the topology structure of one traction LSC of the CRH3 EMUs is deduced. In Section 3, the simulation model of EMUs' dual traction LSCs is built, and a comprehensive simulation verification compared with TDCC is performed in order to verify the superiority of the proposed control strategy from several aspects. In Section 4, a whole dSPACE semi-physical platform is established to certify the control strategy's feasibility in real applications. In Section 5, based on a reduced-order model of the traction network, the simulation model of seven vehicles accessed in the traction network is constructed to verify the suppression effect of LFO, and the sensibility analysis of parameters under the condition of seven EMUs accessed in the traction network is discussed, in order to further explore the impact on LFO occurrence and the performance of traction LSCs when system parameters change. The study idea is shown in Figure 1.

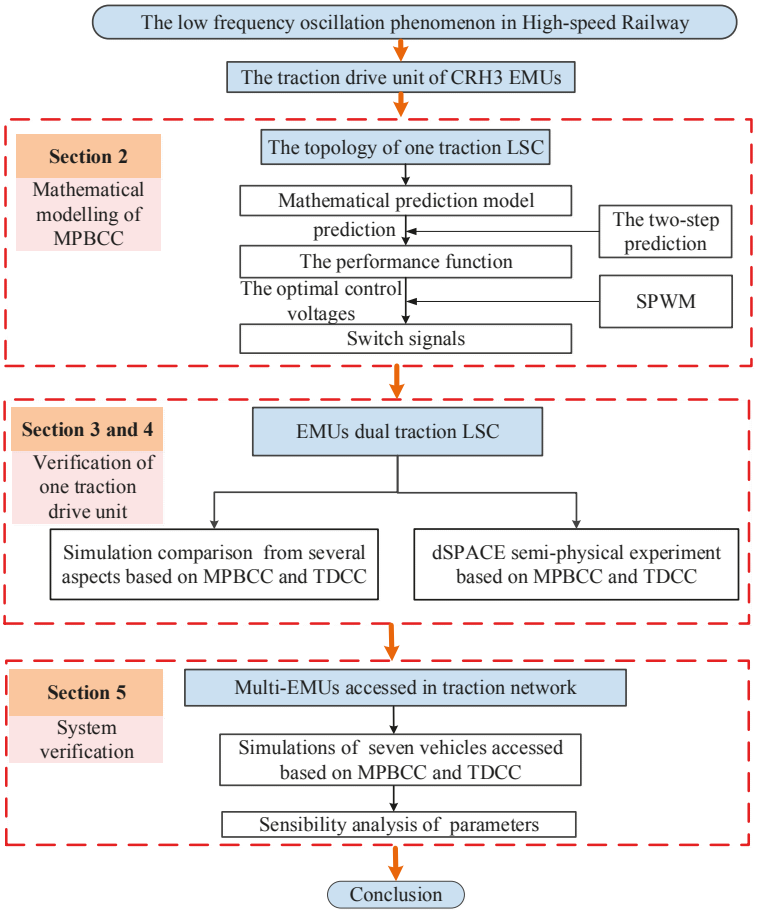

Figure 1. The study idea of the article.

2. Model Predictive Control of One Traction Line-Side Converter of China Railway High-Speed 3 Electric Multiple Units

2.1. Mathematical Model of One Traction Line-Side Converter

The vehicle-grid coupling system of high-speed railway is composed of the traction network and the EMUs traction drive system, as shown in Figure 2. In this paper, a CRH3 EMU is set as the study object; thus, the topology of the traction drive unit of EMUs is a single-phase two-level structure. When the LFO happens, the EMUs just start up and only supply power for the auxiliary facility by DC-side voltage. Therefore, the inverter and motor can be regarded as a pure resistance, and only part of the rectifier is involved in the equivalent circuit of one traction LSC.

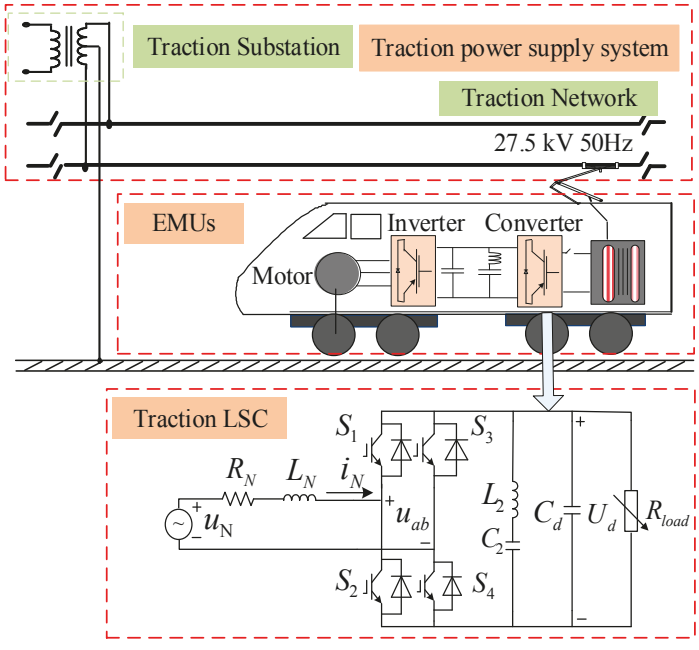

Figure 2. Vehicle-grid coupling system.

In the equivalent circuit of EMUs' traction LSC, L_N and R_N denote the leakage inductance and leakage resistance of the secondary winding of the vehicle transformer in EMUs, respectively. Four IGBTs (S_1, S_2, S_3, and S_4) are used to construct the two-level topology, C_d is the DC-side capacitor, inductance L_2 and capacitor C_2 compose the second-order filter circuit, and the inverter and motor are replaced by a pure resistive load R_{load}.

According to the Kirchhoff voltage law, the relationship between the voltage and current in the AC-side is listed below:

$$u_{ab} = u_N - R_N i_N - L_N \frac{di_N}{dt} \tag{1}$$

where u_N, i_N, and u_{ab} represent the line voltage, line current, and input voltage of the converter, respectively. If the harmonics are neglected, u_N, i_N, and u_{ab} in the dq reference frame are defined as follows:

$$\begin{cases} u_N = u_{Nd}\sin(\omega t) + u_{Nq}\cos(\omega t) \\ i_N = i_{Nd}\sin(\omega t) + i_{Nq}\cos(\omega t) \\ u_{ab} = u_{abd}\sin(\omega t) + u_{abq}\cos(\omega t) \end{cases} \tag{2}$$

where u_{Nd}, i_{Nd}, and u_{abd} are the d-axis components of u_N, i_N and u_{ab}. u_{Nq}, i_{Nq}, and u_{abq} are the q-axis components of u_N, i_N, and u_{ab}, respectively.

Substituting Equation (2) into Equation (1), the mathematical model of one traction LSC can be described as:

$$\begin{cases} u_{abd} = u_{Nd} - R_N i_{Nd} - L_N \frac{di_{Nd}}{dt} + \omega L_N i_{Nq} \\ u_{abq} = u_{Nq} - R_N i_{Nq} - L_N \frac{di_{Nq}}{dt} - \omega L_N i_{Nd} \end{cases} \tag{3}$$

2.2. Model Predictive Control of One Traction Line-Side Converter

2.2.1. Predictive Model of One Traction Line-Side Converter

Applying the first-order discrete approximation to the mathematical model expressed in Equation (3), a discrete dynamic model of one traction LSC in the dq reference frame is depicted by Equation (4):

$$\begin{cases} u_{abd}(k) = u_{Nd}(k) - R_N i_{Nd}(k) - \frac{L_N}{T_s}(i_{Nd}(k+1) - i_{Nd}(k)) + \omega L_N i_{Nq}(k) \\ u_{abq}(k) = u_{Nq}(k) - R_N i_{Nq}(k) - \frac{L_N}{T_s}(i_{Nq}(k+1) - i_{Nq}(k)) - \omega L_N i_{Nd}(k) \end{cases} \tag{4}$$

where T_s is the sampling interval. $i_{Nd}(k)$ and $i_{Nq}(k)$ are the discrete values of i_{Nd} and i_{Nq}, respectively; $i_{Nd}(k+1)$ and $i_{Nq}(k+1)$ are the one-step predictive discrete values of i_{Nd} and i_{Nq}, respectively; and $u_{abd}(k)$ and $u_{abq}(k)$ are the discrete values of the control voltages at the k-th sampling instant.

Thus, $i_{Nd}(k+1)$ and $i_{Nq}(k+1)$ can be predicted at the k-th sampling instant:

$$\begin{cases} i_{Nd}(k+1) = (1 - \frac{T_s R_N}{L_N}) i_{Nd}(k) + T_s \omega i_{Nq}(k) - \frac{T_s}{L_N} u_{abd}(k) + \frac{T_s}{L_N} u_{Nd}(k) \\ i_{Nq}(k+1) = (1 - \frac{T_s R_N}{L_N}) i_{Nq}(k) - T_s \omega i_{Nd}(k) - \frac{T_s}{L_N} u_{abq}(k) + \frac{T_s}{L_N} u_{Nq}(k) \end{cases} \tag{5}$$

The relationship between $u_{ab}(k)$ and $u_{ab}(k-1)$ is satisfied in the following way:

$$\begin{cases} u_{abd}(k) = u_{abd}(k-1) + \Delta u_{abd}(k) \\ u_{abq}(k) = u_{abq}(k-1) + \Delta u_{abq}(k) \end{cases} \tag{6}$$

where $\Delta u_{abd}(k)$ represents the variation between $u_{abd}(k)$ and $u_{abd}(k-1)$, and $\Delta u_{abq}(k)$ represents the variation between $u_{abq}(k)$ and $u_{abq}(k-1)$.

Substituting Equation (6) into Equation (5), then:

$$\begin{cases} i_{Nd}(k+1) = (1 - \frac{T_s R_N}{L_N}) i_{Nd}(k) + T_s \omega i_{Nq}(k) - \frac{T_s}{L_N} u_{abd}(k-1) + \frac{T_s}{L_N} u_{Nd}(k) - \frac{T_s}{L_N} \Delta u_{abd}(k) \\ i_{Nq}(k+1) = (1 - \frac{T_s R_N}{L_N}) i_{Nq}(k) - T_s \omega i_{Nd}(k) - \frac{T_s}{L_N} u_{abq}(k-1) + \frac{T_s}{L_N} u_{Nq}(k) - \frac{T_s}{L_N} \Delta u_{abq}(k) \end{cases} \tag{7}$$

Equation (7) is the prediction model. It should be noted that prediction line current values are decided by present currents, voltages, and the LSC's system parameters.

2.2.2. The Two-Step Prediction

In the digital control system, both the computation time delay and sampling time delay surely exist [28]. Because of the restriction of the hardware and the digital control algorithm, the control voltages calculated by the sampling and predictive currents have to be adopted at the (k + 1)-th sampling instant. Therefore, there is one sampling period delay (T_d) between the calculated control voltage by the controller and the real adopted control voltage, as shown in Figure 3. To eliminate the error caused by T_d, a two-step current prediction is adopted.

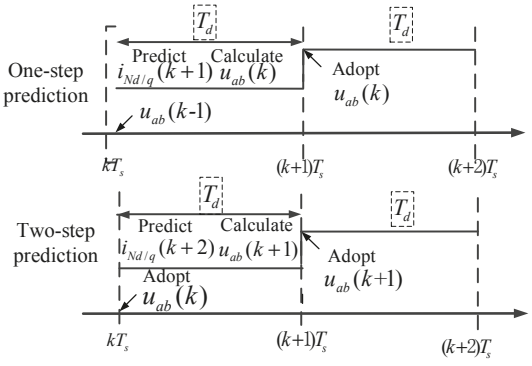

Figure 3. Control voltage in two switching periods.

When two-step prediction is adopted, $i_{Nd}(k+1)$ and $i_{Nq}(k+1)$ are first predicted at the k-th sampling instant according to Equation (8), and then $i_{Nd}(k+2)$ and $i_{Nq}(k+2)$ are predicted according to Equation (9). Thus, the control voltage $u_{abd}(k+1)$ and $u_{abq}(k+1)$ can be calculated at the k-th sampling instant, and then adopted to the rectifier at the k+1-th sampling instant. The delay error is compensated by two-step prediction.

It is worth noting that $i_{Nd}(k+1)$ and $i_{Nq}(k+1)$ are also predicted through two-step prediction at the $(k-1)$-th sampling instant. Thus, $i_{Nd}(k+1)$ and $i_{Nq}(k+1)$, which are predicted at the k-th sampling instant, are considered equal to the predicted values at the $k-1$-th sampling instant. Thus, the control voltage variations $\Delta u_{abd}(k)$ and $\Delta u_{abq}(k)$, which exist in the Equation (7), can be set to zero. The prediction Equation (7) can be rewritten as Equation (8). While $i_{Nd}(k+2)$ and $i_{Nq}(k+2)$ are not predicted before the k-th sampling instant, it cannot be affirmed that the prediction current values are equal to the k-th actual current values. The control voltages $\Delta u_{abd}(k+1)$ and $\Delta u_{abq}(k+1)$ that determine $i_{Nd}(k+2)$ and $i_{Nq}(k+2)$, respectively, cannot be omitted in Equation (9):

$$\begin{cases} i_{Nd}(k+1) = (1-\frac{T_sR_N}{L_N})i_{Nd}(k) + T_s\omega i_{Nq}(k) - \frac{T_s}{L_N}u_{abd}(k-1) + \frac{T_s}{L_N}u_{Nd}(k) \\ i_{Nq}(k+1) = (1-\frac{T_sR_N}{L_N})i_{Nq}(k) - T_s\omega i_{Nd}(k) - \frac{T_s}{L_N}u_{abq}(k-1) + \frac{T_s}{L_N}u_{Nq}(k) \end{cases} \quad (8)$$

$$\begin{cases} i_{Nd}(k+2) = (1-\frac{T_sR_N}{L_N})i_{Nd}(k+1) + T_s\omega i_{Nq}(k+1) - \frac{T_s}{L_N}u_{abd}(k) + \frac{T_s}{L_N}u_{Nd}(k+1) - \frac{T_s}{L_N}\Delta u_{abd}(k+1) \\ i_{Nq}(k+2) = (1-\frac{T_sR_N}{L_N})i_{Nq}(k+1) - T_s\omega i_{Nd}(k+1) - \frac{T_s}{L_N}u_{abq}(k) + \frac{T_s}{L_N}u_{Nq}(k+1) - \frac{T_s}{L_N}\Delta u_{abq}(k+1) \end{cases} \quad (9)$$

2.2.3. The Design of Performance Function

The key to achieving MPC is to obtain the most effective control quantities by solving the performance function optimally. In this paper, the optimal control voltage would be obtained.

The performance function is composed of the predicted current components at the $(k+2)$-th sampling instant and the control voltage variations, with corresponding weighting coefficients [29]. The function is defined as follows:

$$w(k) = \alpha_1[i_{Nd}{}^*(k) - i_{Nd}(k+2)]^2 + \alpha_2[i_{Nq}{}^*(k) - i_{Nq}(k+2)]^2 + \beta_1\Delta u_{abd}^2(k+1) + \beta_2\Delta u_{abq}^2(k+1) \quad (10)$$

where α_1, α_2, β_1, and β_2 represent the weighting coefficients of the line current and voltage variations.

There are no analytical or numerical methods or control design theories to adjust these parameters; currently, they are determined based on empirical procedures. In [30], an approach based on an empirical procedure is presented to obtain suitable weighting factors. When more objectives are

considered, the weighting coefficients are usually obtained using trial and error procedures and running time-consuming simulations [31]. Since the front two components in Equation (10) are both the current variables, weighting factors can be considered as the same, as are the back two components. Thus, if two of weighting coefficients are decided, the other two can also be set, which can be clearly seen from Table A1.

In order to make $i_{Nd}(k+2)$ and $i_{Nq}(k+2)$ track their references $i_{Nd}(k)^*$ and $i_{Nq}(k)^*$, the variations of the control voltage need to be kept as small as possible. To do this, take the derivative of Equation (10) to find the extreme point, as shown in Equation (11):

$$\begin{cases} \frac{\partial w(k)}{\partial \Delta u_{abd}(k+1)} = 0 \\ \frac{\partial w(k)}{\partial \Delta u_{abq}(k+1)} = 0 \end{cases} \tag{11}$$

Substituting $i_{Nd}(k+2)$ and $i_{Nq}(k+2)$ of Equation (9) and $w(k)$ of Equation (10) into Equation (11), the optimal control variables $\Delta u_{abd}(k+1)$ and $\Delta u_{abq}(k+1)$ can be derived as Equation (12). In addition, the output control voltages $u_{abd}(k)^*$ and $u_{abq}(k)^*$ can be depicted by Equation (13):

$$\begin{cases} \Delta u_{abd}(k+1) = \frac{-L_N T_s \alpha_1}{T_s^2 \alpha_1 + L_N^2 \beta_1} \{ i_{Nd}{}^*(k) - [(1 - \frac{T_s R_N}{L_N}) i_{Nd}(k+1) + T_s \omega i_{Nq}(k+1) - \frac{T_s}{L_N} u_{abd}(k) + \frac{T_s}{L_N} u_{Nd}(k+1)] \} \\ \Delta u_{abq}(k+1) = \frac{-L_N T_s \alpha_2}{T_s^2 \alpha_2 + L_N^2 \beta_2} \{ i_{Nq}{}^*(k) - [(1 - \frac{T_s R_N}{L_N}) i_{Nq}(k+1) - T_s \omega i_{Nd}(k+1) - \frac{T_s}{L_N} u_{abq}(k) + \frac{T_s}{L_N} u_{Nq}(k+1)] \} \end{cases} \tag{12}$$

$$\begin{cases} u_{abd}(k)^* = u_{abd}(k+1) = u_{abd}(k) + \Delta u_{abd}(k+1) \\ u_{abq}(k)^* = u_{abq}(k+1) = u_{abq}(k) + \Delta u_{abq}(k+1) \end{cases} \tag{13}$$

The optimal control voltages that minimize the performance function are calculated by Equation (13), and then fed to a modulator stage to generate the PWM drive signal g at the k-th instant. An MBPCC controller of LSCs can be designed based on the deducing process of prediction model, the delay compensation, and the solution of performance function. Figure 4 shows the block diagram of the MBPCC. A PI controller is adopted in the voltage loop to regulate the DC-side voltage, and its output is set as the current d-axis reference $i_{Nd}(k)^*$. In addition, the q-axis current reference $i_{Nq}(k)^*$ generally needs to equal zero to achieve the unit power factor.

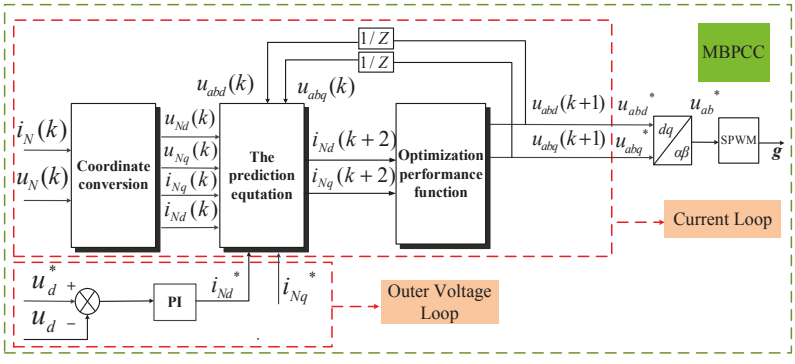

Figure 4. Block diagram of model-based predictive current control (MBPCC).

When LFO happens in high-speed railways, the fluctuation of the traction network's voltage will disturb the performance of the EMUs' LSC. Currents and voltages of the controller cannot trace well with the references, and lead to greater deterioration of fluctuation. MBPCC is a current-controlled strategy constituted by a prediction model and the performance function. By making the performance function minimal, the optimal control variables can be calculated to ensure the prediction current

value tracking the references. Therefore, it is possible to adopt MBPCC to optimize the performance of the converter controller and suppress the LFO.

3. Simulations of One Traction Drive Unit of Electric Multiple Units

To validate the feasibility and effectiveness of the proposed method, simulation verifications based on the model of EMUs' dual traction LSCs, namely the traction drive unit, were carried out from several aspects, by comparing with the control performance of traditional TDCC in MATLAB /SIMULINK, respectively. The simulation model of EMUs' dual traction LSCs was built as shown in Figure 5. The adjustable parameters in the TDCC and MBPCC controllers were regulated into the most appropriate values, as listed in Tables A1 and A2.

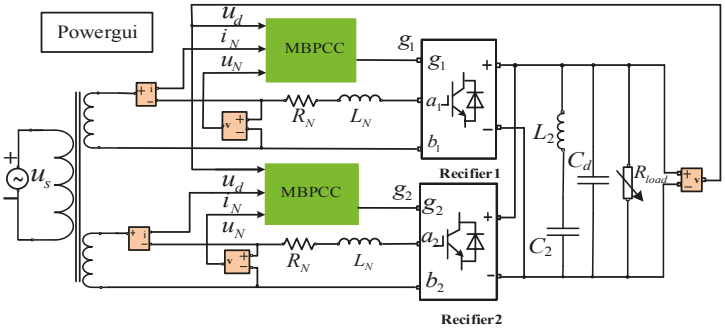

Figure 5. The circuit of electric multiple units' (EMUs') dual traction line-side converters (LSCs), based on MBPCC.

The block diagram of TDCC is shown in Figure 6. The outer voltage control loop uses a PI controller to keep the DC-side voltage equal to its reference value, and the PI output provides the reference of input current. The proportional controller of the inner current control loop makes the input current track its reference value.

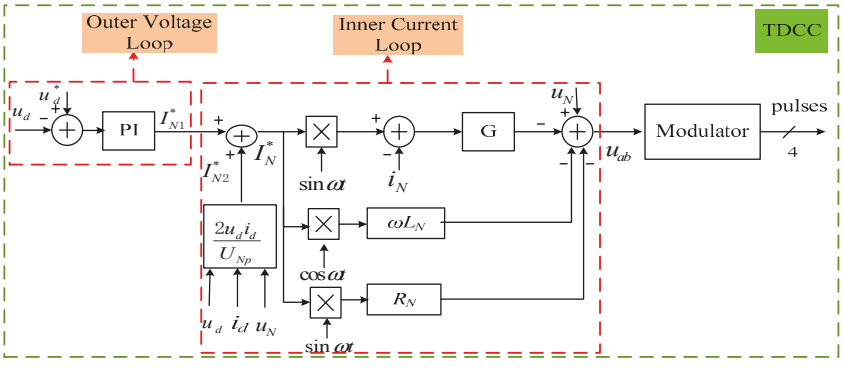

Figure 6. Block diagram of transient direct current control (TDCC).

3.1. Start-Operation Process

The start-operation process of EMUs' dual traction LSCs is divided into three periods—namely, the pre-charge period, the uncontrolled rectifier period, and the nominal load period. In the simulation, the initial time of the three stages was set to 0 s, 0.2 s, and 0.4 s, respectively. To compare MBPCC with

TDCC, the waveforms of u_N and i_N, as well as u_d are depicted in Figure 7. The performance indexes of the u_d of EMUs' dual traction LSCs are shown in Table 1. Figure 8 shows the fast Fourier transform (FFT) analysis results of the i_N with MBPCC and TDCC.

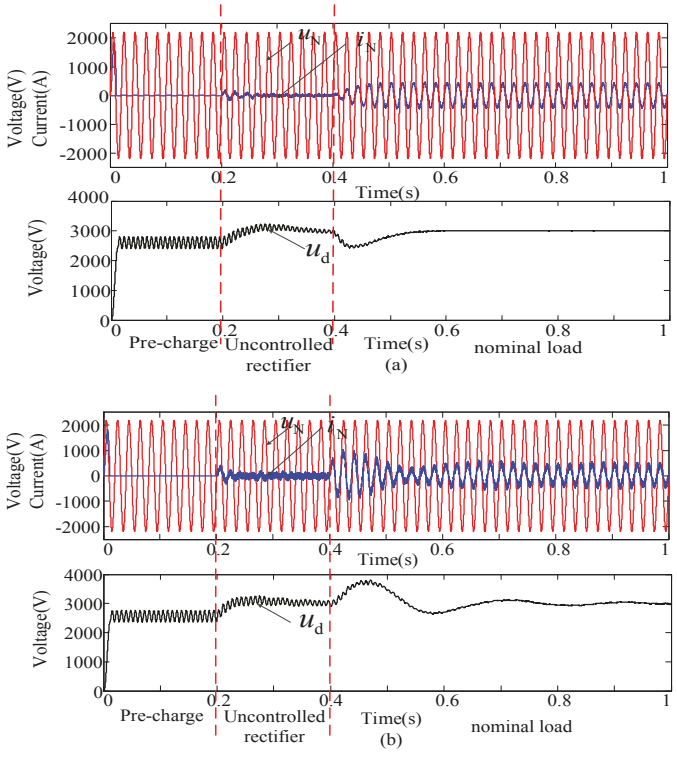

Figure 7. Simulation waveforms of u_N with i_N, as well as u_d, using (**a**) MBPCC and (**b**) TDCC.

Table 1. Comparison of performance indexes.

Control	Overshoot	Peak Time	Adjustment Time	Voltage Fluctuation
MBPCC	3.33%	0.10 s	0.25 s	±10 V
TDCC	26.70%	0.12 s	0.40 s	±40 V

In Figure 7, the pre-charge and uncontrolled rectifier periods of TDCC are almost the same as MBPCC's. When the nominal load is accessed, the u_d based on TDCC achieves the reference value after 0.4 s, with a large overshoot. However, the u_d based on MBPCC achieves stability after 0.25 s, and the overshoot is about 100 V, far less than that of the PI control. The voltage fluctuation range of MBPCC is only ±10 V, while the voltage fluctuation based on TDCC is larger. In Figure 8, the total harmonic distortion (THD) of i_N based on MBPCC is 4.76%, apparently lower than that of TDCC. In the control system based on MBPCC, there are more high-order harmonics around the odd switching frequency, which is considered as a drawback of the control strategy. Overall, MBPCC presents a better performance and dynamic response, due to the smaller overshoot, shorter adjustment time, and tinier voltage fluctuation.

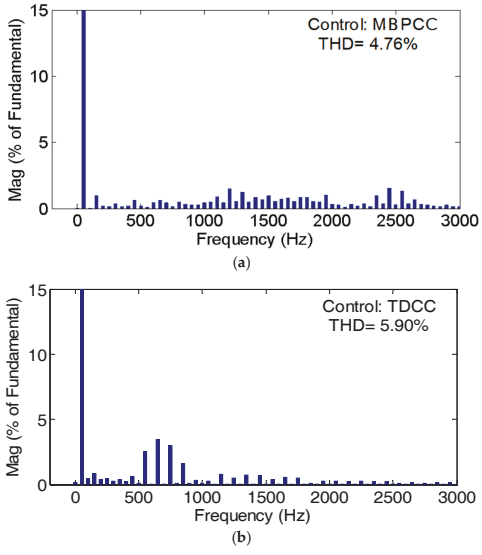

Figure 8. FFT results for i_N under (**a**) MBPCC and (**b**) TDCC.

3.2. Sudden-Load-Change Process

To further validate the dynamic response performance, the simulations under the sudden-load-change condition were carried out. Figure 9 shows the simulation waveforms of the dynamic response of the u_d under the condition of the load changing suddenly, based on MBPCC and TDCC, respectively. The load changes at 1 s, from 10 Ω to 0.01 Ω. Based on MBPCC, the u_d has gone through a period of voltage decline from 3000 V to about 2500 V, and returns to 3000 V after 0.5 s, with a ±20 V voltage fluctuation later. In contrast, the u_d based on TDCC drops by nearly 800 V, and fluctuates in the range of ±50 V after becoming stable again. Therefore, it can be concluded that the MBPCC has a better capacity for resisting disturbance than the transient PI control, because of smaller voltage decline and fluctuation when the load changes suddenly.

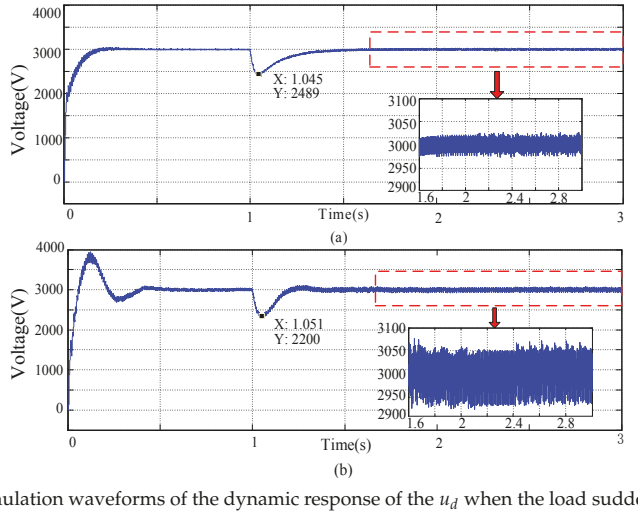

Figure 9. Simulation waveforms of the dynamic response of the u_d when the load suddenly changes, with (**a**) MBPCC and (**b**) TDCC.

3.3. Track Performance

At first, we measured i_{Nd}^* when the outer voltage loop plays a role in obtaining the reference current value. i_{Nd}^* was about equal to 830 A, and i_{Nq}^* was set to zero. Based on the measured values, we replaced the outer voltage loop by a step signal, to test the track performance while the reference current steps up or down similarly, a step signal replaces the constant module, in order to detect the track performance while the reference current i_{Nq}^* steps up or down.

As shown in Figure 10a, i_{Nd} decreased with i_{Nd}^*, varying from 830 A to 600 A at 0.3 s, and i_{Nq} returned to zero after a prompt downward fluctuation. In Figure 10b, i_{Nd} increases, with i_{Nd}^* varying from 830 A to 1000 A, and i_{Nq} rapidly returns the setting value i_{Nq}^* after an upward shock. Similar conditions can be seen in Figure 11, when i_{Nq}^* varies. In two cases, i_{Nd} and i_{Nq} can quickly track the reference current values of i_{Nd}^* and i_{Nq}^* in a very short time, regardless of whether i_{Nd}^* or i_{Nq}^* steps up or down. Thus, MBPCC could guarantee that the system has good track performance when the reference current value changes.

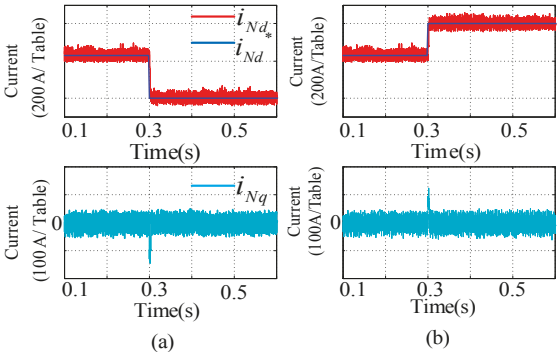

Figure 10. Simulation waveforms of i_{Nd} and i_{Nq} when (**a**) i_{Nd}^* varies from 830 A to 600 A and when (**b**) i_{Nd}^* varies from 830 A to 1000 A.

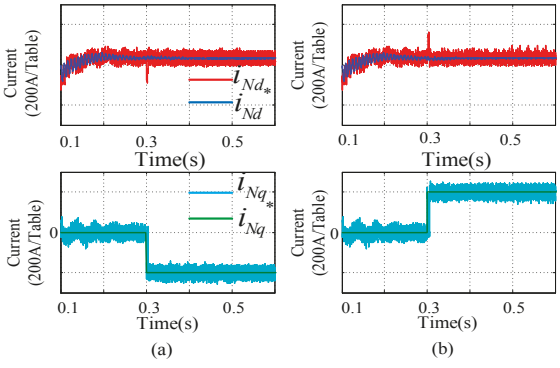

Figure 11. Simulation waveforms of i_{Nd} and i_{Nq} when (**a**) i_{Nq}^* varies from 0 A to −200 A and (**b**) when i_{Nq}^* varies from 0 A to 200 A.

In conclusion, MBPCC presents a better control performance for EMUs' dual traction LSCs, due to the smaller overshoot, shorter adjustment time, and tinier voltage fluctuation in the start-operation process, as well as its greater capacity for resisting disturbance and better track performance between the actual current and the reference current.

4. Semi-Physical Test of Electric Multiple Units' Dual Traction Line-Side Converter

To reflect the real application condition, a whole dSPACE semi-physical experimental platform was established. The dSPACE semi-physical experimental platform included the dSPACE simulator, the physical control circuit chassis, a power supply, and an external PC, as shown in Figure 12. The dSPACE simulator was used to simulate the circuit topology of EMUs' dual traction LSCs, and connected with the PC through a network line, so as to import the circuit simulation model from the PC to the dSPACE simulator. The physical control circuit chassis was connected to the PC through the data cable, in order to achieve the control algorithm program import and debugging. The power supply was supplied to the physical control circuit chassis.

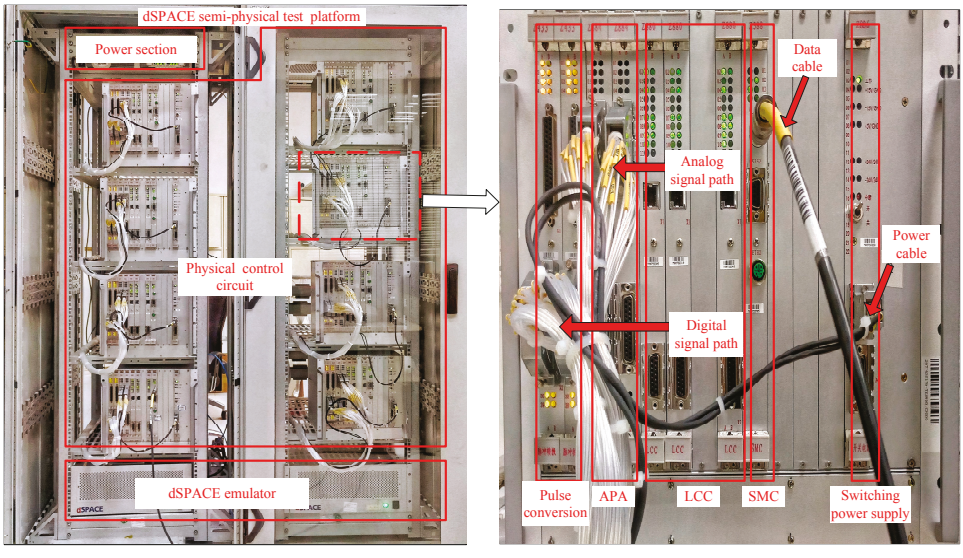

Figure 12. The dSPACE semi-physical experimental platform.

The most important part of the dSPACE semi-physical experimental platform was the physical control circuit chassis, which was composed of the main five modules, as shown in right-hand section of Figure 12:

(1) Switching power supply module: the switching power supply module has the function of a power supply for the entire physical control circuit chassis.
(2) SMC module: the SMC module realizes the data transmission of the physical control circuit chassis and the outside. After control program is compiled on the computer, the SMC module achieves the connection with the computer through the data cable, and control strategy is imported into the physical control circuit chassis.
(3) LCC module: an LCC module contains four internal DSPs, each of which controls a single converter. A physical control circuit chassis contains three LCC modules, so it can control six dual traction LSCs.
(4) APA module: the dSPACE simulation voltage and current signals are transmitted to the APA module through the analog signal channel, and the module achieves the signal acquisition of the physical control circuit chassis.
(5) Pulse conversion module: the pulse conversion module outputs the digital control signal of EMUs; thus, it can realize the control for EMUs directly.

Figures 13 and 14 show the simulation waveforms of u_N and i_N, as well as u_d when the system of dual traction LSCs are tested on the dSPACE semi-physical platform using MBPCC and TDCC, respectively. The numerical value on the abscissa multiplied by $8e^{-5}$ represents the simulation time. The process is performed from startup to normal working conditions.

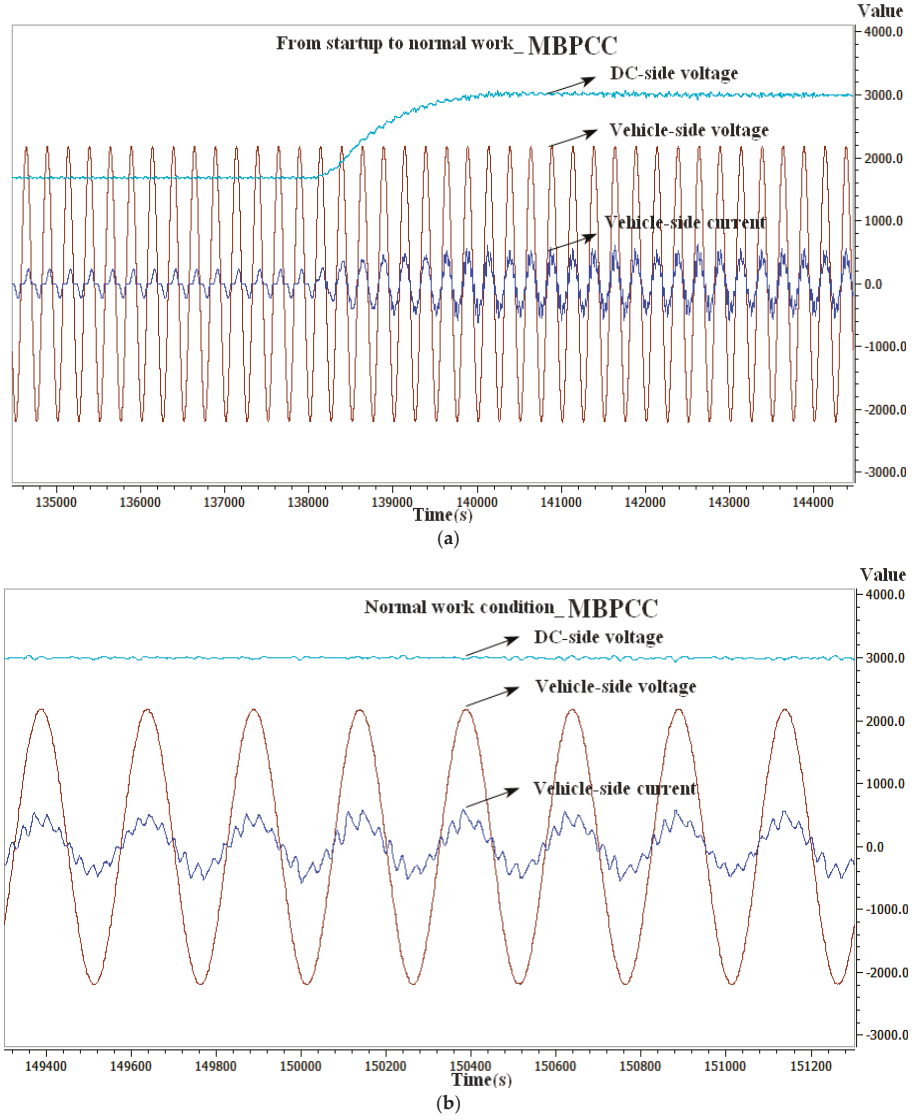

Figure 13. Waveforms of u_N and i_N, as well as u_d using MBPCC: (**a**) the process from startup to normal work; and (**b**) normal working conditions.

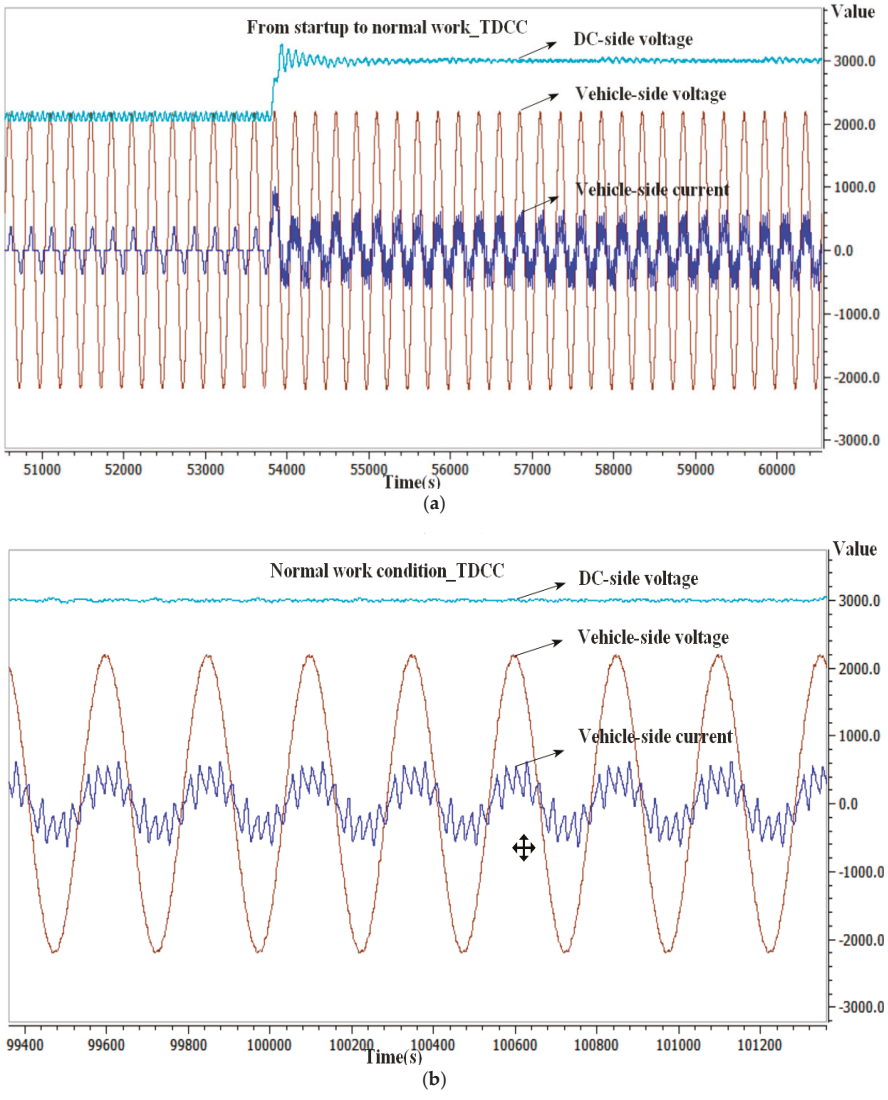

Figure 14. Waveforms of u_N and i_N, as well as u_d, using TDCC (**a**) the process from startup to normal work and (**b**) under normal working conditions.

The experimental results on the dSPACE semi-physical platform are almost in accordance with the simulation results in MATLAB. In Figure 13a, the u_d based on MPBCC achieves the reference value without the overshoot. As seen in Figure 13b, i_N can remain in phase with u_N, which means that the dual traction LSCs operate with a unified power factor. Compared with TDCC, as shown in Figure 14, i_N based on MBPCC has the smaller harmonic distortion.

5. System Verification

The dSPACE semi-physical experiment when multi-EMUs are accessed in the power supply system is still a challenge. To verify the suppression effect of LFO and perform further sensibility analyses,

the simulations of seven EMUs accessed in traction network were performed in MATLAB/SIMULINK. The autotransformer power supply system is mostly adopted in high-speed railways of China. The structure of a traction network is very complicated because of a mass of multi-conductor transmission lines that are distributed, as well as the mutual coupling effect [5]. Therefore, considering the practical factors, such as the skin effect of lines and external disturbances, it is more reasonable to adopt a reduced-order method to model the traction network [5,32] than the Thevenin-equivalent method used in [33]. Avoiding a duplication of effort, the modeling process of the vehicle-grid coupling system is no longer described.

5.1. The Effect of Suppressing Low-Frequency Oscillation

Based on the TDCC controller, when seven vehicles are accessed in the reduced-order model of traction network, LFO occurs in both voltage and current, as shown in Figure 15. The u_d fluctuates between 2600 V and 3600 V. It can also be found that the traction network voltage arrives at the wave crest while the grid-side current reaches the wave trough. The amplitude fluctuation of voltages and currents will influence the performance of the EMUs' LSC, and even lead to a traction blockade.

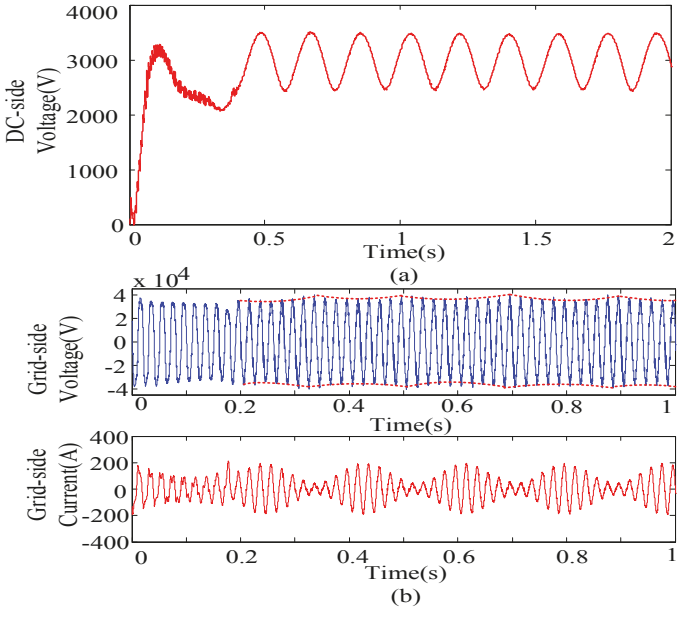

Figure 15. Waveforms of seven EMUs accessed with TDCC: (**a**) u_d; and (**b**) grid-side voltage and current.

By adopting the proposed MBPCC strategy, the system can still achieve stability when the number of multi-EMUs accessed in the traction network reaches seven. Figure 16 shows the simulation results when seven EMUs are accessed. It can be observed that the LFO does not appear even though vehicle numbers have reached their critical value. In a stable state, the u_d remains stable at about 3000 V, and the voltage deviation is $\pm$10 V. The fluctuations of grid-side voltage and current are small.

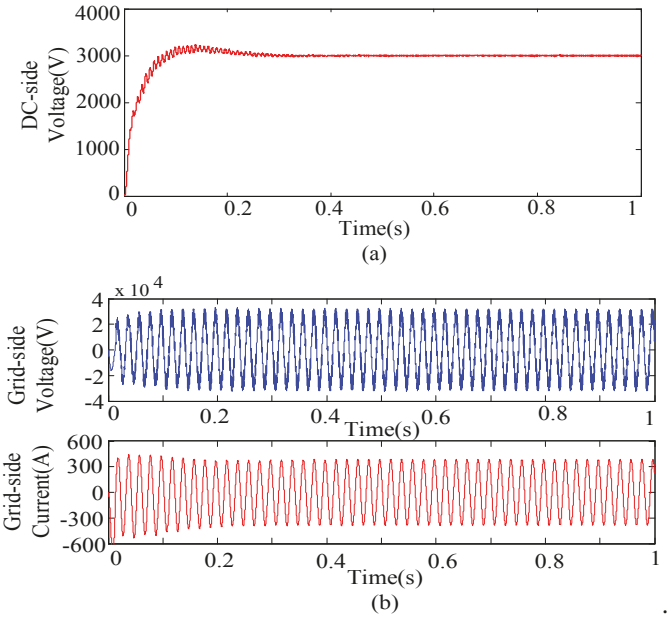

Figure 16. Waveforms of seven EMUs accessed with MBPCC: (**a**) u_d and (**b**) grid-side voltage and current.

5.2. Analysis of System Parameters

The analysis of parameter sensitivity is necessary to find out their influence on the stability of the vehicle-grid coupling system. In this paper, in order to find out the effects of different external parameters on the LFO and the performance of traction LSC, three parameters (the load resistance R_{load}, equivalent leakage inductance, L_N and the distance to power supply D) are discussed when seven vehicles are accessed in the traction network.

5.2.1. Load Resistance R_{load}

Figure 17 shows the waveforms of the u_d under TDCC and MBPCC, when the load resistance R_{load} is set as 20, 50, 75, or 100 Ω, respectively. As seen in Table 2 and Figure 17, when the load resistance R_{load} varies, both the overshoot and adjustment time of the u_d under MBPCC have only some tiny variations.

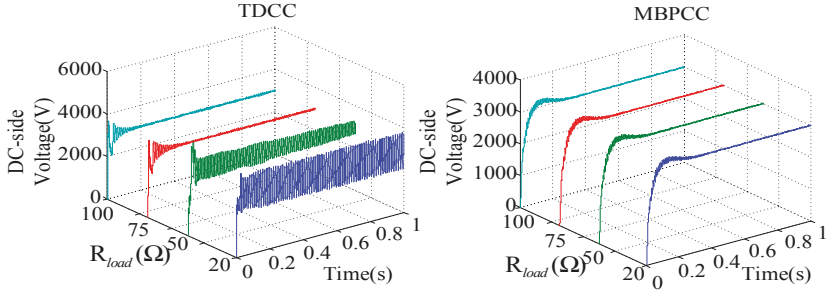

Figure 17. Waveforms of u_d when R_{load} = 20, 50, 75, or 100 Ω.

Table 2. Performance of the system.

Item	Value	TDCC		MBPCC	
		Oscillation Pattern	Oscillation Peak (V)	Overshoot (V)	Regulation Time (s)
R_{load} (Ω)	20	Stable	3600	3200	0.25
	50	Damping	[3500, 3350]	3200	0.25
	75	No	-	3200	0.25
	100	No	-	3200	0.25
L_N (H)	0.001	No	-	3200	0.25
	0.002	Damping	[3500, 3350]	3200	0.25
	0.004	Stable	3600	3200	0.25
	0.006	Stable	3700	3200	0.25
D (km)	10	Damping	[3240, 3530]	3200	0.20
	20	Damping	[3240, 3520]	3200	0.20
	30	Damping	[3300, 3520]	3200	0.30
	40	Stable	3500	3300	0.50

(1) Damping oscillation: the oscillation peak diminishes gradually and returns final to a stable state; (2) Stable oscillation: the oscillation peak abidingly maintains a value [9].

However, LFO happens under TDCC when the load resistance is small. The smaller R_{load} is, the severer the oscillation is. LFO would not occur once R_{load} exceeds a value about 75 Ω. Therefore, it can be concluded that the load resistance has fewer effects on the proposed method than TDCC.

5.2.2. Equivalent Leakage Inductance L_N

In Figure 18, when the equivalent leakage inductance of vehicle transformer L_N varies from 0.001 H to 0.006 H, the system under MBPCC maintains an initially good dynamic performance, with little change in the u_d's overshoot and regulation time. Hence, MBPCC can keep good performance and be unaffected by the change of L_N, while TDCC is very sensitive. When L_N is set as 0.001 H, the LFO does not happen. With the increase of L_N, oscillation appears, and the oscillation peak enlarges gradually.

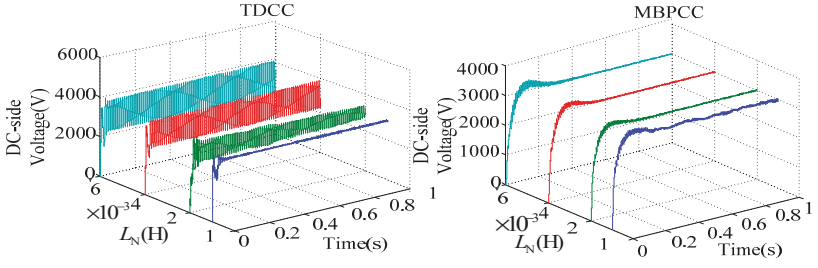

Figure 18. Waveforms of u_d when L_N = 0.001, 0.002, 0.004, and 0.006 H.

5.2.3. Distance to Power Supply D

D represents the distance to the power supply in the traction network. The larger D is, the larger the equivalent impedance on the line side will be. As seen in Figure 19 and Table 2, with the change of D, the influence on MBPCC's control performance is slight, because the overshoot and adjustment time change only slightly more than before, and the LFO does not happen.

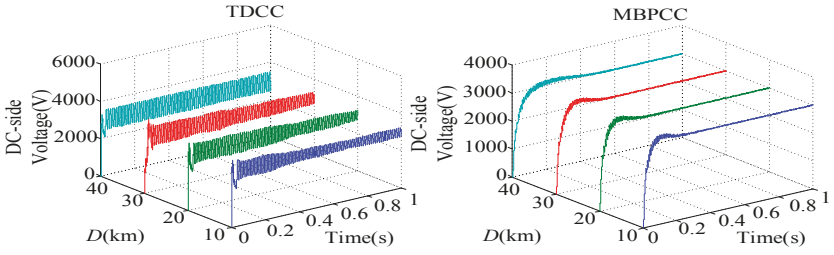

Figure 19. Waveforms of u_d when D = 10, 20, 30, and 40 km.

As for TDCC, the oscillation phenomenon can be observed when D was chosen as 10, 20, 30, and 40 km. The oscillation peak value is about 3500 V at first, and then gradually diminishes in the former three cases; when D is 40 km, the oscillation peak will be kept at 3500 V. The details are listed in Table 2. It was found that the oscillation peak varies from 3530 V to 3240 V within 1 s when D is 10 km, and from 3520 V to 3300 V when D is 30 km. The damping capability of LFO decreases with the increase of D under TDCC.

Contrasting results show that MBPCC can be almost unaffected by the three parameters, and LFO does not happen when these parameters change. However, the performance of TDCC is sensitive to the three parameters. Both the oscillation pattern and oscillation peak can be easily influenced when the parameters change.

6. Conclusions

To optimize the control performance of EMUs' traction drive units, namely dual traction LSCs, and suppress LFO in vehicle-grid coupling system of high-speed railways, MBPCC is proposed in order to apply the traction LSC of CRH3 EMUs. After theoretical analysis, simulation verifications, and semi-physical verifications, the performance of MBPCC is demonstrated in comparison to TDCC, and the advantages of each listed below:

(1) Simulation verifications in MATLAB of EMUs' dual traction LSCs based on MBPCC and TDCC were implemented from three aspects. The results prove that MBPCC can obtain better dynamic and static performances, such as a smaller THD, tinier overshoot in start-operation process, greater capacity for resisting disturbance under load changing suddenly, and a better track performance.

(2) Semi-physical verifications in the dSPACE semi-physical experimental platform were realized. The results certified the effectiveness of MBPCC and its superiority in real applications, when compared with TDCC.

(3) When the multi-EMUs were assessed in the reduced-order model of traction network, the results showed that MBPCC can ensure the system's stability and suppress LFO more efficiently compared with TDCC.

(4) The influences of different external parameters R_{load}, L_N, and D in the vehicle-grid coupling system under MBPCC and TDCC have been discussed in detail. It could be concluded that these three parameters have a tiny impact on MBPCC, while they greatly influence the performance of TDCC. Both the oscillation pattern and oscillation peak under TDCC can be easily influenced when parameters change.

The proposed method can be applied for the control of EMUs' traction LSCs, and provide a good effect on the suppression of LFO. Moreover, MBPCC is insensitive to system parameters, which provides greater possibilities for its application. There is some advanced work regarding MBPCC that can be studied in the future. In the aspect of physical verification, multi-EMUs accessed in the model of the traction network should be realized in order to increase the reliability for suppressing LFO. With respect to algorithm optimization, combining predictive control with the disturbance

observer can further advance the performance and robustness of the system, which can deal with the modeling errors and uncertainties, disturbances, and sensor noise.

Author Contributions: The individual contribution of each co-author with regards to the reported research and writing of the paper is as follows. Z.L. and Y.W. conceived the idea, Y.W. performed experiments and data analysis, and all authors wrote the paper. All authors have read and approved the final manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix

The parameters of the traction LSC of CRH3 EMUs under MBPCC and TDCC are listed in Tables A1 and A2.

Table A1. Parameters of EMUs' dual traction LSCs under MBPCC.

System Parameter	Value	Control Parameter	Value
u_s	25 kV	K_{iv}	0.1
L_N	0.004 H	K_{pv}	9
R_N	0.06 Ω	α_1	1
L_2	0.00084 H	α_2	1
C_2	0.003 F	β_1	0.0002
C_d	0.006 F	β_2	0.0002
U_d	3000 V	–	–
R_{load}	10 Ω	–	–

Table A2. Parameters of EMUs' dual traction LSCs under TDCC.

System Parameter	Value	Control Parameter	Value
u_s	25 kV	K_{iv}	0.1
L_N	0.004 H	K_{pv}	9
R_N	0.06 Ω	G	1
L_2	0.00084 H	–	–
C_2	0.003 F	–	–
C_d	0.006 F	–	–
U_d	3000 V	–	–
R_{load}	10 Ω	–	–

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High-Efficiency Design and Control of Zeta Inverter for Single-Phase Grid-Connected Applications

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Abstract: The conventional zeta inverter has been used for single-phase grid-connected applications. However, it has high switching losses to operate at high switching frequency in the continuous conduction mode (CCM). To address this drawback, this paper suggests a high-efficiency zeta inverter using active clamp and synchronous rectification techniques. The proposed inverter utilizes the active clamp circuit for reducing switching losses. The non-complementary switching scheme is adopted for not only clamping the switch voltage stresses, but also alleviating the circulating energy. In addition, the synchronous rectification is implemented for reducing the body diode conduction of power switches. By using the silicon carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs), the switching performance of the proposed inverter is improved. Its operation principle and control strategy are presented. A 220-W prototype has been designed and tested to evaluate the performance of the proposed inverter.

Keywords: zeta inverter; active clamp; synchronous rectification; power efficiency

1. Introduction

With the fast growth of renewable energy markets, many single-stage isolated inverters have been developed for single-phase grid-connected applications [1–9]. Among them, the zeta inverter [7–9] has been gaining attention due to the advantages of its low grid current ripple and low circuit component count, compared to other single-stage inverters such as flyback inverters [1–4] and Cuk inverters [5,6]. Of course, although the zeta inverter has large current ripples at the dc side, similar to the flyback inverter, it has been widely adopted for single-phase photovoltaic applications [7–9] due to its simple and flexible circuitry.

As the zeta inverter operates at a constant switching frequency, it has two operation modes: discontinuous conduction mode (DCM) and continuous conduction mode (CCM). The DCM zeta inverter has been used for low-power applications [7]. The grid current is easily controlled, as its control transfer function for the grid current is linear in DCM [8]. However, as the power level increases, the DCM zeta inverter suffers from high conduction losses. The DCM zeta inverters need to be connected in parallel to alleviate conduction losses.

When the zeta inverter operates in CCM, it can withstand a higher power level than the DCM zeta inverter. The CCM zeta inverter has been suggested in [9]. Figure 1 shows its circuit diagram, which is equivalent to the circuit diagram in [9]. It consists of the primary circuit (S_{P1}, L_m, L_{lk}) and the secondary circuit (C_S, S_{S1} ~ S_{S4}, L_g). T is a high-frequency transformer, which has the magnetizing inductor L_m and the leakage inductor L_{lk}. The CCM zeta inverter has achieved higher efficiency than the DCM zeta inverter by lowering conduction losses [9]. However, the CCM zeta inverter suffers from high switching losses. In the primary circuit, the switch S_{P1} operates at a high switching frequency to regulate the grid current i_g. When S_{P1} is turned off, a high voltage spike is generated due to the energy stored in the leakage inductor L_{lk}, which increases switching losses [10].

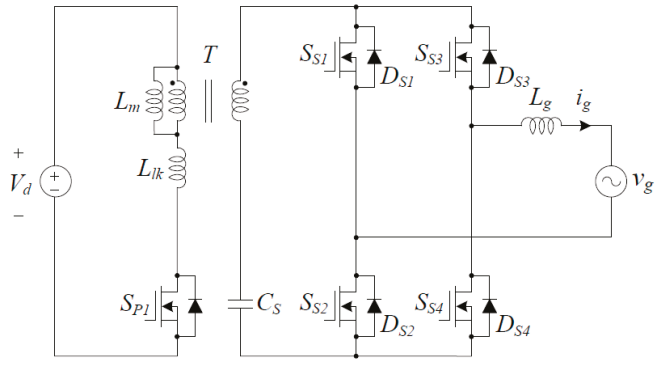

Figure 1. Circuit diagram of the zeta inverter.

The secondary circuit provides the current path to fold the grid voltage v_g and gives the freewheeling path for the grid current i_g. The switches $S_{S1} \sim S_{S4}$ operate at grid frequency according to the polarity of v_g. S_{S2} and S_{S3} are always turned on for the positive grid cycle, while S_{S1} and S_{S4} are always turned on for the negative grid cycle. For the positive grid cycle, when S_{P1} is turned on, i_g flows through S_{S2} and S_{S3}. As S_{P1} is turned off, i_g flows through S_{S2}, S_{S3}, D_{S1}, and D_{S4}. D_{S1} and D_{S4} are the body diodes, which are turned on for the freewheeling of i_g. However, when S_{P1} is turned on again, D_{S1} and D_{S4} are not turned off instantly due to the slow reverse recovery process [11]. The reverse recovery currents of D_{S1} and D_{S4} cause high voltage spikes across D_{S1} and D_{S4}. They are also transferred to the primary circuit, which increases the turn-on switching losses of S_{P1}. It is worse when high-voltage silicon (Si) metal oxide semiconductor field effect transistors (MOSFETs) are adopted, because their body diodes have poor reverse recovery characteristics. These drawbacks limit the practical use of the CCM zeta inverter, despite its advantages.

This paper proposes a high-efficiency zeta inverter to cope with the above-mentioned drawbacks. Figure 2 shows the circuit diagram of the proposed inverter. The active clamp circuit has been used for reducing switching losses in the primary circuit. The active clamp circuit has the auxiliary switch S_{P2} and the clamp capacitor C_P. Conventionally, the auxiliary switch S_{P2} operates complementary to the main switch S_{P1} [12]. As the energy stored in L_{lk} is absorbed in C_P, the switch voltages are clamped to a constant voltage. However, this conventional method increases the circulating current in the primary circuit. It causes additional power losses due to high circulating energy. To address this drawback, the non-complementary switching scheme [13] has been adopted. In the non-complementary method, S_{P2} is turned on for a short time before S_{P1} is turned on. As the leakage energy is recycled with reduced circulating current, power losses associated with the circulating energy can be minimized in the proposed inverter.

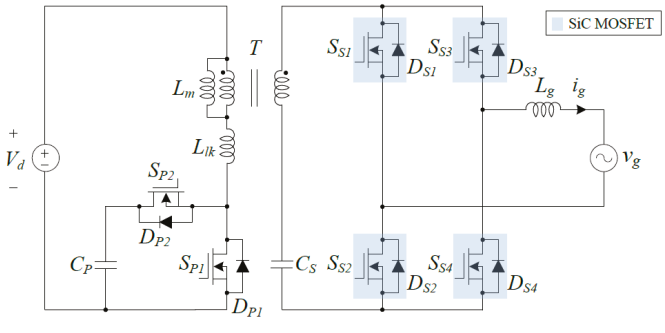

Figure 2. Circuit diagram of the proposed inverter.

In the secondary circuit, the synchronous rectification [14] is used for reducing the body diode conduction of MOSFETs. With synchronous rectification, S_{S1} (S_{S2}) and S_{S4} (S_{S3}) are turned on for the positive (negative) grid cycle when S_{P1} is turned off. It allows i_g to freewheel through the MOSFET channels instead of the body diodes. It avoids the body diode conduction, increasing the power efficiency, because the voltage drop across the on-state resistance of the MOSFET is lower than the forward voltage drop of the body diode [15]. The silicon carbide (SiC) MOSFET has been utilized for the synchronous rectification of S_{S1} ~ S_{S4}. Due to the advantages over Si MOSFETs such as wider bandgap and higher electric field capacity [16], it improves the switching performance of the proposed inverter.

This paper is organized as follows. Section 2 describes the operation principle of the proposed inverter in the steady-state condition, along with the analysis of active clamp and synchronous rectification techniques. It also describes the control strategy for the CCM operation of the proposed inverter. Section 3 discusses the experimental results to verify the performance of the proposed inverter. Section 4 presents the conclusion of this paper.

2. Proposed Inverter

2.1. Operation Principle

Figure 3 shows the circuit diagram of the proposed inverter, which shows the reference directions of currents and voltages. The proposed inverter consists of the primary circuit (S_{P1}, S_{P2}, C_P, L_m, L_{lk}) and the secondary circuit (C_S, S_{S1} ~ S_{S4}, L_g). The active clamp circuit consists of S_{P2} and C_P. T is a high-frequency transformer, which has the magnetizing inductor L_m and the leakage inductor L_{lk}. It is assumed that L_m >> L_{lk}. Its turns ratio n is N_S / N_P. N_P is the primary winding turns. N_S is the secondary winding turns. All of the power switches are considered ideal except for their body diodes. V_d is the dc input voltage. v_g is the grid voltage. L_m and L_g are large enough so that the currents i_{Lm} and i_g are continuous during one switching period T_s, respectively. C_P and C_S are large enough so that the voltages V_{Cp} and V_{Cs} are constant during T_s, respectively. V_{Cs} is considered as $|v_g|$ because the secondary circuit provides the current path to fold v_g.

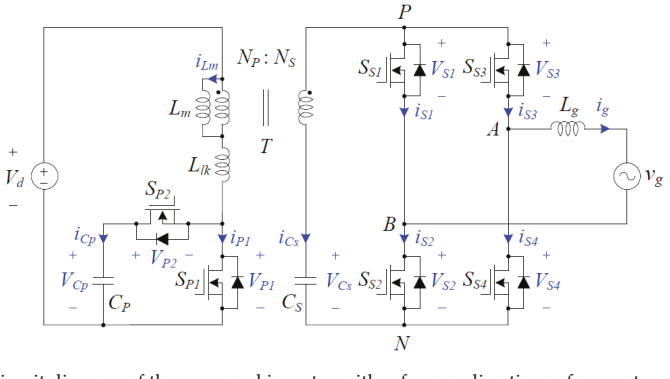

Figure 3. Circuit diagram of the proposed inverter with reference directions of currents and voltages.

Figure 4 shows the switching circuit diagrams of the proposed inverter during T_s for the positive grid cycle. Figure 5 shows the switching waveform diagrams of the proposed inverter during T_s for the positive grid cycle. $V_{gate,P1}$ and $V_{gate,P2}$ are the gate signals for S_{P1} and S_{P2}, respectively. $V_{gate,S1}$ ~ $V_{gate,S4}$ are the gate signals for S_{S1} ~ S_{S4}, respectively. S_{P1} and S_{P2} operate with a constant high switching frequency f_s (= $1/T_s$). S_{P2} is turned on for a short time before S_{P1} is turned on. For the positive grid cycle, S_{S2} and S_{S3} are always turned on. S_{S1} and S_{S4} operate complementary to S_{P1}. The proposed inverter has four switching modes during T_s for the positive grid cycle, which are outlined below.

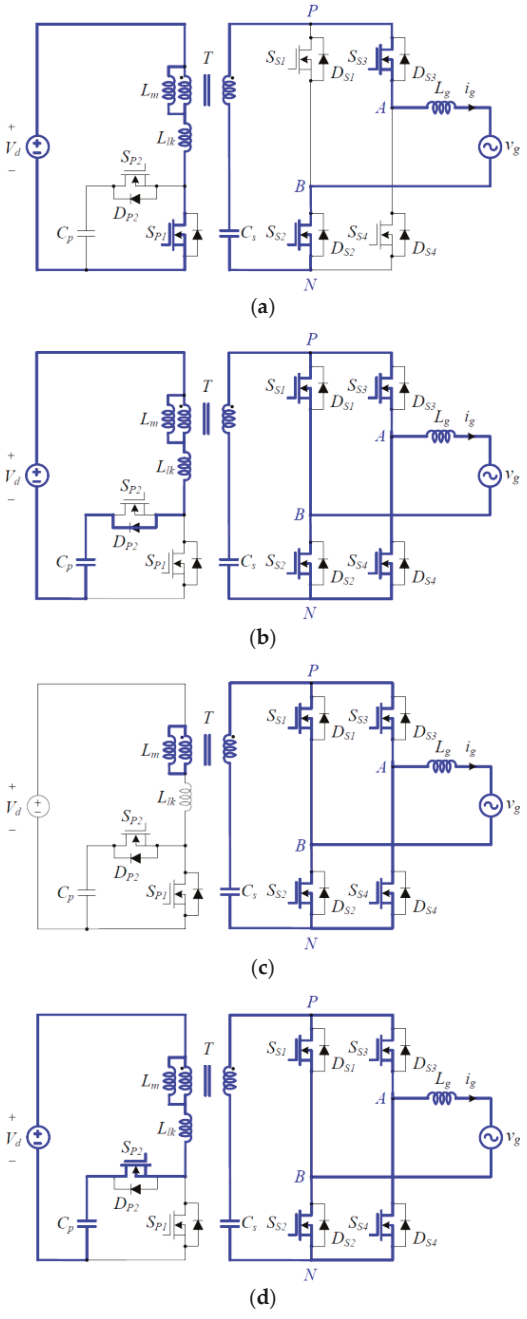

Figure 4. Switching circuit diagrams of the proposed inverter during T_s for the positive grid cycle: (**a**) Mode 1; (**b**) Mode 2; (**c**) Mode 3; and (**d**) Mode 4.

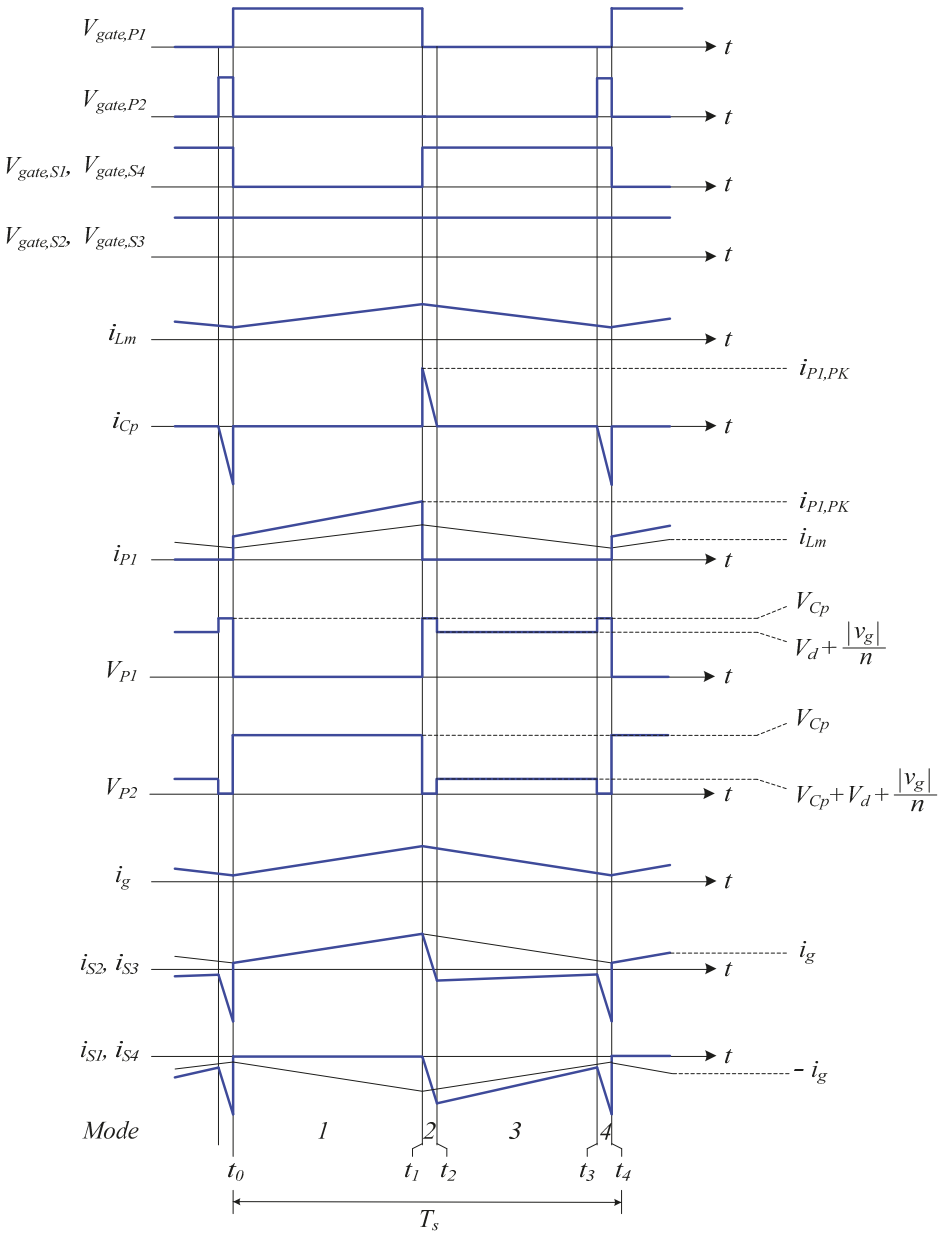

Figure 5. Switching waveform diagrams of the proposed inverter during T_s for the positive grid cycle.

Mode 1 [t_o–t_1]: At $t = t_o$, S_{P1} is turned on. L_m and L_{lk} store the energy from V_d. i_{Lm} increases linearly at the rate of $di_{Lm}/dt = V_d/(L_m + L_{lk})$. The voltage across the secondary winding of T is $nL_mV_d/(L_m + L_{lk})$. i_g increases linearly at the rate of $di_g/dt = nL_mV_d/(L_m + L_{lk})/L_g$.

Mode 2 [t_1–t_2]: At $t = t_1$, D_{P2} is turned on as S_{P1} is turned off. The energy stored in L_{lk} is stored in C_P. The switch voltage V_{P1} is clamped to V_{Cp}. S_{S1} and S_{S4} are turned on in this mode. As the voltage

across the secondary winding of T is v_g, i_{Lm} decreases linearly at the rate of $di_{Lm}/dt = -v_g/nL_m$. As i_g freewheels through $S_{S1} \sim S_{S4}$, i_g decreases linearly at the rate of $di_g/dt = -v_g/L_g$.

Mode 3 [t_2–t_3]: At $t = t_2$, D_{P2} is turned off as i_{Cp} becomes zero. The switch voltage V_{P1} is clamped to $V_d + v_g/n$. The switch voltage V_{P2} is clamped to $V_{Cp} + V_d + v_g/n$. i_{Lm} and i_g keep decreasing linearly as in Mode 2.

Mode 4 [t_3–t_4]: At $t = t_3$, S_{P2} is turned on for transferring the energy stored in C_P to the grid. The absorbed leakage energy is recycled to the grid. The switch voltage V_{P1} is clamped to V_{Cp}. i_{Lm} and i_g keep decreasing linearly as in Mode 2.

From Mode 2 to Mode 4, the following current relations are obtained as $i_{Cs} = -i_{S1} - i_{S3} = -i_{S2} - i_{S4}$ and $i_g = i_{S2} - i_{S1} = i_{S4} - i_{S3}$ with respect to the nodes P, N, A, and B. Next, the switching cycle begins as S_{P1} is turned on, and S_{P2}, S_{S1}, and S_{S4} are turned off. For the negative grid cycle, S_{S1} and S_{S4} are always turned on. S_{S2} and S_{S3} operate complementary to S_{P1}. The operation principle for the negative grid cycle is not described here, because it can be explained analogously as the operation principle for the positive grid cycle.

2.2. Active Clamp Circuit

In the active clamp circuit, S_{P2} is turned on for a short period before S_{P1} is turned on. The absorbed leakage energy is recycled as the energy stored in C_P is transferred to the grid. Figure 6 shows the detailed timing diagrams for $V_{gate,P1}$, $V_{gate,P2}$, and i_{Cp}. T_{ON} is the turn-on time of S_{P1}. T_{OFF} is the turn-off time of S_{P1}. T_{DP2} is the turn-on time of D_{P2}. T_{SP2} is the turn-on time of S_{P2}. As S_{P2} is turned on, the capacitor current i_{Cp} can be represented as:

$$i_{Cp}(t) = -\frac{V_{Cp} - V_d - |v_g|/n}{L_{lk}}t. \tag{1}$$

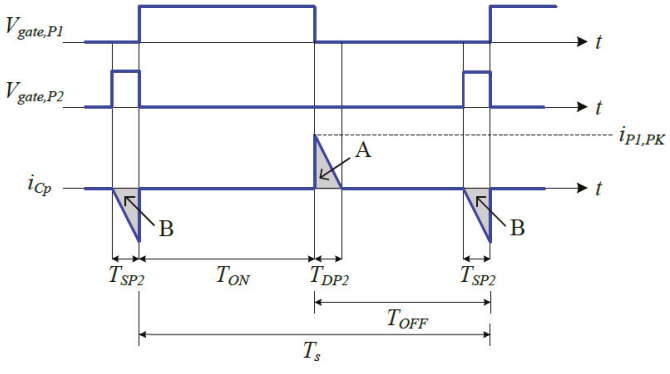

Figure 6. Detailed timing diagrams for $V_{gate,P1}$, $V_{gate,P2}$, and i_{Cp}.

By the charge balance for the capacitor C_P during T_s, the areas A and B for two current waveforms should be equal to:

$$\frac{1}{2}i_{P1,PK}T_{DP2} = \frac{V_{Cp} - V_d - |v_g|/n}{2L_{lk}}T_{SP2}^2 \tag{2}$$

where $i_{P1,PK}$ is the peak value of i_{P1}. Supposing that $T_{DP2} = T_{SP2}$, the capacitor voltage V_{Cp} is represented as:

$$V_{Cp} = V_d + \frac{|v_g|}{n} + \frac{L_{lk}i_{P1,PK}}{T_{SP2}}. \tag{3}$$

Also, the circulating energy E_{Cir} during T_{SP2} is represented as:

$$E_{Cir} = \frac{(V_{Cp} - V_d - |v_g|/n)^2}{2L_{lk}} T_{SP2}^2. \quad (4)$$

The circulating energy E_{Cir} will be smaller as T_{SP2} is getting shorter. However, in the active clamp method using the complementary switching scheme [12], the circulating energy is related with the turn-off time T_{OFF}, which is much longer than T_{SP2}. Thus, the non-complementary switching scheme results in higher power efficiency by reducing the circulating energy.

2.3. Synchronous Rectification with SiC MOSFETs

Figure 7 shows the detailed switching circuit diagrams for the operation principle of the secondary circuit for the positive grid cycle. Figure 7a shows the switching circuit diagram of the secondary circuit in the previous inverter in Figure 1. i_g freewheels through the body diodes D_{S1} and D_{S4} when S_{P1} is turned off. When S_{P1} is turned on, D_{S1} and D_{S4} are not turned off immediately because of the slow reverse recovery process [11]. Then, the diode reverse recovery currents cause high voltage spikes across D_{S1} and D_{S4}. Also, the diode reverse recovery currents are transferred to the primary circuit through the transformer, which causes high current spikes for S_{P1}. On the other hand, Figure 7b shows the switching circuit diagram of the secondary circuit in the proposed inverter. When S_{P1} is turned off, S_{S1} and S_{S4} are turned on. i_g freewheels through the MOSFET channels instead of the body diodes, which minimizes the conduction of the body diodes. When S_{P1} is turned on again, S_{S1} and S_{S4} are turned off without the reverse recovery process of the body diodes.

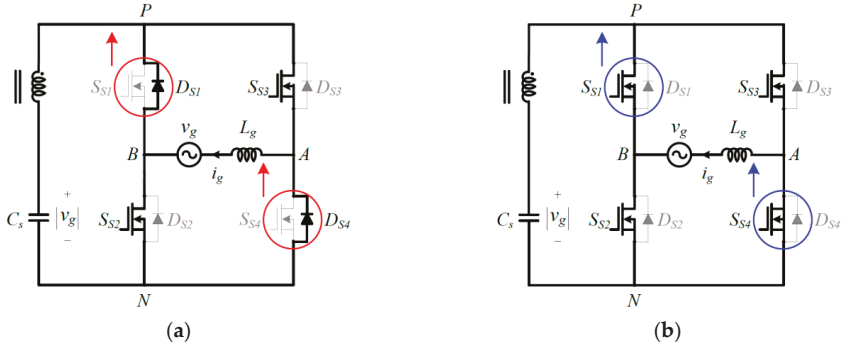

Figure 7. Detailed switching circuit diagrams for the operation principle of the secondary circuit for the positive grid cycle: (**a**) previous inverter; and (**b**) proposed inverter.

When S_{S1} and S_{S4} are turned off, the voltage across the secondary winding of T is $nL_mV_d/(L_m + L_{lk})$. The switch voltage stresses V_{S1} and V_{S4} are represented as:

$$V_{S1} = V_{S4} = |v_g| + \frac{nL_mV_d}{L_m + L_{lk}}. \quad (5)$$

The switch voltage stresses V_{S2} and V_{S3} are identical to V_{S1} and V_{S4} in Equation (5). Suppose that the system parameters are given as V_d = 48 V, n = 4.5, and v_g = 220 V_{rms} with negligible leakage inductor. The switch voltage stress is approximately calculated as 527 V without considering any voltage oscillations. Practically, the use of high voltage (>700 V) MOSFETs is inevitable to withstand the switch voltage stresses for a high switching frequency. However, when Si MOSFETs are adopted for $S_{S1} \sim S_{S4}$, the proposed inverter will suffer from high conduction losses due to the high on-state resistances of Si MOSFETs. Thus, the SiC MOSFET is an attractive alternative to the Si MOSFET for high-frequency and high-voltage applications. Due to its advantages over Si MOSFETs such as

its wider bandgap and higher electric field capacity, it improves the switching performance of the proposed inverter, increasing the power efficiency.

2.4. Control Strategy

Supposing that the leakage inductor is negligible, the volt-second balance for L_g during T_s gives the following voltage equation as:

$$nV_dDT_s - v_g(1-D)\,T_s = 0 \tag{6}$$

where D is the duty cycle of S_{P1}. By rearranging Equation (6), we have the relation between v_g and V_d as:

$$\frac{v_g}{V_d} = \frac{nD}{1-D}. \tag{7}$$

Assuming no power losses in the inverter circuit, we have the relation between i_d and i_g as:

$$\frac{i_d}{i_g} = \frac{nD}{1-D} \tag{8}$$

where i_d is the input current. Suppose that C_P keeps the charge balance, i_d is considered as i_{P1} during T_s. Then, the following current relations are represented as:

$$i_d = i_{P1} = kDi_{Lm} \tag{9}$$

where k is a proportional factor. From equations (8) and (9), we have the relation between i_{Lm} and i_g as:

$$i_{Lm} = \frac{n}{k(1-D)}i_g. \tag{10}$$

The average voltage for L_m during T_s can be represented with respect to the deviation Δi_{Lm} of i_{Lm} as:

$$V_dD - \frac{|v_g|}{n}(1-D) = L_m\frac{\Delta i_{Lm}}{T_s}. \tag{11}$$

From Equation (11), D can be represented as:

$$D = \frac{|v_g|}{|v_g| + nV_d} + \frac{n}{|v_g| + nV_d}\left(\frac{L_m\Delta i_{Lm}}{T_s}\right). \tag{12}$$

By using equations (7) and (10), D in Equation (12) can be written as:

$$D = D_n + D_c = \frac{|v_g|}{|v_g| + nV_d} + \frac{nL_m}{kV_dT_s}\Delta i_g \tag{13}$$

where D_n is the nominal duty cycle, and D_c is the control duty cycle as:

$$\begin{array}{c} D_n = \frac{|v_g|}{|v_g|+nV_d} = \frac{V_g|\sin\omega t|}{V_g|\sin\omega t|+nV_d}, \\ D_c = \frac{nL_m}{kV_dT_s}\Delta i_g. \end{array} \tag{14}$$

V_g is the absolute peak value of v_g. ω is the angular frequency of v_g. Supposing that v_g is measured exactly with a phase-locked loop (PLL) [17], D_n plays the role of providing the nominal voltage compensation. By using D_n, the non-linear system in Equation (11) is transformed to the first-order linear system, which can be controlled by the control duty cycle D_c. In order to regulate

the grid current i_g with low harmonic currents, D_c is implemented by a proportional-resonant (PR) control [18] whose ideal transfer function $C_{PR}(s)$ is:

$$C_{PR}(s) = k_p + \frac{k_r s}{s^2 + \omega^2} \tag{15}$$

where k_p and k_r are the PR control gains, respectively. However, it is unable to realize the PR controller in Equation (15) with an infinite gain. Thus, the following non-ideal transfer function is adopted in practice as:

$$C_{PR}(s) = k_p + \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + \omega^2} \tag{16}$$

where ω_c is the angular frequency at the cutoff frequency of the controller. In addition, the harmonic compensators can be added to the PR controller to minimize the harmonic currents for the selective harmonic frequencies [19]. Its transfer function $C_{HC}(s)$ is expressed as:

$$C_{HC}(s) = \sum_{h=3,5,7} \frac{2k_{rh}\omega_c s}{s^2 + 2\omega_c s + (h\omega)^2} \tag{17}$$

where h is the harmonic order and k_{rh} is the resonant control gain for each harmonic frequency. Since the third, fifth, and seventh harmonics are significant under the grid environment, the third to seventh harmonic compensators are implemented. The harmonic compensators provide high gains at the selected harmonic frequencies, helping minimize the steady-state error and the disturbance by the selected frequency components. Figure 8 shows the control block diagram of the proposed inverter. I^*_g is the peak magnitude of the current reference i^*_g. The duty cycle D is generated by summing D_n and D_c.

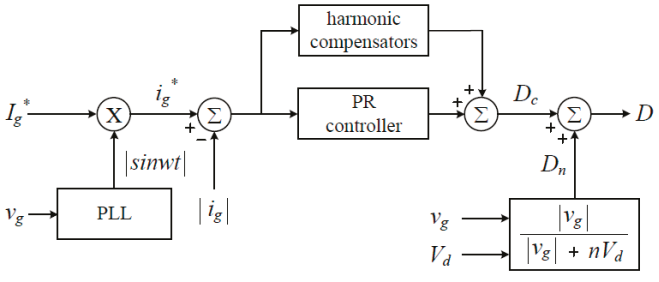

Figure 8. Control block diagram of the proposed inverter.

3. Experimental Results

A 220-W prototype system has been designed and tested to evaluate the performance of the proposed inverter. Table 1 shows the system parameters and the circuit components. As a SiC MOSFET, UJC1206k (UnitedSiC) has been used for $S_{S1} \sim S_{S4}$. As a digital signal controller, dsPIC30F6015 (Microchip) has been used for implementing the current controller and generating the duty cycle signals for all of the power switches. Figure 9 shows the picture of the prototype system. The prototype system includes the power circuit and the control circuit. Even though it is not optimized for the commercialized level, it is expected that the proposed inverter could achieve high power density if it is implemented with advanced devices such as gallium nitride (GaN) devices [20] and planar transformers [21].

Table 1. System parameters and circuit components.

Symbol	Quantity	Value
V_d	dc input voltage	48 V
v_g	grid voltage	60 Hz/220 V_{rms}
f_s	switching frequency	50 kHz
L_m	magnetizing inductor	60 μH
L_{lk}	leakage inductor	0.5 μH
N_P	primary winding turns	14
N_S	secondary winding turns	63
C_P	clamp capacitor	1.0 μF
S_{P1}, S_{P2}	primary swiches	IXFK150N30P3
C_S	secondary capacitor	1.0 μF
S_{S1} ~ S_{S4}	secondary switches	UJC1206K
L_g	filter inductor	2.0 mH

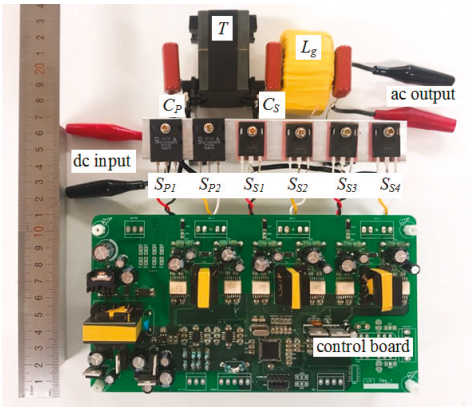

Figure 9. Picture of the prototype system.

The proposed inverter has been simulated to verify its operation principle. It has been simulated by the physical security information management (PSIM) software for the system parameters in Table 1. Figure 10 shows the simulation waveforms of the proposed inverter. The steady state operation of the proposed inverter can be verified from Figure 10a–d. Figure 10e,f show the simulation waveforms of the proposed inverter in the transient state condition. Figure 10e shows v_g and i_g as the output power changes from 110 W to 220 W. Figure 10f shows v_g and i_g as the output power changes from 220 W to 110 W.

Figure 11 shows the experimental waveforms of the previous inverter in Figure 1. The previous inverter has been designed and tested for the same system parameters as the proposed inverter. It uses the same circuit components in Table 1, except that STW40N95K5 (STMicroelectronics), as a Si MOSFET, has been adopted for S_{S1} ~ S_{S4}. Figure 11a shows the gate signal $V_{gate,P1}$ and the switch voltage V_{P1} for S_{P1}. When S_{P1} is turned off, V_{P1} has a high voltage spike, which results from the energy stored in the transformer leakage inductor. Figure 11b shows the gate signal $V_{gate,P1}$ and the switch current i_{P1} for S_{P1}. When S_{P1} is turned on, i_{P1} has a high current spike, which results from the reverse recovery current of the body diodes in the secondary circuit.

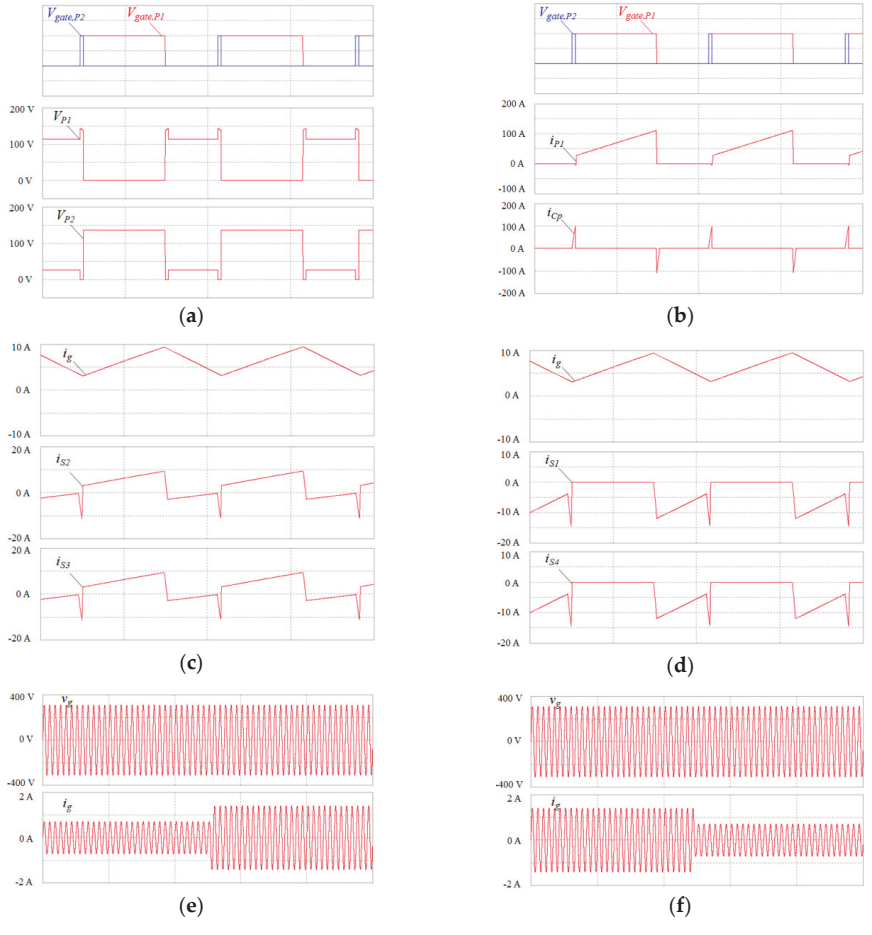

Figure 10. Simulation waveforms: (**a**) $V_{gate,P1}$, $V_{gate,P2}$, V_{P1}, and V_{P2}; (**b**) $V_{gate,P1}$, $V_{gate,P2}$, i_{P1}, and i_{Cp}; (**c**) i_g, i_{S2}, and i_{S3}; (**d**) i_g, i_{S1}, and i_{S4}; (**e**) v_g and i_g from 110 W to 220 W; and (**f**) v_g and i_g from 220 W to 110 W.

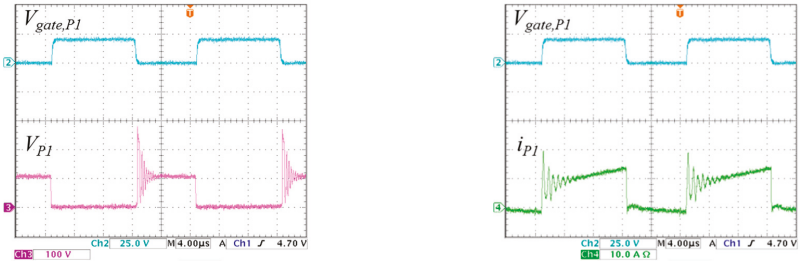

Figure 11. Experimental waveforms of the previous inverter: (**a**) $V_{gate,P1}$ and V_{P1}; and (**b**) $V_{gate,P1}$ and i_{P1}.

Figure 12 shows the experimental waveforms of the proposed inverter. Figure 12a shows $V_{gate,P1}$, $V_{gate,P2}$, and V_{P1}. Figure 12b shows $V_{gate,P1}$, $V_{gate,P2}$, and V_{P2}. As shown in Figure 12a,b, V_{P1} and

V_{P2} are maximally clamped to the capacitor voltage V_{Cp}. Figure 12c shows $V_{gate,P1}$, $V_{gate,P2}$, and i_{P1}. The switch current i_{P1} in Figure 12c has lower current spike than the switch current i_{P1} in Figure 11b because of the synchronous rectification of the secondary circuit. Figure 12d shows $V_{gate,P1}$, $V_{gate,P2}$, and i_{Cp}. It is observed that the capacitor charging and discharging currents are well balanced in the proposed inverter.

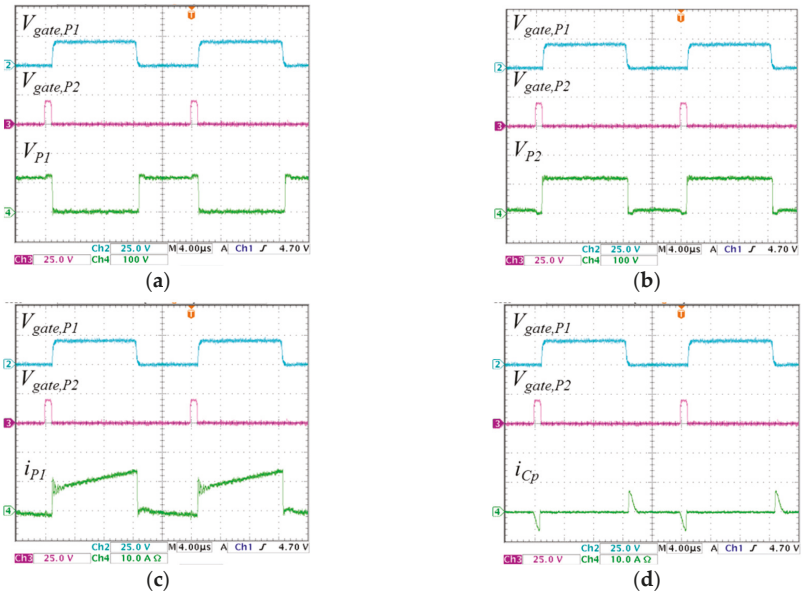

Figure 12. Experimental waveforms of the proposed inverter: (**a**) $V_{gate,P1}$, $V_{gate,P2}$, and V_{P1}; (**b**) $V_{gate,P1}$, $V_{gate,P2}$, and V_{P2}; (**c**) $V_{gate,P1}$, $V_{gate,P2}$, and i_{P1}; and (**d**) $V_{gate,P1}$, $V_{gate,P2}$, and i_{Cp}.

Figure 13 shows the experimental waveforms in the secondary circuit for the positive grid cycle. Figure 13a shows V_{S1} in the previous inverter. It is observed that there is high voltage oscillation across S_{S1}, which results from the slow reverse recovery process of the body diode of the Si MOSFET. Figure 13b shows $V_{gate,S1}$ and V_{S1} in the proposed inverter. With synchronous rectification, the SiC MOSFET channel has been used for the rectification. It is shown that voltage oscillation across S_{S1} has been much alleviated due to the fast switching operation of the SiC MOSFET. The switch currents i_{S1}, i_{S2}, i_{S3}, and i_{S4} are shown from Figure 13c–f with respect to i_g in the proposed inverter.

Figure 14 shows the experimental waveforms of the proposed inverter. Figure 14a shows v_g and i_g as the proposed inverter supplies 110 W into the grid. Figure 14b shows v_g and i_g as the proposed inverter supplies 220 W into the grid. As i_g is in phase with v_g, the power factor is measured as 0.99 in Figure 14.

Figure 15 shows the measured power efficiency curves. The curve A shows the measured power efficiency of the previous inverter. It has achieved the peak efficiency of 93.5% at the rated power. The curve B shows the measured power efficiency of the proposed inverter when the synchronous rectification has been implemented without the active clamp circuit. The proposed inverter has improved the power efficiency, achieving the peak efficiency of 94.2% at the rated power. The curve C shows the measured power efficiency of the proposed inverter when both active clamp and synchronous rectification techniques have been implemented. The proposed inverter has achieved the peak efficiency of 95.0% at the rated power by using active clamp and synchronous rectification techniques.

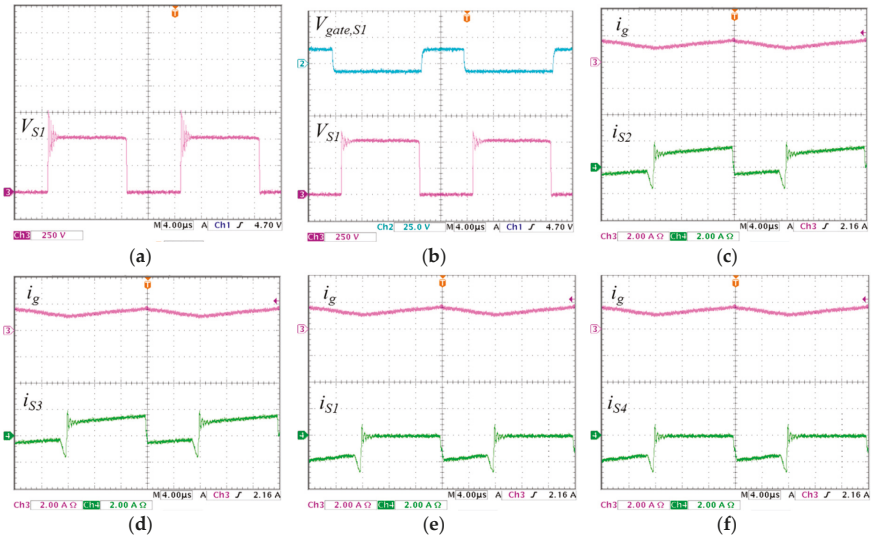

Figure 13. Experimental waveforms in the secondary circuit for the positive grid cycle: (**a**) V_{S1} in the previous inverter; (**b**) $V_{gate,S1}$ and V_{S1} in the proposed inverter; (**c**) i_g and i_{S2} in the proposed inverter; (**d**) i_g and i_{S3} in the proposed inverter; (**e**) i_g and i_{S1} in the proposed inverter; and (**f**) i_g and i_{S4} in the proposed inverter.

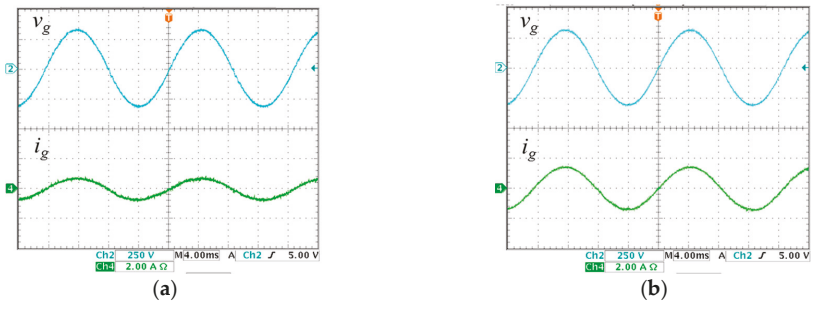

Figure 14. Experimental waveforms of the proposed inverter: (**a**) v_g and i_g as the proposed inverter supplies 110 W into the grid; and (**b**) v_g and i_g as the proposed inverter supplies 220 W into the grid.

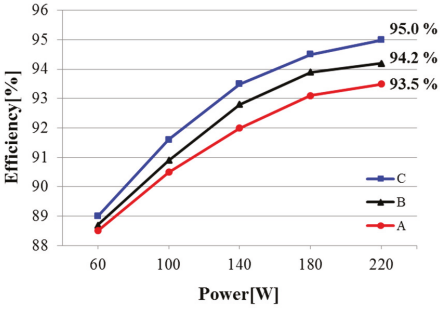

Figure 15. Measured power efficiency curves.

Figure 16a shows the measured power efficiency curves up to 440 W. The prototype system has shown the peak efficiency of 95.0% at 220 W. The efficiency decreases gradually as the output power level goes up from 300 W to 440 W. The prototype system has achieved the efficiency of 94.3% at 440 W. Figure 16b shows the measured power efficiency curves for 50 kHz and 100 kHz, respectively. As the switching frequency increases, the power efficiency decreases because of the switching losses. In order to improve the power efficiency and the power density further, the circuit design scheme should be advanced by considering the GaN devices [20] and the planar transformers [21] for megahertz operations.

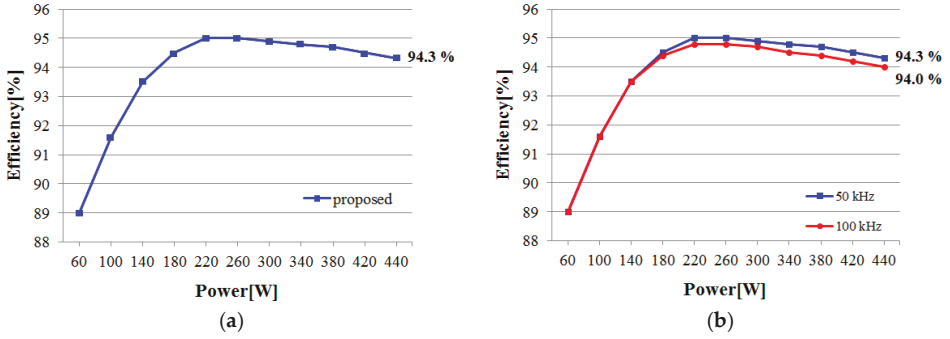

Figure 16. Measured power efficiency curves: (**a**) power efficiency curves up to 440 W; and (**b**) power efficiency curves for different switching frequencies.

4. Conclusions

This paper has proposed a high-efficiency zeta inverter using active clamp and synchronous rectification techniques for single-phase grid-connected applications. The operation principle of the proposed inverter has been described. The active clamp and synchronous techniques adopted in the proposed inverter have been explained. The non-complementary switching scheme has been applied to the active clamp circuit. It effectively reduces the switching losses and circulating current in the primary circuit. The synchronous rectification with SiC MOSFETs alleviates switching losses in the secondary circuit. The control strategy for the CCM operation of the proposed inverter has been presented. A 220-W prototype system has been designed and tested to evaluate the performance of the proposed inverter. Experimental results have shown that the proposed inverter has improved the power efficiency by reducing switching losses, compared to the previous inverter.

Author Contributions: W.-Y.C. managed the project and wrote the manuscript. M.-K.Y. performed the experiments, analyzed the data, and edited the manuscript.

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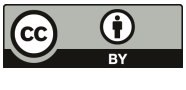

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Analysis, Modeling, and Control of Half-Bridge Current-Source Converter for Energy Management of Supercapacitor Modules in Traction Applications

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Abstract: In this work, an in-depth investigation was performed on the properties of the half-bridge current-source (HBCS) bidirectional direct current (DC)-to-DC converter, used to interface two DC-link voltage sources with a high-voltage-rating mismatch. The intended implementation is particularly suitable for the interfacing of a supercapacitor (SC) module and a battery stack in a hybrid storage system (HSS) for automotive applications. It is demonstrated that the use of a synchronous rectification (SR) modulation scheme benefits both the power-stage performance (in terms of efficiency and reliability) and the control-stage performance (in terms of simplicity and versatility). Furthermore, an average model of the converter, valid for every operating condition, is derived and utilized as a tool for the design of the control system. This model includes the effects of parasitic elements (mainly the leakage inductance of the transformer) and of the converter snubbers. A 3 kW prototype of the converter was used for experimental validation of the converter modeling, design, and performance. Finally, a discussion on the control strategy of the converter operation is included.

Keywords: hybrid storage systems; power electronic converters; half-bridge current-source converters; supercapacitors

1. Introduction

Among electrical energy storage passive devices, Supercapacitors (SC) outstand as one of the preferred solutions when very high power densities and long life cycles are required. These features also are used in Hybrid Storage Systems (HSS), where SC can be combined with other distinct storage devices, such as electrochemical batteries or fuel cells [1–19]. In these hybrid systems, SC usually operate as power sources, as they provide the required peak power commanded by the load. In turn, the combined device (e.g., the electrochemical battery) work as an energy source, providing the long-term energy required for the given operating conditions, such as islanding operation or back-up energy support after a fault ride-through sequence, etc.

The integration of SC into HSS has been covered extensively in the current state-of-the-art, by analyzing the modeling and operation of power electronic topologies, by proposing control algorithms and methods, and by investigating hierarchical energy management systems [20–27]. Although being the simplest and most inexpensive scheme, the direct connection between the storage systems prevents to fully exploit the high charging and discharging instant power ratings of SCs. This scheme also prevents a tight control on the independent power flows shared among the energy storage devices [28,29]. Therefore, practically every implemented solution found in the technical literature includes a bidirectional direct current (DC)-to-DC converter. These solutions can be categorized into

three different classes: a series connection of the storage devices [6,7], a cascaded connection of the storage subsystems [8,9], and finally a parallel connection of the storage elements [10–12]. From a detailed analysis of the technical literature, the parallel configuration, depicted in Figure 1, outstands as the most practical solution that allows a full control of the power flow sharing scheme required for the application, as well as a complete SC voltage-range utilization, despite that in this case the bidirectional converter needs to be rated for the peak value of the required power [13,14].

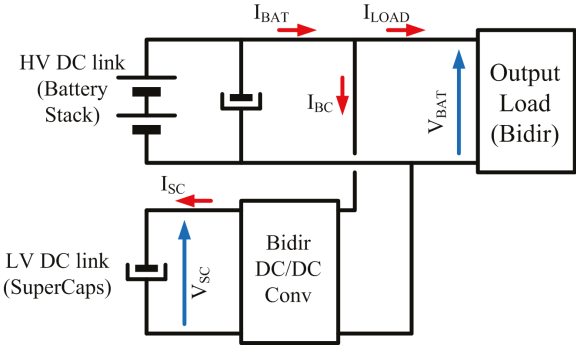

Figure 1. Parallel configuration for interfacing supercapacitors (SCs) with primary energy source (battery stack).

The bidirectional boost converter is formed by the typical connection present in a single phase leg of an inverter. It has two transistors, a series inductor connected between the mid-point of the transistors and the output, plus two capacitors intended to filter the input and the output of the converter. This scheme is generally adopted as the simplest and best-known solution. With this configuration, the peak power ratings required by most applications can be ensured by an assembly of few SC connected in series. This structure is also beneficial in terms of balancing the voltage at each SC module in the assembly. As a consequence, the SC side voltage ratings of the converter are usually much smaller than the voltage levels found at the DC-link. In addition, upon transient variations, the SC side voltage must allow variations from 80 to 20% of the SC ratings, in order to use efficiently the stored energy at the device. On the other side, the voltage at the DC-link may remain almost constant, as to optimize the full system design and operation. Hence, the range of the voltage gain between the input and the output of the bidirectional converter can typically surpass ratios of 1 to 10 and above, depending on the application.

Therefore, the boost converter is no longer a suitable solution, and so alternative topologies that allow for a high voltage gain need to be analyzed. Among these options, the most widely used include the use of a High-Frequency (HF) transformer [30–38]. Studies on the simplest isolated configurations, such as the bidirectional versions of the Flyback converter, the Forward Current-Source converter, the Push-Pull Current-Source converter, and the Half-Bridge Current-Source (HBCS) converter have been carried out [33–35]. These comparative analyses were carried out on the basis of the number of components, the switch stresses at the converters, and other figures of merit such as the utilization factor of the magnetic elements. This comparison shows how the bidirectional HBCS DC-to-DC converter is most suitable in low to medium power applications, for structures that directly interface the storage devices. Thus, the HBCS topology is of interest in HSS with storage devices arranged as shown in Figure 1 with the battery directly forming the DC bus at the converter. This is particularly interesting in traction applications, for which the weight and size of the full system are major concerns, and variable DC-link systems are considered as a suitable option [28,29].

When a given power profile is demanded by the load, the SC converter must react very quickly, in order to prevent the battery from providing the transient power. Given the current-source behavior

of the low-voltage side of the HBCS converter, and provided that a tight, fast current control is implemented by generating the adequate SC current reference, the power delivered by this converter can successfully protect the battery from delivering fast, high power peaks, thus enhancing the performance and increasing the reliability of the full system. Other works have investigated the potential use of power converters for interfacing both the battery and the SC module, leading to more complex topologies and control methods [20,24,27,39].

The HBCS topology was introduced in an application to HSS in [11], but the power ratings of the laboratory demonstrator was only 100 W. Later, a 3 kW setup was reported in [35], being able to operate in open-loop, steady-state, both charging and discharging operation modes. A measured efficiency beyond 90% was then reported for the full range of operation. The authors in [35] analyzed the static gain of the HBCS converter, using conventioal switching patterns. Furthermore, they considered neither the modeling nor the control stage for closed-loop operation of the converter. On the other hand, the authors of [40,41] showed preliminary research conducted to unify the transfer function of the converter acting in a bidirectional operation scheme, as well as the dynamic behavior.

The present work investigates more in depth the performance of the HBCS converter in vehicle applications. Firstly, a unified control strategy of the converter, on the basis of a synchronous rectification switching pattern, is provided. By using this pattern, the converter can be controlled with a simple, unique control law valid for every operating condition. This allows the implementation of a full bidirectional SC current control, thus enabling a fast, tight power flow control in the storage system. Once this switching pattern is established and validated, the main contribution of this work is the extension of previously existing circuital models of the converter by including non-ideal effects of the parasitic elements in the transformer of the converter, as well as the dissipative effect of the losses in the system. The performance of the proposed model was validated through simulations and experiments carried out on a 3 kW laboratory prototype. The proposed model was also compared against the simplified ideal model. Finally, this work discusses the control strategy that can be implemented in the converter. A basic HBCS current loop was analyzed, designed, and implemented, with the aim to demonstrate its feasibility; finally, a discussion on the possibilities of the high-level control strategy is also included at the end of the paper.

This paper is organized as follows. Section 2 presents the conventional modulation strategy implemented in the state-of-the-art for the HBCS converter. After that, Section 3 evaluates the Synchronous Rectification (SR) scheme in the converter operation, considering both the charging and discharging modes of operation. It also demonstrates experimentally the benefits of SR operation for this topology. Section 4 further discusses the implications of SR in terms of the simplification of the control of the converter; most importantly, this section provides an averaged model of the HBCS converter, suitable to aid in the design of the control stage. Also, this model is validated through simulations. Subsequently, in Section 5 the current control algorithm is discussed and tested through simulations. This section also deals with the overall control scheme of the system. Section 6 validates the full model and the control scheme outlined in the previous sections by showing experimental results obtained with a laboratory prototype of a HBCS converter. Finally, Section 7 discusses the conclusions of the research and proposes some future developments.

2. Special Characteristics of the HBCS Converter

Figure 2 shows the HBCS converter. Because this converter is a bidirectional topology, no predefined input or output are established. For the coming discussion, the SC side is also referred to as the Low-Voltage (LV) side, signifying that this side generally has the lower of the rated voltages involved in the analysis. On the other hand, the alternate energy source (i.e., battery) and the DC-link are referred to as the High-Voltage (HV) side.

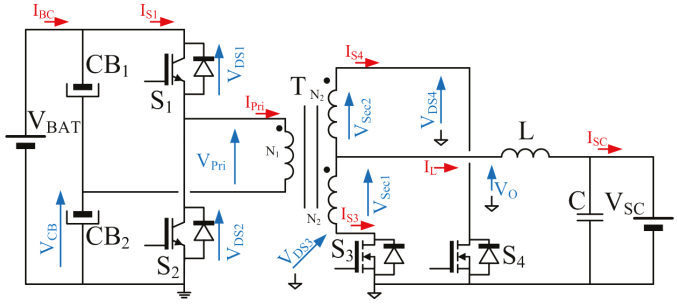

Figure 2. Layout of Half-Bridge Current-Source (HBCS) bidirectional converter. The references for the current and voltage considered for the analysis are shown.

The modulation scheme for the HBCS converter, as presented in [35], is obtained by shifting the command pulse waveforms of each switch in the primary- or secondary-side by 180º. Initially, the control parameters implemented at both charging and discharging operation modes were different. In charging mode, where the energy flows to the SC from the DC link side, switches S_3 and S_4 remain always turned off. This forces the current to flow only through the diodes of S_3 and S_4. Figure 3 shows the main current and voltage instant waveforms of the converter for charging (a) and discharging (b) modes. The switching pattern is defined by establishing the gate-to-emitter voltages of switches S_1 to S_4, denoted as V_{GE1}–V_{GE4}, respectively. The rest of the waveforms are consistent with the references in Figure 2. The modulation of switches S_1 and S_2 (Figure 3a) is carried out by shifting by 180º the control pulses, considering a given duty ratio, D:

$$D = \frac{T_{S1\,ON}}{T_S}, \tag{1}$$

where $T_{S1\,ON}$ is the interval when switch S_1 remains turned on and T_S is the switching period. In order to avoid a simultaneous conduction of switches S_1 and S_2 at the battery side, and given that the switching pattern requires a fixed 180° phase shift between the firing signals of V_{GE1} and V_{GE2}, D is restricted to $0 < D < 0.5$. The voltage gain between the LV and HV sides, G_{CHRGE}, is

$$G_{CHRGE} = \frac{V_{SC}}{V_{BAT}} = D \cdot \frac{N_2}{N_1}, \tag{2}$$

where N_1 and N_2 are the primary- and secondary-side number of turns of the HF transformer, respectively; V_{SC} is the voltage across the SC; and V_{BAT} is the DC-link voltage, that is, the battery voltage according to its state of charge. The magnetizing inductance of the transformer is neglected, because it is assumed that it is very high.

Figure 4 shows the current paths for the different switching modes of the converter, during the SC charging operation scheme. When switch S_1 is turned on and S_2 is turned off (Figure 4a), a positive current I_P flows flows through the primary side, considering the references in Figure 2. Current flows through the portion of the secondary winding connected to switch S_3, the output filter, and the SC; thus, the anti-parallel diode of switch S_3 carries the secondary-side current. Figure 4b, in turn, shows the switching mode when both transistors S_1 and S_2 are turned off. The inductor current I_L splits equally between the two parts of the secondary winding, flowing through the anti-parallel diodes of S_3 and S_4. Finally, Figure 4c depicts the current paths when S_2 is turned on and S_1 is turned off. This mode is similar to that shown in Figure 4a but considers the 180° phase shift between S_1 and S_2.

During the discharging mode, the energy flows back to the DC-link from the the SC. In this case, the switches under control are S_3 and S_4, while S_1 and S_2 are kept continuously turned off. Again, the modulation of S_3 and S_4 is implemented through a 180º shifting scheme, while the turn-on intervals

are kept equal. Figure 3b shows the key waveforms obtained for this operation mode. The independent parameter for this mode, D', is defined as:

$$D' = \frac{T_{S3\ ON}}{T_S}, \tag{3}$$

where $T_{S3\ ON}$ is the interval when S_3 is turned on. The constraint for this parameter is now $0.5 < D' < 1$, thus forcing an overlap in the conduction of S_3 and S_4. This overlapping is required because of the current-source behavior of the LV side of the converter. For this topology, unless at least one switch in the pair S_3–S_4 is turned on, an abrupt interruption of the current flowing through the inductor would lead to a dangerous overvoltage across the magnetic element, that might damage the converter. For the discharging operation mode, the voltage gain can be defined as:

$$G_{DISCHRGE} = \frac{V_{BAT}}{V_{SC}} = \frac{1}{1 - D'} \frac{N_1}{N_2}. \tag{4}$$

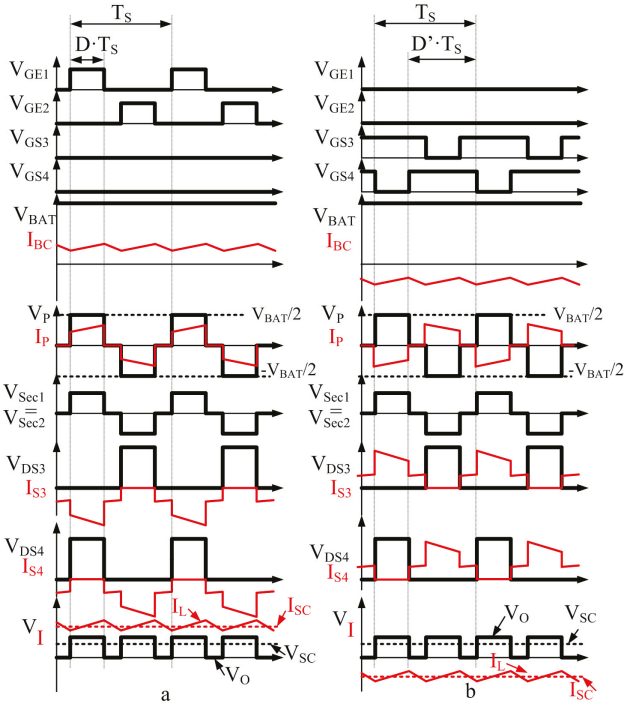

Figure 3. Main voltage (black) and current (red) waveforms of the half-bridge current-source (HBSC) for charging (**a**) and discharging (**b**) operation modes.

The switching modes for discharging the SC are represented in Figure 5. The current path when S_4 is turned off and S_3 is turned on is shown in Figure 5a. On the other hand, Figure 5b shows the current flowing through the switches when both S_3 and S_4 are turned on. Finally, it can be seen in Figure 5c how the current flows when switch S_4 is turned on and S_3 remains off. A close look at Figure 5a–c shows that the current paths are the same as those shown in Figure 4a–c, respectively, but with the directions of the currents reversed.

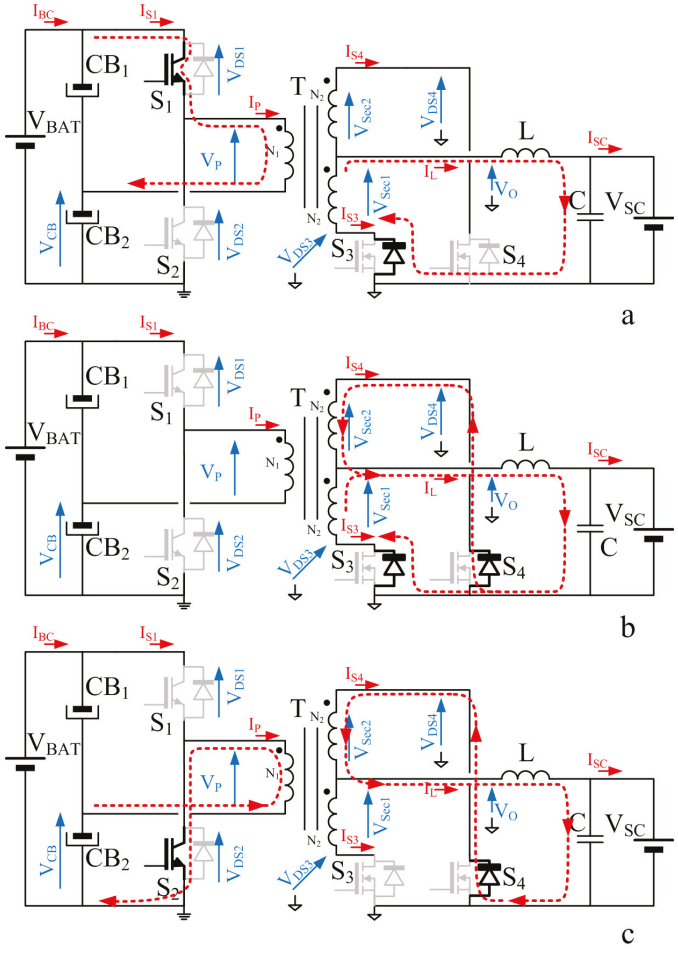

Figure 4. Switching modes of the half-bridge current-source (HBCS) converter operating during supercapacitor (SC) charging operation mode. (**a**) Switch S_1 on and switch S_2 off. (**b**) Both switches S_1 and S_2 off. (**c**) Switch S_1 off and switch S_2 on.

By using the control laws stated in Equations (2) and (4), both the charging and discharging control strategies can be easily designed. However, this modulation pattern requires the calculation of two independent control parameters, defined as the duty cycles of S_1 and S_3, depending on the operation mode under consideration, given by charging and discharging modes, respectively. This approach, though, yields to some issues at the boundary between these operation modes, given that the switches that must be controlled change abruptly. Therefore, if both control schemes are implemented independently, a smooth transition between modes of operation is prevented. However, this issue is easily avoided provided that SR is implemented. This SR pattern is introduced in the next section for the HBCS converter. The benefits for the control of the converter are discussed in the forthcoming sections.

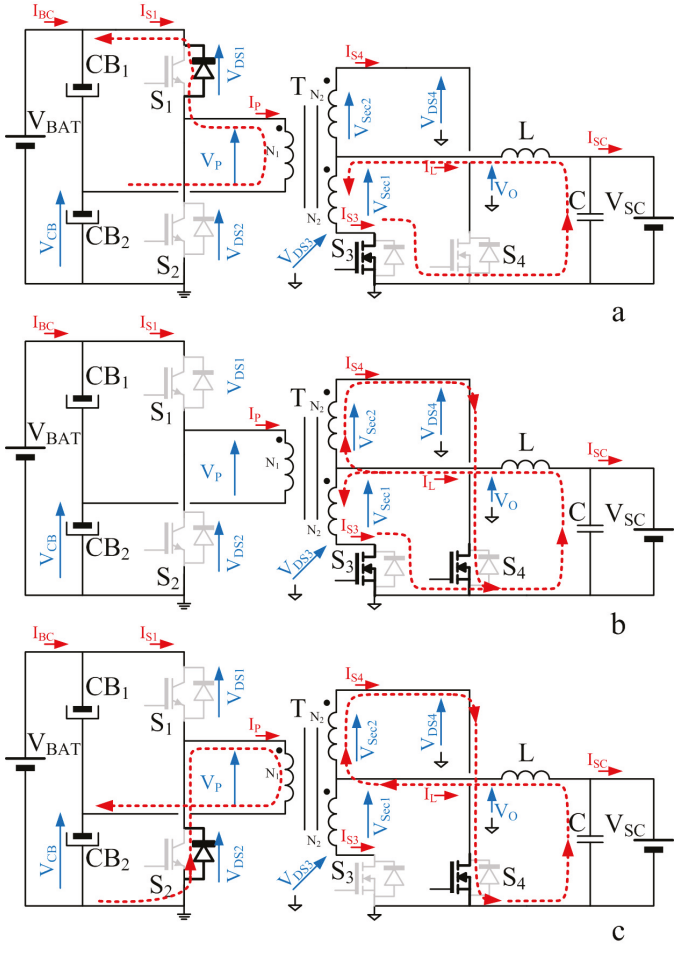

Figure 5. Switching modes of the half-bridge current-source (HBCS) converter operating during supercapacitor (SC) discharging operation mode. (**a**) Switch S_3 on and switch S_4 off. (**b**) Both switches S_3 and S_4 turned on. (**c**) Switch S_3 off and switch S_4 on.

3. Synchronous Rectification in the HBCS Converter

SR is a common strategy that establishes a given switching pattern for the switches in power electronic converters. Upon several conditions, it can decrease conduction losses, thus boosting the efficiency of the converter. This technique has already been described in the technical literature related with hybrid systems applications [36–38]. This technique takes advantage of the low on-state voltage of a MOSFET transistor, when compared to the forward voltage of its body diode. Given the equivalent series circuit of a diode, formed by a threshold voltage, V_{TH}, and a dynamic resistor, R_{DYN}, then the conduction losses, for the diode turned on, are given by:

$$P_{C-DIODE} \propto V_{TH} \cdot I_D + R_{DYN} \cdot I_D^2. \quad (5)$$

Moreover, the conduction losses in a MOSFET can be expressed as:

$$P_{C-MOSFET} \propto R_{DS\ ON} \cdot I_D^2, \tag{6}$$

where $R_{DS\ ON}$ is the drain-to-source on-resistance of the channel. As a result of an analysis of the equivalent circuit of the switch, the current tends to flow through the path with a lower voltage drop. In the HBCS converter depicted at Figure 2, S_3 and S_4 have already been implemented as MOSFET switches, with inherent anti-parallel body diodes. As a consequence, SR can be directly applied.

In order to validate the performance of the SR switching pattern, a reference design is considered for a 3 kW HBCS converter. The main characteristics of the setup are detailed in Table 1.

Table 1. Characteristics of half-bridge current-source (HBCS) design.

Parameter	Max.	Min.
SC voltage	45 V	25 V
HV DC-link voltage	350 V	
Switching frequency	20 kHz	
SC discharge-mode duty ratio	0.75	0.55
SC charge-mode duty ratio	0.45	0.25
Output power (SC disch. mode)	3 kW	1.6 kW
Output power (SC chrg mode)	3 kW	1.6 kW
SC current	65 A	−65 A
Transformer turns ratio	3.5:1:1	

Figure 6 shows a graphical representation of the expression of the drain-to-source voltage, V_{DS}, as well as the power dissipated through conduction losses, P_{COND}, both as a function of the current flowing through the drain of the transistor, I_D. These power and voltage values are given for both the transistor and diode elementary devices. For this study, the actual values given in the datasheets of the real components selected, in this case the $SKM121AR$ power MOSFET modules from SEMIKRON, have been used. The dotted black line shows the voltage at the MOSFET as a function of the current I_D. This line shows the typical load line of a resistive component. As a consequence, the power dissipated as a function of the I_D in the MOSFET is given by a quadratic relationship expressed in Equation (6), drawn as a filled black line in Figure 6. The voltage drop across the diode, in turn, is shown as an horizontal dotted gray line. The power dissipated in the diode, as a function of the current I_D, therefore follows a linear behavior, represented by a filled gray line. As can be seen, both power characteristics, those of the MOSFET and the diode, have an intersection point labeled as I_{LIM}. For I_D current values below I_{LIM}, the MOSFET losses are smaller than the diode losses, and therefore the synchronous rectification implies higher efficiencies compared to the standard switching pattern. For the real values of the devices under consideration, I_{LIM} is equal to

$$I_{LIM} = 70\ \text{A}. \tag{7}$$

From Table 1, the maximum value of the SC current, which is also the maximum currents allowed to flow through S_3 and S_4, has a value of 65 A. Therefore, and considering Figure 6, the conduction losses at the secondary side of the converter operating in charging mode will be decreased, provided that SR is implemented as the switching pattern. As a consequence, the whole efficiency of the converter will increase. It must be notice that in this case the switches at the DC link side have been implemented by means of IGBT switches. Therefore, and given that for this switch technology the current flowing from the emitter to the collector can only flow through the anti-parallel diode (and not through the transistor itself, as in the previous case), the use of a SR scheme during the SC discharge mode will not mean a decrease in the converter losses. In any case, a critical point for this analysis is to state that SR can still be used in this mode of operation without affecting the performance of the converter. This issue will be discussed in Section 4.

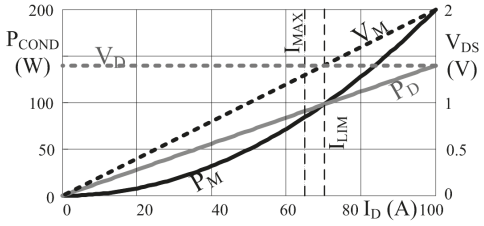

Figure 6. Drain-to-source voltage (V_{DS}, dashed lines) and conduction losses (P_{COND}, filled lines) for both diode conduction (gray) and MOSFET conduction (black), for the half-bridge current-source (HBCS) prototype.

A first set of experiments was carried to validate the feasibility of the SR switching pattern implementation in the HBCS converter. For this validation, and in order to register the steady-state operation of the converter, the setup was configured to supply a resistive load from a voltage source. The values of measured efficiencies in charging operation mode, for the standard and the SR schemes, are given in Figure 7. Three different resistive loads (1.0, 0.67 and 0.5 Ω, respectively), were used in the measurements. The voltage at the power source was kept constant at 300 V_{DC}. Due some practical constraints at the experimental setup, the voltage levels at the LV side were limited to three values, V_{SC} = 25 V, V_{SC} = 30 V, and V_{SC} = 34 V. From the plots at Figure 7, it can be deduced an increase in the converter efficiency in all cases.

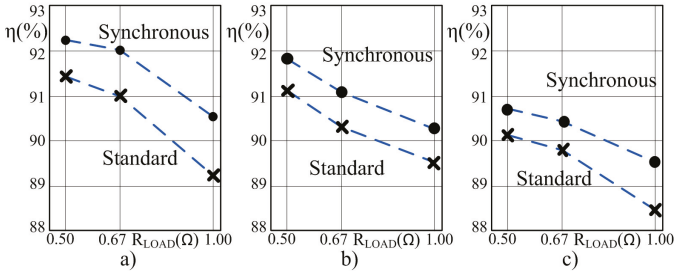

Figure 7. Graphical relationship of experimental efficiency measurements between standard and synchronous rectification switching schemes, as a function of load resistance. (**a**) V_{SC} = 25 V. (**b**) V_{SC} = 30 V. (**c**) V_{SC} = 34 V.

4. Full Model of the Converter under Synchronous Rectification

As a result of the use of SR, the HV and LV side switches, S_1–S_2 and S_3–S_4, present complementary control signals. In particular, the gating signals of S_3 and S_4, are the complementary signals of S_1 and S_2, respectively, as it was sketched in the waveforms shown in Figure 3a,b. This condition defines an obvious relationship upon SR scheme between the values of the parameter D of switches S_1–S_2 and D' of switches S_3–S_4. This can be expressed as

$$D = 1 - D' \quad . \tag{8}$$

As a result, a single, independent control parameter can be established for every operation mode in the converter, given that the remaining parameters are calculated automatically. This parameter is the duty ratio of switch S_1, noted by D. Equation (8), together with Equations (2) and (4), determines

a unique equation to define the voltage gain of the topology, G_{HBCS}. This equation is, as mentioned, true for every mode of operation and charging condition:

$$G_{HBCS} = \frac{V_{SC}}{V_{BAT}} = D \cdot \frac{N_2}{N_1}. \quad (9)$$

Thus, with SR, the control law turns out to be unique, regardless of the mode of operation.

Once the switching strategy is defined, an accurate model of the converter needs to be established in order to properly design the control system. The simplest averaged large-signal model for the converter is shown in Figure 8. This basic model has already been explored in the definition and implementation of a control strategy for the topology [40]. The basic model has been implemented considering ideal switching and reactive devices. For the average circuit, the transistors and the HF transformer have been modeled by the two dependent sources within the dashed frames at Figure 8. The output value of these sources depend on the duty ratio D and on the turns ratio of the transformer, N_2/N_1. Downstream from these, the second order L–C filter is present.

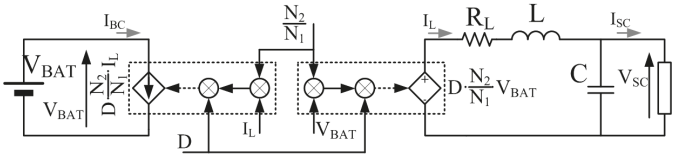

Figure 8. Large-signal averaged model based on ideal components.

In order to check this model, the performance of the circuit depicted in Figure 8 was compared with a full switching model of the HBCS converter, implemented in PSIM. In these simulations, a resistive load replaced the SCs, with the aim of having initial steady-state operation conditions. The dynamic behavior is obtained by imposing a small step in the duty ratio of the converter after reaching the steady state. In the tests shown in Figure 9, the step goes from 0.34 to 0.36. This picture shows the simulated waveforms of the output voltage (V_{SC}), input (I_{BC}) and output (I_{SC}) currents, and the inductor current (I_L), compared with their corresponding averaged values obtained from the basic model. The performance of the basic model differs significantly from the switching converter behavior. Even thought the natural frequency is mainly the same, there are two effects of mismatch in the behavior of the model. Firstly, the switching system is more damped than the dynamic response given by the model. Moreover, the equilibrium values after the transient are smaller in the switching circuit.

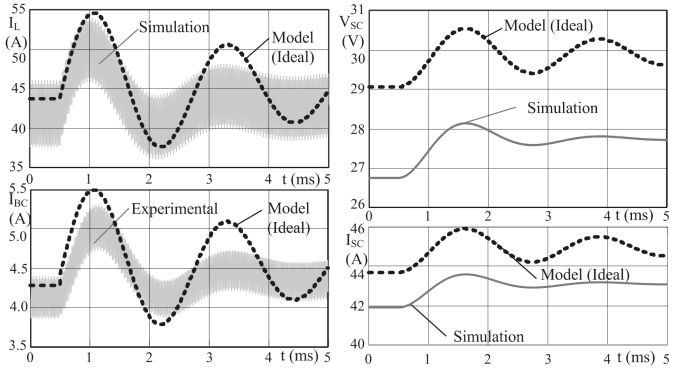

Figure 9. Simulation waveforms (gray) and averaged value of model based on ideal components (black), for filter current (I_L), load output current (I_{SC}), load voltage (V_{SC}), and input current (I_{BC}).

In order to solve this disagreement between the model and the switching circuit, an improved model has been developed. This model firstly accounts for the effects of the parasitic resistors of the transformer, the R_{DS} of the transistors at the HV side, and the snubbers. These effects are jointly modeled by a series resistance, R_{loss}, which adds a dissipative term in the model that contributes to increase the damping factor. However, the most significant effect is due to the leakage inductance of the transformer, depicted in Figure 10. Some waveforms are depicted in Figure 11 to describe the contribution of this leakage inductance in the full model. For simplicity in this analysis, the overall primary side leakage inductance is obtained as the sum of the measured primary- and reflected measured secondary-side leakage inductances.

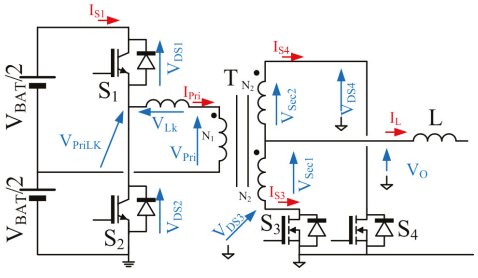

Figure 10. Half-bridge current-source (HBCS) converter equivalent circuit, including the overall leakage inductor at the primary side of the transformer.

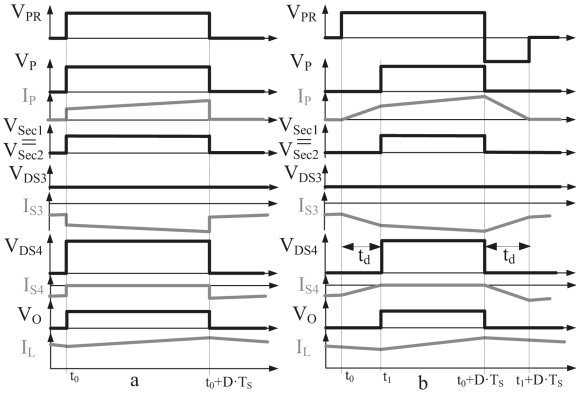

Figure 11. (**a**) Switching waveforms with ideal transformer. (**b**) Switching waveforms with overall leakage inductor at the primary side.

The waveform sequence starts when S_1 and S_2 are turned off, and thus there is no current flowing through the primary side of the transformer. In this situation, the output inductor current splits equally through the diodes at switches S_3 and S_4. At time t_0, S_1 is turned on, forcing the primary side voltage, V_P, to be half the voltage across the battery:

$$V_P = \frac{V_{BAT}}{2}. \tag{10}$$

The high inductance of the filter, L, causes I_L to keep flowing practically unchanged to the load. For the ideal transformer in Figure 11a, the current immediately flows through S_1, and thus the diodes

of S_3 and S_4 are instantly turned-off. As a consequence, the secondary side voltages at the transformer instantly are equal to:

$$V_{Sec1} = V_{Sec2} = \frac{V_{BAT}}{2}\frac{N_2}{N_1}. \tag{11}$$

Nonetheless, for the real transformer case depicted in Figure 10, the leakage inductance prevents the secondary side current to change instantly (Figure 11b). Upon this situation current keeps flowing through the secondary sides of the transformer, S_3 and S_4. The secondary side voltages remain null immediately after turning on S_1, and thus the voltage at the leakage inductor equals the primary-side voltage. This issue affects the operation of the system. For instance, in charging mode, both HV-side switches, S_1 and S_2, are in the off-state just before S_1 is turned on. It can be seen in Figures 2 and 3a that each diode at the secondary side carries half I_L, while the voltages at the primary side, V_P, and at the common node of the secondary windings, V_O, are null:

$$I_{S3} = I_{S4} = -\frac{I_L(t)}{2} = -\frac{I_L}{2}, \tag{12}$$

$$V_0 = 0, \tag{13}$$

$$V_P = 0. \tag{14}$$

Equation (12) describes as well that the inductor current is considered as constant within a switching interval. When S_1 turns on at t_0, and given that current keeps on flowing through the LV side diodes, then the voltage V_P does not vary. Instead, because V_{DS1} equals zero, the voltage at the primary side of the real transformer (i.e., considering the parasitic inductance), V_{PR}, equals half the voltage at the battery:

$$V_{PR} = \frac{V_{BAT}}{2}. \tag{15}$$

Therefore, the values of the voltage across the leakage inductor, V_{Lk}, and the current at the primary side of the transformer, I_{Lk}, can be calculated as:

$$V_{Lk} = \frac{V_{BAT}}{2}, \tag{16}$$

$$I_{Lk} = I_{PR} = \frac{1}{L_{Lk}}\frac{V_{BAT}}{2} \cdot t. \tag{17}$$

As mentioned previously, the overall leakage inductance L_{Lk} takes into account the measured leakage inductor at the primary ($L_{Lk_{Pri}}$) and secondary ($L_{Lk_{Sec}}$) sides of the real transformer, referred to the primary side:

$$L_{Lk} = L_{Lk_{Pri}} + \frac{L_{Lk_{Sec}}}{2}\left(\frac{N_1}{N_2}\right)^2. \tag{18}$$

Upon these conditions, the inductance L_{Lk} is linearly charged. The currents through S_3 and S_4 are given by:

$$I_{S3} = -\frac{I_L}{2} - \frac{I_{PR}}{2}\frac{N_1}{N_2}, \tag{19}$$

$$I_{S4} = -\frac{I_L}{2} + \frac{I_{PR}}{2}\frac{N_1}{N_2}. \tag{20}$$

At instant t_1, I_{S4} is null, turning S_4 off, and thus from this instant the current I_L equals the current through the body diode of S_3:

$$I_{S3} = -I_L, \tag{21}$$

$$I_{S4} = 0. \tag{22}$$

As a consequence, the dead time t_d, defined as the interval between instants t_0 and t_1,

$$t_d = t_1 - t_0 \tag{23}$$

is the time it takes for the current I_{S3} to reach $-I_L$ after S_1 is turned on. This condition can be expressed as:

$$\frac{-I_L}{2} - \frac{1}{2}\frac{N_1}{N_2}\frac{V_{BAT}}{2}\frac{1}{L_{Lk}}(t_1 - t_0) = -I_L(t). \tag{24}$$

The explicit expression for t_d can thus be obtained:

$$t_d = 2 \cdot \frac{N_2}{N_1}\frac{I_L(t)}{V_{BAT}} \cdot L_{Lk}. \tag{25}$$

It is important to note that t_d represents a completely different behavior in the full model when compared to the basic one. For the basic model, when switch S_1 is turned on, V_O equals to half the battery voltage, obviously referred to the secondary side. Instead, for the full model, V_O is zero during t_d just after turning S_1 on, and then reaches the same $V_{BAT}/2$ for the rest of the interval when S_1 remains turned on. This situation affects the final voltage gain at the topology, given that the effective duty ratio of the converter, D_{eff}, is actually smaller for the full model than for the basic one. This D_{eff} can be defined now as:

$$D_{eff} = \frac{D_1 \cdot T_S - t_d}{T_S}. \tag{26}$$

As it can be deduced from Equation (25), the expression of the dead time is a non-linear function of a manifold of system parameters. Hence, the resulting model that takes this t_d into account is a non-linear model. The large-signal circuital model that considers t_d (and also R_{loss}) is shown in Figure 12. Additionally, the Equivalent Series Resistor, ESR_C, of the filter capacitor C has been included.

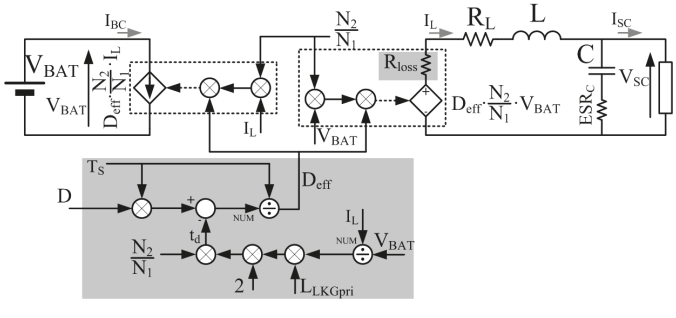

Figure 12. Full averaged large-signal model based on real components, parasitic elements, and snubbers.

The full average model has been simulated and compared with the switching circuit, in order to evaluate its performance. These simulations, shown in Figure 13, have been carried out in the same conditions that were established for the previous simulations of the basic model shown in Figure 9.

It can be seen how the new complete model tracks much more accurately the simulated waveforms at the switching model, again for a duty step from 0.34 to 0.36. Therefore it can be concluded that the dynamic behavior of the HBCS converter with the proposed SR scheme is truly represented by the obtained full model.

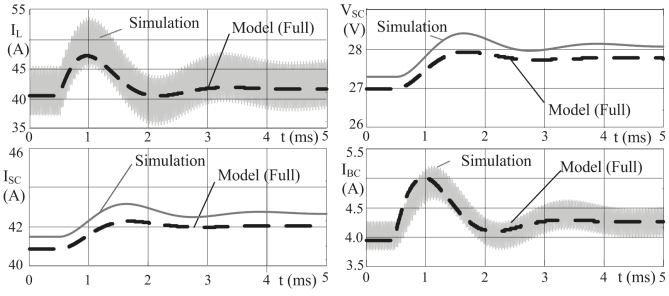

Figure 13. Simulation waveforms (gray) and averaged value of model based on the parameters of real components (black), for filter current (I_L), load output current (I_{SC}), load voltage (V_{SC}) and input current (I_{BC}).

An important remark on this behavior ir that this response corresponds to a second order system, as it is expected from a resistive load at the output of the *L*–*C* filter at the LV side. In the proposed application, the load is an assembly of SC. If this assembly is considered as an ideal pure capacitive load, given that the capacitance value of these devices is very large, then the output voltage would remain constant during the transient, and thus the dynamic behavior of the output voltage can be disregarded. For a more realistic approach, the SC assembly will be modeled by an equivalent circuit formed by a series resistor and the SC capacitor. Still, the SC will present a very large capacitance value, and therefore it behaves practically as a DC voltage source. Thus, the AC small signal model of the SC is given by the series resistor only, and the behavior of the full system is again corresponding to a second order system.

At this point, a small-signal model can be derived. Figure 14 shows the model that emerges after linearizing and perturbing the large signal full model, which has the following parameters:

$$R_1 = \frac{t_d}{T_S} \tag{27}$$

$$R_2 = \frac{2 \cdot D \cdot L_{Lk_{Pri}}}{T_S} \left(\frac{N_2}{N_1}\right)^2 \tag{28}$$

$$K_1 = \frac{N_2}{N_1} \cdot I_L \left(1 - \frac{t_d}{T_S}\right) \tag{29}$$

$$K_2 = 2 \cdot \frac{t_d}{T_S} \cdot D \cdot \frac{N_2}{N_1} \tag{30}$$

$$K_3 = \frac{N_2}{N_1} \cdot V_{BAT} - \frac{2 \cdot I_L^2 \cdot L_{Lk_{Pri}}}{T_S} \left(\frac{N_2}{N_1}\right)^2 \tag{31}$$

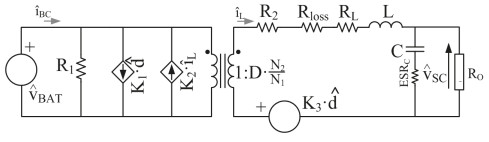

Figure 14. Full Small Signal Model of the system.

This last model finally allows the design and tuning of the control system, since the most significant dynamics of the system are taken into account. The second order behavior of the system, represented in the previous analysis, can be also derived from this model. In fact, the output voltage to duty ratio transfer function, can be calculated as:

$$\left.\frac{\hat{v}_{SC}}{\hat{d}}\right|_{\hat{v}_{BAT}=0} = \frac{K_3 \cdot R_0}{R_0 + ESR_C} \cdot \frac{1 + s \cdot C \cdot ESR_C}{\frac{R_{EQ} + R_0}{R_0 + ESR_C} + s \cdot \left[\frac{L}{R_0 + ESR_C} + C \cdot \left(R_{EQ} + \frac{R_0 \cdot ESR_C}{R_0 + ESR_C}\right)\right] + s^2 \cdot L \cdot C} \tag{32}$$

where

$$R_{EQ} = R_2 + R_{loss} + R_L \tag{33}$$

5. Proposed Control Scheme for the HBCS Converter

An adequate design of the control stage of the converter is needed in order to ensure the required power flows in the hybrid storage system under consideration [20–29]. In order to obtain the desired operating performance of the system, a High Level Control System provides the instant power references that each storage device must supply to the DC link. From this power reference, the HV current value of the HBCS converter, I^*_{BC} can be calculated. This scheme is depicted in Figure 15 [40].

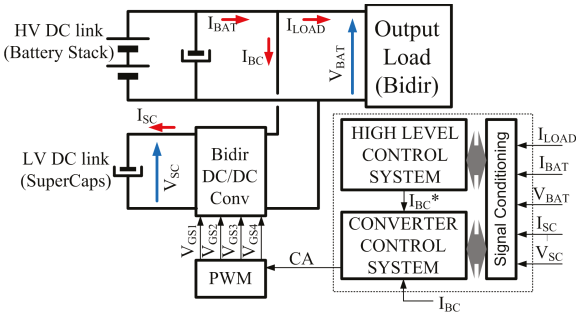

Figure 15. Control Strategy for the HBCS converter.

Considering that the final control parameter is the inductor current, I_L, the converter control stage covers two different aspects: Firstly, it is required that this stage generates a reference for such current, I^*_L, starting from the HV side current, I^*_{BC}. In addition, it implements a feedback control loop for such inductor current.

5.1. Feedback Control Loop for the SC current

This inductor current control loop is shown in Figure 16a. It must be noticed how the average value of I_L equals the average value of I_{SC}. In order to design and tune the regulator, the inductor voltage to inductor current transfer function $G(s)$ can be defined as:

$$G(s) = \frac{1}{R_L + s \cdot L} \tag{34}$$

For the current loop, a standard PI regulator has been designed. This regulator is tuned using the zero-pole cancellation method, and setting the desired bandwidth of the current loop. The regulator consists of a pure integrator and a zero that cancels the pole given by the inductance L and the ESR of the filter inductor, R_L. This ensures that the final bandwidth of the controlled system can be designed to a target value. The characteristic frequency of this zero might change upon eventual variations of the equivalent series resistor due temperature excursions, ageing, or even manufacturing tolerances.

However, assuming an adequate design of this inductor filter, then the ESR of this magnetic element will be relatively small; therefore, the variations in this parameter will not significantly affect the final performance of the controlled system. Once the regulator is tuned, the final implementation needs to obtain the expression of the duty ratio, D, from the control action of the current loop, CA. Considering Equations (25) and (26) and Figure 12, the relationship between D and V_L can be calculated:

$$V_L = D_{eff} \cdot \frac{N_2}{N_1} \cdot V_{BAT} - V_{SC} = D \cdot \left(1 - \frac{t_d}{T_S}\right) \frac{N_2}{N_1} \cdot V_{BAT} - V_{SC}. \tag{35}$$

Finally,

$$D = \frac{N_1}{N_2} \cdot \frac{V_L + V_{SC}}{V_{bat} - \frac{N_2}{N_1} \cdot \frac{2 \cdot I_L \cdot L_{Lk_{Pri}}}{T_S}}. \tag{36}$$

Figure 16b shows the implemented control scheme. The shaded box implements Equation (36), obtaining the duty ratio D from the control action of the current loop, CA, which is V_L. Figure 17 shows simulations of the performance of this inner loop for a bandwidth of 500 Hz. This plot provides a sequence of current steps as a reference to the current loop, I_L^*. It can be seen how the actual current value tracks perfectly the reference. Moreover, the current can swiftly change its direction, changing automatically from charging to discharging operation modes, even for large relative current steps. This feature is a consequence of using the discussed SR modulation scheme in the topology.

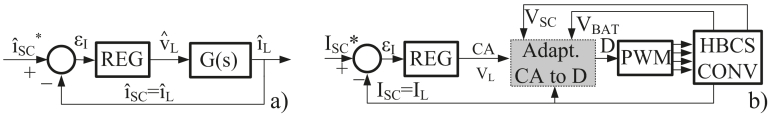

Figure 16. Inner control loop approach (**a**) for designing and tuning the regulator and (**b**) for implementing the control scheme.

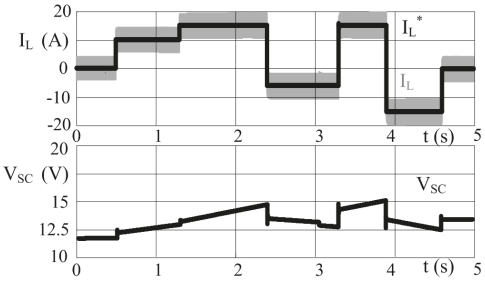

Figure 17. Simulation of inductor current I_L (gray, upper plot) and supercapacitor (SC) voltage V_{SC} (black, lower plot) during step changes in the commanded current (black, lower plot). Positive current corresponds to charging mode, negative to discharging mode.

5.2. Generation of the SC Current Reference

The complete control scheme is shown in Figure 18. An external estimator stage is designed to generate the feedback loop current reference, I_L^*, from the original I_{BC}^* reference. The relationship between the HV-side current and the inductor current can be obtained from the model in Figure 14 as

$$\hat{i}_{BC} = K_1 \cdot \hat{d} + \frac{1}{R_1} \cdot \hat{v}_{BAT} + \left(\frac{N_2}{N_1} \cdot D - K_2 \right) \cdot \hat{i}_L, \tag{37}$$

$$\left. \frac{\hat{i}_{BC}}{\hat{i}_L} \right|_{\substack{\hat{d}=0 \\ \hat{v}_{BAT}=0}} = \frac{N_2}{N_1} \cdot D - K_2. \tag{38}$$

The value of the inductor current reference, I_L^*, is estimated from the HV-side current, I_{BC}^*, by means of the model, as is given in Equation (38). Other control strategies based on additional feedback loops, such as a cascaded control loop to generate the inductor current reference, would imply a more complex implementation of the controller, in terms of computation, number of sensors, filtering and signal conditioning stages, and so on. In addition, they would provide a decrease in the dynamics, given that the external loop dynamics requires a bandwidth significantly smaller than that of the inner loop, in order to ensure a good overall performance.

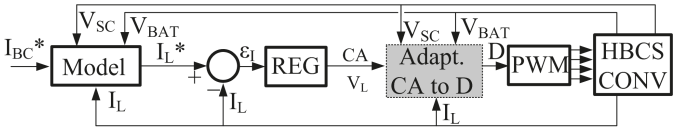

Figure 18. Complete control scheme for the half-bridge current-source (HBCS) converter.

6. Experimental Results

Figure 19 shows a 3 kW laboratory prototype of the HBCS, used in this work for the practical demonstration of the system performance. The main characteristics of the setup are detailed in Table 1. Preliminary results of the performance of this setup were reported in [35].

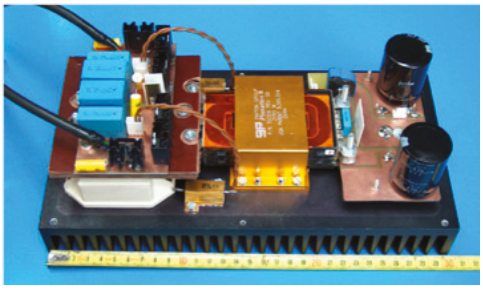

Figure 19. Laboratory prototype of the half-bridge current-source (HBCS) converter.

Figure 20 shows the experimental waveform of the converter, with the same operating conditions as reported in Figure 9. It can be seen how the experimental waveforms were very similar to the simulated waveforms for the switching converter. It also can be seen how the ideal model failed to track the real waveforms properly.

Similarly, Figure 21 compares the proposed complete model, including the effects of the parasitic leakage inductance of the transformer and the resistance to account for the losses, against the experimental waveforms, resembling the conditions stated for Figure 13. This validates the obtained model for the HBCS converter, as the complete model tracked the real converter waveforms very accurately.

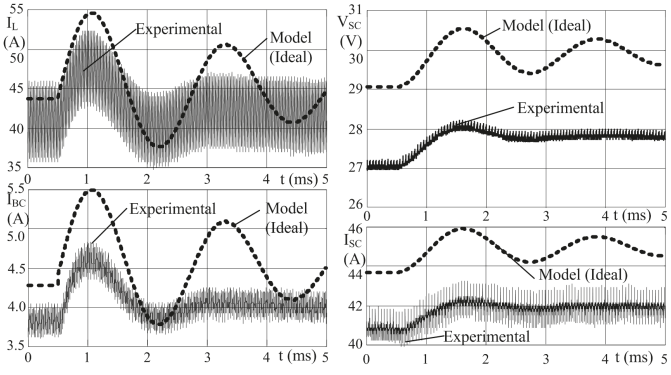

Figure 20. Experimental waveforms (gray) and averaged value of model based on ideal components (black, dashed), for filter current (I_L), load output current (I_{SC}), load voltage (V_{SC}), and input current (I_{BC}).

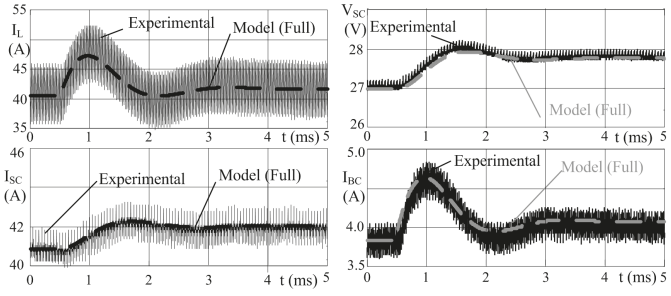

Figure 21. Experimental waveforms (gray) and averaged value of model based on real components (black), for filter current (I_L), load output current (I_{SC}), load voltage (V_{SC}), and input current (I_{BC}).

In order to validate experimentally the implementation of the control scheme, a series of current reference steps were implemented in the converter. The reference steps that were provided to the simulations, shown in Figure 17, were also supplied to the laboratory prototype. Figure 22 shows the performance of the experimental setup. It can be seen how the real converter performed as expected, thus validating the converter control scheme.

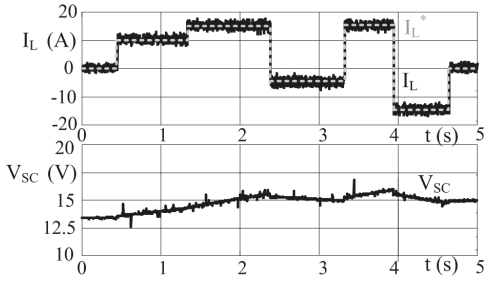

Figure 22. Inductor current I_L (black, upper plot) and supercapacitor (SC) voltage V_{SC} (black, lower plot) during step changes in the commanded current I_L^* (referenced by dashed gray lines). Positive current corresponds to charging mode, negative to discharging mode.

In order to check the dynamics of the inner control loop, a detailed experimental response of one of such current steps is shown in Figure 23.

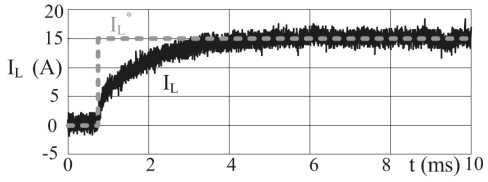

Figure 23. Inductor current I_L (black) and reference I_L^* (grey) during one step change.

7. Conclusions and Future Developments

This research has demonstrated the feasibility of the HBCS converter as a bidirectional power converter for HSS systems in traction applications, where the DC-link is directly connected to the battery bank. The main topics covered include the analysis and design of the power and control stages, the modeling including parasitic elements of the topology, and a validation procedure through a laboratory prototype.

As a first contribution, it has been demonstrated that the use of SR is a suitable switching scheme in the converter, given the demonstrated benefits in the efficiency and the enhancement in the control system implementation. By means of this switching pattern, a full, bidirectional power flow control can be simply implemented in the converter. Moreover, this feature is obtained at no cost, since the required hardware elements to implement SR pattern are present in the conventional HBCS topology.

Another key contribution is to include the parasitic elements in the topology aiming to obtain a highly representative circuital model of the converter. This model has been demonstrated by means of simulations and through experiments in a 3 kW laboratory setup. With the information derived from this dynamic model, the design of the control stage for the HSS can be easily implemented. This research also has provided a design example of a current control loop in order to govern the power flow in the HSS outlined.

A series of future developments arise from this research. One of these developments is the implementation of the HSS in a full powertrain for vehicle applications, including the integration of the HBCS converter control with the complete high-level control system. Another development covers the optimization of the converter power topology and control system, including the definition of the control strategy for the complete system. Additionally, the extension of the application of the HBCS converter to other types of loads (e.g., inductive loads) can be considered in future research.

Author Contributions: J.G. and F.G.C. conceived the research and designed and performed the experiments; all the authors analyzed the data and contributed to the discussion and conclusions.

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Abbreviations

The following abbreviations are used in this manuscript:

CA	Control action
DC	Direct current
ESR	Equivalent series resistor
LV	Low-voltage
HBCS	Half-bridge current-source
HF	High-frequency
HSS	Hybrid storage system
HV	High-voltage
IGBT	Insulated-gate bipolar transistor
MOSFET	Metal-oxide-semiconductor field-effect transistor
SC	Supercapacitor
SR	Synchronous rectification

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Novel Step-Down DC–DC Converters Based on the Inductor–Diode and Inductor–Capacitor–Diode Structures in a Two-Stage Buck Converter

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Abstract: This paper explores and presents the application of the Inductor–Diode and Inductor-Capacitor-Diode structures in a DC–DC step-down configuration for systems that require voltage adjustments. DC micro/picogrids are becoming more popular nowadays and the study of power electronics converters to supply the load demand in different voltage levels is required. Multiple strategies to step-down voltages are proposed based on different approaches, e.g., high-frequency transformer and voltage multiplier/divider cells. The key question that motivates the research is the investigation of the aforementioned Inductor–Diode and Inductor–Capacitor–Diode, current multiplier/divider cells, in a step-down application. The two-stage buck converter is used as a study case to achieve the output voltage required. To extend the intermediate voltage level flexibility in the two-stage buck converter, a second switch was implemented replacing a diode, which gives an extra degree-of-freedom for the topology. Based on this modification, three regions of operation are theoretically defined, depending on the operational duty cycles δ_2 and δ_1 of switches S_2 and S_1. The intermediate and output voltage levels are defined based on the choice of the region of operation and are mapped herein, summarizing the possible voltage levels achieved by each configuration. The paper presents the theoretical analysis, simulation, implementation and experimental validation of a converter with the following specifications; 48 V/12 V input-to-output voltage, different intermediate voltage levels, 100 W power rating, and switching frequency of 300 kHz. Comparisons between mathematical, simulation, and experimental results are made with the objective of validating the statements herein introduced.

Keywords: DC–DC converter; experimental verification; Inductor–Diode; Inductor–Capacitor–Diode; nonisolated; step-down; two-stage buck converter; voltage regulation

1. Introduction

In the last century, AC systems predominated as the most widespread method for energy generation, transmission, and distribution. For regular AC generation, large power plants, e.g., coal, hydro, and nuclear, have been used to centrally generate energy. Alternatives, such as wind and solar generation, are more frequently being installed to decentralize the energy production and lower the CO_2 emitted by the energy production [1,2].

Wind farms (AC generation) are more common in remote regions (on and off-shore) where the wind is conducive for generation. Solar (DC generation), on the other hand, started to become viable for application in high populated areas where the sun irradiation is high enough to achieve maximum power generation. DC systems started to be developed and implemented in pilot projects and real

applications because they have proved to be more efficient than AC systems in terms of transformation steps [3], costs [4], and power transfer capability [5]. Applications of DC system such as in micro- and nanogrids [6,7], datacenters [8,9], and aircrafts, where redundancy and backup is mandatory, are currently on the rise. DC system technology can also be implemented in isolated/remote/emerging regions [10]. In these systems, redundancy normally is indispensable in order to keep the system operational even if a component and/or a converter fails. Furthermore, DC loads are common especially in low voltage/low power applications, for instance, in computer and battery chargers, USB and USB-C ports, and LED lights. These type of loads are commonly found in offices and residences.

Discussions among the voltage levels that are implemented in these systems are extensively presented in the literature [11], for instance, with a voltage between 350 and 400 V for distribution in unipolar or bipolar [6,12,13] DC configurations to supply high power equipments. The 48 V level is [14,15] normally adopted as an intermediate bus stage to supply the low voltage/low power loads aforementioned. The 48 V level is also getting more common in battery systems for Electric Vehicles (EV), and it is considered for residential applications due to its user safety approach.

A DC picogrid, based on state-of-the-art architectures [3,6,16], is depicted in Figure 1, which emulates a building and/or residence with a DC grid implementation. In this grid, a bipolar DC network is realized (P0N poles), which has the possibility of injecting the energy generated by the panels in the AC grid or, alternatively, directly supply DC loads bypassing the DC–AC–DC transformation.

A lot of effort has been spent to propose new topologies and systems to interconnect PV generation in AC or DC grids with, respectively, microinverters [17–19] and microconverters (DC power optimizers) [20–24] which, in essence, are step-up converters since the PV panel output voltage is lower than the AC grid or DC bus voltages. The control aspects of this system and MPPT strategies are common subjects in the literature [20,25–27].

Different strategies to step-up the voltage have been studied and proposed in the literature, such as: isolated step-up topologies [17,21,28], coupled-inductor, nonisolated topologies [29–35], nonisolated topologies with Capacitor–Diode/switch structure [19,36–38], nonisolated topologies with Inductor–Diode/switch [39,40] and nonisolated topologies with Capacitor–Diode/switch and Inductor–Diode/switch structures [41,42]. These structures are known, respectively, as switched-capacitors and switched-inductors. An adaptation of the Inductor–Diode structure is proposed in [43], where a capacitor replaces one diode and changes the gain of the structure for step-up applications. Each of the above-mentioned strategies to step-up voltages has its advantages and disadvantages. For instance, isolated topologies and coupled inductor topologies have the flexibility of, based on the turns ratio of the magnetic device, select the suitable output voltage requirement, although it is known that these magnetic components are, together with heatsinks, the bulkiest components in a converter. Switched capacitor and switched inductors do not bring this flexibility once the gain is defined based on the operational duty cycle of the active switches. Inductors are more reliable components than capacitors, giving an advantage in terms of reliability, while capacitors are more compact and more suited for high power density applications.

In step-down conversion ratio converters, the Capacitor–Diode/switch structures are commonly used to improve the step-down ratio of the converters [44–46]. On the other hand, the implementation of an Inductor–Diode/switch and Inductor–Capacitor–Diode structures in the step-down conversion ratio is not extensively discussed in the literature, with few exceptions that explore both step-up and step-down structures [39]. The structures evaluated in this paper are shown in Figure 2. The Inductor–Diode structure shown in Figure 2 can offer a redundant path if one diode of the structure fails in open-circuit, as proposed in [47]. In steady-state, the inductors can be considered as current sources and, due to the structure operability discussed in Section 4, mitigate the implementation of current sensors for control purposes, since the current balance between the inductors is naturally achieved without any control strategy (switched-inductor characteristic). The only sensor that might be consider for implementation is a voltage sensor, if the application requires a regulated and constant

output voltage level for the entire load range of operation. For instance, a contraction technique was proposed to control a regular step-down converter [48].

With these considerations, the objective of this paper is to investigate the influence of the Inductor–Diode (ID) and Inductor–Capacitor–Diode (ICD) structures in the step-down conversion stage from 48 V to 12 V input-to-output voltage. The main contributions of this paper are (1) an analysis of the influence of the ID and ICD structures in a step-down conversion system; (2) the presentation of a full theoretical analysis of the converters generated; (3) applying the ID and ICD structures in a quadratic buck converter; (4) analyzing the intermediate voltage level behavior for different operational points, showing the intermediate voltage flexibility of the circuit, which is beneficial for a voltage regulation point of view; (5) creating a flexible test bench to be able to validate the proposed converters and; (6) experimentally validatation with waveforms of the topologies studied in the paper.

The paper is organized as follows; Section 2 presents the analysis of the ID and ICD structure in a regular single-stage buck converter and its impact on the gain of the converter. Section 3 presents the two-stage buck converter, known as quadratic buck converter [49], to enable the converter applying the ID and ICD structures to achieve the required output voltage levels. The operational principle of the topologies generated by the proposed intra-exchangeability is explained in Section 4. Section 5 explores the simulation results of the proposed topologies, showing the intermediate and output voltage levels that are obtained for each possible configuration. Section 6 describes the experimental test bench built for further validation, showing experimental waveforms that validate the theoretical analysis presented in Sections 3 and 4. Section 7 presents the main conclusions and future work suggestions.

2. Impact of Inductor–Diode and Inductor–Capacitor–Diode Structures in a Step-Down Converter

This section has the objective of investigating the influence of the ID and ICD structure in a step-down buck converter. Inductor I, shown in Figure 3, is replaced by ID and ICD structures and the PWM modes are described herein. The main difference between the ID and ICD structures is that the capacitor of the ICD is also charged during the magnetization of the inductors. When discharging, the capacitor also discharges, providing energy to the load. The capacitor stores part of the energy that is delivered to the load, which helps decrease the size of the inductors, since less energy is stored in their magnetic field. Additionally, the capacitor changes the voltage applied across the inductors during demagnetization, which changes the gain of the structures, as described herein.

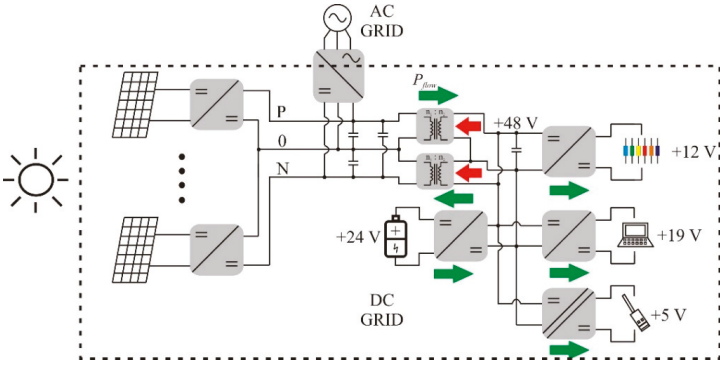

Figure 1. A basic DC picogrid, highlighting the PV generation and DC step-up conversion; the bipolar DC network (P0N); the battery energy storage system (BESS); and the DC loads supplied by DC–DC step-down converters.

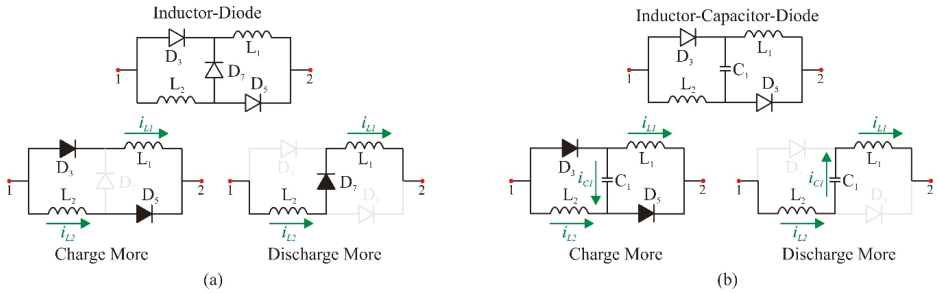

Figure 2. (**a**) Inductor–Diode (ID) structure and its charge and discharge modes and (**b**) Inductor–Capacitor–Diode (ICD) structure and its charge and discharge modes.

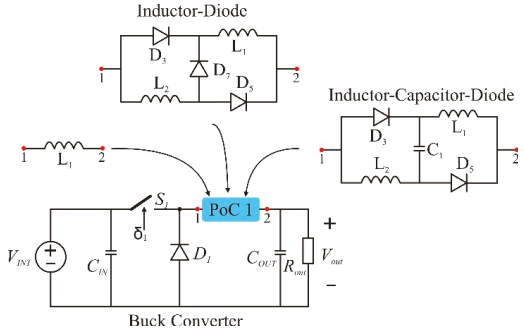

Figure 3. DC–DC Buck Converter with Point-of-Connection 1 (PoC1) to interchange inductor (I), Inductor–Diode (ID) and Inductor–Capacitor–Diode (ICD) structures.

2.1. PWM Mode 1

In this PWM mode, the switch S_1 commutates from 'open' to 'close', changing the equivalent circuit of the converter. The equivalent circuit for this mode is shown in Figure 4a,b for the ID and ICD applications in PoC1, respectively. During this mode, the voltage applied in the inductor terminals V_{L1} and V_{L2} is positive, due to the step-down mechanism, and energy is magnetically stored in the inductors during the process. The voltage applied across the inductors terminals has the same level (internally in ID and ICD structures), which leads to similar current level in the inductors of the structures. In the ID structure, the inductors store energy during this PWM Mode while in the ICD structure the inductors and the capacitor of the structure store energy.

2.2. PWM Mode 2

In this PWM mode, the switch S_1 commutates from 'close' to 'open'. The equivalent circuit for this mode is shown in Figure 4c,d for the ID and ICD structures, respectively. During this PWM mode, the voltage applied across the inductors terminals V_{L1} and V_{L2} is negative, since diode D_1 is forward biased, leading to a demagnetization of these inductors. The current across both inductors is equal as these components are in series, which guarantees the same negative voltage level across the inductors of the structures during the demagnetization. The demagnetization mechanism for both structures is similar, since in both structures the inductors are connected in series and the same current flows through the passive components.

From the above PWM mode analysis, the theoretical voltage profile for all the inductors in both structures are presented in (1). These equations are applied in (2) to obtain the conversion gain of the structures, in steady-state.

$$\begin{array}{cc} ID & ICD \\ \begin{cases} V_{L1} = V_{L2} = V_{IN} - V_{OUT} \ \ during \ \ \delta_1 \\ V_{L1} = V_{L2} = -\frac{V_{OUT}}{2} \ \ during \ \ (1-\delta_1) \end{cases} & \begin{cases} V_{L1} = V_{L2} = V_{C1} = V_{IN} - V_{OUT} \ \ during \ \ \delta_1 \\ V_{L1} = V_{L2} = \frac{V_{IN}}{2} - V_{OUT} \ \ during \ \ (1-\delta_1) \end{cases} \end{array} \quad (1)$$

$$\overline{V_L} = \int_0^{T_S} v_L dt = 0 \quad (2)$$

2.3. Theoretical Gain in Continuous Conduction Mode

To obtain the theoretical voltage gain profile of the topologies, operation in steady-state is considered, which allows the application of (1) in (2) to obtain the ideal gain of the structures. After some mathematical manipulation, the theoretical expression that represents the gain of the Inductor–Diode (ID) and Inductor–Capacitor–Diode (ICD) structures, respectively, is graphically represented in Figure 5. From Figure 5, it is noticed that the operational voltage range tackled in this paper cannot be realized with the ICD structure, since its gain range is, ideally, between [0.5 ; 1]. To overcome this, the quadratic buck converter—a nonlinear step-down converter generated by two buck converters connected in series with each other—as depicted in Figure 6, is the base topology used to generate the converters proposed in this paper. This converter presents an intermediate stage, giving an extra degree of freedom for implementation, since two voltage levels are generated in the same converter and both can be used to supply loads.

Only one switch is implemented on the power stage of the conventional quadratic buck, which has the benefit of control strategy simplification; and the intermediate voltage level is in the function of the duty cycle applied to switch S_1. If a second switch is introduced in the power stage, the degree of freedom for voltage regulation in the intermediate stage is guaranteed by the duty cycle of the second switch S_2, although the control strategy might increase in complexity, if applicable. Since the objective of the topologies is to improve the flexibility of the conversion ratio and the overall system, the quadratic buck with two switches is the converter that will be extensively explored in the next section, together with the intra-exchangeable PoC structures presented in Figure 3.

3. Double-Switch Two-Stage Quadratic Buck Converter for Voltage Regulation

As previously mentioned, the two-stage buck converter, most known as quadratic buck converter, is the base topology used for the intra-exchangeable methodology used herein for testing multiple configurations, based on the ID and ICD structures, applied for voltage regulation. Since a second stage is now implemented in the power circuit, the intra-exchangeability increases the amount of topologies that can be generated. More specifically, with three structures and two stages, the number of topologies generated is $3^2 = 9$, where only the conventional quadratic buck is already explored in the literature. Figure 6 exemplifies the possible configurations that can be obtained from the proposed intra-exchangeability between a regular inductor (I) and the ID and ICD structures. When an I structure is connected to PoC1 and PoC2, the regular quadratic buck is obtained. In total, nine topologies are generated from this method and, since two switches are implemented in the power stage with independent duty cycles, three regions of operation can be explored and will be briefly discussed herein. The regions of operation are highlighted in Figure 6, named as region 1, when duty cycle δ_2 is higher than duty cycle δ_1; region 2, when δ_1 is higher than δ_2; and region 3, when both duty cycles are equal. The switch realization is based on a MOSFET with an antiparallel diode, as shown in Figure 6.

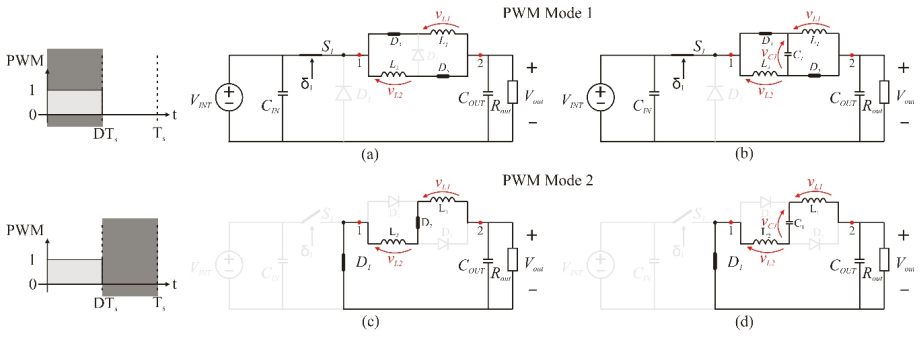

Figure 4. (**a**) PWM mode 1 for ID structure; (**b**) PWM mode 1 for ICD structure; (**c**) PWM mode 2 for ID structure, and (**d**) PWM mode 2 for ICD structure.

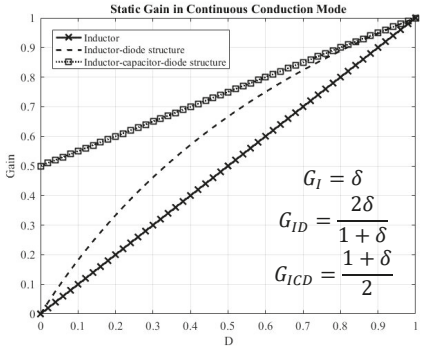

Figure 5. Continuous conduction mode graphical gain representation.

3.1. Region 1 ($\delta_2 > \delta_1$)

Operating in Region 1, the two stages of the quadratic buck structure operate independently, leading to intermediate and output voltages, depending on the duty cycles δ_2 and δ_1. The intermediate voltage across capacitor C_{inter} depends on the structure connected in PoC2 and the duty cycle δ_2 to command switch S_2. The output voltage, on the other hand, depends on both structures connected in PoC2 and PoC1, since the intermediate voltage level is the input voltage of the first stage. The equations presented in Figure 5 are reused to find the intermediate and output voltages generated by this integration. Table 1 summarize the analysis, showing the theoretical gain profile of the intermediate stage and output stage in function of the input voltage of the circuit and the duty cycle of switches S_1 and S_2. For instance, if the ID structure is applied in PoC1 and the I structure in PoC2, the intermediate and output voltages of the circuit are, respectively, related to equations δ_2 and $\delta_2 \frac{2\delta_1}{1+\delta_1}$, , which means that the intermediate voltage is regulated by the nominal set point of the duty cycle applied in S_2 and the output voltage depends on the duty cycles applied to S_1 and S_2. The analysis considers that the duty cycles are independent, and with no phase-shift between each other.

3.2. Region 2 ($\delta_2 < \delta_1$)

Operating in this region, the second stage of the quadratic buck depends on the first stage, since the duty cycle of switch S_1 is higher than the duty cycle of switch S_2. Consequently, the intermediate capacitor continues to discharge even if the switch S_2 is in 'off'-state (due to the antiparallel diode between drain-source points of S_2). In this operational region, the duty cycle δ_1 defines the intermediate

voltage level and the output voltage level. Table 2 summarizes the voltage levels in this region of operation.

3.3. Region 3 ($\delta_2 = \delta_1 = \delta$)

Region 3 is the region when both switches operate with the same duty cycle ($\delta_2 = \delta_1 = \delta$) and the duty cycles are in phase with each other. For this case, the intermediate and output voltages are subject to the operational duty cycle of the circuit. The theoretical analysis, shown in Section 4, is related to operation in Region 3. Table 3 summarize the voltage gain of the topologies generated by this intra-exchangeability.

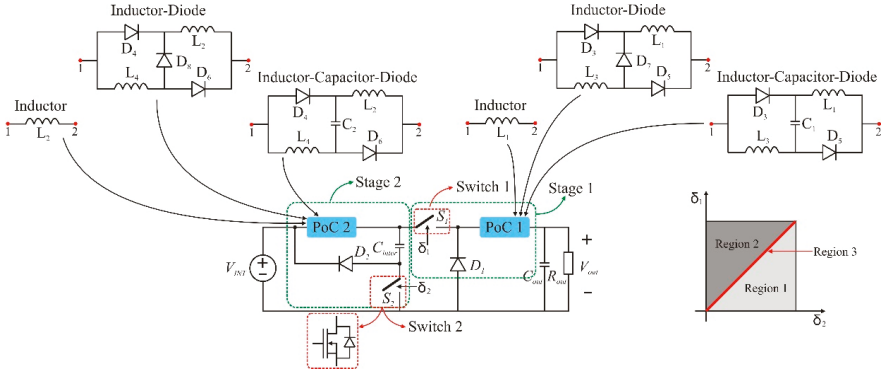

Figure 6. Quadratic Buck with two Point-of-Conncetions (PoCs) implemented and possible configurations achieved by the intra-exchangeability between I, ID, and ICD structures. Additionally, the operational regions for different duty cycle possibilities and switch realization.

Table 1. Theoretical Gain Analysis for all possible combinations between I, ID, and ICD structures in the quadratic buck configuration operating in Region 1. Intermediate and output voltage profiles in function of the input voltage of the circuit.

PoC1 / PoC2	I		ID		ICD	
	$\frac{V_{inter}}{V_{IN}}$	$\frac{V_{OUT}}{V_{IN}}$	$\frac{V_{inter}}{V_{IN}}$	$\frac{V_{OUT}}{V_{IN}}$	$\frac{V_{inter}}{V_{IN}}$	$\frac{V_{OUT}}{V_{IN}}$
I	δ_2	$\delta_2\delta_1$	δ_2	$\delta_2 \frac{2\delta_1}{1+\delta_1}$	δ_2	$\delta_2 \frac{1+\delta_1}{2}$
ID	$\frac{2\delta_2}{1+\delta_2}$	$\frac{2\delta_2}{1+\delta_2}\delta_1$	$\frac{2\delta_2}{1+\delta_2}$	$\frac{2\delta_2}{1+\delta_2}\frac{2\delta_1}{1+\delta_1}$	$\frac{2\delta_2}{1+\delta_2}$	$\frac{2\delta_2}{1+\delta_2}\frac{1+\delta_1}{2}$
ICD	$\frac{1+\delta_2}{2}$	$\frac{1+\delta_2}{2}\delta_1$	$\frac{1+\delta_2}{2}$	$\frac{1+\delta_2}{2}\frac{2\delta_1}{1+\delta_1}$	$\frac{1+\delta_2}{2}$	$\frac{1+\delta_2}{2}\frac{1+\delta_1}{2}$

where δ_2 and δ_1 are the duty cycle of switches S_2 and S_1, respectively.

Table 2. Theoretical Gain Analysis for all possible combinations between I, ID, and ICD structures in the quadratic buck configuration operating in Region 2. Intermediate and output voltage profiles in function of the input voltage of the circuit.

PoC1 / PoC2	I		ID		ICD	
	$\frac{V_{inter}}{V_{IN}}$	$\frac{V_{OUT}}{V_{IN}}$	$\frac{V_{inter}}{V_{IN}}$	$\frac{V_{OUT}}{V_{IN}}$	$\frac{V_{inter}}{V_{IN}}$	$\frac{V_{OUT}}{V_{IN}}$
I	δ_1	δ_1^2	δ_1	$\frac{2\delta_1^2}{1+\delta_1}$	δ_1	$\delta_1 \frac{1+\delta_1}{2}$
ID	$\frac{2\delta_1}{1+\delta_1}$	$\frac{2\delta_1^2}{1+\delta_1}$	$\frac{2\delta_1}{1+\delta_1}$	$\left(\frac{2\delta_1}{1+\delta_1}\right)^2$	$\frac{2\delta_1}{1+\delta_1}$	δ_1
ICD	$\frac{1+\delta_1}{2}$	$\frac{1+\delta_1}{2}\delta_1$	$\frac{1+\delta_1}{2}$	δ_1	$\frac{1+\delta_1}{2}$	$\left(\frac{1+\delta_1}{2}\right)^2$

Table 3. Theoretical Gain Analysis for all possible combinations between I, ID, and ICD structures in the quadratic buck configuration operating in Region 3. Intermediate and output voltage profiles in function of the input voltage of the circuit.

PoC1 / PoC2	I		ID		ICD	
	$\frac{V_{inter}}{V_{IN}}$	$\frac{V_{OUT}}{V_{IN}}$	$\frac{V_{inter}}{V_{IN}}$	$\frac{V_{OUT}}{V_{IN}}$	$\frac{V_{inter}}{V_{IN}}$	$\frac{V_{OUT}}{V_{IN}}$
I	δ	δ^2	δ	$\frac{2\delta}{1+\delta}\delta$	δ	$\delta\frac{1+\delta}{2}$
ID	$\frac{2\delta}{1+\delta}$	$\frac{2\delta}{1+\delta}\delta$	$\frac{2\delta}{1+\delta}$	$\left(\frac{2\delta}{1+\delta}\right)^2$	$\frac{2\delta}{1+\delta}$	$\frac{2\delta}{1+\delta}\frac{1+\delta}{2}$
ICD	$\frac{1+\delta}{2}$	$\frac{1+\delta}{2}\delta$	$\frac{1+\delta}{2}$	$\frac{1+\delta}{2}\frac{2\delta}{1+\delta}$	$\frac{1+\delta}{2}$	$\left(\frac{1+\delta}{2}\right)^2$

Although nine different topologies are realized in this analysis, only six different output voltage profiles are obtained, since the topologies I-ID/ID-I, I-ICD/ICD-I and ID-ICD/ICD-ID provide the same output voltage profile, while different intermediate voltage profiles are observed. Figure 7 shows the graphical representation of the output voltage profiles presented in Table 3. It is noticed that, due to the equations of the voltage profile shown in Figure 5, the highly nonlinear behavior of the quadratic buck converter is attenuated when the ID or ICD structures are used in one of the PoCs. The gain of the topologies, mathematically expressed in Table 3 and graphically in Figure 7, is less nonlinear if compared with the conventional quadratic converter, which is interesting for control purposes. These converters, however, are not suitable for applications that require high step-down capability, since the ID and ICD structures decrease the step-down capability of the structure, as shown in Figure 5 for application in a regular buck and Figure 7 in the quadratic version. Although the component part count increases for ID and ICD implementation, it also increases the flexibility to achieve multiple intermediate voltage levels to supply different loads.

On comparison of Table 2, related to region 2, and Table 3, related to region 3, it is noticed that the gain of the structures are the same. As mentioned in the previous subsection, this behavior occurs because the antiparallel diode of switch S_2 continue to conduct even if switch S_2 is in 'off'-state until switch S_1 commutates from 'close' to 'open'. This analysis concludes that operational regions 2 and 3 generate similar PWM modes and, consequently, the same intermediate and output voltage levels while region 1 is distinguished by the independence between the stages. Section 4 will further discuss the operational principle of the double switch quadratic buck with ID and ICD structures, for operation in Region 3.

4. Operational Principle of the Double Switch Quadratic Buck Converter in Region 3

Similar to Section 2, where the one-stage I, ID, and ICD topologies have been introduced, this section introduces the PWM modes of the two-stage I, ID, and ICD topologies, where the PWM signal remains the same. The phase shift between δ_2 and δ_1 is considered zero (in phase with each other) for the specific analysis but if differs from zero, the gain behavior shown in Tables 1–3 will differ, since the phase-shift will influence the PWM stages and, consequently, the gain of the structures. The equivalent circuit for the first and second stages, considering all the possibilities between the exchangeable circuits, are present in Figure 8a,b, respectively. In order to evaluate the main characteristics of the topologies, the equivalent circuits presented in Figure 8 are used to mathematically evaluate the voltage and current stresses in all power components. This information is crucial to further dimension the components for practical implementation.

The voltage stress across each power semiconductor are extracted from the PWM mode stages in Figure 8 and summarized in Table 4. The voltage stress across switch S_1 and diode D_1 is affected by the structure applied in PoC2, for instance, if the I structure is applied to PoC2, the voltage stress across switch S_1 is defined by $(1+\delta)V_{IN}$, while if the ID structure is applied in PoC2, the voltage stress across switch S_1 is defined by equation $\frac{(1+3\delta)}{(1+\delta)}V_{IN}$. Similarly, the voltage stress across diodes $D_3/D_5/D_7$, connected to PoC1, are related to the structure connected in PoC1. For instance, maintaining PoC2

fixed with the ID structure, if the ID structure is connected to PoC1, the voltage across the diodes D_3/D_5 is expressed by $\frac{\delta^2}{(1+\delta)^2}V_{IN}$ and, if PoC1 is changed for an ICD structure, the voltage across diodes D_3/D_5 is expressed by $\frac{\delta}{(1+\delta)}V_{IN}$. Switch S_2 and diode D_2 stresses are independent on the structures and are equal to the input voltage V_{IN}. The voltage stress across diodes D_3-D_4-D_5-D_6-D_7-D_8, which are the diodes implemented in the ID and ICD structures, are related to the operational duty cycle, input voltage, and in which PoC the structures are implemented.

Similarly, the PWM modes also provide the RMS current stress in each power semiconductor. To evaluate the RMS current stress in all components, equation (3) is introduced, where i_{x1} is the current that the semiconductor conducts during the first PWM mode and i_{x2} is the current conducted during the second PWM mode. Applying (3), the current stress in each semiconductor is characterized and presented in Table 5. Different than the voltage stress, the current stress of switches S_2 and D_2 depend on the structure connected to PoC2 but are independent of the structure connected to PoC1. For instance, the RMS current stress across switch S_2 is expressed by $\frac{I_{IN}(1-\delta)}{\delta}\sqrt{\frac{1}{\delta}}$ if the I structure is connected to PoC2, and expressed by $\frac{I_{IN}(1-\delta)}{2\delta}\sqrt{\frac{1}{\delta}}$ if the ID structure is connected. It is also noticed that the current is independent on PoC1, in this case.

The analysis abovementioned is important in order to select the components for experimental validation, since the RMS current and voltage stress are the most important characteristics to select MOSFETs and diodes. The next section presents a numerical simulation for the proposed converter performed in PLECS (4.0.2, Plexim GmbH, Zurich, Switzerland).

$$i_{xRMS} = \sqrt{\frac{1}{T_S}\left(\int_0^{DT_S} i_{x1}^2 dt + \int_{DT_S}^{T_S} i_{x2}^2 dt\right)} \tag{3}$$

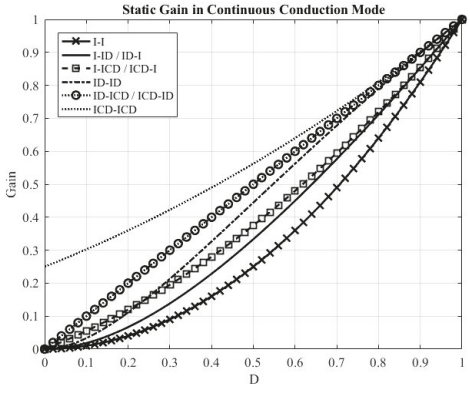

Figure 7. Continuous conduction mode graphical gain representation.

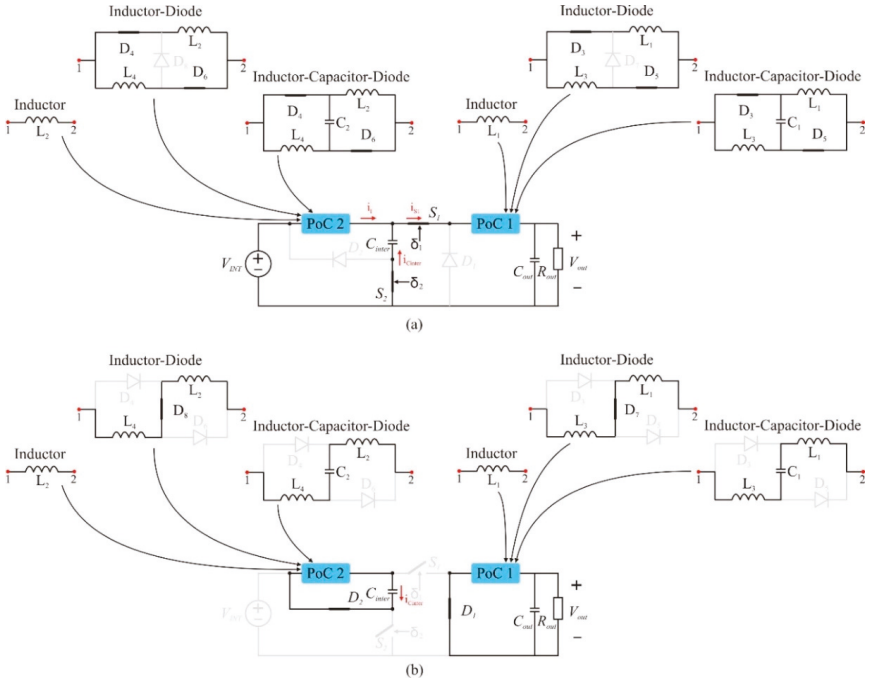

Figure 8. (**a**) Equivalent circuit for PoC 2 and PoC 1 applying I, ID, and ICD structures during the first PWM mode and (**b**) equivalent circuit for PoC 2 and PoC 1 applying I, ID, and ICD structures during the second PWM mode.

Table 4. Voltage stress sum up for all power semiconductors in the power stage. Equations are in function of the input voltage.

PoC2-PoC1	S_1	S_2	D_1	D_2	D_3/D_5	D_4/D_6	D_7	D_8
I-I	$(1+\delta)V_{IN}$	V_{IN}	δV_{IN}	V_{IN}	-	-	-	-
I-ID					$\frac{\delta^2}{(1+\delta)}V_{IN}$		$\frac{(1-\delta)\delta}{(1+\delta)}V_{IN}$	
I-ICD					$\delta\frac{V_{IN}}{2}$		-	
ID-I	$\frac{(1+3\delta)}{(1+\delta)}V_{IN}$		$\frac{2\delta}{(1+\delta)}V_{IN}$		-	$\frac{\delta}{(1+\delta)}V_{IN}$	$\frac{2(1-\delta)\delta}{(1+\delta)^2}V_{IN}$	$\frac{(1-\delta)}{(1+\delta)}V_{IN}$
ID-ID					$\frac{\delta^2}{(1+\delta)^2}V_{IN}$			
ID-ICD					$\frac{\delta}{(1+\delta)}V_{IN}$		-	
ICD-I	$\frac{(3+\delta)}{2}V_{IN}$		$\frac{(1+\delta)}{2}V_{IN}$		-	$\frac{V_{IN}}{2}$	$\frac{(1-\delta)}{2}V_{IN}$	-
ICD-ID					$\delta\frac{V_{IN}}{2}$			
ICD-ICD					$\frac{(1+\delta)}{4}V_{IN}$		-	

Table 5. RMS Current stress sum up for all power semiconductors in the power stage. Equations are in function of the input current.

PoC2-PoC1	S_1	S_2	D_1	D_2	D_3/D_5	D_4/D_6	D_7	D_8
I-I	$\frac{I_{IN}}{\delta}\sqrt{\frac{1}{\delta}}$	$\frac{I_{IN}(1-\delta)}{\delta}\sqrt{\frac{1}{\delta}}$	$\frac{I_{IN}}{2\delta^2}\sqrt{(1-\delta)}$	$\frac{I_{IN}}{\delta}\sqrt{(1-\delta)}$	-	-	-	-
I-ID			$\frac{I_{IN}}{2\delta^2}\sqrt{(1-\delta)}$		$\frac{I_{IN}}{2\delta}\sqrt{\frac{1}{\delta}}$		$\frac{I_{IN}}{2\delta^2}\sqrt{(1-\delta)}$	
I-ICD			$\frac{I_{IN}}{\delta(1+\delta)}\sqrt{(1-\delta)}$		$\frac{I_{IN}}{\delta(1+\delta)}\sqrt{\frac{1}{\delta}}$		-	
ID-I	$\frac{I_{IN}(1+\delta)}{2\delta}\sqrt{\frac{1}{\delta}}$	$\frac{I_{IN}(1-\delta)}{2\delta}\sqrt{\frac{1}{\delta}}$	$\frac{I_{IN}(1+\delta)}{2\delta^2}\sqrt{(1-\delta)}$	$\frac{I_{IN}}{2\delta}\sqrt{(1-\delta)}$	-	$\frac{I_{IN}}{2}\sqrt{\frac{1}{\delta}}$	$\frac{I_{IN}(1+\delta)}{4\delta^2}\sqrt{(1-\delta)}$	$\frac{I_{IN}}{2\delta}\sqrt{(1-\delta)}$
ID-ID			$\frac{I_{IN}(1+\delta)}{4\delta^2}\sqrt{(1-\delta)}$		$\frac{I_{IN}(1+\delta)}{4\delta}\sqrt{\frac{1}{\delta}}$			
ID-ICD			$\frac{I_{IN}}{2\delta}\sqrt{(1-\delta)}$		$\frac{I_{IN}}{2\delta}\sqrt{\frac{1}{\delta}}$		-	
ICD-I	$\frac{2I_{IN}}{(1+\delta)}\sqrt{\frac{1}{\delta}}$	$\frac{I_{IN}(1-\delta)}{(1+\delta)}\sqrt{\frac{1}{\delta}}$	$\frac{2I_{IN}}{\delta(1+\delta)}\sqrt{(1-\delta)}$	$\frac{I_{IN}}{(1+\delta)}\sqrt{(1-\delta)}$	-	$\frac{I_{IN}}{(1+\delta)}\sqrt{\frac{1}{\delta}}$	$\frac{I_{IN}}{\delta(1+\delta)}\sqrt{(1-\delta)}$	-
ICD-ID			$\frac{I_{IN}}{\delta(1+\delta)}\sqrt{(1-\delta)}$		$\frac{I_{IN}}{(1+\delta)}\sqrt{\frac{1}{\delta}}$			
ICD-ICD			$\frac{2I_{IN}}{(1+\delta)^2}\sqrt{(1-\delta)}$		$\frac{2I_{IN}}{(1+\delta)^2}\sqrt{\frac{1}{\delta}}$		-	

5. Numerical Simulations

A numerical simulation was carried out to show the available intermediate voltage levels when an output voltage of 12 V is set as standard output voltage. The 12 V voltage level can supply low voltage/low power loads to, for instance, LEDs or to charge small batteries (unidirectional power flow to charge, since the topologies are unidirectional); this is one of the main reasons to fix the output voltage on this level. The simulation and experimental parameters are presented in Table 6.

Different intermediate voltage levels are generated, depending on the structure connected in PoC2 and the operational duty cycle of the converter, as shown in Table 3. The simulation model was develop in PLECS. The only configuration that is not able to be simulated and experimentally validated in this paper is the ICD-ICD structure, since the input/output voltage level is 48 V/12 V and the theoretical gain of this structure is 0.25 < ICD-ICD < 1, making it impossible to provide the required output voltage.

A simulation is performed for each configuration and the results are shown in Figure 9. The conventional quadratic buck with I-I is show in Figure 9a, generating an intermediate voltage level of 24 V. According to Table 3, the I-ID and ID-I configurations generates the same output voltage but different intermediate voltage levels for operation with the same duty cycle. This behavior is proved via simulation and presented in Figure 9b,d, where the voltage level of 20.25 V (I-ID) and 28.5 V (ID-I) are obtained for a duty cycle of 42.2%.

Similarly, the topologies I-ICD and ICD-I operate with the same duty cycle (36.6%) and input/output voltages, however the intermediate voltage level changes since is applied different structures in PoC2. Simulation results shown in Figure 9c,g confirm the analysis, since an intermediate voltage of 17.6 V (I-ICD) and 32.8 V (ICD-I) are obtained and available to supply loads in different voltage ranges in a flexible way. The structures ID-ICD and ICD-ID are also evaluate via simulation for similar input/output voltages. Intermediate voltages of 19.2 V (ID-ICD) and 30 V (ICD-ID) are obtained and shown in Figure 9f,h, respectively, validating the theoretical analysis presented in Table 3. Additionally, the last configurations present similar overall gain (δ) with the regular buck converter, however they present an additional voltage level that can be used to supply additional loads in different voltage levels. The drawback of the structure, compared with the conventional buck, is the component part count, since the number of inductors and diodes in the power stage increase.

Finally, the ID–ID structure is briefly discussed herein. Figure 9e shows the voltage levels obtained from simulation. Similarly with the conventional I-I quadratic buck, an intermediate voltage level

of 24 V is obtained, however an operational duty cycle of 33.3% is used to match the desired output voltage of 12 V.

The simulations were performed with a switching frequency of 300 kHz (switching period of 3.33 µs), since this frequency was used to calculate the I, ID, and ICD inductances for further implementation of the structures. All the inductances were select to present a 20% ripple current limit across the inductors in nominal power. A summary of the theoretical inductor current expressions in each scenario is present in Table 7, in function of the input current I_{IN}. From the PWM mode stages discussed in the previous section and shown in Figure 8a,b, the inductors of the ID and ICD structures charge its terminals in parallel and discharge in series, which guarantees natural balance between the internal currents of the structure. This characteristic enable the non-use of current sensors to control the inductor current, since this control is guarantee directly by the ID and ICD structures, also known as switched-inductor structures. The drawback, as previously mentioned, is the increase in the number of components in the power stage.

With the objective of validating the equations shown in Table 7, a comparison between the theoretical analysis and numerical simulation results was performed and shown in Table 8. The input/output voltage of the circuit is 48 V/12 V and a rated input power of 100 W. The different configurations operate with their respective duty cycles to generate an output voltage of 12 V (check Figure 7 for duty cycle). The comparison shows that the theoretical equations match the simulation results, which proves the validity of the equations to select the correct inductances for experimental verification.

Table 6. Simulated and experimental parameters for validation.

Variable	Symbol	Value/Model
Input Voltage	V_{IN}	48 V
Output Voltage	V_{OUT}	12 V
Input Power	P_{IN}	100 W
Output Capacitance	C_{OUT}	20 uF
Switching Frequency	f_s	300 kHz
Switch Technology	S_1/S_2	STMicroeletronics 100 V 0.0145 Ohm typ 30 A

Table 7. Theoretical expressions for current across the inductors of the structures.

PoC2-PoC1	I_{L2}	I_{L4}	I_{L1}	I_{L3}
I-I	$\frac{I_{IN}}{\delta}$	-	$\frac{I_{IN}}{\delta^2}$	-
I-ID			$\frac{I_{IN}}{2\delta^2}$	
I-ICD			$\frac{I_{IN}}{\delta(1+\delta)}$	
ID-I	$\frac{I_{IN}}{2\delta}$		$\frac{I_{IN}(1+\delta)}{2\delta^2}$	-
ID-ID			$\frac{I_{IN}(1+\delta)}{4\delta^2}$	
ID-ICD			$\frac{I_{IN}}{2\delta}$	
ICD-I	$\frac{I_{IN}}{(1+\delta)}$		$\frac{2I_{IN}}{\delta(1+\delta)}$	-
ICD-ID			$\frac{I_{IN}}{\delta(1+\delta)}$	

Table 8. Inductor current comparison: theoretical/simulation.

PoC2-PoC1	I_{L2}	I_{L4}	I_{L1}	I_{L3}
	theo./sim.	theo./sim.	theo./sim.	theo./sim.
I-I	4.16 A/4.164 A	-	8.32 A/8.324 A	-
I-ID	4.95 A/4.955 A		5.868 A/5.871 A	
I-ICD	5.628 A/5.662 A		4.12 A/4.12 A	
ID-I	2.464 A/2.465 A		8.304 A/8.306 A	-
ID-ID	3.093 A/3.098 A		6.191 A/6.201 A	
ID-ICD	4.1 A/4.096 A		4.1 A/4.096 A	
ICD-I	1.515 A/1.517 A		8.281 A/8.272 A	-
ICD-ID	1.65 A/1.643 A		6.601 A/6.567 A	

6. Experimental Verification and Test Bench

6.1. Region 2 ($\delta_2 < \delta_1$)/Region 3 ($\delta_2 = \delta_1 = \delta$)

This subsection will discuss the results obtained for operation in Region 3 ($\delta_2 = \delta_1 = \delta$). The topologies, discussed in Sections 3 and 4, were realized for further validation. A test bench was built for experimental verification of the configurations discussed herein. Figure 10 shows the test bench setup, together with a simplified bench schematic. It is shown in Figure 10 that a function generator (equipment (4)) is used to generate the PWM signals to drive S_1 and S_2. The experimental results shown herein are in open-loop operation, without a control strategy to regulate the intermediate and output voltage levels. Figure 11 shows the converter realization (middle) surrounded by the PoCs (PoC2 and PoC1) developed for each configuration (the inductors were selected based on the 20% maximal current ripple for each structure).

The PoCs, developed to test the different configurations, were designed separately following the plug-n-play methodology. As shown in the converter realization in Figure 11, the PoC2 and PoC1 are actual points of connection, where different external boards are connected to test different inductor configurations (I, ID, and/or ICD). Points 1 and 2, for PoC2, and 3 and 4, for PoC1, are available to connect the external PoCs. Additionally, Table 6 present the parameters defined for the experimental setup, in which the switching frequency of 300 kHz was select to simulate and experimental validation.

When comparing the waveforms presented in Figure 9a–h (simulation) and in Figure 12a–h (experimental), it can be seen that the voltage levels in all topologies are similar in shape (DC shape) and in amplitude. Figures 9 and 12 present the input, intermediate, and output voltages of the converter for the following configurations (PoC2-PoC1); (a) I-I, (b) I-ID, (c) I-ICD, (d) ID-I, (e) ID–ID, (f) ID-ICD, (g) ICD-I, and (h) ICD-ID. Small deviations are observed between the amplitude values in simulation and in the experimental waveforms due to the nonidealities inherent in the components selected to build the prototype. We also noticed that spikes of voltage appears in all voltage levels. This behavior is common in circuits that operate in high frequency, since internal parasitics of the components and also the parasitic inductances related to tracks and soldering points start to become prominent. Additionally, the commutation between 'on'- and 'off'-stages of switches S_1 and S_2 also generate internal oscillations in the circuit.

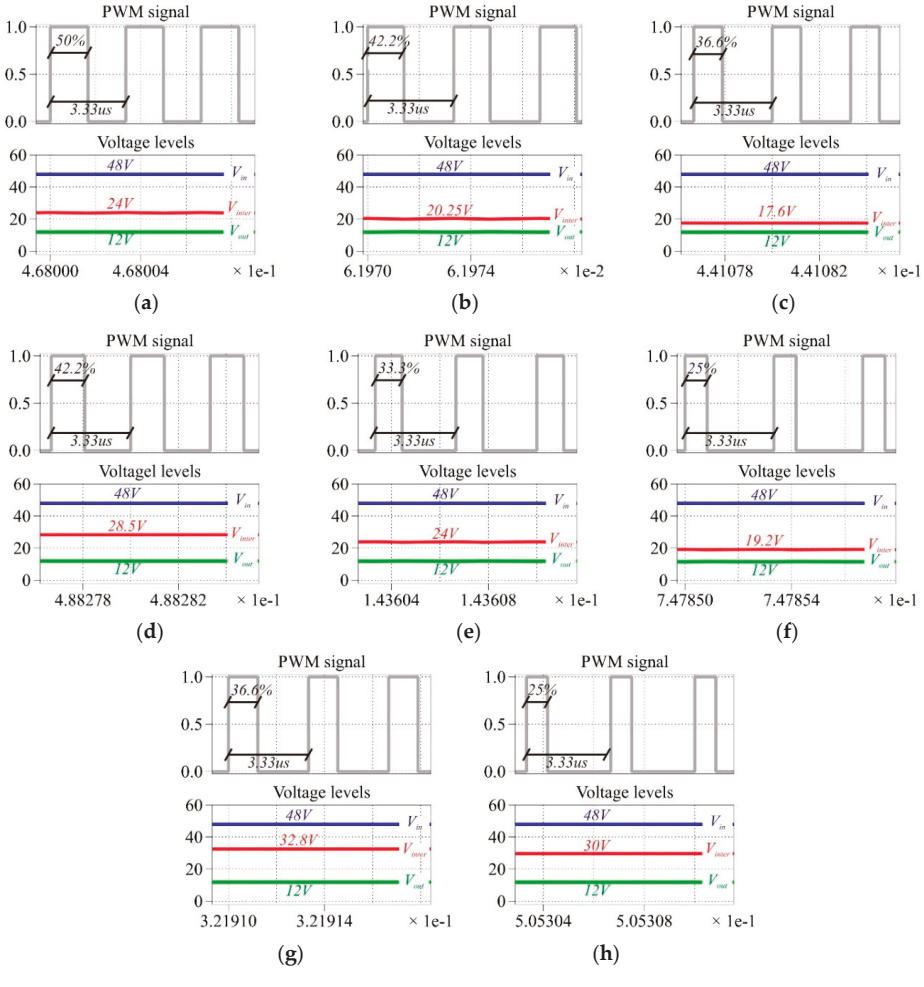

Figure 9. Simulation results showing the different intermediate voltage levels obtained by exchanging the structures for an input/output voltage of 48 V/12 V. PoC2-PoC1: (**a**) I-I; (**b**) I-ID; (**c**) I-ICD; (**d**) ID-I; (**e**) ID–ID; (**f**) ID-ICD; (**g**) ICD-I; and (**h**) ICD-ID, respectively.

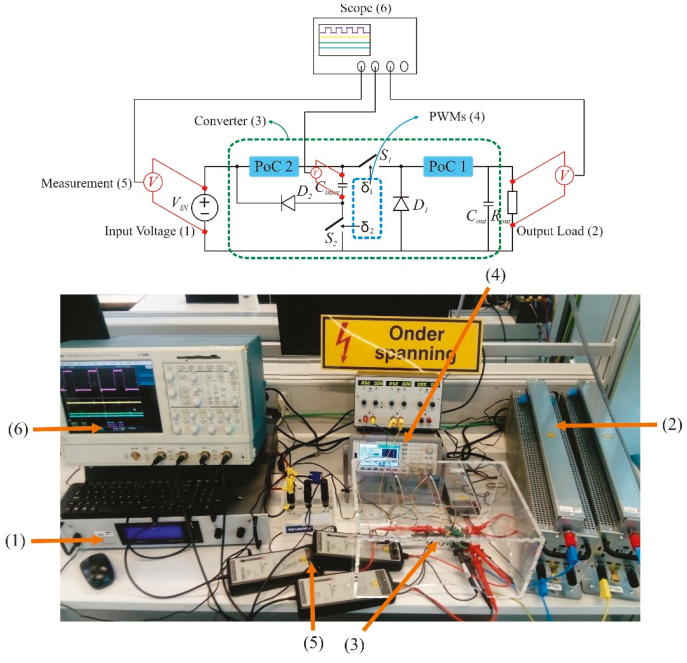

Figure 10. Test bench for experimental realization with (1) input source, (2) output load, (3) quadratic PoC converter, (4) PWM generator, (5) voltage measurements, and (6) scope.

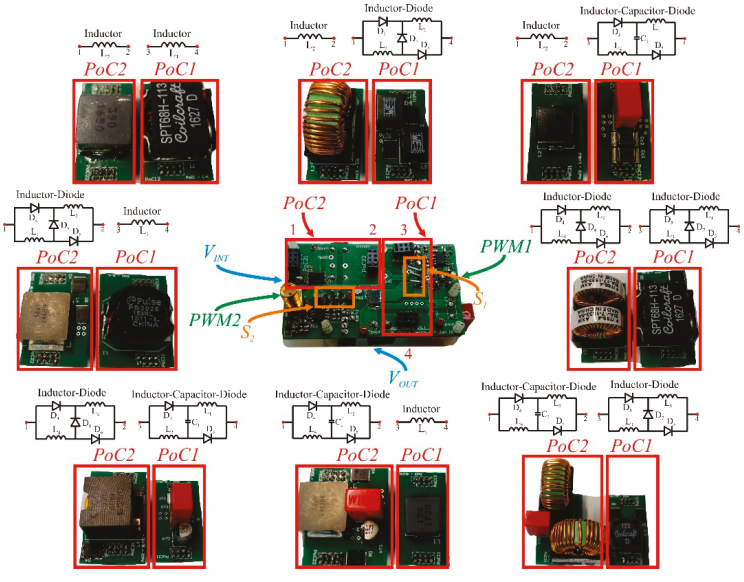

Figure 11. Converter realization (middle) surrounding by PoCs (PoC2 and PoC1) developed to experimental validation of the proposed topologies.

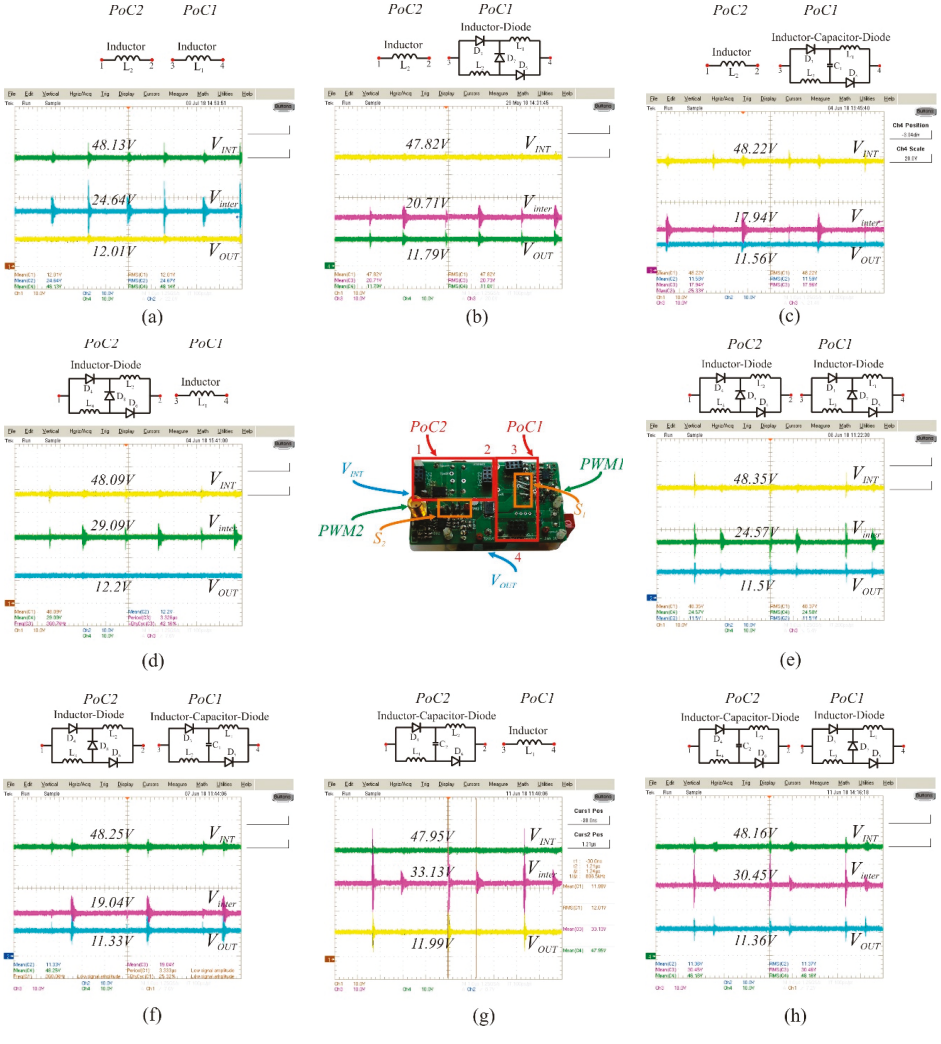

Figure 12. Voltage levels for different structures configurations. From top to bottom and left to right: (**a**) I-I with δ = 0.5; (**b**) I-ID with δ = 0.422; (**c**) I-ICD with δ = 0.366; (**d**) ID-I with δ = 0.422; (**e**) ID-ID with δ = 0.333; (**f**) ID-ICD with δ = 0.25; (**g**) ICD-I with δ = 0.366 and; and (**h**) ICD-ID with δ = 0.25.

As mentioned in Section 3, the gain analysis performed for the operation in region 2 and 3 results in the same gain expressions. The experimental results shown herein are for operation in region 3, but can be extended for the case when region 2 is in operation.

As discussed previously, is was shown that for different operating points and configurations connected in PoC2 and PoC1, different intermediate voltage levels are obtained for an input/output voltage of 48 V/12 V. This voltage, which varies from 33 V to 18 V depending the configuration, is available in the intermediate stage and can be used to supply loads in a broad range. Depending the required intermediate voltage, the best suited configuration can be selected to connect in PoC2 and PoC1. The ICD structure, as shown in Figure 5, limits the gain in the region between [0.5 ; 1], and can be used for a small voltage regulations with a certain accuracy. The ID structure, on the other hand, presents a nonlinear gain behavior in the range between [0 ; 1]. For the same duty cycle, this

structure can be used to achieve gains in between the regular buck with I structure and the buck with ICD structure, with the disadvantage of a nonlinear gain.

6.2. Region 1 ($\delta_2 > \delta_1$)

For operation in region 1, an extra PWM mode is performed between the normal PWM modes 1 and 2, during the switching period. This extra PWM mode guarantee the independence between stages 1 and 2, leading to the gain presented in Table 1 for all possible PoC configurations. We noticed that the intermediate gain depends only on the duty cycle δ_2, while the output gain is relate to duty cycles of both stages, since the converters are cascade connected.

Figure 13 shows the PWM modes for operation in region 1 for the I-ICD configuration. Nevertheless, this analysis can be extended for all configurations. As previously mentioned, an extra PWM mode arises during the switching period (PWM mode 2 in this analysis). Switch S_1—the component which is subject to the greatest voltage stress among the power components—as highlighted in Table 4, blocks only the intermediate voltage level during the switch transient between 'on' and 'off' while when operates in regions 2 and 3, the switch blocks the sum between the intermediate voltage and the input voltage. This phenomenon enables the reduction of switching losses in this component once the voltage that the component blocks during the switching transient has a lower value compared with the normal operation, although the maximum voltage that the switch needs to block remains in the same level as shown in Table 4.

Figure 14 presents an experimental verification of the stages discussed previously and shown in Figure 13. Figure 14a presents a waveform with the significant voltage levels of the circuit. As expected, an intermediate voltage of 19.5 V is achieved for a duty cycle of 40% applying the I structure in PoC2. Additionally, Figure 14a also presents the second voltage regulation stage made by the ICD structure connected in PoC1, operating with a duty cycle of 25%, in which a voltage of 11.2 V is achieved at the output of the converter. Figure 14b presents the PWMs applied to the circuit and its switching period, together with the input/output voltage of the circuit. As expected, input and output voltages are in accordance with the theoretical analysis above presented.

Finally, Figure 14c shows the experimental results of the voltage stress across the active semiconductors S_1 and S_2. For the same duty cycle abovementioned, the voltage stress across switch S_2 is independent of the operational duty cycle and equal to the input voltage, as shown in Figure 14c. Additionally, the stress across switch S_1 was also evaluated and presented in Figure 14c. It is verified that, as theoretically explained, the voltage that the switch blocks during transition between 'on' and 'off' stages is the intermediate voltage across C_{inter}, although the maximum voltage stress is related to the sum of input and intermediate voltages (verify PWM mode 3 between points 2–3 in Figure 13). Moreover, the switching losses generated by the overlap between current and voltage during the transition time decrease due to the lower blocking voltage during this transition. For operation in region 1, the addition of switch S_2 with independent duty cycle improves the flexibility of the system and decreases the switching losses across switch S_1.

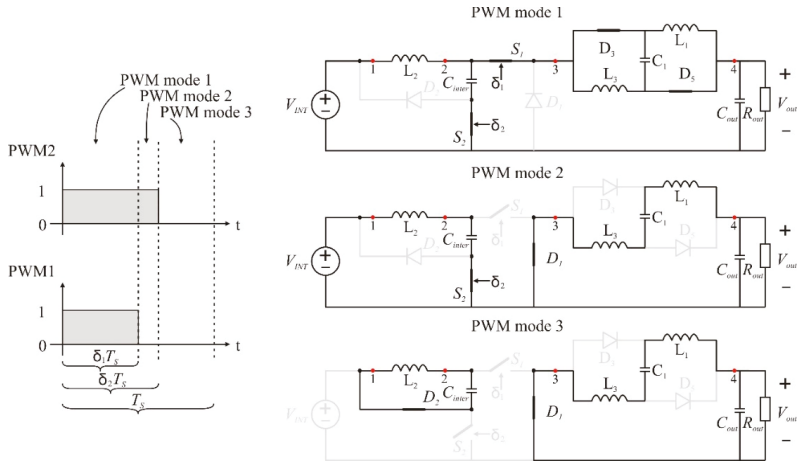

Figure 13. PWM modes with the equivalent circuits during one switching period when $\delta_2 > \delta_1$.

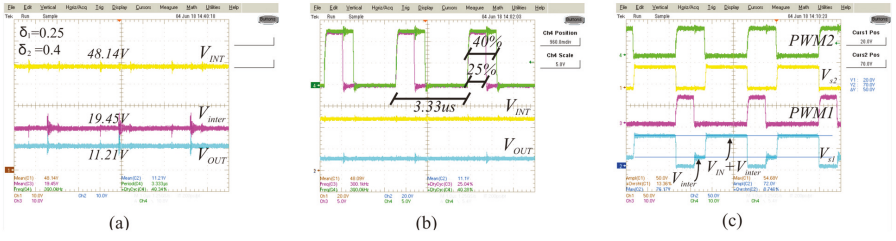

Figure 14. Experimental results for operation in region 1 for operation with $\delta_2 = 0.4$ and $\delta_1 = 0.25$ and switching frequency of 300 kHz: (**a**) input, intermediate and output voltages; (**b**) input and output voltages together with the respective duty cycles; and (**c**) PWMs and voltage stress across switches S_1 and S_2.

As discussed previously, the introduction of the ID and ICD structures in a step-down configuration (one-stage buck or quadratic buck) enable the possibility to change the voltage level of these structures. When applied in a one-stage buck converter, the ICD structure present similar voltage gain $\left(\frac{1+D}{2}\right)$ as the converter proposed in [50]. The structures, however, present different functionalities, since the abovementioned structure is a switched capacitor based converter with one switch, three diodes, one inductor, and three capacitors in the power stage while the structure, herein presented, is a switched inductor based topology with one switch, three diodes, two inductors, and one capacitor in the power stage. In terms of component part count number, the one-stage ICD structure present lower amount of components compared with the switched capacitor version that present similar gain [50]. The ID structure, on the other hand, presents a nonlinear step-down behavior with one extra diode and one less capacitor in the power stage (compared with the above-mentioned converters).

The ID structure is also explored in step-up configurations [39] and, when applied in a step-down structure, it changes the structure to a one composed by two inductors and two diodes, which leads to a gain of $\frac{D}{1+D}$, performing a higher step-down ratio them the ID structure. A topology with different switched capacitor/inductor structure is proposed for similar voltage gains [44] Comparing these topologies with the quadratic-buck configuration applying the ID and I structures (see Table 3), the gain of these structures is $\frac{2D*D}{1+D}$. The proposed structures, although implement more components in

the power stage, present a higher step-down ratio for duty cycles lower than 0.5. For duty cycles above 0.5, the proposed converter present lower step-down capability with higher component part count.

The one-stage buck converter present similar gain (D) compared with the quadratic buck applying ID and ICD structures in PoC1 or PoC2 (see Table 3). For a component part count point of view, the conventional buck converter present more benefits compared to the structures above-mentioned, since the conventional buck converter present the lowest part count structure for a DC–DC step-down configuration. On the other hand, the converters proposed herein present multiple output ports, e.g., intermediate and output voltages, and, according to the analysis presented herein, if a second switch S_2 is implemented, these voltage levels can be independently regulated (operation in Region 1), which is beneficial for an application point of view.

The major advantage that the topologies proposed herein have is the flexibility to adjust the intermediate voltage level according with the project specifications. The experimental results presented in Figures 12 and 14 show that, for the same input/output voltage, different intermediate voltage levels can be obtained depending on the operational regions (Region 1, 2, or 3) and the structure applied to PoC1 and PoC2. The main disadvantage, however, is the number of components in the power stage. When applied in a quadratic buck converters, the ID and ICD structures increase the number of semiconductor and magnetics in the power stage. This feature is undesired in some applications that power density is required, since extra space is required to place all the components. As previously mentioned, the ID and ICD structures are suited for lower voltage regulations and are not applicable if high step-down conversion ratios are required.

7. Conclusions

The analysis in this paper shows the influence of the ID and ICD structures, previously applied in step-up topologies, in a step-down configuration from 48 V to 12 V input-to-output voltage. To achieve the required voltage levels, a quadratic buck structure was implemented since the first analysis showed that the ID and ICD structures have a lower voltage regulation capability compared with the conventional I structure and, if a single stage buck converter is considered for application, the ICD structure cannot achieve the required output voltage level.

A complete theoretical analysis with PWM stages for all possible regions of operation, voltage gain, voltage/current profiles, and simulation is shown for all possible configurations generated by the substitution of the structures in PoC2 and PoC1. Voltage and current stress were evaluated for dimensioning and component selection to subsequently build the prototype for experimental validation. The analysis showed that the ID and ICD structures change the voltage and current profile depending on which PoC is connected. It is proven that the addition of a second switch S_2, together with the operation in Region 1, decreases the voltage stress during turn-off of switch S_1. The main advantage of the proposed approach is that the intermediate voltage level can be selected according to the application, since switch S_2 is implemented and the ID and ICD structures provide different voltage profiles that can be desired for specific operational duty cycles.

The main advantages of the proposed topologies compared to the conventional buck and quadratic buck converters are as follows.

(1) The addition of the second switch S_2 and the possibility to choose between I, ID, and ICD structures to connect in PoC2 and PoC1, increase the flexibility of the circuit, resulting in a broad range of intermediate and output voltage levels.
(2) The circuits with ID and/or ICD feature diode and inductor redundancy, which leads to lower current stress and a fail-safe structure, after all, if one diode/inductor fails in open-circuit, the system can still maintain its functionality but with limited power.
(3) The implementation of S_2 also increase the number of regions of operation, since region 1 is now a possible region of operation. In this region, the blocking voltage of switch S_1 decreases from $V_{IN} + V_{inter}$ to only V_{inter}, as shown in Section 6.

A test bench was assembled and experimental results showing that the ID and ICD structures can be used for small voltage adjustments in a step-down application were presented. Simulation and experimental waveforms were presented to validate the theoretical analysis in Section 4. The ID and ICD proved to be effective structures for applications where small voltage adjustments are required, but did not prove being useful solutions when a high step-down voltage level is required due to its gain characteristics.

8. Patent

A patent related to this work was filled in on the 15th of May 2018, with application number GB1807795.8 at the UKIPO (reference [47]).

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Review

Challenges and Design Requirements for Industrial Applications of AC/AC Power Converters without DC-Link

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Abstract: AC/AC converters that do not have a DC energy storage element, such as a matrix chopper and a matrix converter, are increasingly becoming alternatives to conventional two-stage AC/DC/AC converters and thyristor choppers. In such systems, the main DC-link capacitor does not exist, so the system provides more reliable operation and makes it possible to reduce the financial costs of its construction. It should be noted that AC/AC converters without an energy storage element in a form of DC-link capacitors have not been implemented on an industrial scale. The reasons involve technical aspects and cost components. The main aim of this paper is to present some of the challenges and selected design requirements for industrial applications of AC/AC high reliability power converters.

Keywords: power electronic converter; AC/AC converter; matrix converter; reliability

1. Introduction

The development of power electronic converters has led to them being applied in various areas of life, such as: industrial and household applications, renewable energies, Flexible AC transmission systems and micro grids, as well as automotive and transport applications. In the development of power converter topologies, much more attention is being paid to the, reliability [1,2] efficiency and robustness of power electronics converters [3–6]. Automotive industry and transport have very strict reliability requirements in power electronics systems due to safety requirements. Moreover, the industrial and energy sectors are striving for improvement in the efficiency and robustness of power electronics systems. Likewise, home solutions are often designed as economical and sustainable eco-friendly devices. Additionally, some novel devices have a smaller size, and have achieved higher power density and robustness for very high loads. This is a general trend in all areas of technology. High power density, higher switching frequency, and reduced overall dimensions of passive components and power electronic converters are possible due to the use of power transistors made using silicon carbide (SiC) or gallium nitride (GaN) technology [7–10].

In low-voltage industrial systems, the most commonly used topology is the unidirectional AC/DC/AC converter. The bidirectional (four-quadrant) structure of such a converter is a system called a back-to-back converter (B2B) (Figure 1) [11]. The power stage of converters contains power transistors with a heatsink and heat dissipation system, a DC-link capacitor, an input filter to provide a unit input power factor, and measurement and control units. In medium-voltage industrial systems, multilevel converters with DC-link are commonly used [12,13]. Multilevel converters offer numerous advantages compared with the two-level converter, e.g., better power quality and lower switching losses, low transistor voltage stress, and high voltage capability. It is evident that the multilevel converters will be used for medium voltage or high power electronic systems. However, in general terms, it can be concluded that the two-level converters will be used in low-voltage systems with lower power. In addition, the specialized design of low voltage power electronics converters using

SiC or GaN semiconductors, with the optimization of cooling systems, enables the construction of power plants with high efficiency or power densities. In the last decade, apart from the development of power electronics devices, there has also been a significant development of capacitors used in DC circuits. Aluminum electrolytic capacitors are probably the most common capacitors used in the DC-link circuits of modern power electronic converters. In addition, other technologies employed in the production of such capacitors are the multi-layer ceramic structure or the metallized-polypropylene structure [11]. Despite the significant reduction in the dimensions of modern capacitors used in DC circuits, these capacitors still constitute the main component increasing the dimensions, weight, and price of power converters. Furthermore, the capacitor is the component that is most often damaged due to disturbances from the power grid and as a result of improper operation. Figure 2 shows the elements that are most often damaged in circuits of power electronic converters [1,2,14]. For this reason, the most common electrolytic capacitors are the cause of the premature shortening of the lifespan of the converter device [11]. The ageing of DC-link capacitors is manifested by the increase in their equivalent series resistance R_{ESR}. The heating up of the electrolyte and its consequent evaporation and deterioration of electrical parameters is the most significant factor in the degradation of the electrolytic capacitor. One of the main reasons for the increase in capacitor temperature is the ripple of the capacitor current. In addition, the second most critical parameter for the failure of the capacitor is its voltage capacity, usually determined by the rated voltage or operating voltage, surge voltage, or allowed short-term maximum voltage. The voltage parameter is so critical that exceeding its nominal values for a few tenths of a second can cause an immediate failure or significantly accelerate the degradation of capacitor nominal parameters. For the presented reasons, in power converters, especially high power ones, particular attention is paid to environmental and operational conditions affecting their lifespan, with special emphasis on DC-link capacitors.

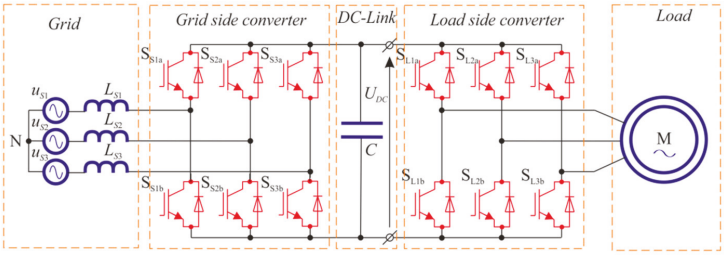


Figure 1. Two-level back-to-back converter with DC-link.

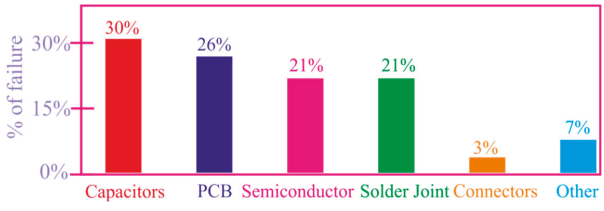


Figure 2. Distribution of faults in power electronic converters [14].

The development of power converters that do not have large capacitors in their structure (DC-link) is an interesting solution to reduce their cost and size. In addition, this can achieve greater reliability and thus extend their operating time [15–18]. Such converters are often considered an alternative solution for atypical applications and are not found in many industrial applications. One of the main reasons concerns technical aspects related to the small number of available and dedicated semiconductor power devices, as well as DSP processors with a sufficient number of PWM outputs and A/D converters.

An additional difficulty is undoubtedly the complex algorithms for modulation of the switch control function and transistor current commutation.

AC/AC converters without DC-link capacitors have several topologies with different functionalities. One of the main functionalities is the possibility to change the frequency of the output current/voltage ($f_L = const$ [16], $f_L = var$ [15–18]). In addition, different structures of AC/AC converters are distinguished, such as direct and indirect (with a fictitious DC-link) topology. An example of an AC/AC converter without an intermediate circuit capacitor and $f_L = const$ is a matrix controller (matrix chopper), whereas $f_L = var$ is a matrix converter.

This paper will present a review of current commercial applications of the AC/AC converters whose topologies do not have a DC energy storage element (capacitor or inductor). Particular attention will be paid to the technological issues and barriers concerning the design of such converters. In addition, possible construction solutions as well as potential applications will be indicated. The originality of this research is in the presentation of requirements and challenges for practical or future-proof applications of AC/AC high-reliability power converters. The paper includes (1) a review of semiconductor power elements dedicated to the discussed converters, (2) an indication of expectations regarding integrated intelligent modules and new SiC technologies, and (3) an indication of the development of modern control techniques (e.g., model predictive control (MPC)). In addition, new application possibilities of the discussed converters in AC power systems, (e.g., compensators for voltage changes) are indicated and their beneficial properties are discussed.

2. Description of Selected Topologies

The analysis presented in the article will be based on topologies of two converters: a matrix controller (chopper) and a matrix converter. Based on these, the main design problems and limitations related to the available components and the industrial application will be indicated.

One of the basic applications of AC/AC choppers, as an alternative to thyristor choppers, is in electric drive systems used as a soft-start for an AC motor. Issues with industrial temperature control and lighting intensity control are the further areas of AC/AC chopper application. A schematic diagram of the three phase AC/AC matrix controller power circuit is presented in Figure 3a [16]. The system consists of six bidirectional switches. Three switches are connected to the input terminals, while the other three are connected in parallel to the load. Control of the switches is carried out by means of the PWM signal (Figure 3b), and a duty cycle determines the RMS value of the output voltage. In addition, the choppers have an input low-pass filter to eliminate the higher harmonics components of the current drawn by the converter, which result from the frequency of the PWM signal. The second kind of structure based on the chopper shown in Figure 3a is the matrix-reactance chopper, which also enables the increase in amplitude of the output voltage [19] as well as various other types of compensators for AC voltage fluctuations in the power grid [20,21].

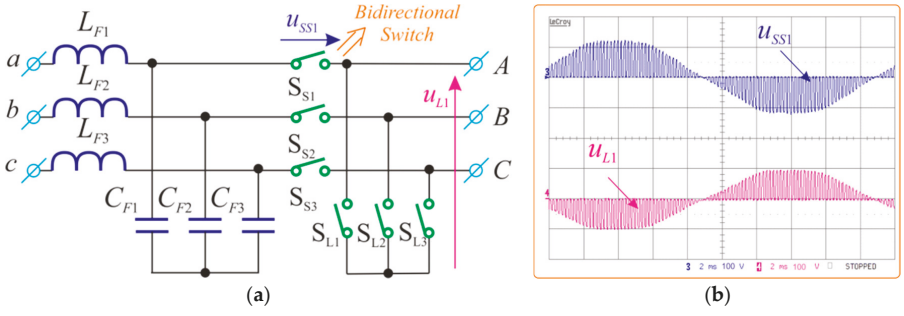


Figure 3. AC/AC controller: (**a**) main circuit; (**b**) voltage time waveforms.

The main advantages of the AC/AC chopper compared to the classic thyristor chopper are derived from the sinusoidal current drawn from the mains, and the use of LC output filters to obtain sinusoidal output voltages. Such properties allow one to work with the unit input power factor and use these choppers in systems of electricity conditioners [20,21]. The high switching frequency of the power transistors makes it possible to minimize the sizes for the input and output LC passive filters. The disadvantage of chopper devices is the increased internal losses resulting from the large number of power transistors and the necessity of using additional snubber devices on each of the power electronics switches or of using overvoltage protection of bidirectional switches with a clamp circuit [16,22].

The most widely known of frequency converters (f_L = *var*) without DC-link is the matrix converter (MC) in its direct topology shown in Figure 4a [15–18,22–24]. Generally, in three-phase systems, the MC consists of nine bidirectional switches connected in a matrix—each input is connected to each output. Similar to the matrix controller, there is an input low pass filter in the MC topology that fulfills identical functions. MC output voltages are formed from pieces of input voltages, shown in Figure 4b, as exemplary experimental time waveforms.

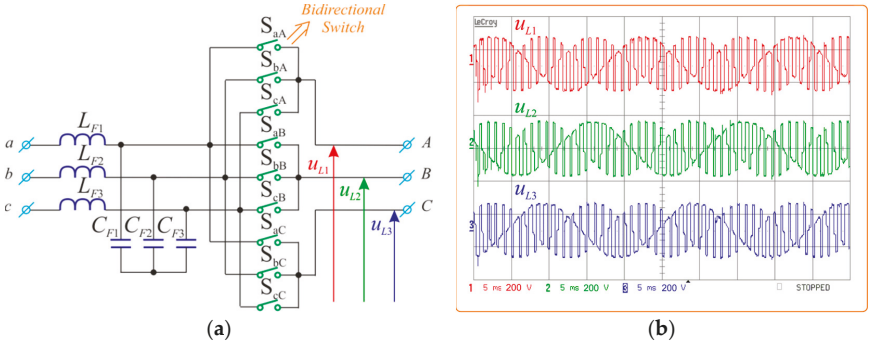


Figure 4. Matrix converter: (**a**) main circuit; (**b**) voltage time waveforms.

The MC is a four-quadrant topology with adjustable input power factor and a sinusoidal shape of input and output currents. In addition, the MC is a fully semiconductor device without large capacitor circuit capacitors. Similarly to chopper devices, there is a necessity to use additional overvoltage protection of bidirectional switches with a clamp circuit, where small capacitors accumulating commutation voltage spikes should be used. The disadvantages of the MC are the large number of power transistors and the associated complex control and switching strategies. In addition, the voltage gain of MCs does not exceed 0.866, which, for applications in variable speed drives, requires the use of motors with lower rated voltages.

In both MC and AC/AC chopper topologies, the main elements are bi-directional power electronic switches. These switches allow switching of both the positive and negative sine wave of the supply voltage and, in the case of the MC, the bi-directional power flow. Bidirectional switches, as will be discussed in the next section, have a configuration of transistors and diodes other than those used in classical, commonly used voltage inverters. Therefore, the commercial development of available bidirectional switches in various configurations is important for the development of AC/AC converters without DC-link circuits.

3. Design, Construction, and Implementation Barriers

The development of AC/AC converters encounters problems related to misunderstanding the specificity of their operation, especially in the context of MCs. In this chapter, basic construction problems and development barriers related to technological differences in relation to commonly used

frequency converters will be indicated. Barriers hindering development include, among others, a lack of semiconductor components in more complex modules than single transistors, a specific distribution of control signals, a complex transistor switching strategy, and a large number of measuring sensors. However, in spite of these problems, this chapter will indicate the first commercial applications of AC/AC converters without DC-link and provide guidelines for the modular construction of intelligent power modules that would significantly contribute to the development of this technology. An important development impulse may also be the implementation of control methods that are developed for other topologies such as model predictive control. The number of topics discussed in this chapter results from the need to indicate both the application potential and difficulties in designing the discussed converters.

3.1. Power Semiconductors

As already mentioned in the previous chapter, bi-directional switches are used in the discussed converters. Basic configurations of such bidirectional switches made in Si technology are presented in Figure 5. Such configurations of Insulated Gate Bipolar Transistor (IGBT) transistors and diodes allow conducting currents in both directions and blocking voltages for positive and negative polarity.

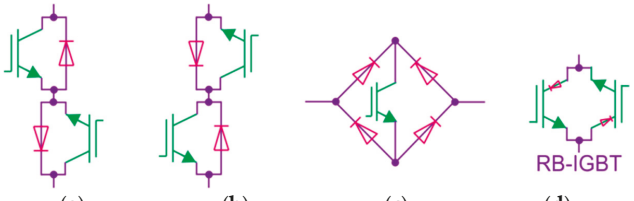


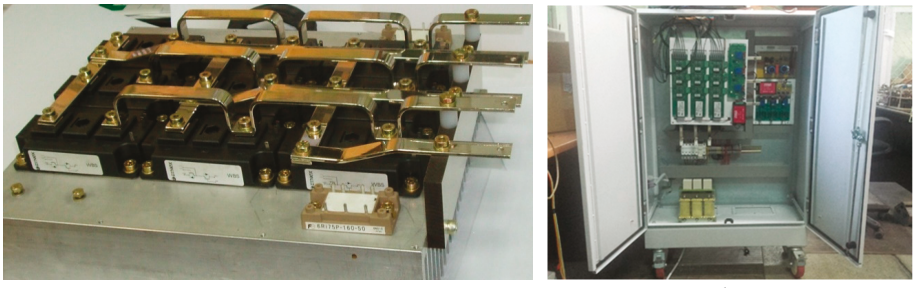
Figure 5. Bi-directional switches: (**a**) Common emitter IGBT, (**b**) common collector IGBT, (**c**) IGBT with a diode bridge, and (**d**) RB-IGBT reverse blocking IGBTs.

3.1.1. Si Semiconductors

AC/AC converters are full semiconductor systems and must be constructed of bi-directional switches. For power converters commonly used in industry, there are many developed modules containing complex structures on the market for the transistors or diode connections. However, for AC/AC converters, there are very few commercially available semiconductor modules that have bi-directional switches in their structure. As shown in Figure 5, the most commonly used configurations of bi-directional switches are IGBTs with anti-parallel diodes (two topologies, a common collector, and a common emitter). In addition, there are switches with a diode bridge and a single IGBT transistor, and reverse blocking IGBT (RB-IGBT), where anti-parallel diodes can be eliminated [21]. It is possible to build bi-directional switches with a combination of various discrete elements, but the creation of advanced power electronic devices in the form of integrated power modules facilitates a reduction in dimensions of the converter, allows higher power densities, and produces high reliability. Few examples of power modules for the bidirectional switches or complex structures are currently available on the market, though some of these modules are now commercially available. Table 1 lists the selected of manufacturers that have commercially available power modules with bi-directional switches.

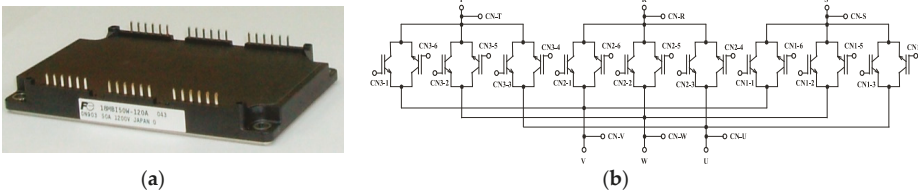
The first example of the use of bi-directional Dynex Semiconductor switches with rated parameters of 1.2 kV and 200 A is illustrated in the structure of the matrix converter shown in Figure 6. An example of a structure containing a single housing topology of a matrix converter with RB-IGBT transistors is the module presented in Figure 7. The module is manufactured by the FUJI Electric company and its nominal parameters are 1.2 kV/50 A. As generally known, in addition to the power element, a dedicated transistor gate driver is also needed. In this case, designers can use existing drivers used in other converter topologies. However, there are dedicated drivers for available bi-directional modules. Examples of such dedicated drivers include Concept [14] drivers for Dynex switches (Figure 8a)

and Semicron drivers and transistors presented in Figure 8b,c. These are examples of bi-directional switches. In the catalogues of other semiconductor companies, such solutions are found often and with increasing frequency. Based on the above review, it can be said that the number of dedicated components is gradually increasing over time. It should be noted that, without systematic growth of proposals for new, dedicated components for the design and construction of AC/AC converters, there will be no significant development of these topologies. The main direction of development should be to reduce component costs and increase their reliability.



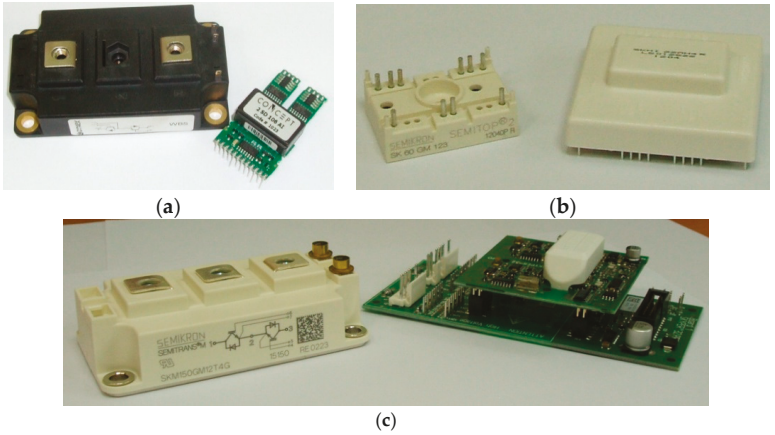
(**a**) (**b**)

Figure 6. MC construction: (**a**) Dynex 1.2 kV/200 A IGBT; (**b**) a built-in MC structure in the control cabinet.



(**a**) (**b**)

Figure 7. Matrix-connected RB-IGBTs module: (**a**) photograph; (**b**) topology structure.



(**a**) (**b**)

(**c**)

Figure 8. A photograph of the IGBTs with dedicated drivers: (**a**) Dynex IGBT with Concept driver; (**b**,**c**) Semicron drivers and IGBTs.

Table 1. Available, selected commercial modules with bidirectional switches.

Switch Model	Characteristic	Manufacturer	Number of Bidirectional Switches
DIM200MBS12-A	1.2 kV/200 A	DYNEX	1
DIM400PBM17-A	1.7 kV/400 A	DYNEX	1
DIM600EZM17-E	1.7 kV/600 A	DYNEX	1
SK 60GM123	1.7 kV/60 A	SEMICRON	1
SKM 150GM12T4G	1.2 kV/60 A	SEMICRON	1
SML150MAT12	1.2 kV/150 A	SEMELAB	3
SML300MAT06	0.6 kV/300 A	SEMELAB	3
18MBI50W-120A	1.2 kV/ 50A	FUJI	9
18MBI100W-060A	0.6 kV/100 A	FUJI	9
18MBI100W-120A	1.2 kV/100 A	FUJI	9
18MBI200W-060A	0.6 kV/200 A	FUJI	9

3.1.2. SiC Semiconductors

Thanks to the development of semiconductor power electronics with silicon carbide (SiC), which has certain advantageous features such as high temperature operation, low losses, and higher switching speeds, a full power electronic converter structure has also been developed. Moreover, thanks to the semi-conductor being made using SiC technology, a further improvement in the converters power density can be achieved. Because this is a technology that has not fully achieved technological maturity, there are some problems in the implementation of power converters with SiC devices due to the high speed of switching devices and the design of devices for the gate drive.

The most promising SiC devices are the normally-off SiC JFET, SiC MOSFET, and SiC BJTs. The bi-directional switch topologies in SiC technology are shown in Figure 9. Potential improvements regarding the efficiency and performance of SiC components in the context of bi-directional power electronics switches are reported in [24–27]. As demonstrated by existing research, the use of transistors made in SiC technology enables a significant increase in the efficiency of converters for switching frequencies of several dozen kHz. Sample results illustrating the beneficial properties of SiC transistors, taken from [24], are presented in Figure 10.

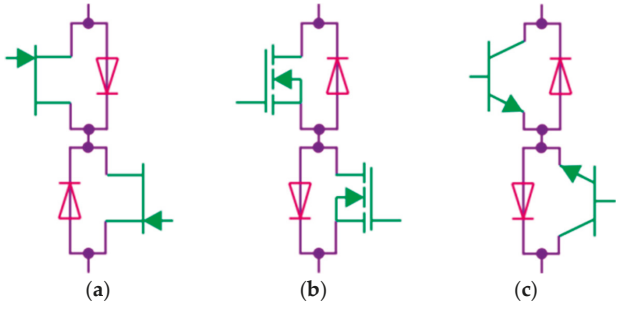


Figure 9. Main topologies for SiC bi-directional switches: (**a**) common drain anti-paralleled JFET, (**b**) common source anti-paralleled SiC MOSFET, and (**c**) common emitter anti-paralleled SiC BJT.

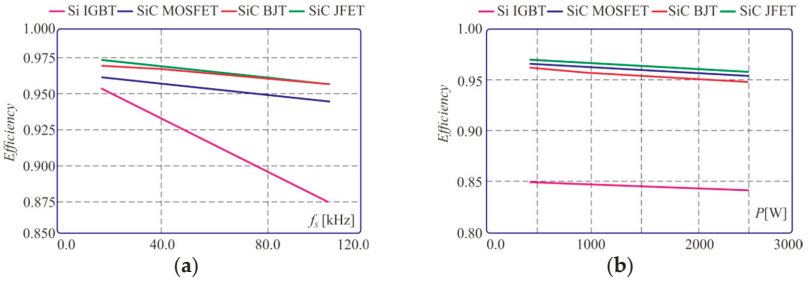


Figure 10. Illustration of the beneficial properties of the use of SiC transistors, taken from [24], presents the efficiency of a two-phase to single-phase 2.5 kW MC in Si and SiC technology (**a**) as a function of switching frequency at T_c = 125 °C and (**b**) as a function of power at f_s = 100 kHz, T_c = 125 °C.

3.2. Control Units

The MC power stage circuit is made up from a table of nine bi-directional switches which provides a total of 18 transistors. The specificity of the MC construction also requires the generation of a PWM switching sequence. In addition, special attention should be paid to maintaining a safe current commutation strategy when the transistors are switched. An additional difficulty in the modulation process of the transistors control functions is the distribution of control pulses in a single period of the control sequence T_{Seq}. Since there are three bidirectional switches connected in one output branch (six transistors) and two or three of them cannot be switched on simultaneously, the switching sequence will be responsible for three switching operations during one period T_{Seq} (Figure 11a). In the classic bridge voltage inverter, for a single branch, there are two transistors working alternately. A pair of complementary control signals are then generated and are negated in relation to each other (Figure 11b). In addition, additional dead times (dead-band) are used to ensure correct current commutation. Modern DSP processors and microcontrollers have built-in PWM modulators that generate complementary control signals that occur in classic bridge voltage inverters with built-in dead time generation functions [28]. The control implementation for the matrix converter using built-in PWM modulators is not simple and requires either multiple-core systems (at least two) or additional logic circuits. It is also possible to solve this problem using software I/O outputs instead of built-in PWM modulator procedures. These are, of course, more complicated solutions than in the classic branches of the inverter bridge.

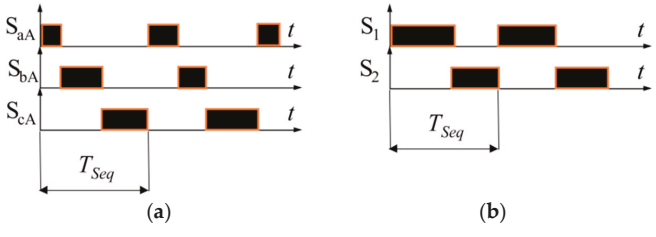


Figure 11. Distribution of control pulses in a single period of the control sequence T_{Seq}: (**a**) in the phase leg of a matrix converter, (**b**) in the phase leg of a classical inverter.

In addition to the algorithm for the modulation of switch control signals in the MC, it is necessary to use complex current switching algorithms for transistors. Several commutation strategies can be found in the scientific literature [17,21], where the most widely known is the four-step current commutation strategy. In this method, the current direction in the output line is used to determine switching sequences of transistors. The commutation process for one output phase is shown in

Figure 12a. An analogous switching pattern occurs between any transistors in each MC output stage. Examples of control sequences obtained at the FPGA output are shown in Figure 12b.

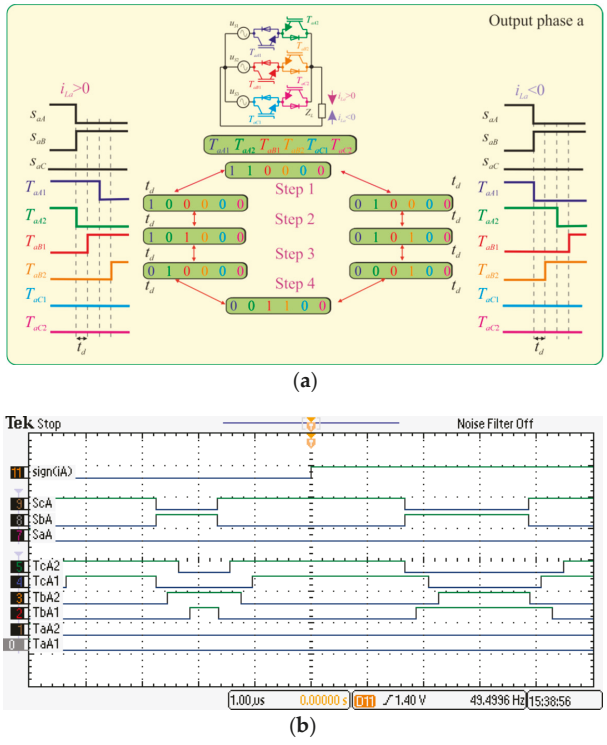


Figure 12. Four-step commutation process in one output phase of the MC: (**a**) switching diagram; (**b**) control signals from FPGA devices.

The digital implementation of the two presented algorithms of modulation and commutation requires the use of complex computing systems often combining DSP and FPGA devices. [29]. The control algorithms for a given application (electric drive, voltage compensator, etc.) and modulation algorithm are in most cases implemented in the DSP, while the FPGA, observing safe commutation rules, is used in the part related to the separation of control signals and transfer to individual transistors, so as to perform additional tasks to supplement the DSP function.

A significant limitation preventing faster development of AC/AC converters, such as MCs, is the large number of transistors and hence the need for DSPs with a large number of PWM outputs. The solution to this problem may be the rapid development of FPGAs, which has occurred in recent years. In the scientific literature, first articles related to the implementation of complete MC control algorithms implemented solely on FPGA have appeared [30,31]. Such an implementation is much more difficult when advanced mathematical functions such as trigonometric functions are used. Additionally, I/O systems in particular should be defined using a software solution, especially those related to cooperation with A/D and D/A converters. Nevertheless, parallelism and the speed of calculation means that FPGAs can replace DSP processors.

3.3. Measurement of Voltages and Currents

In order to correctly implement the control, modulation, and commutation algorithms in MCs, it is necessary to measure the values of voltages and currents [21,32]. Measured voltage and current signals

are used, among others, in (1) semisoft commutation strategies, (2) fault detections, (3) modulation process (e.g., SVM), (4) phase-locked loop (PLL) units, (5) current loops in control algorithms, and (6) the clamp protection circuit. The measuring transducers should ensure galvanic isolation between the measured signals and the components of the control system and match the level of signals to the A/D converters. The most popular voltage and current measurement devices are LEM type transducers [33]. Of course, there are also many other manufacturers of this type of device, e.g., ABB, Honeywell, Allegro Microsystems, and Chen Young [34]. Transducer devices are quite expensive, so the measurement of voltages or currents can also be made on the basis of differential and isolated amplifiers, which are cheaper. Devices with galvanic isolation use optical, capacitive, or inductive insulation barriers. Table 2 presents examples of voltage and current measuring amplifiers as well as selected types of transducers [34].

Table 2. Selected available voltage and current measurement amplifiers and transducers.

Model	Isolation/Operation	Manufacturer	Type
HCPL-7860	Optic	Avago Technologies	Current
HCPL-786J	Optic	Agilent	Current
HCPL-7800	Optic	Avago Technologies	Current
ISO124	capacitive	Texas Instruments	Current/Voltage
ISO120/121	capacitive	Burr-Brown Corporation	Current/Voltage
INA270	difference amplifier	Texas Instruments	Current
LM358	difference amplifier	Texas Instruments	Current
AD8210	difference amplifier	Analog Devices	Current.
ACS752SCA-100	magnetic	Allegro MicroSystems	Current
ACS756xCB	magnetic	Allegro MicroSystems	Current
LV-25	magnetic	LEM	Voltage
LTS 25-NP	magnetic	LEM	Current
MP25P1	magnetic	ABB	Current
VS500B	magnetic	ABB	Voltage

One of the more precise issues related to the measurement of currents in AC/AC converters is the detection of its direction needed to ensure correct commutation of the tan resistors [21]. Due to the inductive nature of the load and the switched output voltage, the currents in the circuits of AC/AC converters contain higher harmonics. Therefore, accurate determination of the current direction is an issue requiring either advanced software algorithms or additional electronic circuits. The software solution for determining the current direction can be implemented using the network voltage synchronization algorithms (PLL) [35]. It is also possible to use an additional electric circuit that will perform the function of determining the current direction in a hardware manner. An example of such a solution based on a zero-crossing detector is shown in Figure 13 [36].

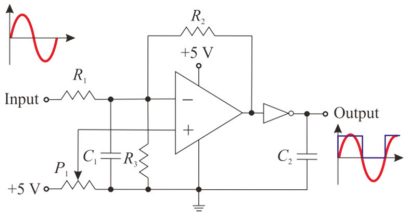


Figure 13. Circuit diagram of the zero-crossing detector.

3.4. Commercialization of Prototype Solutions

The first major challenge for AC/AC converters without a DC-link element is the commercialization of the semiconductor components and other elements necessary for their design and implementation.

The market situation of the semiconductor switches is discussed in Section 3.1.1. A growing number of dedicated semiconductor modules is visible. However, is this enough for faster development of power converters? This question is important because despite the growing interest in scientific research in this field, there are few AC/AC converters without DC-link available on the market. One of the first manufacturers of matrix converters is the Yaskawa Electric Corporation [32]. The Yaskawa products of an MC include low-voltage and medium-voltage solutions. The low-voltage MC solution is the classic matrix converter shown in Figure 7a. The classic MC product portfolio has two voltage levels: 200 V (from 9 to 63 kVA) and 400 V (from 10 to 114 kVA) [32]. In contrast, the solution for medium voltage is designed as a multi-level structure (Figure 14a). It uses a three-phase to single-phase MC structure as a basic power block (Figure 14b). By combining three blocks in series, a phase voltage three times higher than the voltage of a single module can be obtained (Figure 14a). The multilevel MC has similar features to the classical matrix converter. The medium voltage MC product portfolio has two voltage levels: a 3.3 kV level ranging from 200 to 3000 kVA and a 6.6 kV level from 400 to 6000 kVA [32].

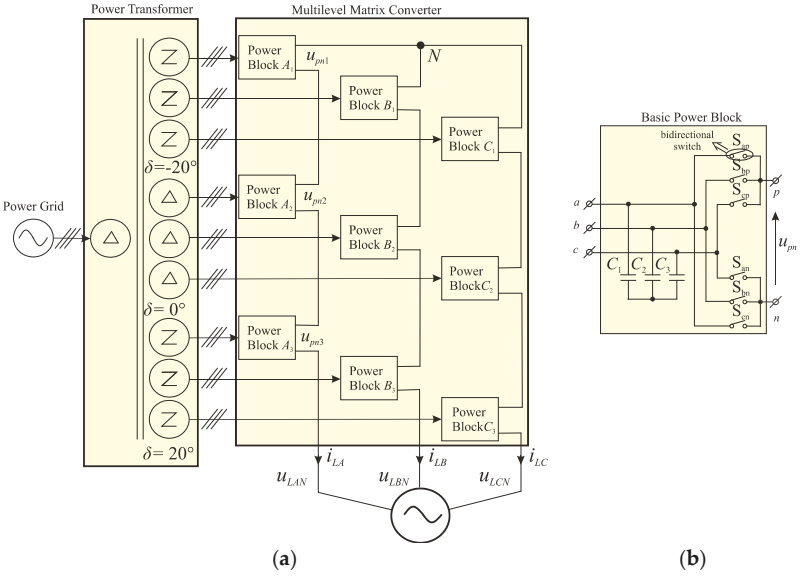


Figure 14. Multilevel, medium voltage matrix converters: (**a**) a multilevel MC with nine basic power switch blocks; (**b**) a three-phase to single-phase (3 × 2) MC power block.

3.5. Modular Construction

In commercially available modules dedicated to the discussed converters, there are no solutions for intelligent modules with power semiconductors, protection devices, drivers, or measurement sensors in their structure. This subsection indicates the expectations regarding this type of intelligent solution based on previous experience.

The power-electronic building block (PEBB) is the concept of building converters from basic modules. The effect of this approach is to increase the reliability and dimensions of power electronic converters [37,38]. The PEBB concept is used to integrate the following components into one module: power supply devices, gate drives, communication interfaces, measuring sensors, snubber protection circuits, and other components necessary for the proper operation of the converter. The concept of the PEBB offers a means for hardware standardization of power electronics systems.

In the analyzed AC/AC power converters, depending on the topology, there are several basic blocks presented in Figure 15. Figure 15a is the most widely used single bidirectional switch structure,

which consists of two active switches and two diodes anti-parallel with them. Practical implementation of such a basic block can be realized by using power electronic switches with the dedicated driver systems that are shown in Figure 8. Figure 15b shows a basic structure for a single leg of the matrix converter structure. This basic block may be used for the construction of both the classical MC (Figure 4a) as well as the multilevel MC (Figure 14). Two prototypes of power module in such configurations as SML150MAT12 and SML300MAT06 are proposed and presented in Table 1. Another basic block from Figure 15c is the arrangement of a three-to-single phase MC, which can be used in a multilevel MC (Figure 14) or can be operated as a rectifier [39]. The most complex block power is the whole structure of the MC in a single device shown in Figure 15d. Manufacturers of semiconductor power devices offer several of these dedicated structures, as shown in Table 1.

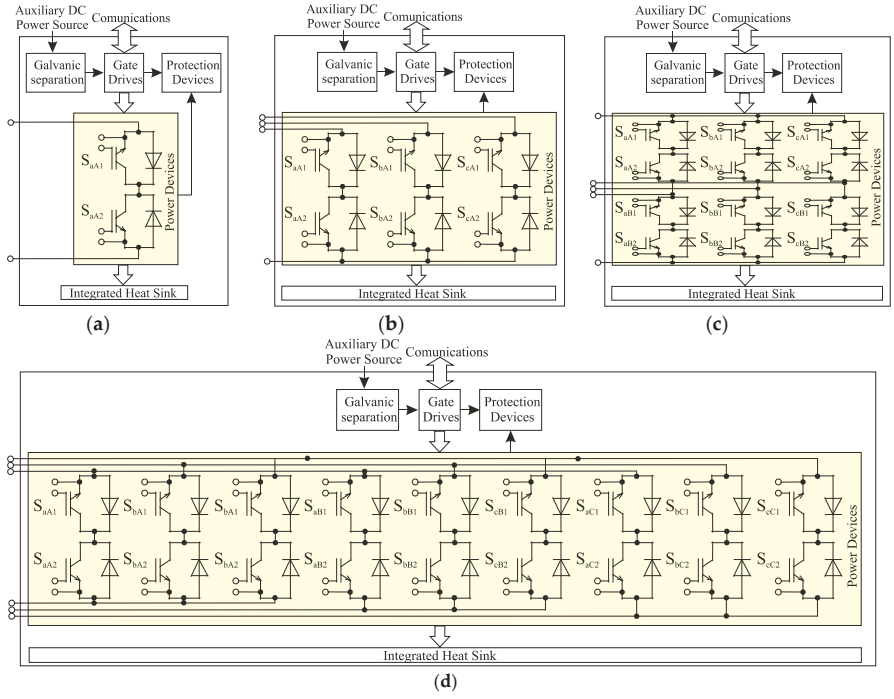


Figure 15. Common switching structures for power-electronic building blocks (PEBBs) in AC/AC power converters (**a**) single bidirectional switch structure, (**b**) single output phase of MC switch configuration, (**c**) two phase of MC switch configuration, (**d**) three phase of MC switch configuration.

3.6. The Development of Modulation Methods

The development of varied technologies is related to the possibility of following the evolving trends in technology. In this subsection, it is shown that, in the discussed topologies, it is possible to implement recent commonly developed methods of predictive control.

Modulation strategies in AC/AC converters without capacitors in the intermediate circuit are not a simple issue due to the high number of transistors. AC/AC choppers have much simpler modulation strategies. Most modulation techniques have been determined for classical, direct MCs, and they are presented in a review article [22]. In recent years, MPC has been the best developed method of modulation. At discrete time T_d, MPC examines a model of a controlled system and predicts its condition in the next step. The configuration of converter switches is selected to ensure a minimum value of the cost function [40]. Scientific publications with MPC of an MC show better

achievements in the quality of current and voltage waveforms, torque ripple, and internal switching power losses [30,41,42]. An example MPC scheme for the MC is shown in Figure 16, and this example is one that minimizes the cost function related to the accuracy of shaping the output current and the input power factor. Development of predictive control methods in AC systems without DC-link capacitors is a future area of extensive conceptual and implementation research.

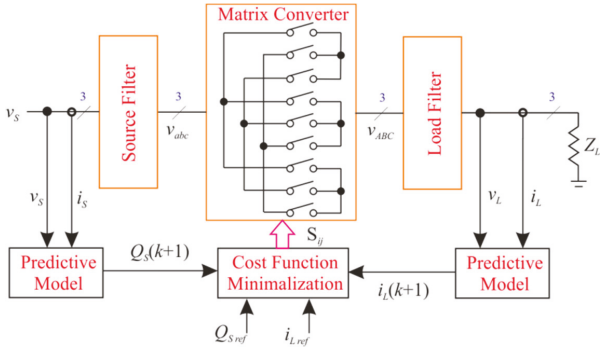


Figure 16. Model predictive control (MPC) of an MC with minimalization of the output current ripples and input power factor (reactive power).

The AC/AC chopper modulation algorithms are not complicated and are based only on the change in the control pulse duty factor. Research on control algorithms is mainly related to increasing efficiency, identifying faults, and optimizing their operation during component failures. New system structures are also being developed that produce significantly better properties regarding efficiency and power density [43,44].

4. Novel Applications of AC/AC Converters without DC-Link Capacitor

The classic application of frequency converters such as the matrix converter is to variable speed electric drives, while the AC/AC choppers are used in applications such as industrial process heating, the control of lighting intensity, or the soft-start of an induction AC motor. These applications are ubiquitously described in the literature and will not be analyzed in this article.

New potential areas for the application of choppers and AC/AC frequency converters without a DC-link circuit are in such devices as compensators for voltage fluctuations in the electric power grid and power flow controllers [19,45,46]. An example of such a compensator with a power flow control function is the hybrid transformer (HT) with a matrix converter or a matrix chopper [45,46], which is shown in Figure 17. The HT contains two main units: (1) a conventional three-phase transformer with two pairs of secondary windings and (2) a three-phase AC/AC converter. The first pair of output windings supplies the converter, whereas the second pair is connected in series with the output terminals of the converter. The compensating voltage is generated at the output of the converter. The output voltage of the whole HT is the sum of the power converter output voltage and the second secondary winding voltage of the transformer. The output terminals of the HT are connected with a sensitive load or a protected small industrial plant. The disadvantage of the HT is the necessity of using transformers with two pairs of secondary windings. Furthermore, under normal supply voltage conditions, the inverter can be switched off, resulting in this part of the transformer generating additional power losses.

A hybrid transformer with a matrix chopper allows compensation only for the amplitude of the supply voltage; using a matrix converter, it is possible to compensate for both symmetrical and asymmetrical voltage changes as well as harmonic distortions. As an example, to illustrate the beneficial properties of an HT with an MC, the results of the MPC algorithm (Figure 18) are presented

in Figure 19 [47]. As can be seen from Figure 19, the output voltage of the compensator is kept at a constant amplitude with no harmonic distortion, despite large fluctuations in the main voltage.

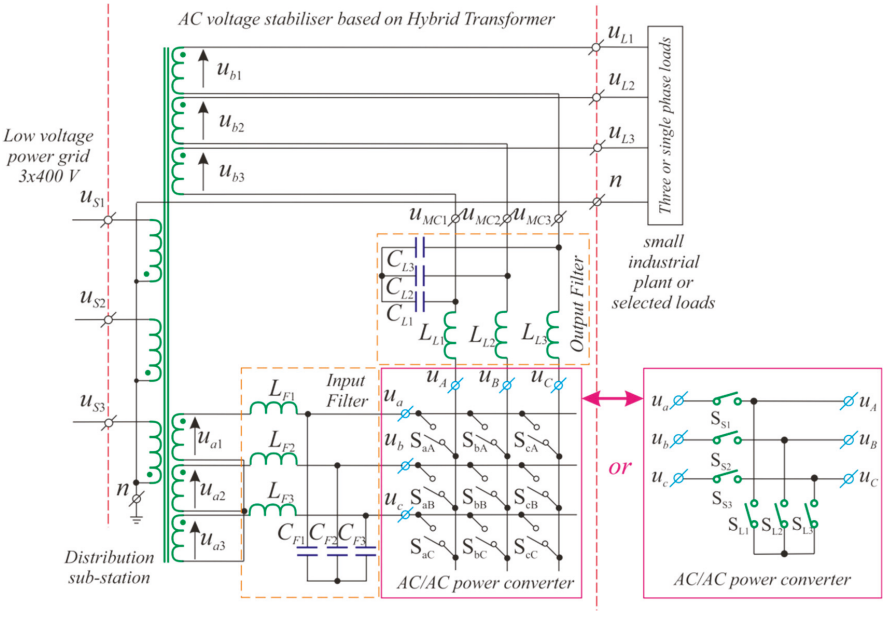


Figure 17. Compensator for voltage fluctuations, based on the HT with an MC or matrix chopper, installed at connection terminals of an industrial plant, a building, or selected industrial loads.

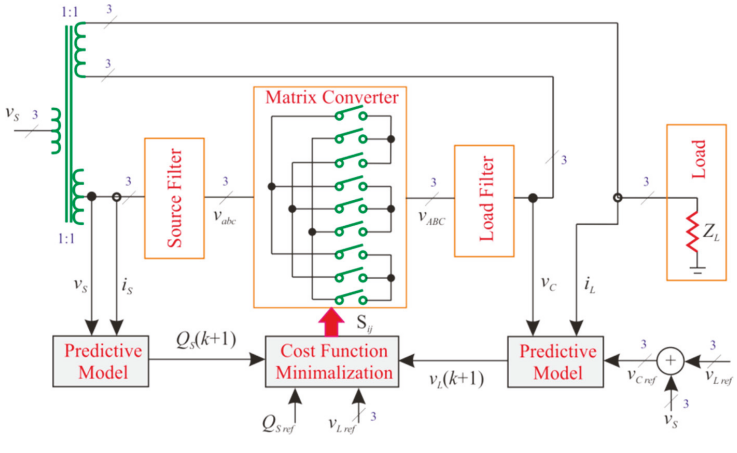


Figure 18. MPC of an HT voltage compensator with an MC and minimalization of the output voltage tracking error and input power factor.

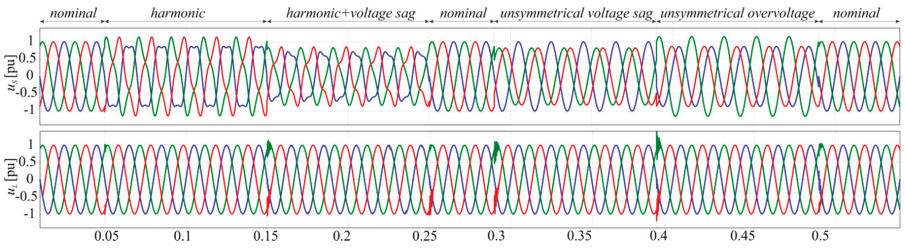


Figure 19. Results of compensations of electric power grid voltage fluctuation using an HT with an MC and MPC control (author's simulation results); red – voltage phase 1, blue – voltage phase 2, green – voltage phase 3.

If such an HT were connected to a dual-source network, it would be possible to regulate the power flow in the system by changing the phase angle of the compensator output voltage [46]. As can be seen from the above applications, AC/AC converters without a DC-link capacitor can be used in non-standard applications in low voltage power grids.

The main requirements for devices installed in the power system are a high reliability and a high efficiency factor. For an AC/AC converter, the parts most sensitive to damage are the power electronic elements. The installed converters should permit continuous work even after the occurrence of a fault in the power electronic converter, ensuring greater reliability. The reliability is high if the load can work with source voltage parameters (or slightly modified) even when damage has occurred in the power electronic part [19]. In this case, the bypass circuits should be used to disconnect or short-circuit the defective converter. In Figure 20, the single phase equivalent models of example AC/AC converters without a DC-link capacitor installed in the power system are presented. In the case of damage to the power electronic unit (AC/AC), the topologies based on the configuration shown in Figure 20a,b, could still operate with source (v_S) parameters, after activation of the additional bypass switch. In the case of the configuration shown in Figure 20c, the reliability can be assessed as low. In the event of damage to the AC/AC converter, the whole circuit must be turned off, because it is unable to continue to operate. As a result, all receivers connected to the load side have to be shut off.

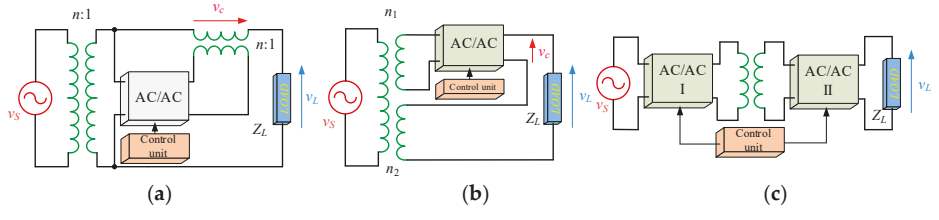


Figure 20. Single phase equivalent models of AC/AC converters installed in the power grid, (**a**,**b**) high reliability configurations, (**c**) low reliability configuration.

5. Conclusions

The presented converter offers a number of important benefits. However, such devices are still not widely used. Their application at the industrial level has been halted due to the fact that there are a number of challenges that must be overcome. This article has identified the challenges faced by the designers of such systems. The main aim of this article was to identify the problems that need to be addressed by research to enable the use of such converters without DC energy storage elements.

The main barrier to the development of AC/AC converters is due to the small number of available semiconductor power components. In addition, there are virtually no solutions in the form of intelligent modules that also include gate drivers and systems providing additional measuring and protection

functions. It should be pointed out that minimizing the size of AC/AC converters without a DC-link circuit will become possible as a result of the development of modules which will be dedicated and optimized in terms of functionality, size, and performance of intelligent power modules. Another constraint is met in the complex algorithms for the modulation and commutation of transistors, which requires the construction of complex systems most often equipped with DSP and FPGA. In addition, the complexity of the above-mentioned algorithms also involves the use of additional electronic circuits, such as current flow detectors or a clamp protection circuit.

Finally, the article identifies the application possibilities of the analyzed topologies in modern power systems. The potential of modern control algorithms based on MPC has also been indicated. Comparative analysis shows that the use of such algorithms produces very good properties in voltage or current signal shapes.

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6.78-MHz, 50-W Wireless Power Supply Over a 60-cm Distance Using a GaN-Based Full-Bridge Inverter

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Abstract: An inductive wireless power transfer system is proposed as a power supply for an on-line monitoring system for an overhead catenary. Because of the high voltage (25 kV_{rms}) applied to the catenary, galvanic isolation was required to supply power to the attached monitoring system. The proposed wireless power system was able to transmit 50 W over a distance of 60 cm at 6.78 MHz. Design methodologies for the transmitter and the receiver coils, 6.78-MHz GaN-based full-bridge inverter, and rectifier are proposed in this paper. Pareto optimality, a multi-objective optimization technique, was used to determine optimal solutions in terms of efficiency and copper usage. A 100-W, 6.78-MHz full-bridge inverter was developed using 100 V, 35 A, E-HEMT GaN MOSFETs. Because of the high operating frequency, two factors were considered in the design of the full-bridge inverter, (1) close placement of the gate driver and the switch to minimize parasitic inductance and the resulting fluctuation of the drive signal and (2) effective heat dissipation from the switches and gate drivers for a high power rating. In addition, a full-wave rectifier was built using Schottky barrier diodes with a reverse recovery time of a few tens of nano-seconds. The developed wireless power system was experimentally evaluated. The measured coil-to-coil efficiency was 77%, and the measured efficiencies of the inverter and the rectifier were 92% and 93%, respectively. The overall system efficiency was 57% for a transfer of 47 W. Finally, the dependences of the efficiency on the distance, operating frequency, and load were evaluated.

Keywords: wireless power transfer; inductive power transfer; Pareto optimality; coil design; magnetics design; GaN-based inverter and converter

1. Introduction

Applications of inductive wireless power transfer (WPT) technology have transitioned from W level biomedical devices to MW level transportation systems [1–8]. Among the various applications, application that the WPT system is useful as a power supply: an on-line monitoring system for a high-voltage catenary (see Figure 1a) [9]. Because of the high-voltage (25 kV_{rms}) of the catenary, the monitoring system cannot obtain power from a low-voltage grid (110 V_{rms} or 220 V_{rms}) without having a sufficient insulation or isolation gap. According to [10], the minimum isolation distance between a 25-kV_{rms} overhead wire and ground is 25 cm (30-cm isolation distance is recommended). This is the reason that the lengths of the insulators used for 25-kV_{rms} catenaries are longer than 30 cm (60 cm or longer insulators are common). Therefore, any system that supplies a low voltage power to the 25-kV_{rms} catenary needs to transmit power over the lengths of the insulators.

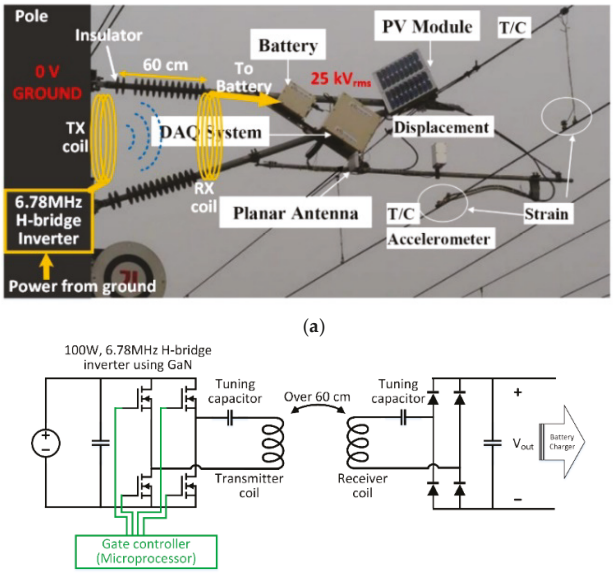


Figure 1. Configurations of the target catenary monitoring system and the WPT system: (**a**) Target system configuration; (**b**) Block diagram of the wireless power transfer system.

Previously, a 12-V, 12-Ah Pb-battery and a photovoltaic (PV) battery charger were used as an energy source. The PV charger was attached to an arm of a support pole (see Figure 1a). It solved the high voltage isolation problem. However, the size and weight of the PV module required to supply sufficient power (larger than 50 W) to the monitoring system were too large and heavy to be installed on the arm.

Instead of the PV module, an inductive WPT system was proposed that is able to wirelessly transmit energy over the insulator in [11,12]. According to [13], the inductive WPT system was more efficient compared to other technologies like a capacitive WPT system or a far-field power radiating system. The distance between the coils of the target WPT system was over 60 cm and output power was 50 W. The operating frequency of the system was 6.78 MHz (the highest frequency allowed for a WPT system [14]) to achieve efficient power transmission for this large air-gap. Because of the high operating frequency and large output power, the development of low-loss transmitter and receiver coils and a high efficiency 6.78-MHz inverter are required to construct an effective WPT system. There have been many previous studies that worked on such large air-gap, MHz frequencies WPT systems.

Sample et al. proposed a 7.65-MHz, 70-cm distance WPT system in 2011 [15]. The authors used two circular coils with diameters of 59 cm as a transmitter and a receiver. The measured coil-to-coil efficiency was 70% at 30 W, 70-cm power transmission. The main focus of the paper was to determine the optimal operating frequencies depending on the change of the distance between the coils. Duong and Lee published a paper demonstrating 30-mW transmission over a distance of 60 cm with a peak efficiency of 46% [16]. In this paper, the main focus of the paper was a mathematical analysis of the coil-to-coil system using an equivalent circuit modeling technique. Lee et al. proposed a coil design methodology for a large air-gap system in [17]. The design methodology identified a feasible design space as its first step. Then the coil-to-coil efficiency, copper usage, control stability, and other performance metrics were calculated in the entire design space, and a weighted sum of the metrics was calculated to determine an optimal design for the transmitter and the receiver coils. Based on the proposed methodology, a 95% coil-to-coil efficiency was achieved at a distance of 30 cm and 3.74-MHz

operation. However, these aforementioned papers did not consider the feasibility and efficiency of MHz operation inverters, even though it is challenging to build an efficient high-power converter at these high frequencies.

The literature [18–22] focused on the development of high efficiency MHz switching class-E amplifiers for loosely-coupled WPT systems. Class-E amplifiers are very common in radio-frequency (RF) application since the amplifier requires only one low-side switch for power conversion. However, the class-E inverter requires a bulky DC inductor, and the optimal circuit parameters (e.g., shunt capacitances) are highly dependent on the operating conditions (load, duty cycle, and operating frequency, etc.) [23]. Therefore, the class-E inverter requires fine tuning of the circuit parameters depending on the load and operation conditions.

Instead of the class-E inverter, recent rapid evolution of large bandgap semiconductor switches (Silicon-carbide (SiC) and Gallium-nitride (GaN) Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)) and their gate drivers have enabled significant advancement of radio-frequency half- and full-bridge switch-mode inverters. Multiple papers reported on GaN-based full-bridge inverters for WPT systems in 2017 [24–26]. Zhao et al. proposed a multi-frequency pulse-width-modulation (MFPWM) scheme which was implemented using a GaN-based full-bridge inverter [24]. Using MFPWM, an inverter can simultaneously transmit power to two receivers that operate at 100 kHz and at 6.78 MHz. Since the focus of the research was the transmission of power to multiple receivers, rather than improvement of the inverter efficiency using GaN switches, the efficiency of the developed inverter was not sufficiently high to be used for a system operating at a few tens of Watts. Bonache-Samaniego et al. proposed a self-oscillating resonant converter that operates at 6.78 MHz [25]. The gate signals of the developed full-bridge inverter's GaN switches were generated using the sensed current of the resonant tank. The proposed system was useful in the construction of a low cost and simple inverter. However, it was not suitable for the control of the operating frequency, duty, or power level. Xue and Zhang demonstrated a 50-W, 6.78-MHz, 90% efficiency GaN-based inverter for a WPT system. The main focus of the paper was the design of a filter network to achieve a wider zero-voltage-switching (ZVS) range and higher efficiency at light loads. The research used a 13.56-MHz oscillator and a D-flip-flop to generate a 6.78-MHz gate drive signal. The output power was controlled using a phase-shift control of the legs of the inverter based on a phase delay element.

In this paper, a novel 50-W, 60-cm distance wireless power system operating at a frequency of 6.78 MHz is proposed. The design and fabrication methodologies for the transmitter and the receiver coils, a 100-W, 6.78-MHz H-bridge inverter using GaN switches, and a 50-W, 6.78-MHz full-wave rectifier design are investigated. The power level and efficiency of the proposed system were experimentally evaluated. In the first part of the paper, design methodology for the transmitter and receiver coil is proposed using a Pareto optimality, a multi-objective optimization technique. The designed coils are fabricated on a printed-circuit-board (PCB) for ease of mass-production. The dominant sources of losses of the PCB coils are identified and the methods for fabrication of low-loss coils at 6.78-MHz frequencies are presented. The details of a 100-W, 6.78-MHz operating E-HEMT GaN-based H-bridge inverter is explained in the following section. The H-bridge inverter is developed to supply power to the transmitter coil. The gate signals of the switches are controlled using a commercial 32-bit digital-signal-processor, and the details of the PCB layout techniques for low parasitic inductance and an effective heat dissipation are discussed. Finally, the performance evaluation of the developed system is presented using experimental results. Efficiencies and losses of each component of the system are measured and compared. Also, the dependence of the DC-to-DC efficiency on the distance, load, and operating frequency is evaluated with the test-bed.

2. Target System Configuration

A photo of the target catenary monitoring system is shown in Figure 1a. The catenary monitoring system has multiple sensors that were installed on the catenary, a data acquisition (DAQ) system that gathers information from the sensors and wirelessly transmits the information to a data center, and a

battery pack as an energy source. A WPT system that can transmit 50 W over a 60-cm distance (the length of the insulator) is proposed. A schematic of the proposed WPT system is shown in Figure 1b. The proposed WPT system collects power from a 220-V_{rms} single-phase grid and converts it to DC with a diode rectifier. Then, it is converted to a 6.78-MHz AC voltage and supplied to the transmitter (TX) coil using a GaN-based H-bridge inverter. The induced voltage of a receiver coil that is weakly coupled to the transmitter is rectified and supplied to the battery using a full-wave diode rectifier. The design details of the transmitter and the receiver coils, 6.78-MHz resonant inverter, and receiver side rectifier are described in following sections.

3. Development of Transmitter and Receiver coils

3.1. Transmitter and Receiver coil Design

There were three main constraints with regard to the design of the transmitter (TX) and the receiver (RX) coils; (1) the maximum sizes of the TX and RX coils were limited to 40 cm × 40 cm, (2) the minimum distance between the TX and RX coil was 60 cm. (3) the required output power was 50 W, and load resistance was 6 Ω. For full utilization of the given space, square coils were assumed for the TX and RX coils as shown in Figure 2. The design parameters to be determined for a square coil were the inner diameter (d_{in}), turn spacing (s), width of the turn (w), and the number of turns of the transmitter and the receiver coils (n_{tx} and n_{rx}). The design spans for the parameters are summarized in Table 1.

Table 1. Design spans of transmitter and receiver coils.

Parameters	Design Limits	Parameters	Design Limits
Inner diameter, d_{in}	10–30 cm	Trace width, w	1–2.5 cm
Turn spacing, s	0.5–2 cm	# of turns, n	1–8 turns

Pareto optimality [27], a multi-objective optimization theory, was applied in the coil design process. The maximization of the power transfer efficiency (η) and minimization of the total usage of the copper (m) were two objectives during optimization. The power transfer efficiency and total mass of the copper depending on the coil shape change were calculated using (1) [28] and (2).

$$\eta = \frac{1}{1 + \frac{R_2}{R_L} + \left(\frac{R_L + R_2}{\omega_0 M}\right)^2 \frac{R_1}{R_L}} \tag{1}$$

$$mass\ (m) = \rho * l * w * t \tag{2}$$

where, ω_0 is the operating frequency of the system, M is the mutual inductance between the transmitter and the receiver, R_1 and R_2 are the equivalent series resistances (ESRs) of the transmitter and the receiver coils, respectively, R_L is the load resistance of the system, ρ is the density of the copper, l, w and t are the total length, width, and the thickness of the coil trace, respectively. The mutual inductance and the ESRs of the TX and RX coils were calculated for each combination of the inner diameter, turn-spacing, width of the turn, and the number of the turns. The mutual inductance was calculated using a numerical integration of the flux linkage between the coils. According to [29], the z-directional magnetic field intensity at point P (H_z) generated by a square transmitter coil follows (3).

$$H_z = \frac{I}{4\pi} \sum_{i=1}^{n_{tx}} \oint \frac{\vec{dl}_i \times \vec{r}_i}{r_i^3},\ \lambda = \sum_{k=1}^{n_{rx}} \oint \mu_0 H_z\, dA_k,\ M = \frac{\lambda}{I} \tag{3}$$

Then, the total flux linkage (λ) at the receiver coil and resulting mutual inductance (M) can be calculated. H_z is the z-directional magnetic field intensity at point P, I is the current flowing in the transmitter coil, n_{tx} is the number of turns of the transmitter coil, $\vec{dl}_i$ is the infinitesimal displacement

vector of i-th turn of the transmitter and $\vec{r}_i$ is a direction vector from $d\vec{l}_i$ to the point (see Figure 3), dA_k is the infinitesimal area element in k-th turn of the receiver coil, μ_0 is the permeability of air, λ is the total flux linkage at receiver coil, and M is the resulting mutual inductance. The ESRs of the transmitter and the receiver coils were calculated using (4).

$$R = \frac{l}{\sigma \delta w} \tag{4}$$

where l is the total length of the coil, w is the width of the trace of the coil, σ is the conductivity of copper, and δ (= 25.4 µm) is the skin-depth of the copper at 6.78 MHz. Figure 4 shows a $\eta - m$ distribution in the entire coil design space.

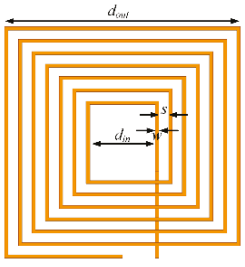


Figure 2. Geometric design parameters of the square coils.

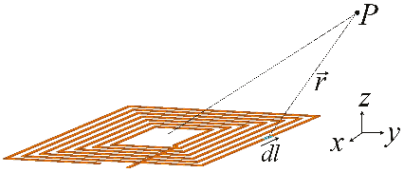


Figure 3. H-field calculation diagram.

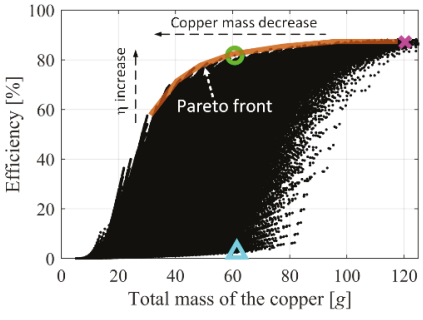


Figure 4. Pareto front of the WPT system.

From the figure, it should be noted that the WPT coils with the same total mass of copper have very different efficiencies depending on their design. For example, the first WPT system (identified by the cyan triangular point in Figure 4 had an 8-turn transmitter coil with a 10 cm inner diameter, 40 cm outer diameter, 6 mm of turn spacing, and 13 mm turn width. The receiver of the first WPT system was a 1-turn coil with a 10 cm inner diameter, 12.6 cm outer diameter, 6 mm of turn spacing, and 13 mm turn width. The second WPT system (identified by green circular point in Figure 4 had a 3-turn transmitter coil with a 30 cm inner diameter, 40 cm outer diameter, 5 mm of turn spacing and 13 mm turn width. Its receiver coil was a 3-turn with a 30 cm inner diameter, 40 cm outer diameter,

5 mm of turn spacing, and 13 mm turn width. The total mass of both systems was 60 g; however, the power transfer efficiency of the first system was 2.4% at 60 cm of air-gap while the efficiency of the second system was 82%.

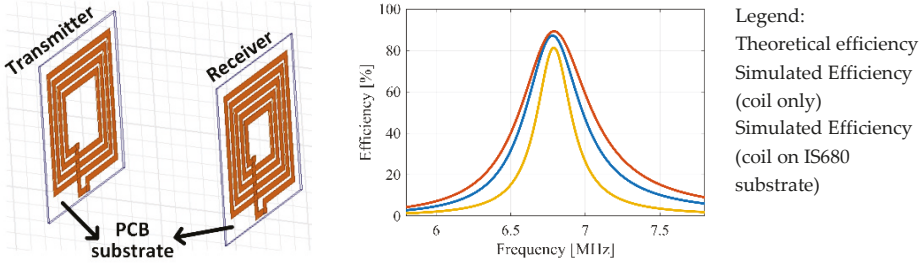
Since the goal function was to maximize the efficiency while minimizing copper usage, non-dominated solutions (Pareto front) were located at the upper left corner of the plot. The brown line in the figure represents the Pareto front. Among the non-dominated solutions, one of the solutions with 87% efficiency and 110 g of copper usage was selected for the TX and RX coil design. This solution is denoted as a magenta X in the plot. It is notable that the decision was made for high efficiency rather than low copper mass. The selected design parameters for the TX and RX coils are summarized in Table 2.

Table 2. Selected design of the transmitter and receiver coils.

Parameters	Transmitter Coil	Receiver Coil
Inner diameter d_{in}	18 cm	12 cm
Outer diameter d_{out}	39.8 cm	39.6 cm
Turn spacing, s	0.7 cm	0.7 cm
Trace width, w	2.2 cm	2.2 cm
Trace thickness	71 µm	71 µm
Number of turns, n	4	5
Substrate thickness	1.6 mm	1.6 mm

3.2. Finite Element Analysis of Transmitter and Receiver

The selected design was evaluated by finite element analysis (FEA) results using the full-wave simulation software ANSYS HFSS (19.0, ANSYS, Canonsburg, PA, USA) and ANSYS DESIGNER (19.0, ANSYS, Canonsburg, PA, USA). Figure 5a shows a simulation model of the WPT system and Figure 5b shows the resulting coil-to-coil efficiency vs. operating frequency for a 6 Ω load. The theoretical efficiency was calculated using (1). It should be noted that the theoretical and the simulated results are in good agreement with each other.



(a) (b)

Figure 5. Finite element simulation model and simulated efficiencies: (**a**) FEA model; (**b**) Simulated efficiency.

3.3. High Q coil Fabrication

Because of the large diameter and a small number of turns of the TX and RX coils, the coils were fabricated using a PCB for ease of mass-production. Fabrication of a high-quality factor transmitter and the receiver coils on the PCB is discussed in a previous paper [12]. A summary of the previous paper is provided in this chapter. At high frequencies, especially in the MHz frequency ranges, the reduction of three primary types of losses was important to achieve high quality factor (Q-factor) coils on the PCB. These include skin-effect loss, proximity-effect loss, and dielectric loss. Because of the target WPT system's high operating frequency, skin- and proximity-effect losses were critical in the process of analyzing the Ohmic loss of the copper trace. In addition, the dielectric loss of the PCB

substrate was important in determining the entire loss of the PCB coil because it can dominate other losses when the coil is not designed properly. According to the full-wave simulation results in [12], the dielectric loss was approximately 10 times greater than the Ohmic loss when the PCB substrate was a very common material, FR-4. A low dissipation factor PCB material (IS680 [30]) was very effective in reducing dielectric loss (see Table 3). Figure 6a,b show the distributions of the dielectric losses at the transmitter and the receiver coils when they transfer 50 W to a load.

Table 3. Comparison of material properties of FR-4 and IS680.

Parameters	FR-4	IS680
Relative permittivity	4.8	3.2
Loss tangent	0.017	0.0032
Dielectric strength	20 kV/mm	30 kV/mm
Thermal conductivity	0.29 W/m/K	0.32 W/m/K

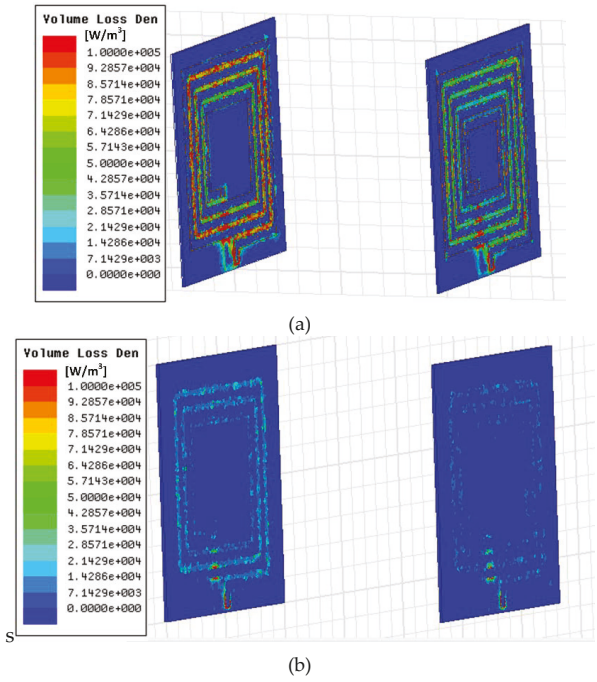


Figure 6. Configuration of the WPT system: (**a**) Dielectric loss density-FR4; (**b**) Dielectric loss density-IS680.

It should be noted that the transmitter and receiver coils using FR-4 substrates have much higher dielectric losses compared to the losses associated with the coils using the IS680 substrates. For further reduction of the dielectric loss, compensation capacitors were distributed in the middle of the coil windings as shown in Figure 7. This was helpful in reducing the electric field intensities between the adjacent turns and additional improvements of the Q-factors of the coils [12]. Figure 7 shows photos of the printed transmitter and receiver coils on IS680 substrates with distributed capacitors.

Circuit parameters of the transmitter and the receiver coils were measured using an impedance analyzer and were compared with theoretical and simulation results. Table 4 shows a summary of

the parameters. Theoretical self-inductances of the coils were calculated using Wheeler's formula (5) in [31] while mutual inductance and resistances were calculated using (3) and (4).

$$L_S = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho} \tag{5}$$

wher K_1 = 2.34, K_2 = 2.75, $\rho = (d_{out} - d_{in})/(d_{out} + d_{in})$ is the fill ratio, $d_{avg} = (d_{out} + d_{in})/2$ is the average diameter, d_{out} is an outer diameter, and n is the number of turns. The measured self- and mutual-inductances and the ESRs of the coils matched the simulation results very well. It was notable that the measured Q-factors of the transmitter and the receiver coils were greater than 300, which is remarkably high compared to conventional coils on the PCBs.

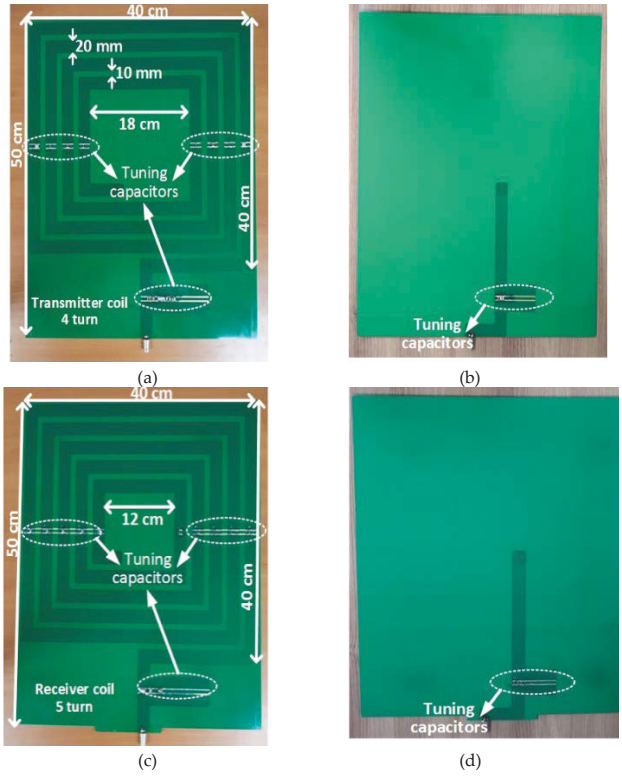


Figure 7. Photos of transmitter and receiver coils: (**a**) Top of transmitter coil; (**b**) Bottom of transmitter coil; (**c**) Top of receiver coil; (**d**) Bottom of receiver coil.

Table 4. Circuit parameters of the designed coils at 6.78 MHz.

Circuit Parameters	Theoretical		FEA Results		Measurement	
	TX	RX	TX	RX	TX	RX
Self-inductance [μH]	6.67	7.15	6.5	7.53	6.24	7.2
AC resistance [Ω]	0.31	0.38	0.48	0.70	0.58	0.81
Q-factor @ 6.78 MHz	916	801	576	458	458	379
Mutual-inductance [μH]	0.11		0.11		0.09	
Coupling coefficient	0.016		0.016		0.013	

3.4. Coil-to-Coil Power Transfer Performance

From the full-wave simulation results, an efficiency in excess of 81% was expected for a 50-W power transfer. To experimentally evaluate the fabricated coils, they were tuned using ceramic capacitors. The resulting tuned frequencies of the coils were measured using a network analyzer, E5061B (Keysight). Figure 8 shows the measured magnitude of the scattering parameters (S-parameters) of the transmitter and the receiver coils when they were 60 cm away from each other. S11 (blue line) and S22 (green line) had their minimum values at the tuned frequency, 6.87 MHz. S21 (red line), the transmission coefficient, was also maximized at the tuned frequency. This tuned frequency was 1.3% higher than the target frequency of 6.78 MHz, but this tuning frequency error was ignored in the experiment because the error has a negligible impact on the peak power transfer efficiency as shown in Figures 9 and 10. Moreover, a GaN-based H-bridge inverter that will be explained in a following section could adjust its output frequency in 0.01-MHz steps.

The coil-to-coil efficiency was measured using two different tests. The first measurement was performed using the E5061B and its real-time WPT coil analysis software that can simulate coil-to-coil efficiency in real-time with arbitrary load settings based on the measured S-parameters of the resonant coils [32]. Using the S-parameters of the coils, the input and output power, efficiency, and the input impedance of the coil-to-coil system were simulated in real-time. The simulation results are shown in Figure 9. The blue and red lines show the input and the output power of the coils when the input voltage of the transmitter coil is set to 20 V_{rms} and a virtual load of 6 Ω is connected to the receiver coil. As shown in the figure, the peak power transfer efficiency was approximately 77% when the operating frequency was 6.87 MHz with input and output powers of 84 W and 65 W, respectively. This result was a little lower than the FEA results in Figure 5b. This is because the measured ESRs of the coils were a little higher than the simulated results of the FEA as shown in Figure 7.

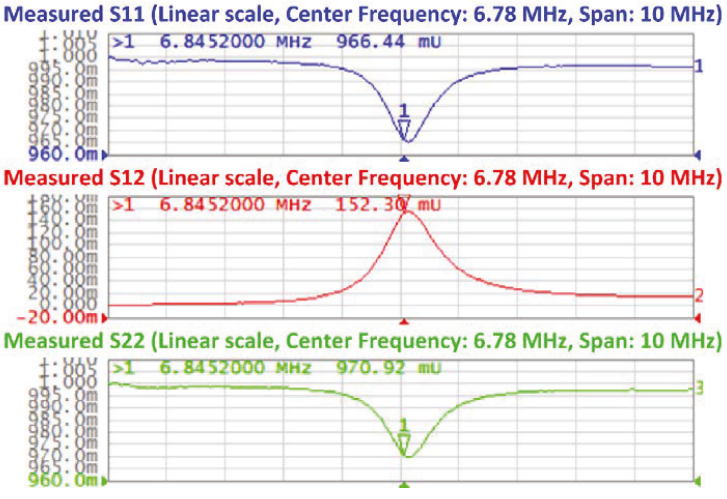


Figure 8. Measured S-parameters of the transmitter and receiver coils.

The coil-to-coil efficiency was evaluated experimentally as well. Using a variable frequency H-bridge inverter, the power transfer efficiency between the transmitter and the receiver coils was measured at various frequencies. In regard to the measurement of the coil-to-coil efficiency, an oscilloscope (HDO8108A, TeledyneLecroy, Chestnut Ridge, NY, USA) with a 12-bit ADC resolution, 10 GS/s sample rate, 1 GHz bandwidth, a differential voltage probe (HVD3605A, TeledyneLecroy, Chestnut Ridge, NY, USA) and a current probe (CP031, TeledyneLecroy, Chestnut Ridge, NY, USA) with a measurement bandwidth of 100 MHz (14 times higher than 6.87 MHz) were used. The measured

efficiency is plotted in Figure 10. A peak power transfer efficiency occurred when the operating frequency was 6.86 MHz, which was very close to the result in Figure 9. The peak value was 77%, which was very similar to the real-time simulated results in Figure 9. These results demonstrate the validity of the coil design and fabrication methodologies described in Sections 3.1 and 3.3.

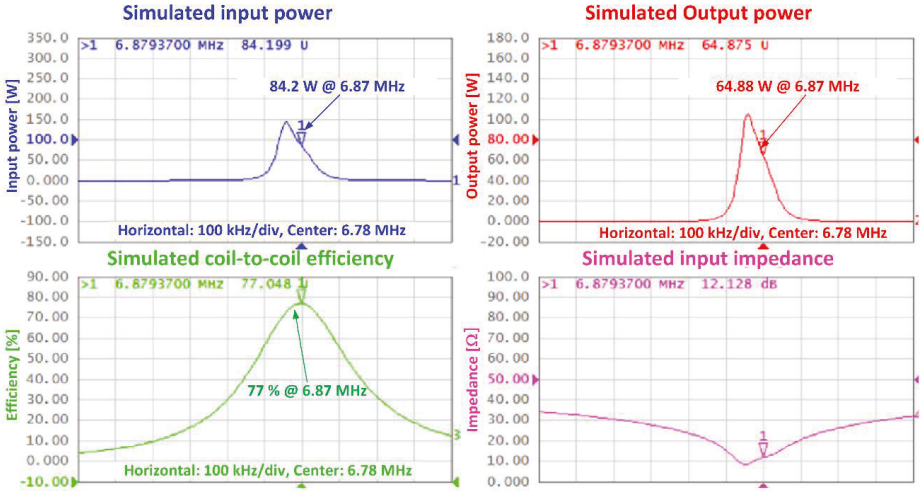
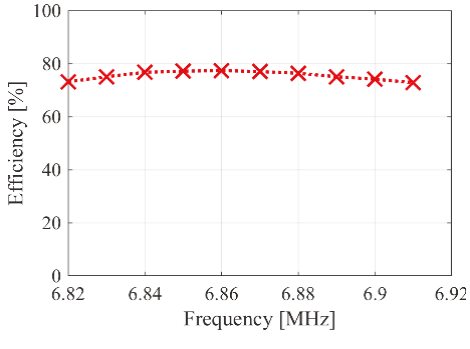


Figure 9. Real-time simulation results using Keysight's WPT analysis software (with 20 V_{rms} input voltage and 6 Ω load resistance setting).



Measurement conditions:

Distance: 60 cm
Input voltage: 20 V_{rms}
Load: 6 Ω

Figure 10. Measured coil-to-coil efficiency with 6 Ω load resistor.

4. 6.78-MHz, 100-W, 92% Efficiency H-Bridge Inverter

In order to supply 50 W using the 77% efficient transmitter and receiver coils, the development of a high efficiency, 6.78-MHz, 100-W, H-bridge inverter was investigated. Four GS61004B, 100-V, 35-A, enhancement mode HEMT (High-electron-mobility transistor) GaN switches (GaN Systems, Ottawa, ON, Canada), and two TI's LM5113 half-bridge drivers (TI, Dallas, TX, USA) were used. A TI's 32-bit microcontroller, TMS320F28377S (TI, Dallas, TX, USA), was used as a gate signal generator and a power controller. The details of the developed inverter are presented in the following sections.

4.1. PCB Layout

After multiple failures in an attempt to develop a high-frequency inverter, the authors discovered that the PCB layout of the driver and GaN switches were the most important factors in determining its performance. Two features are of notable importance in the PCB design. The first is a parasitic

inductance between the gate driver and the GaN switch. Due to the high operating frequency (6.78 MHz), parasitic inductances between the gate drivers and the switches form resonance circuits with the input capacitances of the GaN switches. This resulted in unwanted ringing of the gate drive signal. This ringing caused undesirable on/off and failures of the GaN switches.

The second aspect to be considered is a heat dissipation of the GaN switches to achieve high power generation (100 W) compared to the size of the switch package. The GS61004B switch was designed to sink heat to the bottom side of its package, especially through its source pad. Per its datasheet, the required PCB pattern under its source and drain pin is over 25 × 25 mm^2 for optimum heat dissipation. However, this large pad requirement leads to a large gap between the gate driver and the GaN switch and resulted in a large parasitic inductance between the driver and switch. Figure 11a shows the initial PCB layout of the inverter that focused on the heat dissipation of the four switches. In this initial design, the PCB pattern under the source pin of the switches was 25 mm × 25 mm. To avoid additional thermal burden on the PCB, the gate drivers (LM5113) were positioned 4 cm away from the GaN switches. However, this 4-cm separation caused significant ringing of the gate drive signal and the operation of the GaN switches was not stable even at 0.5 MHz.

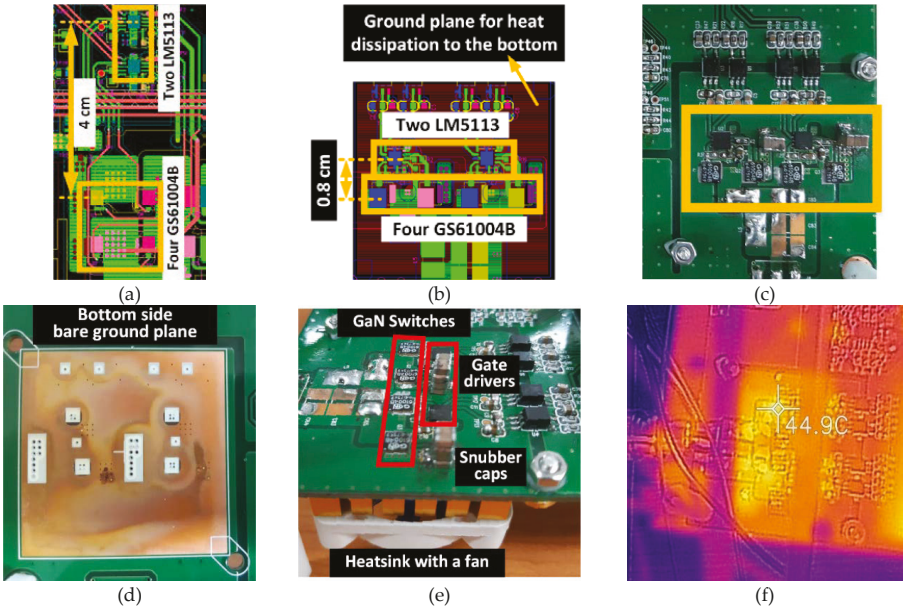


Figure 11. Configuration of the WPT system: (**a**) Initial design; (**b**) Revised design; (**c**) Fabricated inverter; (**d**) Bottom side ground plane; (**e**) Assembled heatsink and a fan; (**f**) Thermal image of the inverter at 81-W output.

Figure 11b shows a revised version of the inverter. The gate drivers were placed 0.8 cm above the switches and only 5 mm × 5 mm of the PCB pattern was allocated to the source pin of the high-side GaN switch. With this compact layout of the driver and switches, the gate signal ringing problem was eliminated. However, the revised version did not allocate sufficient pad area for heat dissipation of the switches. Instead of a large pad, a heat sink was installed at the bottom layer of the PCB in this revised version. The ground plane at the bottom layer of the PCB was uncovered as shown in Figure 11c. The generated heat from the switches and gate drivers was transferred to this bottom plane and cooled using a heat sink that was assembled with a fan (see Figure 11d). A thermal image of the fabricated inverter is shown in Figure 11e. The maximum temperature rise of the GaN switch's package was 15 °C compared to its initial temperature when the inverter output power was 81 W. Figure 12 shows a

measured input and output voltages and currents of the inverter with 25 V_{rms} input voltage and 6 Ω load. The measured input power was 88 W and output power was 81 W. Therefore, the efficiency of the resonant inverter was 92%.

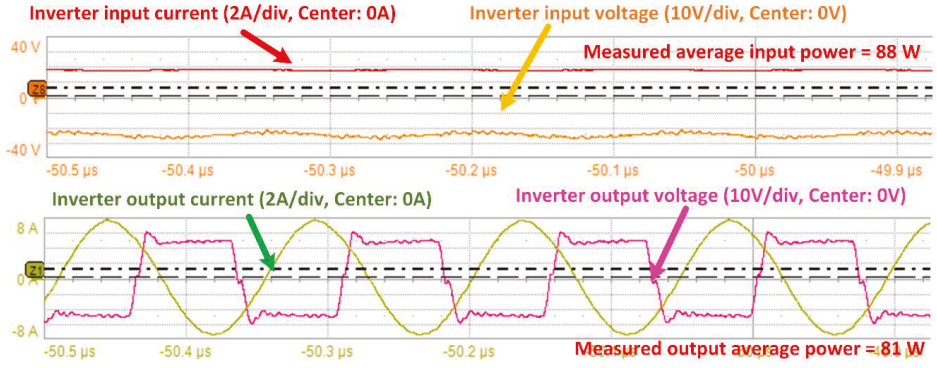


Figure 12. Input and output power of the H-bridge inverter. Measurement conditions: distance: 60 cm, input voltage: 25 V_{rms}, load: 6 Ω.

4.2. Switch Control

The gate drive signals of the inverter were digitally controlled using a TI's 200-MHz, 32-bit microcontroller unit (MCU), TMS320F28377S. The resolution of a PWM (Pulse width modulation) module of the MCU was 5 ns when the system clock was 200 MHz. The PWM module was able to generate pulses with periods of 145 ns (6.67 MHz) or 150 ns (6.89 MHz) with a single count change. PWM signals in the frequency range of 6.67 MHz to 6.89 MHz could not be generated. However, the target WPT system had very high Q coils and the transmitted power and efficiency were very sensitive to the operating frequency as shown in Figure 9. Therefore, the regular PWM module was not suitable for 6.78-MHz operation. Instead of the regular PWM module, a high-resolution pulse width modulation (HRPWM) module capable of enhancing the resolution of the PWM to 180 ps was used for fine adjustment of the PWM frequency. Using the HRPWM, it was possible to change the operating frequency in 0.01-MHz steps. Phase-shift control and frequency control of the inverter switches were easily implemented using the MCU. Figure 13 shows a photo of the entire assembled inverter board.

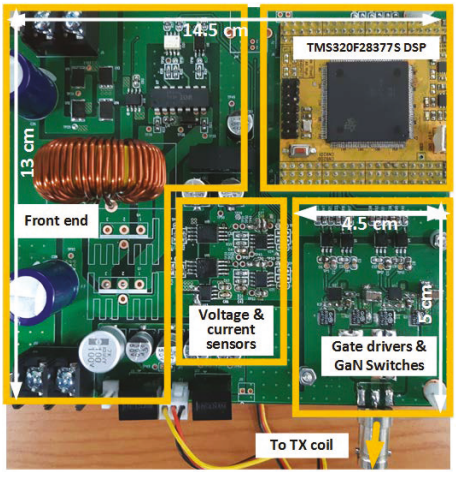
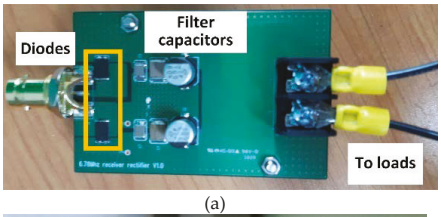


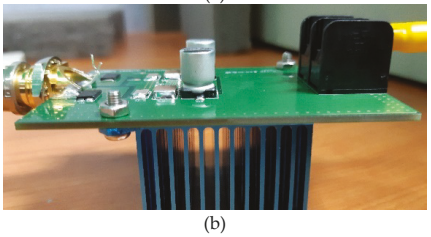
Figure 13. A photo of the assembled H-bridge inverter.

5. Receiver Side Full-Wave Rectifier Design

The series-tuned receiver coil was coupled to a full-bridge rectifier. The rectifier diodes were 100-V, 8-A, Schottky barrier diodes (PMEG100V080ELPD from NXP, Eindhoven, Netherlands) with a 10-ns reverse recovery time when the forward current is 0.5 A. To minimize unwanted parasitic inductances and capacitances that can alter the tuning frequency of the RX coil, four diodes were placed very close to the BNC terminals. Two low-side diodes were connected on top of the PCB and high-side diodes were connected at the bottom of the PCB as shown in Figure 14a. Multiple ceramic capacitors and two polymer aluminum capacitors were used as a filter. The diodes were designed for heat dissipation through its cathode pad. Therefore, a heat sink was installed at the rectifier's positive DC plane as shown in Figure 14b.



(a)



(b)

Figure 14. Photos of full-wave rectifier: (**a**) Top-view (**b**) Side-view.

6. Experimental Evaluation

6.1. Experimental Setup

Figure 15 shows a configuration of the test-bed. The H-bridge inverter was connected to the transmitter resonant tank through a coaxial cable (16 AWG, American wire guage) with a BNC termination. Also, the receiver coil was connected to the diode rectifier with the same coaxial cable and termination. A Chroma's DC electronic load, 63102 (Chroma, Foothill Ranch, CA, USA) was used with a constant resistor mode setting.

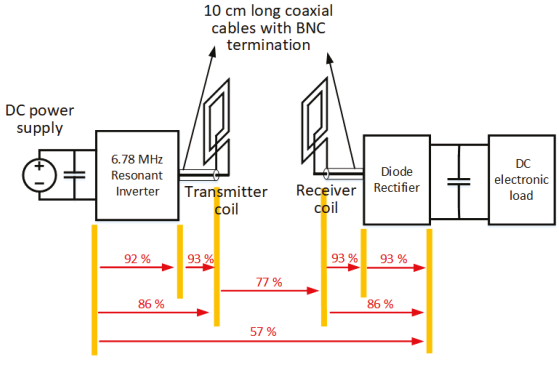


Figure 15. Configuration of the test-bed.

Figure 16 shows a photo of the entire test-bed. Instead of the DC electronic load, two 20-W, 12-V DC light bulbs were connected to the rectifier's output terminal to demonstrate wireless energy transmission over 60 cm. Using this test-bed, the power transfer efficiency at various distances, load power, and operating frequency was measured.

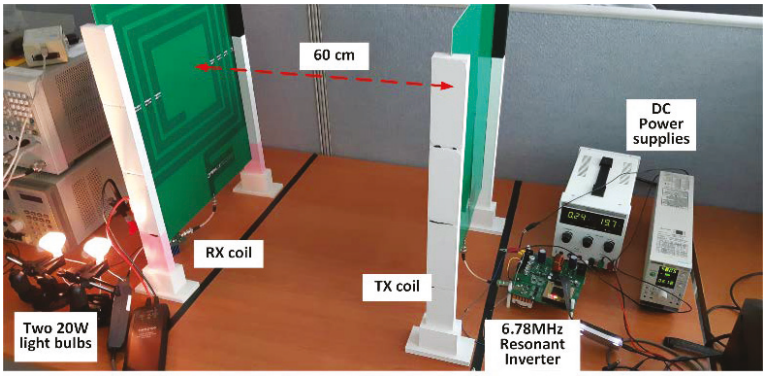


Figure 16. A photo of the experimental setup.

6.2. Efficiency Analysis of the Developed System

Figure 17 shows the measured input DC voltage and current of the H-bridge inverter and output DC voltage and current of the rectifier when the load resistance was 6 Ω. Because the efficiency was maximized when the operating frequency was 6.86 MHz, the switching frequency of the inverter was 6.86 MHz. The measured output power was 47.1 W while the measured input power was 82.3 W. Therefore, the measured DC-to-DC power transfer efficiency was 57%. This result was relatively low compared to the measured efficiency between the coils which was 77% at its rated operation.

For a loss analysis of the developed system, the efficiency of every component of the system was measured and denoted in Figure 15. It was found that additional losses were coming from the 16 AWG coaxial cables. This is a notable point since a coaxial cable of only 10 cm in length had a comparable power transfer efficiency to the inverter and the rectifier. Although the cross-sectional area of the coaxial cable (1.3 mm^2) was sufficient to carry a 5-A_{rms} transmitter current at low frequencies, it was not appropriate to carry the same current at 6.78 MHz.

Figure 18 shows the estimated loss percentages of the developed system. The conduction losses of the H-bridge inverter and the RX side rectifier were calculated using $R_{DS(on)}$ (37 mΩ) and the forward voltage drop of the rectifying diodes based on their datasheet. The switching loss of the inverter was calculated by subtracting the conduction loss from the total loss associated with the inverter. The losses of the transmitter and receiver coils were calculated using their measured resistance and measured root-mean-square (RMS) of the currents of the coils. It should be noted that the losses of the transmitter and receiver coils overwhelmed other losses. The switching loss of the inverter was second largest loss in the developed system. Therefore, the coil design and fabrication method were key in improving the efficiency of this loosely-coupled WPT system. To evaluate the effectiveness of the developed system on large distance power transmission, efficiency values were measured at various distances of the transmitter and the receiver coils. The distance was increased from 60 cm to 80 cm in 5-cm steps.

Figure 19 shows the measured efficiencies when the load was 6 Ω, the input power was 80 W, and the operating frequency was 6.86 MHz. When the distance was 60 cm, the efficiency was 57%. However, this value monotonically decreased to 29% when the distance was 80 cm. It is notable that the total efficiency is reduced by approximately 7% for every 5-cm increase in the distance of the coils. This shows that the efficiency of the proposed system is sensitive to the distance of the coils. For this outdoor large air-gap WPT system, appropriate fixtures and installation guidelines are required to

prevent a significant degradation of its performance due to wind and other severe weather conditions. The impact of the operating frequency on the efficiency of the test-bed was also evaluated as shown in Figure 20. The measured overall efficiency was also maximized when the operating frequency was 6.86 MHz. The efficiency decreased as the operating frequency moved away from the tuned frequency. The efficiency was decreased to 38% when the operating frequency was 6.94 MHz. This is 0.08 MHz higher than the tuned frequency. This result demonstrates that fine control of the inverter operating frequency is a critical factor of power transfer efficiency.

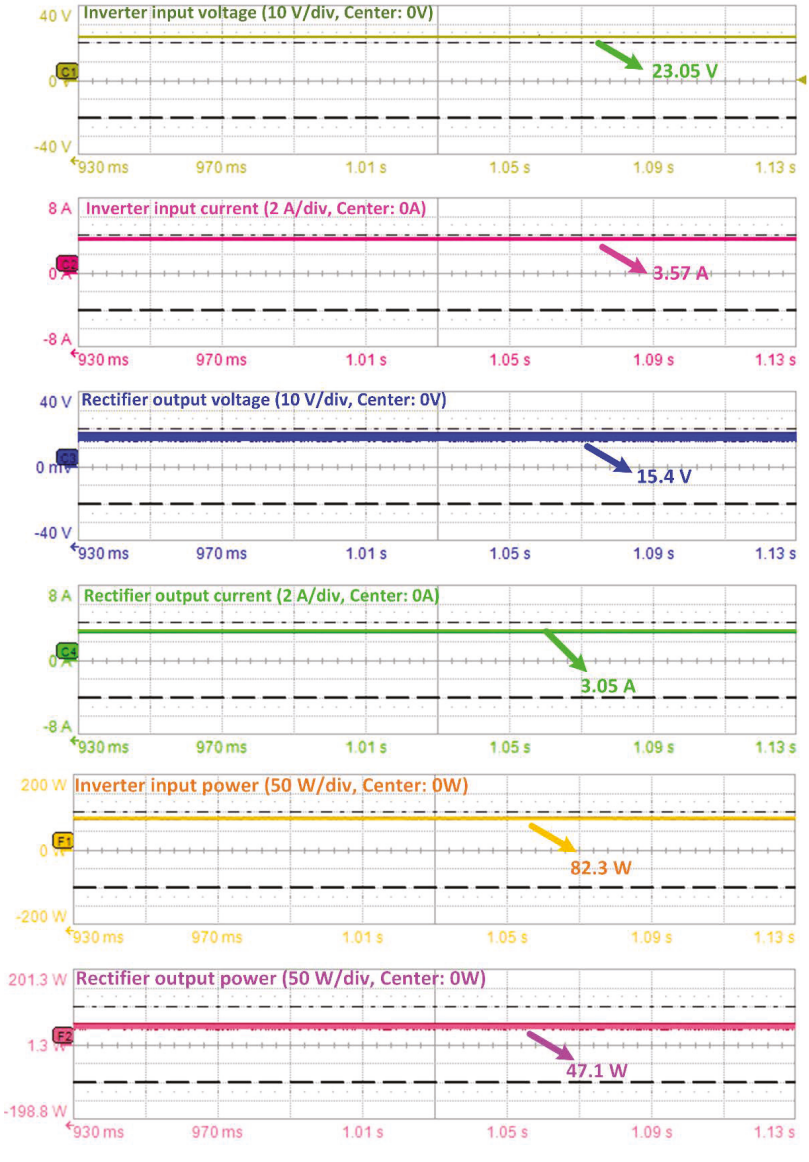


Figure 17. Measured input and output DC voltages and currents at the rated output power. Measurement conditions: distance: 60 cm, operating frequency = 6.86 MHz, load: 6 Ω.

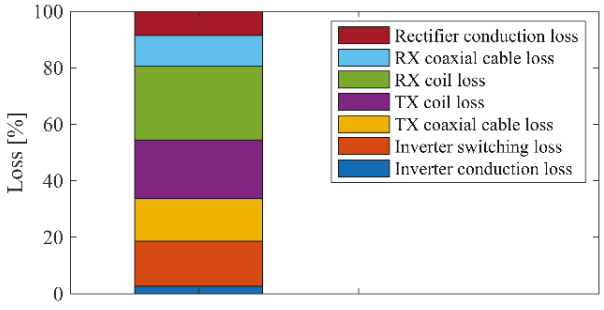
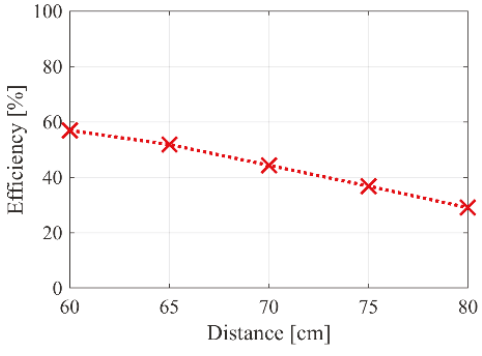


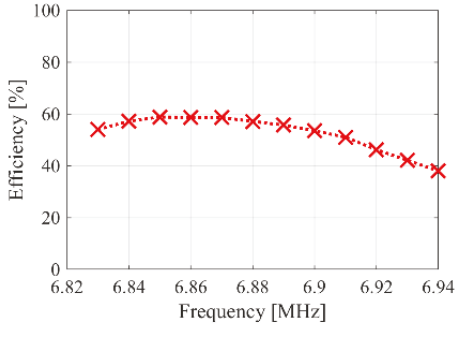
Figure 18. Estimated percentage losses of the developed system.



Measurement conditions:

$R_L = 6\ \Omega$
$P_{in} = 80$ W
$f = 6.86$ MHz

Figure 19. Efficiency dependent on distance.

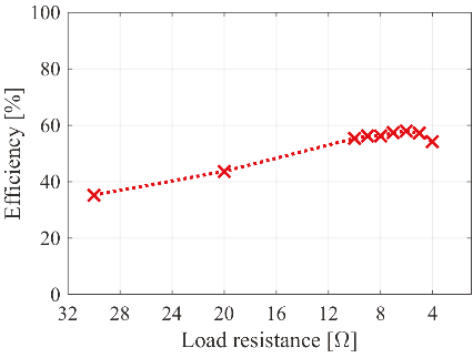


Measurement conditions:

$R_L = 6\ \Omega$
$P_{in} = 80$ W

Figure 20. Efficiency dependence on frequency.

Finally, the impact of load resistance on the efficiency of the system was evaluated. Figure 21 shows the result of an efficiency vs. load resistance plot. When the load resistance has a rated value $R_L = 6\ \Omega$, the power transfer efficiency is maximized to 57%. As the load resistance increased or decreased, the power transfer efficiency decreased, and the efficiency is only 35% when the load resistance is 30 Ω. This plot shows that there is an optimal load resistance for a maximum power transmission.



Measurement conditions:

f = 6.86 MHz

Figure 21. Efficiency dependence on load resistance.

7. Conclusions

In this paper, a new 6.78-MHz, 50-W, over 60 cm wireless power transfer system is proposed. The design and fabrication methodologies for the coils, a GaN-based 6.78-MHz H-bridge inverter, and a rectifier were explained. Using a multi-objective optimization method, Pareto optimality, the transmitter and the receiver coil were determined to a 4-turn and a 5-turn, 40 cm × 40 cm square coils. The selected transmitter and receiver coils were fabricated on a PCB. It was shown that the dielectric loss of the PCB substrate can dominate Ohmic loss of copper traces at MHz frequencies. A PCB substrate with very low dissipation factor was used to reduce the dielectric loss of the coils. The fabricated coils had over 350 Q-factors at 6.78 MHz. The peak coil-to-coil efficiency for the WPT system was 77% at 60 cm air-gap.

In addition, a 6.78-MHz, 100-W, 92% efficiency, GaN-based H-bridge inverter was developed. Two important points were considered in the development of the inverter: a low parasitic inductance of the gate drive circuit and a good heat dissipation of the GaN switch at its rated output power. Parasitic inductances between the gate drivers and GaN switches caused significant ringing of the on/off signals and poor operation performances even at sub-MHz frequencies. A close positioning of the gate driver to the switch was the key for 6.78-MHz operation. However, the congregating of the gate drivers and switches was inferior in cooling and heat dissipation of the inverter. To resolve the thermal issues, the ground plane at the bottom of the PCB was uncovered, and a heatsink with a fan was attached to the PCB. The fabricated 6.78-MHz resonant inverter had a 92% efficiency and the peak temperature was lower than 45 °C at its rated output. Using a high-resolution PWM module of the TI's MCU, the switching signals could be changed in 0.01-MHz steps. This was very helpful in fine tuning of the high Q-factor coils. Using a full-wave rectifier that was built using four Schottky barrier diodes, the induced voltage and current of the receiver coil were converted to DC values.

The measured DC-to-DC efficiency of the developed WPT system was 57% when the output power was 47 W. The efficiencies of individual components of the system were measured and lossy parts were identified. The impacts of the coil distance, operating frequency, and load resistance on the power transfer efficiency were also evaluated. As the distance increased from 60 cm to 80 cm, the efficiency decreased from 57% to 29% (about a half of the initial value). Therefore, the distance was important in the efficiency of the WPT system. Also, the efficiency decreased from 57% to 38% when the operating frequency was increased from 6.86 MHz to 6.94 MHz (a change of only 0.08 MHz). Finally, the dependence of efficiency on the load resistance was tested. It was shown that there was an optimal load value that maximizes the efficiency, and this value was determined to be 6 Ω, which corresponds to the target-rated load resistance of the developed system.

Author Contributions: Conceptualization, S.-H.L. and M.-Y.K.; methodology, S.-H.L. and M.-Y.K.; software analysis, K.-P.Y.; validation, S.-H.L., K.-P.Y., and M.-Y.K..; formal analysis, S.-H.L.; investigation, M.-Y.K.,

writing—original draft preparation, S.-H.L.; writing—review and editing, K.-P.Y. and M.-Y.K.; supervision, M.-Y.K..; project administration, S.-H.L. and K.-P.Y.; funding acquisition, S.-H.L. and M.-Y.K..

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Conflicts of Interest: The authors declare no conflict of interest.

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Supervisory Control for Wireless Networked Power Converters in Residential Applications†

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Abstract: This paper presents a methodology to design and utilize a supervisory controller for networked power converters in residential applications. Wireless networks have been interfaced to multiple power factor correction (PFC) converters which are proposed to support reactive power. Unregulated reactive power support from PFC converters could cause reactive power deficiency and instability. Therefore, a supervisory controller is necessary to govern the operation of PFC converters. WiFi and WirelessHART networks have been used to implement the supervisory controller. Different nodes of the power network are connected by wireless communication links to the supervisory controller. Asynchronous communication links latency and uncertain states affect the control and response of the PFC converters. To overcome these issues, the supervisory controller design method has been proposed based on the system identification and the Ziegler-Nichols rule. The proposed supervisory controller has been validated by using a hardware-in-the-loop (HIL) test bed. The HIL testbed consisted of an OP4510 simulator, a server computer, Texas Instrument-Digital Signal Controllers (TI-DSCs), WiFi and WirelessHART modules. Experimental results show that the proposed supervisory controller can help to support and govern reactive power flow in a residential power network. The proposed method of controller design will be useful for different small-scale power and wireless network integration.

Keywords: networked power converters; PFC converters; reactive power resources; supervisory controller; HIL Testbed

1. Introduction

According to the US Department of Energy, residential loads have consumed 20.44% of the total energy in 2017 [1]. Residential loads consume both active and reactive power. Reactive power demand in a home is usually fulfilled from the grid. Recently, power factor correction converters have been integrated into some of the residential appliance, which minimizes reactive power consumption from the grid [2–5]. A recent study shows that additional reactive power could be supported from renewable resources and power factor correction (PFC) converters in residential applications [6,7]. However, unregulated reactive power support from PFC converters could cause reactive power deficiency and instability. To utilize the additional reactive power resources in a residential power network, a supervisory controller is necessary. A supervisory controller should monitor and control the reactive power flow in the residential power network. This paper presents a methodology to design

a supervisory controller which governs reactive power flow in a residential power network. Wireless networks were used to implement the proposed supervisory controller.

The supervisory controller for large power and energy management systems are well established technology. It is known as supervisory control and data acquisition (SCADA) [8]. Because of the scalability, SCADA is not an appropriate tool to control reactive power flow in a small residential power network. Distributed controllers for power converters have been developed using communication network [9,10]. It has potential for wireless network integration but does not provide a centralized solution for reactive power management. A supervisory controller has been validated using an FPGA for power converters in Reference [11]. Reference [11] has only a single controller for multiple converters, which manages all PWM signals without a communication network. Other power and energy management systems have been implemented using fuzzy logic, distributed, model predictive and supervisory controller in References [12–17]. However, these solutions don't give the opportunity to control power flow using a communication network in a residential application. As a result, a solution has been proposed by assuming that there are reactive power resources as well as a communication network available in the residential applications [18,19].

The possible energy sources in residential applications include utility grid, solar panel, wind generator, stored energy, and so forth. These energy sources supply both active and reactive power. In the residential applications, energy is consumed by different kinds of loads , which include high-consumption applications such as HVAC systems, ovens or refrigerators, along with low-power devices such as televisions and light fixtures. Conventional residential loads consume both active power, P and reactive power, Q. However, smart loads which use PFC converters could contribute reactive power, Q, rather than consuming [6]. Examples of smart loads include HVAC systems, electric vehicle (EV) chargers, computers, televisions and other digital appliances [20–22]. Typically, this is accomplished through the use of boost PFC converters [23,24]. As a result, these appliances have the readily available converters to support reactive power. The main role of these converters is to supply specified current and voltage to the appliances. However, these converters can contribute a specified amount of reactive power to the grid without hampering their main functionality.

Recent advances in technology has has trended towards connecting residential appliances to networks. The connectivity to networks and management of appliance features is represented by smart technologies and Internet of Things [21]. The connectivity to appliances has been implemented using WiFi, WirelessHART, Bluetooth, Zigbee and Ethernet [25–28]. By using this connectivity, some specific parameters of power converters can be monitored and controlled [19].

Appliances as reactive power resources and the connection to a wireless network facilitates the opportunity to implement supervisory controller. However, the reactive power management system now becomes more complex because of the integration of power network and wireless network. This system has multiple power nodes which are connected by communication links. Multiple wireless communication links have different delays, asynchronous latency and uncertainty. These factors affects the operation of PFC converters which ultimately affects the reactive power management system. Due to the system complexity and delays, the top-level supervisory controller can't be designed accurately using a conventional state space averaging method. To address this issue, a system identification-based supervisory controller design method has been proposed in this paper. The proposed method considers uncertainty, complexity and delays. It uses the Ziegler-Nichols rule to design a proportional-integral (PI) controller. The proposed supervisory controller has been implemented in a server computer and validated using an hardware in the loop (HIL) test bed set up.

The HIL test bed was built to simulated a residential power network in real-time using OPAL-RT OP4510 [29]. The power converters of have been controlled by Texas Instrument Digital Signal Controllers (TI DSC) [30]. WirelessHART and Wi-Fi networks were used for connectivity [31,32]. Level shifting and scaling circuit were built to make the TI DSC compatible for OP4510.

Multiple tests were conducted using the HIL test bed to validate the feasibility and compatibility of the supervisory controller. The performance of the supervisory controller has been evaluated by

analyzing the dynamic response for reactive power support. Test results show that PFC converters can support reactive power to the residential application in different conditions with the help of an optimal supervisory controller. Section 2 of this paper describes the proposed scenario for this power network. Section 3 describes the proposed supervisory controller design method. HIL testbed and experimental results are presented in Sections 4 and 5, respectively.

2. Networked Power Converters

Considering the wireless connectivity to smart residential appliances, a scenario for a residential power network has been proposed in the following.

2.1. Power Network Configuration

The proposed residential power network configuration is shown in Figure 1 which has both conventional lagging load and PFC connected smart loads. A supervisory controller has been implemented in the power network using wireless nodes. Figure 1 shows the active and reactive power supplies from grid. Conventional loads with a lagging power factor are represented by a single block in Figure 1. Three separate PFC connected smart loads are distributed and are assumed to contribute reactive power. Based on the active and reactive power supply and consumption, the balanced power condition could be described by (1) and (2).

$$P_g = P_L + \sum_{n=1}^{N} P_n \tag{1}$$

$$Q_g = Q_L - \sum_{n=1}^{N} Q_n \tag{2}$$

where, P_g is the active power consumption from grid, Q_g is the reactive power consumption from grid, P_L is the active power consumption of conventional residential loads, Q_L is the reactive power consumption of conventional residential loads, P_n is the active power consumption of PFC connected loads, Q_n is the reactive power consumption or contribution of PFC connected loads.Here, n denotes the PFC number and N is the number of available PFC connected resources. The reactive power resources and loads are described pictorially in Figure 1 for $N = 3$.

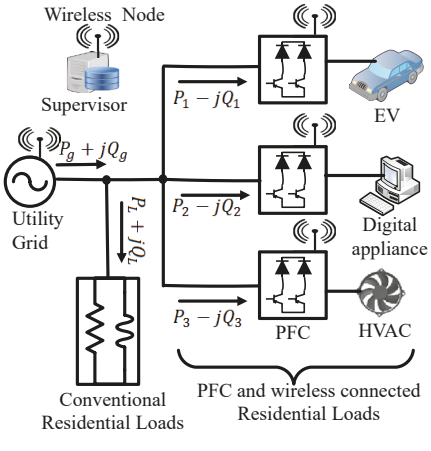


Figure 1. Reactive power resources in wireless networked residential loads.

2.2. PFC Connected Smart Residential Load

PFC converters for the appliance in Figure 1 can support reactive power. The circuit configuration for a PFC converter supporting reactive power is shown in Figure 2. Bridgeless unidirectional single phase boost PFC converter topology has been used in Figure 2. This converter has two diodes, D_1, D_2 and two semiconductor switches, Q_1, Q_2, input inductor, L and DC bus capacitor, C. The detailed analysis of the circuit is available in References [6,7,33]. Each converter is controlled by using a PFC controller. It generates complementary pulse width modulated (PWM) signals for Q_1 and Q_2 [34].

The controller for PFC converter can supply a specified amount of reactive power.

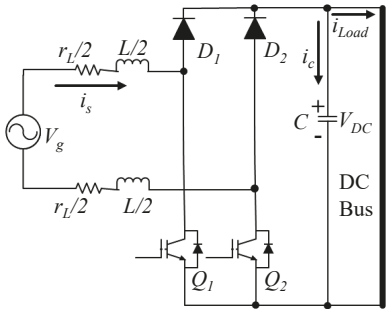


Figure 2. Circuit diagram of a bridgeless ac-dc boost power factor correction (PFC) converter.

This type of PFC controller is shown in Figure 3. The controller takes Q^* as reactive power reference and contributes Q to the power network.

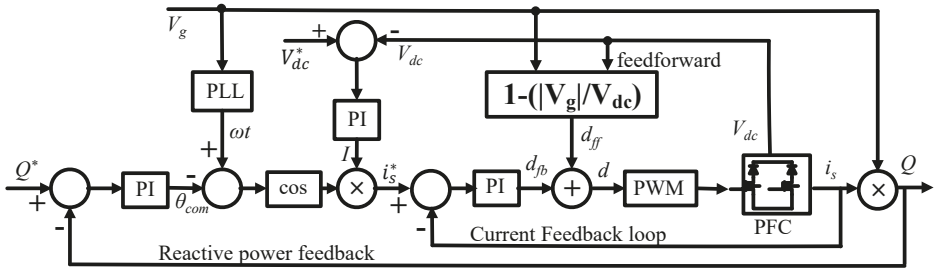


Figure 3. Control diagram of a bridgeless ac-dc boost PFC converter.

The controller initially maintains the proper DC bus voltage and in-phase current. Then, by controlling current, it makes the PFC converter the leading load and contributes reactive power to the network. This controller uses both feedback and feedforward terms to maintain inner current and outer voltage loops. Output current, DC link voltage and reactive power measurements are used as feedback signals for PI controllers. Phase angle, ωt, is determined by phase lock loop (PLL) using grid voltage, V_g .Feedback and feedforward duty cycle values are added before the generation of PWM signals.

The inner current loop is the fastest control loop in this controller and maintains leading-phase current based on the compensation angle, θ_{com} and the output of the voltage control. DC voltage feedback control is maintained by a PI controller, voltage reference, V_{dc}^* and feedback V_{dc}. The θ_{com} is determined by using a PI controller and reactive power feedback. A sinusoidal signal is reconstructed using PLL and a cosine function. The reactive power compensation loop has 2 key Equations (3) and (4).

$$Q_{err}(t) = Q^*(t) - Q(t) \tag{3}$$

$$\theta_{com}(s) = (k_p + \frac{k_i}{s})Q_{err}(s) \tag{4}$$

The DC output voltage is maintained by generating current reference, $I(s)$, using (5) and (6).

$$V_{dc_{err}}(t) = V_{dc}^*(t) - V_{DC}(t) \tag{5}$$

$$I(s) = (k_p + \frac{k_i}{s})V_{dc_{err}}(s) \tag{6}$$

AC current reference, i_s^*, is obtained by I, ωt and θ_{com}.

$$i_s^*(t) = I \times cos(\omega t - \theta_{com}) \tag{7}$$

Error in the inner current loop is calculated by applying the following equation.

$$i_{err}(t) = i_s^*(t) - i_s(t) \tag{8}$$

Current error is compensated by feedback duty, d_{fb}, using (9).

$$d_{fb}(s) = (k_p + \frac{k_i}{s})i_{err}(s) \tag{9}$$

Feedforward duty, d_{fb} is generated from (10).

$$d_{ff}(s) = 1 - \frac{V_g}{V_{dc}} \tag{10}$$

Finally, feedback and feedforward duty is added to generate PWM signal.

$$d(s) = d_{fb}(s) + d_{ff}(s) \tag{11}$$

The detailed description and design of the PFC controller for reactive power support is available in Reference [6]. The waveforms of input current, duty and PWM switching signal are shown Figure 4.

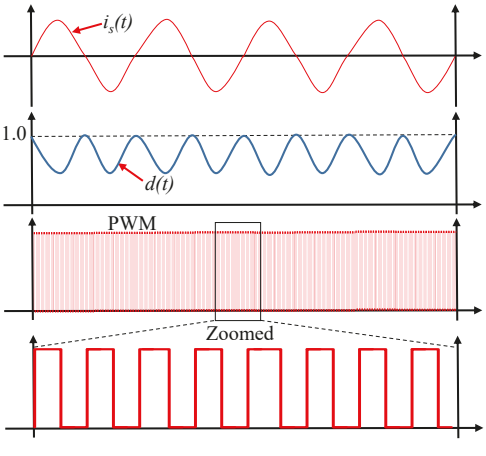


Figure 4. Waveforms during PFC switching.

2.3. Wireless Network and Supervisory Reactive Power Control

To improve the overall power factor in the proposed scenario, a supervisory controller has been included in Figure 1 using the wireless connectivity. The proposed power network has three PFC converters.These PFC converter can contribute a specified amount of reactive power Q^* as discussed in Section 2. However, reactive power demand could change with time. In demand-varying conditions, the supervisory controller identifies the reactive power demand and maintains equal amount of reactive power support from the PFC converters. If the load demand for reactive power increases, the supervisory controller ensures more reactive power. On the other hand, if the load demand decreases, the supervisory controller decreases reactive power supplied. Through this method, the supervisory controller tries to maintain unity power factor for the proposed scenario. It is recommended to maintain the grid's power factor ($p.f.$) as close to 1.00 possible [35]. From the definition of power factor, the following equation can be written.

$$p.f. = cos\phi = \frac{P_g}{\sqrt{P_g^2 + Q_g^2}} \tag{12}$$

From (12), it is clear that the power factor will be unity if and only if $Q_g = 0$. In that case, the condition of (2) becomes the condition of (13).

$$Q_L = \sum_{n=1}^{N} Q_n \tag{13}$$

In dynamic conditions, (13) can be expressed by (14).

$$Q_g(t) = Q_L(t) - \sum_{n=1}^{N} Q_n(t) \tag{14}$$

where, t represents time. The grid reactive power is minimized by making $Q_g(t)$ close to 0. To minimize $Q_g(t)$, the supervisory control technique was applied as shown in Figure 5. In this proposed technique, a proportional integral (PI) controller is used to compensate $Q_g(t)$ to 0.

The supervisory controller is shown in Figure 5 and named as supervisor. Supervisor is comprised of a PI controller, reference and distributor. Q_{ref} is set to zero, so that Q_g become zero. From the difference of the Q_{ref} and Q_g, the error is generated. Based on the error, the PI controller sets a reference of total reactive power demand, Q_d. Q_d is total reactive power that need to be fulfilled by all available PFC converters. Using a distributor, this demand is distributed and assigned to individual PFC controllers. Individual PFC controllers get command for reactive power references of $Q_1^*, Q_2^*, ..., Q_N^*$. The commands are obtained though wireless network. After performing the control, PFC converters contribute $Q_1, Q_2, ..., Q_N$ amounts of reactive power to the power network. Individual PFC converter has individual local control loops to maintain reactive power support. These local controllers get the reference from supervisory controller based on their capacity.

The response time, wireless communication delay and capacity of the PFC converters are factors of the supervisory control design consideration. The supervisor is a single input multiple output (SIMO) system. The power network of the smart home is considered as a multiple input single output system (MISO). The whole system is a single input single output (SISO) feedback system. A host program maintains the supervisory controller. A varmeter measures reactive power consumption from the grid, Q_g. Q_g is the feedback for the supervisory controller.

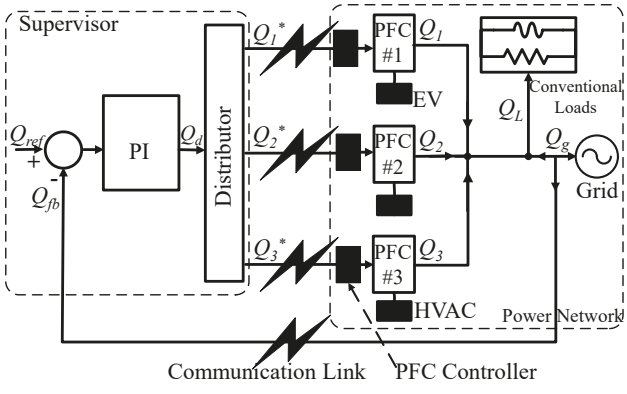


Figure 5. Supervisory control for reactive power resources using wireless connectivity.

3. Supervisory Controller Design

The supervisory controller governs the distributed PFC connected loads using wireless communication link and a server. The response of the supervisory controller is slower than the individual PFC controllers. The control system configuration, design challenges and solution are discussed below.

3.1. Control System Configuration

The functional block diagram of the supervisory reactive power control scheme is shown in Figure 5 for the power network of Figure 1. Figure 5 describes the role of the supervisor which is comprised of a PI controller and a distributor. To design the proper PI controller, the system should be analyzed in the control system perspective. By that manner, supervisory reactive power compensation system can be modeled as in the control system as shown in Figure 6.

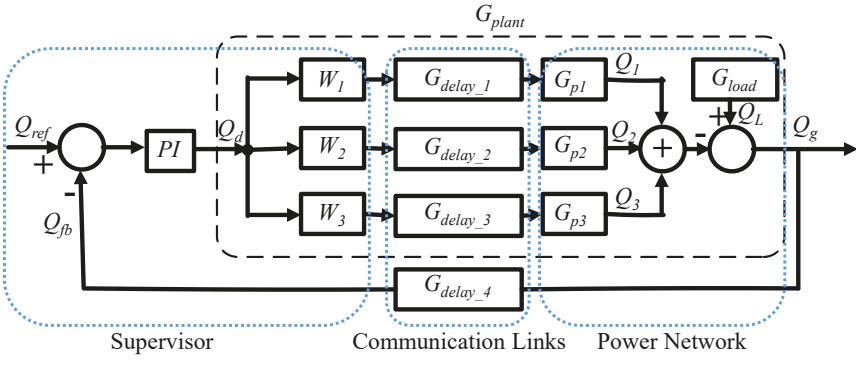


Figure 6. Control block diagram for reactive power compensation with multiple PFCs.

In the control block diagram, W_1, W_2 and W_3 are the weighting factors of the distributor. $G_{delay\_n}(s)$ is the transfer function of the communication delay due to wireless links. G_{load} is the transfer function for conventional loads. $G_{p1}(s)$, $G_{p2}(s)$ and $G_{p3}(s)$ are transfer functions of the PFC converters including their controllers for reactive power compensation. To design the proper PI controller, all PFC converters, delays and loads transfer functions have been put together and considered as plant, $G_{plant}(s)$. The output of the PI controller determines the reactive power demand, Q_d. The transfer function of the overall feedback loop can be written as in (15).

$$H(s) = \frac{G_{PI}(s)G_{delay\_4}(s)G_{plant}(s)}{1 + G_{PI}(s)G_{delay\_4}(s)G_{plant}(s)} \tag{15}$$

For asynchronous unequal delays and dynamic loading conditions the transfer function of the plant can be written as in (16).

$$G_{plant}(s) = G_{load}(s) - tr\left(\begin{pmatrix} W_1 & 0 & 0 \\ 0 & W_2 & 0 \\ 0 & 0 & W_3 \end{pmatrix}\begin{pmatrix} G_{delay\_1}(s) & 0 & 0 \\ 0 & G_{delay\_2}(s) & 0 \\ 0 & 0 & G_{delay\_3}(s) \end{pmatrix}\begin{pmatrix} G_{p1}(s) & 0 & 0 \\ 0 & G_{p2}(s) & 0 \\ 0 & 0 & G_{p3}(s) \end{pmatrix}\right) \tag{16}$$

where, $G_{plant}(s) = \frac{Q_g(s)}{Q_d(s)}$, $G_{p1}(s) = \frac{Q_1(s)}{Q_1^*(s)}$, $G_{p2}(s) = \frac{Q_2(s)}{Q_2^*(s)}$, $G_{p3}(s) = \frac{Q_3(s)}{Q_3^*(s)}$. tr denotes trace of the matrix. Although Equations (15) and (16) are seem like deterministic representation of the feedback system, the dynamic nature of $G_{plant}(s)$ can cause this representation to yield inaccurate results. $G_{plant}(s)$, changes with the change of $G_{load}(s)$, $G_{delay}(s)$, $G_{p1}(s)$, $G_{p2}(s)$, $G_{p3}(s)$, W_1, W_2 and W_3 . $G_{load}(s)$ changes with the change of load demand. The response of $G_{p1}(s)$, $G_{p2}(s)$ and $G_{p3}(s)$ are mutually independent and asynchronous because of the different command schedules for different PFC converters. The transfer functions for $G_{p1}(s)$, $G_{p2}(s)$ and $G_{p3}(s)$) can be determined from Section 2.2. $G_{delay}(s)$ is the reason for multiple phase shifts between commands. W_1, W_2 and W_3 are variable with respect to the capacity of the PFC converters. As a result, $G_{plant}(s)$ has uncertainty, non-linearity and multiple asynchronous phase shifts in dynamic conditions.

3.2. System Identification

Because of the uncertainty, non-linearity and asynchrony, accurate G_{plant} can't be determined from (16) at any instant. So, alternative method is proposed to get the transfer function response characteristics. System identification method is applied to get the characteristic of the system. The system has been identified for G_{plant}, G_{p1}, G_{p2} and G_{p3} by applying step input and measuring settling time. The settling time is the main feature that has been used to design supervisory controller considering it is an asynchronous distributed system. The settling time depends on the transfer function of the system.

3.3. Solution for Multiple Asynchronous Phase Shift

Different settling time, wireless communication delay time and overall response time for the proposed supervisory control system are explained by timing diagram in Figure 7. The timeslots t_1, t_2 and t_3 are communication delay time for PFCs; in other words those are settling time of G_{delay_n}. After these time slots PFCs execute their received command from supervisory controller within their settling times. The received commands are reference amount of reactive power assigned for the individual PFC converters. The necessary times for reactive power compensation of PFC's are t_{1_s} , t_{2_s} and t_{3_s}; in other words these are settling time of G_{p1}, G_{p2} and G_{p3}. t_w is a flexible waiting time before getting reactive power measurement from varmeter.

t_g is the communication time slot assigned for varmeter to send data to supervisor. The optimal value of t_w and t_g are determined by from the experiments. The value of t_{1_s} , t_{2_s} , t_{3_s} , t_w and t_g are determined by system identification method as discussed in Section 3.2. The overall value of t_1, t_2 and t_3 depends on the communication link and should be determined with certainty. The value of t_w can be adjusted to ensure certainty of the response. All the time slots are added in (17) to get the minimum optimal sample time, T_s, for the supervisory controller.

$$T_s = t_w + t_g + t_1 + \sum_{n=1}^{N=3} t_{n\_s} \tag{17}$$

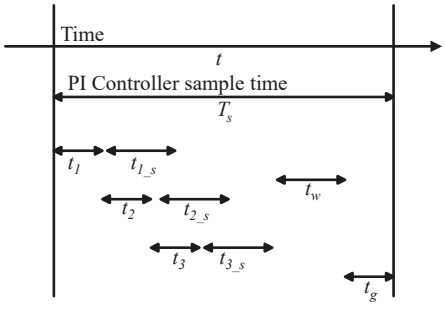


Figure 7. Time slots consideration for supervisory controller design.

3.4. PI Controller Design

The minimum sample time, T_s, is used to design the discrete PI controller. The block diagram for the discrete PI controller is shown in Figure 8a. The integrator for the PI controller has a sample time of T_s. The output of the PI controller is Q_d, which is the reactive power demand from all of the PFC converters. Since the system has certainty of response using the sampling time of T_s, Ziegler-Nichols rule can be used to design PI compensator for this system [36–38]. Using the rule, the values of K_p and K_i are determined by (18) and (19) for the ultimate gain K_u.

$$K_p = 0.5K_u \tag{18}$$

$$K_i = 0.45K_u \tag{19}$$

For the wireless communication, communication time is much higher than response time of PFC converters that is, $t_1 >> t_{1\_s}$. The value of ultimate gain K_u is 1 for such system.

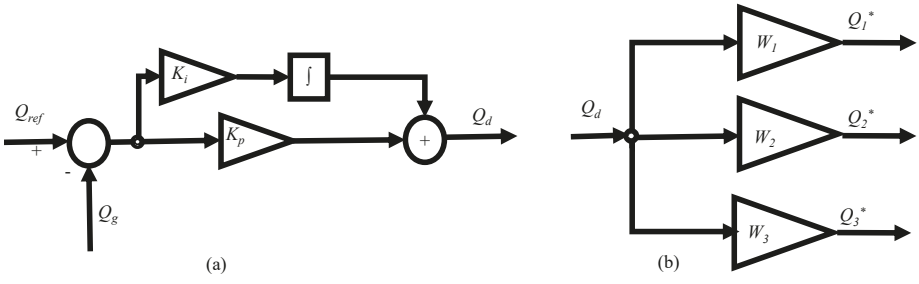


Figure 8. Detail diagram of supervisory control (**a**) proportional-integral (PI) controller (**b**) Distributor.

3.5. Distributor Design

The value of the Q_d is distributed by the weighting factors W_1, W_2 and W_3. The weighting factors are determined from the maximum reactive power support capacities (Q_{1_max}, Q_{2_max} and Q_{3_max}) of the PFC converters. The value of weighting factors can be determined from (20).

$$W_n = \frac{Q_{n\_max}}{Q_{1\_max} + Q_{2\_max} + Q_{3\_max}} \tag{20}$$

4. Testbed Description

The configuration for hardware-in-the-loop (HIL) testbed for the proposed supervisory controller and scenario is shown in Figure 9.

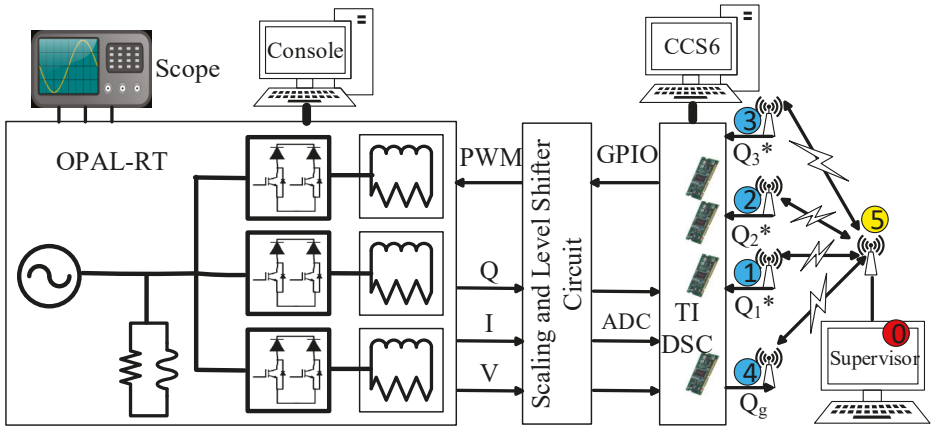


Figure 9. Block diagram of the testbed.

The testbed consists of an Opal-RT real-time simulator OP4510, TI-DSCs, scaling and level shifter circuits, AwiaTech wirelessHART modules [39], ESP8266 Wi-Fi modules [40] and communication links. The proposed power network has been simulated in real-time using OP4510 real-time simulator. The waveforms of voltages, currents and reactive power were observed from both the oscilloscope and the computer console connected to the OP4510. The real time simulation data is also stored in .mat files from the console for further analysis. The measured voltages, currents and reactive powers from OPAL-RT are scaled down using the Op-Amp based circuit to use in the ADC of the TI-DSCs. One of the TI-DSCs transmits the value of reactive power consumption from the grid input power node. The rest of the TI- DSCs are designated to control the PFC converters. The controller of Figure 3 has been implemented to those TI-DSCs. TI-DSCs were programmed using Code Composer Studio v.6 (CCS6). All the TI-DSCs are connected to AwiaTech wirelessHART modules and ESP8266 Wi-Fi modules via serial (UART) connections for the communication links to the supervisor. Communication nodes are numbered from 0 to 5 in Figure 9. The connections of ESP8266 Wi-Fi and AwiaTech wirelessHART modules were switchable in the node 1–4. Node 5 has different configurations based on the communication preference. The description of wireless network configuration will be discussed in the Subsection 4.3.1.

The HIL testbed is validated by three types of physical devices: wireless modules, digital controllers and real time simulator. The actual testbed setup is shown in Figure 10. OP4510 is used to simulate the power stages in real time; TI-DSCs are used as controllers of the PFC converters; AwiaTech wirelessHART or ESP8266 Wi-Fi modules are used as interface of communication link; Op-Amp based circuits have been used for the ADC scaling and buffers have been used for the level shifting of PWM signals; a supervisory controller have been implemented in the computer that is connected to the internet and the master AwiaTechHART module. The supervisory controller ensures zero reactive power consumption from the grid. The components of the test bed are described in the following subsections.

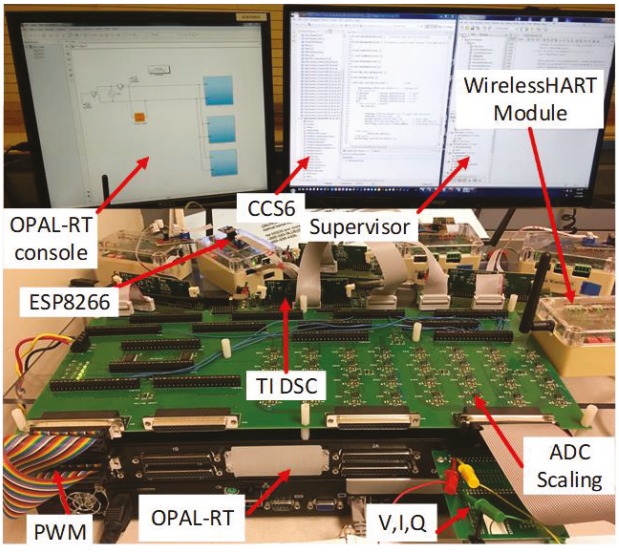


Figure 10. Hardware in the loop testbed set up.

4.1. Hardware Description

4.1.1. Real Time Simulator

The power stages of the PFC converters, loads, measurement of voltage and current and active and reactive power are simulated in real-time (RT) using OPAL-RT real-time simulator, OP4510. It has 128 I/O channels, a quad core INTEL Xeon 3.3 GHz processor as well as a Kintex 7 FPGA for sub-microsecond simulation time steps [41]. Each core of the processor has the capability to simulate up to 20 µs time step. The system is compatible with Simulink and the SimPowerSystems library. The OP4510 is also connected to an oscilloscope to monitor voltage, current and reactive power in real time. For this testbed, analog values of voltages and currents are routed from the FPGA based model to the DAC channels directly. The PWM signals are interfaced with digital input pins which drive the FPGA based modesl of IGBTs. These two steps ensure sub-microsecond RT simulation. The reactive power is calculated using Fourier transform in the CPU core at a step of 25 µs and later routed to DAC channels.

4.1.2. ADC Scaling and Level Shifting Circuit

The analog output signals for V, I and Qs are $\pm$16 V in OP4510. The ADC level of TI-DSCs is limited to 0–3.3 V. To interpret and match the analog signal level properly, Op-Amp (TL082C) based scaling and offsetting circuits have built. The GPIO of TI-DSC has a logic level of 3.3 V and OP4510 takes 5 V PWM input. As a result, a 74HC240D IC has been used as a buffer for level shifting. The level shifting and ADC scaling circuit has been built up in the same PCB as shown in Figure 10. The PCB also has connectivity to Opal-RT by two DB37 connectors and connect TI-DSCs with the 20 pin connectors. This circuit has 32 analog and 32 digital re-routable channels. The ADC scaling and level shifting circuit is shown in Figure 11.

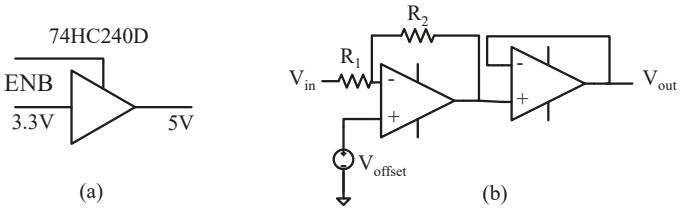


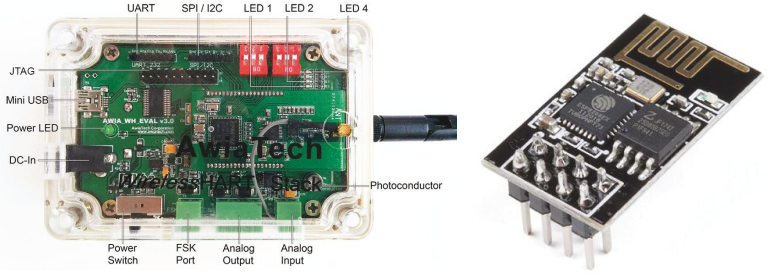
Figure 11. Interface circuit: (**a**) level shifting (**b**) ADC scaling.

4.1.3. Texas Instruments Digital Signal Controller

The TI-DSC, TMS320F28335, was selected to control the PFC converters that were simulated in real-time on the OP4510. In addition, the DSC code includes UART communication which interfaces either the AwiaTech wirelessHART or the ESP8266 Wi-Fi modules. The TMS320F28335 is a 32 bit floating point processor with clock speeds up to 150 MHz and 18 PWM channels [42].

4.1.4. WirelessHART and AwiaTech Wireless 220 Module

To implement the communication system for the testbed, AwiaTech WirelessHART (Wireless Highway Addressable Remote Transducer) modules were chosen. WirelessHART is a simple, secure, reliable, real-time and open-standard networking technology, operating in the 2.4 GHz ISM radio band [43]. It uses a time-synchronized, self-organizing and self-healing mesh network architecture. At the bottom of its communication stack, WirelessHART adopts IEEE 802.15.4-2006 [31] as the physical layer. On top of that, WirelessHART defines its own time-synchronized data link layer. In WirelessHART, communications are precisely scheduled based on Time Division Multiple Access (TDMA) and employ a channel hopping scheme for added system data bandwidth and robustness [43]. AwiaTech Wireless provides a variety of interfaces such as UART, JTAG, SPI/I2C and USB, which provides us the flexibility for interconnecting the TI DSC. The features of this module are shown in Figure 12a.



(**a**) AwiaTech WirelessHART Module (**b**) ESP8266 Wi-Fi module

Figure 12. Wireless communication modules.

4.1.5. WiFi and ESP8266 Module

Four ESP8266 modules have been used in the test bed [40]. ESP8266 has serial communication (UART) features as in Figure 12b. It can give any microcontroller access to your WiFi network and maintain TCP/IP protocol by IEEE standard 802.11/b/g/e [32]. These modules have been programmed using an Arduino programming environment.

4.2. Software Components Description

4.2.1. TI DSC Code Architecture

The PFC controller has a 20 µs sample time. It generates a 50 kHz PWM signal. One interrupt has been used to compute ADC values, scaling, controller operation and the PWM update. For the low speed communication links, a polling method has been used. The communication function is executed in an infinite while loop. All the functions are executed within a 20 µs window.

The ADC interrupt and controller computations consume only 12 µs and the remaining 8 µs is designated for communication through UART. Figure 13 describes the interrupt and while loop structure.

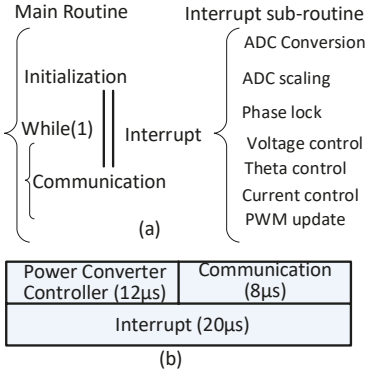


Figure 13. (**a**) Code structure of TI DSC (**b**) Execution time of code sections.

4.2.2. Host Program

AwiaTech wireless provides a Java package "Host" which is encapsulated within a series of APIs, enabling users to write programs which process all the data acquired from WirelessHART network. Based on these APIs, "Host" software is customized as an interface between the wireless network and the supervisory controller. This design separates communication and control, which provides scalability to use other wireless communication technologies without modifying the controller code. In addition, this architecture enables the convenient use of other languages. The host program has been modified using TCP/IP link as well. The TCP/IP link has been used to maintain communication links to the ESP8266.

4.2.3. Supervisory Controller Implementation

The supervisory controller gives the control signal to the power converters. It is also capable of collecting data from the input port of the power network. The algorithm for the supervisory controller is written in C++ code and later called from the JAVA platform which maintains communication functions. The supervisory controller has a low speed proportional integral controller with a limiter and distributor as discussed in Section 3.

4.2.4. Dataflow

A complete dataflow is presented in Figure 14. The data flow in the test bed is composed of 8 steps, starting from a TI DSC and ending in a TI DSC. First, a TI-DSC sends a HART-IP command containing data to the AwiaTech wireless (device) through UART. Second, AwiaTech wireless forwards this command to the access point based on WirelessHART standard. Third, the access point sends data to a desktop running Host and Gateway software with UART over USB using a FTDI chip. Fourth,

after Host receives the data, it forwards it to the supervisory controller. For the WiFi network, HART-IP has been decoded at ESP8266 and sent to the AP and host through the Wi-Fi. Our Host program will exchange messages with the controller through Stdin and Stdout. The dataflow in the other direction will follow the same steps in reverse.

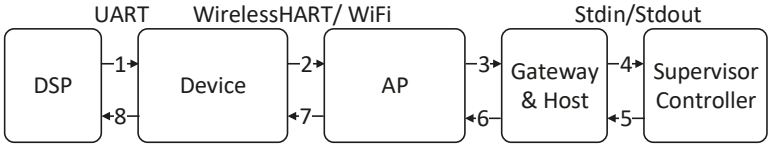


Figure 14. Dataflow between TI DSC and supervisory controller.

4.3. Communication Link Description

4.3.1. Wireless Communication Set Up

The communication network topology for WiFi and WirelessHART has been shown in Figure 15.

Either all ESP8266 or all AwaiaTech modules are connected to the TI-DSC through UART. The UART to module connections are switchable for Wi-Fi and wirelessHART. Four AwiaTech modules maintain communication links with a fifth AwiaTech wireless module, which is connected to a host computer, where the supervisory controller is running.

On the other hand ESP8266 is connected to the internet via Wi-Fi and a router. The supervisory controller can use internet to control the PFC converters for Wi-Fi network preference. Multiple unidirectional PFC converters contribute reactive power support by following a reference command by a supervisory controller via wireless modules. Real-time algorithms or strategies for energy and power management systems can validate their performance in this testbed. The network topology in our experiments is shown in Figure 16, the blue circles are devices connected to TI DSCs; the yellow circle is the access point and the red circle is the gateway. A dotted line indicates the wireless communication through WirelessHART or WiFi. The solid line indicates the wired communication through USB or Ethernet. The numbers on the lines show the signal strength of the wireless links. The Figure 16 shows all the components in our network and their unique IDs, types and scan periods.

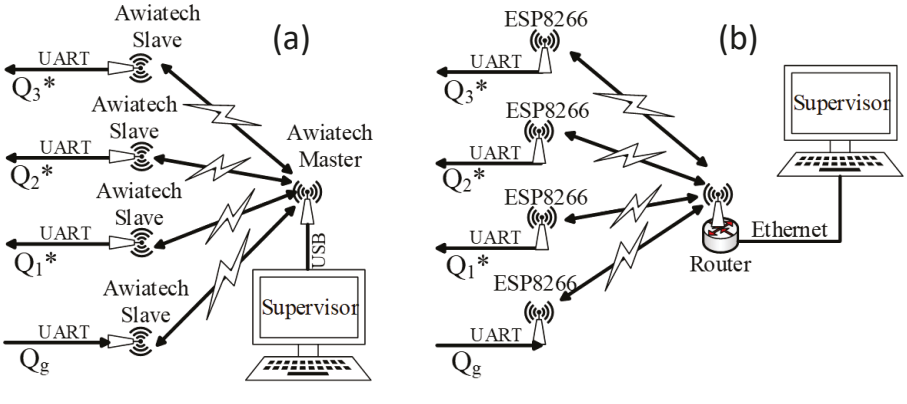
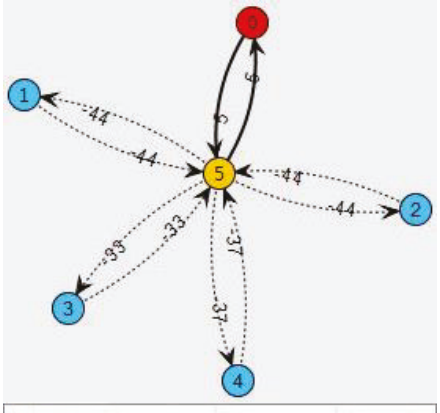


Figure 15. Wireless network topologies for testbed (**a**) WirelessHART (**b**) WiFi.



ID	Unique ID	Type	Scan Period
4	001b1ee28e0203f4	DEVICE	_0_ms
3	001b1ee28e0203f3	DEVICE	_0_ms
0	001b1ef981000002	GATEWAY	_0_ms
2	001b1ee28e0203f0	DEVICE	_0_ms
5	001b1ee18b020321	AP	_0_ms
1	001b1ee28e0203f2	DEVICE	_4_sec

Figure 16. Wireless network topology.

4.3.2. Integrity of the Specification

The Figure 17 shows an example of simplified network schedule which is shared with all the devices and the access point in the network. The super-frame size is 500 ms and two up-links and down-links for each device are statically allocated inside one superframe. In Figure 17, a time slot is represented by a small square with a number and an arrow. For example, 2 ↑ means the time slot is scheduled for Device 2 as an up-link. The wireless message exchanging sequence is shown in Figure 17. At the beginning of a super-frame, the TI-DSC sends measurement to Device 1.

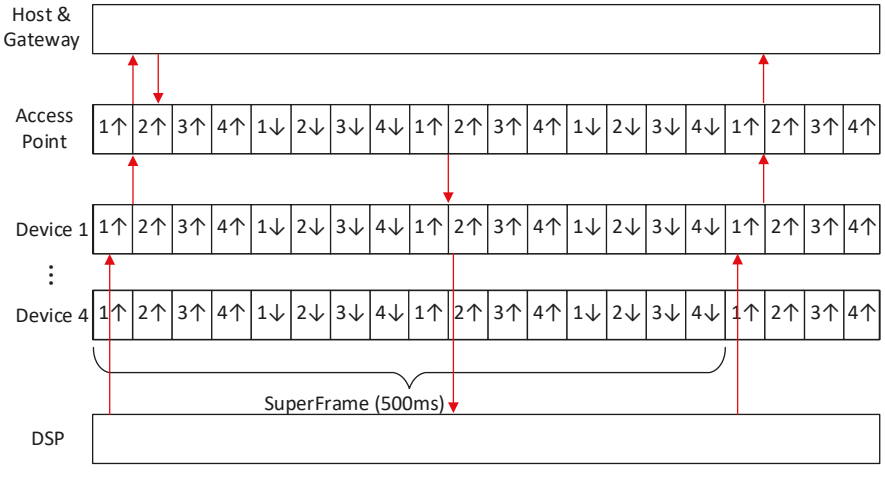


Figure 17. Communication schedule configuration.

Then Device 1 sends the data to an access point within its own timeslot. After receiving the data, the access point sends the data to the host. Next, the Host software will send what it just received to the supervisor controller for calculation. After that, the controller will send data back to control the TI DSC. It will go through the path in reverse. The access point will get the data and wait for the time slot allocated for Device 1. Once the time slot arrives, the access point sends the data down to Device 1 and then Device 1 sends data to the TI-DSC through UART. Theoretically, if we set the super-frame length to be 500 ms and within one super-frame and we allocate two time slots as up-links, the smallest sampling period would be 250 ms. However, due to the noisy wireless environment, we chose a much larger sampling rate and super-frame length. From the wireless link test, we were able to make the super-frame size 1.5 s without any data loss.

5. Experimental Results

The test bed has been implemented to validate the supervisory controller for reactive power support using the proposed power network of Figure 1. OP4510 has simulated the power network in real-time. It takes PWM signal as input and gives analog signals as output. Rest of the components are actual physical device in the HIL test bed. Multiple tests have been conducted to validate the idea of reactive power support and supervisory controller.

5.1. Reactive Power Compensation in a Single PFC Converter

Reactive power has been supported by applying controller of Figure 3 to a PFC converter. The wave form of voltage and current in a PFC converter for different conditions has been captured using an oscilloscope and shown in the following figure. The waveforms are collected from the analog output of the OP4510 real-time simulator. PFC 1 has been built up as in the circuit of Figure 2 using $r_L = 1$ mΩ, $L = 2$ mH, $C = 2000$ μF and $r_C = 2$ mΩ. PFC 1 is rated for $V_{in} = 120$ V(rms), $f = 60$ Hz, $P_{out} = 1.1$ kW, $V_{out} = 250$ V(DC) and $R_{Load} = 56.79753$ Ω. Different power conversion criteria for PFC 1 under conditions of Figure 18 are shown in the Table 1.

Figure 18a shows the input current and voltage waveforms without applying any control that is, current flows through the diode only.

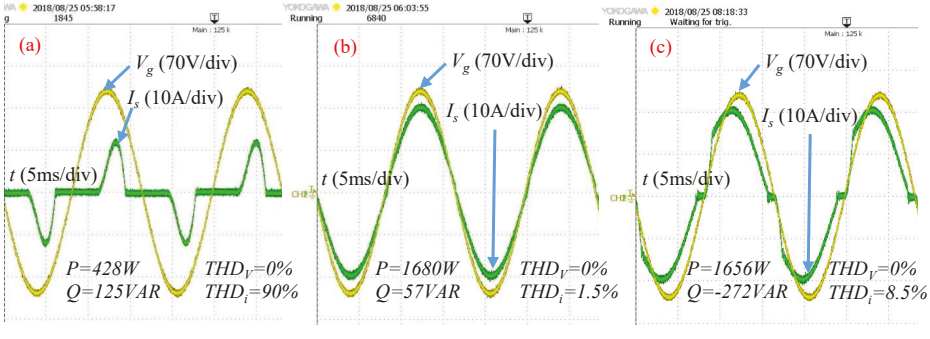


Figure 18. Input voltage and current waveforms in PFC 1: (**a**) no controller, (**b**) in phase controller, $\theta \approx 0$ and (**c**) leading phase controller, $\theta < 0$.

Table 1. Power conversion in PFC 1 for different conditions.

Conditions at Figure 18	P_{in} (W)	Q_{in} (VAR)	THD_{V_g} (%)	THD_{I_s} (%)	$V_{out}(DC)$ ($Volt$)	P_{out} (W)
a	428	125	0	90	154	396
b	1680	57	0	1.5	250	1100
c	1656	−272	0	8.5	250	1100

This condition has very poor performance and can not fulfil the rated conditions. It has very high total harmonic distortion (THD) for the input current. After applying the reactive power compensation algorithm of Figure 3, voltage and current are almost in phase as in Figure 18b. Reactive power has not been injected for this case that is, reactive power reference is zero, $Q_1^* = 0$. Although Q_1^* is equal to zero but, Q_1 is not exactly zero because of delays, offset and measurement errors. In this case, current distortion is minimum. Leading phase of current has been achieved as in Figure 18c as Q_1^* has been set to negative values. Hence, reactive power has been supported by PFC 1. In this case, the current is not a pure sine wave at zero crossing because of zero crossing distortion. The distortion phenomenon has been considered to determine the maximum capacity of reactive power support (Q_{max1}) for PFC 1. Since, the household load is very small with respect to grid, the voltage supply has been considered to be coming from an infinite bus. As a result, distortion for input voltage, THD_{V_g} is zero in the realtime simulation.

5.2. Reactive Power Support Using Supervisory Controller

After setting up the communication networks successfully, the HIL test was conducted for the proposed residential power network. For the proposed scenario, rated grid voltage is 120 V(rms), 60 Hz. Conventional load is 1500 VA with 0.8 power factor that is, P_L = 1200 W, Q_L = 900 VAR. Rated output voltage, V_{out}, of all three PFCs is 250 V(DC). Output power, P_{out}, rating of the PFC's are 1.1 kW, 1.5 kW and 1.7 kW.

Weighting factors used in supervisory controller W_1, W_2 and W_3 are 0.25, 0.35 and 0.4 respectively. Reactive power has been supported by the PFC converters to the load as shown in the in Figure 19. In this case, real-time simulation has been conducted for communication and control sample time, T_s = 4 s. Supervisory controller engagement time has been set as reference, $T = 0$, on the time axis. Logged data from OP4510 shows that reactive power consumption from grid Q_g becomes 0 VAR within 75 s of applying the controller. The initial and final value of the reactive power for the grid, the load and the PFCs is shown in the Table 2.

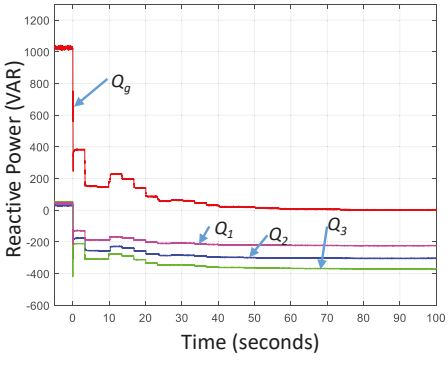


Figure 19. Reactive power support by 3 PFC converters and supervisory controller.

Table 2. Reactive power in different nodes of the proposed power network.

State	Time (s)	Q_g (VAR)	Q_L (VAR)	Q_1 (VAR)	Q_2 (VAR)	Q_3 (VAR)
Initial	0	1025	900	44	33	48
Final	75	0	900	−225	−305	−371

5.3. Reactive Power Support in Different Conditions

The performance of the supervisory controller has been tested for different conditions.

5.3.1. Variation of Load

The designed supervisory controller has been tested for loading conditions of (P_L = 1350 W, Q_L = 654 VAR), (P_L = 1200 W, Q_L = 900 VAR) and (P_L = 1050 W, Q_L = 1072 VAR). For all loading conditions, Q_g become 0 VAR within 75 s.

5.3.2. Variation of Wireless Network

The supervisory controller was tested using WirelessHART and Wi-Fi. It compensated grid reactive power for both networks as shown in Figure 20a.

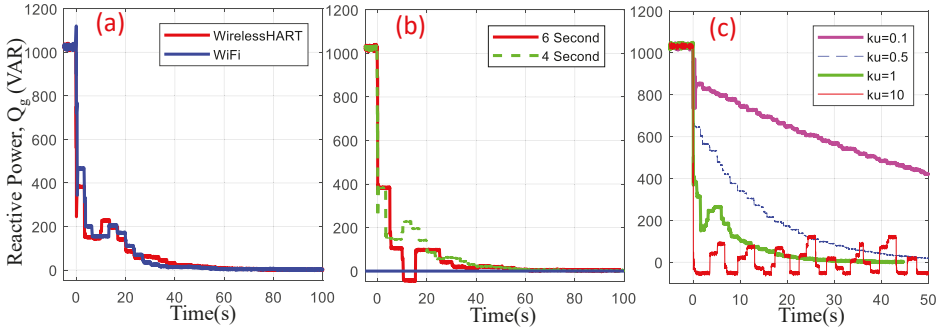


Figure 20. Performance of supervisory controller: (**a**) network variation, (**b**) sampling time variation and (**c**) gain variation.

5.3.3. Sampling Time Variation

The effect of different communication sampling times has been evaluated in Figure 20b. For four and six second sampling times, supervisory controller regulated Q_g to 0 VAR. The higher the sampling time, the slower the response time for overall reactive power compensation. Minimum stable communication and control sampling time for this system has been measured to be 1.5 s. This sampling time has been used for optimal controller.

5.3.4. Gain Variation and Optimal Controller

To verify the optimal supervisory controller, the response of reactive power compensation has been compared for different k_u, k_p and k_i gains. The response has been judged by settling time, overshoot, undershoot and stability. Figure 20c shows performance of supervisory controller with different gains. This controller has used T_s = 1.5 s communication sampling time. The settling time and other factors of performance for the PI compensator are shown in Table 3.

Table 3. Supervisory controllers performance with different PI gains.

K_u	K_p	K_i	Stability	Settling Time	Comments
0.1	0.05	0.045	Stable	250 s	Very slow response
0.5	0.25	0.225	Stable	75 s	slow response
0.8	0.4	0.36	Stable	45 s	Good response
1	0.5	0.45	Stable	40 s	Optimum response
2	1	0.9	Marginally stable	20 s	Undershoots happen, large steady state error, inject Q to grid
5	2.5	2.25	Unstable	–	Undershoots happen, large steady state error, distributor failure
10	5	4.5	Unstable	–	Completely unstable

5.4. Reactive Power Support in Dynamic Load

Different load profiles of Table 4 have been applied to test the supervisory controller. Reactive power demand were changed as the load changed.

Load profile 1 has been applied for the conditions of Figure 21a,c. Load profile 2 has been applied and results have been gathered in Figure 21b. The PFC converters used for Figure 21a,b have the power rating(P_{out}) of P_1 = 1.1 kW, P_2 = 1.5 kW and P_3 = 1.7 kW. The maximum reactive power supply capacity of those PFC converters are $Q_{max1} = -300$ VAR, $Q_{max2} = -400$ VAR and $Q_{max3} = -600$ VAR. Q_{max1}, Q_{max2} and Q_{max3} have determined the weighting factors W_1, W_2 and W_3 by (20). Load profile 1 is based on the power factor change and load profile 2 is based on apparent power demand increment.

Dynamic response of Figure 21c used load profile 1 but it used identical 3 PFC converters. In this case, P_1 = 1.5 kW, P_2 = 1.5 kW, P_3 = 1.5 kW, $Q_{max1} = -400$ VAR, $Q_{max2} = -400$ VAR, and $Q_{max3} = -400$ VAR. As a result, reactive power contribution from PFC converters is equal at different times in the real time simulation.

Load profiles have been implemented by changing the loads using an external switch. As a result there is a transient reactive power spike and an unequal load profile duration. For all of these conditions, the optimal controller has been used, which ensured the stable and quickest response. THD_{V_g} and THD_{I_g} have also been recorded for all the tests. THD_{V_g} for all the tests is 0% as the grid has been considered as an ideal voltage source in the real-time simulation. THD_{I_g} has varied between 4% to 10.65% for all the loading conditions after the settling times. It was observed that an increase in real and reactive power consumption ratio correlated with a decrease in THD_{I_g}.

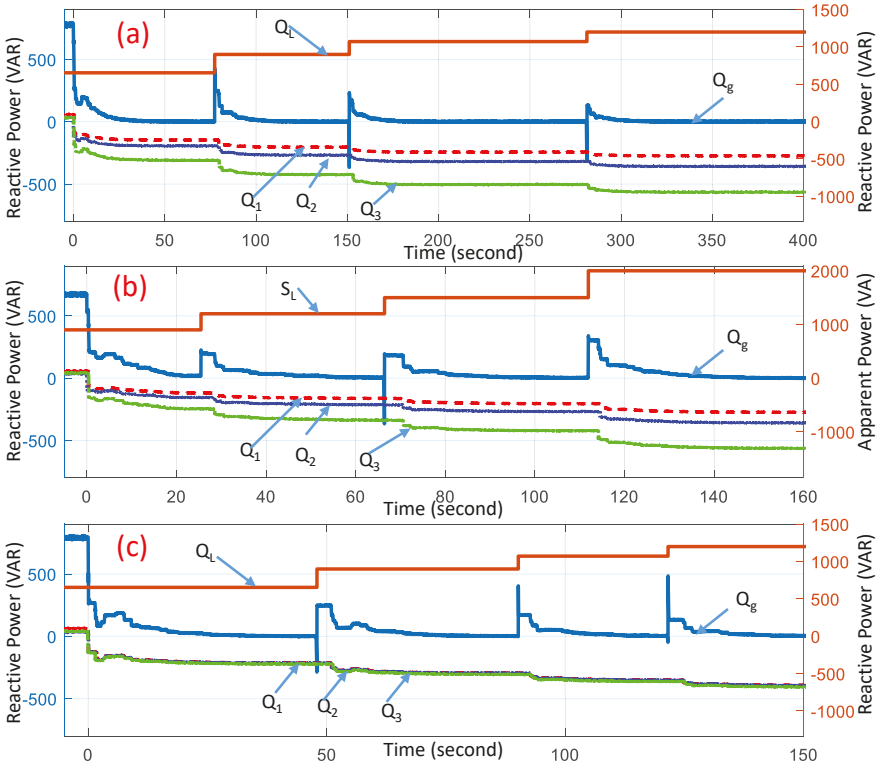


Figure 21. Reactive power support in dynamic loads: (**a**) load profile 1, (**b**) load profile 2 and (**c**) Load profile 1 with equal reactive power support capability.

Table 4. Load profiles for dynamic performance test.

Load Profile 1				
Loading Stage	S_L (VA)	P_L (W)	Q_L (VAR)	*Power Factor*
1	1500	1350	654	0.9
2	1500	1200	900	0.8
3	1500	1050	1072	0.7
4	1500	900	1200	0.6
Load Profile 2				
Loading Stage	S_L (VA)	P_L (W)	Q_L (VAR)	*Power Factor*
1	900	720	540	0.8
2	1200	960	720	0.8
3	1500	1200	900	0.8
4	2000	1600	1200	0.8

6. Conclusions

The PFC converters are considered as reactive power resources in this paper. The supervisory controller is proposed to manage those resources. The WiFi and WirelessHART have provided the interface between the supervisory controller and reactive power resources. The optimal sampling time of the supervisory controller has been determined by various tests. The optimal gain is explained theoretically and validated experimentally. The dynamic performance of the supervisory controller has been validated using different load profiles with the reactive power demand, PFC capacity and load variations. The HIL test results prove the concept and feasibility of additional reactive power support from PFC converters in residential applications. The proposed controller design method will be useful for other small-scale power and wireless network integration.

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New DC Grid Power Line Communication Technology Used in Networked LED Driver

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Abstract: In order to reduce the cost and improve the reliability, real-time performance, and installation convenience of remote-controlled light-emitting diode (LED) lighting systems, a networked LED driving technology based on the direct current (DC) grid power line carrier is proposed. In this system, an alternating current (AC)/DC bus converter converts the mains into a DC bus with multiple distributed LED drive powers on the DC bus. The AC/DC bus converter receives the user's control command and modulates it into the DC bus voltage. The DC bus waveform changes to a square wave containing the high and low changes of the address information and command information. The LED drive power of the corresponding address receives energy from the DC bus and demodulates the commands, such as turning the lights on and off, dimming, etc., and performs the action. In order to make the waveform of the AC/DC bus converter have better rising and falling edge, this paper adopts the half-bridge topology with variable modal control. In the modulation process, the circuit works in buck mode and boost mode. Distributed LED drivers have DC/DC circuits and very simple demodulation circuits that dissipate energy and information from the DC bus. Through experiments, the technology not only simplifies the use of communication technology in application, but also reduces the application difficulty.

Keywords: PLC; bus converter; DC bus; LED driver

1. Introduction

With the rapid development of light-emitting diode (LED) technology, it is widely predicted that LED will become a new generation of lighting sources. Smart network control is a hot research topic in the field of LED lighting applications. In this application, multiple LED devices generally form an intelligent lighting system through a network, and the LED devices can usually be remotely controlled. In addition to road lighting for large-scale applications [1–4], most of these smart LED lighting systems are often used indoors or outdoors, and the scale is small [5–7].

Figure 1 shows a case for a small-scale LED smart lighting system, such as for commercial lighting, home lighting, landscape lighting, wall washers, high pole lights, etc. In these applications, the number of lamps is small, the distance between two adjacent LED light sources is relatively close, and a computer is typically used to remotely control turning on, turning off, and dimming the lights.

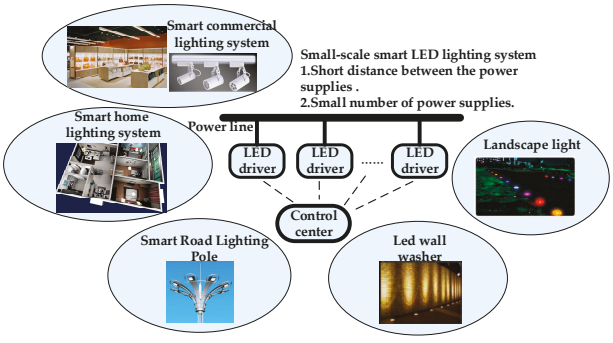


Figure 1. Common small networked control light-emitting diode (LED) smart lighting system.

In this small LED smart lighting system, communication between LED drivers is necessary to achieve control. Which communication technology is used determines the real-time performance and reliability of control in the system, while at the same time it also affects the cost, installation, and maintenance. Figure 2 shows descriptions of several common traditional lighting system communication schemes and their characteristics. These small LED lighting systems require a lower-cost solution, however, for 0–10 V, pulse-width modulation (PWM) control, digital addressable lighting interface (DALI) [8–14] and other remote-control schemes, and additional communication lines must be laid, which is unfavorable for installation and maintenance and costs more. Power line communication (PLC) [15–18] and the remote-control scheme of micropower wireless communication have advantages in practical applications due to the convenient installation. However, the cost of such a solution is still high, which is not conducive to its promotion. Table 1 lists the characteristics of these four options.

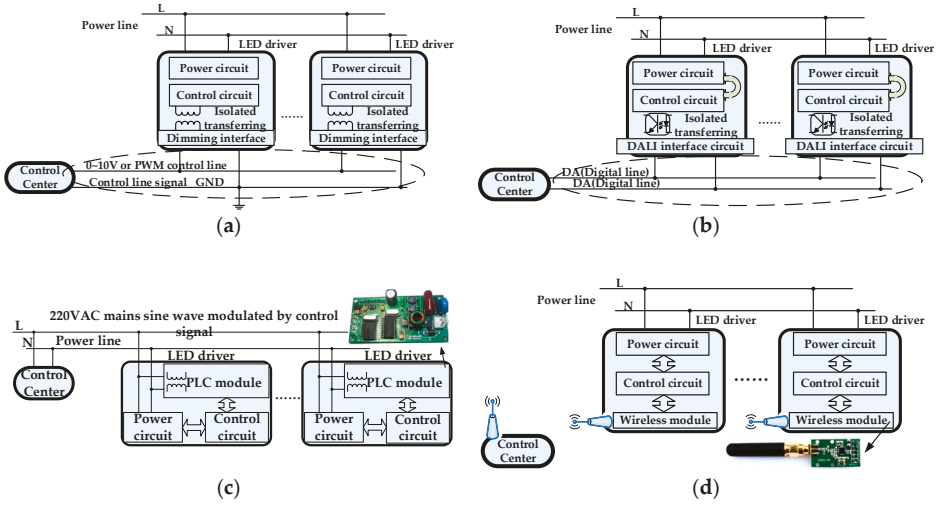


Figure 2. Common traditional remote control schemes: (**a**) 0–10 V or pulse-width modulation (PWM); (**b**) digital addressable lighting interface (DALI); (**c**) traditional alternating current (AC) grid power line communication; (**d**) traditional wireless.

Table 1. Features of common traditional remote control schemes.

Remote Control Scheme	Control Lines	Installation	Cost
0–10 V or PWM	2 Lines	Complex	High
DALI	2 Lines	Complex	High
Power line communication (PLC)	No	Very simple	High
Wireless	No	Simple	High

From the perspective of installation, the micropower wireless communication scheme needs to consider factors such as antenna and electromagnetic interference, which is greatly affected by space, and the PLC scheme is simpler. If the PLC solution can be further simplified, the cost and installation aspects are more advantageous. However, the traditional PLC solution is mainly used for alternating current (AC) mains grid, such as remote meter reading [19–21] and other applications. In the AC mains grid, PLC technology is relatively mature, and it is difficult to have major technological breakthroughs in a short period of time. It is difficult to reduce costs significantly. If power electronics can be used to transmit information while energy is being converted, the PLC module in Figure 2c may no longer be needed and the system cost may be greatly reduced. In the AC mains grid, since the existing transmission and distribution schemes are already very mature, it is difficult to implement communication using power electronics technology. However, if a direct current (DC) grid or an AC microgrid is constructed, it is easy to realize communication while transmitting DC power in the grid.

The LED lighting system based on DC grid has received attention. In [22] an indoor LED smart lighting system was proposed based on DC grid, as shown in Figure 3. The system uses an AC/DC converter to change AC mains to DC bus, and a number of distributed DC/DC LED drivers are connected to the DC bus. The system implements intelligent control and energy saving, but with the DALI communication protocol, a separate control line is still required. A similar DC bus architecture is also proposed in [23].

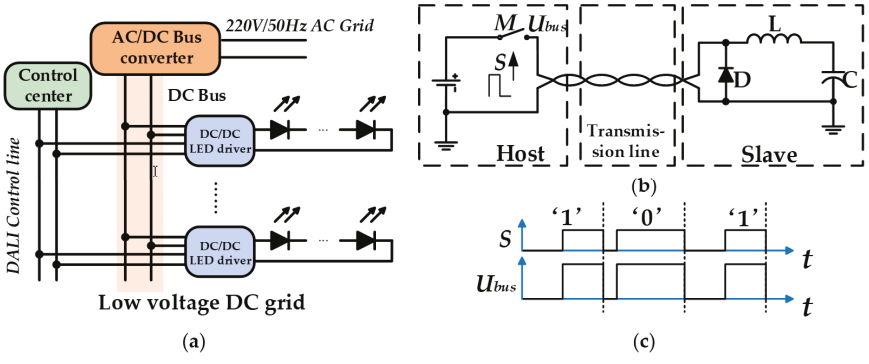


Figure 3. Traditional LED lighting system technology based on direct current (DC) grid: (**a**) Traditional networked LED system based on DC grid; (**b**) Traditional DC grid PLC technology; (**c**) the drive signal waveform of host switch M and the waveform of bus voltage U_{bus}.

PLC in the DC grid has also been studied in recent years, and this technology can eliminate the control line in Figure 3a. A novel DC PLC solution was proposed in [24], which is cheaper for small-scale power line communication applications. Figure 3b,c show the basic principle, as shown in the waveform: when the host switch M is turned on, the voltage U_{bus} goes high, representing logic 1. When switch M is turned off, voltage U_{bus} goes low, representing logic 0. The circuit works in the structure of the buck circuit, and the energy is stored in the output capacitor C of the slave. The change of the voltage U_{bus} during the energy transfer is detected by the slave, and the simultaneous transmission of energy and signals is realized. However, due to the influence of parasitic parameters

on the transmission line, the switching device of the circuit is subject to greater voltage stress than the conventional buck circuit.

Some papers have proposed DC PLC schemes [25–29], but they all need additional communication lines. They bring larger parasitic parameters and cause front-stage metal-oxide-semiconductor field effect transistor (MOSFET) high current spikes and damage when the MOSFETs are working at high frequency. So the front-stage MOSFETs need better performance requirements. They are more complicated if used for LEDs.

In order to overcome the problems of the above two types of research, this paper proposes a remotely controlled LED lighting system similar to the DC grid structure of Figure 3a, but with the control line omitted. In this system, an AC/DC bus converter converts the mains into a DC bus, and multiple distributed LED drivers are connected to the DC bus. The AC/DC DC bus converter receives the user's control command and modulates it into the DC bus voltage. The DC bus waveform changes to a square wave containing the high and low changes of the address information and the command information. The LED driving power source corresponding to the address receives energy from the DC bus and demodulates commands such as turning on the light, turning off the light, dimming, etc. In order to make the waveform of AC/DC DC bus converter have better rising and falling edge, this paper adopts the half-bridge topology with variable modal control. In the modulation process, the circuit works in buck mode and boost mode. Distributed LED drivers have DC/DC circuits and very simple demodulation circuits that dissipate energy and information from the DC bus.

With this remote control scheme, the following problems are solved:

1. Compared with 0–10 V, PWM, and DALI controlled systems, the communication line is omitted.
2. The traditional AC mains PLC module is saved, and the signal transceiving function is realized by power electronic technology.
3. Compared with the existing DC PLC technology, the influence of power line on communication is greatly reduced, and communication reliability is improved.

Compared with the conventional schemes described above, this scheme is simpler and costs less. This paper verifies the feasibility of this technology by experiments.

2. Light-Emitting Diode (LED) Networked Drive Technology Based on Direct Current (DC) Grid Power Line Communication (PLC)

2.1. System Architecture

The specific architecture of the LED lighting system proposed in this paper is shown in Figure 2a. It includes a control center, an AC/DC bus converter, a DC bus, and a distributed LED driver. The control center sends control signals to the LEDs to the AC/DC bus converter. This type of technology is relatively mature and can be used for wireless communication such as a General Packet Radio Service (GPRS). The bus converter converts the AC mains into a DC bus voltage v_{bus} with a maximum value of 48 V, and modulates the information to be transmitted into the bus voltage to make it high and low DC levels. The high voltage represents logic 1 and the low voltage represents logic 0. The DC bus is the transmission line, and the distributed LED driver as the load extracts energy from the DC bus drives the LED light source and demodulates the signal from the bus.

2.2. New DC Power Line Carrier Energy and Information Demodulation Principle

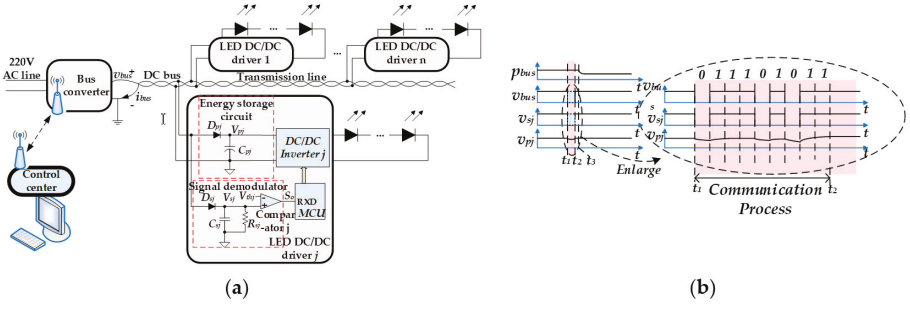
The master/slave communication mode is between the AC/DC bus converter and the distributed LED driving power source. The former is the master, the latter is the slave, and the DC bus is used as the medium to provide energy and transfer information to the slave.

The LED driver power supply includes three parts: an energy demodulation circuit, a signal demodulation circuit, and a DC/DC converter. The energy and signal demodulation circuits are both half-wave rectification circuits, as shown in Figure 4a. Taking the *j*th LED driving power supply in

Figure 4a as an example, the energy demodulating circuit is connected in series with the DC/DC converter, and the output of the signal demodulating circuit is connected to the control circuit of the DC/DC converter. The difference between the two is that the energy demodulation circuit's output capacitance C_{pj} has a large capacitance value. When the v_{bus} voltage is 0, the energy of the DC/DC converter of the latter stage can still be supplied for a period of time, that is, v_{pj} is maintained within the allowable ripple voltage range to keep the circuit working properly.It remains stable for a long time; the output capacitance value C_{sj} of the latter is small. When the v_{bus} voltage is 0, v_{sj} is discharged through the resistor R_{sj} and quickly falls to 0, so that the change of v_{sj} is consistent with the change of v_{bus}. Taking the waveform in Figure 4b as an example, the process of demonstrating a remote dimming operation has the following stages:

t_1: The output of the AC/DC bus converter is 48 V DC, and the load is full power. During this time, the bus converter receives the *j*th LED drive power dimming command from the control center to address A_j.

t_1–t_2: The bus converter modulates the information into the DC bus, and the bus voltage v_{bus} changes to the waveform shown in Figure 4b. All LED drive power supplies receive the command, but only the *j*th addresses A_j. The drive power source executes the dimming command. The total power on the busbar drops from time t_3 when the command is executed. The communication protocol can adopt a mature scheme such as RS232 or a custom scheme.



(**a**) (**b**)

Figure 4. Networked control LED system based on DC grid PLC: (**a**) system architecture diagram; (**b**) system key waveforms.

2.3. Working Principle of Bus Converter Based on Variable Modal Control

The key device for system energy and information modulation is the AC/DC bus converter. Figure 5a,b shows a schematic diagram and the corresponding buck and boost working modes. The circuit is divided into two stages. The first stage is a power factor correction (PFC) circuit to achieve a high power factor. The output is a fixed DC voltage V_g as the input of the second stage.

The second stage is a half-bridge circuit, the output is a DC bus, and the DC bus is connected to several LED driving power sources. The LED driving power can be regarded as the active load of the second-stage half-bridge circuit, and the total equivalent power is p_{LED}. D_1 and D_2 are body diodes of the half-bridge circuit MOSFETs M_1 and M_2, respectively. The control circuit has a single-chip microcomputer (MCU), which samples the output voltage v_{bus} through the sampling resistors R_1 and R_2, and $R_{Boostcs}$ and R_{Buckcs} are sampling resistors, respectively sampling the inductor currents in boost and buck modes.

In different situations, the half-bridge circuit operates in buck mode or boost mode. Figure 5c shows the main waveforms of these two modes.

t_0–t_1: The AC/DC bus converter does not send a signal to the LED driver, and its output voltage is constant DC 48 V. The upper tube M_1 is operated as a high-frequency switch, the lower tube M_2 is stopped, the half-bridge circuit operates in buck mode as shown in Figure 5a, and the body diode

D_2 of the M_2 acts as a freewheeling diode of the buck circuit. The bus converter charges capacitor C_2, which supplies energy to the distributed LED driver.

t_1–t_{11}: The bus converter receives the command and modulates it into the bus voltage v_{bus}, causing it to change to high and low DC levels. Defining the signal S_{in} passed, when S_{in} is logic 0, the bus converter operates in boost mode, and when S_{in} is logic 1, the bus converter operates in buck mode. When in boost mode, the upper tube M_1 stops working, and M_2 operates as a high-frequency switch. The body diode D_1 of the M_1 operates as a freewheeling diode of the boost circuit, as shown in Figure 5b. At this time, the energy on the bus voltage v_{bus} across the output capacitor C_2 is quickly transferred to the half-bridge input capacitor C_1, and the level rapidly drops to zero. Since the LED driving power supply in Figure 4a has diodes D_{pj} and D_{sj}, the change in bus voltage does not affect the energy and signal demodulating circuits in the LED driving power supply.

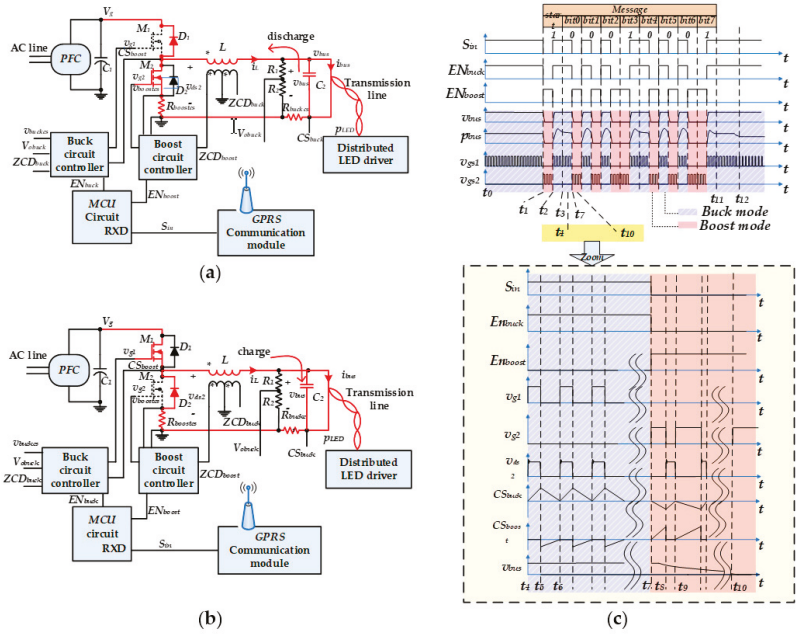


Figure 5. Work principles of bus converter: (**a**) circuit principle of buck mode; (**b**) circuit principle of boost mode; (**c**) working waveform.

The half-bridge circuit adopts different working modes, so that in buck mode, the bus voltage v_{bus} across capacitor C_2 can rise rapidly; in boost mode, the bus voltage v_{bus} across capacitor C_2 can be quickly reduced. There are three advantages to using this method of variable mode control:

(1) The bus voltage v_{bus} changes rapidly, which is beneficial to improve the signal transmission speed and facilitate the operation of the signal demodulation circuit in the LED driver.

(2) If there is no boost mode, the bus converter should make the busbar low voltage and can only rely on the load to discharge naturally. However, in the case of light load of the bus converter, especially when the load is turned off, when the bus converter is equivalent to no-load, the DC bus voltage v_{bus} drops to 0, which takes a long time, and the energy storage of the LED driving power capacitor C_{pj} may not last so long. Boost mode allows the bus to quickly go low under light load conditions.

(3) Since boost mode feeds back the energy of output capacitor C_2 to input capacitor C_1, it can be used again next time, so the energy utilization efficiency in the communication process is higher.

t_{12}–: After the drive power supply executes the dimming command, the total p_{bus} power on the bus is reduced.

As shown in Figure 5a,b, it is divided into two modes, buck and boost. Due to the poor reverse recovery performance of the body diode of the MOSFET, the circuit uses boundary current mode (BCM) regardless of buck or boost mode. The control circuits of both modes are controlled by ST L6562. In buck mode, M_2 is always off and its body diode D_2 operates as a freewheeling diode of the buck circuit. In the main circuit, the signal ZCD_{Buck} that controls M1 turn-on, the peak current signal CS_{Buck} that controls M1 turn-off, and the output voltage signal V_{oBuck} are sampled into the buck circuit controller. In boost mode, M_1 is always off, and its body diode D_1 acts as a freewheeling diode of the boost circuit. In the main circuit, the signal ZCD_{Boost} that controls M_2 turn-on and the peak current signal CS_{Boost} that controls M_2 turn-off are sampled into the boost control circuit.

In the t_4–t_{10} time of Figure 5c, the specific working waveforms of the two working modes are given. At time t_4, the transmitted signal S_{in} is still high, EN_{Buck} is high, and EN_{Boost} is low, indicating that the circuit is in buck mode, M1 is operational, M_2 is disabled, and its drive signal V_{g2} is always low. The body diode D_2 of M_2 operates as a freewheeling diode of the buck circuit. The energy flow of the circuit flows from capacitor C_1 to C_2, as shown in Figure 5a.

$$v_g - v_{bus} = L\frac{i_{Lpk}}{t_5 - t_4} \tag{1}$$

where i_{Lpk} is the peak value of the inductor current during this period.

t_5–t_6: M_1 is turned off, the inductor current drops, the body diode D_2 of M_2 continues to flow, CS_{Boost} is negative voltage, and the half-bridge midpoint voltage V_{ds2} is low. The voltage and current in the circuit satisfy Equation (2), and the circuit gain relationship still satisfies the law of the buck circuit, as in Equation (3).

$$v_{bus} = L\frac{i_{Lpk}}{t_6 - t_5} \tag{2}$$

$$v_{bus} = \frac{t_5 - t_4}{t_6 - t_4} \cdot v_g \tag{3}$$

t_6–t_7: The circuit repeats the working process of the t_4–t_6 switching cycle until time t_7, the transmission signal S_{in} becomes low level, EN_{Buck} is low, and EN_{Boost} is high, indicating that the circuit is in boost mode; M_2 can work, M_1 is disabled, and its drive signal V_{g1} is always low. The body diode D_1 of M_1 operates as a freewheeling diode of the boost circuit. The energy flow of the circuit flows as shown in Figure 5b from capacitor C_2 to C_1.

t_7–t_8: M_2 is turned on, the inductor current rises in the reverse direction, CS_{Buck} is negative voltage, and the half-bridge midpoint voltage V_{ds2} is low. The voltage and current in the circuit satisfy the law of the general boost circuit, as shown in Equation (4).

$$v_{bus} = L\frac{-i_{Lpk}}{t_8 - t_7} \tag{4}$$

t_8–t_9: M_2 is turned off, the inductor current drops, the body diode D_1 of M_1 continues to flow, CS_{Buck} is negative voltage, and the half-bridge midpoint voltage V_{ds2} is high. The voltage and current in the circuit satisfy Equation (5), and the circuit gain relationship still satisfies the law of the boost circuit, as in Equation (6).

$$v_g - v_{bus} = L\frac{-i_{Lpk}}{t_9 - t_8} \tag{5}$$

$$v_g = \frac{t_9 - t_7}{t_9 - t_8} \cdot v_{bus} \tag{6}$$

t_9–t_{10}: The circuit repeats the working process of the t_7–t_9 switching cycle until t_{10}, because the voltage on C_2 is already very low, meaning that most of the energy on C_2 is fed back to C_1.

The working principle of the bus converter described above is that the modal control of the circuit realizes the transformation of the high and low levels on capacitor C_2 to achieve the purpose of simultaneously transmitting energy and information.

2.4. Distributed LED Drive Power DC/DC Converter Working Principle

The distributed LED drive power directly drives the light source and demodulates the communication information from the DC bus. The driving power source is divided into an energy demodulating circuit, an information demodulating circuit, and a DC/DC converter. The principles of the first two have already been introduced. Here, the working principle of the DC/DC converter is introduced.

In theory, there are many solutions for implementing the DC/DC converter of the driving power supply. This paper introduces the principle of demodulation energy and information by taking the buck circuit as an example. Figure 6 shows the schematic and key waveforms of the DC/DC converter in the distributed drive power supply of Figure 4a.

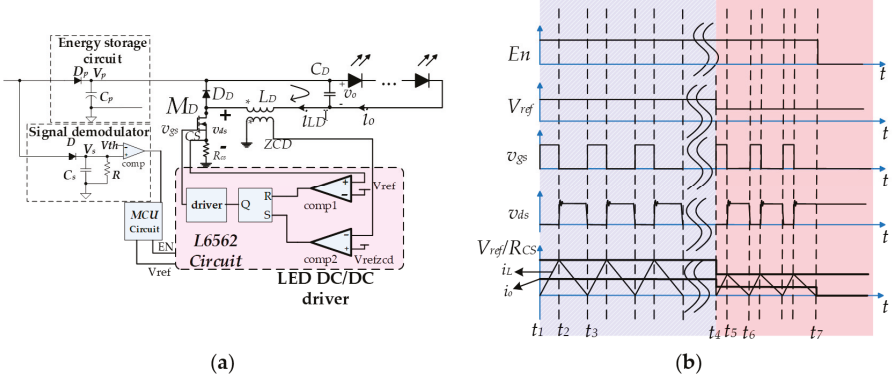


Figure 6. Principle of distributed drive power DC/DC converter: (**a**) schematic diagram; (**b**) key waveform.

The DC/DC converter uses a buck circuit and operates in a critical mode. Due to the critical mode, the output current i_o and the peak value i_{LDpk} of the inductor current i_{LD} satisfy the following relationship:

$$i_o = \frac{1}{2} i_{LDpk} \tag{7}$$

According to Equation (7), the output current i_o can be made constant by controlling i_{LDpk} to be constant. The control circuit is implemented by chip L6562. The specific working process is as follows:

t_1–t_2: The enable signal EN given by the microcontroller allows the DC/DC converter to operate. The MOSFET MD is turned on and the inductor current rises. The voltage and current in the circuit meet the following equation:

$$V_p - v_o = \frac{L_d \cdot i_{LDpk}}{t_2 - t_1} \tag{8}$$

t_2–t_3: At time t_2, the voltage on the sampling resistor R_{CS} reaches the threshold value V_{ref} of comparator comp1, comp1 gives a positive level, and the output level of the RS flip-flop becomes low, so that the M_D is turned off. At this time, the diode D_D starts freewheeling, and the inductor current decreases. At time t_3, since the inductor current drops to zero, the Z_{CD} voltage drops, and the comparator comp2 output is high, causing the RS flip-flop output to be high, and the drive circuit starts driving the M_D to conduct and begins to enter the next switching cycle. During this period, the voltage and current in the circuit satisfy Equation (9), and the circuit gain relationship still satisfies the law of the buck circuit, as in Equation (10).

$$v_o = \frac{L_d \cdot i_{LDpk}}{t_3 - t_2} \tag{9}$$

$$v_o = \frac{t_2 - t_1}{t_3 - t_1} \cdot V_p \tag{10}$$

The t_3–t_4 circuit repeats the switching cycle state of t_1–t_3. It should be pointed out that V_{ref} is given by the single-chip circuit and V_{ref} changes, according to Equation (7); the output current also changes.

t_4–t_7: The single-chip circuit receives the dimming command from the bus converter, reduces the V_{ref} voltage, and reduces the output current i_o of the DC/DC converter.

t_7: The single-chip circuit receives the shutdown command from the bus converter, turns the enable signal EN to low, the DC/DC converter stops working, and the output current is zero.

Through the working principles described above, the distributed LED driving power supply can drive the LED load according to the command sent by the bus converter.

3. Experimental Verification

The principles of system operation were introduced in the previous section, and the working process of the bus converter and distributed LED driver power supply is analyzed in detail. In order to verify the technology mentioned in this section, this paper establishes a verification system as shown in Figure 4a. The physical diagram is shown in Figure 7. System parameters are shown in Table 2.

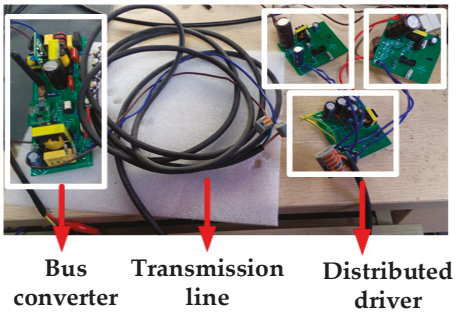


Figure 7. Picture of demo system.

Table 2. System key parameters.

Bus Converter	Quantity	1
	Input voltage	220 V/50 Hz
	PFC voltage	400 V
	Output voltage maximum	48 V
	Total power maximum	30 W
	Communication baud rate	9600
Distributed LED Driver	Quantity	3
	Single rated power	10 W
	Single load structure	3 W LED 3 series 3 parallel
	Single load rated current	700 mA

3.1. Bus Converter Working Principle Verification

The main task of the bus converter is to convert the AC mains into the bus of the DC grid. During the transition, the DC grid output voltage is modulated into a signal that is communicated to the distributed LED drive power source, allowing both signal and energy to be delivered simultaneously. This experiment mainly verifies this function.

Figure 8 shows the input and output waveforms of the bus converter. It can be seen that under the 220 V AC mains, the bus converter converts it into a 48 V DC bus v_{bus}. After the communication signal S_{in} is modulated into the v_{bus}, the S_{in} changes, and the v_{bus} also changes in the same waveform to achieve simultaneous transmission of energy and information. Due to the presence of the PFC circuit, the power factor is approximately 1, and the input voltage and current waveforms are approximately the same.

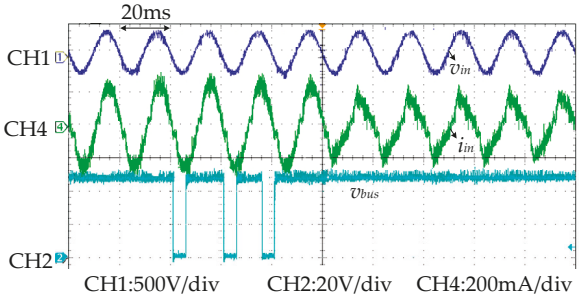


Figure 8. Input and output waveforms of bus converter.

According to the above description, when the DC bus voltage v_{bus} is high, the bus converter is in buck mode, and the output v_{bus} is high. When v_{bus} is low, in order to quickly reduce the voltage of the bus converter output capacitor C_2, the bus converter goes into boost mode, so that the C_2 energy is quickly transferred to the bus converter input capacitor C_1 for continued use in the next cycle. Figure 9 shows the main waveforms of the modal transformation. The pass signal S_{in} is the same as the enable signal of buck mode. It can be seen from the waveform that in steady state, the bus converter operates in buck mode, the signal S_{in} is high, the drive V_{g1} of the upper tube M_1 is working, the drive V_{g2} of the lower tube M_2 is low, and the output voltage v_o is constantly 48 V. When the bus converter receives the command, it modulates the signal S_{in} into the output bus, causing it to become a square wave with the same high and low conversion as S_{in}. At this time, buck and boost modes of the bus converter are switched according to the transmission signal.

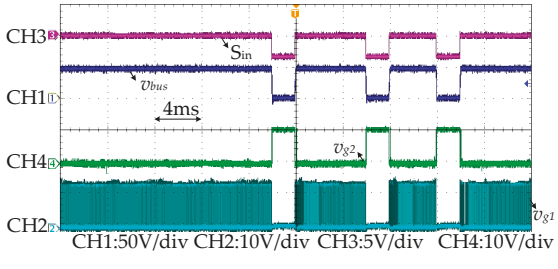


Figure 9. Main waveforms of bus converter during steady state and communication.

The output transformer of the bus converter is continuously charged and discharged during the signal modulation process. It is essentially the energy flow relationship between the input capacitance C_1 of the bus converter and the output capacitor C_2. Figure 10 shows the experimental relationship of energy flow. It can be seen from Figure 10 that in buck mode, the buck sampling resistor voltage v_{Buckcs} is positive, the boost sampling resistor voltage $v_{Boostcs}$ is negative, and the bus converter output capacitor C_2 is charged. In boost mode, the buck sampling resistor voltage v_{Buckcs} is negative, the boost sampling resistor voltage $v_{Boostcs}$ is positive, and the bus converter output capacitor C_2 energy is transferred to the input capacitor C_1.

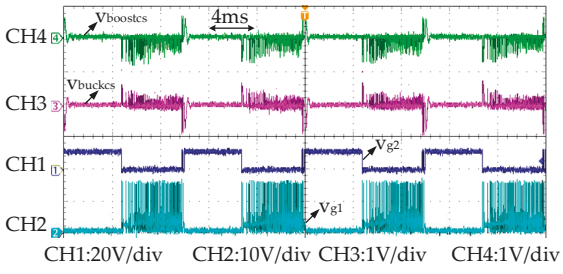


Figure 10. Energy flow relationship in the process of bus converter modal transformation.

As mentioned above, since the bus converter needs to use a body diode of a MOSFET of half-bridge topology as a freewheeling tube in either buck or boost mode, the reverse recovery capability of the MOSFET body diode is poor, in order to reduce this. The effect is that the circuit uses a critical mode. Figure 11a,b shows the key waveforms of the bus converter in buck and boost mode during communication. In buck mode, the sampling resistor voltage v_{Buckcs} and the half-bridge midpoint voltage v_{ds2} are visible, and the circuit operates in a critical mode, avoiding the loss caused by the reverse recovery of the body diode D_2 of the lower tube M_2. In boost mode, the sampling resistor voltage $v_{boostcs}$ and the half-bridge midpoint voltage v_{ds2} are visible, and the circuit operates in a critical conduction mode, avoiding the loss caused by the reverse recovery of the body diode D_1 of the upper MOSFET M_1. This experiment verifies the working principle of the bus converter.

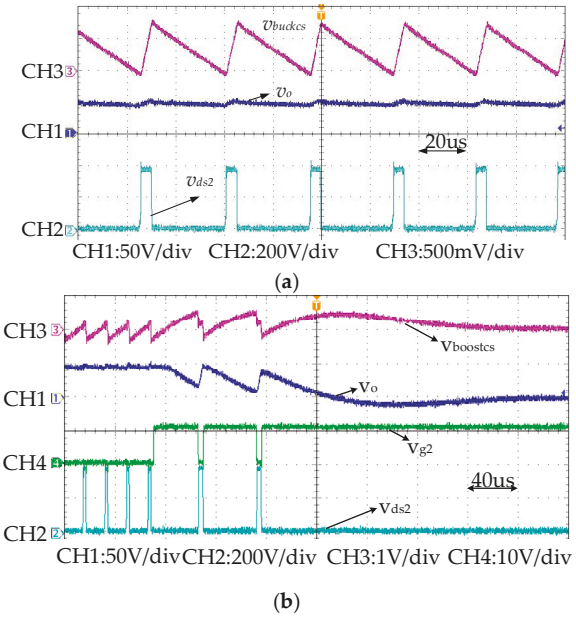


Figure 11. Critical conduction mode waveforms of the bus converter under (**a**) buck mode and (**b**) boost mode.

3.2. Distributed LED Driver Power Supply Working Principle Verification

The main task of the distributed LED drive power source is to receive the energy of the DC bus and demodulate the information. This experiment mainly verifies this function.

Figure 12 shows the main waveforms of the energy and information demodulation of the distributed LED driver power supply during communication. It can be seen from Figure 6 that when the enable signal EN is 1, the MOSFET M_D starts to work. As shown in Figure 12, v_{gs} is a high-low level transition of the driving signal of the MOSFET M_D, enabling the distributed LED driver to operate, so that the bus voltage v_{bus} is high level. At this time through the modulation and demodulation of the signal circuit, so that v_s is also high level, and in the energy circuit, v_p is also high level output. When the enable signal EN is 0, the MOSFET M_D stops working. At this time, the driving signal v_{gs} of M_D is kept low. At this time, in the signal circuit, v_s is also low, and in the energy circuit, due to the capacitance of C_p, as shown in the figure, is slightly dropped and can be maintained within the allowable ripple voltage range to keep the circuit working properly.

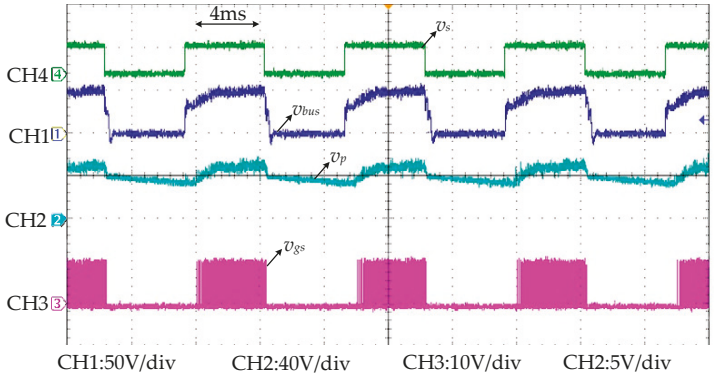


Figure 12. Distributed LED drive power energy and information.

In this section, the distributed LED driver power supply uses a critical conduction mode buck circuit, and the output current i_o is a constant current source. Figure 13 shows the operating waveform of the drive power supply. v_{cs} is the voltage of sampling resistance R_{cs}, R_{cs} is used to sample the current flowing through it. Figure 6a shows, when M_D is turned on, the current of inductor L_D flows through Rcs. v_{gs} is the drive signal of M_D, and v_{ds} is the voltage between drain and source of M_D. The circuit operates in a critical conduction mode, avoiding the loss caused by the reverse recovery of the body diode D_1 of the upper MOSFET M_1, and reducing circuit losses.

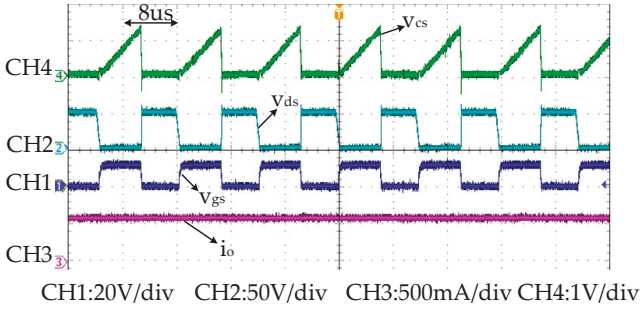


Figure 13. Critical conduction mode waveforms of distributed LED driver.

The LED driving power supply executes the command after demodulating the information on the DC bus. Figure 14 shows the waveform of the action performed after a drive power supply receives a light-off command. When the bus converter receives the command from the control center, it means to turn off the light, so that v_{bus} changes as shown in Figure 14, this signal represents the command

"LED off at a certain address". Through the modulation and demodulation of the circuit, the signal is passed through the signal conditioning circuit to the LED driver at an address as shown in Figure 6a, so that it performs the light-off action, as shown in the CS waveform, and finally becomes a low level.

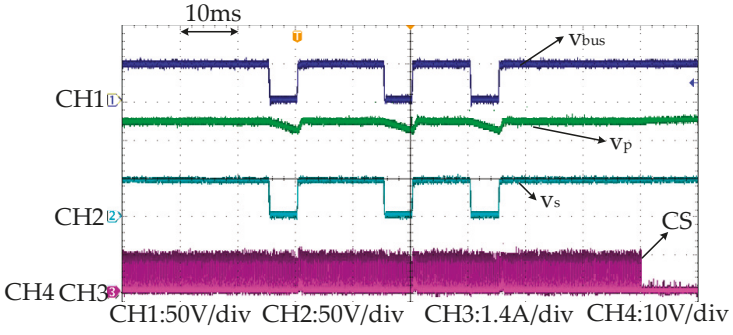


Figure 14. Execution command waveforms of distributed LED driver.

4. Conclusions

With common traditional lighting system remote control schemes like 0–10 V, PWM control, and DALI, two additional communication lines must be used, which brings installation inconvenience and costs more. Traditional PLC or wireless technologies do not need two communication lines. Although they are easy to install, they are not easy to popularize because of their high cost. A DC power grid based on the new power line carrier technology proposed in this paper enables the LED driving power source to have not only energy conversion capability, but also communication capability by using power electronics to realize communication technology. In order to realize the communication function of the driving power source, the proposed system includes a bus converter and a distributed driving power source. The bus converter modulates the information into the DC bus through variable modal control, from which the distributed drive power demodulates energy and information. In contrast with 0–10 V, PWM control, and DALI, this technology does not need communication lines, it is easier to install, and the cost is lower. Compared with the traditional PLC, its communication circuit is simpler, so the cost is lower. Compared with wireless technology, the radio frequency module can be omitted, so the cost is decreased and the installation is simpler. This technology not only simplifies the use of communication technology in application, but also reduces the difficulty of application. The prototype system validated the effectiveness of the technology. It is possible that this technology can also be used in other applications besides LED.

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Nomenclature

V_{bus}	DC bus voltage
i_{bus}	DC bus current
p_{bus}	DC bus input power
v_{pj}	Output capacitance voltage of the energy storage part in the *j*th LED DC/DC driver
C_{pj}	Output capacitance of the energy storage part in the *j*th LED DC/DC driver
v_{sj}	Output capacitance voltage of the signal demodulation part in the *j*th LED DC/DC driver
C_{sj}	Output capacitance of the signal demodulation part in the *j*th LED DC/DC driver
v_{thj}	Comparator reference of the signal demodulation part in the *j*th LED DC/DC driver
R_{sj}	C_{sj} Discharge resistance of the signal demodulation part in the *j*th LED DC/DC driver
S_o	The input signal from the signal demodulation part to MCU in the *j*th LED DC/DC driver
A_j	The address of the *j*th LED DC/DC driver
C_1	Input capacitance of the bus converter
C_2	Output capacitance of the bus converter
V_g	Output voltage of PFC in the bus converter
v_{g1}	Drive signal of the bridge's upper MOSFET in the bus converter
v_{g2}	Drive signal of the bridge's lower MOSFET in the bus converter
CS_{boost}	Peak current signal in Boost mode
CS_{buck}	Peak current signal in Buck mode
$R_{boostcs}$	Sampling resistance of Boost mode
R_{buckcs}	Sampling resistance of Buck mode
ZCD_{buck}	Control signal that M_1 is turn on
ZCD_{boost}	Control signal that M_2 is turn off
V_{obuck}	Feedback signal of sampling output voltage in Buck mode
i_L	Inductor current in the bus converter
R_1	Sampling resistor
R_2	Sampling resistor
S_{in}	Signal transmitted by the bus converter
V_{buckcs}	Voltage across the sampling resistor Rbuckcs in buck mode
$V_{boostcs}$	Voltage across the sampling resistor Rboostcs in boost mode
V_{ds2}	The midpoint voltage of bridge in the bus converter
EN_{buck}	Enable signal of Buck mode
EN_{boost}	Enable signal of Boost mode
i_o	Output current of the LED DC/DC driver
i_{LD}	The current of inductance L_D in the LED DC/DC driver
i_{LDpk}	The current peak of inductance L_D in the LED DC/DC driver
V_p	Output capacitance voltage of the energy storage part in the LED DC/DC driver
C_p	Output capacitance of the energy storage part in the LED DC/DC driver
V_s	Output capacitance voltage of the signal demodulation part in the LED DC/DC driver
C_s	Output capacitance of the signal demodulation part in the LED DC/DC driver
V_{th}	Comparator reference of the signal demodulation part in the LED DC/DC driver
R_s	Cs Discharge resistance of the signal demodulation part in the LED DC/DC driver
L_D	Inductance of the LED DC/DC driver
C_D	Output capacitor of the LED DC/DC driver
v_o	Output voltage of the LED DC/DC driver
R_{cs}	Sampling resistance of the LED DC/DC driver
EN	Enable signal of L6562 in the LED DC/DC driver
V_{ref}	Comparator reference of L6562's comp1 in the LED DC/DC driver
V_{refzcd}	Comparator reference of L6562's comp2 in the LED DC/DC driver
V_{ds}	Voltage between drain and source of M_D

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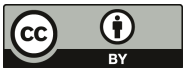

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High Efficiency Solar Power Generation with Improved Discontinuous Pulse Width Modulation (DPWM) Overmodulation Algorithms

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Abstract: The efficiency of a photovoltaic (PV) system strongly depends on the transformation process from solar energy to electricity, where maximum power point tracking (MPPT) is widely regarded as a promising technology to harvest solar energy in the first step. Furthermore, inverters are an essential part of solar power generation systems. Their performance dictates the power yield, system costs and reliable operation. This paper proposes a novel control technology combining discontinuous pulse width modulation (DPWM) and overmodulation technology to better utilize direct current (DC) electrical power and to reduce the switching losses in the electronic power devices in conversion. In order to optimize the performance of the PV inverter, the overmodulation region is refined from conventional two-level space vector pulse width modulation (SVPWM) control technology. Then, the turn-on and turn-off times of the switching devices in different modulation areas are deduced analytically. A new DPWM algorithm is proposed to achieve the full region control. An experimental platform based on a digital signal processing (DSP) controller is developed for validation purposes, after maximum power is achieved via a DC/DC converter under MPPT operation. Experimental results on a PV system show that the DPWM control algorithm lowers the harmonic distortion of the output voltage and current, as well as the switching losses. Moreover, better utilization of the DC-link voltage also improves the PV inverter performance. The developed algorithm may also be applied to other applications utilizing grid-tie power inverters.

Keywords: DPWM; MPPT; photovoltaic power system

1. Introduction

Currently, there is great concern about global warming due to the rapid depletion of fossil fuels [1]. Thus, the utilization of renewable energy has received increasing attention in industry and research communities. Solar energy is one of the most promising renewable energy sources in the world, and photovoltaic (PV) power generation systems are a growing area for research and development [2].

Conventionally, the efficiency of direct-coupled PV systems could be very low due to the high dependence on the irradiance and temperature conditions. This can be overcome by continuously tracking the maximum power point (MPP) of the system at varied conditions of irradiance and temperature [3–5]. This method is known as maximum power point tracking (MPPT). In order to

realize MPPT, DC/DC converters are commonly used in the PV power system. Moreover, the PV modules are usually connected in series to raise the output direct current (DC) voltage and, in parallel, to increase the output power. However, this will lead to a multi-peak effect, which poses a challenge to maintain the equal terminal voltage across PV modules.

On the other hand, inverters are a key component in solar photovoltaic systems, and their performance determines the power yield, system costs and reliable operation [6–8]. Most PV inverters adopt a two-level control technique based on the space vector pulse width modulation (SVPWM). The multi-peak effect potentially increases the switching losses in the power switching devices [9–12]. In order to reduce this effect, a synchronous pulse width modulation (PWM) method is often utilized in cascaded inverters [13]. When the DC voltage is low, an overmodulation control mode is adopted for the two inverters. Therefore, a T-type three-level overmodulation strategy is developed [14–16]. By doing so, PV inverters can still achieve maximum power point tracking (MPPT) which can prolong the running time of PV inverters and improve the output power. However, these technologies increase the complexity and the cost of photovoltaic power generation systems, as well as the switching losses and total harmonic distortion (THD) of the PV systems [17–20].

In this paper, a new discontinuous pulse width modulation (DPWM) scheme is proposed to achieve optimal control of PV inverters along with MPPT in a boost DC/DC converter. It combines DPWM and overmodulation to reduce device conducting periods, based on two-level SVPWM control technology [21]. As a result, the device power losses are reduced effectively. Moreover, the overmodulation segment control method can also reduce the harmonic distortion of the output voltage and improve the DC-link voltage utilization. Thereby, the overall system efficiency will be increased.

The contents are organized as follows: An equivalent circuit of a PV power system under an MPPT scheme is presented in Section 2, followed by the introduction of a DPWM overmodulation algorithm in Section 3. Section 4 demonstrates both simulation and experimental results in detail. The key findings are summarized in Section 5.

2. Equivalent Circuit of a PV Power System

Figure 1 shows the structure of a typical photovoltaic system. The MPPT control of PV panels is achieved by a DC/DC converter, which can also maintain the voltage stability of the DC bus. The PV inverter (DC/AC converter) can achieve the active/reactive power control.

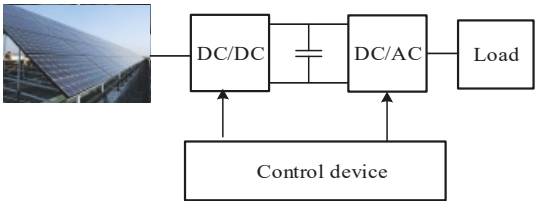


Figure 1. Structure of the photovoltaic (PV) power.

2.1. Perturbation and Observation (P&O) MPPT Algorithm

Conventionally, MPPT is embedded in a converter to determine the duty cycle that maximizes the PV power yield [22]. A perturbation and observation method (P&O) is used to find the maximum power point [23] by altering the array terminal voltage and then comparing the PV output power with its previous value. If the power increases while voltage increases, the PV array is operating in the correct direction; otherwise, the operational point should be adjusted to its the opposite direction [24,25]. The main advantage of P&O lies in its simplicity. This method shows its effectiveness, provided that solar irradiation does not change very quickly. As shown in Figure 2, there are four operational points,

A, B, C and D. From point A to point B, the PV power increases while the voltage of point B is higher than that of point A. Therefore, the next perturbation voltage keeps increasing, or vice versa. If the operation starts from point C to D, PV power decreases while the voltage of point C is higher than the voltage of point D. The next operation should be changed to the opposite direction. Therefore, the next perturbation reduces the voltage so as to redirect the trajectory towards the maximum power point. Accordingly, four scenarios are summarized in Table 1.

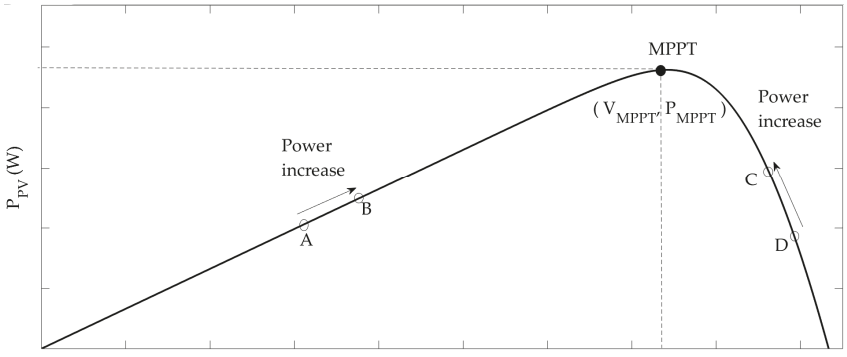


Figure 2. Maximum power point tracking (MPPT) from different trajectories.

Table 1. Trajectory analysis with perturbation and observation (P&O) MPPT.

No.	Scenario	Example Route	Action
1	$P_{current} > P_{previous}$ & $V_{current} > V_{previous}$	A → B	Increase voltage
2	$P_{current} > P_{previous}$ & $V_{current} < V_{previous}$	D → C	Decrease voltage
3	$P_{current} < P_{previous}$ & $V_{current} > V_{previous}$	C → D	Decrease voltage
4	$P_{current} < P_{previous}$ & $V_{current} < V_{previous}$	B → A	Increase voltage

A boost DC/DC converter is adopted to adjust the terminal voltage by regulating the duty ratio *D*. It will therefore incur the change of the equivalent power output which in turn realizes the maximum power output of a PV array. A flowchart of the P&O method is shown in Figure 3.

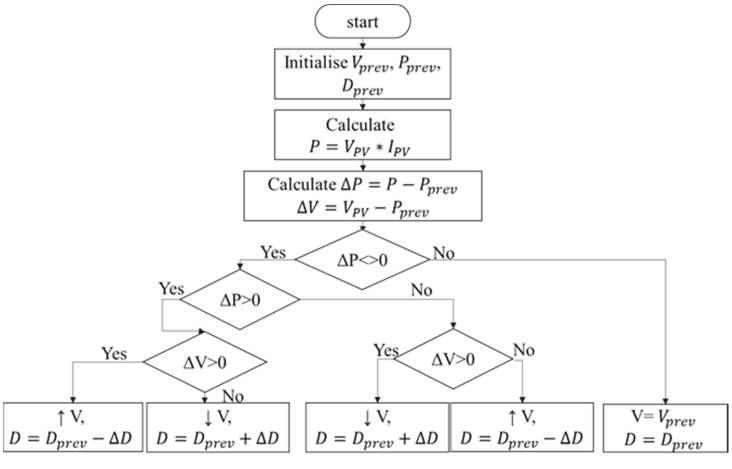


Figure 3. Flowchart of the P&O method for MPPT.

2.2. A Boost DC-DC Converter and the Equivalent Circuit

In this study, a boost converter is adopted to operate the voltage via changing D. A boost converter is expected to connect with the output of PV arrays to produce the equivalent output voltage equal to the voltage V_{mpp} at the maximum power point, with equivalent resistance equal to R_{mpp} with the current I_{mpp} over the output circuit, as shown in Figure 4. Selecting a proper DC-DC converter with reasonable circuit parameters is essential.

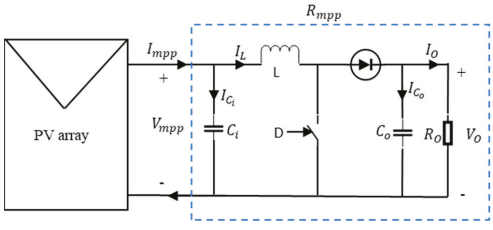


Figure 4. Equivalent circuit including a PV array and a boost DC-DC converter.

To design a boost converter for a PV system, key elements in the selection include the inductance of an inductor L', the capacitance of an input capacitor C_i, the input resistance R_{mpp}, capacitance of an input capacitor C_i, and the load resistance R_O. The purpose of this boost converter is to realize the equivalent circuit resistance to R_{mpp}. Therefore, the maximum output power under the current condition can be produced via this boost converter from a PV array.

The maximum power point resistance R_{mpp} is calculated based on the maximum power point voltage V_{mpp} and the maximum power point current I_{mpp} by using a simple calculation in Equation (1). R_O can be calculated by Equation (2). The duty ratio D can be derived from Equation (3). Assuming there is no power loss in circuit, an energy balance equation can be established (Equation (4)).

$$R_{mpp} = \frac{V_{mpp}}{I_{mpp}} \tag{1}$$

$$R_O = \frac{R_{mpp}}{(1-D)^2} \tag{2}$$

$$\text{Or} \qquad D = 1 - \sqrt{\frac{R_{mpp}}{R_O}} \tag{3}$$

$$p_{mpp} = \frac{V_{mpp}^2}{R_{mpp}} = \frac{V_O^2}{R_O} \tag{4}$$

$$\text{Or} \qquad \frac{V_{mpp}^2}{V_O^2} = \frac{R_{mpp}}{R_O} \tag{5}$$

Equation (5) presents the relationship between resistance and voltage. The output voltage is calculated from Equation (5) to Equation (6).

$$V_O = V_{mpp}\sqrt{\frac{R_O}{R_{mpp}}} \tag{6}$$

The inductance can be estimated by many methods [26,27]. A general calculation is given by Equation (7).

$$L' = \frac{V_{mpp} \cdot D}{I_{mpp} \cdot \gamma_{IL} \cdot f} \tag{7}$$

where f and γ_{IL} refer to the switching frequency and the inductor current ripple factor.

Input capacitor C_i can be calculated according to Equation (8).

$$C_i = \frac{D}{8 \cdot L \cdot \gamma_{Vmpp} \cdot f^2} \tag{8}$$

Output capacitor C_O can be calculated according to Equation (9) [28].

$$C_O = \frac{D}{R_O \cdot \gamma_{VO} \cdot f} \tag{9}$$

where the current ripple factor γ_{IL} and the voltage ripple factors γ_{Vmpp}, γ_{VO} are refined within 5%.

2.3. Division of the Overmodulation Area

Figure 5 presents the main circuit topology of the three-phase grid-tie inverter, where U_d is the DC-link voltage, i_a, i_b, and i_c are the inverter output currents, L is the filter inductance, and R is the filter inductance equivalent series resistance, respectively.

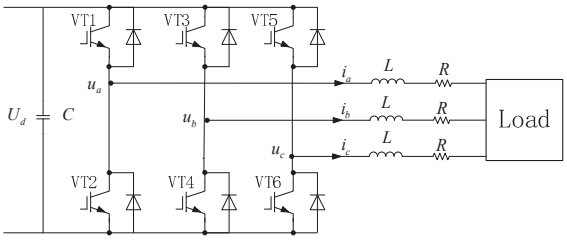


Figure 5. Topology of the three-phase grid-tie inverter.

In the inverter, the on-state of the upper arm switches and the off-state of the lower arm switches are defined as "1"; otherwise, they are "0". Therefore, the three bridge arms of the inverter have eight switch states, corresponding to eight basic voltage space vectors: u_0(000), u_1(100), u_2(110), u_3(010), u_4(011), u_5(001), u_6(101) and u_7(111). The SVPWM modulation voltage vector and the sector distribution of the PV inverter are demonstrated in Figure 6. The amplitude of u_1~u_6 is $\frac{2}{3}U_d$, and the phase angles of u_1~u_6 differ by 60°.

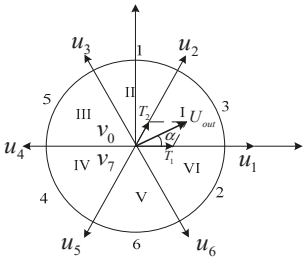


Figure 6. Space voltage vectors and sector distribution.

According to the volt-second balance principle:

$$U_{out} \cdot T_s = u_1 \cdot T_1 + u_2 \cdot T_2 \tag{10}$$

where U_{out} is the given output voltage vector, T_1 is the action time for u_1, T_2 is the action time for u_2, and T_s is the switching period.

The output space rotating vector with a constant rotating speed and a constant amplitude is achieved by the vector addition of adjacent vectors. The output range is in the inscribed circle of the regular hexagon constituted by the vectors $u_1 \sim u_6$, which are also known as the linear modulation areas. The maximum amplitude of the output phase voltage is given by:

$$u_{m\_line} = \frac{2 \cdot U_d}{3} \cdot \cos 30^\circ = \frac{U_d}{\sqrt{3}} \tag{11}$$

If the PV inverter is controlled by the six-step wave mode outside of the linear modulation area, the amplitude of the phase voltage can be obtained [29].

$$u_{m\_max} = \frac{2 \cdot U_d}{\pi} \tag{12}$$

The region from outside the linear modulation area to the six-step maximum output voltage area is called the overmodulation area. The modulation coefficient m is defined as:

$$m = \frac{\pi \cdot U_{out}}{2 \cdot U_d} \tag{13}$$

There are three different regions as per the modulation coefficient. In the linear modulation area, $m < 0.907$; in the overmodulation area I, $0.907 < m < 0.952$; in the overmodulation area II, $0.952 < m < 1$. Figure 7 shows the trajectory of the synthesized voltage vector in the overmodulation areas. The simplified formulas for overmodulation areas I and II are given by [30–33].

$$\alpha_r = \frac{\pi}{6} - \arccos\left(\frac{U_d}{\sqrt{3} \cdot U_{out}}\right) \tag{14}$$

$$\begin{cases} \alpha_h = 6.40 \cdot m - 6.09 & (0.952 \le m < 0.9800) \\ \alpha_h = 11.57 \cdot m - 11.34 & (0.9800 \le m < 0.9975) \\ \alpha_h = 48.96 \cdot m - 48.43 & (0.9975 \le m < 1) \end{cases} \tag{15}$$

Take sector I for example. In overmodulation area I, the rotational speed of the output voltage vector remains constant and the amplitude is limited by the hexagon. The vertex of the trajectory follows the thick solid line of ABCD. In overmodulation area II, the rotation speed of the output voltage vector changes and the amplitude is limited. When $\alpha < \alpha_h$, the output voltage vector is u_1. When $\alpha_h \le \alpha < \frac{\pi}{3} - \alpha_h$, the trajectory of the output voltage vector is the BC solid line. When $\alpha \ge \frac{\pi}{3} - \alpha_h$, the output voltage vector is u_2. When $\alpha_h = \frac{\pi}{6}$, the output voltage vector traces at the vertex of the regular hexagon, and the modulation coefficient is the maximum ($m = 1$). The remaining sectors are the same.

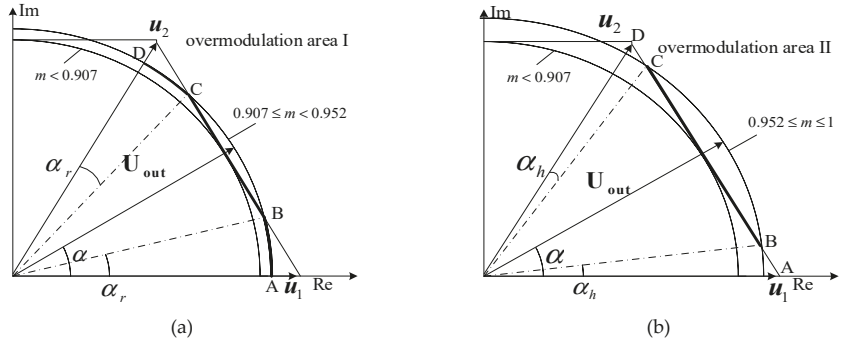


Figure 7. Synthesized voltage vector locus. (**a**) Overmodulation area I; (**b**) Overmodulation area II.

2.4. Full Modulation Region Voltage Vector

The key to controlling the voltage vector in the full modulation area is to determine the action time of the voltage vector according to the modulation coefficient m.

Take sector I for example again: U_{out} is synthesized by two basic voltage space vectors u_1(100) and u_2(110) and it is known that $u_1 = \frac{2}{3}U_d$, $u_2 = \frac{2}{3}U_d \cdot e^{j\frac{\pi}{3}}$. According to the sine theorem:

$$\frac{U_{out}}{\sin\frac{2\pi}{3}} = \frac{u_1 \cdot \frac{T_1}{T_s}}{\sin\left(\frac{\pi}{3} - \alpha\right)} = \frac{u_2 \cdot \frac{T_2}{T_s}}{\sin(\alpha)} \tag{16}$$

The action time T_1 and T_2 can be further calculated. When $T_1 + T_2 < T_s$, the zero vector u_0(000) or u_7(111) is used to fill the remaining time T_0.

(1) SVPWM linear modulation area ($m < 0.907$)

It can be obtained from Equation (16):

$$\begin{cases} T_1 = \sqrt{3} \cdot T_s \cdot \frac{U_{out}}{U_d} \cdot \sin\left(\frac{\pi}{3} - \alpha\right) \\ T_2 = \sqrt{3} \cdot T_s \cdot \frac{U_{out}}{U_d} \cdot \sin(\alpha) \\ T_0 = T_s - T_1 - T_2 \end{cases} \tag{17}$$

(2) Overmodulation area I ($0.907 \le m < 0.952$)

(i) When $0 \le \alpha \le \alpha_\gamma$ or $\frac{\pi}{3} - \alpha_\gamma \le \alpha \le \frac{\pi}{3}$, T_1, T_2 and T_0 are calculated in the same way as Equation (17).

(ii) When $\alpha_\gamma \le \alpha < \frac{\pi}{3} - \alpha_\gamma$,

$$\begin{cases} T_1 = T_s \cdot \frac{\sin\left(\frac{\pi}{3} - \alpha\right)}{\sin\left(\frac{\pi}{3} + \alpha\right)} \\ T_2 = T_s \cdot \frac{\sin(\alpha)}{\sin\left(\frac{\pi}{3} + \alpha\right)} \\ T_0 = 0 \end{cases} \tag{18}$$

(3) Overmodulation area II ($0.952 \le m < 1$)

(i) When $0 \le \alpha < \alpha_h$,

$$T_1 = T_s,\ T_2 = 0,\ T_0 = 0 \tag{19}$$

(ii) When $\alpha_h \le \alpha < \frac{\pi}{3} - \alpha_h$,

$$\gamma = \frac{\pi}{6} \cdot \frac{(\alpha - \alpha_h)}{\left(\frac{\pi}{6} - \alpha_h\right)}$$

$$\begin{cases} T_1 = T_s \cdot \frac{\sin\left(\frac{\pi}{3} - \gamma\right)}{\sin\left(\frac{\pi}{3} + \gamma\right)} \\ T_2 = T_s \cdot \frac{\sin\gamma}{\sin\left(\frac{\pi}{3} + \gamma\right)} \\ T_0 = 0 \end{cases} \tag{20}$$

(iii) When $\frac{\pi}{3} - \alpha_h \le \alpha < \frac{\pi}{3}$,

$$T_1 = 0,\ T_2 = T_s,\ T_0 = 0 \tag{21}$$

3. DPWM Overmodulation Algorithm

In traditional SVPWM modulation algorithms, A, B, and C from the given voltage vector U_{out} are calculated from the $\alpha - \beta$ coordinate plane.

$$\begin{cases} A = U_\beta \\ B = U_\alpha \cdot \sin 60^\circ - U_\beta \cdot \cos 60^\circ \\ C = -U_\alpha \cdot \sin 60^\circ - U_\beta \cdot \cos 60^\circ \end{cases} \tag{22}$$

where U_α and U_β are the α, β components of U_{out} in the $\alpha-\beta$ coordinate plane, respectively. S is defined as:

$$S = \text{sign}(A) + 2\cdot\text{sign}(B) + 4\cdot\text{sign}(C) \tag{23}$$

Thus, the relationship between sectors N and S can be obtained, as shown in Table 2.

Table 2. Relationship between S and N.

S	1	2	3	4	5	6
Sector N	II	VI	I	IV	III	V

As for the DPWM scheme, the switches are controlled only by the zero vector u_0 or u_7 in a triangular carrier cycle, as shown in Figure 8. u_7 is selected in the 60° range centred around the basic vectors u_1, u_3 and u_5, while u_0 is selected in other sectors. The DPWM sector number and its action conditions are tabulated in Table 3. There are twelve 30° sectors in the DPWM, as compared to six sectors in conventional SVPWM.

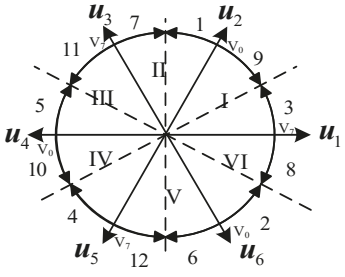


Figure 8. The sector distribution of the discontinuous width pulse modulation (DPWM).

Table 3. DPWM sector number and its action conditions.

Action condition	Sector N	S for the 30°	Sector
$\frac{U_\beta}{U_\alpha} < \tan\left(\frac{\pi}{6}\right)$	I	3 (True)	9 (False)
	IV	10 (True)	4 (False)
$U_\alpha > 0$	II	1 (True)	7 (False)
	V	6 (True)	12 (False)
$\frac{U_\beta}{U_\alpha} < -\tan\left(\frac{\pi}{6}\right)$	III	11 (True)	5 (False)
	VI	2 (True)	8 (False)

As for the DPWM modulation, the power devices switch four times in one sector because only u_0 or u_7 is used as the zero vector in one sector. Meanwhile, for the SVPWM modulation, the power devices switch six times in one sector because the vectors u_0 and u_7 are simultaneously applied (each action time is $T_0/2$).

Therefore, the switching frequency of the power devices in the DPWM modulation is reduced by one-third compared to the SVPWM modulation, and the switching sequence of the first sector is shown in Figure 9. According to the literature [34], the switching losses of the inverter power device include turn-on loss P_{on} and turn-off loss P_{off}:

$$P_{on} = \frac{1}{8}\cdot U_d\cdot t_{rN}\cdot\frac{I_{CM}^2}{I_{CN}}\cdot f_s \tag{24}$$

$$P_{off} = U_d \cdot I_{CM} \cdot t_{fN} \cdot f_s \cdot \left(\frac{1}{3\pi} + \frac{1}{24} \cdot \frac{I_{CM}}{I_{CN}} \right) \tag{25}$$

where t_{rN} and t_{fN} are the turn-on time and turn-off time, respectively; f_s is the switching frequency of power devices; I_{CN} is the forward current of IGBT; I_{CM} is the amplitude of the sinusoidal current.

Switching losses are proportional to f_s according to Equations (26) and (27), so the switching losses of the DPWM modulation can be reduced by one-third compared to the switching losses of the SVPWM modulation.

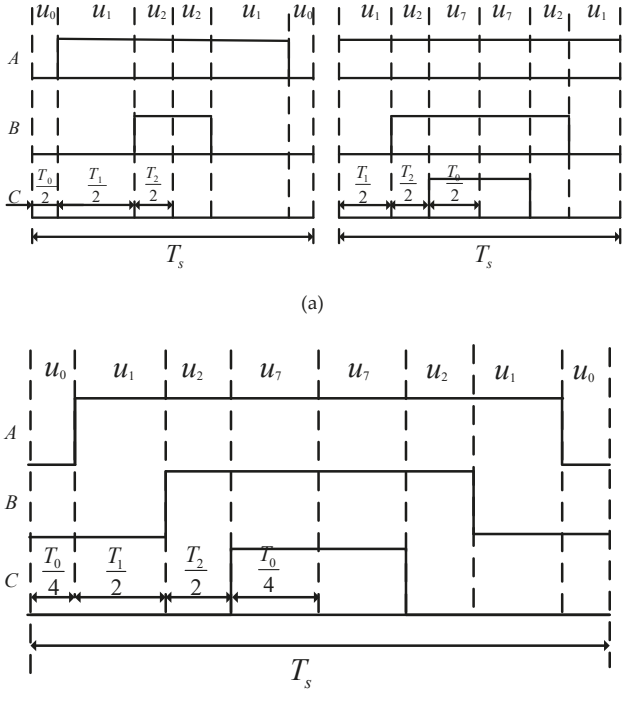


Figure 9. Switching sequences. (**a**) DPWM; (**b**) SVPWM.

4. Simulation and Experimental Validation of the Proposed Scheme

A PV inverter experimental test rig based on digital signal processing (DSP) is developed to verify the DPWM control algorithm as Figure 10a shown. DSP takes a high-performance 32-bit fixed-point TMS320F2812 as the controller (clock frequency 150 MHz, working voltage 3.3 V, Texas Instruments Incorporated, TX, USA); its chip contains 128 K 16-bit FLASH, 16-way 12-bit A/D conversion, two event managers and so on. Experimental tests are carried out by five photovoltaic panels (as shown in Figure 10b) in series under an ambient temperature of 25 °C and a daylight illuminance of 1000 W/m^2; the parameters of a single photovoltaic module are presented in Table 4. The output voltage range of the DC/DC converter (5 kW) is 100-400 V. The power module model of the DC/AC converter (2 kW) is PM30RSF060 (as shown in Figure 10c), and its maximum switching frequency is 20 kHz.

Before the proposed system is validated by the experimental tests, an MPPT algorithm with the associated equivalent circuit is simulated.

Table 4. Photovoltaic module parameters.

Open-Circuit Voltage (V)	Short-Circuit Current (A)	Max Voltage (V)	Max Current (A)	Max Power (W)
45.2	5.36	37.1	5.11	190

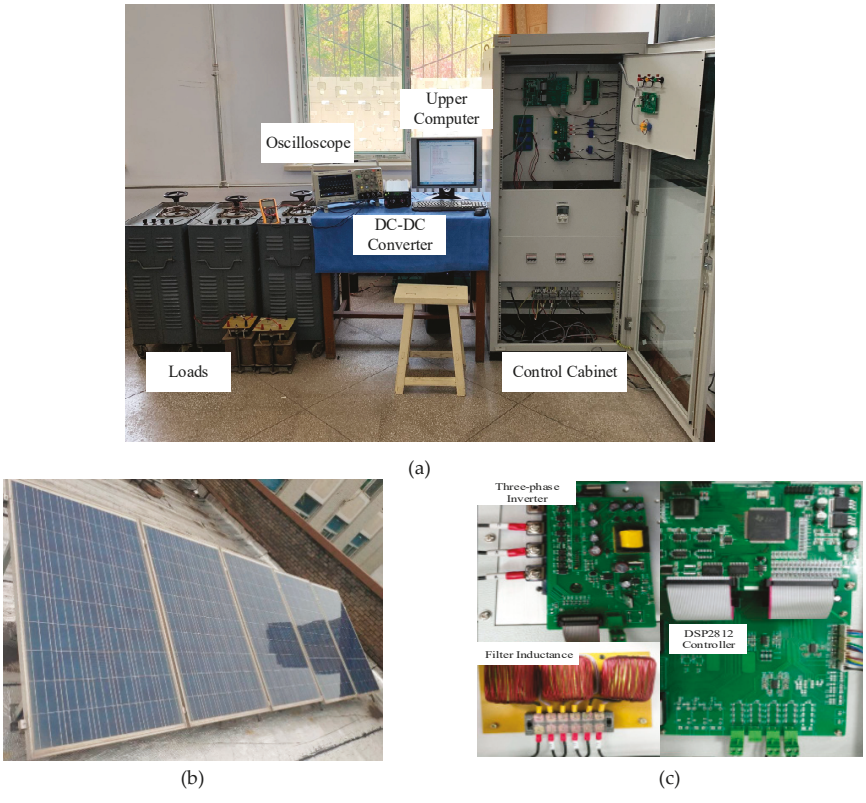


Figure 10. Experimental system. (**a**) Test rig; (**b**) Photovoltaic modules; **(c)** DC/AC converter.

4.1. Simulation Results of Different Varied Solar Irradiations

In a PV power system, the weather conditions, such as cloudy, rainy, dust, etc., will influence the power conversion. In most applications in this field, solar irradiation is considered as one of the most important factors in power generation, where weather variation will be mostly reflected in solar irradiation. We therefore test the PV power system performance as the solar irradiation varies. A series of waveforms in Figure 11 provides the auto-tracking process when the MPPT algorithm works with the DC/DC converter. Through the DC/DC converter, the output DC voltage of photovoltaic modules is kept at 140 V while the duty ratio D is 0.735 in the reference condition. In order to validate the performance of a DC/DC converter with the MPPT algorithm, varied solar irradiations are applied to the PV array. The performance is shown in Figure 11a–d.

As Figure 11a–d show, the current, the voltage and the power of the PV panel spontaneously follow the rapid variation of the solar irradiation. The proposed PV power system reaches the target of maximal utilisation of solar energy with limited oscillation, which in turn validates the excellent performance of the MPPT scheme applied in this investigation.

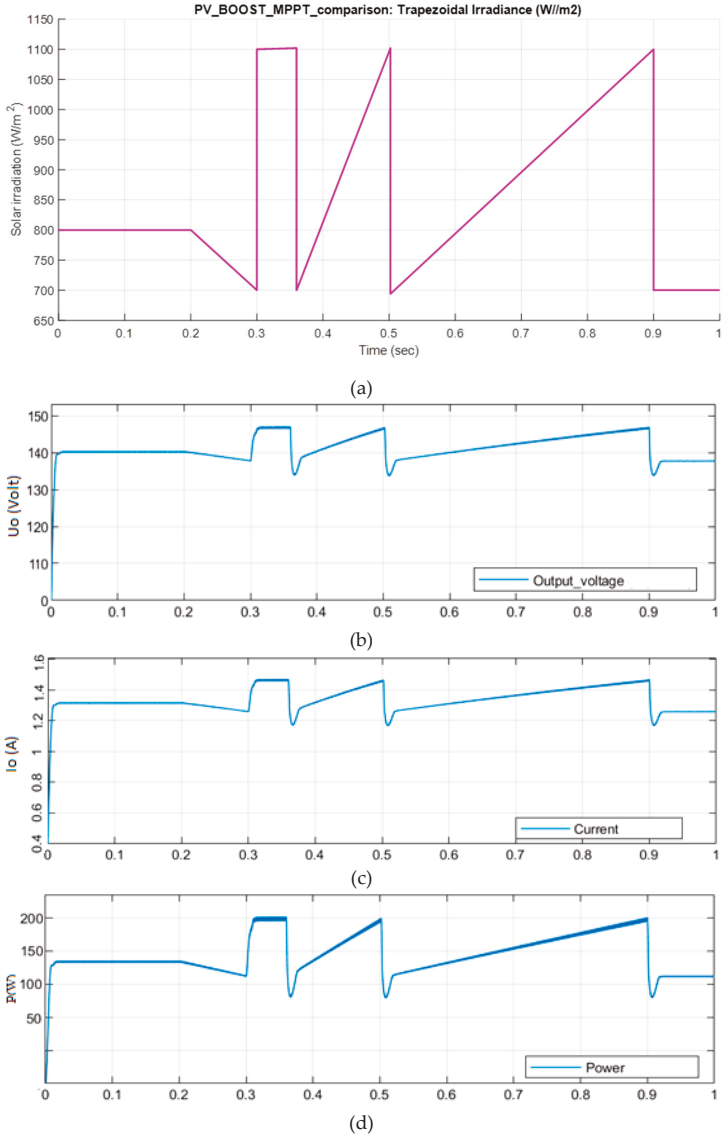


Figure 11. The performance of the DC/DC converter with varied solar irradiation. (**a**) Varied solar irradiation; (**b**) the output voltage at maximum power point (MPP); (**c**) the output current at MPP; (**d**) the output power at MPP.

4.2. DC/AC under the DPWM scheme

The DC/AC converter runs with a three-phase symmetrical resistive load (R_L = 40 Ω, L_L = 10 mH). The switching period is selected as T_s = 0.0002 s. The test waveforms are collected by the Tektronix oscilloscope TDS2024 (Test equipment Solutions Ltd, Berkshire, UK).

The control algorithm is designed to implement the proposed DPWM scheme. The flow chart of the DPWM algorithm can be obtained according to Equations (17)-(21), as shown in Figure 12.

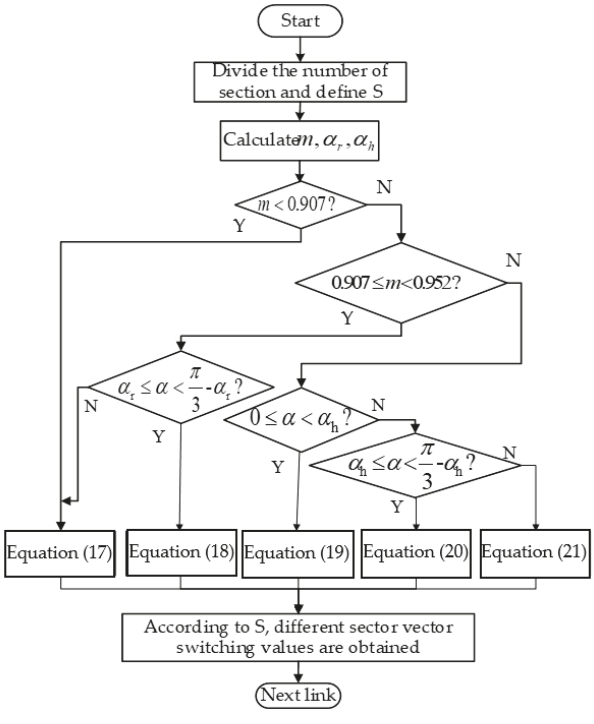


Figure 12. Flowchart of the proposed DPWM regions algorithm.

The transformation sequence of the DPWM overmodulation sector is shown in Figure 13.

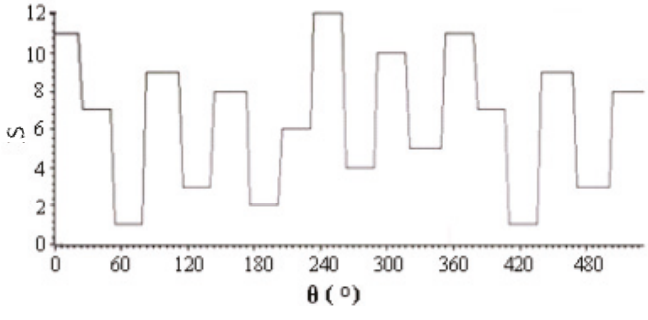


Figure 13. Sector transformation sequence.

The SVPWM modulation waveform in the linear modulation area and the DPWM modulation waveform with different modulation coefficients are shown in Figure 14.

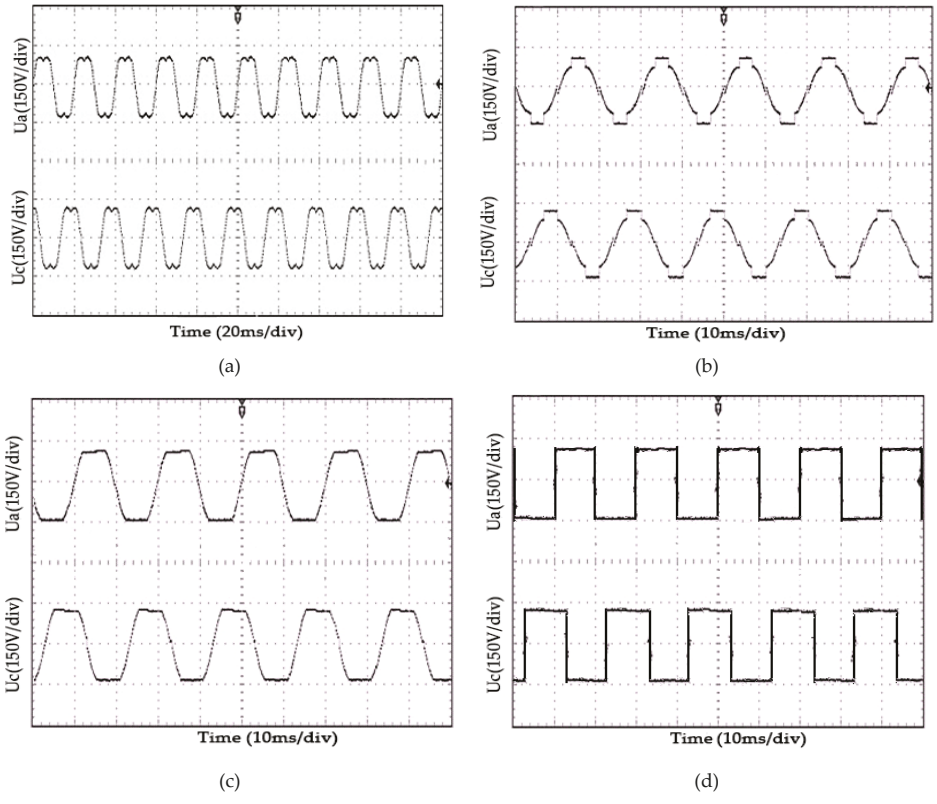


Figure 14. Modulation waveforms under different modulation schemes. (**a**) Space vector pulse width modulation (SVPWM); (**b**) DPWM (m = 0.778); (**c**) DPWM (m = 0.916); (**d**) DPWM (m = 1).

It can be seen from the figures that as the modulation coefficient increases, the peak of the DPWM modulation wave is gradually flattened and finally operates in the square wave operation state, thereby achieving linear control of the inverter output fundamental voltage over the entire modulation range.

When the modulation coefficient m = 0.92, the output pulse waveforms of TMS320F2812 under different strategies are shown in Figure 15. The waveforms of the output phase voltage and current are presented in Figure 16 and the spectral analysis results of the current are shown in Figure 17.

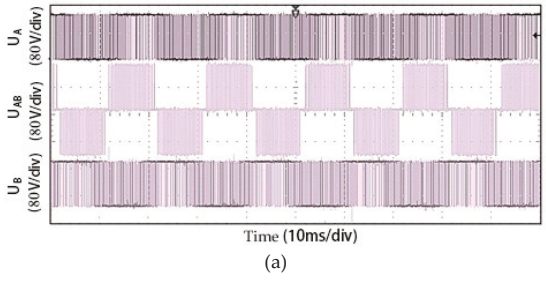
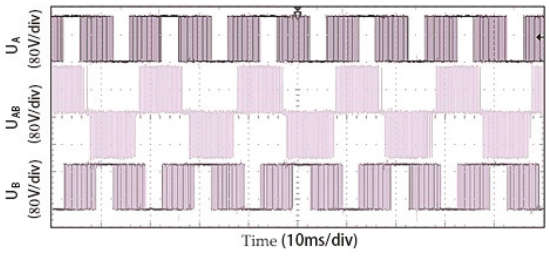
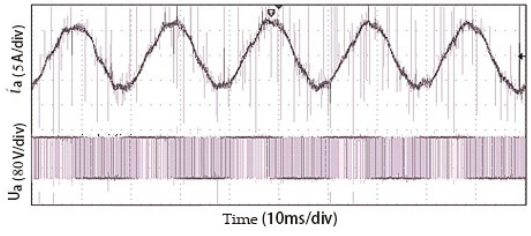


Figure 15. *Cont.*

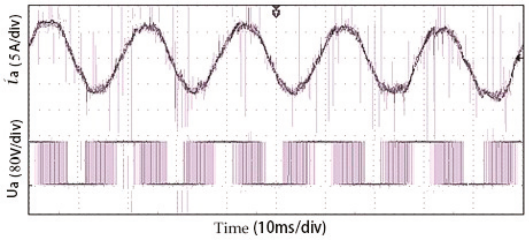


(b)

Figure 15. Pulse waveforms under different modulation schemes. (**a**) SVPWM; (**b**) DPWM.

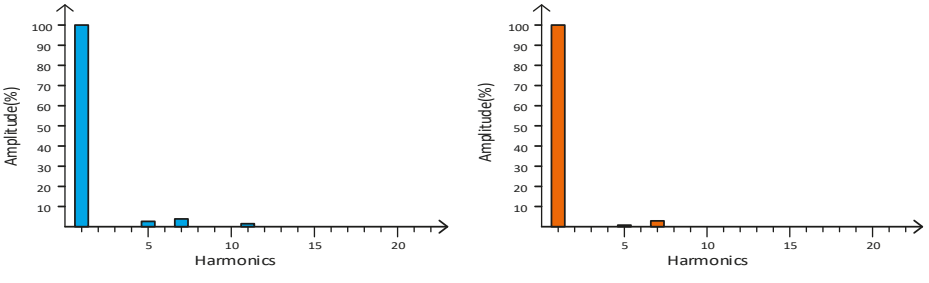


(a)



(b)

Figure 16. Output voltage and current waveforms. (**a**) SVPWM; (**b**) DPWM.



(a) (b)

Figure 17. Spectral analysis results of the current. (**a**) SVPWM; (**b**) DPWM.

From Figures 15–17, it can be seen that the upper and lower arms are not operated in the one-third period under the proposed strategy. Compared with the switching control pulse of conventional SVPWM with the same carrier frequency, the switching time is reduced by one-third. The switching

losses can be effectively reduced so as to increase the efficiency. The harmonic contents of the load current measured by the spectrum analyzer are presented in Figure 17 and Table 5.

Table 5. Harmonic contents in the load current.

Harmonics	SVPWM	DPWM
5th	3.55%	0.93%
7th	4.84%	3.68%
11th	1.61%	0
THD	6.58%	4.40%

Clearly, the amplitude of the 5th, 7th and 11th harmonics under the DPWM modulation strategy are lower than that of the SVPWM modulation strategy. The THD of the conventional SVPWM modulation strategy is 6.58%, while that of the DPWM overmodulation strategy is reduced to 4.4%. The current waveforms of the proposed DPWM algorithm are close to sinusoidal, and it appears to have a higher utilization ratio of the DC voltage than the SVPWM. In turn, this leads to reduced switching losses and improved THD.

5. Conclusions

This paper has proposed a high-efficiency PV power generation system by combining an MPPT algorithm and a new control technology evolving from DPWM and overmodulation. It can realize the modulation of a full area on the basis of traditional SVPWMs. A DC/DC converter with an inverter simulation model and an experimental test rig are developed to justify the proposed method. The main contributions of this work are:

(i) A P&O MPPT algorithm is applied to a boost DC/DC converter so as to effectively harvest solar energy and transform to DC electricity;
(ii) A novel control technology is proposed, combining discontinuous pulse width modulation (DPWM) and overmodulation technology to better utilize the DC-link voltage.
(iii) It has been shown by measurements that through implementing this algorithm, the switching losses in the power electronic devices are reduced.
(iv) The test results have confirmed that the DPWM overmodulation algorithm can effectively reduce harmonic distortion of the three-phase output voltage and current. It has also improved the conversion efficiency of photovoltaic systems.
(v) The proposed technology is simple to implement in practical PV inverters as there are no alterations to existing hardware design. It may also be applied to other grid-tie inverters to improve their performance.

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Nomenclature

α	Angle between the output voltage vector and the horizontal axis
α_γ	Angle between the intersection of the output voltage vector and the hexagon boundary, and the vertex of hexagon
α_h	Control angle to determine how long the output voltage vector stays at the vertex of hexagon
γ_{IL}	Current ripple factor of the inductor
γ_{VO}	Voltage ripple factor of the inductor

C_i,	Capacitance of the input capacitor in DC/DC converter
C_o,	Capacitance of the output capacitor in DC/DC converter
D	Duty ratio of DC/DC converter
f	Switching frequency of a DC/DC converter
i_a, i_b, i_c	Inverter output currents
I_{mpp}	Equivalent output current at maximum power point
L	Filter inductance
L_L	Symmetrical load inductance
L'	Inductance of a DC/DC converter
m	Modulation coefficient
N	Sector
p_{mpp}	Maximum power of a PV module
R	Filter inductance
R_L	Symmetrical load resistance
R_{mpp}	Equivalent resistance at maximum power point
R_O	Load resistance of the DC/DC converter
S	Sector number
T_1,T_2, T_0	Action time of adjacent fundamental voltage vectors and zero vector
T_s	Switching period
$u_0 \sim u_7$	Basic voltage space vectors
U_α,U_β	Two components of the output voltage vector in the $\alpha - \beta$ coordinates
U_d	DC-link voltage
u_m	Amplitude of the phase voltage
u_{m_max}	Maximum phase voltage in linear modulation area
U_{out}	Output voltage
V_{mpp}	Equivalent output voltage at maximum power point
V_O	Load voltage of the DC/DC converter
t_{rN}	Turn-on time
t_{fN}	Turn-off time
f_s	Switching frequency of power devices
I_{CN}	Forward current of IGBT
I_{CM}	Amplitude of the sinusoidal current

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