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Micro- and Nanotechnology of Wide Bandgap Semiconductors

Edited by
Anna B. Piotrowska, Eliana Kamińska and Wojciech Wojtasiak

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About the Editors

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Editorial

Micro- and Nanotechnology of Wide-Bandgap Semiconductors

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Gallium Nitride and Related Wide-Bandgap Semiconductors (WBS) have constantly received a great amount of attention in recent years. The main reason behind it is that several relevant high-power/high-frequency material parameters of semiconductors such as high breakdown field and low intrinsic carrier concentration, scale advantageously with bandgap. Semiconductor devices based on WBS allow for operation under extreme conditions, like high temperatures and electric fields. A huge range of wavelengths from IR to deep UV, enabling bandgap engineering together with excellent electron transport properties, makes nitrides attractive for electronic and optoelectronic devices as well. Today, nitride-based devices are widely used in high-performing radars (mainly 3D AESA), telecommunications (LTE-A, 5G), power electronic systems, light-emitting diodes and lasers. Despite substantial progress over the last twenty years, all these devices are still the subject of intense research to reach their full potential [1–4].

In this Special Issue, eight papers are published, covering various aspects of wide-bandgap semiconductor device technology, from substrates through epi-growth and semiconductor doping, to novel process modules for HEMTs, vertically integrated LEDs and laser diodes, and NWs-based nanoLEDs.

K. Grabianska et al. reported on the recent progress in bulk GaN technology achieved at Unipress, Poland [5]. Two processes, namely basic ammonothermal growth and halide vapor phase epitaxy have been thoroughly investigated and their advantages, disadvantages, and prospects discussed in detail. The authors suppose that within few years high-quality 2-in. truly bulk GaN substrates will be offered in large quantities, but today the main method for mass fabrication will be HVPE with Am-GaN crystals as seeds.

M. Stepniak et al. [6] investigated the process of selective-area metalorganic vapour-phase epitaxy (SA-MOVPE) of GaN and AlGaN/GaN hetereostructures intended for HEMT technology with bottom-up architecture. Excellent growth uniformity, appropriate structure profile, and precise control of compositional gradient were obtained. The applicability of the SA-MOVPE process in making GaN-based 3D nano- and microstructures for electroacoustic, electromechanic, and integrated optics devices and systems was discussed.

K. Sierakowski et al. [7] reported on high-pressure post-implant annealing of GaN at high temperatures. The thermodynamics of the process was discussed and its application for GaN processing was investigated in two aspects. First focused on GaN:Mg for p-type doping, second on GaN:Be treated as a case study for analysing mechanisms of dopant diffusion. Different configurations of the annealing process were studied in order to prevent GaN surface from decomposition. Mg activation exceeding 70% was reached together with electrical properties similar to those of MOVPE-doped GaN.

AlGaN/GaN metal-insulator-semiconductor high-electron-mobility transistors (MISHEMT) with a low-temperature epitaxy (LTE)-grown single crystalline AlN gate dielectric were demonstrated by M. Whiteside et al. [8]. Post-gate annealing effects were

studied in detail showing considerable increase of 2DEG mobility and reduction of interface state density at the AlN/GaN interface after post-gate annealing. Consequently, important increase of extrinsic transconductance, reduction of reverse gate leakage, and suppression of drain current were reached in final LTE-AlN MISHEMT.

D. Gryglewski et al. proposed a novel approach to characterizing self-heating process in GaN-based HEMTs [9]. An advanced measurement system based on DeltaVGS method with implemented software enabling accurate determination of device channel temperature and thermal resistance was developed. Three types of GaN-based HEMTs were taken into consideration—commercially available GaN-on-SiC (CGH27015F and TGF2023-2-01) and GaN-on-Si (NPT2022) devices, as well as model GaN-on-Am-GaN HEMT [10]. The main advantage of the proposed approach is that it allows taking into account the self-heating effect of transistors during design of microwave devices and high-power amplifiers for systems using variable-envelope signals such as LTE-A and 5G radios.

Marcin Siekacz et al. demonstrate the applications of tunnel junctions (TJs) for new concepts of monolithic nitride-based multicolour light-emitting diode (LED) and laser diode (LD) stacks [11]. GaN-on-GaN epistructures under investigation were grown by plasma-assisted molecular beam epitaxy (PAMBE). A stack of four LDs operated at pulse mode with emission wavelength of 453 nm and two-colour (blue and green) LEDs were demonstrated. The presented design is a viable alternative to achieving III-nitride high-power pulse laser diodes for such applications such as gas sensing or LIDARs. The stack of multicolour LEDs interconnected by TJs is promising for white-colour, phosphorus-free LEDs and for LED array displays. The use of TJs simplifies the electrical connections to buried LED structures, eliminating the need of p-type contacts application.

The two next paper addressed the topic of GaN-based nanowires, promising building blocks for future generation of electronic and optoelectronic devices. These nanostructures facilitate, for instance, the integration of GaN-based devices with Si electronics. Additionally, complicated heterostructures can be grown in the form of NWs with a crystallographic quality not achievable in the case of comparable planar hetereostructures for nanoLED.

M. Sobanska et al. made use of Kelvin probe force microscopy to assess the polarity of GaN nanowires (wurtzite structures) grown by plasma-assisted Molecular Beam Epitaxy on Si (111) substrates [12]. They showed that uniformity of the polarity of GaN nanowires critically depends on substrate processing prior to the growth. Several methods of surface preparation were investigated, and their results indicated that reversal of nanowires' polarity can be prevented by growing them on a chemically uniform substrate surface, particularly on in situ formed SiN_x or ex situ deposited AlOy buffers.

Anna Reszka et all. [13] reported on growth, optical and electrical properties of GaN/AlGaN Nanowire LEDs fabricated on Si (111) substrates by plasma-assisted molecular beam epitaxy (PAMBE). No catalyst was used to induce the nucleation of the NWs. The nanowire LEDs included three GaN quantum wells in the area of the p–n junction. The research focused on the influence of switching the growth polarity. Spatially and spectrally resolved cathodoluminescence spectroscopy and imaging, e-beam-induced current microscopy, the nano-probe technique, and scanning electron microscopy were used for structural analysis, and complemented by photo- and electro-luminescence characterization. The interpretation of the experimental data was supported by the results of numerical simulations of the electronic band structure. Their results proved that intentional polarity inversion between the n- and p-type parts of NWs is a potential path towards the development of efficient nanoLED NW structures.

We would like to take this opportunity to thank all authors for submitting papers to this Special Issue. We also hope that readers will find new and useful information on GaN and related semiconductors technology for high-power/high-frequency electronic and optoelectronic devices.

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Review

GaN Single Crystalline Substrates by Ammonothermal and HVPE Methods for Electronic Devices

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Abstract: Recent results of GaN bulk growth performed in Poland are presented. Two technologies are described in detail: halide vapor phase epitaxy and basic ammonothermal. The processes and their results (crystals and substrates) are demonstrated. Some information about wafering procedures, thus, the way from as-grown crystal to an epi-ready wafer, are shown. Results of other groups in the world are briefly presented as the background for our work.

Keywords: GaN; crystal growth; ammonothermal method; HVPE

1. Introduction

It seems that the lack of native wafers, of high structural quality, appropriate size, and electric properties, limits the development of GaN-based electronic devices. Highly conductive substrates are required for preparing high-power vertical transistors (i.e., the Metal-Oxide Semiconductor Field-Effect Transistor; MOSFET) or Schottky diodes. Semi-insulating GaN (SI-GaN) wafers are needed for preparing lateral devices, i.e., high electron mobility transistors (HEMTs). The nitride community is still working on the best technology for crystalizing GaN and fabricating GaN substrates. Growing GaN is, however, a rather challenging process. The compound melts at a very high temperature (exceeding 2200 °C) and the nitrogen pressure necessary for congruent melting is expected to be higher than 6 GPa [1–3]. GaN should, thus, be grown by other techniques requiring a lower pressure and temperature. Crystallization from the gas phase or solution has to be applied. Today, three technologies are mainly developed: sodium flux, ammonothermal, and halide vapor phase epitaxy (HVPE). The last one is the most popular one and developed by the industry. HVPE-GaN wafers are fabricated by such Japanese companies like SCIOCS by Sumitomo Chemical [4], Sumitomo Electric Industries (SEI) [5], Mitsubishi Chemical Corporation (MCC) [6], and Furukawa Metals [7]. HVPE-GaN substrates are also manufactured by Chinese Nanowin [8] and EtaResearch [9] as well as by French Lumilog by Saint Gobain [10]. All these companies sell highly conductive and semi-insulating 2-inch and even 4-inch HVPE-GaN substrates. They are all prepared from HVPE-GaN grown on foreign seeds, which lower the product's structural quality.

Companies and research institutes working on the ammonothermal method are the following: Institute of High Pressure Physics Polish Academy of Sciences (IHPP PAS; Warsaw, Poland) [11], SixPoint Materials Inc. (Buellton, CA, USA) [12], University of California Santa Barbara (Santa Barbara, CA, USA) [13], University of Stuttgart (Stuttgart, Germany), University of Erlangen (Erlangen, Germany) [14], MCC (Tsukuba, Japan) [15], Tohoku University (Sendai, Japan) [16], and Kyocera

(formerly Soraa, Inc., Santa Barbara, CA, USA/Kyoto, Japan) [17]. Two-inch as well as smaller ammonothermal GaN (Am-GaN) substrates are sold in limited quantities only by IHPP PAS [18].

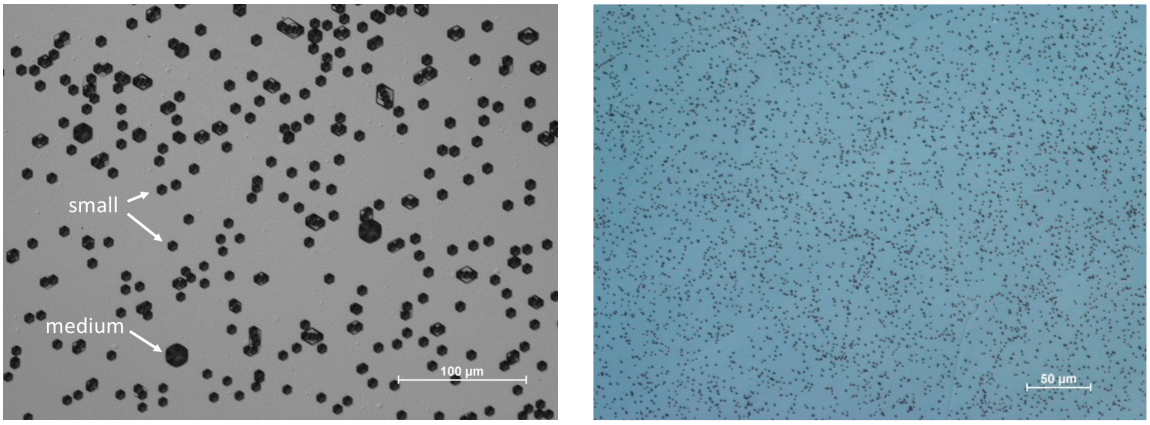
The sodium flux method is mostly developed at Osaka University [19] and their GaN crystals or substrates are not available on the market. It should be, however, remarked that a 6-inch sodium flux crystal has already been demonstrated [20].

In this paper, the results of GaN bulk growth performed in Poland, at IHPP PAS, are briefly presented. Two technologies are described: HVPE and ammonothermal. Their advantages, disadvantages, and challenges are analyzed. It should be noted that no one has demonstrated a real bulk GaN crystal yielding several tens of wafers per boule. The technology allowing to reach this goal has also not been presented. The reasons for the lack of thick GaN are explained in this paper. During a growth process performed in a chosen vertical direction, crystallization occurs also in lateral directions. This, together with an anisotropy of growth, is the reason why obtaining truly bulk GaN is so difficult, even if native seeds of high structural quality are used. A few solutions that could help to further develop bulk GaN growth are, however, shown. Some information about wafering procedures, thus, the way from an as-grown crystal to an epi-ready wafer, are also demonstrated. Results presented by other groups crystallizing GaN are used as reference. The beginning of the paper focuses on the requirements for GaN substrates. Then, HVPE-GaN crystallized on foreign seeds is discussed. In the next step, the ammonothermal method is presented and analyzed. The recent progress is shown. At the end of this paper, new results of HVPE-GaN grown on native Am-GaN seeds are discussed.

2. Requirements for GaN Substrates

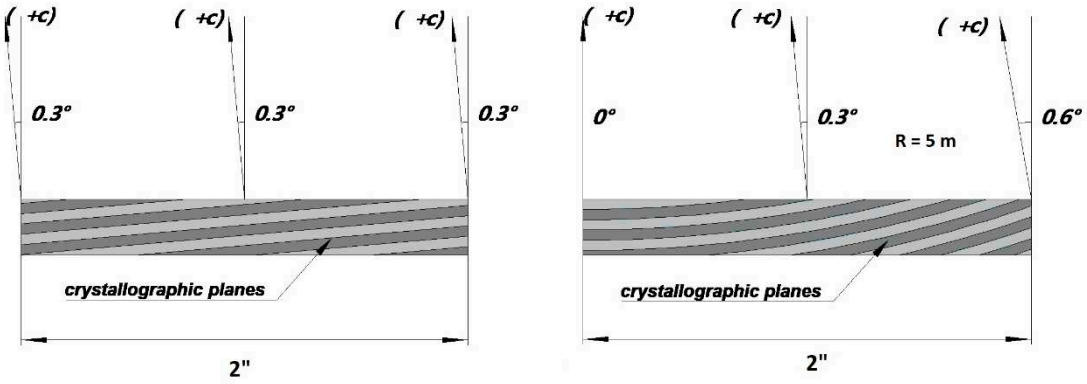
The most important property of a GaN substrate is its structural quality. The threading dislocation density (TDD) should be as low as possible and uniform across a wafer. In the case of GaN, the (0001) surface (c-plane) is mainly considered. Today, the lowest value of TDD, of the order of 10^4 cm^{-2}, is reported for Am-GaN [21–23]. This value is two orders of magnitude lower than TDD in commercially available HVPE-GaN wafers. It is well known that TDD is well correlated with the etch pit density (EPD) [24]. In fact, EPD is a parameter much more often used when describing a GaN wafer and its properties. It is much easier and cheaper to etch a surface of a substrate, count the pits and determine their density, than to analyze dislocations by transmission electron microscopy (TEM). Additionally, if TDD is of the order of 10^6 cm^{-2} or lower, it is difficult to detect dislocations by TEM. Therefore, in this paper, we refer only to values of EPD. When the (0001) GaN surface is etched three kinds of pits can be distinguished: large, medium, and small. According to Weyher et al. [24], these pits are correlated to screw, mixed, and edge dislocations, respectively. The data collected for Am-GaN and HVPE-GaN grown on Am-GaN seeds show that the density of large pits (screw dislocations) varies from 10^0 to 10^1 cm^{-2}. In turn, the density of medium and small pits (mixed and edge dislocations) is at the level of 5×10^4 cm^{-2} [23,25]. Figure 1 allows to compare EPD on the c-plane surface of a typical Am-GaN wafer from IHPP PAS and commercially available HVPE-GaN.

The low EPD is not the most important feature of GaN substrates. Flatness of crystallographic planes (see Figure 2) seems to be more important. It guarantees a uniform off-cut of the substrate, which, in turn, allows for epitaxial growth of any future device structure with an atomic step flow. Generally, the variation of off-cut across the surface should not be higher than 0.1°. This is the main and basic requirement for promoting the step flow, controlling the composition of ternary alloys in the device layers, as well as the incorporation of dopants and unwanted impurities [26–28]. For a 2-inch wafer, the required value of radius of curvature should be higher than 15 m. In commercially available HVPE-GaN substrates, the radius is at the level of 5 m, but in the case of 2-inch Am-GaN, it is usually around 30 m. The off-cut uniformity is also important for preparing an epi-ready surface of a substrate. This is also one of the most important requirements for a wafer. The surface, usually (0001) in the case of GaN, should be epi-ready, without any subsurface damage, with the value of the root means square (RMS) lower than 0.1 nm, and clean (see Figure 3).



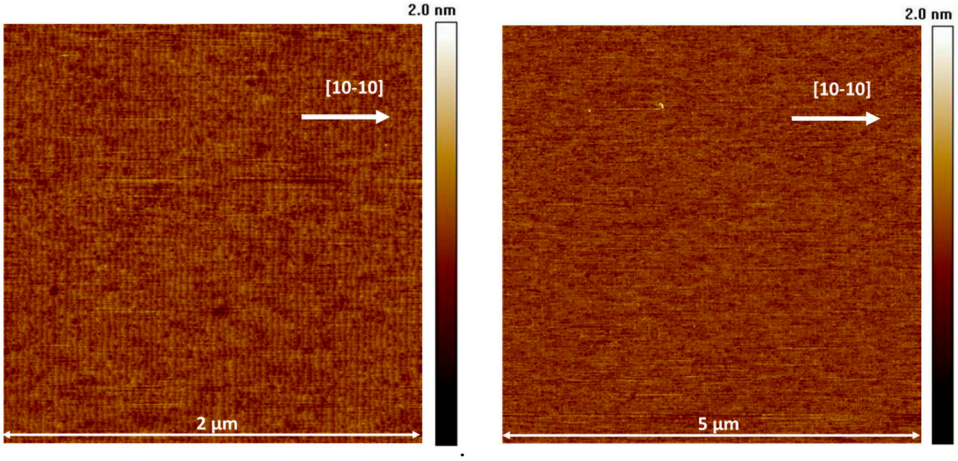
(**a**) (**b**)

Figure 1. Optical microscope images of (0001) surface (after etching in KOH-NaOH solution at 500 °C) of commercially available 2-inch: (**a**) Am-GaN wafer; medium and small pits visible; EPD = 5×10^4 cm^{-2} (15 min etching); (**b**) HVPE-GaN; it is difficult to distinguish the size of pits; EPD = 5×10^6 cm^{-2} (5 min etching; longer time would result in overlapping of pits and lowering the EPD); attention should be paid to different scales on both pictures; difference in pit sizes between (**a**) and (**b**) results from different etching time.



(**a**) (**b**)

Figure 2. Scheme of GaN substrates with two kinds of (0001) crystallographic planes: (**a**) flat; (**b**) bent.



(**a**) (**b**)

Figure 3. Example of typical atomic force microscopy image of epi-ready (0001) surface of 2-inch ammonothermal GaN wafer fabricated at IHPP PAS: (**a**) 2 µm × 2 µm area and (**b**) 5 µm × 5 µm area.

Last but not least, there is a requirement for a GaN wafer regarding its free carrier concentration. A high, of the minimum order of 10^{18} cm^{-3}, and uniform value is needed if the substrate will be used for a vertical device (e.g., MOSFET). This allows to fabricate, in a relatively easy way, a stable and low-resistance ohmic contact to the bottom part of the substrate. Obviously, SI substrates with resistivity higher than 10^8 Ω·cm at room temperature (RT) are needed for lateral devices.

3. HVPE-GaN Wafers—Crystallization on Foreign Seeds

HVPE is a method of crystallization from gas phase. Figure 4 represents a scheme of a typical HVPE horizontal quartz reactor used at IHPP PAS. In a quartz tube, there are two zones with different temperatures: (i) low (800–900 °C), where hydrochloride (HCl) reacts with gallium (Ga) to synthesize gallium chloride (GaCl) and (ii) high (1000–1100 °C), where GaCl reacts with ammonia (NH_3) and GaN is crystallized. All reactants are transported by a carrier gas (N_2, H_2, Ar, He, or their mixtures). The temperature is set with a multi-zone resistive canthal-based heater. In many cases, the resistive heating of the growth zone is replaced by RF heating. Details of such a reactor configuration were presented in many papers, e.g., [23,29,30]. Thermodynamics of GaN crystal growth process is well described in References [31,32].

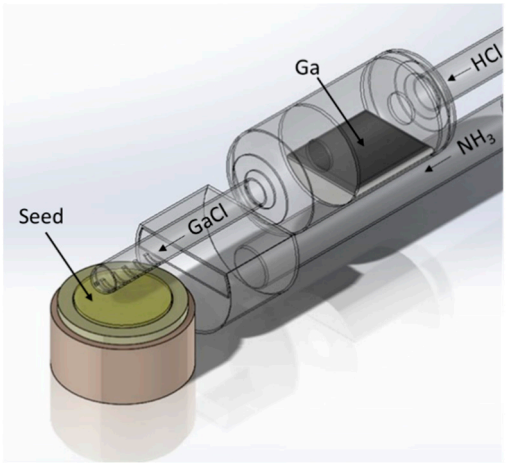


Figure 4. Scheme of horizontal HVPE reactor working at IHPP PAS. All reactants are transported by carrier gas.

The HVPE technology demonstrates two great advantages: (i) a relatively high growth rate, which exceeds 100 μm/h and (ii) a possibility to crystallize high-purity material; concentrations of unintentional dopants (silicon, oxygen, iron) are generally of the order of 10^{16} cm^{-3} or even lower. A doping process with germanium or silicon to achieve highly conductive crystals as well as with carbon or iron for SI ones is well recognized and described in the literature, e.g., [33–37]. The main crystallographic growth direction in the HVPE technology is [0001] (the c-direction). GaN is predominantly crystallized on a foreign seed. It is either a gallium arsenide (GaAs) substrate with a low-temperature buffer layer of GaN or a metal-organic vapor phase epitaxy (MOVPE) GaN on sapphire template [38,39]. GaN crystallized on GaAs consists of areas (e.g., arranged in stripes) of high (10^8 cm^{-2}) and low (5×10^4 cm^{-2}) EPD [40,41]. Thus, the (0001) surface of a GaN substrate (after chemical etching of GaAs) is neither macroscopically uniform nor flat, which makes it impossible to prepare it to an epi-ready state. The bending of crystallographic planes is not observed thanks to similar thermal expansion coefficients of GaN and GaAs as well as the existence of inversion domains that reduce stress in GaN [38].

As mentioned earlier, the second kind of seeds are MOVPE-GaN/sapphire templates [39,42,43]. In this case, stress induced by the difference in thermal expansion coefficients of new-grown thick HVPE-GaN and sapphire results in a well-controlled self-separation of GaN during the cooling

process. This way, free-standing (FS) crystals are obtained. Substrates prepared from them will have macroscopically flat c-plane surfaces, uniform EPD of the order of 5×10^6 cm^{-2}, but bent crystallographic planes. The last results from the difference between the lattice constants and thermal expansion coefficients of sapphire and GaN. The value of the bowing radius of crystallographic planes of a typical GaN substrate does not exceed 10 m. It is not possible to prepare an epi-ready surface with a uniform off-cut. The substrates are plastically deformed and have dislocation bundles creating a cellular network [44].

In the authors' opinion, the HVPE technology requires a fresh approach. The only way to further develop GaN substrates is GaN-on-GaN crystallization. Since there are no native HVPE-GaN seeds of high structural quality, the ones prepared by the ammonothermal method can be very useful.

4. Ammonothermal Crystal Growth of GaN

The scheme of the ammonothermal growth is the following: polycrystalline GaN (feedstock) is dissolved in supercritical ammonia enriched with mineralizers in the first zone of a high-pressure autoclave. The dissolved feedstock is transported to the second zone, where the solution is supersaturated and crystallization of GaN on native seeds takes place. An appropriate temperature gradient applied between the dissolution and crystallization zones enables the convective mass transport. Mineralizers are added to ammonia in order to accelerate its dissociation and enhance the solubility of GaN. The growth is proceeded in a different environment: basic or acidic, depending on the type of mineralizer. The ammonobasic process makes use of alkali metals or their amides, while in ammonoacidic growth, halide compounds are present. A negative temperature coefficient of solubility is observed in the ammonobasic approach [45,46]. As a consequence, the chemical transport of GaN is directed from the low-temperature solubility zone (with the feedstock) to the high-temperature crystallization one (with the seeds). The pressure of ammonia in the reactor is usually between 100 and 600 MPa and the typical growth temperature is in the range 400–750 °C [47].

Schemes of the high-pressure autoclave and a time-temperature relation of the two temperature zones applied for the basic ammonothermal crystallization developed at IHPP PAS are presented in Figure 5a,b, respectively. Red and green curves (see Figure 5b) represent, respectively, the temperature of the feedstock and growth zones. At the beginning, the zone with feedstock is heated and the material starts to dissolve in ammonia. Herein, the feedstock temperature is higher than the temperature of the crystal growth zone. During the dissolution stage, a back etching process occurs; the seeds are etched and they couple with the solution; a full contact is maintained between the surfaces of the GaN seeds and ammonia. Then, the crystal growth zone is heated to a temperature higher than that in the feedstock zone. In turn, the temperature of the feedstock zone decreases and the crystal growth starts. After a few months, the autoclave is cooled down, ammonia is released, and the crystals can be removed.

The basic ammonothermal growth at IHPP PAS consists of two parts [11]: (i) increase of the size of the seeds; they can be gradually enlarged (in diameter) by taking advantage of the lateral growth phenomena in non-polar and/or semi-polar directions and (ii) seed multiplication, which is concentrated on crystallization mainly in the vertical direction (in the [000-1] direction), after the growth process, the crystals are sliced perpendicularly to the growth direction and they can either increase the population of seeds used for subsequent growth runs or be subject to the wafering process (substrate fabrication). It should be remarked that the crystallization in the [0001] direction is treated as parasitic with an unstable morphology. In order to avoid the growth in this direction, specially prepared holders are used for the seeds. As a result, the (000-1) surface or side surfaces (non-polar and semi-polar) can be exposed for growth, while the (0001) face is always masked.

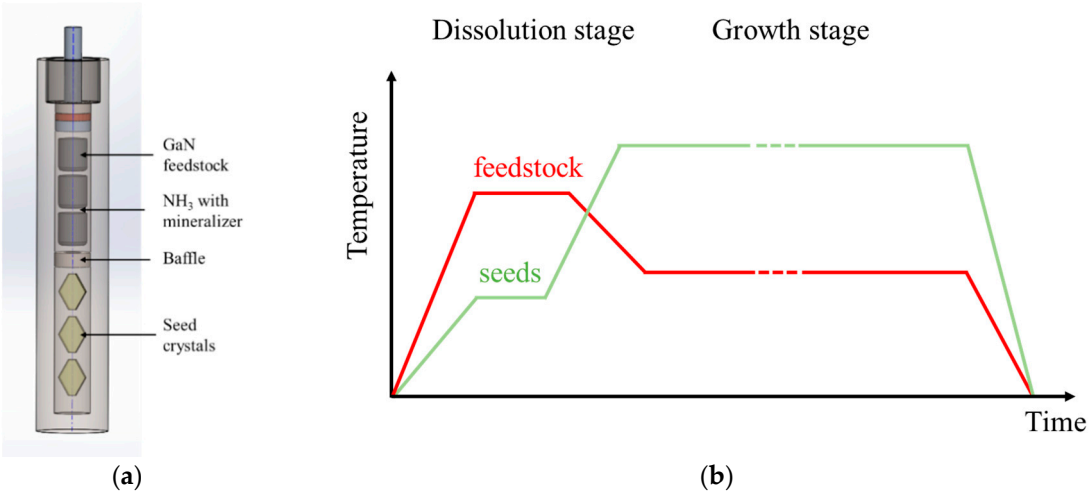
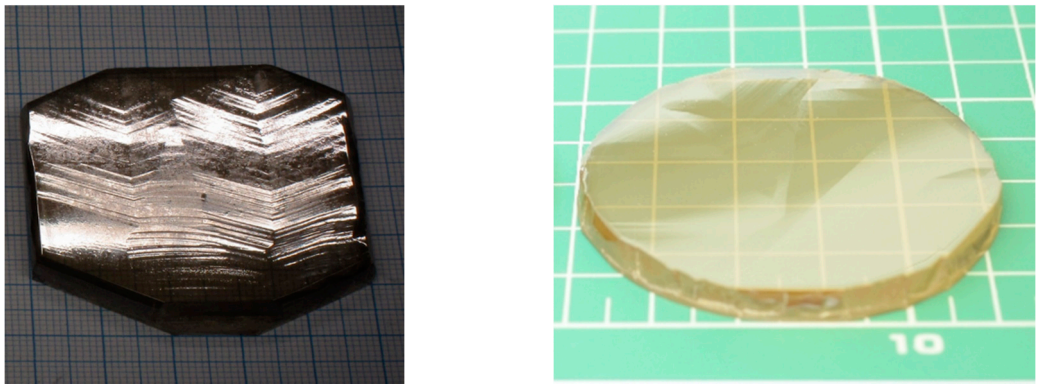


Figure 5. Scheme of: (**a**) high pressure ammonothermal autoclave; (**b**) temperature-time profiles of feedstock (red curve) and crystal growth zones (green curve) during a typical ammonothermal crystallization process at IHPP PAS.

One of the most important factors limiting Am-GaN growth in the [000-1] direction (seed multiplication) is associated with the anisotropy of growth as well as crystallization that occurs in the lateral directions at the edges of the crystal. It was shown [11] that the kinds and concentrations of impurities incorporated into GaN growing on the non-polar (11–20) and (10–10) facets and on the (000-1) plane are vastly different. This causes stress and finally leads to a plastic deformation of the growing Am-GaN crystals and appearance of cracks close to the edges [11]. Changing the shape of a seed from an irregular (hexagonal) to a round one (see Figure 6) as well as masking its edges with a metal border allowed us to grow stress-free and crack-free GaN. Both the formation of side facets as well as uncontrolled growth in the lateral directions were hindered. The border effectively counteracts the crystallization in all unwanted lateral directions. Only one facet, the (000-1) plane, was crystallized. It should be noted that it is much easier to provide a metal border around the growing crystal when the seed is round. Therefore, there were no cracks visible in the round-shaped crystals. Applying this new shape allowed to increase the yield of an ammonothermal crystal growth process. Before, cracks from the edges had been able to propagate to the center of a crystal during wafering procedures. The quantity of substrates obtained from crystals had been low. Thus, the lack of cracks at the edges seems very important from the point of view of GaN substrate production. It should be noted that each crystal after the growth process is subject to a significant mechanical treatment. Firstly, slicing is performed, and the Am-GaN seed is retrieved. It can be re-used in an ammonothermal crystallization run. In turn, the new-obtained crystal is misoriented and ground. Then, it is cut into a round shape. The primary and secondary flats are formed. Furthermore, edge grinding is performed. Next, the crystal is lapped and polished. At the end, its (0001) surface is prepared to an epi-ready state by chemo-mechanical polishing (CMP) and cleaning.

Today, one ammonothermal growth process allows to obtain a few tens of crystals with a diameter larger than 2.1-inch (see Figure 7a) and of high structural quality. This, in turn, enables to fabricate high structural quality (crystallographically flat and with low EPD) 2-inch GaN wafers (see Figure 7b). Unintentionally doped Am-GaN is n-type with free carrier concentration in the range $1 \times 10^{18} - 2 \times 10^{19}$ cm^{-3} [11]. The main unintentionally incorporated donor is oxygen. No intentional n-type doping is performed. Doping with Mn allows to compensate the oxygen donors and crystallize material with high resistivity (exceeding 10^{12} Ω·cm at 300 °C) [11].



(**a**) (**b**)

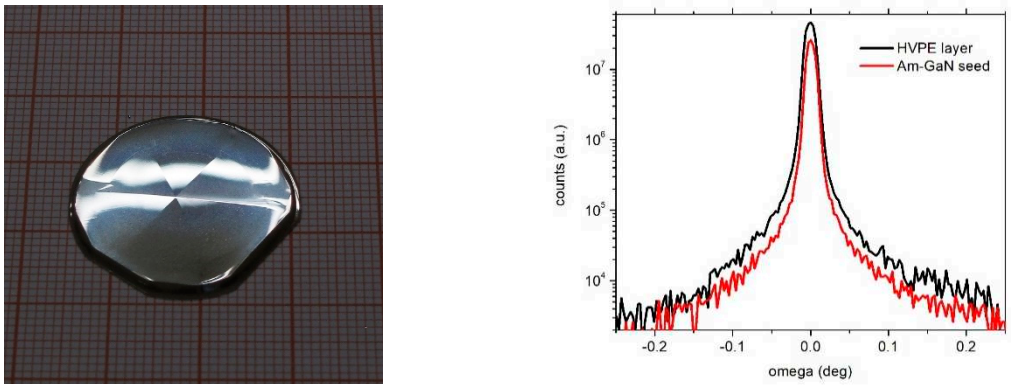
Figure 6. Examples of as-grown Am-GaN crystals of different shape: (**a**) 'old' hexagonal (**b**) 'new' round.

(**a**) (**b**)

Figure 7. (**a**) Am-GaN as-grown crystals from one crystal growth process; grid 1 mm; (**b**) 2-inch ammonothermal GaN substrate; primary flat (PF) and secondary flat (SF) are marked.

5. HVPE-GaN on Native Ammonothermal GaN Seeds

One of the important disadvantages of the ammonothermal crystal growth process is the low growth rate. The average value in the [000-1] direction is between 1 and 2 μm/h. Thus, as already mentioned, the ammonothermal method can be used as the source of seeds for HVPE growth. The first results of such a hybrid approach: HVPE-GaN growth on Am-GaN, were presented by IHPP PAS in 2013 [48]. Then, similar work was shown by MCC [49], and later, many other papers were published. They are summarized in References [23,50]. The growth of unintentionally doped HVPE-GaN on an Am-GaN seed proceeds in a hillock mode (see Figure 8a) with an average rate higher than 100 μm/h. The very high structural quality of an Am-GaN seed can be preserved in an HVPE layer (see Figure 8b). Doping processes performed to obtain highly conductive crystals (silicon or germanium) or SI ones (iron, carbon, or manganese), were also examined for HVPE-GaN grown on Am-GaN seeds. Crystals of high structural quality and required electrical properties were obtained. The free carrier concentration exceeded 1×10^{19} cm^{-3} [50]. It should be mentioned that in the case of highly resistive HVPE-GaN crystals doped with carbon or manganese, resistivity higher than 10^9 Ω·cm at 300 °C was detected [37]. It is a very important result, since the operating temperature of high power-high frequency electronic devices based on SI-GaN substrates is at least 300 °C.

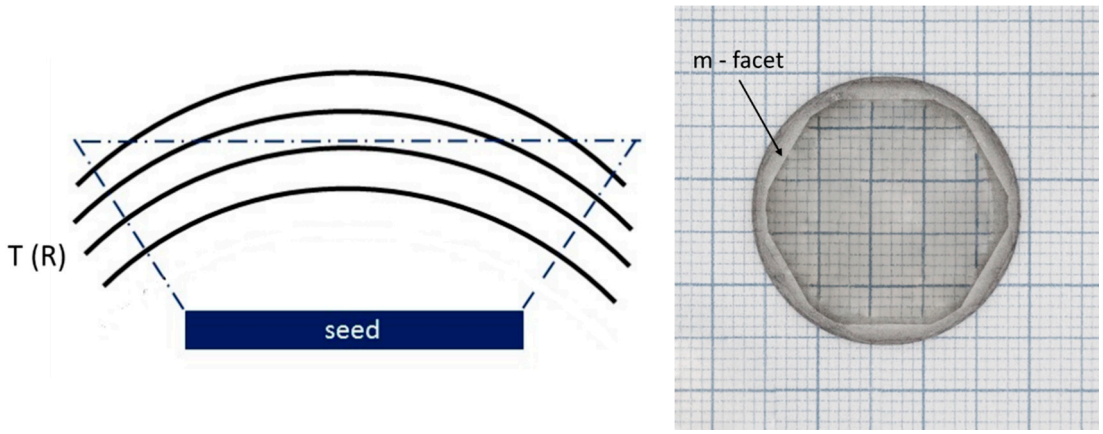


(**a**) (**b**)

Figure 8. HVPE-GaN grown on Am-GaN seed at IHPP PAS: (**a**) morphology; one central hillock is well visible; (**b**) X-ray rocking curve of Am-GaN seed and FS HVPE-GaN layer; full with half maximum (FWHM) for (00.2) reflection keeps the same value as Am-GaN seed: 43 arcsec and 50 arcsec, respectively.

It was observed that during the homoepitaxial crystallization of HVPE-GaN in the [0001] direction the non-polar and semi-polar growth of "wings" (laterally-grown material) leads to the formation of large stress close to the edges of the growing crystal. The reason for this is a different incorporation of dopants (mainly oxygen) into HVPE-GaN grown in the [0001] than in lateral directions. This leads, in turn, to different lattice parameters of the crystallized material [23,51,52]. The stress from the edges is much more significant than the one generated by the lattice mismatch between the seed and the deposited layer. Avoiding lateral growth during crystallization in the [0001] direction seems essential for developing the GaN bulk growth technology.

Like in the case of the ammonothermal process, growth in the lateral directions on the edges of the seed can also be eliminated in HVPE by using a metal ring (e.g., molybdenum). It increases the dissociation of ammonia. The supersaturation close to the edges of the crystal with the ring decreases. No growth takes place in the lateral directions. Unfortunately, the side facets are still formed. The main issue is to find such growth conditions that will allow to form only the side facets that grow faster than the material in the [0001] direction. Then, they will disappear and the crystal will increase its lateral size by growing only in the [0001] direction. According to a hypothesis by Professor Zlatko Sitar from North Carolina State University (USA) [53], such conditions may be achieved by controlling the thermal field around a crystal. It has to reach its final shape by adapting to this field rather than taking the hexagonal habit. The equilibrium shape can be overpowered by a proper design of the thermal field. In this case, the crystal will follow the thermal field and grow in a direction perpendicular to the isotherms. The idea is schematically shown in Figure 9. Such an approach was presented by HexaTech for aluminum nitride (AlN) growth by physical transport deposition (PVT) [54]. Obviously, the formation of supersaturation in the PVT and HVPE methods varies significantly. The supersaturation is the difference of thermodynamic potentials at the interface between a crystal and its environment. In the case of PVT it is almost unambiguous with the temperature distribution on the growing surface. In HVPE, reactions of all vapor species have to be considered. It should, however, be stated that if the equilibrium crystal shape of GaN can be overcome, it will be a transformative achievement for the HVPE technology. It has never been demonstrated before and will allow to grow true bulk GaN crystals of high purity, eventually yielding several tens of wafers per boule. To this day, the formation of side facets has not been defeated and they are still created during HVPE-GaN growth in the [0001] direction. In spite of this, MCC has already demonstrated 4-mm-thick HVPE-GaN-on-Am-GaN [22] and IHPP PAS showed 3-mm-thick HVPE-GaN-on-Am-GaN (see Figure 9b) [55].



(**a**) (**b**)

Figure 9. (**a**) Scheme of temperature distribution close to the growing crystal surface: it may allow for controlled crystal expansion and prevent crystallization on the sidewalls; (**b**) three-mm-thick HVPE-GaN grown on Ammono-GaN; equilibrium hexagonal crystal habit is well visible; c-plane is reduced; grid 1 mm.

6. Conclusions

The growth of high structural quality bulk GaN crystals can only be performed using GaN-on-GaN technology. Today, the main method for mass fabrication of GaN crystals is HVPE. This is due to its high growth rate and purity. The process repeatability is also the highest. Ammonothermal method can provide seeds for HVPE growth. However, if the ammonothermal technology is improved, it will become a great competitor for HVPE. It should be remembered that during one ammonothermal process, a few tens of crystals can be grown. Table 1 summarizes the advantages and disadvantages of the two methods presented in this paper. Most probably, the economy will decide which technology will be applied in the future.

Table 1. Summarized advantages and disadvantages of HVPE and ammonothermal crystal growth methods.

	HVPE	Ammonothermal
Advantages	1. high purity 2. high growth rate 3. easy doping 4. reproducibility	1. few tens of crystals in one run 2. reproducibility
Disadvantages	1. requires high structural quality native seeds 2. side facets formation 3. one or a few crystals in one run	1. requires high structural quality native seeds 2. low growth rate 3. low purity

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Conflicts of Interest: The authors declare no conflict of interest.

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Growth Uniformity in Selective Area Epitaxy of AlGaN/GaN Heterostructures for the Application in Semiconductor Devices

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Abstract: The design of modern semiconductor devices often requires the fabrication of three-dimensional (3D) structures to integrate microelectronic components with photonic, micromechanical, or sensor systems within one semiconductor substrate. It is a technologically challenging task, as a strictly defined profile of the device structure is obligatory. This can be achieved either by chemical etching or selective deposition on a masked substrate. In this paper, the growth uniformity of AlGaN/GaN heterostructures during selective-area metalorganic vapour-phase epitaxy (SA-MOVPE) was studied. Such structures are typically used in order to fabricate high-electron-mobility transistors (HEMT). The semiconductor material was deposited through 200 µm long stripe-shaped open windows in a SiO_2 mask on GaN/sapphire templates. The window width was varied from 5 µm to 160 µm, whereas mask width separating particular windows varied from 5 µm to 40 µm. The experiment was repeated for three samples differing in GaN layer thickness: 150 nm, 250 nm, and 500 nm. Based on theoretical models of the selective growth, a sufficiently uniform thickness of epitaxially grown AlGaN/GaN heterostructure has been achieved by selecting the window half-width that is smaller than the diffusion length of the precursor molecules. A Ga diffusion length of 15 µm was experimentally extracted by measuring the epitaxial material agglomeration in windows in the dielectric mask. Measurements were conducted while using optical profilometry.

Keywords: selective area growth; selective epitaxy; AlGaN/GaN heterostructures; gallium nitride; edge effects; effective diffusion length; MOVPE

1. Introduction

Group III nitrides, including (Al, In, Ga)N compounds, gained importance at the turn of the 20th and 21st centuries, especially in the field of optoelectronics and high power electronics. Gallium nitride is characterised by a wide band gap (3.4 eV) [1], high chemical and temperature stability [2] and large piezoelectric coefficients [3]. Its unique properties make it a material of choice for many advanced semiconductor devices, such as: high temperature devices, high electron mobility transistors (HEMT), microwave instruments, facet lasers, electroacoustic transducers and electromechanical resonators, field emitters or integrated optics devices. Those devices consist of 3D structures, such as U-shaped and V-shaped grooves, mesa structures, nanowire matrices or planar waveguides, which can be produced in two ways. In top-down architecture, the epitaxial layer is spatially patterned by wet or dry chemical etching, whereas, in bottom-up architecture, structures are selectively grown while using dielectric masks. Because of this, it is possible to integrate many opto-electro-mechanical devices

within one semiconductor substrate, which is required in order to achieve compactness, high stability, and efficiency, as well as minimise losses in modern, technologically advanced semiconductor devices [4].

Metalorganic vapour-phase epitaxy (MOVPE) is the most popular method that is used industrially to produce high quality gallium nitride layers. The possibility of precise control of several process parameters allows for the fabrication of sophisticated planar nano- and microstructures. The use of SA-MOVPE to get 3D semiconductor epitaxial growth on the nano- and micro scale is a promising, but challenging, approach. Numerous factors have to be addressed in the technological process. First of all, conducting epitaxy on a masked substrate causes heterogeneous layer growth in the window area. This phenomenon is called the edge effect and it results from excessive accumulation of epitaxial material adjacent to the dielectric mask. This is also associated with a different growth rate of a structure relative to non-selective deposition [4]. Homogeneous structure growth along the window area is necessary for keeping continuous metallization for the contact layer and close fitting between semiconductor components.

Two mechanisms of mass transport into the window area could be distinguished during the MOVPE process: vapour-phase diffusion and surface diffusion. The diffusion length of precursor molecules in vapour is several orders of magnitude greater than the surface diffusion length of the adatoms [5]. It was proved, for the first time, by Gibbon regarding InP selective deposition [6]. Mass diffusion is caused by precursor concentration gradient between masked and unmasked substrate surface. The Laplace Equation (1) describes the precursor concentration φ in the steady state

$$\nabla^2 \varphi = 0. \tag{1}$$

The mass flux to the substrate surface is balanced by molecule incorporation into grown layer, as local thermodynamic equilibrium can be established in the vicinity of the growth interface [7]. This can be formulated by a combination of Fick's first law and Langmuir adsorption model (2) [6]

$$-(D\nabla\varphi)\cdot\overrightarrow{n} = k\varphi \tag{2}$$

where D is diffusion coefficient, k is surface reaction rate, and $\overrightarrow{n}$ refers to the normal vector. Assuming that no crystal growth occurs on the dielectric mask, the reaction rate on masked substrate is equal to zero (3)

$$-(D\nabla\varphi)\cdot\overrightarrow{n} = 0 \ (on\ mask). \tag{3}$$

The ratio D/k is the key factor influencing the shape of the structure profile in the window area. It used to be called the effective lateral diffusion length of precursor molecules λ_{eff} [4,8–10]. Molecules are incorporated with similar probability into the epitaxial structure within the whole window area when the effective diffusion length is greater than the half-width of the window. Otherwise, the uneven accumulation of epitaxial material will be observed [4–6,8–18]. Surface diffusion additionally influences structure shape adjacent to the mask. The overall participation of surface diffusion in the profile of an epitaxial structure increases with the thickness of the deposited layer [14,19]. The diffusion length is strongly dependent on the composition and material parameters of the precursors in the reactor chamber, as well as the carrier gas type [5] and process parameters, such as pressure or temperature [4]. The effective diffusion length is primarily affected by the group III precursors concentration, as group V molecules have a minor influence on the growth rate [20].

A crucial aspect of the selective area epitaxy (SAE) of AlGaN/GaN heterostructures is a horizontal gradient of the $Al_xGa_{1-x}N$ composition that is caused by the difference in the diffusion lengths of Al and Ga molecules. Compositional variation is primarily derived by vapour-phase diffusion [9,19]. Based on Lennard–Jones potential theory, diffusion length is assumed to be inversely proportional to the square of the Lennard–Jones theorem length σ [4]. The effective diffusion length of Al molecules is expected to be smaller than the effective diffusion length of Ga molecules when using TMAl (trimethylaluminium)

and TMGa (trimethylgallium) as precursors for AlGaN deposition, as σ is longer in TMAl than in TMGa [21]. This leads to a larger concentration of Al adjacent to the mask when compared to the window center. Precise control of compositional variation is substantial for the fabrication of highly efficient optoelectronic devices while using multiple quantum wells (MQWs), as the application of MQWs causes a decrease of carrier lifetime and an increase of radiative recombination efficiency [15,19]. On the other hand, compositional uniformity is required in the heterojunction band-gap engineering for the application of HEMT or planar waveguides.

There were researches that were conducted for both rectangular [5,6,8–10,15,16] and hexagonal windows in the mask [11–13,22]. All of them showed that the edge effect is strongly dependent on the structure geometry and configuration of the dielectric mask. According to Hara, the profile of selectively grown layer can be described as (4) [16]

$$h_x = (h_{edge} - h_{planar}) \exp\left(-x \cdot \lambda_{eff}^{-1}\right) + h_{planar} \tag{4}$$

where h_x refers to layer thickness at the distance x from the mask edge, h_{edge} is the layer thickness adjacent to the mask, and h_{planar} indicates the thickness of the non-selectively deposited epitaxial layer under the same growth conditions. Equation (4) allows for the calculation of the effective diffusion length based on the measurements of the epitaxial material agglomeration in windows in the dielectric mask. By dividing both sides of Equation (4) by h_{planar}, an equation describing growth rate enhancement (GRE) at the distance x from the mask edge is obtained:

$$GRE_x = (GRE_{edge} - 1) \exp\left(-x \cdot \lambda_{eff}^{-1}\right) + 1. \tag{5}$$

In order to maximize the GRE value difference, window half-width as the distance from the mask edge was chosen:

$$GRE_{center} = (GRE_{edge} - 1) \exp\left(-w \cdot (2\lambda_{eff})^{-1}\right) + 1. \tag{6}$$

The effective diffusion length λ_{eff} can be then calculated by

$$\lambda_{eff} = -\frac{w}{2 \ln\left(\frac{GRE_{center}-1}{GRE_{edge}-1}\right)} = -\frac{w}{2 \ln(\gamma)} \tag{7}$$

where

$$\gamma = \frac{GRE_{center} - 1}{GRE_{edge} - 1}. \tag{8}$$

The effective diffusion length has been estimated so far either by calculation while using the Hara Equation (4) [10,16,18] or by fitting mathematical models to the experimental data (simulations) [4–6,8,9,11,14,17]. Published research overwhelmingly focused on the selective epitaxy of GaAs and its ternary compounds. This paper presents a new method for the estimation of the precursor molecules diffusion length according to the relative height difference between the edge and center of the grown heterostructure.

2. Materials and Methods

The test structures were deposited on GaN/sapphire templates while using an AIXTRON CCS 3 × 2″ epitaxial system. Figure 1 shows the layers scheme of the investigated structures. An undoped GaN buffer layer with a total thickness of 1950 nm was grown prior to selective epitaxy. Trimethylgallium (TMGa) and ammonia (NH_3) with different molar ratios were used as precursors for GaN growth with H_2 as a carrier gas. Next, a 400 nm thick SiO_2 mask was deposited by PECVD (plasma enhanced chemical vapour deposition), followed by UV photolithography. The selective epitaxy of AlGaN/GaN heterostructures with AlN cladding and cap layers was conducted at 1060 °C and pressure of 10 kPa with NH_3 flow of 67 mmol·min^{-1}, and TMGa and TMAl flow of 65 µmol·min^{-1}

and 8.6 µmol·min^{-1}, respectively. The selected conditions ensured that the epitaxial layer was deposited in the mass-transport limited growth regime [23]. Three samples differing in GaN thickness (150 nm, 250 nm, and 500 nm) were successfully fabricated. Epitaxial lateral overgrowth was not observed.

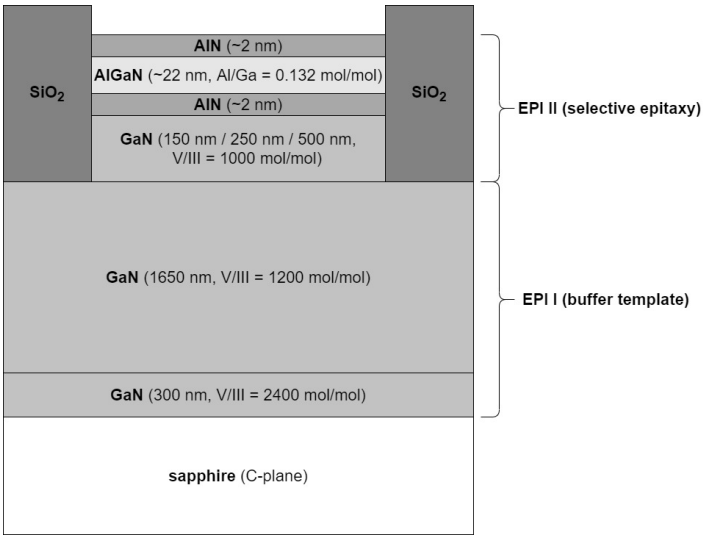

Figure 1. Layer scheme of the investigated structures.

Figure 2 presents the configuration of the SiO_2 mask. Selective epitaxy was conducted in windows of different width w (from 5 µm to 160 µm) and length of 200 µm. The distance between windows (mask width m) varied from 5 µm to 40 µm. The rectangular heterostructure deposited selectively between two dielectric masks could be used as the active region of a high electron mobility transistor [24].

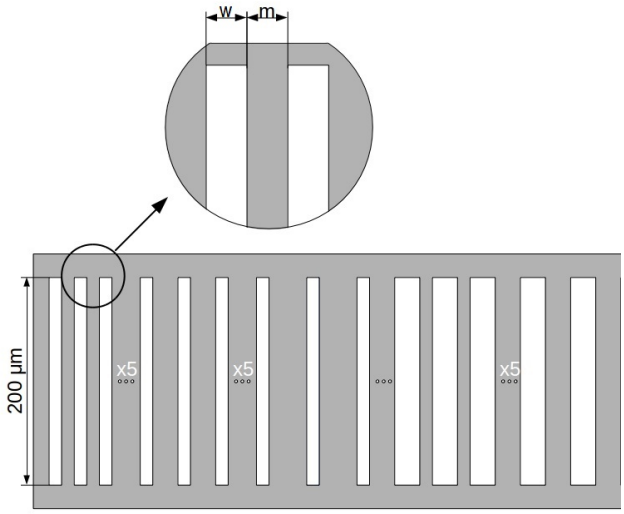

Figure 2. Configuration of the dielectric mask (m) and open windows (w).

The measurements of the epitaxial material agglomeration in windows in the dielectric mask were conducted while using Taylor Hobson Talysurf CCI optical profilometer. Coherence correlation interferometry was used as a measurement technique with 0.01 nm vertical and 0.6 µm lateral resolution. The layers profile has been determined after the removal of the dielectric mask. The whole structure was covered with a 10 nm layer of gold in order to increase the measurement accuracy. This caused an increase in the reflection coefficient and reduction of the optical beam interference

on the heterostructure. Additional measurements were performed while using Bruker Multimode V Atomic Force Microscope for measurements accuracy comparison. The data presented in this study are available in the Supplementary Materials. Measurement data have been divided into three sets depending on the thickness of the GaN layer (150 nm, 250 nm and 500 nm).

3. Results and Discussion

Figure 3 shows a part of the AlGaN/GaN heterostructure profile with the 500 nm thick GaN layer. The abscissa axis shows the profile width, whereas the ordinate axis shows the profile height relative to the GaN buffer layer surface. Increased material accumulation adjacent to the dielectric mask was observed. Fluctuations in the material growth rate at the mask edge were evaluated in dependence of the surface of the masked and exposed area, based on the obtained profiles. The overall layer profile was assembled of fragments that were measured separately. A separate calibration of the structure height reference point was conducted for each part. This resulted in a nonuniform buffer surface layer level that is visible in Figure 3. Additionally, the substrate deformed due to stresses that arose in the deposited layer.

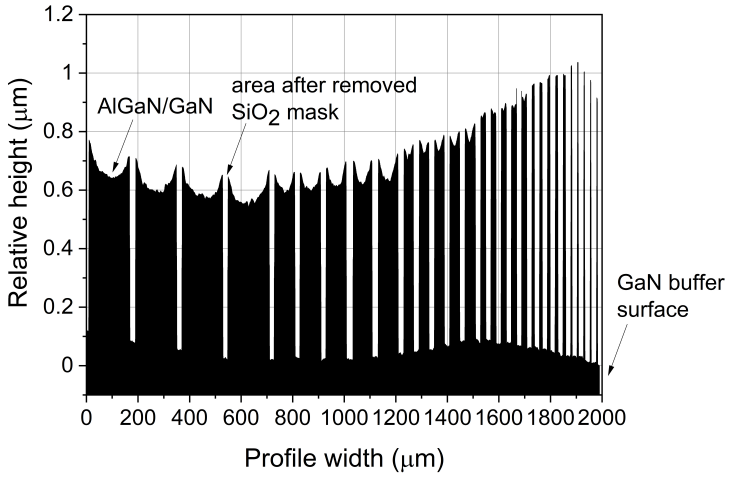

Figure 3. Part of the AlGaN/GaN heterostructure profile with 500 nm thick GaN layer.

The following parameters were calculated for each window separately (Figure 4) in order to eliminate measurement errors that result from substrate deformation:

- average structure height adjacent to the mask h_{edge} as a mean of structure height relative to the bottom of the mask on the left h_{el} and right h_{er} side of the structure;
- average structure height at the window center h_{center} as a mean of structure height relative to the bottom of the mask on the left h_{cl} and right h_{cr} side of the structure;
- window width w;
- average mask width m as a mean of mask width on the left m_l and right m_r side of the window; and,
- edge growth factor σ as a relative height difference between h_{edge} and h_{center} (9).

$$\sigma = \frac{h_{edge}}{h_{center}} - 1[\%] \tag{9}$$

A detailed analysis of the measured profile was conducted for the sample with a 500 nm thick GaN layer. Figure 5 (variable window width) and Figure 6 (variable mask width) present growth rate enhancement as a function of location relative to the window center. The presented results are cross-sections of selected test structures. Figure 5 shows that, with increasing window width, for a constant mask width and layer thickness, the height of the epitaxial structure decreases significantly

and the edge growth factor increases. The average structure height at the window center for a 5 µm wide window is almost twice as large as for a 160 µm wide window. The shape of the profile is similar for different window widths. When reducing the size of the window, the structure edges are brought closer, without a significant change in the shape of the profile. For narrow windows ($w < 20$ µm), structure edges overlap, which results in a nearly uniform layer surface.

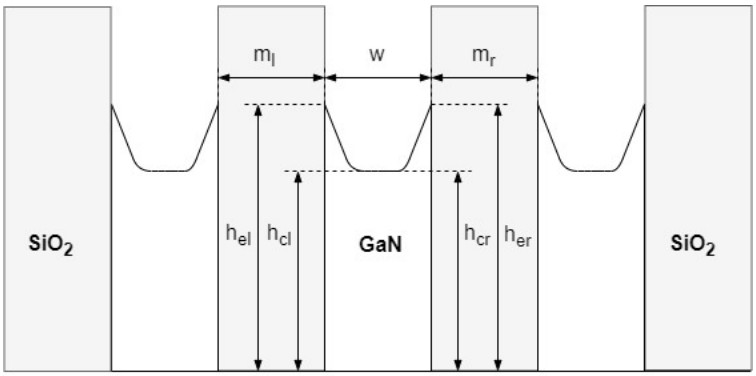

Figure 4. Parameters characterising the test structures.

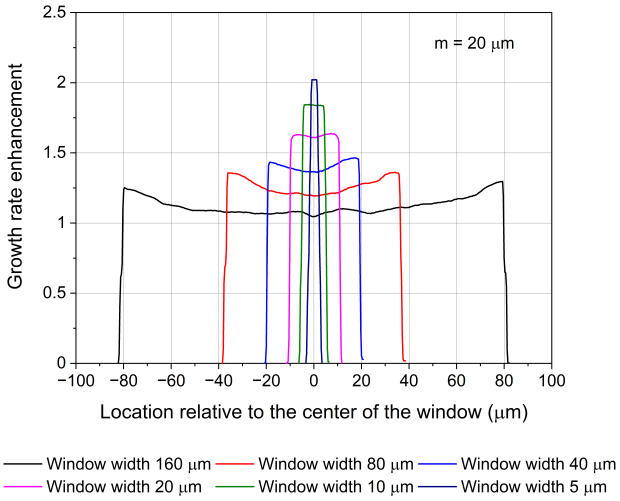

Figure 5. Growth rate enhancement (GRE) as a function of location relative to the window center (layer thickness 500 nm). Variable window width w, constant mask width m = 20 µm.

Figure 6 shows that, with increasing mask width, for a constant window width and layer thickness, the height of the epitaxial structure increases with a slight change in the shape of the profile.

The GRE of the epitaxial structure as a function of window width is presented in Figure 7 (adjacent to the mask) and in Figure 8 (in the window center). GRE decreases exponentially with increasing windows width. This agrees with previous findings by Tanaka [11], and it can be easily understood, as the same amount of material has to be deposited on a larger area. The vertical dimensions of the layer are also affected by the surrounding mask width. The structure height increases with increasing mask width. All of the approximation curves were fitted to the measurement data while using orthogonal distance regression method with the value of the adjusted R-squared over 0.99.

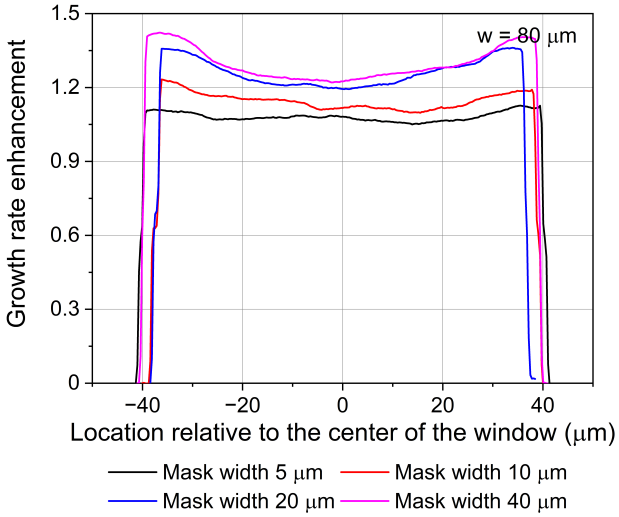

Figure 6. GRE as a function of location relative to the window center (layer thickness 500 nm). Variable mask width m, constant window width w = 80 μm.

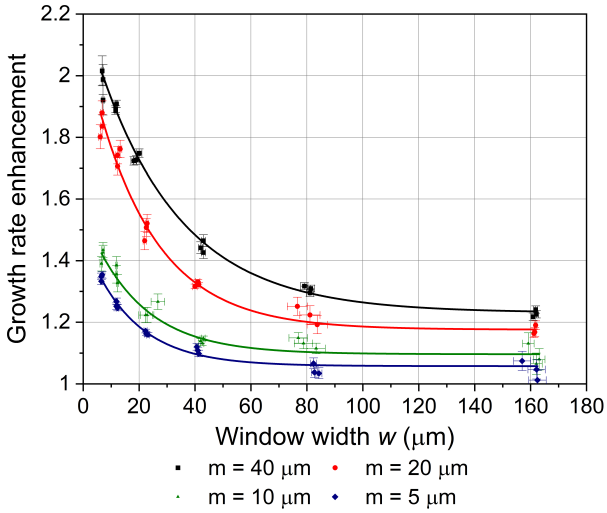

Figure 7. GRE as a function of the window width adjacent to the mask $GRE_{edge} = f(w)$ (layer thickness 500 nm).

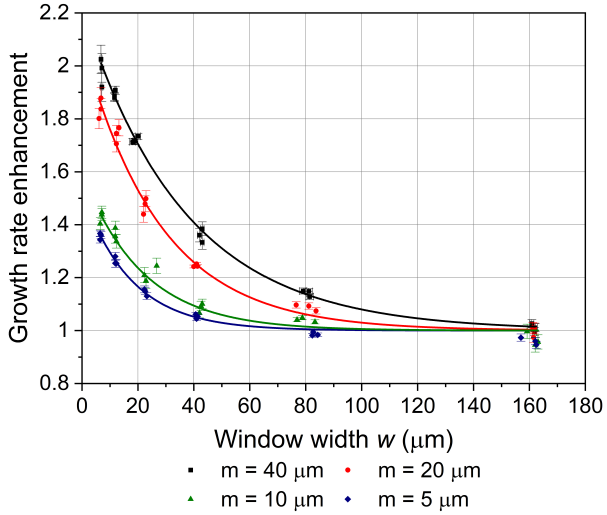

Figure 8. GRE as a function of the window width in the window center $GRE_{center} = f(w)$ (layer thickness 500 nm).

The relation between GRE and window width can be expressed as (10)

$$GRE(w) = GRE_0 + GRE_{ex} \cdot \exp\left(-\lambda_{eff}^{-1} \cdot w\right) \tag{10}$$

where GRE_0 refers to the minimal growth rate enhancement for a window width much greater than the effective diffusion length ($w \gg \lambda_{eff}$), and GRE_{ex} is the excess growth rate enhancement dependent on the window width. The effective diffusion length λ_{eff} defines the steepness of the relation between the GRE and the window width. Greater λ_{eff} means that the epitaxial material diffusing from the mask will be distributed over a larger area. Table 1 depics the values of GRE_0, GRE_{ex}, and λ_{eff} for different mask widths. Error margins have been estimated as the statistical error of the orthogonal distance regression method.

The sensitivity matrix $\boldsymbol{X}$ (11) has been calculated in order to analyse the influence of the parameters GRE_0, GRE_{ex}, and λ_{eff} on the absolute growth rate enhancement

$$\boldsymbol{X} = \frac{\partial \boldsymbol{GRE(w)}}{\partial \boldsymbol{\theta}} \tag{11}$$

where $\boldsymbol{\theta}$ is a vector of parameters: GRE_0, GRE_{ex}, and λ_{eff}. The values of sensitivity to particular parameters may vary significantly, thus the dimensionless normalized sensitivity matrix $\boldsymbol{X_n}$ (12) was calculated by the multiplication of sensitivity matrix $\boldsymbol{X}$ and normalization diagonal matrix $\boldsymbol{D_n}$

$$\boldsymbol{X_n} = \boldsymbol{X}\boldsymbol{D_n}. \tag{12}$$

Matrix $\boldsymbol{D_n}$ satisfies the Equation (13)

$$\boldsymbol{D_n} = \left(\left(\boldsymbol{X}^T\boldsymbol{X}\right) \circ \boldsymbol{I}\right)^{-0.5} \tag{13}$$

where $\boldsymbol{I}$ is the identity matrix and $\circ$ denotes the Hadamard product. Normalized sensitivity to GRE_0, GRE_{ex}, and λ_{eff} as a function of window width, for a constant mask width $m = 40$ µm, is presented in Figure 9. GRE at the window edge was considered. The value of GRE_0 is independent of window width and it has a dominant influence on growth rate enhancement for windows that are much broader than the effective diffusion length ($w \gg \lambda_{eff}$) (14)

$$\lim_{w \to \infty} GRE(w) = GRE_0. \tag{14}$$

Window center will not be affected by lateral diffusion provided that $w \gg \lambda_{eff}$, thus $GRE_0 = 1$ at the window center.

Excess growth rate enhancement GRE_{ex} has the greatest impact on absolute GRE for windows that are narrower than effective diffusion length. It is related to the constant amount of material that has to be deposited on a variable surface area. Reducing window width leads to higher GRE, as the same amount of epitaxial material has to be deposited on a smaller area (15)

$$\lim_{w \to 0} GRE(w) = GRE_0 + GRE_{ex} \tag{15}$$

Effective diffusion length influences GRE the most for a window width equal to λ_{eff}.

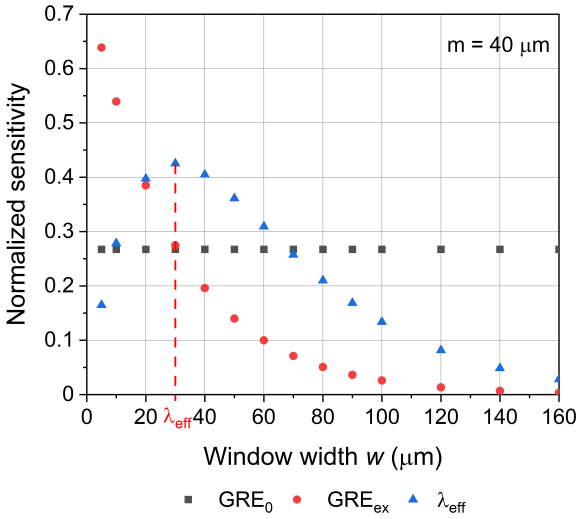

Figure 9. Normalized sensitivity of GRE to GRE_0, GRE_{ex} and λ_{eff} as a function of window width, for a constant mask width $m = 40$ μm (at the window edge).

Figure 10 presents the γ ratio as a function of window width. For windows that are narrower than 20 μm, γ is equal to one. This indicates uniform growth within the whole window area, as the structure height at the window edge is equal to the structure height at the window center. Because of this, Hara Equation (4) cannot be used for estimating the effective diffusion length in this range ($w < \lambda_{eff}$). For wide windows, γ approaches zero. It means that layer at the window center is equal in height to the layer deposited non-selectively, thus window center was not affected by mass diffusing from the dielectric mask.

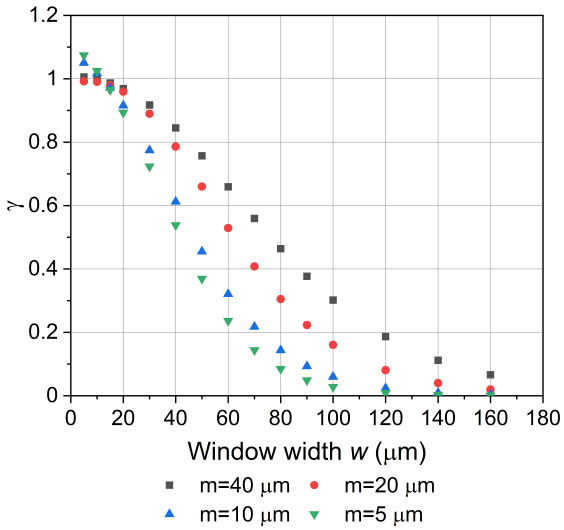

Figure 10. $\gamma = \frac{GRE_{center}-1}{GRE_{edge}-1}$ ratio as a function of window width $\gamma = f(w)$.

Figure 11 presents the effective diffusion length that was calculated using the Hara Equation (4) for different window and mask widths. Window widths that were smaller than 20 μm were not included. It can be easily seen that λ_{eff} calculated while using Equation (4) depends on both window and mask width. Effective diffusion length decreases exponentially with an increasing window width. Offset values for different mask widths are within error margin of λ_{eff} estimated while using Equation (10) at the window edge, thus Equation (10) is coherent with Equation (4) and Equation (4) should be used only to windows that are much wider than the exact value of the effective diffusion length (here: $w > 4\lambda_{eff}$). Table 1 illustrates the offset values. For similar process conditions, λ_{eff} of

about 30 µm has been reported [4,11,25]. It is expected that the effective diffusion length will decrease with decreasing temperature [4,9,19,25] and increasing pressure [4,5,9,19,25]. Similarly, an increase in the temperature causes an increase in the effective diffusion length [4,8,25]. Therefore, the calculated values of the effective diffusion length are in agreement with previous reports.

Table 1. Estimated parameters of the $GRE = f(w)$ relation at the window edge and at the window center for different mask widths.

	Window Edge			Window Center			Hara Equation
m (µm)	GRE_0 **(-)**	GRE_{ex} **(-)**	λ_{eff} **(µm)**	GRE_0 **(-)**	GRE_{ex} **(-)**	λ_{eff} **(µm)**	λ_{eff} **(µm)**
40.00 ± 1.29	1.23 ± 0.01	0.98 ± 0.02	29.64 ± 1.53	1	1.22 ± 0.02	36.71 ± 0.89	32.07 ± 1.71
20.00 ± 1.47	1.18 ± 0.01	0.93 ± 0.04	22.19 ± 1.08	1	1.09 ± 0.04	27.81 ± 0.88	22.74 ± 1.12
10.00 ± 1.40	1.10 ± 0.01	0.46 ± 0.03	19.23 ± 2.51	1	0.60 ± 0.04	21.67 ± 1.95	16.34 ± 0.80
5.00 ± 0.83	1.06 ± 0.01	0.41 ± 0.02	17.02 ± 1.34	1	0.53 ± 0.03	17.34 ± 1.23	13.02 ± 0.65

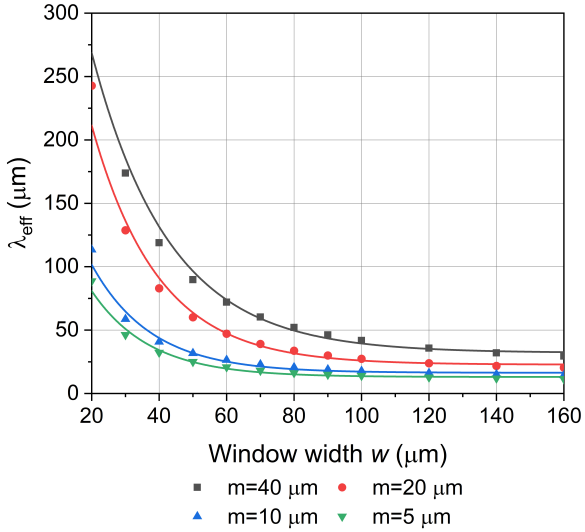

Figure 11. Theoretical effective diffusion length as a function of window width, for different mask widths $\lambda_{eff} = f(w)$ (Hara Equation (4)).

Figure 12 presents the effective diffusion length that was calculated using Equation (10) at the window edge and center as a function of the mask width. Both of the relations are linear and they share the same intercept equal to 15 µm that can be interpreted as the lateral vapour diffusion length of Ga λ_{Ga}, independent of the mask configuration and structure geometry. Slopes of approximation lines are equal to 0.5 μm^{-1} and 0.3 μm^{-1} for the window center and window edge, respectively. Therefore, Equation (10) can be transformed into Equations (16) and (17).

$$GRE(w) = GRE_0 + GRE_{ex} \cdot \exp\left(-(\lambda_{Ga} + 0.3m)^{-1} \cdot w\right) \ (at\ the\ window\ edge) \quad (16)$$

$$GRE(w) = GRE_0 + GRE_{ex} \cdot \exp\left(-(\lambda_{Ga} + 0.5m)^{-1} \cdot w\right) \ (at\ the\ window\ center) \quad (17)$$

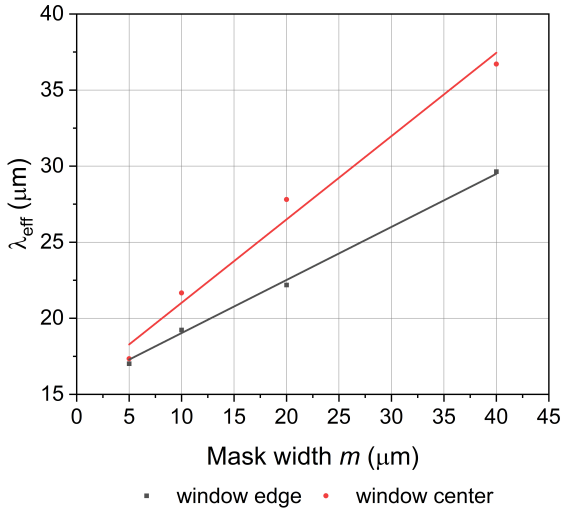

Figure 12. Effective diffusion length at the window edge and the window center as a function of the mask width $\lambda_{eff} = f(m)$.

Figure 13 presents the edge growth factor as a function of window width. It can be seen that the larger the window width and the greater the distance between windows, the greater the difference in structure height between the edge and the window center. This effect is also visible in Figure 3, showing the layer altitude profile. An increased agglomeration of epitaxial material adjacent to the mask may not be observed for narrow windows, while more intense layer growth will be seen throughout the entire window area. This increase will be faster for smaller window area and larger mask area.

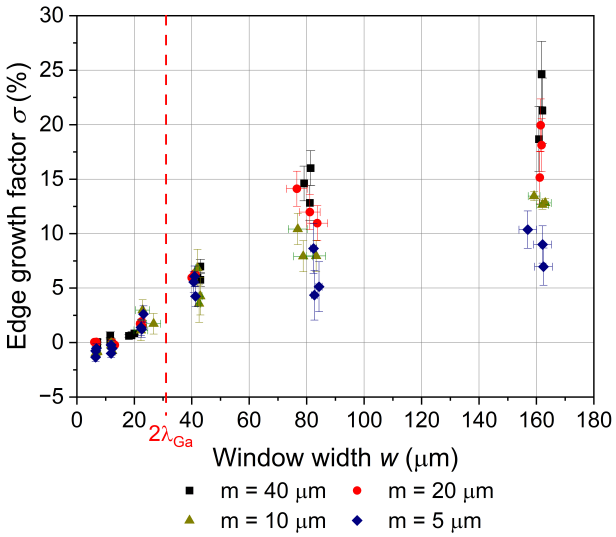

Figure 13. Edge growth factor as a function of window width $\sigma = f(w)$ (layer thickness 500 nm).

Uniform layer growth will be observed, provided that the distance between the mask center and window center will be smaller than the effective diffusion length (18)

$$0.5m + 0.5w < \lambda_{eff}. \tag{18}$$

When considering Equation (17), this condition can be expressed as

$$w < 2\lambda_{Ga}. \tag{19}$$

Figure 13 marks a value of $2\lambda_{Ga}$. It can be seen that, for a window width smaller than $2\lambda_{Ga}$, nearly uniform layer growth was observed. In order to compare measurement accuracy, a heterostructure with a 250 nm thick GaN layer was additionally profiled while using atomic force microscope (AFM). Edge growth factor as a function of window width calculated using different profiling methods is presented in Figure 14. Optical profilometer and AFM both have similar accuracy regarding window widths satisfying the condition (19).

GRE as a function of location relative to the window center for a constant window and mask width and different nominal GaN layer thickness is presented in Figure 15. Figure 16 presents the edge growth factor as a function of the mask surface to the window surface ratio for three different GaN layer thicknesses. Figures 15 and 16 suggest that GRE is independent of the structure thickness, thus growth uniformity cannot be achieved by the modification of the deposition time or the mask configuration. The edge growth factor can be minimised by selection of the sufficiently narrow dielectric mask, but uniform front of crystallization for a constant window width can only be achieved by modification of the diffusion length of precursor molecules. This can be achieved by a variation of the process parameters, such as temperature or pressure [4].

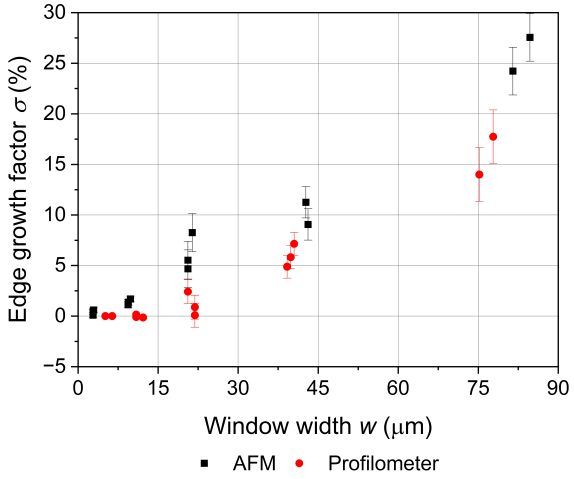

Figure 14. Edge growth factor as a function of window width $\sigma = f(w)$ (layer thickness 250 nm); comparison of optical profilometer and atomic force microscope (AFM).

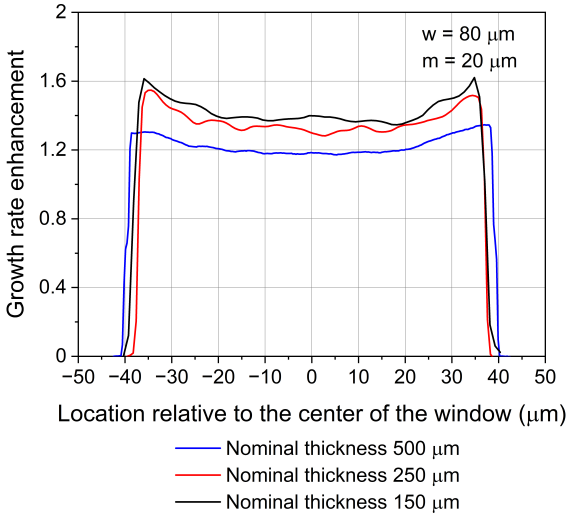

Figure 15. GRE as a function of location relative to the window center. Variable nominal GaN layer thickness, constant window width w = 80 μm, and mask width m = 20 μm.

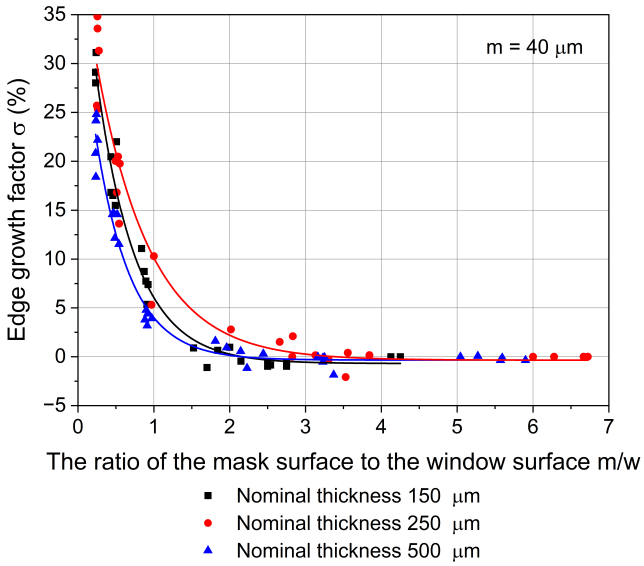

Figure 16. Edge growth factor as a function of the mask surface to the window surface ratio $\sigma = f(\frac{m}{w})$. Constant mask width $m = 40$ μm.

4. Conclusions

Control of the growth uniformity in selecive area epitaxy is a crucial aspect regarding the fabrication of the modern semiconductor devices. It applies to both the structure profile and compositional gradient. In this paper, a uniform front of crystallization of AlGaN/GaN heterostructure was achieved by the selection of the window half-width smaller than the Ga diffusion length of 15 μm. Ga diffusion length was estimated at 1060 °C and a pressure of 100 mbar based on the relative height difference between the edge and the center of the grown heterostructure. It was presented that uniform layer growth cannot be achieved by the modification of the mask configuration or the deposition time.

Supplementary Materials: Measurement data are available online at http://www.mdpi.com/2079-9292/9/12/2129/s1 .

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Conflicts of Interest: The authors declare no conflict of interest.

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Review

High Pressure Processing of Ion Implanted GaN

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Abstract: It is well known that ion implantation is one of the basic tools for semiconductor device fabrication. The implantation process itself damages, however, the crystallographic lattice of the semiconductor. Such damage can be removed by proper post-implantation annealing of the implanted material. Annealing also allows electrical activation of the dopant and creates areas of different electrical types in a semiconductor. However, such thermal treatment is particularly challenging in the case of gallium nitride since it decomposes at relatively low temperature (~800 °C) at atmospheric pressure. In order to remove the implantation damage in a GaN crystal structure, as well as activate the implanted dopants at ultra-high pressure, annealing process is proposed. It will be described in detail in this paper. P-type GaN implanted with magnesium will be briefly discussed. A possibility to analyze diffusion of any dopant in GaN will be proposed and demonstrated on the example of beryllium.

Keywords: ion implantation; gallium nitride; thermodynamics; ultra-high-pressure annealing; diffusion; diffusion coefficients

1. Introduction

Electronic devices prepared by GaN-on-GaN technology are still at the beginning of their road to commercialization. Two different technologies can be applied for preparing GaN-on-GaN vertical devices (e.g., metal–oxide–semiconductor field-effect transistor (MOSFET)). The structure can be grown by epitaxial techniques with some procedures, such as regrowth and/or etching, needed due to the device architecture, or by ion implantation [1,2]. The latter approach seems to be much less demanding and more perspective. The implantation process has been commonly applied in semiconductors for selective area n- and p-type doping. Such approach allows one to reduce the device size and to control the electric field configuration in devices. However, the implantation process destroys the crystal structure of the material. In order to rebuild it, appropriate (for a given compound) temperature treating is required. The temperature required to remove the damage is around 50–70% of the melting temperature of a given compound [3]. Temperature treatment is also important in order to activate the

implanted ions [4–6]. In case of Mg, the sole process of implantation of ions into GaN does not result in p-type conductivity at room temperature [7]. The reason for this is not only the rather high ionization energy of Mg in GaN. The implantation process results in introducing defects that compensate the implanted dopant. It was assumed that they were nitrogen vacancies. Uedono et al. showed that these defects were coupled gallium and nitrogen vacancies [8]. It was also presented that annealing at temperature higher than 1100 °C allows one to decrease the defect density. It should be stressed that GaN loses its thermal stability close to 800 °C at atmospheric pressure [9]. Therefore, annealing it at higher temperature results in surface decomposition. It is possible to apply an AlN capping layer in order to protect the surface. However, it was suggested that during annealing vacancy-type defects agglomerate near the interface between the AlN cap and GaN [8]. Therefore, the best approach is to avoid using a capping layer. One of the possible solutions is to anneal implanted GaN at much higher temperature but, then, also at high nitrogen pressure. Such technology is called the ultra-high-pressure annealing (UHPA). UHPA is strictly derived from the well-known high nitrogen pressure solution (HNPS) growth technology of GaN [10]. First GaN monocrystals of the highest structural quality were obtained by the HNPS method [11]. They were grown from a solution of atomic nitrogen in liquid gallium (Ga) at temperature of the order of 1500 °C and nitrogen (N_2) pressure of 1 GPa. If Ga is removed from such a system, it is possible to anneal any material in the temperature and pressure conditions described above. This is the foundation of the UHPA technology. Today, it serves to anneal implanted GaN (see, e.g., [12–16]) as well as different kinds of glasses and foams (see, e.g., [17–21]).

In this paper, the basis of applying the UHPA technology only for GaN is described. At the beginning, the thermodynamics of this process is briefly explained. Next, the UHPA configuration is presented and analyzed. P-type GaN implanted with magnesium (Mg) is discussed based on recent results obtained in cooperation with Nagoya University in Japan. Then, application of the UHPA technology for analyzing the diffusion mechanism of beryllium (Be) in GaN is demonstrated. It is treated as a case study since the presented approach allows one to examine the diffusion of any element in GaN. A summary is given at the end of this paper.

2. Thermodynamic Basics

In 1984, Karpinski et al. [9] determined the pressure–temperature (p–T) equilibrium curve for the GaN-Ga-N_2 system. This curve is presented in Figure 1a. The p–T area where GaN exists is clearly seen. Figure 1b shows the Gibbs free energy (G) as a function of temperature for GaN and its constituent, N_2 [11]. With increasing temperature, the G curves decrease. It happens faster in the case of N_2. Thus, at atmospheric pressure at around 800 °C, the G curves for GaN and N_2 intersect and GaN loses its thermodynamic stability. Increasing the N_2 pressure shifts the Gibbs free energy of nitrogen into higher ranges, according to the equation:

$$G = U + pV\text{-}TS \quad (1)$$

where U represents the internal energy, V-volume, and S-entropy.

Then, the stability region of GaN is extended. Thus, high nitrogen pressure (in fact nitrogen activity) stabilizes the existence of GaN at higher temperature. It should be, however, remembered that GaN is a binary compound and at very high temperature Ga vapor pressure is also required to secure GaN against decomposition.

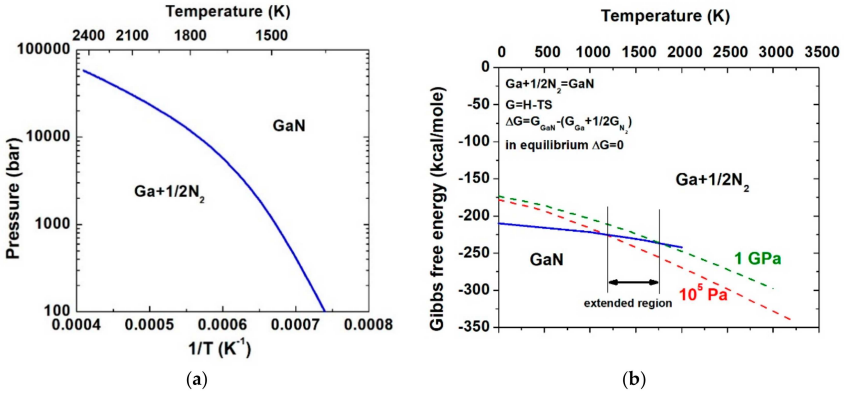


Figure 1. (**a**) Experimental p–T equilibrium curve for the GaN-Ga-N_2 system [9]; (**b**) Gibbs free energy (G) for GaN and N_2; visible temperature shift of GaN stability area if N_2 pressure is increased [11].

3. Ultra-High-Pressure Annealing Process

During the UHPA process, a GaN sample is placed in a crucible. The crucible is then positioned in a resistive furnace and in a high-pressure reactor. In such a configuration, annealing of GaN at nitrogen rich conditions can be performed. If no changes are introduced, the compound will only have contact with the N_2 gas phase. However, as already mentioned, Ga vapor might be needed for protecting GaN against decomposition during annealing at relatively high temperature. The presence of Ga vapor can be provided in two ways: (1) the GaN sample is covered by GaN powder; (2) the GaN sample is placed close to a Ga droplet. The first solution bases on the assumption that the GaN powder decomposes faster than the GaN sample and, therefore, Ga vapor is above the annealed sample. The second way is more elegant and bases on the assumption that the Ga droplet evaporates and, therefore, Ga vapor is close to the surface of the annealed sample. In this paper, examination of the three described configurations: only in N_2, with GaN powder, and with a Ga droplet, will be presented. They are shown in Figure 2. For each UHPA process, two GaN samples of high structural quality were prepared: one with the (0001) surface and the second one with the (000-1) surface prepared to an epi-ready state. Figure 3 shows atomic force microscopy (AFM) images of the mentioned surfaces. In both cases, values of the root mean square (RMS) were lower than 0.1 nm. GaN samples grown by halide vapor phase epitaxy (HVPE-GaN) were used (for details see [22]). This material is characterized by high structural quality with threading dislocation density of the order of 5×10^4 cm^{-2}, flat crystallographic planes (bowing radius higher than 20 m) as well as high purity (donor and acceptor concentration lower than 10^{17} cm^{-3}).

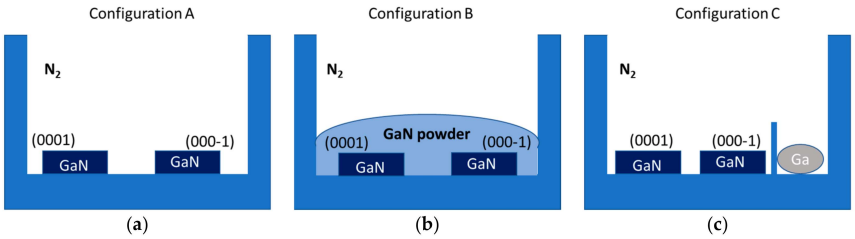
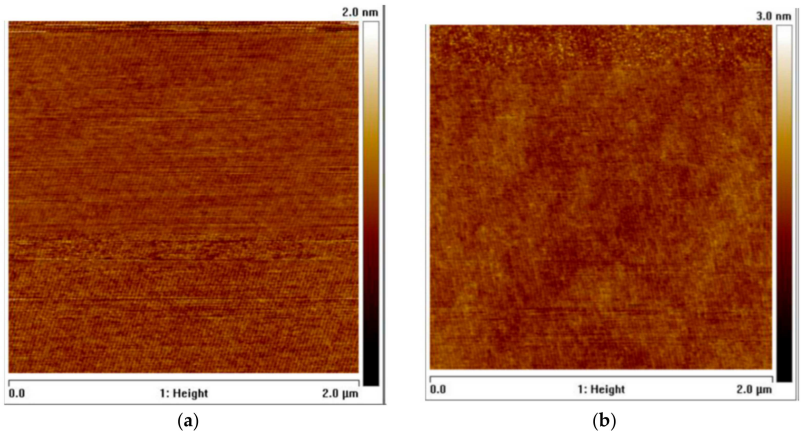


Figure 2. Three configurations for annealing HVPE-GaN samples with exposed (0001) and (000-1) surfaces: (**a**) in N_2 rich conditions; samples have direct contact only with N_2 (configuration A); (**b**) covered by polycrystalline GaN powder (configuration B); (**c**) close to Ga droplet (configuration C); the samples are placed in a crucible (represented by blue box in the figure), resistive heater and high pressure autoclave (reactor).

Figure 4 demonstrates AFM images of the samples' surfaces after annealing at 1400 °C under N_2 pressure of 0.7 GPa for 15 min. A lower value of RMS (of the order of 0.5 nm) was noted for samples covered with GaN powder. Multiple atomic steps were clearly visible. The samples

annealed at nitrogen rich conditions and placed close to the gallium droplet (configurations A and C in Figure 2, respectively) demonstrated higher RMS close to 1 nm. In the case of samples annealed in configuration A, Ga droplets and pinholes were detected. The samples annealed in configuration C showed areas without steps but with small beads. These results showed that only annealing in configuration B did not lead to GaN surface decomposition. Thus, this configuration was chosen for annealing implanted GaN.



(**a**) (**b**)

Figure 3. AFM images of HVPE-GaN surfaces: (**a**) (0001); (**b**) (000-1); RMS = 0.1 nm.

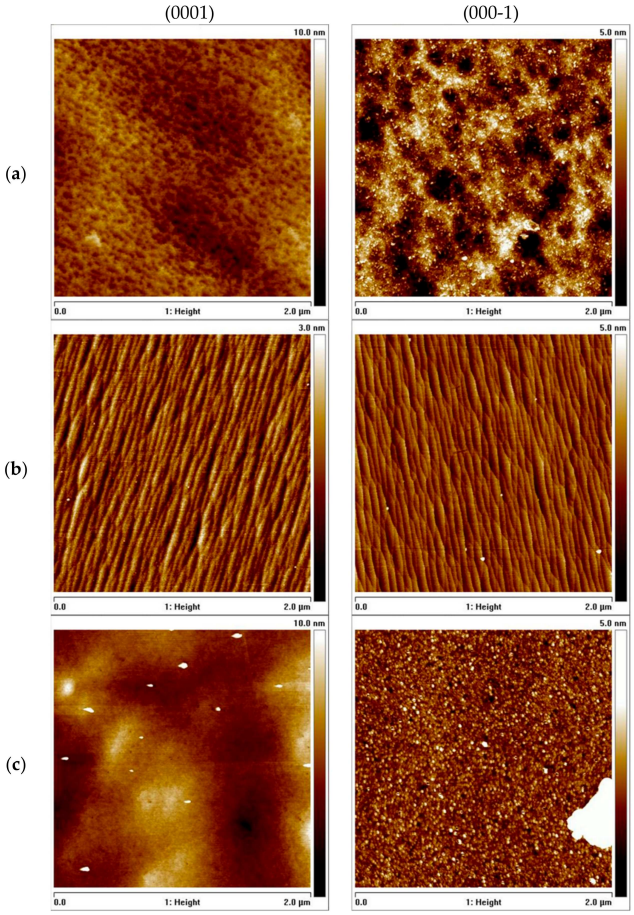
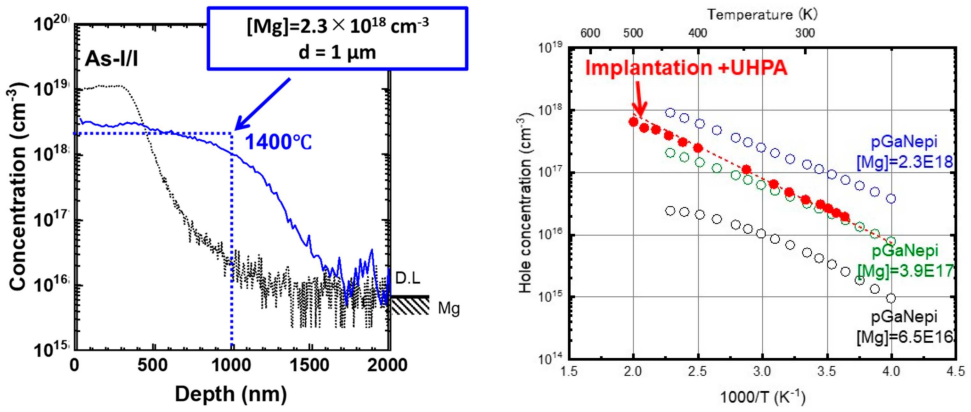


Figure 4. AFM images of the samples' surfaces: (0001)—left column and (000-1)—right column, respectively, annealed in three configurations presented in Figure 2; annealing: (**a**) configuration A—only in N_2; (**b**) configuration B—covered by GaN powder; (**c**) configuration C—with Ga droplet close to the samples' surfaces.

4. P-Type GaN by Mg Implantation

As mentioned, the implantation process has been commonly applied for controlling the selective area doping of both n- and p-type regions, which allow one to reduce the device size and control the electric field configuration in devices. In the case of GaN, high n-type carrier concentration has already been demonstrated by using a relatively large ion dosage [4,23]. Obtaining highly conductive p-type after ion implantation still remains a challenge. Recently, a very effective activation by UHPA of Mg-implanted p-type GaN has been announced [24]. Investigating Mg diffusion during the UHPA process also started [25–27].

Magnesium was implanted into n-type GaN deposited by metalorganic vapor phase epitaxy (MOVPE). The 2-µm-thick MOVPE layer was grown on an HVPE-GaN substrate. The ion implantation process was performed at room temperature. A 300-nm-deep box-shaped profile with Mg concentration of 10^{19} cm^{-3} was obtained. The UHPA process was performed at 1400 °C for 5 min under N_2 pressure of 1 GPa. The sample was covered by polycrystalline GaN powder. Figure 5a shows Mg profiles after implantation and after annealing. The diffusion of Mg into the sample (up to 1 µm) was observed. The average Mg concentration in a 1-µm-thick layer was of the order of 10^{18} cm^{-3}. AC Hall measurements, described in detail in [24], demonstrated that the layer is p-type GaN with hole concentration of 10^{17} cm^{-3} and mobility 25 cm^2 V^{-1} s^{-1} at room temperature (see Figure 5b). A comparison of electrical results between the p-type GaN resulting from implantation followed by UHPA and an MOVPE-GaN layer doped with Mg [28] showed that the same results can be obtained by both methods.



(**a**) (**b**)

Figure 5. (**a**) Comparison of Mg profile after implantation and UHPA; (**b**) temperature-dependent hole concentration for samples processed by Mg ion implantation and UHPA compared to MOVPE-GaN doped with Mg; modified from Sakurai et al. [24] with permission of AIP Publishing.

No doubt, achieving efficient p-type conductivity in Mg-implanted GaN depends on post-implantation annealing conditions. Up to now, p-type GaN with 70% activated Mg atoms was obtained only by UHPA at 1400 °C [24]. Conventional annealing at atmospheric pressure and 1300 °C (with an AlN cup sputtered on GaN surface) allowed us to obtain activation of Mg atoms at the level of 25% [2]. Additionally, atomic-resolution transmission electron microscopy analysis showed that interstitial-type extended defects and inversion domains with Mg segregation formed during the conventional annealing [29]. These defects are not observed in the samples treated by UHPA [26,27].

5. Diffusion Mechanism of Beryllium in GaN—Case Study

As can be remarked, the UHPA leads to diffusion of implanted dopants in GaN. It seems that such experiments allow one to analyze the diffusion phenomenon in GaN and determine the diffusion coefficients of any dopant. In what follows, we will analyze the diffusion of Be in GaN. Unintentionally

doped HVPE-GaN layers deposited on ammonothermal GaN substrates [30] were used as samples for ion implantation. Implantation of Be ions was performed with a dose of 2.9×10^{15} cm^{-2} at energy of 200 keV, without the use of a through film and at room temperature. UHPA was applied as post-implantation annealing. It was performed at nitrogen pressure of 1 GPa, temperature varying in the range 1200–1400 °C and for two different times: 15 and 30 min.

Secondary ion mass spectrometry (SIMS) measurements allowed us to examine the depth profiles of Be. Results for samples as-implanted and annealed for 15 and 30 min are presented in Figure 6. Only Be profiles are shown. No significant changes were observed in the case of other elements. Concentrations of oxygen and silicon in HVPE-GaN used for implantation were lower than 10^{17} cm^{-3}. It should be noted that all other elements apart from Be, especially atmospheric impurities like hydrogen and carbon, were below the SIMS background level. The data presented in Figure 6 indicate that: (1) the detection limit of Be is 10^{15} cm^{-3}; (2) annealing at 1200 °C and 1400 °C changes the Be profile; Be reaches the depth of 8 μm at 1400 °C; (3) diffusion profiles exhibit a characteristic kink (marked in Figure 6); (4) in the sample annealed at 1400 °C, the Be reservoir remains at the depth of the maximum concentration of the as-implanted sample; it indicates that the top of the layer, around 1 μm from the surface, can be regarded as an infinite source of Be dopant for all annealing conditions.

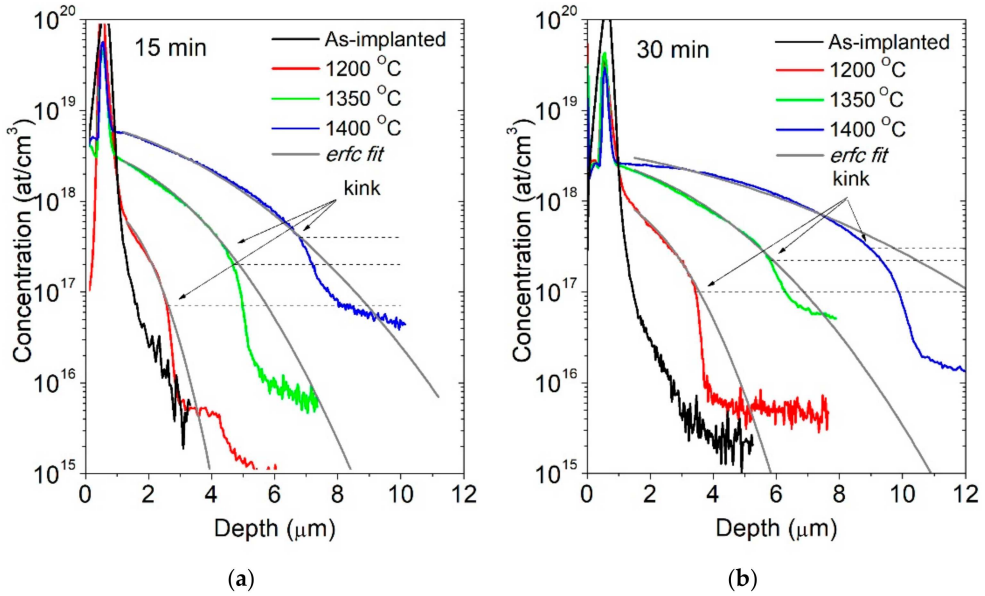


Figure 6. Results of SIMS measurements. Be depth profiles for samples as-implanted and annealed in the temperature range 1200 °C–1400 °C for: (**a**) 15 min; examples of the kink are marked, (**b**) 30 min; gray curves are error function (erfc) function fitting; black dotted lines indicate the concentration level of the kink in the profile.

If an infinite source of a species is used, the diffusion profiles (concentration C of the examined species) are described by a complementary error function (erfc):

$$C(x,t) = C_S erfc\left(\frac{x}{\sqrt{4Dt}}\right) \quad (2)$$

where C_S is the maximum concentration of the diffused species, corresponding to the surface concentration in the case of infinite source experiment; D is the diffusion coefficient; t is annealing time; x is the depth from the source of the species. Fitting curves were determined based on the erfc function. They are also presented in Figure 6. C_S and D were used as fitting parameters. Magnitudes of the diffusion coefficients obtained from the fitting of Equation (1) changed significantly from 4×10^{-12} cm^2 s^{-1} to 6×10^{-11} cm^2 s^{-1} for 1200 °C and 1400 °C, respectively. However, it is clearly

seen that the erfc relation is well fitted only to the upper parts of the SIMS profiles (above the characteristic kink). Therefore, the diffusion coefficients calculated in such a way are valid for high Be concentration. A drop (kink) in the Be depth profile appears at a certain Be concentration. This concentration increases when the annealing temperature rises. Such a deviation from the erfc fitting in the profile indicates a change in the diffusion coefficient. For a system, in which D of a species is concertation-dependent, the method described by Matano [31] is applied. According to this approach the standard Fick's law equation is transformed into:

$$\frac{\partial C}{\partial t} = \frac{\partial}{\partial x} D\left(\frac{\partial C}{\partial x}\right) \tag{3}$$

where t and x are time and depth variables, respectively.

A following variable: $\eta = x/t^{1/2}$, can be applied if the boundary conditions are known. This results in a dependence of concentration only on η instead of x and t. Then, the equation can be integrated with respect to η between $C = 0$ and $C = C_l$, where C_l is a specific value of concentration. Since the analyzed experimental profile is plotted for a specific diffusion time, t can be treated as constant when η is replaced by x and t. For C equal to 0, dC/dx is also equal 0. Therefore, the final equation for the diffusion coefficient is the following:

$$D\left(C^1\right) = -\frac{1}{2t}\left(\frac{dx}{dC}\right)\Big|_{C^1} \int_0^{C_1} x dC \tag{4}$$

This way, the diffusion coefficient for concentration C_1 can be derived from a dopant depth profile by transforming the plot from a $C(x)$ to $x(C)$ function and then integrating. Beryllium depth profiles transformed using Equation (4) are presented in Figure 7a,b for 15-min and 30-min annealing processes, respectively. The Matano method (also known as Boltzmann–Matano method [32]) allowed us to determine the diffusion coefficients for lower concentrations of Be, where there is a divergence between the erfc fit and the SIMS data. Values of the diffusion coefficients are indicated by lines in Figure 7.

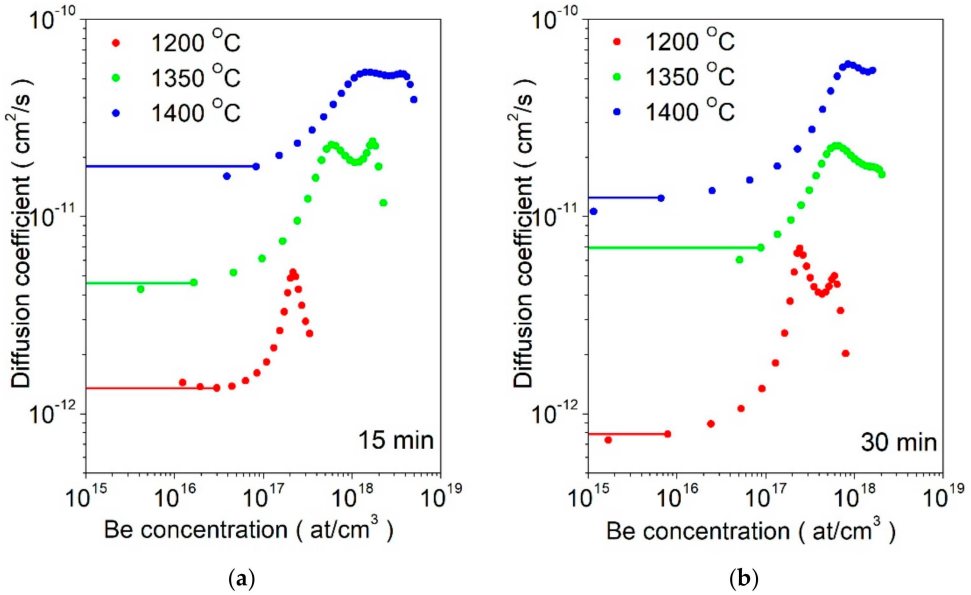


Figure 7. Matano analysis of Be depth profiles according to Equation (3) for samples annealed for: (**a**) 15 min and (**b**) 30 min; lines indicate the diffusion coefficients for low concentration of Be; two peaks are visible for high Be concentrations; they may result from the departure from the Matano analysis at the initial Be profile.

The diffusion coefficients calculated from Equation (2), based on the erfc fit and the ones derived from the Matano analysis for both annealing durations, are presented as a function of $1000/T$ in Figure 8. A classical Arrhenius equation was used to fit the dependence of the diffusion coefficients on inverse temperature:

$$D = D_0 exp\left(\frac{-E_A}{kT}\right) \tag{5}$$

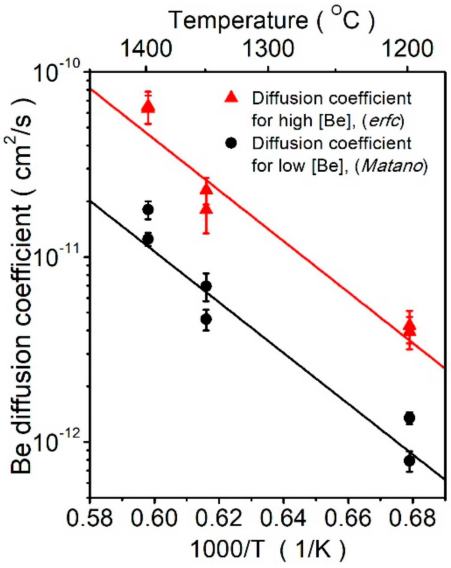


Figure 8. Diffusion coefficients of Be atoms in GaN as a function of inverse temperature; Arrhenius plot from erfc fitting (red filled triangles and line) and Matano analysis (black filled circles and line).

Results of such fitting, prepared for data from the erfc and Matano analysis, are also presented in Figure 8.

The temperature-independent pre-exponent factor D_0, as well as the activation energy for both Be diffusion mechanisms, was determined from Equation (2) using the erfc fitting and the Matano analysis. The results are presented in Table 1.

Table 1. Temperature-independent pre-exponent factor D_0 and the activation energy for the Be diffusion.

	Pre-Exponent Factor D_0 (cm^2 s^{-1})	**Activation Energy (eV)**
Higher Be concentration (erfc fitting)	$7.8 \pm 1 \times 10^{-3}$	2.73 ± 0.05
Lower Be concentration (Matano analysis)	$1.8 \pm 1 \times 10^{-3}$	2.72 ± 0.05

All the results presented in the above suggest two mechanisms, fast and slow, of Be diffusion in GaN. The first process is most probably a pure interstitial mechanism through octahedral lattice sites (for details, see [33]). The slower one is an interstitial–substitutional diffusion mechanism involving Ga vacancies and tetrahedral lattice sites. The ratio of atoms involved in both mechanisms depends on the concentration of Ga vacancies. Such a result shows that controlling the Ga vacancy concentration can influence the rate of diffusion of the Be dopant in GaN.

6. Summary

The UHPA technology and its application for GaN was presented. Different configurations of the annealing process were studied in order to prevent GaN surface, both (0001) and (000-1), from decomposition. The experiments performed at 1400 °C involved placing GaN samples in N_2 rich conditions, close to a Ga droplet, covered by polycrystalline GaN powder. Only the last configurations resulted in surfaces with visible atomic steps. Therefore, UHPA can be successfully applied for GaN

samples without the need to place a cap layer. The described annealing technology, preceded with Mg ion implantation, results in p-type GaN with the dopant activation exceeding 70% and electrical properties similar to those of MOVPE-doped GaN. This makes UHPA a very promising technology for fabricating devices with selectively doped areas. The high temperature applied in UHPA allows one to study the diffusion process of different elements in GaN. This was presented in the example of Be. Both the diffusion coefficients, as well as two different mechanisms of diffusion, were determined.

Author Contributions: K.S.—crystal growth experiments, UHPA experiments, characterization, preparing the manuscript; R.J.—SIMS measurements, theoretical analysis; B.L.—UHPA experiments, characterization; P.K.—UHPA experiments; M.I.—review and editing; M.T.—Be implantation; T.K., H.S.—Mg implantation, Hall and SIMS measurements, supervision, review and editing; M.B.—UHPA experiments, supervision, review and editing. All authors have read and agreed to the published version of the manuscript.

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Demonstration of AlGaN/GaN MISHEMT on Si with Low-Temperature Epitaxy Grown AlN Dielectric Gate

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Abstract: AlGaN/GaN metal-insulator-semiconductor high-electron-mobility transistors (MISHEMT) with a low-temperature epitaxy (LTE)-grown single crystalline AlN gate dielectric were demonstrated for the first time and the post-gate annealing effects at 400 °C were studied. The as-deposited LTE-AlN MISHEMT showed a maximum drain current (I_{Dmax}) of 708 mA/mm at a gate bias of 4 V and a maximum extrinsic transconductance (g_{mmax}) of 129 mS/mm. The 400 °C annealed MISHEMT exhibited an increase of 15% in g_{mmax}, an order of magnitude reduction in reverse gate leakage and about a 3% suppression of drain current (I_D) collapse. The increase of g_{mmax} by post-gate annealing is consistent with the increase of 2DEG mobility. The suppression of I_D collapse and the reduction of gate leakage current is attributed to the reduction of interface state density (5.0×10^{11} $cm^{-2}eV^{-1}$) between the AlN/GaN interface after post-gate annealing at 400 °C. This study demonstrates that LTE grown AlN is a promising alternate material as gate dielectric for GaN-based MISHEMT application.

Keywords: LTE; AlN; AlGaN/GaN; interface state density; conductance-frequency; MISHEMT

1. Introduction

AlGaN/GaN based high-electron-mobility transistors (HEMTs) have demonstrated excellent high-frequency and high-power performance owing to their excellent material properties, such as large breakdown field, wide band gap and high electron mobility [1–4]. However, two of the major limiting factors that conventional GaN HEMTs with Schottky metal gates suffer from are a high gate leakage current, and current collapse [5]. The high gate-leakage occurs due to the Schottky metal contact, while current collapse is caused by charge trapping at the surface states present on the AlGaN surface. To solve these issues, various materials such as Al_2O_3 [6,7], HfO_2 [8] or ZrO_2 [9] have been used as both a passivation layer and gate dielectrics. Among non-oxide insulators, AlN is an attractive high-k dielectric material for III–N metal-insulator-semiconductor high-electron-mobility transistors (MISHEMTs) due to its high breakdown field and high dielectric constant [10,11]. In addition, AlN is of interest due to its high thermal conductivity (200 $WK^{-1}m^{-1}$), which makes it suitable for use as a passivation layer to suppress the self-heating [12]. AlN has also been reported to help reduce current collapse [13]. There are two main methods used for the deposition of AlN namely metal-organic chemical vapor deposition [14] (MOCVD) and plasma-enhanced atomic layer deposition [15,16] (PEALD). However, the growth temperature of MOCVD (>600 °C) is not desirable for the fabrication of AlGaN/GaN HEMTs. Furthermore, using a lower growth temperature also has the advantage of preventing tensile strain-induced cracking of AlN layer in AlN based MIS-HEMTs [17,18]. PEALD is

a different approach to grow AlN films which can form a better interface with GaN at 350 °C but with a low deposition rate [19]. Recently, Dikme et al. [20] realized thick single crystalline AlN layers on Si and sapphire substrates at 200 °C using a novel technique called low-temperature epitaxy (LTE). In this technique, AlN is deposited as a combination of physical vapor deposition (PVD) and chemical vapor deposition (CVD). LTE also allows for thick (~1 µm) crystalline films to be grown at low-temperatures which is compatible with III-V device processing. We have recently reported the properties of interface states for AlGaN/GaN metal-insulator-semiconductor diodes (MIS-diodes) using the LTE grown AlN [21,22] So far, no reports have discussed the AlGaN/GaN MISHEMTs with LTE-AlN and its post-gate annealing effects. In this paper, we report AlGaN/GaN MISHEMTs on Si substrate with LTE grown AlN through DC, pulsed I-V and interface trap characterization and analysis.

2. Materials and Methods

The AlGaN/GaN HEMT structure on Si (111) substrate was grown by MOCVD. It consists of i-GaN (2 nm) cap layer, i-$Al_{0.27}Ga_{0.73}N$ (18 nm) barrier layer, i-GaN (800 nm) buffer layer and transition layer (1400 nm). The resistivity of the Si substrate is >10,000 Ω.cm. Hall samples of (i) as-grown HEMT without LTE-AlN, (ii) HEMT with as-deposited ~8 nm LTE-AlN, (iii) HEMT with LTE-AlN annealed at 400 °C and (iv) HEMT with LTE-AlN annealed at 450 °C were prepared and their results at room temperature are summarized in Table 1. The MISHEMT fabrication process started with mesa isolation by reactive ion etching (RIE) using a Cl_2/BCl_3 mixture. The ohmic contacts consisting of Ti/Al/Ni/Au (20/120/40/50 nm) was deposited followed by rapid thermal annealing at 825 °C for 30 s in an N2 atmosphere. Transmission line measurements showed a contact resistance of 0.4 Ω mm. Next, the gate dielectric layer using single crystalline AlN with a thickness of ~8 nm was deposited at 200 °C by LTE. The thickness of the deposited LTE-AlN has previously been confirmed by TEM and is reported elsewhere [22]. The novel growth method combines physical vapor deposition (PVD) and chemical vapor deposition (CVD). The Al source is solid Al with a purity of 5N, while the N source is N_2 gas with purity of 5N8. The N was activated by a linear ion gun close to the sample surface and the Al was sputtered in a way that its beam overlaps with the ion gun beam. The substrate temperature was in the range of 200–225 °C and the deposition pressure was in the upper 10^{-3} mbar range with a total power density of around 5–7 W/cm^2. Before the deposition, the sample was cleaned with a weak Ar/H_2 plasma to remove the native oxide. More details of the growth conditions can be found in the paper by Dikme et al. [20,21].

Table 1. 2DEGproperties of AlGaN/GaN with and without AlN and its post deposition annealing at 400 °C and 450 °C for 300 s in N_2.

2DEG Parameters	AlGaN/GaN HEMT Structure			
	Without LTE-AlN [22]	With LTE-AlN		
		As-dep. [22]	Annealing Temperature °C	
			400	450
Sheet Resistance (Ω/□)	591	523	520	512
Hall Mobility (cm^{2}V^{-1}s^{-1})	1440	1210	1330	1360
Sheet Carrier Concentration (×10^{12} cm^{-2})	7.35	9.89	9.02	8.76

The gate metal stack Ni/Au (50/200 nm) was subsequently formed on the LTE grown AlN by electron beam evaporation. Finally, metal thickening (Ti/Au 10/400 nm) was also performed after AlN etching by Cl2/BCl3/Ar (40/20/10 sccm) plasma. The inset of Figure 1a shows the cross-sectional schematic diagram of the fabricated MISHEMTs with LTE-grown AlN. For this study, we have used device dimensions of $L_g/L_{sg}/L_{gd}/W_g$ = 2/2/2/(2 × 100) µm. To study the post-gate annealing effects a MISHEMT sample with ~8 nm of LTE-AlN were annealed at 400 °C in a N_2 atmosphere using rapid thermal annealing process. A post-gate annealing temperature of 400 °C was chosen as there

was minimal changes to the Hall parameters after post deposition annealing at 450 °C (see Table 1). A lower temperature is also beneficial, as higher temperatures have previously been shown to cause degradation of Ni/Au gates [23,24].

3. Results and Discussion

Figure 1 shows (a) the capacitance-voltage (C-V) and (b) gate leakage current (I_{gleak}) characteristics of Schottky diode (MS-diode), LTE-AlN MIS-diode with and without post-gate annealing. At zero-bias, the capacitance density of 373 nF/cm^2 and 302 nF/cm^2 for 200 µm diameter conventional Schottky diode and MIS-diode were obtained, respectively. After annealing, there is no significant change in capacitance density at 0 V. With reference to Schottky diode, the LTE-AlN MIS-diode exhibited 2 orders of magnitude lower I_{gleak} at −20 V (Figure 1b). After post-gate annealing at 400 °C, MIS-diodes exhibited about an order of magnitude further reduction in I_{gleak}. The improvement in I_{gleak} is attributed to the improvement of interface properties of LTE-AlN on GaN/AlGaN after the 400 °C annealing.

Figure 2 shows (a) current–voltage (I_{ds}-V_{ds}) and (b) transfer characteristics of LTE-AlN/AlGaN/GaN MISHEMTs without and with post-gate annealing at 400 °C. The as-deposited AlN MISHEMT showed a maximum drain current (I_{Dmax}) of 708 mA/mm at a gate bias of 4 V and a maximum extrinsic transconductance (g_{mmax}) of 129 mS/mm. After annealing, MISHEMT exhibited I_{Dmax} of 684 mA/mm at a gate bias of 4 V and g_{mmax} of 148 mS/mm. The decrease in I_{Dmax} after annealing originates from a change in two-dimensional electron gas (2DEG) carrier concentration (n_s), as $I_D \propto n_s$. As shown in Table 1, after annealing at 400 °C, n_s was found to decrease by 9% (from 9.89×10^{12} cm^{-2} to 9.02×10^{12} cm^{-2}) which results in the 9% reduction in I_{Dmax}. Similarly, the 15% improvement of g_{mmax} after post-gate annealing is attributed to an increase in electron mobility as well as a reduction of interface states [25]. This is attributed to a reduction in Coulomb scattering from the dielectric layer near the AlGaN/GaN interface [26]. The enhanced mobility was confirmed by Hall measurements, which shows an ~10% improvement (from 1210 cm^{2}V^{-1}s^{-1} to 1330 cm^{2}V^{-1}s^{-1}) in 2DEG Hall mobility (μ_n), as seen in Table 1. From the Figure 2b, it is clear that AlN MISHEMT exhibited an order of magnitude improvement in the device I_{ON}/I_{OFF} ratio after the post-gate annealing at 400 °C, which is due to the reduction of drain current at OFF-state. This is possibly caused by a reduction on traps at the AlN/GaN interface reducing the available leakage current conduction paths. The threshold voltages (V_{th}) of the devices were measured at −3.95 V and −3.8 V for as-deposited MISHET and post-gate annealed MISHEMT at 400 °C, respectively. V_{th} can be expressed as

$$V_{th} = V_{th0} - \frac{Q_{it}}{C_{AlN}} \quad (1)$$

where V_{th0} is the threshold voltages without any interface states, Q_{it} is the interface-trapped charge density and C_{AlN} is the capacitance of the AlN layer. After annealing at 400 °C there is a minimal positive shift in threshold voltage which could be caused by a slight reduction of interface traps at LTE-AlN/GaN interface. This is verified by the frequency-dependent conductance measurements discussed in the later section. A similar occurrence was also reported after post-gate annealing by Zhou et al. for Al_2O_3 and Shih et al. for HfO_2 [8,25]. In these cases, it was postulated that the positive V_{th} shift was caused by a reduction in positively charged traps and interface traps or positive fixed/mobile charges, and was confirmed by a reduction in calculated interface states after annealing. A benchmarking table between these devices and those published elsewhere can be seen in Table 2 [15,27–29].

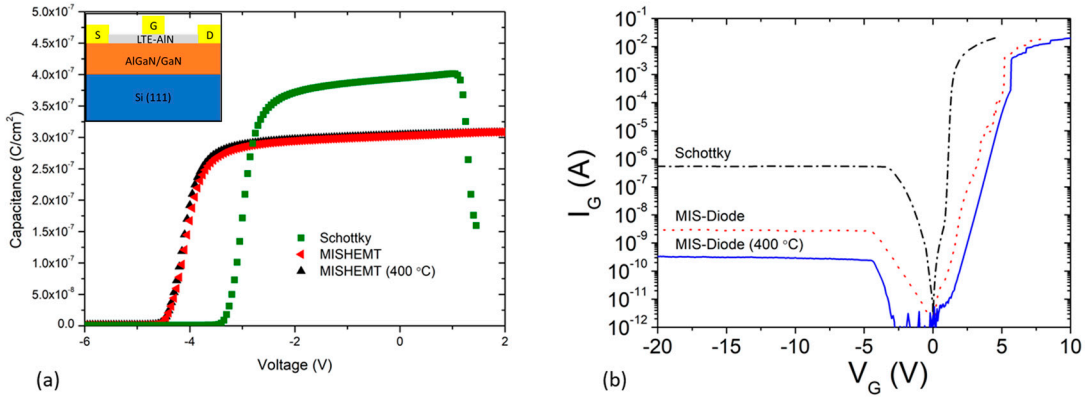

Figure 1. (**a**) C-V characteristics and (**b**) two terminal I_{gleak}-V_g (200 um diameter diodes) characteristics of Ni/AlGaN/GaN Schottky diode, as-deposited LTE-AlN/AlGaN/GaN metal-insulator-semiconductor diode [22] and post-gate annealed MIS-diode at 400 °C. Inset: Schematic cross-sectional diagram of fabricated AlGaN/GaN MISHEMTs with LTE grown AlN on Si substrate.

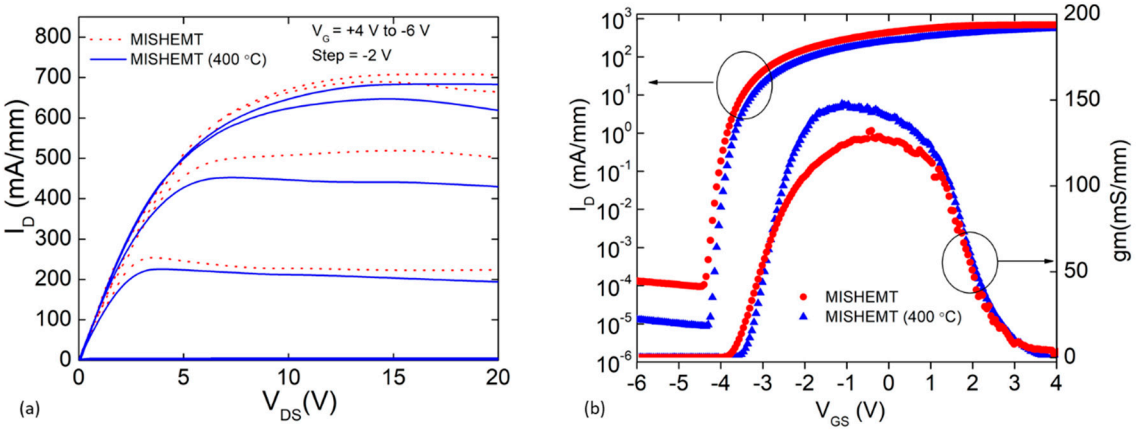

Figure 2. (**a**) DC I_{DS}-V_{DS} and (**b**) transfer characteristics of as-deposited LTE-AlN/AlGaN/GaN MISHEMT and post-gate annealed MISHEMT at 400 °C.

Table 2. A benchmarking table for MISHEMT on AlGaN/GaN using AlN as a gate dielectric layer.

Reference	Thickness (nm)	Substrate	Deposition Method	Device Dimensions L_g/W_g (μm)	I_{dmax} (mA/mm)	g_{mmax} (mS/mm)	On/Off Ratio (Orders of Magnitude)
[15]	10.6	Si	ALD	2.5/60	563 @ 5V	87	~5
[27]	10	Sapphire	ALD	1/200	600 @ 4V	127	~9
[28]	20	Sapphire	PEALD	0.5/50	~1050 @ 2 V	289	~3
[29]	8	SiC	Reactive Sputtering	0.4/200	~1250 @ 2 V	260	~3
This work	8	Si	LTE	2/(2 × 100)	684 @ 4V	148	~8

Figure 3 shows pulsed I_D-V_D characteristics of (a) as-deposited MISHEMTs with LTE-AlN and (b) MISHEMTs with post-gate annealing at 400 °C. The devices were subjected to the pulse width/period of 100 μs/10ms and quiescent biases of (V_{gs0}, V_{ds0}) = (0, 0) and (−6, 20) V was used for the pulsed I-V measurements. The as-deposited LTE-AlN MISHEMT exhibited a I_D/I_{Dmax} ratio of 0.91 for both quiescent biases (V_{gs0}, V_{ds0}) = (0, 0) and (−6, 20). This indicates that the devices exhibited around 9% drain current (I_D) collapse. After annealing at 400 °C, the I_D/I_{Dmax} ratio of MISHEMT increases to 0.94. Therefore, about 3% I_D collapse was suppressed after post-gate annealing at 400 °C. The improvement in current collapse in 400 °C annealed MISHEMT is attributed to the reduction of interface states at the AlN/GaN interface.

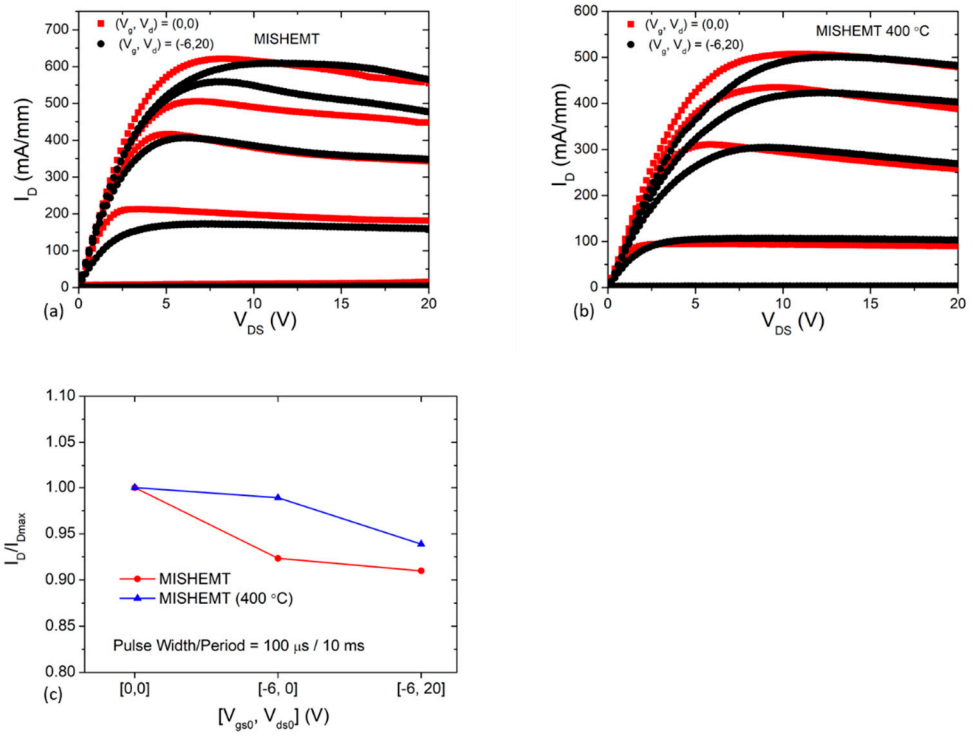

Figure 3. Pulsed I_{DS}-V_{DS} characteristics at quiescent bias points of (V_{gs0}, V_{ds0}) = (0, 0), (−6, 20) for (**a**) LTE-AlN MISHEMTs, (**b**) 400 °C annealed MISHEMTs and (**c**) normalized I_D with I_{Dmax} for as-deposited LTE-AlN/AlGaN/GaN MISEMT and annealed MISHEMT at 400 °C vs. the quiescent bias points (V_{gs0}, V_{ds0}) = (0, 0), (−6, 0), (−6, 20) V.

In order to quantify the amount of interface states at the LTE-AlN/GaN interfaces, frequency-dependent conductance measurements were performed at selected biases to estimate the density of interface states (D_{it}) and trap time constant (τ_{it}). The frequency was varied from 1 kHz to 5 MHz over a wide range of gate voltages (V_g). Figure 4a shows the typical G_p/ω versus ω graph of LTE-AlN MISHEMT with post-gate annealed at 400 °C measured at different V_g values between −4.1 V to −3.5 V. The D_{it} calculations were performed using the conductance-frequency method, which is widely used for interface calculations [21,30,31]. The two peak regions in the G_p/ω plots correspondingly indicate the presence of both low frequency (slow traps) and high frequency (fast traps). The exhibited fast traps are associated interface traps of the AlGaN/GaN hetero-interface [15,32], while the observed slow traps are associated with the AlN/GaN interface. The estimated D_{it} is shown in Figure 4b for the as-deposited LTE-AlN MIS-diode, as well as the MIS-diodes with post-gate annealing at 400 °C. The minimum D_{it} were estimated as 7.6×10^{11} $cm^{-2}eV^{-1}$ and 5.0×10^{11} $cm^{-2}eV^{-1}$ for the as-deposited MIS-diode and MIS-diode with post-gate annealing at 400 °C, respectively. With reference to as-deposited MIS-diode, a reduction of D_{it} (24%) has been observed in the MIS-diode after post-gate annealing at 400 °C. This reduction of interface traps can be associated with the suppression of I_D collapse. Annealing at 400 °C helps to reduce the slow deep level traps thus reducing the remote Coulomb scattering from the AlN layer and improving the mobility.

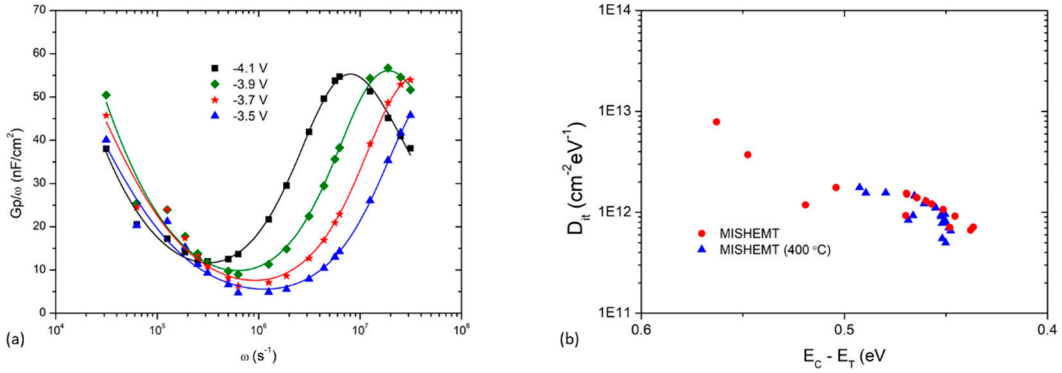

Figure 4. (**a**) G_p/ω versus radial frequency plot for different gate voltages of post-gate annealed LTE-AlN MIS-diode at 400 °C (solid lines are fitting curves). (**b**) Distribution of interface state density as a function of the gate voltage of as-deposited LTE-AlN MIS-diodes [22] and post-gate annealed MIS-diodes at 400 °C.

4. Conclusions

In summary, AlGaN/GaN MISHEMTs on Si has been demonstrated for the first time with LTE grown AlN as a dielectric layer. The influence of post-gate annealing at 400 °C was also studied using DC, pulsed I-V and interface state characteristics. After the LTE-AlN deposition the LTE-AlN MISHEMT showed a maximum drain current (I_{Dmax}) of 708 mA/mm at a gate bias of 4 V and a maximum extrinsic transconductance (g_{mmax}) of 129 mS/mm. By employing a post-gate annealing scheme at 400 °C in an N_2 atmosphere there was about a 15% of increase in g_{mmax} and an order of magnitude reduction of gate leakage. About a 3% improvement of I_D collapse suppression was also observed after post-gate annealing at 400 °C. The reduction of I_{gleak} and I_D collapse could be due to the reduction of interface state density of about 25%. This study indicates that the optimized post-gate annealing, which in our case is at 400 °C, is a viable way to have improved device characteristics in AlGaN/GaN MISHEMTs with LTE grown AlN.

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Characterization of Self-Heating Process in GaN-Based HEMTs

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Abstract: Thermal characterization of modern microwave power transistors such as high electron-mobility transistors based on gallium nitride (GaN-based HEMTs) is a critical challenge for the development of high-performance new generation wireless communication systems (LTE-A, 5G) and advanced radars (active electronically scanned array (AESA)). This is especially true for systems operating with variable-envelope signals where accurate determination of self-heating effects resulting from strong- and fast-changing power dissipated inside transistor is crucial. In this work, we have developed an advanced measurement system based on DeltaV_{GS} method with implemented software enabling accurate determination of device channel temperature and thermal resistance. The methodology accounts for MIL-STD-750-3 standard but takes into account appropriate specific bias and timing conditions. Three types of GaN-based HEMTs were taken into consideration, namely commercially available GaN-on-SiC (CGH27015F and TGF2023-2-01) and GaN-on-Si (NPT2022) devices, as well as model GaN-on-GaN HEMT (T8). Their characteristics of thermal impedance, thermal time constants and thermal equivalent circuits were presented. Knowledge of thermal equivalent circuits and electro–thermal models can lead to improved design of GaN HEMT high-power amplifiers with account of instantaneous temperature variations for systems using variable-envelope signals. It can also expand their range of application.

Keywords: GaN HEMT; self-heating effect; microwave power amplifier; thermal impedance; thermal time constant; thermal equivalent circuit

1. Introduction

It is now commonly accepted that high electron-mobility transistors based on gallium nitride (GaN HEMT) are the best choice for high-frequency and high-power devices, such as high-power amplifiers (HPAs) used in new generation radars, including active electronically scanned array (AESA), and modern wireless communication systems, i.e., LTE-A and 5G radios [1–4]. Due to the large complexity of signals applied in modern radars and new radios, power amplifiers have to meet stringent requirements concerning not only their linearity, output power level and efficiency but also appropriate heat management [5]. This is because both kinds of mentioned systems are operated by variable-envelope signals.

In AESA radar pulses, the signals are not only frequency-modulated but can be also modulated both in phase and amplitude [6,7]. The same concerns high-speed wireless networks which use quadrature amplitude modulation (QAM) with a large peak-to-average power ratio (PAPR). For instance, the PARP

is 8.5–10 dB for LTE-A and more than 13 dB for 5G [8]. Such high variations in output power result in large changes of power dissipated in a transistor of HPA and thereby temperature variations in an active area of transistor. In addition, the transistors in transmitting amplifiers are often operated under fast-changing thermal conditions as response to quick and large signal envelope changes in time, e.g., during RF pulse or pulse-to-pulse [9], as well as the LTE-A signal.

It is obvious that temperature fluctuations cause changes in the transistor's electrical characteristics. This is a serious problem for the variable-envelope signals which are particularly sensitive to distortions caused by HPAs as a result of nonlinearity and self-heating effect of transistor. The impact both effects and discloses itself in the form of amplifier transmittance changes in time [10]. In the case of power amplifiers for wireless networks, parameters such as AM-AM and AM-PM conversions are often used to describe the effect of transistor nonlinearity. However, these are static parameters that do not show the instantaneous variations in signal amplitude and phase.

We think that the impact of transistor self-heating effect on its performances should be determined by the time-dependent transmittance changes, showing separately the changes in amplitude and phase.

Transistor nonlinearities have been quite thoroughly described and implemented in popular large-signal models, e.g., Angelov's HEMT model [11]. In contrast, the thermal effect in the transistor, especially GaN HEMT is not so widely recognized and is usually modeled using either R_{th} under static conditions or a simple 1-section low-pass (parallel R_{th}-C_{th}) circuit as in the microwave transistor models provide by e.g., Wolfspeed (Durham, NC, USA), MACOM (Lowell, MA, USA), Modelithics (Tampa, FL, USA). This approach is not satisfying for fast-changing variable-envelope excitations. Therefore, we propose to describe self-heating effect in transistor by means of transient thermal impedance $Z_{th}(t)$ and more complex, multi-section, equivalent thermal circuit of transistor.

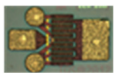
The paper presents our own approach to the thermal characterization of GaN HEMTs using thermal impedance measurements $Z_{th}(t)$ correlated with the solution of heat conduction equation in the GaN HEMT structure by means of FDTD method [12]. As a result that GaN-based epi-structures for HEMTs are grown on various substrates, namely on SiC, Si and GaN and consist of several epi-layers, each with different thermal properties. The results of simulations and measurements enable the thermal time constants appearing in the transistor structure to be identified.

2. Scope of the Research

2.1. Samples

The following GaN-based HEMTs have been a test subject in our study: commercially available GaN-on-SiC HEMTs CGH27015F (packaged) from Wolfspeed, and TGF2023-2-01 (die) from Qorvo (Greensboro, NC, USA), GaN-on-Si HEMT NPT2022 (packaged) from MACOM and GaN-on-GaN HEMT (marked T8) fabricated within PolHEMT project [13,14]. The T8 transistor was made on epitaxial layers grown on a truly bulk monocrystalline semi-insulating GaN. Testing was performed on two gates of 0.8 µm length and 500 µm width structure. The dies were mounted to the plate in test board using EPO-TEK H20E glue approx. 0.025 mm. Typical performance and electrical characteristics of the selected GaN HEMTs are given in Table 1 (manufacturer's data).

Table 1. Typical performance and application information of high electron-mobility transistors based on gallium nitride (GaN HEMT) samples.

Parameter	CGH27015F	TGF2023-2-01	NPT2022	T8
Frequency Range	2.3–2.9 GHz	DC–14 GHz	DC–2 GHz	DC–12 GHz
Breakdown Voltage V_{DS}	120 V	40 V	160 V	120 V
Channel Temperature	175 °C	225 °C	200 °C	295 °C
Thermal Resistance R_{th}	8 °C/W	16 °C/W	1.7 °C/W	30 °C/W
Test Conditions (V_{DS}, I_{DQ})	28 V, 100 mA	28 V, 125 mA	48 V, 600 mA	28 V, 65 mA
Saturated Output Power	15 W	5 W	100 W	2 W
Power Gain	13 dB@2.5 GHz	16 dB@3 GHz	16 dB@2 GHz	14 dB@3 GHz
View				

2.2. Electrical Characterization of Thermal Properties

In general terms we follow the well-known DeltaV_{GS} measurement technique at the constant current of forward-biased gate-to-source diode in MESFET or HEMT (MIL-STD-750D-3 standard, method 3104) [15,16]. However, our approach is different from the previous ones by specific bias and timing conditions of the transistor during the measurements.

The knowledge of thermal impedance $Z_{th}(t)$ allows calculating the channel temperature $T_j(t)$ for any shape of dissipated power $P_d(t)$ as follows [17]:

$$T_j(t) = T_0 + \int_0^t P_d \times Z'_{th}(t-\tau)d\tau \quad (1)$$

where:

$T_j(t)$—channel temperature response;
T_0—ambient temperature (heatsink);
$Z'_{th}(t)$—time derivative of $Z_{th}(t)$;
P_d (t)—dissipated power.

The thermal impedance $Z_{th}(t)$ of different elements is often modeled, through the electro–thermal analogy, by lumped electrical equivalent circuit which contains a number of thermal resistances R_{th} and thermal capacitances C_{th} connected in an appropriate way. Typically, in simplified terms, the thermal equivalent circuit consists of several parallel R_{th}-C_{th} circuits connected in series [18]. Each of the low-pass circuits R_{thi}-C_{thi} corresponds to a thermal time constant τ_i in an exponential approximation of thermal impedance $Z_{th}(t)$ characteristic. Such a lumped electrical model can be used to calculate the channel temperature using one of popular circuit simulators like ADS or SPICE. That approach is very convenient, because the temperature of active area of transistors can be simulated using the tool applied anyway for analysis of electrical parameters.

As previously mentioned the developed system of thermal impedance $Z_{th}(t)$ measurement was inspired by the method 3104 from MIL-STD-750D-3 standard which uses the effect of the voltage drop $\Delta V_{GS}(t)$ at a forward–biased junction as a sensor of the temperature. Furthermore, the temperature values of the gate-source diode and the transistor channel are identical. The basic formula for that measurement technique was derived from the Schottky's diode equation and is expressed as follows:

$$V_{GS} = n \times V_b - \frac{n \times k \times T_j}{q}\left[2ln(T_j) - ln\left(\frac{I_G}{A \times W}\right)\right] \quad (2)$$

where:

I_G—junction forward current;
A—effective Richardson constant;
W—the junction surface;
q—charge of the electron;
k—Boltzmann constant;
n—ideality factor;
V_b—built-in barrier voltage.

At the constant gate current I_G, the voltage drop ΔV_{GS} across the source—gate junction decreases almost linearly with the rise of temperature and is given by:

$$\Delta V_{GS} = K \times \Delta T_j \tag{3}$$

where: K—constant.

The $Z_{th}(t)$ measurement procedure consists of the following steps:

- preparation of a test board with connected transistor marked as DUT in Figure 2b.
- gate-source voltage $V_{GS}(t)$ recording.
- K factor measurement—calibration.
- thermal impedance $Z_{th}(t)$ calculation.

Examples of test boards for packaged transistors and chips measurements are presented in Figure 1a,b, respectively. The test board consists of a printed board circuits (PCB) placed on a thick metal base plate (usually made of copper) which should be characterized by high thermal inertia. The transistor bottom is thermally connected to this plate. The temperature at the bottom of the transistor (T_0) must be constant during the $V_{GS}(t)$ recording. Otherwise the T_0 temperature changes must be taken into account in the last step of the procedure i.e., thermal impedance $Z_{th}(t)$ calculation. The transistor can be biased in active state in heating phase of the $V_{GS}(t)$ recording procedure. Since the GaN HEMTs are generally potentially unstable the stabilizing circuits are required on the PCB to protect the transistor against damage.

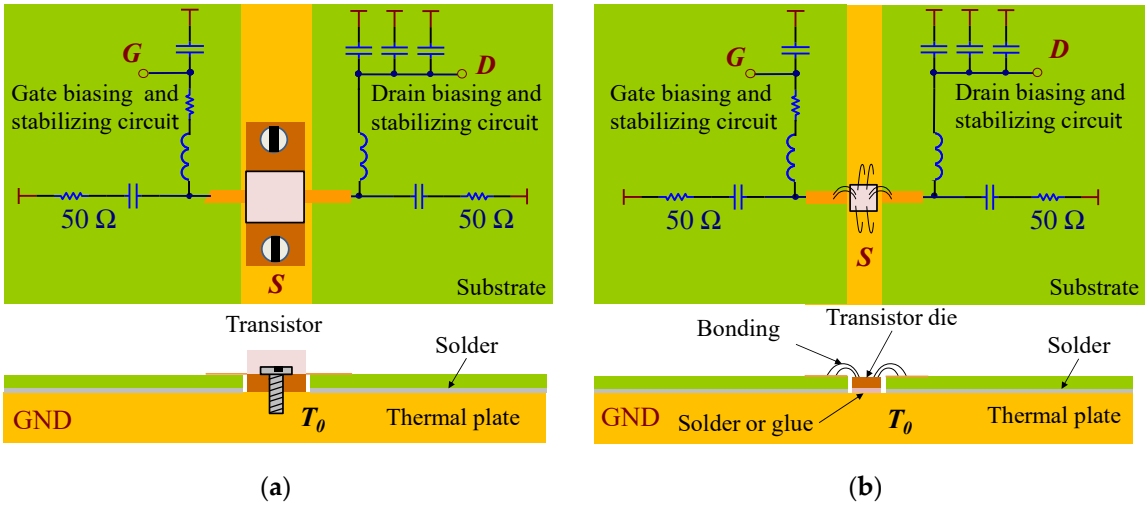


Figure 1. The outline of the test boards: (**a**) packaged transistor and (**b**) die (chip).

The simplified block diagram of the proposed $Z_{th}(t)$ measurement system with the timing diagram of $V_{GS}(t)$ recording procedure is shown in Figure 2. In the methods based on the MIL-STD-750D-3 standard the gate-to-source diode is forward-biased all the time and the operating point of the transistor

during the heating phase is placed in "on" region of the DC I-V output characteristic i.e., with relatively low V_{DS} DC voltage ($V_{DS} \leq V_{knee}$) and high I_D drain current. In that conditions the power dissipated in transistors is significantly lower and hence the R_{th} value is also smaller than in the case of normal transistor operation in transmitter's amplifier when RF signal is amplified i.e., the average value of the drain current is higher than at the quiescent operating point (without RF power, as in classes AB, B and C). Therefore, in our thermal measurements, the operating point of the tested transistor is selected so that it corresponds to the expected maximum power from the amplifier, especially when typical V_{DS} bias voltage for power GaN HEMTs is over a 28 V to 50 V voltage range.

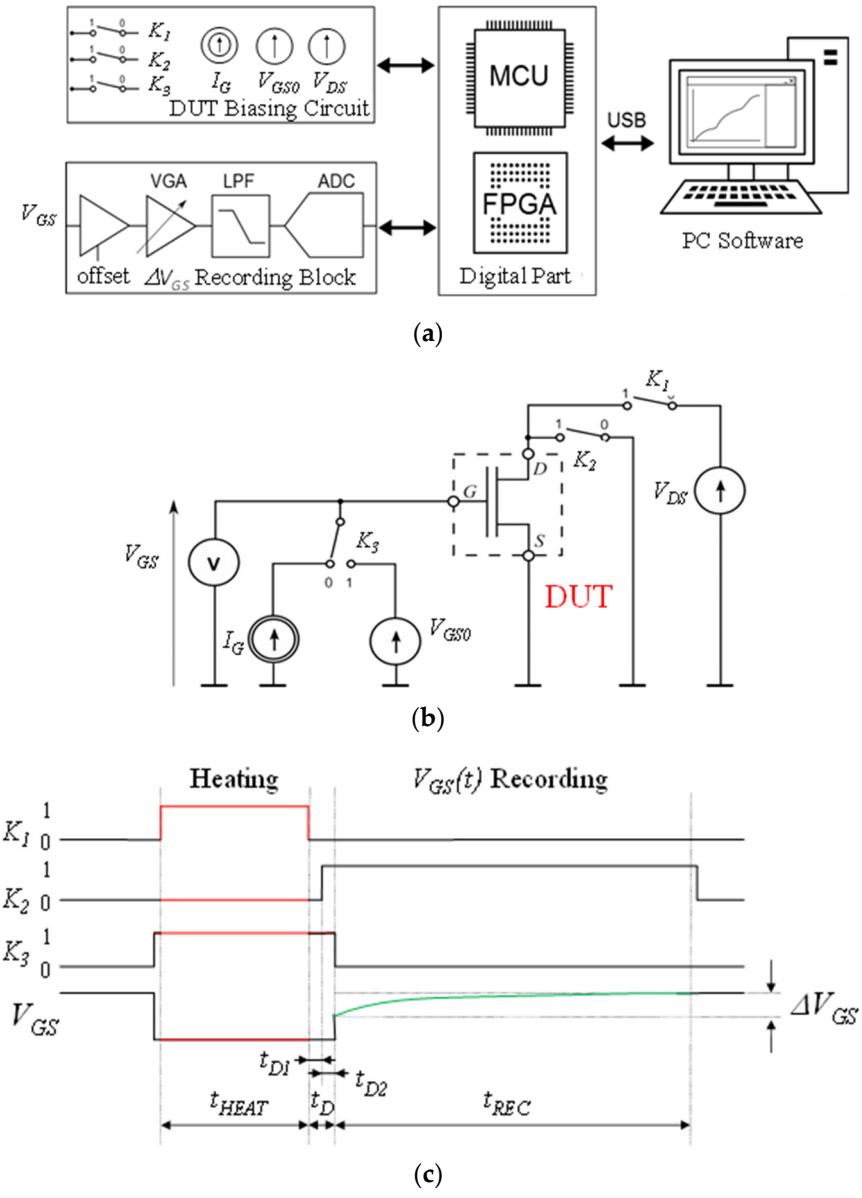


Figure 2. (**a**) Simplified block diagram of thermal impedance $Z_{th}(t)$ measurement system; (**b**) DUT biasing circuit; (**c**) timing diagram of $V_{GS}(t)$ recording procedure.

Information on the influence of V_{DS} voltage on thermal resistance R_{th} is scarce and ambiguous. From one side strong thermal resistance R_{th} changes versus V_{DS} voltage for GaAs MESFET transistors (the constant level of power was dissipated in transistors during the tests) was observed [15]. On the other hand weak dependence of $Z_{th}(t)$ or R_{th} for GaAs (no more than 10%) [19] and GaN (no more

6%) [20,21] transistors for V_{DS} change was demonstrated. As reported in [22–24], the $Z_{th}(t)$ changes mainly follow dependence of thermal conductivity of GaN HEMT layers on temperature.

Our test setup (Figure 2) was designed to be very flexible, and it allows setting wide range V_{DS} bias voltages and I_D current during the heating phase. It includes extra K_2, K_3 switches and controlled V_{GS0} voltage source. The V_{GS0} setting range is −6–0 V and V_{DS} from 0 V to +50 V. The control range of current source I_G is 0.1–10 mA. The proposed $V_{GS}(t)$ recording procedure (Figure 2c) is also different from the method based on MIL-STD-750D-3 standard.

At the beginning the keys are set up in the following positions: K_1, K_3 position "1", K_2 position "0" and the transistor is biased at the chosen operating point and heated by DC power dissipated therein. After the heating pulse the keys K_1, K_2 and K_3 are switched to the positions 0 and 1, respectively. This is the start of $V_{GS}(t)$ sampling during the cooling phase of the DUT. The forward gate current remains constant and it equal to I_G after the heating time while the drain-source voltage source V_{DS} circuit is open i.e., drain current is 0. The switching time of K_1, K_2 and K_3 keys is less than 10 ns but in practice, the total switching time between heating end and the start of recording phase t_D is less than 100 ns. In the commercially available measurement systems that time is close to 5 µs [25]. The t_D time depends on input capacitance C_{gs} of transistor and I_G value. Therefore, gate current I_G value should be as high as possible. The forward gate current is limited by the maximum allowed level specified for the transistor. Furthermore, time delay is also determined by bias and stabilization circuits. In MIL-STD-750D standard the V_{GS} voltage is only measured in two-time moments: before heating and as quick as possible after heating. These two V_{GS} values allow calculating only the thermal resistance R_{th}. This is the main purpose of MIL-STD-750D-3 standard as it is clearly indicated in description. Therefore, this method is aimed at the testing transistors in packages, especially die attachment quality [15].

As shown in Figure 2a, the $V_{GS}(t)$ sampling is performed by means the recording block and digital part of the system. The recording time t_{REC} as well as the sampling frequency f_s can be changed. At the beginning of the recoding phase f_s achieves 100 MHz and after 1 s drops to 10 Hz. The recording is continued up to the moment when the lack is significant changes of $V_{GS}(t)$. The maximum recording time of $V_{GS}(t)$ is 90 s. This ploy enables significantly reducing the amount of $V_{GS}(t)$ recorded data. The $V_{GS}(t)$ and $Z_{th}(t)$ characteristics are similar to the response of low pass filter. Therefore, there is no need to record of $V_{GS}(t)$ samples with the maximum sampling frequency up to end of measurement procedure.

After $V_{GS}(t)$ recording, the calibration is needed to calculate K factor values. The DUT is placed in a thermal test chamber and the V_{GS} voltages across the forward-biased gate-to-source Schottky junction for a number of different temperatures are stationary measured. The I_G value is constant and the same as during in $V_{GS}(t)$

recording. The concept of K factor measurement is presented in Figure 3.

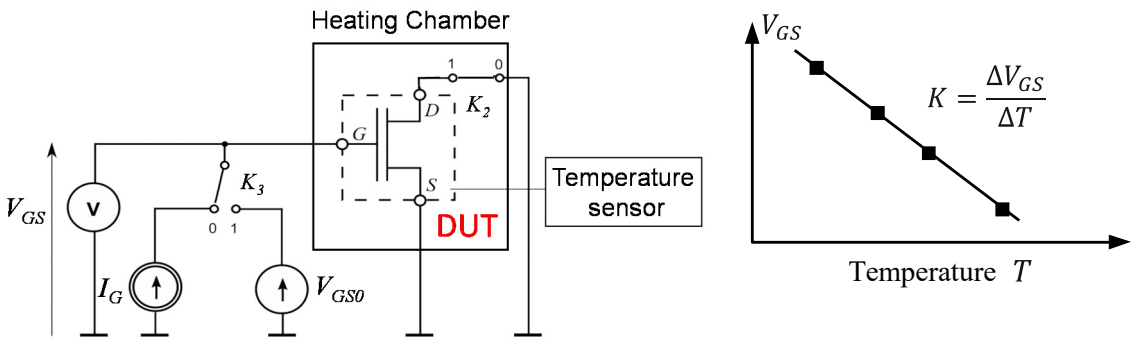


Figure 3. The concept of K factor measurement.

The last step of the measurement procedure is channel temperature $T_j(t)$ and thermal impedance calculation $Z_{th}(t)$. The channel temperature $T_j(t)$ of transistor is given by following formula:

$$\Delta T_j(t) = T_0 + K \times V_{GS}(t) \tag{4}$$

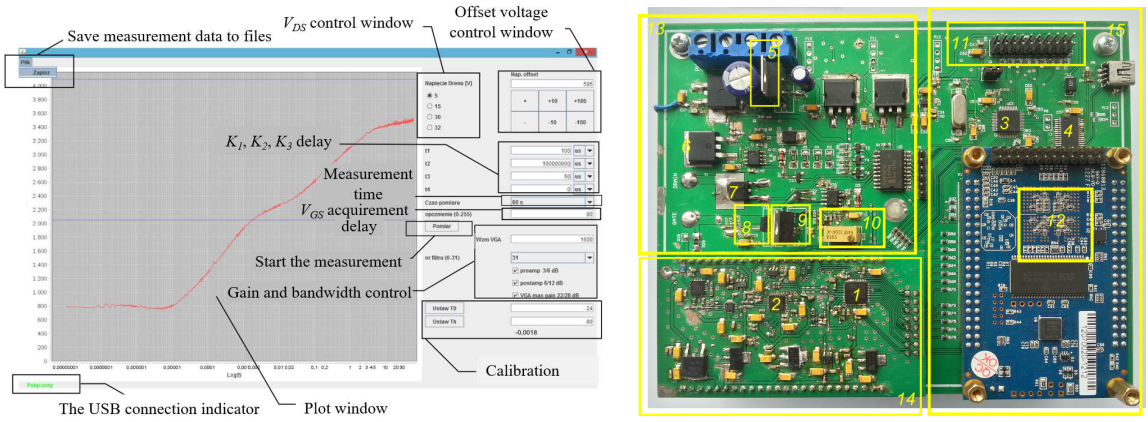
As shown in Figure 2c the $V_{GS}(t)$ is acquired during the transistor cooling. Under these conditions, as shown in Figure 2c, the thermal impedance $Z_{th}(t)$ can be calculated as follows:

$$Z_{th}(t) = \frac{T_j(0) - T_j(t)}{P_{dc}} \tag{5}$$

where:

$T_j(0)$—calculated channel temperature at the beginning of the $V_{GS}(t)$ recording;
P_{DC}—dissipated power in transistor during heating phase.

The $Z_{th}(t)$ measurement system consists of the hardware (microcontroller and FPGA), firmware and PC software. The FPGA block controls the K_1–K_3 switches, acquires and stores the $V_{GS}(t)$ data from A/D converter. The communication between hardware and PC is realized by microcontroller (MCU) using USB standard. The $V_{GS}(t)$ data from FPGA is transferred to PC via MCU. The MCU controls the components of the recording block and the V_{GSO}, V_{DS} voltage sources. All parameters of $V_{GS}(t)$ recording procedure (Figure 2b,c) can be set using PC software. The PC software also allows pre-processing of the received data, calculation of $Z_{th}(t)$ impedance and finally visualization of the results. The graphical user interface of the PC software is presented in Figure 4a. The $Z_{th}(t)$ measurement results can be exported to text file in *.csf format. The PC software has been written in Java using the Eclipse environment. The photo of hardware of the $Z_{th}(t)$ measurement system is shown in Figure 4b.



(**a**) (**b**)

Figure 4. (**a**) Graphical user interface (GUI); (**b**) photo of $Z_{th}(t)$ measurement system hardware. (1—A/D converter, 2—VGA, 3—MCU, 4—USART/USB converter, 5—V_{DS} voltage regulator, 6—K_1 switch, 7—K_2 switch, 8—I_G current source, 9—V_{GS} voltage regulator, 10—V_{GS0} adjusting, 11—MCU programing connector, 12—FPGA located at bottom side, 13—DUT biasing circuit, 14—recording block, 15—digital part of the system).

3. Results

The $Z_{th}(t)$ and $T_j(t)$ of CGH27015 and T8 are presented in Figure 5a–d, respectively. The GaN-on-SiC HEMT CGH27015F was mounted in the test board shown in Figure 1a. During the heating phase the CGH27015F was biased as follows: V_{DS} = 28 V (P_D = 14 W) and V_{DS} = 15 V (P_D = 7 W) at the same current I_D = ~0.5 A.

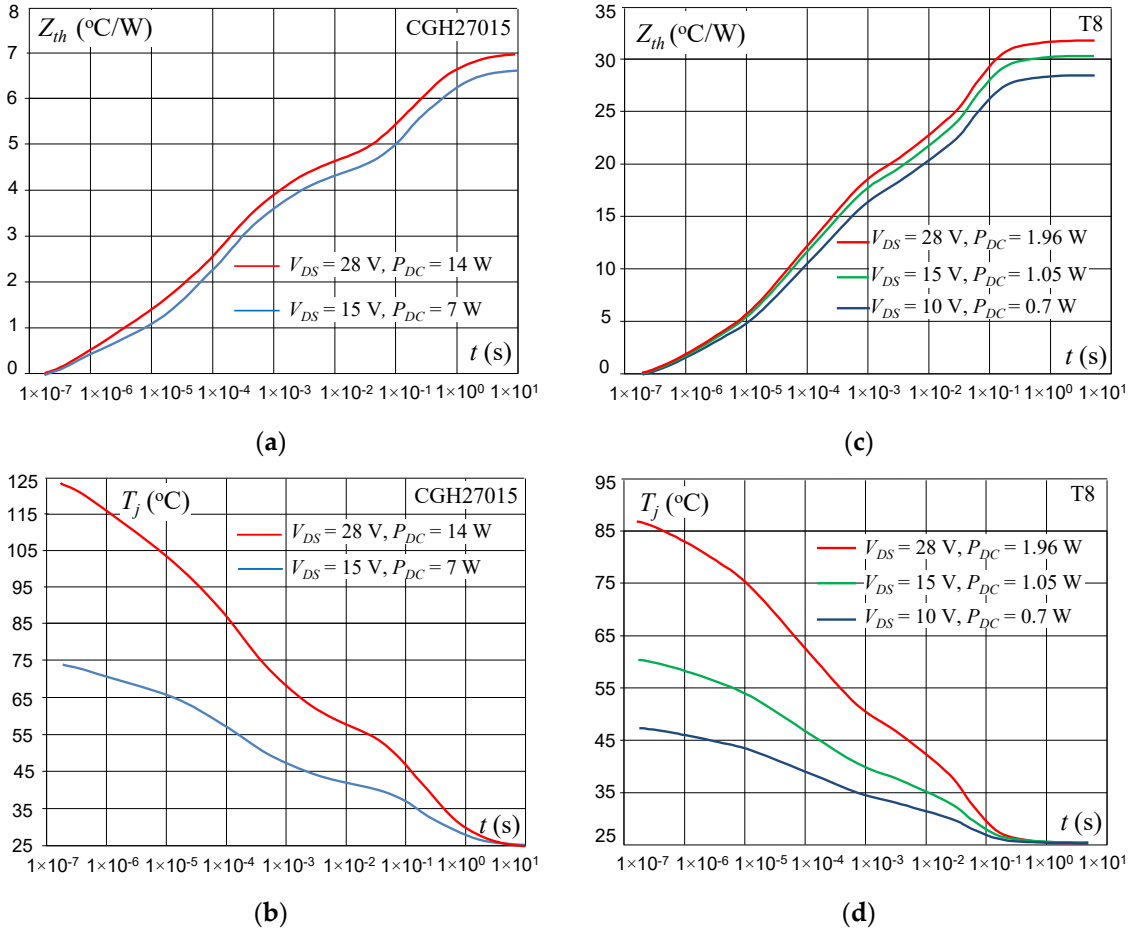


Figure 5. GaN-on-SiC CGH27015F and GaN-on-GaN HEMT T8 (**a**,**c**) thermal impedance $Z_{th}(t)$ and (**b**,**d**) channel temperature $T_j(t)$ measurements, respectively.

During the heating phase the T8 was biased: V_{DS} = 28 V (P_D = 1.96 W), V_{DS} = 15 V (P_D = 1.05 W) and V_{DS} = 10 V (P_D = 0.7 W) with the same drain current of 70 mA. The next results of T8 and GaN-on-SiC TGF2023-2-01 measurements presented in Figure 6 were performed under modified conditions i.e., the same power level was dissipated inside dies during heating phase of measurement procedure. In this phase, dissipated power level inside T8 was P_D = 0.75 W and voltage V_{DS} = 5 V, 10 V, 15 V, 20 V and 28 V (Figure 6a,b). The $Z_{th}(t)$ and the $T_j(t)$ of TGF2023-2-01 are shown in Figure 6c. In this case the dissipated power level was P_D = 2.5 W and the V_{DS} = 5 V, 10 V, 15 V, 20 V and 28 V.

The $Z_{th}(t)$ changes (T8) shown in Figure 5c, when different power levels were dissipated in GaN HEMTs, are bigger in comparison to $Z_{th}(t)$ changes indicated in Figure 6c for the same power dissipated in transistors and different drain-to-source voltages. The impact of Ga-on-Si HEMT NPT2022 voltage V_{DS} on the $Z_{th}(t)$ characteristics, as shown Figure 7a, is slightly larger to similar $Z_{th}(t)$ characteristics of GaN-on-SiC HEMT TGF2023-2-01 (Figure 6a). Generally, obtained results confirm the lack of significant dependence of impedance $Z_{th}(t)$ on GaN HEMT bias voltage.

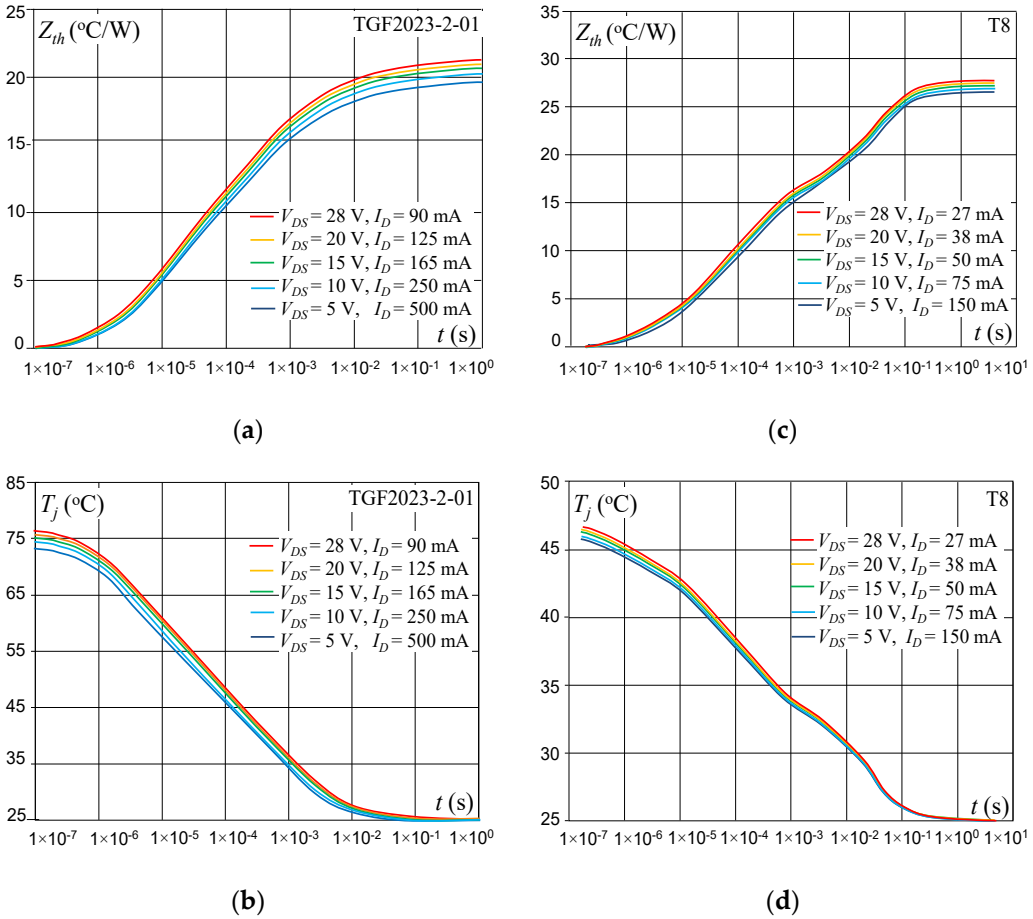


Figure 6. Thermal impedance $Z_{th}(t)$ and channel temperature $T_j(t)$ measurements for the same power level dissipated inside dies during the heating phase: (**a**,**b**) GaN-on-SiC TGF2023-2-01 (Qorvo), (**c**,**d**) GaN-on-GaN HEMT T8, respectively.

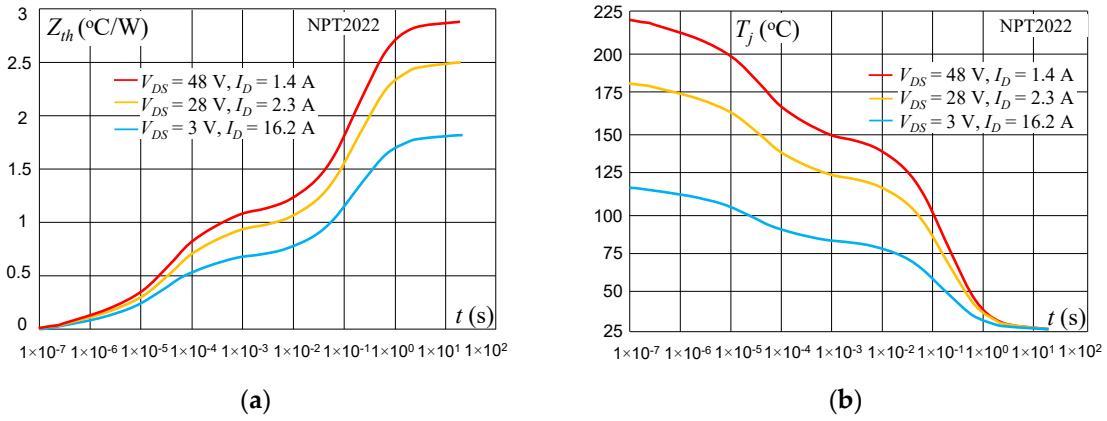


Figure 7. GaN-on-Si HEMT NPT2022 (MACOM) (**a**) thermal impedance $Z_{th}(t)$ and (**b**) channel temperature $T_j(t)$ measurements.

The "tank" and "filter" configurations of R_{th}-C_{th} thermal model are considered [18]. These configurations are also known as Cauer and Foster. Both models are capable to quite accurately fit the thermal impedance $Z_{th}(t)$ characteristics. The "tank" circuit consists of a chain of parallel circuits R_{th}-C_{th} which is simple to mathematical description. We have developed the automatic routine of "tank" model fitting in Mathcad software. The input data for this software are the $Z_{th}(t)$ measurement

results stored in text format file (*.csf). For assumed number of R_{th}-C_{th} cells, the software allows calculating maximum error of fitting curve.

The thermal "tank" models of selected HEMTs were calculated at following bias points: CGH27015F—V_{DS} = 28 V, I_D = 0.5 A, T8—V_{DS} = 28 V, I_D = 72 mA, TGF2023-2-01—V_{DS} = 28 V, I_D = 90 mA, NPT2022—V_{DS} = 48 V, I_D = 1.5 A. These operating points correspond to output power levels close to the maximum for each transistor. The $Z_{th}(t)$ characteristics were fitted to measurements with the error lower than 1% and are shown in Figure 8.

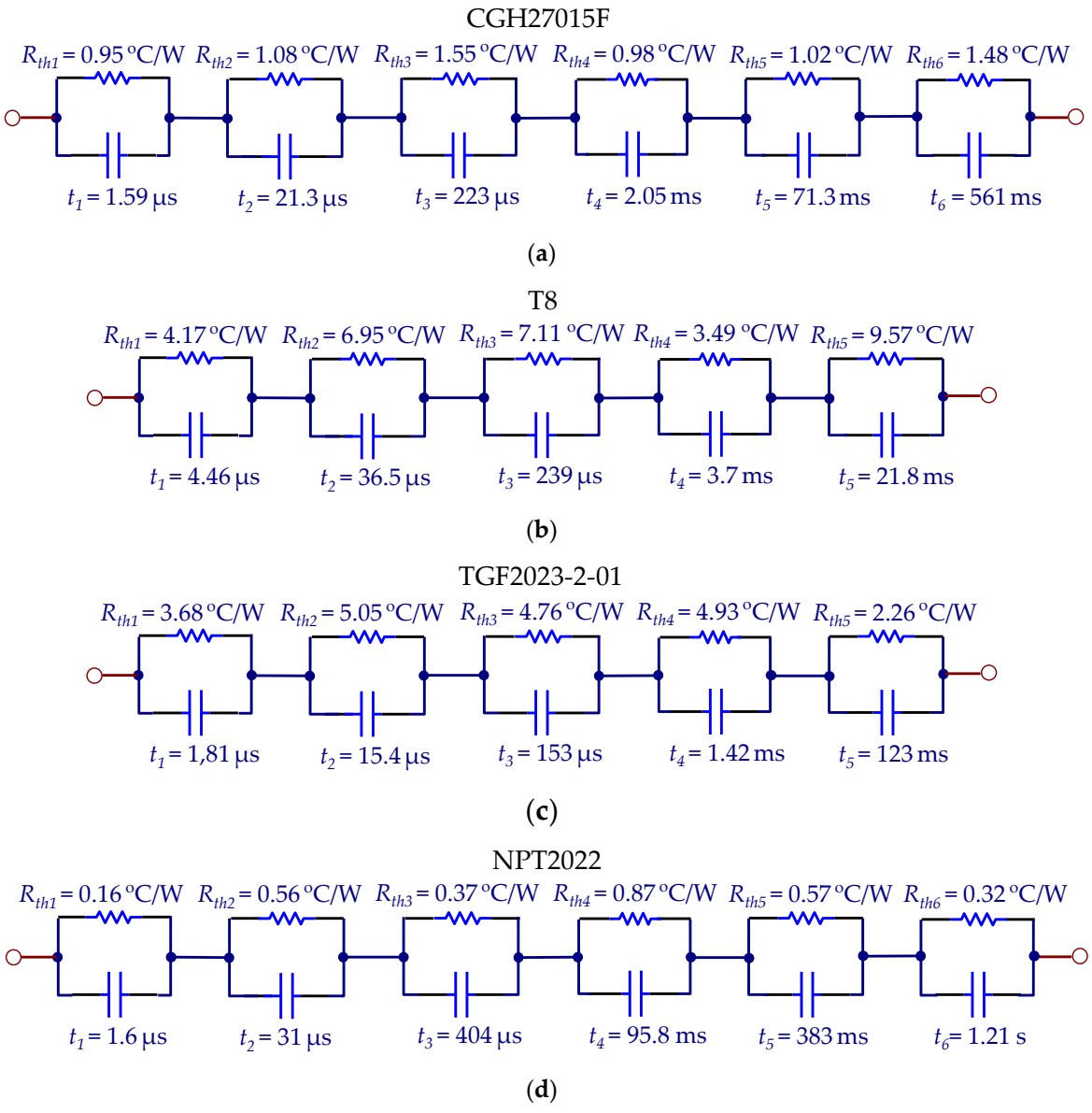


Figure 8. (**a**) CGH27015F (Wolspeed), (**b**) T8 PolHEMT, (**c**) TGF2023-2-01 (Qorvo), (**d**) NPT2022 (MACOM) thermal GaN HEMT models.

As shown in Figure 8, the thermal models of packaged devices CGH27015F and NPT2022 are more complicated than T8 and TGF2023-2-01 die models. The last thermal cell in CGH27015F and NPT2022 models correspond to flange (or package) and thermal attachment to the cooling plate. Thermal time constants referred to individual epi-layers of GaN HEMT and depend on the sizes and material properties. However, it is rather impossible to identify in such a way physical properties of GaN-based epi-layers as the 3-D thermal problem has been reduced to the equivalent of a lumped element.

To verify thermal impedance measurements the transistor T8 was thermal modeled using 3-dimensional equation of heat conduction which is solved by means of FDTD method [12–26]. The T8 die modeled GaN HEMT structure and the assumed heat model flow are shown in Figure 9a,b, respectively. The heating area was located under the top transistor metallization, marked "red" in Figure 9. The constant heat density across all heating areas was assumed. The thermal parameters of transistor materials were constant and temperature independent too. Their values are shown in the transistor heat model flow. To reduce the simulation time the adoptive mesh was applied. The minimal mesh size was 1 µm and it was at the top of thermal structure. The calculations were performed in MATLAB. Due to the very time-consuming calculations the thermal plate size was reduced. The simulation of T8 thermal impedance $Z_{th}(t)$ take about 24 h on PC equipped with i7 Intel processor and 16 GB RAM. The simulations and measurements of thermal impedance $Z_{th}(t)$ of GaN HEMT T8 are shown in Figure 10.

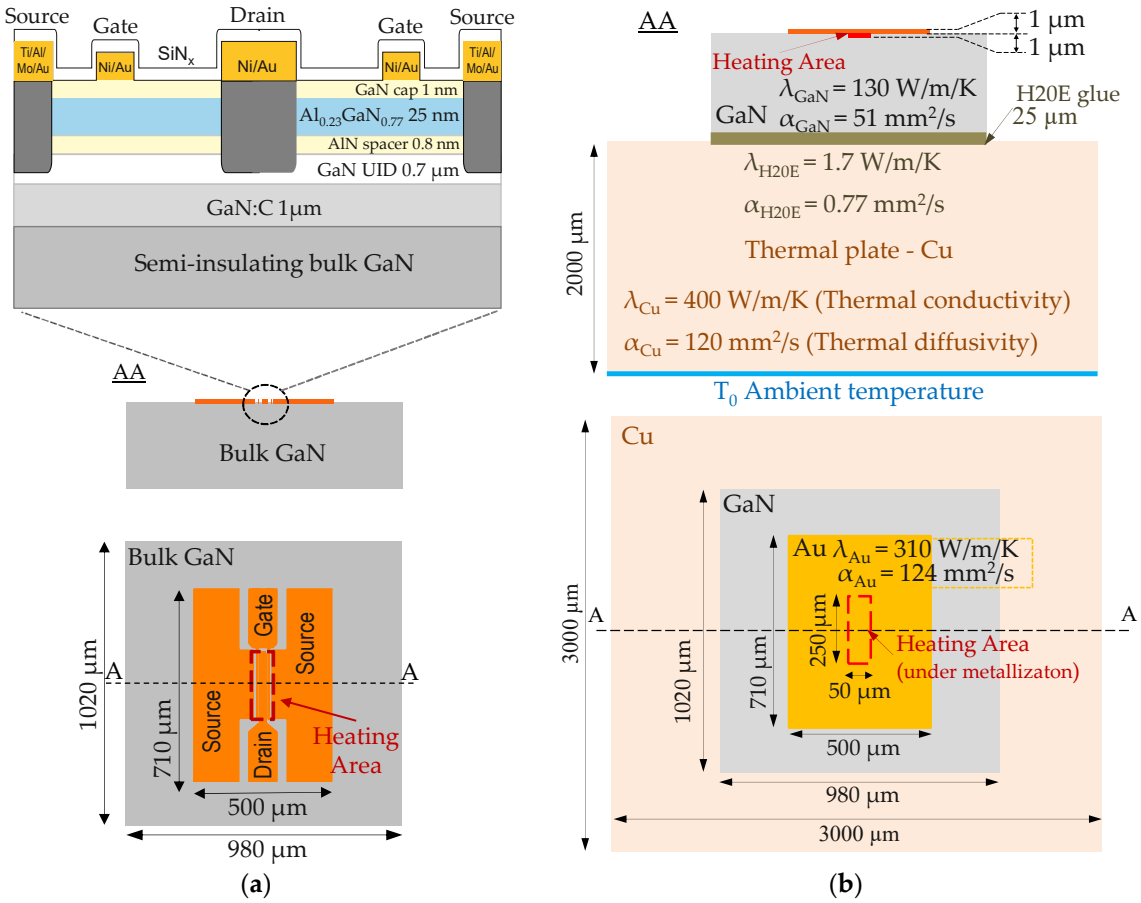


Figure 9. (**a**) GaN-on-GaN HEMT T8 structure; (**b**) T8 thermal model for FDTD simulation.

As shown in Figure 10, the $Z_{th}(t)$ calculations and measurements are consistent. The highest difference is at the beginning of $Z_{th}(t)$ characteristic and it is probably caused by the too large mesh of 1µm. The HEMT heating area thickness across vertical direction is much smaller.

Good compliance of the thermal measurements with the manufacturer's data was also achieved. For example, the thermal resistance measurement of CGH27015F is $Z_{th}(t \to \infty) = 7$ °C/W (Figure 5a) while R_{th} value given in the datasheet is 8 °C/W in the section "absolute maximum ratings" [27]. R_{th} values given by manufacturers are usually the "worst case" across the production.

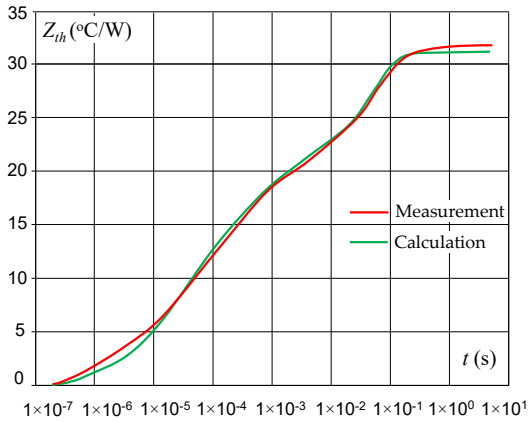


Figure 10. Calculated and measured thermal impedance $Z_{th}(t)$ of GaN-on-GaN HEMT T8.

Analyzing thermal characteristics (Figures 5 and 7) and thermal models shown in Figure 8a,d of packaged transistors CGH27015F and NPT2022 a significant difference in thermal resistance of GaN HEMTs on SiC and Si substrates may be observed. Considering only semiconductor structure (without flange) of both HEMTs with scaling factor ca. 5 (as output power ratio with correction for size of chip and package) GaN-on-Si HEMT NPT2022 R_{th} exceeds 9 while for GaN-on-SiC HEMT R_{th} is approx. 4.5 °C/W. This fact has been confirmed during measurements of the L-band 100 W amplifier with NPT2022 under pulse and CW (continuous wave) operation conditions. In case CW amplifier excitation, far below maximal output power obtained at the pulse operation, both output power and gain dropped sharply [28]. Moreover, the case temperature increased rapidly above recommended value by manufacturer. To correctly compare thermal properties of GaN-on-SiC HEMT (Quorvo TGF2023-2-01) and GaN-on-GaN (T8 HEMT) their size ought to be normalized, i.e., the size of TGF2023-2-01 scaled down to the size of T8 structure. Taking into consideration that GF2023-2-01 is ten-gates structure of 0.3 µm length and 1.25 mm width while T8 HEMT is two-gates of 0.8 µm length and 500 µm width and that the thickness of SiC substrate stands for 90% of the total thickness of GF2023-2-01 HEMT while T8 consists of lattice-matched GaN-based structure one would expect two times higher thermal resistance of GaN-on-GaN HEMT while in reality it is only 30% higher. The reason for that is boundary-effect leading to additional thermal boundary resistance at the interface of SiC substrate and GaN-based epi-structure in GaN-on-SiC HEMT [29,30].

4. Conclusions

Novel approach to characterizing self-heating process in GaN-based HEMTs has been proposed. It relies on measuring thermal impedance $Z_{th}(t)$ basing on MIL-STD-750D-3 standard and followed by solving 3-D heat conduction equation by means of FDTD. The thermal impedance $Z_{th}(t)$ of the GaN HEMT is calculated from the gate-to-source voltage measurements of the forward biased diode during cooling time after the heating pulse. A characteristic feature of our method is that during the heating phase the HEMT is biased at the operating point in which it will operate during its normal use in the transmitter's amplifiers of modern radar and wireless communication systems. Furthermore, the time delay between the heating end and the start of monitoring of V_{GS} samples is less than 100 ns while the commercial measurement systems typically have delays as long as 5 µs. The $Z_{th}(t)$ characteristics enable the thermal time constants to be calculated.

The above procedures have been successfully applied to characterization of various commercial GaN HEMTs, namely CGH27015F (Wolfspeed) and TGF2023-2-01 (Qorvo) on SiC substrate, and NPT2022 (MACOM) on Si substrate as well as with T8 laboratory GaN-on-Ammono GaN HEMT.

The value of thermal resistance R_{th} values calculated using thermal measurements for commercially available GaN-on-SiC HEMTS are consistent with manufacturer's data. The impact of material substrate on thermal features of GaN-based transistors is clearly visible. Specifically, GaN-on-Si HEMTs show

much worse thermal parameters than GaN-on-SiC. The thermal characteristics of dies i.e., TGF2023-2-01 and T8 are very similar.

The main advantage of the proposed approach is that it allows taking into account the self-heating effect of transistors during design of microwave devices. That kind of knowledge can be very important in the design of high-power amplifiers for systems using variable-envelope signals such as LTE-A and 5G radios. In addition, our method enables the thermal time constants referred to the individual GaN HEMT layers to be identified. The obtained multi-section thermal equivalent circuit of transistor and resulting thermal model may be included in GaN HEMT electrical models which are implemented in popular RF and microwave simulators. Since the GaN HEMT consists of several layers, each with different thermal properties, our measurements allow evaluating heat flow across the structure as well as determining an attachment quality die to flange or package. This is especially important when designing amplifiers with transistor chips or transistors in housing for soldering on printed board circuits (PCB).

Author Contributions: Conceptualization, D.G. and W.W. concept and implementation of modified DeltaVGS measurement system, E.K. and A.P.; GaN-on-SI Ammono GaN HEMTs, conceiving building blocks and process flow of device structures, methodology, D.G. and W.W.; GaN HEMT thermal impedance measurements, software, D.G. and W.W.; software development, calculation of parameters of GaN HEMT thermal equivalent circuits, simulations of GaN HEMT thermal characteristics using 3-D FDTD method, validation, D.G., W.W. and A.P.; formal analysis, W.W.; investigation, D.G., W.W., E.K. and A.P.; resources, D.G., W.W., E.K. and A.P.; original draft preparation, W.W.; manuscript review and editing, E.K. and A.P.; visualization, D.G. and W.W.; supervision, W.W. and A.P.; project administration, A.P.; funding acquisition, W.W. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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Vertical Integration of Nitride Laser Diodes and Light Emitting Diodes by Tunnel Junctions

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Abstract: We demonstrate the applications of tunnel junctions (TJs) for new concepts of monolithic nitride-based multicolor light emitting diode (LED) and laser diode (LD) stacks. The presented structures were grown by plasma-assisted molecular beam epitaxy (PAMBE) on GaN bulk crystals. We demonstrate a stack of four LDs operated at pulse mode with emission wavelength of 453 nm. The output power of 1.1 W and high slope efficiency of 2.3 W/A is achieved for devices without dielectric mirrors. Atomically flat surface after the epitaxy of four LD stack and low dislocation density is measured as a result of proper TJ design with optimized doping level. The strain compensation design with InGaN waveguides and AlGaN claddings is shown to be crucial to avoid cracking and lattice relaxation of the 5 µm thick structure. Vertical connection of n-LDs allows for cascade emission of photons and increases the quantum efficiency n-times. The two-color (blue and green) LEDs are demonstrated. Application of TJs simplifies device processing, reducing the need for applications of *p*-type contact. The key factor enabling demonstration of such devices is hydrogen-free PAMBE technology, in which activation of buried *p*-type layers is not necessary.

Keywords: molecular beam epitaxy; nitrides; laser diode; tunnel junction

1. Introduction

The main breakthrough in III-N optoelectronic devices was related with the development of the *p*-type Mg doped layers [1]. The relatively poor *p*-type conductivity and fabrication of low resistance ohmic *p*-type contacts are still among the most challenging issues in nitrides. Recently, increased attention has been dedicated to the interband tunnel junctions (TJs) [2] for the efficient conductivity conversion from *p*-type to *n*-type in III-nitride devices [3–7]. Application of tunnel junctions (TJs) offers more freedom in device design—e.g., it eliminates the need for *p*-type contact deposition [5,8–10]. However, the utilization of TJs in wide band semiconductors is a counterintuitive approach because it is well known that the tunneling probability through *p*–*n* junction decreases exponentially with the energy gap. The additional complication, which slowed down the progress of the nitride TJs' development, was related with the *p*-type doping procedure used by metal-organic vapor phase epitaxy (MOVPE), the dominant technology for the nitride optoelectronics devices. In MOVPE it is difficult to activate the *p*-type conductivity in the (In)GaN:Mg layers that are buried below *n*-type layers due to the fact that diffusion of hydrogen is completely blocked through *n*-type layers [6,11–13].

The issue with the activation of the Mg doped *p*-type layers is not present for the hydrogen-free plasma-assisted molecular beam epitaxy (PAMBE) technology. In PAMBE, hydrogen is not incorporated into GaN:Mg layers, therefore there is no passivation of Mg dopant and no need for post-growth annealing. For this reason, PAMBE seems to be much better suited than MOVPE for practical realization of the vertical devices with buried *p*-type layers [14]. Recently, making use of PAMBE, it was shown that TJs' resistance for wide bandgap semiconductors can be significantly reduced by making use of the piezoelectric fields in the region of the junction [3,7]. The use of piezoelectric fields and heavy *p*- and *n*-type doping levels allowed us to reduce the TJs' resistance to a level appropriate for a demonstration of the continuous wave operation of nitride laser diodes (LDs) [14].

Efficient TJs enable the realization of different vertical designs of optoelectronic devices. Namely: (1) stacks of LDs or (2) multicolor light emitting diodes (LEDs). The multicolor LEDs can pave a way for efficient low energy consumption matrix displays. The stack of LDs is very attractive for many applications where pulse mode operation is required, such as gas sensing, printing and environment pollution control, or light detection and ranging (LIDAR) in cartography, automotive and industrial systems [15]. It can be very cheap and viable alternative to the arrays of LD bars. It provides much simpler coupling of the light coming from the stack of LDs with external optics than from arrays of LDs, since the spatial separation between vertical devices is two orders of magnitude smaller than for arrays of LD bars. The simultaneous operation of a cascade of *n* LDs increases the slope efficiency (SE) of the full device *n*-times, which makes high-power lasing conditions accessible for smaller currents. In addition, the level of catastrophic optical damage (COD) is *n*-times higher in comparison with a single LD. In spite of the increasing interest, there is only one report on a stack of two III-N LDs grown by MOCVD, which shows very weak evidence of simultaneous laser action from both active regions [16]. This is probably due to difficulties with Mg acceptors activation in buried *p*-type layers. Making use of the PAMBE technology we already demonstrated that it is possible to grow monolithically a stack of two LDs operating at two different wavelengths [17].

In this work we will go a step further and investigate a stack of four LDs operating at the same frequency interconnected by TJs. We demonstrate that by making use of the strain compensation concept, it is possible to grow a 5 μm nitride structure containing thick InGaN and AlGaN layers without generation of lattice relaxation. In addition, we demonstrate the potential of PAMBE for growth of vertically integrated multicolor LEDs.

2. Materials and Methods

2.1. Laser Diodes

The epitaxial structure of the LD stack presented in this work was grown entirely by PAMBE on bulk (0001) GaN crystal with the miscut of 0.5°. The substrate was a commercially available Ammono-GaN crystal with low threading dislocation density (TDD) about 10^5 cm^{-2} [18]. The structure consists of four LD segments interconnected by TJs, as shown schematically in Figure 1a,b. At the top of each LD structure the TJ is placed, which makes it ready for the growth of a subsequent LD. The TJs are located far away (approximately 500 nm) from the waveguides of the LDs to avoid generation of additional optical losses due to heavy *p*-type doping. For such a design, the calculated optical mode overlap with the TJ is extremely low in the order of 10^{-7}. Assuming even a high absorption loss of $\alpha = 4000$ cm^{-1}, the resulting optical loss should be at the level of 0.01 cm^{-1}, which is negligible.

Details of the epitaxial structure of one LD segment with a TJ on top are presented in Figure 1b. At the bottom of each LD there is a 400 nm $Al_{0.05}Ga_{0.95}N$:Si cladding (except the most bottom laser diode, LD4, in which the cladding thickness was 700 nm). The LD segment consists of a 220 nm $In_{0.04}Ga_{0.96}N$ waveguide and a 25 nm $In_{0.17}Ga_{0.83}N$ single quantum well (SQW) [19]. Above the waveguide a 20 nm $Al_{0.14}Ga_{0.86}N$:Mg electron blocking layer (EBL) is placed. EBL is doped with Mg at the level of 2×10^{19} cm^{-3}, followed by upper $Al_{0.05}Ga_{0.95}N$:Mg cladding (Mg doping level is 1×10^{18} cm^{-3}). The TJ region consists of 60 nm $In_{0.02}Ga_{0.98}N$:Mg, a 10 nm $In_{0.17}Ga_{0.83}N$ quantum well

(QW), and 20 nm $In_{0.02}Ga_{0.98}N$:Si. The $In_{0.02}Ga_{0.98}N$ barriers are doped with Mg and Si at the levels of 2×10^{19} cm^{-3} and 4×10^{19} cm^{-3}, respectively. First, 5 nm of the QW is heavily doped with Mg at the level of 1.6×10^{20} cm^{-3} while the following 5 nm of the QW is *n*-type doped at the level of 1.8×10^{20} cm^{-3}. The Mg and Si doping profiles in TJs were optimized to achieve atomically flat surface without defects, which is essential for the growth of the subsequent devices on top within the stack.

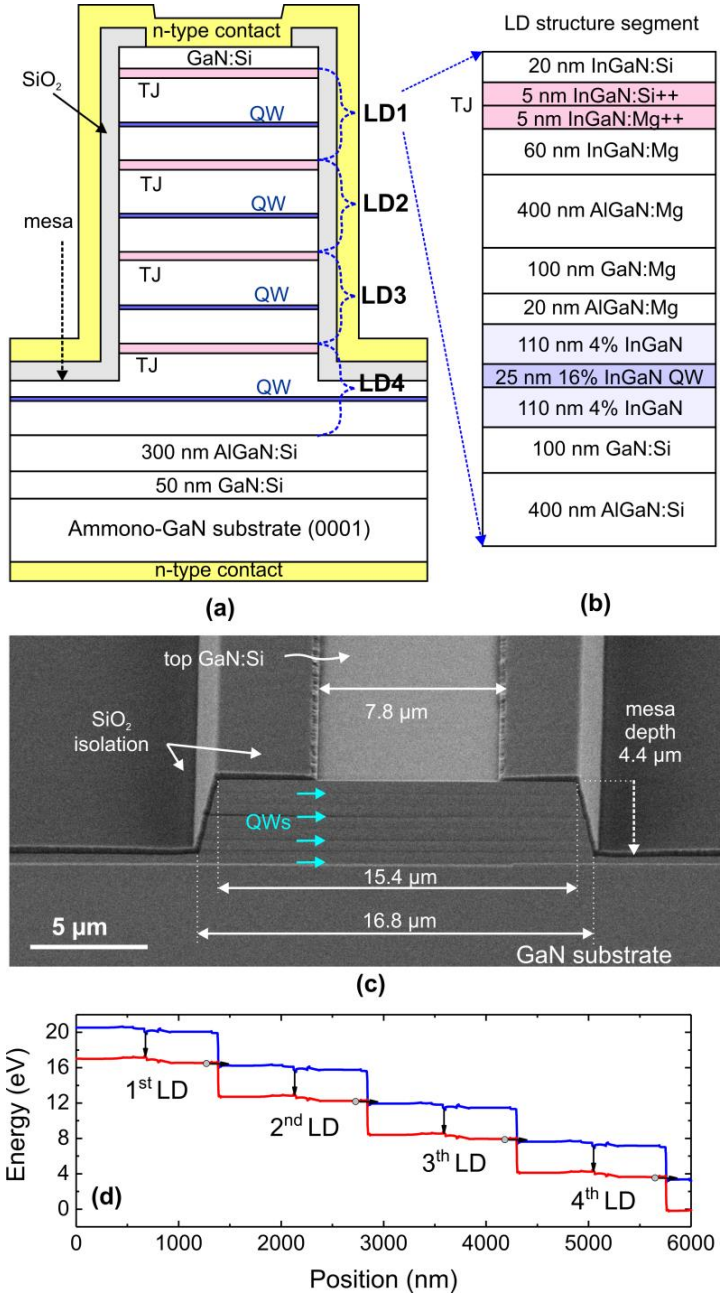

Figure 1. (**a**) Schematic image of the processing design of a stack of four laser diodes (LDs) grown by plasma-assisted molecular beam epitaxy (PAMBE); (**b**) detailed layer structure of a single LD segment; (**c**) scanning electron microscopy (SEM) image of laser mesa viewed at 45° at cleaved laser facet; (**d**) band diagram of stack of four LDs.

The growth conditions of the four LD stack were the same as for a single LD and they are described in detail elsewhere [20]. The growth temperatures were 730 °C for GaN and 650 °C for InGaN layers, respectively. The temperature on the grown surface was monitored (and adjusted if necessary) by laser reflectometry described in detail in [21]. We would like to mention here that the entire structure

was grown on planar GaN substrate without special patterning applied to reduce strain caused by thick AlGaN claddings [22]. The growth of thick AlGaN claddings usually leads to the cracking of the structures. Application of InGaN waveguides surrounded by AlGaN claddings results in strain compensation and allows us to grow such thick structures without lattice relaxation. It is important to stress here, that such an approach allows us also to achieve flat wafers, which is important for device yield during the processing of lasers.

The LDs were processed as a ridge waveguide with the dimensions of 15 μm × 1000 μm. The 4.4 μm deep mesa was formed by reactive-ion etching (RIE) through active regions of the 3 LDs and reaching almost the EBL of the fourth LD (see Figure 1c). The mesa was covered by SiO_2 dielectric. To ensure that the metal contacts will not make a short cut on the mesa sidewalls, the top of the mesa region was also covered partially by SiO_2 (see Figure 1c). The overlap of the dielectric on the mesa surface reduces the size of the metal contact. The metal contact width is about 8 μm, while mesa size is 15 μm. It could be a challenge for standard LDs with *p*-type contact, in which low conductivity of *p*-type material restricts lateral carrier distribution to distances below 1 μm. This could lead to non-uniform current spreading through such processed LDs. However, in our design, the electrons can easily travel from metallization to the mesa edges (*n*-type contact: Ti/Al/Ni/Au) because the current spreading layer is *n*-type. The processed devices were cleaved and tested without dielectric mirror coatings.

The band diagram for the studied LD stack is shown in Figure 1d. Arrows indicate the electron recombination in the QWs and tunneling though the TJs.

2.2. Light Emitting Diodes

The schematic diagram of the stack of 2 LEDs operated at different wavelengths for color mixing is presented in Figure 2. The schematic working idea shown in Figure 2a explains that the power supply of the studied device can be applied either to the whole structure or separately to each of the LEDs. The structure was grown on conductive commercial GaN substrate (Saint Gobain Lumilog) with TDDs in the range from 5×10^6 to 1×10^7 cm^{-2}. Layer sequence is presented in Figure 2b. After 30 nm $In_{0.08}Ga_{0.92}N$ layer, two 2.8 nm $In_{0.23}Ga_{0.77}N$ QWs were grown with 20 nm $In_{0.08}Ga_{0.92}N$ barriers, followed by 20 nm $Al_{0.15}Ga_{0.85}N$:Mg EBL, 100 nm GaN:Mg and the first TJ. Above the first TJ (TJ1), the 100 nm $In_{0.02}Ga_{0.98}N$ doped with Si at the level 5×10^{18} cm^{-3} was located. Then, the second LED was grown—with In content of 17% inside two 2.8 nm InGaN QWs. On top of the second LED, the second TJ (TJ2) was located, followed by 100 nm GaN doped Si at the level of 5×10^{18} cm^{-3}. The upper GaN:Si and 100 nm $In_{0.02}Ga_{0.98}N$:Si located between the bottom (green) and top (blue) LEDs were used for efficient lateral current spreading. The TJ design (thickness of the layers) are the same as for the stack of LDs described before. The differences are in the n- and *p*-type doping of the 10 nm TJ QW region (for TJ details, see Figure 1b). For TJ1, we used moderate doping levels (like for LDs described above) to provide high crystal quality, while for TJ2 the doping was increased: $N_{Si} = 4 \times 10^{21}$ cm^{-3}, $N_{Mg} = 5 \times 10^{20}$ cm^{-3}.

Figure 2c presents a high-angle annular dark-field scanning transmission electron microscopy (HAADF STEM) image of the studied two-color LED structure. High indium content layers, such as InGaN QWs and TJs, are brighter than GaN and AlGaN layers. Sharp interfaces and no extended defects indicate high quality growth. The devices (350×350 μm^2 mesa size) were separated by deep dry etching by reactive ion etching (RIE), down to the substrate. The schematic picture of the LED after processing will be presented in the following part of the paper.

The band diagram for the studied structure is shown in Figure 2d. Again, similarly to the LD stack band diagram shown in Figure 1d, the arrows indicate the electron recombination in QWs and tunneling though the TJs.

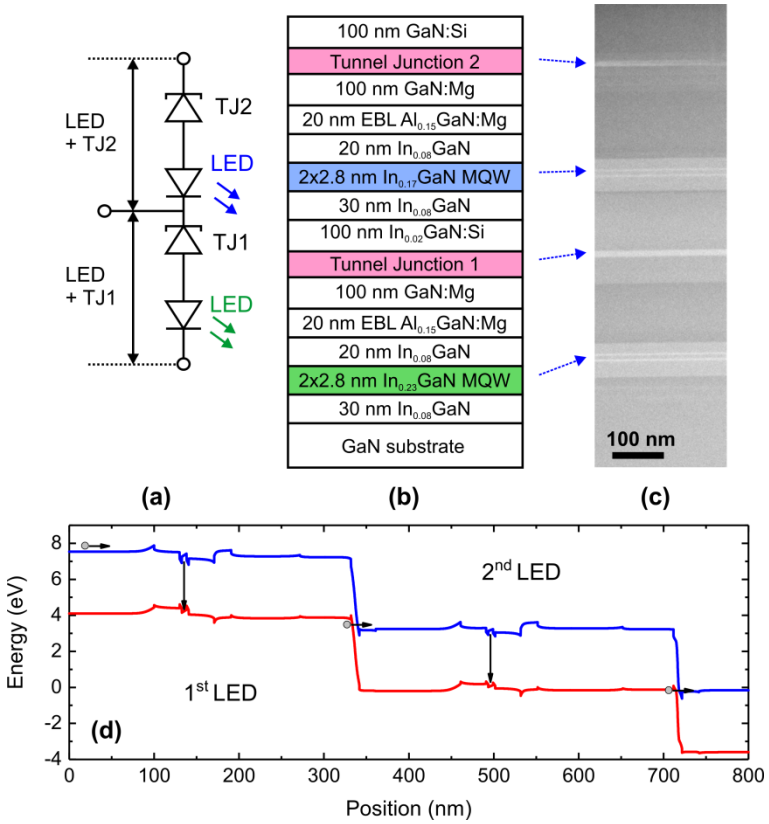

Figure 2. (**a**) Schematic diagram and (**b**) layer sequence of two-color light emitting diode (LED) structure. (**c**) High-angle annular dark-field scanning transmission electron microscopy (HAADF STEM) image presenting the studied two-color LED structure. (**d**) Band structure of two-color LED.

3. Results and Discussion

3.1. Laser Diodes

The LDs were operated with 200 ns long pulses and a repetition rate of 1 kHz. The light–current (L–I) characteristics of the cascade of four LDs are shown in Figure 3a. Three lasing thresholds had been observed: the first one at a current density of 3.8 kA/cm^2 with a slope efficiency of 0.8 W/A; the second one occurred at 5.9 kA/cm^2 and the observed slope efficiency was equal to 1.5 W/A; the third one was at 6.4 kA/cm^2 and the slope efficiency increased to 2.3 W/A. The multiplications of the slope efficiency indicate that the same electrons (and holes) are used three times to generate light—once in each of the three LDs.

To verify the observation of lasing from the LDs' stack, we measured near-field patterns collected using a Gaussian beam telescope setup [23]. Strong filamentation is observed as expected for wide-ridge LDs [24]. At j = 3.8 kA/cm^2, there is only a single near-field pattern for LD1 visible (see Figure 3b). Above the second threshold a second near-field pattern appears below. For current densities higher than 6.4 kA/cm^2, a third peak in the near-field pattern is observed. Further increase of the current density does not change this pattern. This experiment shows that the LDs start the lasing action in the following order: LD1, LD2 and LD3. Furthermore, we observed that LD4 was not lasing. We suspect that the reason why LD4 was not lasing is that the mesa was too shallow. The distance from the surface to the EBL of LD4 is 4.8 µm, while the etching depth measured by SEM (see Figure 1c) was 4.4 µm. Therefore, one can expect very different waveguiding properties for LD4 in comparison to LD1–LD3, which were etched through the whole structure. For LD1–LD3, the optical mode is confined laterally by SiO_2 deposited on the sides of the mesa, while for LD4 the optical mode can spread laterally to unpumped regions (see Figure 1c). This geometry increases the optical confinement factor for LD1–LD3

and increases the internal optical losses for LD4. Therefore, we expect a substantial increase in the lasing threshold current density for LD4.

The maximum optical power obtained for the studied structure was 1.1 W per laser facet and can be further increased using dielectric coatings. Application of this design for *n*-LDs interconnected by (*n*−1) TJs will allow us to increase SE *n*-times. This construction paves a way to achieving III-nitride high-power pulse laser diode stacks for LIDAR applications.

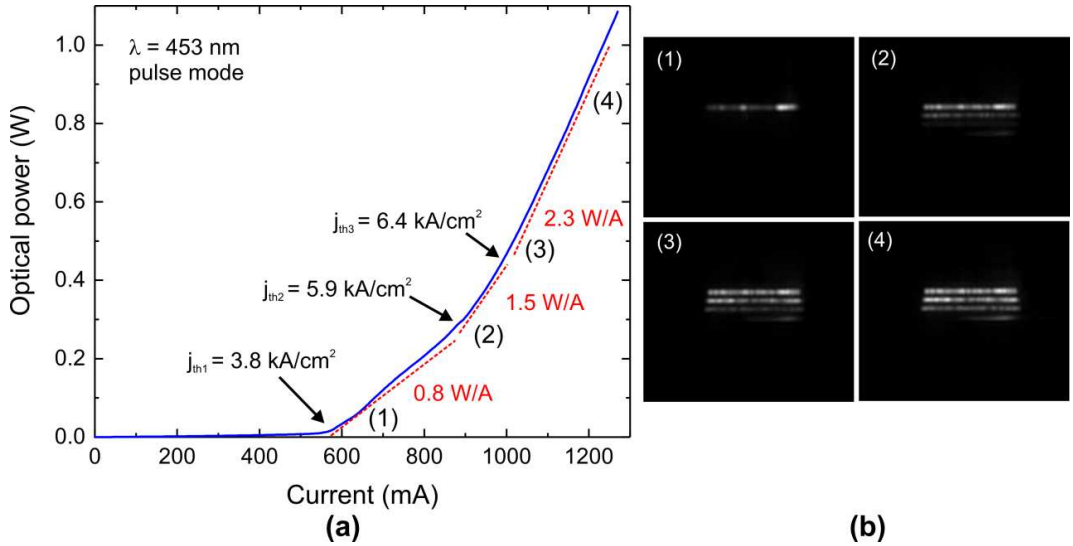

Figure 3. (**a**) The light–current characteristics of the stack of four LDs structure grown by PAMBE. Three lasing thresholds are observed. Total slope efficiency follows the number of lasing devices multiplied by slope efficiency of the first LD; (**b**) the near-field patterns collected by Gaussian beam telescope setup for the lasing regions (1)–(4) denoted in the light–current characteristics.

The important part in the design of the LDs' stack presented in this work is related with optimization of the TJ design and epitaxy. The TJ should have low resistance and the growth should not introduce additional structural defects. In this work, we applied TJ design which consists of InGaN QW to increase the current tunneling probability [3,7]. The *p*- and *n*-type doping levels were optimized to provide low serial resistance of a TJ. However, the *p*-type and *n*-type doping are limited by inherent physical properties or by structural deterioration. For the *p*-type Mg doping, above the doping level 2—5 × 10^{19} cm^{-3}—the self-compensation process is observed, which reduces efficiency of magnesium as an acceptor [25,26]. Contrary to *p*-type, the *n*-type doping is still efficient for very high Si doping levels. Indeed, the increase in the Si doping reduces the tunnel junction resistance, however, for concentrations at the order of 5 × 10^{20} cm^{-3} a deterioration of the surface morphology is observed. The mechanism of this process is probably related to the Si masking effect when the surface is exposed to the very high Si flux. The surface morphology of our four LDs' stack is shown in Figure 4a. The *n*-type Si doping in TJ equals to 1.8 × 10^{20} cm^{-3}. For higher *n*-type doping—above 5 × 10^{20} cm^{-3}—surface roughening is observed, and many dislocations are generated, as shown in Figure 4b. The TJ presented in Figure 4b, was used for our first demonstration of TJ LDs [14]. Heavy Si doping allowed us to achieve a very low resistance TJ; however, high defect density and rough surface morphology would not allow for the growth of subsequent LDs. Note that the surface root mean square roughness measured by atomic force microscope (AFM) at 5 × 5 μm^2 scans is 0.29 nm for the four LDs' stack with optimized TJs and 2.34 nm for the single LD with the highly doped TJ on top of it, see Figure 4a,b, respectively.

The defect density of the four LDs' stack was studied. We used defect-selective etching (DSE) in molten KOH–NaOH eutectics at 450 °C for 15 min. After DSE, etch pit density (EPD) was evaluated using optical microscope images. For a given image, the etch pits are counted per known area and

thus their density is easily calculated. An example of the optical microscope image of the four LDs' stack surface after DSE is shown in Figure 4c, in which the pits (some are marked by arrows) can be observed. In Figure 4c, 24 pits on the area of 13.4 μm^2 result in EPD of 1.8×10^6 cm^{-2}. Note that some pits have a flat bottom that may indicate dislocations generated during epitaxy of the four LDs' stack. The etch pits corresponding to the dislocations which originate from the substrate are denoted with black arrows and their density matches approximately the TDD of the GaN substrates used. The overall low defect density revealed by the DSE shows that the stacking of LDs by TJ using PAMBE is a promising technology for high-power pulse laser diodes [27].

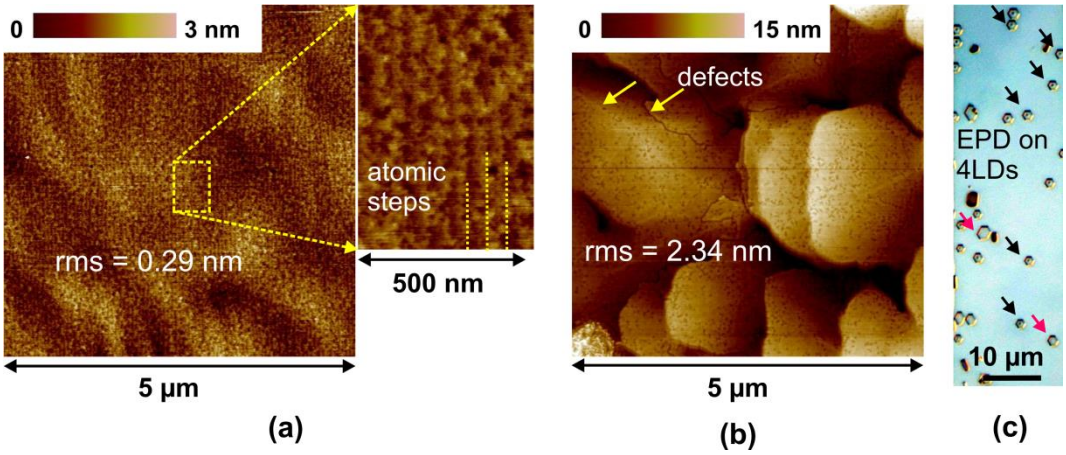

Figure 4. Surface morphology of (**a**) stack of 4 LDs with Si doping in TJ of 1.8×10^{20} cm^{-3}; (**b**) single LD with heavy Si doping in TJ above 5×10^{20} cm^{-3}. (**c**) Optical microscope image of the studied 4 LDs' epitaxial structure after defect-selective etching. Etch pit density is 1.8×10^6 cm^{-2}. Some of etch pits are flat-bottomed, indicated by pink arrows.

3.2. Multicolor Light Emitting Diodes

We analyzed the properties of the device that consisted of two standard LED structures emitting at true blue and green range, interconnected and capped with heavily doped $In_{0.02}Ga_{0.98}N/In_{0.17}G_{0.83}aN/In_{0.02}Ga_{0.98}N$ TJs. The device structure is presented in Figure 2. The electroluminescence taken at different currents is presented in Figure 5 and two emission lines centered at 466 nm and 530 nm are visible. For the bottom and top of the LEDs' stack we used *n*-type Ti/Al/Ni/Au contacts. Two-color LED operates at reasonably low voltages of about 8 V for currents around 150 mA. It is important to point out that the light is extracted through the upper LED region which is not covered by metallization. This is characteristic for TJ LEDs—since electrons are more mobile than holes and TJ enables efficient horizontal current spreading. As an example, in Figure 6 we demonstrate the electroluminescence of our TJ LED devices with different shapes of upper contact metallization which defines the output light pattern.

Further development of such device, when adding the third LED, emitting red color, could lead to a phosphorous-free white LED. We would like to stress here that vertical interconnection by TJs also simplifies the processing of individually addressed LED devices. This could be interesting for the future design of multicolor LED matrix displays. In Figure 7a, a schematic diagram of the etched structure is presented. To obtain middle contact we partially etched the structure down about 400 nm and deposited *n*-type contact (Ti/Al/Ni/Au) to $In_{0.02}Ga_{0.98}N$:Si doped layer (for structure details see Figure 2). It is a great advantage, since there is no need to fabricate *p*-type contacts on the etched surface of the device, which is a challenging issue. Using this configuration, we can bias each LED individually. In Figure 7b, the Current–Voltage (I–V) characteristics of the upper (blue), bottom (green) and both LEDs are presented. We observe a higher turn-on voltage for the green diode (i.e., TJ1 + green LED) than for the blue diode (TJ2 + blue LED). This effect is probable due to the higher voltage drop on TJ1 in comparison to TJ2. In addition, for the green diode, the increase in turn-on voltage can be caused

by stronger piezoelectric field related to higher indium content in green QWs. As was mentioned before, application of TJs simplifies preparation of the contacts on the etched surface. Here, we applied *n*-type contact between green and blue LEDs. The slope of the I–V curve above the turn-on voltage is a measure of the serial resistance of the device. The green LED and both green and blue LEDs have a similar slope. The increased serial resistance for blue LED is due to lateral resistance of the *n*-type layer located below the blue LED. The electrons must travel from the bottom contact of the blue LED for several microns through $In_{0.02}Ga_{0.98}N$:Si layer doped at moderate values (see Figures 2b and 7a). We can eliminate this effect by increased *n*-type doping of this layer and/or by smaller spacing between mesa and the bottom contact.

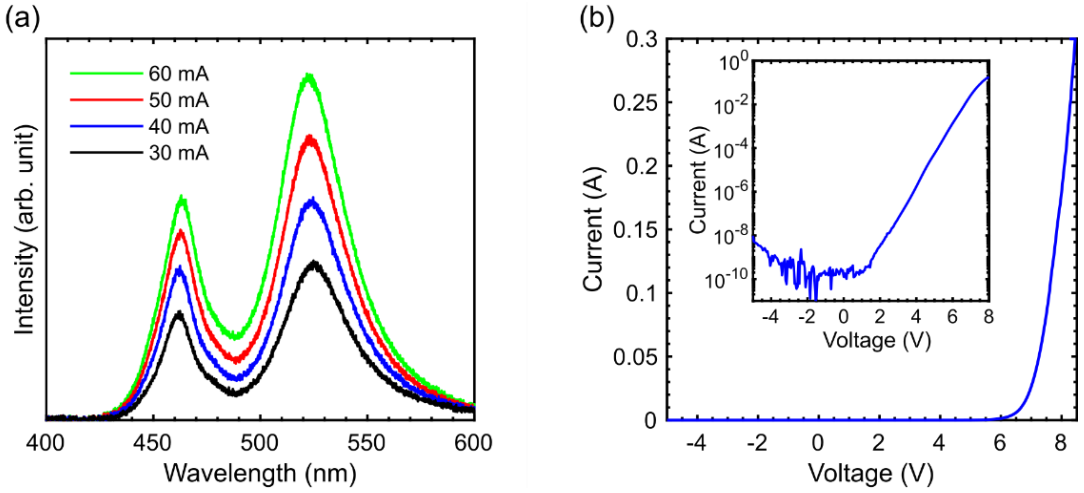

Figure 5. (**a**) The optical spectra of 2 LEDs connected by tunnel junction (TJ) for different driving currents. (**b**) The Current–Voltage (I–V) characteristics for the stack of 2 LEDs; inset to this figure is the same plot in semi-log scale and an indication of very low current leakage in reverse direction.

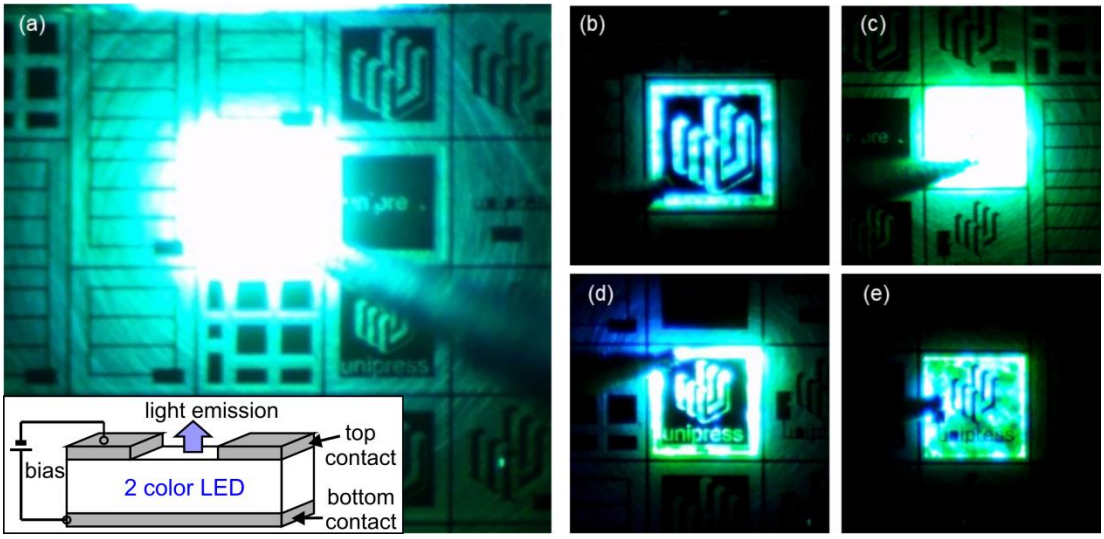

Figure 6. (**a**) The optical microscope image of operating multicolor TJ LEDs with full mesa size of 350 × 350 μm^2, surrounded by other devices. The devices have various geometry of upper metal contact; metallization blocks the light generated in the active region as schematically depicted in the insert and therefore the top contact pads are visible as black. When an LED chip is biased though a needle placed on top, the bright light emission is visible. (**b**–**e**) Operation of LEDs with different metallization patterns.

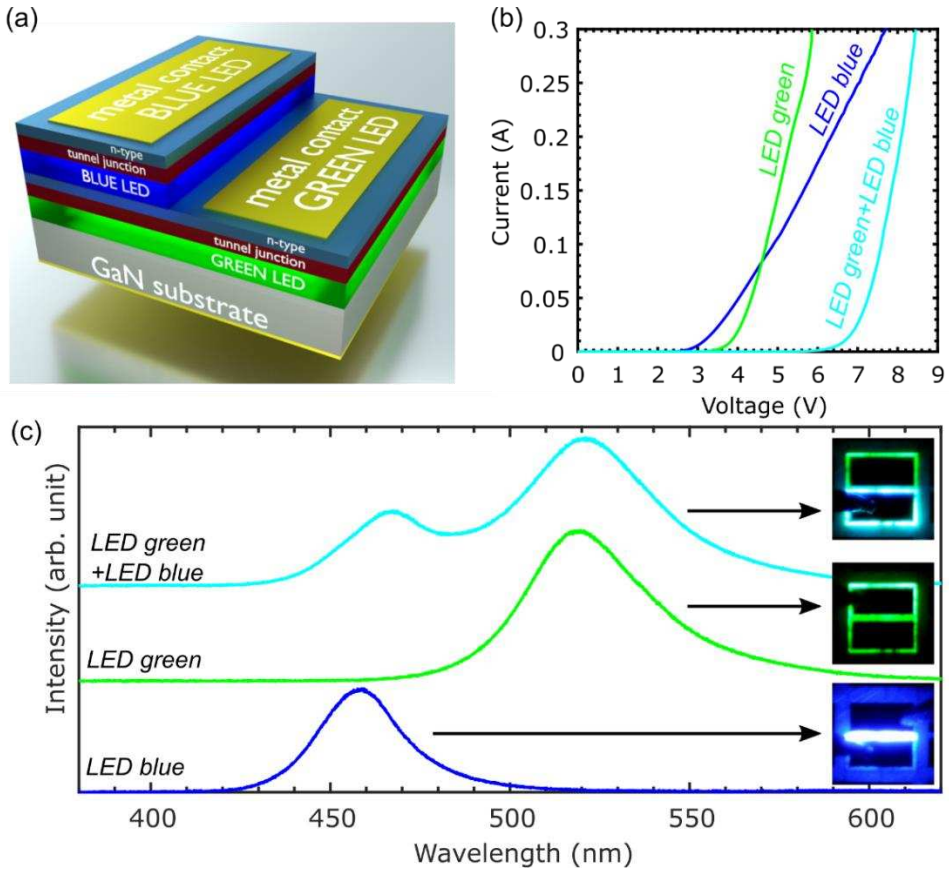

Figure 7. (**a**) Diagram of two LEDs after dry etching and contact deposition. (**b**) I–V and (**c**) spectral characteristics (together with true-color electroluminescence pictures) of blue, green and both LEDs.

4. Conclusions

We demonstrated a stack of four nitride LDs interconnected by TJs grown by PAMBE. We show that it is possible to grow four LDs with a structure almost 5 µm thick without lattice relaxation. Quality of epitaxy and design of TJ are reflected by low dislocation density at the level of low 10^6 cm^{-2}. The lasing wavelength is 453 nm. We show that three LDs are operating simultaneously, and the slope efficiency is increased three times. The first LD started to operate at 3.8 kA/cm^2 with SE equal to 0.8 W/A. When all three LDs were operating, the SE increased to 2.3 W/A. This result, together with the near-field pictures, is proof for simultaneous lasing of three LDs. Application of this design for n-LDs interconnected by $(n - 1)$ TJ will allow us to increase SE n-times. The presented design is a viable alternative to achieving III-nitride high-power pulse laser diodes for many applications such as gas sensing or LIDARs.

We also investigate the stack of multicolor LEDs interconnected by TJs for white color, phosphorus-free LEDs and for LED array displays applications. The use of TJs simplifies the electrical connections to buried LED structures, eliminating the need of p-type contacts application.

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Influence of Si Substrate Preparation Procedure on Polarity of Self-Assembled GaN Nanowires on Si(111): Kelvin Probe Force Microscopy Studies

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Abstract: The growth of GaN nanowires having a polar, wurtzite structure on nonpolar Si substrates raises the issue of GaN nanowire polarity. Depending on the growth procedure, coexistence of nanowires with different polarities inside one ensemble has been reported. Since polarity affects the optical and electronic properties of nanowires, reliable methods for its control are needed. In this work, we use Kelvin probe force microscopy to assess the polarity of GaN nanowires grown by plasma-assisted Molecular Beam Epitaxy on Si(111) substrates. We show that uniformity of the polarity of GaN nanowires critically depends on substrate processing prior to the growth. Nearly 18% of nanowires with reversed polarity (i.e., Ga-polar) were found on the HF-etched substrates with hydrogen surface passivation. Alternative Si substrate treatment steps (RCA etching, Ga-triggered deoxidation) were tested. However, the best results, i.e., purely N-polar ensemble of nanowires, were obtained on Si wafers thermally deoxidized in the growth chamber at ~1000 °C. Interestingly, no mixed polarity was found for GaN nanowires grown under similar conditions on Si(111) substrates with a thin AlO_y buffer layer. Our results show that reversal of nanowires' polarity can be prevented by growing them on a chemically uniform substrate surface, in our case on clean, in situ formed SiN_x or ex situ deposited AlO_y buffers.

Keywords: gallium nitride nanowires; polarity; Kelvin probe force microscopy

1. Introduction

GaN nanowires (NWs) are found as promising building blocks for a future generation of electronic and optoelectronics devices. In general, NWs are almost strain-free objects without lattice misfit defects propagating into the crystalline structure even if grown on highly lattice-mismatched substrates. Therefore, these nanostructures facilitate, for instance, the integration of GaN-based devices with Si electronics. In addition, complicated heterostructures can be ideally grown in the form of NWs with a crystallographic quality not achievable in the case of comparable planar heterostructures. However, the growth of wurtzite GaN nanowires on nonpolar Si substrates raises the issue of GaN NW polarity, which is known to have a critical impact on the structural properties of GaN, such as the incorporation of dopants [1–4], surface reactivity [5] and thermal stability [6], as well as on the nucleation and growth of GaN NWs [7,8]. Polarity also causes the onset of a spontaneous built-in electric field in nitride heterostructures, which, together with a piezoelectric contribution due to strain-related electric polarization, accounts for polarization-induced doping [9] and the formation of two-dimensional electron gas in high-electron mobility transistor structures [10]. Overall, polarity significantly affects

the performance of GaN-based devices, so it must be carefully controlled and kept uniform over a large surface area.

While in planar films one polarization domain may overgrow the other and result in a single film polarity [11], this is very unlikely in NWs due to their low lateral growth rate. It is well established already that GaN NWs grow exclusively under N-rich conditions with the c-axis parallel to the growth direction [12–18]. There is no consensus, however, about NW polarity. Although the majority of self-assembled GaN NWs grown on Si substrates are found to be N-polar, the coexistence of NWs with different polarities inside the NW ensemble has been observed [9,11,19–22]. The formation of mixed-polarity NWs is not fully understood and the parameters influencing this behavior, which include the interface chemistry and the growth procedure, are still under debate. However, it is widely reported that the polarity of self-assembled NWs is determined at the GaN nucleation stage and can be reversed from N- to Ga-polar by the high local surface concentration of impurities like Mg, Si, Ti or O [20,23–30]. These findings clearly indicate that proper substrate preparation is decisive for the achievement of homogeneous polarity. In particular, in the case of growth on Si surfaces, the processing procedure and cleanness of Si further determine the chemical and morphological uniformity of the silicon nitride film created during a Si nitridation step prior to GaN growth. As will be shown, these are critical steps for the successful formation of GaN NW ensembles with uniform N polarity.

In this work, we tested the procedures commonly used to prepare Si(111) substrates prior to plasma-assisted molecular beam epitaxial (PAMBE) growth of GaN NWs regarding their impact on the polarity of ensembles of self-assembled GaN nanowires. From a wide range of techniques used to determine the polarity of NWs (see [31] for a review), Kelvin probe force microscopy (KPFM) was chosen. By contrast to the techniques based on electron microscopy which require complicated sample preparation, are time-demanding and may lead to sample damage, KPFM allows the polarity assessment of a statistically significant number of single NWs over micrometer large surface areas with nanometer resolution and without the need of any special sample preparation [32]. Our studies show that the uniformity of the polarity of GaN NWs on Si(111) strongly depends on the procedure used for the substrate processing prior to NW growth. Interestingly, no mixed polarity was found for GaN NWs grown under similar conditions on Si(111) substrates covered by a thin amorphous AlO_y buffer layer [33,34]. This shows the crucial role the chemistry at the GaN/Si(111) interface plays for the determination of GaN NWs polarity.

2. Experiment

The samples used in this study were grown by PAMBE using a solid-source effusion Ga cell and the radio frequency Addon nitrogen plasma source controlled by an optical sensor of plasma light emission [35]. All samples were grown on n-type low-resistivity (1–30 Ωcm) silicon (111) substrates. Five of them, later referred to as samples A–E, were grown on bare silicon and they differ only by the procedure used for Si substrate cleaning before epitaxial growth. Details of these procedures are listed in Table 1. Irrespective of substrate preparation, all wafers were transferred in air to the PAMBE system and outgassed in the loading chamber at ~150 °C for 1 h and then at ~400 °C in the preparation chamber for 2 h to remove any volatile contamination before the transfer to the growth chamber. The substrate temperature was calibrated prior to growth on bare Si(111) substrate by observation of the 7×7 to 1×1 reflection high-energy electron diffraction (RHEED) pattern transition at 830 °C [36,37]. The growth procedure started by exposing silicon substrates to an active nitrogen flux for 15 min at 750 °C. The aim was to create a thin SiN_x film on the surface as explained in detail in our previous report [17]. Finally, the Ga source was opened to induce incubation of three-dimensional GaN islands which subsequently transformed to NWs [38–41]. In addition, sample F was grown on Si(111) deoxidized by the HF dip, similar to sample A, and then transferred in air to the atomic layer deposition (ALD) system for the deposition of a 15 nm thick amorphous AlO_y buffer layer at 85 °C [42]. Then, the substrate was loaded to the PAMBE system, degassed in loading and preparation chambers as for the rest of the samples and transferred to the growth chamber. No substrate nitridation was used for that sample and, after

reaching the growth temperature and ignition of the N source, the Ga and N shutters were opened simultaneously to start the growth. All samples reported in this work were grown at the temperature of 750 °C and under nitrogen-rich conditions (N/Ga flux ratio of 1.8) to promote NW growth.

Table 1. Substrate preparation steps used for samples A–F. The last column shows the number of nanowires (NWs) analyzed by KPFM and the percentage of NWs with a polarity flip from N to Ga.

Sample	Description of Si Substrate Processing Procedure	% of Ga-Polar NWs
A	Aqueous HF dip followed by thermal desorption of hydrogen passivation in the growth chamber at ~700 °C	18% Ga-polar (125 NWs tested)
B	RCA clean followed by thermal removal of silicon oxide in the growth chamber at ~950 °C for 10 min	4% Ga polar (50 NWs tested)
C	Procedure as for sample B followed by 2 × Ga-induced deoxidation steps in the growth chamber	<3% Ga-polar (180 NWs tested)
D	Thermal oxide desorption in UHV at ~1000 °C for 10 min followed by 2 × Ga-induced deoxidation steps as for sample C	0% Ga-polar (225 NWs tested)
E	Thermal native oxide desorption in the growth chamber at ~1000 °C for 10 min	0% Ga-polar (120 NWs tested)
F	Aqueous HF dip as for sample A followed by transfer in air to the ALD system for deposition of AlO_y buffer	0% Ga-polar (>400 NWs tested)

Frequency-modulation KPFM was used to nondestructively determine the polarity of individual NWs within the assembly. The technique is based on the local measurement of the contact potential difference (CPD) between the NW top facet and the atomic force microscopy (AFM) tip [43,44]. Assuming similar electron affinities in N- and Ga-polar GaN, the measured CPD is used to reveal differences in the work function between polar faces [31], which allows their identification [45]. Calibration of the tip contact potential was performed by measuring the CPD on the N- and the Ga-polar facets of a GaN bulk sample grown by hydride vapor-phase epitaxy. For all Pt-coated tips used, the resulting CPD was typically comprised in the interval of 0.20–0.35 V for the Ga-polar face and 0.75–0.90 V for the N-polar face, the difference between N- and Ga-polar faces measured with the same tip being constant (0.55 ± 0.05 V). Complementary images of KPFM, namely topography and contact potential difference, were analyzed [32]. They allow measuring the polarity of individual NWs over an area of tens of μm^2 and provide good statistics on the polarity of the ensemble.

3. Results and Discussion

Figure 1a shows the AFM topographic view image of sample A. The NWs have a diameter of ~200 nm, but this is convoluted with the tip, which has a diameter of ~20 nm. Figure 1b shows a CPD map of the same area. Some darker NWs, marked by blue arrows, are clearly visible on the map. Figure 1c,d present the CPD value and NW height profiles along the green line, respectively. As seen in Figure 1b,c, the mean CPD value for the majority of the NWs is ~1000 mV, which is compatible with their N polarity. On the contrary, for dark NWs marked by blue arrows, the CPD values drop to ~350 mV. Those values could be attributed to a reverse polarity in Ga-polar NWs. As shown in the last column of Table 1, nearly 18% of 125 NWs checked in total in sample A exhibited reversed polarity.

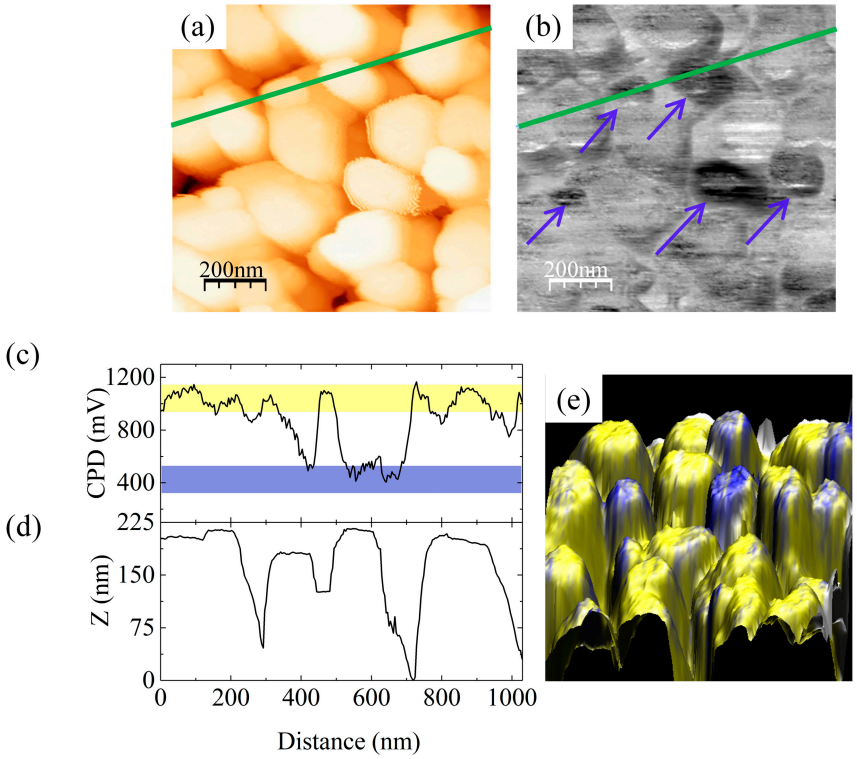

Figure 1. (**a**) AFM topographic view image (1 × 1 μm^2, color scale from 0 to 370 nm) and (**b**) the corresponding contact potential difference (CPD) map (color scale from 0 to 1.5 V) of sample A. Blue arrows in (**b**) mark Ga-polar NWs. The CPD value and NW height profiles along the green line, (**c**) and (**d**), respectively. (**e**) shows the 3D superposition of the topography (xyz axis) and CPD value (color scale). Blue marks Ga-polar and yellow N-polar NWs.

Dipping of the as-received wafer in diluted (~5%) HF acid is the most commonly used procedure for Si substrate preparation before GaN NWs growth by PAMBE [46–50]. This is due to the simplicity of the technique. Moreover, the high-temperature substrate heater required by other methods is not needed. There are a number of studies showing that etching of silicon in a solution of HF removes native silicon oxide and results in hydrogen-terminated and locally ordered surfaces. [51–54]. The hydrogen surface passivation provides protection against oxygen during the wafer transfer to the ultra-high vacuum (UHV) system, where it is removed by annealing at moderate temperatures. Unfortunately, it degrades with exposure to air and moisture. Therefore, the efficiency of surface protection critically depends on the handling of the etched sample. In particular, the time of surface exposure to the laboratory air before transfer to the UHV chamber must be made as short as possible. Moreover, the use of a glove box with dry inert atmosphere connected to the load lock chamber to prevent exposure of the freshly etched sample to oxygen is recommended [55].

Mixed polarity of GaN NWs grown by PAMBE on HF-treated Si substrates is widely observed. Concordel et al. reported the amount of Ga-polar NWs to be below a small percent [20], while the KPFM studies by Minj et al. revealed ~5% of GaN NWs with Ga instead of N polarity [32]. Although these values are much lower than those found in our study, direct comparison is not straight forward since most publications do not provide a precise description of how the freshly etched substrates have been handled.

In the case of sample A, prior to the NW growth, the Si(111) substrate was etched in 5% aqueous HF solution for 1 min, followed by a short deionized water bath and drying with nitrogen. Then, it was transferred in air to the MBE system. The freshly etched substrate was exposed to the air for ~10 min until pumping of the load lock chamber started. After initial thermal treatment in the load chamber as described in Section 2 above, the hydrogen passivation was removed by substrate

annealing in the growth chamber at a temperature of ~700 °C. This resulted in a sharp 7 × 7 RHEED pattern characteristic of a clean, oxide-free Si(111) surface. Despite that, presumably some oxide islands were left on the surface. As proposed by Borysiuk et al. [19], these islands might locally protect the Si(001) substrate against the creation of a SiN_x amorphous layer during the substrate exposure to the nitrogen flux. Thus, after the nitridation stage, the surface was covered by a silicon nitride amorphous layer with some spots of silicon oxide where GaN nucleated, first as zinc-blende (ZB) GaN pyramids and then transformed into wurzite Ga-polar GaN NWs [19].

The hypothesis that on the HF-treated Si substrate the islands of residual oxide were responsible for inducing Ga-polar growth of GaN NWs is strongly supported by results of recent X-ray diffraction measurements [56]. Due to the high intensity of the synchrotron radiation beam used and the application of grazing incidence geometry, the presence of tiny ZB-GaN pyramids that are the seeds for Ga-polar NWs could be detected on the HF-treated Si(001) substrate. For that study, we used a GaN NWs sample grown on HF-treated Si(001). We then compared the results with those obtained for NWs grown on a similar substrate, but for which, after H passivation desorption and substrate nitridation, the so-called gallium-induced surface cleaning [57–60] was used. The procedure consisted of the deposition of a few monolayers of Ga at a low temperature of 500 °C in the absence of active nitrogen, followed by gallium desorption at 800 °C. This step was repeated three times, after which the substrate was nitridated again. It is well established that Ga-induced cleaning leads to the creation of volatile Ga_2O on the substrate that is removed from the surface during heating [61,62]. We anticipated that if after the first nitridation step the substrate was cleaned by gallium flux, the residual silicon oxide islands should be removed, so the second nitridation step could complete the SiN_x film on places initially covered by the oxide. As a result, the concentration of ZB-GaN pyramids should be significantly reduced. This was indeed observed, together with a corresponding reduction in the number of Ga-polar NWs [56].

In silicon manufacturing, the standard way of treating Si wafers before high-temperature processing steps is the well-known RCA clean developed by the Radio Corporation of America in 1965 [63]. In this cleaning procedure, the native oxide on silicon is dissolved and a new oxide layer forms. Such oxide regeneration is an important factor in the removal of particles and chemical impurities from the surface. The thin volatile oxide created on the wafer may be removed at ~800 °C under UHV if a pure silicon surface is needed for epitaxial growth [13,38,64–67]. The Si substrate for sample B was prepared by its exposure for 10 min to a mixture of water-diluted hydrogen peroxide and ammonium hydroxide at 80 °C (SC-1 bath), followed by a short immersion in a 1:20 solution of aqueous HF (oxide removal) and a final etching in a mixture of water-diluted hydrogen peroxide and hydrochloric acid at 80 °C for 10 min (SC-2 bath) [68]. After the deionized water rinse and drying in nitrogen flow, the substrate was annealed in the PAMBE growth chamber at ~950 °C for 10 min to desorb the oxide film. Next, standard substrate nitridation and GaN NW growth were performed. KPFM studies of the as-prepared sample B revealed that 4% of the 50 NWs checked exhibited reversed polarity. This result is similar to that reported by Eftychis et al., who used KOH etching to assess the polarity of GaN NWs grown by PAMBE on RCA-cleaned Si(111) substrates [65].

Interestingly, if after desorption of the oxide film formed by the RCA clean two Ga-triggered deoxidation steps were additionally applied (sample C), the number of Ga-polar NWs reduced only slightly to ~3% (180 NWs analyzed in total). This indicates that oxides were only a fraction of the impurities responsible for the reversed polarity, while the majority of them most probably originated from a residual contamination of chemicals, water, glassware or handling tools.

Next, sample D was prepared, for which, instead of using the RCA clean, the native oxide was thermally desorbed from an as-received wafer in the PAMBE growth chamber at ~1000 °C for 10 min. Then, two Ga-induced surface deoxidation steps were applied before substrate nitridation as for sample C. KPFM studies showed that none of the 225 NWs tested in sample D exhibited Ga polarity. In order to elucidate whether this was due to the thermal oxide desorption itself or the Ga-triggered

deoxidation, sample E was studied for which the substrate was prepared as for sample D but without the Ga-induced surface cleaning steps.

Figure 2a,b show, respectively, the AFM topographic view image and the CPD map of the same area of sample E. The profile in Figure 2c shows a uniform CPD distribution with the mean value of ~850 mV, which is compatible with the nitrogen polarity of the NWs. No dark spots corresponding to Ga-polar NWs, as those marked with arrows in Figure 1b, are found on the CPD map of sample E (120 NWs analyzed in total). This evidences that thermal native oxide desorption at high temperature alone provides a clean Si surface and that additional Ga-triggered deoxidation steps, as those used for sample D, are not necessary. However, it is worthy noticing that results of the substrate cleaning procedure may depend on the particular conditions available in various laboratories. For instance, Carnevalle et al. reported ~10% of Ga-polar NWs grown by PAMBE on Si(111) substrates thermally deoxidized in the growth chamber at a temperature of ~1000 °C [9], i.e., under conditions similar to those used for sample E.

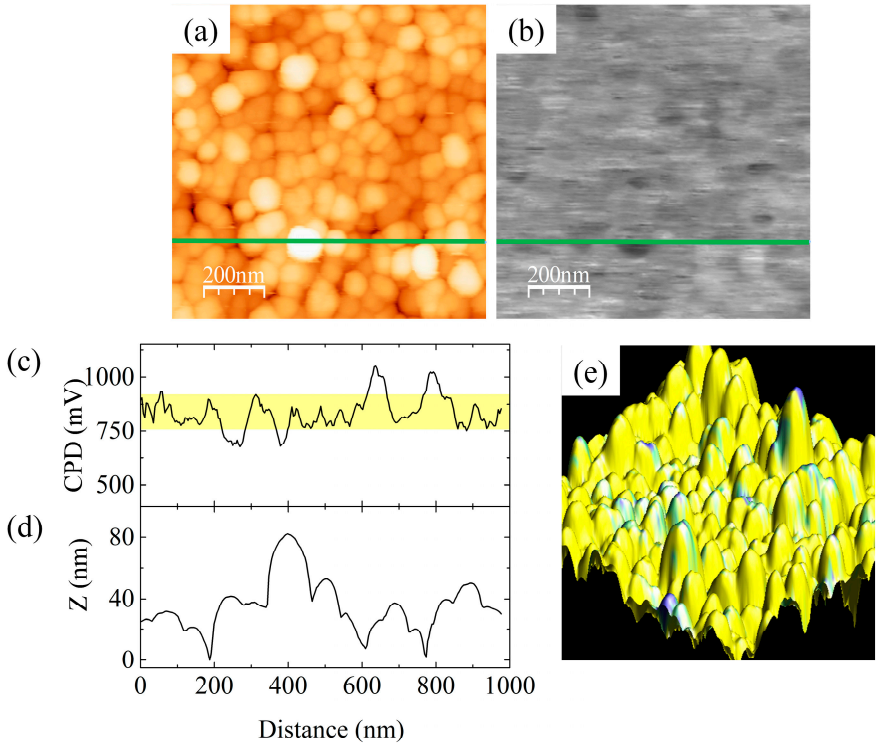

Figure 2. (**a**) AFM topographic view image (1 × 1 μm^2, color scale from 0 to 100 nm) and (**b**) the corresponding CPD map (color scale from 0 to 1.5 V) of sample E. The CPD value and NW height profiles along the green line, (**c**) and (**d**), respectively. (**e**) shows the 3D superposition of the topography (xyz axis) and CPD value (color scale).

In summary, from the silicon substrate cleaning procedures tested in this work, thermal native oxide desorption at high temperature inside the growth chamber provides the best uniformity of polarity in the GaN NWs ensemble. Obviously, the cleaner the surface of the silicon substrate before its nitridation, the cleaner and more chemically uniform the silicon nitride layer on which NWs nucleate. If any contamination is left on the Si surface, it disturbs the SiN_x nucleation layer and may lead to the formation of NWs with reversed polarity. We underline that each of the substrate cleaning techniques presented above resulted in a sharp 7 × 7 RHEED pattern characteristic of a clean, oxide-free Si(111) surface prior to the switching on the nitrogen source. Results of our KPFM studies show that this is not sufficient to ensure uniform N polarity in the whole NW ensemble.

Another strategy for the formation of polarity-uniform GaN NWs arrays by PAMBE is to grow them on a thin uniform buffer layer deposited ex situ on the silicon substrate. If such a buffer is

chemically stable and conformally buries residual impurities on the substrate, it should prevent NW polarity reversal from N to Ga.

Recently, there is an increasing interest in the application of amorphous AlO_y films deposited by ALD as nucleation layers for the PAMBE growth of GaN nanostructures. Such buffers effectively induce selective area formation of GaN NWs on sapphire [33] and GaN [69,70]. As shown in previous studies [34,41,71,72], AlO_y buffer layers significantly enhance the nucleation rate of GaN with respect to nitridated Si without a loss of structural and optical quality [34]. Additionally, AlO_y buffers prevent diffusion of silicon from the substrate [34], facilitating the growth of GaN nanostructures at high temperatures without incorporating any impurities [73], thus potentially leading to exceptional optical properties. However, the polarity of GaN NWs grown by PAMBE on Si(111) substrate with a thin AlO_y buffer layer deposited by ALD has never been tested. In this study, we used KPFM to fill this gap.

Figure 3a shows the AFM topographic view image of sample F. The NWs have a diameter of ~90 nm, but as before, this is convoluted with the AFM tip of ~20 nm diameter. The CPD values shown in the map in Figure 3b and in the CPD line profile in Figure 3c are quite uniform with the mean value of ~750 mV, which is compatible with the N polarity of the NWs. In some points of the map, the CPD value slightly decreases to ~450 mV, but these points do not correspond to the top of the NWs and are assigned to NWs' sidewalls. This allows us to conclude that no mixed polarity with a certainty above 99.8% (more than 400 NWs analyzed) was observed for GaN NWs grown on Si(111) substrates covered by a thin amorphous AlO_y buffer layer.

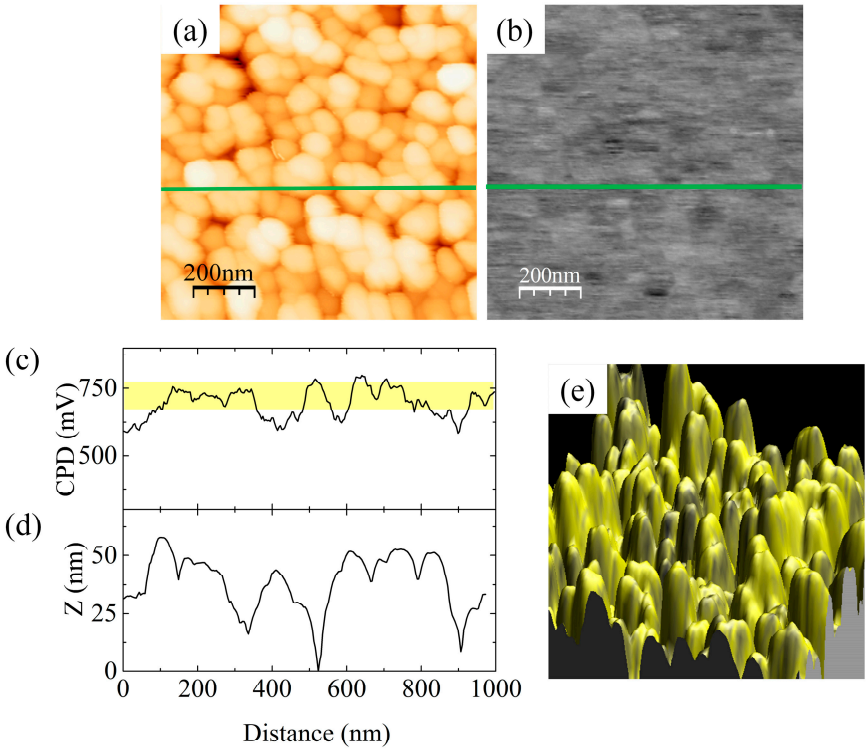

Figure 3. (**a**) AFM topographic view image (1 × 1 μm^2, color scale from 0 to 140 nm) and (**b**) the corresponding CPD map (color scale from 0 to 1.5 V) of sample F. The CPD value and NW height profiles along the green line, (**c**) and (**d**), respectively. (**e**) shows the 3D superposition of the topography (xyz axis) and CPD value (color scale).

Finally, it is worth mentioning that the silicon substrate for sample F was cleaned by a HF dip in the same procedure as used for sample A, and then transferred in air to the ALD system. It took a few hours before the deposition of the buffer layer started. Due to the instability of the H-passivated substrate surface, it certainly got locally oxidized during the long time of unprotected storage. Nevertheless, no

reversed NW polarity was found in sample F. This indicates that the islands of oxide that led to the appearance of Ga-polar NWs in sample A were efficiently covered by the buffer and their presence under the amorphous AlO_y layer had no impact on GaN nucleation.

4. Summary and Conclusions

In this work, the most common procedures used to process Si substrates prior to epitaxial growth are tested to find their impact on polarity uniformity inside the ensemble of self-assembled GaN NWs grown by PAMBE. Since local contamination of the silicon substrate surface eventually disturbs the uniformity of the SiN_x film formed during the nitridation step preceding the GaN nucleation, this might lead to the formation of NWs with reversed Ga polarity.

Kelvin probe force microscopy was used to determine the polarity of GaN NWs. The technique allows the polarity assessment of a statistically significant number of single NWs on the wafer over micrometer large surface areas with nanometer resolution and without the need of any special sample preparation. Complementary images of KPFM, namely topography and contact potential difference, were analyzed.

We showed that the uniformity of the polarity within the ensemble of GaN NWs on Si(111) strongly depends on the procedure used for substrate cleaning. As high as 18% of NWs with reversed polarity (i.e., Ga-polar) were detected by KPFM if the Si substrate was etched in diluted HF and then annealed in the growth chamber to remove hydrogen passivation prior to the substrate nitridation. We ascribe this behavior to the low stability of the hydrogen passivation layer. Apparently, it did not sufficiently protect the freshly etched substrate during its transfer to the UHV system and some islands of oxide were formed, which induced the growth of Ga-polar GaN NWs by the mechanism reported earlier [19]. Such conclusion is strongly supported by previous studies showing that the mixed polarity of GaN NWs on HF-treated Si can be eliminated by additional Ga-triggered deoxidation of the substrate performed just before its nitridation inside the growth chamber [56].

Much better homogeneity of NW polarity was obtained on the Si substrate cleaned by the RCA procedure in which the native oxide was dissolved and a new oxide layer was formed. Next, this oxide was desorbed by annealing in the PAMBE growth chamber at ~950 °C for 10 min. KPFM studies of an NW ensemble grown on such substrate revealed that around 4% of NWs had reversed polarity. This number decreased to less than 3% if after oxide desorption, but before the nitridation step, the substrate was additionally cleaned by Ga-triggered deoxidation. In the latter case, the polarity flip could be due to surface contamination by residual pollution of chemicals, water, glassware or handling tools, instead of local surface oxidation.

The best results, i.e., purely N-polar ensemble of NWs, were obtained on epi-ready Si wafers thermally deoxidized in the growth chamber at ~1000 °C just prior to their nitridation. Additional Ga-induced surface cleaning steps were not needed in that case. Our studies indicate that high-temperature silicon oxide desorption under UHV produces the cleanest Si surface, resulting in the formation of a uniform SiN_x layer that prevents an NW polarity reversal from N to Ga. This requires, however, that a high-temperature substrate heater is available in the PAMBE system, which is not always the case.

It is worth mentioning that each substrate cleaning technique tested in this work resulted in a sharp 7×7 RHEED pattern characteristic of a clean Si(111) surface prior to switching the nitrogen source on. Results of our KPFM studies show that this is not sufficient to ensure uniform N polarity in the whole NW ensemble.

Finally, no mixed polarity with a certainty above 99.8% was found for GaN NWs grown under similar conditions on Si(111) substrates covered by a thin amorphous AlO_y buffer layer. It is well known that the ALD technique produces compact, pinhole-free layers conformally covering the surface. Our results indicate that an ALD-deposited AlO_y buffer efficiently buries oxides that might eventually form during a few hours' storage in air of the HF-dipped Si wafer before buffer deposition in the ALD system. Therefore, possible contamination of the substrate surface under the amorphous AlO_y layer

had no impact on GaN polarity. In summary, our results show that reversal of GaN nanowires' polarity can be efficiently prevented by growing them on a chemically uniform substrate surface, in our case on clean, in situ formed SiN_x or ex situ deposited AlO_y buffers.

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Influence of Growth Polarity Switching on the Optical and Electrical Properties of GaN/AlGaN Nanowire LEDs

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Abstract: For the development and application of GaN-based nanowire structures, it is crucial to understand their fundamental properties. In this work, we provide the nano-scale correlation of the morphological, electrical, and optical properties of GaN/AlGaN nanowire light emitting diodes (LEDs), observed using a combination of spatially and spectrally resolved cathodoluminescence spectroscopy and imaging, electron beam-induced current microscopy, the nano-probe technique, and scanning electron microscopy. To complement the results, the photo- and electro-luminescence were also studied. The interpretation of the experimental data was supported by the results of numerical simulations of the electronic band structure. We characterized two types of nanowire LEDs grown in one process, which exhibit top facets of different shapes and, as we proved, have opposite growth polarities. We show that switching the polarity of nanowires (NWs) from the N- to Ga-face has a significant impact on their optical and electrical properties. In particular, cathodoluminescence studies revealed quantum wells emissions at about 3.5 eV, which were much brighter in Ga-polar NWs than in N-polar NWs. Moreover, the electron beam-induced current mapping proved that the p–n junctions were not active in N-polar NWs. Our results clearly indicate that intentional polarity inversion between the n- and p-type parts of NWs is a potential path towards the development of efficient nanoLED NW structures.

Keywords: nanowires; GaN; AlGaN; LEDs; growth polarity

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1. Introduction

While light emitting diodes (LEDs) or laser diodes (LDs) made of group III nitrides have widely replaced conventional light sources in everyday life and various brands of technology [1–3], they still suffer from drawbacks such as a limited internal quantum efficiency and low light extraction efficiency. These problems are related to structural imperfections (such as a high dislocation density), strong polarization electric fields at interfaces, or inefficient doping in the planar multilayer structures, which are composed of materials with markedly different structural parameters. One solution to at least some of those problems that has been seriously considered is to replace continuous layers of semiconductors with ensembles of quasi-1D nanowires (NWs) grown perpendicularly to the substrate.

III-N compounds and their solid solutions are highly suitable for the construction of photonic devices. Their band gap energies cover a wide range from 0.7 eV for InN, through 3.4 eV for GaN, to 6.1 eV for AlN [4]. In principle, appropriate selection of the nitride composition in the active region of an optoelectronic device should allow for the obtention of electromagnetic radiation from any part of the visible spectrum or a considerable part of the ultraviolet band. Thus, they can be used in the fabrication of lighting systems imitating the daylight spectrum for houses and offices; light source-acceleration of photosynthesis for agriculture; and health care applications. Additionally, full-color displays or high-density optical data storage systems based on nitride laser diodes can be produced. Nitride-based optoelectronic devices can also be applied in UV detection [5,6] for aerospace and automotive engineering, biology/medicine, and astronomy. All the components of these devices, such as quantum wells, barriers, and p- and n-type layers in heterojunctions, can be fabricated from proper nitrides or their alloys. This is an important advantage of group III nitrides compared to many other wide-band-gap materials. Nevertheless, technical problems associated with the complex synthesis of multilayer semiconductor structures make the reproducible fabrication of reliable devices challenging. It is of great importance to select substrates that are lattice-matched and thermally compatible, while also large and cost-effective. While ammonothermal [7,8] and hydride vapor-phase epitaxy (HVPE) [9,10] methods of growing large bulk GaN substrates have already been successfully developed, sapphire or SiC substrates are still routinely used and have shown promising results. The growth of high-quality nitride structures on silicon would make the integration of nitride-based devices with advanced Si microelectronics possible. This would provide a great advancement in optoelectronic device technology.

The lattice mismatch between the substrate and the nitride layer results in dislocations, relieving the strain at the interface but deteriorating the electrical and optical properties of the structure. Various methods, such as buffer layer engineering and the epitaxial lateral overgrowth technique, have been devised to reduce the dislocation density in nitride-layered structures. Replacing 2D layers with a set of quasi 1D NWs improves the strain accommodation conditions at the markedly smaller interface. This effect was also demonstrated for nitride NWs grown on a Si substrate [11]. The appearance of stress-relieving dislocations can be avoided not only between the substrate and the nanowire but also at the interfaces inside the nanowire [12].

The quasi 1D geometry of the structure has more advantages than those already mentioned: For nano-light-emitters created as axial or radial heterostructures, it increases the light generation efficiency; reduces the light losses in the structure; enhances the efficacy of light extraction from the structure; and allows for the growth of multicolor micro-LED pixels [13–15]. Such objects, with a regular shape defined by the crystalline structure and a size comparable to the wavelength of light, can also confine electro-magnetic radiation and play the role of a resonator for such nano-devices. However, some other critical issues influencing the functionality of nanowire-based devices still exist. It is necessary to solve the problems associated with effective p-type doping (in particular, for ternaries with high In or Al contents) in order to reduce defect-related nonradiative recombination channels, including those related to the developed surface of the system. This would improve hole transport, which is limited by defects, and thus tackle the heat management issue in quasi 1D devices. Some of these issues, such as p-type doping, defect creation (e.g., defects caused by stacking faults (SFs) and polarity inversion domains) are directly related to the nanowire growth conditions.

An important feature of NWs is the possibility of fabricating them by a bottom-up growth process, without the use of technically demanding and expensive technological processes, such as photo- or electron-beam lithography, resist deposition, or etching. Instead, the spontaneous formation of NWs governed by the growth conditions is often applied. A variety of growth methods allowing for the fabrication of NWs on various substrates have been successfully tested (including chemical vapor deposition, metalorganic chemical vapor deposition (MOCVD), and molecular beam epitaxy (MBE) [16]), and numerous ex-

amples of ensembles of NWs that are of a highly crystalline quality and have well defined electronic and optical properties have been demonstrated (for a review, see [17]).

Among the techniques currently used to grow III-N low-dimensional structures, MBE has important advantages. The high purity of the source materials and ultra-high-vacuum growth conditions, as well as the availability of many techniques of in-situ growth monitoring, allow for a reduction in the unintentional impurity level and improvement in the crystalline quality of the grown material. In general, the two most commonly used approaches to nanowire growth by MBE are based on spontaneous nucleation and vapor-liquid-solid growth, in which whiskers are grown beneath a catalyst droplet. The former [18] is routinely used to grow nitride NWs, since it eliminates the unwanted contamination of NWs with catalyst atoms. While the MBE method is not suitable for the mass production of devices, it is a convenient tool for studies motivated mainly by an interest in fundamental physical processes involving electrons and photons in NWs. The structure of NWs can be carefully controlled and modified in accordance with the results of microscopic, structural, and optical measurements, even if some uncertainties concerning the NW size or composition, resulting from the spontaneous nature of the growth process, should be borne in mind. However, the conclusions can lead to improvements in the architecture and technology of real devices or, at least, the construction of demonstrator devices.

Full control of the course of the growth process and properties of the resulting system is still far from being established. This leads to a scattering of the important physical properties of NWs, even those obtained on the same substrate in a single process. The inner structure of the nanorods may contain spontaneously formed defects, chemical composition fluctuations, domains with built-in strain, growth polarity domains, etc. Fingerprints of some of these defects can be detected by cathodo- and photoluminescence, for example, stacking faults [19,20] and inverted polarity domains [21,22]. On the other hand, intentionally grown axial or radial heterojunctions, quantum wells, etc., are formed in the NWs in order to study basic physical phenomena (e.g., those related to elementary excitations in semiconductors) or create new functionalities [13,23]. Since the properties fluctuate between nanowires, the parameters should not be analyzed as global quantities describing the sets of many nanowires. It is necessary to investigate the optical and electronic properties of NWs with a submicron or nanometer resolution, which allows the properties of the sub-structures of NWs, such as quantum wells, barriers, and p- or n-type segments in the heterojunctions to be revealed.

In this work, we report on the nano-scale correlation of the morphological, structural, electrical, and optical properties of GaN/AlGaN nanowire LEDs, as observed by a combination of scanning electron microscopy (SEM), spatially and spectrally resolved cathodoluminescence (CL), andelectron beam-induced current (EBIC), atomic force, and Kelvin probe force microscopies. GaN/AlGaN LED nanowire structures with three GaN quantum wells in the p–n junction and AlGaN barriers were grown on silicon (111) substrates, without any catalyst, using plasma-assisted molecular-beam epitaxy. The bottom n-type part of the structure was made of GaN:Si. Then, the GaN wells sandwiched between AlGaN barriers were formed. The top part of the nanowire, which acted as the p-type part of the p–n junction, was composed of AlGaN:Mg. As this part was employed with the intention of forming a quasi-planar base for the top electrical contact of the structure, the growth mode had to be adapted to the conditions, which enhanced the lateral growth, leading to an inversely tapered form of the NWs. Therefore, the upper part of the structure was formed under particularly demanding conditions, and its properties resulted from the interplay of several coinciding physical phenomena. It was grown from an AlGaN solid solution at a reduced growth temperature and under intense Mg-doping, which should give the p-type conductivity. The results of our investigations indicated that unintentional fluctuations in the growth conditions caused the growth polarity to switch from the N- to the Ga-face for a considerable part of the NWs. Such a polarity reversal causes differences in the growth and changes the direction of the built-in spontaneous electric field [24]. The EBIC signal and the CL spectral features recorded for individual NWs proved that in

the N-face NWs, the p–n junctions were not active, and the quantum-well luminescence was reduced. A comparison of the experimental data with the results of the numerical simulations of the electronic band structure of individual NWs facilitated a discussion of the physical mechanisms responsible for the activation or deactivation of the p–n junctions. We ascribed the reduced functionality of the p–n junction to an ineffective Mg-doping of the top part of the NWs grown with N-polarity. This conclusion established the growth parameters that result in the successful growth of functional nanoLEDs in NWs.

2. Samples and Experimental Methods

2.1. Samples

The GaN/AlGaN NW LEDs were grown on in-situ nitridated 3″ Si (111) substrates using plasma-assisted molecular beam epitaxy (PAMBE) in a Riber Compact 21 system with elemental sources of Ga, Al, Si, and Mg. A radio frequency Addon nitrogen plasma cell, controlled by an optical sensor of plasma light emission [25], was used as the source of active nitrogen species. No catalyst was used to induce the nucleation of the NWs. The nanowire LEDs with the three GaN quantum wells in the area of the p–n junction were grown according to the following procedure. First, the 500–600 nm-long GaN nanowires doped with Si (nominal doping level: 5×10^{18} cm^{-3}) were grown under N-rich conditions at a temperature of 790 °C to achieve the n-type part of the structure. Then, the quantum structure was grown. It began with $Al_xGa_{1-x}N$ segments with a gradually increased composition (3%, 6%, 9%, 12%) and was followed by the growth of 3 GaN quantum wells (QWs) with thicknesses of 3.5 nm, which were sandwiched between the 10 nm-thick $Al_{0.15}Ga_{0.85}N$ barriers. The number of QWs and other parameters of the quantum structure were chosen on the basis of our previous experience, and reports are available in the literature (e.g., [26]). As such a configuration provides efficient luminescence, it was suitable for testing the functionality of our nanoLED in NWs. Finally, the p-type part of the structure consisting of 1 µm-thick $Al_{0.2}Ga_{0.8}N$ doped with Mg (nominal doping level: 5×10^{19} cm^{-3}) was grown. The growth temperature at this step was reduced to 715 °C to enhance the lateral growth rate and to broaden the nanowire tops, with the aim of making the further processing of the device easier.

A detailed scheme of the NW LED structure is shown in Figure 1. More details on the growth method used for the fabrication of the NW structures can be found in [27–29]. The contact with the n-type (cathode) was obtained by covering the Si substrate with indium (for electroluminescence measurements) or aluminum (for EBIC studies). The anodes were made by the evaporation of a thin, semitransparent layer of gold on the upper surfaces of the NWs. The anodes for the electroluminescence measurements had a shape characterized by circular spots with a diameter of 1 mm. The layer of gold was continuous and conductive due to the good coalescence of the tops of the NWs, which was obtained by their lateral growth.

2.2. Methods

The morphology of the LED NWs was examined by scanning electron microscopy (SEM) using a field-emission Hitachi SU-70 scanning electron microscope (Hitachi, Tokyo, Japan). The SEM machine, equipped with a Gatan MonoCL3 cathodoluminescence system, including the continuous-flow liquid helium cryo-stage and Gatan electron beam induced current (EBIC) setup, enabled studies of the local optical and electrical properties of single NWs.

High-resolution transmission electron microscopy (TEM) experiments of the LED NW structures were conducted using the FEI Titan 80–300 Cubed high-resolution TEM (HRTEM) operating at 300 keV (FEI Company, Hillsboro, ON, USA).

The photoluminescence (PL) spectra were excited by a system composed of a Ti:Sapphire laser and third harmonic generator at a wavelength of 300 nm, with a pulse frequency of 80 MHz. The time-resolved photoluminescence (TRPL) kinetics were measured using a Hamamatsu C5680 streak-camera (Hamamatsu Photonics, Shizuoka, Japan).

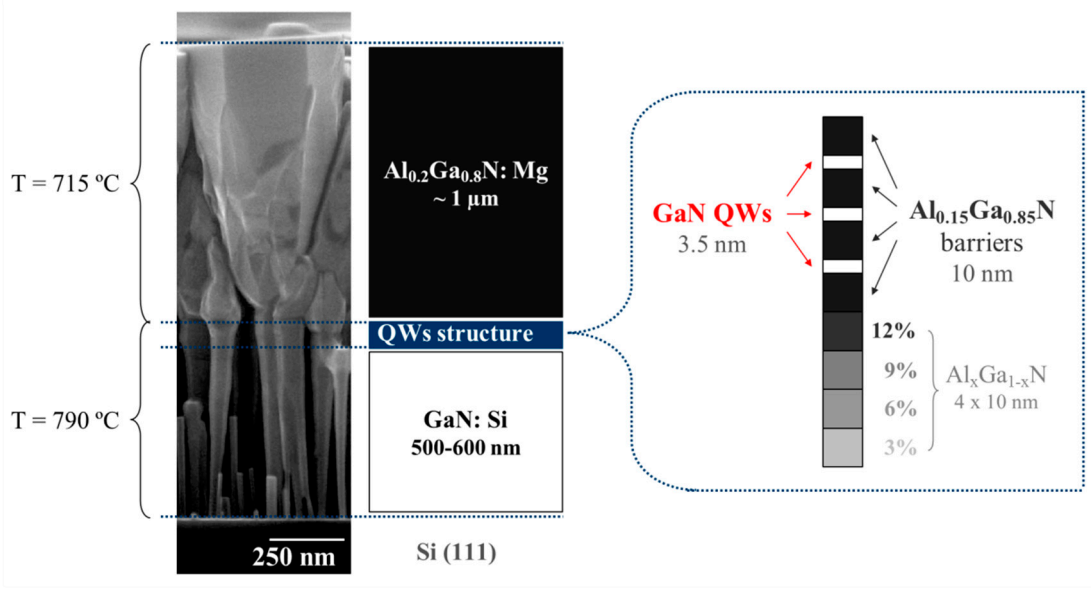


Figure 1. Scanning electron microscopy (SEM) image and scheme of the light emitting diode (LED) nanowire structure, which consists of: a GaN:Si n-type part on the bottom, an active region, which starts with AlGaN segments with an increasing Al content (3%, 6%, 9% and 12%), followed by 3 GaN quantum wells (QWs), which are sandwiched between the $Al_{0.15}Ga_{0.85}N$ barriers and the p-type $Al_{0.2}Ga_{0.8}N$:Mg top.

The I–V characteristics of individual LED NWs were measured in the chamber of the Tescan Lyra3 scanning electron microscope (Tescan Orsay Holding, a.s., Brno-Kohoutovice, Czech Republic) using a Keithley 236 measurement unit. A tungsten tip of a SmarAct nano-probe served as a top ohmic contact (SmarAct GmbH, Oldenburg, Germany).

The atomic force microscopy (AFM) and Kelvin probe force microscopy (KPFM) were carried out in the tapping mode using a MultiMode AFM, with a Nanoscope IIIa controller and Nanoscope Extender (Bruker/Digital Instruments, Billerica, MA, USA).

3. Results

3.1. Morphology and Structure

Despite the fact that the NWs were grown in the same growth process, the SEM investigations revealed two kinds of NW morphologies, as shown in Figure 2.

Figure 2a shows a cross-sectional SEM image, where two types of nanowires can be easily distinguished. Some of them have a regular broadening, with flat sides, and some have an irregular "oval-like" shape in the laterally grown area. In the plane-view SEM (Figure 2b), differences are also clearly visible: some of the NWs have a flat hexagonal top with sharp edges, while the others have a less regular, rough top with rounded edges.

We note that, due to a radial temperature gradient across the wafer, two areas could be easily distinguished on the substrate surface. Area A (Figure 2b, upper panel) is a ~10 mm-wide ring near the edge of the wafer, while area B (Figure 2b, bottom panel) is a circle in the center of the wafer. Independent measurements of the temperature distribution, performed by growing planar GaN layers on such substrates, indicated a ~30 °C higher growth temperature at the wafer periphery than in the central B area. Interestingly, such a temperature profile led to the noticeably higher concentration of hexagonally shaped NWs in area A than in the colder part (area B) of the wafer, as shown in the SEM images.

The TEM studies in the Z-contrast scanning transmission mode (STEM) revealed that both types of NWs contain three 3.5 nm-thick QWs (inset in Figure 2a). The bottom parts and QW regions of NWs are similar in all wires, and differences are observed only in the upper p-type $Al_{0.2}Ga_{0.8}N$:Mg part of the LED structure. The NWs with the flat hexagonal tops are more uniform, while in the NWs with the "oval-like" top area, some features resembling grain boundaries are visible.

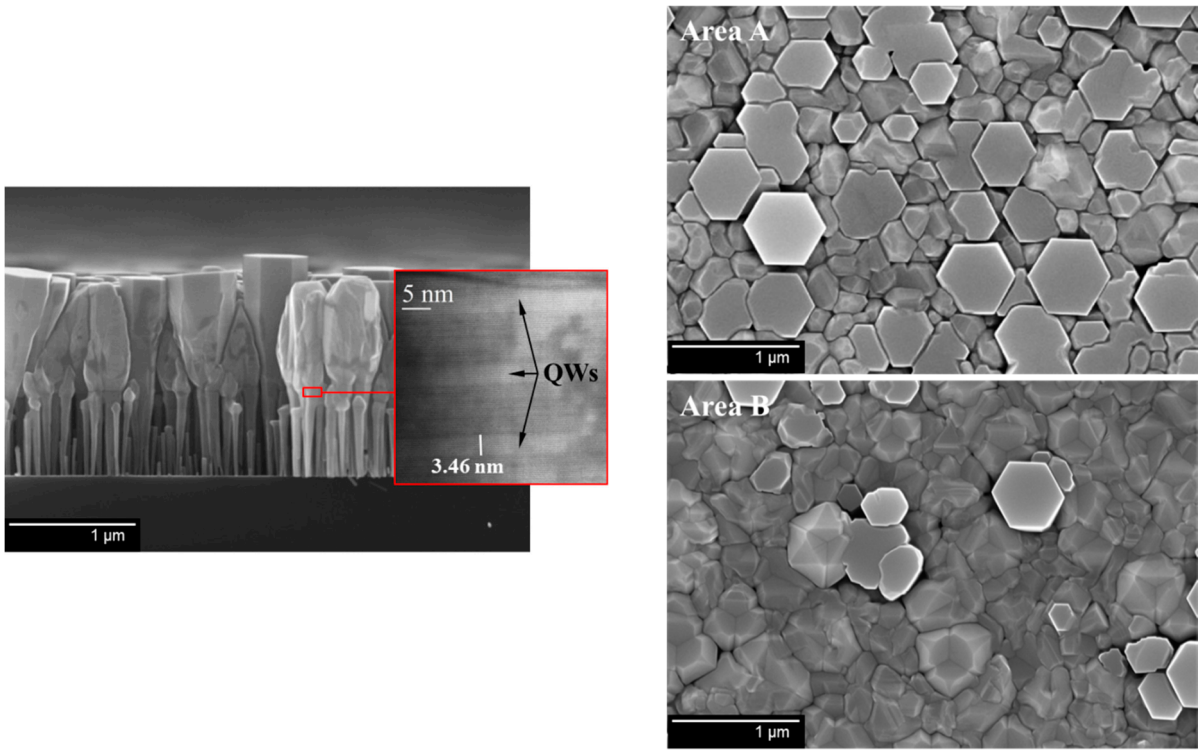
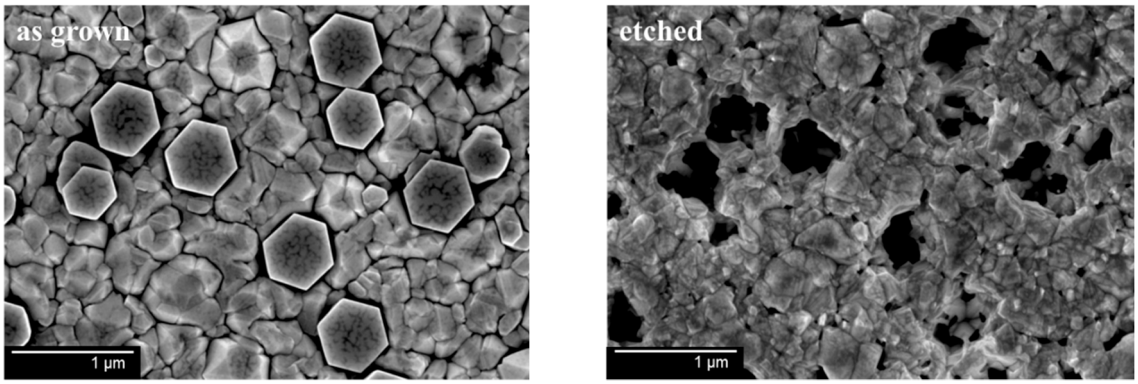


Figure 2. Cross-section SEM and Z-contrast scanning transmission mode (STEM) (inset) images (**a**) and plane-view SEM images (**b**) of the LED NWs. Two types of NWs can be easy distinguished: those with flat sides and hexagonal tops with sharp edges, and those which are "oval-like", with less regular, rough tops and rounded edges. Due to the temperature gradient across the substrate, the ratio of these two types varied. Two types coexist in area A, while in area B, NWs with rounded tops are mainly present.

In the [0001] direction, GaN can grow either in the Ga or N direction, which are referred to as polarities. Most nitride layers are grown in the Ga polarity, while spontaneously nucleated GaN NWs usually grow in the N polarity. However, depending on the interface chemistry and the growth procedure, changes to the Ga polarity inside one NW ensemble are often observed. Since the specific polarity of NWs affects both the optical and electrical properties and result in different properties for two morphologically distinct types of NWs, it is necessary to assess the polarity of individual NWs. This was conducted by the selective etching of the sample in an aqueous solution of potassium hydroxide (KOH). The principle of this method is based on the fact that the etching behavior strongly depends on the chemical nature of the surface. The resulting etching rate, etched surface shape, and roughness are determined by the polarity, which can, therefore, be clearly identified. It was revealed in research by several groups that the KOH etching rate is much lower for Ga-polar GaN surfaces than for N-polar ones (see, for instance, [30–33]).

In our case, the samples were etched in a KOH:H_2O 6.5 g/100 mL solution at a temperature of 160 °C for 10 min. SEM images of the samples' surfaces are presented in Figure 3. In the SEM image of the as-grown sample (Figure 3a), two kinds of NWs are visible—hexagonal- and oval-shaped, as mentioned earlier. Figure 3b presents exactly the same area of the sample, after etching in the KOH solution. It can be seen that the NWs of a hexagonal shape with flat tops have disappeared, while some of the oval-top NWs remain untouched. This experiment proved that the hexagonal-top surfaces were N-polar NWs, while the oval-top ones had Ga polarity.



(**a**) (**b**)

Figure 3. SEM images in the plane-view of the same NW array, before (**a**) and after (**b**) KOH treatment. Before KOH treatment, two kinds of NWs—those with flat hexagonal tops and those with rounded edges—were visible. After etching, the hexagonal ones disappeared, while the oval-top NWs remained untouched.

3.2. Macroscopic Electro- and Photoluminescence

The semiconductor structure inside the NW was designed to work as a light emitting diode. The bottom part was n-type (Si-doped), the upper part was p-type (Mg-doped), and three QWs were placed in the region of the p–n junction in order to trap electrons and holes, which should promote radiative recombination. Figure 4 (upper panel) shows the photoluminescence spectra at different points in the sample. It can be observed that the spectra are significantly different. For example, the GaN-related G1 peak is much stronger in the A area, while area B is dominated by AlGaN emission (peak A4). To check the operation of the NW LED devices, a series of small diodes were prepared for macroscopic electroluminescence (EL) measurements in a few rows, from the edge to the center of the wafer, across the A and B areas. After application of a voltage, blue-violet-UV electroluminescence was only observed in the B area. Diodes in the A area, mostly consisting of the hexagonally shaped top facets, were not active, which agrees well with the I–V data shown in Figure 9. The electroluminescence (EL) spectra of the forward polarized ensemble of the NWs in the B area, as a function of the applied voltage, are plotted in Figure 4 (bottom panel).

We note that in order to obtain a sufficient current, it was necessary to apply a bias of the order of 10 V, which was due to the high resistivity of the NWs. The main decrease in the voltage was most probably in the p-type part of the NWs. Nevertheless, the change in bias caused a change in electric field in the area of QWs, which led to a shift in the emission energy from 3.15 eV up to 3.28 eV, with an increase in the bias (see Figure 4—bottom panel). The effect can be explained as state filling due to a high-density electron current or a reduction in the quantum-confined Stark effect (QCSE). In the second case, an increase in the external voltage led to a reduction in the total electric field, which means that the build-in electric field has the opposite direction to that of the external one. Figure 4 shows the photoluminescence (PL) spectra obtained by the photoexcitation of the diode without voltage and PL (plus EL), observed under a bias of 14 V. In the case of EL, electrons are provided by a cathode, while holes are injected by an anode. The only part of the structure that contains both types of carriers is an active region with the QWs. Thus, in EL, only one peak was visible. During light excitations, electrons and holes were generated throughout the structure, so we could also observe the peak A4 at 3.6 eV, which is related to AlGaN. The A4 peak decreased after the application of the voltage, which was probably caused by the increase in the electric field in the AlGaN part. This meant that the build-in electric field existing in AlGaN without application of an external voltage had the same direction as the external field applied in the forward direction. The EL was only observed at room

temperature, since at lower temperatures, the sample was not electrically conductive. However, it was possible to measure PL at lower temperatures.

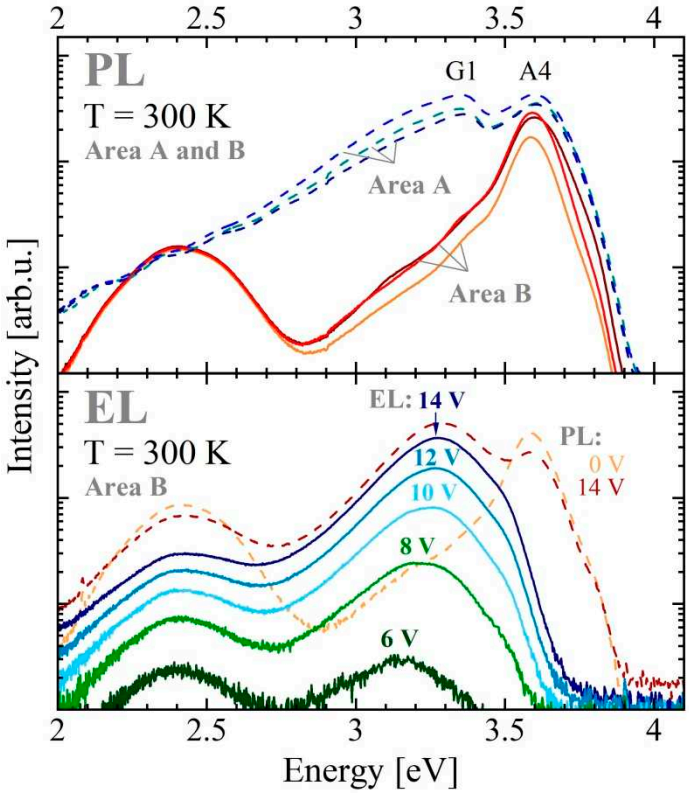


Figure 4. Luminescence spectra at room temperature: PL at different points in the sample (upper panel) and EL at different voltages (bottom panel). It can be observed that the GaN-related G1 peak is much stronger in area A. However, in area B, it was possible to obtain EL, which was dominated by the G1 peak.

A comparison of PL at 4 and 300 K in the A and B areas can be found in Figure 5. The spectra were measured in the time-resolved mode, and the kinetics of the light emission could be determined. At room temperature (upper panels in Figure 5a,b), the AlGaN-related emission was observed in a range above 3.5 eV. It was diminished by fast relaxation (lifetime about 0.1 ns) due to the escape of carriers to GaN. The main GaN peak, G1, was at about 3.4 eV at 300 K. Its lifetime depended on the location in the sample at which it was measured, from 1 ns in area A to 0.2 ns in the B area. It was observed that the GaN peak at t = 0 was at about 3.4 eV, and its energy decreased to 3.3 eV after 2 ns. Such an effect can be caused by the QCSE in the QWs. Since the energy of this peak coincided with the electroluminescence energy, we can assume that it was emitted by the QWs. Due to a shift in the energy gap [34], the luminescence spectra at 4 K are expected to be at an energy that is about 0.1 eV higher, compared to that at room temperature. The AlGaN emission was observed in the 3.6–3.8 eV range, and the GaN emission was at 3.47 eV (G1) and about 3.43 eV (G2). As can be seen in in the bottom panels of Figure 5a,b, the emission dynamics in the A and B areas were similar. The G1 peak was observed only under a high-power excitation. The lifetimes ranged from 0.2 to 0.5 ns for the AlGaN emission and 1–2 ns for the G2 emission. The exciton lifetimes in 3D GaN were below 1 ns [35], but similarly long lifetimes were observed for QWs [26,36] and SF (which was also compared to QW [20]). Therefore, we assumed that G2 is related to QWs.

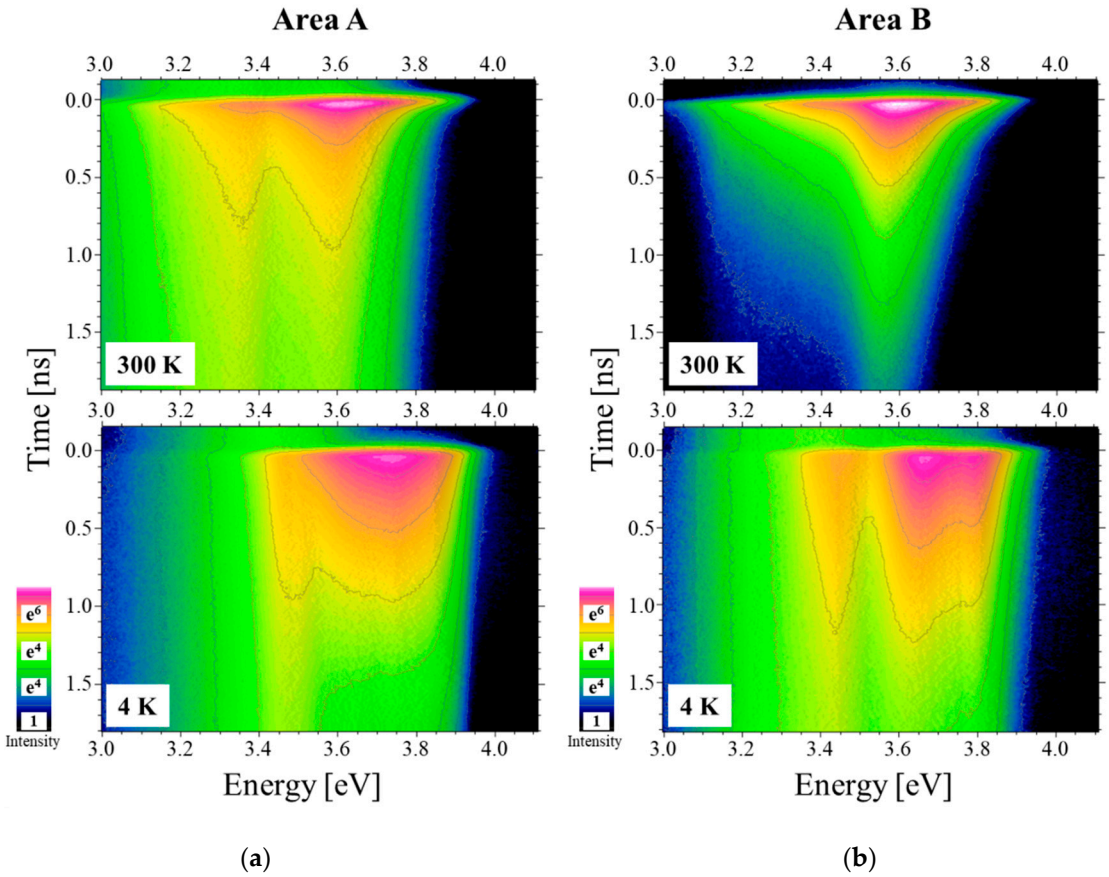


Figure 5. Time-resolved photoluminescence spectra in area A (**a**) and B (**b**) at T = 300 K (upper panels) and T = 4 K (bottom panels). The GaN emission can be seen in the 3.3–3.5 eV range, and that of AlGaN can be observed in the 3.6–3.8 eV range. The lifetimes at a low temperature are visibly longer. It can be noticed that the AlGaN emission decays faster than the GaN emission. In area A, GaN PL has a longer lifetime.

3.3. Microscopic Optical and Electrical Properties

3.3.1. Cathodoluminescence Studies

SEM combined with CL enables a direct correlation of luminescence maps and sample morphologies at the nanoscale level. The high spatial and spectral resolution and high energy excitation of this method make it the perfect tool for studying the optical properties of nanostructures that emit light in the UV range [37–39].

NW arrays were studied by CL spectroscopy and imaging at 5 K using an acceleration voltage (AV) of 5 kV and a beam current (I_b) of 1 nA. Spectra and monochromatic CL maps were collected in the cross-sectional geometry using the photomultiplier mode. In the CL spectrum (Figure 6, central panel), four main emission bands can be distinguished. Two bands—A1: 3.83 eV; and A4: 3.63 eV—are related to AlGaN luminescence. The CL maps (Figure 6, right side) confirmed that the emission comes from the upper (p-type) part of the NWs. The presence of two bands is most probably related to the existence of inhomogeneous Al contents in AlGaN. The third emission line, G1 centered at 3.47 eV, is related to the luminescence of the QWs. The emission of QWs is clearly visible in the corresponding CL map (Figure 6, left side). The fourth one, G3 at 3.3 eV, most probably comes from the recombination of donor–acceptor pairs.

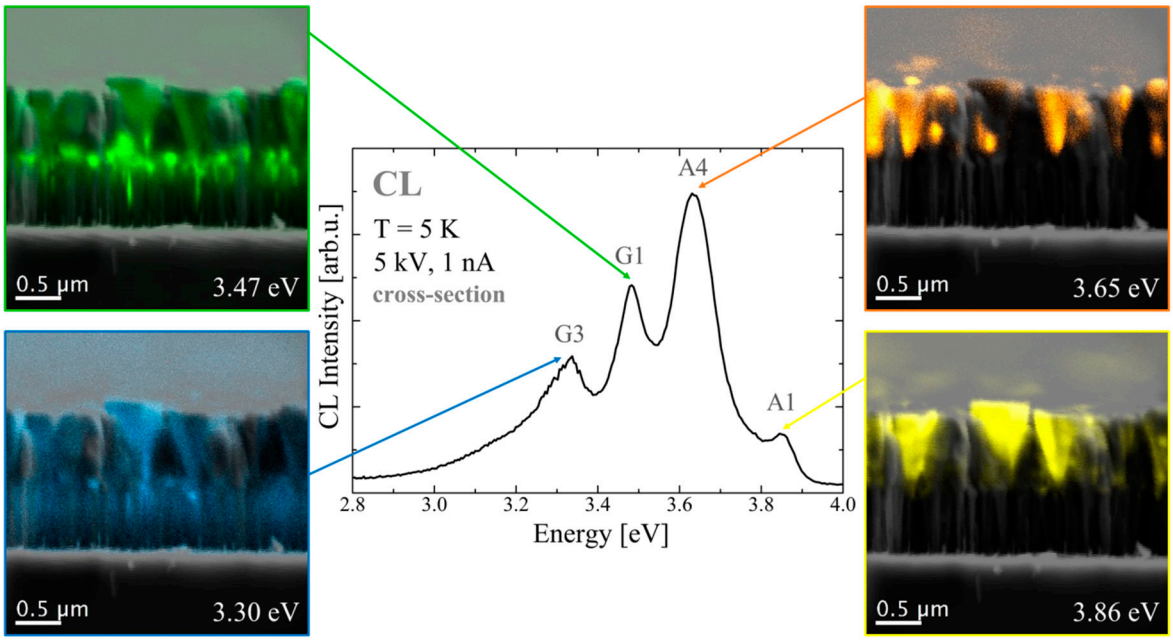


Figure 6. Cathodoluminescence spectrum of the NW array (central panel) and corresponding monochromatic CL maps superimposed with SEM images (sides), collected in the cross-sectional mode. Two bands—A1: 3.83 eV; and A4: 3.63 eV—are related to AlGaN luminescence. In the corresponding CL maps (right side), the emission is visible in the upper (p-type) part of the NWs. The third emission line, G1 centered at 3.47 eV, is related to the luminescence of the QWs, which proves the corresponding CL map (left side). The fourth one, G3 at 3.3 eV, most probably comes from the recombination of donor–acceptor pairs.

To study local optical properties in detail, CL spectrum line-scans at 5 K were recorded for a number of individual NWs (in a cross-sectional geometry) using an AV of 5 kV and I_b of 1 nA. A CCD camera in the CL line-scan mode enabled the acquisition of a series of luminescence spectra of the individual NWs, which were excited with the electron beam point-by-point along the specified line parallel to the NW axis. The direction of the line-scans is illustrated in the SEM insets shown in Figure 7. Typical results are shown in Figure 7. The set of spectra in the upper panel corresponds to the CL line-scan of the nanowire with an oval shape, where the polarity switched to the Ga-one, while the bottom panel shows the spectra for a fully N-polar hexagonal NW.

As can be seen in the upper panel in Figure 7, the bright luminescence from the active region is observed in the Ga-face NWs. Since the QWs emission is the main source of LED radiation, we conclude that a reversal of NW polarity is crucial for LED efficiency. The N-face NWs had a strong emission related to the A4 peak at 3.65 eV, which was emitted in the upper part of the NW.

A series of spectra of the individual NWs was also collected in the top-view configuration. The CL in the spot-mode was measured at 6 K using an AV of 5 kV and I_b of 1.9 nA. The electron beam parameters have been adjusted so that only the upper, p-type $Al_{0.2}Ga_{0.8}N$:Mg part of the LED NW structure was excited. A Monte Carlo simulation of the CL intensity distribution, performed using the Casino v2.48 (2.4.8.1) software [40], allowed us to estimate the size of this region. For AV = 5 kV, about 90% of the CL signal comes from a depth of 200 nm.

Observing Figures 7 and 8, one can easily see that the different peaks in the CL spectra correlate with the differences in the shape of the NWs. The AlGaN:Mg emission was expected to be above 3.5 eV. The hexagonal-shaped (N-polar) NWs emissions corresponded to the A1 and A4 peaks, while the oval-shaped (Ga-polar) NWs emitted mainly at 3.78 eV (peak A2). The lower energy of the oval-shaped NWs implies that these NWs have a lower Al content. Since the Al desorption at used growth temperatures is negligible, irrespective of the polarity,

this was probably caused by the higher Ga incorporation into AlGaN on the N-polar than on the Ga-polar surface, which is similar to the case of In during InGaN growth [41].

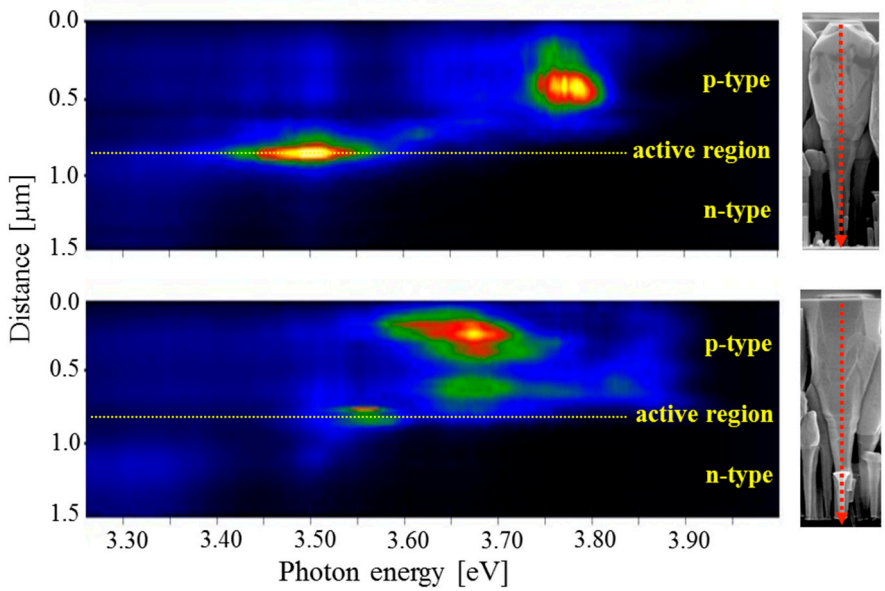


Figure 7. CL line-scans collected along the individual NWs: upper panel—scan along the oval-like NW; bottom panel—scan along the hexagonal one. The bright emission from the active region is observed in the Ga-face NWs. The N-face NWs had a strong emission related to the A4 peak at 3.65 eV, which was emitted in the upper part of the NW. The arrows on the SEM images indicate the direction of the scans.

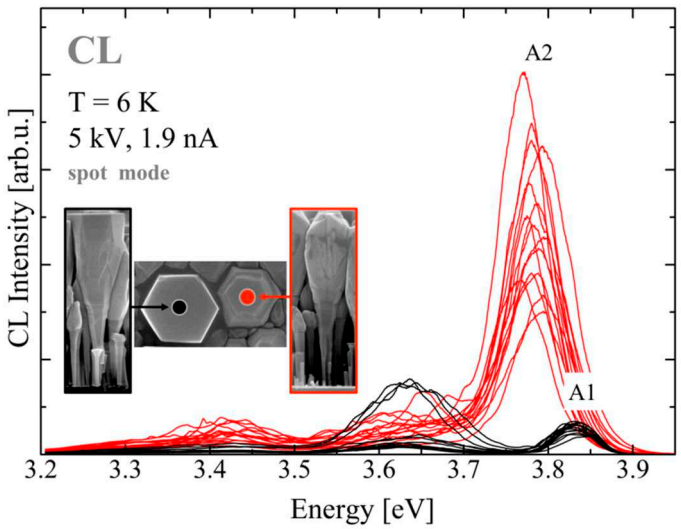


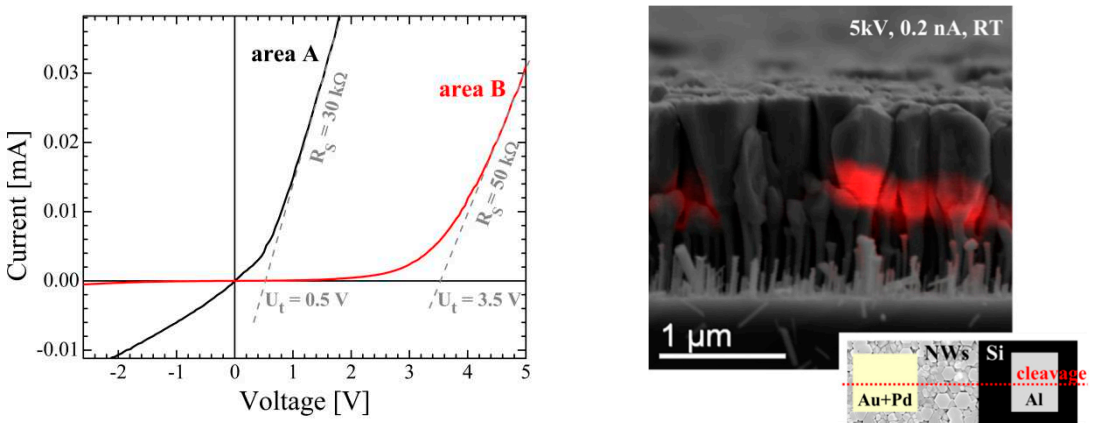
Figure 8. Series of cathodoluminescence spectra collected in the spot-mode using AV = 5 kV, where only the top (p-type) part of the structure is excited. Differences between NWs with flat hexagonal tops (black curves) and irregular ones (red curves) are clearly visible. The inset shows the geometry of the measurements.

3.3.2. EBIC and Nano-Probe Results

The EBIC technique was used to assess and analyze the local electrical properties of the structure. The interaction of the electron beam with the semiconductor structure results in the generation of electron–hole pairs, which are separated in the presence of an internal field near the p–n junction. As a result, an electrical current is generated, providing the EBIC signal.

This technique, combined with SEM, enabled the visualization of the position and continuity of the p–n junction and estimation of the width of the depletion region [42,43].

The electrical measurements conducted on the wafer with the NWs revealed that the NW LED structures in the central B area of the wafer exhibited diode-like I–V curves (Figure 9a), which means that we could expect a current generation caused by an electron beam. The obtained EBIC contrast image is presented in Figure 9b. EBIC measurements were performed at room temperature using an AV of 5 kV and I_b of 0.2 nA, without applying any bias voltage. The Au+Pd contact was deposited on the p-type NW tops using a sputter coater. Al contacts were deposited onto the exposed Si (n-type) substrate using the same method. The sample with deposited contacts was cleaved for EBIC measurements in the cross-sectional geometry. The EBIC contrast (red) superimposed on the SEM image (grey) revealed the position of the active part of the p–n junction. We observed a strong EBIC signal only in the NWs with the "oval-like" shape tops. The depletion region in these LED NWs was located on the side of the p-type part of the structure, and its width was about 300 nm. A Monte Carlo simulation of CL from GaN under such conditions shows that about 65% of the emission originates from a volume with a diameter of 10–15 nm. This also gives us an estimate of the lateral resolution of the EBIC experiment and confirms that it insignificantly interferes with the observed width of the depletion region [40]. This observation meant that the p-type part had a lower concentration of electrically active acceptor dopants, compared to the concentration of donors in the n-type part, even if the nominal concentration of the acceptors was ten times higher. This was due to the weak activation of Mg acceptors.



(**a**) (**b**)

Figure 9. (**a**) Macroscopic I–V curves of the A and B areas of the wafer. Lines fitted to the curves show serial resistance deduced from the slope and turn-on voltage deduced from the crossing with the zero axis. (**b**) SEM image (grey) with the superimposed EBIC signal (red) of the LED NWs. The strong EBIC signal reveals the position of the active p–n junction. The inset shows the geometry of the contacts.

To investigate the I–V characteristics of individual LED NWs, a tungsten-tip nanoprobe was used to form the top ohmic contact. The native tungsten oxide was preliminary removed from the tip using a 30 keV focused Ga+ ion beam. Thin silver wire, glued by conductive silver paste, provided the ohmic contact to the silicon substrate. The bias voltage was applied between the needle and the grounded substrate [44,45]. The current–voltage characteristics were measured for the two different types of nanowires with different shapes and polarities. The measurements were repeated on different spots of the sample, achieving a reasonable reproducibility (see Figure 10). The sharp hexagons (black curves) exhibit nonlinear, symmetrical I–V curves, with a low turn-on voltage. The NWs with the rounded edges (red curves) exhibit nonlinear and nonsymmetrical diode-like I–V curves.

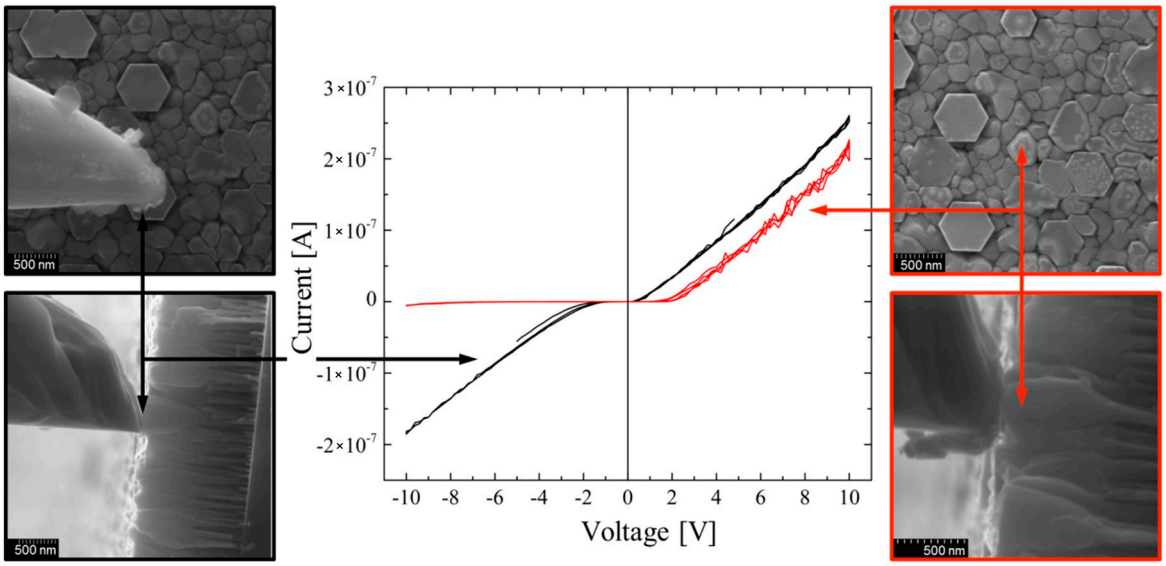


Figure 10. Series of I–V curves (central panel) of individual nanowires (NWs) (black curves: hexagonal top NWs; red curves: irregular NWs) and corresponding SEM images, showing the geometry of the measurements (sides). The sharp hexagons (black curves) exhibit nonlinear, symmetrical I–V curves with a low turn-on voltage, while the NWs with rounded edges (red curves) exhibit nonlinear and nonsymmetrical diode-like I–V curves.

Both the EBIC and nano-probe measurements revealed that the p–n junction works properly only in the NWs with the oval-like top segment and that only these NW structures act efficiently as LED diodes.

3.3.3. Kelvin Probe Force Microscopy

The change in the NW polarity should produce significant differences in the surface potential at the top of the NW. The surface potential profile at the microscale for individual NWs can be measured by Kelvin probe force microscopy (KPFM). The KPFM allows for the determination of the polarity of single NWs over micrometer-large surface areas with a nanometer resolution, without the need for any special sample preparation. In the KPFM studies, the local-contact potential difference (V_{CPD}) between the metallic tip and sample was measured. By scanning the sample surface in KPFM measurements, we can compare the potentials of different wires, and local changes can be determined.

Nitrides of V-group elements, including AlGaN, exhibit a strong built-in electric field caused by spontaneous polarization, together with a piezoelectric contribution due to a strain-related electric polarization along the AlGaN axis. We assume that the potential at the wafer and along the NW up to the QW region is the same for all NWs. Then, above the QW, the polarity is reversed, so the built-in field should be different by a few MV/cm. Consequently, we expected a difference in the potential at the top of the nanowire [30]. The V_{CPD} is expected to be higher at the N-polar than the Ga-polar surfaces. This assumption is in agreement with our calculations presented below and with earlier reports on GaN epitaxial layers [46] and nanowires [47] grown according to the MBE technique.

In the topography map (Figure 11a), the hexagonal wires appear to be higher and brighter. In the KPFM contrast (Figure 11b), still larger brightness differences between the hexagonal-shaped (N-polarity) and oval-shaped (Ga-polarity) NWs are visible. This means that the N-polar wires had a much higher electrical potential than the Ga-polar ones. In Figure 11c, the height and V_{CPD} profiles along the line marked in Figure 11a,b through four NWs are plotted as red and black curves. The black curve denotes the height profile from the AFM topography image, in which two NWs with flat hexagonal tops—NW2 and NW4—and two NWs with rough, oval tops—NW1 and NW3—are visible. The red curve is the profile of V_{CPD} from the KPFM contrast map. It can be seen that the surface potential is not correlated with the height of the NWs and is much higher for the NWs with flat

hexagonal tops; therefore, the contrast shown in the KPFM map is not an artifact resulting from the NW topography. The results of the KPFM experiments are fully consistent with the results concerning the polarity determination, performed by KOH etching of the NWs (see Section 3.1).

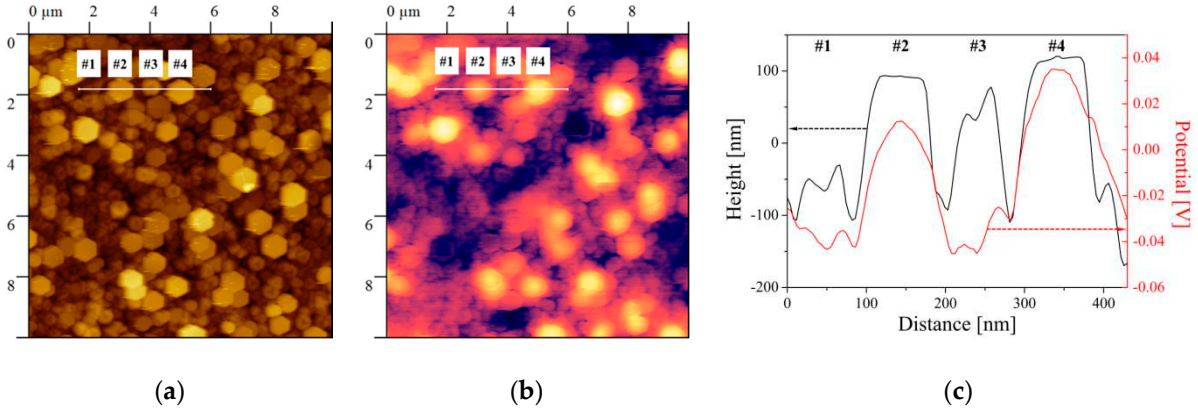


Figure 11. (**a**) Atomic Force Microscopy (AFM) topography (color scale from 0−500 nm), (**b**) the Kelvin probe force microscopy (KPFM) contrast map (color scale from 0−0.2 V), and (**c**) line-scan profiles of the height (in black) and potential on the surface (in red) through four NWs.

4. Discussion

It is known that during the growth of catalyst-free GaN on silicon using the PAMBE technique, the N-rich conditions promote columnar growth, leading to the formation of NWs that are mainly nitrogen-polar [18,48–50]. In the case of our GaN/AlGaN NW LED structures, the n-type part of the structure (GaN:Si) and the active region of the structure with three QWs, which were grown under N-rich conditions, exhibit nitrogen polarity, which was confirmed for many previously grown structures. During the growth of the p-type part, to enhance the Mg incorporation and increase the NW diameter, the temperature was decreased, which promoted lateral growth. However, lowering the growth temperature increases the possibility of stacking fault formation and switching of the polarity to Ga-polar. Moreover, such conditions enabled the more efficient incorporation of Mg dopant [51]. The polarity inversion induced by Mg-doping in GaN has been observed before by many groups, but usually 2D structures were studied, and the polarity changed from Ga- to N-polar in the samples from both the MOCVD and MBE growth processes [52–56]. It was reported that doping of N-face GaN with Mg resulted in a crystalline phase transition from wurtzite to zinc blende [57,58]. However, switching from N- to Ga-polarity was also observed as a result of Mg-doping during PAMBE growth. In one case, it was achieved by exposing the surface of the GaN layer to Mg and N fluxes during growth interruption at a reduced substrate temperature, and the formation of a Mg_xN_y compound was suggested to be responsible for inverting the crystal polarity [59]. In the second case, the polarity of GaN was inverted from the N- to Ga-face by inserting a composite AlN/AlO_x interlayer structure at the inversion interface [60].

In wurtzite structures, the growth polarity strongly influences the incorporation of dopants and impurities and affects the formation of native point defects. Additionally, the doping behavior of Mg and resulting conductivity of the doped structures were found to be strongly dependent on the surface polarity of the growing GaN planes. In the PAMBE process, the incorporation rate of the most common dopant used for achieving p-type conductivity is significantly higher in Ga-polar structures, while N-polar growth inhibits effective Mg doping. A lower Mg incorporation efficiency in N-face GaN has been predicted theoretically [61] and confirmed experimentally [53,62,63].

Oxygen atoms are one of the most common impurities in the GaN growth process, especially if Al-containing alloys are used. Oxygen acts as a shallow donor [64,65] and compensates Mg acceptors. It was widely reported that oxygen incorporation is also dependent on the growth polarity. Oxygen can be incorporated much more easily into N-polar (Al,Ga,In)N films in comparison to metal polar films. The higher oxygen incorporation efficiency on the N-polar surface was associated with a facile exchange between N-surface atoms and oxygen [62,66,67].

In order to understand the origin of different electrical characteristics of the two types of nanowires, a set of band profiles was calculated using a one-dimensional Drift-Diffusion Poisson Schrodinger Solver [68]. For simulation purposes, for each III-nitride layer, we consider only the majority dopant (i.e., acceptor or donor) concentrations, defined as the difference between the majority and minority type of dopant. Keeping in mind that the oxygen (donor) background doping levels that are typically observed are in a range between 1×10^{16}–5×10^{17} atoms/cm^3, the numbers indicated below may be significantly different to those implied by the dopant fluxes introduced during growth. In Figure 12, two band profiles obtained for unbiased structures of both types of NWs are compared. The black dotted line corresponds to the fully N-polar structure with n-type doping (2×10^{18} atoms/cm^3) below the MQW and p-type AlGaN:Mg (2×10^{15} atoms/cm^3) above it. Such a lightly doped structure should result in an extremely thick depletion region and could be easily perturbed by other effects, such as residual oxygen contamination. The blue dashed line in Figure 12 indicates how residual oxygen, at the relatively low concentration of 1×10^{16} atoms/cm^3, in the nominally p-type region changes the band profile, resulting in a lack of p–n junction in the structure. This effect could explain the lack of a rectifying characteristic in N-polar NWs, as shown in Figure 10. The last profile, represented by the red line in Figure 12, corresponds to the structure in which a p-type layer polarity inversion from N- to Ga-polar took place at the beginning, and the incorporation of 5×10^{16} atoms/cm^3 of Mg started. Our calculations show that this corresponds to a depletion width of approximately 300 nm situated above the MQW region, which is in agreement with the results of the EBIC studies. The assumed difference between the Mg concentrations for the Ga- and N-polar structures was in accordance with the previously reported discrepancy between both polarities [53].

In fact, there is only a small difference in doping between the models, which are represented by the black and blue curves in Figure 12. However, as shown in Figure 12, this difference is sufficient to induce a change from a weak p-type to a weak n-type semiconductor. It is possible that some N-polar NWs are slightly p-type, some are slightly n-type, and some are insulating. We have observed that some of them are electrically conductive, such as those shown in Figures 9a and 10, and some are insulating. The slightly n-type NWs have their electric fields screened at the top, which is shown as the flattening of the blue dashed curve in Figure 12. This means that this part of the NW can emit CL, which is in agreement with the observation that some N-polar NWs emitted bright luminescence from their tops. It is also worth noting that the potential on the top of the Ga-face NWs is lower than the potential of the N-face NWs, which is in agreement with the KPFM measurements.

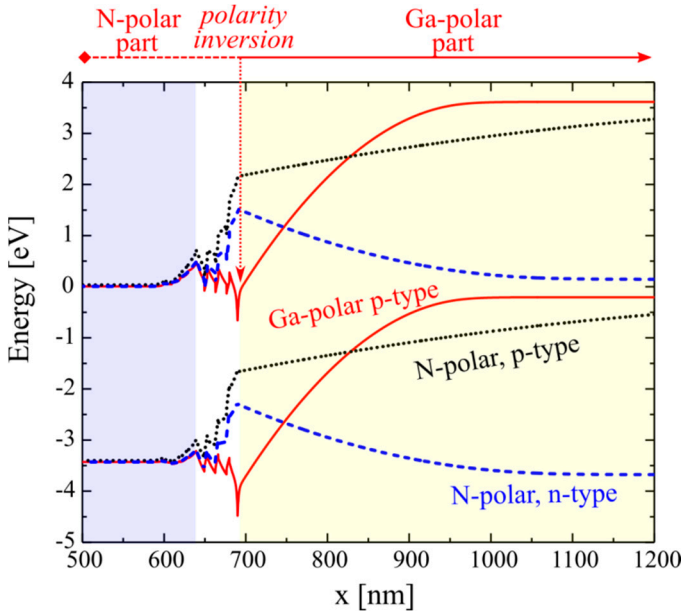


Figure 12. Conduction and valence band profiles for three different nanowire structures, as a function of the location in the wire. The growth direction goes from left to right. The dotted black line denotes the profile for a lightly doped N-polar structure, with a 2×10^{15} atoms/cm^3 Mg concentration. The dashed blue line denotes the profile for the case in which oxygen compensated p-type doping, resulting in n-type doping. The red profile corresponds to the structure in which polarity inversion took place right at the beginning of the p-type layers. The dotted arrow indicates the position where polarity inversion took place for the wire presented in red. From that moment, the structure was Ga-polar, with a 5×10^{16} atoms/cm^3 Mg concentration. The vertical axis shows the electron energy $E = -e\Phi$, where Φ is the potential.

5. Summary and Conclusions

A comprehensive dataset revealing the optical and electrical properties of individual nanoLED structures embedded in GaN/AlGaN NWs emitting EL at approximately 3.3 eV has been collected. The results were obtained by complementary SEM, TEM, CL, and EBIC spectroscopy and imaging; AFM and Kelvin probe force microscopy experiments; and I–V characteristics measurements for individual NWs using a nano-probe. Further information was acquired by studying the properties of NW ensembles using electroluminescence and time-resolved photoluminescence.

We identified two types of nanowires that differ in terms of the shape of their upper parts. KOH etching and KPFM studies show that they have different polarities. We believe that unintentional fluctuations in the conditions during the growth of the Mg-doped AlGaN part of the structure caused a reversal of the growth polarity of some NWs from the N- to Ga-face.

The interpretation of the experimental data was supported by the results of numerical simulations of the electronic band structure of individual NWs, which allowed the physical mechanisms responsible for the activation or deactivation of the p–n junctions, depending on the polarity of the last p-type part in the nanoLED structures, to be discussed.

The experimental techniques with a spatial nano-resolution allowed for the study of the correlating luminescence and electrical properties of NWs, with the growth polarity switching in the p-type AlGaN part of the NW. The CL spectra showed that the N-face NWs had emissions at the highest energy of 3.83 eV, while the Ga-face NWs energy of emissions was mainly at 3.78 eV. The lower emission energy of the Ga-polarity NWs indicated that there was a lower Al content in these NWs. This, in turn, suggested a higher Ga desorption for N-face NWs than for Ga-face NWs. The monochromatic CL maps provided clear evidence of the QW emission at about 3.5 eV at helium temperature, which is the main recombination path producing electroluminescence in nanoLEDs. We observed that only Ga-polar NWs emitted bright luminescence from QWs. This is a clear indication that

switching polarity was crucial for LED efficiency. According to our calculations of the band structure of the NWs, the change in polarity induced an electric field profile that attracted carriers to the region of QWs, which is the necessary condition for bright light emission. The EBIC mapping proved that p–n junctions were not active in N-polarity NWs, while Ga-polar NWs generated a strong current when excited in the junction area. The observed depletion region was mostly on the p-type side of the junction due to the relatively weak activation of Mg acceptors. The time-resolved photoluminescence showed that the lifetime of the QW-related emission was about 1–2 ns, which proved good quality QWs. The electroluminescence experiments showed that an ensemble of the investigated nanoLED NWs was acceptable as a source of UV radiation, with an energy of about 3.3 eV.

The collected data and results of numerical simulations indicate that the intentional polarity inversion between the n- and p-type parts of NWs is a potential path towards the development of efficient nanoLED NW structures. We believe that a more effective p-type doping of AlGaN, supporting an active p–n junction, would prevail over the disadvantage of the possible creation of structural defects in the polarity inversion region.

Author Contributions: Conceptualization, K.P.K., A.R., B.J.K. and Z.R.Z.; methodology, A.R., K.P.K. and B.J.K.; software, H.T.; formal analysis, A.R., K.P.K. and H.T.; investigation, A.R., K.P.K., S.T., S.K., R.B. and U.J.; resources, M.S. and Z.R.Z.; writing—original draft preparation, A.R., K.P.K., B.J.K. and H.T.; writing—review and editing, Z.R.Z., S.T., U.J. and M.S.; visualization, A.R., K.P.K. and H.T.; supervision, K.P.K., B.J.K. and Z.R.Z.; funding acquisition, B.J.K., Z.R.Z. and H.T. All authors have read and agreed to the published version of the manuscript.

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