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Miniaturized Transistors, Volume II

Edited by

Lado Filipovic and Tibor Grasser

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About the Editors

Lado Filipovic

Lado Filipovic (Dr.) is an Assistant Professor (tenure-track) of Modeling and Simulation of Integrated Semiconductor Sensors at TU Wien. He obtained his venia docendi (habilitation) in Semiconductor Based Integrated Sensors and his doctoral degree (Dr.techn.) in Microelectronics from TU Wien in 2020 and 2012, respectively. He holds a Master's degree in Applied Sciences (MASc.) from Carleton University in Ottawa, Canada, which he obtained in 2009. He is a Senior Member of the IEEE and is an active member of the Technical Program Committee for outstanding IEEE sponsored conferences, such as IEEE Sensors, SISPAD, and IIRW. He has been a Principal Investigator in various research projects funded by, e.g., the EU FP7 and Horizon 2020 programs and the Austrian Research Promotion Agency (FFG). His primary research interest is studying the operation, stability, and reliability of novel semiconductor-based sensors using advanced process and device TCAD approaches. One of his research pillars is combining physical and empirical modeling approaches, specifically in the TCAD process. With his team, he is actively investigating metal oxide semiconductors and two-dimensional materials, e.g., graphene, MoS2, and phosphorene for the detection of environmental pollutants and biomarkers from exhaled breath.

Tibor Grasser

Tibor Grasser (Prof. Dr.) is a professor of microelectronics reliability and an IEEE Fellow. He has been the head of the Institute for Microelectronics since 2016. He has edited various books, e.g., on the bias temperature instability, hot carrier degradation, and noise (all Springer), is a distinguished lecturer of the IEEE EDS, is a recipient of the Best and Outstanding Paper Awards at IRPS (2008, 2010, 2012, and 2014), IPFA (2013 and 2014), ESREF (2008), and the IEEE EDS Paul Rappaport Award (2011). He currently serves as an Associate Editor for the IEEE Transactions on Electron Devices following his assignment as Associate Editor for Microelectronics Reliability (Elsevier) and has been involved in various outstanding conferences such as IEDM (General Chair 2021), IRPS, SISPAD, ESSDERC, and IIRW. Prof. Grasser's current research interests include theoretical modeling of performance aspects of 2D and 3D devices (charge trapping and reliability), starting from the ab initio level over more efficient quantum-mechanical descriptions up to TCAD modeling. The models developed in his group have been made available in the most important commercial TCAD environments.

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Editorial

Special Issue on Miniaturized Transistors, Volume II

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Due to the great success of the initial Special Issue on Miniaturized Transistors [1], we have decided to continue addressing the ever-advancing progress in microelectronic device scaling with this second volume. Complementary Metal-Oxide-Semiconductor (CMOS) devices continue to endure miniaturization, irrespective of seeming physical limitations to scaling, helped by advancing fabrication techniques. We also observe that miniaturization does not always refer to the latest technology node for digital transistors. Rather, by applying novel materials and device geometries, we note that a significant reduction in the size of microelectronic devices for a broad set of applications can be achieved. The achievements made in the scaling of devices for applications beyond digital logic (e.g., power applications, optoelectronics, and sensors) are taking the front stage in microelectronic miniaturization. Furthermore, all these achievements are assisted by improvements in the simulation and modeling of the involved materials and device structures. In particular, process and device technology computer-aided design (TCAD) has become indispensable in the design cycle of novel devices and technologies.

There are 19 research papers published in this Special Issue, covering recent advances in research aspects related to transistor miniaturization, including theoretical assessments of novel device geometries, the application of wide bandgap materials for high-power applications, modeling techniques for highly scaled devices, as well as devices for applications in optoelectronics and sensing. Furthermore, three reviews are included in this Special Issue, one which looks into transistor scaling along Moore's Law and presents ideas about what lies ahead [2], another which investigates the applicability of metal oxide/polymer heterojunctions for flexible and portable electronics [3], and a third which performs an analysis of the reliability of highly scaled devices, where the charging kinetics of single defects play a critical role [4].

The three review articles which are provided in this Special Issue nicely summarize the impact of miniaturization on the current semiconductor device landscape. They include transistor scaling along Moore's Law and the introduction of new materials and hetero-junctions for exciting new applications in flexible and portable electronics. However, miniaturisation and scaling come at a price, as is discussed in the third review, which looks into the impact of defects in highly scaled devices. Radamson et al. [2] provide a review on the development of the metal-oxide-semiconductor field-effect transistor (MOSFET) over the last decades while following the international technology roadmap of semiconductors (ITRS). They focus on methodologies, challenges, and difficulties when ITRS approaches the end and discuss new and emerging channel materials beyond the Moore era. Jeong et al. [3] provide a thorough review of the application of hybrid polymer/metal oxide films for flexible and wearable devices. These nanocomposites are excellent materials for flexible electronics due to the combined benefits of durability of the polymers and excellent electronic properties of the metal oxides. The authors highlight the advances made in improving the electrical performance of these devices by studying their mobilities and dielectric constants, as well as looking into interface engineering and its impact on the electronic properties. Waltl [4] wraps up this Special Issue with a thorough look into the reliability of highly scaled semiconductor transistors. As transistors are miniaturized further, single defects play an ever-increasing role in the device performance and reliability.

Waltl takes a look into bias temperature instability (BTI) at the single-defect level to provide an in-depth investigation of charge trapping kinetics of the defects to ultimately provide an accurate assessment of the device lifetime.

The impact of single defects is also studied by Stampfer et al. [5]. The authors of this paper look at the adverse effects of miniaturization. Mainly, they observe how miniaturization leads to increased variability among nominally identical devices, primarily due to the increased relative impact of oxide traps. With random telegraph noise (RTN) measurements, the authors are able to extract the step heights of defects present at the Si/SiO_2 interface. They note that, contrary to recently published studies, a bimodal distribution in step heights can be observed. Cheung, in [6], on the other hand, explores the potential application of a single-defect MOSFET device towards the realization of the elusive quantized current source. Their experimental results on a single-defect MOSFET shows that the one charge pumped per cycle is valid, encouraging further exploration of charge pumping based on quantum current sources.

With increased device scaling and the uncertainty of what lies beyond Moore's law once the physical limits are reached, many researchers are theorizing about novel transistor designs. For this, applying advanced TCAD tools is indispensable. It is no longer a reasonable expectation that any potential design can be tested in a lab, as this comes with extremely high costs, especially at the leading technology nodes. Instead, many researchers rely on TCAD as an initial assessment of their proposed device ideas. With this in mind, in [7], Wulf presents a compact nanotransistor model which allows for the extraction of important device parameters such as the effective height of the source-drain barrier, device heating, and the quality of the coupling between the conduction channel and the contacts. This model is then used to quantitatively describe quantum transport in a variety of industrial nano-FETs. Medina-Bailon et al. [8] presented a quantum enhancement of a 2D Multi-Subband Ensemble Monte Carlo (MS-EMC) simulator, specifically to observe transistor behavior at the nanometer scale. Kim et al. [9] use TCAD simulations to examine the differences between the memory mechanisms in poly-silicon and silicon body one-transistor dynamic random-access memory (1T-DRAM) cells. They found that a poly-silicon 1T-DRAM can perform memory operations by using grain boundaries (GBs) as storage regions in thin body devices with a small floating body (FB) area. Zhang et al. [10] propose an implementation of a novel core-insulator gate-all-around (CIGAA) nanowire transistor which exhibits low off-state current compared to that of traditional gate-all-around (GAA) nanowire devices, making it ideal for future energy-efficient applications. Han et al. [11] proposed a germanium-based GAA transistor, which shows an all-around improved performance when compared to silicon GAA FETs. Specifically, the germainum GAA FET exhibits a higher ON/OFF ratio compared to silicon and a steady and steep average subthreshold swing. Chen et al. [12] presents a three-input, three-channel field effect transistor (TI-TcFET) design with multiple gate contacts (top, front, and back) in order to increase the gate control of the channel. The authors show that the proposed device could be used to simplify complex circuits by using less transistors than in traditional CMOS technology.

Beyond digital logic, high-power electronic devices are playing a very important role in today's technology development. They are essential components in the push towards autonomous vehicles and safer air and space travel, while also providing important progress towards green energy applications and overall increase in energy efficiency. Six papers in this Special Issue look into novelties related to high-power electronic devices, mostly using wide-bandgap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN). Chien et al. [13] study the application of a split-gate trench (SGT) power metal-oxide-semiconductor field-effect transistor (MOSFET) to reduce specific ON resistance. They note that the bottom epitaxial layer of a double-epitaxy structure can be designed to support the breakdown voltage, while the top one can be adjusted to reduce the ON resistance. Jia et al. [14] present a 4H-SiC metal-semiconductor field-effect transistor (MESFET) with layered doped and undoped regions. After optimizing the thickness of the

undoped region, the authors obtained an increase in the power-added efficiency (PAE) of 85.8% and a saturation current increase of 27.4%, when compared to the double-recessed 4H-SiC MESFET. Li et al. [15] tested the surge reliability of 1200 V SiC MOSFETs from various manufactures by stressing them until failure. By decapping the failed devices and observing the cross-section of the damaged cell, they found that high temperature caused by excessive current flow through the devices during the surge tests is the main culprit for failure. In a contribution by Li et al. [16], the authors propose and test a SiC MOSFETs device which is able to meet the requirements of DC microgrid protection. Their prototype was developed, tested, and compared to the silicon-based insulated gate bipolar transistor (IGBT) alternative, showing high promise in its application in a solid-state circuit breaker. Guo et al. [17] looked into the thermal characteristics of pulse-operated AlGaN/GaN high-electron-mobility transistors (HEMTs). Their models show that the maximum channel temperature and thermal impedance of the devices are considerably influenced by the pulse width and power density, while the geometry of the gates, i.e., variations in the gate fingers and their width, have no effect on the channel temperature, as long as the total gate width and active area is kept constant. Zhu et al. [18] propose a new design for a multi-recessed double-recessed p-buffer layer 4H–SiC metal semiconductor field effect transistor (IMRD 4H-SiC MESFET) with high PAE. Their design shows an improvement in the PAE of almost 70%, when compared to similar state-of-the-art designs. In an additional contribution from Zhu et al. [19], a novel AlGaN/GaN HEMT is proposed, with a high gate and a multi-recessed buffer (HGMRB) for high-energy-efficiency applications. Their design promises an increase in the breakdown voltage by 16.7%, while the gate-to-source capacitance is decreased by 17%. The radio frequency (RF) simulations showed impressive PAEs of 90.8%, 89.3%, and 84.4% at 600 MHz, 1.2 GHz, and 2.4 GHz, respectively.

This Special Issue also looks at applications beyond digital logic and high-power applications. Several research papers have been included, which discuss novel sensing and imaging technologies. Cheng et al. [20] studied the potential of using vacuum channel transistors in low-loss and high-speed electronics for operation in high-temperature and high-radiation environments. Their measurements of vertical diodes further show that current and voltage vary based on the pressure and gas composition of the ambient, suggesting a potential application of these devices for gas and pressure sensing. Mao et al. [21] theorized a floating gate transistor with two control gates in order to provide active noise control in bio-electrical measurements. The advantage of their implementation is the ability to use a cost-efficient single-polysilicon CMOS fabrication process. Zhi et al. [22] presented a novel avalanche photodiode (APD) design, which is compatible with Taiwan Semiconductor Manufacturing Company (TSMC)'s standard CMOS process, realizing scaling in these devices by enabling an integration between the optoelectronic and digital components. The fabricated device is able to operate at a wavelength of 850 nm. Finally, McGhee and Georgiev in [23] apply semi-empirical density functional theory (DFT) calculations to study the surface transfer doping process between hydrogen-terminated (100) diamond and the metal oxides MoO_3 and V_2O_5. Their study shows that both oxides act as electron acceptors and inject holes into the diamond structure, meaning that these metal oxides can be described as p-type doping materials for diamond. The study suggests the ability to use deposited metal oxides in an oxygen-rich atmosphere to enhance the surface transfer doping between diamond and the oxides.

Finally, we would like to take this opportunity to thank all the authors for submitting exceptional and highly relevant research papers to this Special Issue. We would also like to sincerely thank all the reviewers who took precious time to carefully examine and help improve the quality of all submitted manuscripts. Peer review is an essential component of good science, and they deserve recognition for the success of this Special Issue. It is our sincere hope that the results provided in this Special Issue prove useful to scientists and engineers who find themselves at the forefront of this rapidly evolving and broadening field. Now, more than ever, it is essential to look for solutions to find the next disrupting technologies which will allow for transistor miniaturization well beyond silicon's physical

limits and the current state-of-the-art. This requires a broad attack, including studies of novel and innovative designs as well as emerging materials which are becoming more application-specific than ever before.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Filipovic, L.; Grasser, T. Editorial for the Special Issue on Miniaturized Transistors. *Micromachines* **2019**, *10*, 300. [CrossRef] [PubMed]
2. Radamson, H.H.; He, X.; Zhang, Q.; Liu, J.; Cui, H.; Xiang, J.; Kong, Z.; Xiong, W.; Li, J.; Gao, J.; et al. Miniaturization of CMOS. *Micromachines* **2019**, *10*, 293. [CrossRef] [PubMed]
3. Jeong, J.W.; Hwang, H.S.; Choi, D.; Ma, B.C.; Jung, J.; Chang, M. Hybrid Polymer/Metal Oxide Thin Films for High Performance, Flexible Transistors. *Micromachines* **2020**, *11*, 264. [CrossRef] [PubMed]
4. Waltl, M. Reliability of Miniaturized Transistors from the Perspective of Single-Defects. *Micromachines* **2020**, *11*, 736. [CrossRef] [PubMed]
5. Stampfer, B.; Schanovsky, F.; Grasser, T.; Waltl, M. Semi-Automated Extraction of the Distribution of Single Defects for nMOS Transistors. *Micromachines* **2020**, *11*, 446. [CrossRef]
6. Cheung, K.P.; Wang, C.; Campbell, J.P. Nanoscale MOSFET as a Potential Room-Temperature Quantum Current Source. *Micromachines* **2020**, *11*, 364. [CrossRef]
7. Wulf, U. A One-Dimensional Effective Model for Nanotransistors in Landauer–Büttiker Formalism. *Micromachines* **2020**, *11*, 359. [CrossRef]
8. Medina-Bailon, C.; Carrillo-Nunez, H.; Lee, J.; Sampedro, C.; Padilla, J.L.; Donetti, L.; Georgiev, V.; Gamiz, F.; Asenov, A. Quantum Enhancement of a S/D Tunneling Model in a 2D MS-EMC Nanodevice Simulator: NEGF Comparison and Impact of Effective Mass Variation. *Micromachines* **2020**, *11*, 204. [CrossRef]
9. Kim, H.; Yoo, S.; Kang, I.M.; Cho, S.; Sun, W.; Shin, H. Analysis of the Sensing Margin of Silicon and Poly-Si 1T-DRAM. *Micromachines* **2020**, *11*, 228. [CrossRef]
10. Zhang, Y.; Han, K.; Li, J. A Simulation Study of a Gate-All-Around Nanowire Transistor with a Core–Insulator. *Micromachines* **2020**, *11*, 223. [CrossRef]
11. Han, K.; Long, S.; Deng, Z.; Zhang, Y.; Li, J. A Novel Germanium-Around-Source Gate-All-Around Tunnelling Field-Effect Transistor for Low-Power Applications. *Micromachines* **2020**, *11*, 164. [CrossRef] [PubMed]
12. Chen, Z.; Hu, J.; Ye, H.; Chu, Z. T-Channel Field Effect Transistor with Three Input Terminals (Ti-TcFET). *Micromachines* **2020**, *11*, 64. [CrossRef] [PubMed]
13. Chien, F.T.; Wang, Z.Z.; Lin, C.L.; Kang, T.K.; Chen, C.W.; Chiu, H.C. 150–200 V Split-Gate Trench Power MOSFETs with Multiple Epitaxial Layers. *Micromachines* **2020**, *11*, 504. [CrossRef] [PubMed]
14. Jia, H.; Liang, Y.; Li, T.; Tong, Y.; Zhu, S.; Wang, X.; Zeng, T.; Yang, Y. Improved DRUS 4H-SiC MESFET with High Power Added Efficiency. *Micromachines* **2020**, *11*, 35. [CrossRef] [PubMed]
15. Li, H.; Wang, J.; Ren, N.; Xu, H.; Sheng, K. Investigation of 1200 V SiC MOSFETs' Surge Reliability. *Micromachines* **2019**, *10*, 485. [CrossRef] [PubMed]
16. Li, H.; Yu, R.; Zhong, Y.; Yao, R.; Liao, X.; Chen, X. Design of 400 V Miniature DC Solid State Circuit Breaker with SiC MOSFET. *Micromachines* **2019**, *10*, 314. [CrossRef]
17. Guo, H.; Chen, T.; Shi, S. Transient Simulation for the Thermal Design Optimization of Pulse Operated AlGaN/GaN HEMTs. *Micromachines* **2020**, *11*, 76. [CrossRef]
18. Zhu, S.; Jia, H.; Wang, X.; Liang, Y.; Tong, Y.; Li, T.; Yang, Y. Improved MRD 4H-SiC MESFET with High Power Added Efficiency. *Micromachines* **2019**, *10*, 479. [CrossRef]
19. Zhu, S.; Jia, H.; Li, T.; Tong, Y.; Liang, Y.; Wang, X.; Zeng, T.; Yang, Y. Novel High-Energy-Efficiency AlGaN/GaN HEMT with High Gate and Multi-Recessed Buffer. *Micromachines* **2019**, *10*, 444. [CrossRef]
20. Chang, W.T.; Hsu, H.J.; Pao, P.H. Vertical Field Emission Air-Channel Diodes and Transistors. *Micromachines* **2019**, *10*, 858. [CrossRef]
21. Mao, C.; Yang, C.; Ma, H.; Yan, F.; Zhang, L. A Smart Floating Gate Transistor with Two Control Gates for Active Noise Control. *Micromachines* **2019**, *10*, 722. [CrossRef] [PubMed]
22. Zhi, W.; Quan, Q.; Yu, P.; Jiang, Y. A 45 nm CMOS Avalanche Photodiode with 8.4-GHz Bandwidth. *Micromachines* **2020**, *11*, 65. [CrossRef] [PubMed]
23. McGhee, J.; Georgiev, V.P. Simulation Study of Surface Transfer Doping of Hydrogenated Diamond by MoO_3 and V_2O_5 Metal Oxides. *Micromachines* **2020**, *11*, 433. [CrossRef] [PubMed]

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Review

Miniaturization of CMOS

Henry H. Radamson [1,2,3,*,†], Xiaobin He [1,†], Qingzhu Zhang [1,4,†], Jinbiao Liu [1,†], Hushan Cui [5,†], Jinjuan Xiang [1,†], Zhenzhen Kong [1,†], Wenjuan Xiong [1,2,†], Junjie Li [1,2,†], Jianfeng Gao [1,†], Hong Yang [1,2,†], Shihai Gu [1,6,†], Xuewei Zhao [1,7,†], Yong Du [1,2,†], Jiahan Yu [1,†] and Guilei Wang [1,2,*,†]

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Abstract: When the international technology roadmap of semiconductors (ITRS) started almost five decades ago, the metal oxide effect transistor (MOSFET) as units in integrated circuits (IC) continuously miniaturized. The transistor structure has radically changed from its original planar 2D architecture to today's 3D Fin field-effect transistors (FinFETs) along with new designs for gate and source/drain regions and applying strain engineering. This article presents how the MOSFET structure and process have been changed (or modified) to follow the More Moore strategy. A focus has been on methodologies, challenges, and difficulties when ITRS approaches the end. The discussions extend to new channel materials beyond the Moore era.

Keywords: FinFETs; CMOS; device processing; integrated circuits

1. Introduction

In 1965, Gordon Moore, the founder of Intel, published his famous paper describing the evolution of transistor density in integrated circuits. Although his first insight was to establish a business roadmap to increase the profit of the company, he later built the fundaments for technology roadmap in the semiconductor industry. Moore's idea was based on doubling the transistor density in the chip every 18 months, which causes the transistors to become smaller in size and consumes lower power while performing at higher speed [1].

With years of continuing MOSFETs (metal oxide effect transistor) down-scaling, different non-ideal factors e.g., short channel effects (SCEs), poor electrostatics integrity, and large device variability appeared. Therefore, conventional bulk FinFET and fully depleted silicon on the insulator (FDSOI) are proposed to improve the above problems by applying low gate voltage to fully deplete the ultra-thin silicon [2]. Currently, bulk FinFET has been widely used in mass production from 22 nm to 10 nm

node and will be extended to the 5-nm node [3–6]. In fact, the critical dimension (CD) of the device, e.g., gate length (L_g), applied voltage (V_{DD}), and effective oxide thickness (EOT) are not strictly scaling, according to the Moore's law. The foundries seek an improvement of driving current (I_{DS}) at the same leakage or achieve the smaller leakage at the same I_{DS}. On the approach to the end of the technology roadmap, the 3-nm node and the traditional bulk FinFET technologies would suffer from enormous challenges [7]. Thus, new device structures, new materials, and new integration approaches have to provide new solutions. Therefore, novel promising device architectures like fin-on-insulator (FOI) FinFET [8–11], scalloped fin FinFET [12], nanowire (NW) FETs, and the stacked NW device [13–15] have demonstrated great improvement for short channel effects (SCEs), leakage control, and higher electron and whole mobility. The fin-on-insulator (FOI) FinFET, fabricated on the bulk Si substrate with a special process takes both advantages of bulk FinFET and SOI technologies. Therefore, it may be one of the most promising candidates for further device scaling. In addition, the low cost and fully Metallic Source and Drain (MSD) process is extensively investigated for the FOI FinFET [9].

Other architecture such as scalloped fin FinFETs with mainstream all-last HKMG (high-*k* and metal-gate) technology could provide a larger control area and obtain a great improvement for SCEs. Stacked gate-all-around (GAA) NW or nano-sheet is also receiving increasing attention among all device structures. This is considered to be the most promising candidate beyond FinFET technologies for a 3-nm node due to its special characteristic, such as quasi-ballistic transport, steep sub-threshold slope, and one-dimensional channel geometry [13,14].

3D-monolithic or 3D sequential CMOS technology is based on stacking active device layers on top of each other with very small 3D contact pitch (similar pitch as a standard contact) [16,17]. This approach could achieve a 14-nm circuit performance by using 3D sequential CMOS technology with lower parasitic resistance, capacitor, and signal delay. In addition, this integration scheme offers a wide spectrum of applications including (i) increasing integration density beyond device scaling, (ii) enabling neuromorphic integration where RRAM is placed between top and bottom tiers, and (iii) enabling low-cost heterogeneous integration for e.g., smart sensing arrays. However, such an integration process faces the challenges of fabricating high-performance devices in the top tier without degrading the electrical characteristics of the bottom tier [18,19].

The CMOS scaling-down in process, V_{DD}, and temperature (PVT) are becoming a major issue for the nanoscale IC design. The need for low power induces supply voltage scaling, which makes voltage variations a significant design challenge. Moreover, the operation frequency is sensitive to die temperature variations. Therefore, it is increased at high junction temperatures. It is known that process variations are a serious concern due to uncertainty in the device and interconnects characteristics. Process variations negatively impact the speed, stability, and power consumption of traditional transistor designs.

With the continuing scaling of devices, the driving current would become bigger and the frequencies of transmitted signals become higher [20,21].

This article presents how the technology roadmap deal with miniaturization of CMOS including advanced lithography for patterning nano-scaled transistors, process integration, (wet and dry) etching, strain engineering with an emphasis on SiGe epitaxy for source/drain (S/D), dopant implantation, gate formation including deposition of high-*k* material, and the metal gate using the atomic layer deposition (ALD) technique, and III-V materials for high carrier mobility in the channel for FinFETs. The discussions have a focus on the challenges and difficulties of the path of More Moore and even provide a glimpse of the beyond Moore era for CMOS.

2. Miniaturization Principles

Figure 1 shows the official technology roadmap, which was originally established in the early 1970s and the semiconductor industries began to down scale the transistors [22]. In 2003, when the transistor size shrunk to sub 100 nm, the nano-electronic era was inaugurated. The continuation of down-scaling lead to the parasitic capacitance and the resistance increased. Lastly, the 2D transistors

were abandoned and 3D FinFETs were introduced. This is considered as a revolutionary design in the transistor world, which paved the path for sub 22 nm FinFETs with high performance and full control on the carrier transport in the channel.

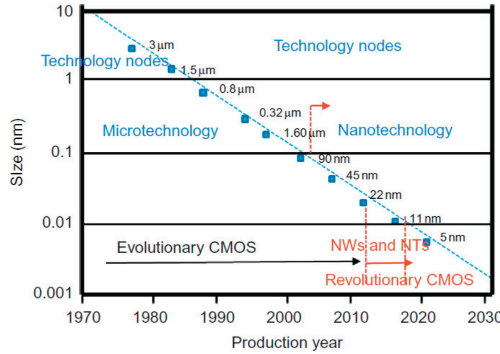


Figure 1. Miniaturization of the transistor gate length in different technology nodes and production years [22].

The down-scaling of the transistors results in operation at lower supply voltages as well as switching with less current.

On one hand, the shorter channel causes lower gate capacitance and higher drive current resulting in faster transistors. On the other hand, the shorter channels contribute to higher S/D and Gate leakage since gate oxide becomes thinner. The smaller transistors have both lower V_{DD} and threshold voltage (V_T) or, in principle, lower dynamic power is obtained. The main rules to miniaturize MOSFET with a factor of γ is demonstrated in Figure 2 [23]. This task is performed for transistors when the gate length and width, oxide thickness, junction depth, and substrate doping are downscaled. Therefore, both supply and threshold voltages are also scaled by a factor of γ. In this way, the electric field is maintained constant. Meanwhile, the density of transistors is increased by factor of γ^2. In this design, the ratio between gate length and width is also unchanged.

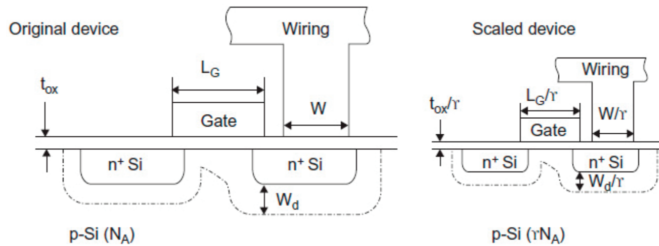


Figure 2. A schematic drawing of MOSFET downscaling [23].

However, information on the size of the pitch in nanometer technologies and the freedom in choosing the size of the transistors can be different. Simply, the pitch parameter may not follow the same trend as the general miniaturization of technologies.

3. Lithography of Nano-Scaled Transistors

A state-of-the-art lithography seeks sharp patterns with high reproducibility. For 20-nm and 14-nm node technology, 193 nm ArF immersion with multiple patterning has been mainly used [24]. Meanwhile, 193-nm immersion with self-aligned double patterning (SADP) and self-aligned quadruple patterning (SAQP) techniques is intended to be used for a 7-nm technology node [24].

SADP is a technique which applied spacer transfer process for small pitch whereas SAQP is applied twice self-aligned double patterning to develop very narrow features [25].

There is a strong effort to apply extreme ultraviolet (EUV) lithography and 193 nm immersion with multi-patterning for a 7-nm node. Although EUV simplifies the patterning process for the 7-nm node, EUV still has issues with resists and mask infrastructure as well as the power source, which have to be solved before high-volume manufacturing.

Figure 3 indicates that the lithography cost depends on the layer and, therefore, the cost of applying either 193i triple patterning or 193i SADP are roughly equal to single-patterning with EUV. This means that the choice of the lithography method depended more on the performance-involved trade-offs [26]. For 7-nm and 5-nm nodes, there is a risk that quad-patterning may occur from 193i and double-patterning from existing EUV tools, or single-patterning from as-yet undelivered high numerical aperture (NA) EUV tools.

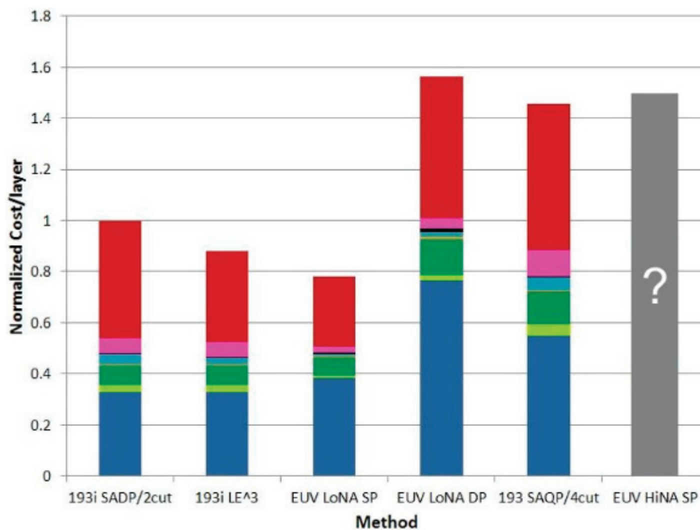


Figure 3. Normalized cost/layer vs. lithography method.

To apply 193 nm immersion lithography with multiple patterning for 7-nm and 5-nm nodes has difficulties. The main problem is overlay, which involves the ability of a scanner to align the various mask layers accurately on top of each other. There may be too many masks at each new node. This slows down throughput in the mask shop, increases the possibility that errors will be introduced, and raises the cost at the same time.

Recently, it has demonstrated excellent industrialization progress of its pellicle, with tests confirming that pellicles can withstand 245 W source power and an offline power lifetime test indicating 400 W capability. Compared to the 7-nm logic node, the requirements for EUV masks is tighter for 5 nm. Meanwhile there is good progress to support 5 nm in areas such as reducing mask blank defects [27,28].

The EUV mask infrastructure is the need to manufacture defect-free photo masks where an actinic mask review capability is a critical success factor [29,30]. The ongoing development for anEUV pellicle solution alleviates industry concern about one significant source of line-yield risk [31]. Because pellicles are currently unavailable for EUV lithography, other measures need to be taken to deal with contamination that can occur during mask transport and usage. Such contamination can indeed occur, and it has been observed by practitioners of EUV lithography. This may occur with sufficient frequency, which justifies the concern for repeating defects that can reduce the yield significantly [32].

In addition to the high EUV sensitivity, low local CD uniformity, and high patterning resolution, the next generation resist systems should also efficiently solve the issues of pattern collapse, resist homogeneity, etch resistance, UV out of band, outgassing, high volume manufacturing (HVM) compatibility, defects, and shelf-life [33].

To improve throughput in HVM, the resist sensitivity to the 13.54-nm wavelength radiation of EUV needs to be improved while the line-width roughness (LWR) specification must be held to low single-digit nm. With a 250 W source and 25 mJ/cm^2 resist sensitivity, an EUV stepper should be able to process ~100 wafer-per-hour (wph), which should allow the affordable process when matching with other lithography technologies.

Figure 4 shows that higher absorption allows the use of thinner resist, which mitigates the issue of line collapse. Resistance as thin as 18 nm has been patterned over a 70-nm thin Spin-On Carbon (SOC) layer without the need for another Bottom Anti-Reflective Coating (BARC).

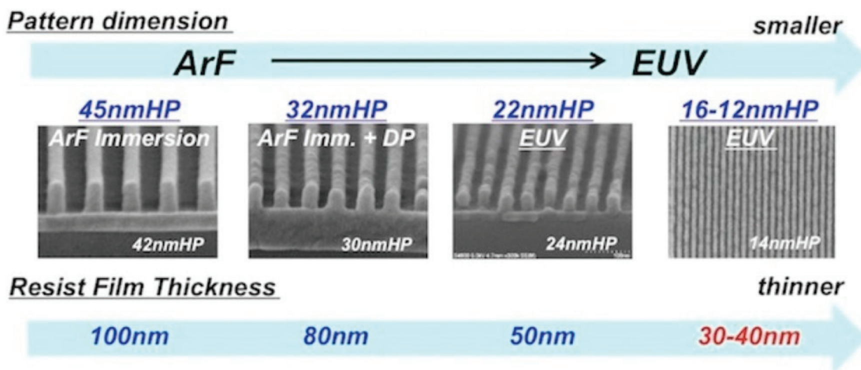


Figure 4. Evolution of the lithography technique where the pattern becomes denser and smaller in each new technology node. To prevent pattern collapse, the thickness of resist is reduced proportionally to the minimum half-pitch (HP) of lines/spaces.

4. Process Integration of New Transistor Architecture

4.1. Process Flow of 2D and 3D Transistors

The process flow of FinFETs consists of the SADP technique, followed by oxide filling, planarization using CMP (chemical mechanical polish), and etching to reach the fin active region and form shallow trench isolation (STI).Afterwards, the process flow is similar to the planar transistors e.g., well doping, dummy gate deposition and patterning, spacer formation, SiGe-epi, and S/D formation, interlayer dielectric zero (ILD0), chemical mechanical polish (CMP), dummy gate etch, high-*k* and metal-gate (HKMG) process, self-aligned contacts (SACs) for silicide and metal formation, local interconnects (LI), and back-end-of-line (BEOL) interconnect construction [34–36], as shown in Figure 5.

- Fin patterning vs. planar active region patterning
- Oxide filling, planarization, and recessing
- Doping to form well isolation
- Gate oxide growth, and dummy gate deposition, planarization and patterning
- Doping to form S/D extentions
- Spacer deposition and patterning
- Epitaxy forming S/D regions (embedded SiGe and raised Si)
- ILD0& CMP
- Dummy gate removal
- Replacement of high-k & metal gate stack
- Self-aligned contact formation
- Back end of line

Figure 5. Process flow for the bulk FinFETs or planar transistors. The FinFETs process are underlined [36].

On the path of CMOS miniaturization, the smaller contact size leads to higher contact resistance and contact-to-gate capacitance. Normally, the parasitic effects had no big impacts on the transistor performance because they were significantly smaller than the resistance and capacitance of the channel. However, both these effects becomes proportional to the gate length, which has been significantly reduced during past years. The parasitic effects became comparable or even larger than the intrinsic channel (gate and body) capacitance and resistance, as is shown in Figure 6.

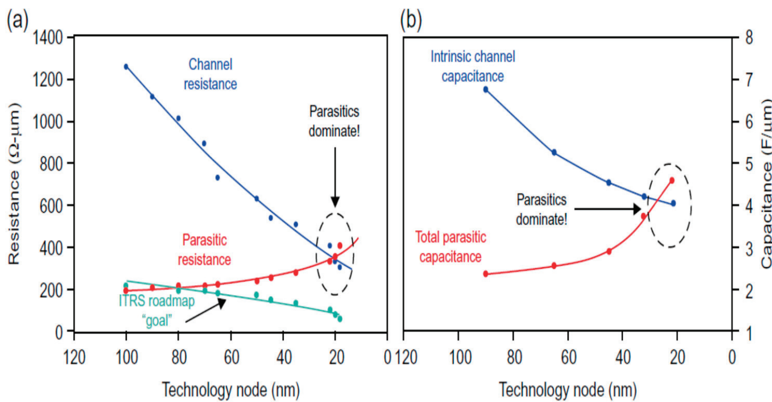


Figure 6. (**a**) Parasitic resistances and (**b**) capacitances in each technology node [22].

The contacted CD of FinFET or lateral GAA NW device is 18 nm for the 10-nm node and the contacted CDs are expected to be 16 nm, 14 nm, and 12 nm for 7 nm, 5 nm, and 3 nm in the future, respectively [37], as is shown in Figure 7. The contacted resistivity has reached sub 10^{-9} $\Omega{\cdot}cm^2$ for advanced CMOS FinFET beyond 7 nm, and the values need to be smaller in the future [38].

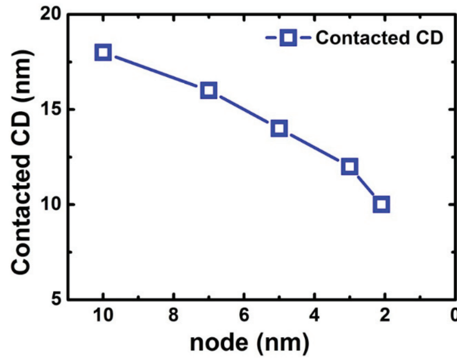


Figure 7. Values of contacted CD for advanced device.

4.2. Challenges in FinFETs' Process

Electrical characteristics of FinFETs are related to the fins' profile and dimensions [39]. In order to transport higher current, longer fins are required, which leads to several challenges to manufacture transistors, as shown in Figure 8.

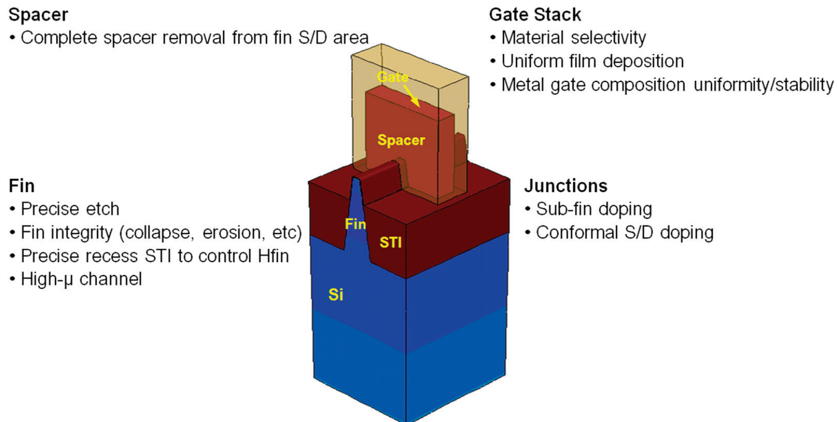


Figure 8. New challenges in the miniaturization of FinFETs [36].

The process of long Si fins creates difficulty for the integration of poly gate, spacer, and replacement metal gate. One of the problems' roots is not easy to etch the poly gate with a high aspect ratio [39]. Charging and micro-loading of etching results in variable L_g. An over-etch process is needed to clean the poly residual, and to remove the offset spacers on the fin-sidewalls [40,41]. Unfortunately, both these over-etchings result in damages of the Si fins. A remarkable Si loss may occur after wet cleaning and the solution has to be more diluted and should be used at low temperatures. Therefore, the dry and wet etching need more attention to be optimized to produce 3D gates with minimum L_g variation and Si loss in fins.

The patterning of fins is performed by SADP [42]. In this process, the depth of fin etching is usually determined by time. Meanwhile, the fins located at the edge of the wafer may show larger profile variation compared to those in the middle. To obtain uniform fin dimensions, dummy features could be used [43]. In this case, some dummy fins are necessary to be cut at the pitch. It is important to mention that, when the fin pitch shrinks and becomes compatible to the overlay limit, cutting fins becomes more difficult. Other steps of the FinFET's process, e.g., fin isolation by STI and channel-stopper doping

become more challenging, because the tighter pitch makes it more difficult to control the STI profile as well as doping variation.

In conclusion, in order to maintain the integrity of fins with a high aspect ratio is a challenging task [32]. The dry etching of fins is not a straight forward task because of the 3D topography. Thus, a plasma pulsing scheme is viable to decrease Si loss [39]. In a similar way, the oxidation of fins is a non-uniform process and it is faster at corner and tip areas.

One of the important issues in the FinFETs process is doping the fins [44,45]. A conformal doping profile in the S/D and extension regions has to be performed to create uniform carrier conduction in the fin-channel. The tight pitch of the fins restricts the incident beam angle in ion implantation (I/I), and may result in shadowing neighboring fins.

During the I/I, the Si fins become amorphous and, later, an annealing treatment is applied for re-crystallization. Unfortunately, this thermal treatment usually leads to poor dopant activation and formation of defects [44]. The poor fin quality has strong impact on the epitaxial quality of SiGe in S/D epitaxy as well as contact resistance in those regions. An increase of Si wafer temperature during I/I could be an appropriate solution to decrease the amorphous depth and fin damage [44,45]. Several reports have presented different innovative doping methods. Solid-source doping, molecular monolayer doping, and conformal plasma doping can improve the doping profile.

5. SiGe Epitaxy of Nano-Scaled Transistors

SiGe was integrated in S/D regions as stressor material for the first time in the 90-nm technology node to induce uniaxial strain in the channel region. Selective epitaxy growth (SEG) of SiGe was applied to fill out the recessed S/D regions. The advantage of uniaxial strain to the biaxial one is higher carrier mobility even for high electric fields. The embedded SiGe in S/D regions has been continuously increased from 19% to 45% when the transistors were miniaturized from 90-nm to 22-nm nodes [46–50]. In a 45-nm node, the shape of recess in S/D regions was modified from a round shape to sigma shape in order to further increase the SiGe strain since the layers could be located closer to the channel [51–53].

Beyond the 22-nm node (3D transistors), the SiGe layers are being grown on the Si fin to raise the S/D regions. The summary of Ge contents in S/D regions for different technology nodes is shown in Figure 9.

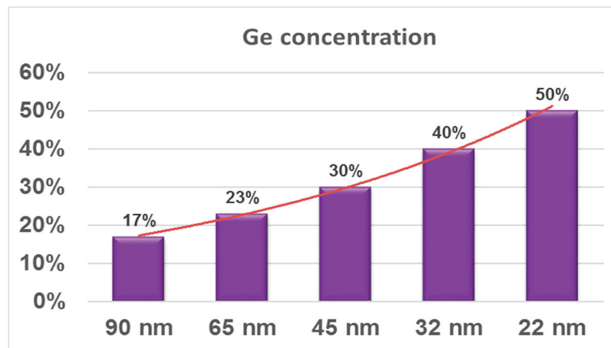


Figure 9. Ge contents in S/D for different technology nodes.

The SEG of SiGe on Si-Fin and nanowires has its own complexity and challenges. The SiGe growth may suffer from a series of problems: facet formation [54,55], defects, micro-loading, non-uniform strain distribution, surface roughness, and the pattern dependency effect [56–60]. Among those problems, the pattern dependency effect occurs when the density and size of the transistor vary in a chip. The reason for the pattern dependency of SEG is mainly non-uniform consumption of reactant gas molecules when the exposed Si area varies in a chip. Hence, more careful optimization of the growth parameters

as well as redesigning chip layout for uniform exposed Si areas could create uniform gas consumption during epitaxy for a successful process [56–60].

Currently, there is a strong attitude to replace the Si channel with SiGe or Ge in FinFETs with a high aspect ratio. The idea behind is to terminate the formed defects close to the fins' sidewall during epitaxial growth. This method is also called high aspect ratio trapping (ART) and by using it, high-quality film in the vertical direction is obtained.

There are two methods to remove the Si and form the trench including the wet etch using Tetramethylammonium hydroxide (TMAH) and the vapor etch using HCl inside the CVD (chemical vapor deposition) chamber. The biggest difference between these two methods is the control of the silicon morphology at the bottom of the trench. A "V-shape" (111)-oriented of Si crystal is formed in the TMAH etch. Meanwhile, the HCl vapor method offers (311)-oriented facets of Si at the bottom of the trench, as shown in Figure 10a–c.

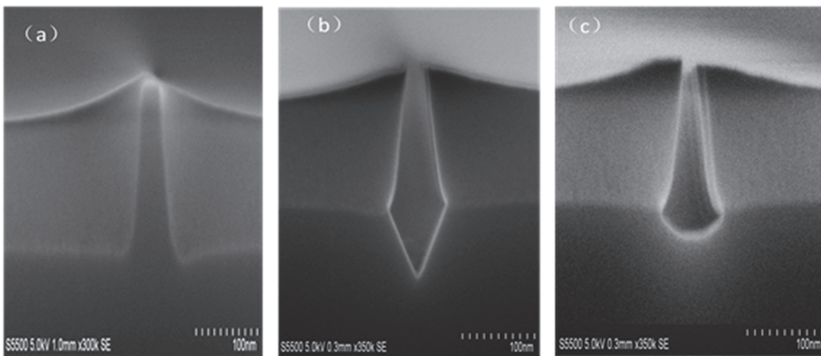


Figure 10. (**a**) Si fin covered with SiO_2 (**b**) removal of Si in the fin after wet-etch by TMAH and (**c**) HCl vapor etch [61].

After filling the fins, the Chemical Mechanical Polish (CMP) technique is used to planarize the lateral overgrown part. Later, the STI oxide is removed by diluted HF solution to expose the Ge or SiGe fin. Figure 11 is the process scheme of SiGe or Ge SEG in the channel region in a FinFET structure. The process initiates to form a "V-shaped" Si recess and growth of the strain relaxed buffer (SRB) of $Si_{0.3}Ge_{0.7}$ [62].

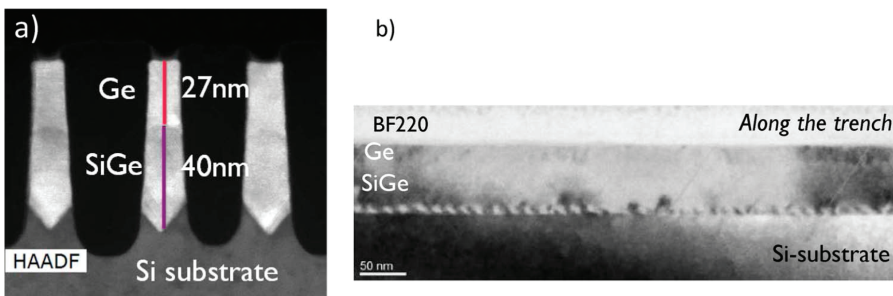


Figure 11. Cross-section TEM of strained Ge-cap/ SRB $Si_{0.3}Ge_{0.7}$ grown in an oxide trench and observed at (**a**) fin cut and (**b**) along the trench. The Si was removed by the wet etch prior to epitaxy [62].

For a better control over a short channel effect, a more aggressive design e.g., the Gate-All-Around (GAA) structure is proposed to be integrated in the near future. For such transistors, SiGe or Ge are proposed to be grown as channel material for high mobility.

For the sub 10-nm technology node and beyond, the nano-wire device might be one of the promising candidates to obtain better gate control and lower leakage current [63–66]. In this approach, SiGe/Si multi-layers are grown where either SiGe or Si can be etched selectively to form channel regions for NWs. Figure 12 illustrates an image of a multilayer SiGe/Si structure with eight periods for forming vertical NWs.

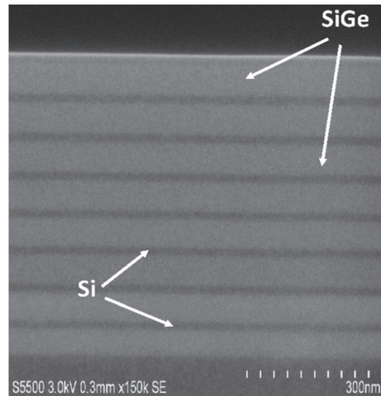


Figure 12. HRSEM of a multilayer of the SiGe/Si structure with eight periods [66].

6. Monolayer Doping

Monolayer doping (MLD) is a self-assembly doping process, which can be applied for doping NWs. This doping method is dominated by a surface chemical reaction between the semiconductor substrate and dopant-containing organic molecules [67–71]. Compared to conventional implantation, MLD introduces fewer defects into the substrates [72–75] and the dopant-containing molecules could attach uniformly on the surface, which results in a better conformal doping profile [73].

The basic procedure of MLD for nano-sheets is shown in Figure 13 [70]. However, the process could be easily used for NWs. The solution aqueous HF or NH_4F was first used to remove the native oxide on the surface and to obtain a hydrogen-terminated surface. Later, the substrate will be immersed into dopants containing liquids or solution of organic materials [70–75]. The organic material could be dopant atoms contained in alkene or alkyne. After that, a low temperature treatment or light irradiation will be adopted to enable a reaction, which is called hydrosilylation to form a covalent bond between the dopant containing molecules and Si atoms of the substrate's surface [70]. A conformal doped junction is formed by capping a thin SiO_2 layer and high temperature RTP (rapid thermal processing) annealing to drive the dopant into the substrate.

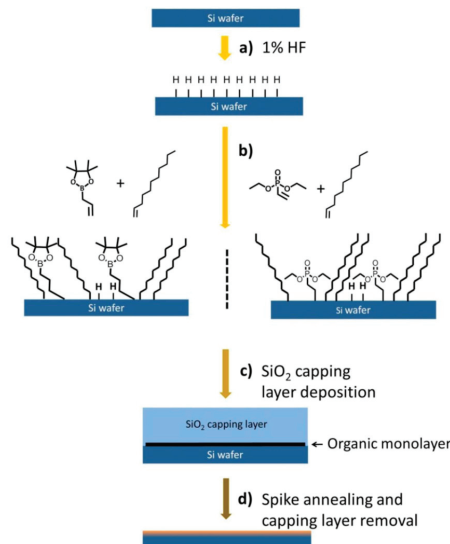


Figure 13. Schematic of the monolayer doping process [70].

The tuning of doping concentration in the MLD process could be realized by either changing the amount of the dopant atom in a molecule (dopant enriched adsorbate) to improve the packing density or by mixing the dopant adsorbate with molecules that lack dopants to reduce the dopant quantity at the interface. The final junction doping level is always determined by dopant solid solubility of the dopant element [71,74].

7. Plasma Doping

Plasma doping is a method based on when the dopants are adsorbed conformally on the surface of Si during the wafer, which is immersed into the plasma and dopant radicals in plasma. The uniform doping profile can be obtained by plasma doping and the damage to the surface can be suppressed by controlling the plasma energy. Recently, this technology has been improved by introducing ion energy decoupled plasma doping. This is based on a pretreatment to corporate decoupled plasma doping. In this way, the dopant level was remarkably raised and the surface damage could be decreased by heating the wafer during the process [68,75,76].

8. High-*k* & Metal Gate (HKMG)

In downscaling of MOSFET, SiO_2 high-*k* material was eventually replaced with high-*k* material and the gate formation in the process flow was moved to the last in order to save the high-*k* integrity.

Table 1 summarizes the thickness of the materials in the gate stack (high-*k* dielectric and SiO_x) from a 45-nm to a 5-nm technology node [77–80]. The thickness of SiO_x decreased dramatically from ~1.2 nm in a 45-nm node to ~0.6 nm in a 14-nm node. In a similar way, high-*k* dielectric (HfO_2) decreased from ~1.5 nm in a 45-nm node to ~1.2 nm in a 14-nm node. As a result, the equivalent oxide thickness of gate dielectric was decreased. In the 14-nm node CMOS, the thickness of SiO_x and HfO_2 have significantly decreased to ~0.6 and ~1.2 nm, compared to ~1.1 and ~1.0 nm for transistors in a 22-nm node. The 0.6 nm of SiO_x contains only four or five layers of atoms, which is very thin. In addition, for reliability of the gate stack, the thickness of SiO_x is an important issue and, consequently, cannot be further decreased. Therefore, it is expected that the thicknesses of SiO_x and HfO_2 would be considered ~0.5 nm and ~1.0 nm beyond a 5-nm node.

Therefore, for high-*k* dielectric gate stack beyond the 5nm CMOS, almost the same gate stack (HfO_2 and SiO_x) will be built and the thickness of these two materials will be nearly unchanged compared with the 14-nm technology node. This is due to the direct tunneling current, which increases exponentially with thinner film thickness.

Table 1. Material selection of high-*k* dielectric and metal gate from 45-nm to 5-nm nodes.

Technology Nodes	Film Thickness (nm)			
	Thermal Oxide	High-*k*	TiAl(N)	TiN
45 nm	~1.2	~1.5	~2	~2.1
32 nm	~1.2	~1.1	~1.7	~2
22 nm	~1.1	~1.0	~1.2	~1.4
14 nm	~0.6	~1.2	~1.2	~1.4
5 nm	~0.5	~1.0	~1.0	~1.2

For the metal-gate, the N metal for NMOSFET (N-type metal-oxide-semiconductor field effect transistor) is still TiAl-based material, and the P metal for PMOSFET (P-type metal-oxide-semiconductor field effect transistor) is TiN. The work function metals for the NMOS (N-type metal-oxide-semiconductor) and PMOS (P-type metal-oxide-semiconductor) in 45 nm and 32 nm node were TiAlN and TiN, respectively [4,81]. Through the tremendous downscaling of CMOS starting from FinFET in a 22-nm node to the GAA (nanowire) structure, the electrostatic gate control is improved. This decreases the requirement of the metal-gate work function [41].

For the GAA structure, the gate-fill is a challenging task, and this increases the requirement of further decreasing the metal-gate thicknesses. Beyond the 5-nm technology node, the thicknesses of the TiAl and TiN metals are expected to be ~1.0 nm and ~1.2 nm, respectively.

For transistors beyond the 5-nm node, the device performance cannot be further improved by optimizing gate stacks. The high-*k* dielectric and metal-gate are simply very thin and cannot be further decreased. For the GAA device structure, the deposition of HKMG requires precision in atomic levels. The ALD technique offers a good control for layer thickness of HfO_2 and TiN. However, for NMOSFET, it is relatively difficult to acquire the N-type work function metal due to the precursor limitation. In this field, TaC_y [82], TaCN [83], TiC [84], $WC_{0.4}$ [85], and ErC_2 [86] were studied for NMOSFET application. However, in most of these processes, plasma enhanced ALD (or PEALD) was used. To some extent, thermal ALD without plasma damage is more suitable for the metal gate. TiAlX films as the metal gate were developed by Chao et al. by the thermal ALD technique using $TiCl_4$, TMA ($Al(CH_3)_3$), and NH_3. It was demonstrated that NH_3 presence in the $TiCl_4$ and TMA reaction makes the film more like TiAlN(C) while its absence makes the film turn to TiAlC. The TiAlC film has a smaller effective work function than the TiAlN(C) film [87]. The effective work function can be tailored from 4.49 eV to 4.79 eV by tuning the process conditions [88]. By introducing the triethylaluminum (TEA) into the process, more Al-doping is obtained in the TiAlC film due the reaction of TEA with $TiCl_4$. The effective work function of the TiAlC with TEA as a precursor can be tunable from 4.46 eV to 4.24 eV [89]. The deposition of TaAlC films using TMA and TEA has almost the same effective work function as TiAlC films grown by TMA and TEA separately, which provide more choices for metal gate selection [90,91]. The effective work function of different metals for NMOSFET are summarized in Table 2 [82–91].

High-*k* material can be applied for a more complicated transistor design, e.g., negative capacitance FET (NCFET). This type of transistor is a strong potential device beyond the 5-nm node CMOS. The reason for choosing NCFET is due to its dramatic improvement in a sub-threshold swing, which has compatible process flow with the conventional CMOS technology, and on-current enhancement [92]. The high-*k* materials suitable for NCFET are considered to be HfZrO and HfO_2 with a thickness below 5 nm.

Table 2. The effective work function of different metals grown by ALD for NMOSFET.

Metal	Dep. Method	Effective Work Function	Ref.
TaC_y	PEALD	4.77–4.54 eV	[84]
TaCN	PEALD	4.37 eV	[85]
TiC	PEALD	5.24 eV–4.45 eV	[86]
$WC_{0.4}$	PEALD	4.2+/-0.1 eV	[87]
ErC_2	ALD	3.9 eV	[88]
TiAlC	thermal ALD	4.79–4.49	[90]
TiAlC	thermal ALD	4.46–4.24	[91]
TaAlC	thermal ALD	4.74–4.49	[92]
TaAlC	thermal ALD	4.65–4.26	[93]

9. Interconnections in CMOS

Tungsten (W) has excellent thermal stability, the highest melting point among all metals, and perfect resistance to electro-migration (EM). The tungsten plug has been used for metal interconnection in integrated circuits to connect different layers of metals to nano transistors. ALD has been widely used for deposition of tungsten. ALD W has been used as gate filling metal (HKMG-last) due to its properties for trench filling [93]. ALD W can be selectively deposited and this is important for advanced sub-10 nanometer transistors, which needs good alignment to underlying structures, and edge definition [94]. W films have an α-phase and a β-phase with different morphologies and electrical properties. W films with an α-phase have the lowest resistivity and an important role in the logic MOSFETs.

The common precursors used for ALD W are SiH_4 [95–108], Si_2H_6 [99], and B_2H_6 [100–103]. Different precursors will form films with different phases. Qiang Xu et al. studied the adhesion, roughness, and pore filling ability of ALD W films using different growth methods and different precursors for the 22-nm technology node, as shown in Figure 14 [104]. The authors demonstrated that the roughness of the W film grown by the ALD technique is clearly better than that of CVD. The roughness of ALD films grown by SiH_4 is better than that of the B_2H_6 precursors. However, the filling performance of SiH_4 is worse than that of B_2H_6.

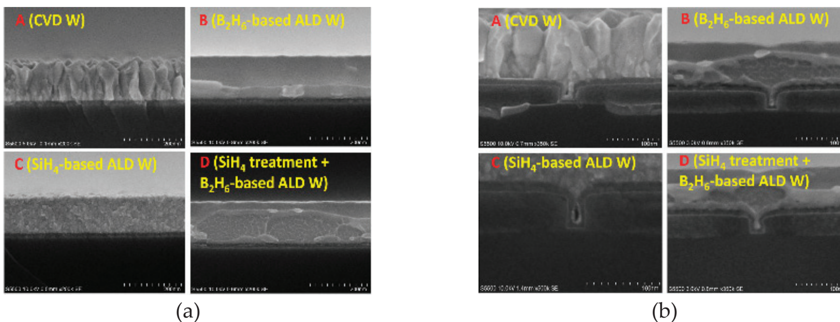


Figure 14. Cross-sectional SEM images of W films grown in different conditions: (**a**) on blank wafers and (**b**) trenches filling capacity [104].

In order to further understand the internal morphology of the ALD W film, Wang et al. measured the morphology of these films by using the XRD technique. It was found that there were two kinds of crystalline phases in the ALD W films grown by SiH_4 as precursors, while the films grown with B_2H_6 were amorphous, as shown in Figure 15 [98].

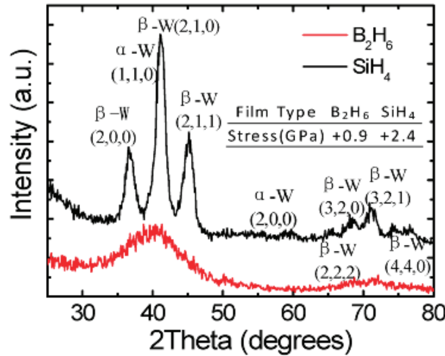


Figure 15. XRD spectra of ALD W using SiH_4 and B_2H_6 and calculated stress data on a blank substrate [98].

In integrated circuits, ALD W with the α-phase is commonly used for metal interconnection or electrode filling. One way to grow tungsten films with α-phase on SiO_2 is to use WF_6 as a precursor and H using hot-wire (HW) assisted atomic layer deposition (HWALD) [105]. Kim et al. demonstrated that tungsten films using B_2H_6 and WF_6 precursors create large grain size α-phase tungsten at 450 °C. Meanwhile, at 395 °C and applying a low flow rate of B_2H_6, smaller grains could be obtained [106].

The initial nucleation process in the growth of ALD has a great influence on the state of the subsequent films. The main factor affecting the nucleation of ALD is the surface active site density. For example, in the study of selective ALD deposition, it was found that hydroxyl bonds were formed on the surface of SiO_2 after wet cleaning, which resulted in the nucleation of SiH_4 and WF_6 on the surface of SiO_2 [94]. However, the nucleation is greatly delayed after the removal of surface hydroxyl groups by heating or using a precursor, which interact with the surface to change the surface characteristics. For example, when B_2H_6 and WF_6 are used as precursors, pretreatment with B_2H_6 accelerates nucleation. At the same time, the resistivity of the film is reduced.

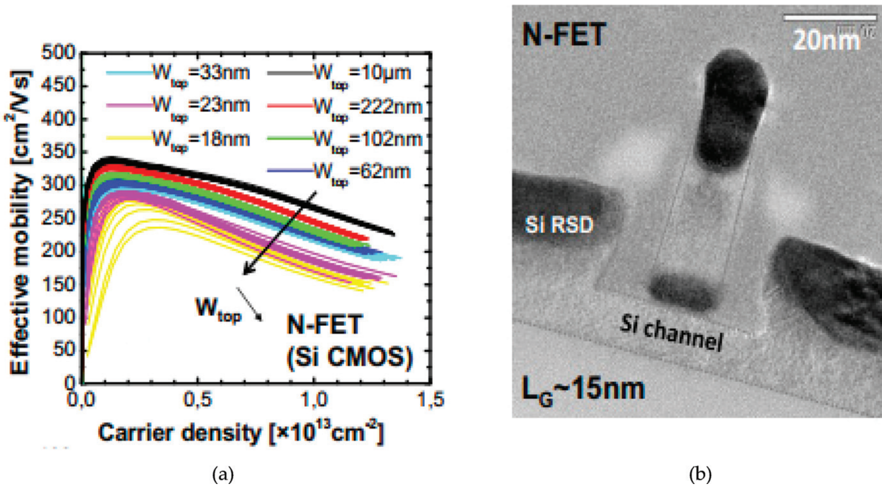
F.H. Fabreguette presented the Quartz crystal microbalance study of the tungsten atomic layer deposition using WF_6 and Si_2H_6. This work found that the growth rate of ALD W was weakly temperature-dependent with an activation energy of 1.5 ±0.1 kcal/mol at T < 250 °C and a lower activation energy of 0.6 ± 0.3 kcal/mol at T > 275 °C [99].

At present, there are few research studies on the theory and interfacial states of ALD W. It is a valuable research direction to study the selective deposition on the basis of interfacial states and the formation mechanism for different crystal phases of W in the future. In the aspect of the device application, the process of preventing the diffusion of the F atom and the B atom through the TiN/Ti layer is also a valuable research direction in the integrated circuit.

10. Stressors SiN_x Contact Etch Stop Layer (CESL) Technology

After integration of the SiGe stressor material in MOSFETs, a large effort was spent to find new methods to increase the strain amount. Among the various methods, stress liner technology, which is based on the SiN_x contact etch stop layer (CESL) received more attention. The strain in these films could be tuned from highly tensile to highly compressive. The stressed nitride contact liners were incorporated into a high performance CMOS flow. This CESL approach resulted in N-FET/P-FET effective drive current enhancement of 15%/32% and saturated drive current enhancement of 11%/20%. In these transistors, a significant enhancement of 60% was achieved in whole mobility without using SiGe [107].

Another example is shown in Figure 16a,b where the CESL was used in Ω-gate CMOS NWs with N-FET. The carrier mobility of transistors lied in a range of 250 to 350 cm^2/Vs for different gate widths [108].



(a) (b)

Figure 16. (**a**) Electron effective mobility in NFET and (**b**) TEM images Ω-Gate CMOS NW transistors for N-FET [108].

10.1. High Tensile Stress CESL

Many growth techniques have been applied to deposit high tensile SiN_x, e.g., LPCVD (low pressure chemical vapor deposition), ALD, and PECVD (plasma enhanced chemical vapor deposition). It is known that Si_3N_4 films produced by the LPCVD technique possess high tensile stress of 2 Gpa. However, the relatively high thermal process makes the process not compatible with Ni silicide [109]. Therefore, PECVD technology with a low thermal budget process was taken as the best choice to deposit CESL [110].

Unfortunately, the hydrogen in PECVD nitride film could not have been pushed out, which pulled down the film tensile stress to about 1 Gpa [111]. There are various reports that demonstrate methods. Plasma treatment and the ultraviolet thermal process (UVTP) can enhance the tensile stress. The latter method breaks Si-H and N-H bonds and pushes out H molecules. This method meets the demand of both high tensile stress, a low thermal budget, and stress amount as high as 1.7 Gpa can be obtained (see Figure 17).

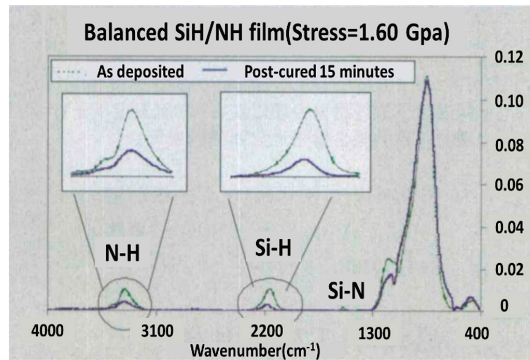


Figure 17. Tensile stress change with a UV cure.

10.2. High Compressive Stress CESL

In order to make high compressive stress CESL, both the RF power source and diluted gas have to be tuned. It is known that the compressive stress has a strong relationship with which a type of diluted gas is used. For example, the compressive value is as low as ~1.2 Gpa when nitrogen is used as diluted gas whereas a mixture of argon and nitrogen could highly increase the compressive stress to ~2.3 Gpa [112]. The compressive strain could be further increased to ~3.1 Gpa by using a diluted gas of hydrogen and argon mixture. The hydrogen reduces the energy loss during bombardment. To obtain further improvement, it is necessary to improve the film's elasticity modulus by applying the carbon element, which could impel hydrogen volatilize (less hydrogen and higher compressive stress). In this case, the SiH_4 precursor has to be replaced with TMS (tetramethylsilane), which contain a carbon element and compressive stress could reach close to 3.5 Gpa.

11. Etching Evolution

Miniaturizing the transistor according to the principles shown in Figure 2 occurred when equivalent oxide thickness (EOT), transistor gate length, and transistor width were scaled down by a constant factor. However, this trend is followed very differently when the CMOS scaling focuses more on low voltages and low power consumption. By entering the 10-nm technology node, the silicon channel is being gradually replaced with silicon-germanium (SiGe), germanium (Ge), or III-V materials because they have remarkably higher carrier mobility [113]. For example, 40,000 $cm^2{\cdot}V^{-1}{\cdot}s^{-1}$ for InGaAs [114] (for electrons) and 1900 $cm^2{\cdot}V^{-1}{\cdot}s^{-1}$ for Ge [115] (for holes) compared to 1400 $cm^2{\cdot}V^{-1}{\cdot}s^{-1}$ for electrons and 450 $cm^2{\cdot}V^{-1}{\cdot}s^{-1}$ for holes in silicon [116]. Not only is the channel material changed, but the transistor shape is changed from a simple fin-like shape to a lateral gate all around (LGAA) or vertical gate all around (VGAA) in order to obtain transport control through the channel region. It means that the fabrication of state-of-art transistors need to be modified.

In this case, a dummy gate poly crystalline was initially formed as a replacement metal gate (RMG) as well as silicon dioxide, which was deposited as dummy gate oxide to give the green light for all the high temperature-annealing processes [117]. Eventually, the gate was removed by a wet process using none metal alkaline solutions. The merits of RMG are first addressed to avoid crystallizations of the high-*k* dielectric during the rapid thermal annealing (RTA) process for dopants activation, which may increase leakage current of the gates [117]. Second, it avoids the chemical reactions between the metal-gate and the high-*k* in RTA processes [118] or it avoids the boron diffusion into high-*k* [118,119].

The RMG process is still used and will be applied for the 7 nm and 5 nm technology node, where the sacrificial material is Si and will be selectively removed from the SiGe channel [120]. The exponential decrease in the alkaline etch rate of SiGe with increasing Ge content enables the selective removal of Si to $Si_{0.75}Ge_{0.25}$. [121–124]. Alkaline etching of Si has been extensively studied and is well understood [125,126]. The etch rate in Si (001) and (110) directions is remarkably faster compared to the Si (111) crystallographic planes [127]. As shown in Figure 18, the selective etching of Si to SiGe was performed at a TMAH 5% solution at 60 °C. In both pictures, the Si underneath material of the NW stack is completely removed. The 7-nm thick Si layers, which are sandwiched in between the $Si_{0.75}Ge_{0.25}$NWs are removed until the (111) limiting planes are formed.

In fabricating the SiGe NWs from the Si/SiGe stack, the conventional alkaline Si etchant such as TMAH (aq) poorly removes the Si sacrificial layer. The selectivity of the Si-vs-SiGe etch is only marginal [128,129]. A surface modifier is employed in ACT® SG-201, which improves the relative etch rates of Si (110) and Si (111) orientations. This solution results in etching selectivity of Si (110)/Si (100) in the range of 1 to 2.5 and Si (111)/Si (100) of about 0.5 or above. By a combination of the Si surface modifier and an effective SiGe corrosion inhibitor in ACT® SG-201, the selectivity of Si (111)/SiGe 25% is significantly improved as compared to the conventional Si etchants. Consequently, ACT® SG-201 is more efficient in removing the sacrificial Si layer in the Si/SiGe stack [130]. The reduced Si etch rate anisotropy in combination with an effective SiGe corrosion inhibitor prevents SiGe loss during the NW release [130].

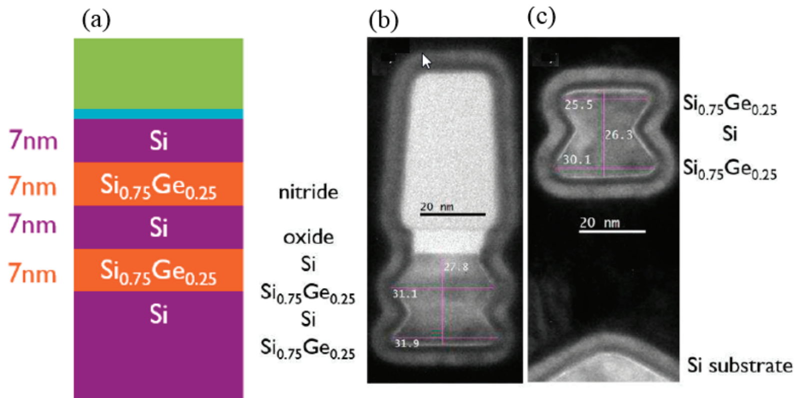


Figure 18. (**a**) Schematic picture of a stack of $Si_{0.75}Ge_{0.25}$/Si NW used for selective etch and TEM across a section of 30-nm wide Si-$Si_{0.75}Ge_{0.25}$ NWs after Si selectively etched (**b**) in TMAH 5% and (**c**) without the oxide-nitride HM [127].

The sacrificial material is SiGe and will be selectively removed from the Ge channel [131–133]. For example, SiGe can be selectively etched to Ge in diluted TMAH 5–25% at 90 °C. Figure 19 shows the $Si_{0.5}Ge_{0.5}$/Ge NWs after selective etching in TMAH 15 or 25%. The Ge NW is not etched in the solution while the $Si_{0.5}Ge_{0.5}$ and substrate are etched anisotropically. The undercut for the 25% TMAH solution is more than for the 15% solution one. The etch rate of the (001), (110), and (111) crystallographic planes of $Si_{0.5}Ge_{0.5}$ were estimated from these cross-sectional scanning electron microscopy (XSEM) images (see Figure 19b,c). The etch rate of the different planes is decreasing in magnitude from (001) to (111) to (110) plane. If the selective removal of Ge is the goal, then oxidizing solutions, e.g., using SC1 solutions can be used due to the high solubility of the Ge-oxide [122,134].

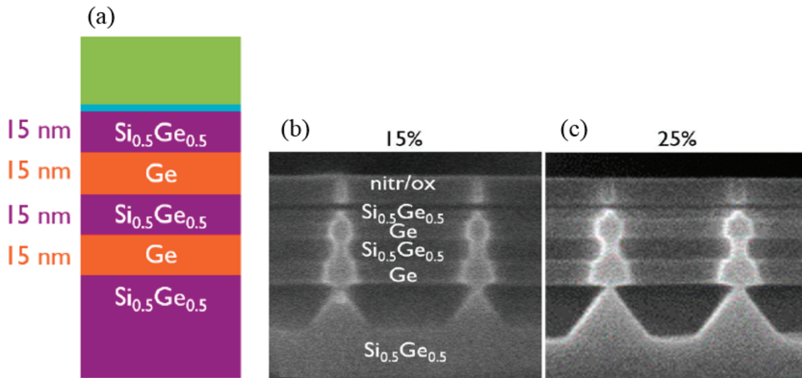


Figure 19. (**a**) Pictorial description of the $Si_{0.5}Ge_{0.5}$/Ge NW stacks used for the selective etch test and SEM images of $Si_{0.5}Ge_{0.5}$-Ge NWs after selective etch for 10 seconds in TMAH with a concentration of (**b**) 15% and (**c**) 25% for 45 and 55 nm wide fins [127].

In fabricating the Ge NW from the SiGe/ Ge stack, two different (i.e., alkaline vs acidic) chemical solutions have been investigated. The alkaline solution (5% TMAH) shows anisotropic SiGe etch behavior as well as a decrease of etch rate when the Ge content is higher than 50%. To overcome the anisotropic etch problem in the alkaline solution, isotropic SiGe etch behavior and better Ge protection are required. Different from the Ge etchant with mixtures of HF-H_2O_2-H_2O [135], the formulated solution ACT® SG-301 employs a selective oxidizer [130], a SiGe etchant, an effective

Ge corrosion inhibitor, and a well-designed solvent system for polarity adjustment. By suitable pH control, the oxidized SiGe sacrificial layer could be effectively removed and the Ge NW damage could be minimized [130].

12. BEOL for Nano-Scale Transistors

Interconnects are a fundamental element of any microelectronic circuit. As semiconductor technology keeps evolving along the trajectory predicted by the Moore's Law, the CD of the BEOL circuits must continue shrinking. However, the scaling of the interconnect dimensions will be led to the deterioration of the interconnect performance and reliability [136]. Twenty years ago, dual damascene copper replaced the subtractive etch of aluminum and the method for BEOL interconnect fabrication [137]. Copper is expected to be used in scaled transistors in the future. However, as the CD narrows, filling the BEOL trench over the structure using the conventional physical vapor deposition-Electro chemical deposition (PVD-ECD) approach becomes more and more challenging. In the 5-nm technology node, interconnect half pitches are expected to reach dimensions of 12 nm [138,139]. For such narrow lines, the intrinsic properties of Cu start to severely limit the interconnect performance. At first, Cu resistivity is increased because of electron scattering at the sidewall and grain boundaries [140–142], which results in an exponential increase in resistivity and resistance. Secondly, there are limitations in scaling the diffusion barrier for the currently used Cu dual-damascene process, which increasingly reduces the Cu volume in interconnect lines [143,144]. Thirdly, barriers and liners do not scale well since strongly reduced thicknesses negatively affect the dielectric breakdown as well as the electromigration (EM) properties [144]. Hence, these issues eventually stop scalable solutions for interconnects.

Materials innovation and integration improvement are the requirements for diffusion barriers in combination with low-*k* dielectrics, the resistance to EM, and lower resistance than the combination of Cu and barrier layers in small dimensions. According to these requirements, there are two methods to improve them. One is to partially modify traditional Cu integration process and the other is to use new materials to replace the Cu integration process.

As the critical dimension continues to shrink to a 5-nm node, the bilayer approach (PVD TaN/Ta) faces scaling challenges, e.g., thickness control and PVD TaN over-hang. Wu et al. reported a novel approach to use thin ($\leq$ 15 Å) ALD-based TaN barriers [145] and Co liner instead of copper electroplating. The use of a post-ALD treatment in a PVD chamber resulted in ALD films with resistivity, density, and a Ta/N ratio similar to industry-standard PVD TaN. This approach enables the conformal Cu barrier without reliability degradation compared to PVD TaN [145]. This new method overcomes the shadowing effect of the traditional PVD approach and improves the metal-fill process window. Furthermore, this method promotes lower via-resistance through barrier thickness reduction, which proves it to be a viable Cu-barrier candidate for the 5-nm node and beyond. However, this approach would only be a short-term alternative due to a size effect of Cu resistivity and TaN high resistance [146].

Van der Veen et al. [147] and Zhang et al. [148] introduced Co via-prefill concept to achieve void-free and bottom-up fill of metal in advanced interconnects, as shown in Figure 20. The via-prefill is beneficial for the Cu damascene process. The direct contact of Co and Cu at the bottom without TaN/Ta barrier interface results in a reduction of via-resistance. Moreover, Co is expected to have a better EM performance compared to Cu due to its higher melting point [143,146,149,150].

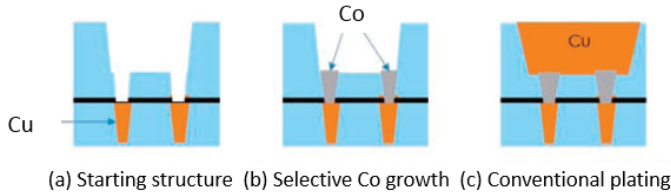


Figure 20. Integration of Co selective growth [148].

Zhang et al. reported, for the first time, a highly selective CVD Co deposition on Cu to fill a 45 nm diameter with 3:1 aspect ratio in a Cu dual damascene structure [148]. The results showed void-free Co-fill of the vias. interuniversity microelectronics centre (IMEC) demonstrated the feasibility of the prefill concept using the electroless deposition (ELD) technique for Co as material to pre-fill vias [147,151,152]. The main benefit of having Co vias is the reduction of the via-resistance. As the via CD shrinks, vias with ELD-Co show larger resistance reduction compared to the conventional PVD-EC Dones. As an example, at 40 nm via critical dimension (CD), the via-resistance reduction is ~30% [151]. For 12 nm chamfered vias with 3 nm metal barrier and Co via prefill, 45% resistance reduction can be achieved [152]. Therefore, the selective Co process for contact and via prefill has the potential to enable future scaling of the advanced technology node.

Marleen et al. benchmarked Ru, Co, and Cu in a damascene vehicle with scaled dimensions down to 11 nm CD and for different aspect ratios [142]. The Ru and Co NWs have higher resistivity, but Ru and Co are both superior to Cu for trenches smaller than 250 nm^2. The difference in resistance for the Ru, Co, and Cu is clearly increased with the decrease of the total wire area, as illustrated in Figure 21 [142]. The slope for Cu increases and it crosses over to Co and Ru at 400 nm^2. Ru effective resistance potentially crosses the Cu curve at 14 nm by assuming that the Cu barrier/liner thickness was 2 nm. The cross-point would happen at 8 nm with 1 nm Cu barrier/liner thickness [141]. Moreover, the EM performance reveals that the barrier-less Ru systems are robust with higher lifetime compared to Cu and Co [142]. These properties make Ru an attractive interconnect candidate for small line widths.

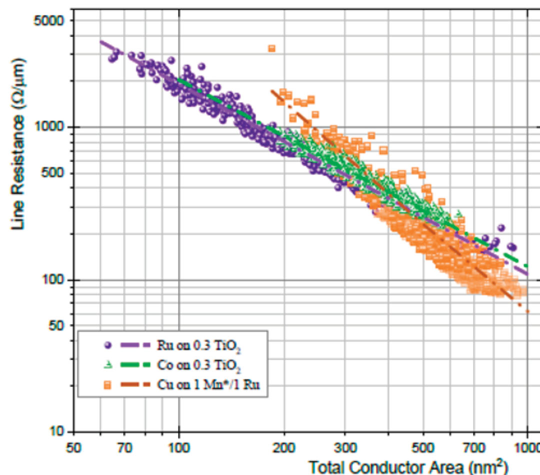


Figure 21. Damascence line resistance vs. the total conductor area of Ru, Co, and Cu NWs [142].

ALD Ru was studied as an option for barrier-less metallization for the future interconnects [141]. Ru shows regular nucleation on SiO_2 without any growth inhibition. The adhesion was significantly increased to 7.0 ± 2.3 J/m^2 by applying an ALD TiN adhesion promoting layer with a thickness as low

as 0.25 nm. The Ru lines with widths of about 10 nm, which show excellent EM behavior on a single damascene test vehicle. Time-dependent dielectric breakdown measurements revealed negligible Ru ion drift into dense low-k dielectrics with k ~3.0 up to 200 °C, which demonstrates that Ru has the potential to be used as a barrierless metallization as a future advanced interconnect solution.

Currently, the damascene implementation of Ru lines is hampered by the availability of optimized CMP. A semi-damascene integration approach is a proposed solution for the multi-level Ru interconnect [153]. This method is formed in low-k and then followed by filling both the via and the trench layers with a single deposition step. Key advantages are that the process can be barrier-less, the grain size can be tuned, and there is no requirement for metal CMP. The trench layer is then patterned using subtractive etch, which eliminates the need for plasma processing of low-*k* trenches. Ru films were patterned using EUV single exposure and subtractive etch to generate lines with CD down to 10.5 nm. This approach has excellent process control, stability, and results in a very high line yield. These results indicate that the subtractive etch of Ru could be a viable interconnect candidate for advanced technology nodes.

Plasma enhanced chemical vapor deposition Co was evaluated to fill dual damascene (DD) structures as an interconnect wiring metal alternative to Cu [139]. The void-free gap fill of damascene structures down to 10 nm CD was demonstrated using just 1 nm ALD TiN liner. A CMP process without Co residues or corrosion has been developed. 22 nm half-pitch Co lines with 1 nm ALD TiN liner in porous ultra low-*k* (ULk) meet the 10-year lifetime time-dependent dielectric breakdown (TDDB) reliability requirement in Figure 22 [139]. EM data indicates that the Co EM performance with 1 nm ALD TiN liner can be better than that of Cu in Figure 23 [139].

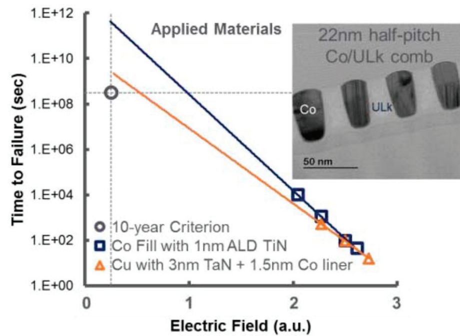


Figure 22. 22-nm half-pitch Co lines/ALD TiN liner compared to Cu [139].

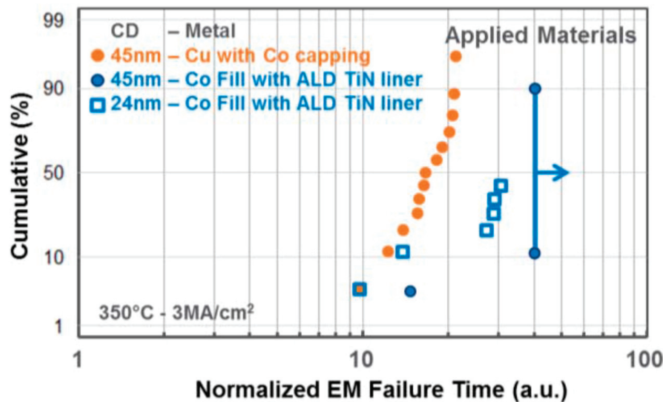


Figure 23. Performance of Co and Cu EM with 1-nm ALD TiN liner [139].

In response to the scaling challenges, Intel introduces a new metallization solution to meet the reliability challenges of technology scaling [154]. At trench contact, electroplating of Co occurs on a chemical vapor deposition (CVD) TiN barrier/adhesion and CVD Co seed layer. EM time to failure is observed to be at least four orders of magnitude higher for Co fill interconnects compared to the Cu alloy (see Figure 24). Moreover, superior intrinsic TDDB and stress induced voiding reliability was also demonstrated for Co low-*k* interconnects. Co shows superior intrinsic properties with respect to Cu.

Chemical vapor deposited tungsten (CVD W) based middle-of-the-line (MOL) contacts and local interconnects have been extensively used in high-performance CMOS logic IC's. The standard process scheme has included a TiN adhesion layer to dielectrics and a nucleation W layer for CVD W, but these layers consume most of the volume in narrow features. A major challenge for W fill scaling is that the line resistance of sheet Rs and plug resistance of contact Rc increase due to a reduction in the volume of the low resistance CVD W bulk material. Recent simulation results of the local interconnect resistance indicated that the M0 and the contact would become dominant contributors to a resistance increase at the 5-nm process node [155]. W M0 and Contact comprise 65% of the total M0/M1 stack resistance due to a narrow CD. Contact shows 43% reduction in M0/M1 resistance.

CVD Cobalt (Co) has been used in recent studies as replacement for W in local interconnect showing a 2.5× line resistance reduction, void-free and seamless fill at the local interconnect level [156]. Unlike W, Co metal does not need high resistivity nucleation layers and can be annealed at low temperature to undergo grain growth and reflow into the high aspect ratio contact plug. Moreover, CVD Co precursors do not attack Ti liner, which enables barrier thickness scaling. The resistivity of Ru [157] is comparable to that of Co in terms of 7 nm MOL critical dimensions. Both Ru and Co have better liner/barrier scalability compared to W. Susan Su-Chen Fanet al. demonstrated Ru metallization assessment on 7 nm MOL with remarkable resistance reduction in the S/D contact and MOL local interconnect [158]. Table 3 summarizes some MOL Metallization Options [158].

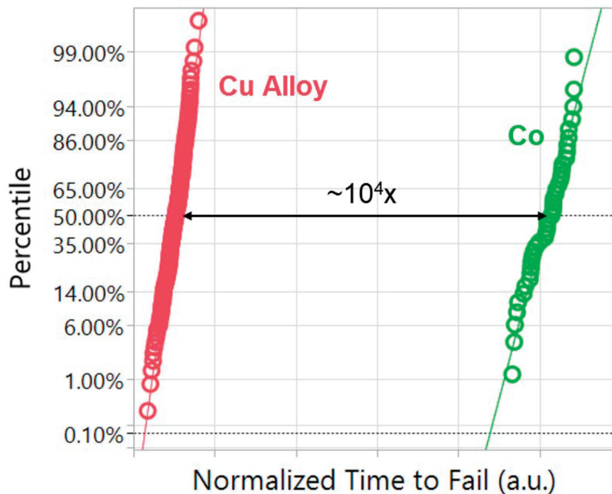


Figure 24. EM lifetime distributions for the Co and Cu alloy [157].

Table 3. Summary of all MOL Metallization Options [158].

No.	Process Name	Material		Normalized Total Resistance
		S/D Contact Level	MOL LI Level	
1	By Scaling	Ti/TiN W	Ti/TiN W	1
2	Process A	Ti/TiN W	Co	0.85
3	Process B	Ti/TiN W	Liner free W	0.7
4	Process C	Liner free W	Co	0.55
5	Process D	Liner free W	Ru	0.55

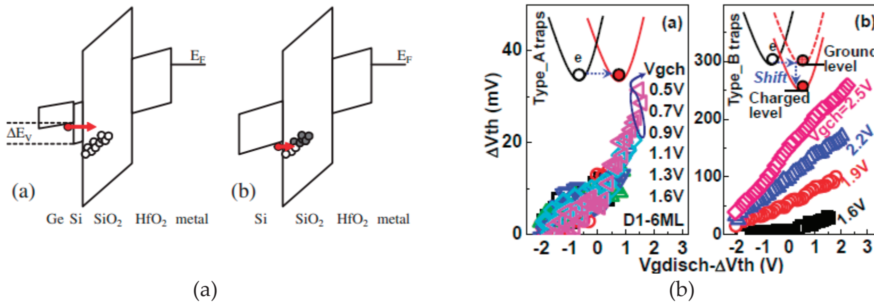
Moreover, the Co/$CoTi_x$ structure on SiO_2/p-Si was investigated to evaluate its feasibility to replace conventional W/TiN/Ti structure of MOL in a future technology node [158–160]. An alloy of Co-20 at.%Ti is chosen as a single layer liner/barrier to replace Ti/TiN. Since the binary phase diagram of the Co-Ti system shows a deep eutectic point at 24.2 at.%Ti, an amorphous phase can be formed as a metastable state, which is a prerequisite structure for a barrier layer. Good adhesion and low film resistivity between Co and $SiO_2$was attained by $CoTi_x$ in as-deposited and annealed samples. The results indicate that the 3 nm thick $CoTi_x$ layer has an excellent diffusion barrier property against Co diffusion at the elevated temperature 500 °C. Therefore, the amorphous $CoTi_x$ alloy could be a promising liner/barrier material in combination with the Co M0/contact structure for advanced technology of the 5-nm node.

13. Reliability

For advanced CMOS technology, the ultra-scale FinFET and Nano sheets are the best candidates for the beyond 5-nm technology node. The reliability issues are becoming more complicated due to the novel materials, novel process, novel integration, and novel structures for the performance improvement.

13.1. New Material—Ge/GeSi

In order to improve the device performance, the novel materials, such as GeSi/Ge, is applied in channel or S/D regions [161–165]. In contrary to traditional silicon technology, the structure of high-*k* and metal gate (HK & MG) stack is changed/improved by novel material application but, at the same time, the interface quality between substrate and gate insulator becomes worse. Therefore, interface quality and reliability of novel materials are actively researched. Based on those, a Si-passivated option was proposed by inserting a thin silicon passivated monolayer between Ge layer and SiO_2 to improve interface quality and reliability together [161–163]. In this case, the band alignment of Ge and Si shows the different carrier transport mechanism under bias temperature instability (BTI) stress. Therefore, the BTI is clearly improved, as shown in Figure 25a. Moreover, in Figure 25b, the two types of electron traps are investigated, which is related to the HK layer thickness and Si-cap growth condition [165]. Furthermore, this is a big issue for the reliability model for new materials, such as the negative bias instability (NBTI) model of SiGe [166,167]. The novel materials can worsen the interface quality and cause serious reliability problems. Therefore, the solution to suppress reliability degradation and to improve performance are important issues.

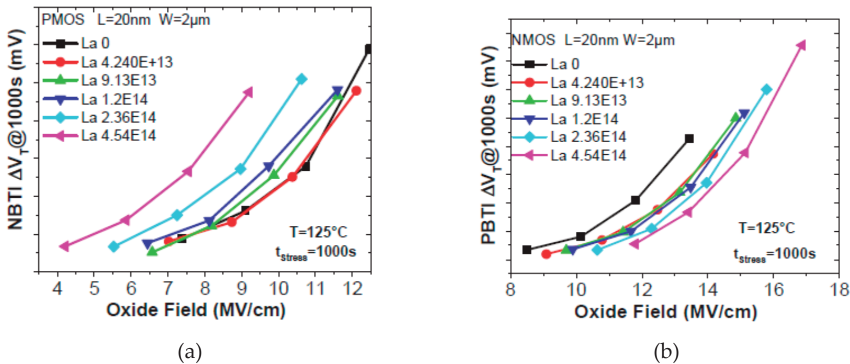


(a) (b)

Figure 25. (**a**) Schematic image of the band alignment of the Ge and Si channel gate stacks during NBTI stress. The Ge/Si valence band offset (Si-passivated Ge FETs) causes the inversion layer to energetically move away from the oxide traps [161] and (**b**) defect energy profiles after filling at low and high Vgch vs. Vgdisch-ΔVth. The insets illustrate the charging mechanisms for two different types of electron traps [162].

13.2. New Process—Dipole Formation

In advanced CMOS technology, in order to reduce the influence of the thermal budget on junction and channel quality, introducing the novel materials and processes are necessary in gate engineering. Therefore, the dipole formation in the gate stack is widely applied in the Replacement Metal Gate (RMG) process [168–173]. Usually, Lanthanum (La) and Aluminum (Al) are used to tune threshold voltage for NFET and PFET due to the different dipole polarity [168–171]. This includes metal deposition (La or Al) and annealing treatment with or without a capping layer [168]. It has been reported that La induced dipole effectively, which makes V_T decrease and positive bias temperature instability (PBTI) improve, but NBTI is worsened [168,169]. Meanwhile, the Al induced dipole increases V_T and BTI becomes worse as well. These results are explained by the band-diagram at the same E-field and Vg stress, as shown in Figure 26 [168]. Recently, IBM and the Applied Material proposed ALD Mg-based dipole method for multi-V_T tuning application. The results discuss the electrical parameters changing by the Mg-based dipole. However, there are no reliability investigations [168].



(a) (b)

Figure 26. (**a**) NBTI V_T shift vs. Eox after 1000 s for all effective La doses in PMOS. La addition causes enhancement of NBTI V_T degradation and (**b**) PBTI V_T shift vs. Eox after 1000 s for all La doses for NMOS. La addition causes reduction of PBTI V_T degradation [168].

13.3. New Integration—Physical Mechanism

Similar to the novel process, the novel integration is also necessary for performance and reliability improvement especially in gate engineering [162–164,174,175]. As an example, Simple Gate Metal

Anneal (SIGMA) [171] is applied for a thin TiN layer as a work function (WF) metal for CMOS (red-marked in Figure 27a). The PBTI lifetime is 100× improved due to the oxygen vacancy effectively decreasing during α-si removal. The CMOS integration flow together with a mechanism for PBTI improvement, which are shown as a band diagram in Figure 27b. For the reliability study, the impurity implantation in the HK&MG stack, such as "Nitrogen Implantation" in the work function metal layer [170] and the thickness tuning of an effective work function metal (EWF) can be investigated [170–173]. The advantage of such a study is to control the V_T shift over a processed wafer, which provides very valuable information for chipmakers. This is a feedback between reliability improvement and novel integration.

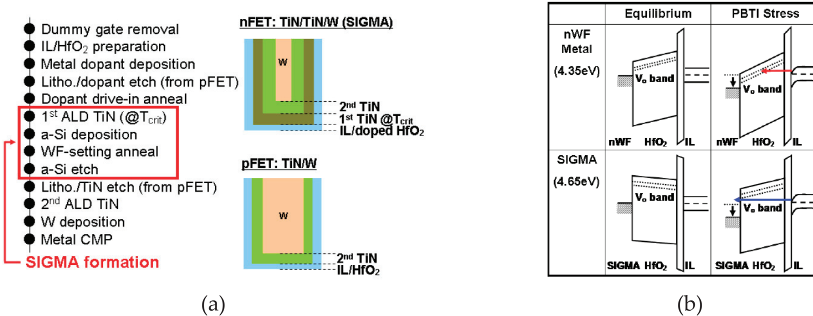


Figure 27. (**a**) CMOS flow and schematics for NFET with SIGMA/W stack and PFET with TiN/W stack and (**b**) PBTI improvement mechanism for the SIGMA stack [174].

13.4. New Structure—Self-Heating (SH) and Random Telegraph Noise (RTN)

In CMOS miniaturization, the random telegraph noise (RTN) needs to be paid more attention to as an indicator for problem source acting on the transistor performance. For advanced CMOS, the self-heating becomes a more serious matter and this has been widely studied [176–179]. It has been reported that PFET has higher RTN than NFET due to an extrinsic origin caused by SiGe in the S/D [177]. Moreover, based on simulation results, the nano-sheet devices exhibit better resilience to a self-heating effect (SHE) in comparison to the FinFETs [177]. In general, SHE is very sensitive to layout design, hot-carrier degradation (HCD), and bias temperature instability (BTI) [178,179]. In the layout design of the nano sheet devices, the width of the nano sheet (Wsh) is the key parameter, which provides a flexible choice to make trade-offs between thermal properties and electrical performance in nanosheet FETs, compared with the NW FETs (see Figure 28) [179]. Usually, the random telegraph noise (RTN) is generated by a single trap, which is explained by the "normal" two-state trap model. This model considers the RTNs caused by two or more traps in a device, which are regarded as independent and may have a superposition effect [180–183]. In general, two categories of RTNs are induced: those by the metastable trap-states and the others by the trap coupling effect, as shown in Figure 29 [180,181]. It has proposed a novel RTN-true random number generators (TRNGs) design, which provides a solution to address speed, design area, power consumption, reliability, and cost simultaneously [182]. In the RTN study of Ge NW nMOSFETs, it shows that the low frequency noise decreases when the channel length scales down from 80 nm to 40 nm because of the near-ballistic transport of electrons [183].

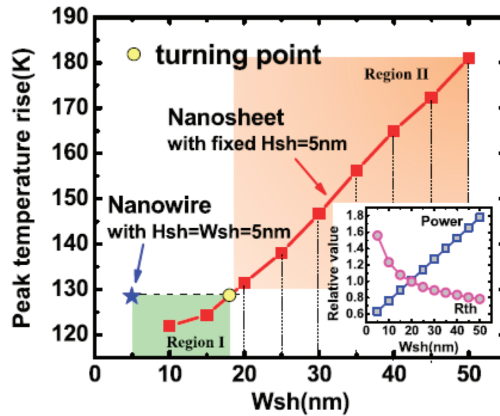


Figure 28. Peak temperature rise in nano-sheet FETs with increased width of nano-sheets (Wsh) [179]. H_{sh} stands for height or thickness of nano-sheets.

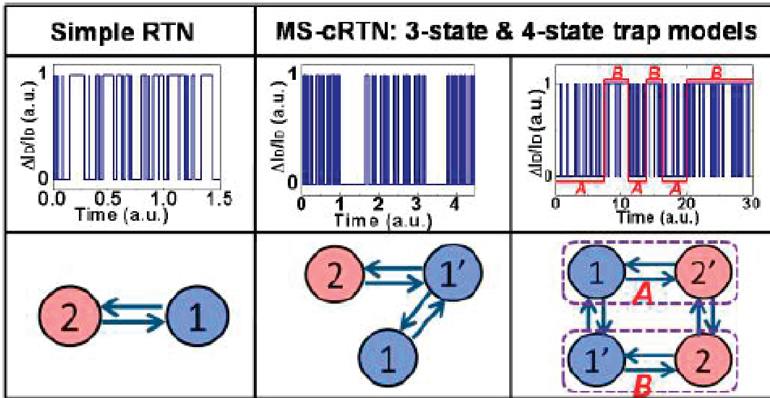


Figure 29. Illustration of the complex RTN induced by a single trap with an additional one or two metastable states, named as MS-cRTN [181].

14. Channel Materials for Beyond Moore Era

14.1. III-V on Silicon

Chipmakers have declined III-V materials at the 7-nm node but the main question still remains whether III-V will happen in advanced CMOS.

There are a lot of challenges in integrating III-V materials on silicon, ranging from epitaxy to etching. For example, the etch rates for ternary compound materials, e.g., InGaAs with complex concentration has to be properly controlled where all atoms will be removed at the same pace. Otherwise, the diffusion of arsenic during a different process could lead to cross-contamination [36].

Whatever, the next step in CMOS technology is, we have to implement the right process for integration of III-V materials on silicon, which are categorized in the three following ways: blanket epitaxy [184,185], selective epitaxy [186,187], and wafer bonding [188].

IMEC demonstrated III-V FinFET and III-V parallel Gate-All-Around (GAA) FET on a silicon substrate by ART technology [186]. They reported InGaAs GAA FETs with channel width down to 7 nm and L_g down to 36 nm, which is the smallest dimensions reported about III-V materials devices on 300 mm Si wafer. Figure 30 shows the TEM of completed devices. I_{ON} above 200 μA/μm is obtained

at I_{OFF} of 100 nA/µm and V_{DS} = 0.5 V on a 300 mm Si platform. The InGaAs S/D improves the peak g_m by 25% relative to InAs S/D.

The same group presented a promising way to manufacture III-V vertical GAA FET [187]. They used an InGaAs nucleation layer for InAs NW SAE on Si and reached nearly 100% yield, but there was no further report on the III-V vertical device yet.

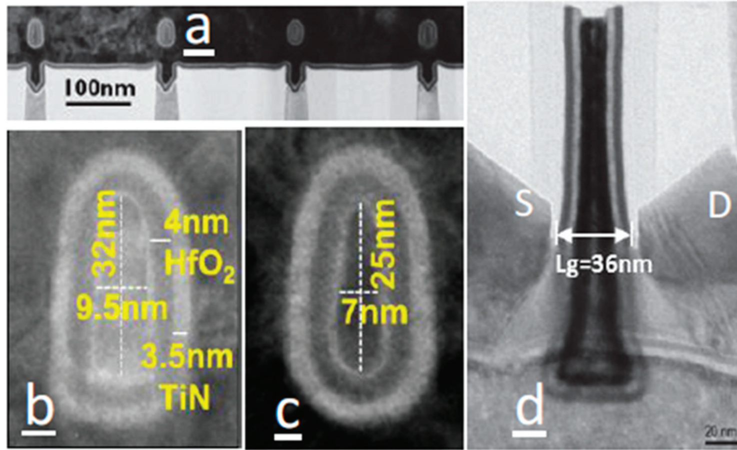


Figure 30. TEM micrographs of completed devices. (**a**) Devices across one gate pattern. (**b**) 9.5 nm-wide channel obtained from 2 cycles of WHALE* where 1 nm conformal interfacial layer was grown by ALD before HfO_2 deposition. (**c**) 7 nm-wide channel obtained from 5 cycles of WHALE* with the same gate stack as shown in (**b**) are used, and (**d**) along the trench showing L_g of 36 nm [186]. * WHALE stands for Wet HCl-based Atomic Layer Etch.

In recent years, IBM demonstrated a series of electronic devices including InGaAs-OI FinFET, InGaAs FET, III-V Tunnel FETs (TFETs), and hybrid InGaAs/SiGe CMOS on a silicon substrate [189–194] by using advanced template-assisted selective epitaxy technology [190].

They reported CMOS-compatible n-channel InGaAs-OI FinFETs by replacing the metal gate (RMG) process flow, as shown in Figure 31 [191–193]. The channel down to L_g = 50 nm with W_{Fin} = 15 nm has proven to have an excellent control on short channel effects [192]. The same device exhibited a record I_{ON} of 156µA/µmfor a supply voltage of 0.5 V and a fixed OFF-state current of 100 nA/µm, with a minimum sub-threshold swing of 92 mV/decade at V_{DS} = 0.5 V and a drain-induced barrier lowering to 57 mV/V. This I_{ON} value is the highest reported to date for CMOS-compatible InGaAs devices integrated on Si.

Furthermore, they show record-performance InGaAs-on-Insulator FinFET with L_g down to 13 nm, where I_{ON} reaches to 249 µA/µm at fixed I_{OFF} = 100 nA/µm and V_D = 0.5 V. This work demonstrates the feasibility of high-performance III-V devices on Si at sub-7 nm nodes [193].

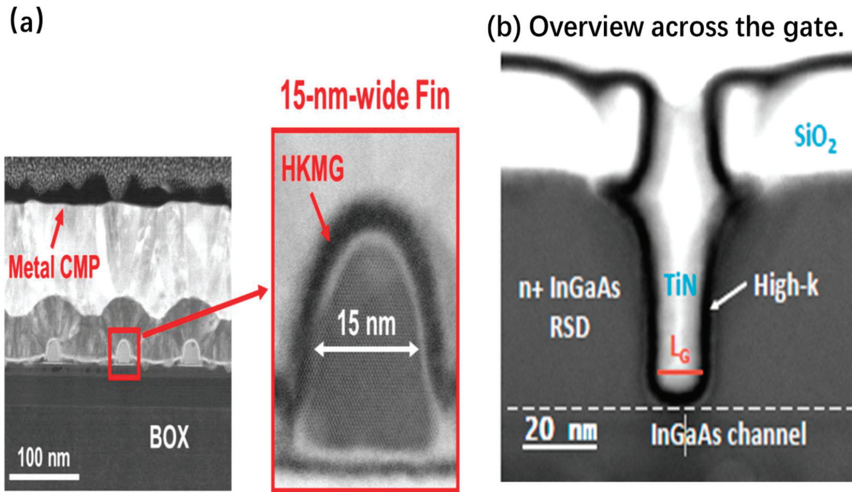


Figure 31. Cross-section images of the self-aligned InGaAs-OI FinFET architecture where (**a**) the scaled HKMG deposited on a 15-nm-wide fin using a highly conformal and uniform PEALD* process [192], and (**b**) shows CS STEM images across the gate showing the InGaAs FinFET with L_g = 13 nm [194]. * plasma-enhanced atomic layer deposition.

14.2. 2D Channel Materials

Over the last decade, various 2D materials have been discovered and studied as promising candidates for next-generation electronic materials due to their unique properties such as atomic thin thickness, high mechanical strength, transparency, and flexibility. There are several interesting 2D materials, which could be applied as channel material in CMOS for beyond the Moore era, as presented below.

14.2.1. Graphene

Graphene is a material composed of carbon atoms closely packed into a single layer two-dimensional honeycomb lattice structure. Graphene has many unique physical properties, which attract attention to use it as channel material beyond Moore.

(1) Ultra-high mobility: The mobility of the suspended exfoliated graphene is as high as about 2 $\times 10^5$ $cm^2 \cdot V^{-1} \cdot s^{-1}$ without considering the charged impurities and ripples [195]. (2) Great thermal conductivity: The thermal conductivity of graphene is superior to that of carbon nanotubes and diamonds. Single-layer graphene has a thermal conductivity of up to 5300 W/mK, which is much higher than metals such as silver and copper with high thermal conductivity [196]. (3) Excellent light transmission: Graphene is almost completely transparent. It only absorbs 2.3% of light and allows all spectral light to pass evenly. Therefore, it also has great application potential in the field of optoelectronic devices [197].

Since the material has almost no bandgap, then a lot of works have been performed to create bandgap for graphene, which can be classified into three types: (1) fabricate graphene nanoribbons (GNR) by cutting graphene sheets into narrow strips, (2) grow bilayer graphene (BLG) by Bernal stacking, and (3) form a heterojunction in graphene by introducing a material with a non-zero bandgap as a barrier.

Single Layer Graphene Field Effect Transistors

The lack of bandgap in the single layer graphene results in such transistors not being able to turn off. Therefore, they can only be used in the field of radiofrequency (RF) circuits. Wu et al. studied the

formation of graphene FETs on SiC substrates. The cutoff frequency of the device with a gate length of 40 nm can be increased up to 350 GHz, which is much better than silicon transistors (40 GHz) under the same conditions [198].

Graphene Nanoribbons Field Effect Transistors

When the width of graphene nanoribbons is less than 10 nm, it exhibits semiconductor characteristics. The bandgap of GNRs is inversely proportional to the ribbon width. Studies have shown that, as the GNR width decreases, the on/off ratio of devices increases. Jiao et al. reported a plasma etching process to produce high quality, narrow GNRs with a bandgap of ~15 meV [199]. Wang et al. demonstrated sub-10 nm GNRs FETs with I_{on}/I_{off} ratio up to 10^6 and on-state current density as high as ~2000 μA/μm at room temperature [200].

Compared to large-area laminar graphene transistors, MOSFETs made from graphene nanoribbons have a significantly improved device current on/off ratio. If high-quality GNRs can be produced on a large scale in the future, such nanoribbon transistors will likely be applied to logic circuits in the future.

Bilayer Graphene Field Effect Transistors

If two graphene layers are asymmetrically stacked, so-called Bernal stacking, and a vertical electric field is applied to them, a bandgap can be generated in graphene. Zhou et al. determined the bandgap of graphene placed on SiC and the bandgap is 0.26 meV when there is only one graphene layer. As the number of layers increases, the bandgap will gradually decrease [201]. Liu et al. demonstrated a large number (>50) of dual-gated field-effect transistors with high on/off current ratios of 15 fabricated at random across the large-area bilayer CVD graphene film, which further confirms the quality of the synthesized graphene [202].

The BLG can be made to have a bandgap by the above method, but its value is small. These values so far are promising for the high mobility graphene application but is still insufficient for logic applications. The mobility of the carriers in the double-layered graphene structure is lower than that of the single-layer graphene without the bandgap.

Graphene Heterojunction Field Effect Transistors

In recent years, a heterojunction was formed on the surface and boundary of the graphene to form a heterojunction transistor by introducing a material with a non-zero bandgap as a barrier to generate a forbidden band. Graphene heterojunction transistors are generally classified into lateral heterojunctions and vertical heterojunctions. This method is a new research hotspot of graphene digital transistors. Moon et al. partially fluorinated the single-layer graphene to obtain a lateral heterojunction structure with a bandgap of about 2.93 eV and a current on/off ratio of 10^6 [203].

Although it is still a great challenge to fabricate a dielectric material that is lattice-matched with graphene, the vertical heterojunction structure can construct a tunnel transistor and achieve a high current on/off ratio of $>10^7$ [204]. In addition, graphene-based vertical heterostructures can be extended from FET electronics to optoelectronics, which is a promising direction.

In general, graphene field effect transistors (GFETs) still have a long way to go from practical applications. Although GFETs have broad application prospects, it also faces many challenges. In addition, other indicators for evaluating digital circuits, such as short channel effects, integration, and power consumption, should be considered.

14.2.2. Graphene-Like Materials as Channel Materials

Transition-metal dichalcogenides (TMDCs), e.g., MoS_2, WSe_2, WS_2, etc. have emerged as a new class of semiconductors that display distinctive properties at the monolayer thickness. They can be used in electronic devices such as transistors and in optical components as emitters and detectors. The band gaps of TMDC monolayers are in the visible range (between 400 nm and 700 nm).

Classes and representative examples of 2D materials together with representative materials for each group are shown in Figure 32 [205].

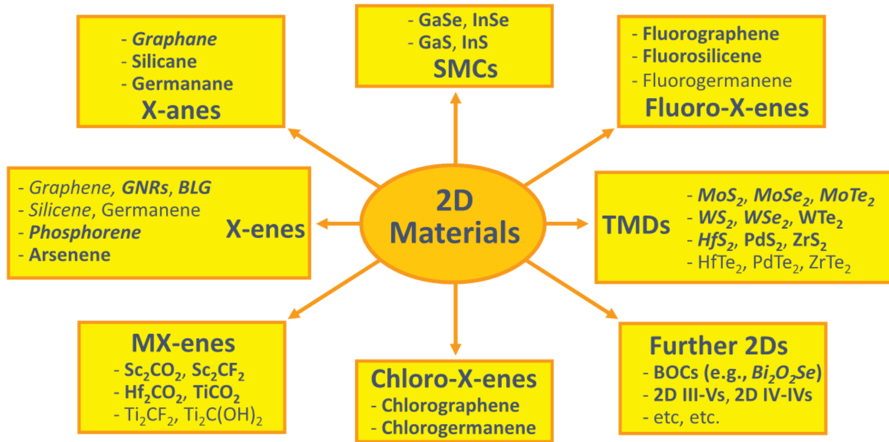


Figure 32. Drawing of different 2D materials [205].

A novel example for 2D transistors is shown in Figure 33. A dual-channel FET based on a vertically stacked hetero-structure of ultrathin n-type MoS_2 and p-type WSe_2 layers for the study of parallel carrier transport (electrons from MoS_2 and holes from WSe_2) have been demonstrated [206].

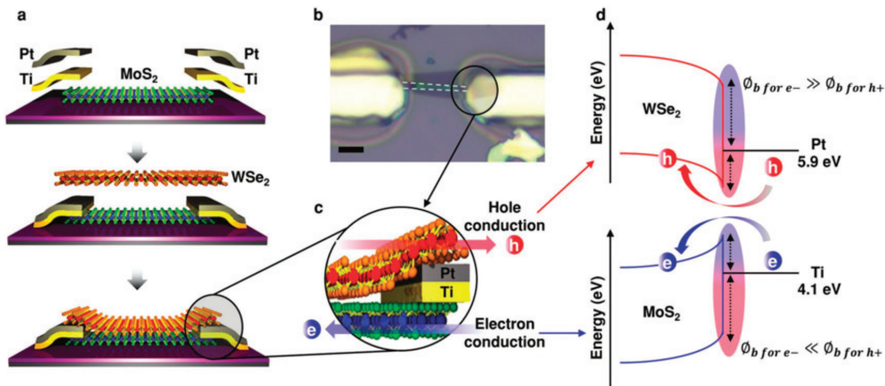


Figure 33. (**a**) Schematic of fabrication, a WSe_2/MoS_2 hetero-structure dual-channel FET. (**b**) Optical picture of a processed transistor. The dashed line shows the bottom MoS_2 layer, (**c**) schematic of electron and hole transport in one channel of dual-channel FET, and (**d**) band diagram WSe_2-Pt metal (top) and MoS_2-Ti. The symbol ϕ_b in the picture stands for the barrier for hole and electrons [206].

Atomic thin molybdenum disulfide (MoS_2) is an ideal semiconductor material for field-effect transistors (FETs) with sub-10-nm channel lengths. The high effective mass and large bandgap of MoS_2 minimize direct source-drain tunneling, while its atomic thin body maximizes the gate modulation efficiency in ultra-short-channel transistors. The sub-10 nm channel-length transistor was fabricated by directed self-assembly patterning of the mono-layer and tri-layer MoS_2. This is done in a 7.5-nm half-pitch periodic chain of transistors where semiconducting (2H) MoS_2 channel regions are connected to metallic-phase (1T) MoS_2 and contact regions. The resulting 7.5-nm channel-length MoS_2 FET has a low off current of 10 pA/µm, an on/off current ratio of $>10^7$, and a subthreshold swing of 120 mV/dec.

To demonstrate and benchmark MoS_2 transistors with channel lengths below 10 nm, two important challenges need to be overcome, which include a suitable lithography technology and a low-contact resistance for the S/D to ensure that the channel resistance will dominate the device behavior. To reduce the contact resistance, a junction between the metallic phase of MoS_2 (1T) and its semiconducting phase (2H) has been used (see Figure 34) [207].

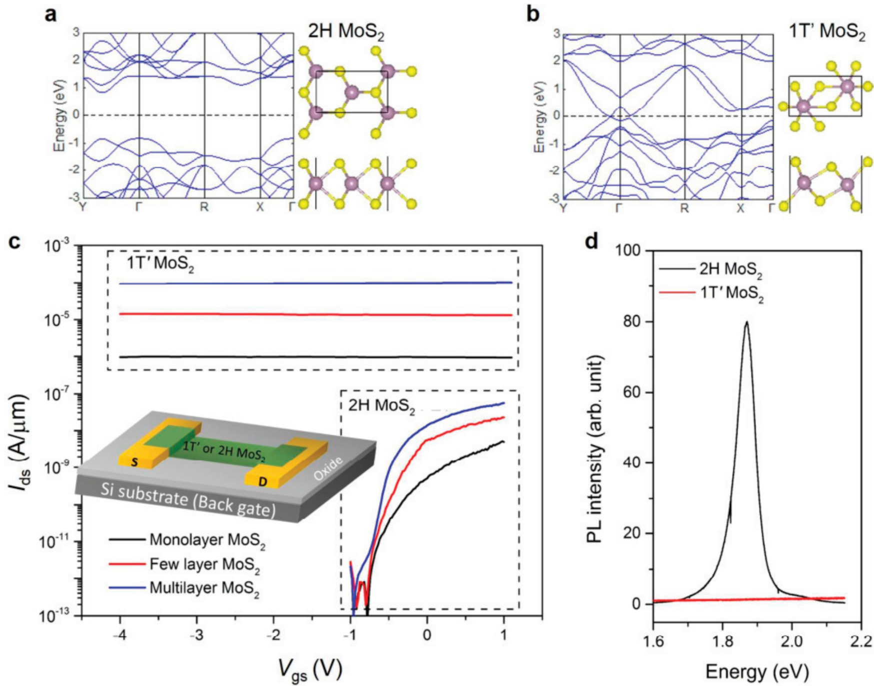
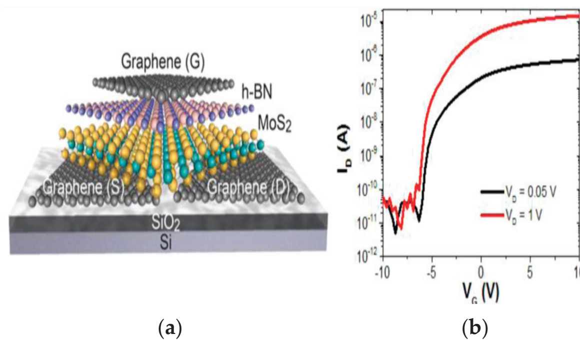


Figure 34. (**a**) and (**b**) Electronic band structures of 2H and 1T′ MoS_2 and their atomic structures. The 2H band structure shows a bandgap of approximately 1.8 eV, while the conduction and valance bands of 1T′ MoS_2 overlap. Therefore, 1T′ MoS_2 has metallic gapless characteristics. (**c**) Transfer characteristics of three MoS_2 FETs with different thicknesses of MoS_2 before and after phase transition treatment. The intrinsic 2H MoS_2 FETs show strong semiconducting behavior with large gate modulation, while the phase transition shows constant current with almost no gate modulation featuring, and (**d**) PL (photoluminescence)spectra of the monolayer 2H and 1T′ MoS_2. The 2H phase shows a strong PL peak at 1.85 eV generated by its bandgap, while the PL of the 1T′ phase is completely quenched due to its gapless metallic characteristics [207].

More complicated 2D material transistors can be realized by using heterogeneous stacks. For example, MoS_2 is used as the active channel material and hexagonal-BN as the top-gate dielectric with graphene S/D (see Figure 35). This transistor exhibits n-type behavior with an ON/OFF current ratio of $>10^6$, and an electron mobility of ~33 cm^2/Vs. The mobility does not degrade at high gate voltages, which presents an important advantage over conventional Si transistors where enhanced surface roughness scattering severely reduces carrier mobility values at high gate-fields [208].



(**a**) (**b**)

Figure 35. (**a**) Schematic of advanced 2D stacks and (**b**) characteristic curves of the transistor.

(1) Tunnel Field Effect Transistors (TFET)

The next generation of transistors in the future has to offer a sub-threshold swing of sub-60 mV/decade with a supply voltage < 0.6 V. In this field, different devices e.g., negative-capacitance FETs [209,210] and tunnel FETs (TFET) [211,212] are proposed. TFET is a gated p-i-n diode where the carriers are injected from the source to the channel region through the band-to-band tunneling (BTBT) mechanism [213]. Therefore, TFTs offer remarkably low I_{OFF} with a steep subthreshold slope.

Since the sub-threshold swing decreases with the gate voltage bias, then the transistors have to be manufactured for a low voltage supply. In order to obtain high tunneling current and a steep slope, the transmission probability through the tunneling barrier has to be close to unity for a small variation of gate voltage. Therefore, the bandgap, the effective carrier mass, and the screening tunneling length have to be minimized for high barrier transparency. Finding appropriate materials for TFETs is an issue to be solved [214,215]. For example, Si-based TFETs have reported poor sub-threshold swing and low ON-current14 due to indirect band gap of 1.12 eV, which causes phonon-assisted tunneling (PAT) [216]. Recent studies suggest 2D materials have great properties for TFET channel material due to their planar structure and mechanical flexibility, outstanding electrostatic integrity, and small band gap with low effective mass. In this case, Graphene nanoribbon [217,218], transition metal di-chalcogenides (MoS_2, WS_2, $MoSe_2$, WSe_2, $MoTe_2$, etc.) [219,220] Phosphorene [221,222], and group IV mono-chalcogenides (GeSe, GeS, SnSe, SnS) have been proposed for TFETs. Both hetero-bilayer [223,224] and hetero-junction transistors 25 are designed. TFT (field-effect transistors) technology is still not mature and needs more reliable fabrication techniques for mass production.

(2) New Devices in the Near Future

Intel has demonstrated a spintronic logic device, so-called magnetoelectric spin–orbit (MESO), which can be scaled down in energy per operation to a level of switching energy. This is 30 times below today's CMOS transistors. MESO may operate at a voltage around 100 mV, which is 5 times below any advanced CMOS. The device functions by a ferroelectric/magnetoelectric switching and topological conversion of spin to charge. In addition, the non-volatility property offers remarkably low standby power, which is crucial for modern computing. MESO has the potential to be developed for multi-generational computing in the future [225].

15. Advanced Characterization for Ultra-Miniaturized CMOS

The continuous refinement of semiconductor manufacturing technologies urges the key sizes of devices to be down scaled while more challenges are created in testing methodologies. The expected measurements are not only focusing on critical dimension and thickness, but also on the 3D device structure on a nanometer scale. In research development in the future, it is necessary to measure the critical dimensions of the device structure, thickness of thin film, surface and interface properties,

physical properties, and surface defects. It is expected that the test equipment should have a high-precision, high-speed, and is non-destructive, which can be used to monitor in-line. The application of advanced measurement strategies of integrated circuit critical dimension in ultra-miniaturized CMOS are presented below.

15.1. CD-SEM

Traditional SEM imaging is slow and cannot meet the needs of the semiconductor industry. High throughput SEM has a high detection speed and has been prepared and developed by processes below 10 nm. High throughput SEM technology is a general term for the integrated application of multiple technologies, including immersion rocker objectives lens, focus tracking technology, charge control technology, and high-speed image acquisition system. Their application makes large-area high-precision scanning imaging a reality, and, compared to imaging speed of the traditional SEM, is more than 300 times faster, where the low-voltage resolution is up to the nanometer level [226].

CD-SEM is an important test device in the front-end process of integrated circuits. CD-SEM is mainly used for in-line measurement of critical dimensions and performance monitoring of critical equipment during chip manufacturing. CD-SEM also plays an important role in optical proximity correction (OPC) model modification. Its main feature is the rapid and accurate automatic image recognition ability. In addition, CD-SEM can realize more test methods by constant optimization and improvement of the algorithm, such as Edge Roughness evaluation, Gap, wiggling, overlay, and center gravity. The advantages of CD-SEM makes the tool more useful in some form of continued applications. However, with the development of integrated circuits in the future, CD-SEM demands improving the resolution and assisting the modeling of OPC 2D graphics [227].

15.2. 3D AFM (Atomic Force Microscope)

3D AFM technology is based on a non-contact technique. In addition, this tool can be tilted at angles up to 38 degrees. AFM testing can be applied in the dimensional space, resolving sidewall and analyzing three-dimensional doping that most testing techniques cannot measure. 3D AFM has the nondestructive measurement of nano precision and accuracy, which can realize automatic analysis and cooperate with efficient production. 3D AFM technology can be used in In-line monitoring and engineering analysis. It overcomes the weakness of CD SEM in measuring CD at the bottom of the sidewall, and can test data more accurately than OCD (optical critical dimension), which saves the derivation work of the optical measurement [228].

15.3. 3D APT (Atom Probe Tomography)

The principle of elemental analysis by TEM/STEM is that an electron beam is required to act on the material and then elemental analysis is performed based on the information of the scattered electrons. At present, the elemental analysis results of TEM/STEM are basically two-dimensional. Due to the limitation of the resolution, for many elements with low atomic number, such as C, N, O, and Al, the resolution of TEM/STEM is low, and energy dispersive spectrometer (EDS), EELS elemental analysis cannot easily distinguish the elements [205]. The above reasons make TEM/STEM not provide the required information in some occasions. APT technology can overcome the problem to distinguish light elements, and directly obtain the element distribution in three-dimensional space in solid samples, which is a significant advantage compared to TEM/STEM technology. In most semiconductor devices, there are often multiple components, and their spatially ordered distribution constitutes nano-devices.

An element map with a high resolution can be obtained in space. Through the use of 3D Atom Probe Tomography (3D APT), the three-dimensional structure of the device can be characterized, and the parameters of the device as well as the size and spatial structure of each component can be understood. As shown in Figure 36, 3D APT volume is based on the standard reconstruction algorithm after density correction of GAA (a) and tri-gate (b) silicon nanowire transistor. An element map with a

high resolution can be obtained in space. The interface of different materials is clearly visible, which can effectively help us understand the structural characteristics of these devices.

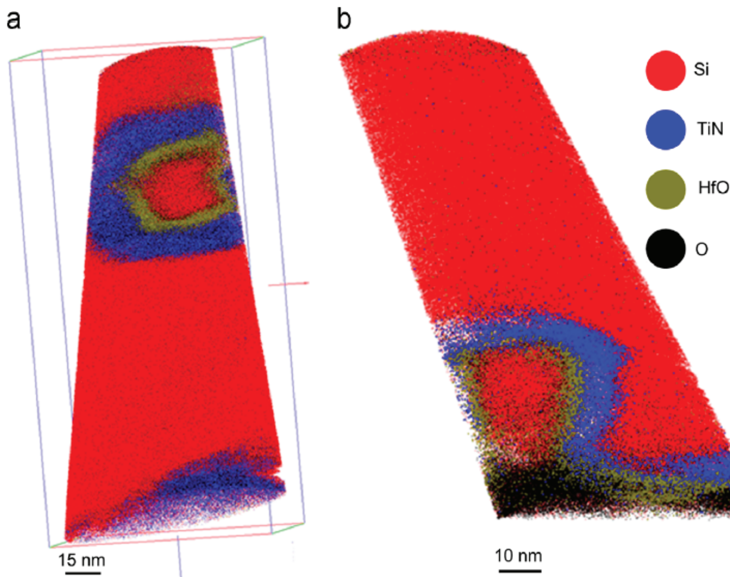


Figure 36. 3D APT volume based on the standard reconstruction algorithm after density correction of GAA (**a**) and tri-gate (**b**) silicon nanowire transistor [229].

3D APT method reveals any non-uniform shape of the apex since the signals are distorted due to irregularity of nano-scaled shapes. In the future, we need to develop an advanced sample preparation technology that contributes for a better structure analysis but also better distinguish the corresponding positions of elements, which reduces the impact of material types. The interface states on resolution and avoiding defects leads to failure of the analysis results. APT also needs to combine more equipment to improve test results and analysis algorithms to restore the three-dimensional structure more realistically. This technology is still developing and improving in the semiconductor field [230,231].

15.4. Optical Critical Dimension

Optical critical dimension (OCD) measurement equipment is widely used in process development and process control with its fast, non-destructive, and non-contact testing methods. The principle is to obliquely illuminate the surface of the film with elliptically polarized light in a broadband band as well as to collect the reflection spectrum, and measure the thickness and width parameters of the three-dimensional structure by optical calculation. A spectral database is formed in the early stage and the collected measured spectra were fitted with the theoretical spectra to obtain the final results. The measurements could include the spectroscopic ellipsometry (SE), Mueller matrix (MM) SE, and normal incident polarized reflectometry, or multi-Angle multi-wavelength OCD [232,233].

Optical critical dimension measurement equipment is widely used in process development and process control with its fast, non-destructive, non-contact testing methods. The CD of the 3D device structure and the thickness of each film layer can be measured. However, OCD faces a new challenge as the size of the node becomes smaller. For example, the measurement is complicated for multi-film parameter measurements, 3D measurements, or to obtain a random structure parameter (roughness) in FinFET. In order to increase the sensitivity of the tool to different structural parameters such as CD or sidewall angle, extensive research has been conducted to use Mueller-matrix spectroscopic

ellipsometry. In this field, using scatterometry as part of a hybrid metering scheme could help reduce parameter uncertainty [234–236].

15.5. Hybrid Metrology

The precision and high-efficiency test equipment has been remarkably improved for next-generations of transistor fabrication. In this field, hybrid metrology improves the metrology performance of complex device structures by combining different test methods. In this way, more functions can be performed and measurement errors are eliminated, which improves the accuracy of test results compared to a single test device.

For FinFET structures, in-line monitoring CD-SEM can measure CD well, but it is not sensitive enough to determine the fin's height. Optical scattering can be used for FinFET structures, but relying on a large number of data for fitting, it greatly increases uncertainty in the measurement.

The FinFET structure can be measured by the CD-SEM, AFM, or TEM. Then, the results are fed into an OCD tool to validate and to compare the measured data from different processes and to examine to which extent these techniques can detect subtle differences in the process [237]. It may be important to use a hybrid metering method to share information across technologies and to reduce uncertainty to an acceptable level. In the future, we may use atomized measurement equipment. The output can then be combined with in-plant metering such as OCD, AFM, and CDSEM to create a hybrid metering solution. Hybrid metrology and artificial intelligence can be integrated in the measurement and data analysis.

15.6. X-Ray Metrology Technologies

Film metrology is an important issue besides CDs. There are three challenges in the metrology arena: compositional, dopant, and strain.

When the technology node moves toward 5 nm, the traditional metrology techniques maybe touch their limits [45]. FinFET and GAA structures create a need for 3D metrology where X-ray plays a significant role by using the following technologies- XRF (X-ray fluorescence), XPS (X-ray photoelectron spectroscopy), XRR (x-ray reflectivity), XRDI (X-ray diffraction image), XRD (X-Ray Diffraction), HRXRD (high resolution X-Ray Diffraction), LEXES (low energy electron induced X-ray emission spectrometry), CD-SAXS, and GISAXS.

XRF is a photometric technique, which is used to look at surface contamination. The XRF/XPS combo tool is applied to determine the composition and chemistry on the surface. XRR handles thin films and XRDI is used to detect wafer level defects such as slip.

HRXRD, or XRD, is a technique to characterize composition, thickness, dopant concentration and strain in devices [238–243]. HRXRD is used to qualify the repeating patterns of FinFETs [244–247]. The LEXES is involved for dopants in materials.

HRXRD is emphasized as an important tool to characterize 10-nm node and beyond. It has been demonstrated that in-line HRXRD can monitor the pre-fin and post-fin etching processes in FinFET [248]. IMEC demonstrated an in-line HRXRD set-up for analyzing composition and strain for nano-scale level devices. They have successfully studied the composition and strain state of etched and selectively grown Ge/SiGe fins as well as multilayer fin width down to 16 nm. The RSM (reciprocal space mapping) of (113) reflection acquired from fins, which provides information about the lattice parameters in two directions, and calculate fin pitch, according to the spacing between first order grating rods in the figure [247]. It is important to mention that HRXRD is also used to characterize III-V fins in sub-10 nm as well.

Beyond metrology for epitaxy application, the semiconductor industry is also exploring new metrology techniques for future requirement to characterize a three-dimensional structure, where the critical dimensions are less than 10 nm. CD small-angle X-ray scattering (CD-SAXS) is non-destructive and a promising technique to characterize the nano-devices [249–251]. This technique collects a series of scattering signals by a small rotation angle of samples. The signals contain both in-plane and

out-of-plane information. This technique is used to reconstruct the 3D reciprocal-space for measuring line profiles of short grating, as shown in Figure 37. CD-SAXS provides real potential solutions for replacing the traditional techniques like CD-SEM and OCD and it is applicable to any type of material-crystalline, polycrystalline, and resists.

Intel and the National Institute of Standards and Technology (NIST) have demonstrated CD-SAXS measurements from patterned 12 nm lines device with 0.5 nm spacing [250]. Using CD-SAXS, an accuracy down to 0.1 nm has been reported. CD-SAXS can be used for 7 nm or 5 nm structures for 3D memory, advanced EPI (epitaxy), and FinFETs with no calibration.

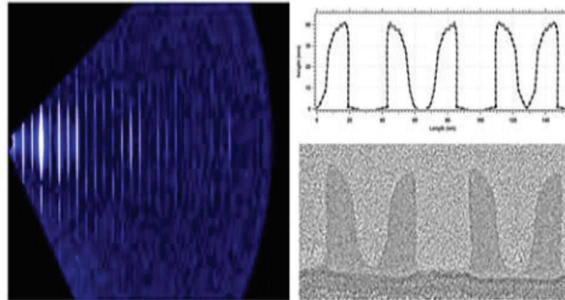


Figure 37. RSM and fits to the scattering profile of samples [250].

Another strategy for measuring critical dimensions is using Grazing-incidence small-angle X-ray scattering (GISAXS) [252]. The measurement geometry of GISAXS is shown in Figure 38 GISAXS can measure small targets, which are sensitive to the grating line profile. The technique shows the ability to extract structural parameters of the gratings depending on scanning the photon energy and the scattering intensity.

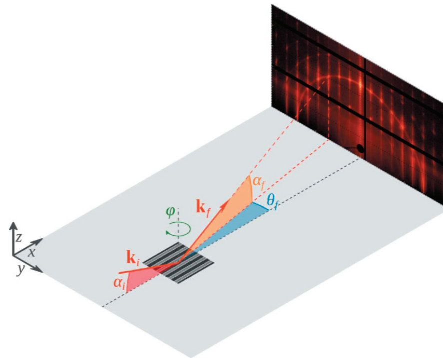


Figure 38. Geometry of GISAXS experiments [252].

15.7. Artificial Intelligence in Metrology

Artificial Intelligence in complex software programs is also involved in metrology recently. Machine learning is an emerging technique, which will not replace metrology tools, but it could help solve the most difficult metrology challenges at 10 nm node technology and beyond. The companies— Nova launched its Artificial Intelligent software NOVAFit™, using machine learning as a complementary method to predict the fin CD values from in-line measurements [253]. By using such a technique, the electrical resistance in interconnects using data from both OCD and electrical

tests could be predicted. The new software program improves metrology capabilities and accelerates time to analyze complex 3D devices with a high aspect ratio.

16. Conclusions

This article has presented the principle of miniaturization of MOSFET and a survey of technology roadmap for CMOS. An overview of transistor processing with a focus on the approach to the end has been provided.

The discussions initiated from state-of-art lithography of nano-scale patterns using the extreme ultraviolet (EUV) lithography and 193 nm immersion with multi-patterning. Even though EUV simplifies the patterning process for the 7 node, EUV still has issues with resists and mask infrastructure as well as power source, which have to be solved before high-volume manufacturing.

Furthermore, the challenges of FinFET processing and their relations to electrical characteristics were discussed.

In FinFETs, high current should be transported in fins. Therefore, longer fins are required. However, there is a difficulty for integration of poly-gate, spacer, and the replacement metal gate. For example, to etch the poly-gate with a high aspect ratio, it suffers from charging and micro-loading of etching, which results in variable gate length. It is concluded that an optimum wet and dry etch at low temperature and low etch rate is needed to avoid gate length variation and Si loss in fins.

SiGe has used as stressor material for source/drain regions starting from a 90 nm technology node. In order to have uniform SiGe epitaxy, a uniform chip layout is needed to minimize the pattern dependency of the growth.

In approach to the end of the technology roadmap, FinFETs become lateral or vertical nanowire transistors (LGAA or VGAA, respectively). In VGAA, the nanowire contains SiGe/Si or SiGe/Ge stack where Si, Ge, or SiGe can act as the channel of the transistor. Si or SiGe material could be selectively etched by using TMAH solution mixed by ACT® SG-201.

In the nanowire transistors, traditional ion implantation cannot be used and new doping strategies e.g., monolayer and plasma doping are required to dope the nanowires.

After planar transistors were changed to 3D FinFETs in 22-nm node, HfO_2 has been accepted as high-*k* material due to its high dielectric constant and a relatively large bandgap. However, the integration of HfO_2 in nano transistors has a problem of the thermal instability of HfO_2/Si interface. The SiO_x interlayer between HfO_2 and Si substrate can improve the interfacial imperfection. The thickness of this SiO_x interlayer and the high-*k* dielectric have been continuously decreased in each new technology node. Si polycrystalline gate-material was also abandoned and metal-gates like TiAlN and TiN were introduced in a gate-last approach to prevent crystallization of the high-*k* material during the thermal treatments.

In integrated circuits, ALD W with α-phase is mainly applied as electrode filling. One way to grow tungsten films with α-phase on SiO_2 is to use WF_6 as a precursor and H using hot-wire (HW) assisted atomic layer deposition (HWALD).

Cu is a classical interconnect material microelectronic circuit. However, as the CD narrows, filling the BEOL trench-over-via structure by Cu becomes more challenging. Introducing Co via the prefill concept makes it possible for void-free and bottom-up fill of metal in advanced interconnects. Co is expected to have a better EM performance compared to Cu due to its higher melting point.

Reliability test over of a processed wafer is very important for IC manufacturers and this becomes more critical when miniaturization of CMOS occurs. The checking points are novel materials, novel process, and novel integration where the reliability characterization provides information about the physical mechanism of degradation.

The random telegraph noise is also an issue that becomes more important for nano-scaled transistors and could act as an indicator for transistor performance. As an example, the self-heating in transistors could be a source for the signal noise.

In the future, when the Beyond Moore era is reached, it is believed new material, e.g., III-V and 2D crystals will be insightful. The main problem is integration of these materials with high quality on Si. So far, III-V devices, e.g., InGaAs-OI FinFET, InGaAs FET, III-V Tunnel FETs (TFETs), and hybrid InGaAs/SiGe CMOS on a silicon substrate by using advanced template-assisted selective epitaxy technology.

Among 2D material Graphene, transition-metal dichalcogenides (TMDCs), e.g., MoS_2, WSe_2, and WS_2 have a strong position for devices. Since the 2D material have a lack of bandgap, then three methods are proposed. The methods include narrow strips, bilayers, and heterojunction in order to create a bandgap.

Many promising devices from 2D materials have been manufactured. As an example, a dual-channel FET based on a vertically stacked hetero-structure of ultrathin n-type MoS_2 and p-type WSe_2 layers for the study of parallel carrier transport (electrons from MoS_2 and holes fromWSe_2) have been demonstrated.

More complicated 2D material transistors can be realized by using heterogeneous stacks. For example, MoS_2 is used as the active channel material and hexagonal-BN as the top-gate dielectric with graphene S/D. This type of transistors exhibit n-type behavior with an ON/OFF current ratio of $>10^6$, and an electron mobility of ~33 cm^2/Vs. The mobility does not degrade at high gate voltages, which presents an important advantage over conventional Si transistors where enhanced surface roughness scattering severely reduces carrier mobility values at high gate-fields.

In the research development in future production, it is necessary to measure the critical dimensions of the device structure, thickness of thin film, surface and interface properties, physical properties, and surface defects. It is expected that the test equipment should have a high-precision, high-speed, and be non-destructive, which can be used to monitor in-line. The famous tools are CD SEM, OCD, and 3D AFM, which can be used for the three-dimensional structure of the device. Recently, a new technique 3D APT, which provides an element map with a high resolution has been developed. In this way, the three-dimensional structure of the device can be characterized.

It is also required to use a combination of these techniques, which could provide information about more complex device structures.

A series of x-ray techniques, e.g., XRF, XPS, XRR, XRDI, XRD, HRXRD, LEXES, CD-SAXS, and GISAXS are also used for in-line measurements. These techniques provide information about crystalline materials for composition, thickness, dopant concentration, and strain in devices.

Recently, Artificial Intelligent in a new software form is also involved in metrology, which can help solve the most difficult metrology challenges at 10-nm node technology and beyond. The new software improves metrology capabilities and accelerates time to solution in complex 3D and High Aspect Ratio devices.

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References

1. Moore, G.E. Cramming More Components onto Integrated Circuits. *Electronics* **1965**, *38*, 114. [CrossRef]
2. Colinge, J.-P. *FinFETs and other Multi-Gate Transistors*; Springer: New York, NY, USA, 2008.

3. Natarajan, S.; Agostinelli, M.; Akbar, S.; Bost, M.; Bowonder, A.; Chikarmane, V.; Chouksey, S.; Dasgupta, A.; Fischer, K.; Fu, Q.; et al. A 14 nm logic technology featuring 2nd-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm^2 SRAM cell size. In Proceedings of the 2014 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2014; pp. 3–7.
4. Li, C.C.; Tsai, T.H.; Yuan, M.S.; Liao, C.C.; Chang, C.H.; Huang, T.C.; Liao, H.Y.; Lu, C.T.; Kuo, H.Y.; Hsieh, K.; et al. A 0.034 mm^2, 725 fs RMS jitter, 1.8%/V frequency-pushing, 10.8–19.3 GHz transformer-based fractional-N all-digital PLL in 10 nm FinFET CMOS. In Proceedings of the 2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits), Honolulu, HI, USA, 15–17 June 2016; pp. 1–2.
5. Xu, M.; Zhu, H.L.; Zhao, L.C.; Yin, H.X.; Zhong, J.; Li, J.F.; Zhao, C.; Chen, D.P.; Ye, T.C. Improved Short Channel Effect Control in Bulk FinFETs with Vertical Implantation to Form Self-Aligned Halo and Punch-Through Stop Pocket. *IEEE Electron Device Lett.* **2015**, *36*, 648–650. [CrossRef]
6. Yang, L.; Zhang, Q.Z.; Huang, Y.B.; Zheng, Z.S.; Li, B.; Li, B.H.; Zhang, X.Y.; Zhu, H.P.; Yin, H.X.; Guo, Q.; et al. Total Ionizing Dose Response and Annealing Behavior of Bulk nFinFETs with ON-State Bias Irradiation. *IEEE Trans. Nucl. Sci.* **2018**, *65*, 1503–1510. [CrossRef]
7. Yakimets, D.; Bardon, M.; Garcia Jang, D.; Schuddinck, P.; Sherazi, Y.; Weckx, P.; Miyaguchi, K.; Parvais, B.; Raghavan, P.; Spessot, A.; Verkest, D.; Mocuta, A. Power aware FinFET and lateral nanosheet FET targeting for 3 nm CMOS technology. In Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017; pp. 20.4.1–20.4.4.
8. Cheng, K.; Seo, S.; Faltermeier, J.; Lu, D.; Standaert, T.; Ok, I.; Khakifirooz, A.; Vega, R.; Levin, T.; Li, J.; et al. Bottom oxidation through STI (BOTS)—A novel approach to fabricate dielectric isolated FinFETs on bulk substrates. In Proceedings of the 2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers, Honolulu, HI, USA, 9–12 June 2014; pp. 1–2.
9. Zhang, Q.; Yin, H.; Luo, J.; Yang, H.; Meng, L.; Li, Y.; Wu, Z.; Zhang, Y.; Zhang, Y.; Qin, C.; et al. FOI FinFET with ultra-low parasitic resistance enabled by fully metallic source and drain formation on isolated bulk-fin. In Proceedings of the 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 3–7 December 2016; pp. 17.13.11–17.13.14.
10. Ma, X.L.; Yin, H.X.; Hong, P.Z.; Xu, W.J. Self-Aligned Fin-On-Oxide (FOO) FinFETs for Improved SCE Immunity and Multi-V-TH Operation on Si Substrate. *ECS Solid State Lett.* **2015**, *4*, Q13–Q16. [CrossRef]
11. Hou, Z.Z.; Zhang, Q.Z.; Yin, H.X.; Xiang, J.J.; Qin, C.L.; Yao, J.X.; Gu, J. Fabrication and Characterization of p-Channel Charge Trapping Type FOI-FinFET Memory with MAHAS Structure. *ECS J. Solid State Sci. Technol.* **2017**, *6*, Q136–Q142. [CrossRef]
12. Xu, W.J.; Yin, H.X.; Ma, X.L.; Hong, P.Z.; Xu, M.; Meng, L.K. Novel 14-nm Scallop-Shaped FinFETs (S-FinFETs) on Bulk-Si Substrate. *Nanoscale Res. Lett.* **2015**, *10*, 249. [CrossRef]
13. Mertens, H.; Ritzenthaler, R.; Hikavyy, A.; Kim, M.S.; Tao, Z.; Wostyn, K.; Chew, S.A.; Keersgieter, A.D.; Mannaert, G.; Rosseel, E.; et al. Gate-all-around MOSFETs based on vertically stacked horizontal Si nanowires in a replacement metal gate process on bulk Si substrates. In Proceedings of the 2016 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 14–16 June 2016; pp. 1–2.
14. Lauer, I.; Loubet, N.; Kim, S.D.; Ott, J.A.; Mignot, S.; Venigalla, R.; Yamashita, T.; Standaert, T.; Faltermeier, J.; Basker, V.; et al. Si nanowire CMOS fabricated with minimal deviation from RMG FinFET technology showing record performance. In Proceedings of the 2015 Symposium on VLSI Technology, Kyoto, Japan, 16–18 June 2015; pp. T140–T141.
15. Zhang, Q.Z.; Yin, H.X.; Meng, L.K.; Yao, J.X.; Li, J.J.; Wang, G.L.; Li, Y.D.; Wu, Z.H.; Xiong, W.J.; Yang, H.; et al. Novel GAA Si Nanowire p-MOSFETs With Excellent Short-Channel Effect Immunity via an Advanced Forming Process. *IEEE Electron Device Lett.* **2018**, *39*, 464–467. [CrossRef]
16. Tu, H.; Zhao, H.; Wei, F.; Zhang, Q.; Du, J. Research Progress in Two-Dimensional Atomic Crystal Materials and Van der Waals Heterostructures. *Chin. J. Rare Met.* **2017**, *41*, 449–465.
17. Pan, Y.; Jia, K.P.; Huang, K.L.; Wu, Z.H.; Bai, G.B.; Yu, J.H.; Zhang, Z.H.; Zhang, Q.Z.; Yin, H.X. Near-ideal subthreshold swing MoS2 back-gate transistors with an optimized ultrathin HfO_2 dielectric layer. *Nanotechnology* **2019**, *30*, 095202. [CrossRef]
18. Brunet, L.; Fenouillet-Beranger, C.; Batude, P.; Beaurepaire, S.; Ponthenier, F.; Rambal, N.; Mazzocchi, V.; Pin, J.; Acosta-Alba, P.; Kerdiles, S.; et al. Breakthroughs in 3D Sequential technology. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018; pp. 7.2.1–7.2.4.

19. Chiarella, T.; Witters, L.; Mercha, A.; Kerner, C.; Dittrich, R.; Rakowski, M.; Ortolland, C.; Ragnarsson, L.A.; Parvais, B.; De Keersgieter, A.; et al. Migrating from planar to FinFET for further CMOS scaling: SOI or bulk? In Proceedings of the 2009 Proceedings of the European Solid State Device Research Conference (ESSCIRC'09), Athens, Greece, 14–18 September 2009; pp. 84–87.
20. Bae, G.; Bae, D.I.; Kang, M.; Hwang, S.M.; Kim, S.S.; Seo, B.; Kwon, T.Y.; Lee, T.J.; Moon, C.; Choi, Y.M.; et al. 3 nm GAA Technology featuring Multi-Bridge-Channel FET for Low Power and High Performance Applications. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018; pp. 28.7.1–28.7.4.
21. Sackinger, E.; Guggenbuhl, W. A high-swing, high-impedance MOS cascode circuit. *IEEE J. Solid-State Circuits* **1990**, *25*, 289–298. [CrossRef]
22. Radamson, H.; Thylen, L. *Monolithic Nanoscale Photonics-Electronics Integration in Silicon and other Group IV Elements*; Elsevier Science & Technology: San Diego, CA, USA, 2014.
23. Frank, D.J.; Dennard, R.H.; Nowak, E.; Solomon, P.M.; Taur, Y.; Wong, H.S.P. Device scaling limits of Si MOSFETs and their application dependencies. *Proc. IEEE* **2001**, *89*, 259–288. [CrossRef]
24. Yaegashi, H. Pattern fidelity control in Multi-patterning towards 7 nm node. In Proceedings of the 2016 IEEE 16th International Conference on Nanotechnology (IEEE-NANO), Sendai, Japan, 22–25 August 2016; pp. 452–455.
25. Jiang, J.; Chakrabarty, S.; Yu, M.F.; Ober, C.K. Metal Oxide Nanoparticle Photoresists for EUV Patterning. *J. Photopolym Sci. Technol.* **2014**, *27*, 663–666. [CrossRef]
26. Mulkens, J.; Hanna, M.; Wei, H.; Vaenkatesan, V.; Megens, H.; Slotboom, D. Overlay and Edge Placement Control Strategies for the 7-nm node using EUV and ArF lithography. In *Extreme Ultraviolet (EUV) Lithography VI*; Wood, O.R., Panning, E.M., Eds.; SPIE: San Jose, CA, USA, 2016; Volume 9422.
27. Kerkhof, M.V.D.; Jasper, H.; Levasier, L.; Peeters, R.; van Es, R.; Bosker, J.W.; Zdravkov, A.; Lenderink, E.; Evangelista, F.; Broman, P.; et al. Enabling sub-10nm node lithography: Presenting the NXE:3400B EUV scanner. Extreme Ultraviolet. *Proc. SPIE* **2017**, *10143*. [CrossRef]
28. Nagahara, S.; Carcasi, M.; Shiraishi, G.; Nakagawa, H.; Dei, S.; Shiozawa, T.; Nafus, K.; De Simone, D.; Vandenberghe, G.; Stock, H.J.; Küchler, B. Photosensitized Chemically Amplified Resist (PSCAR) 2.0 for high-throughput and high-resolution EUV lithography: Dual photosensitization of acid generation and quencher decomposition by flood exposure. *Proc. SPIE* **2017**, *10146*. [CrossRef]
29. Capelli, R.; Hellweg, D.; Dietzel, M.; Koch, M.; Wolke, C.; Kersteen, G. Aerial image based metrology of EUV masks: Recent achievements, status and outlook for the AIMS (TM) EUV platform. In *Extreme Ultraviolet (EUV) Lithography IX*; Goldberg, K.A., Ed.; SPIE: San Jose, CA, USA, 2018; Volume 10583.
30. Wojdyla, A.; Benk, M.P.; Naulleau, P.P.; Goldberg, K.A. EUV photolithography mask inspection using Fourier ptychography. In *Image Sensing Technologies: Materials, Devices, Systems, and Applications V*; Dhar, N.K., Dutta, A.K., Eds.; SPIE: Orlando, FL, USA, 2018; Volume 10656.
31. Turkot, B.; Carson, S.L.; Lio, A.N.; Liang, T.; Phillips, M.; McCool, B.; Stenehjem, E.; Crimmins, T.; Zhang, G.J.; Sivakumar, S. EUV Progress Toward HVM Readiness. In *Extreme Ultraviolet (EUV) Lithography VII*; Panning, E.M., Goldberg, K.A., Eds.; SPIE: San Jose, CA, USA, 2016; Volume 9776.
32. Levinson, H.J.; Brunner, T.A. Current Challenges and Opportunities for EUV Lithography. In *International Conference on Extreme Ultraviolet Lithography 2018*; Ronse, K.G., Hendrickx, E., Naulleau, P.P., Gargini, P.A., Itani, T., Eds.; SPIE: Monterey, CA, USA, 2018; Volume 10809.
33. Li, L.; Liu, X.; Pal, S.; Wang, S.L.; Ober, C.K.; Giannelis, E.P. Extreme ultraviolet resist materials for sub-7 nm patterning. *Chem. Soc. Rev.* **2017**, *46*, 4855–4866. [CrossRef] [PubMed]
34. Jan, C.; Bhattacharya, U.; Brain, R.; Choi, S.; Curello, G.; Gupta, G.; Hafez, W.; Jang, M.; Kang, M.; Komeyli, K.; et al. A 22 nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications. In Proceedings of the 2012 International Electron Devices Meeting, San Francisco, CA, USA, 10–13 December 2012; pp. 3.1.1–3.1.4.
35. Jan, C.; Agostinelli, M.; Buehler, M.; Chen, Z.; Choi, S.; Curello, G.; Deshpande, H.; Gannavaram, S.; Hafez, W.; Jalan, U.; et al. A 32 nm SoC platform technology with 2nd generation high-k/metal gate transistors optimized for ultra low power, high performance, and high density product applications. In Proceedings of the 2009 IEEE International Electron Devices Meeting (IEDM), Baltimore, MD, USA, 7–9 December 2009; pp. 1–4.
36. Radamson, H.H.; Zhang, Y.B.; He, X.B.; Cui, H.S.; Li, J.J.; Xiang, J.J.; Liu, J.B.; Gu, S.H.; Wang, G.L. The Challenges of Advanced CMOS Process from 2D to 3D. *Appl. Sci.* **2017**, *7*, 1047. [CrossRef]

37. International Roadmap for Devices and Systems (IRDS™) 2017 Edition. Available online: https://irds.ieee.org/roadmap-2017 (accessed on 4 April 2019).
38. Wu, H.; Gluschenkov, O.; Tsutsui, G.; Niu, C.; Brew, K.; Durfee, C.; Prindle, C.; Kamineni, V.; Mochizuki, S.; Lavoie, C.; et al. Parasitic Resistance Reduction Strategies for Advanced CMOS FinFETs Beyond 7 nm. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018; pp. 35.4.1–35.4.4.
39. Kise, N.; Kinoshita, H.; Yukimachi, A.; Kanazawa, T.; Miyamoto, Y. Fin width dependence on gate controllability of InGaAs channel FinFETs with regrown source/drain. *Solid-State Electron.* **2016**, *126*, 92–95. [CrossRef]
40. Matsukawa, T.; Liu, Y.; Endo, K.; uchi, S.O.; Masahara, M. Variability origins of FinFETs and perspective beyond 20 nm node. In Proceedings of the IEEE 2011 International SOI Conference, Tempe, AZ, USA, 3–6 October 2011; pp. 1–28.
41. Kavalieros, J.; Doyle, B.; Datta, S.; Dewey, G.; Doczy, M.; Jin, B.; Lionberger, D.; Metz, M.; Rachmady, W.; Radosavljevic, M.; et al. Tri-Gate Transistor Architecture with High-k Gate Dielectrics, Metal Gates and Strain Engineering. In Proceedings of the Digest of Technical Papers—Symposium on VLSI Technology, Honolulu, HI, USA, 13–15 June 2006; pp. 50–51.
42. Jan, C.; Al-amoody, F.; Chang, H.; Chang, T.; Chen, Y.; Dias, N.; Hafez, W.; Ingerly, D.; Jang, M.; Karl, E.; et al. A 14 nm SoC platform technology featuring 2nd generation Tri-Gate transistors, 70 nm gate pitch, 52 nm metal pitch, and 0.0499 um^2 SRAM cells, optimized for low power, high performance and high density SoC products. In Proceedings of the 2015 Symposium on VLSI Circuits (VLSI Circuits), Kyoto, Japan, 17–19 June 2015; pp. T12–T13.
43. Jacob, A.P.; Xie, R.; Sung, M.G.; Liebmann, L.; Lee, R.T.P.; Taylor, B. Scaling Challenges for Advanced CMOS Devices. *Int. J. High Speed Electron. Syst.* **2017**, *26*, 2–76. [CrossRef]
44. Veloso, A.; De Keersgieter, A.; Matagne, P.; Horiguchi, N.; Collaert, N. Advances on doping strategies for triple-gate finFETs and lateral gate-all-around nanowire FETs and their impact on device performance. *Mater. Sci. Semicond. Process.* **2017**, *62*, 2–12. [CrossRef]
45. Current, M.I. Ion implantation of advanced silicon devices: Past, present and future. *Mater. Sci. Semicond. Process.* **2017**, *62*, 13–22. [CrossRef]
46. Ghani, T.; Armstrong, M.; Auth, C.; Bost, M.; Charvat, P.; Glass, G.; Hoffmann, T.; Johnson, K.; Kenyon, C.; Klaus, J.; et al. A 90 nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors. In Proceedings of the IEEE International Electron Devices Meeting 2003, Washington, DC, USA, 8–10 December 2003; pp. 11.16.11–11.16.13.
47. Bai, P.; Auth, C.; Balakrishnan, S.; Bost, M.; Brain, R.; Chikarmane, V.; Heussner, R.; Hussein, M.; Hwang, J.; Ingerly, D.; et al. A 65 nm logic technology featuring 35 nm gate lengths, enhanced channel strain, 8 Cu interconnect layers, low-k ILD and 0.57 μm^2 SRAM cell. In Proceedings of the IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004, San Francisco, CA, USA, 13–15 December 2004; pp. 657–660. [CrossRef]
48. Jan, C.H.; Bai, P.; Biswas, S.; Buehler, M.; Chen, Z.P.; Curello, G.; Gannavaram, S.; Hafez, W.; He, J.; Hicks, J.; et al. A 45 nm low power system-on-chip technology with dual gate (logic and I/O) high-k/metal gate strained silicon transistors. In Proceedings of the 2008 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2008; pp. 1–4. [CrossRef]
49. Natarajan, S.; Armstrong, M.; Bost, M.; Brain, R.; Brazier, M.; Chang, C.-H.; Chikarmane, V.; Childs, M.; Deshpande, H.; Dev, K.; et al. A 32 nm logic technology featuring 2nd-generation high-k+ metal-gate transistors, enhanced channel strain and 0.171 μm^2 SRAM cell size in a 291 Mb array. In Proceedings of the 2008 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2008; pp. 1–3. [CrossRef]
50. Thompson, S.; Sun, G.; Wu, K.; Lim, J.; Nishida, T. Key differences for process-induced uniaxial vs. substrate-induced biaxial stressed Si and Ge channel MOSFETs. In Proceedings of the Electron Devices Meeting, 2004, IEDM Technical Digest, San Francisco, CA, USA, 13–15 December 2004; pp. 221–224.
51. Ohta, H.; Kim, Y.; Shimamune, Y.; Sakuma, T.; Hatada, A.; Katakami, A.; Soeda, T.; Kawamura, K.; Kokura, H.; Morioka, H.; et al. High performance 30 nm gate bulk CMOS for 45 nm node with/spl Sigma/-shaped SiGe-SD. In Proceedings of the IEEE International Electron Devices Meeting, 2005, IEDM Technical Digest, Washington, DC, USA, 5 December 2005; pp. 247–250.

52. Tamura, N.; Shimamune, Y. 45 nm CMOS technology with low temperature selective epitaxy of SiGe. *Appl. Surf. Sci.* **2008**, *254*, 6067–6071. [CrossRef]
53. Qin, C.L.; Yin, H.X.; Wang, G.L.; Hong, P.Z.; Ma, X.L.; Cui, H.S.; Lu, Y.H.; Meng, L.K.; Yin, H.Z.; Zhong, H.C.; et al. Study of sigma-shaped source/drain recesses for embedded-SiGe pMOSFETs. *Microelectron. Eng.* **2017**, *181*, 22–28. [CrossRef]
54. Vescan, L.; Grimm, K.; Dieker, C. Facet investigation in selective epitaxial growth of Si and SiGe on (001) Si for optoelectronic devices. *J. Vac. Sci. Technol. B* **1998**, *16*, 1549–1554. [CrossRef]
55. Dutartre, D.; Talbot, A. Facet propagation in Si and SiGe epitaxy or etching. *ECS Trans.* **2006**, *3*, 473–487. [CrossRef]
56. Mujumdar, S.; Maitra, K.; Datta, S. Layout-Dependent Strain Optimization for p-Channel Trigate Transistors. *IEEE Trans. Electron Devices* **2012**, *59*, 72–78. [CrossRef]
57. Hallstedt, J.; Kolahdouz, M.; Ghandi, R.; Radamson, H.H. Pattern dependency in selective epitaxy of B-doped SiGe layers for advanced metal oxide semiconductor field effect transistors. *J. Appl. Phys.* **2008**, *103*, 054907. [CrossRef]
58. Radamson, H.H.; Kolahdouz, M. Selective epitaxy growth of Si1-x Gex layers for MOSFETs and FinFET. *J. Mater. Sci. Mater. Electron.* **2015**, *26*, 4584–4603. [CrossRef]
59. Wang, G.L.; Moeen, M.; Abedin, A.; Xu, Y.F.; Luo, J.; Guo, Y.L.; Qin, C.L.; Tang, Z.Y.; Yin, H.Z.; Li, J.F.; et al. Impact of pattern dependency of SiGe layers grown selectively in source/drain on the performance of 22 nm node pMOSFETs. *Solid-State Electron.* **2015**, *114*, 43–48. [CrossRef]
60. Qin, C.L.; Wang, G.L.; Kolahdouz, M.; Luo, J.; Yin, H.X.; Yang, P.; Li, J.F.; Zhu, H.L.; Chao, Z.; Ye, T.C.; et al. Impact of pattern dependency of SiGe layers grown selectively in source/drain on the performance of 14 nm node FinFETs. *Solid-State Electron.* **2016**, *124*, 10–15. [CrossRef]
61. Wang, G.; Luo, J.; Qin, C.; Cui, H.; Liu, J.; Jia, K.; Li, J.; Yang, T.; Li, J.; Yin, H.; et al. Integration of Selective Epitaxial Growth of SiGe/Ge Layers in 14nm Node FinFETs. *ECS Trans.* **2016**, *75*, 273–279. [CrossRef]
62. Loo, R.; Hikavyy, A.Y.; Witters, L.; Schulze, A.; Arimura, H.; Cott, D.; Mitard, J.; Porret, C.; Mertens, H.; Ryan, P.; et al. Processing Technologies for Advanced Ge Devices. *ECS J. Solid State Sci. Technol.* **2016**, *6*, P14–P20. [CrossRef]
63. Radamson, H.H.; Luo, J.; Simeon, E.; Chao, Z. *Past, Present and Future of CMOS*; Elsevier: Duxford, UK, 2018.
64. Wang, G.L.; Abedin, A.; Moeen, M.; Kolandouz, M.; Luo, J.; Guo, Y.L.; Chen, T.; Yin, H.X.; Zhu, H.L.; Li, J.F.; et al. Integration of highly-strained SiGe materials in 14 nm and beyond nodes FinFET technology. *Solid-State Electron.* **2015**, *103*, 222–228. [CrossRef]
65. Wan, G.X.; Wang, G.L.; Zhu, H.L. Hetero-Epitaxy and Self-Adaptive Stressor Based on Freestanding Fin for the 10 nm Node and Beyond. *Chin. Phys. Lett.* **2017**, *34*, 4. [CrossRef]
66. Wang, G.L.; Luo, J.; Qin, C.L.; Liang, R.R.; Xu, Y.F.; Liu, J.B.; Li, J.F.; Yin, H.X.; Yan, J.; Zhu, H.L.; et al. Integration of Highly Strained SiGe in Source and Drain with HK and MG for 22 nm Bulk PMOS Transistors. *Nanoscale Res. Lett.* **2017**, *12*, 078502. [CrossRef]
67. Han, K.; Tang, S.; Rockwell, T.; Godet, L.; Persing, H.; Campbell, C.; Salimian, S. A novel plasma-based technique for conformal 3D FINFET doping. In Proceedings of the 2012 12th International Workshop on Junction Technology, Shanghai, China, 14–15 May 2012; pp. 35–37.
68. Felch, S.; Hobbs, C.; Barnett, J.; Etienne, H.; Duchaine, J.; Rodgers, M.; Bennett, S.; Torregrosa, F.; Spiegel, Y.; Roux, L. Plasma doping of silicon fin structures. In Proceedings of the 11th International Workshop on Junction Technology (IWJT), Kyoto, Japan, 9–10 June 2011; pp. 22–25.
69. Linford, M.R.; Chidsey, C.E.D. Alkyl monolayers covalently bonded to silicon surfaces. *J. Am. Chem. Soc.* **1993**, *115*, 12631–12632. [CrossRef]
70. Ye, L.; Pujari, S.P.; Zuilhof, H.; Kudernac, T.; de Jong, M.P.; van der Wiel, W.G.; Huskens, J. Controlling the Dopant Dose in Silicon by Mixed-Monolayer Doping. *ACS Appl. Mater. Interfaces* **2015**, *7*, 3231–3236. [CrossRef]
71. Sieval, A.B.; Vleeming, V.; Zuilhof, H.; Sudholter, E.J.R. An improved method for the preparation of organic monolayers of 1-alkenes on hydrogen-terminated silicon surfaces. *Langmuir* **1999**, *15*, 8288–8291. [CrossRef]
72. Ford, A.C.; Ho, J.C.; Chueh, Y.; Javey, A. Monolayer doping and diameter-dependent electron mobility assessment of nanowires. In Proceedings of the 2009 IEEE International Conference on IC Design and Technology, Austin, TX, USA, 18–20 May 2009; pp. 223–227.

73. Ok, I.; Ang, K.; Hobbs, C.; Baek, R.H.; Kang, C.Y.; Snow, J.; Nunan, P.; Nadahara, S.; Kirsch, P.D.; Jammy, R. Conformal, low-damage shallow junction technology (Xj~5 nm) with optimized contacts for FinFETs as a Solution Beyond 14 nm Node. In Proceedings of the 2012 12th International Workshop on Junction Technology, Shanghai, China, 14–15 May 2012; pp. 29–34.
74. Ho, J.C.; Yerushalmi, R.; Jacobson, Z.A.; Fan, Z.; Alley, R.L.; Javey, A. Controlled nanoscale doping of semiconductors via molecular monolayers. *Nat. Mater.* **2008**, *7*, 62–67. [CrossRef]
75. Long, B.; Verni, G.A.; Connell, J.O.; Holmes, J.; Shayesteh, M.; Connell, D.O.; Duffy, R. Molecular Layer Doping: Non-destructive doping of silicon and germanium. In Proceedings of the 2014 20th International Conference on Ion Implantation Technology (IIT), Portland, OR, USA, 26 June–4 July 2014; pp. 1–4.
76. Kim, Y.S.; Kown, H. Ultra-shallow junction formation on 3D silicon and germanium device structures by ion energy decoupled plasma doping. In Proceedings of the 2017 17th International Workshop on Junction Technology (IWJT), Uji, Japan, 1–2 June 2017; pp. 62–65.
77. Takeuchi, H.; King, T.J. Scaling limits of hafnium-silicate films for gate-dielectric applications. *Appl. Phys. Lett.* **2003**, *83*, 788–790. [CrossRef]
78. Seong, N.J.; Yoon, S.G.; Yeom, S.J.; Woo, H.K.; Kil, D.S.; Roh, J.S.; Sohn, H.C. Effect of nitrogen incorporation on improvement of leakage properties in high-k HfO_2 capacitors treated by N-2-plasma. *Appl. Phys. Lett.* **2005**, *87*. [CrossRef]
79. Zhao, C.; Witters, T.; Brijs, B.; Bender, H.; Richard, O.; Caymax, M.; Heeg, T.; Schubert, J.; Afanas'ev, V.V.; Stesmans, A.; et al. Ternary rare-earth metal oxide high-k layers on silicon oxide. *Appl. Phys. Lett.* **2005**, *86*. [CrossRef]
80. Barlage, D.; Arghavani, R.; Dewey, G.; Doczy, M.; Doyle, B.; Kavalieros, J.; Murthy, A.; Roberds, B.; Stokley, P.; Chau, R. High-frequency response of 100 nm integrated CMOS transistors with high-K gate dielectrics. In Proceedings of the International Electron Devices Meeting. Technical Digest, Washington, DC, USA, 2–5 December 2001; pp. 10.16.11–10.16.14.
81. Packan, P.; Akbar, S.; Armstrong, M.; Bergstrom, D.; Brazier, M.; Deshpande, H.; Dev, K.; Ding, G.; Ghani, T.; Golonzka, O.; et al. High performance 32 nm logic technology featuring 2nd generation high-k + metal gate transistors. In Proceedings of the 2009 IEEE International Electron Devices Meeting (IEDM), Baltimore, MD, USA, 7–9 December 2009; pp. 1–4.
82. Triyoso, D.H.; Gregory, R.; Schaeffer, J.K.; Werho, D.; Li, D.; Marcus, S.; Wilk, G.D. Atomic layer deposited TaC(y) metal gates: Impact on microstructure, electrical properties, and work function on HfO(2) high-k dielectrics. *J. Appl. Phys.* **2007**, *102*, 104509. [CrossRef]
83. Cho, G.H.; Rhee, S.W. Plasma-Enhanced Atomic Layer Deposition of TaCxNy Films with tert-Butylimido Tris-diethylamido Tantalum and Methane/Hydrogen Gas. *Electrochem. Solid State Lett.* **2010**, *13*, H426–H427. [CrossRef]
84. Kim, C.K.; Ahn, H.J.; Moon, J.M.; Lee, S.; Moon, D.I.; Park, J.S.; Cho, B.J.; Choi, Y.K.; Lee, S.H. Temperature control for the gate workfunction engineering of TiC film by atomic layer deposition. *Solid-State Electron.* **2015**, *114*, 90–93. [CrossRef]
85. Zonensain, O.; Fadida, S.; Fisher, I.; Gao, J.W.; Chattopadhyay, K.; Harm, G.; Mountsier, T.; Danek, M.; Eizenberg, M. Work function tuning of plasma-enhanced atomic layer deposited WCxNy electrodes for metal/oxide/semiconductor devices. *Appl. Phys. Lett.* **2015**, *106*, 082107. [CrossRef]
86. Ahn, H.J.; Moon, J.; Koh, S.; Seo, Y.; Kim, C.; Rho, I.C.; Kim, C.H.; Hwang, W.S.; Cho, B.J. Very Low-Work-Function ALD-Erbium Carbide (ErC2) Metal Electrode on High-K Dielectrics. *IEEE Trans. Electron Devices* **2016**, *63*, 2858–2863. [CrossRef]
87. Xiang, J.J.; Zhang, Y.B.; Li, T.T.; Wang, X.L.; Gao, J.F.; Yin, H.X.; Li, J.F.; Wang, W.W.; Ding, Y.Q.; Xu, C.Y.; et al. Investigation of thermal atomic layer deposited TiAlX (X = N or C) film as metal gate. *Solid-State Electron.* **2016**, *122*, 64–69. [CrossRef]
88. Xiang, J.J.; Li, T.T.; Zhang, Y.B.; Wang, X.L.; Gao, J.F.; Cui, H.S.; Yin, H.X.; Li, J.F.; Wang, W.W.; Ding, Y.Q.; et al. Investigation of TiAlC by Atomic Layer Deposition as N Type Work Function Metal for FinFET. *ECS J. Solid State Sci. Technol.* **2015**, *4*, P441–P444. [CrossRef]
89. Xiang, J.J.; Ding, Y.Q.; Du, L.Y.; Xu, C.Y.; Li, T.T.; Wang, X.L.; Li, J.F.; Zhao, C. Investigation of N Type Metal TiAlC by Thermal Atomic Layer Deposition Using $TiCl_4$ and TEA as Precursors. *ECS J. Solid State Sci. Technol.* **2016**, *5*, P299–P303. [CrossRef]

90. Xiang, J.J.; Li, T.T.; Wang, X.L.; Du, L.Y.; Ding, Y.Q.; Wang, W.W.; Li, J.F.; Zhao, C. Thermal Atomic Layer Deposition of TaAlC with TaCl5 and TMA as Precursors. *ECS J. Solid State Sci. Technol.* **2016**, *5*, P633–P636. [CrossRef]
91. Xiang, J.J.; Wang, X.L.; Li, T.T.; Gao, J.F.; Han, K.; Yu, J.H.; Wang, W.W.; Li, J.F.; Zhao, C. Investigation of Thermal Atomic Layer Deposited TaAlC with Low Effective Work-Function on HfO_2 Dielectric Using TaCl5 and TEA as Precursors. *ECS J. Solid State Sci. Technol.* **2017**, *6*, P38–P41. [CrossRef]
92. Khan, A.I.; Chatterjee, K.; Wang, B.; Drapcho, S.; You, L.; Serrao, C.; Bakaul, S.R.; Ramesh, R.; Salahuddin, S. Negative capacitance in a ferroelectric capacitor. *Nat. Mater.* **2015**, *14*, 182–186. [CrossRef] [PubMed]
93. Wang, G.L.; Xu, Q.; Yang, T.; Xiang, J.J.; Xu, J.; Gao, J.F.; Li, C.L.; Li, J.F.; Yan, J.; Chen, D.P.; et al. Application of Atomic Layer Deposition Tungsten (ALD W) as Gate Filling Metal for 22 nm and Beyond Nodes CMOS Technology. *ECS J. Solid State Sci. Technol.* **2014**, *3*, P82–P85. [CrossRef]
94. Lemaire, P.C.; King, M.; Parsons, G.N. Understanding inherent substrate selectivity during atomic layer deposition: Effect of surface preparation, hydroxyl density, and metal oxide composition on nucleation mechanisms during tungsten ALD. *J. Chem. Phys.* **2017**, *146*, 052811. [CrossRef] [PubMed]
95. Kalanyan, B.; Lemaire, P.C.; Atanasov, S.E.; Ritz, M.J.; Parsons, G.N. Using Hydrogen to Expand the Inherent Substrate Selectivity Window During Tungsten Atomic Layer Deposition. *Chem. Mater.* **2016**, *28*, 117–126. [CrossRef]
96. Pai, C.F.; Liu, L.Q.; Li, Y.; Tseng, H.W.; Ralph, D.C.; Buhrman, R.A. Spin transfer torque devices utilizing the giant spin Hall effect of tungsten. *Appl. Phys. Lett.* **2012**, *101*, 122404. [CrossRef]
97. Neumann, L.; Meier, D.; Schmalhorst, J.; Rott, K.; Reiss, G.; Meinert, M. Temperature dependence of the spin Hall angle and switching current in the nc-W(O)/CoFeB/MgO system with perpendicular magnetic anisotropy. *Appl. Phys. Lett.* **2016**, *109*, 142405. [CrossRef]
98. Wang, G.L.; Luo, J.; Liu, J.B.; Yang, T.; Xu, Y.F.; Li, J.F.; Yin, H.X.; Yan, J.; Zhu, H.L.; Zhao, C.; et al. pMOSFETs Featuring ALD W Filling Metal Using SiH4 and B2H6 Precursors in 22 nm Node CMOS Technology. *Nanoscale Res. Lett.* **2017**, *12*, 306. [CrossRef]
99. Fabreguette, F.H.; Sechrist, Z.A.; Elam, J.W.; George, S.M. Quartz crystal microbalance study of tungsten atomic layer deposition using WF6 and Si2H6. *Thin Solid Films* **2005**, *488*, 103–110. [CrossRef]
100. Elam, J.W.; Nelson, C.E.; Grubbs, R.K.; Nelson, C.E. Nucleation and Growth During Tungsten Atomic Layer Deposition on Oxide Surfaces. *MRS Online Proc. Libr. Arch.* **2001**, *386*, 41–52.
101. Luoh, T.; Su, C.T.; Yang, T.H.; Chen, K.C.; Lu, C.Y. Advanced tungsten plug process for beyond nanometer technology. *Microelectron. Eng.* **2008**, *85*, 1739–1747. [CrossRef]
102. Kim, C.H.; Rho, I.C.; Kim, S.H.; Sohn, Y.S.; Kang, H.S.; Kim, H.J. Improvement of Adhesion Performances of CVD-W Films Deposited on B2H6-Based ALD-W Nucleation Layer. *Electrochem. Solid State Lett.* **2009**, *12*, H80–H83. [CrossRef]
103. Kim, C.; Rho, I.; Eun, B.; Kim, H.; Jin, S.; Kang, H. Electrical performances of low resistive W buried gate using B2H6-reduced W nucleation layer technology for 30nm-based DRAM devices. In Proceedings of the 2011 IEEE International Interconnect Technology Conference, Dresden, Germany, 8–12 May 2011; pp. 1–3.
104. Xu, Q.; Luo, J.; Wang, G.L.; Yang, T.; Li, J.F.; Ye, T.C.; Chen, D.P.; Zhao, C. Application of ALD W films as gate filling metal in 22 nm HKMG-last integration: Evaluation and improvement of the adhesion in CMP process. *Microelectron. Eng.* **2015**, *137*, 43–46. [CrossRef]
105. Yang, M.D.; Aarnink, A.A.I.; Schmitz, J.; Kovalgin, A.Y. Low-resistivity alpha-phase tungsten films grown by hot-wire assisted atomic layer deposition in high-aspect-ratio structures. *Thin Solid Films* **2018**, *646*, 199–208. [CrossRef]
106. Kim, S.H.; Kim, J.T.; Kwak, N.; Kim, J.; Yoon, T.S.; Sohn, H. Effects of phase of underlying W film on chemical vapor deposited-W film growth and applications to contact-plug and bit line processes for memory devices. *J. Vac. Sci. Technol. B* **2007**, *25*, 1574–1580. [CrossRef]
107. Yang, H.S.; Malik, R.; Narasimha, S.; Li, Y.; Divakaruni, R.; Agnello, P.; Allen, S.; Antreasyan, A.; Arnold, J.C.; Bandy, K.; et al. Dual stress liner for high performance sub-45nm gate length SOI CMOS manufacturing. In Proceedings of the IEDM Technical Digest, IEEE International Electron Devices Meeting, 2004, San Francisco, CA, USA, 13–15 December 2004; pp. 1075–1077.

108. Nguyen, P.; Barraud, S.; Tabone, C.; Gaben, L.; Cassé, M.; Glowacki, F.; Hartmann, J.; Samson, M.; Maffini-Alvaro, V.; Vizioz, C.; et al. Dual-channel CMOS co-integration with Si NFET and strained-SiGe PFET in nanowire device architecture featuring sub-15nm gate length. In Proceedings of the 2014 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2014; pp. 16.12.11–16.12.14.
109. Jing, W. Strained Silicon—A Technology to Extend Moore's Law. *Microelectronics* **2008**, *38*, 50–56.
110. Orain, S.; Fiori, V.; Villanueva, D.; Dray, A.; Ortolland, C. Method for Managing the Stress Due to the Strained Nitride Capping Layer in MOS Transistors. *IEEE Trans. Electron Devices* **2007**, *54*, 814–821. [CrossRef]
111. Varadarajan, B.; Sims, J.; Singhal, A.; Christensen, M.; Jiang, G.; Ilcisir, K.; Shrinivasan, K.; Ayoub, M.; Dharmadhikari, V. The development of high stress silicon nitride film used in strain silicon. *Integr. Circuit Appl.* **2006**, *2*, 36–39.
112. Wang, J. The application and forecast of high stress silicon nitride films. *Integr. Circuit Appl.* **2008**, *4*, 63–64.
113. Kim, D.; Krishnamohan, T.; Smith, L.; Wong, H.S.P.; Saraswat, K.C. Band to band tunneling study in high mobility materials: III-V, Si, Ge and strained SiGe. In Proceedings of the 2007 65th Annual Device Research Conference, Notre Dame, IN, USA, 18–20 June 2007; pp. 57–58. [CrossRef]
114. Oktyabrsky, S.; Ye, P.D. *Fundamentals of III-V Semiconductor MOSFETs*; Springer: New York, NY, USA, 2010; pp. 1–445. [CrossRef]
115. Kobayashi, M.; Thareja, G.; Ishibashi, M.; Sun, Y.; Griffin, P.; McVittie, J.; Pianetta, P.; Saraswat, K.; Nishi, Y. Radical oxidation of germanium for interface gate dielectric GeO_2 formation in metal-insulator-semiconductor gate stack. *J. Appl. Phys.* **2009**, *106*, 104117. [CrossRef]
116. Si-Silicon Electrical Properties. Available online: http://www.ioffe.ru/SVA/NSM/Semicond/Si/electric.html (accessed on 30 December 2018).
117. Kuhn, K.J. Considerations for Ultimate CMOS Scaling. *IEEE Trans. Electron Devices* **2012**, *59*, 1813–1828. [CrossRef]
118. Hussain, M.M.; Shamiryan, D.; Paraschiv, V.; Sano, K.; Reinhardt, K. Cleaning Challenges of High-κ/Metal Gate Structures. In *Handbook of Cleaning in Semiconductor Manufacturing*; Scrivener Publishing LLC.: Salem, MA, USA, 2011; pp. 249–251. [CrossRef]
119. Huff, H.R.; Richter, C.A.; Green, M.L.; Lucovsky, G.; Hattori, T. *Ultrathin SiO_2 and High-K Materials for ULSI Gate Dielectrics*; Materials Research Society: Warrendale, PA, USA, 1999; Volume 567.
120. Mertens, H.; Ritzenthaler, R.; Arimura, H.; Franco, J.; Sebaai, F.; Hikavyy, A.; Pawlak, B.J.; Machkaoutsan, V.; Devriendt, K.; Tsvetanova, D.; et al. Si-cap-free SiGe p-channel FinFETs and gate-all-around transistors in a replacement metal gate process: Interface trap density reduction and performance improvement by high-pressure deuterium anneal. In Proceedings of the 2015 Symposium on VLSI Technology (VLSI Technology), Kyoto, Japan, 16–18 June 2015; pp. T142–T143.
121. Destefanis, V.; Hartmann, J.M.; Borel, S.; Bensahel, D. High pressure in situ HCl etching of Si(1-x)Ge(x) versus Si for advanced devices. *Semicond. Sci. Technol.* **2008**, *23*, 105019. [CrossRef]
122. Wieser, U.; Iamundo, D.; Kunze, U.; Hackbarth, T.; Konig, U. Nanoscale patterning of Si/SiGe heterostructures by electron-beam lithography and selective wet-chemical etching. *Semicond. Sci. Technol.* **2000**, *15*, 862–867. [CrossRef]
123. Chang, G.K.; Carns, T.K.; Rhee, S.S.; Wang, K.L. Selective etching of SiGe on SiGe/Si heterostructures. *J. Electrochem. Soc.* **1991**, *138*, 202–204. [CrossRef]
124. Carns, T.K.; Tanner, M.O.; Wang, K.L. Chemical Etching of Si1-Xgex In Hf-H_2O_2-CH_3COOH. *J. Electrochem. Soc.* **1995**, *142*, 1260–1266.
125. Seidel, H.; Csepregi, L.; Heuberger, A.; Baumgartel, H. Anisotropic etching of crystalline silicon in alkaline solutions I. Orientation dependence and behavior of passivation layers. *J. Electrochem. Soc.* **1990**, *137*, 3612–3626. [CrossRef]
126. Wang, F.; Shi, Y.; Liu, J.L.; Lu, Y.; Gu, S.L.; Zheng, Y.D. Highly selective chemical etching of Si vs. Si1-xGex using NH4OH solution. *J. Electrochem. Soc.* **1997**, *144*, L37–L39. [CrossRef]
127. Wostyn, K.; Sebai, F.; Rip, J.; Mertens, H.; Witters, L.; Loo, R.; Hikavyy, A.; Milenin, A.; Horiguchi, N.; Collaert, N.; et al. Selective Etch of Si and SiGe for Gate All-Around Device Architecture. *ECS Trans.* **2015**, *69*, 147–152. [CrossRef]
128. Ahles, C.F.; Choi, J.Y.; Wolf, S.; Kummel, A.C. Selective Etching of Silicon in Preference to Germanium and Si0.5Ge0.5. *ACS Appl. Mater. Interfaces* **2017**, *9*, 20947–20954. [CrossRef]

129. Kil, Y.H.; Yang, J.-H.; Kang, S.; Jeong, T.S.; Kim, T.S.; Shim, K.-H. Selective Chemical Wet Etching of Si0.8Ge0.2/Si Multilayer. *J. Semicond. Technol. Sci.* **2013**, *13*, 668–675. [CrossRef]
130. Liu, W.D.; Lee, Y.C.; Sekiguchi, R.; Yoshida, Y.; Komori, K.; Wostyn, K.; Sebaai, F.; Holsteyns, F. Selective Wet Etching in Fabricating SiGe and Ge Nanowires for Gate-all-Around MOSFETs. *Solid State Phenom.* **2018**, *282*, 101–106. [CrossRef]
131. Bogumilowicz, Y.; Hartmann, J.M.; Truche, R.; Campidelli, Y.; Rolland, G.; Billon, T. Chemical vapour etching of Si, SiGe and Ge with HCl; applications to the formation of thin relaxed SiGe buffers and to the revelation of threading dislocations. Semicond. *Sci. Technol.* **2004**, *20*, 127. [CrossRef]
132. Witters, L.; Arimura, H.; Sebaai, F.; Hikavyy, A.; Milenin, A.P.; Loo, R.; Keersgieter, A.D.; Eneman, G.; Schram, T.; Wostyn, K.; et al. Strained Germanium Gate-All-Around pMOS Device Demonstration Using Selective Wire Release Etch Prior to Replacement Metal Gate Deposition. *IEEE Trans. Electron Devices* **2017**, *64*, 4587–4593. [CrossRef]
133. Sebaai, F.; Witters, L.; Holsteyns, F.; Wostyn, K.; Rip, J.; Yukifumi, Y.; Lieten, R.R.; Bilodeau, S.; Cooper, E. Wet Selective SiGe Etch to Enable Ge Nanowire Formation. *Solid State Phenom.* **2016**, *255*, 3–7. [CrossRef]
134. Koyama, K.; Hiroi, M.; Tatsumi, T.; Hirayama, H. Etching characteristics of $Si_{1-x}Ge_x$ alloy in ammoniac wet cleaning. *Appl. Phys. Lett.* **1990**, *57*, 2202–2204. [CrossRef]
135. Bloem, J.; van Vessem, J.C. Etching Ge with Mixtures of HF-H_2O_2-H_2O. *J. Electrochem. Soc.* **1962**, *109*, 33–36. [CrossRef]
136. Markov, I.L. Limits on fundamental limits to computation. *Nature* **2014**, *512*, 147–154. [CrossRef]
137. Edelstein, D.; Heidenreich, J.; Goldblatt, R.; Cote, W.; Uzoh, C.; Lustig, N.; Roper, P.; McDevitt, T.; Motsiff, W.; Simon, A.; et al. Full Copper Wiring in a Sub-0.25 µm CMOS ULSI Technology. In Proceedings of the International Electron Devices Meeting, IEDM Technical Digest, Washington, DC, USA, 10 December 1997; pp. 773–776.
138. Hung, R.; Park, J.H.; Ha, T.H.; Lee, M.; Hou, W.; Lei, J.; Bakke, J.R.; Sharma, S.; Sharma, K.R.; Kim, N.S.; et al. Extreme Contact Scaling with Advanced Metallization of Cobalt. In Proceedings of the 2018 IEEE International Interconnect Technology Conference (IITC), Santa Clara, CA, USA, 4–7 June 2018; pp. 30–32.
139. Bekiaris, N.; Wu, Z.; Ren, H.; Naik, M.; Park, J.H.; Lee, M.; Ha, T.H.; Hou, W.; Bakke, J.R.; Gage, M.; et al. Cobalt fill for advanced interconnects. In Proceedings of the 2017 IEEE International Interconnect Technology Conference (IITC), Hsinchu, Taiwan, 16–18 May 2017; pp. 1–3.
140. Zhang, W.; Brongersma, S.H.; Li, Z.; Li, D.; Richard, O.; Maex, K. Analysis of the size effect in electroplated fine copper wires and a realistic assessment to model copper resistivity. *J. Appl. Phys.* **2007**, *101*, 063703. [CrossRef]
141. Wen, L.G.; Roussel, P.; Pedreira, O.V.; Briggs, B.; Groven, B.; Dutta, S.; Popovici, M.I.; Heylen, N.; Ciofi, I.; Vanstreels, K.; et al. Atomic Layer Deposition of Ruthenium with TiN Interface for Sub-10 nm Advanced Interconnects beyond Copper. *ACS Appl. Mater. Interfaces* **2016**, *8*, 26119–26125. [CrossRef]
142. Veen, M.H.v.d.; Heyler, N.; Pedreira, O.V.; Ciofi, I.; Decoster, S.; Gonzalez, V.V.; Jourdan, N.; Struyf, H.; Croes, K.; Wilson, C.J.; et al. Damascene Benchmark of Ru, Co and Cu in Scaled Dimensions. In Proceedings of the 2018 IEEE International Interconnect Technology Conference (IITC), Santa Clara, CA, USA, 4–7 June 2018; pp. 172–174.
143. Dutta, S.; Kundu, S.; Gupta, A.; Jamieson, G.; Granados, J.F.G.; Bömmels, J.; Wilson, C.J.; Tőkei, Z.; Adelmann, C. Highly Scaled Ruthenium Interconnects. *IEEE Electron Device Lett.* **2017**, *38*, 949–951. [CrossRef]
144. Liang Gong, W.; Adelmann, C.; Pedreira, O.V.; Dutta, S.; Popovici, M.; Briggs, B.; Heylen, N.; Vanstreels, K.; Wilson, C.J.; Elshocht, S.V.; et al. Ruthenium metallization for advanced interconnects. In Proceedings of the 2016 IEEE International Interconnect Technology Conference/Advanced Metallization Conference (IITC/AMC), San Jose, CA, USA, 23–26 May 2016; pp. 34–36.
145. Wu, Z.; Li, R.; Xie, X.; Suen, W.; Tseng, J.; Bekiaris, N.; Vinnakota, R.; Kashefizadeh, K.; Naik, M. PVD-Treated ALD TaN for Cu Interconnect Extension to 5nm Node and Beyond. In Proceedings of the 2018 IEEE International Interconnect Technology Conference (IITC), Santa Clara, CA, USA, 4–7 June 2018; pp. 149–151.
146. Chawla, J.S.; Sung, S.H.; Bojarski, S.A.; Carver, C.T.; Chandhok, M.; Chebiam, R.V.; Clarke, J.S.; Harmes, M.; Jezewski, C.J.; Kobrinski, M.J.; et al. Resistance and electromigration performance of 6 nm wires. In Proceedings of the 2016 IEEE International Interconnect Technology Conference/Advanced Metallization Conference (IITC/AMC), San Jose, CA, USA, 23–26 May 2016; pp. 63–65.

147. Veen, M.H.v.d.; Vandersmissen, K.; Dictus, D.; Demuynck, S.; Liu, R.; Bin, X.; Nalla, P.; Lesniewska, A.; Hall, L.; Croes, K.; et al. Cobalt bottom-up contact and via prefill enabling advanced logic and DRAM technologies. In Proceedings of the 2015 IEEE International Interconnect Technology Conference and 2015 IEEE Materials for Advanced Metallization Conference (IITC/MAM), Grenoble, France, 18–21 May 2015; pp. 25–28.
148. Zheng, J.; Chen, P.; Baum, T.H.; Lieten, R.R.; Hunks, W.; Lippy, S.; Frye, A.; Li, W.; Neill, J.O.; Xu, J.; et al. Selective co growth on Cu for void-free via fill. In Proceedings of the 2015 IEEE International Interconnect Technology Conference and 2015 IEEE Materials for Advanced Metallization Conference (IITC/MAM), Grenoble, France, 18–21 May 2015; pp. 265–268.
149. Hu, C.; Kelly, J.; Chen, J.H.; Huang, H.; Ostrovski, Y.; Patlolla, R.; Peethala, B.; Adusumilli, P.; Spooner, T.; Gignac, L.M.; et al. Electromigration and resistivity in on-chip Cu, Co and Ru damascene nanowires. In Proceedings of the 2017 IEEE International Interconnect Technology Conference (IITC), Hsinchu, Taiwan, 16–18 May 2017; pp. 1–3.
150. Posser, G.; Mishra, V.; Reis, R.; Sapatnekar, S.S. Analyzing the Electromigration Effects on Different Metal Layers and Different Wire Lengths. In Proceedings of the 21st IEEE International Conference on Electronics Circuits and Systems (ICECS), Marseille, France, 7–10 December 2014. [CrossRef]
151. Jiang, Y.; Nalla, P.; Matsushita, Y.; Harm, G.; Wang, J.; Kolics, A.; Zhao, L.; Mountsier, T.; Besser, P.; Wu, H.J. Development of electroless Co via-prefill to enable advanced BEOL metallization and via resistance reduction. In Proceedings of the 2016 IEEE International Interconnect Technology Conference/Advanced Metallization Conference (IITC/AMC), San Jose, CA, USA, 23–26 May 2016; pp. 111–113.
152. Ciofi, I.; Roussel, P.J.; Saad, Y.; Moroz, V.; Hu, C.; Baert, R.; Croes, K.; Contino, A.; Vandersmissen, K.; Gao, W.; et al. Modeling of Via Resistance for Advanced Technology Nodes. *IEEE Trans. Electron Devices* **2017**, *64*, 2306–2313. [CrossRef]
153. Wan, D.; Paolillo, S.; Rassoul, N.; Kotowska, B.K.; Blanco, V.; Adelmann, C.; Lazzarino, F.; Ercken, M.; Murdoch, G.; Bömmels, J.; et al. Subtractive Etch of Ruthenium for Sub-5nm Interconnect. In Proceedings of the 2018 IEEE International Interconnect Technology Conference (IITC), Santa Clara, CA, USA, 4–7 June 2018; pp. 10–12.
154. Griggio, F.; Palmer, J.; Pan, F.; Toledo, N.; Schmitz, A.; Tsameret, I.; Kasim, R.; Leatherman, G.; Hicks, J.; Madhavan, A.; et al. Reliability of dual-damascene local interconnects featuring cobalt on 10 nm logic technology. In Proceedings of the 2018 IEEE International Reliability Physics Symposium (IRPS), Burlingame, CA, USA, 11–15 March 2018; pp. 6E.3-1–6E.3-5.
155. Pandey, R.; Agrawal, N.; Arghavani, R.; Datta, S. Analysis of local interconnect resistance at scaled process nodes. In Proceedings of the 2015 73rd Annual Device Research Conference (DRC), Columbus, OH, USA, 21–24 June 2015; p. 184.
156. Kamineni, V.; Raymond, M.; Siddiqui, S.; Mont, F.; Tsai, S.; Niu, C.; Labonte, A.; Labelle, C.; Fan, S.; Peethala, B.; et al. Tungsten and cobalt metallization: A material study for MOL local interconnects. In Proceedings of the 2016 IEEE International Interconnect Technology Conference/Advanced Metallization Conference (IITC/AMC), San Jose, CA, USA, 23–26 May 2016; pp. 105–107.
157. Xunyuan, Z.; Huai, H.; Patlolla, R.; Wei, W.; Mont, F.W.; Juntao, L.; Chao-Kun, H.; Liniger, E.G.; McLaughlin, P.S.; Labelle, C.; et al. Ruthenium interconnect resistivity and reliability at 48 nm pitch. In Proceedings of the 2016 IEEE International Interconnect Technology Conference/Advanced Metallization Conference (IITC/AMC), San Jose, CA, USA, 23–26 May 2016; pp. 31–33.
158. Fan, S.S.; Chen, J.H.; Kamineni, V.K.; Zhang, X.; Raymond, M.; Labelle, C. Middle of line RC performance study at the 7 nm node. In Proceedings of the 2017 IEEE International Interconnect Technology Conference (IITC), Hsinchu, Taiwan, 16–18 May 2017; pp. 1–3.
159. Hosseini, M.; Ando, D.; Sutou, Y.; Koike, J. Co and CoTix for contact plug and barrier layer in integrated circuits. *Microelectron. Eng.* **2018**, *189*, 78–84. [CrossRef]
160. Hosseini, M.; Koike, J.; Sutou, Y.; Zhao, L.; Lai, S.; Arghavani, R. Amorphous Co-Ti alloy as a single layer barrier for Co local interconnect structure. In Proceedings of the 2016 IEEE International Interconnect Technology Conference/Advanced Metallization Conference (IITC/AMC), San Jose, CA, USA, 23–26 May 2016; pp. 162–164.

161. Hellings, G.; Subirats, A.; Franco, J.; Schram, T.; Ragnarsson, L.; Witters, L.; Roussel, P.; Linten, D.; Horiguchi, N.; Boschke, R. Demonstration of sufficient BTI reliability for a 14-nm finFET 1.8 V I/O technology featuring a thick ALD SiO_2 IL and Ge p-channel. In Proceedings of the 2017 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 2–6 April 2017; pp. FA-5.1–FA-5.4.
162. Ren, P.; Gao, R.; Ji, Z.; Arimura, H.; Zhang, J.F.; Wang, R.; Duan, M.; Zhang, W.; Franco, J.; Sioncke, S.; et al. Understanding charge traps for optimizing Si-passivated Ge nMOSFETs. In Proceedings of the 2016 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 14–16 June 2016; pp. 1–2.
163. Benbakhti, B.; Zhang, J.F.; Ji, Z.; Zhang, W.; Mitard, J.; Kaczer, B.; Groeseneken, G.; Hall, S.; Robertson, J.; Chalker, P. Characterization of Electron Traps in Si-Capped Ge MOSFETs With HfO_2/SiO_2 Gate Stack. *IEEE Electron Device Lett.* **2012**, *33*, 1681–1683. [CrossRef]
164. Bao, R.; Southwick, R.G.; Zhou, H.; Lee, C.H.; Linder, B.P.; Ando, T.; Guo, D.; Jagannathan, H.; Narayanan, V. Differentiated Performance and Reliability Enabled by Multi-Work Function Solution in RMG Silicon and SiGe MOSFETs. In Proceedings of the 2018 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 18–22 June 2018; pp. 115–116.
165. Franco, J.; Kaczer, B.; Chasin, A.; Bury, E.; Linten, D. Hot electron and hot hole induced degradation of SiGe p-FinFETs studied by degradation maps in the entire bias space. In Proceedings of the 2018 IEEE International Reliability Physics Symposium (IRPS), Burlingame, CA, USA, 11–15 March 2018; pp. 5A.1-1–5A.1-7.
166. Waltl, M.; Rzepa, G.; Grill, A.; Goes, W.; Franco, J.; Kaczer, B.; Witters, L.; Mitard, J.; Horiguchi, N.; Grasser, T. Superior NBTI in High-k SiGe Transistors—Part II: Theory. *IEEE Trans. Electron Devices* **2017**, *64*, 2099–2105. [CrossRef]
167. Waltl, M.; Rzepa, G.; Grill, A.; Goes, W.; Franco, J.; Kaczer, B.; Witters, L.; Mitard, J.; Horiguchi, N.; Grasser, T. Superior NBTI in High-k SiGe Transistors—Part I: Experimental. *IEEE Trans. Electron Devices* **2017**, *64*, 2092–2098. [CrossRef]
168. Kumar, P.; Leroux, C.; Mohamad, B.; Toffoli, A.; Romano, G.; Garros, X.; Reimbold, G.; Kumar, P.; Domengie, F.; Segovia, C.S.; et al. Effect of La and Al addition used for threshold voltage shift on the BTI reliability of HfON-based FDSOI MOSFETs. In Proceedings of the 2017 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 2–6 April 2017; pp. 2B-2.1–2B-2.7.
169. Zhang, J.; Ando, T.; Yeung, C.W.; Wang, M.; Kwon, O.; Galatage, R.; Chao, R.; Loubet, N.; Moon, B.K.; Bao, R.; et al. High-k metal gate fundamental learning and multi-Vt options for stacked nanosheet gate-all-around transistor. In Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017; pp. 22.21.21–22.21.24.
170. Vandooren, A.; Franco, J.; Wu, Z.; Parvais, B.; Li, W.; Witters, L.; Walke, A.; Peng, L.; Deshpande, V.; Rassoul, N.; et al. First Demonstration of 3D stacked Finfets at a 45 nm fin pitch and 110nm gate pitch technology on 300 mm wafers. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018; pp. 7.1.1–7.1.4.
171. Lima, L.P.B.; Dekkers, H.F.W.; Lisoni, J.G.; Diniz, J.A.; Van Elshocht, S.; De Gendt, S. Metal gate work function tuning by Al incorporation in TiN. *J. Appl. Phys.* **2014**, *115*, 074504. [CrossRef]
172. Lim, A.E.; Lee, R.T.P.; Samudra, G.S.; Kwong, D.; Yeo, Y. Modification of molybdenum gate electrode work function via (La-, Al-induced) dipole effect at High-k/SiO_2 interface. *IEEE Electron Device Lett.* **2008**, *29*, 848–851. [CrossRef]
173. Bao, R.; Hung, S.; Wang, M.; Chung, K.; Barman, S.; Krishnan, S.A.; Yang, Y.; Tang, W.; Li, L.; Lin, Y.; et al. Novel Materials and Processes in Replacement Metal Gate for Advanced CMOS Technology. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018; pp. 11.14.11–11.14.14.
174. Ando, T.; Kannan, B.; Kwon, U.; Lai, W.L.; Linder, B.P.; Cartier, E.A.; Haight, R.; Copel, M.; Bruley, J.; Krishnan, S.A.; et al. Simple Gate Metal Anneal (SIGMA) stack for FinFET Replacement Metal Gate toward 14nm and beyond. In Proceedings of the 2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers, Honolulu, HI, USA, 9–12 June 2014; pp. 1–2.
175. Ragnarsson, L.; Chew, S.A.; Dekkers, H.; Luque, M.T.; Parvais, B.; Keersgieter, A.D.; Devriendt, K.; Ammel, A.V.; Schram, T.; Yoshida, N.; et al. Highly scalable bulk FinFET Devices with Multi-VT options by conductive metal gate stack tuning for the 10-nm node and beyond. In Proceedings of the 2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers, Honolulu, HI, USA, 9–12 June 2014; pp. 1–2.

176. Bury, E.; Kaczer, B.; Linten, D.; Witters, L.; Mertens, H.; Waldron, N.; Zhou, X.; Collaert, N.; Horiguchi, N.; Spessot, A.; et al. Self-heating in FinFET and GAA-NW using Si, Ge and III/V channels. In Proceedings of the 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 3–7 December 2016; pp. 15.16.11–15.16.14.
177. Chalia, G.; Hegde, R.S. Study of Self-Heating Effects in Silicon Nano-Sheet Transistors. In Proceedings of the 2018 IEEE International Conference on Electron Devices and Solid State Circuits (EDSSC), Shenzhen, China, 6–8 June 2018; pp. 1–2.
178. Cai, L.; Chen, W.; Du, G.; Zhang, X.; Liu, X. Layout Design Correlated with Self-Heating Effect in Stacked Nanosheet Transistors. *IEEE Trans. Electron Devices* **2018**, *65*, 2647–2653. [CrossRef]
179. Chen, W.; Cai, L.; Wang, K.; Zhang, X.; Liu, X.; Du, G. Self-heating induced Variability and Reliability in Nanosheet-FETs Based SRAM. In Proceedings of the 2018 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), Singapore, 16–19 July 2018; pp. 1–4.
180. Wang, R.; Guo, S.; Zhang, Z.; Zou, J.; Mao, D.; Huang, R. Complex Random Telegraph Noise (RTN): What Do We Understand? In Proceedings of the 2018 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), Singapore, 16–19 July 2018; pp. 1–7.
181. Guo, S.; Lin, Z.; Wang, R.; Zhang, Z.; Zhang, Z.; Wang, Y.; Huang, R. Investigation on the amplitude coupling effect of random telegraph noise (RTN) in nanoscale FinFETs. In Proceedings of the 2018 IEEE International Reliability Physics Symposium (IRPS), Burlingame, CA, USA, 11–15 March 2018; pp. P-TX.6-1–P-TX.6-4.
182. Brown, J.; Gao, R.; Ji, Z.; Chen, J.; Wu, J.; Zhang, J.; Zhou, B.; Shi, Q.; Crowford, J.; Zhang, W. A low-power and high-speed True Random Number Generator using generated RTN. In Proceedings of the 2018 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 18–22 June 2018; pp. 95–96.
183. Wangran, W.; Wu, H.; Si, M.; Conrad, N.; Yi, Z.; Ye, P.D. RTN and low frequency noise on ultra-scaled near-ballistic Ge nanowire nMOSFETs. In Proceedings of the 2016 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 14–16 June 2016; pp. 1–2.
184. Takagi, S.; Ahn, D.H.; Gotow, T.; Noguchi, M.; Nishi, K.; Kim, S.; Yokoyama, M.; Chang, C.; Yoon, S.; Yokoyama, C.; et al. III–V-based low power CMOS devices on Si platform. In Proceedings of the 2017 IEEE International Conference on IC Design and Technology (ICICDT), Austin, TX, USA, 23–25 May 2017; pp. 1–4.
185. Mols, Y.; Kunert, B.; Gaudin, G.; Langer, R.; Caymax, M. Study towards integration of In0.53Ga0.47As on 300 mm Si for CMOS sub-7 nm node: Development of thin graded InxGa1-xAs buffers on GaAs. *J. Cryst. Growth* **2016**, *452*, 244–247. [CrossRef]
186. Zhou, X.; Waldron, N.; Boccardi, G.; Sebaai, F.; Merckling, C.; Eneman, G.; Sioncke, S.; Nyns, L.; Opdebeeck, A.; Maes, J.W.; et al. Scalability of InGaAs gate-all-around FET integrated on 300 mm Si platform: Demonstration of channel width down to 7 nm and L-g down to 36 nm. In Proceedings of the 2016 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 14–16 June 2016; pp. 1–2.
187. Liu, Z.Y.; Merckling, C.; Rooyackers, R.; Franquet, A.; Richard, O.; Bender, H.; Vila, M.; Rubio-Zuazo, J.; Castro, G.R.; Collaert, N.; et al. The effect of Ga pre-deposition on Si (111) surface for InAs nanowire selective area hetero-epitaxy. *J. Appl. Phys.* **2018**, *123*, 145301. [CrossRef]
188. Sollier, S.; Widiez, J.; Gaudin, G.; Mazen, F.; Baron, T.; Martin, M.; Roure, M.C.; Besson, P.; Morales, C.; Beche, E.; et al. 300 mm InGaAsOI substrate fabrication using the Smart Cut^{TM} technology. In Proceedings of the 2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), Rohnert Park, CA, USA, 5–8 October 2015; pp. 1–2.
189. Mauthe, S.; Schmid, H.; Mayer, B.; Wirths, S.; Convertino, C.; Baumgartner, Y.; Czornomaz, L.; Sousa, M.; Staudinger, P.; Riel, H.; et al. Monolithic Integration of III–V on silicon for photonic and electronic applications. In Proceedings of the 2018 76th Device Research Conference (DRC), Santa Barbara, CA, USA, 24–27 June 2018; pp. 1–2.
190. Knoedler, M.; Bologna, N.; Schmid, H.; Borg, M.; Moselund, K.E.; Wirths, S.; Rossell, M.D.; Riel, H. Observation of Twin-free GaAs Nanowire Growth Using Template Assisted Selective Epitaxy. *Cryst. Growth Des.* **2017**, *17*, 6297–6302. [CrossRef]
191. Czornomaz, L.; Uccelli, E.; Sousa, M.; Deshpande, V.; Djara, V.; Caimi, D.; Rossell, M.D.; Erni, R.; Fompeyrine, J. Confined Epitaxial Lateral Overgrowth (CELO): A novel concept for scalable integration of CMOS-compatible InGaAs-on-insulator MOSFETs on large-area Si substrates. In Proceedings of the 2015 Symposium on VLSI Technology (VLSI Technology), Kyoto, Japan, 16–18 June 2015; pp. T172–T173.

192. Djara, V.; Deshpande, V.; Sousa, M.; Caimi, D.; Czornomaz, L.; Fompeyrine, J. CMOS-Compatible Replacement Metal Gate InGaAs-OI FinFET with I-ON = 156 mu A/mu m at V-DD = 0.5 V and I-OFF = 100 nA/mu m. *IEEE Electron Device Lett.* **2016**, *37*, 169–172. [CrossRef]
193. Hahn, H.; Deshpande, V.; Caruso, E.; Sant, S.; Connor, E.O.; Baumgartner, Y.; Sousa, M.; Caimi, D.; Olziersky, A.; Palestri, P.; et al. A scaled replacement metal gate InGaAs-on-Insulator n-FinFET on Si with record performance. In Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017; pp. 17.15.11–17.15.14.
194. Deshpande, V.; Djara, V.; O'Connor, E.; Hashemi, P.; Balakrishnan, K.; Caimi, D.; Sousa, M.; Czornomaz, L.; Fompeyrine, J. DC and RF characterization of InGaAs replacement metal gate (RMG) nFETs on SiGe-OI FinFETs fabricated by 3D monolithic integration. *Solid-State Electron.* **2017**, *128*, 87–91. [CrossRef]
195. Li, X.M.; Tao, L.; Chen, Z.F.; Fang, H.; Li, X.S.; Wang, X.R.; Xu, J.B.; Zhu, H.W. Graphene and related two-dimensional materials: Structure-property relationships for electronics and optoelectronics. *Appl. Phys. Rev.* **2017**, *4*, 021306. [CrossRef]
196. Balandin, A.A.; Ghosh, S.; Bao, W.Z.; Calizo, I.; Teweldebrhan, D.; Miao, F.; Lau, C.N. Superior thermal conductivity of single-layer graphene. *Nano Lett.* **2008**, *8*, 902–907. [CrossRef]
197. Bonaccorso, F.; Sun, Z.; Hasan, T.; Ferrari, A.C. Graphene photonics and optoelectronics. *Nat. Photonics* **2010**, *4*, 611–622. [CrossRef]
198. Wu, Y.Q.; Jenkins, K.A.; Valdes-Garcia, A.; Farmer, D.B.; Zhu, Y.; Bol, A.A.; Dimitrakopoulos, C.; Zhu, W.J.; Xia, F.N.; Avouris, P.; et al. State-of-the-Art Graphene High-Frequency Electronics. *Nano Lett.* **2012**, *12*, 3062–3067. [CrossRef]
199. Jiao, L.Y.; Wang, X.R.; Diankov, G.; Wang, H.L.; Dai, H.J. Facile synthesis of high-quality graphene nanoribbons. *Nat. Nanotechnol.* **2010**, *5*, 321–325. [CrossRef]
200. Wang, X.R.; Ouyang, Y.J.; Li, X.L.; Wang, H.L.; Guo, J.; Dai, H.J. Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors. *Phys. Rev. Lett.* **2008**, *100*, 206803. [CrossRef]
201. Zhou, S.Y.; Gweon, G.H.; Fedorov, A.V.; First, P.N.; De Heer, W.A.; Lee, D.H.; Guinea, F.; Castro Neto, A.H.; Lanzara, A. Substrate-induced bandgap opening in epitaxial graphene. *Nat. Mater.* **2007**, *6*, 916. [CrossRef]
202. Liu, W.; Kraemer, S.; Sarkar, D.; Li, H.; Ajayan, P.M.; Banerjeet, K. Controllable and Rapid Synthesis of High-Quality and Large-Area Bernal Stacked Bilayer Graphene Using Chemical Vapor Deposition. *Chem. Mat.* **2014**, *26*, 907–915. [CrossRef]
203. Moon, J.S.; Seo, H.C.; Stratan, F.; Antcliffe, M.; Schmitz, A.; Ross, R.S.; Kiselev, A.A.; Wheeler, V.D.; Nyakiti, L.O.; Gaskill, D.K.; et al. Lateral Graphene Heterostructure Field-Effect Transistor. *IEEE Electron Device Lett.* **2013**, *34*, 1190–1192. [CrossRef]
204. Yuan, S.G.; Yang, Z.B.; Xie, C.; Yan, F.; Dai, J.Y.; Lau, S.P.; Chan, H.L.W.; Hao, J.H. Ferroelectric-Driven Performance Enhancement of Graphene Field-Effect Transistors Based on Vertical Tunneling Heterostructures. *Adv. Mater.* **2016**, *28*, 10048–10054. [CrossRef]
205. Schwierz, F.; Pezoldt, J.; Granzner, R. Two-dimensional materials and their prospects in transistor electronics. *Nanoscale* **2015**, *7*, 8261–8283. [CrossRef]
206. Lee, I.; Rathi, S.; Lim, D.; Li, L.; Park, J.; Lee, Y.; Yi, K.S.; Dhakal, K.P.; Kim, J.; Lee, C.; et al. Gate-Tunable Hole and Electron Carrier Transport in Atomically Thin Dual-Channel WSe_2/MoS_2 Heterostructure for Ambipolar Field-Effect Transistors. *Adv. Mater.* **2016**, *28*, 9519–9525. [CrossRef]
207. Nourbakhsh, A.; Zubair, A.; Sajjad, R.N.; Tavakkoli, K.G.A.; Chen, W.; Fang, S.; Ling, X.; Kong, J.; Dresselhaus, M.S.; Kaxiras, E.; et al. MoS_2 Field-Effect Transistor with Sub-10 nm Channel Length. *Nano Lett.* **2016**, *16*, 7798–7806. [CrossRef]
208. Roy, T.; Tosun, M.; Kang, J.S.; Sachid, A.B.; Desai, S.B.; Hettick, M.; Hu, C.M.C.; Javey, A. Field-Effect Transistors Built from All Two-Dimensional Material Components. *ACS Nano* **2014**, *8*, 6259–6264. [CrossRef]
209. Salahuddin, S.; Datta, S. Use of negative capacitance to provide voltage amplifcation for low power nanoscale devices. *Nano Lett.* **2008**, *8*, 405–410. [CrossRef]
210. Zhirnov, V.V.; Cavin, R.K. Nanoelectronics: Negative capacitance to the rescue? *Nat. Nanotechnol.* **2008**, *3*, 77–78. [CrossRef]
211. Verhulst, A.S.; Vandenberghe, W.G.; Maex, K.; Groeseneken, G. Boosting the on-current of a *n*-channel nanowire tunnel field-effect transistor by source material optimization. *J. Appl. Phys.* **2008**, *104*, 064514. [CrossRef]

212. Avci, U.E.; Morris, D.H.; Young, I.A. Tunnel field-effect transistors: Prospects and challenges. *IEEE J. Electron Devices Soc.* **2015**, *3*, 88–95. [CrossRef]
213. Gandhi, R.; Chen, Z.; Singh, N.; Banerjee, K.; Lee, S. Vertical Si-Nanowire *n*-Type Tunneling FETs with Low Subthreshold Swing (≤50 mV/decade) at Room Temperature. *IEEE Electron Device Lett.* **2011**, *32*, 437–439. [CrossRef]
214. Lu, H.; Seabaugh, A. Tunnel field-effect transistors: State-of-the-art. *IEEE J. Electron Devices Soc.* **2014**, *2*, 44–49. [CrossRef]
215. Kim, S.H.; Kam, H.; Hu, C.; Liu, T.J. Germanium-source tunnel field effect transistors with record high I_{ON}/I_{OFF}. In Proceedings of the 2009 Symposium on VLSI Technology, Honolulu, HI, USA, 16–18 June 2009; pp. 178–179.
216. Luisier, M.; Klimeck, G. Simulation of nanowire tunneling transistors: From the Wentzel–Kramers–Brillouin approximation to full-band phonon-assisted tunneling. *J. Appl. Phys.* **2010**, *107*, 084507. [CrossRef]
217. Zhao, P.; Chauhan, J.; Guo, J. Computational study of tunneling transistor based on graphene nanoribbon. *Nano Lett.* **2009**, *9*, 684–688. [CrossRef]
218. Chin, S.K.; Seah, D.; Lam, K.T.; Samudra, G.S.; Liang, G. Device physics and characteristics of graphene nanoribbon tunneling FETs. *IEEE Trans. Electron Devices* **2010**, *57*, 3144–3152. [CrossRef]
219. Lam, K.T.; Cao, X.; Guo, J. Device performance of heterojunction tunneling field-effect transistors based on transition metal dichalcogenide monolayer. *IEEE Electron Device Lett.* **2013**, *34*, 1331–1333. [CrossRef]
220. Ilatikhameneh, H.; Tan, Y.; Novakovic, B.; Klimeck, G.; Rahman, R.; Appenzeller, J. Tunnel field-effect transistors in 2-D transition metal dichalcogenide materials. *IEEE J. Explor. Solid-State Comput. Devices Circuits* **2015**, *1*, 12–18. [CrossRef]
221. Seo, J.; Jung, S.; Shin, M. The Performance of Uniaxially Strained Phosphorene Tunneling Field-Effect Transistors. *IEEE Electron Device Lett.* **2017**, *38*, 1150–1152. [CrossRef]
222. Chen, F.W.; Ilatikhameneh, H.; Ameen, T.A.; Klimeck, G.; Rahman, R. Thickness engineered tunnel field-effect transistors based on phosphorene. *IEEE Electron Device Lett.* **2017**, *38*, 130–133. [CrossRef]
223. Szabó, Á.; Koester, S.J.; Luisier, M. Ab-initio simulation of van der waals $MoTe_2$–SnS_2 heterotunneling fets for low-power electronics. *IEEE Electron Device Lett.* **2015**, *36*, 514–516.
224. Cao, J.; Logoteta, D.; Özkaya, S.; Biel, B.; Cresti, A.; Pala, M.G.; Esseni, D. Operation and Design of van der Waals Tunnel Transistors: A 3-D Quantum Transport Study. *IEEE Trans. Electron Devices* **2016**, *63*, 4388–4394. [CrossRef]
225. Manipatruni, S.; Nikonov, D.E.; Lin, C.C.; Gosavi, T.A.; Liu, H.; Prasad, B.; Huang, Y.L.; Onturim, E.; Ramesh, R.; Young, I.A. Scalable energy-efficient magnetoelectric spin–orbit logic. *Nature* **2019**, *565*, 35–42. [CrossRef]
226. Watanabe, K.; Takagi, Y.; Obara, K.; Okuda, H.; Nakagaki, R.; Kurosaki, T. Efficient killer-defect control using reliable high-throughput SEM-ADC. In Proceedings of the 2001 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (IEEE Cat. No.01CH37160), Munich, Germany, 23–24 April 2001; pp. 219–222.
227. Patterson, O.D.; Seefeldt, B.; Liang, W.; Hu, H.; Chen, J.; Su, Y.; Yeh, H.T.; Zhang, P. Shortest path CD measurement using contour extraction. In Proceedings of the 2018 29th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC), Saratoga Springs, NY, USA, 30 April–3 May 2018; pp. 313–319.
228. Takamizawa, H.; Shimizu, Y.; Inoue, K.; Toyama, T.; Okada, N.; Kato, M.; Uchida, H.; Yano, F.; Nishida, A.; Mogami, T.; et al. Origin of characteristic variability in metal-oxide-semiconductor field-effect transistors revealed by three-dimensional atom imaging. *Appl. Phys. Lett.* **2011**, *99*, 133502. [CrossRef]
229. Grenier, A.; Duguay, S.; Barnes, J.P.; Serra, R.; Haberfehlner, G.; Cooper, D.; Bertin, F.; Barraud, S.; Audoit, G.; Arnoldi, L.; et al. 3D analysis of advanced nano-devices using electron and atom probe tomography. *Ultramicroscopy* **2014**, *136*, 185–192. [CrossRef]
230. Barnes, J.P.; Grenier, A.; Mouton, I.; Barraud, S.; Audoit, G.; Bogdanowicz, J.; Fleischmann, C.; Melkonyan, D.; Vandervorst, W.; Duguay, S.; et al. Atom probe tomography for advanced nanoelectronic devices: Current status and perspectives. *Scr. Mater.* **2018**, *148*, 91–97. [CrossRef]
231. Giddings, A.D.; Koelling, S.; Shimizu, Y.; Estivill, R.; Inoue, K.; Vandervorst, W.; Yeoh, W.K. Industrial application of atom probe tomography to semiconductor devices. *Scr. Mater.* **2018**, *148*, 82–90. [CrossRef]

232. Patrick, H.J.; Germer, T.A. Progress towards traceable nanoscale optical critical dimension metrology for semiconductors. In *Advanced Characterization Techniques for Optics, Semiconductors, and Nanotechnologies III*; Duparre, A., Singh, B., Gu, Z.H., Eds.; SPIE: San Diego, CA, USA, 2007; Volume 6672.
233. Germer, T.A.; Patrick, H.J.; Silver, R.M.; Bunday, B. *Developing an Uncertainty Analysis for Optical Scatterometry*; SPIE: San Diego, CA, USA, 2009; Volume 7272.
234. Diebold, A.C. Characterization and metrology for nanoelectronics. In *Frontiers of Characterization and Metrology for Nanoelectronics: 2007*; Seiler, D.G., Diebold, A.C., McDonald, R., Garner, C.M., Herr, D., Khosla, R.P., Secula, E.M., Eds.; American Institute of Physics: Melville, NY, USA, 2007; Volume 931, pp. 20–33.
235. Vagos, P.; Rovira, P.I. Mueller Matrix Spectroscopy Using Chiroptic. US Patent 8427645-B2, 23 April 2013.
236. Novikova, T.; De Martino, A.; Ben Hatit, S.; Drevillon, B. Application of Mueller polarimetry in conical diffraction for critical dimension measurements in microelectronics. *Appl. Opt.* **2006**, *45*, 3688–3697. [CrossRef]
237. Liu, S.Y.; Chen, X.G.; Zhang, C.W. Development of a broadband Mueller matrix ellipsometer as a powerful tool for nanostructure metrology. *Thin Solid Films* **2015**, *584*, 176–185. [CrossRef]
238. Vaid, A.; Bin Yan, B.; Jiang, Y.T.; Kelling, M.; Hartig, C.; Allgair, J.; Ebersbach, P.; Sendelbach, M.; Rana, N.; Katnani, A.; et al. A Holistic Metrology Approach: Hybrid Metrology Utilizing Scatterometry, CD-AFM and CD-SEM. In *Metrology, Inspection, and Process Control for Microlithography Xxv, Pt 1 and Pt 2*; Raymond, C.J., Ed.; SPIE: San Jose, CA, USA, 2011; Volume 7971.
239. Radamson, H.H.; Hallstedt, J. Application of high-resolution X-ray diffraction for detecting defects in SiGe(C) materials. *J. Phys. Condes. Matter* **2005**, *17*, S2315–S2322. [CrossRef]
240. Hansson, G.V.; Radamsson, H.H.; Ni, W.X. Strain and relaxation in SI-MBE structures studied by reciprocal space mapping using high-resolution X-ray-diffraction. *J. Mater. Sci. Mater. Electron.* **1995**, *6*, 292–297. [CrossRef]
241. Radamson, H.H.; Sardela, M.R.; Hultman, L.; Hansson, G.V. Characterization of highly sb-doped SI using high-resolution X-ray-diffraction and transmission electron-microscopy. *J. Appl. Phys.* **1994**, *76*, 763–767. [CrossRef]
242. Radamson, H.H.; Kolahdouz, M.; Ghandi, R.; Ostling, M. High strain amount in recessed junctions induced by selectively deposited boron-doped SiGe layers. *Mater. Sci. Eng. B Adv. Funct. Solid-State Mater.* **2008**, *154*, 106–109. [CrossRef]
243. Sardela, M.R.; Radamson, H.H.; Ekberg, J.O.; Sundgren, J.E.; Hansson, G.V. Relation between electrical activation and the B-induced strain in Si determined by reciprocal lattice mapping. *Semicond. Sci. Technol.* **1994**, *9*, 1272–1275. [CrossRef]
244. Hung, P.Y.; Kasper, N.; Nadeau, J.; Ok, I.; Hobbs, C.; Vigliante, A. Application of inline high resolution X-ray diffraction in monitoring Si/SiGe and conventional Si in SOI fin-shaped field effect transistor processes. *J. Vac. Sci. Technol. B* **2012**, *30*, 5. [CrossRef]
245. Medikonda, M.; Muthinti, G.R.; Fronheiser, J.; Kamineni, V.; Wormington, M.; Matney, K.; Adam, T.N.; Karapetrova, E.; Diebold, A.C. Measurement of periodicity and strain in arrays of single crystal silicon and pseudomorphic Si1-xGex/Si fin structures using x-ray reciprocal space maps. *J. Vac. Sci. Technol. B* **2014**, *32*, 021804. [CrossRef]
246. Mochizuki, S.; Murray, C.E.; Madan, A.; Pinto, T.; Wang, Y.Y.; Li, J.T.; Weng, W.H.; Jagannathan, H.; Imai, Y.; Kimura, S.; et al. Quantification of local strain distributions in nanoscale strained SiGe FinFET structures. *J. Appl. Phys.* **2017**, *122*, 135705. [CrossRef]
247. Schulze, A.; Loo, R.; Witters, L.; Mertens, H.; Gawlik, A.; Horiguchi, N.; Collaert, N.; Wormington, M.; Ryan, P.; Vandervorst, W.; et al. Strainand Compositional Analysis of (Si) Ge Fin Structures Using High Resolution X-Ray Diffraction. *Phys. Status Solidi (c)* **2017**, *14*. [CrossRef]
248. Reboh, S.; Coquand, R.; Barraud, S.; Loubet, N.; Bernier, N.; Audoit, G.; Rouviere, J.L.; Augendre, E.; Li, J.; Gaudiello, J.; et al. Strain, stress, and mechanical relaxation in fin-patterned Si/SiGe multilayers for sub-7nm nanosheet gate-all-around device technology. *Appl. Phys. Lett.* **2018**, *112*, 051901. [CrossRef]
249. Wang, C.Q.; Jones, R.L.; Lin, E.K.; Wu, W.L.; Villarrubia, J.S.; Choi, K.W.; Clarke, J.S.; Rice, B.J.; Leeson, M.; Roberts, J.; et al. Line edge roughness characterization of sub-50 nm structures using CD-SAXS: Round-robin benchmark results. In *Metrology, Inspection, and Process Control for Microlithography Xxi, Pts 1–3*; Archie, C.N., Ed.; SPIE: San Jose, CA, USA, 2007; Volume 6518.

250. Sunday, D.F.; List, S.; Chawla, J.S.; Kline, R.J. Determining the shape and periodicity of nanostructures using small-angle X-ray scattering. *J. Appl. Cryst.* **2015**, *48*, 1355–1363. [CrossRef]
251. Sunday, D.F.; Hammond, M.R.; Wang, C.Q.; Wu, W.L.; Kline, R.J.; Stein, G.E. Three-dimensional X-ray metrology for block copolymer lithography line-space patterns. *J. Micro-Nanolithogr. MEMS MOEMS* **2013**, *12*, 031103. [CrossRef]
252. Pfluger, M.; Soltwisch, V.; Probst, J.; Scholze, F.; Krumrey, M. Grazing-incidence small-angle X-ray scattering (GISAXS) on small periodic targets using large beams. *IUCrJ* **2017**, *4*, 431–438. [CrossRef] [PubMed]
253. NovaFit™. Nova's Data Empowered Metrology Solution. Available online: http://www.novami.com/nova-product/novafit (accessed on 4 April 2019).

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Review

Hybrid Polymer/Metal Oxide Thin Films for High Performance, Flexible Transistors

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Abstract: Metal oxides (MOs) have garnered significant attention in a variety of research fields, particularly in flexible electronics such as wearable devices, due to their superior electronic properties. Meanwhile, polymers exhibit excellent mechanical properties such as flexibility and durability, besides enabling economic solution-based fabrication. Therefore, MO/polymer nanocomposites are excellent electronic materials for use in flexible electronics owing to the confluence of the merits of their components. In this article, we review recent developments in the synthesis and fabrication techniques for MO/polymer nanocomposite-based flexible transistors. In particular, representative MO/polymer nanocomposites for flexible and transparent channel layers and gate dielectrics are introduced and their electronic properties—such as mobilities and dielectric constant—are presented. Finally, we highlight the advances in interface engineering and its influence on device electronics.

Keywords: flexible transistors; polymers; metal oxides; nanocomposites; dielectrics; active layers

1. Introduction

Thin-film transistors (TFTs) are the crucial elements in flat-panel display (FPD) applications, including both active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting diode (AMOLEDs) displays [1–3]. In recent years, the traditional amorphous Si (a-Si) TFT technology has achieved higher resolutions, larger screen sizes, and lower power consumptions in FPDs [4,5]. However, the demand for transparent, flexible, and stretchable optoelectronic devices remains, which requires further advancement in crucial component materials, including the semiconductor, the dielectric, and the conductor, as well as the substrates [6–12].

As mechanically flexible and durable semiconductors as well as gate dielectrics, metal oxides (MOs) such as In_2O_3, ZrO_2, Al_2O_3, and TiO_2 are now expected to be one of the most promising materials for next generation display technologies, because of their high carrier mobility, good transparency, excellent uniformity, and reasonable electrical reliability/stability [13–20]. More importantly, MOs exhibit high carrier mobilities even in the amorphous state and satisfactory environmental stability [21,22]. It is worth noting that the amorphous phase is favorable for use in flexible devices compared to the

crystalline phase, as crystalline materials tend to crack when folded. Indium oxide (In_2O_3) is the most heavily investigated metal oxide both as a conductor and a semiconductor, since the extensive 5s orbital overlap leads to a broad conduction band with high electron mobility even in the amorphous state [23]. Furthermore, their large bandgap ensures optical transparency. The conventional strategy to achieve optimal conductivity in In_2O_3 is to chemically dope the compound with various cations such as Sn, Ga, La, or Sc [24–26]. For example, ITO (indium−tin−oxide) exhibits excellent transparency with high conductivity since the Sn ion enhances the carrier density by donating free electrons to the lattice due to the difference in oxidation state between In^{3+} and Sn^{4+} [27,28]. In IGZO (indium−gallium−zinc−oxide), Ga forms stronger chemical bonds with oxygen and suppresses the formation of oxygen deficiencies and free electrons, thereby serving the role of a "stabilizer" or a "suppressor" [29]. Currently, commercially available metal oxide (semi)conductor films are primarily fabricated via capital-intensive vacuum vapor deposition processes, such as sputtering or thermal evaporation, thereby limiting the large scale and economic production of MO films. Post-annealing processes to enhance charge carrier mobility require high processing temperatures to induce metal–oxygen–metal lattice formation. However, such high temperatures are not suitable for fabrication of MO on soft polymeric substrates such as polyimide (PI), polyethylene naphthalate, polyethylene terephthalate, polydimethylsiloxane, and parylene [29–31]. Moreover, mechanical toughness is also required for the use of inflexible and foldable devices.

In this context, novel processing techniques for fabricating flexible MO films with high charge carrier mobilities is in great demand. Organic polymers such as poly(4-vinylphenol) (PVP), polytetrafluoroethylene (PTFE), and polyethylenimine (PEI), therefore, have been utilized as flexible matrices with various MO fillers due to their merits such as flexibility, light-weight, durability, and solution-processability [32–35]. Using MO/polymer nanocomposites, the films can be easily fabricated via solution-based fabrication processes including spin-casting and roll-to-roll.

This review seeks to summarize the recent progress in the synthesis and fabrication techniques of MO/polymer nanocomposites for flexible transistors. In particular, the synthesis of metal oxides/polymers nanocomposites for flexible channel layers and gate dielectrics, alongside their electronic properties such as mobilities and dielectric constant, are presented. Furthermore, advances in interface engineering and their influence on device electronics are highlighted.

2. Synthesis of Metal Oxides

New techniques have continued to emerge for the synthesis of MO nanostructures with controlled shape, size, and composition, because these factors play an important role in any application [36,37]. In particular, the morphology of MOs are strongly dependent on the synthetic route [38,39]. Therefore, it is critical to select an appropriate synthetic technique to achieve the desired morphology of MOs. In general, a lot of approaches have been reported for the synthesis of various MO nanostructures (Figure 1), including precipitation, hydrothermal, sol–gel methods, microwave-assisted synthesis, and chemical vapor deposition (CVD) [37,40–43].

The earliest technique that was developed to synthesize inorganics is the precipitation method. The primary merit of this strategy is its ease of scalability in the synthesis of MOs for commercialization [44]. In a typical process, the precipitation of sparingly soluble hydroxides takes place from an aqueous solution on the addition of a precipitating agent (anion) or ligand (e.g., urea, hexamethylenetetramine, and KOH) to the metal salt solution containing a cation. Subsequently, the precipitated hydroxides are decomposed to metal oxides [45]. It is very difficult to control the uniformity of the product structures via the precipitation approach, owing to a lack of understanding of major processing steps, namely nucleation and growth [46].

Hydrothermal methods are very simple and capable of generating MOs with diverse morphologies, such as spheres, rods, wires, and cones [47–50]. During synthesis, a heterogeneous reaction occurs in an aqueous solvent containing NaOH, KOH, HCl, HNO_3, H_2SO_4, etc. under a particular pressure and temperature [51]. The major benefits of hydrothermal syntheses are its low processing temperature, reduced aggregation of the products, homogeneous crystallinity of the products, and satisfactory

uniformity in composition and purity of the products [52,53]. Occasionally, surfactants such as cetyltrimethylammonium bromide, sodium dodecyl sulfate, and polyvinylpyrrolidine (PVP) are utilized—the surfactant molecules selectively adhere onto the polar surface of the MO crystals, controlling the shape and growth behavior of MO particles [54–56].

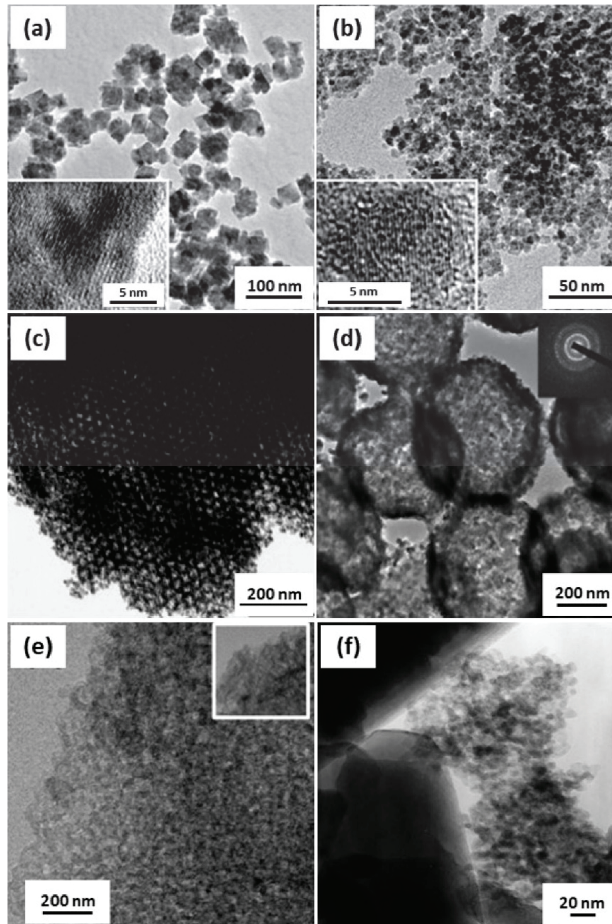

Figure 1. (**a**–**f**) A set of TEM images of diverse MO nanostructures: (**a**) MnO and (**b**) Fe_3O_4 nanoparticles fabricated via microwave-assisted synthesis (Reproduced from [42], Copyright 2008 Royal Society of Chemistry C), (**c**) porous SnO_2 aerosols prepared via sol–gel method (reproduced with permission from [41], Copyright 2005 Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim), (**d**) ZnO hollow spheres synthesized via hydrothermal synthesis (reproduced with permission from [40], Copyright 2008 American Chemical Society), (**e**) In_2O_3 nanoparticles prepared via anodization-precipitation (reproduced with permission from [37], Copyright 2018 American Chemical Society), and (**f**) TiO_2 nanoparticle layer on SiO_2 prepared via CVD, respectively (reproduced with permission from [43], Copyright 2001 Elsevier).

Sol–gel is a general, versatile, and powerful approach for the synthesis of single- or multiple-component MO nanostructures in the form of thin films, powders, and porous materials. This approach is a cost effective and low-temperature process that enables the production of MO

nanostructures with high homogeneity and compositional purity [57,58]. Metal alkoxides [M(OR)$_3$] are primarily used as a precursor to prepare MOs due to their propensity to form homogeneous solution in a variety of solvents in the presence of other alkoxides or metallic derivatives and also due to their reactivity toward nucleophiles such as water [59]. The sol–gel process involves several important steps, such as hydrolysis and condensation, gelation, and drying (Figure 2). Typically, metal precursors such as metal alkoxides and metal chlorides undergo the reactions of hydrolysis and partial condensation to form a colloidal solution. Subsequently, three-dimensional gels are formed immediately via polycondensation of the hydrolyzed precursors. Finally, the resultant gels are converted to xerogel or aerogel based on the method of drying (i.e., supercritical drying or ambient drying) and, furthermore, to the desired MO materials via a thermal treatment. The sol–gel technique can be divided into two routes—namely the aqueous sol–gel and the nonaqueous sol–gel methods. The aqueous sol–gel method requires oxygen for the formation of MOs, which is generally provided by the water solvent. However, this approach is not suitable for the production of MO nanomaterials because the crucial steps (i.e., hydrolysis, condensation, and drying) take place simultaneously and thus result in the formation of bulk MOs [39,60]. In contrast, solvents such as alcohols, ketones, and aldehydes are used to provide the oxygen necessary for the formation of MOs via the nonaqueous sol–gel method [39,61–63]. Additionally, this approach is suitable for the production of MO nanomaterials, rather than their bulk counterparts. The organic solvents serve as important components by controlling morphology, particle size, surface properties, and composition of the resultant MO materials [64].

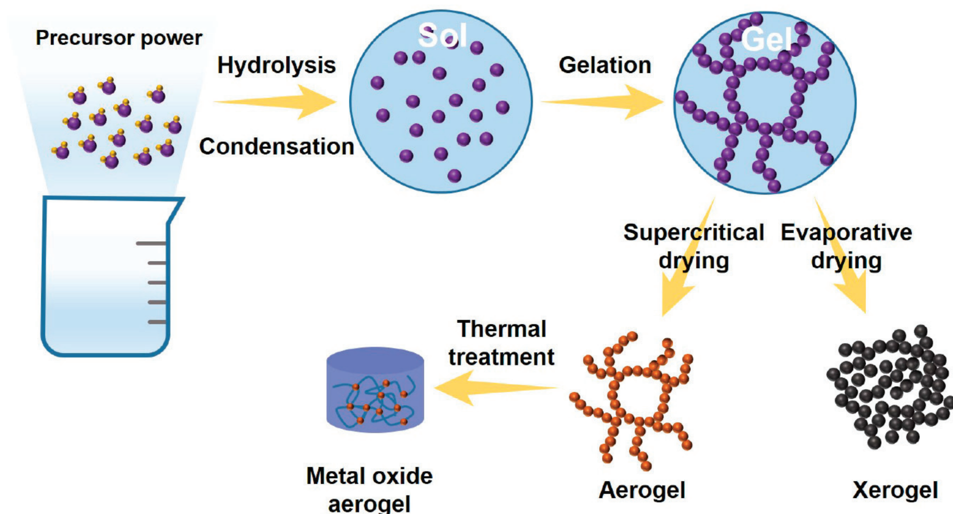

Figure 2. Reaction routes for the production of MO nanostructures by the sol–gel method.

Microwave-assisted synthesis is an approach that applies microwave radiation to chemical reactions for the production of MO nanostructures. This method could allow more efficient, rapid, and homogenous heating of reaction mixtures, thereby accelerating the synthesis of MO nanostructures [65]. Furthermore, the formation of fine MO nanocrystals is enabled by the use of microwave radiation due to the highly focused local heating that can be achieved [66]. Moreover, the microwave-assisted approach can produce a wide range of MO nanostructures, including nanoflakes [67], nanosheets [68], and nanoflowers [69]. However, the microwave-assisted synthesis possesses some drawbacks, such as the high cost of microwave reactor and the limited penetration depth of microwave radiation, indicative of restricted scalability for the commercial synthesis of MO nanoparticles [70].

3. Metal Oxide/Polymer Hybrid Films in Transistors

3.1. Active Channel Layers

Although metal oxides (MOs) exhibit high carrier mobilities and good environmental stability even in the amorphous state, their application in flexible and stretchable devices has been rather limited [25,71–73]. This is because polycrystalline materials suffer from crack formation at the grain boundaries leading to drastic deterioration of structural integrity [74–78]. Recently, amorphous metal oxides (MOs) have been prepared to improve flexibility. However, they are still vulnerable to mechanical stress, yielding cracks under repeated mechanical deformation. On the other hand, polymers exhibit flexibility, solution-processability, and excellent compatibility with organic substrates or active layers [79,80]. In this context, organic–inorganic nanocomposites can gain the synergetic advantages of these two components—namely, mechanical toughness, flexibility, and high mobility [81,82]. Moreover, the incorporation of polymers with MOs successfully inhibits the formation of the crystalline phase which is detrimental to flexible substrates. It should be noted that in general, the trade-off between the mechanical properties and electrical properties is observed in MO/polymer nanocomposites. In other words, while incorporation of polymers to MO films gives rise to an increase in flexibility, it leads to a potential reduction in electrical properties due to phase separations and lack of interconnectivity of MO domains in the resultant composite films. To overcome the issue, various strategies that can improve the interconnectivity of MO domains within the composite films have emerged in recent years, including engineering of weight fraction, surface modification, and morphology control of MO nanoparticles [83–86].

To improve mechanical flexibility of metal oxide (MO) films, polymers such as poly(4-vinylphenol) (PVP), polytetrafluoroethylene (PTFE), and polyethylenimine (PEI) were utilized as doping agents to improve flexibility, as well as to form the amorphous phase of MO [35,87–90]. For example, Yu et al. developed a new low temperature approach to high-mobility amorphous metal oxide semiconductor films via doping with an insulating polymer, poly(4-vinylphenol) (PVP), to fabricate amorphous MO: polymer blend composites, as depicted in Figure 3a [91]. It should be noted that PVP possesses excellent solubility in the In_2O_3 precursor solution and their hydroxyl groups favor coordination with the MO lattice. Such an approach effectively prevents crystallization, controls the carrier concentration in the In_2O_3 channel, and retains conducting pathways for efficient charge transportation. In greater detail, all-amorphous and transparent bottom-gate top-contact thin-film transistors (TFTs) were fabricated via spin-coating of In_2O/PVP precursor solutions on AryLite substrates and annealing at 225–250 °C. They exhibited high transparency (< 80%) and low sheet resistance (< F Ω sq^{-1}). In_2O_3: 5% PVP TFTs exhibited electron mobilities of 11 cm^2 V^{-1} s^{-1}. As the amount of PVP content increases, the In_2O_3 films become amorphous even with 1 wt % of PVP, as confirmed by grazing incidence X-ray diffraction (GIXRD)(Figure 3b). V_T shifts to a positive value and the mobility slightly decreases upon incorporation of PVP, as evidenced in Figure 3c, owing to the carrier concentration modulation from PVP-induced electron traps. The bending/relaxation measurement is to characterize durability of flexible films. A film is bended and relaxed several times with defined radius and then electronic properties are measured. It is worth noting that smaller radius is for more harsh condition; the bending radii that are required for flexible, rollable, and foldable displays are 0r, 10r, and 1r, respectively [92]. The bending tests indicate that the In_2O_3: 5%PVP hybrid films exhibit only a slight decrease in the mobility from 10.9 to 8.9 cm^2 V^{-1} s^{-1} as the bending radius decreases to 10 mm, while the pristine In_2O_3 films, in stark contrast, show dramatic deterioration of the mobility from 22.2 to 0.5 cm^2 V^{-1} s^{-1} (Figure 3d). Importantly, the value retains up to ca. 90% of their performance even after undergoing repeated mechanical stress (bending/relaxing 100 times).

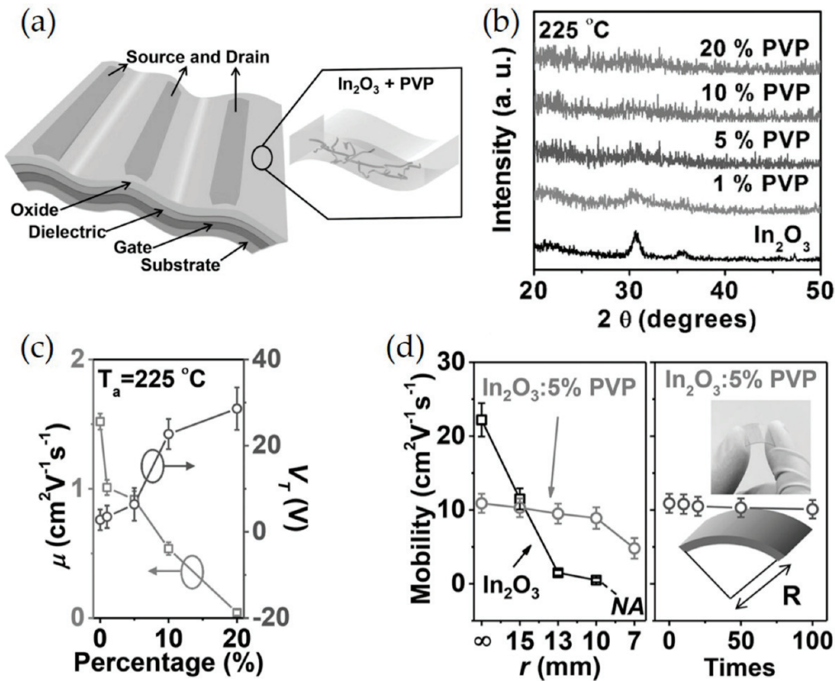

Figure 3. (**a**) Schematic representation of the flexible, transparent TFT structure based on a metal oxide:polymer (In_2O_3: x% PVP) semiconductor blend. (**b**) X-ray diffraction (XRD) patterns of In_2O_3: polymer films with various PVP concentrations: annealing at 225 °C. (**c**) TFT mobility and threshold voltage for In_2O_3: polymer films having different PVP concentrations, processed at 225 °C. (**d**) Dependence of TFT mobilities on bending radius of both neat In_2O_3 TFTs and all-amorphous In_2O_3: 5% PVP TFTs (left), and mobilities on all-amorphous TFT bending cycles at a radius of 10 mm. Inset: Optical image of transparent flexible TFTs. Reproduced with permission from [91], Copyright 2015 Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim.

Polyethylenimine (PEI) is a commercially available polymer capable of efficient n-doping due to the electron-donating nature of the tertiary amine groups (Figure 4a). PEI electron doping has been reported for several organic semiconductors and is widely used in organic photovoltaic cells and transistors to enhance the charge transportation in other organic materials. In this context, Huang et al. fabricated In_2O_3 / PEI TFT devices via doping of metal oxides with PEI [93]. Doping of In_2O_3 with PEI effectively prevents crystallization of MOs, controls the carrier concentration in the In_2O_3 channel, and increases the electron mobility of the In_2O_3 matrix. In greater detail, a PEI-doped In_2O_3 blend (i.e., aqueous PEI-In_2O_3 precursor solutions) was coated on Si substrates with 300 nm SiO_2, followed by annealing at 250 °C for 30 min. The addition of PEI successfully inhibits the formation of crystalline structure, which is unfavorable for application in flexible devices as characterized by GIXRD in Figure 4b. The characteristic peaks at 22.1°, 31.1°, 36.0°, and 46.3° ascribed to crystalline In_2O_3 are strongly suppressed even with a PEI concentration of >1%. Extended X-ray absorption fine structure (EXAFS) measurements correlate the effect of PEI with the TFT mobility. The coordination number (CN) of In-O at the first shell remains intact independent of the PEI doping concentrations, while the second shell CN exhibits the PEI content dependency, decreasing from 6 to 4.05 as the PEI concentration increases (Figure 4c). This indicates that PEI disrupts the formation of lattices, and thus electron conduction pathways. The devices fabricated with polymer concentration of 1–1.5% resulted

in excellent mobility up to 9 $cm^2 V^{-1} s^{-1}$ and high on/off ratio of 10^7, while that fabricated with pure In_2O_3 only exhibited a maximum value of 9 $cm^2 V^{-1} s^{-1}$ (Figure 4d). It is because the electron donating nature of PEI results in doping of In_2O_3 and matrix film microstructure tuning, yielding high mobilities alongside optimal off-current (I_{off}) and threshold voltage (V_{th}).

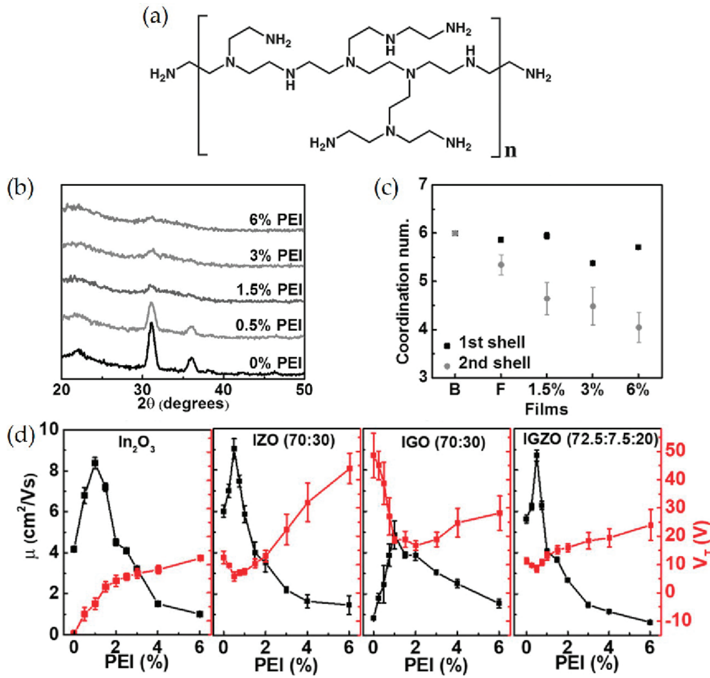

Figure 4. (**a**) Chemical structure of PEI. (**b**) GIXRD patterns of In_2O_3: x% PEI blend films with differing PEI concentrations. (**c**) Derived coordination number, In-O bond lengths for the indicated films. (**d**) TFT mobility and threshold voltage for In_2O_3: *x* wt % PEI (250 °C), IZO: *x* wt % PEI, IGO: *x* wt % PEI, and IGZO: *x* wt % PEI, as a function of the polymer concentration. $T_{annealing}$ = 300 °C. Reproduced with permission from [93], Copyright, 2016 Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim.

The same research group also investigated the charge transportation and film microstructure evolution of PEI-doped amorphous Zn- and/or Ga-incorporated In_2O_3 thin films [94]. PEI doping generality was expanded from binary In_2O_3 to ternary (e.g., In + Zn in IZO, In + Ga in IGO) and quaternary (e.g., In + Zn + Ga in IGZO) metal oxide matrices. PEI-metal oxide precursor solutions on Si wafers with 300 nm wide thermally grown SiO_2 layers were first spin-casted and then thermally annealed at 300 °C. In this study, the effect of PEI doping concentration and the addition of secondary ions (Ga and Zn) to In_2O_3 on the device performance was investigated. It was found that the incorporation of Zn and PEI in In_2O_3 and IGO led to an increase in the surface roughness, thereby degrading the charge transport properties. The crystallinity of In_2O_3 or IG(Z)O was effectively suppressed and it was observed to monotonically decrease as the PEI concentration was increased. The layer formed adjacent to the dielectric improves the efficiency of charge transportation in a channel when PEI content is low because of trap prefilling. When PEI concentration exceeds a certain threshold, the mobility of the resulting devices begins to decrease due to the disruptions in film continuity and increased trap sites.

Na et al. demonstrated flexible IGZO:PTFE TFTs with improved stability and endurability against water exposure using the facile method of blending the MO semiconductor with polytetrafluoroethylene

(PTFE) via plasma polymerization [95]. In greater detail, the IGZO: PTFE layer was co-sputtered with radio frequency magnetron sputtering processes. The hydrophobic nature of PTFE enhances device performance (μ_{FE} exceeding 10 cm^2 V^{-1} s^{-1}) and stability (a V_{th} shift of 0.68 V after an hour of immersion in water) by preventing the adsorption of water molecules on the back surface of TFTs (Figure 5a). Such an approach also improves the electrical stability of IGZO: PTFE TFTs in positive bias stress (PBS), positive bias temperature stress (PBTS), positive bias illumination stress (PBIS), negative bias stress (NBS), negative bias temperature stress (NBTS), and negative bias illumination stress (NBIS) stability tests. Indeed, V_{th} of IGZO: PTFE TFT remains steady, with only a shift of 0.68 V, while that of IGZO TFTs exhibits significant negative shifts by 12.17 V, as depicted in Figure 5b,c. The improved mechanical flexibility resulting from the soft nature of PTFE enhances the mechanical durability, as depicted in Figure 5d. Specifically, the IGZO: PTFE TFT can retain its performance with no substantial change in its electrical characteristics (a V_{th} shift of 0.89 V from 3.95 to 3.06 V) over 10000 bending cycles with a bending radius of 5 mm. In contrast, the IGZO TFTs exhibit a significant V_{th} shift of 5.45 V, from 3.07 to −2.38 V.

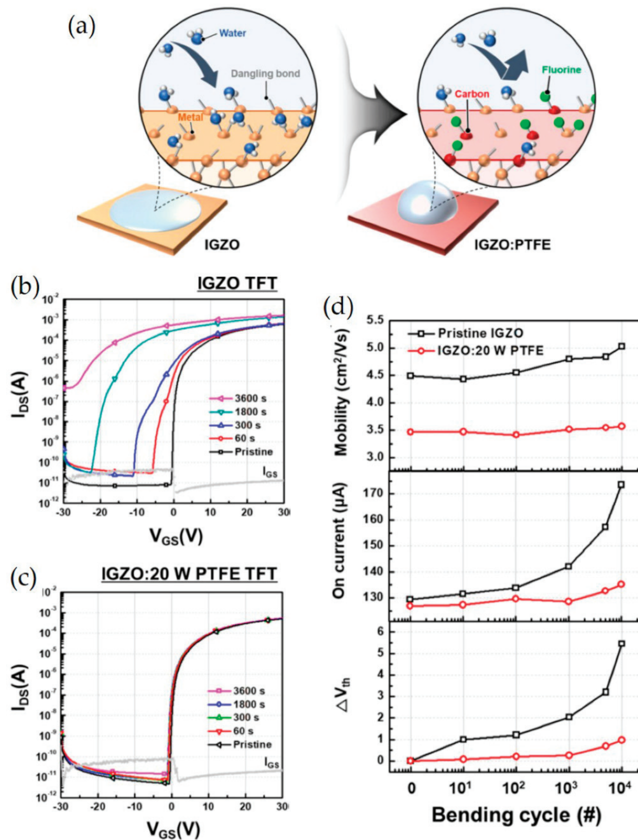

Figure 5. (**a**) Schematic illustration of improved hydrophobicity of the IGZO: PTFE film. Transfer characteristics of (**b**) the IGZO TFT and (**c**) the IGZO: 20 W PTFE TFT upon exposure to water for different times. (**d**) Variations of mobility (μ_{FE}), on-current, and V_{th} for IGZO and IGZO: 20 W PTFE TFTs with respect to bending cycles. Reproduced permission from [95], Copyright, 2018, American Chemical Society.

Sun et al. reported a strategy to control the geometry and enhance device performance of inkjet-printed MOTFT arrays via the addition of an insulating polymer to the precursor solution prior to film deposition [96]. To prevent the formation of a non-uniform geometry during inkjet-printing, the polymer additive, polystyrene (PS) was utilized. It was reported that the addition of high viscous polymers is favorable to eliminate coffee ring effects by significantly reducing the solute mobility and thus suppressing outward capillary flow of solute to the edge. In detail, PS, with different molecular weights ranging from 2000 to 2,000,000, was mixed with indium precursors (i.e., indium nitrate hydrate) and then printed on silicon substrates, followed by annealing at 225 °C for 1 h. Interestingly, 202 with an increase in PS MW, the coffee ring effect gradually faded, as measured by optical microscope in Figure 6a. The change in surface morphology by varying PS MW is attributed to the suppressed capillary flow and the Marangoni effect. The relative viscosities of In_2O_3/PS precursor solutions to those of pristine In_2O_3 solution are 1.02, 1.17, 1.39, and 1.31 for PS with MW of 2000, 20,000, 200,000, and 2,000,000, respectively. Evidently, the use of PS with MW of 20,000 results in smooth films as the increased viscosity inhibits the capillary flow, thus facilitating the depinning of the contact line. The incorporation of PS results in the improvement of carrier mobility from 4.2 $cm^2\ V^{-1}\ s^{-1}$ up to 13.7 $cm^2\ V^{-1}\ s^{-1}$ as PS MW increases from 2000 to 2,000,000, which is about three times that of the pristine In_2O_3 TFTs (Figure 6b). The trap densities for pristine, PS Mw of 2000, 20,000, 200,000, and 2,000,000 were 2.4×10^{12}, 1.2×10^{12}, 1.1×10^{12}, 1.0×10^{12}, and 1.1×10^{12} $cm^{-2}\ eV^{-1}$, respectively. XPS characterization shows that the incorporation of PS obviously impacts local bonding of MO:PS blends, thereby increasing M-O concentration (Figure 6c). Grazing incidence X-ray diffraction indicates that the addition of PS favors the formation of amorphous phase and enhances the M-O lattice contents, both of which facilitate the carrier transportation.

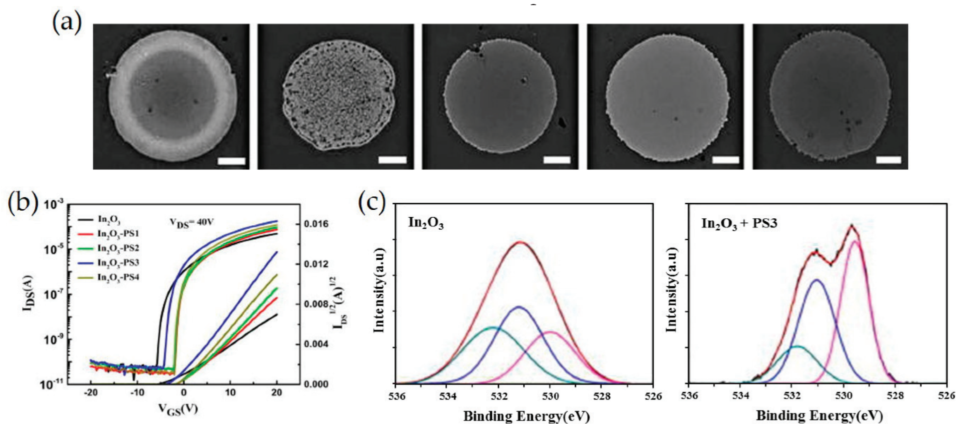

Figure 6. (**a**) Optical microscopy images of In_2O_3 deposition (right to left) without PS, with PS1, with PS2, with PS3, and with PS4. The scale bar is 100 µm. (**b**) Transfer characteristics of inkjet-printed TFTs. (**c**) X-ray photoelectron spectroscopy (XPS) of O 1s spectra. Reproduced with permission from [96], Copyright 2018, American Institute of Physics.

3.2. Dielectric Layers

MOs have been considered to be a crucial component in thin-film electronic systems due to their outstanding electrical and mechanical properties [97–104]. However, the MOs lack flexibility, which limits their use in flexible electronics [105]. Thus far, most thin high-k inorganic metal oxide dielectrics have been fabricated via conventional vacuum-based techniques including pulsed laser deposition (PLD), atomic layer deposition (ALD), magnetron sputtering, and e-beam evaporation. However, these methods are costly and unsuitable to produce large-area flexible oxide electronics. For example, high-quality gate dielectric SiO_2 films are produced via expensive vacuum-based

plasma-enhanced chemical vapor deposition (PECVD) at high temperatures above 300 °C. It is worth noting that such high temperatures may cause deformation or warping of flexible substrates. Although high performances have been achieved, flexibility and stability still limit their application in real products such as wearable devices. Moreover, dielectric layers (e.g., SiO_2) are vulnerable to mechanical stress notwithstanding their extremely thin width, yielding cracks or delamination under mechanical deformation even at small bending radii. In this context, organic dielectrics have garnered substantial attention in the area of flexible devices owing to their flexibility, mechanical stability, low temperature, easy solution processability, and excellent compatibility with flexible organic substrates, despite their low k value [105–110]. Therefore, hybridization of organic and inorganic materials can lead to the improvement in flexibility, dielectric constant, and mechanical toughness of gate dielectric materials [111–119]. The transistor parameters critically depend on the interface formed between dielectric and semiconductor layers since the trapped charges strongly impact the electrical behavior. The hybrid gate dielectrics tend to be compatible with either organic or inorganic semiconductors. As the inorganic constituent, high-k inorganic nanoparticles such as ZrO_2, Al_2O_3, Y_2O_3, Ta_2O_5, and TiO_2 were usually embedded in a polymeric matrix such as poly(methylmethacrylate) (PMMA) and poly(vinylpyrrolidone) [120–122]. However, the inorganic nanoparticles tend to agglomerate, increasing the surface roughness of the hybrid layers, resulting in high gate leakage current and low on/off current ratio. In this section, the development of hybrid organic–inorganic composites with low power consumption, low operating voltage, and compatibility with transparent flexible electronics for the use in dielectric layers will be summarized.

Poly(methyl methacrylate) (PMMA) is an important thermoplastic polymer with excellent transparency, a refractive index of n = 1.49, good chemical resistance, thermal stability, mechanical flexibility, low cost, and a lower dielectric constant (2.9) than that of silicon oxide material (3.9) [123–126]. As a result, PMMA has been mixed with high-k inorganic nanoparticles such as ZrO_2, Al_2O_3, and TiO_2 to provide high optical transparency, low weight, mechanical flexibility, and formability [14,127,128]. The low temperature deposition process towards PMMA-ZrO_2 nanocomposites as dielectric gate layers has been reported [129]. Intriguingly, to prevent phase separation, inorganic oxides were cross-linked with PMMA and trimethoxy-silyl-propyl-methacrylate (TMSPM) molecules that are chemically compatible with both inorganic and organic phases. In greater detail, TFT devices with a ZnO/PMMA-ZrO_2/ITO/glass structure (Figure 7a) were fabricated and their electrical properties, such as threshold voltage, channel mobility, and I_{on}/I_{off} current ratio, were investigated. A hybrid dielectric layer was prepared via a sol−gel reaction among zirconium propoxide (ZP), TMSPM, and methylmethacrylate (MMA) precursors at variable TMSPM molar ratios. The devices fabricated with 0.3 M TMSPM exhibit a mobility of 0.48 cm^2/V s, on/off ratio of 10^6–10^7, and a threshold voltage of 3.3 V. The leakage current density increases from 10^{-6} to 10^{-5} A/cm^2 as the amount of TMSPM content increases in the hybrid insulating layer, as illustrated in the current density versus electric field characteristic curves (Figure 7b). Importantly, the threshold voltage of the devices decreases from 3.3 V to 0.9 V with an increase in the TMSPM amount from 0.3 M to 0.75 M, as measured by transfer curves in Figure 7c. This feature is advantageous for low power consumption.

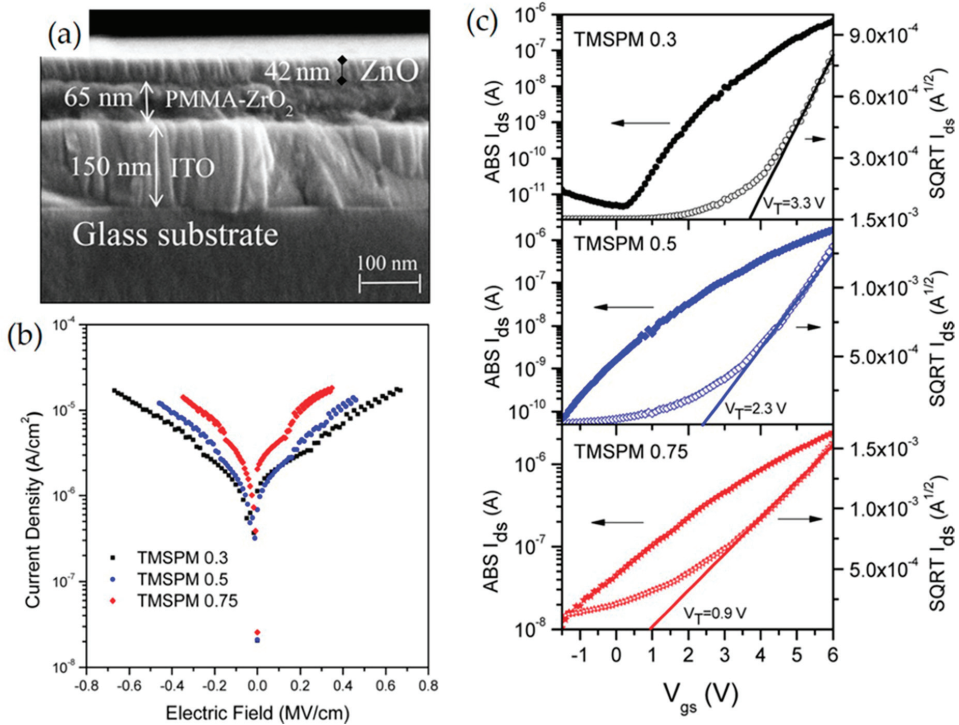

Figure 7. (**a**) SEM image of the TFT cross section, where the PMMA−ZrO_2 layer was deposited with 1:0.3:1 molar ratio. (**b**) Leakage current density vs. electric field of the PMMA–ZrO_2 hybrid layers deposited with different TMSPM molar ratios. (**c**) Transfer characteristics for ZnO-based transistors with PMMA–ZrO_2 as gate dielectric hybrid films at different TMSPM molar concentrations. Reproduced with permission from [126], Copyright 2017, American Chemical Society.

Yttrium oxide (Y_2O_3) nanoparticles exhibit a wide band gap of 6.0 eV, which is advantageous to the aspects of illumination stability of TFTs [130]. In this context, TFTs were fabricated on polyimide (PI) substrates using cross-linked poly(4-vinylphenol) (c-PVP)/ Y_2O_3 nanocomposites as gate insulators [131]. The architecture of the flexible devices was Ag/6,13-bis(triisopropylsilylehtynyl)pentacene(TIPS-pentacene)/ c-PVP:Y_2O_3/c-PVP/PI. In greater detail, the cross-linkable PVP was prepared by dissolving PVP and a cross-linking agent, (methylated poly(melamine-co-formaldehyde), MMF) in propylene glycol methyl ether acetate (PGMEA). TFTs with c-PVP:Y_2O_3 hybrid dielectric exhibited an on-state drain current of −0.165 µA at a gate voltage of −40 V, which is higher than that of devices with only c-PVP (−0.0462 µA), as depicted in Figure 8a,b. However, as illustrated in Figure 8c,d the c-PVP/Y_2O_3 composite films exhibited a higher roughness compared to the c-PVP films, leading to a larger interference in hole conduction at the interface between the insulator and the semiconductor. Additionally, c-PVP: Y_2O_3-based TFTs exhibited a greater number of leakage paths for the gate current compared to c-PVP-based TFTs, possibly owing to several interactions like i) the attraction of hole carriers by the highly polarized Y_2O_3 nanoparticles, ii) flow along the direction of the gate electric field, and iii) repulsion by the positive side and attraction by other adjacent side of the Y_2O_3 nanoparticles (Figure 8e–g).

Kim et al. have introduced TiO_2-polymer composites via cross-linking reactions of these two constituents with low surface energy which allows vertical growth of organic molecules (e.g., pentacene) [132]. In greater detail, a TiO_2 precursor (titanium(IV) butoxide and acetyl acetone)

and poly(4-vinylphenol) (PVP) solution (PVP, poly(melamine-co-formaldehyde) methylated/butylated and propylene glycol methyl ether acetate (PGMEA) solvent) mixture were spin-coated on ITO substrates and then annealed at 200 °C for 1 h. Interestingly, poly(melamine-co-formaldehyde) methylated/butylated acts as the cross-linker, which reacts with the hydroxyl group of the PVP and the ligands of the TiO_2, forming a dense structure. The resulting device exhibits a charge carrier mobility of 0.105 cm^2 V^{-1} s^{-1}, on/off ratio of 10^3, and a leakage current of 10^{-7} A cm^{-2} at ±5 V due to such a dense structure. Furthermore, this homogeneous TiO_2-polymer composite solution is stable in ambient conditions. Bang et al. fabricated bottom-gate ZnO-thin film transistors using PVP/Al_2O_3 dielectrics and investigated the effects of an organic/inorganic dielectric on device performance [133]. The leakage current of the PVP/Al_2O_3 dielectric improved by three times over the PVP counterparts. The saturation mobility of PVP/Al_2O_3 TFTs also improved from 0.05 to 0.8 cm^2 V^{-1} s $^{-1}$ compared to PVP TFTs.

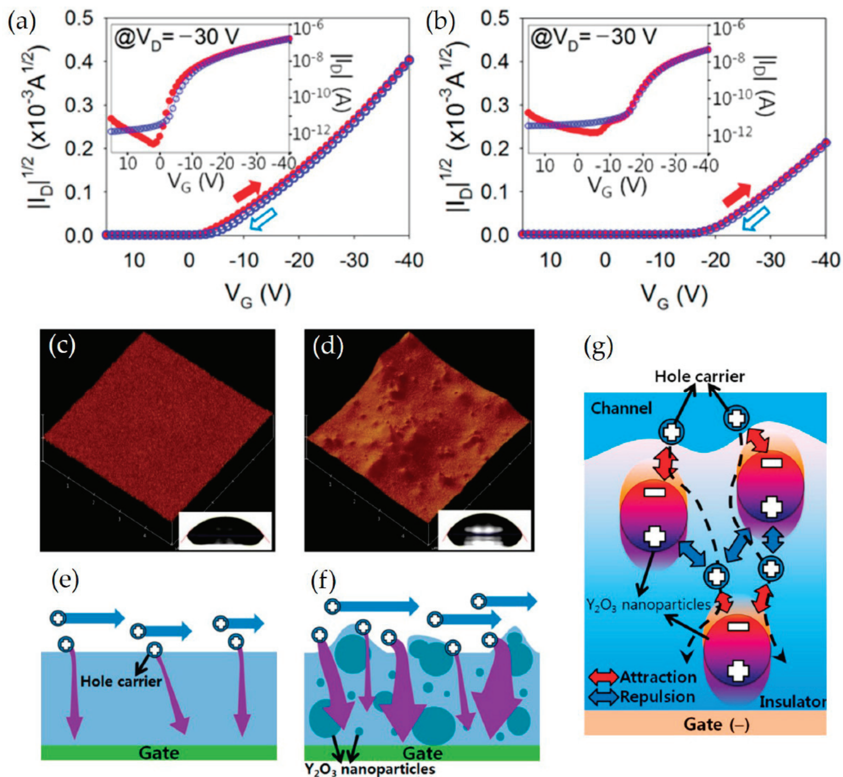

Figure 8. $|I_D|^{1/2}$ vs. V_G plots of TIPS-pentacene TFTs with the (**a**) c-PVP/Y_2O_3 composite and (**b**) c-PVP gate insulators. AFM images of the (**c**) c-PVP and (**d**) c-PVP/Y_2O_3composite films. The insets show the contact angles on both films. Leakage current paths through the (**e**) c-PVP/Y_2O_3 composite and (**f**) c-PVP gate insulators. (**g**) Possible interaction between the holes and the Y_2O_3 nanoparticles in the c-PVP/Y_2O_3 composite insulator. Reproduced with permission from [131], Copyright 2016, MDPI, Basel, Switzerland.

Despite superior mechanical flexibility, organic materials as gate insulators, such as poly-4-vinylphenol (PVP) and polymethyl methacrylate (PMMA), exhibit very low capacitance compared to inorganic dielectrics. In this context, several approaches to improve the capacitance have been introduced. This includes reducing the thickness of dielectric films and incorporating high-k inorganic nanoparticles. However, the use of ultra-thin organic dielectrics often resulted

in structural imperfections, producing current leakage. Kim et al. proposed a novel vapor-phase synthesis method to form an ultrathin, homogeneous, high-k organic−inorganic hybrid dielectric [134]. Hybrid dielectrics are synthesized via initiated chemical vapor deposition (iCVD) in a one-step manner (Figure 9a). This method utilizes 2-hydroxyethyl methacrylate and trimethylaluminum as the monomer and the inorganic precursor, respectively. A uniform and defect-free hybrid dielectric layer with precise thickness below 20 nm and composition can be produced. The hybrid films are formed via following subsequent steps—the injection of vaporized monomers, precursors, and initiators, the thermal decomposition of initiators to form free radicals, the adsorption of monomers and precursors, and free-radical polymerization of monomers. The hybrid dielectric exhibits a high k-value of 7 and a low leakage current density of less than 3×10^{-7} A/cm^2 at 2 MV/cm, even with a thickness of less than 5 nm. The capacitance (C_i) versus electric field and the current density (J) versus electric field characterizations corresponding to varying hybrid film thicknesses were also investigated, as illustrated in Figure 9b. As the thickness decreases, the C_i and J values reach 250 nF/cm^2 and 1×10^{-7} A/cm^2, respectively. The n- and p-type OTFTs were fabricated using the hybrid dielectric deposited via the iCVD process and their charge-transfer curves were studied, as depicted in Figure 9c,d. The hybrid dielectric offered a superior interface between the channel and dielectric and thus induced ideal charge-transfer characteristics. Both n- and p-type OFETs with the hybrid dielectric exhibited no apparent hysteresis and a low leakage current density (<3×10^{-7}A/cm^2 at 2 MV/cm). Furthermore, the dielectric layer exhibited improved chemical stability without any degradation in its dielectric performance. Interestingly, the hybrid dielectric layer retained its excellent dielectric performance under tensile strains of up to 2.6%.

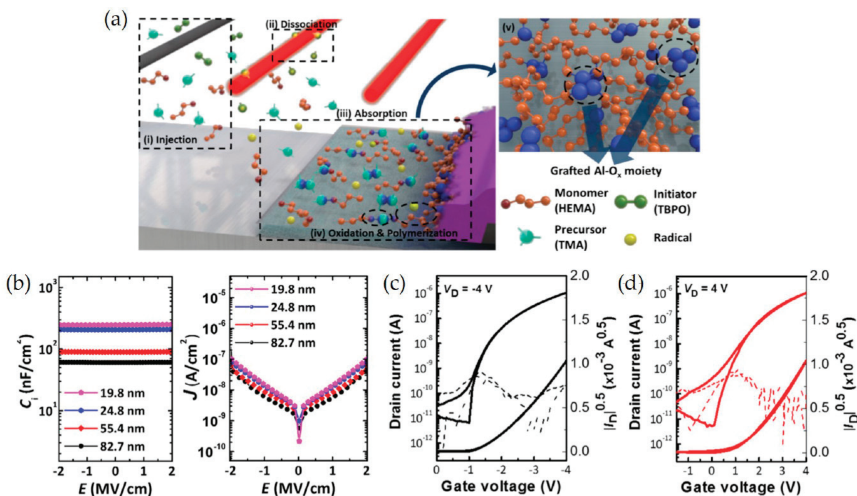

Figure 9. Vapor-phase synthesis of organic–inorganic hybrid dielectrics via iCVD. (**a**) A schematic of the synthesis process: (**i**) Vaporized monomers, organometallic precursor, and initiators are injected. (**ii**) The initiators were thermally decomposed near the heated filament to form radicals (red lines), which are positioned away from the substrate. (**iii**) Monomers, precursor, and radicals were absorbed on the heated substrate. (**iv**) The adsorbed monomers were polymerized and simultaneously reacted with inorganic precursors. (**v**) Uniform dispersion of the inorganic oxides can be achieved in the polymer matrix. (**b**) C_i–E(left), and J–E(right) characteristics of the MIM devices with the hybrid dielectrics (Al concentration: 17.8%) with various thicknesses of 82.7, 55.4, 24.8, and 19.8 nm, respectively. Charge-transfer characteristics of the (**c**) pentacene and (**d**) PTCDI-C13 OTFTs, respectively. Hybrid films 25 and 34 nm thick were used as the gate dielectric for pentacene and PTCDI-C13 OTFTs, respectively. Reproduced with permission from [134], Copyright 2018, American Chemical Society.

The effects of the device architecture on indium zinc oxide (IZO) TFTs with poly(4-vinylphenol-co-methylmethacrylate) (PVP-co-PMMA) gate insulators were investigated [135]. The top gate IZO TFTs exhibited the improved μ_{FE}, SS, V_{th}, and good Ion/off ratio of 8.5 $cm^2 V^{-1} s^{-1}$, 2.0 V per decade, -10.0 V, and 10^7, respectively, compared to the bottom gate IZO TFTs (μ_{FE}, SS, V_{th}, and Ion/off ratio were 9.0 $cm^2 V^{-1} s^{-1}$, 5.0 V per decade, −12.5 V, and 2×10^5, respectively). This is attributed to the energetic ion bombardment in the polymer gate dielectric layer during the sputtering process. The device performance can be further improved by doping the hybrid PVP-co-PMMA gate dielectric with ZrO_2: the μ_{FE}, SS, V_{th} and $I_{on/off}$ ratio in this case were 28.4 $cm^2 V^{-1} s^{-1}$, 0.70 V per decade, −2.0, and 4.0×10^7, respectively.

To improve surface contact with organic molecules and increase dielectric properties, a bilayer structure was introduced. For example, Held et al. fabricated a bilayer hybrid dielectric consisting of a high-k hafnium oxide (HfO_x)/thin PMMA layer with a donor-acceptor polymer, poly(2,5-bis(2-octyldodecyl)–3-(5–(thieno[3,2-b]thiophen-2,5-yl)thiophen-2-yl)–6-(thiophen-2,5-yl)pyrrolo[3,4-c]pyrrole-1,4(2H,5H)-dione) (DPPT-TT) or single-walled carbon nanotubes (SWNTs) as the semiconductor [136]. PMMA layers were spin-casted and hafnium oxide layers were deposited via ALD. The resulting FETs exhibited drastically reduced operating voltages. The PMMA/HfOx hybrid dielectric exhibited low-voltage operation, well-balanced charge carrier transport, low trap densities, and excellent bias stress stability as PMMA ensures a low density of trap states at the semiconductor dielectric interface and HfO_x layers provide high capacitance (Figure 10a). Moreover, the effects of a hybrid dielectric layer for SWNT-FETs were investigated. The SWNT-FETs with only HfO_x dielectric layer exhibit strong threshold shift and hysteresis, as observed in the transfer characteristics (Figure 10b). In contrast, ambipolar transfer characteristics without hysteresis was observed in SWNT-FETs with the hybrid dielectric (Figure 10c). According to bias stress tests, SWNT-FETs with hybrid dielectric exhibit constant on-currents without any noticeable degradation over 10 h, while SWNT/HfO_x FETs suffer an on-current decay of an order of magnitude recorded in Figure 10d.

High performance low-voltage pentacene-based organic TFTs with pentacene/PMMA/Al_2O_3/ITO architecture were fabricated and their electronic characteristics were investigated [137]. In this study, a high-k metal oxide dielectric, Al_2O_3, was used due to its excellent dielectric constant (k = 7.0~9.0) and large bandgap (Eg = 8.45~9.9 eV). PMMA renders improved interfacial properties between Al_2O_3 and organic pentacene. The OFETs with only an Al_2O_3 layer exhibited a field-effect mobility of 0.65 cm^2/Vs, a threshold voltage of −0.6 V,I_{on}/I_{off} ratio of 4×10^3, and a sub-threshold swing of 0.45 V/dec, at operating voltages as low as −4 V. After being modified by PMMA, the mobility increased from 0.65 to 0.84 cm^2/Vs.

Poly(α-methylstyrene) (PαMS) was also applied on top of zirconium oxide (ZrO_2) layers to improve the quality of the interfaces between ZrO_2 and organic semiconductors [138]. In greater detail, a ZrO_2 film was synthesized on Si via a chemical solution process and annealed at temperatures between 400 and 700 °C. PαMS or HMDS layers were then spin-casted and made to undergo vacuum evaporation with pentacene. It was found that the surface modifications greatly affect the electrical performance of the ZrO_2 OTFTs. The surface energy deceased after surface modification and the calculated values are 43.9, 37.8, and 35.5 mJ/m^2 for bare-ZrO_2, HMDS-ZrO_2, and PαMS-ZrO_2, respectively, as depicted in Figure 11a–c. The PαMS modified devices exhibited a higher carrier mobility and on/off ratio than those fabricated with bare ZrO_2 and HMDS-coated ZrO_2 because the PαMS/ZrO_2 layers provide a low surface energy and thus promote the growth of large pentacene crystals. In particular, the carrier mobility of the devices with PαMS-modified ZrO_2 were observed to increase remarkably from 0.08 to 0.51 cm^2/Vs, whereas the carrier mobilities of the devices with bare ZrO_2 and HMDS-modified ZrO_2 remained at values of ~0.06 and ~0.11 cm^2/Vs, respectively, while the dielectric constant of ZrO_2 was increased from 12.17 to 19.70 (Figure 11d). Furthermore, PαMS/ZrO_2 OTFTs fabricated on flexible polyethyleneterephthalate (PET) substrate were demonstrated, as depicted in Figure 11e,f. The flexible OTFTs exhibited typical I_{DS}-V_{GS} curves of the ZrO_2-OFET, exhibiting a ~10^5 on/off-current ratio between +1 V and −5 V of V_{GS} (Figure 11g).

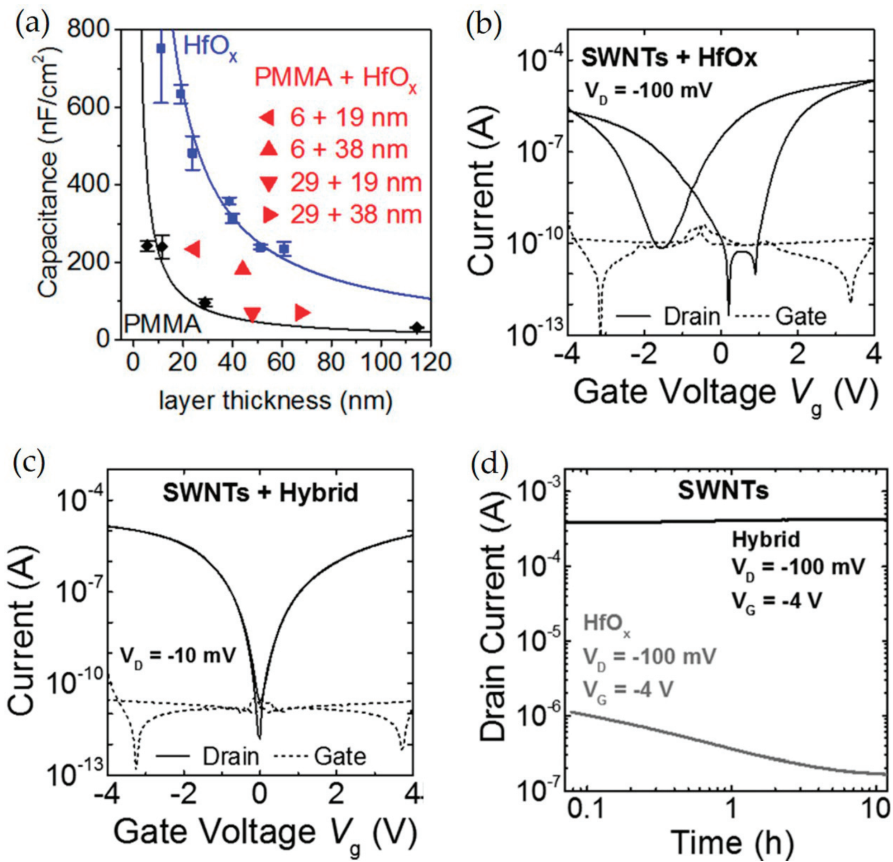

Figure 10. (**a**) Capacitance as a function of total layer thickness for hafnium oxide, PMMA, and hybrid dielectric. Transfer characteristics of network SWNT FETs with (**b**) HfO*x* and (**c**) hybrid dielectric. Channel width/length ratio and channel lengths were 125 and 40 μm, respectively. (**d**) Bias stress tests of SWNT-based transistors with different dielectrics. Reproduced with permission from [136], Copyright 2015 American Institute of Physics.

Ha et al. have reported on low-voltage OTFTs employing solution-processed hybrid bilayer gate dielectric of high-k ZrO_2 and low-k amorphous fluoropolymer, CYTOP [139]. The thin hydrophobic CYTOP layer repels aqueous molecules from an organic active layer. Therefore, such device architecture improves electronic characteristics including field effect mobility (from 0.18 to 0.28 cm^2/Vs), threshold voltage (V_{th}, from 0.4 to -0.1 V), and sub-threshold (S.S., 0.57 to 0.28 V/decade) compared to only high-k ZrO_2 devices. The reduction in defect-states at the interface suppresses photo-induced hysteresis and enhances the stability of device performance against electric bias-stress.

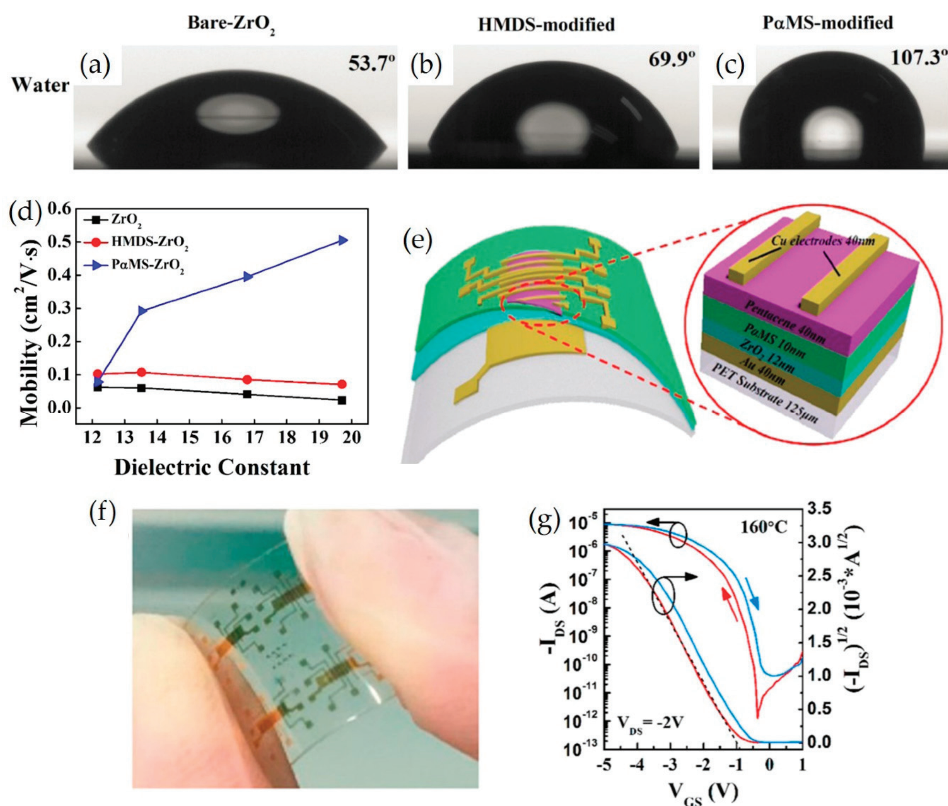

Figure 11. Water contact angles of (**a**) bare-ZrO_2 surface, (**b**) HMDS modified surface, (**c**) PαMS modified surface. (**d**) Field effect hole mobility as a function of ZrO_2 dielectric constant for OFETs with different surface modifications. The mobility was calculated with $V_G = -5$ V and capacity density under $f = 1$ kHz. (**e**) Schematic diagram of the flexible OTFT fabricated on PET substrate and (**f**) the digital photograph of the flexible OTFTs. (**g**) I_{DS}–V_{GS} transfer curves of a ZrO_2-OFET constructed on PET flexible substrate. The channel width and length of the transistor are 750 μm and 50 μm, respectively. Reproduced with permission from [138], Copyright 2016 American Chemical Society.

4. Summary and Outlook

In summary, we first give an overview of the development in polymer/metal oxide nanocomposites for applications in flexible charge transport channels and dielectrics. Recently, metal oxides (MOs) have been fabricated via vacuum-based techniques including pulsed laser deposition (PLD), atomic layer deposition (ALD), magnetron sputtering, and e-beam evaporation, for use in flexible and transparent charge transport channels. Despite their ultra-thin width, only inorganic MO films are vulnerable to repeated mechanical deformation. As a response to low mechanical durability and flexibility, hybrid polymer/MO nanocomposites have been introduced. Hybridization with soft organic materials have proven to be an effective strategy that not only offers mechanical flexibility but also enables solution-based fabrication.

Organic dielectrics have garnered substantial attention owing to their flexibility, mechanical stability, solution processability, and excellent compatibility with flexible organic substrates. However, the low k values of such materials prohibit their application in practical electronic devices. Thereby, high-k inorganic MOs have been employed as fillers. Considering that most of the flexible substrates

and semiconductors are organic materials, hybrid gate dielectrics tend to provide good compatibility with organic substrates and semiconductors.

Despite significant advances in flexible electronics by using polymers, many challenges remain to be surmounted, including poor mechanical durability, low charge-carrier mobility, and low dielectric constants. However, we believe that hybrid nanocomposites will reach their full potential in flexible electronics in the near future, as various methods to overcome their weaknesses are being continuously explored.

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References

1. Ju, S.; Facchetti, A.; Xuan, Y.; Liu, J.; Ishikawa, F.; Ye, P.; Zhou, C.; Marks, T.J.; Janes, D.B. Fabrication of Fully Transparent Nanowire Transistors for Transparent and Flexible Electronics. *Nat. Nanotechnol.* **2007**, *2*, 378. [CrossRef]
2. Park, S.; Vosguerichian, M.; Bao, Z. A Review of Fabrication and Applications of Carbon Nanotube Film-Based Flexible Electronics. *Nanoscale* **2013**, *5*, 1727–1752. [CrossRef] [PubMed]
3. McCoul, D.; Hu, W.; Gao, M.; Mehta, V.; Pei, Q. Recent Advances in Stretchable and Transparent Electronic Materials. *Adv. Electron. Mater.* **2016**, *2*, 1500407. [CrossRef]
4. Khang, D.-Y.; Jiang, H.; Huang, Y.; Rogers, J.A. A Stretchable Form of Single-Crystal Silicon for High-Performance Electronics on Rubber Substrates. *Science* **2006**, *311*, 208–212. [CrossRef] [PubMed]
5. Kim, D.H.; Kim, Y.S.; Wu, J.; Liu, Z.; Song, J.; Kim, H.S.; Huang, Y.Y.; Hwang, K.C.; Rogers, J.A. Ultrathin Silicon Circuits with Strain-Isolation Layers and Mesh Layouts for High-Performance Electronics on Fabric, Vinyl, Leather, and Paper. *Adv. Mater.* **2009**, *21*, 3703–3707. [CrossRef]
6. Faraji, S.; Danesh, E.; Tate, D.J.; Turner, M.L.; Majewski, L.A. Cyanoethyl Cellulose-Based Nanocomposite Dielectric for Low-Voltage, Solution-Processed Organic Field-Effect Transistors (OFETs). *J. Phys. D* **2016**, *49*, 185102. [CrossRef]
7. Schroeder, R.; Majewski, L.A.; Grell, M. High-Performance Organic Transistors Using Solution-Processed Nanoparticle-Filled High-k Polymer Gate Insulators. *Adv. Mater.* **2005**, *17*, 1535–1539. [CrossRef]
8. Cai, W.; Wilson, J.; Zhang, J.; Park, S.; Majewski, L.; Song, A. Low-Voltage, Flexible InGaZnO Thin-Film Transistors Gated with Solution-Processed, Ultra-Thin $Al_x O_y$. *IEEE Electron Device Lett.* **2018**, *40*, 36–39.
9. Majewski, L.A.; Schroeder, R.; Grell, M. One Volt Organic Transistor. *Adv. Mater.* **2005**, *17*, 192–196. [CrossRef]
10. Cai, W.; Park, S.; Zhang, J.; Wilson, J.; Li, Y.; Xin, Q.; Majewski, L.; Song, A. One-Volt IGZO Thin-Film Transistors With Ultra-Thin, Solution-Processed Al_xO_y Gate Dielectric. *IEEE Electron Device Lett.* **2018**, *39*, 375–378. [CrossRef]
11. Cai, W.; Wilson, J.; Zhang, J.; Brownless, J.; Zhang, X.; Majewski, L.A.; Song, A. Significant Performance Enhancement of Very-Thin InGaZnO Thin-Film Transistors by a Self-Assembled Monolayer Treatment. *ACS Appl. Electron. Mater.* **2020**, *2*, 301–308. [CrossRef]
12. Lu, J.; Wong, C.P. Recent Advances in High-k Nanocomposite Materials for Embedded Capacitor Applications. *IEEE. Trans. Dielectr. Electr. Insul.* **2008**, *15*, 1322–1328.
13. Liu, J.; Buchholz, D.B.; Hennek, J.W.; Chang, R.P.; Facchetti, A.; Marks, T.J. All-Amorphous-Oxide Transparent, Flexible Thin-Film Transistors. Efficacy of Bilayer Gate Dielectrics. *J. Am. Chem. Soc.* **2010**, *132*, 11934–11942. [CrossRef] [PubMed]
14. Lee, J.-W.; Ju, B.-K.; Jang, J.; Yoon, Y.-S.; Kim, J.-K. High Mobility Organic Transistor Patterned by the Shadow-Mask with All Structure on a Plastic Substrate. *J. Mater. Sci.* **2007**, *42*, 1026–1030. [CrossRef]

15. Lee, I.-Y.; Park, H.-Y.; Park, J.-H.; Yoo, G.; Lim, M.-H.; Park, J.; Rathi, S.; Jung, W.-S.; Kim, J.; Kim, S.-W. Poly-4-vinylphenol and Poly (melamine-co-formaldehyde)-Based Graphene Passivation Method for Flexible, Wearable and Transparent Electronics. *Nanoscale* **2014**, *6*, 3830–3836. [CrossRef] [PubMed]
16. Trung, T.Q.; Tien, N.T.; Kim, D.; Jang, M.; Yoon, O.J.; Lee, N.E. A Flexible Reduced Graphene Oxide Field-Effect Transistor for Ultrasensitive Strain Sensing. *Adv. Funct. Mater.* **2014**, *24*, 117–124. [CrossRef]
17. Schattka, J.H.; Shchukin, D.G.; Jia, J.; Antonietti, M.; Caruso, R.A. Photocatalytic Activities of Porous Titania and Titania/Zirconia Structures Formed by Using a Polymer Gel Templating Technique. *Chem. Mater.* **2002**, *14*, 5103–5108. [CrossRef]
18. Kim, J.H.; Hwang, B.-U.; Kim, D.-I.; Kim, J.S.; Seol, Y.G.; Kim, T.W.; Lee, N.-E. Nanocomposites of Polyimide and Mixed Oxide Nanoparticles for High Performance Nanohybrid Gate Dielectrics in Flexible Thin Film Transistors. *Electron. Mater. Lett.* **2017**, *13*, 214–221. [CrossRef]
19. Madusanka, N.; Shivareddy, S.G.; Hiralal, P.; Eddleston, M.D.; Choi, Y.; Oliver, R.A.; Amaratunga, G.A.J. Nanocomposites of TiO_2/Cyanoethylated Cellulose with Ultra High Dielectric Constants. *Nanotechnology* **2016**, *27*, 195402. [CrossRef]
20. Beaulieu, M.R.; Baral, J.K.; Hendricks, N.R.; Tang, Y.; Briseño, A.L.; Watkins, J.J. Solution Processable High Dielectric Constant Nanocomposites Based on ZrO_2 Nanoparticles for Flexible Organic Transistors. *ACS Appl. Mater. Interfaces* **2013**, *5*, 13096–13103. [CrossRef]
21. Yang, W.; Song, K.; Jung, Y.; Jeong, S.; Moon, J. Solution-Deposited Zr-doped AlO_x Gate Dielectrics Enabling High-Performance Flexible Transparent Thin Film Transistors. *J. Mater. Chem. C* **2013**, *1*, 4275–4282. [CrossRef]
22. Min, Y.-S.; Cho, Y.J.; Hwang, C.S. Atomic Layer Deposition of Al_2O_3 Thin Films from a 1-methoxy-2-methyl-2-propoxide Complex of Aluminum and Water. *Chem. Mater.* **2005**, *17*, 626–631. [CrossRef]
23. Jeong, S.; Ha, Y.G.; Moon, J.; Facchetti, A.; Marks, T.J. Role of Gallium Doping in Dramatically Lowering Amorphous-Oxide Processing Temperatures for Solution-Derived Indium Zinc Oxide Thin-Film Transistors. *Adv. Mater.* **2010**, *22*, 1346–1350. [CrossRef] [PubMed]
24. Hennek, J.W.; Smith, J.; Yan, A.; Kim, M.-G.; Zhao, W.; Dravid, V.P.; Facchetti, A.; Marks, T.J. Oxygen "getter" Effects on Microstructure and Carrier Transport in Low Temperature Combustion-Processed a-InXZnO (X = Ga, Sc, Y, La) Transistors. *J. Am. Chem. Soc.* **2013**, *135*, 10729–10741. [CrossRef] [PubMed]
25. Banger, K.K.; Peterson, R.L.; Mori, K.; Yamashita, Y.; Leedham, T.; Sirringhaus, H. High Performance, Low Temperature Solution-Processed Barium and Strontium Doped Oxide Thin Film Transistors. *Chem. Mater.* **2014**, *26*, 1195–1203. [CrossRef] [PubMed]
26. Jo, J.W.; Kim, J.; Kim, K.T.; Kang, J.G.; Kim, M.G.; Kim, K.H.; Ko, H.; Kim, Y.H.; Park, S.K. Highly Stable and Imperceptible Electronics Utilizing Photoactivated Heterogeneous Sol-Gel Metal–Oxide Dielectrics and Semiconductors. *Adv. Mater.* **2015**, *27*, 1182–1188. [CrossRef]
27. Khanal, R.; Buchholz, D.B.; Chang, R.P.; Medvedeva, J.E. Composition-Dependent Structural and Transport Properties of Amorphous Transparent Conducting Oxides. *Phys. Rev. B* **2015**, *91*, 205203. [CrossRef]
28. Nadaud, N.; Lequeux, N.; Nanot, M.; Jove, J.; Roisnel, T. Structural Studies of Tin-Doped Indium Oxide (ITO) and $In_4Sn_3O_{12}$. *J. Solid State Chem.* **1998**, *135*, 140–148. [CrossRef]
29. Jin, S.H.; Kang, S.-K.; Cho, I.-T.; Han, S.Y.; Chung, H.U.; Lee, D.J.; Shin, J.; Baek, G.W.; Kim, T.-I.; Lee, J.-H. Water-Soluble Thin Film Transistors and Circuits Based on Amorphous Indium–Gallium–Zinc Oxide. *ACS Appl. Mater. Interfaces* **2015**, *7*, 8268–8274. [CrossRef]
30. Lim, S.H.; Kim, J.; Lee, S.-G.; Kim, Y.S. Water-Soluble Polymer Dielectric with Potential for High Performance Organic Thin-Film Transistors. *Chem. Commun.* **2010**, *46*, 3961–3963. [CrossRef]
31. Byun, H.S.; Xu, Y.-X.; Song, C.K. Fabrication of High Performance Pentacene Thin Film Transistors Using Poly (4-vinylphenol) as the Gate Insulator on Polyethyleneterephthalate Substrates. *Thin Solid Films* **2005**, *493*, 278–281. [CrossRef]
32. Kim, J.-M.; Lee, J.-W.; Kim, J.-K.; Ju, B.-K.; Kim, J.-S.; Lee, Y.-H.; Oh, M.-H. An Organic Thin-Film Transistor of High Mobility by Dielectric Surface Modification with Organic Molecule. *Appl. Phys. Lett.* **2004**, *85*, 6368–6370. [CrossRef]
33. Wei, Q.; You, E.; Hendricks, N.R.; Briseno, A.L.; Watkins, J.J. Flexible Low-Voltage Polymer Thin-Film Transistors Using Supercritical CO_2-Deposited ZrO_2 Dielectrics. *ACS Appl. Mater. Interfaces* **2012**, *4*, 2322–2324. [CrossRef] [PubMed]

34. De Angelis, F.; Cipolloni, S.; Mariucci, L.; Fortunato, G. High-Field-Effect-Mobility Pentacene Thin-Film Transistors with Polymethylmetacrylate Buffer Layer. *Appl. Phys. Lett.* **2005**, *86*, 203505. [CrossRef]
35. Kato, T.; Suzuki, T.; Amamiya, T.; Irie, T.; Komiyama, M.; Yui, H. Effects of Macromolecules on the Crystallization of $CaCO_3$ the Formation of Organic/Inorganic Composites. *Supramol. Sci.* **1998**, *5*, 411–415. [CrossRef]
36. Zukas, B.G.; Gupta, N.R. Interphase Synthesis of Zinc Oxide Nanoparticles in a Droplet Flow Reactor. *Ind. Eng. Chem. Res.* **2017**, *56*, 7184–7191. [CrossRef]
37. Ali, G.; Park, Y.J.; Kim, J.W.; Cho, S.O. A Green, General, and Ultrafast Route for the Synthesis of Diverse Metal Oxide Nanoparticles with Controllable Sizes and Enhanced Catalytic Activity. *ACS Appl. Nano Mater.* **2018**, *1*, 6112–6122. [CrossRef]
38. Cao, H.; Zhou, X.; Zheng, C.; Liu, Z. Two-Dimensional Porous Micro/Nano Metal Oxides Templated by Graphene Oxide. *ACS Appl. Mater. Interfaces* **2015**, *7*, 11984–11990. [CrossRef]
39. Niederberger, M. Nonaqueous Sol–Gel Routes to Metal Oxide Nanoparticles. *Acc. Chem. Res.* **2007**, *40*, 793–800. [CrossRef]
40. Yu, J.; Yu, X. Hydrothermal Synthesis and Photocatalytic Activity of Zinc Oxide Hollow Spheres. *Environ. Sci. Technol.* **2008**, *42*, 4902–4907. [CrossRef]
41. Ba, J.; Polleux, J.; Antonietti, M.; Niederberger, M. Non-Aqueous Synthesis of Tin Oxide Nanocrystals and Their Assembly into Ordered Porous Mesostructures. *Adv. Mater.* **2005**, *17*, 2509–2512. [CrossRef]
42. Bilecka, I.; Djerdj, I.; Niederberger, M. One-Minute Synthesis of Crystalline Binary and Ternary Metal Oxide Nanoparticles. *Chem. Commun.* **2008**, 886–888. [CrossRef] [PubMed]
43. Ding, Z.; Hu, X.; Yue, P.L.; Lu, G.Q.; Greenfield, P.F. Synthesis of Anatase TiO_2 Supported on Porous Solids by Chemical Vapor Deposition. *Catal. Today* **2001**, *68*, 173–182. [CrossRef]
44. Wang, Y.; Lei, Y.; Li, J.; Gu, L.; Yuan, H.; Xiao, D. Synthesis of 3D-Nanonet Hollow Structured Co_3O_4 for High Capacity Supercapacitor. *ACS Appl. Mater. Interfaces* **2014**, *6*, 6739–6747. [CrossRef] [PubMed]
45. Gawande, M.B.; Branco, P.S.; Parghi, K.; Shrikhande, J.J.; Pandey, R.K.; Ghumman, C.A.A.; Bundaleski, N.; Teodoro, O.M.N.D.; Jayaram, R.V. Synthesis and Characterization of Versatile MgO–ZrO_2 Mixed Metal Oxide Nanoparticles and Their Applications. *Catal. Sci. Technol.* **2011**, *1*, 1653–1664. [CrossRef]
46. Sharma, R.K.; Ghose, R. Synthesis of Nanocrystalline CuO–ZnO Mixed Metal Oxide Powder by a Homogeneous Precipitation Method. *Ceram. Int.* **2014**, *40*, 10919–10926. [CrossRef]
47. Li, J.; Liu, X.; Cui, J.; Sun, J. Hydrothermal Synthesis of Self-Assembled Hierarchical Tungsten Oxides Hollow Spheres and Their Gas Sensing Properties. *ACS Appl. Mater. Interfaces* **2015**, *7*, 10108–10114. [CrossRef]
48. Van Tong, P.; Hoa, N.D.; Van Duy, N.; Le, D.T.T.; Van Hieu, N. Enhancement of Gas-Sensing Characteristics of Hydrothermally Synthesized WO_3 Nanorods by Surface Decoration with Pd Nanoparticles. *Sens. Actuators B Chem.* **2016**, *223*, 453–460. [CrossRef]
49. Yeo, J.; Hong, S.; Kim, G.; Lee, H.; Suh, Y.D.; Park, I.; Grigoropoulos, C.P.; Ko, S.H. Laser-Induced Hydrothermal Growth of Heterogeneous Metal-Oxide Nanowire on Flexible Substrate by Laser Absorption Layer Design. *ACS Nano* **2015**, *9*, 6059–6068. [CrossRef]
50. Wang, J.; Yang, P.; Wei, X. High-Performance, Room-Temperature, and No-Humidity-Impact Ammonia Sensor Based on Heterogeneous Nickel Oxide and Zinc Oxide Nanocrystals. *ACS Appl. Mater. Interfaces* **2015**, *7*, 3816–3824. [CrossRef]
51. Lu, B.; Bai, J.; Bo, X.; Zhu, L.; Guo, L. A Simple Hydrothermal Synthesis of Nickel Hydroxide–Ordered Mesoporous Carbons Nanocomposites and Its Electrocatalytic Application. *Electrochim. Acta* **2010**, *55*, 8724–8730. [CrossRef]
52. Liu, Q.; Qin, M.C.; Ke, W.J.; Zheng, X.L.; Chen, Z.; Qin, P.L.; Xiong, L.B.; Lei, H.W.; Wan, J.W.; Wen, J. Enhanced Stability of Perovskite Solar Cells with Low-Temperature Hydrothermally Grown SnO_2 Electron Transport Layers. *Adv. Funct. Mater.* **2016**, *26*, 6069–6075. [CrossRef]
53. Ji, H.; Miao, X.; Wang, L.; Qian, B.; Yang, G. Microwave-Assisted Hydrothermal Synthesis of Sphere-like C/CuO and CuO Nanocrystals and Improved Performance as Anode Materials for Lithium-Ion Batteries. *Powder Technol.* **2013**, *241*, 43–48. [CrossRef]
54. Yayapao, O.; Thongtem, T.; Phuruangrat, A.; Thongtem, S. CTAB-Assisted Hydrothermal Synthesis of Tungsten Oxide Microflowers. *J. Alloys Compd.* **2011**, *509*, 2294–2299. [CrossRef]

55. Zhao, R.; Wang, L.; Chai, Z.-F.; Shi, W.-Q. Synthesis of ThO_2 Nanostructures through a Hydrothermal Approach: Influence of Hexamethylenetetramine (HMTA) and Sodium Dodecyl Sulfate (SDS). *RSC Adv.* **2014**, *4*, 52209–52214. [CrossRef]
56. Xiao, W.; Wang, Z.; Guo, H.; Zhang, Y.; Zhang, Q.; Gan, L. A Facile PVP-Assisted Hydrothermal Fabrication of Fe_2O_3/Graphene Composite as High Performance Anode Material for Lithium Ion Batteries. *J. Alloys Compd.* **2013**, *560*, 208–214. [CrossRef]
57. Vishwas, M.; Narasimha Rao, K.; Arjuna Gowda, K.V.; Chakradhar, R.P.S. Influence of Sn Doping on Structural, Optical and Electrical Properties of ZnO Thin Films Prepared by Cost Effective Sol–Gel Process. *Spectrochim. Acta A* **2012**, *95*, 423–426. [CrossRef]
58. Li, X.; Liu, P.; Mao, Y.; Xing, M.; Zhang, J. Preparation of Homogeneous Nitrogen-Doped Mesoporous TiO_2 Spheres with Enhanced Visible-Light Photocatalysis. *Appl. Catal. B Environ.* **2015**, *164*, 352–359. [CrossRef]
59. Soo, M.T.; Prastomo, N.; Matsuda, A.; Kawamura, G.; Muto, H.; Noor, A.F.M.; Lockman, Z.; Cheong, K.Y. Elaboration and Characterization of Sol–Gel Derived ZrO_2 Thin Films Treated with Hot Water. *Appl. Surf. Sci.* **2012**, *258*, 5250–5258. [CrossRef]
60. Niederberger, M.; Garnweitner, G.; Buha, J.; Polleux, J.; Ba, J.; Pinna, N. Nonaqueous Synthesis of Metal Oxide Nanoparticles:Review and Indium Oxide as Case Study for the Dependence of Particle Morphology on Precursors and Solvents. *J. Sol-Gel Sci. Technol.* **2006**, *40*, 259–266. [CrossRef]
61. Athar, T.; Hakeem, A.; Ahmed, W. Synthesis of MgO Nanopowder via Non Aqueous Sol–gel Method. *Adv. Sci. Lett.* **2012**, *7*, 27–29. [CrossRef]
62. Masthoff, I.C.; Kraken, M.; Menzel, D.; Litterst, F.J.; Garnweitner, G. Study of the Growth of Hydrophilic Iron Oxide Nanoparticles Obtained via the Non-Aqueous Sol–Gel Method. *J. Sol-Gel Sci. Technol.* **2016**, *77*, 553–564. [CrossRef]
63. Singh, I.; Kumar, R.; Birajdar, B.I. Zirconium Doped TiO_2 Nano-Powder via Halide Free Non-Aqueous Solvent Controlled Sol–gel Route. *J. Environ. Chem. Eng.* **2017**, *5*, 2955–2963. [CrossRef]
64. Niederberger, M.; Bartl, M.H.; Stucky, G.D. Benzyl Alcohol and Transition Metal Chlorides as a Versatile Reaction System for the Nonaqueous and Low-Temperature Synthesis of Crystalline Nano-Objects with Controlled Dimensionality. *J. Am. Chem. Soc.* **2002**, *124*, 13642–13643. [CrossRef] [PubMed]
65. Mirzaei, A.; Neri, G. Microwave-Assisted Synthesis of Metal Oxide Nanostructures for Gas Sensing Application: A Review. *Sens. Actuators B Chem.* **2016**, *237*, 749–775. [CrossRef]
66. Xi, G.; He, Y.; Zhang, Q.; Xiao, H.; Wang, X.; Wang, C. Synthesis of Crystalline Microporous SnO_2 via a Surfactant-Assisted Microwave Heating Method: A General and Rapid Method for the Synthesis of Metal Oxide Nanostructures. *J. Phys. Chem. C* **2008**, *112*, 11645–11649. [CrossRef]
67. Vijayakumar, S.; Nagamuthu, S.; Muralidharan, G. Supercapacitor Studies on NiO Nanoflakes Synthesized Through a Microwave Route. *ACS Appl. Mater. Interfaces* **2013**, *5*, 2188–2196. [CrossRef]
68. Mondal, A.K.; Su, D.; Chen, S.; Kretschmer, K.; Xie, X.; Ahn, H.-J.; Wang, G. A Microwave Synthesis of Mesoporous $NiCo_2O_4$ Nanosheets as Electrode Materials for Lithium-Ion Batteries and Supercapacitors. *ChemPhysChem* **2015**, *16*, 169–175. [CrossRef]
69. Ede, S.R.; Anantharaj, S.; Subramanian, B.; Rathishkumar, A.; Kundu, S. Microwave-Assisted Template-Free Synthesis of $Ni_3(BO_3)_2$(NOB) Hierarchical Nanoflowers for Electrocatalytic Oxygen Evolution. *Energy Fuels* **2018**, *32*, 6224–6233. [CrossRef]
70. Bilecka, I.; Niederberger, M. Microwave Chemistry for Inorganic Nanomaterials Synthesis. *Nanoscale* **2010**, *2*, 1358–1374. [CrossRef]
71. Nomura, K.; Ohta, H.; Takagi, A.; Kamiya, T.; Hirano, M.; Hosono, H. Room-Temperature Fabrication of Transparent Flexible Thin-Film Transistors Using Amorphous Oxide Semiconductors. *Nature* **2004**, *432*, 488–492. [CrossRef] [PubMed]
72. Buchholz, D.B.; Ma, Q.; Alducin, D.; Ponce, A.; Jose-Yacaman, M.; Khanal, R.; Medvedeva, J.E.; Chang, R.P.H. The Structure and Properties of Amorphous Indium Oxide. *Chem. Mater.* **2014**, *26*, 5401–5411. [CrossRef] [PubMed]
73. Thomas, S.R.; Pattanasattayavong, P.; Anthopoulos, T.D. Solution-Processable Metal Oxide Semiconductors for Thin-Film Transistor Applications. *Chem. Soc. Rev.* **2013**, *42*, 6910–6923. [CrossRef] [PubMed]
74. Xu, H.; Luo, D.; Li, M.; Xu, M.; Zou, J.; Tao, H.; Lan, L.; Wang, L.; Peng, J.; Cao, Y. A Flexible AMOLED Display on the PEN Substrate Driven by Oxide Thin-Film Transistors Using Anodized Aluminium Oxide as Dielectric. *J. Mater. Chem. C* **2014**, *2*, 1255–1259. [CrossRef]

75. Cairns, D.R.; Witte, R.P.; Sparacin, D.K.; Sachsman, S.M.; Paine, D.C.; Crawford, G.P.; Newton, R.R. Strain-Dependent Electrical Resistance of Tin-Doped Indium Oxide on Polymer Substrates. *Appl. Phys. Lett.* **2000**, *76*, 1425–1427. [CrossRef]
76. Peng, C.; Jia, Z.; Bianculli, D.; Li, T.; Lou, J. In Situ Electro-Mechanical Experiments and Mechanics Modeling of Tensile Cracking in Indium Tin Oxide Thin Films on Polyimide Substrates. *J. Appl. Phys.* **2011**, *109*, 103530. [CrossRef]
77. Xing, G.Z.; Yi, J.B.; Yan, F.; Wu, T.; Li, S. Positive Magnetoresistance in Ferromagnetic Nd-Doped In_2O_3 Thin Films Grown by Pulse Laser Deposition. *Appl. Phys. Lett.* **2014**, *104*, 202411. [CrossRef]
78. Imai, H.; Tominaga, A.; Hirashima, H.; Toki, M.; Asakuma, N. Ultraviolet-Reduced Reduction and Crystallization of Indium Oxide Films. *J. Appl. Phys.* **1999**, *85*, 203–207. [CrossRef]
79. Kim, J.Y.; Lee, K.; Coates, N.E.; Moses, D.; Nguyen, T.-Q.; Dante, M.; Heeger, A.J. Efficient Tandem Polymer Solar Cells Fabricated by All-Solution Processing. *Science* **2007**, *317*, 222–225. [CrossRef]
80. Ma, W.; Yang, C.; Gong, X.; Lee, K.; Heeger, A.J. Thermally Stable, Efficient Polymer Solar Cells with Nanoscale Control of the Interpenetrating Network Morphology. *Adv. Funct. Mater.* **2005**, *15*, 1617–1622. [CrossRef]
81. Le, T.-H.; Kim, Y.; Yoon, H. Electrical and Electrochemical Properties of Conducting Polymers. *Polymers* **2017**, *9*, 150. [CrossRef] [PubMed]
82. Kong, H.J.; Kim, S.; Le, T.-H.; Kim, Y.; Park, G.; Park, C.S.; Kwon, O.S.; Yoon, H. Nanostructured Mesophase Electrode Materials: Modulating Charge-Storage Behavior by Thermal Treatment. *Nanoscale* **2017**, *9*, 17450–17458. [CrossRef] [PubMed]
83. Beek, W.J.; Slooff, L.H.; Wienk, M.M.; Kroon, J.M.; Janssen, R.A. Hybrid Solar Cells Using a Zinc Oxide Precursor and a Conjugated Polymer. *Adv. Funct. Mater.* **2005**, *15*, 1703–1707. [CrossRef]
84. Chen, C.-T.; Hsu, F.-C.; Kuan, S.-W.; Chen, Y.-F. The Effect of C60 on the ZnO-Nanorod Surface in Organic–Inorganic Hybrid Photovoltaics. *Sol. Energy Mater. Sol. Cells* **2011**, *95*, 740–744. [CrossRef]
85. Benabid, F.; Kharchi, N.; Zouai, F.; Mourad, A.-H.I.; Benachour, D. Impact of Co-Mixing Technique and Surface Modification of ZnO Nanoparticles Using Stearic Acid on Their Dispersion into HDPE to Produce HDPE/ZnO Nanocomposites. *Polym. Polym. Compos.* **2019**, *27*, 389–399. [CrossRef]
86. Vivekchand, S.; Kam, K.C.; Gundiah, G.; Govindaraj, A.; Cheetham, A.; Rao, C. Electrical Properties of Inorganic Nanowire–Polymer Composites. *J. Mater. Chem.* **2005**, *15*, 4922–4927. [CrossRef]
87. Shim, M.; Javey, A.; Shi Kam, N.W.; Dai, H. Polymer Functionalization for Air-Stable n-Type Carbon Nanotube Field-Effect Transistors. *J. Am. Chem. Soc.* **2001**, *123*, 11512–11513. [CrossRef]
88. Du, Y.; Liu, H.; Neal, A.T.; Si, M.; Ye, P.D. Molecular Doping of Multilayer MoS_2 Field-Effect Transistors: Reduction in Sheet and Contact Resistances. *IEEE Electron Device Lett.* **2013**, *34*, 1328–1330. [CrossRef]
89. Sun, B.; Hong, W.; Thibau, E.S.; Aziz, H.; Lu, Z.-H.; Li, Y. Polyethylenimine (PEI) As an Effective Dopant To Conveniently Convert Ambipolar and p-Type Polymers into Unipolar n-Type Polymers. *ACS Appl. Mater. Interfaces* **2015**, *7*, 18662–18671. [CrossRef]
90. Fabiano, S.; Braun, S.; Liu, X.; Weverberghs, E.; Gerbaux, P.; Fahlman, M.; Berggren, M.; Crispin, X. Poly(ethylene imine) Impurities Induce n-doping Reaction in Organic (Semi)Conductors. *Adv. Mater.* **2014**, *26*, 6000–6006. [CrossRef]
91. Yu, X.; Zeng, L.; Zhou, N.; Guo, P.; Shi, F.; Buchholz, D.B.; Ma, Q.; Yu, J.; Dravid, V.P.; Chang, R.P.H.; et al. Ultra-Flexible, "Invisible" Thin-Film Transistors Enabled by Amorphous Metal Oxide/Polymer Channel Layer Blends. *Adv. Mater.* **2015**, *27*, 2390–2399. [CrossRef]
92. Jeong, E.G.; Kwon, J.H.; Kang, K.S.; Jeong, S.Y.; Choi, K.C. A Review of Highly Reliable Flexible Encapsulation Technologies towards Rollable and Foldable OLEDs. *J. Inf. Disp.* **2019**, 19–32. [CrossRef]
93. Huang, W.; Zeng, L.; Yu, X.; Guo, P.; Wang, B.; Ma, Q.; Chang, R.P.H.; Yu, J.; Bedzyk, M.J.; Marks, T.J.; et al. Metal Oxide Transistors via Polyethylenimine Doping of the Channel Layer: Interplay of Doping, Microstructure, and Charge Transport. *Adv. Funct. Mater.* **2016**, *26*, 6179–6187. [CrossRef]
94. Huang, W.; Guo, P.; Zeng, L.; Li, R.; Wang, B.; Wang, G.; Zhang, X.; Chang, R.P.H.; Yu, J.; Bedzyk, M.J.; et al. Metal Composition and Polyethylenimine Doping Capacity Effects on Semiconducting Metal Oxide—Polymer Blend Charge Transport. *J. Am. Chem. Soc.* **2018**, *140*, 5457–5473. [CrossRef] [PubMed]
95. Na, J.W.; Kim, H.J.; Hong, S.; Kim, H.J. Plasma Polymerization Enabled Polymer/Metal–Oxide Hybrid Semiconductors for Wearable Electronics. *ACS Appl. Mater. Interfaces* **2018**, *10*, 37207–37215. [CrossRef] [PubMed]

96. Sun, D.; Chen, C.; Zhang, J.; Wu, X.; Chen, H.; Guo, T. High Performance Inkjet-Printed Metal Oxide Thin Film Transistors via Addition of Insulating Polymer with Proper Molecular Weight. *Appl. Phys. Lett.* **2018**, *112*, 012102. [CrossRef]
97. Ha, Y.-G.; Everaerts, K.; Hersam, M.C.; Marks, T.J. Hybrid Gate Dielectric Materials for Unconventional Electronic Circuitry. *Acc. Chem. Res.* **2014**, *47*, 1019–1028. [CrossRef]
98. Wang, G.; Persson, N.; Chu, P.-H.; Kleinhenz, N.; Fu, B.; Chang, M.; Deb, N.; Mao, Y.; Wang, H.; Grover, M.A.; et al. Microfluidic Crystal Engineering of π-Conjugated Polymers. *ACS Nano* **2015**, *9*, 8220–8230. [CrossRef]
99. Yeon Kwon, J.; Kyeong Jeong, J. Recent Progress in High Performance and Reliable N-type Transition Metal Oxide-Based Thin Film Transistors. *Semicond. Sci. Technol.* **2015**, *30*, 024002. [CrossRef]
100. Wager, J.F.; Yeh, B.; Hoffman, R.L.; Keszler, D.A. An Amorphous Oxide Semiconductor Thin-Film Transistor Route to Oxide Electronics. *Curr. Opin. Solid State Mater. Sci.* **2014**, *18*, 53–61. [CrossRef]
101. Navan, R.R.; Prashanthi, K.; Shojaei Baghini, M.; Ramgopal Rao, V. Solution Processed Photopatternable High-k Nanocomposite Gate Dielectric for Low Voltage Organic Field Effect Transistors. *Microelectron. Eng.* **2012**, *96*, 92–95. [CrossRef]
102. Lim, S.; Lee, K.H.; Kim, H.; Kim, S.H. Optimization of Nanocomposite Gate Insulators for Organic Thin Film Transistors. *Org. Electron.* **2015**, *17*, 144–150. [CrossRef]
103. Hou, X.; Ng, S.C.; Zhang, J.; Chang, J.S. Polymer Nanocomposite Dielectric Based on P(VDF-TrFE)/PMMA/$BaTiO_3$ for TIPs-Pentacene OFETs. *Org. Electron.* **2015**, *17*, 247–252. [CrossRef]
104. Rasul, A.; Zhang, J.; Gamota, D.; Takoudis, C. High K Nanocomposite Dielectric for Printed Organic Electronics Applications. *Microelectron. Eng.* **2012**, *93*, 95–99. [CrossRef]
105. Pecunia, V.; Banger, K.; Sirringhaus, H. High-Performance Solution-Processed Amorphous-Oxide-Semiconductor TFTs with Organic Polymeric Gate Dielectrics. *Adv. Electron. Mater.* **2015**, *1*, 1400024. [CrossRef]
106. Sirringhaus, H. 25th Anniversary Article: Organic Field-Effect Transistors: The Path Beyond Amorphous Silicon. *Adv. Mater.* **2014**, *26*, 1319–1335. [CrossRef]
107. Zhang, L.; Wang, H.; Zhao, Y.; Guo, Y.; Hu, W.; Yu, G.; Liu, Y. Substrate-Free Ultra-Flexible Organic Field-Effect Transistors and Five-Stage Ring Oscillators. *Adv. Mater.* **2013**, *25*, 5455–5460. [CrossRef]
108. Khim, D.; Xu, Y.; Baeg, K.-J.; Kang, M.; Park, W.-T.; Lee, S.-H.; Kim, I.-B.; Kim, J.; Kim, D.-Y.; Liu, C.; et al. Large Enhancement of Carrier Transport in Solution-Processed Field-Effect Transistors by Fluorinated Dielectric Engineering. *Adv. Mater.* **2016**, *28*, 518–526. [CrossRef]
109. Li, J.; Liu, D.; Miao, Q.; Yan, F. The Application of a high-k Polymer in Flexible Low-Voltage Organic Thin-Film Transistors. *J. Mater. Chem.* **2012**, *22*, 15998–16004. [CrossRef]
110. Fukuda, K.; Sekine, T.; Shiwaku, R.; Morimoto, T.; Kumaki, D.; Tokito, S. Free-Standing Organic Transistors and Circuits with Sub-Micron Thicknesses. *Sci. Rep.* **2016**, *6*, 27450. [CrossRef]
111. Yu, X.; Smith, J.; Zhou, N.; Zeng, L.; Guo, P.; Xia, Y.; Alvarez, A.; Aghion, S.; Lin, H.; Yu, J.; et al. Spray-Combustion Synthesis: Efficient Solution Route to High-Performance Oxide Transistors. *Proc. Natl. Acad. Sci. USA* **2015**, *112*, 3217–3222. [CrossRef] [PubMed]
112. Chen, H.; Cao, Y.; Zhang, J.; Zhou, C. Large-Scale Complementary Macroelectronics Using Hybrid Integration of Carbon Nanotubes and IGZO Thin-Film Transistors. *Nat. Commun.* **2014**, *5*, 4097. [CrossRef] [PubMed]
113. Rasul, A.; Zhang, J.; Gamota, D.; Singh, M.; Takoudis, C. Flexible High Capacitance Nanocomposite Gate Insulator for Printed Oorganic Field-Effect Transistors. *Thin Solid Films* **2010**, *518*, 7024–7028. [CrossRef]
114. Yang, F.-Y.; Hsu, M.-Y.; Hwang, G.-W.; Chang, K.-J. High-Performance Poly(3-hexylthiophene) Top-Gate Transistors Incorporating TiO_2 Nanocomposite Dielectrics. *Org. Electron.* **2010**, *11*, 81–88. [CrossRef]
115. Park, J.; Lee, J.W.; Kim, D.W.; Park, B.J.; Choi, H.J.; Choi, J.S. Pentacene Thin-Film Transistor with Poly(methyl methacrylate-co-methacrylic acid)/TiO_2 Nanocomposite Gate Insulator. *Thin Solid Films* **2009**, *518*, 588–590. [CrossRef]
116. Lee, W.-H.; Wang, C.C. Effect of Nanocomposite Gate Dielectric Rroughness on Pentacene Field-Effect Transistor. *J. Vac. Sci. Technol. B* **2009**, *27*, 1116–1121. [CrossRef]
117. Lee, W.-H.; Wang, C.C.; Ho, J.C. Improved Performance of Pentacene Field-Effect Transistors Using a Nanocomposite Gate Dielectric. *J. Vac. Sci. Technol. B* **2009**, *27*, 601–605. [CrossRef]
118. Noh, H.Y.; Seol, Y.G.; Kim, S.I.; Lee, N.E. Mechanically Flexible Low-Leakage Nanocomposite Gate Dielectrics for Flexible Organic Thin-Film Transistors. *Electrochem. Solid State Lett.* **2008**, *11*, H218–H221. [CrossRef]

119. Kim, P.; Zhang, X.-H.; Domercq, B.; Jones, S.C.; Hotchkiss, P.J.; Marder, S.R.; Kippelen, B.; Perry, J.W. Solution-Processible High-Permittivity Nanocomposite Gate Insulators for Organic Field-Effect Transistors. *Appl. Phys. Lett.* **2008**, *93*, 013302. [CrossRef]
120. Mohammadian, N.; Faraji, S.; Sagar, S.; Das, B.C.; Turner, M.L.; Majewski, L.A. One-Volt, Solution-Processed Organic Transistors with Self-Assembled Monolayer-Ta_2O_5 Gate Dielectrics. *Materials* **2019**, *12*, 2563. [CrossRef]
121. Jung, Y.; Jun, T.; Kim, A.; Song, K.; Yeo, T.H.; Moon, J. Direct Photopatternable Organic–Inorganic Hybrid Gate Dielectric for Solution-Processed Flexible ZnO Thin Film Transistors. *J. Mater. Chem.* **2011**, *21*, 11879–11885. [CrossRef]
122. Ha, Y.-G.; Jeong, S.; Wu, J.; Kim, M.-G.; Dravid, V.P.; Facchetti, A.; Marks, T.J. Flexible Low-Voltage Organic Thin-Film Transistors Enabled by Low-Temperature, Ambient Solution-Processable Inorganic/Organic Hybrid Gate Dielectrics. *J. Am. Chem. Soc.* **2010**, *132*, 17426–17434. [CrossRef]
123. Morales-Acosta, M.D.; Quevedo-Lopez, M.A.; Gnade, B.E.; Ramírez-Bon, R.M. PMMA-SiO_2 Organic–Inorganic Hybrid Films: Determination of Dielectric Characteristics. *J. Sol-Gel Sci. Technol.* **2011**, *58*, 218–224. [CrossRef]
124. Morales-Acosta, M.D.; Quevedo-López, M.A.; Ramírez-Bon, R. PMMA–SiO_2 Hybrid Films as Gate Dielectric for ZnO Based Thin-Film Transistors. *Mater. Chem. Phys.* **2014**, *146*, 380–388. [CrossRef]
125. Morales-Acosta, M.D.; Alvarado-Beltrán, C.G.; Quevedo-López, M.A.; Gnade, B.E.; Mendoza-Galván, A.; Ramírez-Bon, R. Adjustable Structural, Optical and Dielectric Characteristics in Sol–Gel PMMA–SiO_2 Hybrid Films. *J. Non-Cryst. Solids* **2013**, *362*, 124–135. [CrossRef]
126. Alvarado-Beltrán, C.G.; Almaral-Sánchez, J.L.; Ramírez-Bon, R. Synthesis and Properties of PMMA-ZrO_2 Organic–Inorganic Hybrid Films. *J. Appl. Polym. Sci.* **2015**, *132*. [CrossRef]
127. Lee, W.-J.; Park, W.-T.; Park, S.; Sung, S.; Noh, Y.-Y.; Yoon, M.-H. Large-Scale Precise Printing of Ultrathin Sol–Gel Oxide Dielectrics for Directly Patterned Solution-Processed Metal Oxide Transistor Arrays. *Adv. Mater.* **2015**, *27*, 5043–5048. [CrossRef]
128. Lin, Y.-H.; Thomas, S.R.; Faber, H.; Li, R.; McLachlan, M.A.; Patsalas, P.A.; Anthopoulos, T.D. Al-Doped ZnO Transistors Processed from Solution at 120 °C. *Adv. Electron. Mater.* **2016**, *2*, 1600070. [CrossRef]
129. Alvarado-Beltrán, C.G.; Almaral-Sánchez, J.L.; Mejia, I.; Quevedo-López, M.A.; Ramirez-Bon, R. Sol–Gel PMMA–ZrO_2 Hybrid Layers as Gate Dielectric for Low-Temperature ZnO-Based Thin-Film Transistors. *ACS Omega* **2017**, *2*, 6968–6974. [CrossRef] [PubMed]
130. Shen, Q.; Ogomi, Y.; Chang, J.; Tsukamoto, S.; Kukihara, K.; Oshima, T.; Osada, N.; Yoshino, K.; Katayama, K.; Toyoda, T.; et al. Charge Transfer and Recombination at the Metal Oxide/$CH_3NH_3PbClI_2$/Spiro-OMeTAD Interfaces: Uncovering the Detailed Mechanism Behind High Efficiency Solar Cells. *Phys. Chem. Chem. Phys.* **2014**, *16*, 19984–19992. [CrossRef] [PubMed]
131. Kwon, J.-H.; Zhang, X.; Piao, S.H.; Choi, H.J.; Bae, J.-H.; Park, J. Stability Study of Flexible 6,13-Bis(triisopropylsilylethynyl)pentacene Thin-Film Transistors with a Cross-Linked Poly(4-vinylphenol)/Yttrium Oxide Nanocomposite Gate Insulator. *Polymers* **2016**, *8*, 88. [CrossRef] [PubMed]
132. Kim, J.; Lim, S.H.; Kim, Y.S. Solution-Based TiO_2−Polymer Composite Dielectric for Low Operating Voltage OTFTs. *J. Am. Chem. Soc.* **2010**, *132*, 14721–14723. [CrossRef] [PubMed]
133. Bang, S.; Lee, S.; Jeon, S.; Kwon, S.; Jeong, W.; Kim, H.; Shin, I.; Chang, H.J.; Park, H.-h.; Jeon, H. Al_2O_3 Buffer in a ZnO Thin Film Transistor with Poly-4-vinylphenol Dielectric. *Semicond. Sci. Technol.* **2008**, *24*, 025008. [CrossRef]
134. Kim, M.J.; Pak, K.; Hwang, W.S.; Im, S.G.; Cho, B.J. Novel Vapor-Phase Synthesis of Flexible, Homogeneous Organic–Inorganic Hybrid Gate Dielectric with sub 5 nm Equivalent Oxide Thickness. *ACS Appl. Mater. Interfaces* **2018**, *10*, 37326–37334. [CrossRef]
135. Son, B.-G.; Je, S.Y.; Kim, H.J.; Jeong, J.K. Modification of a Polymer Gate Insulator by Zirconium Oxide Doping for Low Temperature, High Performance Indium Zinc Oxide Transistors. *RSC Adv.* **2014**, *4*, 45742–45748. [CrossRef]
136. Held, M.; Schießl, S.P.; Miehler, D.; Gannott, F.; Zaumseil, J. Polymer/Metal Oxide Hybrid Dielectrics for Low Voltage Field-Effect Transistors with Solution-Processed, High-Mobility Semiconductors. *Appl. Phys. Lett.* **2015**, *107*, 083301. [CrossRef]

137. Ye, X.; Lin, H.; Yu, X.; Han, S.; Shang, M.; Zhang, L.; Jiang, Q.; Zhong, J. High Performance Low-Voltage Organic Field-Effect Transistors Enabled by Solution Processed Alumina and Polymer Bilayer Dielectrics. *Synth. Met.* **2015**, *209*, 337–342. [CrossRef]
138. He, W.; Xu, W.; Peng, Q.; Liu, C.; Zhou, G.; Wu, S.; Zeng, M.; Zhang, Z.; Gao, J.; Gao, X.; et al. Surface Modification on Solution Processable ZrO_2 High-k Dielectrics for Low Voltage Operations of Organic Thin Film Transistors. *J. Phys. Chem. C* **2016**, *120*, 9949–9957. [CrossRef]
139. Ha, T.-J. Low-Voltage and Hysteresis-Free Organic Thin-Film Transistors Employing Solution-Processed Hybrid Bilayer Gate Dielectrics. *Appl. Phys. Lett.* **2014**, *105*, 043305. [CrossRef]

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Review

Reliability of Miniaturized Transistors from the Perspective of Single-Defects

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Abstract: To analyze the reliability of semiconductor transistors, changes in the performance of the devices during operation are evaluated. A prominent effect altering the device behavior are the so called bias temperature instabilities (BTI), which emerge as a drift of the device threshold voltage over time. With ongoing miniaturization of the transistors towards a few tens of nanometer small devices the drift of the threshold voltage is observed to proceed in discrete steps. Quite interestingly, each of these steps correspond to charge capture or charge emission event of a certain defect in the atomic structure of the device. This observation paves the way for studying device reliability issues like BTI at the single-defect level. By considering single-defects the physical mechanism of charge trapping can be investigated very detailed. An in-depth understanding of the intricate charge trapping kinetics of the defects is essential for modeling of the device behavior and also for accurate estimation of the device lifetime amongst others. In this article the recent advancements in characterization, analysis and modeling of single-defects are reviewed.

Keywords: device reliability; nanoscale transistor; bias temperature instabilities (BTI); defects; single-defect spectroscopy; non-radiative multiphonon (NMP) model; time-dependent defect spectroscopy

1. Introduction

The complementary metal-oxide-semiconductor (CMOS) technology is the cornerstone of a vast number of integrated circuits, which are the building blocks of numerous electronic applications. Such circuits typically consist of a large number nMOS and pMOS transistors and their performance and geometry have been successively improved over the last decades. For instance, the width and length of the transistors have been reduced and the gate insulating layers have been thinned. Furthermore new device geometries such as FinFETs [1–3] and gate-all-around FETs [4–7] have been introduced. Notwithstanding this development, the reliable operation of the transistors at their nominal bias conditions is of utmost importance for all technologies. However, the most fundamental device parameters like the threshold voltage, the sub-threshold slope and the on-current, are affected by charge trapping at defects in the atomic structure of the devices. Such defects can be located at the interface between the insulator and substrate, but also inside the insulator and inside the semiconductor bulk material. In order to reduce the defect density of transistors post-oxidation annealing (POA) processes are applied during the fabrication process. The decisive importance of POA for improving the performance of transistors becomes even more obvious when Si and SiC based MOS devices are compared. While H_2 annealing is regularly used within CMOS processes [8–10] similar POA steps could not lead to an improvement of the electron mobility in SiC devices [11]. However, by using NO or NH_3 for POA, a considerable increase in carrier mobility can be observed for SiC MOS transistors [12,13].

Although a number of defects can become passivated using POA during fabrication, the interaction of high energetic carriers with atoms at the semiconductor/insulator interface

during operation can break Si-H bonds and can lead to an electrically active dangling bond [14]. The bond rupture mechanism leading to the creation of interface states is typically referred to hot-carrier-degradation (HCD). In order to explain HCD in miniaturized devices the physical origin for HCD has been recently extended to cold carriers, where a series of collisions with low energetic particles can also lead to the creation of interfaces states [15]. Such an increase of dangling bonds at the interface can be observed as decrease of the device mobility, due to an increase of the interface scattering of carriers. The reduced mobility evolves as a reduction in the sub-threshold slope and can be for instance observed when IDVG measurements are performed [16,17], but can also be evaluated as the CV characteristics of the device alters [18].

Another important reliability issue in miniaturized devices is the so called bias temperature instabilities (BTI) [19–24]. BTI typically manifest as a drift of the drain-source current over time when constant biases are applied to a transistor, and is studied up electric oxide fields of $E_{\mathrm{ox}} \leq 8\,\mathrm{MV/cm}$. The physical origin of this phenomenon is charge trapping at defects which can be located at the semiconductor/oxide interface or directly in the oxide. The impact of BTI on the device behavior is mostly expressed in terms of an equivalent shift of the threshold voltage ΔV_{th}, which can for instance be calculated from the current measurement data using an initial IDVG characteristics of a device, when traditional measurement tools are used [25]. Alternatively, employing the fast-Vth method, where the gate bias is controlled by an operational amplifier in order to obtain a constant current flux through the device, allows for direct measurement of the ΔV_{th} [26]. A typical temporal drift of the source current which can be measured when BTI is studied is shown in Figure 1 (left).

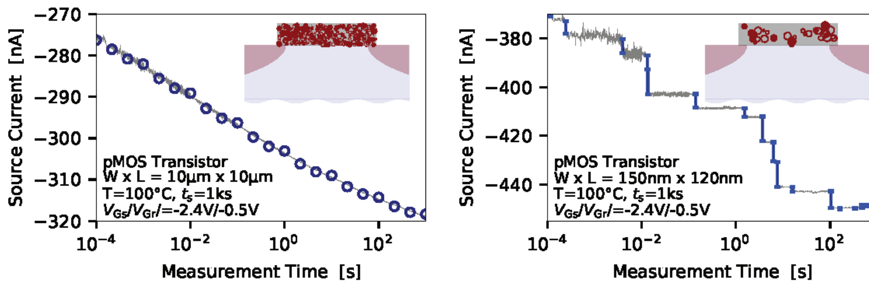

Figure 1. The main difference in the bias temperature instabilities (BTI) behavior of large-area and nanoscale devices is the number of defects contributing to the device behavior, and also the amplitude of impact of a single defect on the current flux through the device. (**left**) While in large-area devices a number of defects is responsible for a continuous drift of the drain-source current over time (**right**) the charge transitions of defects can be directly observed as discrete steps in the respective current signal recorded from nanoscale metal-oxide-semiconductor (MOS) transistors.

The inset indicates the number of defects affecting the device behavior. Quite interestingly, although the same physical mechanism are responsible for charge trapping in large-area and miniaturized devices, the picture of the drift of the device current is different for the scaled MOS transistors, see Figure 1 (right). While the source-current exhibits a continuous drift at large-area devices, charge trapping evolves in discrete steps of the device current, recorded at nanoscale MOS transistors. This is due to the fact that scaling of the devices on the one hand reduces the number of defects per device, but on the other hand the impact of a single defect on the overall device behavior gets considerably increased. Thus nanoscale devices inherently provide a zoom mechanism enabling to study charge trapping at the single-defect level.

The discrete steps in the current signal were first documented by Ralls et al. [27] and have since then been the basis for a number of investigations considering random telegraph noise (RTN) [28–33] aiming at the analysis of the physical origin of charge trapping. An significant advantage of evaluating RTN to conventional trapping analysis is that the charge capture and charge emission times can be

extracted directly from single measurement traces. However, as only defects with a trap level close to the Fermi level of the conducting channel produce RTN signals tracing the bias and temperature dependence of the charge trapping kinetics of certain defect is limited to a very narrow bias and temperature range. To overcome this limitation and to enable a thorough study of the trapping behavior of a multitude of defects the time-dependent defect spectroscopy (TDDS) has been proposed [34,35]. The measurement sequences used for TDDS relies on the measure-stress-measure (MSM) scheme, which will be discussed in the following. Afterwards the TDDS is presented and finally charge trapping models and recent results from single defect studies are reviewed.

2. Measurement Techniques for Characterization of Devices

Over the recent years a number of measurement methods have been developed in order to properly characterize the impact of defects on the device behavior. Most of the methods aim at applying a high stress bias for a specific period of time, and afterwards the state of the device is evaluated considering various ways. For instance stress-IV measurements, where IDVG sweeps are measured after a stress cycle has elapsed [17] have been used, but also hysteresis measurements [36,37], CV measurements [38,39], DLTS measurements [40–44] and on-the-fly methods [45–47] have been applied for assessment of the impact of charge trapping on the device performance. A common observation of the many measurement techniques used is that the ΔV_{th} is observed to recover very fast, as soon as the stress bias is released [26,48–50]. To circumvent this limitation ultra-fast measurement setups have been developed [51,52]. With these methods short measurement delays of a few tens of nanoseconds can be achieved, whereas conventional tools exhibit delays in the hundreds of microseconds regime. The ultra-fast methods clearly reveal a significantly larger ΔV_{th} [52] at nanoseconds delays. However, a considerable disadvantage of the high-speed methods is a typically high measurement noise of more than 10 mV in ΔV_{th}, as the signal-noise-ratio decreases at higher signal bandwidth. Thus the ultra-fast methods do not allow to resolve single charge transitions which are typically in the order of a few microvolt up to 10–15 mV [53,54]. However, a high measurement resolution is inevitable to study the physical mechanism of charge trapping, which has to be performed at the single defect level.

To perform single defect spectroscopy MSM sequences are typically used. Patterns for MSM characterization of charge trapping in large-area devices and miniaturized transistors are shown in Figure 2, and rely on repeatedly applying stress and recovery cycles.

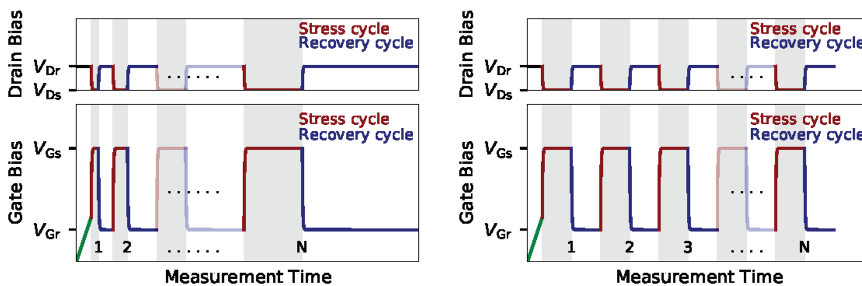

Figure 2. Schematic of the bias signals which are typically used for the measure-stress-measure (MSM) scheme which is applied for (**left**) the characterization of large-area devices, and (**right**) for defect-spectroscopy in nanoscale devices. An IDVG sweep is measured within a narrow gate bias range before the first stress cycle is applied. While the stress and recovery times are successively increased after each cycle for the characterization of large-area devices, N repetitions of the same sequence are performed when single-defects in nanoscale devices are studied.

Before the first stress cycle is applied, an IDVG sweep within a narrow gate bias range is typically performed. As mentioned before, the IDVG characteristics serves for the calculation of the ΔV_{th} from the recorded drain-source current in a post-processing step. The narrow bias range of the voltage

sweep is important in order to preserve the pristine state of the device, as a gate voltage sweep over a too wide bias range can already cause considerable degradation of the device characteristics. If large-area devices are characterized the stress and recovery time of the subsequent measurement cycles are continuously increased for each cycle. By doing so the number of traps which can contribute to the drift of the threshold voltage ΔV_{th} successively increase. It has to be noted that, in order to accurately explain the so measured temporal behavior of ΔV_{th} the entire measurement sequence has to be simulated [55], as the ΔV_{th} also shows a considerable permanent degradation, that is, the ΔV_{th} does not vanish at the end of each recovery trace, and otherwise the permanent part would not be described by the simulations. In contrast to MSM sequences with increasing stress/recovery times applied for the characterization of large-area devices, the a fixed timing is used for stress/recovery cycles when TDDS measurements employing scaled transistors are performed. The main idea is that the defects which emit their charge during the recovery cycle get charged in the next stress cycle again and so on. In this way statistical information on charge capture and emission of defects can be collected and evaluated, which will be discussed in Section 4 in more detail.

An important criterion when applying MSM measurements is the energetic and spatial distribution of the traps which can contribute to the measurement signal. One condition for charge trapping concerns the timing of the MSM sequence and the charge capture and charge emission time of the defects at the respective bias condition and device temperature. The second boundary condition for charge trapping is defined by the stress and recovery bias used for the experiment. These biases determine the so called active energy region (AER) for charge trapping which is shown in Figure 3 for the NBTI/pMOS case.

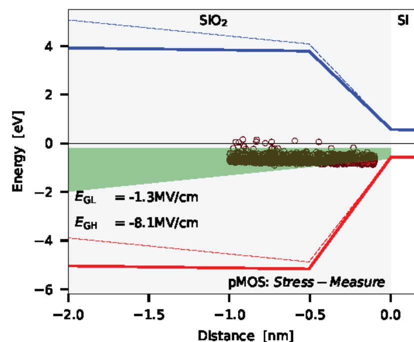

Figure 3. The band-diagram of a pMOS transistor is shown with a possible trap band of defects being responsible for the drift of the threshold voltage when negative BTI (NBTI) is considered. Also shown is the active energy region (AER, green area) for charge trapping which defines the energetic area of the defects which can contribute to the measurement signal at given bias conditions. The transition region shown in the band-diagram between the Si bulk material and the insulator which is in accordance with ab-initio calculations [56–58]. Quite recently, BTI in various technologies has been successfully explain using the modified band-structure [55].

In principle, the defects which exhibit a trap level below the Fermi level of the channel can become charged, and the defects with a trap level above the Fermi level remain neutral. Thus the key prerequisite of a defect to change its charge state during an MSM cycle is that its trap level is shifted below the Fermi level of the channel during the stress phase, but lies above the same during the recovery phase. The green area shown in Figure 3 is the energetic region where this condition is fulfilled, and thus marks the energetic area for defects which can affect the device behavior. Also shown is the hole trap band, which has been extracted for planar pMOS devices employing MSM measurements [55]. For this the reliability simulator Comphy has been used, which relies on the

non-radiative multiphonon (NMP) defect model [34]. Next, the main properties of BTI are briefly discussed and afterwards defect models used to explain charge trapping are outlined.

3. Patterns of Bias Temperature Instabilities

The impact of BTI on the device characteristics is typically expressed in terms of an equivalent shift of the device threshold voltage ΔV_{th}, which can be calculated from the drain-source current behavior using an IDVG characteristics [59]. In general, the impact of BTI on devices can be classified into positive BTI (PBTI), where a positive gate bias is applied at the gate terminal of the MOS transistor during stress, and negative BTI (NBTI), which is referred to when a negative stress bias is used [60]. In the literature mostly the NBTI/pMOS case is considered as in this case the ΔV_{th} appears more pronounced compared to the PBTI/nMOS case. The main reason lies in the about ten times higher trap density present in pMOS devices compared to their nMOS counterparts [61], which makes the assessment of the later with generalized measurement difficult. It has to be mentioned at this point, that recently a custom-designed defect probing instrument has been proposed and used to characterized NBTI and PBTI at ΔV_{th} resolution of a few tens of micro-volts [53]. Despite the challenges for instrumentation, the experiments are typically conducted at accelerated stress conditions, that is, significantly larger biases and temperatures, as used for nominal device operation. The idea is to accelerate device degradation and recovery and to calibrate the models to the corresponding measurement data. Afterwards, the calibrated tools are used to estimate the impact of BTI on the device performance at normal operating conditions. This procedure, however, requires accurate physical models in order to ensure high quality of the extrapolations. Thus suitable models have to be able to explain the different patterns of BTI at various stress and recovery bias conditions and also capture the temperature activation of charge trapping. The most basic properties of BTI are briefly summarized next.

3.1. Temperature Dependence of Charge Emission Times

Several recovery traces recorded at the same stress and biases conditions but at different temperatures are shown in Figure 4 (left) for a large-area transistor. The traces have been normalized to $\Delta V_{\mathrm{th}}(t_{\mathrm{r}} = 1\,\mathrm{ms})$. As can be seen, a similar trend for the recovery behavior of the ΔV_{th} can be observed at different temperatures. This indicates, that only a weak temperature dependence of charge trapping can be extracted from these measurements, which is an important parameter for developing of charge trapping models. But a significant change of the emission time can be observed when the average emission time of defects in nanoscale devices is evaluated, see Figure 4 (right). With increasing device temperature the defects move towards shorter emission times, clearly indicating a considerable temperature activation of the charge trapping kinetics. Although both cases rely on the same physical mechanisms, significant differences in thermal activation can be observed. This underlines once more the importance of investigating the behavior of individual defects in detail and taking this into account in the models.

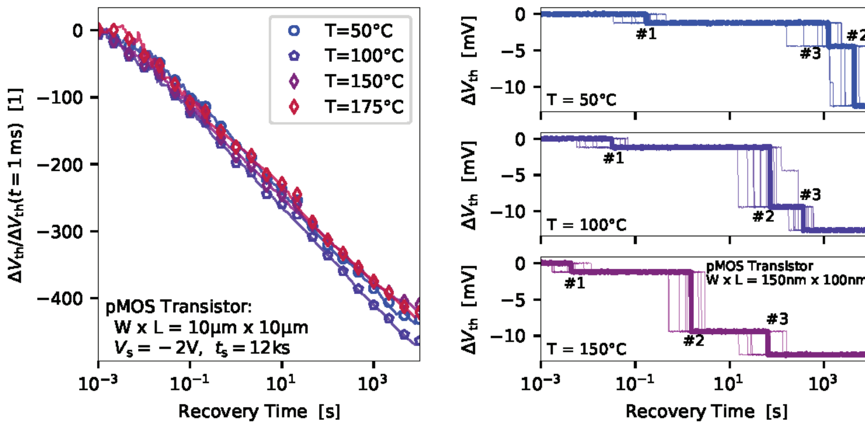

Figure 4. The temporal recovery behavior of a large-area and a nanoscale pMOS transistor is shown at different device temperatures. (**left**) Quite interestingly, the recovery traces of a large-area transistor can show only a very week temperature dependence when normalized to a certain reference value. (**right**) However, single-defect investigations clearly reveal a significant temperature dependence of charge trapping. Also shown here for the nanoscale device are the single recovery traces recorded at the same bias conditions, stress time and device temperature, which are used to determine the average emission time of the visible defects.

3.2. Bias Dependence of Charge Trapping

The bias dependence of charge trapping is shown in Figure 5 for different stress biases and the impact of the recovery bias on the measured ΔV_{th} is visible in Figure 6 for both a typical large-area and a representative miniaturized device. From Figure 5 (left) it becomes evident that at higher stress bias a larger shift of the threshold voltage ΔV_{th} can be recorded. This observation can be explained by an increase of the AER at higher stress bias, and thus more defects are shifted above the Fermi level of the channel during the stress phase, and as a consequence more defects can become charged. In additions to the more defects shifted below the Fermi level, the energy difference between the trap level and the Fermi level increase at higher stress bias. Thus, the larger this energy gap gets the shorter the charge capture times become. This trend can be clearly observed when the charge capture events of defects in nanoscale devices are evaluated, see Figure 5 (right). Another similarity between large-area and nanoscale devices is the increasing number of defects which become charged when the stress bias is increased. Quite interestingly, while for large-area devices charge capture and charge emission are observed to be bias dependent, compare Figure 5 (left) and Figure 6 (left), a notable number of defects in nanoscale device exhibit bias independent charge emission times. This behavior can be observed for defect #2 from Figure 6 (right), whereas the two other defects #1 and #3 emit their charge at shorter emission times at lower recovery bias. In general, the bias independent emission time behavior is associated with so called *fixed traps*, whereas defects exhibiting a bias dependent emission time are typically referred to as *switching traps*. Thus, providing an accurate model to explain the bias dependence of BTI is pretty challenging, as the field dependence of individual defects is observed to be on one hand negligible and on the other hand very strong. In order to explore a more detailed picture of the many peculiarities of the charge trapping kinetics of defects in miniaturized devices the recent findings employing the TDDS are discussed next.

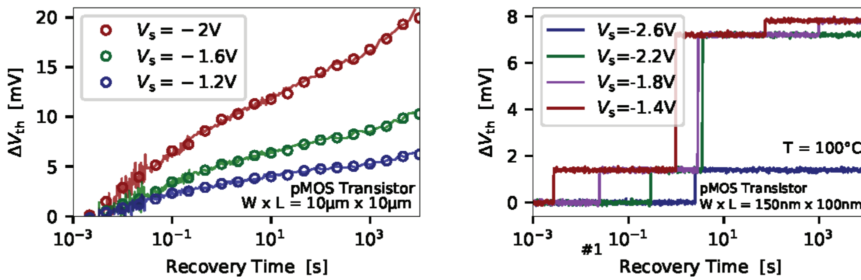

Figure 5. The temporal behavior of the drift of the threshold voltage is shown for pMOS transistors with two different geometries. (**left**) For large-area devices a continuous drift of the V_{th} can be observed. As more defects become charged at higher stress biases the recorded ΔV_{th} increases too. (**right**) In nanoscale devices the number of single charge transitions, that is, the number of discrete steps in the ΔV_{th}, increase with higher stress bias. Also the average charge capture time move toward smaller values at higher stress biases.

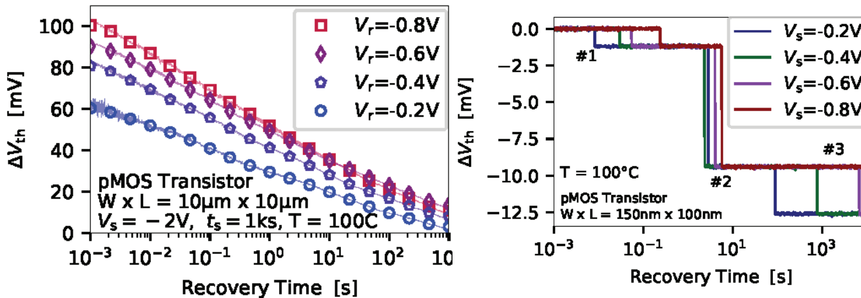

Figure 6. The recovery of the threshold voltage for pMOS transistors is shown from the perspective of a (**left**) large-area transistors and (**right**) a nanoscale transistor. In case of large-area devices the ΔV_{th} shift which recovers appears to be seemingly lower at lower recover bias. However, the main reason for this observation is that the trap level of most of the defects is shifted far above the Fermi level of the channel, compared to the case for larger recovery biases, which leads to small charge emission times below the measurement delay. Thus, a significant bias dependence of the overall device recovery can be observed. The recovery behavior of defects from a nanoscale device exhibit emission times which can be either change with recovery bias (defects #1 and #3), or can be independent of the selected recovery bias (defect #2). Also remarkable is that defects can become shifted outside measurement window when the recover bias becomes too large.

4. Time-Dependent Defect Spectroscopy of Metal-Oxide-Semiconductor (MOS) Transistors

Most of the characterization techniques proposed to investigate defect distributions and densities at various bias and temperature conditions employing large-area devices. One prominent example is the so called deep level transient spectroscopy (DLTS) [40] which has been adopted to extract the interface state density of MOS transistors [62]. In DLTS the interface traps can get charged by majorities when an accumulation pulse is applied. When the bias is switched to deep inversion, the traps emit their charge which can be observed as a temporal change in the device capacitance.

The time-dependent defect spectroscopy (TDDS) makes use of the principle of DLTS, applies it to miniaturized devices and augments it by a statistical analysis. The main prerequisite of TDDS is that the devices are small enough to reveal charge transition events as discrete steps of measurable size in the device current. According to recent reports the step height of the defects is proportional to the effective gate area, that is, $\eta = A\eta_0$ [61,63–66]. In contrast, the number of traps significantly decreases

with the device geometry, that is, $N_\mathrm{T} = N_{\mathrm{T0}}/A$ [66]. Quite remarkable, in most recent technologies less than one trap per device can be present, however, its impact can evolve so pronounced that a charge transition can lead to a serious change of the device characteristics. Thus the proper operation of a single device can be solely determined by only one defect. Furthermore, the step heights produced by the individual defects which have been observed in single-defect investigations are widely distributed, ranging from several tens of micro-volts up to more than 30 mV and even higher depending on the device geometry [53]. To approximate their distribution an exponential distribution can be used [53,67]. The detection limit of the steps is basically given by the limited drain/source current measurement resolution of the instruments used. Note that for TDDS often custom-designed circuits are used enabling highest measurement resolution and performance [53].

The procedure to extract their charge transition kinetics, that is, their respective charge capture and emission times, as well as their steps heights will be discussed next in great detail.

4.1. Extraction of Charge Emission Time

To extract the average charge emission time at a certain gate bias the measure-stress-measure (MSM) scheme from Figure 2 (right) is applied. As already mentioned, during the stress phase a number of defects is energetically shifted below the Fermi level of the channel can become charged. After a certain stress time has elapsed the gate bias is switched to a recovery bias, and the current through the device is recorded, and afterwards mapped to an equivalent ΔV_th which is shown in Figure 7 (top).

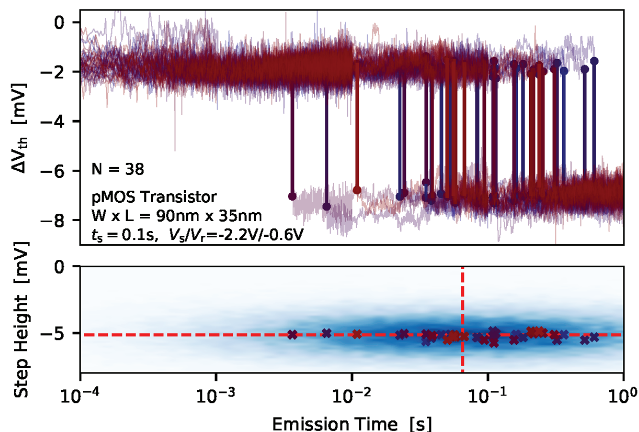

Figure 7. To extract the average charge capture time of a defect at a certain recovery bias the MSM sequence from Figure 2 (right) is applied, and N cycles at the same biases, temperature and stress/recovery times are measured. (**top**) The discrete steps in each recovery trace are extracted and binned into a (**bottom**) 2D histogram, which is called spectral map. In case that a number of emission events from a certain defect is available, a cluster is formed in the spectral map. Each of the clusters can be considered the finger print of a defect. The dashed lines in the spectral map indicate the average emission time, and the average step height, of the defect.

If the device is small enough discrete steps, which correspond to charge emission events of defects, can be observed. Afterwards, a step detection algorithm is applied to the measurement data in order to extract the charge transition events [68,69], which are then binned into a 2D histogram called spectral map, see Figure 7 (bottom). As can be seen, the charge emission transitions form a cluster in the spectral map, which is considered the fingerprint of the defect. The average step height of the defects can be considered to follow a normal distribution due to the measurement noise. To check for the distribution of the single emission time instances the bull percentile function can be analyzed [70,71], see Figure 8 (left).

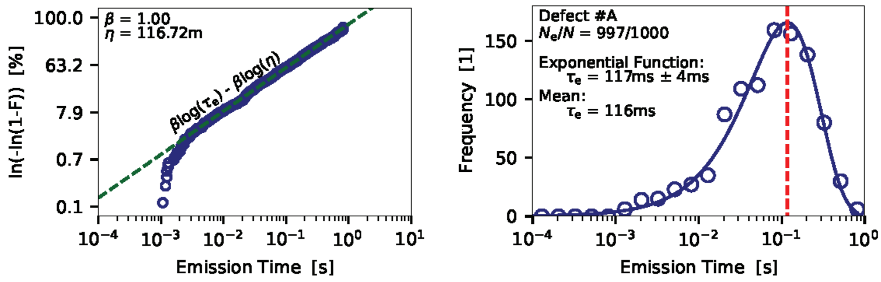

Figure 8. (**left**) The Weibull percentile function of the emission times indicates that the emission times follow an exponential distribution. (**right**) By binning the emission times into a histogram and applying the exponential distribution function the average emission time of the defect can be calculated. An almost equal average emission time is obtained when the mean value of transition times is calculated.

For this the probability estimator [72]

$$F = \frac{i - 0.3}{N_e + 0.4}, \tag{1}$$

with i being the rank of the data point in the emission time series sorted in ascending order, and N_e is the total number of emission events which are assigned to a certain defect. In case of $\beta = 1$, as can be seen for the log-linear function in Figure 8 (left), the Weibull distribution function transfers to an exponential distribution function

$$f_{WB}(x) = \lambda\beta(\lambda x)^{\beta-1}e^{-(\lambda x)^{\beta}} \xrightarrow{\beta=1} f_{EXP}(x) = \lambda e^{-\lambda x}, \tag{2}$$

with $\lambda = 1/\tau_e$. Alternatively, the exponential distribution of the charge emission events also becomes evident when the emission time points are binned into a histogram, see Figure 8 (right). It has to be noted that the quality of the histogram depends on the number of data points available and on the number of chosen bins. A more direct approach to calculate the average charge emission time is to calculate the mean value of the considered emission events

$$\tau_e = \frac{1}{N_e}\sum_{i=0}^{N_e-1} \tau_{e,i}. \tag{3}$$

As noted in Figure 8 (right), by doing so the average emission time calculated lies well within the uncertainty of the estimation using the exponential distribution function. In a next step the charge capture of the defects has be extracted which will be discussed.

4.2. Extraction of Charge Capture Time

In contrast to the direct extraction of the charge emission time from the recovery traces, the charge capture time cannot be determined directly, but can be extracted employing an indirect approach. For charge capture it can be assumed that the longer the stress time is the larger the probability of a defect to get charged becomes, when the same stress bias is considered. Thus, the expectation value of the occupancy, that is, the ratio between the number of recovery traces in which an emission event of the corresponding defect can be observed N_e and the total number of traces measured N_N, follows

$$O(t_s) = A(1 - e^{-\frac{t_s}{\tau_c}}), \tag{4}$$

with A the occupancy and τ_c the charge capture time. The correlation between different stress times and the occupancy function is shown in Figure 9 (middle). As can be seen from the corresponding spectral maps for defect #B, with increasing stress time the respective cluster becomes brighter, that is, the occupancy $O = N_e/N_N$ increases. After the values for the occupancy have been extracted at a number of different stress times, the charge capture time can be estimated by applying Equation (4).

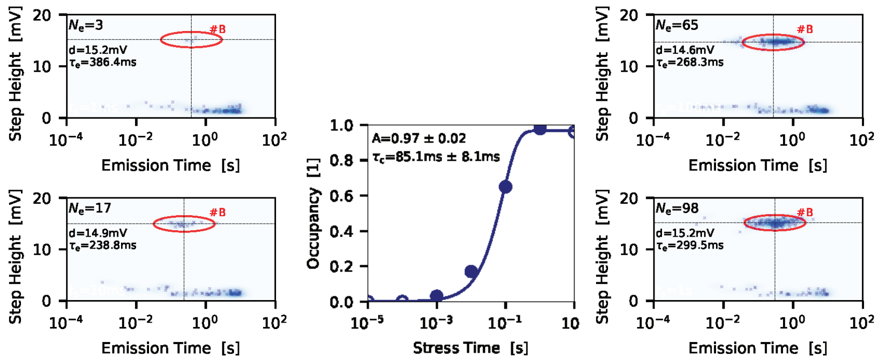

Figure 9. To extract the charge capture time a series of spectral maps (**left** and **right** images) for sequentially increasing stress times is recorded. From each spectral map the occupancy, that is, the ratio between the number of emission events of a certain defect and the number of traces measured, can be extracted. The occupancy follows an exponential behavior (**middle**) enabling to extract the charge capture time at a selected stress bias and device temperature.

To determine the charge emission times over a wider bias range, the extraction method has to be performed for various stress biases. The upper limit for the stress bias is the breakdown voltage of the oxide, and the lower limit is given by the trap level of the defect, as this has to be shifted below the Fermi level of the channel during the stress phase. It has to be noted that, especially for defects with large capture time, the extraction scheme can be very time consuming. In order to extend the the measurement window for slow defects, the measurements can be performed at higher device temperatures, which can significantly elevate the extraction of the charge transition times at low stress biases.

The next steps is to provide an explanation for the extracted charge trapping kinetics of the defect. One promising approach relies on the non-radiative multiphonon theory, and will be amongst others discussed in the following.

5. Modeling of Charge Trapping

Most models developed to explain BTI aim at the reproduction of the temporal behavior of the ΔV_{th} at different stress and recovery biases and at different device temperatures. The measured ΔV_{th} typically shows a recoverable component, that is, the part of ΔV_{th} which can be observed during the recovery cycle, and a permanent component, that is, the fraction of ΔV_{th} which remains at the end of the respective trace. Thus, a suitable model necessarily has to be able to explain both contributions to the measured threshold voltage shift precisely.

A straight-forward approach to explain the experimental data is to use empirical models. However, such models typically aim at describing the data by simple mathematical formulas, but omit the detailed physical mechanism behind the phenomena. In the context of device physics experimental data can often be modeled using a power law or exponential-like functions [73,74]. Although empirical models can be used for comparing different technologies, they have to be treated with care as they do not provide a physics based explanation for the observations. Thus extrapolations of the data, for instance to estimate the device lifetime, may not be very accurate. Another disadvantage of

empirical models is that they have been developed to explain a continuous trend in device threshold degradation and recovery, and are not designed to explain the discrete charge trapping behavior of scaled devices. To describe such a device behavior a stochastic charge trapping model is required rather than an approximation by a simple power law.

Attempts for the description of charge trapping have been based on the assumption that charge capture an emission can be explained by an elastic tunneling process [75–77]. During an elastic tunneling process a charge carrier can transit from a reservoir, that is, the device channel, to a respective defect site and get trapped without changing its energy. In this case, the charge transition rates are found to be proportional to the trap depth, $\tau \propto \exp -x/x_0$, which introduced difficulties when describing the large charge transition times for miniaturized devices which exhibit thin oxides [78,79]. Another limitation of elastic tunneling models is that the tunneling process is almost temperature independent, which cannot account for the considerable temperature dependence of charge trapping, see Figure 4 (right). As a consequence, models which assume elastic tunneling may not provide an accurate description of charge trapping considering BTI.

A very promising approach to model BTI was initially proposed in Reference [78] and has been refined in References [34,80]. The model is based on the concept of charge trapping which has been introduced to describe the stochastic nature of noise signals, that is, RTN and $1/f$ noise [81,82] and relies on hole trapping at defect sites which are located in the oxide supported by a multiphonon emission (MPE) process [75,83]. With MPE processes considerably larger charge capture and emission times can be achieved, which makes the model more suitable for BTI [84]. In the initial approach the HDL model has been used to explain charge trapping of switching oxide traps [85]. One characteristics of switching oxide traps is that their charge capture and emission time are bias dependent. Such a behavior can be described by three-state defect model. Later a notable number of single defect studies revealed that defects can also exhibit bias independent charge emission times. Such a behavior is referred to as fixed oxide traps [80]. Such a behavior can be described by the introduction of an additional defect state to the HDL model, leading to the four-state defect model shown in Figure 10.

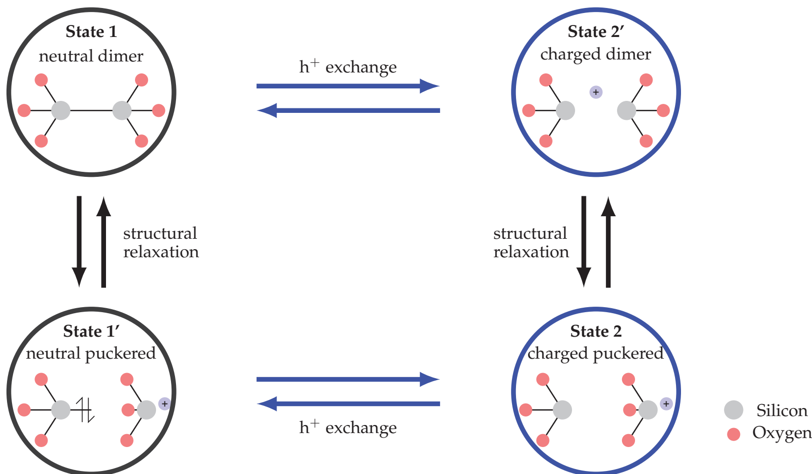

Figure 10. The non-radiative multiphonon (NMP) defect model has been proposed to explain the charge trapping kinetics of single defects. The model considers four defect states, two neutral defect states 1 and 1′ and two charged defect states 2′. The prime states are considered the meta-stable states of the system whereas the other states are the stable states. Either by exchanging a charge carrier or by structural relaxation the defect can charge its current state within in the NMP model. For a certain defect candidate, here shown for the E′ center, a certain atomic configuration of a defect can be assigned to one of the states of the defect model.

The four-state NMP model consists of two stable states (1 and 2) and two metastable states (1′ and 2′). In the model the transitions between the defect states are either described by an NMP process for the transitions where a charge exchange takes place, that is, $1 \rightarrow 2'$ or $2 \rightarrow 1'$, or by a thermal barrier, that is, $1 \rightarrow 1'$ or $2 \rightarrow 2'$, where the defect undergoes a structural relaxation but does not change its charge state. A significant difference between both barriers is that the charge transfer reaction leads to bias dependent transition times, while the thermal barriers results in bias independent transition times. In order to ensure the physical accuracy of the model an atomic configuration of a certain defect candidate can be assigned to each state of the model. In Figure 10 the atomic configurations of the so called E′ center, which have been calculated using *ab-initio* methods, are shown [86]. This defect class has been proposed as hole trap candidate in pMOS transistors [87,88]. Further trap candidates are defects involving hydrogen, namely defects in the hydrogen bridge configuration [89,90] or hydroxyl E' centers [91]. The elongated oxygen bond has been proposed as suitable electron trap candidate for charge trapping in nMOS devices [92].

In the final section of this paper the different charge trapping behavior of defects which have been observed from single defect investigations and the corresponding configuration of the defect model to explain the trap behavior is discussed.

6. Results

In the following, results from single defect studies performed on nanoscale devices are discussed in detail. The shown charge trapping kinetics has been extracted either by applying TDDS, or from RTN measurements, and is modeled considering the four-state defect model. It can be observed that the model nicely explains the experimental data. In addition to the charge trapping kinetics, the impact of the defects on the device behavior is also an important parameter for device reliability assessment. This can be analyzed by calculating distribution function of step heights of the single charge transition events, which is subject of the second part of this section.

6.1. Charge Trapping Kinetics of Single Defects

Extensive studies employing the previously mentioned TDDS have been carried out using utilizing pMOS and nMOS transistors. These investigations reveled many peculiarities visible in the charge trapping kinetics of the defects, which all have to be covered by a uniform model. It has been observed that the charge emission times of traps can be either (i) bias-dependent, which is typically referred to as *switching trap*, or (ii) bias-independent, a behavior which is assigned to so called *fixed oxide traps*. In both cases strong bias dependent charge capture times are observed. Another remarkable observation is that (iii) defects can show a volatile behavior [93]. More detailed, a small number of defects have been observed to vanish from the spectral map and some of them reappeared in the spectral maps at a later time point. It has to be noted that volatile defects have been observed in nMOS and pMOS devices using SiON and high-k gate stacks and are thus not limited to any particular technologies. As the phenomenon is stochastic, it is very difficult study it systematically. However, these defects will an essential clue on the chemical nature of oxide traps.

In Figures 11 (left) and 12 (left) the charge trapping kinetics of two defects which have been extracted from SiON pMOS transistors is shown.

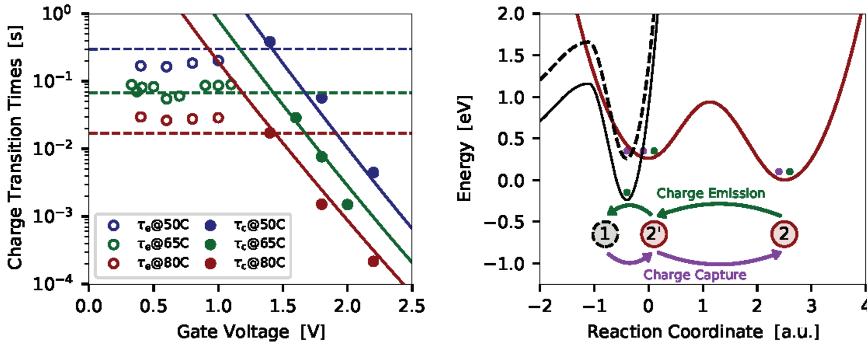

Figure 11. (**left**) The charge trapping kinetics for a *fixed trap* is shown at different temperatures (symbols ... measurement data, lines ... simulations). As can be seen, the fixed trap shows bias dependent charge capture times, but bias independent charge emission times. (**right**) To explain this behavior three states of the defect model are used and the pathways for charge capture an emission are shown together with the corresponding approximation for the potential energy surfaces.

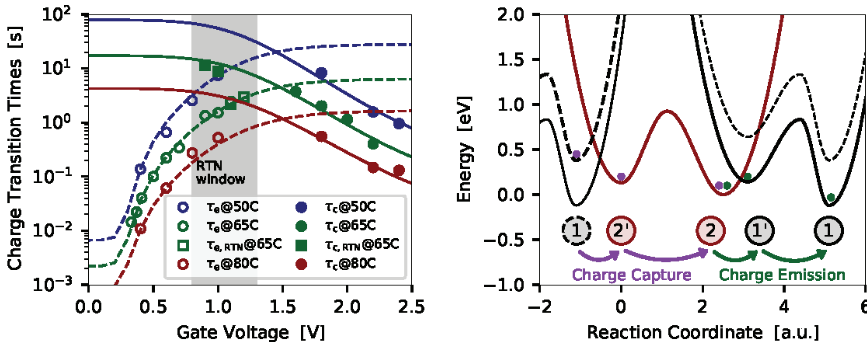

Figure 12. (**left**) The charge transition times of a *switching trap* shows bias dependent charge capture and charge emission times (symbols ... measurement data, lines ... simulations). (**right**) To explain the bias and temperature dependence the four state defect model is used and the corresponding approximation for the potential energy surfaces (PES) is shown. This kind of defect requires four defect states in order to properly capture the trapping behavior.

The defect presented in Figure 11 (left) shows a fixed trap characteristic with bias-independent charge emission times, but bias dependent charge capture times. The corresponding configuration coordinate diagram with the potential energy surfaces (PESs) used to describe the charge transitions is given in Figure 11 (right). As already mentioned, the energy of the atomic configuration of the different defect states of the NMP model is calculated using density functional theory. The transitions from one defect state to another are then approximated by a harmonic oscillator, which is represented by the PESs. The PESs either describe the situation of a neutral defect where the carrier is in its reservoir, or describe the situation where a carrier is trapped at a defect. A transition between the two states, that is, a charger transfer reaction, can occur when a carrier surpasses the energy barrier between two states. To account for the bias dependence the relative position of the PESs is shifted according to the change of the trap level when a gate bias is applied at the device. In case of a fixed trap, the transition barrier between the states 1 and 2′ becomes relatively small when a gate bias is applied, see dashed PES in Figure 11 (right). The system can further overcome the thermal barrier between the states 2′ and 2, and finally transit to the stable charge state 2. In summary, the charge transition proceeds via the pathway $1 \rightarrow 2' \rightarrow 2$. The switching trap from Figure 12 follows the same pathway when a charge

capture event occurs. However, the charge emission behaviors different for both cases. In case of the fixed trap, the thermal barrier between the states 2 and 2′ determines the charge emission process, while the barrier between the states 2′ and 1 is very small, see solid PES in Figure 11. Thus, the charge emission follows the pathway $2 \rightarrow 2' \rightarrow 1$. In contrast, charge emission for the switching trap proceeds via the pathway $2 \rightarrow 1' \rightarrow 1$. Here the barrier between the states 2 and 1′ (solid PES in Figure 12) determines the charge emission time. It has to be noted that the charge transition processes, meaning the transitions between different charge states of a defect, can be observed in the measurements as discrete steps in the current. The thermal barriers are given by the overall charge trapping dynamics, but transitions via these barriers are not directly visible in the measurement data.

Once the defect model is calibrated to a number of defects the parameters can be extended to explain BTI in large-area devices. For this the trap levels and energy barriers are considered distributed, which enables to calculate a number of defects with different configuration of their PESs. Finally, the superposition of an large ensemble of defects allow explanation of BTI in large-area devices [94]. Based on this accurate lifetime estimations can be made. Quite recently, the two-state defect model has been implemented into a 1D reliability simulator Comphy [55] and successfully applied to explain BTI in various technologies. Lately it has also been demonstrated that the defect model in combination with TCAD simulations can nicely explain charge trapping in SiC transistors, where a good agreement between the extracted trap parameters and results from DFT calculations has been observed [11]. Furthermore, it has been demonstrated that empirical models typically omit effects like saturation of the ΔV_{th} with increasing stress time, but rather predict indefinitely large ΔV_{th} when the stress time becomes very large. However, such extrapolations are rather un-physical and pessimistic, thus a physics based approach for explaining charge trapping, like the NMP defect model in combination with TCAD simulations, considering the charge trapping kinetics of single defects to explain charge trapping is preferred.

6.2. Distribution of Step Heights of Single Defects

To estimate the impact of a single defect on the device behavior the charge sheet approximation (CSA), which assumes that the oxide charge is spread over the insulator according to [75]

$$\Delta V_{\mathrm{th}} = -\frac{q}{\epsilon_0 \epsilon_{\mathrm{r}} W L} t_{\mathrm{ox}} \left(1 - \frac{x_{\mathrm{T}}}{t_{\mathrm{ox}}}\right), \tag{5}$$

with the elementary charge q, the dielectric constants ϵ_0 and ϵ_{r}, the oxide thickness t_{ox} and the position of the trap x_{T}, is typically used. By applying the CSA the trap density can be estimated from a given ΔV_{th} [55,95]. However, considering the CSA typically leads to an overestimation of the trap density, as the real average impact of a defect on the overall ΔV_{th} has been observed to be more pronounced, when measurements of different technologies are evaluated [25,49,96]. In order to determine the average impact of a single trap on the ΔV_{th}, the distribution function (CDF) of step heights has to be created and analyzed [25,96]. To extract the CDF stress-recovery measurements have to be performed employing a number of devices of the same technology. For each device one recovery trace is measured after the device has been stressed for typically 1 ks at oxide fields up to 10 MV/cm. Afterwards, the charge transitions of each trace are extracted and the CDF created, see Figure 13.

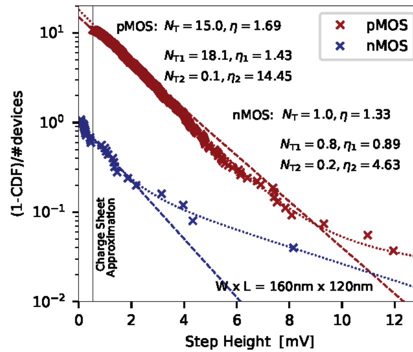

Figure 13. The complementary cumulative distribution function (CDF) is shown for nMOS and pMOS SiON transistors of equal active gate area. The insulator thickness is t_{ox} = 2.2 nm for all devices. As can be seen, the complementary CDF reveals two branches for both kinds of transistors. Such a behavior can be well described by Equation (8) (dashed lines consider uni-modal exponential distribution, dotted lines consider bi-modal exponential distribution). Additionally, the maximum step height calculated considering the CSA is also shown (solid black line). As can be clearly seen, the CSA significantly underestimates the effective impact of the single defects on the overall shift of device threshold voltage. Furthermore, it can be seen the number of active traps seems to be higher in pMOS devices compared to the nMOS counterparts.

It can be seen, that the step heights are exponentially distributed and can be described by the respective probability distribution function (PDF)

$$f(\Delta V_{\mathrm{th}}) = \frac{1}{\eta} \mathrm{e}^{-\frac{\Delta V_{\mathrm{th}}}{\eta}} \tag{6}$$

with η the mean threshold voltage shift caused by a single charge transition event of a certain defect. From the PDF the cumulative distribution function (CDF) can now be calculated

$$F(\Delta V_{\mathrm{th}}) = \int f(\Delta V_{\mathrm{th}}) \mathrm{d}\Delta V_{\mathrm{th}} = 1 - \mathrm{e}^{-\frac{\Delta V_{\mathrm{th}}}{\eta}}. \tag{7}$$

To study the distribution of the step heights the complementary CDF is used, and is evaluated normalized to the number of devices

$$\frac{1 - CDF}{\#devices} = \sum_i N_i \mathrm{e}^{-\frac{\Delta V_{\mathrm{th}}}{\eta_i}}, \tag{8}$$

with N_i the average number of active defects per devices. The expression above already accounts for multi-modal behavior of the experimental complementary CDFs. Note, one advantage of the normalization of the complementary CDF is that the number of traps per device is directly accessible from the plots.

A remarkable observation here is that the distribution function of the step heights follow a bi-modal exponential distribution. Recent studies [63] suggest that the bi-modal exponential distribution is typical for devices employing high-k gate stacks, where one branch is attributed to charge transfer reactions between the channel and the high-k layer, and the second branch accounts for channel/SiO_2 trap interaction. However, it turned out that bi-modal exponential distributions can also be observed for devices with an SiON insulator [53,96]. In Reference [96] it has been suggested that the two branches of the complementary CDF measured from nMOS devices can be separated into gate/defect and channel/defect interactions.

Another important finding is that exponentially distributed amplitudes have also been found for RTN signals [97–99]. These findings strengthen the link between RTN and BTI [25,80]. Furthermore, the average contribution of a single trap to the threshold voltage shift η plays an important role in the context of device variability in deeply scaled devices [67,99–101].

7. Conclusions

The characterization and accurate modeling of the reliability of miniaturized transistors poses a major challenge for measurement instrumentation, defect modeling and device simulation. In order to explain the experimental observation empirical models are often used. However, such models typically omit certain observations, like saturation of the drift of the threshold voltage with increasing stress time. In order to provide a physical description of the measurement data the four-state defect model has been proposed, and is discussed here. The defect model is based on the charge trapping kinetics of single defects which can be observed in miniaturized devices. To extract the trapping behavior the time-dependent defect spectroscopy (TDDS) can be used. From recent TDDS studies it has been observed that defects exhibit bias dependent charge capture times, but certain defects exhibit bias-independent charge emission times while others show bias-dependent charge emission times. Both characteristics can be nicely explained by the defect model. To explain the behavior of large-area devices a number of defects with distributed trap levels and energy barriers for charge transitions have to be calculated, and their superposition enable to describe the devices' behavior. These simulations can be further used to accurately extract the lifetime of the devices under various operating conditions. Finally, the distribution function of step heights is discussed, and it is shown that the typically use charge sheet approximation significantly underestimates the effective impact of a defect on the device behavior. This is especially important for circuit designers to ensure a high robustness of the applications against charge trapping.

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References

1. Hisamoto, D.; Lee, W.-C.; Kedzierski, J.; Anderson, E.; Takeuchi, H.; Asano, K.; King, T.-J.; Bokor, J.; Hu, C. A folded-channel MOSFET for deep-sub-tenth micron era. In Proceedings of the International Electron Devices Meeting 1998. Technical Digest, San Francisco, CA, USA, 6–9 December 1998; pp. 1032–1034. [CrossRef]
2. Huang, X.; Lee, W.-C.; Kuo, C.; Hisamoto, D.; Chang, L.; Kedzierski, J.; Anderson, E.; Takeuchi, H.; Choi, Y.-K.; Asano, K.; et al. Sub 50-nm FinFET: PMOS. In Proceedings of the International Electron Devices Meeting 1999. Technical Digest, Washington, DC, USA, 5–8 December 1999; pp. 67–70.
3. Yu, B.; Chang, L.; Ahmed, S.; Wang, H.; Bell, S.; Yang, C.-Y.; Tabery, C.; Ho, C.; Xiang, Q.; King, T.-J.; et al. FinFET scaling to 10 nm gate length. In Proceedings of the Digest. International Electron Devices Meeting, San Francisco, CA, USA, 8–11 December 2002; pp. 251–254.
4. Loubet, N.; Hook, T.; Montanini, P.; Yeung, C.; Kanakasabapathy, S.; Guillom, M.; Yamashita, T.; Zhang, J.; Miao, X.; Wang, J.; et al. Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET. In Proceedings of the IEEE Symposium on VLSI Technology, Kyoto, Japan, 5–8 June 2017; pp. T230–T231.
5. Yang, B.; Buddharaju, K.D.; Teo, S.H.G.; Singh, N.; Lo, G.Q.; Kwong, D.L. Vertical Silicon-Nanowire Formation and Gate-All-Around MOSFET. *IEEE Electron Device Lett.* **2008**, *29*, 791–794. [CrossRef]
6. Bangsaruntip, S.; Cohen, G.M.; Majumdar, A.; Zhang, Y.; Engelmann, S.U.; Fuller, N.C.M.; Gignac, L.M.; Mittal, S.; Newbury, J.S.; Guillorn, M.; et al. High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling. In Proceedings of the 2009 IEEE International Electron Devices Meeting (IEDM), Baltimore, MD, USA, 7–9 December 2009; pp. 1–4.
7. Yeo, K.H.; Suk, S.D.; Li, M.; Yeoh, Y.; Cho, K.H.; Hong, K.; Yun, S.; Lee, M.S.; Cho, N.; Lee, K.; et al. Gate-All-Around (GAA) Twin Silicon Nanowire MOSFET (TSNWFET) with 15 nm Length Gate and 4 nm

Radius Nanowires. In Proceedings of the 2006 International Electron Devices Meeting, San Francisco, CA, USA, 11–13 December 2006; pp. 1–4.
8. Kato, Y.; Takao, H.; Sawada, K.; Ishida, M. The Characteristic Improvement of Si (111) Metal–Oxide–Semiconductor Field-Effect Transistor by Long-Time Hydrogen Annealing. *Jpn. J. Appl. Phys.* **2004**, *43*, 6848–6853. [CrossRef]
9. Xiong, W.; Gebara, G.; Zaman, J.; Gostkowski, M.; Nguyen, B.; Smith, G.; Lewis, D.; Cleavelin, C.R.; Wise, R.; Yu, S.; et al. Improvement of FinFET electrical characteristics by hydrogen annealing. *IEEE Electron Device Lett.* **2004**, *25*, 541–543. [CrossRef]
10. Pollack, G.P.; Richardson, W.F.; Malhi, S.D.S.; Bonifield, T.; Shichijo, H.; Banerjee, S.; Elahy, M.; Shah, A.H.; Womack, R.; Chatterjee, P.K. Hydrogen passivation of PolySilicon MOSFET's from a plasma Nitride source. *IEEE Electron Device Lett.* **1984**, *5*, 468–470. [CrossRef]
11. Schleich, C.; Berens, J.; Rzepa, G.; Pobegen, G.; Rescher, G.; Tyaginov, S.; Grasser, T.; Waltl, M. Physical Modeling of Bias Temperature Instabilities in SiC MOSFETs. In Proceedings of the 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 7–11 December 2019.
12. Pippel, E.; Woltersdorf, J.; Olafsson, H.Ö.; Sveinbjörnsson, E.Ö. Interfaces between 4H-SiC and SiO2: Microstructure, nanochemistry, and near-interface traps. *J. Appl. Phys.* **2005**, *97*, 034302. [CrossRef]
13. Berens, J.; Rasinger, F.; Aichinger, T.; Heuken, M.; Krieger, M.; Pobegen, G. Detection and Cryogenic Characterization of Defects at the SiO2/4H-SiC Interface in Trench MOSFET. *IEEE Trans. Electron Devices* **2019**, *66*, 1213–1217. [CrossRef]
14. Bravaix, A.; Guerin, C.; Goguenheim, D.; Huard, V.; Roy, D.; Besset, C.; Renard, S.; Randriamihaja, Y.M.; Vincent, E. Off State Incorporation into the 3 Energy Mode Device Lifetime Modeling for Advanced 40 nm CMOS Node. In Proceedings of the 2010 IEEE International Reliability Physics Symposium, Anaheim, CA, USA, 2–6 May 2010; pp. 55–64. [CrossRef]
15. Tyaginov, S.; Starkov, I.; Enichlmair, H.; Park, J.; Jungemann, C.; Grasser, T. Physics-Based Hot-Carrier Degradation Models. *ECS Trans.* **2011**, 321–352.
16. Doyle, B.S.; Mistry, K.R. The characterization of hot carrier damage in p-channel transistors. *IEEE Trans. Electron Devices* **1993**, *40*, 152–156. [CrossRef]
17. Bury, E.; Chasin, A.; Vandemaele, M.; Van Beek, S.; Franco, J.; Kaczer, B.; Linten, D. Array-Based Statistical Characterization of CMOS Degradation Modes and Modeling of the Time-Dependent Variability Induced by Different Stress Patterns in the $\{V_G, V_D\}$ bias space. In Proceedings of the 2019 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 31 March–4 April 2019; pp. 1–6.
18. Cohen, N.L.; Paulsen, R.E.; White, M.H. Observation and characterization of near-interface oxide traps with C-V techniques. *IEEE Trans. Electron Devices* **1995**, *42*, 2004–2009. [CrossRef]
19. Miura, Y.; Matukura, Y. Investigation of Silicon-Silicon Dioxide Interface Using MOS Structure. *Jpn. J. Appl. Phys.* **1966**, *5*, 180. [CrossRef]
20. Grasser, T.; Kaczer, B.; Aichinger, T.; Goes, W.; Nelhiebel, M. Defect Creation Stimulated by Thermally Activated Hole Trapping as the Driving Force Behind Negative Bias Temperature Instability in SiO2, SiON, and High-k Gate Stacks. In Proceedings of the 2008 IEEE International Integrated Reliability Workshop Final Report, South Lake Tahoe, CA, USA, 12–16 October 2008; pp. 91–95. [CrossRef]
21. Schroder, D.K.; Babcock, J. Negative Bias Temperature Instability: Road to Cross in Deep Submicron Silicon Semiconductor Manufacturing. *J. Appl. Phys.* **2003**, *94*, 1–18. [CrossRef]
22. Gerrer, L.; Ding, J.; Amoroso, S.; Adamu-Lema, F.; Hussin, R.; Reid, D.; Millar, C.; Asenov, A. Modelling RTN and BTI in nanoscale MOSFETs from device to circuit: A review. *Microelectron. Reliab.* **2014**, *54*, 682–697. [CrossRef]
23. Onishi, K.; Choi, R.; Kang, C.S.; Cho, H.-J.; Kim, Y.H.; Nieh, R.E.; Han, J.; Krishnan, S.A.; Akbar, M.S.; Lee, J.C. Bias-temperature instabilities of polysilicon gate HfO/sub 2/ MOSFETs. *IEEE Trans. Electron Devices* **2003**, *50*, 1517–1524. [CrossRef]
24. Martin-Martinez, J.; Rodriguez, R.; Nafria, M.; Aymerich, X. Time-Dependent Variability Related to BTI Effects in MOSFETs: Impact on CMOS Differential Amplifiers. *IEEE Trans. Device Mater. Reliab.* **2009**, *9*, 305–310. [CrossRef]
25. Kaczer, B.; Grasser, T.; Roussel, P.J.; Franco, J.; Degraeve, R.; Ragnarsson, L.A.; Simoen, E.; Groeseneken, G.; Reisinger, H. Origin of NBTI Variability in Deeply Scaled pFETs. In Proceedings of the 2010 IEEE International Reliability Physics Symposium, Anaheim, CA, USA, 2–6 May 2010; pp. 26–32. [CrossRef]

26. Reisinger, H.; Blank, O.; Heinrigs, W.; Muhlhoff, A.; Gustin, W.; Schlunder, C. Analysis of NBTI Degradation- and Recovery-Behavior Based on Ultra Fast VT–Measurements. In Proceedings of the 2006 IEEE International Reliability Physics Symposium Proceedings, San Jose, CA, USA, 26–30 March 2006; pp. 448–453. [CrossRef]
27. Ralls, K.S.; Skocpol, W.J.; Jackel, L.D.; Howard, R.E.; Fetter, L.A.; Epworth, R.W.; Tennant, D.M. Discrete Resistance Switching in Submicrometer Silicon Inversion Layers: Individual Interface Traps and Low-Frequency ($\frac{1}{f}$) Noise. *Phys. Rev. Lett.* **1984**, *52*, 228–231. [CrossRef]
28. Uren, M.J.; Day, D.J.; Kirton, M.J. 1/f and Random Telegraph Noise in Silicon Metal-Oxide-Semiconductor Field-Effect Transistors. *Appl. Phys. Lett.* **1985**, *47*, 1195–1197. [CrossRef]
29. Nagumo, T.; Takeuchi, K.; Yokogawa, S.; Imai, K.; Hayashi, Y. New analysis methods for comprehensive understanding of Random Telegraph Noise. In Proceedings of the 2009 IEEE International Electron Devices Meeting (IEDM), Baltimore, MD, USA, 7–9 December 2009; pp. 1–4. [CrossRef]
30. Tega, N.; Miki, H.; Pagette, F.; Frank, D.J.; Ray, A.; Rooks, M.J.; Haensch, W.; Torii, K. Increasing threshold voltage variation due to random telegraph noise in FETs as gate lengths scale to 20 nm. In Proceedings of the IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 15–17 June 2009; pp. 50–51.
31. Veksler, D.; Bersuker, G.; Vandelli, L.; Padovani, A.; Larcher, L.; Muraviev, A.; Chakrabarti, B.; Vogel, E.; Gilmer, D.C.; Kirsch, P.D. Random telegraph noise (RTN) in scaled RRAM devices. In Proceedings of the 2013 IEEE International Reliability Physics Symposium (IRPS), Anaheim, CA, USA, 14–18 April 2013; pp. MY.10.1–MY.10.4. [CrossRef]
32. Wang, R.; Guo, S.; Zhang, Z.; Zou, J.; Mao, D.; Huang, R. Complex Random Telegraph Noise (RTN): What Do We Understand? In Proceedings of the 2018 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), Singapore, 16–19 July 2018; pp. 1–7. [CrossRef]
33. Simicic, M.; Weckx, P.; Parvais, B.; Roussel, P.; Kaczer, B.; Gielen, G. Understanding the Impact of Time-Dependent Random Variability on Analog ICs: From Single Transistor Measurements to Circuit Simulations. *IEEE Trans. VLSI Syst.* **2019**, *27*, 601–610. [CrossRef]
34. Grasser, T.; Reisinger, H.; Wagner, P.J.; Goes, W.; Schanovsky, F.; Kaczer, B. The Time Dependent Defect Spectroscopy (TDDS) for the Characterization of the Bias Temperature Instability. In Proceedings of the 2010 IEEE International Reliability Physics Symposium, Anaheim, CA, USA, 2–6 May 2010; pp. 16–25. [CrossRef]
35. Grasser, T.; Reisinger, H.; Wagner, P.J.; Kaczer, B. The Time Dependent Defect Spectroscopy for the Characterization of Border Traps in Metal-Oxide-Semiconductor Transistors. *Phys. Rev. B* **2010**, *82*, 245318. [CrossRef]
36. Rao, V.R.; Wittmann, F.; Gossner, H.; Eisele, I. Hysteresis behavior in 85-nm channel length vertical n-MOSFETs grown by MBE. *IEEE Trans. Electron Devices* **1996**, *43*, 973–976. [CrossRef]
37. Chatty, K.; Banerjee, S.; Chow, T.P.; Gutmann, R.J. Hysteresis in transfer characteristics in 4H-SiC depletion/accumulation-mode MOSFETs. *IEEE Electron Device Lett.* **2002**, *23*, 330–332. [CrossRef]
38. Pacelli, A.; Lacaita, A.L.; Villa, S.; Perron, L. Reliable extraction of MOS interface traps from low-frequency CV measurements. *IEEE Electron Device Lett.* **1998**, *19*, 148–150. [CrossRef]
39. Romanjek, K.; Andrieu, F.; Ernst, T.; Ghibaudo, G. Improved split C-V method for effective mobility extraction in sub-0.1-μm Si MOSFETs. *IEEE Electron Device Lett.* **2004**, *25*, 583–585. [CrossRef]
40. Lang, D.V. Deep-level transient spectroscopy: A new method to characterize traps in semiconductors. *J. Appl. Phys.* **1974**, *45*, 3023–3032. [CrossRef]
41. Bains, S.K.; Banbury, P.C. AC hopping conductivity and DLTS studies on electron-irradiated boron-doped silicon. *Semicond. Sci. Technol.* **1987**, *2*, 20–29. [CrossRef]
42. Scholz, F.; Hwang, J.; Schroder, D. Low frequency noise and DLTS as semiconductor device characterization tools. *Solid-State Electron.* **1988**, *31*, 205–217. [CrossRef]
43. McLarty, P.K.; Ioannou, D.E.; Colinge, J.P. Bulk traps in ultrathin SIMOX MOSFET's by current DLTS. *IEEE Electron Device Lett.* **1988**, *9*, 545–547. [CrossRef]
44. McLarty, P.K.; Ioannou, D.E. DLTS analysis of carrier generation transients in thin SOI MOSFETs. *IEEE Trans. Electron Devices* **1990**, *37*, 262–266. [CrossRef]
45. Denais, M.; Parthasarathy, C.; Ribes, G.; Rey-Tauriac, Y.; Revil, N.; Bravaix, A.; Huard, V.; Perrier, F. On-the-Fly Characterization of NBTI in Ultra–Thin Gate Oxide pMOSFET's. In Proceedings of the IEEE International Electron Devices Meeting, San Francisco, CA, USA, 13–15 December 2004; pp. 109–112. [CrossRef]

46. Deora, S.; Maheta, V.D.; Islam, A.E.; Alam, M.A.; Mahapatra, S. A Common Framework of NBTI Generation and Recovery in Plasma-Nitrided SiON p-MOSFETs. *IEEE Electron Device Lett.* **2009**, *30*, 978–980. [CrossRef]
47. Bezza, A.; Rafik, M.; Roy, D.; Federspiel, X.; Mora, P.; Ghibaudo, G. Frequency dependence of TDDB PBTI with OTF monitoring methodology in high-k/metal gate stacks. In Proceedings of the 2014 IEEE International Reliability Physics Symposium, Waikoloa, HI, USA, 1–5 June 2014; pp. GD.6.1–GD.6.4.
48. Lelis, A.J.; Habersat, D.; Green, R.; Ogunniyi, A.; Gurfinkel, M.; Suehle, J.; Goldsman, N. Time Dependence of Bias-Stress-Induced SiC MOSFET Threshold-Voltage Instability Measurements. *IEEE Trans. Electron Devices* **2008**, *55*, 1835–1840. [CrossRef]
49. Waltl, M.; Grill, A.; Rzepa, G.; Goes, W.; Franco, J.; Kaczer, B.; Mitard, J.; Grasser, T. Superior NBTI in high-k SiGe Transistors-Part I: Experimental. *IEEE Trans. Electron Devices* **2017**, *64*, 2092–2098. [CrossRef]
50. Kerber, A.; Kerber, M. Fast Wafer Level Data Acquisition for Reliability Characterization of Sub-100 nm CMOS Technologies. In Proceedings of the IEEE International Integrated Reliability Workshop Final Report, South Lake Tahoe, CA, USA, 13–15 December 2004; pp. 41–45. [CrossRef]
51. Du, G.A.; Ang, D.S.; Teo, Z.Q.; Hu, Y.Z. Ultrafast Measurement on NBTI. *IEEE Electron Device Lett.* **2009**, *30*, 275–277. [CrossRef]
52. Yu, X.; Lu, J.; Liu, W.; Qu, Y.; Zhao, Y. Ultra-fast (ns-scale) Characterization of NBTI Behaviors in Si pFinFETs. *IEEE J. Electron Devices Soc.* **2020**, *8*, 577–583. [CrossRef]
53. Waltl, M. Ultra-Low Noise Defect Probing Instrument for Defect Spectroscopy of MOS Transistors. *IEEE Trans. Device Mater. Reliab.* **2020**, *20*, 242–250. [CrossRef]
54. Reisinger, H.; Grasser, T.; Gustin, W.; Schlünder, C. The statistical analysis of individual defects constituting NBTI and its implications for modeling DC- and AC-stress. In Proceedings of the 2010 IEEE International Reliability Physics Symposium, Anaheim, CA, USA, 2–6 May 2010; pp. 7–15. [CrossRef]
55. Rzepa, G.; Franco, J.; O'Sullivan, B.J.; Subirats, A.; Simicic, M.; Hellings, G.; Weckx, P.; Jech, M.; Knobloch, T.; Waltl, M.; et al. Comphy—A Compact-Physics Framework for Unified Modeling of BTI. *Microelectron. Reliab.* **2018**, *85*, 49–65. [CrossRef]
56. Kaneta, C.; Yamasaki, T.; Uchiyama, T.; Uda, T.; Terakura, K. Structure and electronic property of Si(100)SiO_2 interface. *Microelectron. Eng.* **1999**, *48*, 117–120. [CrossRef]
57. Yamashita, Y.; Yamamoto, S.; Mukai, K.; Yoshinobu, J.; Harada, Y.; Tokushima, T.; Takeuchi, T.; Takata, Y.; Shin, S.; Akagi, K.; Tsuneyuki, S. Direct observation of site-specific valence electronic structure at the SiO_2/Si interface. *Phys. Rev. B* **2006**, *73*, 045336. [CrossRef]
58. Huiwen, Z.; Yongsong, L.; Lingfeng, M.; Jingqin, S.; Zhiyan, Z.; Weihua, T. Theoretical study of the SiO_2/Si interface and its effect on energy band profile and MOSFET gate tunneling current. *J. Semicond.* **2010**, *31*, 082003. [CrossRef]
59. Ullmann, B.; Puschkarsky, K.; Waltl, M.; Reisinger, H.; Grasser, T. Evaluation of Advanced MOSFET Threshold Voltage Drift Measurement Techniques. *IEEE Trans. Device Mater. Reliab.* **2019**, *19*, 358–362. [CrossRef]
60. Schroeder, D. Negative Bias Temperature Instability: What do we understand? *Microelectron. Reliab.* **2007**, *47*, 841–852. [CrossRef]
61. Waltl, M.; Goes, W.; Rott, K.; Reisinger, H.; Grasser, T. A Single-Trap Study of PBTI in SiON nMOS Transistors: Similarities and Differences to the NBTI/pMOS Case. In Proceedings of the 2014 IEEE International Reliability Physics Symposium, Waikoloa, HI, USA, 1–5 June 2014; pp. XT18.1–XT18.5. [CrossRef]
62. Wang, K.L.; Evwaraye, A.O. Determination of interface and bulk-trap states of IGFET's using deep-level transient spectroscopy. *J. Appl. Phys.* **1976**, *47*, 4574–4577. [CrossRef]
63. Toledano-Luque, M.; Kaczer, B.; Simoen, E.; Roussel, P.; Veloso, A.; Grasser, T.; Groeseneken, G. Temperature and Voltage Dependences of the Capture and Emission Times of Individual Traps in High-k Dielectrics. *Microelectron. Eng.* **2011**, *88*, 1243–1246. [CrossRef]
64. Toledano-Luque, M.; Kaczer, B.; Roussel, P.; Cho, M.; Grasser, T.; Groeseneken, G. Temperature Dependence of the Emission and Capture Times of SiON Individual Traps after Positive Bias Temperature Stress. *J. Vac. Sci. Technol. Nanotechnol. Microelectron. Mater. Process. Meas. Phenom.* **2010**, *29*, 1–2. [CrossRef]
65. Kaczer, B.; Grasser, T.; Martin-Martinez, J.; Simoen, E.; Aoulaiche, M.; Roussel, P.; Groeseneken, G. NBTI from the Perspective of Defect States with Widely Distributed Time Scales. In Proceedings of the 2009 IEEE International Reliability Physics Symposium, Montreal, QC, Canada, 26–30 April 2009; pp. 55–60. [CrossRef]

66. Kaczer, B.; Franco, J.; Weckx, P.; Roussel, P.J.; Bury, E.; Cho, M.; Degraeve, R.; Linten, D.; Groeseneken, G.; Kukner, H.; et al. The defect-centric perspective of device and circuit reliability—From individual defects to circuits. In Proceedings of the 2015 45th European Solid State Device Research Conference (ESSDERC), Graz, Austria, 14–18 September 2015; pp. 218–225.
67. Toledano-Luque, M.; Kaczer, B.; Roussel, P.J.; Franco, J.; Ragnarsson, L.A.; Grasser, T.; Groeseneken, G. Depth localization of positive charge trapped in silicon oxynitride field effect transistors after positive and negative gate bias temperature stress. *Appl. Phys. Lett.* **2011**, *98*, 183506. [CrossRef]
68. Stampfer, B.; Schanovsky, F.; Grasser, T.; Waltl, M. Semi-Automated Extraction of the Distribution of Single Defects for nMOS Transistors. *Micromachines* **2020**, *11*, 446. [PubMed]
69. Canny, J. A Computational Approach to Edge Detection. *IEEE Trans. Pattern Anal. Mach. Intell.* **1986**, *PAMI-8*, 679–698. [CrossRef]
70. Bernard, A.; Bos-Levenbach, E.J. *The Plotting of Observations on Probability-Paper*; Stichting Mathematisch Centrum: Amsterdam, the Netherlands, 1955.
71. Hudak, D.; Tiryakioğlu, M. On estimating percentiles of the Weibull distribution by the linear regression method. *J. Mater. Sci.* **2009**, *44*, 1959–1964. [CrossRef]
72. Tiryakioğlu, M.; Hudak, D. On estimating Weibull modulus by the linear regression method. *J. Mater. Sci.* **2007**, *42*, 10173–10179. [CrossRef]
73. McPherson, J.W. *Reliability Physics and Engineering: Time-To-Failure Modeling*; Springer: Berlin, Germany, 2010.
74. Huard, V.; Denais, M.; Parthasarathy, C. NBTI degradation: From physical mechanisms to modelling. *Microelectron. Reliab.* **2006**, *46*, 1–23. [CrossRef]
75. Tewksbury, T. Relaxation Effects in MOS Devices due to Tunnel Exchange with Near-Interface Oxide Traps. Ph.D. Thesis, MIT, Cambridge, MA, USA, 1992.
76. Shen, C.; Li, M..; Foo, C.E.; Yang, T.; Huang, D.M.; Yap, A.; Samudra, G.S.; Yeo, Y. Characterization and Physical Origin of Fast Vth Transient in NBTI of pMOSFETs with SiON Dielectric. In Proceedings of the 2006 International Electron Devices Meeting, San Francisco, CA, USA, 11–13 December 2006; pp. 1–4.
77. Islam, A.E.; Kufluoglu, H.; Varghese, D.; Mahapatra, S.; Alam, M.A. Recent Issues in Negative-Bias Temperature Instability: Initial Degradation, Field Dependence of Interface Trap Generation, Hole Trapping Effects, and Relaxation. *IEEE Trans. Electron Devices* **2007**, *54*, 2143–2154. [CrossRef]
78. Grasser, T.; Kaczer, B.; Goes, W.; Aichinger, T.; Hehenberger, P.; Nelhiebel, M. A Two-Stage Model for Negative Bias Temperature Instability. In Proceedings of the 2009 IEEE International Reliability Physics Symposium, Montreal, QC, Canada, 26–30 April 2009; pp. 33–44.
79. Campbell, J.P.; Lenahan, P.M.; Cochrane, C.J.; Krishnan, A.T.; Krishnan, S. Atomic-scale defects involved in the negative-bias temperature instability. *IEEE Trans. Device Mater. Reliab.* **2007**, *7*, 540–557. [CrossRef]
80. Grasser, T.; Reisinger, H.; Goes, W.; Aichinger, T.; Hehenberger, P.; Wagner, P.; Nelhiebel, M.; Franco, J.; Kaczer, B. Switching Oxide Traps as the Missing Link between Negative Bias Temperature Instability and Random Telegraph Noise. In Proceedings of the 2009 IEEE International Electron Devices Meeting (IEDM), Baltimore, MD, USA, 7–9 December 2009; pp. 729–732.
81. Weissman, M. 1/f noise and other slow, nonexponential kinetics in condensed matter. *Rev. Mod. Phys.* **1988**, *60*, 537–571. [CrossRef]
82. Fleetwood, D.M.; Xiong, H.D.; Lu, Z..; Nicklaw, C.J.; Felix, J.A.; Schrimpf, R.D.; Pantelides, S.T. Unified model of hole trapping, 1/f noise, and thermally stimulated current in MOS devices. *IEEE Trans. Nucl. Sci.* **2002**, *49*, 2674–2683. [CrossRef]
83. Kirton, M.; Uren, M. Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (1/f) noise. *Adv. Phys.* **1989**, *38*, 367–468. [CrossRef]
84. Henry, C.; Lang, D. Nonradiative Capture and Recombination by Multiphonon Emission in GaAs and GaP. *Phys. Rev. B* **1977**, *15*, 989–1016. [CrossRef]
85. Lelis, A.J.; Oldham, T.R. Time dependence of switching oxide traps. *IEEE Trans. Nucl. Sci.* **1994**, *41*, 1835–1843. [CrossRef]
86. Schanovsky, F. Atomistic Modeling in the Context of the Bias Temperature Instability. Ph.D. Thesis, TU Wien, Vienna, Austria, 2013.
87. Lenahan, P.M.; Conley, J.F. What can electron paramagnetic resonance tell us about the Si/SiO_2 system? *J. Vac. Sci. Technol. Microelectron. Nanometer Struct. Process. Meas. Phenom.* **1998**, *16*, 2134–2153. [CrossRef]

88. Lenahan, P.M.; Campbell, J.P.; Krishnan, A.T.; Krishnan, S. A Model for NBTI in Nitrided Oxide MOSFETs Which Does Not Involve Hydrogen or Diffusion. *IEEE Trans. Device Mater. Reliab.* **2011**, *11*, 219–226. [CrossRef]
89. de Nijs, J.M.M.; Druijf, K.G.; Afanas'ev, V.V.; van der Drift, E.; Balk, P. Hydrogen induced donor-type Si/SiO2 interface states. *Appl. Phys. Lett.* **1994**, *65*, 2428–2430. [CrossRef]
90. Blöchl, P.E.; Stathis, J.H. Aspects of defects in silica related to dielectric breakdown of gate oxides in MOSFETs. *Phys. Condens. Matter* **1999**, *273–274*, 1022–1026. [CrossRef]
91. Grasser, T.; Goes, W.; Wimmer, Y.; Schanovsky, F.; Rzepa, G.; Waltl, M.; Rott, K.; Reisinger, H.; Afanas'ev, V.; Stesmans, A.; et al. On the Microscopic Structure of Hole Traps in pMOSFETs. In Proceedings of the 2014 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2014.
92. El-Sayed, A.M.; Watkins, M.B.; Afanas'ev, V.V.; Shluger, A.L. Nature of intrinsic and extrinsic electron trapping in SiO_2. *Phys. Rev. B* **2014**, *89*. [CrossRef]
93. Grasser, T.; Waltl, M.; Goes, W.; Wimmer, Y.; El-Sayed, A.M.; Shluger, A.L.; Kaczer, B. On the volatility of oxide defects: Activation, deactivation, and transformation. In Proceedings of the 2015 IEEE International Reliability Physics Symposium, Monterey, CA, USA, 19–23 April 2015; pp. 5A.3.1–5A.3.8.
94. Waltl, M.; Rzepa, G.; Grill, A.; Gös, W.; Franco, J.; Kaczer, B.; Witters, L.; Mitard, J.; Horiguchi, N.; Grasser, T. Superior NBTI in High-k SiGe Transistors - Part II: Theory. *IEEE Trans. Electron Devices* **2017**, *64*, 2099–2105. [CrossRef]
95. O'Sullivan, B.J.; Ritzenthaler, R.; Dentoni Litta, E.; Simoen, E.; Machkaoutsan, V.; Fazan, P.; Ji, Y.; Kim, C.; Spessot, A.; Linten, D.; et al. Overview of Bias Temperature Instability in Scaled DRAM Logic for Memory Transistors. *IEEE Trans. Device Mater. Reliab.* **2020**, *20*, 258–268. [CrossRef]
96. Waltl, M. Separation of electron and hole trapping components of PBTI in SiON nMOS transistors. *Microelectron. Reliab.* **2020**, in press. [CrossRef]
97. Asenov, A.; Balasubramaniam, R.; Brown, A.R.; Davies, J.H. RTS amplitudes in decananometer MOSFETs: 3-D simulation study. *IEEE Trans. Electron Devices* **2003**, *50*, 839–845. [CrossRef]
98. Takeuchi, K.; Nagumo, T.; Yokogawa, S.; Imai, K.; Hayashi, Y. Single-charge-based modeling of transistor characteristics fluctuations based on statistical measurement of RTN amplitude. In Proceedings of the IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 15–17 June 2009; pp. 54–55.
99. Ghetti, A.; Monzio Compagnoni, C.; Spinelli, A.S.; Visconti, A. Comprehensive Analysis of Random Telegraph Noise Instability and Its Scaling in Deca–Nanometer Flash Memories. *IEEE Trans. Electron Devices* **2009**, *56*, 1746–1752. [CrossRef]
100. Franco, J.; Kaczer, B.; Roussel, P.J.; Mitard, J.; Cho, M.; Witters, L.; Grasser, T.; Groeseneken, G. SiGe Channel Technology: Superior Reliability Toward Ultrathin EOT Devices—Part I: NBTI. *IEEE Trans. Electron Devices* **2013**, *60*, 396–404. [CrossRef]
101. Franco, J.; Kaczer, B.; Toledano-Luque, M.; Roussel, P.J.; Kauerauf, T.; Mitard, J.; Witters, L.; Grasser, T.; Groeseneken, G. SiGe Channel Technology: Superior Reliability Toward Ultra-Thin EOT Devices—Part II: Time-Dependent Variability in Nanoscaled Devices and Other Reliability Issues. *IEEE Trans. Electron Devices* **2013**, *60*, 405–412. [CrossRef]

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Semi-Automated Extraction of the Distribution of Single Defects for nMOS Transistors

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Abstract: Miniaturization of metal-oxide-semiconductor field effect transistors (MOSFETs) is typically beneficial for their operating characteristics, such as switching speed and power consumption, but at the same time miniaturization also leads to increased variability among nominally identical devices. Adverse effects due to oxide traps in particular become a serious issue for device performance and reliability. While the average number of defects per device is lower for scaled devices, the impact of the oxide defects is significantly more pronounced than in large area transistors. This combination enables the investigation of charge transitions of single defects. In this study, we perform random telegraph noise (RTN) measurements on about 300 devices to statistically characterize oxide defects in a Si/SiO_2 technology. To extract the noise parameters from the measurements, we make use of the Canny edge detector. From the data, we obtain distributions of the step heights of defects, i.e., their impact on the threshold voltage of the devices. Detailed measurements of a subset of the defects further allow us to extract their vertical position in the oxide and their trap level using both analytical estimations and full numerical simulations. Contrary to published literature data, we observe a bimodal distribution of step heights, while the extracted distribution of trap levels agrees well with recent studies.

Keywords: MOSFET; reliability; random telegraph noise; oxide defects; SiO_2

1. Introduction

The amorphous SiO_2 used as the insulator material in silicon metal-oxide-semiconductor field effect transistors (MOSFETs) contains electrically active defects, often referred to as traps. These traps cause a number of effects detrimental to the operating characteristics and reliability of the devices [1,2]. The most prominent reliability issues in these devices related to charge trapping are the so called bias temperature instabilities (BTI) [3–5] and random telegraph noise (RTN) [6–8]. While BTI can be observed in large-area and nanoscale devices, RTN is mainly studied on scaled technologies.

With shrinking of the gate area of a MOSFET, the average number of defects present in the oxide decreases, see Figure 1. The smaller number of defects, however, does not lead to a reduction in threshold voltage shift or noise power, as one might intuitively expect. This is due to the larger influence defects in scaled devices have on the channel [9,10]. Below a certain gate area, single charge transitions can be observed as discrete steps in the drain current, enabling the characterization of RTN. While for large-area and nanoscale devices a similar average degradation of the threshold voltage can be observed, device-to-device variability is seriously affected by device scaling [11,12]. As a consequence, accurate characterization of nanoscale devices requires a higher number of samples than required for large area device studies. For this, we measure RTN on more than 300 scaled devices to evaluate the impact of defects on these devices. We further analyze part of the defects in more detail using an analytical approximation, to determine their distribution in depth and energy. Finally, we use

numerical defect simulation to reproduce some of the defects' charge trapping kinetics and compare the obtained distributions to the distributions from the analytical approximation and literature data.

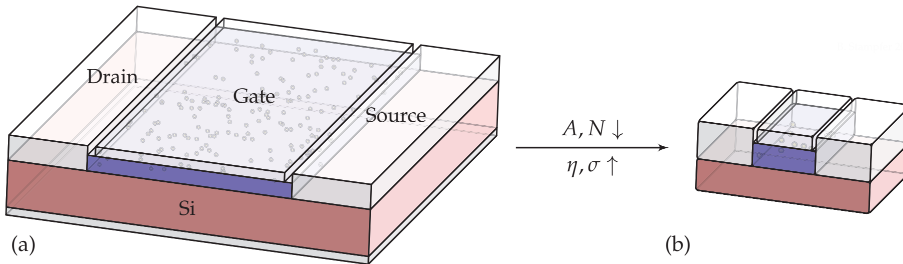

Figure 1. Illustration of oxide defects in (**a**) large- and (**b**) small area devices. As the gate area A is reduced, fewer defects N will be present in the device, but on average each defect will have a larger impact η on the overall degradation. This increases variability σ among nominally identical devices, but also allows characterization of single defects using methods such as random telegraph noise (RTN) analysis and time-dependent defect spectroscopy (TDDS).

2. Materials and Methods

In the following, the devices used in this work and the measurements carried out are discussed. Afterwards, an efficient method to analyze the recorded data is given. Finally, an analytical approximation for the trap level and the trap position is discussed. Using the proposed methodology the trap bands can be extracted from the measurement data. While the focus of this study is on Si/SiO_2 devices, the methodology is possible on other technologies, given that small devices are available which are also stable enough to record RTN in a reproducible fashion [13–15].

2.1. Devices and Measurements

The devices investigated in this study are planar Si/SiO_2 devices with an effective gate area of $A \approx 0.15\,\mu m^2$. For all measurements, we use a custom defect probing instrument (DPI) [16] which is configured with three voltage sources for the gate, drain, and bulk terminals of the transistor and a low-noise trans-impedance amplifier with switchable amplification, in combination with a sampling input for measuring drain-source current I_{DS}, connected to the source of the device. The devices are contacted using a Cascade/FormFactor PA300 semi-automatic wafer prober (FormFactor, Inc., Livermore, CA, USA), which is fully shielded. Electrical connections between the prober and the measurement instrument are made with double shielded TRIAX cables (Keithley Instruments, Solon, OH, USA) to further reduce spurious noise.

To obtain statistics about the defects active in the devices, automated measurements are performed on around 300 devices. In our measurement scheme, the transfer characteristic is recorded for each device, followed by RTN measurements. The initial $I_D(V_G)$ curve is used to verify proper operation of the tested device, to determine at which voltages the RTN signals are measured, and to map the recorded $I_D(t)$ RTN data to $\Delta V_{th}(t)$. In order to minimize stress to the device prior the RTN measurement, the initial $I_D(V_G)$ characteristics are recorded within a narrow gate bias window; see Figure 2.

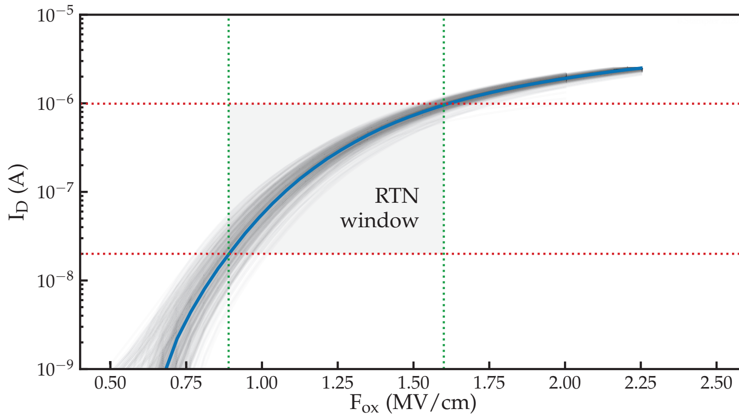

Figure 2. Transfer characteristics measured on approximately 300 nominally identical devices, with the average characteristic indicated in blue. The bias range (green) and current range (red) used for RTN measurements in this work is indicated using dotted lines.

The RTN traces are recorded at the gate voltages corresponding to 20, 50, 100, 300, and 1000 nA for each device. These values are selected to achieve maximum current resolution for the measurements ranges available. The drain-source voltage used for both the $I_D(V_G)$and RTN measurements is -100 mV.

For each gate bias point, one long and five short RTN traces are recorded. The long traces feature a sampling time of $T_s = 10$ ms and a total recording time of $t_r = 1$ ks, while the short traces are sampled with $T_s = 100$ µs for $t_r = 10$ s. This allows us to characterize defects with a wider range of transition times, while keeping the number of samples per trace manageable [17]. An example of a fast-sampled RTN trace recorded is shown in Figure 3. The trace was mapped from I_D(t) to ΔV_{th}(t). For this, each I_D value in the trace is replaced with the corresponding V_G from the initial $I_D(V_G)$, and finally subtracted from the applied V_G [18].

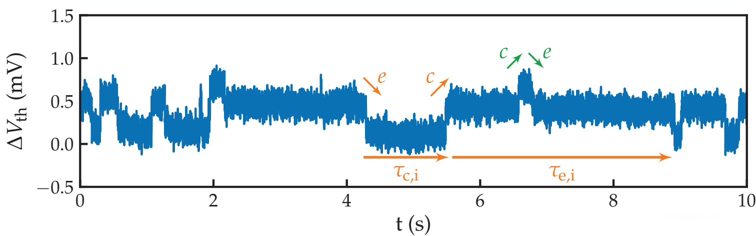

Figure 3. Random telegraph noise traces recorded on a device with $T_s = 100$ µs. Two active defects with similar step heights are clearly visible. The arrows show steps and dwelling times linked to charge capture (c) and charge emission (e) events of the defects.

To characterize individual defects in detail, additional RTN measurements are performed on selected devices, with measurement parameters tailored to the defects under investigation. All measurements are performed at 30 °C unless indicated otherwise.

2.2. Noise Parameter Extraction

To obtain the average step heights η as well as the charge capture and charge emission times $\tau_{c,e}$ of the defect signals comprising the recorded traces, a 1D variant of the Canny edge detector [19,20] is first applied on the ΔV_{th} data. This method is chosen because (i) there are only few defects per device

on average, (ii) the signal-to-noise ratio is reasonably high, and (iii) the method requires little manual interaction. Other methods which could be used for this step include time-lag methods [21,22] or methods based on hidden Markov models [23,24].

To determine the positions of the steps, the ΔV_{th}(t) data is convoluted with the first derivative of a Gaussian pulse with a chosen standard deviation σ_{g}, truncated in time to $\pm L = 5\sigma_{\text{g}}$:

$$h(t) = \Delta V_{\text{th}}(t) * g(t) = \int_{-L}^{L} \Delta V_{\text{th}}(t-\delta) g(\delta) d\delta \quad (1)$$

The resulting signal is then compared to a threshold value, which is chosen to suppress spurious responses. Local maxima in the signal above this threshold level then give the locations of steps t_i in the original trace. With the positions of the steps, their height η_i can be determined from the original signal, resulting in a list of steps (t_i, η_i) as shown in Figure 4. From the list of steps, the average step heights and transition times of the defect responses can be determined, given the defects are distinguishable in step height. If this is not the case, i.e., multiple defects with similar step heights contribute to a trace, this may lead to erroneous results. This is indicated in the data by successive positive or negative steps and a non-exponential distribution of the calculated transition times.

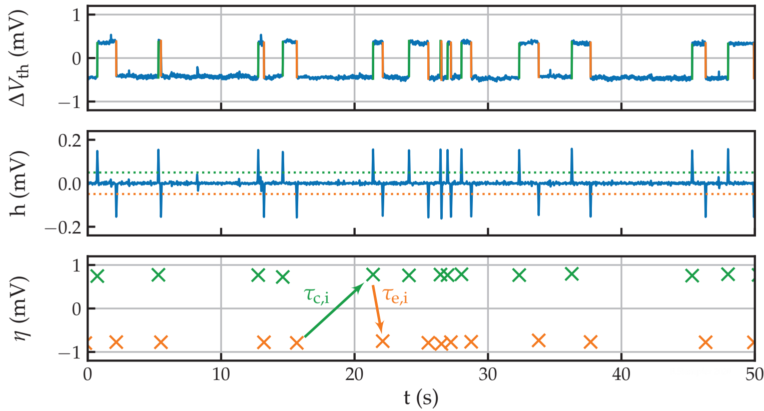

Figure 4. Noise parameter extraction using the Canny algorithm. To find steps in a ΔV_{th} trace, it is convoluted with the first derivative of a Gaussian pulse. This yields a signal h, as shown in the center panel, with peaks at the positions of the steps. Thresholding is then applied to h to suppress noise. Finally, the positions of the steps are obtained from the positions of the local maxima in h. The height of the steps may be obtained either from the peaks in h or from the original trace. The result is a list of steps (t_i, η_i) from which, ideally, the average step height η, capture time τ_c, and emission time τ_e for each defect can be extracted.

2.3. Defect Parameter Estimation

From defects which are close to the Fermi level at measurement conditions, spatial and energetic positions can be estimated from their capture and emission times measured at a number of voltages [6,25,26]. The central assumption for this estimation is that a defect at the Fermi level $E_{\text{t}} = E_{\text{f}}$ has an occupancy of 50%, i.e., $\tau_c = \tau_e$. It is further assumed that the rate equations for charge capture from the channel, and charge emission to the channel can be written in the form:

$$k_{\text{c,e}} = k_{0\text{c,e}} \exp\left(-\frac{\mathcal{E}_{\text{c,e}}}{k_{\text{B}}T}\right), \quad (2)$$

with the capture and emission rates $k_{c,e} = 1/\tau_{c,e}$, prefactors $k_{0c,e}$, energy barriers for capture and emission $\mathcal{E}_{c,e}$, the Boltzmann constant k_B, and the device temperature T. From the logarithm of Equation (2):

$$\ln k_{c,e} = \ln k_{0c,e} - \frac{\mathcal{E}_{c,e}}{k_B T} \tag{3}$$

its dependence on the gate bias is expressed:

$$\frac{\partial \ln k_{c,e}}{\partial V_G} = \frac{\partial \ln k_{0c,e}}{\partial V_G} - \frac{1}{k_B T}\frac{\partial \mathcal{E}_{c,e}}{\partial V_G}. \tag{4}$$

Assuming the bias dependence of the prefactor can be neglected, and subtracting Equation (4) for capture and emission yields

$$\frac{\partial \ln k_c/k_e}{\partial V_G} = -\frac{1}{k_B T}\frac{\partial(\mathcal{E}_c - \mathcal{E}_e)}{\partial V_G} = -\frac{1}{k_B T}\frac{\partial E_t}{\partial V_G}. \tag{5}$$

Here, $\partial(\mathcal{E}_c - \mathcal{E}_e)$ is replaced by the change in trap level ∂E_t. This is possible due to

$$\mathcal{E}_c - \mathcal{E}_e = (E_{max} - E_r) - (E_{max} - E_t) = E_t - E_r \tag{6}$$

where the bias independent reservoir energy E_r and the peak of the energetic barrier E_{max} [27]. Note that this makes no assumptions on the shape of the energetic barriers between the two states of the system. Assuming the device is operating in inversion and a homogeneous oxide field is applied, the change in effective trap energy with gate voltage can be expressed with the position of the defect in the oxide as

$$\frac{\partial E_t}{\partial V_G} = -q\frac{d}{t_{ox}}. \tag{7}$$

Equations (5) and (7) yield the relative position of the defect in the oxide

$$\frac{d}{t_{ox}} = -\frac{k_B T}{q}\left(\frac{\partial \ln \tau_c/\tau_e}{\partial V_G}\right), \tag{8}$$

written with $\tau_{c,e} = 1/k_{c,e}$. Integrating Equation (7) gives the thermodynamic trap level of the defect:

$$E_t = -q\frac{d}{t_{ox}}V_G + C. \tag{9}$$

At the gate voltage $V_{G,i}$, where the measured capture and emission times intersect, the trap level is equal to the channel Fermi level at this voltage $E_t = E_{f,i}$.:

$$E_{f,i} = -q\frac{d}{t_{ox}}(V_{G,i}) + C. \tag{10}$$

Finally, substituting C from Equation (10) in Equation (9) and evaluating at $V_G = -V_{FB} - V_S$ yields the trap level at zero field

$$E_{t,0} = E_{f,i} + q\frac{d}{t_{ox}}(V_{G,i} - \phi_s - V_{FB}), \tag{11}$$

with the oxide electric field F_{ox}, the surface potential ϕ_s and flatband voltage V_{FB}.

3. Results

Based on the methodology presented above, the recorded RTN traces are analyzed. The extracted noise parameters are used to find the distributions of step height, vertical defect position and energy level.

3.1. Threshold Voltage Shift and Number of Defects

A plot showing the complimentary cumulative density function (1-CDF, or CCDF) of the step heights extracted from the measurement data of approximately 300 devices is shown in Figure 5. For a single defect distribution, an exponential distribution of step heights, i.e., a straight line in the CCDF plot, is expected [28]. In this case, however, the measurements seems to comprise two separate distributions of defects. As a consequence, defects with responses between 3 mV to 5 mV seem slightly more common than expected.

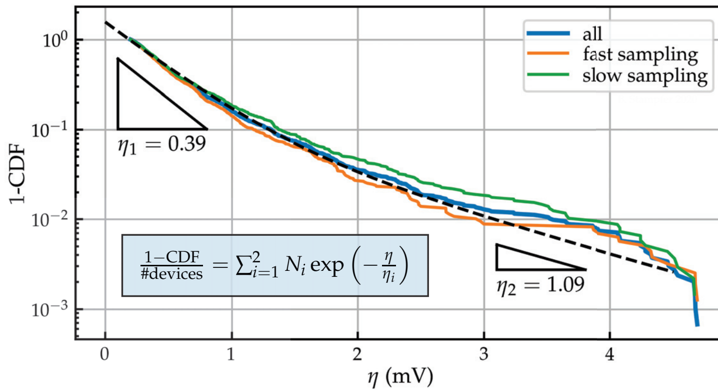

Figure 5. Complementary cumulative density function (1-CDF) of the step heights η extracted from our measurements, shown for both the slow and the fast sampled data. The distribution seems to be bimodal, composed of a defect distribution with a smaller average impact η_1 and a distribution with a larger impact η_2.

3.2. Energy and Position

Examples of defects characterized in more detail are shown in Figure 6. Using the method described in Section 2.3, trap levels and positions of defects are estimated for around 100 defects.

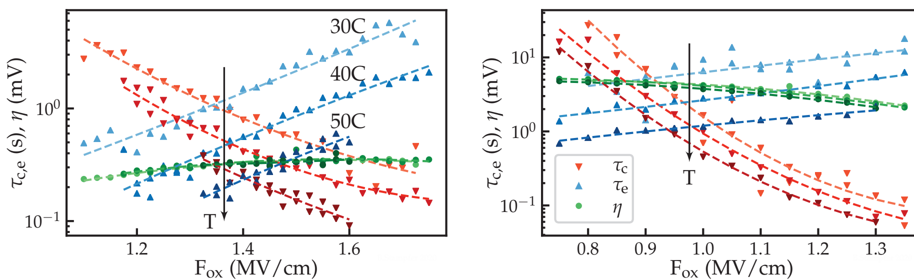

Figure 6. Two defects characterized in detail. From the intersection points and the steepness of the charge capture and emission times, the positions and the trap levels of the defects can be estimated.

The results are shown in histograms for distance and trap level in Figure 7. Most of the defects which have been characterized are found between 0.5 t_{ox} and 0.8 t_{ox}, which seems to be the depth at which the electron defect band corresponds with the Fermi level at the measurement bias. This places the trap level of the extracted defects around 0.4 eV above the Fermi level, which according to our numerical device simulations is close to the Si conduction band.

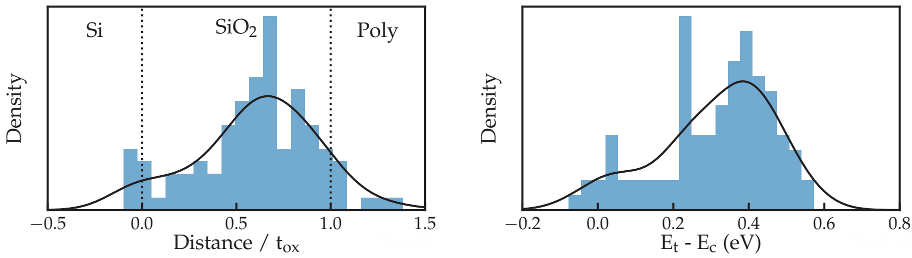

Figure 7. Distributions of positions and trap levels extracted using Equation (8) and Equation (11). Note that the measured distribution in position should not be interpreted as the complete distribution of defects in the device. It is rather a result of the energetic distribution of the defects in conjunction with the characterization window, which is diagonal in energy and distance, given by the Fermi level at measurement conditions.

As can further be seen in Figure 7, the estimation given by Equation (8) suggests some defects to be located outside the oxide. This is due to a number of shortcomings in this methodology:

(i) The estimation only accounts for interaction with the channel, defects interacting primarily with the gate might have inverted capture and emission time behavior which results in a negative distance.
(ii) The prefactor which is assumed as constant in the estimation does change with the logarithm of the channel carrier density. This leads to some overestimation of the distance.
(iii) The estimation is based on the values and first derivatives of the capture and emission times at the intersection point. Measurements which do not show $\tau_c = \tau_e$ within the measurement window need to be extrapolated, which leads to inaccuracies.
(iv) Some defects may not be adequately described using a two state model [29].

In Figure 8, the extracted defects are shown in a simulated band diagram. Furthermore, defect bands which were obtained from positive bias temperature instability (PBTI) and negative bias temperature instability (NBTI) experiments on n- and pMOS transistors, respectively, are indicated at energy values taken from [30].

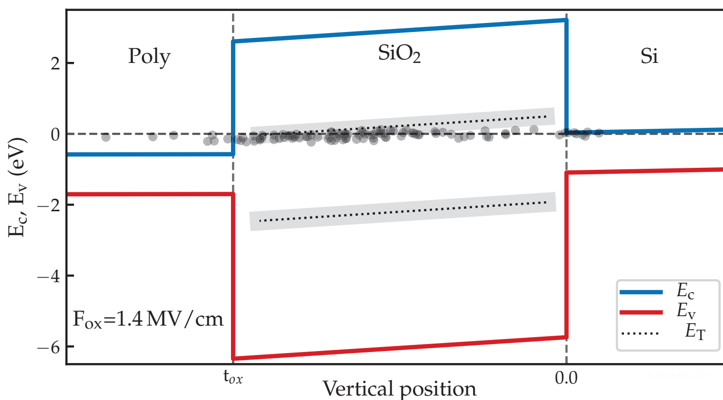

Figure 8. Simulated band diagram showing the locations of defects extracted using Equation (8) and Equation (11). In addition, defect bands as given in [30] are shown in comparison. Notice how some defects appear located outside of the SiO_2 layer. This shows the shortcomings of the estimation used. The estimation does not account for defect interaction with the gate, which often results in negative d/t_{ox} and it generally overestimates the distance of the defects due to the neglected prefactor.

For the electron trap band this is around 0.5 eV above the conduction band, which is around 0.1 eV higher than the values we extract from the measured defects. This might be due to defects closer to the gate interacting primarily with the gate instead of the channel, effectively limiting our measurement range in energy. A number of defects show up with distances around zero, i.e., with very small bias dependencies of their τ_c/τ_e ratios. They may be located close to either the Si/SiO_2 interface or to the SiO_2/poly interface.

3.3. Simulation

To obtain more accurate data, the capture and emission time behavior for a subset of the defects characterized using the estimation formulas is replicated using technology computer aided design (TCAD) simulation [31]. For the simulations, an effective two-state nonradiative multi phonon (NMP) model is used. Only those measurements are used where the intersection point lies within the measurement range. This removes the peak close to the interface observed in Figures 7 and 8. The distributions for the resulting distances and energies are shown in Figure 9.

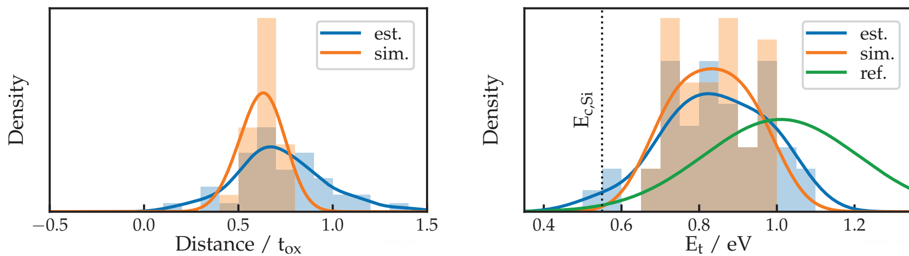

Figure 9. Distributions of positions and trap levels from technology computer aided design (TCAD) simulations compared to the estimations made for the same defects. Energies are referenced from Si-midgap, with $E_{f,i}$ taken from the simulation. The electron defect band at $E_t = 1.01$ eV from [30] is shown for comparison. The defects we observe are distributed mainly in the lower half of this band.

It can be seen that the simulation results are in good agreement with the data obtained from the estimations. The average depth assigned to the measured defects is slightly lower in the simulation and all defects are confined to the oxide. It can be further observed that the average of the energy distribution is slightly lower compared to the estimation. Compared to the electron defect band at $E_t = 1.01\,\text{eV} \pm 0.218\,\text{eV}$ from [30], which was obtained from PBTI experiments on nMOS transistors, we extract only defects in the lower half of this band, as only those can contribute to the measured RTN.

4. Discussion

The distributions of step heights in Si/SiO_2 devices which have been reported in literature can commonly be explained using a single exponential distribution. However, in the underlying work we clearly observe a bimodal distribution of the measured step heights, which one would not expect for Si/SiO_2 devices. Bimodal distributions are commonly observed for PBTI only in high-k devices, where they are thought to originate from traps in both the bulk high-k layer and the interstitial layer [32–34]. A simple approximation of the threshold voltage shift expected is possible using the charge sheet approximation, which gives values below 0.2 mV for these devices. This agrees within the limits of this approximation to the smaller η_1 observed. However, the origin of the larger η_2 in this technology needs further investigation.

In this work, we use an analytical approximation to extract the trap levels and spatial distribution from a large set of RTN measurements and compare the results to TCAD simulations. The results for the energetic and spatial distributions show good agreement between the estimated and the simulated

parameters, considering the approximations made in the estimation. The energetic distribution of the extracted defects covers the lower half of an electron defect band obtained from simulations reported recently. Due to the limited scanning range of the RTN measurements performed, no defects could be measured in the upper half of this band. A possibility to extend the energetic range of the investigations in a future work could be the combination of the obtained RTN data with data obtained from TDDS measurements.

Author Contributions: Conceptualization, all; methodology, B.S. and F.S.; software, B.S. and M.W.; validation, B.S., M.W. and T.G.; formal analysis, B.S.; investigation, B.S. and M.W.; resources, M.W. and T.G.; data curation, B.S. and M.W.; writing–original draft preparation, B.S.; writing–review and editing, all; visualization, B.S.; supervision, M.W. and T.G.; project administration, T.G.; funding acquisition, T.G. All authors have read and agreed to the published version of the manuscript.

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References

1. Lenahan, P. Atomic Scale Defects Involved in MOS Reliability Problems. *Microelectron. Eng.* **2003**, *69*, 173–181. [CrossRef]
2. Rzepa, G.; Waltl, M.; Goes, W.; Kaczer, B.; Grasser, T. Microscopic Oxide Defects Causing BTI, RTN, and SILC on High-k FinFETs. In Proceedings of the 2015 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Washington, DC, USA, 9–11 September 2015; pp. 144–147.
3. Denais, M.; Huard, V.; Parthasarathy, C.; Ribes, G.; Perrier, F.; Revil, N.; Bravaix, A. Interface Trap Generation and Hole Trapping under NBTI and PBTI in Advanced CMOS Technology with a 2-nm Gate Oxide. *IEEE Trans. Devices Mater. Reliab.* **2004**, *4*, 715–722. [CrossRef]
4. Grasser, T.; Kaczer, B.; Gös, W.; Reisinger, H.; Aichinger, T.; Hehenberger, P.; Wagner, P.J.; Franco, J.; Toledano-Luque, M.; Nelhiebel, M. The Paradigm Shift in Understanding the Bias Temperature Instability: From Reaction-Diffusion to Switching Oxide Traps. *IEEE Trans. Electron Devices* **2011**, *58*, 3652–3666. [CrossRef]
5. Stathis, J.H.; Mahapatra, S.; Grasser, T. Controversial Issues in Negative Bias Temperature Instability. *Microelectron. Reliab.* **2018**, *81*, 244–251. [CrossRef]
6. Ralls, K.S.; Skocpol, W.J.; Jackel, L.D.; Howard, R.E.; Fetter, L.A.; Epworth, R.W.; Tennant, D.M. Discrete Resistance Switching in Submicrometer Silicon Inversion Layers: Individual Interface Traps and Low-Frequency ($\frac{1}{f}$) Noise. *Phys. Rev. Lett.* **1984**, *52*, 228–231. doi:10.1103/PhysRevLett.52.228. [CrossRef]
7. Uren, M.; Day, D.; Kirton, M. 1/f and Random Telegraph Noise in Silicon Metal-Oxide-Semiconductor Field-effect Transistors. *Appl. Phys. Lett.* **1985**, *47*, 1195–1197. [CrossRef]
8. Ghetti, A.; Compagnoni, C.; Spinelli, A.; Visconti, A. Comprehensive Analysis of Random Telegraph Noise Instability and Its Scaling in Deca–Nanometer Flash Memories. *IEEE Trans. Electron Devices* **2009**, *56*, 1746–1752. [CrossRef]
9. Fukuda, K.; Shimizu, Y.; Amemiya, K.; Kamoshida, M.; Hu, C. Random Telegraph Noise in Flash Memories-Model and Technology Scaling. In Proceedings of the 2007 IEEE International Electron Devices Meeting, Washington, DC, USA, 10–12 December 2007; IEEE: Piscataway, NJ, USA, 2007; pp. 169–172.
10. Kükner, H.; Weckx, P.; Franco, J.; Toledano-Luque, M.; Cho, M.; Kaczer, B.; Raghavan, P.; Jang, D.; Miyaguchi, K.; Bardon, M.G.; et al. Scaling of BTI Reliability in Presence of Time-Zero Variability. In Proceedings of the 2014 IEEE International Reliability Physics Symposium, Waikoloa, HI, USA, 1–5 June 2014; IEEE: Piscataway, NJ, USA, 2014; p. CA-5.
11. Kaczer, B.; Grasser, T.; Roussel, P.J.; Franco, J.; Degraeve, R.; Ragnarsson, L.; Simoen, E.; Groeseneken, G.; Reisinger, H. Origin of NBTI Variability in Deeply Scaled pFETs. In Proceedings of the 2010 IEEE International Reliability Physics Symposium, Anaheim, CA, USA, 2–6 May 2010; pp. 26–32. doi:10.1109/IRPS.2010.5488856. [CrossRef]
12. Toledano-Luque, M.; Kaczer, B.; Roussel, P.; Cho, M.; Grasser, T.; Groeseneken, G. Temperature Dependence of the Emission and Capture Times of SiON Individual Traps after Positive Bias Temperature Stress. *J. Vac. Sci. Technol. B* **2011**, *29*, 01AA04. [CrossRef]

13. Park, S.; Lee, S.; Kang, Y.; Park, B.G.; Lee, J.H.; Lee, J.; Jin, G.; Shin, H. Extracting Accurate Position and Energy Level of Oxide Trap Generating Random Telegraph Noise (RTN) in Recessed Channel MOSFET's. In Proceedings of the 40th European Solid-State Device Research Conference (ESSDERC), Seville, Spain, 14–16 September 2010; pp. 337–340.
14. Grill, A.; Stampfer, B.; Waltl, M.; Im, K.S.; Lee, J.H.; Ostermaier, C.; Ceric, H.; Grasser, T. Characterization and Modeling of Single Defects in GaN/AlGaN fin-MIS-HEMTs. In Proceedings of the 2017 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 2–6 April 2017; p. 3B–5.
15. Stampfer, B.; Zhang, F.; Illarionov, Y.Y.; Knobloch, T.; Wu, P.; Waltl, M.; Grill, A.; Appenzeller, J.; Grasser, T. Characterization of Single Defects in Ultrascaled MoS2 Field-Effect Transistors. *ACS Nano* **2018**, *12*, 5368–5375, doi:10.1021/acsnano.8b00268. [CrossRef]
16. Waltl, M. Ultra-Low Noise Defect Probing Instrument for Defect Spectroscopy of MOS Transistors. *Trans. Elec. Dev.* **2020**, submitted. [CrossRef]
17. Kapila, G.; Reddy, V. Impact of Sampling Rate on RTN Time Constant Extraction and its Implications on Bias Dependence and Trap Spectroscopy. *IEEE Trans. Device Mater. Reliab.* **2014**, *14*, 616–622.
18. Grasser, T.; Wagner, P.J.; Hehenberger, P.; Goes, W.; Kaczer, B. A Rigorous Study of Measurement Techniques for Negative Bias Temperature Instability. *IEEE Trans. Device Mater. Reliab.* **2008**, *8*, 526–535. [CrossRef]
19. Canny, J. A Computational Approach to Edge Detection. In *Readings in Computer Vision*; Elsevier: Amsterdam, The Netherlands, 1987; pp. 184–203.
20. McIlhagga, W. The Canny Edge Detector Revisited. *Int. J. Comput. Vis.* **2011**, *91*, 251–261. [CrossRef]
21. Martin-Martinez, J.; Diaz, J.; Rodriguez, R.; Nafria, M.; Aymerich, X. New Weighted Time Lag Method for the Analysis of Random Telegraph Signals. *IEEE Electron Device Lett.* **2014**, *35*, 479–481. doi:10.1109/LED.2014.2304673. [CrossRef]
22. Maestro, M.; Diaz, J.; Crespo-Yepes, A.; Gonzalez, M.; Martin-Martinez, J.; Rodriguez, R.; Nafria, M.; Campabadal, F.; Aymerich, X. New High Resolution Random Telegraph Noise (RTN) Characterization Method for Resistive RAM. *Solid-State Electron.* **2016**, *115*, 140–145. [CrossRef]
23. Ghahramani, Z.; Jordan, M.I. Factorial Hidden Markov Models. In *Advances in Neural Information Processing Systems 9, Proceedings of the 1996 Conference*; MIT Press: Cambridge, MA, USA, 1996; pp. 472–478.
24. Frank, D.J.; Miki, H. Analysis of Oxide Traps in Nanoscale MOSFETs Using Random Telegraph Noise. In *Bias Temperature Instability for Devices and Circuits*; Springer: Berlin, Germany, 2014; pp. 111–134.
25. Kirton, M.; Uren, M. Noise in Solid-State Microstructures: A New Perspective on Individual Defects, Interface States and Low-Frequency (1/f) Noise. *Adv. Phys.* **1989**, *38*, 367–468. [CrossRef]
26. Nagumo, T.; Takeuchi, K.; Hase, T.; Hayashi, Y. Statistical Characterization of Trap Position, Energy, Amplitude and Time Constants by RTN Measurement of Multiple Individual Traps. In Proceedings of the 2010 International Electron Devices Meeting, San Francisco, CA, USA, 6–8 December 2010; IEEE: Piscataway, NJ, USA, 2010; pp. 28–30.
27. Goes, W.; Wimmer, Y.; El-Sayed, A.M.; Rzepa, G.; Jech, M.; Shluger, A.; Grasser, T. Identification of Oxide Defects in Semiconductor Devices: A Systematic Approach Linking DFT to Rate Equations and Experimental Evidence. *Microelectron. Reliab.* **2018**, *87*, 286–320. [CrossRef]
28. Kaczer, B.; Roussel, P.; Grasser, T.; Groeseneken, G. Statistics of Multiple Trapped Charges in the Gate Oxide of Deeply Scaled MOSFET Devices-Application to NBTI. *IEEE Electron Device Lett.* **2010**, *31*, 411–413. [CrossRef]
29. Grasser, T. Stochastic Charge Trapping in Oxides: From Random Telegraph Noise to Bias Temperature Instabilities. *Microelectron. Reliab.* **2012**, *52*, 39–70. [CrossRef]
30. Rzepa, G.; Franco, J.; O'Sullivan, B.; Subirats, A.; Simicic, M.; Hellings, G.; Weckx, P.; Jech, M.; Knobloch, T.; Waltl, M.; et al. Comphy—A Compact-Physics Framework for Unified Modeling of BTI. *Microelectron. Reliab.* **2018**, *85*, 49–65. [CrossRef]
31. Global TCAD Solutions. GTS Framework. Available online: http://www.globaltcad.com/framework (accessed on 17 April 2020).
32. Weckx, P.; Kaczer, B.; Chen, C.; Franco, J.; Bury, E.; Chanda, K.; Watt, J.; Roussel, P.J.; Catthoor, F.; Groeseneken, G. Characterization of Time-dependent Variability using 32k Transistor Arrays in an Advanced HK/MG Technology. In Proceedings of the 2015 IEEE International Reliability Physics Symposium, Monterey, CA, USA, 19–23 April 2015; pp. 3B.1.1–3B.1.6. doi:10.1109/IRPS.2015.7112702. [CrossRef]

33. Oshima, A.; Komawaki, T.; Kobayashi, K.; Kishida, R.; Weckx, P.; Kaczer, B.; Matsumoto, T.; Onodera, H. Physical-based RTN Modeling of Ring Oscillators in 40-nm SiON and 28-nm HKMG by Bimodal Defect-Centric Behaviors. In Proceedings of the 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Nuremberg, Germany, 6–8 September 2016; IEEE: Piscataway, NJ, USA, 2016; pp. 327–330.
34. Waltl, M.; Rzepa, G.; Grill, A.; Goes, W.; Franco, J.; Kaczer, B.; Witters, L.; Mitard, J.; Horiguchi, N.; Grasser, T. Superior NBTI in High-*k* SiGe Transistors - Part I: Experimental. *IEEE Trans. Electron Devices* **2017**, *64*, 2092–2098. doi:10.1109/TED.2017.2686086. [CrossRef]

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Nanoscale MOSFET as a Potential Room-Temperature Quantum Current Source

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Abstract: Nanoscale metal-oxide-semiconductor field-effect-transistors (MOSFETs) with only one defect at the interface can potentially become a single electron turnstile linking frequency and electronic charge to realize the elusive quantized current source. Charge pumping is often described as a process that 'pumps' one charge per driving period per defect. The precision needed to utilize this charge pumping mechanism as a quantized current source requires a rigorous demonstration of the basic charge pumping mechanism. Here we present experimental results on a single-defect MOSFET that shows that the one charge pumped per cycle mechanism is valid. This validity is also discussed through a variety of physical arguments that enrich the current understanding of charge pumping. The known sources of errors as well as potential sources of error are also discussed. The precision of such a process is sufficient to encourage further exploration of charge pumping based on quantum current sources.

Keywords: nanoscale; mosfet; quantum current

1. Introduction

Accurate electrical measurements are the very foundation of modern science and the accurate measurement of electric current is particularly challenging due to the lack of a convenient standard. As part of the effort to bring an end to the use of physical objects to define measurement units, the 26th General Conference on Weights and Measures redefined the ampere as the flow of $1/(1.602176634 \times 10^{-19})$ elementary charges per second [1], linking electric current to the fundamental unit of charge. Hailed as a landmark moment in scientific progress, this redefinition using a natural constant brings a new urgency to the development of a current source that adheres to such a definition. This is advantageous not only as a practical calibration standard but also to complete the quantum metrology triangle (QMT) for checking the consistency of fundamental constants [2].

Efforts to control the serial flow of electrons to define current have been ongoing for three decades, starting with the electron turnstile operating at millikelvin temperature [3–7]. These turnstile measurements realize current, I, such that $I = ef$ where e is the elementary electronic charge and f is the control frequency. Such a source will meet the modern definition of current exactly. While there have been demonstrations meeting the metrology precision needs [7], the current level is limited to the picoampere range, which is too low for practical purposes. Various alternatives have been explored to increase the current level [8–14], however, the increased current level costs accuracy. While some of these approaches have shown theoretical pathways to achieve accuracy at higher current levels [15], the measurements require cryogenic operation temperature and high magnetic fields [16]. If realized they will not be practical current standards deployable outside of a highly specialized laboratory.

2. Materials and Methods

All the single electron transistors (SET) or electron turnstiles rely on a Coulomb blockade process. Artificially fabricated quantum dots are not generally small enough and therefore cryogenic operation is a necessity. Note that a 2014 review of quantum current sources picked the tunable barrier pump as the leading candidate for a primary current standard because it requires "only" the pumped helium-3 cryostat instead of a dilution-refrigerator [17]. For the proposed quantum current source in this work, the quantum dot is replaced with a broken bond, and instead of a Coulomb blockade, the Pauli's exclusion principle is relied upon to enforce the quantized flow of electrons.

Production quality nanoscale metal-oxide-semiconductor field-effect-transistors (MOSFETs) are small enough that the interface between the gate dielectric and the channel can have only a few defects or no defect at all. MOSFETs with only one interface defect can be down selected from arrays of billions of MOSFETs to generate a statistically relevant population of single defect devices suitable for parallel charge pumping to achieve an accurate quantized current source at relevant current levels.

The well-known charge-pumping (CP) process [18] can potentially meet this quantized current source need as it supposes to shuttle one charge from the source and drain of the MOSFET to the substrate per interface defect per charge-pumping cycle. This interpretation of CP has been widely accepted [19] but never fully demonstrated at the single defect level. A few reports in the literature [20–24] claimed to have observed one charge per cycle per defect, but there is always more than one charge per cycle in all these reports and the precision has been poor, until now.

Commercial n-channel MOSFETs with 50 nm effective channel length and 100 nm channel width were measured using the charge-pumping technique described in [18] (switching between strong accumulation and strong inversion) (Figure 1). The gate oxide is 1.6-nm-thick SiON. The square wave gate voltage switched from −1.3 V to +1.25 V, satisfying the strong accumulation and strong inversion conditions while not completely overwhelming the measurement with gate leakage current. The 0.1 V source and drain bias is the experimentally determined lowest net-zero leakage point. Many devices were measured and devices with 0, 1, 2, and 3 (and more) defects were found and easily identified by the quantized nature of the measured current level. This is consistent with the expected interface defect density ($10^{10}/cm^2$) in commercial MOSFETs. Devices with only one defect provide the most unambiguous proof and are the focus of the following discussion.

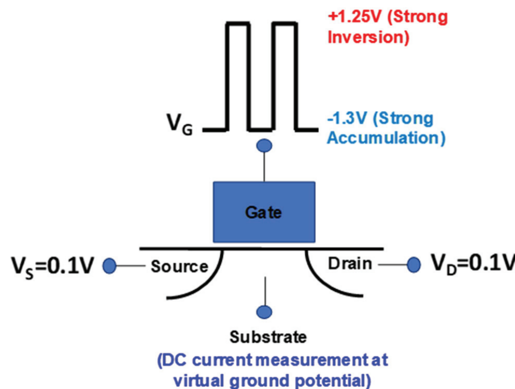

Figure 1. MOS charge-pumping measurement arrangement. Square wave is applied to the gate to switch the channel between strong accumulation and strong inversion. Source and drain are set to 0.1 V. Charge-pumping current is measured from the substrate as DC using a current amplifier with virtual ground input.

3. Results

Figure 2 shows the measured charge-pumping current as a function of frequency (100 kHz to 40 MHz) with three different gate square wave rise and fall times, on the same transistor. The noise floor of the measurement set up is 10 fA root-mean-square. Since each data point is the average of 800 measurements, the uncertainty of the measured current is on the order of 0.3 fA. The accuracy of the frequency has not been checked, however. The frequency response is clearly a linear function that satisfies $I = nef$ with ne the slope of the line in the unit of Coulombs per cycle. There are two lines for each rise/fall time. One is the raw (open diamond) data, and the other is gate leakage current corrected (solid circle) data.

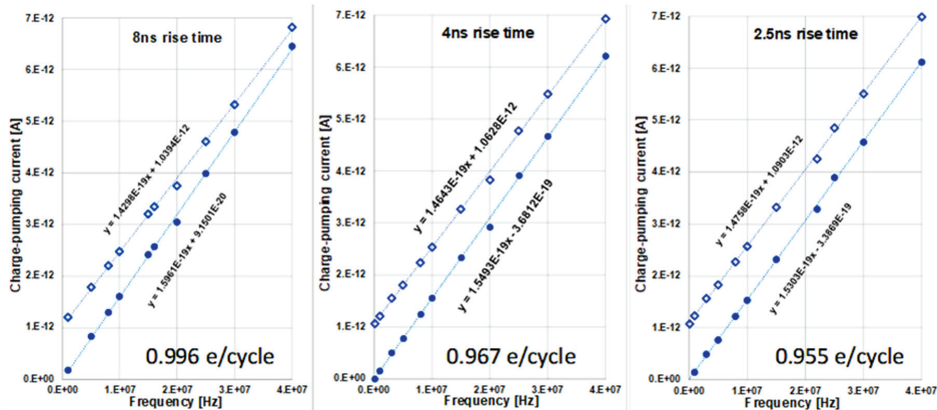

Figure 2. Measured and leakage corrected charge-pumping current as a function of frequency and their corresponding least square fits for three different rise/fall times. The charge per cycle at the bottom is extracted from the slope of the leakage corrected least square fit line, dividing by 1.6022×10^{-19} Coulomb.

To perform the gate leakage correction, we begin with the knowledge that charge-pumping current at zero frequency should be zero. Thus, the measured net current at zero frequency is entirely due to gate leakage. Since gate leakage current is an exponential function of gate voltage, gate leakage primarily occurs during the strong accumulation/inversion portions of the gate waveform and is small during the rising and falling edges of the gate waveform. For fixed rising/falling edges, increasing the frequency of the gate waveform decreases the time spent in strong accumulation/inversion and decreases the effective gate leakage current [25]. A common problem in the charge-pumping experiment is that when the frequency is too low, the measured current is dominated by leakage current and noise, providing little information of value. Thus, most experiments start at a moderate frequency, which in our case is 100 kHz. As seen in Figure 2, this frequency is low enough that in the linear plot it is very close to the zero-frequency point. This leads us to approximate the measured current at 100 kHz as pure leakage current L_{leak}. The frequency-dependent gate leakage can be calculated (assuming an ideal trapezoidal waveform) from the known rise/fall time t_r. The method is as follows: At each frequency f, the period is $\tau = 1/f$. Subtracting the rise and fall time from this time period results in the time period during which gate leakage occurs. Thus, the leakage contribution to the measured current, A, decreases with increasing frequency by a fraction of $R = 2t_r/\tau$. The corrected charge-pumping current, for each frequency, is therefore $\mathrm{CP} = \mathrm{A} - (1 - \mathrm{R})\mathrm{L}_{\mathrm{leak}}$.

After subtracting leakage current from the measured current, the slopes of the post correction data are steeper. Converting the slope to charge per cycle using $e = 1.6022 \times 10^{-19}$ Coulomb, we get $n = 0.996$, 0.967 and 0.955 for the rise/fall time of 8 ns, 4 ns and 2.5 ns respectively. These n values are closer to 1 than any reported in the literature and they strongly suggest that one charge is indeed

pumped per defect per cycle. There is an apparent trend of a bigger deviation to one charge per cycle as rise/fall time gets shorter. It is most likely due to increases in the deviation (overshoot and ringing) to perfect trapezoidal waveform with faster rise/fall time. Such deviations make leakage correction less accurate.

Note that a traditional explanation of n dependent on rise/fall time predicts an opposite trend—n increases with faster rise/fall time [26]. This explanation is based on the idea of emission loss. The assumption behind the emission loss mechanism is a continuous distribution of defect energy states spanning the entire silicon band gap. This explanation clearly cannot work when there is only one defect.

4. Discussion

The results shown here are clearly confounded by the leakage current, and the correction procedure is somewhat limited. Notice that the leakage-corrected data for the 2.5 ns rise time plot in Figure 2 is missing the first point, which has a value of −8.9 fA, suggesting a slight over-correction exists. There are two sources of leakage, namely gate leakage and junction leakage. Gate leakage can be eliminated by simply using a thicker gate oxide. For example, increasing the gate oxide thickness from 2 nm to 7 nm will reduce the gate leakage by as much as 15 orders of magnitude [27]. For junction leakage, a properly made junction can have leakage down to less than 10^{-19} A for the small device geometry used in this work [28]. Fortunately, these very properties are also required for the cell transistor of dynamic random-access memory (DRAM), and DRAM is a very well-developed technology. Thus, testing the method on DRAM cell transistors is the natural next step.

It is useful to examine if the elimination of leakage could lead to high enough accuracy.

Figure 3 shows the charge-pumping concept in detail: At strong inversion (Figure 3A), the surface potential barrier in the channel (blue curve) is suppressed so that electrons from source and drain flood the channel (red arrows), allowing the empty defect site (x) to capture an electron (red circle). As the gate voltage is reversed toward depletion, the surface potential barrier increases and electrons from the channel flow back out to source and drain as shown in Figure 3B. The electron that was captured by the defect remains as shown in (Figure 3C). As the gate voltage continues to change toward strong accumulation (Figure 3E), holes from the substrate flood the channel. The captured electron at the defect site can recombine with a hole (the red circle disappears). As the gate voltage changes back toward depletion, all the holes flow back to the substrate, except the one that recombined with the electron. The empty defect is now ready to capture an electron the next time the channel is flooded with electrons (Figure 3A) and the net result of one charge-pumping cycle is to move one electron from the source and drain to the substrate (as a missing hole).

Provided that the gate leakage can be minimized, the crucial remaining barriers to utilizing charge pumping to achieve a high precision quantized current source are insurance that: (1) there is only one charge captured per defect, (2) the capture process is fully complete, and (3) the captured charge will not be lost by emission before recombination occurs.

Perhaps the most important question surrounding this approach is an insurance of single charge capture per defect site per cycle. It has been shown that only interface defects contribute to the charge-pumping current [29]. It has been argued that the interface defect is a P_{b0} center [30,31], which is an interfacial dangling bond on a silicon atom, which is back bonded to three additional silicon atoms. This silicon dangling bond defect is well-known to be amphoteric, meaning that it can capture an electron to become negatively charged or lose an electron to become positively charged, as suggested by electron spin resonance (ESR) spectroscopy [30,31]. This would mean Figure 3 is incomplete. While the process represented in Figure 3G to Figure 3A involves the neutral dangling bond defect capturing an electron to become negatively charged, the neutral dangling bond losing a charge is omitted as it should happen between Figures 3E and 3F. However, this would mean two charges are pumped per CP cycle instead of one and would be inconsistent with the data in Figure 2.

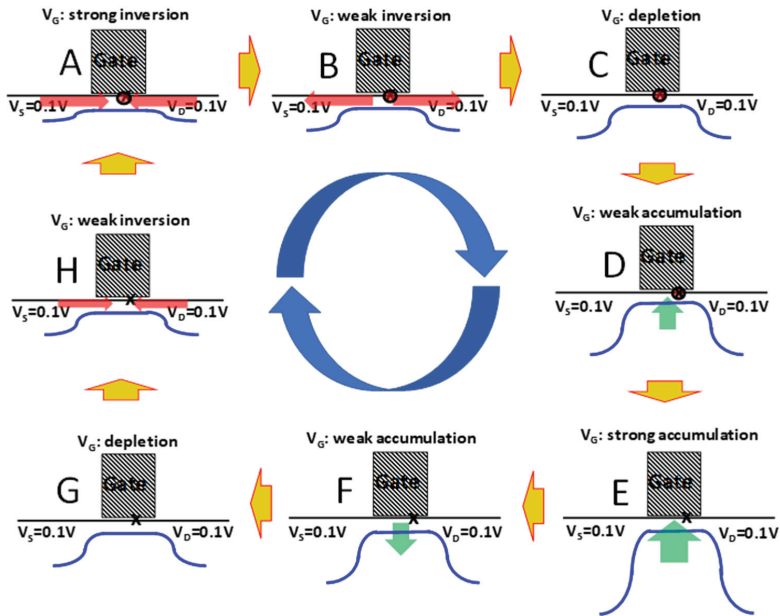

Figure 3. Illustration of the charge-pumping concept. Blue line is the surface potential drawing in one dimension varying from source to drain. Red arrows indicate electron flux (minority carriers in a n-channel metal-oxide-semiconductor field-effect-transistor (MOSFET)). Green arrows indicate hole flux. X indicates an interface defect, and x with a red circle indicates an electron is captured on the defect site. The cycling of the gate voltage from strong inversion (**A**) to depletion (**D**) to strong accumulation (**E**) to depletion (**G**) and back to (**A**) serves to modulate the surface potential in the channel and therefore controls the flow of electrons from source and drain and holes from the substrate.

The idea that all true interface states are P_{b0} centers is not universally accepted [32,33]. There could be another true interface state that is not amphoteric. If the defect responsible for results shown in Figure 2 is one such non-amphoteric defect, the mystery is solved. Though, this is unsupported by the majority of the ESR literature.

If the defect is a P_{b0} center, one possible reason for the discrepancy is that the defect can still be amphoteric but only one of the charged states is involved in the CP process. The evidence of the amphoteric nature of the interface states comes mainly from capacitance-voltage (CV) and electron-spin-resonance (ESR) studies [30]. There are clearly two defect energy peaks in some measured CV curves separated by ~0.7 eV, indicating that the defect energy level is gate bias-dependent but has two stable values. Similarly, the ESR signal remains strong between the energies defined by these two CV peak locations, which clearly suggests that both peaks represent the neutral silicon dangling bond. At energies beyond these two peaks, either higher or lower, the ESR signal vanishes, indicating the defect has either captured an electron to become negatively charged or lost the electron to become positively charged [34].

Here we propose that the two CV peaks correspond to two stable configurations of the same dangling bond under the bias. One might expect, when the gate bias is in inversion, the silicon dangling bond has more sp^3-like character (tetrahedral, the field vertical to the interface pulls the electron away from the silicon atom) and resembles the expected configuration of a defect with a captured electron. This configuration is also called the acceptor state. Similarly, when gate is negative, the same silicon atom has a more sp^2-like character (planar, the field pushes the electron toward the atom) and

resembles the configuration of the positively charged defect (the silicon atom has three bonds, or six bonding electrons). This configuration is also called the donor state [34].

Note that silicon normally does not bond in sp^2 fashion because the remaining p_z orbital must form a π bond [35], which is difficult due to its size. However, for the donor state to be an efficient configuration to capture a hole, it must resemble the configuration of the final state—missing an electron, or a silicon atom that has only three valence electrons. Since the fourth electron is absent, there is no need to form the π bond when the rest of the three electrons form sigma bonds with neighboring silicon atoms. In the intermediary state, before hole capture, the fourth electron is localized on the silicon but sp^2 reconfiguration has not yet occurred due to the energetic cost. The fourth electron remains non-bonding (dangling), and there is only a small energy penalty to lose this non-bonding electron. (capture a hole if available).

As sp^3 and sp^2 are known stable configurations of hybridized orbitals, intermediary configurations are symmetry forbidden and therefore unlikely. At energies between these two peak values, we do not have other configurations but a distribution between these two configurations. The total number of dangling bonds remains unchanged. This explains why the ESR signal remains flat.

Between stable configurations (low energy levels) is an energy barrier, making the conversion between one configuration to another only observable when the gate voltage is swept very slowly (as those in ESR or CV experiments). To get an idea of how hard it is to convert between these two configurations, an analogue may be drawn from reconfiguration energy in the capture and emission charge in the near interface dielectric region. It has recently been shown that this reconfiguration energy is of the order 0.7 eV, and capture is followed by an extremely slow emission due at least in part to the large configuration energy barrier associated with capture [36]. Since the donor/accepter configurations discussed above are also subject to a strong driving force—the electric field, the sp^2/sp^3 reconfiguration is observable when the voltage sweep is very slow. The situation is quite different in CP experiments where the time spent at strong inversion or accumulation is too short for the neutral dangling bond defect to change from one configuration to the other even though the field is switched back and forth. In other words, while both dangling bond configurations are accessible in CP experiments, only one configuration participates in the charge pumping process. Figure 4 illustrates the two possible CP cycles each involving only one configuration of the same dangling bond defect.

Figure 4a,b shows how CP starting with one energy state of the dangling bond will stick to that same energy state throughout the CP cycle. In both cases, panel c illustrates that capturing a hole by the accepter state or capturing an electron by the donor state is prohibited (large energy barrier) without reconfiguration, which occurs on time scales much longer than the CP half cycle. Note that in both cases, the CP cycle can start at panel c instead of a, and the result is equivalent. This explains the data in Figure 2 and why there is only one charge per interface defect per CP cycle. We note that this speculative explanation of the charge pumping process does deviate from the conventional explanation. However, this fine point may have been lost in the initial formulations of the CP process since the early observations were undoubtedly dealing with an energy continuum of interface states due to the larger defect densities. In the limit of charge pumping a single interface state defect, the charge capture process deals with discrete energy levels that act to further confound CP interpretation. We note that this already complex scenario can be further complicated by the presence of the P_{b1} interface defect variants [37,38].

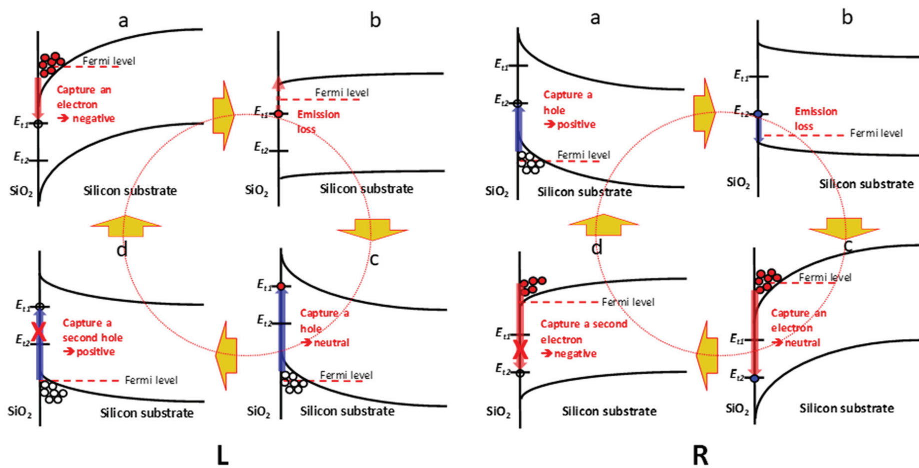

Figure 4. Band diagram of the Si/SiO$_2$ interface showing the two energy levels, E_{t1} and E_{t2}, of a dangling bond defect. **L**: CP cycle involving only the sp^3-like accepter energy state E_{t1}. (**a**) At strong inversion, the E_{t1} state captures an electron to become negatively charged; (**b**) sweeping through depletion toward accumulation provides a small time-energy window for emission loss; (**c**) at strong accumulation, the E_{t1} state captures a hole to become neutral again; (**d**) while still accumulated, the neutral E_{t1} state does not have enough time to convert to E_{t2} state and cannot capture another hole to become positively charged. **R**: CP cycle involving only the sp^2-like donor energy state E_{t2}. (**a**) At strong accumulation, the E_{t2} state captures a hole to become positively charged; (**b**) sweeping through depletion toward inversion provides a small time-energy window for emission loss; (**c**) at strong inversion, the E_{t2} state captures an electron to become neutral again; (**d**) while still inverted, the neutral E_{t2} state does not have enough time to convert to E_{t1} state and cannot capture another electron to become negatively charged.

Figure 4 also illustrates several factors that can potentially degrade the precision of the quantum current source. As per the above discussion, it is somewhat difficult to ensure that only one charge is pumped per defect per cycle. From the above discussion, the barrier that prohibits an accepter state to act like a donor state or vice versa is not infinite. One might be able to modify this barrier by modifying the strength of the accumulation or inversion biases as well as the time available to overcome it (CP frequency). Limiting the accumulation and inversion biases and increasing the CP frequency obviously are fruitful propositions. However, these measures will worsen our insurance that the charge capture process has enough time to complete (factor 2).

Referring to Figure 4, panels a and c for both cases L and R represents the capturing processes. The completeness of charge capture (factor 2) depends on the capture rate and the available capture time (half the CP period). The capture rate is dependent on the density of carriers available. Thus, the time available for capture and the density of available carriers are the keys to this obstacle. Fortunately, the density of carriers available for capture, and thus the capture rate, grows exponentially with increasing inversion or accumulation bias. So, to achieve complete capture, the inversion and accumulation biases need to be increased and the capture time needs to be extended. We note that both requirements are the exact opposite tactics used to ensure that only one charge is captured per defect per cycle (factor 1). An optimum compromise exists and that will determine the ultimate precision of the quantum current source.

Figure 4 panel b of both cases L and R illustrates the process that is susceptible to emission loss (factor 3). As the gate voltage is swept from strong inversion/accumulation through depletion toward accumulation/inversion, there is a short time window when the captured charge can emit out of the defect state. This time window is a small fraction of the rise/fall time of the CP waveform, and the

probability of emission depends on the depth of the defect energy state in the silicon band gap. The traditional CP theory [26] predicts finite emission loss regardless of how fast one makes the rise/fall time because it assumes a continuous distribution of defect energy states throughout the silicon band gap. As mentioned above, this picture clearly not applicable here. The depth of both E_{t1} and E_{t2} are known and they are deep enough that they would be normally considered negligible in traditional CP. However, using CP as a high precision quantized current standard requires a consideration of this emission loss. Again, shorter CP rise/fall time is the direct means to minimize this factor.

5. Conclusions

In summary, we propose and demonstrate a potential quantized current source based on charge pumping in a nanoscale MOSFET. Confounding factors such as gate leakage, single and complete charge capture per cycle, and emission loss have been discussed in detail. Many of the experimental tradeoffs discussed above are in conflict such that an experimental middle ground must be explored before one can estimate accuracy. The potential of using CP as a quantized current source is clearly demonstrated. The advantage of room temperature operation, potential for high current level, and the reliance on matured technology make the proposed method quite appealing as a quantized current standard that can be deployed outside the laboratory.

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References

1. In Proceedings of the 26th General Conference on Weights and Measures (CGPM), Versailles, France, 16 November 2018. Available online: https://www.bipm.org/en/cgpm-2018/ (accessed on 31 March 2020).
2. Likharev, K.K.; Zorin, A.B. Theory of Bloch-wave oscillations in small Josephson Junctions. *J. Low Temp. Phys.* **1985**, *59*, 347–382. [CrossRef]
3. Averin, D.V.; Likharev, K.K. Coulomb blockade of single-electron tunneling, and coherent oscillations in small tunnel junctions. *J. Low Temp. Phys.* **1986**, *62*, 345–373. [CrossRef]
4. Geerligs, L.J.; Anderegg, V.F.; Holweg, P.A.M.; Mooij, J.E.; Pothier, H.; Esteve, D.; Urbina, C.; Devoret, M.H. Frequency-locked turnstile device for single electrons. *Phys. Rev. Lett.* **1990**, *64*, 2691. [CrossRef] [PubMed]
5. Kouwenhoven, L.P.; Johnson, A.T.; van der Vaart, N.C.; Harmans, C.J.P.M.; Foxon, C.T. Quantized current in a quantum-dot turnstile using oscillating tunnel barriers. *Phys. Rev. Lett.* **1991**, *67*, 1626. [CrossRef] [PubMed]
6. Pothier, H.; Lafarge, P.; Urbina, C.; Esteve, D.; Devoret, M.H. Single-Electron Pump Based on Charging Effects. *Europhys. Lett.* **1992**, *17*, 249. [CrossRef]
7. Keller, M.W.; Martinis, J.M.; Zimmerman, N.M.; Steinbach, A.H. Accuracy of electron counting using a 7-junction electron pump. *Appl. Phys. Lett.* **1996**, *69*, 1804. [CrossRef]
8. Shilton, J.M.; Talyanskii, V.I.; Pepper, M.; Ritchie, D.A.; Frost, J.E.F.; Ford, C.J.B.; Smith, C.G.; Jones, G.A.C. High-frequency single-electron transport in a quasi-one-dimensional GaAs channel induced by surface acoustic waves. *J. Phys. Condens. Matter* **1996**, *8*, L531. [CrossRef]
9. Blumenthal, M.D.; Kaestner, B.; Li, L.; Giblin, S.; Janssen, T.J.B.M.; Pepper, M.; Anderson, D.; Jones, G.; Ritchie, D.A. Gigahertz quantized charge pumping. *Nat. Phys.* **2007**, *3*, 343. [CrossRef]
10. Kaestner, B.; Kashcheyevs, V.; Amakawa, S.; Blumenthal, M.D.; Li, L.; Janssen, T.J.B.M.; Hein, G.; Pierz, K.; Weimann, T.; Siegner, U.; et al. Single-parameter nonadiabatic quantized charge pumping. *Phys. Rev. B* **2008**, *77*, 153301. [CrossRef]
11. Pekola, J.P.; Vartiainen, J.J.; Mottonen, M.; Saira, O.-P.; Meschke, M.; Averin, D.V. Hybrid single-electron transistor as a source of quantized electric current. *Nat. Phys.* **2008**, *4*, 120. [CrossRef]
12. Maisi, V.F.; Pashkin, Y.A.; Kafanov, S.; Tsai, J.S.; Pekola, J.P. Parallel pumping of electrons. *New J. Phys.* **2009**, *11*, 113057. [CrossRef]

13. Mooij, J.E.; Nazarov, Y.V. Superconducting nanowires as quantum phase-slip junctions. *Nat. Phys.* **2006**, *2*, 169. [CrossRef]
14. Astafiev, O.V.; Ioffe, L.B.; Kafanov, S.; Pashkin, Y.A.; Arutyunov, K.Y.; Shahar, D.; Cohen, O.; Tsai, J.S. Coherent quantum phase slip. *Nature* **2012**, *484*, 355. [CrossRef] [PubMed]
15. Pekola, J.P.; Saira, O.-P.; Maisi, V.F.; Kemppinen, A.; Möttönen, M.; Pashkin, Y.A.; Averin, D.V. Single-electron current sources: Toward a refined definition of the ampere. *Rev. Mod. Phys.* **2013**, *85*, 1421. [CrossRef]
16. Giblin, S.P.; Kataoka, M.; Fletcher, J.D.; See, P.; Janssen, T.J.B.M.; Griths, J.P.; Jones, G.A.C.; Farrer, I.; Ritchie, D.A. Towards a quantum representation of the ampere using single electron pumps. *Nat. Commun.* **2012**, *3*, 930. [CrossRef] [PubMed]
17. Janssen, T.J.B.M.; Giblin, S.; See, P.; Fletcher, J.; Kataoka, M. Redefinition of the Ampere. *Meas. Control.* **2014**, *47*, 315–322. [CrossRef]
18. Brugler, J.; Jespers, P. Charge pumping in MOS devices. *IEEE Trans. Electron Devices* **1969**, *16*, 297–302. [CrossRef]
19. Schroder, D.K. *Semiconductor Material and Device Characterization*, 3rd ed.; John Wiley & Sons: Hoboken, NJ, USA, 2015; ISBN 978-0-471-73906-7.
20. Groeseneken, G.; Wolf, D.I.; Bellens, R.; Maes, E.H. Charge Pumping of Single Interface Traps in Submicron MOSFET's. In Proceedings of the 24th European Solid-State Device Research Conference ESSDERC'94, Edinburgh, UK, 11–15 September 1994.
21. Groeseneken, G.; De Wolf, I.; Bellens, R.; Maes, H.E. Observation of single interface traps in submicron MOSFET's by charge pumping. *IEEE Trans. Electron Devices* **1996**, *43*, 940–945. [CrossRef]
22. Saks, N.S.; Groeseneken, G.; DeWolf, I. Characterization of individual interface traps with charge pumping. *Appl. Phys. Lett.* **1996**, *68*, 1383–1385. [CrossRef]
23. Tsuchiya, T.; Ono, Y. Charge pumping current from single Si/SiO2 interface traps: Direct observation of Pb centers and fundamental trap-counting by the charge pumping method. *Jpn. J. Appl. Phys. Part 1* **2015**, *54*, 1–7.
24. Tsuchiya, T.; Lenahan, P.M. Distribution of the energy levels of individual interface traps and a fundamental refinement in charge pumping theory. *Jpn. J. Appl. Phys.* **2017**, *56*, 31301. [CrossRef]
25. Ryan, J.T.; Zou, J.; Southwick, R.; Campbell, J.P.; Cheung, K.; Oates, A.S.; Huang, R. Frequency-Modulated Charge Pumping With Extremely High Gate Leakage. *IEEE Trans. Electron Devices* **2015**, *62*, 769–775. [CrossRef]
26. Bosch, G.V.D.; Groeseneken, G.; Heremans, P.; Maes, H. Spectroscopic charge pumping: A new procedure for measuring interface trap distributions on MOS transistors. *IEEE Trans. Electron Devices* **1991**, *38*, 1820–1831. [CrossRef]
27. Cheung, K.P. *Plasma Charging Damage*; Springer: London, UK, 2001; Chapter 1; ISBN 1-85233-144-5.
28. Horikawa, M.; Mizutani, T.; Noda, K.; Kitano, T. Precise Measurement of P-N Junction Leakage Current Generated in Si Substrate. *Proc. IEEE Int. Conf. Microelectr. Test Struct.* **1995**, *80*, 113.
29. Ryan, J.; Campbell, J.; Cheung, K.; Suehle, J.; Ma, Z.; Seiler, D. Charge Pumping for Reliability Characterization and Testing of Nanoelectronic Devices. In *Metrology and Diagnostic Techniques for Nanoelectronics*; Ma, Z., Seiler, D.G., Eds.; Pan Stanford Publishing Ltd.: Singapore, 2017; ISBN 978-981-4745-08-6.
30. Lenahan, P.M.; Conley, J.F., Jr. What can electron paramagnetic resonance tell us about the Si/SiO 2 system? *J. Vac. Sci. Technol. B Microelectron. Nanometer Struct.* **1998**, *16*, 2134. [CrossRef]
31. Poindexter, E.H.; Gerardi, G.J.; Rueckel, M.-E.; Caplan, P.J.; Johnson, N.M.; Biegelsen, D.K. Electronic traps and Pb centers at the Si/SiO2 interface: Band-gap energy distribution. *J. Appl. Phys.* **1984**, *56*, 2844. [CrossRef]
32. Stathis, J.; Dori, L. Fundamental chemical differences among Pb defects on (111) and (100) silicon. *Appl. Phys. Lett.* **1991**, *58*, 1641–1643. [CrossRef]
33. Cartier, E.; Stathis, J.H. Atomic hydrogen-induced degradation of the Si/SiO_2 Structure. *Microelectron. Eng.* **1995**, *28*, 3. [CrossRef]
34. Lenahan, P.M.; Dressendorfer, P.V. Hole traps and trivalent silicon centers in metal/oxide/silicon devices. *J. Appl. Phys.* **1984**, *55*, 3495. [CrossRef]
35. Jose, D.; Datta, A. Structures and Chemical Properties of Silicene: Unlike Graphene. *Acc. Chem. Res.* **2014**, *47*, 593–602. [CrossRef]
36. Cheung, K.; Veksler, D.; Campbell, J. Local Field Effect on Charge-Capture/Emission Dynamics. *IEEE Trans. Electron Devices* **2017**, *64*, 5099–5106. [CrossRef] [PubMed]

37. Mishima, T.D.; Lenahan, P.M.; Weber, W. Do P_{b1} centers have levels in the Si band gap? Spin-dependent recombination study of the P_{b1} "hyperfine spectrum". *Appl. Phys. Lett.* **2000**, *76*, 3771–3773. [CrossRef]
38. Campbell, J.P.; Lenahan, P.M. Density of states of P-b1 Si/SiO2 interface trap centers. *Appl. Phys. Lett.* **2002**, *80*, 1945–1947. [CrossRef]

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A One-Dimensional Effective Model for Nanotransistors in Landauer–Büttiker Formalism

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Abstract: In a series of publications, we developed a compact model for nanotransistors in which quantum transport in a variety of industrial nano-FETs was described quantitatively. The compact nanotransistor model allows for the extraction of important device parameters as the effective height of the source-drain barrier, device heating, and the quality of the coupling between conduction channel and the contacts. Starting from a basic description of quantum transport in a multi-terminal device in Landauer–Büttiker formalism, we give a detailed derivation of all relevant formulas necessary to construct our compact nanotransistor model. Here we make extensive use of the the R-matrix method.

Keywords: nanotransistor; quantum transport; Landauer–Büttiker formalism; R-matrix method

1. Introduction

Around 2005–2010, the transistors obeying Moore's law where strained high-k metal gate MOSFETs with channel lengths between 20–40 nm. At this point a further reduction of the transistor size in a conventional MOSFET becomes difficult because of short channel effects that reduce the gate voltage control over the conduction channel. To counteract this loss of control new transistor architectures were developed. In industrial applications the FinFET and the SOI transistor architecture hwere applied to continue Moore's law to presently below 10nm gate length. It is now generally accepted that in this length-regime quantum transport becomes dominant and Moore's law thus enters the domain of quantum electronics.

In a series of papers [1–8], we developed a compact transistor model in which quantum transport in a variety of industrial nano-FETs could be described quantitatively [6–8]. Our compact transistor model allows for the extraction of important device parameters as the effective height of the source-drain barrier of the transistor, device heating, and the overlap between the wave functions in the contacts and in the electron channel thus describing the quality of the coupling between conduction channel and contacts. Our starting point is a general description of quantum transport in a multi-terminal device in Landauer–Büttiker formalism which we formulate in the R-matrix formalism [1,2]. Using the R-matrix formalism as the essential tool, we give in this paper a systematic and comprehensive derivation of all relevant formulas necessary to construct our compact transistor model.

The concept of Landauer–Büttiker formalism was pioneered by Frenkel [9], Ehrenberg and Hönl [10], Landauer [11,12], Tsu and Esaki [13], Fisher and Lee [14], and Büttiker [15–17]. The central quantities of Landauer–Büttiker formalism are the transmission coefficients of the scattering solutions of the Schrödinger equation. In recent decades, Landauer–Büttiker formalism has been applied in fundamental research to numerous mesoscopic systems. Well-known examples include interferometric measurements in an Aharonov-Bohm ring [15,18], the quenching of the quantum Hall effect in small junctions [19,20], the quantized conductance in ballistic point contacts [21,22], resonant transport through double barrier systems [23], Coulomb blockade oscillations [24,25], spintronic effects [26–28], and Hanbury Brown and Twiss experiments on current fluctuations [29–32].

For formal developments as well as for numerical- and analytical evaluations of the mentioned transmission coefficients of the scattering functions we employ the R-matrix method. This method was introduced by Wigner and Eisenbud and has been widely used in atomic and nuclear physics (for reviews see Refs. [33,34]). A similar method was developed by Kapur and Peierls [35]. The application of the R-matrix technique to mesoscopic semiconductor systems was demonstrated by Smrčka [36] for one-dimensional structures. Since then it has been applied to a variety of other semiconductor nano-structures as point contacts [37], quantum dots [38,39], resonant tunneling in double barrier systems [40], four-terminal cross-junctions [41], gate all around and double gate MOSFETs [42,43], nanowire transistors [44], spin FETs [45], magneto-transport in nanowires [46], ballistic transport in wrinkled superlattices [47], and spin controlled logic gates [48]. A conceptual advantage of the R-matrix method is that for the construction of the transmission coefficients only properties of general wave function solutions of the time-independent Schrödinger equation are necessary (see Equation (21)). This is in contrast to the often used non-equillibrium Green's function approach [49] which relies on the calculation of Green's functions from which the transmission coefficients have to be calculated via the Fisher-Lee relation [14]. Moreover, the existence of the discrete representation of the R-matrix in the eigenbasis of the Wigner–Eisenbud functions (see Equation (22)) allows for the systematic construction of the one-dimensional effective transistor model used in Refs. [6–8] as will be described in Sections 5–8.

2. Landauer–Büttiker Formula for Multi-Terminal Devices

Our model for a multi-terminal system was described in Refs. [1,2]. It consists of a central quantum system located in the scattering volume Ω_0 which is in contact with N terminals denoted with the index $s = 1 \ldots N$ (see Figure 1). In the scattering volume the potential acting on charge carriers can be arbitrary. For each terminal we assume the existence of, first, a reservoir R_s for the charge carriers in which their chemical potential μ_s is defined and, second, a contact region Ω_s to the scattering volume in which coherent scattering states Ψ^s are formed (see Equation (4)). The Ψ^s are thus outgoing from this contact and they are coherent in the volume $\Omega = \Omega_0 \cup (\cup_s \Omega_s)$. As illustrated in Figure 1 we define in each Ω_s a local coordinate system spanned by a triple or orthonormal basis vectors $\vec{n}_s$, $\vec{t}_s^1$, and $\vec{t}_s^2$ so that we can write

$$\vec{r} = \vec{R}_s + x_s\vec{t}_s^1 + y_s\vec{t}_s^2 + z_s\vec{n}_s \equiv \vec{R}_s + z_s\vec{n}_s + \vec{r}_{\perp;s}, \tag{1}$$

where $\vec{R}_s$ points to the origin of the local coordinate system. The coordinate z_s varies in the longitudinal direction and x_s and y_s in the two transverse directions. For the interface Γ_s between Ω_s and Ω_0 one has $z_s = 0$ with z_s growing towards the interior of the contact region. Furthermore, $\vec{n}_s$ is the surface normal vector to Γ_s. We require that the potential energy V of the charge carriers (electrons) in the contact regions takes the form

$$V(\vec{r} \in \Omega_s) = V_s(\vec{r}_{\perp;s}) - eU_s. \tag{2}$$

Here we assume that the reservoir R_1 is grounded with the chemical potential $\mu_1 = \mu$. To each of the other reservoirs $s \neq 1$ a gate voltage U_s is applied where we formally define $U_1 = 0$. Then one has $\mu_s = -eU_s + \mu$. As usual in the Landauer–Büttiker approach, the scattering states Ψ^s which are formed in Ω_s are occupied according to the Fermi–Dirac distribution function with the chemical potential μ_s. Furthermore, in R_s the outgoing parts of the scattering states $\Psi^{s' \neq s}$ arriving in s are absorbed completely, without any back-reflection.

Following further the theoretical framework of Landauer and Büttiker we start from the scattering solutions of the stationary Schrödinger equation

$$\left[-\frac{\hbar^2}{2m^*} \triangle + V(\vec{r}) - E\right] \Psi(\vec{r}, E) = 0 \tag{3}$$

in the coherence region Ω. The relevant wave functions can be taken to vanish outside the coherence volume leading to the boundary condition $\Psi(\vec{r} \in \Gamma, E) = 0$ where Γ is the surface of Ω excluding the $\bar{\Gamma}_s$ (see Figure 1). The scattering solutions Ψ^{sn} out-going from contact s can be written in each of the contacts $\Omega_{s'}$ as

$$\Psi^{sn}(\vec{r} \in \Omega_{s'}, E) = \exp\left(-ik_{sn}z_s\right)\Phi_{sn}(\vec{r}_{\perp;s})\delta_{s,s'} + \sum_{n'} S_{s'n',sn}(E) \exp\left(ik_{s'n'}z_{s'}\right)\Phi_{s'n'}(\vec{r}_{\perp;s'}). \tag{4}$$

Here the transverse mode functions Φ_{sn} are the solutions of the eigenvalue problem

$$\left[-\frac{\hbar^2}{2m^*}\Delta_{\vec{r}_{\perp;s}} + V_s(\vec{r}_{\perp;s}) - E_\nu^\perp\right]\Phi_\nu(\vec{r}_{\perp;s}) = 0 \tag{5}$$

defining the index of the transverse mode n, the composite mode index $\nu = (s, n)$, and $\Delta_{\vec{r}_{\perp;s}} = \partial^2/\partial x_s^2 + \partial^2/\partial y_s^2$. The wave numbers of the harmonic waves in Equation (4) are given by

$$k_\nu = \hbar^{-1}\sqrt{2m^*(E - E_\nu^\perp + eU_s)}. \tag{6}$$

The first factor on the right hand side of Equation (4) is the in-going part characterizing the scattering state. The second factor on the r.h.s. contains the out-going components which are determined by the S-matrix $S_{\nu'\nu}$. In Section 3 we construct the S-matrix $S_{\nu'\nu}$ in the R-matrix approach.

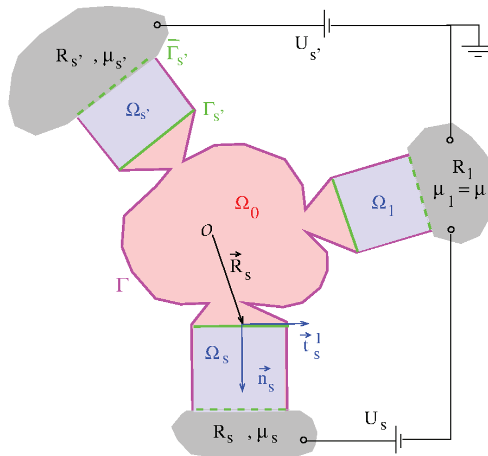

Figure 1. Idealized multi-terminal system: $N = 3$ terminals denoted with the index s are connected to the central scattering volume Ω_0 (red). Each terminal is associated, first, with a charge carrier reservoir R_s defining the chemical potential μ_s (grey) of the carriers. Second, it is associated with a contact region Ω_s (blue) in which coherent scattering states are formed. In green we plot the interfaces Γ_s between the Ω_s and Ω_0 (solid) as well as the interfaces $\bar{\Gamma}_s$ between the Ω_s and R_s (dashed). The coherence volume Ω of the scattering states comprises the set union of Ω_0 and all Ω_s. Here Γ is the surface of Ω excluding the $\bar{\Gamma}_s$ (magenta).

The total electric current I_s in terminal s is calculated in Appendix A. We find

$$I_s = \frac{2e}{h}\sum_{s'}\int_{-\infty}^{\infty} dE[f(E-\mu_s) - f(E-\mu_{s'})]T_{s's}(E) \tag{7}$$

with the Fermi–Dirac distribution $f(x) = [e^{x/(k_BT)} + 1]^{-1}$, the elementary charge e, the current transmission sum

$$T_{s's}(E) = \sum_{nn'} \Theta(E - E_{sn}^{\perp} + eU_s)\Theta(E - E_{s'n'}^{\perp} + eU_{s'})|\tilde{S}_{s'n',sn}(E)|^2 = T_{ss'}(E), \tag{8}$$

and the current S-matrix

$$\tilde{S}_{\nu'\nu} = k_{\nu'}^{1/2} S_{\nu'\nu} k_{\nu}^{-1/2}. \tag{9}$$

3. Construction of the S-matrix with the R-matrix Method

We write the general solution of Equation (3) in each of the Ω_s in the form

$$\Psi(\vec{r} \in \Omega_s, E) = \sum_n \Psi_{sn}^{in} \exp\left(-ik_{sn}z_s\right)\Phi_{sn}(\vec{r}_{\perp;s}) + \sum_n \Psi_{sn}^{out} \exp\left(ik_{sn}z_s\right)\Phi_{sn}(\vec{r}_{\perp;s}). \tag{10}$$

Because of the linearity of the problem the S-matrix in Equation (4) can be defined as the linear mapping from the Ψ^{in} onto the Ψ^{out} of the form

$$\Psi_{\nu}^{out} = \sum_{\nu'} S_{\nu\nu'} \Psi_{\nu'}^{in}. \tag{11}$$

To construct $S_{\nu\nu'}$ we expand the wave function in the scattering volume Ω_0 in the orthonormal and complete set of Wigner–Eisenbud functions $\chi_l(\vec{r})$,

$$\Psi(\vec{r}, E) = \sum_{l=1}^{\infty} a_l(E)\chi_l(\vec{r}) \tag{12}$$

with

$$a_l(E) = \int_{\Omega_0} d\vec{r}\, \chi_l(\vec{r})\Psi(\vec{r}, E) \tag{13}$$

(see Appendix B). The Wigner–Eisenbud functions χ_l are the solutions of the Schrödinger equation

$$\left[-\frac{\hbar^2}{2m^*}\Delta + V(\vec{r}) - \mathcal{E}_l\right]\chi_l(\vec{r}) = 0 \tag{14}$$

in the domain Ω_0. Here one imposes Wigner–Eisenbud boundary conditions, i.e., Neumann boundary conditions of vanishing normal derivative on the Γ_s,

$$\frac{\partial \chi_l}{\partial \vec{n}_s} = 0 \quad \text{for} \quad \vec{r} \in \Gamma_s \tag{15}$$

and Dirichlet boundary conditions on the remaining surface of Ω_0 denoted with $\partial\Omega_0$ writing

$$\chi_l = 0 \quad \text{for} \quad \vec{r} \in \partial\Omega_0. \tag{16}$$

In Appendix B, we show that Wigner–Eisenbud energies $\mathcal{E}_l$ are real and that the Wigner–Eisenbud functions $\chi_l(\vec{r})$ can be chosen real. The normalization is taken as $\int_{\Omega_0} d\vec{r}|\chi_l(\vec{r})|^2 = 1$. To calculate the expansion coefficients a_l we multiply Equation (3) from the left with $\chi_l(\vec{r})$ and Equation (14) from

the left with $\Psi(\vec{r}, E)$. Subtraction of the former equation from the latter and subsequent integration over the whole domain Ω_0 yields with the second Green's identity

$$\begin{aligned}(E - \mathcal{E}_l) \int_{\Omega_0} d\vec{r}\, \chi_l(\vec{r})\Psi(\vec{r}, E) &= -\frac{\hbar^2}{2m^*} \int_{\Omega_0} d\vec{r}\, \left[\chi_l(\vec{r}) \triangle \Psi(\vec{r}, E) - \Psi(\vec{r}, E) \triangle \chi_l(\vec{r})\right] \\ &= -\frac{\hbar^2}{2m^*} \sum_{s=1}^{N} \int_{\Gamma_s} d\Gamma_s \vec{n}_s \left[\chi_l(\vec{r})\nabla\Psi(\vec{r}, E) - \Psi(\vec{r}, E)\nabla\chi_l(\vec{r})\right]. \end{aligned} \tag{17}$$

In the area integration of Equation (17) as well as in the remaining area integrations over the Γ_s we assume according to Equation (1) the parameterization $\vec{r} = \vec{r}(x_s, y_s) = \vec{R}_s + x_s\vec{t}_s^1 + y_s\vec{t}_s^2$ of Γ_s so that

$$d\Gamma_s = dx_s dy_s \left| \frac{\partial \vec{r}}{\partial x_s} \times \frac{\partial \vec{r}}{\partial y_s} \right| = dx_s dy_s \left| \vec{t}_s^1 \times \vec{t}_s^2 \right| = dx_s dy_s. \tag{18}$$

Using in Equation (17) the notation

$$\Psi^S(\vec{r} \in \Gamma_s, E) = \frac{1}{m^*} \vec{n}_s \nabla\Psi(\vec{r} \in \Gamma_s, E) \tag{19}$$

for the outward surface derivative, applying Equation (13) on the l. h. s., and inserting the boundary conditions for the Wigner–Eisenbud functions, one obtains

$$a_l(E) = -\frac{\hbar^2}{2} \frac{1}{E - \mathcal{E}_l} \sum_s \int_{\Gamma_s} d\Gamma_s\, \chi_l(\vec{r})\, \Psi^S(\vec{r}, E). \tag{20}$$

Returning to Equation (12) it follows that

$$\Psi(\vec{r}, E) = \sum_s \int_{\Gamma_s'} d\Gamma_s'\, R(\vec{r}, \vec{r}'; E)\Psi^S(\vec{r}', E) \tag{21}$$

with

$$R(\vec{r}, \vec{r}'; E) = -\frac{\hbar^2}{2} \sum_{l=1}^{\infty} \frac{\chi_l(\vec{r})\chi_l(\vec{r}')}{E - \mathcal{E}_l}. \tag{22}$$

For $\vec{r} \in \Gamma_s$ we write $\Psi(\vec{r}(x_s, y_s), E) = \Psi(\vec{r}_{\perp;s}, E)$ and establish the expansion

$$\Psi(\vec{r}_{\perp;s}, E) = \sum_n \Psi_{sn}\Phi_{sn}(\vec{r}_{\perp;s}) \tag{23}$$

in the complete orthonormal and real function system of the Φ_{sn} with

$$\Psi_{sn} = \int_{\Gamma_s} d\Gamma_s\, \Phi_{sn}(\vec{r}_{\perp;s})\Psi(\vec{r}_{\perp;s}, E). \tag{24}$$

An analogous expansion

$$\Psi^S(\vec{r}_{\perp;s}, E) = \sum_{sn} \Psi_{sn}^S \Phi_{sn}(\vec{r}_{\perp;s}) \tag{25}$$

holds for the surface derivative. Inserting the expansions Equations (23) and (25) in Equation (21) one obtains after a projection onto Φ_ν

$$\Psi_\nu = \sum_{\nu'} R_{\nu\nu'}\Psi_{\nu'}^S \tag{26}$$

with the R-matrix

$$R_{\nu\nu'} = \int_{\Gamma_s} d\Gamma_s \int_{\Gamma_{s'}} d\Gamma_{s'}'\, \Phi_\nu(\vec{r}_{\perp;s})\Phi_{\nu'}(\vec{r}_{\perp;s'}')R(\vec{r}, \vec{r}'; E) = -\frac{\hbar^2}{2} \sum_{l=1}^{\infty} \frac{\chi_{l\nu}\chi_{l\nu'}}{E - \mathcal{E}_l}, \tag{27}$$

where

$$\chi_{l\nu} = \int_{\Gamma_s} d\Gamma_s \, \Phi_\nu(\vec{r}_{\perp;s}) \chi_l(\vec{r}). \tag{28}$$

Inserting in Equation (26) $\Psi_\nu = \Psi_\nu^{in} + \Psi_\nu^{out}$ and $(\Psi^S)_\nu = -(ik_\nu/m^*)(\Psi_\nu^{in} - \Psi_\nu^{out})$ one arrives at

$$\sum_{\nu'}(\delta_{\nu\nu'} - \frac{i}{m^*} R_{\nu\nu'} k_{\nu'}) \Psi_{\nu'}^{out} = -\sum_{\nu'}(\delta_{\nu\nu'} + \frac{i}{m^*} R_{\nu\nu'} k_{\nu'}) \Psi_{\nu'}^{in}.$$

Defining further a diagonal k-matrix $k_{\nu\nu'} = \delta_{\nu\nu'} k_{\nu'}$ we formally write

$$S = -\frac{1 + \frac{i}{m^*} Rk}{1 - \frac{i}{m^*} Rk}. \tag{29}$$

With the symmetrical current R-matrix

$$\Omega_{\nu\nu'} = k_\nu^{1/2} R_{\nu\nu'} k_{\nu'}^{1/2} \tag{30}$$

it follows for the current S-matrix in Equation (9) that

$$\begin{aligned} \tilde{S} &= k^{1/2} S k^{-1/2} = -k^{1/2}(1 + iRk) k^{-1/2} k^{1/2} (1 - iRk)^{-1} k^{-1/2} = -(1 + i\Omega)(k^{-1/2})^{-1}(1 - iRk)^{-1}(k^{1/2})^{-1} \\ &= -(1 + i\Omega)[k^{1/2}(1 - iRk)k^{-1/2}]^{-1} = -\frac{1 + i\Omega}{1 - i\Omega} = 1 - \frac{2}{1 - i\Omega}. \end{aligned} \tag{31}$$

Here we exploited that for three square matrices one has $(ABC)^{-1} = C^{-1}B^{-1}A^{-1}$. The current transmission matrix is thus seen to be symmetrical while the S-matrix is not symmetrical.

4. Transistor Model

The application of our model for a general multi-terminal system in Section 2 to a conventional n-channel nano-MOSFET is discussed in Ref. [1] (see in particular Figure 3 therein) and in Ref. [2]. Neglecting tunneling currents to the gate we here treat the transistor as a two-terminal device including only the source, $s = 1$, and the drain, $s = 2$. The relevant structure elements of a nano-MOSFET can be taken from Figure 2a depicting the heavily n-doped source- and drain contact, the shallow junction extensions (SJEs) of the contacts, the conduction channel in the p-substrate, and the overlap of the conduction channel with the SJE. The semiconductor-insulator interface is located at $y = 0$. It is represented by a cut-off of the wave functions. The assignment of the structure elements of the nano-MOSFET to the structure elements of the general multi-terminal system in Figure 1 is shown in Figure 2b: The SJEs are assumed to be identical to having the depth D. The SJE of the source is then associated with the cubic contact region Ω_1 with $x \leq 0$, $0 \leq y \leq D$, and $0 \leq z \leq W$. Here W is the width of the transistor. The SJE of the drain is associated with the cubic contact region Ω_2 with $x \geq L$, $0 \leq y \leq D$, and $0 \leq z \leq W$. Here Ω_1 and Ω_2 are semi-infinite corresponding to $\mathcal{L}_s \to \infty$ (see Figure A1). The cubic scattering region Ω_0 with $0 \leq x \leq L$, $0 \leq y \leq D$, and $0 \leq z \leq W$ includes the conduction channel of length L and the overlap of the conduction channel with the SJEs. The interfaces Γ_s are located at $x = 0$ for $s = 1$ and at $x = L$ for $s = 2$. The basis vectors of the local coordinate systems in Equation (1) are $\vec{n}_1 = -\vec{e}_x$ and $\vec{n}_2 = \vec{e}_x$ for the outward normal vectors. Furthermore, we choose $\vec{t}_1^1 = \vec{t}_2^1 = \vec{e}_y$ and $\vec{t}_1^2 = \vec{t}_1^2 = \vec{e}_z$. The local coordinates are $z_1 = -x$, $z_2 = x - L$, $x_1 = x_2 = y$, and $y_1 = y_2 = z$. In Equation (2) we assume the simplest case $V_s = 0$ renaming for $U_2 = U_D$. We take the limit $D \to \infty$ as well as $W \to \infty$ so that electron gas in the heavily doped source and drain in Ω_1 and Ω_2 can be treated as a three dimensional free Fermi gas with the chemical potential

$$\frac{\mu}{k_B T} = X_{1/2}\left[\frac{4}{3\sqrt{\pi}}\left(\frac{E_F}{k_B T}\right)^{3/2}\right] \tag{32}$$

where X_j is the inverse function the Fermi–Dirac integral

$$F_{1/2}(u) = \frac{1}{\Gamma(3/2)} \int_0^\infty dv \frac{v^{1/2}}{e^{v-u}+1}. \tag{33}$$

The Fermi energy above the bottom of the conduction band is given by

$$E_F = \frac{\hbar^2}{2m^e} \frac{3\pi^2 N_D}{N_V}^{2/3} \tag{34}$$

with the doping concentration N_D in the contacts (full ionization of donors), the valley-degeneracy $N_V = 6$ and the effective mass taken as $m^e = (m_1^2 m_2)^{1/3} = 0.33 m_0$. Here $m_1 = 0.19 m_0$ and $m_2 = 0.98$ are the effective masses corresponding to the principle axes of the constant energy ellipsoids.

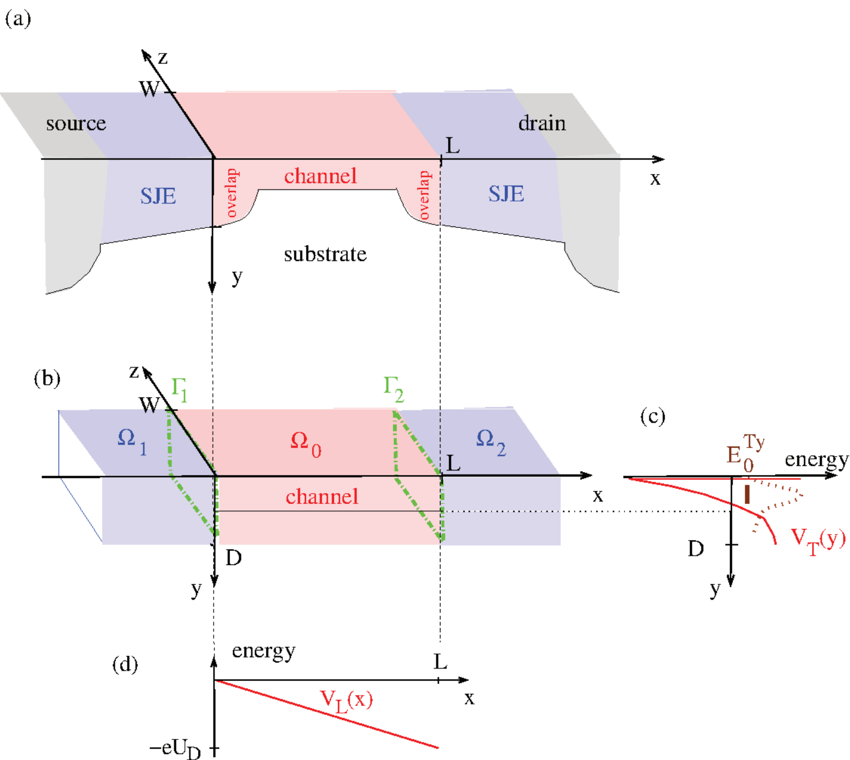

Figure 2. (**a**) Structure elements of a conventional nano-MOSFET: Source- and drain contact with shallow junction extensions SJEs, the latter in blue. In red the conduction channel and the overlap between conduction channel and SJE. The semiconductor-insulator interface is located at $y = 0$. (**b**) Assignment of the above structure elements to the structure elements of the general multi-terminal system in Figure 1: The SJEs are associated with cubic contact regions Ω_s. (**c**) In red: Transverse confinement potential $V_T(y)$ of the conduction channel in the separable ansatz for the potential in Equation (35). In brown the lowest subband energy E_0^{Ty} in the channel confinement potential as defined in Equation (62) (solid) and the corresponding eigenfunction (dotted). (**d**) Linear drop of the applied drain voltage leading to a linear longitudinal potential $V_L(x)$ in Equation (35).

For the potential in the scattering area Ω_0 we choose a separable form

$$V(\vec{r} \in \Omega_0) = V_T(y) + V_L(x) \tag{35}$$

(see Figure 2c,d). Here the transverse potential V_T is the confinement potential for the conduction channel of the transistor. A natural choice for V_T is the confinement potential present in a simple MOS-structure without source- and drain contact as discussed in Refs. [50,51]. Then $V_T(y)$ corresponds to the potential determined in Equation (4) of [50]. As pointed out in Refs. [50,51] in the electron channel a strong lateral sub-band quantization exists so that only the lowest subband of the channel confinement potential with a bottom energy of E_0^{Ty} corresponding to E_0 in Ref. [50] is occupied (see Figure 2c and Equation (62)). Here only the two constant energy ellipsoids with the heavy mass m_2 perpendicular to the (100)-interface are occupied. This leads to a valley degeneracy of $g_v = 2$ in the channel and the effective mass entering (3) is the light mass $m^* = m_1$ [5]. The longitudinal potential V_L arises from the applied drain voltage assumed to fall off linearly so that

$$V_L(x) = -\frac{x}{L} eU_G. \tag{36}$$

The described transistor model has several special properties which can be used to simplify our general multi-terminal model described in Section 2:

- P1 The transistor is treated as two-terminal system.
- P2 *Axial contacts*: For all Γ_s the surface normal vectors are aligned so that $\vec{n}_s = \pm\vec{n}$. For our transistor model $\vec{n}_2 = -\vec{n}_1 = \vec{n} = \vec{e}_x$.
- P3 *Global separability (see Figure 2b)*: In a system with axial contacts in $\vec{n} = \vec{e}_x$-direction the potential in the scattering area Ω_0 is the sum of a longitudinal potential $V_L(x)$ varying in $\vec{n}$-direction and transverse potential $V_T(y,z)$ varying in the two transverse directions. In the transistor model this separation is given in Equation (35).
- P4 *Abrupt transition (see Figure 2c)* : An inspection of Equations (2) and (35) shows that in the general case the potentials in the contact regions and in the scattering volume come together to form an abrupt transition.
- P5 *Planarity*: For a planar device one can define one or two global transverse coordinates valid in all Ω_s and in Ω_0 on which the potential does not depend. In our transistor model one global transverse coordinate exists which is the width-coordinate z.
- P7 *Single mode approximation:* One assumes strong transverse quantization in the scattering area. Then splitting of the transverse quantum levels induced by V_T is so strong that only the lowest transverse level E_0^T has to be taken into account.

As we will demonstrate in the next sections, on account of the listed special properties the R-matrix approach allows for a systematic reduction of the general theory for a multi-terminal device to a one-dimensional effective transistor model.

5. The R-matrix in a Separable Two-Terminal System

We consider a two-terminal system as in Figure 2b which fulfills the global separability condition P3 in Section 4 (see Figure 3). Inserting the separable potential Equation (35) in Equation (14) makes possible a product ansatz for the Wigner–Eisenbud functions

$$\chi_l(\vec{r}) = \chi_\lambda(x)\phi_k(y,z) \tag{37}$$

with $l = (k, \lambda)$. Here the transverse functions are defined by

$$\left[-\frac{\hbar^2}{2m^*}\left(\frac{d^2}{dy^2} + \frac{d^2}{dz^2}\right) + V_T(y,z) - E_k^T\right]\phi_k(y,z) = 0 \tag{38}$$

with the boundary conditions

$$\phi_k(0,z) = \phi_k(W,z) = \phi_k(y,0) = \phi_k(y,D) = 0. \tag{39}$$

The longitudinal functions are the solutions of

$$\left[-\frac{\hbar^2}{2m^*}\frac{d^2}{dx^2} + V_L(x) - \mathcal{E}_\lambda^L\right]\chi_\lambda(x) = 0 \tag{40}$$

with the one-dimensional Wigner–Eisenbud boundary conditions

$$\chi'_\lambda(0) = \chi'_\lambda(L) = 0. \tag{41}$$

Upon insertion of Equation (37) in Equation (14) one obtains

$$\mathcal{E}_l = \mathcal{E}_\lambda^L + E_k^T. \tag{42}$$

The product ansatz Equation (37) is permissible in the two-terminal system since the one-dimensional Wigner–Eisenbud boundary condition in Equation (41) is compatible with the general Wigner–Eisenbud boundary conditions in Equations (15) and (16). To construct the R-matrix with Equation (37) we write Equation (28) as

$$\chi_{l\nu} = \int_{\Gamma_s} d\Gamma_s\, \Phi_\nu(\vec{r}_{\perp;s})\chi_l(\vec{r}) = \chi_\lambda(x_s)c_{ksn} \tag{43}$$

the overlap factor

$$c_{ksn} = \int_0^D dy \int_0^W dz\phi_k(y,z)\Phi_{sn}(y,z). \tag{44}$$

The Equation (27) becomes

$$R_{\nu\nu'}(E) = -\frac{\hbar^2}{2}\sum_{\lambda k}\frac{c_{ksn}\chi_\lambda(x_s)c_{ks'n'}\chi_\lambda(x_{s'})}{E - \mathcal{E}_\lambda^L - E_k^T}. \tag{45}$$

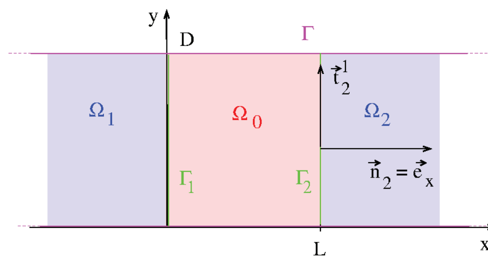

Figure 3. The two-terminal system in Figure 2b where the z-direction is omitted for simplicity. Axial contacts in x-direction: $\vec{n}_2$ points in x-direction, $\vec{n}_1$ in minus x-direction.

6. Effective Approximation and One-Dimensional Effective Scattering Problems

In effective approximation Equation (6) is simplified in the form

$$k_\nu(E) \sim \sqrt{\frac{2m^*}{\hbar^2}\left[E - E_s^{\perp 0} + eU_s\right]} = k_s^{ef}(E), \tag{46}$$

where $E_s^{\perp 0}$ is the smallest transverse mode energy, $E_s^{\perp 0} = \min_n(E_{sn}^{\perp})$. One then finds from Equations (30) and (45)

$$\Omega_{sn,s'n'} = k_{sn}^{1/2} R_{sn,s'n'} k_{s'n'}^{1/2} = \sum_k c_{ksn} c_{ks'n'} \Omega_{ss'}^k \tag{47}$$

with

$$\Omega_{ss'}^k = -\frac{\hbar^2}{2m^*}(k_s^{ef})^{1/2}(k_{s'}^{ef})^{1/2} \sum_\lambda \frac{\chi_\lambda(x_s)\chi_\lambda(x_{s'})}{E - \mathcal{E}_\lambda^L - E_k^T}. \tag{48}$$

The inversion of $1 - i\Omega$ in Equation (31) can now be carried out analytically with the result

$$\left(\frac{1}{1 - i\Omega}\right)_{sns'n'} = \sum_k c_{ksn} c_{ks'n'} \left(\frac{1}{1 - i\Omega^k}\right)_{ss'} \tag{49}$$

(see Appendix C). Going back to Equation (31) one finds for $s \neq s'$

$$|\tilde{S}_{sn,s'n'}|^2 = \left| \left(\frac{2}{1 - i\Omega}\right)_{sn,s'n'} \right|^2 = \sum_{kk'} c_{k,sn} c_{k,s'n'} c_{k'sn} c_{k's'n'} \left(\frac{2}{1 - i\Omega^k}\right)_{ss'} \left(\frac{2}{1 - i\Omega^{k'}}\right)_{ss'}^*. \tag{50}$$

With this relation Equation (A4) becomes with $I_D = I_2$

$$I_D = \frac{2e}{h} \sum_{kk'} \int_{-\infty}^{\infty} dE C_{kk'}(E) \left[f(E - \mu) - f(E - \mu + eU_D) \right] \left(\frac{2}{1 - i\Omega^k}\right)_{ss'} \left(\frac{2}{1 - i\Omega^{k'}}\right)_{ss'}^* \tag{51}$$

with the overlap matrix

$$C_{kk'}(E) = \sum_{n,n'} c_{ksn} c_{ks'n'} c_{k'sn} c_{k's'n'} \Theta\left[E - E_{sn}^{\perp}\right] \Theta\left[E - E_{s'n'}^{\perp} + eU_D\right]. \tag{52}$$

In Appendix D, we demonstrate that instead of using Equation (48) to find $(1 - i\Omega^k)$ with subsequent inversion one can calculate the matrices $(1 - i\Omega^k)^{-1}$ occurring in Equation (51) according to

$$\left(\frac{1}{1 - i\Omega^k}\right)_{21} = -\frac{\sqrt{k_1^{ef} k_2^{ef}}}{2} t^{ef}. \tag{53}$$

Here the t^{ef} are the transmission coefficients resulting in an effective one-dimensional scattering problem associated with the 1d-Schrödinger equation

$$\left[-\frac{\hbar^2}{2m^*} \frac{d^2}{dx^2} + V^{ef}(x) - E \right] \psi^{ef}(x) = 0 \tag{54}$$

with effective scattering potential

$$V^{ef}(x) = \begin{cases} E_1^{\perp 0} & \text{for } x < 0 \\ E_k^T + V_L(x) & \text{for } 0 \leq x \leq L \\ E_2^{\perp 0} - eU_D & \text{for } x > L. \end{cases} \tag{55}$$

Here the asymptotics of the source incident scattering states of the effective scattering problem associated with Equation (54) are given by

$$\psi^{ef}(x < 0) = e^{ik_1^{ef} x} e^{ik_1^{ef} x} + r^{ef} e^{-ik_1^{ef} x}, \tag{56}$$

and

$$\psi^{ef}(x \geq L) = t^{ef} e^{ik_2^{ef}(x - L)}. \tag{57}$$

Appendix E contains a simple, stable and fast recursive algorithm which we used to find the effective transmission coefficients t^{ef}. It is seen from Equation (55) that the quantum levels E_k^T of the confinement potential in the conduction channel that arise in Equation (38) act as offsets in the effective potential.

7. Planar Systems and Supply Functions

In planar systems, the potential is taken as translationally invariant in the z-direction so that $V_s = V_s(y)$ and $V_T = V_T(y)$. For the interface regions Ω_s we insert in Equation (5)

$$\Phi_{sn}(y,z) = \Phi_{sn_y n_z}(y,z) = \Phi_{sn_y}(y)\sqrt{\frac{2}{W}}\sin\left(\frac{n_z\pi}{W}z\right) \tag{58}$$

to find

$$\left[-\frac{\hbar^2}{2m^*}\frac{d^2}{dy^2} + V_s(y) - E^{\perp y}_{sn_y}\right]\Phi_{sn_y}(y) = 0 \tag{59}$$

with $n = (n_y, n_z)$ and

$$E^{\perp}_{sn} = E^{\perp y}_{sn_y} + \frac{\hbar^2}{2m^*}\left(\frac{n_z\pi}{W}\right)^2. \tag{60}$$

For the scattering region we insert in Equation (38)

$$\phi_k(y,z) = \phi_{k_y,k_z}(y,z) = \zeta_{k_y}(y)\sqrt{\frac{2}{W}}\sin\left(\frac{k_z\pi}{W}z\right) \tag{61}$$

to obtain

$$\left[-\frac{\hbar^2}{2m^*}\frac{d^2}{dy^2} + V_T(y) - E^{Ty}_{k_y}\right]\zeta_{k_y}(y) = 0, \tag{62}$$

with $k = (k_y, k_z)$ and

$$E^T_k = E^{Ty}_{k_y} + \frac{\hbar^2}{2m^*}\left(\frac{k_z\pi}{W}\right)^2. \tag{63}$$

With Equations (58) and (62) the overlap factor in Equation (44) becomes

$$c_{ksn} = \delta_{n_z k_z}\int_0^W dy\Phi_{sn_y}(y)\zeta_{k_y}(y) \equiv \delta_{n_z k_z}\bar{c}_{k_y sn_y}. \tag{64}$$

Furthermore from Equation (48) one has

$$\Omega^k_{ss'} = \Omega^{k_y,k_z}_{ss'} = -\frac{\hbar^2}{2m^*}(\bar{k}^{ef}_{s'})^{1/2}(\bar{k}^{ef}_s)^{1/2}\sum_\lambda \frac{\chi_\lambda(x_s)\chi_\lambda(x_{s'})}{E^{xy} - \mathcal{E}^L_\lambda - E^{Ty}_{k_y}} \equiv \bar{\Omega}^{k_y}_{s's}(E^{xy}) \tag{65}$$

with the conserved energy in the xy-plane

$$E^{xy} = E - \frac{\hbar^2}{2m^*}\left(\frac{k_z\pi}{W}\right)^2, \tag{66}$$

and from Equation (46) $k^{ef}_s \sim [(2m^*/\hbar^2)(E^{xy} - E^{\perp y0}_s + eU_s)]^{1/2} = \bar{k}^{ef}_s(E^{xy})$, where $E^{\perp y0}_s = \min_{n_y}(E^{\perp y}_{sn_y})$. In Appendix F it is derived that

$$I_D = \frac{2e}{h}\sum_{k_y k'_y}\int_{-\infty}^{\infty} dE^{xy} C_{k_y k'_y}(E^{xy})\left[S(E^{xy}-\mu) - S(E^{xy}-\mu+eU_D)\right]\left[\frac{2}{1-i\bar{\Omega}^{k_y}(E^{xy})}\right]_{ss'}\left[\frac{2}{1-i\bar{\Omega}^{k'_y}(E^{xy})}\right]^*_{ss'} \tag{67}$$

with wave function overlap

$$C_{k_y k'_y}(E^{xy}) = \sum_{n_y n'_y} \bar{c}_{k_y s n_y} \bar{c}_{k_y s' n'_y} \bar{c}_{k'_y s n_y} \bar{c}_{k'_y s' n'_y} \Theta\left[E^{xy} - E^{\perp y}_{s n_y}\right] \Theta\left[E^{xy} - E^{\perp y}_{s' n'_y} + eU_D\right] \tag{68}$$

and the supply function

$$S(\alpha) = \sum_{n_z} f\left[\alpha + \frac{\hbar^2}{2m^*}\left(\frac{n_z \pi}{W}\right)^2\right]. \tag{69}$$

In the limit $W \to \infty$ we can write with $\Delta k_z = \pi/W$

$$S(\alpha) = \frac{W}{\pi}\sum_{n_z} \Delta k_z f\left(\alpha + \frac{\hbar^2}{2m^*}k_z^2\right) \to \frac{W}{\pi}\int_0^\infty dk_z \frac{1}{e^{\frac{1}{k_B T}\left(\alpha + \frac{\hbar^2}{2m^*}(n_z \Delta)^2\right)} + 1}. \tag{70}$$

Upon introducing

$$y = \frac{1}{k_B T}\frac{\hbar^2}{2m^*}k_z^2 \Rightarrow k_z = \sqrt{\frac{2m^* k_B T}{\hbar^2}}y^{1/2} \Rightarrow dk_z = \sqrt{\frac{2m^* k_B T}{\hbar^2}}\frac{1}{2}y^{-1/2}dy \tag{71}$$

it results that

$$S(\alpha) = \frac{W}{\sqrt{\pi}}\sqrt{\frac{m^* k_B T}{2\hbar^2}}F_{-1/2}\left(-\frac{\alpha}{k_B T}\right). \tag{72}$$

Here the Fermi–Dirac-Integral is given by

$$F_j(x) = \frac{1}{\Gamma(j+1)}\int_0^\infty dy y^j \frac{1}{1 + e^{y-x}} \tag{73}$$

with $\Gamma(1/2) = \sqrt{\pi}$.

In Appendix D, we show that one can calculate the matrices $(1 - i\bar{\Omega}^{k_y})^{-1}$ in Equation (67) from the transmission coefficients resulting in a modified effective one-dimensional scattering problem. Here Equations (53)–(77) are substituted by

$$\left[-\frac{\hbar^2}{2m^*}\frac{d^2}{dx^2} + \bar{V}^{ef}(x) - E^{xy}\right]\bar{\psi}^{ef}(x) = 0, \tag{74}$$

for $D \to 0$

$$\bar{V}^{ef}(x) = \begin{cases} 0 & \text{for } x < 0 \\ E^{Ty}_{k_y} + V_L(x) & \text{for } 0 \le x \le L \\ -eU_D & \text{for } x > L, \end{cases} \tag{75}$$

$$\bar{\psi}^{ef}(x < 0) = e^{i\bar{k}_1^{ef} x} + r^{ef} e^{-i\bar{k}_1^{ef} x}, \tag{76}$$

$$\bar{\psi}^{ef}(x \ge L) = \bar{t}^{ef} e^{i\bar{k}_2^{ef}(x-L)}, \tag{77}$$

and

$$\sqrt{\bar{k}_1^{ef}\bar{k}_2^{ef}}\,\bar{t}_1^{k_y} = -\left(\frac{2}{1 - i\bar{\Omega}^{k_y}}\right)_{21}. \tag{78}$$

8. Single-Mode Approximation and One-Dimensional Effective Model

As pointed out in Section 4, for a conventional nanotransistor only the lowest subband of the channel confinement potential with a bottom energy of E_0^{Ty} resulting at $k_y = 1$ is occupied (see Figure 2c and Equation (62)). Taking into account only $k_y = 1$-terms Equation (67) becomes

$$I_D = \frac{2N_v^{ch}e}{h}C\int_0^\infty dE^{xy}\left[S(E^{xy}-\mu) - S(E^{xy}-\mu+eU_D)\right]\mathcal{T}^{ef}(E^{xy}) \tag{79}$$

with

$$\mathcal{T}^{ef}(E^{xy}) = \left[\frac{2}{1-i\bar{\Omega}^1(E^{xy})}\right]_{ss'}\left[\frac{2}{1-i\bar{\Omega}^1(E^{xy})}\right]^*_{ss'} = k_1 k_2 |t^{ef}|^2 \tag{80}$$

(compare with Equation (1) of Ref. [8]). Here we neglected in the wave function overlap the energy dependence, $C_{11}(E^{xy}) \to C\Theta(E^{xy})$ and introduced the valley degeneracy of $N_v^{ch} = 2$ in the n-type conduction channel.

As described in Section 7 the effective transmission coefficient $\bar{t}^{ef}$ is calculated from the source-incident scattering states of the 1d-Schrödinger Equation (74) with the effective scattering potential given by

$$\bar{V}^{ef}(x) = \begin{cases} 0 & \text{for } x < 0 \\ V_0 - eU_D\frac{x}{L} & \text{for } 0 \le x \le L \\ -eU_D & \text{for } x > L, \end{cases} \tag{81}$$

where set in Equation (75) $V_L(x) = -eU_D x/L$ (linear decrease of the drain voltage) and $E_1^{Ty} = V_0$. The parameter V_0 is interpretable as the effective height of the source-drain barrier. The parameters V_0 and C as well as T are adjusted to experiments in Refs. [6–8].

9. Summary

Starting from a basic description of quantum transport in a multi-terminal device in Landauer–Büttiker formalism in Refs. [1,2] we give a detailed derivation of all relevant formulas necessary to construct a one-dimensional effective model for a nanotransistor described in Refs. [6–8]. In this model, quantum transport in nano-FETs can be described quantitatively. Important device parameters can be extracted as the effective height of the source-drain barrier of the transistor, device heating, and the quality of the coupling between conduction channel and contacts.

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Appendix A. Derivation of the Formula for the Current

We calculate the total current I_s in contact s starting from the decomposition

$$I_s = I_s^{in} - \sum_{s'=1}^{N} I_{s'\to s}^{out} \tag{A1}$$

(see Figure A1). Here I_s^{in} is the absolute value of the current in contact s created by the in-going parts of all scattering states

$$\Psi^{sn}(\vec{r},k) \equiv \Psi^{sn}(\vec{r},E = E_{sn}(k)) \tag{A2}$$

where $E_{sn}(k) = (\hbar^2/2m^*)k^2 + E_{sn}^{\perp} - eU_s$. Furthermore, $I_{s'\to s}^{out}$ is the absolute value of the current in contact s created by the out-going parts of all scattering states $\Psi^{s'n'}(\vec{r}, k')$ where s', n' and k' are arbitrary, thus including the case $s' = s$ also. From current conservation one has

$$\sum_{s'=1}^{N} I_{s\to s'}^{out} = I_s^{in}. \tag{A3}$$

From Equations (A1) and (A3) it results that

$$I_s = \sum_{s'=1}^{N} (I_{s\to s'}^{out} - I_{s'\to s}^{out}) = \sum_{s'}^{N, s'\neq s} (I_{s'\to s}^{out} - I_{s\to s'}^{out}). \tag{A4}$$

In Figure A1 the direction of the current contributions is given by the arrows for positive charge carriers. For n-type conduction the arrows have to be reversed.

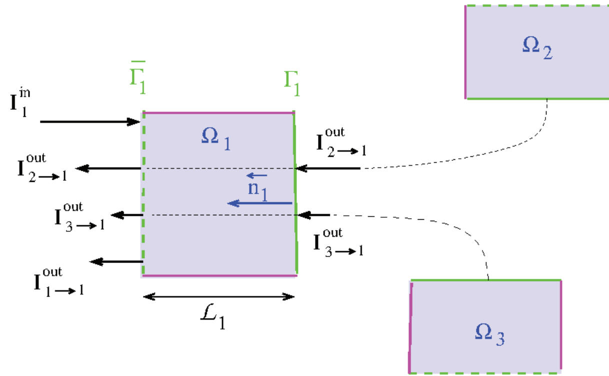

Figure A1. The formulation of Equation (A1) for contact $s = 1$ in a $N = 3$-terminal device at $\bar{\Gamma}_1$ (see also Figure 1). The current component directed in $-\vec{n}_1$-direction is I_1^{in}. The three current components in $\vec{n}_1$-direction are $I_{1\to 1}^{out}$, $I_{1\to 2}^{out}$, and $I_{1\to 3}^{out}$. Because there are no scattering processes in Ω_1 it holds that $I_{1\to 2}^{out}$ and $I_{1\to 3}^{out}$ are the same in Γ_1 and $\bar{\Gamma}_1$ (see dashed horizontal lines).

Appendix A.1. Current Contribution of a Single Scattering State

We decompose

$$I_{s\to s'}^{out} = \sum_{nk} I_{s\to s'}^{out,n}(k) \tag{A5}$$

where $I_{s\to s'}^{out,n}(k)$ is the absolute value of the current in contact s' created by the out-going part of the scattering state $\Psi^{sn}(\vec{r}, k)$ given by

$$I_{s\to s'}^{out,n}(k) = f_{FD}(E_{sn}(k) - \mu_s) \int_{\Gamma_{s'}} d\Gamma_{s'} j^{out}(\vec{r}). \tag{A6}$$

Here for $\vec{r} \in \Omega_{s'}$

$$j^{out}(\vec{r}) = \vec{n}_{s'}\vec{j}(\vec{r}) \tag{A7}$$

with

$$\vec{j}(\vec{r}) = \frac{e\hbar}{2m^* i} |\mathcal{N}|^2 \left[\Psi^{sn}(\vec{r}, k)^* \nabla \Psi^{sn}(\vec{r}, k) - \Psi^{sn}(\vec{r}, k) \nabla \Psi^{sn}(\vec{r}, k)^*\right] \tag{A8}$$

since from Equation (A4) the case $s = s'$ can be excluded. In Equation (A8) $\mathcal{N}$ is the continuum normalization constant to be constructed in Equation (A17). The issue of the k-summation in Equation (A5) is addressed in Section A.2. From Equation (4) we have for $\vec{r} \in \Omega_{s'}$

$$\Psi^{sn}(\vec{r},k) = \sum_{n'} S_{s'n',sn} \exp\left(ik_{s'n'}z_{s'}\right)\Phi_{s'n'}(x_{s'},y_{s'}) \tag{A9}$$

and

$$\vec{n}_{s'}\nabla\Psi^{sn}(\vec{r},k) = \frac{\partial}{\partial z_{s'}}\Psi^{sn}(\vec{r},k) = \sum_{n'} S_{s'n',sn} ik_{s'n'} \exp\left(ik_{s'n'}z_{s'}\right)\Phi_{s'n'}(x_{s'},y_{s'}) \tag{A10}$$

where

$$k_{s'n'} = \hbar^{-1}\sqrt{2m^*(E_{sn}(k) - E^{\perp}_{s'n'} + eU_{s'})}. \tag{A11}$$

The area integration in Equation (A6) leads to

$$I^{out,n}_{s\to s'}(k) = \frac{e\hbar}{m^*}|\mathcal{N}|^2 f_{FD}(E_{sn}(k) - \mu_s) \sum_{n'}^{\text{prop}} k_{s'n'}|S_{s'n',sn}|^2 \tag{A12}$$

where the index prop restricts the summation to propagating waves with real, positive $k_{s'n'}$.

Appendix A.2. Summation Over Scattering States

To calculate $I^{out}_{s\to s'}$ according to Equation (A5) one sums Equation (A12) over all scattering states, i. e. over all n and k, according to their occupation in the form

$$I^{out}_{s\to s'} = \sum_n \sum_j D_k \Delta k I^{out,n}_{s\to s'}(k) \to D_k \sum_n \int_0^{\infty} dk I^{out,n}_{s\to s'}(k), \tag{A13}$$

with the discretization

$$k \to k_j = j\Delta k > 0 \quad \text{for} \quad j \in \mathbb{N}^0. \tag{A14}$$

Here the constant D_k is the density of scattering states in k-space which we will address in Equation (A16). The width of the k-intervals Δk is assumed to be small so that the k-integration can be replaced by a Riemann sum. As usual, one determines D_k and $\mathcal{N}$ by assigning to each normalized propagating solution of the Schrödinger equation in Ω_s of the form

$$\mathcal{N} e^{ikz}\Phi_{sn}(y,z) \tag{A15}$$

the normalized scattering state $\mathcal{N}\Psi^{sn}(\vec{r},k)$ which has the in-going part in Equation (A15). As is well-known, this corresponds to the expectation that each in-coming particle is represented by a wave-package. When the particle is located deeply in the interior of Ω_s it does not 'feel' the quantum system and it can be equivalently represented by a superposition of the plane waves in Equation (A15) or the in-going part of the normalized scattering states $\mathcal{N}\Psi^{sn}(\vec{r},k)$. The plane waves solutions Equation (A15) can now be counted and normalized introducing artificial boundary conditions in Ω_s in the interval $0 \le z_s < \mathcal{L}_s$ (see Figure A1) so that

$$k_j = j\frac{2\pi}{\mathcal{L}_s} \Rightarrow D_k = \frac{2}{2\pi/\mathcal{L}_s} \tag{A16}$$

where in the last step we included a simple spin-degeneracy factor of two. The normalization then follows from

$$1 = |\mathcal{N}|^2 \int_0^{\mathcal{L}_s} dz |e^{ikz}|^2 \Rightarrow \mathcal{N} = \frac{1}{\sqrt{\mathcal{L}_s}} \tag{A17}$$

Upon insertion in Equation (A13) one finds with $|\mathcal{N}|^2 D_k = 1/\pi$

$$I^{out}_{s\to s'} = \frac{e\hbar}{m^*}\frac{1}{\pi}\sum_{nn'}^{\text{prop}}\int_0^\infty dk f[E_{sn}(k)-\mu_s]k_{s'n'}(k)|S_{s'n',sn}(E_{sn}(k))|^2. \tag{A18}$$

Substituting further

$$E = E_{sn}(k) = (\hbar^2/2m^*)k^2 + E^\perp_{sn} - eU_s \tag{A19}$$

so that

$$k = \sqrt{\frac{2m^*}{\hbar^2}}\left(E_{sn}(k) - E^\perp_{sn} + eU_s\right)^{1/2} \Rightarrow \frac{dk}{dE} = \sqrt{\frac{m^*}{2\hbar^2}}\left(E_{sn}(k) - E^\perp_{sn} + eU_s\right)^{-1/2} = \frac{m^*}{\hbar^2}k(E)^{-1}. \tag{A20}$$

With $dk \to (dk/dE)dE$ one obtains from Equation (A18)

$$\begin{aligned}
I^{out}_{s\to s'} &= \frac{1}{\pi}\frac{e\hbar}{m^*}\frac{m^*}{\hbar^2}\sum_n^{prop}\int_{E^n_\perp - eU_s}^\infty dE\sum_{n'}^{\text{prop}} f(E-\mu_s)k_{s'n'}(E)|S_{s'n',sn}(E)|^2 k_{sn}(E)^{-1} \\
&= \frac{2e}{h}\sum_n\int_{-\infty}^\infty dE\Theta(E-E^\perp_{sn}+eU_s)\sum_{n'} f(E-\mu_s)k_{s'n'}(E)|S_{s'n',sn}(E)|^2 k_{sn}(E)^{-1}\Theta(E-E^\perp_{s'n'}+eU_{s'}) \\
&= \frac{2e}{h}\int_{-\infty}^\infty dE f(E-\mu_s)\sum_{nn'}\Theta(E-E^\perp_{sn}+eU_s)\Theta(E-E^\perp_{s'n'}+eU_{s'})k_{s'n'}(E)|S_{s'n',sn}(E)|^2 k_{sn}(E)^{-1} \\
&= \frac{2e}{h}\int_{-\infty}^\infty dE f(E-\mu_s)T_{s's}(E)
\end{aligned} \tag{A21}$$

with the current transmission sum

$$\begin{aligned}
T_{s's}(E) &= \sum_{nn'}\Theta(E-E^\perp_{sn}+eU_s)\Theta(E-E^\perp_{s'n'}+eU_{s'})k_{s'n'}(E)|S_{s'n',sn}(E)|^2 k_{sn}(E)^{-1} \\
&= \sum_{nn'}\Theta(E-E^\perp_{sn}+eU_s)\Theta(E-E^\perp_{s'n'}+eU_{s'})|\tilde{S}_{s'n',sn}(E)|^2 = T_{ss'}(E).
\end{aligned} \tag{A22}$$

The symmetry relation $\tilde{S}_{s'n',sn} = \tilde{S}_{sn,s'n'}$ is shown in Equation (31). Because $T_{s's} = T_{ss'}$ one finds from Equation (A21) from

$$I_s = (I^{out}_{s\to s'} - I^{out}_{s'\to s}) = \frac{2e}{h}\int_{-\infty}^\infty dE[f(E-\mu_s) - f(E-\mu'_s])T_{s's}(E). \tag{A23}$$

Appendix B. Properties of the Wigner–Eisenbud Problem

(1) *Hermiticity:*
We take two functions $\psi_1(\vec{r})$ and $\psi_2(\vec{r})$ obeying the Wigner–Eisenbud boundary conditions Equations (15) and (16), i. e., with the Neumann boundary conditions $[\partial\psi/\partial\vec{n}_s](\vec{r}\in\Gamma_s) = 0$ and Dirichlet boundary condition $\psi(\vec{r}\in\partial\Omega_0) = 0$. From second Green's theorem it follows directly that

$$\int_{\Omega_0} dv\,(\psi_1^*\Delta\psi_2 - \psi_2\Delta\psi_1^*) = \sum_s\int_{\Gamma_s} d\Gamma_s\vec{n}_s\,(\psi_1^*\nabla\psi_2 - \psi_2\nabla\psi_1^*) = 0. \tag{A24}$$

As desired, one immediately obtains the hermicity condition

$$\int_{\Omega_0} dv\,[\psi_1^*(H\psi_2) - \psi_2(H\psi_1)^*] = -\frac{\hbar^2}{2m}\int_{\Omega_0} dv\,(\psi_1^*\Delta\psi_2 - \psi_2\Delta\psi_1^*) = 0. \tag{A25}$$

(2) *The Wigner–Eisenbud energies are real:*
The Wigner–Eisenbud functions are the eigenfunctions of H,

$$[H - \mathcal{E}_l]\chi_l = 0 \tag{A26}$$

obeying Wigner–Eisenbud conditions. Setting in Equation (A25) $\psi_1 = \psi_2 = \chi_l$ it follows that

$$0 = \int_{\Omega_0} dv \chi_l^* H \chi_l - \int_{\Omega_0} dv \chi_l \, [H\chi_l]^* = [\mathcal{E}_l - \mathcal{E}_l^*] \underbrace{\int_{\Omega_0} dv \chi_l^* \chi_l}_{\in \mathbb{R}^+} . \tag{A27}$$

(3) *The Wigner–Eisenbud functions can be chosen real:*
Since the $\mathcal{E}_l$ are real the complex conjugate of Equation (A26) is given by

$$[H - \mathcal{E}_l]\chi_l^* = 0. \tag{A28}$$

From the sum of Equations (A26) and (A28) one obtains

$$[H - \mathcal{E}_l](\chi_l + \chi_l^*) = 0 \Rightarrow [H - \mathcal{E}_l]Re(\chi_l) = 0 \tag{A29}$$

and from the difference

$$[H - \mathcal{E}_l](\chi_l - \chi_l^*) = 0 \Rightarrow [H - \mathcal{E}_l]Im(\chi_l) = 0. \tag{A30}$$

Therefore, if a complex function χ_l is a solution of Equation (A26) then χ_l^* is a solution too and one can choose instead of χ_l two real solutions $Re(\chi_l)$ and $Im(\chi_l)$.

(4) *The Wigner–Eisenbud functions are orthogonal:*
For two Wigner–Eisenbud functions with different energies $\mathcal{E}_l \neq \mathcal{E}_{l'}$ we write

$$[H - \mathcal{E}_{l'}]\chi_{l'} = 0. \tag{A31}$$

Setting in Equation (A25) $\psi_1^* = \psi_1 = \chi_{l'}$ and $\psi_2^* = \psi_2 = \chi_l$

$$0 = \int_{\Omega_0} dv \, [\chi_{l'}(H\chi_l) - \chi_l(H\chi_{l'})^*] = \underbrace{(\mathcal{E}_l - \mathcal{E}_{l'})}_{\neq 0} \int_{\Omega_0} dv \chi_{l'} \chi_l. \tag{A32}$$

For degenerate Wigner–Eisenbud functions $\mathcal{E}_l = \mathcal{E}_{l'}$ two orthogonal linear combinations can be constructed with standard methods.

(5) *Completeness:*
As described in (1) the operator H is hermitic, it is second order in the derivatives and linear. Then the set of its eigenfunctions χ_l, the Wigner–Eisenbud functions, is complete. Thus, with (3) and (4) the χ_l can be chosen as a complete, real, orthonormal function system.

Appendix C. Verification of Equation (49)

We verify this equation explicitly:

$$
\begin{aligned}
\left[(1-i\Omega)\left(\frac{1}{1-i\Omega}\right)\right]_{sns'n'} &= \sum_{s''n''}(1-i\Omega)_{sn,s''n''}\left(\frac{1}{1-i\Omega}\right)_{s''n'',s'n'} \\
&= \sum_{s''n''k'}(\delta_{sn,s''n''}-i\Omega_{sn,s''n''})c_{k's''n''}c_{k's'n'}\left(\frac{1}{1-i\Omega^{k'}}\right)_{s''s'} \\
&= \sum_{s''n''kk'}(c_{ksn}c_{ksn''}\delta_{s,s''}-ic_{ksn}c_{ks''n''}\Omega^{k}_{ss''})c_{k',s''n''}c_{k',s'n'}\left(\frac{1}{1-i\Omega^{k'}}\right)_{s''s'} \\
&= \sum_{s''n''kk'}c_{ksn}\underbrace{c_{ks''n''}c_{k's''n''}}_{\delta_{kk'}}c_{k',s'n'}(\delta_{s,s''}-i\Omega^{k}_{ss''})\left(\frac{1}{1-i\Omega^{k'}}\right)_{s''s'} \\
&= \sum_{s''kk'}c_{ksn}\delta_{kk'}c_{k's'n'}(1-i\Omega^{k})_{ss''}\left(\frac{1}{1-i\Omega^{k'}}\right)_{s''s'} \\
&= \sum_{s''k}c_{ksn}c_{ks'n'}(1-i\Omega^{k})_{ss''}\left(\frac{1}{1-i\Omega^{k}}\right)_{s''s'} = \delta_{ss'}\sum_{k}\underbrace{c_{ksn}c_{ksn'}}_{\delta_{nn'}} = \delta_{ss'}\delta_{nn'}.
\end{aligned}
\tag{A33}
$$

Here we applied the relations in under-braces

$$\sum_{n}c_{ksn}c_{k'sn} = \delta_{kk'} \qquad \text{and} \qquad \sum_{k}c_{ksn}c_{ksn'} = \delta_{nn'}. \tag{A34}$$

To derive the first relation we formulate the completeness of the Φ_{sn} and the ϕ_k writing

$$\sum_{n}\Phi_{sn}(y,z)\Phi_{sn}(y',z') = \delta(x-x')\delta(y-y') = \sum_{k}\phi_k(y,z)\phi_k(y',z'). \tag{A35}$$

Projection onto $\phi_{k''}(y,z)$ and $\phi_{k'}(y',z')$ yields immediately

$$\sum_{n}c_{k''sn}c_{k'sn} = \delta_{k'',k'}. \tag{A36}$$

The second relation in Equation (A34) is derived by inserting in the orthogonality relation

$$\int_0^D dy\int_0^W dz\Phi_{sn}(y,z)\Phi_{sn'}(y,z) = \delta_{nn'} \tag{A37}$$

the expansion $\Phi_{sn}(y,z) = \sum_k c_{ksn}\phi_k(y,z)$. It is seen that

$$\delta_{nn'} = \sum_{kk'}c_{ksn}c_{k'sn'}\int_0^D dy\int_0^W dz\phi_k(y,z)\phi_{k'}(y,z) = \sum_{kk'}c_{ksn}c_{k'sn'}\delta_{kk'} = \sum_{k}c_{ksn}c_{ksn'}. \tag{A38}$$

Appendix D. R-matrix Theory in One Dimension

We define the Wigner–Eisenbud functions in one dimension as the solutions of the hermitic eigenvalue problem

$$\left[-\frac{\hbar^2}{2m^*}\frac{d^2}{dx^2}+V^{ef}(x)-\mathcal{E}^{ef}_{\lambda}\right]\chi_\lambda(x) = 0 \tag{A39}$$

with the effective 1d-scattering potential given in Equation (55) and von-Neumann boundary conditions

$$\chi'_\lambda(0) = \chi'_\lambda(L) = 0. \tag{A40}$$

A comparison with Equation (40) yields identical eigenfunctions χ_λ and eigenenergies shifted by E_k^T,

$$\mathcal{E}_\lambda^{ef} = \mathcal{E}_\lambda^L + E_k^T. \tag{A41}$$

The χ_λ constitute a complete orthonormal system in which the scattering states ψ^{ef} in Equation (54) can be expanded in the domain $x \in [0, L]$. One has

$$\psi^{ef}(x) \equiv \psi(x) = \sum_{\lambda=1}^{\infty} a_\lambda \chi_\lambda(x), \tag{A42}$$

where

$$a_\lambda = \int_0^L \psi(x)\chi_\lambda(x)dx. \tag{A43}$$

The left-multiplication of Equation (54) with $\chi_\lambda(x)$ and left-multiplication of Equation (A39) with $\psi(x)$ leads after integration to

$$-\frac{\hbar^2}{2m}\int_0^L dx \left[\chi_\lambda(x)\frac{d^2}{dx^2}\psi(x) - \psi(x)\frac{d^2}{dx^2}\chi_\lambda(x)\right] = \left(E - \mathcal{E}_\lambda^L - E_k^T\right)\underbrace{\int_0^L dx\, \psi(x)\chi_l(x)}_{a_\lambda}.$$

Partial integration on the left side and application of the von-Neumann boundary conditions Equation (A40) leads to

$$-\frac{\hbar^2}{2m}\left[\chi_\lambda(L)\frac{d\psi}{dx}(L) - \chi_\lambda(0)\frac{d\psi}{dx}(0)\right] = \left(E - \mathcal{E}_\lambda^L - E_k^T\right)a_\lambda. \tag{A44}$$

Following Equation (19) we introduce the outward directed normal derivatives

$$\psi^S(0) = -\frac{1}{m^*}\frac{d\psi}{dx}\Big|_{x=0} \quad \text{as well as} \quad \psi^S(L) = \frac{1}{m^*}\frac{d\psi}{dx}\Big|_L \tag{A45}$$

and obtain

$$-\frac{\hbar^2}{2}\frac{\chi_\lambda(0)\psi^S(0) + \chi_\lambda(L)\psi^S(L)}{E - \mathcal{E}_\lambda^L - E_k^T} = a_\lambda. \tag{A46}$$

Upon multiplication with $\chi_\lambda(x)$ and summation λ one finds

$$\psi(x) = \sum_{\lambda=1}^{\infty} a_\lambda(E)\chi_\lambda(x) = R^k(x,0)\psi_S(0) + R^k(x,L)\psi_S(L), \tag{A47}$$

with

$$R^k(x,x') = -\frac{\hbar^2}{2}\sum_{\lambda=1}^{\infty}\frac{\chi_\lambda(x)\chi_\lambda(x')}{E - \mathcal{E}_\lambda^L - E_k^T}. \tag{A48}$$

From evaluation of this equation for $x_1 = 0$ and $x_2 = L$ one finds in correspondence to Equation (26)

$$\psi(x_s) = \sum_{s'} R_{ss'}^k \psi^S(x_s) \Rightarrow \vec{\psi} = R^k \vec{\psi}^S, \tag{A49}$$

where we define the 2×2 R-matrix

$$R_{ss'}^k = -\frac{\hbar^2}{2m^*}\sum_{\lambda=1}^{\infty}\frac{\chi_\lambda(x_s)\chi_\lambda(x_{s'})}{E - \mathcal{E}_\lambda^L - E_k^T} \tag{A50}$$

and the two-component vectors

$$(\vec{\psi})_s = \psi(x_s) \quad \text{and} \quad (\vec{\psi}^S)_s = \psi^S(x_s). \tag{A51}$$

A comparison of Equation (A50) with Equation (48) yields

$$\Omega^k_{ss'} = (k^{ef}_s)^{1/2}(k^{ef}_{s'})^{1/2}R^k_{ss'}. \tag{A52}$$

We now proceed as in Equation (10) and decompose the general solution of the wave function in the contacts in an in-going part and an out-going part, $\psi(x) = \psi^{in}(x) + \psi^{out}(x)$, where

$$\psi^{in}(x) = \begin{cases} \psi^{in}_1 e^{ik^{ef}_1 x} & \text{for } x < 0 \\ \psi^{in}_2 e^{-ik^{ef}_2 (x-L)} & \text{for } x > L \end{cases} \tag{A53}$$

and

$$\psi^{out}(x) = \begin{cases} \psi^{out}_1 e^{-ik^{ef}_1 x} & \text{for } x < 0 \\ \psi^{out}_2 e^{ik^{ef}_2 (x-L)} & \text{for } x > L. \end{cases} \tag{A54}$$

As in Equation (11), the S-matrix is the linear mapping of the in-going part onto the out-going part

$$\vec{\psi}^{out} = S^k \vec{\psi}^{in} \tag{A55}$$

with the two-component vector

$$(\vec{\psi}^{in})_s = \psi^{in}_s \quad \text{and} \quad (\vec{\psi}^{out})_s = \psi^{out}_s. \tag{A56}$$

The source-incident scattering states are associated with $\psi^{in}_1 = 1$ and $\psi^{in}_2 = 0$, $\psi^{out}_1 = S^k_{11} = r^k_1$ and $\psi^{out}_2 = S^k_{21} = t^k_1$. The drain-incident scattering states are associated with $\psi^{in}_1 = 0$ and $\psi^{in}_2 = 1$, $\psi^{out}_1 = S^k_{12} = t^k_2$ and $\psi^{out}_2 = S^k_{22} = r^k_2$. One finds the relation between S-matrix and the transmission- and reflection coefficients

$$\begin{pmatrix} S^k_{11} & S^k_{12} \\ S^k_{21} & S^k_{22} \end{pmatrix} = \begin{pmatrix} r^k_1 & t^k_2 \\ t^k_1 & r^k_2 \end{pmatrix}. \tag{A57}$$

Using Equations (A53) and (A54) it results for $x \leq 0$

$$\frac{d\psi^{in}(x)}{dx} = ik^{ef}_1 \psi^{in}(x) \quad \text{and} \quad \frac{d\psi^{out}(x)}{dx} = -ik^{ef}_1 \psi^{out}(x), \tag{A58}$$

and for $x \geq L$

$$\frac{d\psi^{in}(x)}{dx} = -ik^{ef}_2 \psi^{ein}(x) \quad \text{and} \quad \frac{d\psi^{out}(x)}{dx} = ik^{ef}_2 \psi^{out}(x). \tag{A59}$$

It follows that

$$\vec{\psi}_S = ik^{ef}\vec{\psi}^{out} - ik^{ef}\vec{\psi}^{in}, \tag{A60}$$

with the diagonal wave number matrix $(k^{ef})_{ss'} = \delta_{ss'}k^{ef}_s$. From Equation (A49), $\vec{\psi} = \vec{\psi}^{in} + \vec{\psi}^{out}$, and Equation (A60) it follows that

$$\left(iR^k k^{ef} - 1\right)\vec{\psi}^{out} = \left(iR^k k^{ef} + 1\right)\vec{\psi}^{in}. \tag{A61}$$

A comparison with Equation (A55) leads to

$$S^k = -\frac{1 + iR^k k^{ef}}{1 - iR^k k^{ef}}. \tag{A62}$$

For the current matrix we find with Equation (A52)

$$\tilde{S}^k = (k^{ef})^{1/2} S^k (k^{ef})^{-1/2} = \frac{1 + i(k^{ef})^{1/2} R^k (k^{ef})^{1/2}}{1 - i(k^{ef})^{1/2} R^k (k^{ef})^{1/2}} - \frac{1 + i\Omega^k}{1 - i\Omega^k} = \frac{-2 + 1 - i\Omega^k}{1 - i\Omega^k} = 1 - \frac{2}{1 - i\Omega^k}. \tag{A63}$$

It is now decisive that with the definition of the R^k in Equation (A50) it results that

$$(\Omega^k)_{ss'} = (k_s^{ef})^{1/2} R^k_{ss'} (k_{s'}^{ef})^{1/2} = -\frac{\hbar^2}{2m^*} (k_s^{ef})^{1/2} (k_{s'}^{ef})^{1/2} \sum_{\lambda=1}^{\infty} \frac{\chi_\lambda(x_s)\chi_\lambda(x_{s'})}{E - \mathcal{E}_\lambda^L - E_k^T} \tag{A64}$$

identical with Equation (48). From Equation (A57) one has

$$\tilde{S}^k_{21} = \sqrt{k_1^{ef} k_2^{ef}}\, t_1^k = -\left(\frac{2}{1 - i\Omega^k}\right)_{21}. \tag{A65}$$

In Section 6, we identified ψ^{ef} with the source-incident scattering state characterized through the asymptotic in Equations (76) and (77). Therefore we identify $t_1^k = t^{ef}$ and Equation (A70) becomes Equation (53).

In Equation (65) we define for the planar system in Section 7

$$\bar{\Omega}^{k_y}_{s's}(E^{xy}) = -\frac{\hbar^2}{2m^*} (\bar{k}_{s'}^{ef})^{1/2} (\bar{k}_s^{ef})^{1/2} \sum_{\lambda} \frac{\chi_\lambda(x_s)\chi_\lambda(x_{s'})}{E^{xy} - \mathcal{E}_\lambda^L - E_{k_y}^{Ty}} \equiv \bar{\Omega}^{k_y}_{s's}(E^{xy}) \tag{A66}$$

with the conserved energy in the xy-plane

$$E^{xy} = E - \frac{\hbar^2}{2m^*} \left(\frac{k_z \pi}{W}\right)^2 \tag{A67}$$

and $k_{sn}(E) = \bar{k}_s^{ef}(E^{xy})$. Comparing Equation (A66) with Equation (A64) one can adopt the result Equation (A70) for the planar system if one identifies $k \leftrightarrow k_y$ $E \leftrightarrow E^{xy}$, $k_s^{ef}(E) \leftrightarrow \bar{k}_s^{ef}(E^{xy})$, and $E_k^T \leftrightarrow E_{k_y}^{Ty}$. This way an effective one-dimensional scattering problem associated with the 1d-Schrödinger equation

$$\left[-\frac{\hbar^2}{2m^*}\frac{d^2}{dx^2} + V^{ef}(x) - E^{xy}\right] \psi^{ef}(x) = 0 \tag{A68}$$

results with the effective scattering potential in the limit $W \to 0$ given by

$$V^{ef}(x) = \begin{cases} 0 & \text{for } x < 0 \\ E_{k_y}^{Ty} + V_L(x) & \text{for } 0 \leq x \leq L \\ -eU_D & \text{for } x > L. \end{cases} \tag{A69}$$

The transmission coefficients $\bar{t}_1^{k_y}$ of the source-incident scattering functions of Equation (A68) yield

$$\bar{t}_1^{k_y} = \bar{S}^{k_y}_{21} = \sqrt{k_1^{ef} k_2^{ef}}\, \bar{t}_1^{k_y} = -\left(\frac{2}{1 - i\bar{\Omega}^{k_y}}\right)_{21}. \tag{A70}$$

Appendix E. Numerical Evaluation of the Transmission Coefficients in One Dimension

In the finite difference method, the one-dimensional Schrödinger equation

$$\left[-\frac{\hbar^2}{2m}\frac{d^2}{dx^2}+V(x)-E\right]\psi(x,E)=0 \tag{A71}$$

becomes

$$\psi_{n+1}+\psi_{n-1}-2\psi_n+\frac{2m\Delta^2}{\hbar^2}(E-V_n)\psi_n=0. \tag{A72}$$

Here we discretize the real axis in the form $x \to x_n = n\Delta$ with $\Delta \to 0$. Requiring $L = N\Delta$ one has $N+1$ grid points in the scattering area $0 \le x \le L$. Furthermore, we introduce $V(x) \to V(x_n) \equiv V_n$, $\psi(x,E) \to \psi(x_n,E) \equiv \psi_n$, and $d^2/(dx^2) \to (\psi_{n+1}+\psi_{n-1}-2\psi_n)/\Delta^2$. In view of Equation (81) we assume the asymptotics $V_{n<0}=0$ (source) and $V_{n>N}=-eU_D$ (drain). The source-incident scattering states then follow the asymptotic

$$\psi_n = \begin{cases} r\exp(-ik_1 n\Delta)+\exp(ik_1 n\Delta) & \text{for } n<0 \\ t\exp(ik_2(n-N)\Delta) & \text{for } n>N \end{cases} \tag{A73}$$

with $k_s=\sqrt{2m(E-V_s)}/\hbar^2$ with $V_1=0$ and $V_2=-eU_D$. To construct the source-incident scattering states we transform Equation (A72) for $\phi_n=\psi_n/t$ into a downward recursion

$$\phi_{n-1}=-\phi_{n+1}+\left[2+\frac{2m\Delta^2}{\hbar^2}(V_n-E)\right]\phi_n. \tag{A74}$$

For ϕ_n one has

$$\phi_n = \begin{cases} \frac{r}{t}\exp(-ik_1 Ln/N)+\frac{1}{t}\exp(ik_1 Ln/N) & \text{for } n<0 \\ \exp(ik_2 L(n-N)/N) & \text{for } n>N. \end{cases} \tag{A75}$$

with the known asymptotic on the drain side

$$\phi_{n>N}=\exp(ik_2 L(n-N)/N). \tag{A76}$$

The the downward recursion Equation (A74) is started with, for example,

$$\phi_{N+2}=\exp(2ik_2 L/N) \quad \text{and} \quad \phi_{N+3}=\exp(3ik_2 L/N) \tag{A77}$$

to construct ϕ_n in the entire range. Especially one obtains

$$\phi_{-2}=\frac{1}{t}\exp(-2ik_1 L/N)+\frac{r}{t}\exp(2ik_1 L/N) \tag{A78}$$

and

$$\phi_{-3}=\frac{1}{t}\exp(-3ik_1 L/N)+\frac{r}{t}\exp(3ik_1 L/N). \tag{A79}$$

The Equations (A78) and (A79) represent two linear equations for the two unknown t and r. One finds

$$t=\frac{\exp(-3ik_1 L/N)-\exp(-ik_1 L/N)}{\phi_{-3}-\exp(ik_1 L/N)\phi_{-2}}. \tag{A80}$$

Appendix F. Derivation of the Supply Function

Starting from Equation (51) it follows that

$$
\begin{aligned}
I_D &= \frac{2e}{h}\sum_{nn'kk'}\int_{-\infty}^{\infty} dE\,[f(E-\mu)-f(E-\mu+eU_D)]\,c_{ksn}c_{ks'n'}c_{k'sn}c_{k's'n'} \\
&\quad \times \left(\frac{2}{1-i\Omega^{k}}\right)_{ss'}\left(\frac{2}{1-i\Omega^{k'}}\right)^{*}_{ss'}\Theta\left[E-E^{\perp}_{sn}\right]\Theta\left[E-E^{\perp}_{s'n'}+eU_D\right] \\
&= \frac{2e}{h}\sum_{n_y n_z n'_y n'_z k_y k_z k'_y k'_z}\int_{-\infty}^{\infty} dE\,[f(E-\mu)-f(E-\mu+eU_D)]\,\bar{c}_{k_y s n_y}\delta_{n_z k_z}\bar{c}_{k_y s' n'_y}\delta_{n_z k'_z}\bar{c}_{k'_y s n_y}\delta_{n'_z k_z}\bar{c}_{k'_y s' n'_y}\delta_{n'_z k'_z} \\
&\quad \times \left(\frac{2}{1-i\Omega^{k_y k_z}}\right)_{ss'}\left(\frac{2}{1-i\Omega^{k'_y k'_z}}\right)^{*}_{ss'}\Theta\left[E-E^{\perp}_{s n_y n_z}\right]\Theta\left[E-E^{\perp}_{s' n'_y n'_z}+eU_D\right] \\
&= \frac{2e}{h}\sum_{n_y n_z n'_y k_y k'_y}\int_{-\infty}^{\infty} dE\,[f(E-\mu)-f(E-\mu+eU_D)]\,\bar{c}_{k_y s n_y}\bar{c}_{k_y s' n'_y}\bar{c}_{k'_y s n_y}\bar{c}_{k'_y s' n'_y} \\
&\quad \times \left(\frac{2}{1-i\Omega^{k_y n_z}}\right)_{ss'}\left(\frac{2}{1-i\Omega^{k'_y n_z}}\right)^{*}_{ss'}\Theta\left[E-E^{\perp}_{s n_y n_z}\right]\Theta\left[E-E^{\perp}_{s' n'_y n_z}+eU_D\right] \qquad \text{(A81)} \\
&= \frac{2e}{h}\sum_{n_z n_y n'_y k_y k'_y}\int_{-\infty}^{\infty} dE^{xy}\left[f\left(E^{xy}+\frac{\hbar^2}{2m^*}\left(\frac{n_z\pi}{W}\right)^2-\mu\right)-f\left(E^{xy}+\frac{\hbar^2}{2m^*}\left(\frac{n_z\pi}{W}\right)^2-\mu+eU_D\right)\right]\bar{c}_{k_y s n_y}\bar{c}_{k_y s' n'_y}\bar{c}_{k'_y s n_y}\bar{c}_{k'_y s' n'_y} \\
&\quad \times \left[\frac{2}{1-i\bar{\Omega}^{k_y}(E^{xy})}\right]_{ss'}\left[\frac{2}{1-i\bar{\Omega}^{k'_y}(E^{xy})}\right]^{*}_{ss'}\Theta\left[E^{xy}-E^{\perp y}_{s n_y}\right]\Theta\left[E^{xy}-E^{\perp y}_{s' n'_y}+eU_D\right] \qquad \text{(A82)} \\
&= \frac{2e}{h}\sum_{k_y k'_y}\int_{-\infty}^{\infty} dE^{xy}\bar{C}_{k_y k'_y}(E^{xy})\,[S(E^{xy}-\mu)-S(E^{xy}-\mu+eU_D)]\left[\frac{2}{1-i\bar{\Omega}^{k_y}(E^{xy})}\right]_{ss'}\left[\frac{2}{1-i\bar{\Omega}^{k'_y}(E^{xy})}\right]^{*}_{ss'} \qquad \text{(A83)}
\end{aligned}
$$

with

$$C_{k_y k'_y}(E^{xy}) = \sum_{n_y n'_y}\bar{c}_{k_y s n_y}\bar{c}_{k_y s' n'_y}\bar{c}_{k'_y s n_y}\bar{c}_{k'_y s' n'_y}\Theta\left[E^{xy}-E^{\perp y}_{s n_y}\right]\Theta\left[E^{xy}-E^{\perp y}_{s' n'_y}+eU_D\right] \qquad \text{(A84)}$$

and

$$S(\alpha) = \sum_{n_z} f\left[\alpha+\frac{\hbar^2}{2m^*}\left(\frac{n_z\pi}{W}\right)^2\right]. \qquad \text{(A85)}$$

Going over from Equation (A81) to Equation (A82) we made use of Equation (65) with $k_z = n_z$.

References

1. Nemnes, G.A.; Wulf, U.; Racec, P.N. Nano-transistors in the Landauer-Büttiker formalism. *J. Appl. Phys.* **2004**, *96*, 596. [CrossRef]
2. Nemnes, G.A.; Wulf, U.; Racec, P.N. Nonlinear I-V characteristics of nanotransistors in the Landauer-Büttiker formalism. *J. Appl. Phys.* **2005**, *98*, 84308. [CrossRef]
3. Wulf, U.; Richter, H. Scale-invariant drain current in nano-FETs. *J. Nano Res.* **2010**, *10*, 49–61. [CrossRef]
4. Wulf, U.; Richter, H. Scaling in quantum transport in silicon nano-transistors. *Solid State Phenom.* **2010**, *10*, 156–158. [CrossRef]
5. Wulf, U.; Richter, H. Scaling properties of ballistic nano-transistors. *Nanoscale Res. Lett.* **2011**, *6*, 365. [CrossRef]
6. Wulf, U.; Krahlisch, M.; Kučera, J.; Richter, H.; Höntschel, J. A quantitative model for quantum transport in nano-transistors. *Nanosyst. Phys. Chem. Math.* **2013**, *4*, 800–809.
7. Wulf, U.; Kučera, J.; Richter, H.; Wiatr, M.; Höntschel, J. Characterization of nanotransistors in a semiempirical model. *Thin Solid Films* **2016**, *613*, 6–10. [CrossRef]
8. Wulf, U.; Kučera, J.; Richter, H.; Horstmann, M.; Wiatr, M.; Höntschel, J. Channel Engineering for Nanotransistors in a Semiempirical Quantum Transport Model. *Mathematics* **2017**, *5*, 68. [CrossRef]
9. Frenkel, J. On the electrical resistance of contacts between solid conductors. *Phys. Rev.* **1930**, *36*, 1604. [CrossRef]
10. Ehrenberg, W.; Hönl, H. Zur Theorie des elektrischen Kontakte. *Zeitschrift für Phys.* **1931**, *68*, 289. [CrossRef]

11. Landauer, R. Spatial variation of currents and fields due to localized scatterers in metallic conduction. *IBM J. Res. Develop.* **1957**, *1*, 223. [CrossRef]
12. Landauer, R. Electrical transport in open and closed systems. *Z. Phys. B* **1987**, *68*, 217. [CrossRef]
13. Tsu, R.; Esaki, L. Tunneling in a finite superlattice. *Appl. Phys. Lett.* **1973**, *22*, 562. [CrossRef]
14. Fisher, D.S.; Lee, P.A. Relation between conductivity and transmission matrix. *Phys. Rev. B* **1981**, *23*, 6851. [CrossRef]
15. Büttiker, M.; Imry, Y.; Landauer, R.; Pinhas, S. Generalized many-channel conductance formula with application to small rings. *Phys. Rev. B* **1985**, *31*, 6207. [CrossRef]
16. Büttiker, M. Four-terminal phase-coherent conductance. *Phys. Rev. Lett.* **1986**, *57*, 1761. [CrossRef]
17. Büttiker, M. Symmetry of electrical conduction. *IBM J. Res. Dev.* **1988**, *32*, 317. [CrossRef]
18. Sharvin, D.Y.; Sharvin, Y.V. Magnetic-flux quantization in a cylindrical film of a normal metal. *JETP Lett.* **1981**, *34*, 272.
19. Roukes, M.L. Quenching of the Hall effect in a one-dimensional wire. *Phys. Rev. Lett.* **1987**, *59*, 3011. [CrossRef]
20. Baranger, H.U.; Stone, A.D. Quenching of the Hall resistance in ballistic microstructures: A collimation effect. *Phys. Rev. Lett.* **1989**, *63*, 414. [CrossRef]
21. van Wees, B.J.; van Houten, H.; Beenakker, C.W.J.; Williamson, J.G.; Kouwenhoven, L.P.; van der Marel, D.; Foxon, C.T. Quantized conductance of point contacts in a two-dimensional electron gas. *Phys. Rev. Lett.* **1988**, *60*, 848. [CrossRef]
22. Wharam, D.A.; Thornton, T.H.; Newbury, R.; Pepper, M.; Ahmed, H.; Frost, J.E.F.; Hasko, D.G.; Peacock, D.C.; Ritchie, D.A.; Jones, G.A.C. One-dimensional transport and the quantisation of the ballistic resistance. *J. Phys. C* **1988**, *21*, L209. [CrossRef]
23. Mizuta, H.; Tanoue, T. The Physics and Applications of Resonant Tunneling Diodes. In *Cambridge Studies in Semiconductor Physics and Microelectronic Engineering* 2; Cambridge University Press: Cambridge, UK, 1995.
24. Meirav, U.; Kastner, M.A.; Wind, S.J. Single-electron charging and periodic conductance resonances in GaAs nanostructures. *Phys. Rev. Lett.* **1990**, *65*, 771. [CrossRef] [PubMed]
25. Meir, Y.; Wingreen, N.S.; Lee, P.A. Transport through a strongly interacting electron system: Theory of periodic conductance oscillations. *Phys. Rev. Lett.* **1991**, *66*, 3048. [CrossRef] [PubMed]
26. Awschalom, D.D.; Loss, D.; Samarth, N. (Eds.) *Semiconductor Spintronics and Quantum Computation*; Springer: Berlin, Germany, 2002.
27. Greilich, A.; Yakovlev, D.R.; Shabev, A.; Efros, A.L.; Yugova, I.A.; Oulton, R.; Stavarche, V.; Reuter, D.; Wieck, A.; Bayer, M. Mode locking of electron spin coherences in singly charged quantum dots. *Science* **2006**, *313*, 341. [CrossRef] [PubMed]
28. Koppens, F.H.L.; Buizert, C.; Tielrooij, K.J.; Nowack, K.C.; Meunier, T.; Kouwenhoven, L.P.; Vandersypen, L.M.K. Driven coherent oscillations of a single electron spin in a quantum dot. *Nature* **2006**, *442*, 766. [CrossRef]
29. Brown, R.H.; Twiss, R.Q. A new type of interferometer for use in radio astronomy. *Philos. Mag.* **1954**, *45*, 663–682. [CrossRef]
30. Büttiker, M. Scattering theory of current and intensity noise correlations in conductors and wave guides. *Phys. Rev. B* **1992**, *46*, 12485. [CrossRef]
31. Henny, M.; Oberholzer, S.; Strunk, C.; Heinzel, T.; Ensslin, K.; Holland, M.; Schönenberger, C. The fermionic hanbury brown and twiss experiment. *Science* **1999**, *284*, 296. [CrossRef]
32. Chen, Y.; Webb, R.A. Positive Current Correlations Associated with Super-Poissonian Shot Noise. *Phys. Rev. Lett.* **2006**, *97*, 66064. [CrossRef]
33. Lane, A.M.; Thomas, R.G. R-Matrix Theory of Nuclear Reactions. *Rev. Mod. Phys.* **1958**, *30*, 257. [CrossRef]
34. Burke, P.G.; Berrington, K.A. (Eds.) *Atomic and Molecular Processes: An R-matrix Approach*; Institute of Physics Publishing: Bristol, UK, 1993.
35. Kapur, P.L.; Peierls, R. The dispersion formula for nuclear reactions. *Proc. Roy. Soc. (London)* **1938**, *A166*, 277.
36. Smrčka, L. R-matrix and the coherent transport in mesoscopic systems. *Superlattices Microstruct.* **1990**, *8*, 221. [CrossRef]
37. Wulf, U.; Kučera, J.; Racec, P.N.; Sigmund, E. Transport through quantum systems in the R-matrix formalism. *Phys. Rev. B* **1998**, *58*, 16209. [CrossRef]

38. Onac, E.; Kučera, J.; Wulf, U. Vertical magnetotransport through a quantum dot in the R-matrix formalism. *Phys. Rev. B* **2001**, *63*, 85319. [CrossRef]
39. Racec, E.R.; Wulf, U.; Racec, P.N. Fano regime of transport through open quantum dots. *Phys. Rev. B* **2010**, *82*, 85313. [CrossRef]
40. Racec, E.R.; Wulf, U. Resonant quantum transport in semiconductor nanostructures. *Phys. Rev. B* **2001**, *64*, 115318. [CrossRef]
41. Jayasekera, T.; Morrison, M.A.; Mullen, K. R-matrix theory for magnetotransport properties in semiconductor devices. *Phys. Rev. B* **2006**, *74*, 235308. [CrossRef]
42. Mil'nikov, G.; Mori, N.; Kamakura, Y.; Ezaki, T. R-matrix theory of quantum transport and recursive propagation method for device simulations. *J. Appl. Phys.* **2008**, *104*, 044506. [CrossRef]
43. Mil'nikov, G.; Mori, N.; Kamakura, Y. R-matrix method for quantum transport simulations in discrete systems. *Phys. Rev. B* **2009**, *79*. [CrossRef]
44. Nemnes, G.A.; Ion, L.; Antohe, S. Self-consistent potentials and linear regime conductance of cylindrical nanowire transistors in the R-matrix formalism. *J. Appl. Phys.* **2009**, *106*, 11371. [CrossRef]
45. Nemnes, G.A.; Manolescu, A.; Gudmundsson, V. Reduction of ballistic spin scattering in a spin-FET using stray electric fields. *J. Phys. Conf. Sert* **2012**, *338*, 012012. [CrossRef]
46. Manolescu, A.; Nemnes, G.A.; Sitek, A.; Rosdahl, T.O.; Erlingsson, S.I.; Gudmundsson, V. Conductance oscillations of core-shell nanowires in transversal magnetic fields. *Phys. Rev. B* **2016**, *93*, 205445. [CrossRef]
47. Mitran, T.; Nemnes, G.; Ion, L.; Dragoman, D. Ballistic electron transport in wrinkled superlattices. *Phys. E* **2016**, *81*, 131. [CrossRef]
48. Nemnes, G.A.; Dragoman, D. Reconfigurable quantum logic gates using Rashba controlled spin polarized currents. *Physica E* **2019**, *111*, 13. [CrossRef]
49. Datta, S. *Electronic Transport in Mesoscopic Systems*; Cambridge University Press: Cambridge, UK, 1995.
50. Stern, F. Self-Consistent Results for n-Type Si Inversion Layers. *Phys. Rev. B* **1972**, *5*, 4891. [CrossRef]
51. Ando, T.; Fowler, A.B.; Stern, F. Electronic properties of two-dimensional systems. *Rev. Mod. Phys.* **1982**, *54*, 437. [CrossRef]

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Quantum Enhancement of a S/D Tunneling Model in a 2D MS-EMC Nanodevice Simulator: NEGF Comparison and Impact of Effective Mass Variation

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Abstract: As complementary metal-oxide-semiconductor (CMOS) transistors approach the nanometer scale, it has become mandatory to incorporate suitable quantum formalism into electron transport simulators. In this work, we present the quantum enhancement of a 2D Multi-Subband Ensemble Monte Carlo (MS-EMC) simulator, which includes a novel module for the direct Source-to-Drain tunneling (S/D tunneling), and its verification in the simulation of Double-Gate Silicon-On-Insulator (DGSOI) transistors and FinFETs. Compared to ballistic Non-Equilibrium Green's Function (NEGF) simulations, our results show accurate I_D vs. V_{GS} and subthreshold characteristics for both devices. Besides, we investigate the impact of the effective masses extracted Density Functional Theory (DFT) simulations, showing that they are the key of not only the general thermionic emission behavior of simulated devices, but also the electron probability of experiencing tunneling phenomena.

Keywords: direct source-to-drain tunneling; transport effective mass; confinement effective mass; multi-subband ensemble Monte Carlo; non-equilibrium Green's function; DGSOI; FinFET

1. Introduction

Conventional and novel transistor architectures have been scaled down in the last decades to achieve better performance and larger integration with both lower power consumption and cost. However, conventional bulk complementary metal-oxide-semiconductor (CMOS) technologies present different problems with scaling, such as short-channel effects, reduction of the mobility, leakage current, degradation of the ON and OFF currents (I_{ON}/I_{OFF}), or variability issues. Novel CMOS transistor architectures, such as Full-Depleted Silicon-On-Insulator (FDSOI) and FinFET, were introduced to mitigate the unwanted effects. Furthermore, in the area of nanotransistor transport simulations, one needs to assess the importance of new phenomena that were not relevant in previous technological nodes [1] in order to explain the electrical behavior of aggressively scaled nanodevices. The simulation of these new phenomena is therefore mandatory to investigate and design the next technology generations and to extend the end of the scaling Roadmap.

At present, different approaches incorporating quantum confinement and tunneling into semi-classical models have become popular due to their modular implementation and reduced computational cost in comparison to purely quantum transport simulation techniques. In particular, the direct Source-to-Drain tunneling (S/D tunneling) starts to play an important role degrading the

subthreshold behavior when the channel length is reduced to below 10 nm [2,3], being traditionally considered as a scaling limit in ballistic Non-Equilibrium Green's Function (NEGF) calculations [4], distorting the MOSFET operation at transistor channel lengths around 3nm [2]. This tunneling mechanism allows electrons to tunnel from the source to the drain through the narrow potential barrier existing between both regions, which is controlled by the gate. As a result, the current is increased, eroding the gate control and the subthreshold slope and increasing the leakage. In the simulation of the direct tunneling phenomena, the employed band structure model must accurately represent the experimental energy gaps and effective masses for the most relevant subbands.

The aim of this work is twofold. First, we will discuss the quantum upgrade of our semi-classical 2D Multi-Subband Ensemble Monte Carlo (MS-EMC) simulation tool [5] through the inclusion of a novel S/D tunneling model. Second, we will perform a comprehensive study of how the effective mass variation in confined channels impacts the transport properties and the S/D tunneling. In particular, we have calibrated our tunneling model against the 2D NEGF solver included in the new simulation environment Nano-Electronic Simulation Software (NESS) [6] bearing in mind that the S/D tunneling is naturally included in the quantum NEGF approach. To understand the impact of electron effective mass variation, the bulk effective masses (m_{bulk}) and calibrated effective masses (m_{eff}) from Density Functional Theory (DFT) are used in the MS-EMC model, which is the preferred technique to calculate the electronic band structure of confined nanostructures.

The paper is organized as follows. Section 2 provides a general overview of the simulation framework, including the outline of the simulated devices (Section 2.1), a brief description of NEGF-NESS (Section 2.2) and MS-EMC tools (Section 2.3). It also reports the S/D tunneling model incorporated in the MS-EMC tool (Section 2.4), together with the effective mass calculation and the corresponding extracted values (Section 2.5). The main findings are presented in Section 3 considering ballistic transport for MS-EMC vs. NEGF comparison (Section 3.1) as well as diffusive simulations for the study of the effective mass variation impact (Section 3.2). Finally, conclusions are drawn in Section 4.

2. Simulation Framework and Device Structures

2.1. Description of the Simulated Devices

In this work, we have compared two double-gate device architectures, with the main difference related to the confinement direction: a planar Double-Gate Silicon-On-Insulator (DGSOI) transistor and a vertical FinFET. Their description including orientation and design parameters can be found in Figure 1. The corresponding bulk effective masses are summarized in Table 1. The confinement direction for these devices on standard wafers [100] changes from (100) for DGSOI to $(0\bar{1}1)$ for FinFET, whereas the transport direction <011> is the same for both. The difference in the confinement direction modifies the electron distribution in the subbands and, consequently, the electrostatic potential profile. In addition, the carrier transport effective mass is also modified [7] as it is shown in Section 2.5.

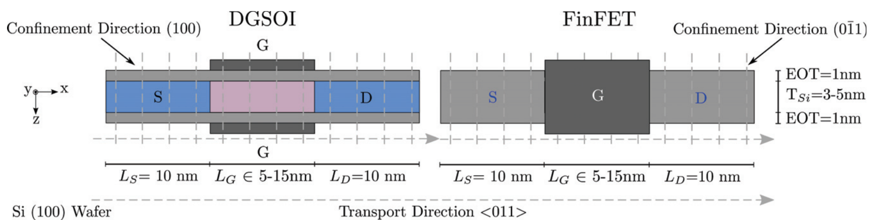

Figure 1. Double-Gate Silicon-On-Insulator (DGSOI) and FinFET structures analyzed in this paper with L_G ranging from 5 to 15 nm and T_{Si} = 3–5 nm. The 1D Schrödinger equation is solved in the confinement direction for each grid point and the Boltzmann Transport Equation (BTE) is solved by the MC method in the transport plane.

Table 1. Silicon bulk effective masses (m_{bulk}) for the different crystallographic directions considered in the DGSOI and FinFET devices. Herein, m_x and m_z are the transport and confinement masses, respectively; m_y is the effective mass in the periodic transverse direction; m_0 is the free electron mass; and the subindex of Δ represents the degeneracy factor associated with the conduction band valley.

Device	Valley	m_{bulk}		
		m_x	m_y	m_z
DGSOI	Δ_2	m_t = 0.193 m_0	m_t = 0.193 m_0	m_l = 0.912 m_0
(100)<011>	Δ_4	$\frac{2m_l m_t}{m_l+m_t}$ = 0.319 m_0	$\frac{m_l+m_t}{2}$ = 0.553 m_0	m_t = 0.193 m_0
FinFET	Δ_2	m_t = 0.193 m_0	m_l = 0.912 m_0	m_t = 0.193 m_0
(0$\bar{1}$1)<011>	Δ_4	$\frac{m_l+m_t}{2}$ = 0.553 m_0	m_t = 0.193 m_0	$\frac{2m_l m_t}{m_l+m_t}$ = 0.319 m_0

At this stage, it is important to highlight that, although the FinFET is a 3D structure and our simulation approach is 2D, it has been shown that FinFETs with fin heights much higher than the corresponding thicknesses show similar behavior in all transport regimes when using 2D and 3D simulations [8].

The devices under consideration have been parametrized for gate lengths ranging from 5 to 15 nm. A channel thickness T_{Si} = 3 nm has been chosen for the MS-EMC vs. NEGF comparison. As for the effective mass variation impact, these devices have been simulated for two different channel thickness T_{Si} = 5 nm and T_{Si} = 3 nm in order to capture the effect of the channel thickness reduction. The rest of the technological parameters remains constant: a SiO_2 gate oxide with EOT = 1 nm and a metal gate work function of 4.385 eV.

2.2. Description of the 2D NEGF Module Inside NESS

The effective-mass real-space Hamiltonian can be expressed as,

$$E' \, \psi(x,z,y) = \left[-\frac{\hbar^2}{2m_x}\frac{\partial^2}{\partial x^2} - \frac{\hbar^2}{2m_z}\frac{\partial^2}{\partial z^2} + \frac{\hbar^2 k_y^2}{2m_y} + V(x,y,z) \right] \psi(x,z,y), \tag{1}$$

assuming y-direction as the periodic transverse direction. The total energy E' can also be written as $E' = E_x + \frac{\hbar^2 k_y^2}{2m_y}$, where E_x is the electron energy in the transport direction. The Hamiltonian in Equation (1) is then transformed to the mode-space representation in order to reduce the computational cost of quantum transport simulations [9]. This was carried out by means of a recursive NEGF approach [10] as implemented in NESS [6] to extract the most relevant physical quantities such as the carrier charge and current. Further, we briefly summarize the main expressions of the NEGF formalism.

For 2D devices and by exploiting the effective-mass approximation, all the transverse modes k_y can be treated as independent devices in parallel. Then, within the ballistic regime and under steady-state conditions, the retarded and lesser Green's function for the active device region are written, in matrix notation, as:

$$G^R(E_x) = \left[E_x \mathbf{I} - \tilde{H}_M - \Sigma_S^R(E_x) - \Sigma_D^R(E_x) \right]^{-1}, \tag{2}$$

$$G^<(E_x) = G^R(E_x) \left[\Sigma_S^<(E_x) + \Sigma_D^<(E_x) \right] G^{R\dagger}(E_x), \tag{3}$$

where H_M and $\Sigma_C^{R/<}$ are the Hamiltonian and the retarded/lesser contact self-energies ($C = S/D$) in the mode-space representation, respectively. The retarded Green's function at the contacts $G^R = g_C^R$ is

calculated by means of the Sancho-Lopez-Rubio recursive method [11], allowing straightforwardly the evaluation of Σ_C^R as

$$\Sigma_C^R(E_x) = t_M \cdot g_C^R(E_x) \cdot t_M^\dagger \tag{4}$$

where the mode-space hopping parameters t_M are computed as in Ref. [9]. The lesser contact self-energy $\Sigma_C^<$ can be then computed from:

$$\Sigma_C^<(E_x) = -F_{S/D}(E_x)(g_C^R(E_x) - g_C^{R\dagger}(E_x)). \tag{5}$$

with

$$F_{S/D}(E_x) = \frac{L_y}{2\pi} \int \mathrm{d}k_y f_{S/D} \left(E_x + \frac{\hbar^2 k_y^2}{2m_y} \right), \tag{6}$$

where $f_{S/D}$ is the Fermi-Dirac distribution and L_y is the periodic length in y-direction. Finally, the 3D carrier concentration and current are calculated in the mode-space representation as follows:

$$n(x_i, y, z_j) = -\frac{i}{\Delta x_i \Delta z_j L_y} \sum_{nm} \int \frac{\mathrm{d}E_x}{2\pi} \phi_n(z_j) G_{nm}^<(x_i, x_i; E_x) \phi_m^*(z_j), \tag{7}$$

$$I(x_i) = -\frac{2e}{\hbar L_y} \int \frac{\mathrm{d}E_x}{2\pi} \mathrm{Tr} \left[t_M(i) G^<(x_{i+1}, x_i; E_x) - G^<(x_i, x_{i+1}; E_x) t_M^\dagger(i) \right]. \tag{8}$$

where $\phi_n(z)$ is the confinement wave-function for the subband n, whereas, matrices $t_M(i)$ couple two successive layers. Finally, Equations (1) to (3), (5) and (7) are solved self-consistently with Poisson's equation.

2.3. General Overview of the 2D MS-EMC Tool

The 2D MS-EMC simulation framework [5] used in this work is based on a decoupled mode-space quantum transport [12] and a semi-classical approach. The simulator solves the Schrödinger equation in the discretization slices along the confinement direction and the Boltzmann Transport Equation (BTE) in the transport plane (Figure 1). Both equations are coupled through the 2D Poisson equation in the whole 2D simulation domain to keep the self-consistency of the solution. This tool has been widely used in different scenarios including the study of different tunneling mechanisms in similar devices [13]. Due to the modular design of our MS-EMC tool, the inclusion of these tunneling phenomena can be successfully included via additional modules that treat them as separate transport mechanisms without increasing the computational time in comparison to purely quantum simulators. These modules can be switched on or off depending on the simulation scenario, offering the possibility of studying each tunneling mechanism independently.

2.4. Description of the S/D Tunneling Model Inside the 2D MC-EMC Tool

S/D tunneling has been included as a separated transport mechanism in the 2D MS-EMC tool described in Section 2.3. It has been implemented as a stochastic mechanism evaluated for each superparticle at the end of the Monte Carlo cycle [14]. When this tunneling mechanism is considered, an electron near the S/D potential barrier will be either reflected or transmitted through it.

The first step is to calculate the tunneling probability by the Wentzel-Kramers-Brillouin (WKB) approximation [15]. It mainly depends on the energy and position of the carrier in the device; the transport effective mass (namely m_x in Tables 1 and 2); and the energy profile of the i-th subband determining the shape of the tunneling barrier ($E_i(x)$), which is calculated as a solution of the 1D Schrödinger equation. The probability of tunneling through the barrier is equivalent to the transmission coefficient, and determines the fraction of electrons experiencing S/D tunneling at a given energy below the potential barrier. The tunneling probability of the electron for a given energy ($\mathrm{T}_{WKB}(\mathrm{E}_x)$) is:

$$T_{WKB}(E_x) = \exp\left\{ -\frac{2}{\hbar} \int_a^b \sqrt{2m_x(E_i(x) - E_x)}\, dx \right\}, \tag{9}$$

where a and b are the limits of the tunneling path, and E_x is the total energy in the transport plane considering only the projection of the kinetic energy in the direction that faces the potential barrier.

It has been reported for the short-gate length devices that this model overesitimated the number of superparticles experiencing S/D tunneling compared to NEGF approach [16]. This model was compared to NEGF simulations showing an overestimation of the number of superparticles experiencing S/D tunneling, especially for short-gate length devices. In order to reduce this discrepancy, the tunneling model in Equation (9) has been reformulated following a non-local WKB probability approach as stated in Appendix B of Ref. [17]. In the context of a 2D simulation domain, the new S/D tunneling probability for a given energy ($T_{DT}(E_x)$) is now defined as:

$$T_{DT}(E_x) = \frac{\Delta_y}{2\sqrt{\pi}} \left[\hbar \int_a^b \frac{dx}{\sqrt{2m_x(E_i(x) - E_x)}} \right]^{-1/2} \cdot T_{WKB}(E_x), \tag{10}$$

where Δ_y is the mesh spacing in the direction normal to transport. As this direction is not taken into account in our 2D MS-EMC tool, the value of Δ_y has been calibrated to fulfill the following conditions: *(i)* the force $T_{DT}(E_x)$ to be in the range [0–1]; *(ii)* to be small enough to be consistent with the periodic boundary condition in the y direction; and *(iii)* to have similar degradation in the subthreshold region compared to NEGF calculations for the device with L_G = 7.5 nm (shown in Section 3.1). In order to assess the S/D tunneling impact as a function of the gate length, Δ_y has been calculated according to the mesh spacing in the transport direction (Δ_x). A fixed number of mesh points is taken in our calculation in the transport direction regardless of the gate length of the considered device, so that Δ_x varies as L_G does so. In this particular study, we have chosen $\Delta_y = 0.05\Delta_x$, which corresponds to Δ_y = 0.01 nm for the device with L_G = 7.5 nm.

The second step is to determine whether the particle tunnels or not by using a rejection criterion. To do so, a uniformly distributed random number r_{DT} is generated between 0 and 1 and compared to $T_{DT}(E_x)$. If $r_{DT} \leq T_{DT}(E_x)$, the superparticle will cross the barrier; otherwise, it will turn back suffering a back-scattering. Finally, if the superparticle undergoes S/D tunneling, its motion inside the potential barrier is described using Newton's mechanics considering an inverted potential profile and ballistic transport [18].

2.5. Description of the Effective Mass Calculation

To adopt more reasonable conduction band structures in nanoscaled structures, we accurately calculate m_{eff} by using DFT implemented in QuantumATK tool of Synopsys [19]. Table 2 summarizes the values of the masses for both devices (DGSOI and FinFET) studied here. It is also important to highlight at this point that the lowest energy subband changes from Δ_2 in the planar transistor to Δ_4 in the vertical one.

Figure 2 shows the difference of the longitudinal (m_l) and transverse (m_t) effective masses calculated as a function of the silicon thickness (T_{Si}) for the two different confinement orientations. It is clearly shown that the effective masses tend to m_{bulk} for larger T_{Si}. Although these masses (m_l and m_t) are included in the 2D MS-EMC tool as input parameters, it is important to analyze the modification of m_x (transport mass), m_z (confinement mass) and m_y (mass in the direction normal to transport). Their expressions are shown in Table 1, and their particular values are grouped in Table 2 for the two T_{Si} values herein considered. In order to study the impact of T_{Si} reduction, the deviations (in %) of m_l, m_t and their combinations included in Table 1 have been calculated (Figure 3) as $100 \cdot |m_{bulk} - m_{eff}|/m_{eff}$. It is interesting to mention that the deviation in m_t is more noticeable than that of $(m_t + m_l)/2$, which corresponds to m_x in the S/D tunneling model for the fundamental subband of the planar and vertical

devices, respectively. In particular, they drop from ∼35% (DGSOI devices) to ∼15% (FinFETs) for T_{Si} = 3 nm and from ∼17.5% (DGSOI devices) to ∼2.5% (FinFETs) for T_{Si} = 5 nm.

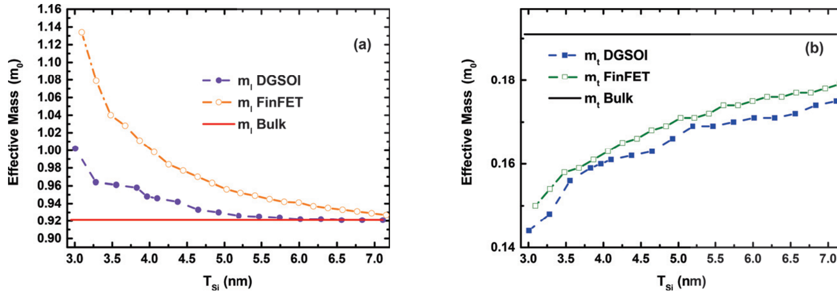

Figure 2. (**a**) Longitudinal (m_l) and (**b**) transverse (m_t) effective masses calculated using Density Functional Theory (DFT) as well as the bulk effective masses as a function of the silicon thickness (T_{Si}) for DGSOI ((100) Confinement Orientation) and FinFET ((0$\bar{1}$1) Confinement Orientation) devices.

Table 2. Effective masses (m_{eff}) considering the DGSOI and FinFET devices herein studied with silicon thickness T_{Si} = 3–5 nm using DFT simulations included in QuantumATK of Synopsys [19]. Notice that m_x and m_z are the transport and confinement masses, respectively, m_y is the mass in the direction normal to transport, m_0 is the free electron mass, and the subindex of Δ represents the degeneracy factor associated with the conduction band valley.

Device	Valley	T_{Si} = 3 nm			T_{Si} = 5 nm		
		m_x	m_y	m_z	m_x	m_y	m_z
DGSOI (100)<011>	Δ_2	0.144 m_0	0.144 m_0	1.002 m_0	0.166 m_0	0.166 m_0	0.93 m_0
	Δ_4	0.252 m_0	0.573 m_0	0.144 m_0	0.282 m_0	0.548 m_0	0.166 m_0
FinFET (0$\bar{1}$1)<011>	Δ_2	0.15 m_0	1.134 m_0	0.15 m_0	0.171 m_0	0.956 m_0	0.171 m_0
	Δ_4	0.642 m_0	0.15 m_0	0.265 m_0	0.563 m_0	0.171 m_0	0.29 m_0

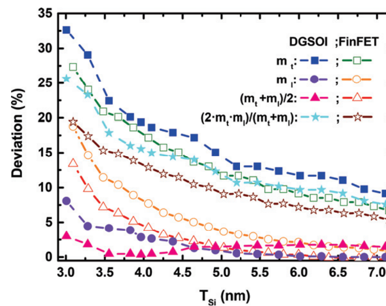

Figure 3. Deviation (%) of the longitudinal (m_l) and transverse (m_t) effective masses and their combinations needed in Table 2 as a function of the silicon thickness (T_{Si}) for DGSOI ((100) confinement orientation) as well as FinFET ((0$\bar{1}$1) confinement orientation) devices.

3. Simulation Results and Discussions

3.1. Comparison of MS-EMC with S/D Tunneling Models vs. NEGF

The I_D vs. V_{GS} characteristics obtained from ballistic simulations of the DGSOI and FinFET devices at V_{DS} = 500 mV with gate length ranging from 5 nm to 15 nm are shown in Figure 4. Four types of simulations are displayed: *(1)* the NEGF approach in the NESS tool, *(2)* the MS-EMC tool without any type of tunneling, and the MS-EMC tool with the S/D tunneling module using *(3)*

$T_{WKB}(E_x)$ and *(4)* $T_{DT}(E_x)$. In order to attain a good I_{ON}/I_{OFF} behavior, the work function for the devices with Lg = 5 nm was chosen to be 5 eV rather than 4.385 eV, as for the rest of cases. In general, the I_D vs. V_{GS} characteristics were shifted to have the same threshold current (I_{TH}), showing similar I_{ON} in all the cases. The particular values of I_{TH} as a function of the gate length are included in Figure 4 too.

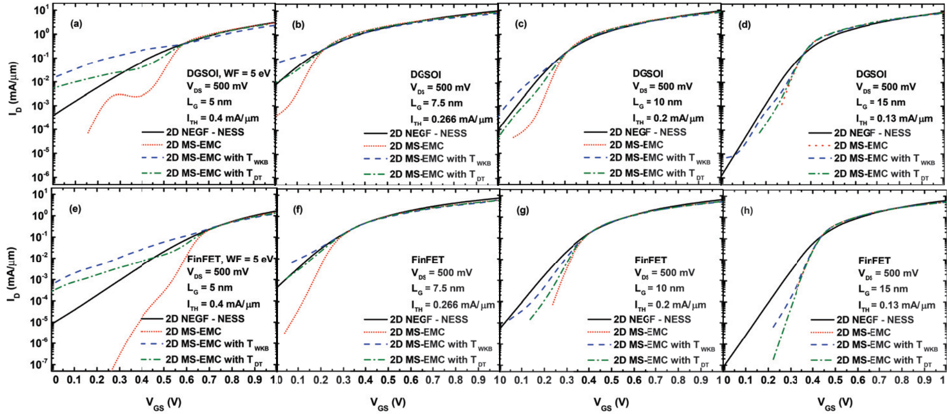

Figure 4. I_D vs. V_{GS} in the DGSOI and FinFET devices at V_{DS} = 500 mV with L_G 5 nm (**a**,**e**), 7.5 nm (**b**,**f**), 10 nm (**c**,**g**), and 15 nm (**d**,**h**), considering the four types of simulations are: *(1)* Non-Equilibrium Green's Function (NEGF) approach in the Nano-Electronic Simulation Software (NESS) tool, *(2)* Multi-Subband Ensemble Monte Carlo (MS-EMC) tool without any type of tunneling, and MS-EMC tool with the Source-to-Drain tunneling (S/D tunneling) module using *(3)* $T_{WKB}(E_x)$ and *(4)* $T_{DT}(E_x)$.

Regarding the OFF region, where S/D tunneling was more noticeable, we can reach the following conclusions when the MS-EMC results are compared against NEGF. First, the simulation without any tunneling reduced I_{OFF} substantially due to the absence of particles below the barrier. Second, there was an overestimation of I_{OFF} when the tunneling probability was calculated by $T_{WKB}(E_x)$, specially for $L_G \leq 10$ nm. Third, when the tunneling probability was chosen as $T_{DT}(E_x)$, the current was comparable to NEGF, showing a reduction of I_{OFF}. In particular for L_G = 7.5 nm, it was really similar to NEGF because, as anticipated earlier, the parameter Δ_y included in Equation (10) was calibrated against the NEGF results. Fourth, the S/D tunneling was important in ultra-scaled devices with $L_G \leq 10$ nm due to the dimensions of the potential barrier. Consequently, for L_G = 15 nm, there was almost no difference in the OFF current among the different MS-EMC cases. Moreover, the inherent statistical nature of the MC method also manifested in Figure 4a by the fluctuations in the subthreshold regime for the simulation without any tunneling module.

Figure 5 shows the average number of electrons affected by S/D tunneling for the simulations considered in Figure 4. In general, the drain current in Monte Carlo simulators was calculated by the spatial average of the electron current along the channel. Therefore, the number of electrons located inside the potential barrier due to the S/D tunneling model contributed to the increase of the total current. On the other hand, as depicted in Figure 5, the $T_{DT}(E_x)$ probability reduced the number of electrons crossing the potential barrier compared to the $T_{WKB}(E_x)$ case and thus there was a reduction of I_{OFF}. It is also worth to mention that the number of electrons affected by S/D tunneling approached the same value at high V_{GS} regime for both approaches ($T_{WKB}(E_x)$ and $T_{DT}(E_x)$) and for both devices regardless of the gate length.

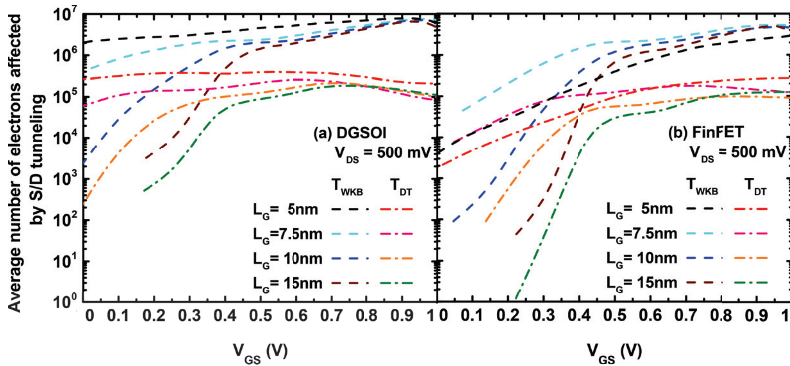

Figure 5. Average number of electrons (in arbitrary units) affected by S/D tunneling as a function of the V_{GS} in the (**a**) DGSOI and (**b**) FinFET devices at V_{DS} = 500 mV with L_G = 5, 7.5, 10, and 15 nm, for the MS-EMC tool with the S/D tunneling module using $T_{WKB}(E_x)$ and $T_{DT}(E_x)$.

The subthreshold swing (SS) is one of the main parameters used to determine the behavior of electronic devices in the OFF region. In practice, the best MOSFET implementations cannot reduce SS < 60 mV/dec. For the SS calculation, we have considered the I_D decade between 10^{-3} mA/μm and 10^{-2} mA/μm (or between 10^{-2} mA/μm and 10^{-1} mA/μm) in order to avoid the stochastic noise of the Monte Carlo simulations at very low V_{GS}.

Figure 6 shows the SS difference (ΔSS) between MS-EMC and NEGF simulations. In general, and for all values of V_{DS}, we have reached the following three conclusions. First, ΔSS was negative for the MC simulation without any tunneling due to its lower I_{OFF} compared to NEGF case. Second, ΔSS tended to zero for the FinFET device with $L_G \geq 7.5$ nm, showing the excellent agreement between both approaches for that device. Third, for L_G = 15 nm, ΔSS was again negative due to the lower I_{OFF} of the different MS-EMC simulations.

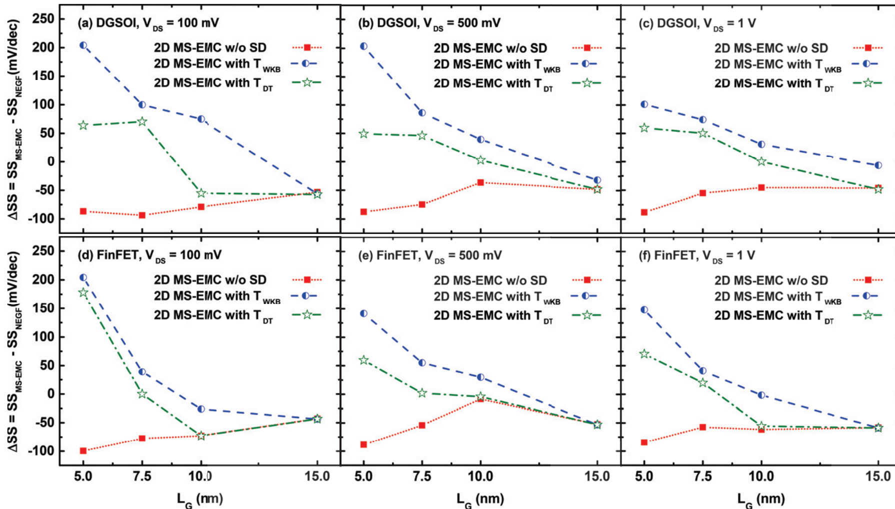

Figure 6. ΔSS as a function of the gate length in the DGSOI and FinFET devices at V_{DS} = 100 mV (**a**,**d**), V_{DS} = 500 mV (**b**,**e**), and V_{DS} = 1 V (**c**,**f**), calculated as the difference between the 2D NEGF-NESS and the 2D MS-EMC tools considering the three combinations: a simulation without any tunneling module and both S/D tunneling modules with $T_{WKB}(E_x)$ and $T_{DT}(E_x)$ probabilities.

3.2. Impact of the Effective Mass Choice

In general, the utilization of m_{eff} instead of m_{bulk} results in a shift of the I_D vs. V_{GS} characteristics ([20]). Accordingly, we have focused on the study of this impact on the threshold voltage shift (ΔV_{TH}) calculated as the difference of V_{TH} using m_{eff} and m_{bulk} (Figure 7). V_{TH} has been calculated in this work using the constant drain current method [21]. In this section, non-equilibrium simulations (including acoustic phonon, optical, phonon, surface roughness, and Coulomb scattering mechanisms) have been considered using the 2D MS-EMC tool with the three possible combinations: *(1)* without any tunneling module, *(2)* with S/D tunneling using $T_{WKB}(E_x)$, and *(3)* with S/D tunneling using $T_{DT}(E_x)$.

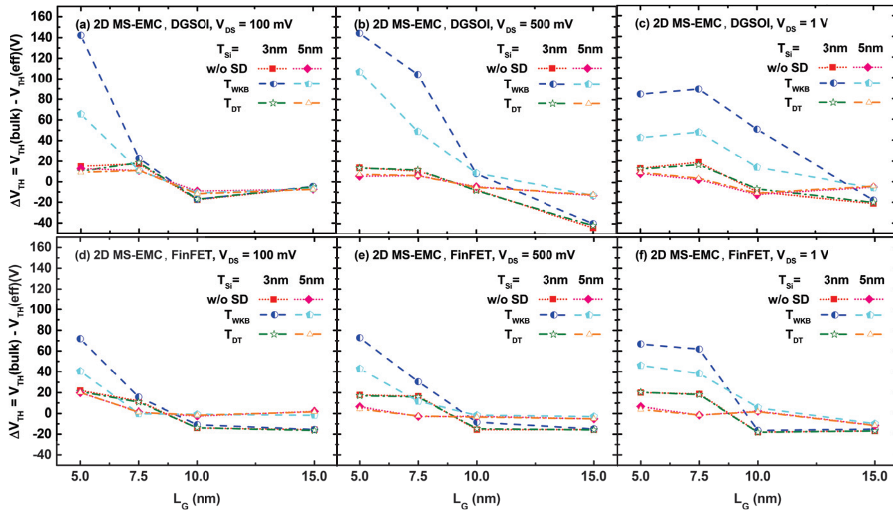

Figure 7. ΔV_{TH} as a function of the gate length in the DGSOI and FinFET devices with silicon thickness T_{Si} = 3–5 nm at V_{DS} = 100 mV (**a**,**d**), V_{DS} = 500 mV (**b**,**e**), and V_{DS} = 1 V (**c**,**f**), considering the three 2D MS-EMC combinations: without any tunneling module and with both S/D tunneling modules using $T_{WKB}(E_x)$ and $T_{DT}(E_x)$ probabilities.

Four observations can be made based on the ΔV_{TH} curves displayed in Figure 7. First, ΔV_{TH} was positive for the ultra-scaled devices (L_G = 5 and 7.5 nm) because the use of m_{eff} increases the current, whereas the opposite trend ($\Delta V_{TH} < 0$) was observed for devices with $L_G \geq 10$ nm. Second, ΔV_{TH} was reduced for thicker devices (T_{Si} = 5 nm) because m_{eff} tends to m_{bulk} when T_{Si} increases. Third, a similar behavior is shown in Figure 7 for the simulations without any tunneling and with $T_{DT}(E_x)$. However, when the tunneling probability was calculated using $T_{WKB}(E_x)$ the difference between using m_{eff} instead of m_{bulk} is greater due to the overestimation of the superparticles experiencing S/D tunneling. This effect became more relevant when the device size is reduced. In fact, this influence was significant for L_G = 5 nm at all V_{DS} and it was extended to longer devices as V_{DS} increased. Fourth, the impact of the effective mass choice was smaller in the FinFET compared to the DGSOI device due to the lower deviation of its effective transport mass (m_x) shown in Figure 3.

4. Conclusions

This work presents the quantum enhancement of a semi-classical 2D MS-EMC simulator and its application to DGSOI transistors and FinFETs. It has been demonstrated as a useful tool for the optimization of devices targeting sub-10 nm nodes thanks to its higher computational efficiency. Two different approaches to consider S/D tunneling in MC are described in this work and their results with FinFET and DGSOI are compared to those from NEGF formalism. One of these models needs to

be calibrated against quantum transport simulations. Results obtained from the MS-EMC code show an excellent agreement with the NEGF simulations in the subthreshold region. The impact of realistic effective masses, calculated from first principles, on electron transport has also been studied by means of MS-EMC simulations. Our findings suggest that effective masses variation alters in a significant way the tunneling probability in the subthreshold regime, in agreement with reported results in the literature.

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References

1. Wong, H.S. Beyond the conventional transistor. *IBM J. Res. Dev.* **2002**, *46*, 133–168. [CrossRef]
2. Iwai, H. Future of nano CMOS technology. *Solid-State Electron.* **2015**, *112*, 56–67. [CrossRef]
3. Grillet, C.; Logoteta, D.; Cresti, A.; Pala, M.G. Assessment of the Electrical Performance of Short Channel InAs and Strained Si Nanowire FETs. *IEEE Trans. Electron Devices* **2017**, *64*, 2425–2431. [CrossRef]
4. Wang, J.W.J.; Lundstrom, M. Does source-to-drain tunneling limit the ultimate scaling of MOSFETs? In Proceedings of Technical digest–IEDM, International Electron Devices Meeting 2002, San Francisco, CA, USA, 8–11 December 2002; pp. 707–710. [CrossRef]
5. Sampedro, C.; Medina-Bailon, C.; Donetti, L.; Padilla, J.; Navarro, C.; Marquez, C.; Gámiz, F. Multi-Subband Ensemble Monte Carlo Simulator for Nanodevices in the End of the Roadmap. In Proceedings of the International Conference on Large-Scale Scientific Computations, Sozopol, Bulgaria, 10–14 June 2019; Lecture Notes in Computer Science (LNCS) post-proceedings.. [CrossRef]
6. Berrada, S.; Dutta, T.; Carrillo-Nunez, H.; Duan, M.; Adamu-Lema, F.; Lee, J.; Georgiev, V.; Medina-Bailon, C.; Asenov, A. NESS: new flexible Nano-Electronic Simulation Software. In Proceedings of the 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Austin, TX, USA, 24–26 September 2019; pp. 22–25. [CrossRef]
7. Rahman, A.; Lundstrom, M.S.; Ghosh, A.W.; Rahman, A.; Lundstrom, M.S.; Ghosh, A.W. Generalized effective-mass approach for n-type metal-oxide-semiconductor field-effect transistors on arbitrarily oriented wafers. *J. Appl. Phys.* **2005**, *97*. [CrossRef]
8. Sampedro, C.; Donetti, L.; Gámiz, F.; Godoy, A. 3D Multi-Subband Ensemble Monte Carlo Simulator of FinFETs and Nanowire Transistors. In Proceedings of 2014 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Yokohama, Japan, 9–11 September 2014; pp. 21–24. [CrossRef]
9. Luisier, M.; Schenk, A.; Fichtner, W. Quantum transport in two- and three-dimensional nanoscale transistors: Coupled mode effects in the nonequilibrium Greens function formalism. *J. Appl. Phys.* **2006**, *100*, 043713. [CrossRef]
10. Svizhenko, A.; Anantram, M.P. Role of scattering in nanotransistors. *IEEE Trans. Electron Devices* **2003**, *50*, 1459–1466. [CrossRef]
11. Sancho, M.P.L.; Sancho, J.M.L.; Sancho, J.M.L.; Rubio, J. Highly convergent schemes for the calculation of bulk and surface Green functions. *J. Phys. F Met. Phys.* **1985**, *15*, 851–858. [CrossRef]
12. Venugopal, R.; Ren, Z.; Datta, S.; Lundstrom, M.S.; Jovanovic, D. Simulating quantum transport in nanoscale transistors: Real versus mode-space approaches. *J. Appl. Phys.* **2002**, *92*, 3730–3739. [CrossRef]
13. Medina-Bailon, C.; Padilla, J.; Sadi, T.; Sampedro, C.; Godoy, A.; Donetti, L.; Georgiev, V.; Gámiz, F.; Asenov, A. Multisubband Ensemble Monte Carlo Analysis of Tunneling Leakage Mechanisms in Ultrascaled FDSOI, DGSOI, and FinFET Devices. *IEEE Trans. Electron Devices* **2019**, *66*, 1145–1152. [CrossRef]

14. Medina-Bailon, C.; Padilla, J.; Sampedro, C.; Godoy, A.; Donetti, L.; Gámiz, F. Source–to–Drain Tunneling Analysis in FDSOI, DGSOI and FinFET Devices by Means of Multi-Subband Ensemble Monte Carlo. *IEEE Trans. Electron Devices* **2018**, *65*, 4740–4746. [CrossRef]
15. Griffiths, D.J. The WKB approximation. In *Introduction to Quantum Mechanics*; Prentice Hall: Bergen, NJ, USA, 1995; pp. 274–297.
16. Medina-Bailon, C.; Sampedro, C.; Padilla, J.L.; Godoy, A.; Donetti, L.; Gamiz, F.; Asenov, A. MS-EMC vs. NEGF: A comparative study accounting for transport quantum corrections. In Proceedings of the EUROSOI-ULIS 2018 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS 2018), Granada, Spain, 19–21 March 2018; pp. 1–4. [CrossRef]
17. Carrillo-Nunez, H.; Ziegler, A.; Luisier, M.; Schenk, A. Modeling direct band-to-band tunneling: From bulk to quantum-confined semiconductor devices. *J. Appl. Phys.* **2015**, *117*, 1234501. [CrossRef]
18. Shen, C.; Yang, L.T.; Samudra, G.; Yeo, Y.C. A new robust non-local algorithm for band-to-band tunneling simulation and its application to Tunnel-FET. *Solid-State Electron.* **2011**, *57*, 23–30. [CrossRef]
19. QuantumATK version O-2018.06. Available online: https://www.synopsys.com/silicon/quantumatk.html (accessed on 1 June 2019).
20. Medina-Bailon, C.; Lee, J.; Sampedro, C.; Padilla, J.; Donetti, L.; Georgiev, V.; Gámiz, F.; Asenov, A. Impact of Effective Mass on Transport Properties and Direct Source-to-Drain Tunneling in Ultrascaled Double Gate Devices: a 2D Multi-Subband Ensemble Monte Carlo study. In Proceedings of the Nanotechnology Materials and Devices Conference (NMDC), Stockholm, Sweden, 27–30 October 2019; pp. 1–4.
21. Schroder, D.K. *Semiconductor Material and Device Characterization*; John Wiley & Sons: Hoboken, NJ, USA, 2006.

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Analysis of the Sensing Margin of Silicon and Poly-Si 1T-DRAM

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Abstract: Recently, one-transistor dynamic random-access memory (1T-DRAM) cells having a polysilicon body (poly-Si 1T-DRAM) have attracted attention as candidates to replace conventional one-transistor one-capacitor dynamic random-access memory (1T-1C DRAM). Poly-Si 1T-DRAM enables the cost-effective implementation of a silicon-on-insulator (SOI) structure and a three-dimensional (3D) stacked architecture for increasing integration density. However, studies on the transient characteristics of poly-Si 1T-DRAM are still lacking. In this paper, with TCAD simulation, we examine the differences between the memory mechanisms in poly-Si and silicon body 1T-DRAM. A silicon 1T-DRAM cell's data state is determined by the number of holes stored in a floating body (FB), while a poly-Si 1T-DRAM cell's state depends on the number of electrons trapped in its grain boundary (GB). This means that a poly-Si 1T-DRAM can perform memory operations by using GB as a storage region in thin body devices with a small FB area.

Keywords: one-transistor dynamic random-access memory (1T-DRAM); polysilicon; grain boundary; electron trapping

1. Introduction

Conventional one-transistor one-capacitor dynamic random-access memory (1T-1C DRAM) has reached its scaling limit due to the difficulty of miniaturizing capacitors. Therefore, capacitor-less one-transistor dynamic random-access memory (1T-DRAM), which does not need complicated capacitor fabrication, has been studied as a possible replacement for 1T-1C DRAM [1–14]. 1T-DRAM can be densely integrated because it has a small $4F^2$ cell size with a silicon-on-insulator (SOI) transistor as its basic structure. However, its memory performance deteriorates with decreased transistor size. As its channel length is decreased, its body needs to be thin enough to prevent short channel effects, thus reducing the floating body (FB) which is the charge storage region. In addition, 1T-DRAM is expensive because it requires the use of an SOI wafer.

In recent years, poly-Si 1T-DRAM has gained much attention [15–20]. This type of device stores its charge in its grain boundary (GB) instead of in the FB, and therefore it is advantageous for short channel devices; its charge can be stored in the GB even with a thin body. In addition, an SOI structure with a poly-Si channel can be easily obtained by annealing deposited amorphous silicon. This feature facilitates a three-dimensional (3D) stack architecture that is cost effective and provides superior scalability.

In this paper, we investigate the memory operating mechanisms of silicon 1T-DRAM and poly-Si 1T-DRAM by using device simulation. As a result, we reveal the reasons for the different memory operating characteristics of two 1T-DRAM by analyzing the changes in the devices' charge and energy band diagrams.

2. Simulation Method

Simulations were performed to confirm the differences between 1T-DRAM operations according to their channel materials using the SENTAURUS TCAD tool. Figure 1a,b shows the cross-sections of the simulated devices. The structure is a single gate SOI transistor and the channel materials are single crystal silicon and polycrystalline silicon, respectively, as seen in the figure. The device parameters for the simulations were as follows: gate length (L_g) = 200 nm, body thickness (T_{body}) = 30/40/50 nm (typically 40 nm), gate oxide thickness (T_{ox}) = 4 nm, buried oxide (T_{box}) = 100 nm, source/drain doping concentration (N^+: Arsenic) = 1×10^{20} cm^{-3}, channel doping concentration (P: Boron) = 1×10^{17} cm^{-3}, electron mobility (m_e) = 200 cm^2/V·s, and hole mobility (m_h) = 100 cm^2/V·s. Although both silicon and poly-Si body devices were simulated with the same mobility value, the poly-Si device reduced the drain current due to the charge trapping phenomenon in a single GB. It represented the mobility degradation of poly-Si as compared with silicon in the practical device. For the poly-Si channel, it was assumed that a single vertical grain boundary exists in the middle of the body to simplify simulation. The trap parameter was based on the work of [21]. In recent research, the energy band change as a function of the donor and acceptor type trap densities was confirmed; the investigators verified that donor type traps had little influence on band peak while acceptor type traps had a strong effect on it [18]. In addition, we studied the effect of the capture cross-section, (the probability of capturing carriers in the GB) on memory operating characteristics [22]. On the basis of this research, we chose a typical trap distribution for use in the simulation, as shown in the inset graph of Figure 1c [21–23]. The red and black lines, respectively, represent the donor type trap density and acceptor type trap density. The tails of the conduction and valance bands have an exponential distribution, and near the mid-gap, they have a Gaussian distribution. Figure 1c shows the transfer characteristics of 1T-DRAM with silicon and with poly-Si channels. For the poly-Si channel, the threshold voltage and the subthreshold swing values tend to increase as compared with the silicon channel because electrons are trapped in the GB under an inversion condition. Similarly, in the off state, the current of the poly-Si is smaller than that of the silicon, because less gate induced drain leakage (GIDL) occurs due to the reduction of the electric field in GB of poly-Si.

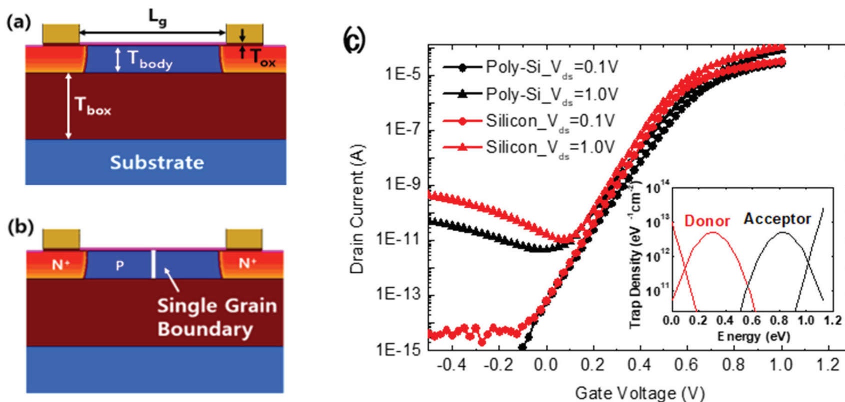

Figure 1. Cross-section of the simulated structure of (**a**) silicon one-transistor dynamic random-access memory (1T-DRAM); and (**b**) poly-Si 1T-DRAM; (**c**) transfer characteristics of silicon 1T-DRAM and poly-Si 1T-DRAM devices (inset, density of states used for poly-Si 1T-DRAM).

Transient simulations were performed to investigate dynamic 1T-DRAM operations. Table 1 shows the operating bias conditions and time conditions for both the silicon and poly-Si devices. The write "1" operation provides hole charges to the device's body using band-to-band tunneling, and the write "0" operation supplies electron charges to the body by applying a forward bias to the drain. In the read operation, a low drain voltage for non-destructive read and a gate voltage that maximized the sensing margin were applied. During the hold period, the gate and drain were set to 0 V to maintain the state of the cell. The write "1" time and write "0" time were set to a time sufficient for hole charge generation and electron charge supply, respectively. The hold time was set as a variable parameter to investigate retention characteristics of memory devices over time.

Table 1. Bias conditions for one-transistor dynamic random-access memory (1T-DRAM) operation.

	Write "1"	Write "0"	Read	Hold
V_g (V)	−2	0	0.6 (Silicon 1T-DRAM) 0.7 (Poly-Si 1T-DRAM)	0
			–	
V_d (V)	2	−1.5	0.1	0
Time (ns)	500	150	10	–

3. Results and Discussion

3.1. Transient Characteristics of Silicon and poly-Si 1T-DRAM

Figure 2a,b shows the transient characteristics of silicon and poly-Si 1T-DRAM cells for states "0" and "1" and three T_{body} values. The x-axis is the hold time, and the y-axis is the read current after writing "1" or "0". With the sensing margin defined as the drain current difference (ΔI_{DS}) between states "1" and "0" at the hold time of 10 ns, Table 2 shows the margin for the three T_{body} values for both devices. In both the silicon and poly-Si 1T-DRAMs, the sensing margin decreases in proportion to $T_{body.}$ However, the acceptable sensing margin is about 3 uA [4], and the sensing margin of silicon devices are smaller than 3uA regardless of T_{body}. For the 50 nm and 30 nm T_{body} values, the sensing margin of poly-Si 1T-DRAM decreases only 30%, while that of silicon decreases by 90%, as shown Table 2. Another remarkable aspect shown in Figure 2a,b is that the read current increase/decrease trend is reversed between the two devices regardless of the body thickness. Silicon 1T-DRAM shows a decrease in state "1" current, while its state "0" current is maintained over time. In contrast, for the poly-Si 1T-DRAM, the read current of state "1" is maintained over time, and the read current of state "0" tends to increase. In order to analyze the cause of these opposing trends, the charges in the devices' FB and GB at a 40 nm T_{body} are compared.

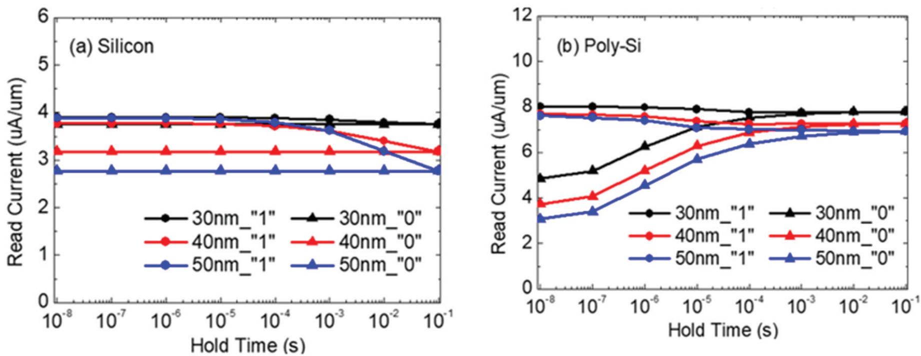

Figure 2. Transient characteristics of (**a**) silicon and (**b**) poly-Si 1T-DRAM according to T_{body}/@T = 300 K.

Table 2. Sensing margin of silicon and poly-Si 1T-DRAMs for varied T_{body}.

T_{body}	Sensing Margin of Silicon 1T- DRAM (uA/um)	Sensing Margin of Poly-Si 1T- DRAM (uA/um)
30 nm	0.15	3.16
40 nm	0.59	3.96
50 nm	1.11	4.54

Figure 3a shows the charge variation in the FB of silicon 1T-DRAM according to the hold time. The black lines represent the number of holes, and the red lines represent the number of electrons in each state. The figure shows that the number of electrons in the FB is similar for states "0" and "1". However, when the hold time is small, the number of holes in state "1" is larger than it is in state "0" since the excess holes generated by the write "1" operation are stored in the FB. These holes lower the threshold voltage by forward biasing the FB. Therefore, the read current of state "1" is larger than that of state "0". This difference disappears as the excess holes in state "1" decrease by recombination over time. In summary, the excess holes in state "1" play an important role in silicon 1T-DRAM state detection, as previously reported.

Figure 3b shows how the trapped charge varies with hold time in the GB of poly-Si 1T-DRAM. In contrast to silicon 1T-DRAM, the difference in the trapped hole charge between states "0" and "1" is small while the difference in the trapped electron charge is large. After a write "0" operation, the excess electrons are trapped in the GB, reducing the number of free electrons for the read operation. Therefore, the read current of state "0" is reduced for short hold times, as shown in Figure 2b. These trapped electrons detrap with time and the read "0" current gradually increases. This can be confirmed by observing the variation in the energy band diagram over time.

Figure 4 shows the conduction band energy diagrams of poly-Si 1T-DRAM at two hold times. The black and red lines are the diagrams for the hold times of 10^{-8} s and 10^{-1} s, respectively. After a write "0" operation, trapped electrons in the GB create a peak in the conduction band, as shown in Figure 4a. This energy peak is a barrier to current flow, therefore, the peak value of the conduction band is inversely proportional to the read current. Therefore, the poly-Si 1T-DRAM's read "0" current is smaller than that of its read "1" current when the hold time is 10^{-8} s, as Figure 2b illustrates. However, the peak value decreases over time as trapped electrons in the GB detrap. This is consistent with the read "0" current increases with longer hold time, in Figure 2b. Unlike state "1", a blue arrow in Figure 4a shows that there is large conduction band difference in state "0" for hold times of 10^{-8} s and 10^{-1} s.

The result is that the read "1" current is constant up to 10^{-1} s as shown in Figure 2b. This indicates that poly-Si 1T-DRAM data states can be distinguished by the number of trapped electrons in state "0".

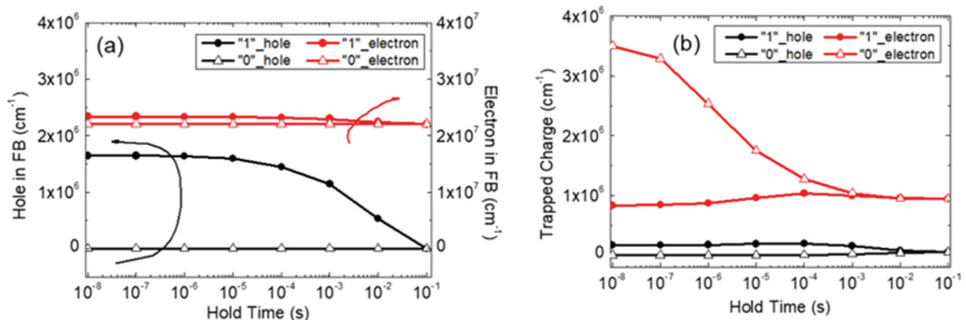

Figure 3. Charge variation according to the hold time (**a**) in the floating body (FB) of silicon 1T-DRAM and (**b**) in the grain boundary (GB) of poly-Si 1T-DRAM/@T = 300 K.

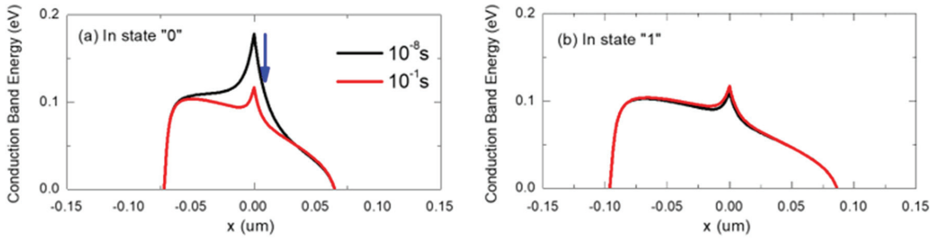

Figure 4. Conduction band energy diagram of poly-Si 1T-DRAM at two hold times (black lines, 10^{-8} s and red lines, 10^{-1} s). (**a**) During the read "0" period and (**b**) during the read "1" period.

We confirmed from our study results that the principle of data storage differs with the body material of 1T-DRAM. Silicon 1T-DRAM uses an FB as its hole storage region in the "1" state, and poly-Si 1T-DRAM uses a GB as an electron storage region in the "0" state. These results indicate why the sensing margin of silicon 1T-DRAM is dramatically reduced with decreasing T_{body}, while the margin in poly-Si 1T-DRAM is little affected by $T_{body,}$ as shown in Figure 2a,b. The reduction of FB space for holes in silicon 1T-DRAM means it cannot be scaled to short channel devices with its limited sensing margin for a thin T_{body}. However, since poly-Si 1T-DRAM uses its GB for memory operation instead of an FB, it is suitable for short channel devices even in a thin body.

3.2. The Effect of Grain Size on Sensing Margin Characteristics

A poly-Si 1T-DRAM's GB is important to its characteristics. However, a random number of GBs are distributed in a channel since the grain size of poly-Si cannot be easily controlled. Therefore, a study of the memory characteristics' dependence on the number of GBs in the channel and the grain size of poly-Si is necessary. In order to analyze this effect, structures having one to four GBs in poly-Si channel are used in our simulation, as shown in Figures 1b and 5a–c. Since the grain size means the gap between GBs, many GBs in the channel indicate that the grain size is small in these figures. In addition, we examined the three structures with different GB locations and grain size for each number of GBs to investigate the effect of GB location or grain size. Figure 5d–f shows the simulated device structure with different locations for 3 GBs. In these figures, the grain size depends on the location. For example, the grain size of Figure 5d is 50 nm, whereas that of Figure 5f is 70 nm.

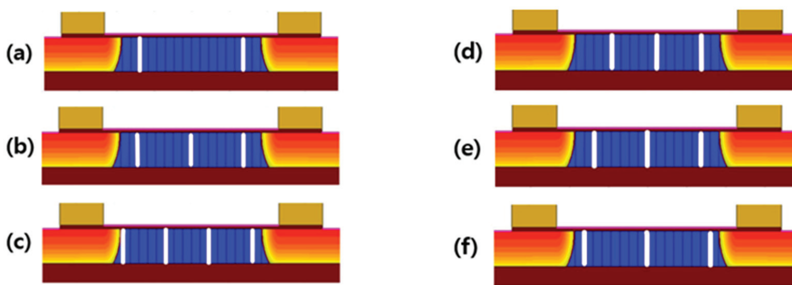

Figure 5. The simulated structure of poly-Si body 1T-DRAM with (**a**) 2 GBs; (**b**) 3 GBs; and (**c**) 4 GBs in a channel; (**d–f**) the simulated structure of 3 GBs poly-Si body 1T-DRAM with different GBs location /@T = 300 K.

Figure 6 shows the sensing margin of poly-Si 1T-DRAM as a function of the number of GBs in the channel. In Figure 6a, the sensing margin is inversely proportional to the number of GBs. This is due to increasing trapped electron charge as the number of GBs increases, as shown in Figure 6b. On the one hand, more GBs mean that the trap density in the channel increases proportionally, and therefore trapped electron charge also increase.

Since the trapped charge reduces free electrons in the poly-Si channel, the drain current of the device decreases, and this results in sensing margin degradation.

On the other hand, the GBs location and grain size have little influence on the sensing margin characteristics as compared with the number of GBs in the channel. Therefore, the number of GBs should be considered to predict the sensing margin of poly-Si 1T-DRAM.

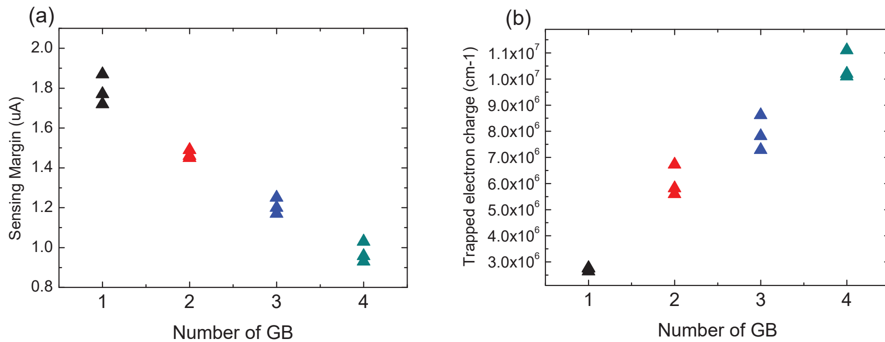

Figure 6. (**a**)Sensing margin and (**b**) trapped electron charge according to the number of GBs in the poly-Si channel of poly-Si 1T-DRAM.

4. Conclusions

This paper reports on work that a 1T-DRAM's operating characteristics differ according to its body material. The paper also illustrates the causes of the differences by analyzing the change in charge and the energy band diagrams over time. In a conventional silicon 1T-DRAM, the excess holes in the FB produce a read current difference between the "0" and "1" state. In contrast, when the body material is polycrystalline silicon, it was confirmed that the number of trapped electrons in its GB plays an important role in state distinguishment. In addition, it was verified that the same characteristics are obtained even if the T_{body} is changed.

A thin T_{body} in silicon 1T-DRAM significantly reduces the device's sensing margin, while the poly-Si 1T-DRAM retains its margin. In terms of stability, it is important for large memory windows to remain stable for memory characteristics. However, due to the lack of storage region in a thin body device, silicon has a significantly small window. It means silicon 1T-DRAM cannot have stable memory characteristics. Therefore, poly-Si 1T-DRAM has an advantage for transistor scaling because it can operate in a thin body. In addition, it enables the fabrication of a 3D stacked structure that significantly improves the degree of integration. In order to further improve the performance of poly-Si 1T-DRAM, a study focused on how to efficiently store trapped electrons in the GB is required.

In addition, this paper confirms the effect of GB properties on the sensing margin characteristics of poly-Si 1T-DRAM. The sensing margin decreases in inverse proportion to the number of GBs in the polycrystalline silicon channel due to increased trapped electron charge. It was also verified that the number of GBs in the channel rather than their locations or grain size has a significant effect on the sensing margin characteristics of poly-Si 1T-DRAM.

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References

1. Ranica, R.; Villaret, A.; Malinge, P.; Mazoyer, P.; Lenoble, D.; Candelier, P.; Jacquet, F.; Masson, P.; Bouchakour, R.; Fournel, R.; et al. A One Transistor Cell on Bulk Substrate (1T-Bulk) for Low-Cost and High Density EDRAM. In Proceedings of the Digest of Technical Papers, 2004 Symposium on VLSI Technology, Honolulu, HI, USA, 15–17 June 2004; pp. 128–129. [CrossRef]
2. Rodriguez, N.; Gamiz, F.; Cristoloveanu, S. A-RAM Memory Cell: Concept and Operation. *IEEE Electron Device Lett.* **2010**, *31*, 972–974. [CrossRef]
3. Rodriguez, N.; Cristoloveanu, S.; Gamiz, F. Novel Capacitorless 1T-DRAM Cell for 22-Nm Node Compatible With Bulk and SOI Substrates. *IEEE Trans. Electron Devices* **2011**, *58*, 2371–2377. [CrossRef]
4. Jeong, H.; Song, K.-W.; Park, I.H.; Kim, T.-H.; Lee, Y.S.; Kim, S.-G.; Seo, J.; Cho, K.; Lee, K.; Shin, H.; et al. A New Capacitorless 1T DRAM Cell: Surrounding Gate MOSFET With Vertical Channel (SGVC Cell). *IEEE Trans.Nanotechnol.* **2007**, *6*, 352–357. [CrossRef]
5. Lee, M.; Moon, T.; Kim, S. Floating Body Effect in Partially Depleted Silicon Nanowire Transistors and Potential Capacitor-Less One-Transistor DRAM Applications. *IEEE Trans. Nanotechnol.* **2012**, *11*, 355–359. [CrossRef]
6. Bawedin, M.; Cristoloveanu, S.; Flandre, D. A Capacitorless 1T-DRAM on SOI Based on Dynamic Coupling and Double-Gate Operation. *IEEE Electron Device Lett.* **2008**, *29*, 795–798. [CrossRef]
7. Giusi, G.; Iannaccone, G. Junction Engineering of 1T-DRAMs. *IEEE Electron Device Lett.* **2013**, *34*, 408–410. [CrossRef]
8. Song, K.; Jeong, H.; Lee, J.; Hong, S.; Tak, N.; Kim, Y.; Cho, Y.; Joo, H.; Kim, S.; Song, H.; et al. 55 Nm Capacitor-Less 1T DRAM Cell Transistor with Non-Overlap Structure. In Proceedings of the 2008 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2008; pp. 797–800. [CrossRef]
9. Lee, C.-W.; Yan, R.; Ferain, I.; Kranti, A.; Akhvan, N.D.; Razavi, P.; Yu, R.; Colinge, J.P. Nanowire Zero-Capacitor DRAM Transistors with and without Junctions. In Proceedings of the 10th IEEE International Conference on Nanotechnology, Seoul, Korea, 17–20 August 2010; pp. 242–245. [CrossRef]
10. Wan, J.; Le Royer, C.; Zaslavsky, A.; Cristoloveanu, S. A Compact Capacitor-Less High-Speed DRAM Using Field Effect-Controlled Charge Regeneration. *IEEE Electron Device Lett.* **2012**, *33*, 179–181. [CrossRef]
11. Ansari, M.H.R.; Navlakha, N.; Lin, J.-T.; Kranti, A. Doping Dependent Assessment of Accumulation Mode and Junctionless FET for 1T DRAM. *IEEE Trans. Electron Devices* **2018**, *65*, 1205–1210. [CrossRef]
12. Ansari, M.H.R.; Navlakha, N.; Lin, J.-T.; Kranti, A. 1T-DRAM with Shell-Doped Architecture. *IEEE Trans. Electron Devices* **2019**, *66*, 428–435. [CrossRef]
13. Lee, W.; Choi, W.Y. A Novel Capacitorless 1T DRAM Cell for Data Retention Time Improvement. *IEEE Trans. Nanotechnol.* **2011**, *10*, 462–466. [CrossRef]
14. Biswas, A.; Dagtekin, N.; Grabinski, W.; Bazigos, A.; Le Royer, C.; Hartmann, J.-M.; Tabone, C.; Vinet, M.; Ionescu, A. Investigation of Tunnel Field-Effect Transistors as a Capacitor-Less Memory Cell. *Appl. Phys. Lett.* **2014**, *104*, 092108. [CrossRef]
15. Lin, J.-T.; Huang, K.-D.; Jheng, B.-T. Performances of a Capacitorless 1T-DRAM Using Polycrystalline Silicon Thin-Film Transistors With Trenched Body. *IEEE Electron Device Lett.* **2008**, *29*, 1222–1225.
16. Kim, M.; Cho, W. Capacitorless 1T-DRAM on Crystallized Poly-Si TFT. *J. Nanosci. Nanotechnol.* **2011**, *11*, 5608–5611. [CrossRef] [PubMed]
17. Han, J.-W.; Ryu, S.-W.; Kim, D.-H.; Kim, C.-J.; Kim, S.; Moon, D.-I.; Choi, S.-J.; Choi, Y.-K. Fully Depleted Polysilicon TFTs for Capacitorless 1T-DRAM. *IEEE Electron Device Lett.* **2009**, *30*, 742–744.
18. Baek, M.-H.; Lee, S.-H.; Kwon, D.W.; Seo, J.Y.; Park, B.-G. Hole Trapping Phenomenon at the Grain Boundary of Thin Poly-Si Floating-Body MOSFET and Its Capacitor-Less DRAM Application. *J. Nanosci. Nanotechnol.* **2017**, *17*, 2906–2990. [CrossRef]
19. Jang, T.; Baek, M.-H.; Kim, H.; Park, B.-G. An Analysis of Hole Trapping at Grain Boundary or Poly-Si Floating-Body. *J. Nanosci. Nanotechnol.* **2018**, *18*, 6584–6587. [CrossRef] [PubMed]
20. Chen, Y.-T.; Sun, H.-C.; Huang, C.-F.; Wu, T.-Y.; Liu, C.W.; Hsu, Y.-J.; Chen, J.-S. Capacitorless 1T Memory Cells Using Channel Traps at Grain Boundaries. *IEEE Electron Device Lett.* **2010**, *31*, 1125–1127. [CrossRef]
21. Colalongo, L.; Valdinoci, M.; Baccarani, G.; Migliorato, P.; Tallarida, G.; Reita, C. Numerical Analysis of Poly-TFTs under off Conditions. *Solid-State Electron.* **1997**, *41*, 627–633. [CrossRef]

22. Kim, H.-J.; Kang, I.-M.; Cho, S.-J.; Sun, W.-K.; Shin, H.-S. Analysis of operation characteristics of junctionless poly-Si 1T-DRAM in accumulation mode. *Semicond. Sci. Technol.* **2019**, *34*, 105007. [CrossRef]
23. Ram, M.S.; Abdi, D.B. Single Grain Boundary Dopingless PNPN Tunnel FET on Recrystallized Polysilicon: Proposal and Theoretical Analysis. *IEEE J. Electron Devices Soc.* **2015**, *3*, 291–296. [CrossRef]

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A Simulation Study of a Gate-All-Around Nanowire Transistor with a Core–Insulator

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Abstract: Ultra-low power and high-performance logical devices have been the driving force for the continued scaling of complementary metal oxide semiconductor field effect transistors which greatly enable electronic devices such as smart phones to be energy-efficient and portable. In the pursuit of smaller and faster devices, researchers and scientists have worked out a number of ways to further lower the leaking current of MOSFETs (Metal oxide semiconductor field effect transistor). Nanowire structure is now regarded as a promising candidate of future generation of logical devices due to its ultra-low off-state leaking current compares to FinFET. However, the potential of nanowire in terms of off-state current has not been fully discovered. In this article, a novel Core–Insulator Gate-All-Around (CIGAA) nanowire has been proposed, investigated, and simulated comprehensively and systematically based on 3D numerical simulation. Comparisons are carried out between GAA and CIGAA. The new CIGAA structure exhibits low off-state current compares to that of GAA, making it a suitable candidate of future low-power and energy-efficient devices.

Keywords: CMOS; core-insulator; gate-all-around; field effect transistor; GAA; nanowire

1. Introduction

Ultra-low power and high-performance logical devices have been the driving force for the continued scaling of complementary metal oxide semiconductor field effect transistors which greatly enable electronic devices such as smart phones to be energy-efficient and portable, while system scaling enabled by the Moore's law is facing challenges due to the scarcity of resources such as power and interconnect bandwidth. Constrained by the limited capacity of battery, portable electronic devices are hard to have an "always-on" feature and have to be recharged frequently, causing great inconvenience to users. To reduce the overall power consumption, researchers have worked out a number of ways to reduce the off-state current of CMOS devices [1]. By fabricating the whole system on anSOI (Silicon on insulator) wafer, the stand-by current of the system can greatly reduce due to the low off-state current of SOI MOSFET [2]. However, the SOI MOSFET has self-heating effect due to poor heat conductivity of buried silicon dioxide layer (BOX) which increases device operating temperature, reduces carrier mobility as well as causes performance degradation [3,4]. By introducing new physical mechanics into CMOS devices, researchers are able to lower the subthreshold slope of transistors and hence reduce the leaking current of whole system. These types of devices include Impact Ionization MOS (IMOS) [5] and Tunnel Field Effect Transistors (TFET) [6]. Technically, IMOS is a reverse biased p-i-n diode with a control gate. The control gate is used to control impact ionization phenomenon between two junctions. The avalanche breakdown is a very fast and gated diode pulsed into breakdown can show subthreshold slopes much lower than 60 mV/dec [7], and thus exhibits lower off-state current compared with a conventional MOSFET [8]. However, due to the need of drastic doping profile, the fabrication of IMOS requires costly millisecond annealing techniques which

greatly limits its application [9]. A tunnel field effect transistor is designed using the band-to-band tunneling effect. The carriers are injected by a band-to-band tunneling effect from a valence band of source for a N-type TFET, which is totally different from conventional CMOS devices that use thermionic emission [10]. The physical mechanics of TFET allow them not to be constrained by the Boltzmann limit (about 60 mV/dec at room temperature). Thus, TFET has the potential to be used as low-power devices for its extremely low off-state current. However, the TFETs fabricated are not competitive with conventional MOSFETs which are based on thermionic emission. Low on-state current and high average subthreshold slope (V_g-dependent subthreshold slope) are main limitations of TFET devices [11,12]. Gate-All-Around (GAA) CMOS FET is based on conventional CMOS FET; it features a circular gate around the channel. GAA MOSFET is compatible with an existing CMOS fabrication process; it has the superior electrostatic control compared with FinFET and planar CMOS FET. The ITRS predicted that, beyond 2020 [1], a transition to Gate-All-Around and vertical nanowires devices will be needed when there will be no room left for the scaling because GAA devices are the ultimate structure in terms of electrostatic control to scale to the shortest possible effective channel length. While we found the potential of GAA devices has not been fully discovered, by introducing a core-Insulator into conventional GAA devices (we called it a Core–Insulator Gate-All-Around nanowire), the off-state current is expected to be further lowered, which makes it more suitable for fabricating low-power devices. The introduction of a Core–Insulator does not have any exotic materials, so it is highly compatible with a current fabrication process. Our experiments show that, because of the presence of Core–Insulator, the off-state current is lowered by more than two times, and it shows better subthreshold characteristics. We believe that this newly proposed structure can be a promising candidate of future low-power and energy-efficient CMOS devices.

2. Device Structure and Experiment Methodology

2.1. Descriptions of CIGAA Structure

The difference between conventional GAA and CIGAA (Core-Insulator Gate-All-Around) is that a CIGAA structure has a Core–Insulator between the channel, as shown in Figure 1. The material of Core–Insulator can be SiO_2, Si_3N_4 and so on, and the impact of different material of Core–Insulator will be addressed in the following paragraph. We use HfO_2 as a gate dielectric because it has a low leaking current and high dielectric constant, which can greatly improve the performance of the device without increasing the gate leaking current. The channel of CIGAA structure is not a solid cylinder as that of conventional GAA structure; it is a tubular channel. The gate metal should be carefully selected to tune the work function for a particular threshold voltage requirement.

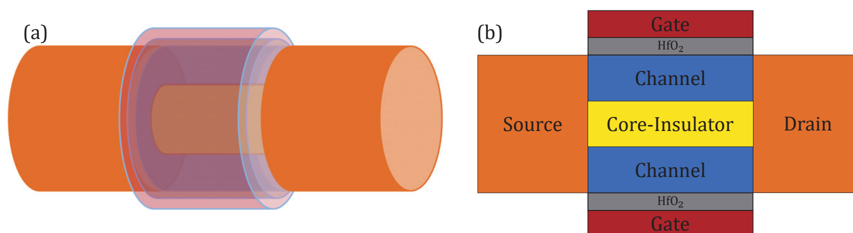

Figure 1. The schematic 3D structure and cross section of CIGAA: (**a**) 3D view of CIGAA; (**b**) cross-sectional view of CIGAA. The illustrations are not depicted proportionally to the really devices; we made some exaggeration for a clear visualization.

2.2. Simulation Physical Models

Our simulation platform is Sentaurus TCAD 2017 Version N-2017.09 [13]. To describe the current densities of electrons and holes, we introduced a Drift–Diffusion [14] model that takes into account the contribution of electron affinity, the band gap as well as the spatial variations [15,16] of the electrostatic

potential. Because the oxide thickness and channel width have reached quantum-mechanical length scales, the wave nature of electrons and holes can no longer be neglected, thus Density-Gradient [17] is used to simulate quantization effects. In order to describe the effects of electron–hole scattering, the screening of ionized impurities by charge carriers, and the clustering of impurities, Philips Unified Mobility [18] is used. Since HfO_2/Silicon interface can lead to a mobility degradation [19,20], we also must take this into consideration by including a Lombardi Mobility Degradation model [21]. Hurkx Trap Assisted Tunneling models [22–24] are incorporated to simulate the tunneling effects at such small dimensions. In addition, a quantum potential model [25] was also taken into consideration. Because the source and drain are highly doped, we use a band gap narrowing model [26] to simulate this effect.

2.3. Structure Parameters Used for Simulation

All the parameters of our experiment are shown in Table 1 and Figure 2. Both structures have the same diameter as well as doping profiles. The source/drain doping concentration is 1×10^{20} atoms/cm^3. Channel is lightly doped, which is 1×10^{15} atoms/cm^3. For this article, channel length is fixed to 15 nm and the length of drain and source are both fixed to 10 nm. The diameter of Core–Insulator is set from 2.0 nm to 14 nm. The gate dielectric is HfO_2, and the thickness is shown in a table. For comparison, we have also simulated a conventional GAA nanowire of the same overall dimensions.

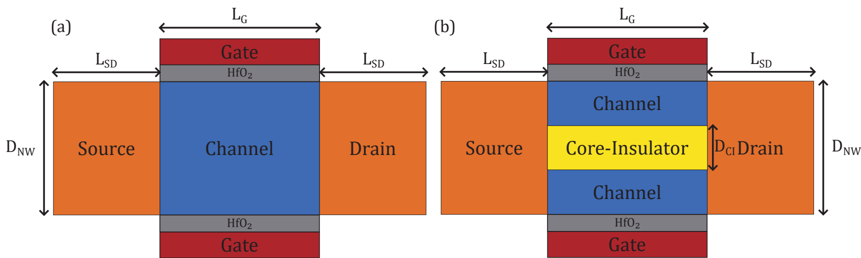

Figure 2. The overall dimension of CIGAA and GAA: (**a**) parameters used for GAA; (**b**) parameters used for CIGAA.

Table 1. Design parameter values for CIGAA and GAA.

Variables	Values
Gate Length (L_g)	15 nm
HfO_2 Thickness	1.0 nm/2.0 nm
Channel Thickness ($D_{NW}/2D_{CI}/2$)	1.0 to 8.0 nm
Source/Drain Length (L_{SD})	10 nm
Core–Insulator Diameter (D_{CI})	2 nm to 14 nm
Source/Drain Doping	1×10^{20}
Channel Doping	1×10^{15}
Core–Insulator	Si_3N_4, SiO_2, HfO_2

2.4. Considerations of Workfunction

Ideally, conventional GAA and CIGAA will have different threshold voltage although they have same geometric parameters, since the presence of Core–Insulator will affect the device threshold voltage. In order to better illustrate and compare the performance of two structures, in other words, to have a fair comparison, we must tune their gate workfunction to ensure they have same threshold voltage, so that we can compare their performance by the same benchmark. It is noteworthy that it is hard to tune the workfunction at any desired value in the real fabrication process, although it can be

easily achieved in TCAD simulation; all we want is to compare the performance difference between CIGAA and GAA under TCAD simulation.

2.5. Suggested Fabrication Process Flow for CIGAA

Based on the previous works of nanotube MOSFETs [27–29], the suggested fabrication process flow for CIGAA is shown in Figure 3. The CIGAA can be realized using the process flow suggested in [28] with some major changes. The first steps of the fabrication process is to form a cylindrical-shaped outer silicon layer with a sidewall using electron beam lithography (EBL) and sidewall deposition (Figure 3a–e), as suggested in [28]. Then, the source side spacer is formed using low-pressure chemical vapor deposition (LPCVD), and the following step (Figure 3f) is to remove unnecessary spacer material that is covered on the sidewall and cylindrical-shaped outer silicon layer using lithography and etching. Subsequently, gate oxide should be formed; the first is to deposit a thin layer HfO_2 using low-pressure chemical vapor deposition (LPCVD). To remove redundant HfO_2, lithography is used to protect gate oxide and anisotropic etching to remove unnecessary HfO_2, as shown in Figure 3g–i. The next step is to form and partial removal of gate metal, as shown in Figure 3j,k. Subsequently, a sacrificial layer surrounding the top spacer is deposited using low-pressure chemical vapor deposition (LPCVD) and chemical mechanical polishing (CMP), which is shown in Figure 3l,m. Using selective etching followed by deposition of nitride and removal of the sacrificial layer, as shown in Figure 3n–p, the structure is prepared to form Core–Insulator. By anisotropic etching of silicon, the channel is formed, as shown in Figure 3q. The following step is to deposit Core–Insulator; this is illustrated in Figure 3r. Finally, the drain side is deposited with silicon and spacer, and the contacts are formed to finalized the device, as shown in Figure 3s–u.

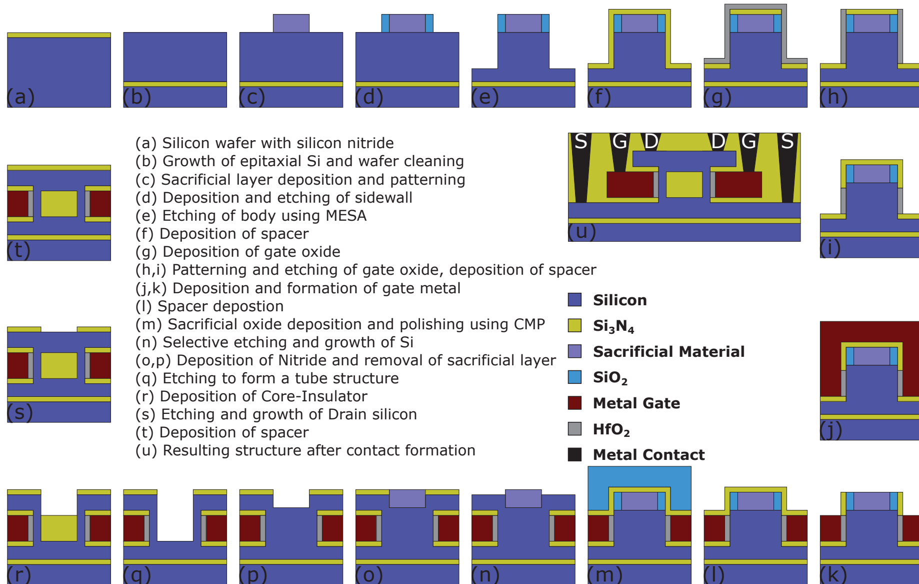

Figure 3. Suggested fabrication process flow for CIGAA.

3. Results and Discussions

3.1. Basic Characteristics of CIGAA and GAA

Figure 4a shows the result of on-state current (I_{on}). The on-state current of both structures increase linearly when channel thickness (T_{ch}) increases, since the increment of channel thickness means that

the effective width of channel will also increase. When T_{ox} is same, CIGAA exhibits a slightly lowered on-state current compared with that of GAA. The on-state current degradation of CIGAA is due to the reduction of the total volume of channel because of the presence of Core–Insulator, which results in smaller effective channel width. However, the inversion layer forms closely to the interface of HfO_2/Silicon and is extremely thin; the total on-state current only has a small degradation. In addition, Figure 5a,b show that the on-state electron density of CIGAA at the HfO_2/Silicon interface is much higher than that of GAA, which explains the negligible degradation of the on-state current. Both structures show an increment of off-state current when channel thickness increases, as shown in Figure 4b. The off-state current of CIGAA is about 2 to 5 times lower than that of GAA, which means that CIGAA has the nature to be used to fabricate a low-power device. The good performance of an off-state current can be clearly explained by examining the electron density plot. Figure 6a,b show the electron density of GAA and CIGAA at off-state (V_{GS} = 0 V), respectively. It is evident that both two structures have almost the same electron density distribution in the channel. However, when we examine the CIGAA, the inner part of the channel where Core–Insulator is located should have the identical electron density distribution with that of GAA if the silicon is not replaced by Core–Insulator, which means that the current path is narrower than that of GAA, resulting in a smaller off-state current.

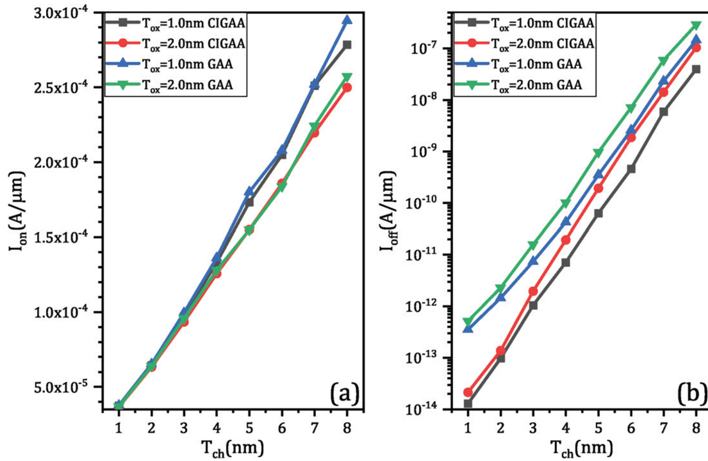

Figure 4. The simulation results of CIGAA and GAA: (**a**) on-state current (I_{on}) of CIGAA and GAA; (**b**) off-state current (I_{off}) of CIGAA and GAA. Both of the two figures are plotted when D_{CI} = 4.0 nm.

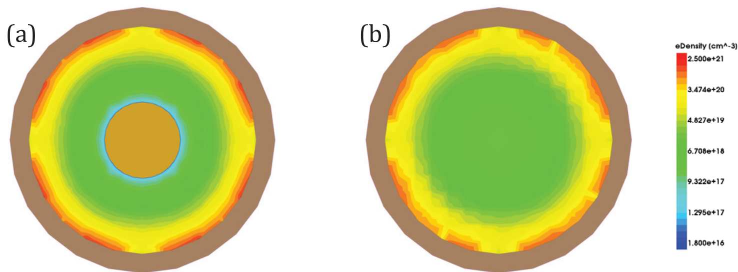

Figure 5. The electron density plot of CIGAA and GAA, the devices are at on state: (**a**) electron density of GAA; (**b**) electron density of CIGAA. Both figures are plotted when V_{GS} = V_{DS}, V_{DS} = 1 V. Metal gate and part structures are not included in the figure for clarity.

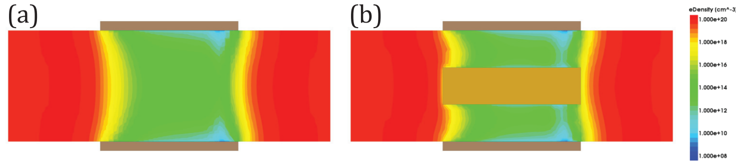

Figure 6. The electron density plot of CIGAA and GAA, the devices are at off state: (**a**) electron density of GAA; (**b**) electron density of CIGAA. Both figures are plotted when V_{GS} = 0 V, V_{DS} = 1 V. Metal gate and part structures are not included in the figure for clarity.

The characteristics of GAA and CIGAA in terms of subthreshold slope, switching ratio, and drain-induced barrier lowing are shown in Figure 7a–c, respectively. The subthreshold slope of CIGAA always outperforms that of GAA when they have the same T_{ox}. Equation (1) [30] can perfectly explain the good results of CIGAA. Due to the reduction of off-state current, while I_{ON} and V_{DD} remain constant, the subthreshold slope is lowered:

$$S_{avg} = \frac{V_T - V_{GOFF}}{\log_{10} \frac{I_T}{I_{OFF}}} \approx \frac{V_{DD}}{\log_{10} \frac{I_{ON}}{I_{OFF}}} \tag{1}$$

Since the off-state current are lowered, the switching ratio of CIGAA is expected to be lower than that of GAA, as shown in Figure 7b.

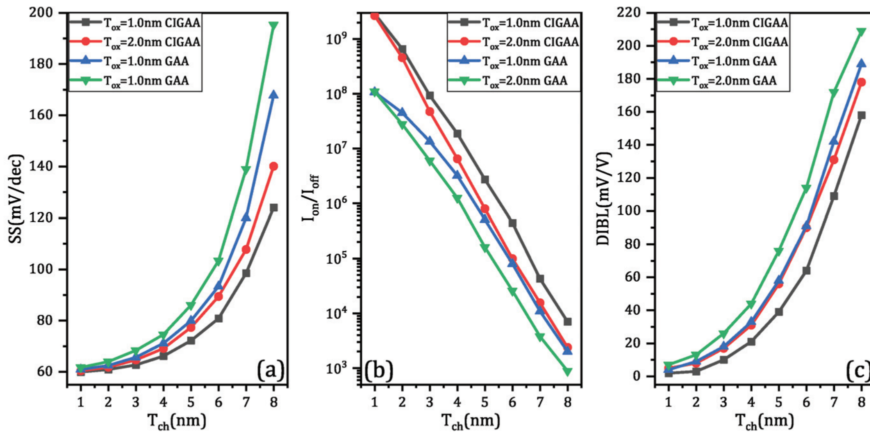

Figure 7. The simulation results of CIGAA and GAA: (**a**) subthreshold slope (SS) of CIGAA and GAA; (**b**) switching ratio (I_{on}/I_{off}) of CIGAA and GAA; (**c**) drain-induced barrier lowering (DIBL) of CIGAA and GAA. All three of the figures are plotted when D_{CI} = 4.0 nm.

3.2. Impact of Core–Insulator Diameter and Material on Device Performance

We have set up experiments to further investigate the impact of Core–Insulator diameter and material on device performance. To simplify the experiments, we fixed the nanowire diameter to 8 nm (as shown in Table 2) and the Core–Insulator materials are Si_3N_4, SiO_2, and HfO_2.

Table 2. Design parameter values for CIGAA.

Channel Thickness (nm)	Core–Insulator Diameter (nm)
1	7
2	6
3	5
4	4
5	3
6	2
7	1

The results in terms of on-state current and off-state current are shown in Figure 8a,b, respectively. Changing of Core–Insulator material only have a minor effect on on-state current based on Figure 8a. In fact, as D_{CI} increases, the impact of Core–Insulator on on-state current become more and more significant. Unlike on-state current, the changing of Core–Insulator material has a conspicuous influence on the off-state current. According to the simulation results (as shown in Figure 8b), SiO_2 can effectively suppress current flow under off-state, HfO_2 is the worst material to achieve low off-state current among the three, and Si_3N_4 is better than HfO_2. No matter what the Core–Insulator material is, the on-state current will decrease when D_{CI} increases, since D_{CI} increases means that channel thickness decreases which lead to the reduction of an effective channel width. Likewise, the off-state current will decrease when D_{CI} increases because a larger Core–Insulator helps to suppress off-state current.

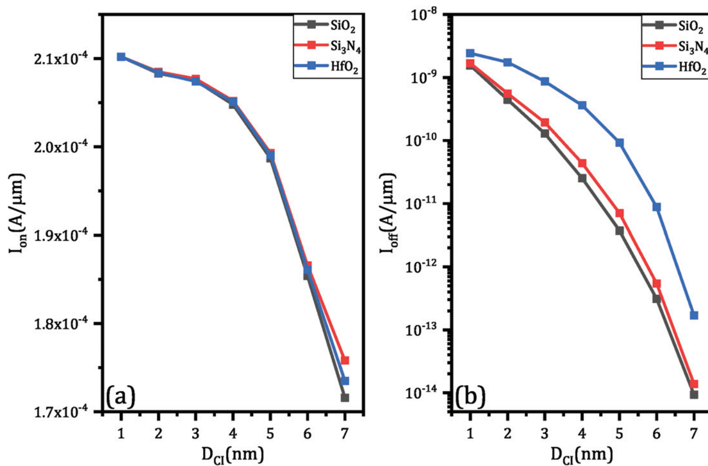

Figure 8. The simulation results of CIGAA and GAA in terms of different Core–Insulator material and D_{CI}: (**a**) on-state current. (**b**) off-state current. Both figures are plotted when D_{NW} is fixed to 8 nm.

As for subthreshold swing, switching ratio and DIBL, increasing D_{CI} results in better performance, as shown in Figure 9a–c, respectively. SiO_2 can effectively enhance device performance, Si_3N_4 is less useful than SiO_2 and HfO_2 is the worst choice. In real fabrication, it is important to decide the D_{CI} according to application requirements. SiO_2 is the best material among the three to achieve better performance. Since larger D_{CI} can reduce on-state current, so the first thing to do is to select D_{CI}, which enables on-state current to be large enough.

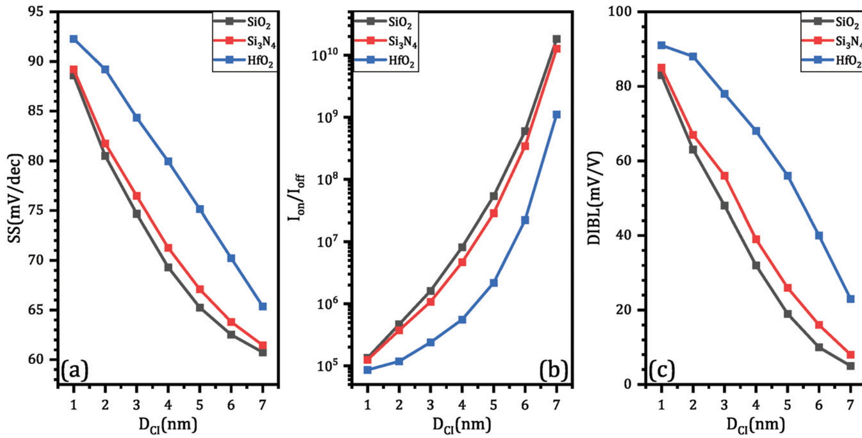

Figure 9. The simulation results of CIGAA and GAA in terms of different Core–Insulator material and D_{CI}: (**a**) subthreshold swing (SS); (**b**) switching ratio (I_{on}/I_{off}); (**c**) drain-induced barrier lowering (DIBL). All three figures are plotted when D_{NW} is fixed to 8 nm.

3.3. Impact of Core–Insulator Length on Device Performance

Due to the limitations of existing fabrication technology, it is hard to fabricate a device that has a Core–Insulator exactly the same length as its channel, which is shown in Figure 10. Thus, we have to further investigate the impact of Core–Insulator length on device performance. There are two possible situations: one is that the Core–Insulator extends itself into source and drain by L_{ext}, as shown in Figure 10a. The other is that the Core–Insulator recesses itself into channel by L_{ext}, as shown in Figure 10b.

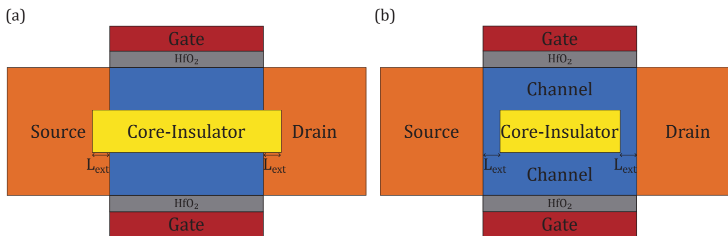

Figure 10. The illustrations which show the issue of Core–Insulator's extension and contraction: (**a**) the Core–Insulator extends itself into source and drain by L_{ext}; (**b**) the Core–Insulator recesses itself into channel by L_{ext}.

The results are shown in Table 3. A positive L_{ext} represents the situation that is shown in Figure 10a, and a negative L_{ext} represents the situation that is shown in Figure 10b. From the results, we can notice that the performance of CIGAA only has slight variations and can be neglected. When L_{ext} changes from −2 nm to 2 nm, the Core–Insulator extends itself into source, resulting in a volume reduction of the channel. This reduction causes the effective channel width to be further lowered, which finally results in a reduction in on-state and off-state current. The simulation results reveal that a small variation in fabrication will not cause noticeable performance degradation.

Table 3. Impact of Core–Insulator Length on Device Performance.

L_{ext} (nm)	ΔI_{on} (%)	ΔI_{off} (%)	$\Delta I_{on}/I_{off}$ (%)	ΔSS (%)	ΔDIBL (mV)
−2	0.3	0.5	−0.5	0.7	1
−1	0	0.8	−0.8	0.4	1
0	0	0	0	0	0
1	−0.5	−0.7	0.6	−0.5	0
2	−1.1	−0.4	0.9	−0.7	−1

3.4. Parasitic Capacitance of CIGAA and GAA

One important concern about the newly proposed structure is its parasitic capacitance, since the presence of Core–Insulator may affect the charge distribution of CIGAA. We have investigated the impact of Core–Insulator materials, channel thickness, and Core–Insulator diameter on the device's parasitic capacitance. Figure 11a,b show that the changing of Core–Insulator material will significantly affect the device's parasitic capacitance. When the Core–Insulator material is HfO_2, the gate capacitance is about three times larger than that of CIGAA with Si_3N_4 Core–Insulator, six times larger than that of CIGAA with SiO_2 Core–Insulator. As channel thickness increases, the gate capacitance will also increase, as shown in Figure 11a. When T_{ox} is the same, CIGAA with SiO_2 Core–Insulator shows the smallest gate capacitance, while CIGAA with HfO_2 Core–Insulator shows the largest gate capacitance. In addition, the gate capacitance of CIGAA with SiO_2 Core–Insulator and CIGAA with Si_3N_4 Core–Insulator are lower than that of GAA. When Core–Insulator diameter increases, the gate capacitance of CIGAA increases simultaneously. HfO_2 cannot be used as Core–Insulator material because it provides fairly large gate capacitance, while Si_3N_4 and SiO_2 can be used as Core–Insulator material. SiO_2 is the best material among the three, and it provides the smallest gate capacitance.

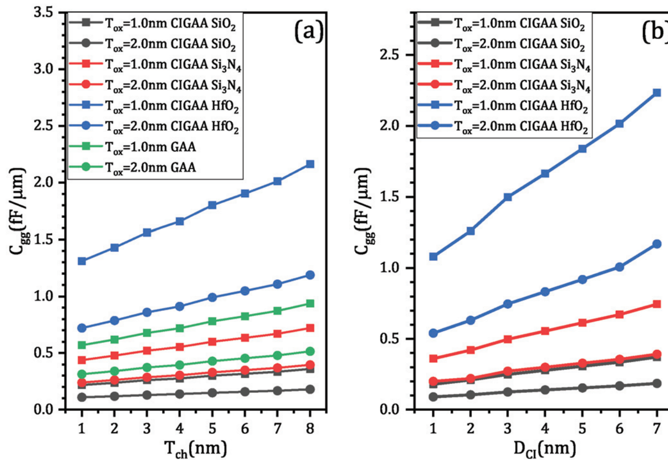

Figure 11. Gate capacitance dependence on: (**a**) channel thickness; (**b**) the Core–Insulator diameter D_{CI}.

4. Conclusions

We have studied the device performance of our proposed CIGAA nanowire using 3D TCAD simulation. Due to CIGAA's lowered off-state current enabled by Core–Insulator, it shows high on-state current, low off-state current, low subthreshold swing, and high switching ratio. CIGAA has the potential to be used to fabricate low-power systems. Thus, the CIGAA nanowire is a promising candidate to extend CMOS scaling roadmap and future low power CMOS devices.

Author Contributions: Y.Z. and K.H. participated in the design of this study, and they both performed the statistical analysis, data acquisition, data analysis, and manuscript preparation. Y.Z. carried out data analysis, manuscript preparation, collected important background information, and drafted the manuscript. J.L. provided assistance for data acquisition and manuscript review. All authors have read and agreed to the published version of the manuscript.

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Abbreviations

The following abbreviations are used in this manuscript:

BOX	Buried oxide layer
CIGAA	Core-Insulator Gate-All-Around
CMOS	Complementary metal oxide semiconductor
CMP	Chemical mechanical polishing
EBL	Electron beam lithography
FET	Field effect transistor
IMOS	Impact Ionization MOS
ITRS	International Technology Roadmap for Semiconductors
GAA	Gate-All-Around
LPCVD	Low-pressure chemical vapor deposition
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
SOI	Silicon on insulator
TCAD	Technology computer aided design
TFET	Tunnel field effect transistor

References

1. Carballo, J.A.; Chan, W.T.; Gargini, P.A.; Kahng, A.B.; Nath, S. Itrs 2.0: Toward a re-framing of the semiconductor technology roadmap. In Proceedings of the 2014 IEEE 32nd International Conference on Computer Design (ICCD), Seoul, Korea, 19–22 October 2014; pp. 139–146.
2. Bruel, M. Silicon on insulator material technology. *Electron. Lett.* **1995**, *31*, 1201–1202. [CrossRef]
3. Orouji, A.A.; Moghadam, H.A.; Dideban, A. Double window partial soi-ldmosfet: A novel device for breakdown voltage improvement. *Phys. E Low-Dimens. Syst. Nanostruct.* **2010**, *43*, 498–502. [CrossRef]
4. Zhang, B.; Li, Z.; Hu, S.; Luo, X. Field enhancement for dielectric layer of high-voltage devices on silicon on insulator. *IEEE Trans. Electron Devices* **2009**, *56*, 2327–2334. [CrossRef]
5. Ramaswamy, S.; Kumar, M.J. Junctionless impact ionization mos: Proposal and investigation. *IEEE Trans. Electron Devices* **2014**, *61*, 4295–4298. [CrossRef]
6. Lu, H.; Seabaugh, A. Tunnel field-effect transistors: State-of-the-art. *IEEE J. Electron Devices Soc.* **2014**, *2*, 44–49. [CrossRef]
7. Gopalakrishnan, K.; Griffin, P.B.; Plummer, J.D. Impact ionization mos (i-mos)—Part I: Device and circuit simulations. *IEEE Trans. Electron Devices* **2004**, *52*, 69–76. [CrossRef]
8. Toh, E.H.; Wang, G.H.; Chan, L.; Lo G.Q.; Samudra, G.; Yeo, Y.C. Strain and materials engineering for the i-mos transistor with an elevated impact-ionization region. *IEEE Trans. Electron Devices* **2007**, *54*, 2778–2785. [CrossRef]

9. Colinge, J.P.; Lee, C.W.; Afzalian, A.; Akhavan, N.D.; Yan, R.; Ferain, I.; Razavi, P.; O'neill, B.; Blake, A.; White, M.; et al. Nanowire transistors without junctions. *Nat. Nanotechnol.* **2010**, *5*, 225. [CrossRef] [PubMed]
10. Koga, J.; Toriumi, A. Three-terminal silicon surface junction tunneling device for room temperature operation. *IEEE Electron Device Lett.* **1999**, *20*, 529–531. [CrossRef]
11. Settino, F.; Lanuzza, M.; Strangio, S.; Crupi, F.; Palestri, P.; Esseni, D.; Selmi, L. Understanding the potential and limitations of tunnel fets for low-voltage analog/mixed-signal circuits. *IEEE Trans. Electron Devices* **2017**, *64*, 2736–2743. [CrossRef]
12. Boucart, K.; Ionescu, A.M. Double-gate tunnel fet with high-K gate dielectric. *IEEE Trans. Electron Devices* **2007**, *54*, 1725–1733. [CrossRef]
13. *TCAD Sentaurus and N Version*; Synopsys Inc.: Mountain View, CA, USA, 2017.
14. Singh, N.; Agarwal, A.; Bera, L.K.; Liow, T.Y.; Yang, R.; Rustagi, S.C.; Tung, C.H.; Kumar, R.; Lo, G.Q.; Balasubramanian, N.; et al. High-performance fully depleted silicon nanowire (diameter/spl les/5 nm) gate-all-around cmos devices. *IEEE Electron Device Lett.* **2006**, *27*, 383–386. [CrossRef]
15. Pezzimenti, F.; Bencherif, H.; Yousfi, A.; Dehimi, L. Current-voltage analytical model and multiobjective optimization of design of a short channel gate-all-around-junctionless mosfet. *Solid-State Electron.* **2019**, *161*, 107642. [CrossRef]
16. Pezzimenti, F. Modeling of the steady state and switching characteristics of a normally off 4h-sic trench bipolar-mode fet. *IEEE Trans. Electron Devices* **2013**, *60*, 1404–1411. [CrossRef]
17. Zhuge, J.; Tian, Y.; Wang, R.; Huang, R.; Wang, Y.; Chen, B.; Liu, J.; Zhang, X.; Wang, Y. High-performance si nanowire transistors on fully si bulk substrate from top-down approach: simulation and fabrication. *IEEE Trans. Nanotechnol.* **2009**, *9*, 114–122. [CrossRef]
18. Klaassen, D.B.M. A unified mobility model for device simulation—I. model equations and concentration dependence. *Solid-State Electron.* **1992**, *35*, 953–959. [CrossRef]
19. Jaikumar, M.G.; Karmalkar, S. Calibration of mobility and interface trap parameters for high temperature tcad simulation of 4h-sic vdmosfets. In *Materials Science Forum*; Trans Tech Publication: Zürich, Switzerland, 2012; Volume 717, pp. 1101–1104.
20. Singh, J.; Kumar, M.J. A planar junctionless fet using sic with reduced impact of interface traps: Proposal and analysis. *IEEE Trans. Electron Devices* **2017**, *64*, 4430–4434. [CrossRef]
21. Lombardi, C.; Manzini, S.; Saporito, A.; Vanzi, M. A physically based mobility model for numerical simulation of nonplanar devices. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **1988**, *7*, 1164–1171. [CrossRef]
22. Marchi, M.D.; Sacchetto, D.; Frache, S.; Zhang, J.; Gaillardon, P.; Leblebici, Y.; Micheli, G.D. Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire fets. In Proceedings of the 2012 International Electron Devices Meeting, San Francisco, CA, USA, 10–13 December 2012; pp. 4–8.
23. Marchi, M.D.; Zhang, J.; Frache, S.; Sacchetto, D.; Gaillardon, P.; Leblebici, Y.; Micheli, G.D. Configurable logic gates using polarity-controlled silicon nanowire gate-all-around fets. *IEEE Electron Device Lett.* **2014**, *35*, 880–882. [CrossRef]
24. Yang, J.; He, J.; Liu, F.; Zhang, L.; Liu, F.; Zhang, X.; Chan, M. A compact model of silicon-based nanowire mosfets for circuit simulation and design. *IEEE Trans. Electron Devices* **2008**, *55*, 2898–2906. [CrossRef]
25. Brown, A.R.; Watling, J.R.; Roy, G.; Riddet, C.; Alexander, C.L.; Kovac, U.; Martinez, A.; Asenov, A. Use of density gradient quantum corrections in the simulation of statistical variability in mosfets. *J. Comput. Electron.* **2010**, *9*, 187–196. [CrossRef]
26. Palankovski, V.; Kaiblinger-Grujin, G.; Selberherr, S. Study of dopant-dependent band gap narrowing in compound semiconductor devices. *Mater. Sci. Eng. B* **1999**, *66*, 46–49. [CrossRef]
27. Fahad, H.M.; Hussain, M.M. High-performance silicon nanotube tunneling fet for ultralow-power logic applications. *IEEE Trans. Electron Devices* **2013**, *60*, 1034–1039. [CrossRef]
28. Musalgaonkar, G.; Sahay, S.; Saxena, R.S.; Kumar, M.J. Nanotube tunneling fet with a core source for ultrasteep subthreshold swing: A simulation study. *IEEE Trans. Electron Devices* **2019**, *66*, 4425–4432. [CrossRef]

29. Tekleab, D.; Tran, H.H.; Sleight, J.W.; Chidambarrao, D. Silicon Nanotube Mosfet. U.S. Patent 8,871,576, 28 October 2014.
30. Ionescu, A.M.; Riel, H. Tunnel field-effect transistors as energy-efficient electronic switches. *Nature* **2011**, *479*, 329. [CrossRef]

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A Novel Germanium-Around-Source Gate-All-Around Tunnelling Field-Effect Transistor for Low-Power Applications

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Abstract: This paper presents a germanium-around-source gate-all-around tunnelling field-effect transistor (GAS GAA TFET). The electrical characteristics of the device were studied and compared with those of silicon gate-all-around and germanium-based-source gate-all-around tunnel field-effect transistors. Furthermore, the electrical characteristics were optimised using Synopsys Sentaurus technology computer-aided design (TCAD). The GAS GAA TFET contains a combination of around-source germanium and silicon, which have different bandgaps. With an increase in the gate-source voltage, band-to-band tunnelling (BTBT) in silicon rapidly approached saturation since germanium has a higher BTBT probability than silicon. At this moment, germanium could still supply current increment, resulting in a steady and steep average subthreshold swing (SS_{AVG}) and a higher ON-state current. The GAS GAA TFET was optimised through work function and drain overlapping engineering. The optimised GAS GAA TFET exhibited a high ON-state current (I_{ON}) (11.9 µA), a low OFF-state current (I_{OFF}) (2.85×10^{-9} µA), and a low and steady SS_{AVG} (57.29 mV/decade), with the OFF-state current increasing by 10^7 times. The GAS GAA TFET has high potential for use in low-power applications.

Keywords: band-to-band tunnelling (BTBT); tunnelling field-effect transistor (TFET); germanium-around-source gate-all-around TFET (GAS GAA TFET); average subthreshold swing

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1. Introduction

Owing to rapid advances in semiconductor device technology, fifth-generation communication devices, wearable devices, Internet of Things, and numerous information technology devices have been developed. In the scaling of semiconductor devices to the nanoscale regime in accordance with Moore's law, power consumption is one of the major impediments. Decreasing the supply voltage is an effective way to reduce power consumption. However, in conventional metal-oxide-semiconductor field-effect transistors (MOSFETs), subthreshold swing (SS) is limited to 60 mV/decade ($SS = (kT/q) \times \ln 10$) at room temperature. This limitation prevents the supply voltage from being reduced at the same pace as the scaling of the physical dimensions of semiconductor devices [1–5]. To overcome this problem, researchers have been studying devices with a steep SS. Owing to their conduction mechanisms, such as impact ionization and band-to-band tunnelling (BTBT), differing from that of conventional MOSFETs, the ionization MOS (I-MOS), which is based on impact ionization, and tunnelling field-effect transistor (TFET), which is based on BTBT, can achieve the SS, lower than 60 mV/decade. Therefore, both these transistors have attracted considerable research interest. However, I-MOS is not suitable for low-power applications owing to its high breakdown voltage [6–9]. By contrast, TFETs provide a

steeper SS, a lower OFF-state current (I_{OFF}) and a lower supply voltage compared to conventional MOSFETs [10–15] and are suitable for low-power applications.

As mentioned, TFETs are based on BTBT conduction mechanism. This implies that the flow of drain current in n-channel-TFET occurs through tunnelling of charge carriers from the valence band of the source to the conduction band of the channel region [16]. Consequently, TFETs have a low I_{OFF} and can achieve a sub-60 mV/decade SS. The task of reducing the SS has drawn considerable attention and many studies have been conducted in this regard. The minimum point subthreshold swing (SS_{MIN}) was 5 mV/decade in [17] and 11 mV/decade in [18]. However, focusing only on reducing SS_{MIN} is insufficient. In low-power applications, the average subthreshold swing (SS_{AVG}) is far more significant than SS_{MIN} [3]. SS_{AVG} is generally calculated as

$$SS_{\mathrm{AVG}} = \frac{V_{\mathrm{T}} - V_{\mathrm{OFF}}}{log(I_{\mathrm{T}}) - log(I_{\mathrm{OFF}})}$$

where V_{T} is the threshold voltage, I_{T} is the current at V_{T}, and V_{OFF} is the gate voltage in the OFF-state. Unfortunately, in conventional Si TFETs, as the gate-source voltage increases, BTBT rapidly approaches saturation, which causes SS_{AVG} to increase dramatically. Hence, unlike conventional MOSFETs where SS_{AVG} is approximately equal to SS_{MIN}, the value of SS_{AVG} in conventional Si TFETs is always considerably larger than SS_{MIN} [19,20]. However, SS_{AVG} dramatically increases as V_{gs} increases, resulting in SS_{AVG} and SS_{MIN} differing considerably and SS_{AVG} becoming unsteady. This is a disadvantage of conventional Si TFETs. Owing to the large bandgap and carrier mass of the silicon material, conventional Si TFETs have another disadvantage: A low ON-state current (I_{ON}) [21–23]. To overcome these disadvantages, significant research has been conducted and several device structures have been proposed. It has been shown that the use of a narrow-bandgap material such as germanium(Ge) as the source base to implement a heterojunction structure could lead to a considerably higher I_{ON} [24–29]. In particular, owing to its small screening length and high gate controllability, TFETs with a gate-all-around (GAA) structure have been extensively studied for achieving a high I_{ON} [2,18,19]. Conventional Si TFETs exhibit a steep SS_{MIN} and a low I_{ON} [30]. While heterojunction TFETs exhibit a high I_{ON}, their SS_{MIN} and SS_{AVG} need to be improved [28]. Thus, further research on TFET devices is required to achieve a steady SS_{AVG} and a higher I_{ON}.

In this paper, we propose a novel germanium-around-source gate-all-around TFET (GAS GAA TFET). In this device, the source is surrounded by germanium and a germanium-silicon heterojunction is formed at source. The GAS GAA TFET is expected to have a high I_{ON} and a steady SS_{AVG} and suppress the SS degradation behaviour. The characteristics of the device were investigated in detail to evaluate its capability for low-power applications.

2. Device Structures and Simulation Methods

Figure 1a shows a schematic of the proposed GAS GAA TFET with a channel radius (r) of 12 nm, and Figure 1c depicts a cross-sectional view of the device. T_{Ge} is the thickness of the germanium layer, which surrounds silicon in the source. The channel and drain of the device were made of silicon. The gate dielectric material was hafnium oxide (HfO_2) and the thickness (T_{ox}) of the oxide layer was 2 nm. The doping concentrations of the source, channel, drain, and around-source germanium were 5×10^{19} cm^{-3} (p-type), 1×10^{15} cm^{-3} (p-type), 1×10^{17} cm^{-3} (n-type), and 5×10^{19} cm^{-3} (p-type), respectively. The channel length, source length, and drain length were 30, 40, and 40 nm, respectively. All design parameters are presented in Table 1. Figure 1b shows a schematic of the control groups silicon gate-all-around TFET (Si GAA TFET) and germanium-based-source gate-all-around TFET (Ge-source GAA TFET), and Figure 1d presents a cross-sectional view of the control groups. The distinction between the Si GAA TFET and the Ge-source GAA TFET lies in the material of the source. The source material of the former is silicon, while that of the latter is germanium. The Si GAA TFET and Ge-source GAA TFET are identical to the GAS GAA TFET, except for the source.

All simulation results in this study were obtained using the nonlocal BTBT model, Shockley–Read–Hall recombination model, bandgap narrowing model, and doping dependence mobility model in Synopsys Sentaurus TCAD. The parameters used to calibrate the nonlocal BTBT model were $A = 4 \times 10^{14}$ cm^{-3}s^{-1}, and $B = 19 \times 10^{6}$ V/cm for silicon and $A = 1.46 \times 10^{17}$ cm^{-3}s^{-1}, and $B = 3.59 \times 10^{6}$ V/cm for germanium [1].

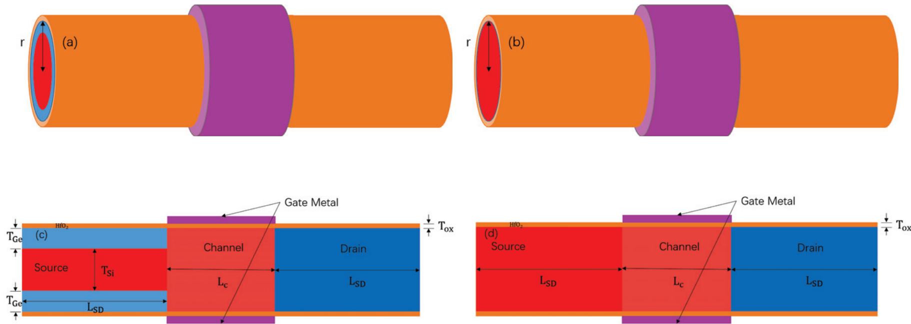

Figure 1. Schematics of the (**a**) germanium-around-source (GAS) gate-all-around (GAA) tunnelling field-effect transistor (TFET) and (**b**) Si GAA TFET and Ge-source GAA TFET. Cross-sectional views of the (**c**) GAS GAA TFET and (**d**) Si GAA TFET and Ge-source GAA TFET.

Table 1. Parameters used for the Synopsys Sentaurus technology computer-aided design (TCAD) simulation.

Parameters	Definations	Value
r	Device radius	12 nm
L_{SD}	Lateral length of source and drain	40 nm
L_C	Lateral length of channel	30 nm
T_{ox}	Gate oxide thickness	2 nm
T_{Ge}	Thickness of around-source germanium	Variable
T_{Si}	Thickness of silicon surrounded by germanium	Variable
N_S	P-type source doping concentration	5×10^{19} cm^{-3}
N_C	P-type channel doping concentration	1×10^{15} cm^{-3}
N_{SGe}	P-type around-source germanium doping concentration	5×10^{19} cm^{-3}
N_D	N-type drain doping concentration	1×10^{17} cm^{-3}

3. Simulation Results and Discussion

3.1. Thickness of Germanium (T_{Ge})

Figure 2a shows the $I_D - V_{gs}$ transfer characteristics of the proposed GAS GAA TFET for different T_{Ge} values. The T_{Ge} values considered were 2, 4, 6, 8, and 10 nm, and the gate material's work function was 4.53 eV. The transfer characteristics show that I_{ON} increases with T_{Ge} since the effective tunnelling barrier width decreases with an increase in T_{Ge} [31]. For low-voltage operation, germanium (bandgap = 0.66 eV) showed a higher BTBT rate than silicon (bandgap = 1.12 eV). The internal mechanism responsible for the GAS GAA TFET performance improving with an increase in T_{Ge} from 2 to 10 nm can be inferred from the energy band diagrams shown in Figure 2c. The energy band diagrams are for a lateral-section of the source corresponding to the cut line A-A' in Figure 2b. In Figure 2c, the bandgaps of germanium and silicon are shown; germanium has a narrower bandgap than silicon. As T_{Ge} changed from 2 to 10 nm, the area of the narrow bandgap material increased in the source. The BTBT probability (T_{WKB}) is given by the Wentzel–Kramers–Brillouin (WKB) approximation ($T_{WKB} \simeq exp(\frac{-4\lambda\sqrt{2m^*}\sqrt[3]{E_g}}{3q\hbar+\Delta\phi})$, and I_{ON} is correlated with T_{WKB} [2]. Hence, an increase in T_{Ge} from 2 to 10 nm leads to germanium becoming the main semiconductor material. In the formula for T_{WKB}, E_g is

the bandgap of the main semiconductor material in the device, and germanium becoming the main semiconductor material reduces E_g, which improves I_{ON}.

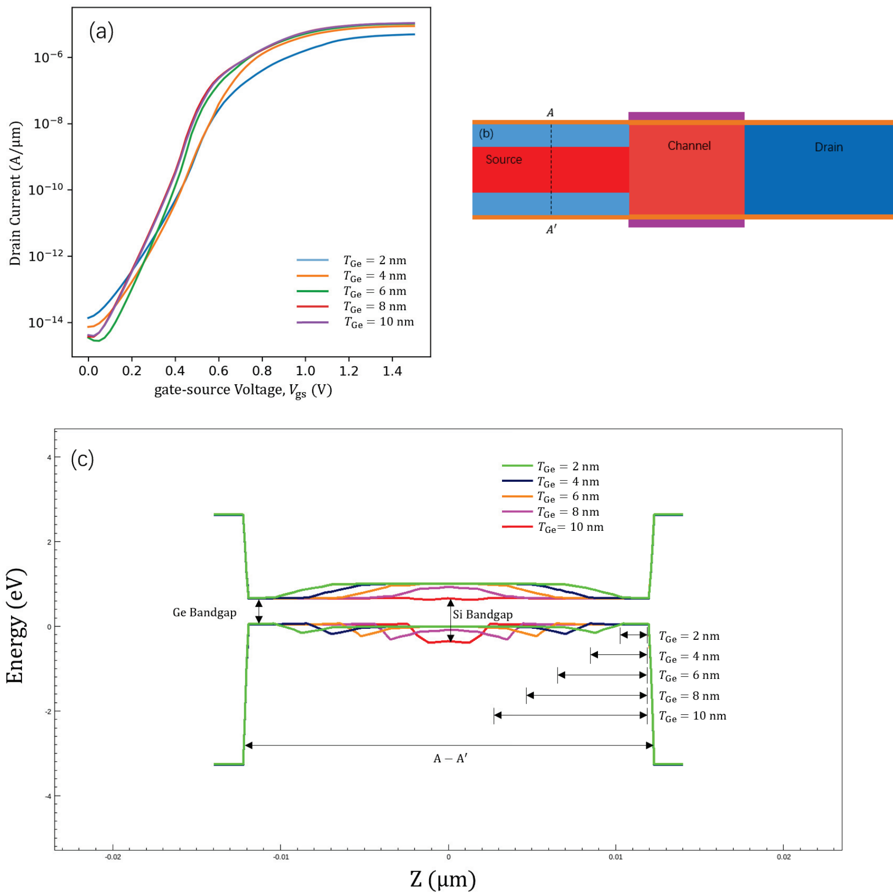

Figure 2. (**a**) $I_D - V_{gs}$ transfer characteristics for different T_{Ge} values from 2 to 10 nm. (**b**) Cross-sectional view of the GAS GAA TFET; AA' represents a cut line. (**c**) Energy band diagram for the GAS GAA TFET along the cut-line AA' shown in (**b**).

3.2. Effect of Germanium-Around-Source (GAS)

Figure 3a shows a comparison of the transfer characteristics of the proposed GAS GAA TFET for T_{Ge} = 6 nm with the Si GAA TFET and Ge-source GAA TFET. For a fair comparison, the gate material work function for the Si GAA TFET was tuned to 4.1 eV to obtain approximately the same onset voltage (V_{ONSET}) as the GAS GAA TFET and Ge-source GAA TFET; the onset voltage is the voltage after which the drain current increases exponentially with the gate voltage as shown in Figure 3 [1]. The gate material work function for the GAS GAA TFET and Ge-source GAA TFET was 4.53 eV. The GAS GAA TFET exhibited a steady and steeper SS_{AVG} than the Si GAA TFET and Ge-source GAA TFET, and a higher ON-state current than the Si GAA TFET. Here, the threshold voltage (V_T) was defined as the voltage where the current increased by a factor of 10^7. I_T and V_T of the GAS GAA TFET, Si GAA TFET, and Ge-source GAA TFET were 10^{-7} A and 0.579 V, 10^{-11} A and 0.537 V, and 10^{-6} A and 0.663 V, accordingly. Moreover, SS_{AVG} for these devices was 65, 68.71, and 83.71 mV/decade,

separately. Figure 3b shows a comparison of the SS as a function of the gate-source voltage (V_{gs}) among the GAS GAA TFET, Si GAA TFET, and Ge-source GAA TFET. Evidently, the SS of the GAS GAA TFET is steadier than that of the Si GAA TFET in a wide voltage range, and it is lower than those of the Si GAA TFET and Ge-source GAA TFET for most of the V_{gs} range considered. Since the trends of the GAS GAA TFET and the Ge-source GAA TFET curves are similar, we calculated their variances. In the range of V_{gs} = 0.15 V to 0.5 V, the variance of the GAS GAA TFET is 81.92 (mV/decade)^2 and the variance of the Ge-source GAA TFET is 108.01 (mV/decade)^2. Moreover, it proves that GAS GAA TFET is steadier than Ge-source GAA TFET in a wide voltage. As shown in the BTBT generation contour plot in Figure 4, the BTBT electron generation rate varies with V_{gs}. Since the germanium-around-source structure involves a combination of silicon and germanium, at V_{gs} = 0.1 V and V_{DS} = 1 V, BTBT generation for the GAS GAA TFET in Figure 4b is greater than that for the Si GAA TFET in Figure 4a and less than that for the Ge-source GAA TFET in Figure 4c. With an increase in V_{gs} to 0.5 V, BTBT generation for silicon is near saturation and the around-source germanium is dominant resulting in the highest level of BTBT generation being $7.461e + 29$ cm^{-3}s^{-1} in Figure 4e. For the effectiveness of line tunnelling, a certain number of electrons are required (to form a virtual p-n junction) in the direction of the gate electric field. As shown in Figure 5a,c, a large volume of the channel region gets inverted, reducing the effective p-region at the virtual p-n junction at the gate interface. Therefore, line tunnelling occurs at the source, where the inversion region is not formed, as shown in Figure 4d,f [17]. Because the germanium-around-source structure changes the electric field, the around-source germanium region is also inverted in Figure 5b. This triggers line tunnelling in the silicon area at the boundary with the germanium layer and causes additional line BTBT tunnelling in the silicon area. Those phenomena of around-source germanium becoming dominant and the occurrence of line tunnelling give rise to enhanced tunnelling when BTBT generation for silicon reaches saturation, apart from suppressing the SS degradation behaviour and making SS_{AVG} of the GAS GAA TFET steadier compared with the Si GAA TFET and Ge-source GAA TFET. They also improve I_{ON} compared with the Si GAA TFET.

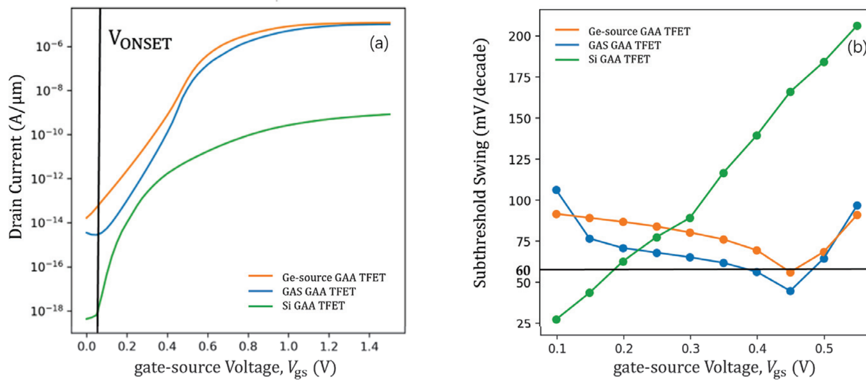

Figure 3. (**a**) $I_D - V_{gs}$ transfer characteristics and (**b**) $SS - V_{gs}$ curves for GAS GAA TFET, Ge-source GAA TFET, and Si GAA TFET.

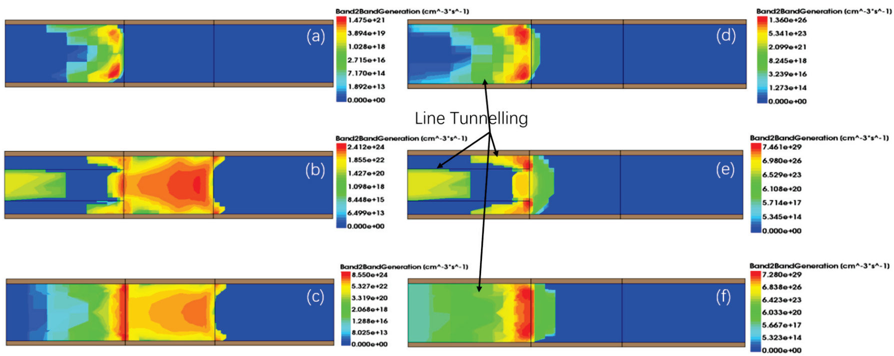

Figure 4. Two-dimensional band-to-band tunnelling (BTBT) generation contour plots for the (**a**,**d**) Si GAA TFET, (**b**,**e**) GAS GAA TFET, and (**c**,**f**) Ge-source GAA TFET. Panels (**a**–**c**) are for V_{DS}= 1 V and V_{gs} = 0.1 V and panels (**d**–**f**) are for V_{DS} = 1 V and V_{gs} = 0.5 V.

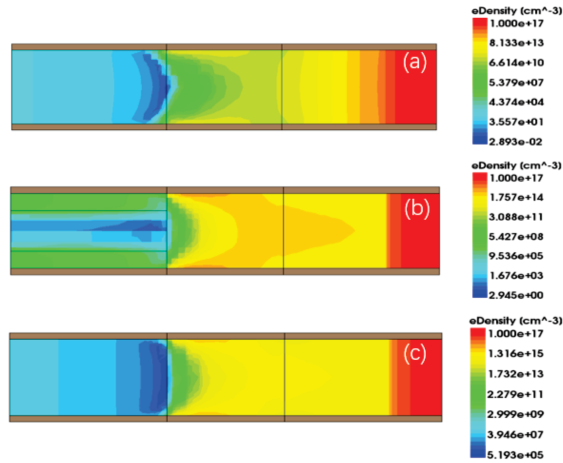

Figure 5. Two-dimensional electron density contours for the (**a**) Si GAA TFET, (**b**) GAS GAA TFET, and (**c**) Ge-source GAA TFET at V_{DS} = 1 V and V_{gs} = 0.5 V in thermal equilibrium.

3.3. Optimised GAS GAA TFET

With a decrease in the tunnelling length between the channel and the drain, the number of electrons that can tunnel from the valence band of the channel into the conduction band of the drain increases. This section discusses the use of work function [32] and drain overlapping engineering [33,34] for suppression of the ambipolar conduction effect on the GAS GAA TFET performance (Figure 2). Figure 6a shows the $I_D - V_{gs}$ transfer characteristics of the GAS GAA TFET and optimised GAS GAA TFET. A schematic of the GAS GAA TFET with drain overlapping is shown in Figure 6b. Except for the gate material work function, which was tuned to 4.4 eV, and the 5 nm overlapping drain, there was no difference between the optimised GAS GAA TFET and the GAS GAA TFET at T_{Ge} = 6 nm. The optimised structure had a lower electric field at the channel and drain interface, as shown in Figure 6c. The lower electric field reduced the tunnelling probability at the channel and drain interface. The decrease in the tunnelling probability in turn reduced the ambipolar behaviour. In the transfer characteristics of the optimised GAS GAA TFET and GAS GAA

TFET in Figure 6a, it is evident that the ambipolar behaviour of the former is alleviated. This results in the transfer characteristics of the optimised GAS GAA TFET being almost linear from V_{gs} = 0 V. The optimised GAS GAA TFET shows superior performance such as a steeper SS_{AVG} and a lower I_{OFF}, apart from reduced ambipolar behaviour. A comparison of the optimised GAS GAA TFET with the GAS GAA TFET, Si GAA TFET, and Ge-source GAA TFET in terms of SS_{MIN}, SS_{AVG}, I_{ON}, and I_{OFF} is presented in Table 2.

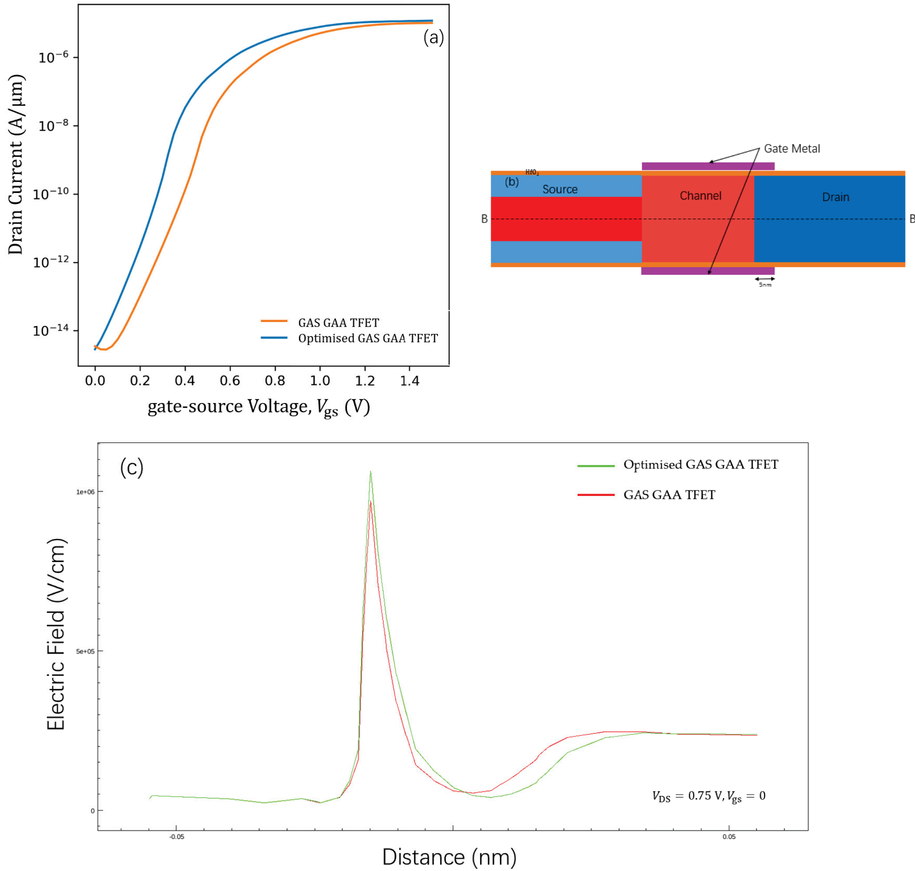

Figure 6. (**a**) $I_D - V_{gs}$ transfer characteristics for the optimised and GAS GAA TFETs. (**b**) A cross-sectional view of the optimised GAS GAA TFET with a 5 nm drain overlapping; BB′ represents a cut line. (**c**) The electric field along the cut-line BB′ shown in (**b**).

Table 2. A comparison of optimised GAS GAA TFET with GAS GAA TFET, Si GAA TFET, and Ge-source GAA TFET.

	Si GAA TFET	Ge-Source GAA TFET	GAS GAA TFET	Optimised GAS GAA TFET
SS_{MIN} (mV/dec.)	26.835	58.645	45.720	39.501
SS_{AVG} (mV/dec.)	68.71	83.71	65	57.29
I_{ON} (μA/um)	9.38×10^{-4}	11.7	10.2	11.9
I_{OFF} (μA/um)	5.05×10^{-13}	1.722×10^{-8}	3.49×10^{-9}	2.85×10^{-9}

3.4. Process Flow

Figure 7 summarizes the suggested fabrication processes for the GAS GAA TFET. The processes start with the formation of a cylindrical-shaped outer silicon layer via etching using electron beam lithography (EBL) followed by sacrificial sidewall deposition in Figure 7a–d [1]. The radius of dielectric, after deposition and patterning, determines the thickness of silicon and germaniums ($r = \frac{1}{2}T_{Si} + T_{Ge}$) in Figure 7b. Figure 7e shows the deposition of gate oxide. Figures 7f,g depict depositing a gate electrode on gate oxide layers and both gate electrode and gate oxide layer are partially removed, and then above gate oxide layer is deposited to form a spacer [35]. Afterwards, a sacrificial layer surrounding the above gate oxide layer is deposited followed by planarization in Figure 7h. Figure 7i illustrates the selective removal of the above gate oxide layer and the sacrificial layer followed by molecular beam epitaxy (MBE) to grow an in-situ boron-doped Ge layer as the around-source germanium [36]. Figure 7j depicts a TEOS layer deployed and planarized. Figure 7k shows all the layers exposing to the mesa [35]. Moreover, the in-suit boron-doped silicon is deposited as the germanium-around-source in Figure 7l. Finally, contacts and metal are formed for accessing the source, drain and gate in Figure 7m.

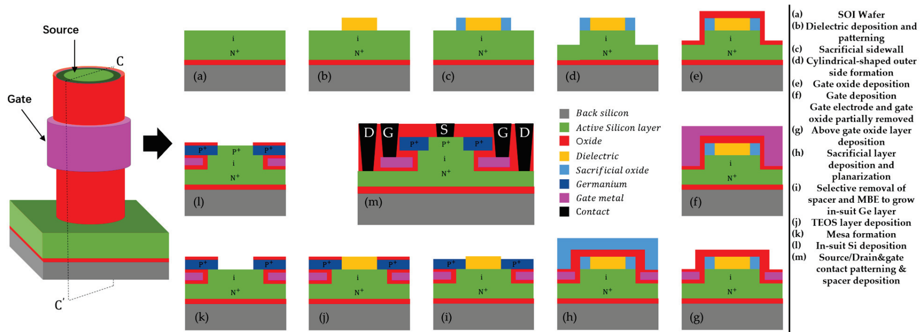

Figure 7. Fabrication process flow of a GAS GAA TFET along the cross section CC′.

4. Conclusions

In this paper, we propose a novel GAS GAA TFET, with a steady and steeper SS_{AVG} and a higher I_{ON} than conventional TFETs such as the Si GAA TFET and Ge-source GAA TFET. The use of a germanium-around-source configuration and a combination of two materials with different bandgaps in the source suppressed the SS degradation, made SS_{AVG} steady and steeper compared with the Ge-source GAA TFET, and resulted in I_{ON} being higher than that of the Si GAA TFET. The effect of an increase in the thickness of the germanium layer on I_{ON} was investigated. Furthermore, the ambipolar behaviour of the GAS GAA TFET could be alleviated through work function and drain overlapping engineering. The optimised GAS GAA TFET showed a steady and steep SS_{AVG} of 57.29 mV/decade, a significantly high I_{ON} of 11.9 μA and a low I_{OFF} of 2.85×10^{-9} μA, and absence of ambipolar behaviour. These features indicate the high potential of the device for use in low-power applications.

Author Contributions: K.H. and S.L. participated in the design of this study, and they both performed the statistical analysis, data acquisition, data analusis and manuscript preparation. K.H. carried out data analysis and manuscript preparation. S.L. collected important background information and drafted the manuscript. Z.D. provide assistance for data acquisition and manuscript review. Y.Z. and J.L. performed literature search and chart drawing. All authors have read and approved the content of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript besides parameters in Table 1:

BTBT	band-to-band tunnelling
T_{WKB}	band-to-band tunnelling probability
E_{g}	the bandgap of main semiconductor material in device
GAS GAA TFET	germanium-around-source gate-all-around tunnel field-effect transistor
Si GAA TFET	silicon gate-all-around tunnel field-effect transistor
Ge-source GAA TFET	germanium-based-source gate-all-around tunnel field-effect transistor
SS	subthreshold swing
SS_{MIN}	minimum point subthreshold swing
SS_{AVG}	average subthreshold swing
I_{ON}	ON-state current
I_{OFF}	OFF-state current
I_{D}	drain current
I_{T}	current at V_T
V_{ON}	the voltage where OFF-state current increased by a factor of 10^7 times
$\mathrm{V}_{\mathrm{ONSET}}$	the voltage after which the drain current increases exponentially with the gate voltage
V_{DS}	drain-source voltage
V_{gs}	gate-source voltage
V_{T}	threshold voltage
EBL	electron beam lithography
MBE	molecular beam epitaxy
TEOS	Tetraethylortho Silicate

References

1. Musalgaonkar, G.; Sahay, S.; Saxena, R.S.; Kumar, M.J. Nanotube tunnelling FET with a Core Source for Ultrasteep Subthreshold Swing: A Simulation Study. *IEEE Trans. Electron Devices* **2019**, *66*, 4425–4432. [CrossRef]
2. Beohar, A.; Vishvakarma, S.K. Performance enhancement of asymmetrical underlap 3D-cylindrical GAA-TFET with low spacer width. *Micro Nano Lett.* **2016**, *11*, 443–445. [CrossRef]
3. Wu, C.; Huang, Q.; Zhao, Y.; Wang, J.; Wang, Y.; Huang, R. A Novel Tunnel FET Design With Stacked Source Configuration for Average Subthreshold Swing Reduction. *IEEE Trans. Electron Devices* **2016**, *63*, 5072–5076. [CrossRef]
4. Lin, H.H.; Hu, V.P. Device design of vertical nanowire III-V heterojunction TFETs for performance enhancement. In Proceedings of the 2018 7th International Symposium on Next Generation Electronics (ISNE), Taipei, Taiwan, 7–9 May 2018; pp. 1–4.
5. Seo, J.H.; Yoon, Y.J.; Lee, H.G.; Kang, I.M. Design optimization InGaAs/GaAsSb-based heterojunction Gate-all-around (GAA) arch-shaped tunnelling field-effect transistor (A-TFET). In Proceedings of the 2018 International Conference on Electronics, Information, and Communication (ICEIC), Honolulu, HI, USA, 24–27 January 2018; pp. 1–2.
6. Gopalakrishnan, K.; Griffin, P.B.; Plummer, J.D. Impact ionization MOS (I-MOS)—Part I: Device and circuit simulations. *IEEE Trans. Electron Devices* **2005**, *52*, 69–76. [CrossRef]
7. Musalgaonkar, G.; Sahay, S.; Saxena, R.S.; Kumar, M.J. An impact ionization MOSFET with reduced breakdown voltage based on backgate misalignment. *IEEE Trans. Electron Devices* **2018**, *66*, 868–875. [CrossRef]
8. Onal, C.; Woo, R.; Koh, H.Y.; Griffin, P.B.; Plummer, J.D. A novel depletion-IMOS (DIMOS) device with improved reliability and reduced operating voltage. *IEEE Electron Device Lett.* **2009**, *30*, 64–67. [CrossRef]

9. Kumar, M.J.; Maheedhar, M.; Varma, P.P. Bipolar I-MOS—An impact-ionization MOS with reduced operating voltage using the openbase BJT configuration. *IEEE Trans. Electron Devices* **2015**, *62*, 4345–4348. [CrossRef]
10. Mamidala, J.K.; Vishnoi, R.; Pandey, P. *Tunnel Field-Effect Transistors (TFET)*; John Wiley and Sons Ltd.: West Sussex, UK, 2016.
11. Saurabh, S.; Kumar, M.J. *Fundamentals of Tunnel Field-Effect Transistors*; CRC Press: Boca Raton, FL, USA, 2016.
12. Abdi, D.B.; Kumar, M.J. In-built N+ pocket p-n-p-n tunnel field-effect transistor. *IEEE Electron Device Lett.* **2014**, *35*, 1170–1172. [CrossRef]
13. Lin J.T.; Wang T.C.; Lee W.H.; Yeh C.T.; Glass S.; Zhao, Q.T. Characteristics of recessed-gate TFETs with line tunnelling. *IEEE Trans. Electron Devices* **2018**, *65*, 769–775. [CrossRef]
14. Nagavarapu, V.; Jhaveri, R.; Woo, J.C. The tunnel source (PNPN) n-MOSFET: A novel high performance transistor. *IEEE Trans. Electron Devices* **2008**, *55*, 1013–1019. [CrossRef]
15. Zhu, J.; Zhao, Y.; Huang, Q.; Chen, C.; Wu, C.; Jia, R.; Huang, R. Design and simulation of a novel graded-channel heterojunction tunnel FET with high ION/IOFF ratio and steep swing. *IEEE Electron Device Lett.* **2017**, *38*, 1200–1203. [CrossRef]
16. Beohar, A.; Yadav, N.; Vishvakarma, S.K. Analysis of trap-assisted tunnelling in asymmetrical underlap 3D-cylindrical GAA-TFET based on hetero-spacer engineering for improved device reliability. *Micro Nano Lett.* **2017**, *12*, 982–986. [CrossRef]
17. Musalgaonkar, G.; Sahay, S.; Saxena, R.S.; Kumar, M.J. A Line tunnelling Field-Effect Transistor Based on Misaligned Core–Shell Gate Architecture in Emerging Nanotube FETs. *IEEE Trans. Electron Devices* **2019**, *66*, 2809–2816. [CrossRef]
18. Shirazi, S.G.; Karimi, G.R.; Mirzakuchaki, S. GAA CNT TFETs Structural Engineering: A Higher ON Current, Lower Ambipolarity. *IEEE Trans. Electron Devices* **2019**, *66*, 2822–2830. [CrossRef]
19. Lu, H.; Seabaugh, A. Tunnel field-effect transistors: State-ofthe-art. *IEEE J. Electron Devices Soc.* **2014**, *2*, 44–49. [CrossRef]
20. Huang, Q.; Huang, R.; Wu, C.; Zhu, H.; Chen, C.; Wang, J.; Guo, L.; Wang, R.; Ye, L.; Wang, Y. Comprehensive performance re-assessment of TFETs with a novel design by gate and source engineering from device/circuit perspective. In Proceedings of the 2014 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2014 ; pp. 13–33.
21. Appenzeller, J.; Lin, Y.M.; Knoch, J.; Chen, Z.; Avouris, P. Comparing carbon nanotube transistors-the ideal choice: A novel tunnelling device design. *IEEE Trans. Electron Devices* **2005**, *52*, 2568–2576. [CrossRef]
22. Toh, E.H.; Wang, G.H.; Samudra, G.; Yeo, Y.C. Device physics and design of double-gate tunnelling field-effect transistor by silicon film thickness optimization. *Appl. Phys. Lett.* **2007**, *90*, 63507. [CrossRef]
23. Avci, U.E.; Morris, D.H.; Young, I.A. Tunnel field-effect transistors: Prospects and challenges. *IEEE J. Electron Devices Soc.* **2015**, *3*, 88–95. [CrossRef]
24. Vanlalawpuia, K.; Bhowmick, B. Investigation of a Ge-Source Vertical TFET with Delta-Doped Layer. *IEEE Trans. Electron Devices* **2019**, *66*, 4439–4445. [CrossRef]
25. Kim, S.H.; Jacobson, Z.A.; Liu, T.J. Impact of body doping and thickness on the performance of Germanium-source TFETs. *IEEE Trans. Electron Devices* **2010**, *57* , 1710–1713. [CrossRef]
26. Damrongplasit, N.; Shin, C.; Kim, S.H.; Vega, R.A.; Liu, T.-J.K. Study of Random Dopant Fluctuation Effects in Germanium-Source Tunnel FETs. *IEEE Trans. Electron Devices* **2011**, *58*, 3541–3548. [CrossRef]
27. Lee, Y.; Nam, H.; Park, J.-D.; Shin, C. Study of work-function variation for high-K/metal-gate ge-source tunnel field-effect transistors. *IEEE Trans. Electron Devices* **2015**, *62*, 2143–2147. [CrossRef]
28. Beohar, A.; Shah, A.P.; Yadav, N.; Vishvakarma, S.K. Design of 3D cylindrical GAA-TFET based on germanium source with drain underlap for low power applications. In Proceedings of the 2017 International Conference on Electron Devices and Solid-State Circuits (EDSSC), Hsinchu, Taiwan, 18–20 October 2017; pp. 1–2.
29. Jhan, Y.-R.; Wu, Y.-C.; Hung, M.-F. Performance enhancement of nanowire tunnel field-effect transistor with asymmetry-gate based on different screening length. *IEEE Electron Device Lett.* **2013**, *34*, 1482–1484. [CrossRef]
30. Kumar, M.J.; Janardhanan, S. Doping-less tunnel field effecttransistor: Design and investigation. *IEEE Trans. Electron Devices* **2013**, *60*, 3285–3290. [CrossRef]
31. Jang, W.D.; Yoon, Y.J.; Cho, M.S.; Jung, J.H.; Lee, S.H.; Jang, J.; Bae, J.-H.; Kang, I.M. Design and Optimization of Germanium-Based Gate-Metal-Core Vertical Nanowire Tunnel FET. *Micromachines* **2019**, *10*, 749. [CrossRef]

32. Raad, B.; Kondekar, P.; Sharma, D.; Nigam, K. Dielectric and work function engineered TFET for ambipolar suppression and RF performance enhancement. *Electron. Lett.* **2016**, *52*, 770–772. [CrossRef]
33. Singh, P.; Chauhan, V.K.; Ray, D.D.; Dash, S.; Mishra, G.P. Ambipolar Performance Improvement of Dual Material TFET Using Drain Underlap Engineering. In Proceedings of the 2018 IEEE Electron Devices Kolkata Conference (EDKCON), Kolkata, India, 24–25 November 2018; pp. 274–277.
34. Lee, J.S.; Seo, J.H.; Cho, S.; Lee, J.-H.; Kang, S.-W.; Bae, J.-H.; Cho, E.-S.; Kang, I.M. Simulation study on effect of drain underlap in gate-all-around tunnelling field-effect transistors. *Curr. Appl. Phys.* **2013**, *13*, 1143–1149. [CrossRef]
35. Tekleab, D.; Tran, H.H.; Sleight, J.W.; Chidambarrao, D. Silicon Nanotube MOSFET. U.S. Patent 8,871,576, 28 October 2014.
36. Bae, T.-E.; Suzuki, R.; Nakane, R.; Takenaka, M.; Takagi, S. Effects of ge-source impurity concentration on electrical characteristics of Ge/Si hetero-junction tunnelling FETs. In Proceedings of the 2017 Fifth Berkeley Symposium on Energy Efficient Electronic Systems and Steep Transistors Workshop (E3S), Berkeley, CA, USA, 19–20 October 2017; pp. 1–3.

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T-Channel Field Effect Transistor with Three Input Terminals (Ti-TcFET)

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Abstract: In this paper, a novel T-channel field effect transistor with three input terminals (Ti-TcFET) is proposed. The channel of a Ti-TcFET consists of horizontal and vertical sections. The top gate is above the horizontal channel, while the front gate and back gate are on either side of the vertical channel. The T-shaped channel structure increases the coupling area between the top gate and the front and back gates, which improves the ability of the gate electrodes to control the channel. What's more, it makes the top gate have almost the same control ability for the channel as the front gate and the back gate. This unique structure design brings a unique function in that the device is turned on only when two or three inputs are activated. Silvaco technology computer-aided design (TCAD) simulations are used to verify the current characteristics of the proposed Ti-TcFET. The current characteristics of the device are theoretically analyzed, and the results show that the theoretical analysis agrees with the TCAD simulation results. The proposed Ti-TcFET devices with three input terminals can be used to simplify the complex circuits in a compact style with reduced counts of transistors compared with the traditional complementary metal–oxide–semiconductor/ fin field-effect transistors (CMOS/FinFETs) with a single input terminal and thus provides a new idea for future circuit designs.

Keywords: new device; three-input transistor; T-channel; compact circuit style

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1. Introduction

Because of short-channel effects, the size of metal-oxide-semiconductor (MOS) devices is seriously restricted. In order to continue Moore's law, many new device structures have been proposed, such as silicon-on-insulator metal-oxide-semiconductor field-effect-transistors (SOI MOSFETs) with a single-gate structure, fin field-effect transistor (FinFETs) with a double-gate structure [1], and tri-gate field effect transistors (FETs) [2], Ω-gate FETs [3], and Gate-All-Around (GAA)FETs with a multi-gate structure. Among these devices, FinFET has been widely used in chip fabrication since it can considerably improve the ability of the gate electrode to control the channel and thus suppress the short-channel effects.

Most of the multi-gate devices mentioned above have only one input terminal. However, previous studies have shown that designing a circuit with devices with multiple input terminals is more flexible and efficient than using single-input ones [4,5]. The two-input low-threshold FinFET device proposed in the literature [6–10] is equivalent to two parallel transistors, while the two-input high-threshold FinFET device is equivalent to two series transistors. Therefore, the circuit can be simplified to reduce the transistor count by using two-input low-threshold and high-threshold FinFETs, thus reducing power consumption and the chip area. If a device has more input terminals, it is possible to achieve more flexible and efficient circuit designs.

This paper proposes a novel T-channel field effect transistor with three input terminals (Ti-TcFET). The invented T-type channel structure allows the device to have three independent input gates: the top

gate, front gate, and back gate. Because of the device structure with a T-type channel, the coupling areas among the top gate and the front and back gates are increased, which increases the control capability of the gates to the channel. This unique structure design brings a unique function in that the device is turned on only when two or three inputs are activated. Compared with traditional FinFETs with a single input terminal, the proposed Ti-TcFET devices with three input terminals can provide more flexible circuit realizations in a compact style. The proposed Ti-TcFET devices can be fabricated by adding only a small number of process steps on the basis of the current mainstream FinFET process.

This paper is organized as follows. In Section 2, the structure of the proposed device is introduced, and its device parameters are presented. The key processing steps of Ti-TcFET devices are also included in Section 2. In Section 3, the current characteristics of the device are theoretically analyzed, and Silvaco technology computer-aided design (TCAD) simulations are used to verify the accuracy of theoretical analysis. In Section 3, we illustrate how to carry out performance optimization for the proposed Ti-TcFET devices, and device performances are analyzed and evaluated in terms of turn-on and turn-off currents and switching current ratio. The compact circuits based on Ti-TcFET devices are also included in Section 3. We show that Ti-TcFET devices can be used to simplify complex circuits in a compact style with reduced transistor counts compared with the traditional complementary metal–oxide–semiconductor/ fin field-effect transistors (CMOS/FinFETs) with a single input terminal. Finally, the work of this paper is summarized in the last section.

2. Device Structure and Description

This section takes an N-type Ti-TcFET as an example to present the structure and parameters of the proposed device. We also give the fabrication process of Ti-TcFET devices in this section.

2.1. The Structure of the Ti-TcFET

Figure 1a shows a 3D diagram of the N-type Ti-TcFET, while Figure 1b is a cross-sectional diagram of the N-type Ti-TcFET. As seen in Figure 1a, the device has three independent input gates, termed the top gate, front gate, and back gate. From Figure 1b, we can see that the T-type channel of the Ti-TcFET is divided into horizontal and vertical sections. H_{Fin1} and T_{Si1} are the fin height and thickness of the vertical channel, respectively, while H_{Fin2} and T_{Si2} are the fin height and thickness of the horizontal channel, respectively. By adjusting the fin height H_{Fin2} of the horizontal channel, the contact area between the top gate and the horizontal channel can be changed, thus changing the coupling strength between the top gate and the front and back gates. The gate-to-channel control capability can be varied by adjusting the gate work function and the thickness T_{ox} of the high-K dielectric hafnium(IV) oxide (HfO_2).

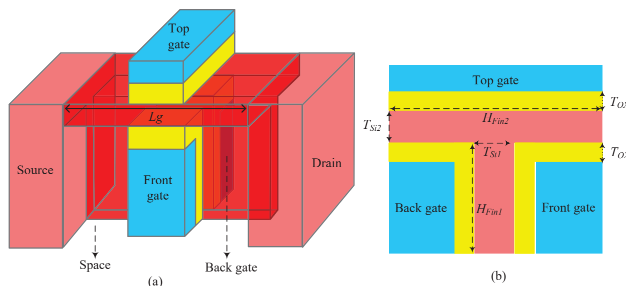

Figure 1. Structure of the N-type T-channel field effect transistor with three input terminals (Ti-TcFET) device: (**a**) 3D diagram, and (**b**) cross-sectional view.

In this work, SiO_2 is used as the substrate material for the device. The channel material is silicon, and the gate oxide material employs high-K dielectric HfO_2. The device parameters of the Ti-TcFET are

shown in Table 1. The optimum values of H_{Fin1} T_{Si1}, H_{Fin2}, T_{Si2}, T_{OX} (HfO_2 thickness), and L_g (channel length) are listed in Table 1. The doping concentrations N_{drain} and N_{source} of the source and drain regions are 2×10^{20} cm^{-3}, and the channel doping concentration N_{channel} is 1×10^{16} cm^{-3}. The gate work function Φ_m of the N-type Ti-TcFET is set to 4.95 eV, while the gate work function of the P-type Ti-TcFET is selected to be 4.55 eV.

Table 1. Parameters of the T-channel field effect transistor with three input terminals (Ti-TcFET) device.

Parameter	Optimized Value	Parameter	Optimized Value
Gate dielectric thickness (T_{ox})	3 nm	Drain doping (N_{drain})	2×10^{20} cm^{-3}
Channel thickness 1 (T_{Si1})	4 nm	Source doping (N_{source})	2×10^{20} cm^{-3}
Channel thickness 2 (T_{Si2})	4 nm	Channel doping (N_{channel})	1×10^{16} cm^{-3}
Fin height 1 (H_{Fin1})	40 nm	Gate work function (Φ_m)	4.52 eV (P-type)
Fin height 2 (H_{Fin2})	84 nm		4.95 eV (N-type)
Gate length (L_g)	24 nm	-	-

2.2. Key Processing Steps for the Ti-TcFET Device

On the basis of a traditional SOI-independent FinFET process [11], Ti-TcFET devices can be fabricated by adding a few processing steps. A key fabrication process is shown in Figure 2.

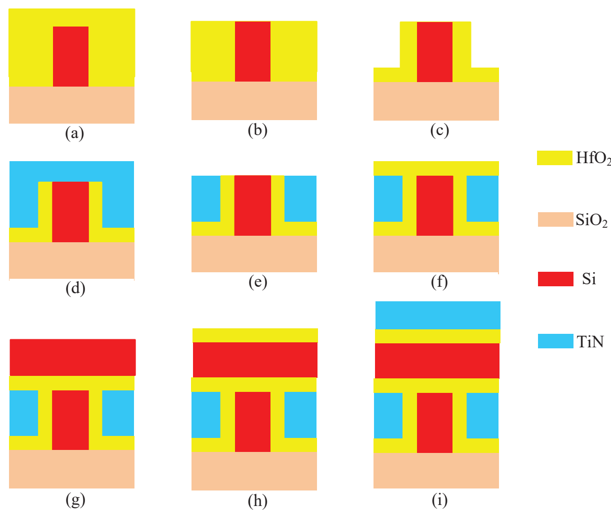

Figure 2. Key process steps of the Ti-TcFET device. (**a**) Silicon-on-insulator (SOI) layers were etched down to the buried oxide layer to produce the bodies of the devices; (**b**) chemical mechanical polishing (CMP) processing was used to remove the extra part of gate oxide above the top of the fin; (**c**) the extra part of gate oxide was etched back; (**d**) a Si_3N_4 gate electrode mask was deposited and patterned; (**e**) the gate pattern was etched into the Si_3N_4 and through the TiN to form the gate electrodes; (**f**) the high-K dielectric was deposited by using atomic layer deposition (ALD) processing; (**g**) a suitable horizontal channel structure was established by using smart-cut processing; (**h**) the high-K dielectric layer was deposited by using ALD processing; (**i**) the gate pattern was etched into the silicon and through the TiN to form the top gate electrodes.

A SiO_2 film was firstly grown as a mask for the silicon fin etching, and then the hard-mask and SOI layers were etched down to the buried oxide layer to produce the bodies of the devices, as shown in Figure 2a [11]. A high-K dielectric layer was deposited by using atomic layer deposition (ALD) processing. Next, chemical mechanical polishing (CMP) processing was used to remove the extra

part of gate oxide above the top of the fin, as shown in Figure 2b. The extra part of gate oxide was etched back, and only the required part on the two sides of the fin remained, as shown in Figure 2c [11]. Thereafter, a Si_3N_4 gate electrode mask was deposited and patterned, as shown in Figure 2d. The gate pattern was etched into the Si_3N_4 and through the TiN to form the gate electrodes, as shown in Figure 2e. The high-K dielectric was deposited by using ALD processing, as shown in Figure 2f. In order to reduce the difficulty of the process, the horizontal channel and vertical channel were separated by HfO_2, as shown in Figure 2g. Figure 2g shows how a suitable horizontal channel structure was established by using smart-cut processing. In order to establish the gate oxide layer of the top gate, the high-K dielectric layer was deposited by using ALD processing, as shown in Figure 2h. A Si_3N_4 gate electrode mask was deposited and patterned, and finally, the gate pattern was etched into the silicon and through the TiN to form the top gate electrodes, as shown in Figure 2i.

3. Results and Discussion

In this section, the current characteristics of the device are theoretically analyzed by modeling the threshold voltage of Ti-TcFETs, and then Silvaco TCAD simulations are used to verify the accuracy of the theoretical analysis. The Lombardi constant voltage and temperature (CVT), Fermi–Dirac carrier statistics (FERMIDIRAC), Shockley–Read–Hall (SRH) models, and the Bohm quantum potential (BQP) models were considered in these TCAD simulations [12]. The performance optimizations for the proposed Ti-TcFET devices were carried out by selecting the channel thickness, gate oxide thickness, and gate work function, and device performances were evaluated in terms of turn-on and turn-off currents and switching current ratio. The several basic logic cells such as the "majority-not" [13,14], NOT-AND (NAND), and NOT-OR (NOR) logic cells, and the full adder realized by using the proposed Ti-TcFET devices are illustrated, showing that Ti-TcFET devices can be used to simplify complex circuits in a compact style with reduced transistor counts.

3.1. The Threshold Voltage of Ti-TcFET Devices

The Ti-TcFET device has three inputs. The threshold voltage of any gate is affected by the bias voltage of the other two gates because of the coupling effect among the three gates. In other words, the threshold voltage of a gate is a function of the voltages of the other two gates. Taking the threshold voltage of the top gate of the N-type Ti-TcFET as an example, the relationship between the threshold voltage and other gate voltages (front gate and back gates) is analyzed.

The relationship between the threshold voltage of the top gate and the bias voltages of the front gate and back gate can be measured by introducing the coupling coefficients $\gamma_{top\text{-}gate}$ and $\gamma_{top\text{-}back}$ [15,16], as shown in Equations (1) and (2).

$$r_{top\text{-}front} = \frac{\Delta V_{THt}}{\Delta V_{front\text{-}gate}} = \frac{C_{si} \cdot C_{oxf}}{C_{oxt} \cdot \left(3C_{oxf} + 2C_{si}\right)} \cong \frac{T_{oxf}}{2T_{oxf} + 6.3T_{si}}, \quad (1)$$

$$r_{top\text{-}back} = \frac{\Delta V_{THt}}{\Delta V_{back\text{-}gate}} = \frac{C_{si} \cdot C_{oxb}}{C_{oxt} \cdot (3C_{oxb} + 2C_{si})} \cong \frac{T_{oxb}}{2T_{oxb} + 6.3T_{si}}, \quad (2)$$

where V_{THt} is the threshold voltage of the top gate, $V_{front\text{-}gate}$ and $V_{back\text{-}gate}$ are the voltages of the front gate and back gate, respectively, C_{oxf}, C_{oxb}, and C_{oxt} are the oxide capacitance of the front gate, back gate, and top gate, respectively, C_{si} and T_{si} are the body capacitance and thickness of the channel, respectively, and T_{oxf} and T_{oxb} are e thickness of the front and back gates, respectively.

TCAD simulation show that the threshold voltage V_{THt} of the top gate is not completely linear to the bias voltages of the front and back gates. After considering the secondary effect, the threshold voltage V_{THt} of the top gate can be written as Equation (3).

$$V_{THt} = V_{TH0} - r_{top\text{-front}} \cdot V_{front\text{-}gate} - r_{top\text{-}back} \cdot V_{back\text{-}gate} - \alpha \cdot \left(V^2_{front\text{-}gate} + V^2_{back\text{-}gate}\right) \\ -\beta \cdot V_{front\text{-}gate} \cdot V_{back\text{-}gate} \quad (3)$$

where V_{TH0} is the threshold voltage of the top gate when both $V_{front\text{-}gate}$ and $V_{back\text{-}gate}$ are at 0 V, and α and β are the fitting parameters.

The threshold voltage of the top gate versus the voltages of the front gate and the back gate is shown in Figure 3. In Figure 3, the points are the threshold voltages of the Ti-TcFET device obtained by the TCAD simulations, while the lines are the theoretical calculation results obtained by Equation (3) in different voltages of the front and back gates. The results show that the theoretical formula of the threshold voltage agrees with the TCAD simulation results.

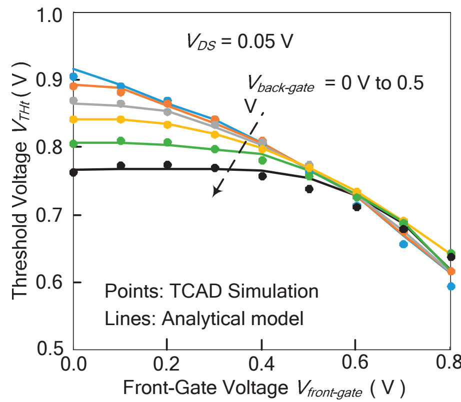

Figure 3. Comparison between calculated and simulated threshold voltages of the top gate versus the front gate in different back gate voltages at V_{DS} = 50 mV.

As the size of nanoscale devices decreases, quantum mechanical effects will begin to affect device performance. The threshold voltage drift ΔV_{TH} caused by the quantum mechanical effect can be written as follows [17]:

$$\Delta V_{TH} = \frac{S}{v_T \ln 10} \Delta \Psi, \quad (4)$$

where $v_T = kT/q$ is the thermal voltage—where k is Boltz constant, T is the thermodynamic temperature, and q is the electronic charge quantity—and S is the subthreshold swing of the device. $\Delta\Psi$ is

$$\Delta \Psi = \Psi_S^{QM} - \Psi_S^{CL}, \quad (5)$$

where Ψ_S^{QM} and Ψ_S^{CL} are the potential at the silicon–oxide interface when considering the quantum models and semi-classical models, respectively.

The Ti-TcFETs have been simulated considering both the Bohm quantum potential (BQP) models and semi-classical models. The threshold voltage of the device is reduced by 0.018 V when considering the BQP quantum compared with semi-classical models. Studies have shown that the amount of threshold voltage drift caused by quantum effects will become obvious when the channel silicon thickness is very thin (<2 nm) [18]. For undoped devices with a bulk silicon thickness (>4 nm), the threshold voltage drift caused by quantum effects is small [18].

3.2. Drain Current of the Ti-TcFET

The drain current I_D of the Ti-TcFET device can be expressed by Equation (6).

$$I_D = I_S \cdot \frac{H_{Fin2}T_{Si2}}{L_g} \cdot \left(V_{top\text{-}gate} - V_{THt}\right)^{\lambda}, \quad (6)$$

where I_S and λ are fitting parameters. For short-channel devices, the range of λ is about 1.3 to 1.5 [19].

The drain current of the Ti-TcFET device versus the voltages of the top gate is shown in Figure 4, where V_{DS} is 0.8 V, $V_{front\text{-}gate}$ is 0 V, and $V_{back\text{-}gate}$ changes from 0.2 V to 0.8 V. In Figure 4, the points are obtained by the TCAD simulations, while the lines are the theoretical calculation results of the drain current for different voltages of the top gate. The results show that the theoretical formula of the drain current agrees with the TCAD simulation results.

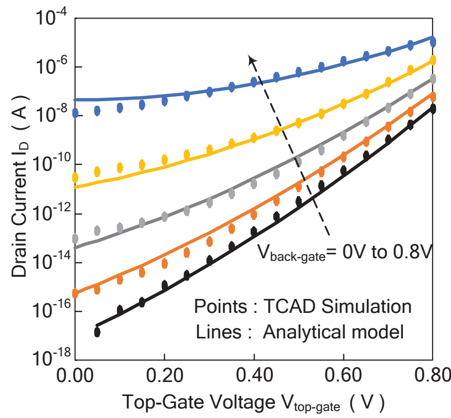

Figure 4. Comparison between the calculated and simulated drain current versus the voltages of the top gate in different back-gate voltages at V_{DS} = 0.8 V and $V_{front\text{-}gate}$ = 0 V.

3.3. Subthreshold Current of the Ti-TcFET

Referring to the literature [20,21], the subthreshold leakage current I_{sub} of the Ti-TcFET device can be calculated by Equation (7):

$$I_{sub} = I_w \cdot \frac{H_{Fin2}T_{Si2}}{L_g} \cdot e^{\frac{(V_{top\text{-}gate}-V_{THt})+m\cdot(V_{top\text{-}gate}-V_{THt})^2}{n\cdot v_T}} \cdot \left(1 - e^{\frac{-q\cdot V_{DS}}{v_T}}\right) \cdot e^{b1\cdot V_{top\text{-}gate}+b2\cdot V_{top\text{-}gate}^2+b3\cdot V_{top\text{-}gate}\cdot V_{THt}}, \quad (7)$$

where I_w, m, $b1$, $b2$, and $b3$ are fitting parameters and n is subthreshold slope parameter.

The drain current of the Ti-TcFET device versus the voltages of the top gate is shown in Figure 5, where V_{DS} is 0.8 V, $V_{front\text{-}gate}$ is 0 V, and $V_{back\text{-}gate}$ changes from 0 V to 0.5 V. In Figure 5, the points are obtained by TCAD simulations, while the lines are the theoretical calculation results of the drain current for different voltages of the top gate. The calculated subthreshold drains agree well with the simulated subthreshold current for $V_{top\text{-}gate}$ > 0.1 V.

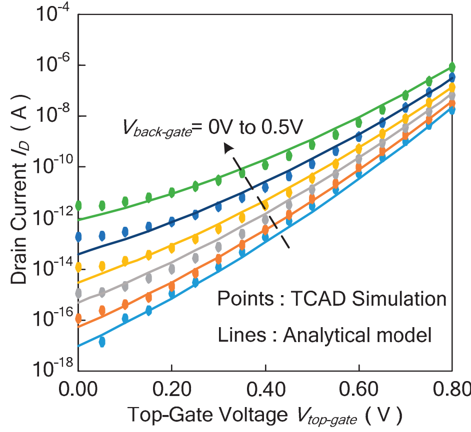

Figure 5. Comparison between the calculated and simulated subthreshold drain current versus the voltages of the top gate in different back-gate voltages at V_{DS} = 0.8 V and $V_{front\text{-}gate}$ = 0 V.

3.4. Performance Optimization of the Ti-TcFET Devices

In order to obtain high-performance Ti-TcFET devices, the following two goals should be achieved. If only one gate is activated, the current should be as small as possible. If any two of the three gates are activated, the current should be as large as possible. In other words, the maximum turn-off current I_{off} should be small and the minimum turn-on current I_{on} should be large. In this subsection, we study the influence of device size and parameters on device performance by changing the channel thickness, gate oxide thickness, and gate work function, and then select the optimized device size and parameters.

In order to achieve the first goal, Ti-TcFET devices should have a high-threshold voltage when only one gate is activated. The threshold voltage of a Ti-TcFET is approximated by Equation (8):

$$V_{Tht} = V_{inv} + \Phi_m + \frac{Q_D}{C_{ox}} + V^{QM} - V^{SCE}, \tag{8}$$

where V_{inv} is a constant, Φ_m is the work function difference of the electrode and the silicon, Q_D is the channel depletion charge, C_{ox} is the oxide capacitance of the front gate, back gate, and top gate, and V^{QM} and V^{SCE} are the threshold voltage increase caused by quantum-mechanical effect models and short-channel effects, respectively. From Equation (8), the threshold voltage of the device can be adjusted by selecting a suitable Φ_m and C_{ox}.

In order to achieve the second goal, Ti-TcFET devices should have a low subthreshold slope, so that the device achieves a large turn-on current with a small turn-off current. The subthreshold slope S is given by Equation (9) [22]:

$$S = \frac{\partial V_{top\text{-}gate}}{\partial \log I_D} = \ln 10 \cdot \frac{kT}{q} \cdot \frac{\Delta V_{top\text{-}gate}}{\Delta \psi_{Si}} = 60 \cdot \frac{\Delta V_{top\text{-}gate}}{\Delta \psi_{Si}}, \tag{9}$$

where ψ_{Si} is the surface potential at the gate electrode. The subthreshold slope can be approximated by Equation (10) [23]:

$$S = 60 \cdot \frac{T_{oxt} + 2.1T_{Si} + T_{oxb}}{T_{oxb}} = 60 \cdot \left(\frac{2.1T_{Si}}{T_{OX}} + 2\right), \tag{10}$$

From Equation (10), we can get the relationship between the subthreshold slope S, channel thickness T_{Si}, and gate oxide thickness T_{ox}, which can be used to optimize the performances of Ti-TcFET devices.

3.4.1. Effect of Channel Thickness on Current Characteristics

Figure 6 shows the effect of channel thickness T_{si} on current characteristics at $V_{front\text{-}gate}$ = 0 V and $V_{back\text{-}gate}$ = 0.8 V. When the voltage $V_{top\text{-}gate}$ of the top gate is set as 0.8 V, the two inputs of the N-type Ti-TcFET are at 0.8 V, and thus the device should be turned on. Its drain current is named as I_{on} (turn-on current). When the voltage of the top gate $V_{top\text{-}gate}$ is 0 V, only one input of the Ti-TcFET is at 0.8 V, and thus the device should be turned off. Its drain current is named as I_{off} (turn-off current).

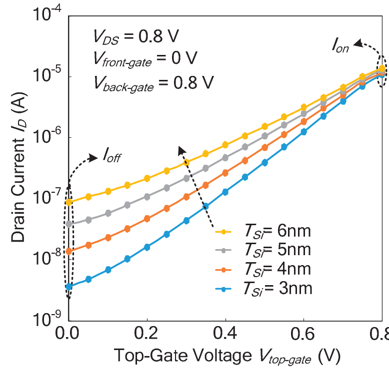

Figure 6. The turn-on current I_{on} and turn-off current I_{off} at different channel thicknesses T_{Si}.

From Figure 6, it ca be seen that as the channel thickness reduces from 6 nm down to 3 nm, I_{on}/I_{off} (the switching current ratio) increases. From Equation (10), the subthreshold slope S of the devices reduces when the channel thickness T_{Si} reduces. The results show that the TCAD simulations agree with the theoretical formula. In order to have enough I_{on} and an acceptable I_{on}/I_{off}, the optimized T_{Si} is set to 4 nm.

3.4.2. Effect of Gate Oxide Thickness on Current Characteristics

Figure 7 shows the effect of gate oxide thickness T_{OX} on current characteristics at $V_{front\text{-}gate}$ = 0 V and $V_{back\text{-}gate}$ = 0.8 V according to the TCAD simulations. As the gate oxide thickness T_{OX} increases from 2.0 nm to 3.5 nm, I_{on}/I_{off} increases. As shown in Equation (10), when the gate oxide thickness T_{OX} increases, the subthreshold slope S of the Ti-TcFET devices decreases, so that I_{on}/I_{off} increases. The results show that the theoretical formula agrees with the TCAD simulations. In order to have enough I_{on} and an acceptable I_{on}/I_{off}, the optimized gate oxide thickness T_{OX} is set to 3 nm.

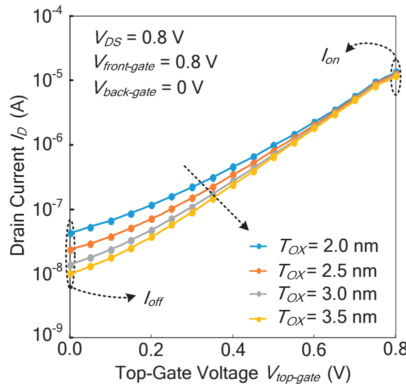

Figure 7. The turn-on current I_{on} and turn-off current I_{off} at different thickness T_{OX} of the dielectric HfO_2.

3.4.3. Effect of Gate Work Function on Current Characteristics

Figure 8 shows the effect of the gate work function on current characteristics at $V_{front\text{-}gate} = 0$ V and $V_{back\text{-}gate} = 0.8$ V according to the TCAD simulations. From Figure 8, it can be seen that as the gate work function Φ_m increases from 4.85 eV to 5.00 eV, I_{off} decreases. As shown in Equation (8), a high-threshold voltage can be achieved by increasing the gate work function Φ_m, so that I_{off} decreases. The results show that the theoretical formula agrees with the TCAD simulations. In order to reduce I_{off}, the optimized gate work function is set to 4.95 eV.

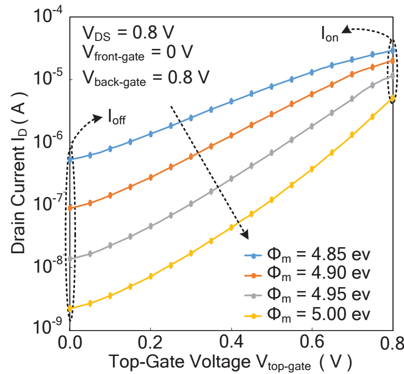

Figure 8. The turn-on current I_{on} and turn-off current I_{off} with different gate work functions Φ_m.

3.5. Drain-Induced Barrier Lowering (DIBL) and S of the Optimized Ti-TcFET Devices

The drain-induced barrier lowering (DIBL) can be calculated by using Equation (11):

$$DIBL(mV/V) = \frac{\Delta V_{Tht}}{\Delta V_{DS}}, \tag{11}$$

As shown in Equation (11), the DIBL is defined as the difference in threshold voltage when the drain voltage is increased. The drain current of the Ti-TcFET is shown in Figure 9 when $V_{front\text{-}gate} = 0$ V and $V_{back\text{-}gate} = 0.8$ V. From Figure 9, the DIBL of the Ti-TcFET device is about 41.48 mV/V when $V_{front\text{-}gate} = 0$ V and $V_{back\text{-}gate} = 0.8$ V. Our TCAD simulations show that the DIBL of the Ti-TcFET device is almost the same as the standard FinFET device when using the same device parameters.

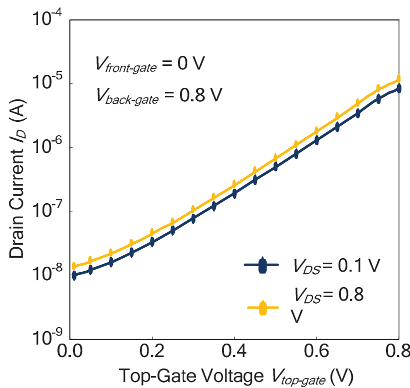

Figure 9. Drain current of the Ti-TcFET when $V_{front\text{-}gate} = 0$ V and $V_{back\text{-}gate} = 0.8$ V.

The drain current of the Ti-TcFET is shown in Figure 10 when $V_{top\text{-}gate} = V_{front\text{-}gate} = V_{back\text{-}gate}$. From Figure 10, it can be seen that the subthreshold slope *S* of the Ti-TcFET devices is about 62.6 mV/dec. The TCAD simulations show that the subthreshold slope *S* of the Ti-TcFET device is also almost the same as the standard FinFET device when using the same device parameters.

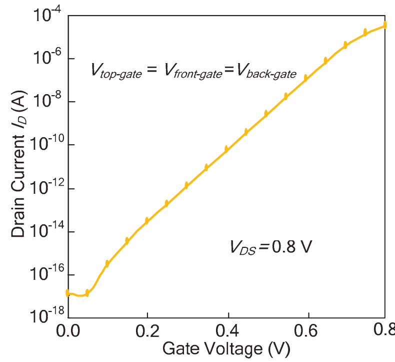

Figure 10. Drain current of the Ti-TcFET when $V_{top\text{-}gate} = V_{front\text{-}gate} = V_{back\text{-}gate}$.

3.6. Scaling Factors of the Ti-TcFET Devices

The minimum turn-on current and maximum turn-off current are shown in Figure 11 as channel length L_g and fin height H_{Fin} scale down, where the scaling factor (SF) is set as 0.707. From Figure 11a, as the channel length L_g and fin height H_{Fin} scale down, the minimum turn-on current reduces slowly. From Figure 11b, as the channel length L_g and fin height H_{Fin} scale down, the maximum turn-off drain is almost a constant.

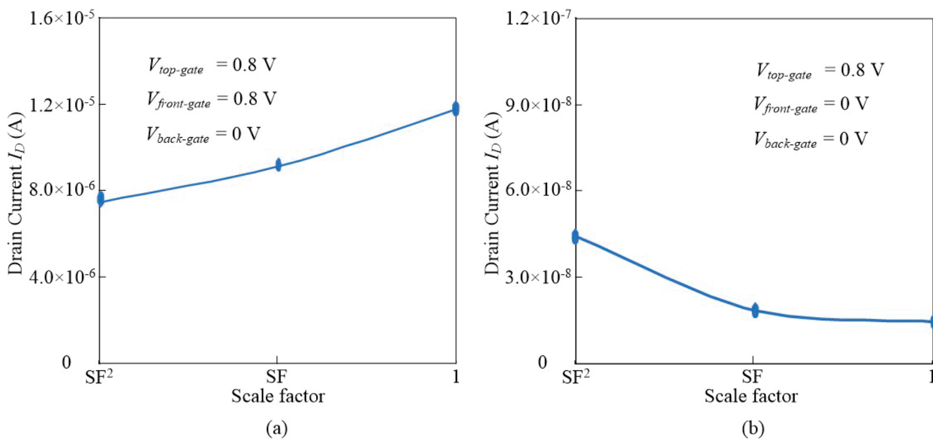

Figure 11. (**a**) The minimum turn-on current as channel length L_g and fin height H_{Fin} scale down, and (**b**) the maximum turn-off current as channel length L_g and fin height H_{Fin} scale down. The scaling factor (SF) is set as 0.707.

3.7. Performance Analysis of the Ti-TcFET Devices

The Ti-TcFET device has three input terminals, and each input terminal has two logic values with logic "1" (0.8 V) and logic "0" (0 V), so that the device has eight switching modes. Taking the N-type Ti-TcFET as an example, eight working modes are illustrated in Figure 12. When only one or fewer inputs are "1", the device is turned off, as shown in Figure 12a. In Figure 12a, there are four switching

modes in the turn-off state. When two or three inputs are "1", the device is turned on, as shown in Figure 12b. In Figure 12b, there are also four switching modes in the turn-on state.

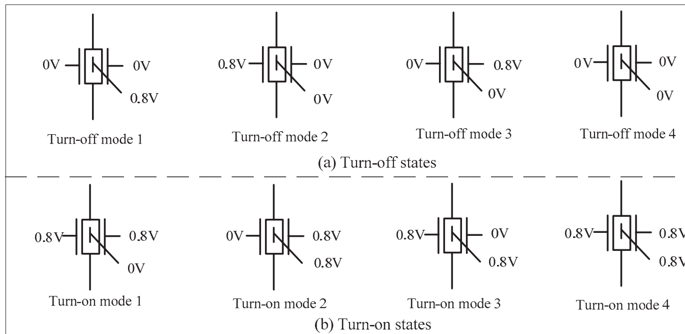

Figure 12. Eight switching modes of the Ti-TcFET device.

Using the optimized parameters and device sizes listed in Table 1, the turn-on and turn-off currents of N-type and P-type Ti-TcFETs working in eight switching modes are listed in Tables 2 and 3, respectively.

Table 2. The turn-on current and turn-off currents of the N-type Ti-TcFET.

State	$V_{top\text{-}gate}$, $V_{front\text{-}gate}$, $V_{back\text{-}gate}$	I_D (A)	Normalized
Turn-off mode 1	0.8 V, 0 V, 0 V	2.06×10^{-8}	0.0005
Turn-off mode 2	0 V, 0.8 V, 0 V	1.40×10^{-8}	0.0004
Turn-off mode 3	0 V, 0 V, 0.8 V	1.40×10^{-8}	0.0004
Turn-off mode 4	0 V, 0 V, 0 V	1.47×10^{-17}	3.81×10^{-13}
Turn-on mode 1	0 V, 0.8 V, 0.8 V	1.17×10^{-5}	0.3031
Turn-on mode 2	0.8 V, 0 V, 0.8 V	1.17×10^{-5}	0.3031
Turn-on mode 3	0.8 V, 0.8 V, 0 V	1.14×10^{-5}	0.2953
Turn-on mode 4	0.8 V, 0.8 V, 0.8 V	3.86×10^{-5}	1.0000

Table 3. The turn-on current and turn-off currents of the P-type Ti-TcFET.

State	$V_{top\text{-}gate}$, $V_{front\text{-}gate}$, $V_{back\text{-}gate}$	I_D (A)	Normalized
Turn-off mode 1	0 V, 0.8 V, 0.8 V	1.57×10^{-8}	0.0007
Turn-off mode 2	0.8 V, 0 V, 0.8 V	1.06×10^{-8}	0.0004
Turn-off mode 3	0.8 V, 0.8 V, 0 V	1.06×10^{-8}	0.0004
Turn-off mode 4	0.8 V, 0.8 V, 0.8 V	2.75×10^{-17}	1.15×10^{-12}
Turn-on mode 1	0.8 V, 0 V, 0 V	7.48×10^{-6}	0.3116
Turn-on mode 2	0 V, 0.8 V, 0 V	7.09×10^{-6}	0.2954
Turn-on mode 3	0 V, 0 V, 0.8 V	7.09×10^{-6}	0.2954
Turn-on mode 4	0 V, 0 V, 0 V	2.40×10^{-6}	1.0000

Table 2 lists the turn-on current I_{on} and turn-off current I_{off} of the N-type Ti-TcFET in the four turn-on modes and four turn-off modes, respectively. The normalized currents are listed in the rightmost column in Table 2. From Table 2, it can be seen that the maximum turn-off current among the four turn-off modes is 2.06×10^{-8} A, while the minimum turn-on current among the four turn-on modes is 1.14×10^{-5} A. In the worst case, I_{on}/I_{off} (switching current ratio) is 553. In order to increase I_{on}/I_{off}, some new materials such as ferroelectric materials and two-dimensional materials can be used.

Ferroelectric materials can enhance the internal gate voltage through the negative capacitance effect, so that I_{on}/I_{off} (switching current ratio) increases greatly and the subthreshold swing decreases below 60 mV/dec [24]. Two-dimensional (2D) semiconductors, such as transition metal dichalcogenides (TMDs), have the potential for ultra-scaled transistor technology beyond 10 nm node technology because of their atomically thin layered channel and low dielectric constant, which offer strong electrostatic control [25].

Table 3 shows the turn-on current I_{on} and turn-off current I_{off} of the P-type Ti-TcFET in the four turn-on modes and four turn-off modes, respectively. The normalized currents are also listed in the rightmost column in Table 3. From Table 3, it can be seen that the maximum turn-off current among the four turn-off modes is 1.57×10^{-8} A, while the minimum turn-on current among the four turn-on modes is 7.09×10^{-6} A. In the worst case, the switching current ratio is 452.

3.8. Logic Cells Based on Ti-TcFET Devices

A single Ti-TcFET transistor can implement three input "majority-not" switch functions [26,27], and thus only one N-type Ti-TcFET and one P-type Ti-TcFET are needed to realize a "majority-not" logic cell, as shown in Figure 13a. From Figure 13a, the "majority-not" logic cell using traditional CMOS/FinFET devices needs 10 transistors. The transistor counts of the "majority-not" cell using the proposed Ti-TcFET devices is only one-fifth of that of the "majority-not" cell using traditional CMOS/FinFET devices, which shows that the proposed Ti-TcFET devices with three input terminals have a higher information processing capacity than traditional CMOS/FinFETs with a single input terminal.

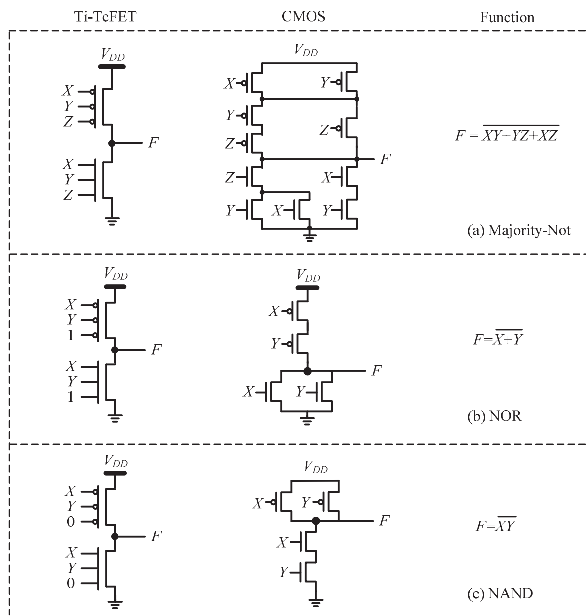

Figure 13. The logic cells based on Ti-TcFET devices: (**a**) majority-not, (**b**) NOT-OR (NOR), and (**c**) NOT-AND (NAND).

The Ti-TcFET devices can also be used to implement other logic gates in a compact style, such as NOR and NAND, as shown in Figure 13b,c, respectively. For more complex logic circuits, such as a full adder, the circuit structure can also be simplified by using Ti-TcFET devices, as shown in Figure 14a. For comparison, Figure 14b shows the full adder using traditional CMOS/FinFETs.

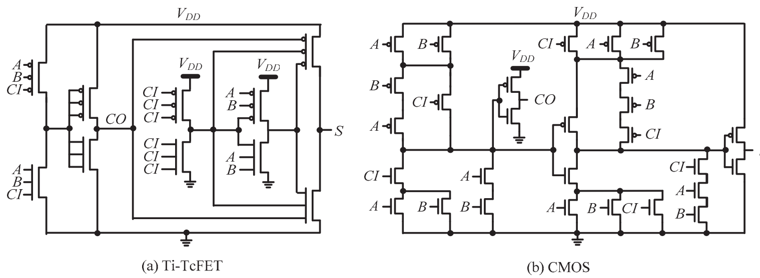

Figure 14. Full adders based on Ti-TcFET devices (**a**) and complementary metal–oxide–semiconductor (CMOS) devices (**b**).

The power consumption, delay, and power delay product of the one-bit full adder using Ti-TcFET devices and standard FinFET devices are compared in Table 4. From Table 4, the power consumption and power delay product of the one-bit full adder based on Ti-TcFET devices are smaller than standard FinFET devices, with an acceptable delay penalty.

Table 4. The power consumption, delay, and power delay product of the one-bit full adder using Ti-TcFET devices and standard FinFET devices.

Full Adder	Power Consumption (nW)	Delay (pS)	Power Delay Product (zJ)
FinFET	19.29	44.38	856
Ti-TcFET	9.26	59.59	554

4. Conclusions

In this paper, a novel T-channel field effect transistor with three input terminals (Ti-TcFET) is proposed. The T-channel structure increases the coupling area between the top gate and the front and back gates so that the device can realize the "majority-not" function well. By adjusting the gate work function, channel thickness, and the thickness of the gate oxide layer, the performance of the Ti-TcFET device is optimized. The results show that when the gate work function Φ of the N-type Ti-TcFET is 4.95 eV, T_{Si} = 4 nm, and T_{OX} = 3 nm, the minimum turn-on current I_{on} is 1.14×10^{-5} A and the maximum turn-off I_{off} is 2.06×10^{-8} A, with the switching current ratio I_{on}/I_{off} of 553. When the gate work function Φ of the P-type Ti-TcFET is 4.52 eV, T_{Si} = 4 nm, and T_{OX} = 3 nm, the minimum turn-on current I_{on} is 7.09×10^{-6} A and the maximum turn-off current I_{off} is 1.57×10^{-8} A, with the switching current ratio I_{on}/I_{off} of 452. The purpose of this paper was to propose a three input device to simplify the circuit structure and thus to provide a new idea for future circuit designs.

In the future, we will optimize the N-type and P-type Ti-TcFETs by applying new materials such as ferroelectric materials and two-dimensional materials, which should be helpful to increase the switching current ratio of the device and to decrease the leakage current.

Author Contributions: Z.C. (Zeqi Chen) and J.H. designed the structure of the device; Z.F.C. (Zhufei Chu) designed the circuits; H.Y. performed the experiments and wrote this paper. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Colinge, J.P.; Gao, M.H.; Romano-Rodriguez, A.; Maes, H.; Claeys, C. Silicon-on-insulator'gate-all-around device'. In Proceedings of the 1990 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 9–12 December 1990; pp. 595–598.
2. Kavalieros, J.; Doyle, B.; Datta, S.; Dewey, G.; Doczy, M.; Jin, B.; Lionberger, D.; Metz, M.; Rachmady, W.; Radosavljevic, M.; et al. Tri-gate transistor architecture with high-k gate dielectrics, metal gates and strain engineering. In Proceedings of the 2006 Symposium on VLSI Technology, 2006. Digest of Technical Papers, Honolulu, HI, USA, 13–15 June 2006; pp. 50–51.
3. Yang, F.L.; Chen, H.Y.; Chen, F.C.; Huang, C.C.; Chang, C.Y.; Chiu, H.K.; Lee, C.C.; Chen, C.C.; Huang, H.T.; Chen, C.J.; et al. 25 nm CMOS omega FETs. In Proceedings of the 2002 International Electron Devices Meeting, San Francisco, CA, USA, 8–11 December 2002; pp. 255–258.
4. Liu, C.; Zheng, F.; Sun, Y.; Li, X.; Shi, Y. Highly flexible SRAM cells based on novel tri-independent-gate FinFET. *Superlattices Microstruct.* **2017**, *110*, 330–338. [CrossRef]
5. Liu, C.; Zheng, F.; Sun, Y.; Li, X.; Shi, Y. Novel tri-independent-gate FinFET for multi-current modes control. *Superlattices Microstruct.* **2017**, *109*, 374–381. [CrossRef]
6. Datta, A.; Goel, A.; Cakici, R.T.; Mahmoodi, H.; Lekshmanan, D.; Roy, K. Modeling and circuit synthesis for independently controlled double gate FinFET devices. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2007**, *26*, 1957–1966. [CrossRef]
7. Tawfik, S.A.; Kursun, V. Low-power and compact sequential circuits with independent-gate FinFETs. *IEEE Trans. Electron Devices* **2007**, *55*, 60–70. [CrossRef]
8. Gupta, S.K.; Kulkarni, J.P.; Roy, K. Tri-mode independent gate FinFET-based SRAM with pass-gate feedback: Technology–circuit co-design for enhanced cell stability. *IEEE Trans. Electron Devices* **2013**, *60*, 3696–3704. [CrossRef]
9. Zhang, X.; Hu, J.; Luo, X. Optimization of dual-threshold independent-gate FinFETs for compact low power logic circuits. In Proceedings of the 2016 IEEE 16th International Conference on Nanotechnology (IEEE-NANO), Sendai, Japan, 22–25 August 2016; pp. 529–532.
10. Ni, H.; Hu, J.; Yang, H.; Zhu, H. Comprehensive Optimization of Dual Threshold Independent-Gate FinFET and SRAM Cells. *Act. Passive Electron. Compon.* **2018**, *2018*, 1–10. [CrossRef]
11. Fried, D.M.; Duster, J.S.; Kornegay, K.T. Improved independent gate N-type FinFET fabrication and characterization. *IEEE Electron Device Lett.* **2003**, *24*, 592–594. [CrossRef]
12. *ATLAS User's Manual Volume I*. Silvaco International. Available online: https://dynamic.silvaco.com/dynamicweb/jsp/downloads/DownloadManualsAction.do?req=silen-manuals&nm=atlas (accessed on 30 August 2016).
13. Amaru, L.; Gaillardon, P.E.; De Micheli, G. Majority-inverter graph: A new paradigm for logic optimization. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2015**, *35*, 806–819. [CrossRef]
14. Amarú, L.; Gaillardon, P.E.; De Micheli, G. Majority-inverter graph: A novel data-structure and algorithms for efficient logic optimization. In Proceedings of the 51st Annual Design Automation Conference, San Francisco, CA, USA, 1 June 2014; pp. 1–6.
15. Han, J.W.; Kim, C.J.; Choi, Y.K. Universal potential model in tied and separated double-gate MOSFETs with consideration of symmetric and asymmetric structure. *IEEE Trans. Electron Devices* **2008**, *55*, 1472–1479. [CrossRef]
16. Ghai, D.; Mohanty, S.P.; Thakral, G. Comparative analysis of double gate FinFET configurations for analog circuit design. In Proceedings of the 2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS), Columbus, OH, USA, 4 August 2013; pp. 809–812.
17. Granzner, R.; Schwierz, F.; Polyakov, V.M. An analytical model for the threshold voltage shift caused by two-dimensional quantum confinement in undoped multiple-gate MOSFETs. *IEEE Trans. Electron Devices* **2007**, *54*, 2562–2565. [CrossRef]
18. Fossum, J.G. Physical insights on nanoscale multi-gate CMOS design. *Solid-State Electron.* **2007**, *51*, 188–194. [CrossRef]
19. Hu, C. Low-voltage CMOS device scaling. In Proceedings of the IEEE International Solid-State Circuits Conference-ISSCC'94, San Francisco, CA, USA, 16 February 1994; pp. 86–87.

20. Lin, X.; Wang, Y.; Pedram, M. Stack sizing analysis and optimization for FinFET logic cells and circuits operating in the sub/near-threshold regime. In Proceedings of the Fifteenth International Symposium on Quality Electronic Design, Santa Clara, CA, USA, 3 March 2014; pp. 341–348.
21. Harris, D.M.; Keller, B.; Karl, J.; Keller, S. A transregional model for near-threshold circuits with application to minimum-energy operation. In Proceedings of the 2010 International Conference on Microelectronics, Cairo, Egypt, 19 December 2010; pp. 64–67.
22. Rostami, M.; Mohanram, K. Dual-V_{th} independent-gate FinFETs for low power logic circuits. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2011**, *30*, 337–349. [CrossRef]
23. Masahara, M.; Surdeanu, R.; Witters, L.; Doornbos, G.; Nguyen, V.H.; Vrancken, C.; Jurczak, M.; Biesemans, S. Experimental investigation of optimum gate workfunction for CMOS four-terminal multigate MOSFETs (MUGFETs). *IEEE Trans. Electron Devices* **2007**, *54*, 1431–1437. [CrossRef]
24. McGuire, F.A.; Lin, Y.C.; Price, K.; Rayner, G.B.; Khandelwal, S.; Salahuddin, S.; Franklin, A.D. Sustained sub-60 mV/decade switching via the negative capacitance effect in MoS_2 transistors. *Nano Lett.* **2017**, *17*, 4801–4806. [CrossRef]
25. Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-layer MoS_2 transistors. *Nat. Nanotechnol.* **2011**, *6*, 147–150. [CrossRef] [PubMed]
26. Chu, Z.; Tang, X.; Soeken, M.; Petkovska, A.; Zgheib, G.; Amarù, L.; Xia, Y.; Ienne, P.; De Micheli, G.; Gaillardon, P.E. Improving circuit mapping performance through mig-based synthesis for carry chains. In Proceedings of the on Great Lakes Symposium on VLSI 2017, New York, NY, USA, 10 May 2017; pp. 131–136.
27. Navi, K.; Moaiyeri, M.H.; Mirzaee, R.F.; Hashemipour, O.; Nezhad, B.M. Two new low-power full adders based on majority-not gates. *Microelectron. J.* **2009**, *40*, 126–130. [CrossRef]

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150–200 V Split-Gate Trench Power MOSFETs with Multiple Epitaxial Layers

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Abstract: A rating voltage of 150 and 200 V split-gate trench (SGT) power metal-oxide- semiconductor field-effect transistor (Power MOSFET) with different epitaxial layers was proposed and studied. In order to reduce the specific on-resistance ($R_{on,sp}$) of a 150 and 200 V SGT power MOSFET, we used a multiple epitaxies (EPIs) structure to design it and compared other single-EPI and double-EPIs devices based on the same fabrication process. We found that the bottom epitaxial (EPI) layer of a double-EPIs structure can be designed to support the breakdown voltage, and the top one can be adjusted to reduce the $R_{on,sp}$. Therefore, the double-EPIs device has more flexibility to achieve a lower $R_{on,sp}$ than the single-EPI one. When the required voltage is over 100 V, the on-state resistance (R_{on}) of double-EPIs device is no longer satisfying our expectations. A triple-EPIs structure was designed and studied, to reduce its R_{on}, without sacrificing the breakdown voltage. We used an Integrated System Engineering-Technology Computer-Aided Design (ISE-TCAD) simulator to investigate and study the 150 V SGT power MOSFETs with different EPI structures, by modulating the thickness and resistivity of each EPI layer. The simulated $R_{on,sp}$ of a 150 V triple-EPIs device is only 62% and 18.3% of that for the double-EPIs and single-EPI structure, respectively.

Keywords: split-gate trench power MOSFET; multiple epitaxial layers; specific on-resistance

1. Introduction

Trench power MOSFETs have become a superior device in the medium-to-low voltage power application field. In conventional trench MOSFETs, the gate is isolated from the drain region only by the gate oxide. This results in that trench MOSFETs exhibit large switching losses due to a high gate-to-drain capacitance (C_{gd}), which limits its application. In order to reduce the device-switching losses, many studies, such as a thick-bottom oxide layer (TBOX) design, W-gated, and RESURF stepped oxide (RSO) MOSFET, were proposed [1–4]. All of these structures feather a thick oxide between gate electrodes and drain area, to reduce device C_{gd}. The RSO structure uses a thicker oxide at the lower portion of the trench, to reduce C_{gd}, while it applies a thinner one at the upper portion of the trench, to be the gate oxide. Because the stepped gate electrode plays a role as an extended field plate (FP) to modulate the electric field (EF) around it, this structure not only reduces the feedback capacitance but also the R_{on}, by using a low-resistivity epitaxial layer. Although RSO design can reduce the C_{gd}, switching losses are still a big issue when a device is used in a high-frequency application. Split-gate trench (SGT) devices overcame that problem by adding a source electrode located between the gate and drain [5–9]. There are two parts in the trenches for a split-gate structure: The upper electrode is

the gate, and the lower one is connected by a separate contact to the source, to play as a field plate to balance the charge in the n^- drift epitaxy region. This field plate is surrounded with a thick oxide to be a MOS structure that induces a silicon depletion region once the electrode is biased at a more negative potential than the n^- silicon region [10–12]. Furthermore, the extended field plate along the drift epitaxy layer shapes the electric field in the drift region that enables the drift depletion area to support a higher drain voltage by using a lower resistivity epitaxy layer to reduce device specific on-resistance [5,13]. In addition, the C_{gd} of an SGT can be reduced significantly because the gate electrodes are shielded from the drain region by these FPs [10,14,15].

Even RSO and SGT power MOSFETs can provide an effective way to reduce device feedback capacitance and R_{on} simultaneously. The on-state resistance for a device used in a higher voltage system (100 to 200 V) increases sharply, owing to a high-resistivity epitaxial layer. For 20–30 V low-voltage SGT devices, the channel resistance portion is dominant and amounts to over 60%–85% of the total device resistance. However, this channel resistance is reduced to only 30%–20% for 60–70 V middle-voltage-rating devices [16,17]. When the device rating voltage reaches 150–200 V, the drift resistance occupies about 90% of the total device resistance [16,18]. To achieve a high breakdown voltage (V_{BR}) design without increasing the R_{on} too much, a gradient, two-stepped oxide or multiple stepped oxide designs were applied to the trenches and shown to improve device performance effectively [18–21]. Since the potential of the field plate (bottom gate) on the oxide around it is different everywhere, that leads to a different depletion strength and electric field between two trenches along the cell depth, [18–21] use oxide engineering to improve device performance. On the other hand, double split-gate resurf stepped oxide UMOS can overcome the non-uniform problem [15]; however, the oxide and poly process in the trenches is too complicated. The abovementioned methods could make the drift region have a more uniform EF distribution to sustain a higher V_{BR}. However, these structures required multiple depositions and etching steps that complicate the fabrication process. Superjunction structures and wide bandgap SiC material devices are alternative ways to provide high-voltage and low-$R_{on,sp}$ solutions [22–25]. However, the built-in superjunction depletion layer limits the scalability to lower voltages (<500 V) [3]. In addition, besides cost issues, low channel mobility owing to a high density of SiC/SiO_2 interface traps and undesirable higher turn on voltage of the body diode of a wide bandgap SiC power MOSFET make SiC devices less attractive than Si ones for lower-voltage applications [26–28]. Lower-voltage SiC power MOSFETs have not yet been demonstrated [10]. For a device structure with a rating voltage below 200 V, Si SGT power MOSFET dominates and plays an important role in reducing the device $R_{on,sp}$ in power applications.

In this study, we proposed a 150 V SGT power MOSFET with multiple EPIs, to improve the device characteristics, and applied the same way to design a 200 V SGT power device. The single-EPI structures are wildly used in the low-voltage (<50 V) SGT power MOSFETs design. When required device rating voltage is up to 50–100 V, single-EPI device makes this scheme suffer a sharply increased R_{on}. A double-EPI-layers structure was used to improve device R_{on} characteristics in some studies [29,30]. Compared to the single-EPI one, the double-EPIs device has a higher device output current than the single one. This unique merit allows for the possibility of the double-EPIs design to reduce $R_{on,sp}$, as well as its power consumption. In this study, we wanted to design and modify the EPI structures rather than the complicated fabrication ways mentioned in [15,18–21], to reduce device R_{on} and sustain a high V_{BR} at the same time. When device ranting voltage is designed to over 100 V, we find that the R_{on} of double-EPIs structure is no longer satisfying our expectations. Therefore, a triple-EPIs structure was applied, to modify the EF distributions between two trenches, instead of only depending on its magnitude supported by the bottom EPI. This design makes us have more flexibilities in designing the bottom EPI with a lower resistivity specification, to achieve a lower $R_{on,sp}$ device. In double-EPIs design, the bottom EPI layer is used to support the V_{BR}, and the top one could be used to modify the EF and reduce the R_{on}. For a triple-EPIs structure, the top and bottom EPI layers play the same roles as those is the double-EPIs device. The middle one is used to lower the $R_{on,sp}$ if the top and bottom EPI layers can be properly designed. We applied ISE-TCAD to simulate and investigate by analyzing

device potential and EF distributions with different epitaxial layers for all devices [31]. The $R_{on,sp}$ of a triple-epitaxial-layer structure is much lower than those applied with a single- or double-epitaxial layer based on the same fabrication process.

2. Device Structure and Simulation

Multiple EPI structures were applied in this study. Figure 1 shows the trench location related to each structure with different epitaxial layers designs. The process steps of simulation for a three-epitaxial-layer device are shown in Figure 2. We started with a designed three EPIs above an n^+ substrate. Detailed layers' information is listed in Table 1. A trench was first defined and etched to the top of the bottom EPI. An oxide and polysilicon (Poly-Si) were sequentially deposited. After that, the deposited Poly-Si was etched back, to form a bottom gate. Then, the gate oxide was grown thermally, and a Poly-Si layer was deposited to fill the trenches and then etched to play the gates. Next, the device was implanted to accomplish the p^--well and n^+-well as the channel and the source region, respectively. After an oxide was deposited and contact holes were opened, an etching process was applied, and a p^+ implantation was employed to improve the device's ruggedness. Finally, a metal was formed to be the source electrode. Figure 3 shows the cross-section of this SGT power MOSFET structure with three epitaxial layers.

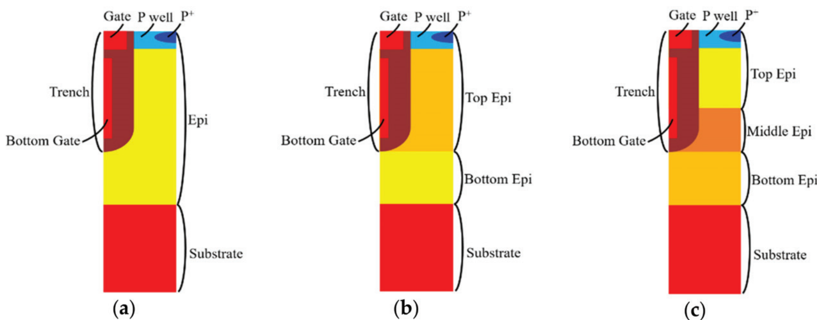

Figure 1. Split-gate trench power MOSFET structure with (**a**) single EPI, (**b**) double EPIs, and (**c**) triple EPIs.

Table 1. The simulation parameters that were used for the triple-EPIs structure.

Parameter	Value
Cell pitch	3.24 µm
Thickness of top EPI	4 µm
Resistance of top EPI	0.9 Ω·cm
Thickness of middle EPI	2 µm
Resistance of middle EPI	0.16 Ω·cm
Thickness of bottom EPI	4 µm
Resistance of bottom EPI	0.68 Ω·cm
Depth of trench	6 µm
Width of trench	1.8 µm
Thickness of bottom oxide	0.8 µm
Thickness of gate oxide	0.06 µm

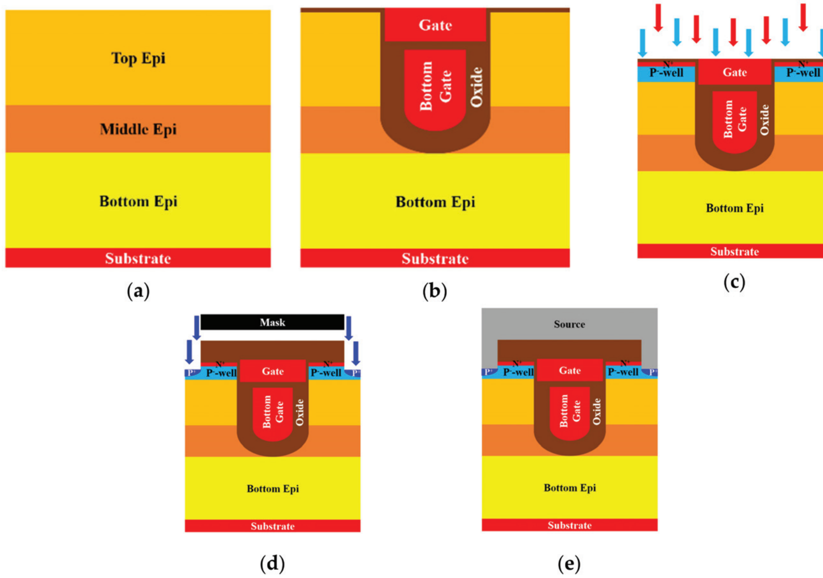

Figure 2. Main simulated fabrication process for the triple-EPIs SGT power MOSFET: (**a**) three designed epitaxial layers; (**b**) defining the trench, bottom gate, and gate; (**c**) forming the channel and the source areas; (**d**) opening the contact holes and implanting the p^+; (**e**) depositing the metal pads.

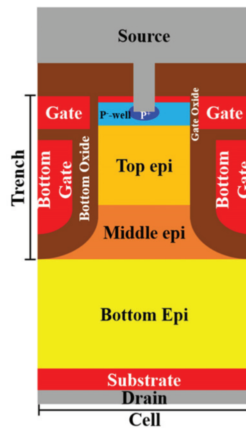

Figure 3. The cross-section diagram of a triple-EPIs SGT power MOSFET.

3. Results and Discussion

First, we constructed a 150 V device by using a double-EPIs structure. The trench depth we used here was 6 µm, from the top to the bottom EPI. For a double-EPIs structure, to improve its V_{BR}, a thicker thickness or a higher-resistivity bottom EPI is required. However, it will increase R_{on} significantly. Then, we apply the same EPI thickness and trench depth as double-EPIs structure to all devices in the simulation. For comparison, we adopted the same bottom EPI specification for the double structure used as for the single-EPI device. For a triple-EPIs device, the EPI specifications are adjusted to achieve a balance to have a maximum V_{BR} and a minimum $R_{on,sp}$. The EPI information for all structures is list in Table 2. All the devices simulated here use the same trench depth (6 µm). Different top- and

middle-EPI-thickness designs are studied for a triple-EPIs device. Figure 4a shows the EF distributions with different top- and middle-EPI-thickness designs. We can see that the EF distributions between two trenches can be modified by different top and middle EPI thickness. Our approach to improving the EF distributions between two trenches is similar to that proposed in [15]. We used triple EPIs and [15] double split-gates with different bias in the trenches, to achieve the same purpose. The R_{on} is not affected by the top EPI too much; however, different electric field distributions with different EPI combinations here give us more room to design a high V_{BR} device. One can expect that the highest breakdown voltage can be obtained in the largest area of the EF integration, with respect to the cell depth [19,22]. In our study, the best top-and middle-EPI-thickness ratio to sustain a high V_{BR} device is 1:2. Figure 4b presents the simulated V_{BR} and $R_{on,sp}$ with different EPI-thickness designs.

Table 2. The parameters that were used for the single-, double-, and triple-EPI structure simulation.

Device	EPI Thickness (μm)	EPI Resistance (Ω·cm)
Single EPI	10	1.4
Double EPIs	Top EPI = 6 Bottom EPI = 4	Top EPI = 0.35 Bottom EPI = 1.4
Triple EPIs	Top EPI = 4 Middle EPI = 2 Bottom EPI = 4	Top EPI = 0.9 Middle EPI = 0.16 Bottom EPI = 0.68

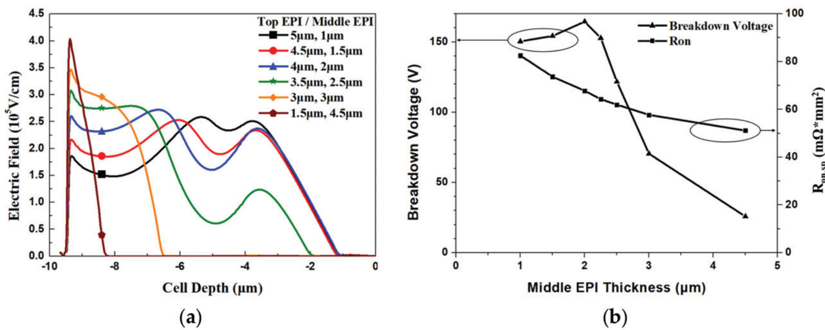

Figure 4. (**a**) The simulated electric field curves in the middle of the cell and (**b**) the simulated V_{BR} and $R_{on,sp}$ with different top- and middle-EPI-thickness designs with the same total and bottom EPI thickness.

Figures 5 and 6 show the simulated potential and EF distributions for all structures under the same total EPI thickness. From the simulation, it is obvious that the triple-EPIs device can sustain a higher V_{BR} easily than the others. A middle EPI layer is used to increase the EF magnitudes and then enhance the breakdown, as well as lower the $R_{on,sp}$ simultaneously. In addition, it offers us more flexibility to adjust the resistivity of the bottom EPI, to further reduce its $R_{on,sp.}$ The EF distribution curves in the cell center for all structures are shown in Figure 7. From this figure, the triple-EPIs design shows it has more uniform EF distributions between two trenches to sustain a higher V_{BR}. In Figure 7, it is obvious that the two-layer structure can increase the device top electric field between two trenches; however, it decreases to a low value at p^--well/n^-EPI as the single one does. A triple-EPIs structure is designed to enhance the device EF between two trenches at the top and p^- well/n^- EPI area between two trenches to enhance device breakdown voltage. From Figure 7, we can observe a more uniform electric field distribution and the largest area under EF integration along the cell depth can be found in the triple-EPIs design. Therefore, the breakdown voltage of a triple-EPIs device can be improved. All devices' performances are summarized in Table 3. By using the same EPI thickness, the triple-EPIs design has the highest breakdown voltage than other EPI structures.

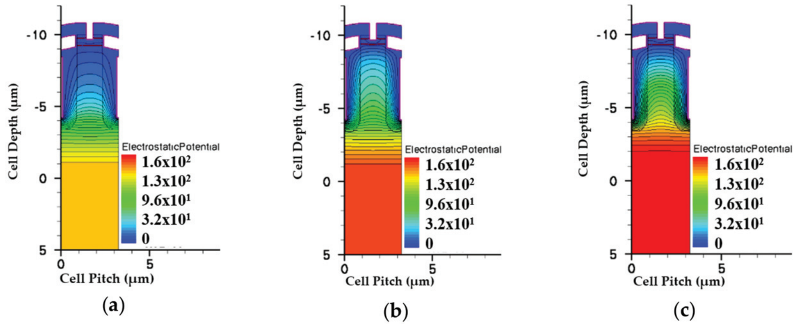

Figure 5. The simulated potentials for the split-gate trench power MOSFET with (**a**) single EPI, (**b**) double EPIs, and (**c**) triple EPIs at the same EPI thickness. The color bars are scaled on the same degree.

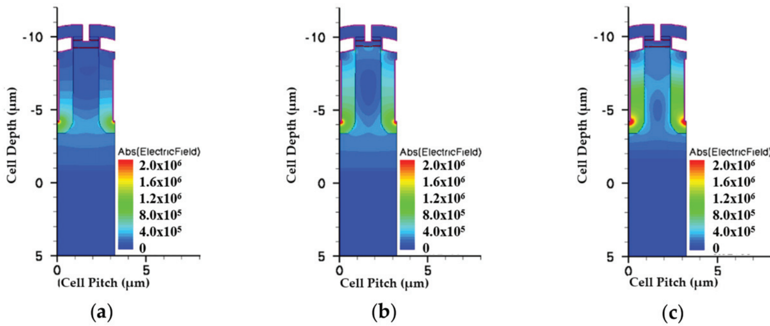

Figure 6. The simulated electric fields for the split-gate trench power MOSFET with (**a**) single EPI, (**b**) double EPIs, and (**c**) triple EPIs at the same EPI thickness. The color bars are scaled on the same degree.

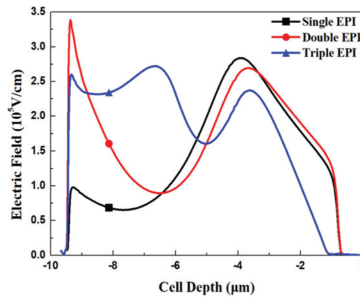

Figure 7. The simulated electric field curves for all devices with single EPI, double EPIs, and triple EPIs with the same total EPI thickness.

Table 3. The characteristics of single-EPI, double-EPIs, and triple-EPIs SGT power MOSFET with the same total EPI thickness.

Device	Breakdown Voltage (V)	R_{on} (m$\Omega\cdot$mm^2)	EPI Thickness (μm)
Single EPI	130.93	181.16	10
Double EPIs	153.85	98.23	10
Triple EPIs	164.49	67.79	10

Then we modified single-EPI and double-EPIs specifications to sustain the same V_{BR} that a triple design can achieve. To increase the V_{BR} of these two devices, the thickness and resistance of each EPI layer, as well as the trench depth, have to be increased. The EPI information for all structures is list in Table 4. Figure 8 shows the potential profiles for all devices. It can be seen that, in order to sustain a higher rating voltage, the thickness and resistivity of the single-EPI and double-EPIs structure must be thickened and increased to achieve a high V_{BR}. The EF magnitude distributions of all structures are shown in Figures 9 and 10. We can find that, the less EPI layers that are used, the lower the electric field valley, which weakens the support of a high V_{BR} with a small $R_{on,sp}$. The triple-EPIs structure uses a middle EPI to enhance its electric field in the middle of the trench, where there is an EF valley observed in other structures. Therefore, a triple-EPIs structure is much easy to sustain a high V_{BR} than other devices.

Table 4. The parameters that were used for the single-EPI, double-EPIs, and triple-EPIs structure simulation.

Device	EPI Thickness (μm)	EPI Resistance (Ω·cm)	Trench Depth (μm)
Single EPI	15	2	8
Double EPIs	Top EPI = 9 Bottom EPI = 4	Top EPI = 0.35 Bottom EPI = 1.4	8
Triple EPIs	Top EPI = 4 Middle EPI = 2 Bottom EPI = 4	Top EPI = 0.9 Middle EPI = 0.16 Bottom EPI = 0.68	6

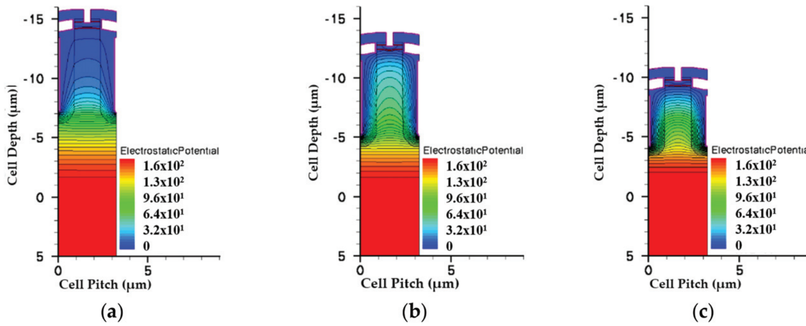

Figure 8. The simulated potentials for the split-gate trench power MOSFET with (**a**) single EPI, (**b**) double EPIs, and (**c**) triple EPIs at 150 V rating voltage. The color bars are scaled on the same degree.

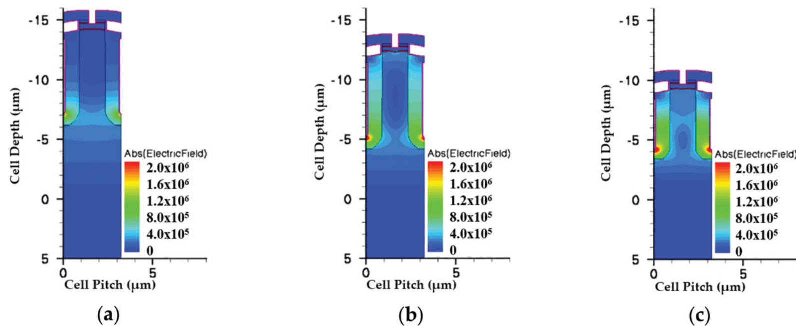

Figure 9. The simulated electric fields for the split-gate trench power MOSFET with (**a**) single EPI, (**b**) double EPIs, and (**c**) triple EPIs at 150 V rating voltage. The color bars are scaled on the same degree.

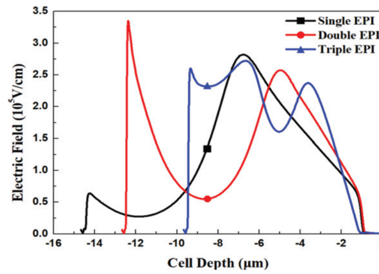

Figure 10. The simulated electric field curves for the split-gate trench power MOSFET with single EPI, double EPIs, and triple EPIs at 150 V rating voltage.

Figure 11 shows the output characteristics for all structures with the same V_{BR} of 164 V. It can be observed that the R_{on} of a triple-EPIs design is much lower than those of the others. The triple-EPIs structure can sustain a higher V_{BR}, owing to a more uniform electric field distribution between two trenches that is attributed to top- and middle-EPI design. It makes a triple-EPIs device more flexible on resistivity and thickness design for bottom EPI to achieve a low R_{on} characteristic. Table 5 demonstrates the $R_{on,sp}$ for all devices with the same V_{BR}. The simulated $R_{on,sp}$ of a triple-EPIs device with a rating voltage of 150 V is only 62% and 18.3% of the one for the double-EPIs and single-EPI structure, respectively. Although a double-EPIs structure has better $R_{on,sp}$ than the single one, the long trench depth, accompanied by a long top EPI thickness, makes it is hard to maintain a uniform electric field between two trenches. Therefore, a higher resistivity bottom EPI spec is required to sustain a high rating voltage that results in a higher R_{on} than the triple-EPIs design. Compared with other methods mentioned in [15,18–21], the multiple-EPIs structure does not complicate the process in manufacturing, and a higher-V_{BR} and a lower-$R_{on,sp}$ device can be achieved.

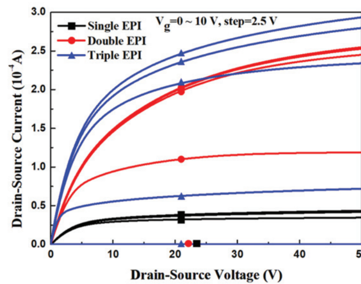

Figure 11. The output characteristic of the split-gate trench power MOSFET with single EPI, double EPIs, and triple EPIs.

Table 5. The characteristic of single-EPI, double-EPIs, and triple-EPIs 150 V rating voltage split-gate trench power MOSFET at the same cell pitch.

Device	Breakdown Voltage (V)	R_{on} (mΩ·mm^2)	Cell Pitch (μm)
Single EPI	164.2	369.85	3.24
Double EPIs	164.23	109.56	3.24
Triple EPIs	164.49	67.79	3.24

We also use the same method to construct 200 V SGT devices with different EPI designs. Similar electrical field distributions and output characteristics with Figures 10 and 11 can be obtained, respectively, if we modify the best epitaxial specification. Table 6 lists the parameters that we used for all 200 V SGT devices' simulation and shows their characteristics. Again, the triple-EPIs structure

demonstrates more flexibility to achieve a lower $R_{on,sp}$ than the single-EPI and double-EPIs devices under the same breakdown voltage design.

Table 6. The parameters that were used for the single-EPI, double-EPIs, and triple-EPIs structure simulation.

Device	EPI Thickness (μm)	EPI Resistance (Ω·cm)	Breakdown Voltage (V)	R_{on} (mΩ·mm^2)
Single EPI	16	4.8	222.79	729.7
Double EPIs	Top EPI = 6 Bottom EPI = 9	Top EPI = 0.3 Bottom EPI = 3	221.73	286.47
Triple EPIs	Top EPI = 4 Middle EPI = 2 Bottom EPI = 7.5	Top EPI = 0.8 Middle EPI = 0.17 Bottom EPI = 2.1	221.33	184.36

Figure 12 compares the specific on-resistance performance of our proposed SGT devices with that of the other middle-voltage devices reported in [4,15,21,32–40], ideal silicon limit, and super junction (SJ) limit for cell pitch = 5 and 10 μm in the 50–200 V range. Form Figure 12, we observe that the triple-EPIs structure and those using a double split-gate device [15] and stepped oxide SGTs [18,20,21] can achieve a very low $R_{on,sp}$ in the middle-voltage range because they all can maintain more uniform EF distributions between two trenches. Compared with a double split-gate device and stepped oxide ones, our triple-EPIs devices do not require the complicated double split-gate or oxide-engineering process in the trenches and is compatible with the conventional SGT process.

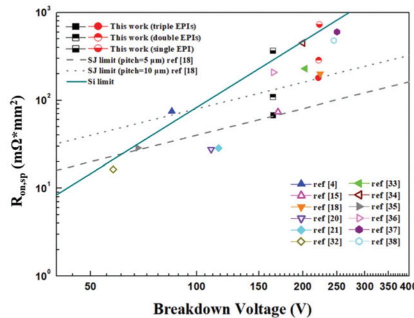

Figure 12. The comparison of $R_{on,sp}$ against V_{BR} relationship of middle-voltage SGT structures, super junction devices, ideal silicon limit and super junction (SJ) limit (cell pitch = 5 and 10 μm).

4. Conclusions

A 150–200 V rating voltage triple-EPIs SGT-power MOSFET was proposed, studied, and compared with a single-EPI and double-EPIs structure. The middle EPI in the triple-EPIs structure is used to increase the low electric field between two trenches, thereby increasing the breakdown voltage and reducing the on-resistance. Compared with the single-EPI and double-EPIs structures, the triple-EPIs SGT-power MOSFET had a lower on-resistance. The simulated $R_{on,sp}$ of a triple-EPIs device with a rating voltage of 150 V is only 62% and 18.3% of the one for the double-EPIs and single-EPI structure, respectively.

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References

1. Takaya, H.; Morimoto, J.; Hamada, K.; Yamamoto, T.; Sakakibara, J.; Watanabe, Y.; Soejima, N. A 4H-SiC trench MOSFET with thick bottom oxide for improving characteristics. In Proceedings of the 25th International Symposium on Power Semiconductor Devices & ICs, Kanazawa, Japan, 26–30 May 2013; pp. 43–46.
2. Darwish, M.; Yue, C.; Lui, K.H.; Giles, F.; Chan, B.; Chen, K.i.; Pattanayak, D.; Chen, Q.; Terrill, K.; Owyang, K. A new power W-gated trench MOSFET (WMOSFET) with high switching performance. In Proceedings of the 15th International Symposium on Power Semiconductor Devices & ICs, Cambridge, UK, 14–17 April 2003; pp. 24–27.
3. Gajda, M.A.; Hodgkiss, S.W.; Mounfield, L.A.; Irwin, N.T.; Koops, G.E.J.; Dalen, R.V. Industrialisation of resurf stepped oxide technology for power transistors. In Proceedings of the 18th International Symposium on Power Semiconductor Devices & ICs, Naples, Italy, 4–8 June 2006; pp. 109–112.
4. Koops, G.E.J.; Hijzen, E.A.; Hueting, R.J.E.; Zandt, M.A.A. RESURF stepped oxide (RSO) MOSFET for 85V having a record-low specific on-resistance. In Proceedings of the 16th International Symposium on Power Semiconductor Devices & ICs, Kitakyushu, Japan, 24–27 May 2004; pp. 185–188.
5. Goarin, P.; Koops, G.E.J.; Van Dalen, R.; Cam, C.L.; Saby, J. Split-gate resurf Oxide (RSO) MOSFETs for 25V applications with record low gate-to-drain charge. In Proceedings of the 19th International Symposium on Power Semiconductor Devices & ICs, Jeju, Korea, 27–30 May 2007; pp. 61–64.
6. Vershinin, K.; Moens, P.; Bauwens, F.; Narayanan, E.M.S.; Tack, M. A new method to improve tradeoff performance for advanced power MOSFETs. *IEEE Electron. Device Lett.* **2009**, *30*, 416–418. [CrossRef]
7. Baliga, B.J. Power Semiconductor Devices having Improved High Frequency Switching and Breakdown Characteristics. U.S. Patent 5998833, 7 December 1999.
8. Zeng, J. Ultra Dense Trench-Gated Power Device with the Reduced Drain-Source Feedback Capacitance and Miller Charge. U.S. Patent 6 683 346, 27 January 2004.
9. Zhang, W.; Ye, L.; Fang, D.; Qizo, M.; Xizo, K.; He, B.; Li, Z.; Zhang, B. Model and experiments of small-size vertical devices with field plate. *IEEE Trans. Electron. Devices* **2019**, *66*, 1416–1421. [CrossRef]
10. Williams, R.K.; Darwish, M.N.; Blanchard, R.A.; Siemieniec, R.; Rutter, P.; Kawaguchi, Y. The trench power MOSFET: Part I—history, technology, and prospects. *IEEE Trans. Electron. Devices* **2017**, *64*, 674–691. [CrossRef]
11. Kobayashi, K.; Sudo, M.; Omura, I. Power loss analysis of 60 V trench field-plate MOSFETs utilizing structure based capacitance model for automotive application. In Proceedings of the 10th International Conference on Integrated Power Electronics Systems, Stuttgart, Germany, 20–22 March 2018; pp. 122–127.
12. Kobayashi, K.; Sudo, M.; Omura, I. Structure-based capacitance modeling and power loss analysis for the latest high-performance slant field-plate trench MOSFET. *Jpn. J. Appl. Phys.* **2018**, *57(4S)*, 04FR14. [CrossRef]
13. Peake, S.T.; Rutter, P.; Hodgskiss, S.; Gajda, M.; Irwin, N. A fully realized 'field balanced' trenchMOS technology. In Proceedings of the 20th International Symposium on Power Semiconductor Devices & ICs, Orlando, FL, USA, 18–22 May 2008; pp. 28–31.
14. Williams, R.K.; Darwish, M.N.; Blanchard, R.A.; Siemieniec, R.; Rutter, P.; Kawaguchi, Y. The trench power MOSFET—Part II: Application specific VDMOS, LDMOS, packaging, and reliability. *IEEE Trans. Electron. Devices* **2017**, *64*, 692–712. [CrossRef]
15. Wang, Y.; Hu, H.F.; Dou, Z.; Yu, C.H. Way of operation to improve performance for advanced split-gate resurf stepped oxide UMOSFET. *IET Power Electron.* **2014**, *7*, 2964–2968. [CrossRef]
16. Park, C.; Havanur, S.; Shibib, A.; Terrill, K. 60 V rating split gate trench MOSFETs having best-in-class specific resistance and figure-of-merit. In Proceedings of the 28th International Symposium on Power Semiconductor Devices & ICs, Prague, Czech Republic, 12–16 June 2016; pp. 387–390.
17. Takaya, H.; Miyagi, K.; Hamada, K.; Okura, Y.; Tokura, N.; Kuroyanagi, A. Floating island and thick bottom oxide trench gate MOSFET (FITMOS)—A 60V ultra low on-resistance novel MOSFET with superior internal body diode. In Proceedings of the 17th International Symposium on Power Semiconductor Devices & ICs, Santa Barbara, CA, USA, 23–26 June 2005; pp. 1–4.

18. Park, C.; Azam, M.; Dengel, G.; Shibib, A.; Terrill, K. A new 200 V dual trench MOSFET with stepped oxide for ultra low RDS(on). In Proceedings of the 31st International Symposium on Power Semiconductor Devices & ICs, Shanghai, China, 19–23 May 2019; pp. 95–98.
19. Chen, Y.; Liang, Y.C.; Samudra, G.S. Design of gradient oxide-bypassed superjunction power MOSFET devices. *IEEE Trans. Power Electron.* **2007**, *22*, 1303–1310. [CrossRef]
20. Kobayashi, K.; Kato, H.; Nishiguchi, T.; Shimomura, S.; Ohno, T.; Nishiwaki, T.; Aida, K.; Ichinoseki, K.; Oasa, K.; Kawaguchi, Y. 100-V class two-step-oxide field-plate trench MOSFET to achieve optimum RESURF effect and ultralow on-resistance. In Proceedings of the 31st International Symposium on Power Semiconductor Devices & ICs, Shanghai, China, 19–23 May 2019; pp. 99–102.
21. Kobayashi, K.; Nishiguchi, T.; Katoh, S.; Kawano, T.; Kawaguchi, Y. 100 V class multiple stepped oxide field plate trench MOSFET (MSO-FP-MOSFET) aimed to ultimate structure realization. In Proceedings of the 27th International Symposium on Power Semiconductor Devices & ICs, Kowloon Shangri-La, Hong Kong, 10–14 May 2015; pp. 141–144.
22. Daniel, B.J.; Parikh, C.D.; Patil, M.B. Modeling of the coolMOS/sup TM/ transistor—Part I: Device physics. *IEEE Trans. Electron. Devices* **2002**, *49*, 916–922. [CrossRef]
23. Lorenz, L.; Deboy, G.; Knapp, A.; Marz, M. COOLMOS/sup TM/-a new milestone in high voltage power MOS. In Proceedings of the 11th International Symposium on Power Semiconductor Devices & ICs, Toronto, ON, Canada, 26–28 May 1999; pp. 3–10.
24. Kondekar, P.N.; Parikh, C.D.; Patil, M.B. Analysis of breakdown voltage and on resistance of super junction power MOSFET CoolMOS/sup TM/ using theory of novel voltage sustaining layer. In Proceedings of the 33rd Annual IEEE Power Electronics Specialists Conference, Cairns, QLD, Australia, 23–27 June 2002; pp. 1769–1775.
25. Tian, K.; Hallén, A.; Qi, J.; Shenhui, M.; Fei, X.; Zhang, A.; Liu, W. An improved 4H-SiC trench-gate MOSFET with low on-resistance and switching loss. *IEEE Trans. Electron. Devices* **2019**, *66*, 2307–2313. [CrossRef]
26. Chen, L.; Guy, O.J.; Jennings, M.R.; Igic, P.; Wilks, S.P.; Mawby, P.A. Study of 4H–SiC trench MOSFET structures. *Solid State Electron.* **2005**, *49*, 1081–1085. [CrossRef]
27. Palmour, J.W.; Cheng, L.; Pala, V.; Brunt, E.V.; Lichtenwalner, D.J.; Wang, G.; Richmond, J.; O'Loughlin, M.; Ryu, S.; Allen, S.T.; et al. Silicon carbide power MOSFETs: Breakthrough performance from 900 V up to 15 kV. In Proceedings of the 26th International Symposium on Power Semiconductor Devices & ICs, Waikoloa, HI, USA, 15–19 June 2014; pp. 79–82.
28. Li, X.; Tong, X.; Huang, A.Q.; Tao, H.; Zhou, K.; Jiang, Y.F.; Jiang, J.N.; Deng, X.C.; She, X.; Zhang, B.; et al. SiC trench MOSFET with integrated self-assembled three-level protection schottky barrier diode. *IEEE Trans. Electron. Devices* **2018**, *65*, 347–351. [CrossRef]
29. Wang, Q.; Li, M.; Sharp, J.; Challa, A. The effects of double-epilayer structure on threshold voltage of ultralow voltage trench power MOSFET devices. *IEEE Trans. Electron. Devices* **2007**, *54*, 833–839. [CrossRef]
30. Li, M.; Crellin, A.; Ho, I.; Wang, Q. Double-epilayer structure for low drain voltage rating n-channel power trench MOSFET devices. *IEEE Trans. Electron. Devices* **2008**, *55*, 1749–1755. [CrossRef]
31. *ISE-TCAD Manuals*; Release 10.0; Integrated Systems Engineering: Zurich, Switzerland, 2004.
32. Yamaguchi, H.; Urakami, Y.; Sakakibara, J. Breakthrough of on-resistance Si limit by Super 3D MOSFET under 100V breakdown voltage. In Proceedings of the 18th International Symposium on Power Semiconductor Devices & ICs, Naples, Italy, 4–8 June 2006.
33. Hattori, Y.; Nakashima, K.; Kuwahara, M.; Yoshida, T.; Yamauchi, S.; Yamaguchi, H. Design of a 200V super junction MOSFET with n-buffer regions and its fabrication by trench filling. In Proceedings of the 16th International Symposium on Power Semiconductor Devices & ICs, Kitakyushu, Japan, 24–27 May 2004; pp. 189–192.
34. Weber, Y.; Morancho, F.; Reynes, J.; Stefanov, E. A New Optimized 200V Low On-Resistance Power FLYMOSFET. In Proceedings of the 20th International Symposium on Power Semiconductor Devices & ICs, Orlando, FL, USA, 18–22 May 2008; pp. 149–152.
35. Miura, Y.; Ninomiya, H.; Kobayashi, K. High performance superjunction UMOSFETs with split p-columns fabricated by multi-ion-implantations. In Proceedings of the 17th International Symposium on Power Semiconductor Devices & ICs, Santa Barbara, CA, USA, 23–26 May 2005; pp. 1–4.

36. Van Dalen, R.; Rochefort, C. Electrical characterisation of vertical vapor phase doped (VPD) RESURF MOSFETs. In Proceedings of the 16th International Symposium on Power Semiconductor Devices & ICs, Kitakyushu, Japan, 24–27 May 2004; pp. 451–454.
37. Nitta, T.; Minato, T.; Yano, M.; Uenisi, A.; Harada, M.; Hine, S. Experimental results and simulation analysis of 250V super trench power MOSFET (STM). In Proceedings of the 12th International Symposium on Power Semiconductor Devices & ICs, Toulouse, France, 22–25 May 2000; pp. 77–80.
38. Kurosaki, T.; Shishido, H.; Kitada, M.; Oshima, K.; Kunori, S.; Sugai, A. 200V multi RESURF trench MOSFET (MR-TMOS). In Proceedings of the 15th International Symposium on Power Semiconductor Devices & ICs, Cambridge, UK, 14–17 April 2003; pp. 211–214.
39. Chen, X.B.; Mawby, P.A.; Board, K.; Salamab, C.A.T. Theory of a novel voltage-sustaining layer for power devices. *Microelectron. J.* **1998**, *29*, 1005–1011. [CrossRef]
40. Chen, Y.; Liang, Y.C.; Samudra, G.S. Theoretical analyses of oxide-bypassed superjunction power metal oxide semiconductor field effect transistor devices. *Jpn. J. Appl. Phys.* **2005**, *44(2R)*, 847. [CrossRef]

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Improved DRUS 4H-SiC MESFET with High Power Added Efficiency

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Abstract: A 4H-SiC metal semiconductor field effect transistor (MESFET) with layered doping and undoped space regions (LDUS-MESFET) is proposed and simulated by ADS and ISE-TCAD software in this paper. The structure (LDUS-MESFET) introduced layered doping under the lower gate of the channel, while optimizing the thickness of the undoped region. Compared with the double-recessed 4H-SiC MESFET with partly undoped space region (DRUS-MESFET), the power added efficiency of the LDUS-MESFET is increased by 85.8%, and the saturation current is increased by 27.4%. Although the breakdown voltage of the device has decreased, the decrease is within an acceptable range. Meanwhile, the LDUS-MESFET has a smaller gate-source capacitance and a large transconductance. Therefore, the LDUS-MESFET can better balance DC and AC characteristics and improve power added efficiency (PAE).

Keywords: 4H-SiC MESFET; simulation; power added efficiency (PAE)

1. Introduction

As a third-generation semiconductor, silicon carbide (SiC) has significant advantages in materials and devices, with high critical electrical field, high thermal conductivity, and high electron saturation velocity [1–3]. SiC based metal-semiconductor field-effect transistors (MESFETs) have become the key components for high-power, high-efficiency and high-frequency microwave applications because of their excellent properties. They offer wider bandwidth operation and lower system size than Si and GaAs based on MESFET technologies [4–7]. Based on those excellent performance, 4H-SiC MESFETs have broad application prospects in aerospace, satellite communications, and active phased array radars. Previously, the main research on SiC-MESFET was to balance the DC and AC characteristics and improve the output power density. With the idea of energy saving and emission reduction, high efficiency and low energy consumption have become the direction of device design. Thus, some improved structures have been reported for improving the power added efficiency. Such as a novel 4H-SiC MESFET with multi-recessed p-buffer layer for high energy-efficiency applications [8], an improved UU-MESFET with high power added efficiency [9], multi-recessed 4H–SiC metal semiconductor field effect transistor (MRD-MESFET) with high power added efficiency [10], an improved 4H-SiC MESFET with a partially low doped channel [11]. However, the trade-off between PAE and DC AC parameters is still a troublesome problem.

The DRUS-MESFET [12] is proposed to increase the breakdown voltage and improve the output power density of the device based on the double-recessed MESFET (DR-MESFET) [13]. But the saturation current and PAE of the device is low. Considering the saturation current and the power added efficiency, an improved double-recessed 4H-SiC MESFET with partly undoped space region (LDUS-MESFET) is proposed and simulated. The new structure introduced layered doping under the

lower gate and optimized the thickness of the undoped region. Using software ISE-TCAD and ADS to simulate the LDUS-MESFET, the DC and AC parameter values and power added efficiency of the device are obtained. By comparing with the DRUS-MESFET, it can be seen that the LDUS-MESFET is more in line with "green high efficiency, energy saving and emission reduction" thoughts.

2. Device Structure and Simulation Method and Fabrication Feasibility

2.1. Device Structure

Schematic cross-section of the DRUS-MESFET and the LDUS-MESFET are shown in Figure 1a,b, respectively. They both have a semi-insulating substrate, a p-type buffer layer, an n-type channel layer, and two highly doped n-type cap layers. The semi-insulating substrate is modeled as a compensation-doped (vanadium) semiconductor with a high concentration of deep level impurities [13]. Among them, the role of the p buffer layer is to reduce the influence of substrate defects on the active layer and improve noise performance and device gain [14]. Both of these structures have upper and lower gates, which control a thinner and a thicker part of the channel, respectively. The difference between the two structures is that the LDUS-MESFET has a layered doping under the lower gate, wherein the upper layer region has a doping thickness of H_1 = 0.05 μm and a concentration of 6×10^{17} cm^{-3} (to have a meaningful comparison, the lower layer region doping concentration of the LDUS-MESFET based on the DRUS-MESFET is also set at 3×10^{17} cm^{-3}), and the thickness of the undoped space region (US) is optimized for high efficiency. The optimization result is H_2 = 0.05 μm. The other parameters of the two structures are shown in Table 1.

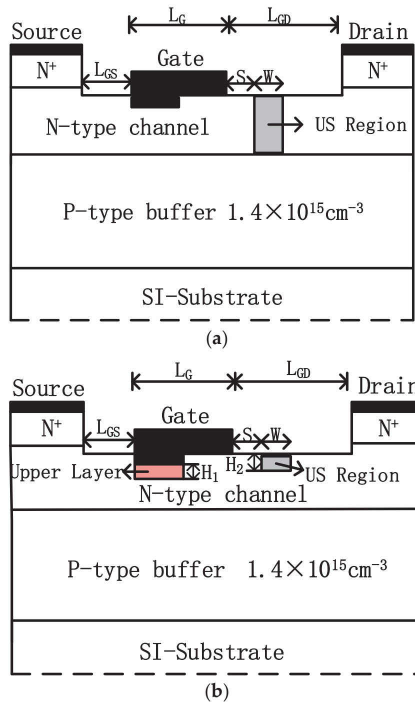

Figure 1. Schematic cross sections of the (**a**) double-recessed 4H-SiC MESFET with partly undoped space region (DRUS-MESFET), (**b**) 4H-SiC metal semiconductor field effect transistor with layered doping and undoped space regions (LDUS-MESFET).

Table 1. Common parameters of the two structures

Parameters	Values
P-Buffer Concentration	1.4×10^{15} cm^{-3}
N-Channel Concentration	3×10^{17} cm^{-3}
N-Cap layers Concentration	2×10^{19} cm^{-3}
Upper layer Concentration	6×10^{17} cm^{-3}
N-Cap layers Thickness	0.2 μm
N-Channel Thickness	0.25 μm
P-Buffer Thickness	0.5 μm
Recess gate Thickness	0.05 μm
Recess gate Width	0.35 μm
W	0.3 μm
S	0.2 μm
L_{gs}	0.5 μm
L_{gd}	1.0 μm
L_s	0.5 μm
L_d	0.5 μm
L_g	0.7 μm
H_1	0.05 μm
H_2	0.05 μm

2.2. Simulation Method

Two dimensional numerical device characteristics are realized with ISE-TCAD. The simulator is calibrated with experimental data in the micrometer regime [15], and the agreement between experimental data and simulation results is obtained as shown in Figure 2. In order to accurately simulate the electrical characteristics of the 4H-SiC MESFET device structure, the main physical models used are mobility (Enormal, Doping Dep, High Field saturation (GradQuasiFermi)), recombination (Auger, SRH (DopingDep)), incomplete ionization, effective intrinsic density (Band Gap Narrowing (OldSlotboom)). The DC and AC parameters of the device are obtained by ISE-TCAD simulation, and these parameters are input into the ADS software to simulate the power added efficiency of the device. In the ADS simulation, the model used is EE-FET3, an empirical analytical nonlinear model used to fit the electrical properties of MESFETs. And the working bias conditions were set as follows: V_{gs} was −3.5 V, V_{ds} was 28 V, RF was 1.2 GHz and input power Pavs was 24 dBm.

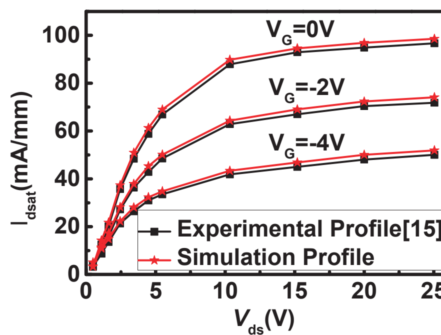

Figure 2. Comparison of experimental data and simulation data on output current.

2.3. Fabrication Feasibility

The LDUS-MESFET can be fabricated using the same procedures as reported in [16]. It is worth noting that the doping concentration of 6×10^{17} cm^{-3} region under the lower gate can be formed by ion implantation and activation process. Through high temperature and multi-energy ion implantation with phosphorous, and activation of the implanted ions can be achieved by inductively heating at a

desired time and temperature in an Ar atmosphere [17]. The formation of undoped space region is formed by high energy ion implantation of deep level vanadium and high temperature annealing (the resistivity of the US region is 2×10^6–7.6×10^6 Ω·cm).

The recessed gate area of the transistors can be fabricated as reported in [16] as follows: First, a thermal oxide layer is deposited on top of the channel, the thermal oxide layer is etched through the position of the recessed area and continues to be etched into the interior of the channel to form a recessed area having a thickness of 0.05 µm. Second, Nickel with a work function of 5.1 eV was deposited on the recessed area to form a Schottky contact.

3. Results and Discussion

3.1. The Effect of the Doping Concentration (N_d) and Thickness(H_1) of the Upper Layer Region on the Device Parameters

The effect of the thickness and doping concentration of the upper layer region on DC and AC parameters are shown in Figure 3. It can be seen from the Figure 3a that as the doping concentration increases, the absolute value of the threshold voltage increases significantly. When H_1 is less than 0.05 µm, the absolute value of Threshold voltage (V_t) is gradually decreasing with the increase of H_1. Because there is a longitudinal concentration gradient in the channel. The concentration gradient produces a longitudinal electric field that weakens the pinch-off voltage, which results in a decrease in the absolute value of the threshold voltage. When H_1 is greater than 0.05 µm, the absolute value of V_t is increasing with the increase of H_1. Because as the doping thickness increases, the number of electrons in the channel increases, causing the threshold voltage to drift negatively. At H_1 = 0.05 µm, the absolute value of the threshold voltage has a minimum value. In Figure 3b. As the doping concentration increases, Gate-source capacitance (C_{gs}) also increases. At the same time, C_{gs} shows an upward trend with the increase of H_1. In Figure 3c,d, as the doping concentration increases, the saturation current (I_{dsat}) increases significantly, and the breakdown voltage decreases. When H_1 rises from 0 to 0.05 µm, the saturation current increases rapidly. When H_1 increases from 0.05 µm, the rising trend of saturation current becomes slow.

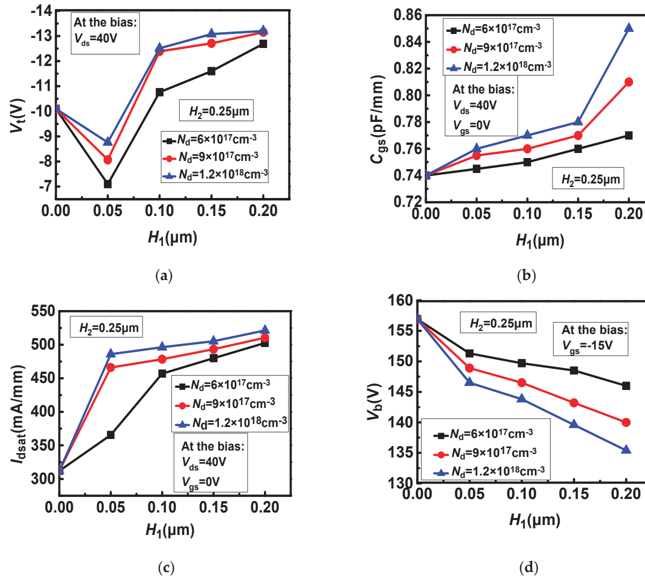

Figure 3. The effect of H_1 and N_d on the device parameters: (**a**) V_t–N_d and H_1, (**b**) C_{gs}–N_d and H_1, (**c**) I_{dsat}–N_d and H_1, (**d**) V_b–N_d and H_1.

3.2. The Effect of the Doping Concentration (N_d) and Thickness of the Upper Layer Region (H_1) on PAE

The influences of the doping concentration and thickness of upper layer region on PAE is shown in Figure 4. It can be seen from the figure that as the doping concentration of the upper layer region increases, the PAE significantly decreases. When the thickness of the upper layer region is less than 0.05 µm, the PAE increases with the increase of H_1. When H_1 is greater than 0.05 µm, the PAE decreases with the increase of H_1. When the thickness of the upper layer region is 0.05 µm, the PAE reaches a maximum value.

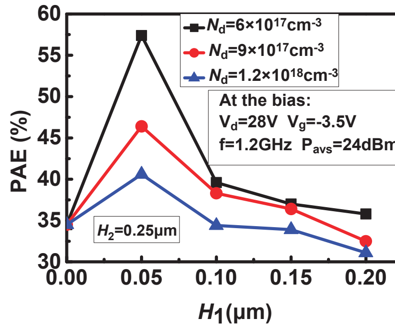

Figure 4. The effects of N_d and H_1 on the PAE.

3.3. Optimization of the Undoped Region Thickness (H_2)

Based on the thickness and doping concentration of the upper layer region determined above, the thickness of the undoped region is optimized to obtain better power added efficiency and DC AC parameters. The effect of the thickness of the undoped region on the DC, AC parameters and PAE of the device is shown in Figure 5. In Figure 5a. We can see that as H_2 increases, the absolute value of the threshold voltage gradually decreases. At the same time, when H_2 is less than 0.05 µm, the breakdown voltage increases as H_2 increases, when H_2 is greater than 0.05 µm, the breakdown voltage shows a basically constant trend with the increase of H_2. In Figure 5b. As H_2 increases, the transconductance (g_m) shows a decreasing trend. When H_2 is less than 0.15 µm, the transconductance decline trend is more gradual. When H_2 is greater than 0.15 µm, the transconductance decreases sharply as H_2 increases. When H_2 increases, C_{gs} shows an upward trend. In Figure 5c. As H_2 increases, the saturation current shows a linear decline. When H_2 is less than 0.05 µm, the PAE increases as H_2 increases, and when H_2 is greater than 0.05 µm, the PAE decreases as H_2 increases. The PAE reaches the maximum at H_2 = 0.05 µm.

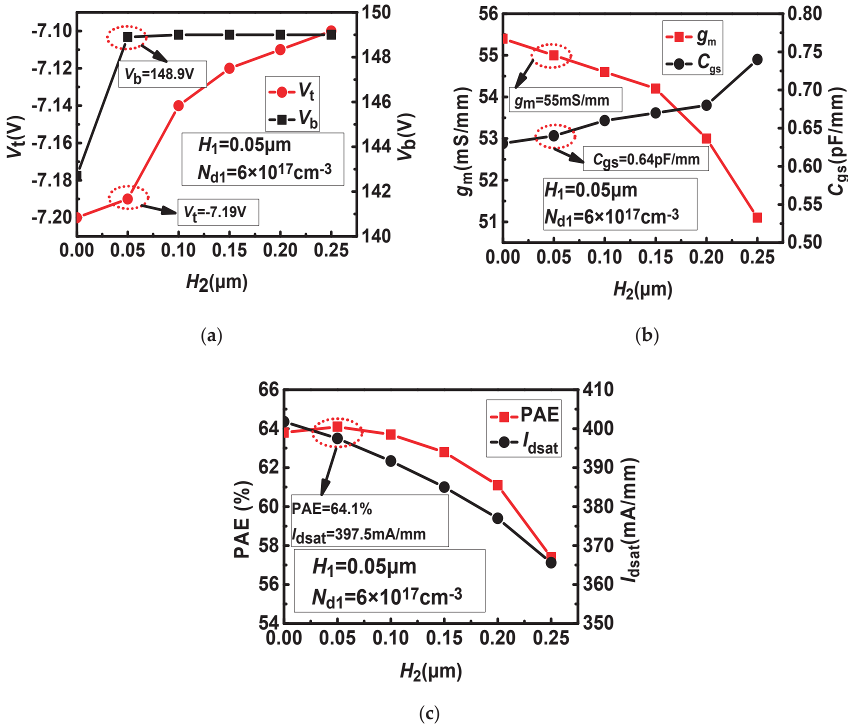

Figure 5. The effect of H_2 on the device parameters: (**a**) V_t, V_b–H_2, (**b**) g_m, C_{gs}–H_2, (**c**) PAE, I_{dsat}–H_2.

3.4. Mechanism to Improve Device Parameters

Through the analysis of Figures 4 and 5, it can be acquired that when H_1 = 0.05 μm, H_2 = 0.05 μm, $N_d = 6 \times 10^{17}$ cm^{-3}, the power added efficiency reaches the maximum value of 64.1%. It can be seen from Equation (1) that PAE is an efficiency that considers DC and AC parameters [18]. The parameters V_t, g_m and C_{gs} simulated above have an impact on power added efficiency. The larger the absolute value of the threshold voltage of the device, the more difficult it is that the gate voltage is pinched off, which results in higher DC power consumption and smaller PAE. As the maximum transconductance of the device increases, the power-added efficiency of the device tends to decrease linearly. This is because when the device transconductance increases, it means that the ability of the gate to control the current is increased, and the channel resistance is increased, resulting in an increase in the DC power consumption of the device, and the power added efficiency of the device is reduced. The larger the C_{gs}, the greater the energy lost when charging and discharging the capacitor, resulting in a larger P_{dc}, which in turn reduces the PAE. The LDUS-MESFET has a smaller threshold voltage and capacitance than the DRUS-MESFET. Although the transconductance is improved compared with the DRUS-MESFET, it can be seen from the simulation that the threshold voltage V_t and C_{gs} have a greater influence on the PAE than the transconductance. So the PAE of the LDUS-MESFET is 85.8% higher than the DRUS-MESFET.

$$\text{PAE} = \frac{P_{out} - P_{in}}{P_{dc}} \tag{1}$$

where P_{out} is output power, P_{in} is input power and P_{dc} is DC power.

It can be seen from Table 2 that the saturation current is increased by 27.4% compared with the DRUS-MESFET. It can be obtained from Equation (2) that the saturation current is proportional to the amount of charge in the channel and the effective thickness of the channel [14]. Heavy doping

under the lower gate and reducing the thickness of the undoped region in the channel increase the saturation current. The breakdown occurs at the edge of the gate near the drain side, and the thickness of the undoped region has a certain influence on the breakdown voltage. So the LDUS-MESFET has a lower breakdown voltage than the DRUS-MESFET. But the range of reduction is acceptable. The transconductance reflects the gate voltage's ability to control the channel current of the device. The partly high doping under the lower gate makes the transconductance of the LDUS-MESFET larger than the DRUS-MESFET. The threshold voltage refers to the gate-source voltage when the channel is pinched off. Since the LDUS-MESFET has a longitudinal concentration gradient in the channel, the concentration gradient produces a longitudinal electric field that weakens the pinch-off voltage, which results in a decrease in the absolute value of the threshold voltage. So the LDUS-MESFET has a smaller threshold voltage than the DRUS-MESFET. Compared with the DRUS-MESFET, the LDUS-MESFET has a reduced thickness of the undoped region near the drain side of the gate. So that the drain side depletion layer can be expanded and the source side expansion is reduced, this makes C_{gs} decrease.

$$I_{dsat} = Q(x)v(x) = Zb(x)qn(x)v(x) \quad (2)$$

where Z is the channel width, $b(x)$ is the effective depth of the channel, q is the electron charge, $n(x)$ is the electron density, and $v(x)$ is the electron velocity.

Table 2. Comparison of performance parameters of the two structures.

Parameters	DRUS-MESFET	LDUS-MESFET
I_{dsat} (mA/mm)	312	397.5
V_b (V)	156.9	148.9
g_m (mS/mm)	43.8	55
V_t (V)	−10.1	−7.19
C_{gs} (pF/mm)	0.74	0.64
PAE (%)	34.5	64.1

4. Conclusions

An improved DRUS 4H-SiC MESFET with layered doping under lower gate is proposed and simulated in this paper to increase the PAE of the device. On the basis of the DRUS-MESFET, in order to maximize the power added efficiency, an upper layer region of 0.05 µm thick is introduced under the lower gate, and the thickness of the partly undoped region of the DRUS-MESFET was optimized. The structure achieves a PAE of 64.1%, which is 85.8% larger than the DRUS-MESFET. In addition, the LDUS-MESFET has a certain improve in saturation current, threshold voltage, transconductance, and gate-source capacitance. Although the breakdown voltage is reduced, the drop value is within the acceptable range. Overall, the LDUS-MESFET has wider application in the radio frequency direction.

Author Contributions: Data curation, X.W.; formal analysis, T.Z.; project administration, H.J.; writing—original draft, Y.L.; writing—review and editing, T.L., Y.T., S.Z., and Y.Y. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Hjelmgren, H.; Allerstam, F.; Andersson, K. Transient simulation of microwave SiC MESFET with improved trap models. *IEEE Trans. Electron. Devices* **2012**, *57*, 729–732. [CrossRef]
2. Zhang, Y.R.; Zhang, B.; Li, Z.J. Two-dimensional analysis of the interface state effect on current gain for a 4H-SiC bipolar junction transistor. *Chin. Phys. B* **2010**, *19*. [CrossRef]

3. Chen, F.-P.; Zhang, Y.-M.; Zhang, Y.-M.; Lu, H.-L.; Song, Q.-W. Simulation research on offset field-plate used as edge termination in 4H-SiC merged PiN-Schottky diodes. *Chin. Phys. B* **2010**, *19*. [CrossRef]
4. Zhang, X.J.; Yang, Y.T.; Duan, B.X.; Chen, B.; Chai, C.-C.; Song, K. New 4H silicon carbide metal semiconductor field-effect transistor with a buffer layer between the gate and the channel layer. *Chin. Phys. B* **2012**, *21*. [CrossRef]
5. Zhu, C.L.; Zhao, P.; Xia, J.H. Characterization of SiC MESFETs with narrow channel layer. *Microelectron. Eng.* **2006**, *83*, 72–74.
6. Raynaud, C.; Tournier, D.; Morel, H.; Planson, D. Comparison of high voltage and high temperature performances of wide bandgap semiconductors for vertical power devices. *Diam. Relat. Mater.* **2010**, *19*, 1–6. [CrossRef]
7. Dimitrijev, S.; Han, J.; Moghadam, H.A.; Aminbeidokhti, A. Power-switching applications beyond silicon: Status and future prospects of SiC and GaN devices. *MRS Bull.* **2015**, *40*, 399–405. [CrossRef]
8. Jia, H.J.; Wu, Q.Y.; Hu, M. A novel 4H-SiC MESFET with multi-recessed p-buffer layer for high energy-efficiency applications. *Superlattices Microstruct.* **2017**, *112*, 97–104. [CrossRef]
9. Jia, H.; Wu, Q.; Hu, M.; Yang, Z.; Ma, P.; Luo, Y.; Yang, Y. An Improved UU-MESFET with High Power Added Efficiency. *Micromachines* **2018**, *9*, 573. [CrossRef] [PubMed]
10. Zhu, S.; Jia, H.; Wang, X.; Liang, Y.; Tong, Y.; Li, T.; Yang, Y. Improved MRD 4H-SiC MESFET with High Power Added Efficiency. *Micromachines* **2019**, *10*, 479. [CrossRef] [PubMed]
11. Jia, H.; Tong, Y.; Li, T.; Zhu, S.; Liang, Y.; Wang, X.; Zeng, T.; Ynag, Y. An Improved 4H-SiC MESFET with a Partially Low Doped Channel. *Micromachines* **2019**, *10*, 555. [CrossRef] [PubMed]
12. Orouji, A.A.; Aminbeidokhti, A. A novel double-recessed 4H-SiC MESFET with partly undoped space region. *Superlattices Microstruct.* **2011**, *50*, 680–690. [CrossRef]
13. Zhu, C.L.; Rusli; Tin, C.C.; Zhang, G.H.; Yoon, S.F.; Ahn, J. Improved performance of SiC MESFETs using double-recessed structure. *Microelectron. Eng.* **2006**, *83*, 92–95. [CrossRef]
14. Sze, S.M.; Ng, K.K. *Physics of Semiconductor Devices*, 3rd ed.; John Wiley & Sons: Hoboken, NJ, USA, 2007; pp. 303–304, 386–398.
15. Weitzel, C.E.; Palmour, J.W.; Carter, C.H. 4H-SiC MESFET with 2.8 W/mm power density at 1.8 GHz. *IEEE Electron. Device Lett.* **1994**, *15*, 406–408. [CrossRef]
16. Andersson, K.; Sudow, M.; Nilsson, P.A. Fabrication and characterization of field-plated buried-gate SiC MESFETs. *IEEE Electron. Device Lett.* **2006**, *27*, 573–575. [CrossRef]
17. Razavi, S.M.; Zahiri, S.H.; Hosseini, S.E. A novel 4H–SiC MESFET with recessed gate and channel. *Superlattices Microstruct.* **2013**, *60*, 516–523. [CrossRef]
18. Lee, T.H. *The Design of CMOS Radio-Frequency Integrated Circuits*; Cambridge University Press: Cambridge, UK, 1998.

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Investigation of 1200 V SiC MOSFETs' Surge Reliability

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Abstract: In this work, the surge reliability of 1200 V SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) from various manufactures has been investigated in the reverse conduction mode. The surge current tests have been carried out in the channel conduction and non-conduction modes. The experimental results show that the maximum surge currents that the devices can withstand are similar for both cases. It is found that short circuits occurred between the gate and the source in the failed devices. The characteristics of the body diode have also changed after the tests. By measuring the device characteristics after each surge current is applied, it can be concluded that the damages to the gate oxide layer and the body diode occurred only when the maximum surge current is applied. By decapping the failed devices and observing the cross section of the damaged cell, it is found that high temperature caused by excessive current flow through the devices during the surge tests is the main reason for the device failure. Finally, the TCAD simulation of the devices has been carried out to bring insight into the operation of the devices during the surge events.

Keywords: 1200 V SiC MOSFET; body diode; surge reliability; silvaco simulation

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1. Introduction

For decades, silicon material has always been the main semiconductor material used to power electronic devices. However, the performance of silicon devices has approached its theoretical limit determined by the material characteristics. While various applications demand ever-increasing performance from power devices, silicon can no longer meet the requirements of high power, high frequency, high speed and high temperature. Therefore, more attention has been paid to power electronic devices based on wide bandgap semiconductor materials [1,2].

Compared with Silicon, wide bandgap semiconductors SiC, GaN and diamond have the advantages of wide bandgap, high thermal conductivity and high saturation speed. Due to their excellent performance, wide bandgap semiconductors are more suitable for high voltage, high temperature and high switching frequency applications [3,4]. While power devices based on diamond are still in the early research stage [5], some GaN and SiC products are already available in the commercial market. At present, commercial GaN devices are mainly high electron mobility transistors (HEMTs) rated 600 V and below [6,7]. On the other hand, SiC devices are more widely available in voltage ranges between 600 and 3300 V [8,9].

Although wide bandgap semiconductor materials have a lot of advantages, their high cost and poor reliability restrict their large scale commercialization. Current surges are common in the power electronics circuits. For example, the devices have to withstand several folds of the rated current during the startup process of a power factor correction (PFC) circuit or an inverter-fed motor drive. The maximum surge current that a device can withstand is usually referred to as its surge current capability. Excessive surge current will cause irreversible damage to devices,

and continuous surge current will also have a negative impact on the device performance. Therefore, surge capability is an important parameter of devices requiring detailed investigation. Among the three wide bandgap semiconductors mentioned above, SiC devices are the most mature. At this point, metal-oxide-semiconductor field-effect transistor (MOSFET) is the SiC commercial product attracts the most attention. Therefore, in this work, surge capability of SiC MOSFETs has been studied.

Until now there have been a number of surge reliability studies of Si diodes [10] and insulated-gate bipolar transistors (IGBTs) [11–13]. Considerable research work about the surge reliability of SiC devices has also been carried out in recent years, but the results mainly focused on the reliability of SiC Schottky diodes [14–17]. On the SiC MOSFET, most reliability work has been carried on under short-circuit conditions. Some researchers have investigated the failure of SiC MOSFETs under short circuit and surge current conditions with a thermal model [18]. Some researchers have tested the maximum surge currents of 1200 V SiC MOSFETs' body diodes under various conditions [19,20]. The test conditions were varied by changing temperatures, pulse width of surge currents, gate voltages and so on. Some have also compared the surge reliability of SiC MOSFET's body diodes to those of other Si devices' body diodes [21–24]. However, in these works only measurement results were presented. Analysis on the internal causes of the device failure has not been presented.

In this paper, the surge reliability of SiC MOSFETs operating in the reverse conduction mode has been studied. Firstly, several 1.2 kV SiC MOSFETs from several major manufactures has been tested in the channel conduction and non-conduction modes to get the maximum surge currents that the devices could withstand. The performance changes of devices after each surge test were checked to help to understand the process of the failure. In order to find out the failure mechanism, anatomy work has been done to two representative failed devices to identify the damages inside the devices. The results have been analyzed in depth. At last, TCAD simulation has been employed to obtain some insight into the operation of the devices during the surge events.

2. Materials and Methods

The SiC MOSFETs studied in this paper were vertical N- channel power MOSFETs with a planar gate structure. Shown in Figure 1 is the cell structure of the SiC MOSFET C2M0080120D from Cree Company (Durham, NC, USA). The drain electrode is located at the bottom of the device, in contact with the N+ substrate region. The source electrode and the gate electrode are located on the top of the device, separated by the interlayer insulator. The channel is located in the P− well region, between the N+ source region and the N− drift region. The P+/P− well regions and N− drift region form a PN junction, which is the body diode. The dimension of the regions inside the device has been obtained by SEM. The doping concentrations of the regions have been derived from the device characteristics and the dimension of the regions. The structure parameters of MOSFET are shown in Table 1.

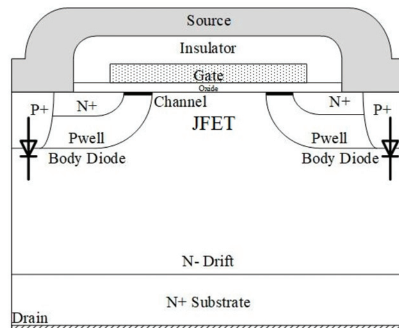


Figure 1. Cell structure of SiC metal-oxide-semiconductor field-effect transistor (MOSFET).

Table 1. Structure parameters of the metal-oxide-semiconductor field-effect transistor (MOSFET) shown in Figure 1.

Region	Numerical Value	Unit
Doping concentration in P−well region	Surface 7×10^{16}, internal peak 1×10^{18}	cm^{-3}
Depth of P−well region	0.5	µm
Doping concentration in N− drift region	8.85×10^{15}	cm^{-3}
Depth of N- drift region	10	µm
Doping concentration in N++ substrate region	1×10^{19}	cm^{-3}
Depth of N++ substrate region	170	µm
Doping concentration in N+ region	3×10^{18}	cm^{-3}
Depth of N+ region	0.2	µm
Doping concentration in P+ region	1×10^{19}	cm^{-3}
Length of channel	0.96	µm
Thickness of gate oxide layer	0.05	µm
Length of junction field-effect transistor (JFET) region	2.4	µm

2.1. The Reverse Conduction Characteristics of SiC Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

Until now, there have been a lot of studies on SiC MOSFETs' body diodes. Their static characteristics are similar to those of the ordinary diodes [25–28].

In Figure 2a, the transfer characteristics of the SiC MOSFET C2M0160120D manufactured by Cree Company is measured to obtain the threshold voltage and plotted. It can be seen that the MOSFET has a threshold voltage of around 2.6 V. By changing the gate voltages, the reverse I-V curves of the device are tested and the results are shown in Figure 2b.

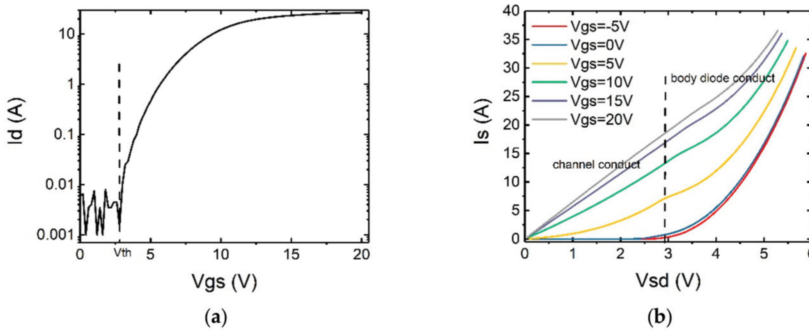


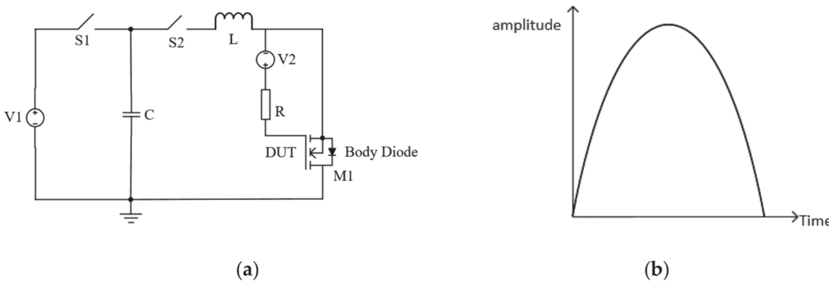
Figure 2. (**a**) Transfer characteristic with V_{ds} = 10 V and (**b**) reverse I-V curves of C2M0160120D from Cree.

In the reverse conduction mode, there are two possible parallel current paths, namely, the body diode and the MOS channel. The body diode only turns on when the voltage across the P+ or P−well/N− drift junction exceeds its turn-on voltage (approx. 2.7 V under room temperature), which explains the I-V curve with $V_{gs} = -5$ V in Figure 2b. On the other hand, when reverse-biased, the MOS channel opens when V_{gd} exceeds V_{th} and current flows from source to drain. This explains the I-V curves with V_{gs} = 5 V to 20 V where the reverse current of the device increases starting from V_{sd} = 0 V. When V_{gs} = 0 V, the MOS channel starts reverse conducting at V_{sd} = 2.6 V and the body diode starts conducting at V_{sd} = 2.7 V, which gives an I-V curve very similar to that of $V_{gs} = -5$ V [29]. It is also interesting to note that, for V_{gs} = 5 V to 20 V, the I-V curves start to bend upwards when V_{sd} exceeds 3 V. This is because of the addition of the body current to the existing MOS current. Once turned-on, the current in the body diode increases exponentially with voltage. As a result, the body diode becomes the main conducting path with further increase of the bias voltage.

2.2. Setup of the Surge Current Tests

The simplified schematic of the surge current reliability test circuit is shown in Figure 3. To test the surge reliability of the device-under-test (DUT), this circuit is operated in the following steps. Firstly, S_1 is closed and S_2 remains open. The voltage source V_1 charges the capacitor C. Then, S_1 is open and S_2 is closed. The charge stored in capacitor C is discharged through the DUT ($M1$) and the inductor L. A large instantaneous current flows through the DUT. The LC oscillation circuit is used to generate a sinusoidal surge current. The period of the current was determined by the inductance L and capacitance C, which could be expressed as:

$$T = 2\pi\sqrt{LC} \tag{1}$$



(**a**) (**b**)

Figure 3. (**a**) Simplified schematic of the surge current test circuit, (**b**) the waveform of the surge current.

In the tests, the sinusoidal current period is set as 20 ms [30]. The values of C and L are chosen as: C = 2 mF, L = 5 mH to satisfy the equation. The magnitude of the sinusoidal current is determined by the following formula:

$$\frac{1}{2}CU^2 = \frac{1}{2}LI^2 \tag{2}$$

in which U is the voltage of V_1 and I is the amplitude of the sinusoidal current flowing through the DUT. During the tests, the amplitude of the surge current is increased gradually by adjusting voltage source V_1.

In this experiment, 1200 V SiC MOSFETs from several major manufacturers were selected for testing. They were C2M0080120D and C2M0160120D from Cree, SCT3160KLGC11 from ROHM (Kyoto, Japan), SCT10N120 from STM (Geneva, Switzerland) and LSIC1MO120E0160 from Lifflefuse (Chicago, IL, USA). The major parameters for the tested devices have been listed in Table 2.

Table 2. Device parameters from the datasheets.

	V_{ds} (V)	$R_{ds(on)}$ (mΩ)	I_{ds} (A)/ Body Diode I_F (A)	V_{gs} (V)	V_{th} (V)
SCT10N120	1200	500	12/12	−10/25	5.5
C2M0080120D	1200	80	36/36	−5/20	2.8
C2M0160120D	1200	160	19/19	−5/20	3
LSIC1MO120E0160	1200	160	22/22	−5/20	3.6
SCT3160KLGC11	1200	160	17/17	−4/22	5

All the devices mentioned above were tested under the reverse conduction state. A half-wave sinusoidal current pulse with a pulse width of 10 ms was used. The amplitude of the current was increased gradually until the device failed. After each test, the device was cooled down to the room temperature before the next test started, so as to prevent the heat generated in the device from affecting the results of the subsequent tests. The surge failure of the device could be determined by observing the distortion of the voltage V_{ds}.

The maximum surge current capability of each device was obtained from the tests. The tests have been carried out in the channel conduction and non-conduction modes. Therefore, two gate-source voltage biases, 10 V and −3 V, were applied respectively. For every device type and each test condition, three samples were tested.

After the device failed, the static characteristics were measured and compared to the characteristics obtained before the surge currents were applied. These measurements include the transfer characteristic, the reverse I-V characteristics and the resistance between electrodes.

3. Results

The surge test results of devices were shown in Figures 4 and 5.

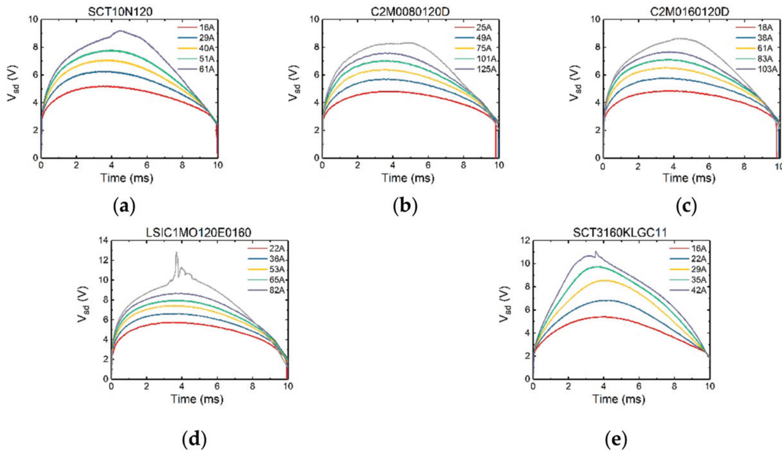


Figure 4. The variation of voltage V_{sd} of (**a**) SCT10N20, (**b**) C2M0080120D, (**c**) C2M0160120D, (**d**) LSIC1MO120E0160, (**e**) SCT3160KLGC11 SiC MOSFETs when varying surge current amplitude with V_{gs} = −3 V.

In Figure 4, V_{gs} is set to −3 V. It can be seen that initially there is a sudden rise in the voltage curve. Since with V_{gs} = −3 V, the current largely flows through the body diode region. The magnitude of the sudden rise corresponds to the on-set voltage of the body diode. Then the voltage increases accordingly with the current. However, it can be seen that the peak of the voltage does not occur when the current reaches its peak value (which is at 5 ms for a 20 ms-period sinusoidal current waveform). It is because in the bipolar mode, the device has a negative temperature coefficient. During each test pulse, as the device is continuously heated up, the voltage peak appears somewhat earlier than the current peak.

In Figure 5, V_{gs} is set to 10 V. Initially there is no sudden rise of the voltage, since the channel is turned on and it carries all the current. When the voltage V_{sd} exceeds the on-set voltage of the body diode (~2.7 V), the slope of the voltage curve changes as the body diode starts to conduct. Comparing Figures 4 and 5, the maximum surge currents of the SiC MOSFETs' in channel conduction and non-conduction modes are very close to each other. This is due to the fact that at V_{sd} of 6 V and higher (with a likely high junction temperature), the body diode is operating in a bipolar mode with heavy conductivity modulation, making it the dominant current path against the MOS channel. Therefore, whether the channel is conducting or not does not significantly impact the surge current capability of the device. It is also found that the device failure occurs at the time of 3.5 ms in both cases.

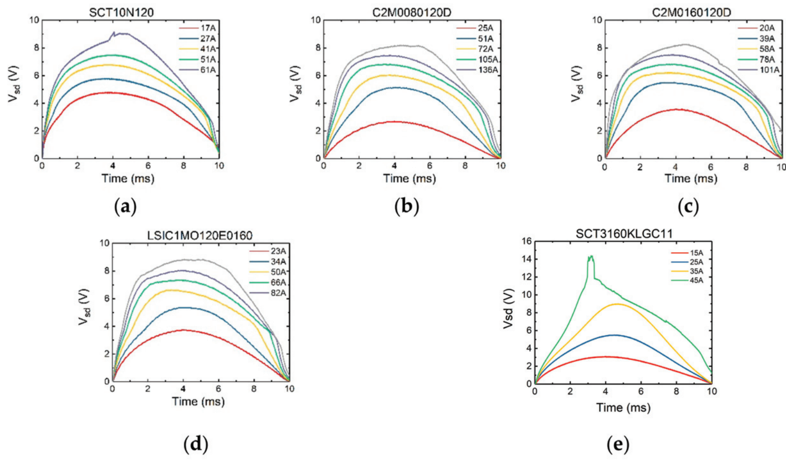


Figure 5. The variation of voltage V_{sd} of (**a**) SCT10N20, (**b**) C2M0080120D, (**c**) C2M0160120D, (**d**) LSIC1MO120E0160, (**e**) SCT3160KLGC11 SiC MOSFETs when varying surge current amplitude with V_{gs} = 10 V.

The maximum surge currents that the devices can withstand are listed in Table 3. It can be seen that in general the maximum surge current is about 5 times of rated current.

Table 3. Maximum surge current that a device can withstand.

	I_{ds} (A)/ Body Diode I_F (A)	$R_{ds(on)}$ (mΩ)	Maximum Surge Current (A)	Maximum Surge Current/Rated Current
SCT10N120	12/12	500	61	5
C2M0080120D	36/36	80	155	4.3
C2M0160120D	19/19	160	105	5.5
LSIC1MO120E0160	22/22	160	95	4.3
SCT3160KLGC11	17/17	160	42	2.5

4. Discussion

4.1. Analysis of Test Result

4.1.1. Comparison of Devices' Characteristics before and after the Surge Reliability Tests

In this section, the characteristics of the failed MOSFETs have been measured and summarized. According to their behaviors after the tests, the devices can be classified into two groups: The devices in the first group cannot block the reverse voltage anymore, while the devices in the other group still have the reverse voltage blocking capability. Therefore, the following work focuses on two devices representing these two cases respectively: SCT10N120 from STM and C2M0160120D from Cree.

The first failure phenomenon is the short circuit between the gate and the source. During the test, it was found that when the failure occurred, the gate-source voltage dropped to 0 V and a bias voltage could not be applied to the gate. It was preliminary judged that the short circuit occurred between the gate and the source. Therefore, the resistances between the electrodes of MOSFETs before and after the surge failure were tested and shown in Table 4. It can be seen that the resistances before the surge tests are very large and out of the measurement range of the digital multimeter. However, the resistances between the gate and the source of the damaged devices are less than 1 Ω, indicating that the gate is short circuited to the source. In addition, R_{ds} of the device SCT10N120 after the test is 14 kΩ, which means that damage has also occurred in regions between the drain and the source.

Table 4. Measured resistances between electrodes before and after surge tests.

Device	R_{gs} (Ω)	R_{ds} (Ω)
Before the tests	>100 M	>100 M
SCT10N120, after tests	0.4	14 k
C2M0160120D, after tests	0.08	>100 M

The second abnormal behavior is that the performance of the body diode has changed. In Figures 6 and 7, the forward I-V and reverse blocking characteristics of the failed devices were measured and compared against those before failure.

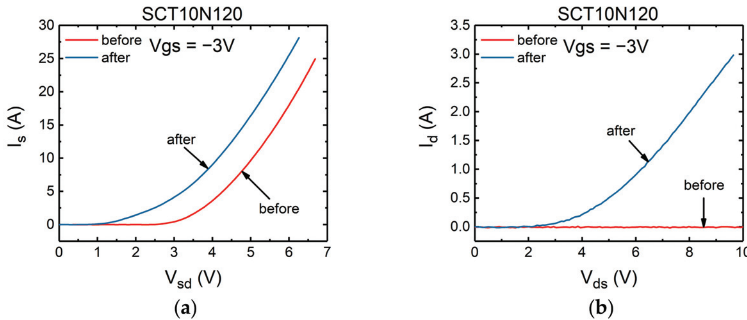


Figure 6. The characteristics of SiC MOSFET's body diode (SCT10N120) before and after the failure (**a**) forward conduction characteristics, (**b**) reverse blocking characteristics.

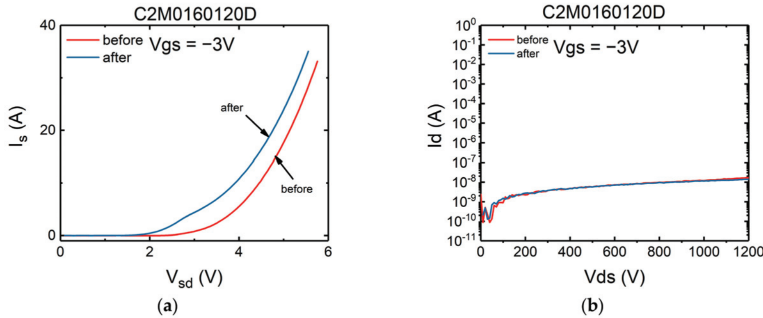


Figure 7. The characteristics of SiC MOSFET's body diode (C2M1060120D) before and after the failure (**a**) forward conduction characteristics, (**b**) reverse blocking characteristics.

As shown in Figure 6, for some devices represented by SCT10N120 (STM), the performance of the body diode has changed significantly after the tests, while the devices represented by C2M0160120D (Cree) was not damaged as badly as SCT10N120 (see Figure 7). For both devices, the forward voltage drops of the body diodes have decreased, but the voltages of Cree's device were reduced less. In terms of the reverse blocking capability, the difference is more significant. Device SCT10N120 has completely lost its reverse blocking capability. However, the Cree device C2M0160120D still exhibits excellent reverse blocking capability.

4.1.2. Static Characteristic Variation of the Tested Device

In the sections above, the results of the surge reliability tests and the behaviors of the failed devices have been presented and summarized. However, device failure did not necessarily occur at the test the maximum surge current was applied. The damage might have accumulated when the surge current

was increased gradually. To help to understand the process of the failure and find out the failure mechanisms of the devices, the characteristics of the devices have been measured after every surge current was applied.

The damage of SiC MOSFETs usually occurs in the gate oxide layer, so it is necessary to observe the change of the gate oxide layer's characteristics. Whether the gate oxide layer is damaged or not can be observed from the change of the transfer curves. Thus, the transfer characteristics have been measured with V_{ds} = 10 V. The sub-threshold swing is a performance index to measure the switching rate [31]. It is closely related to the interface trap density of gate oxide layer. It represents the variation of the gate voltage required for a ten-fold change in the drain current when the device is operating in the sub-threshold region. It is also called S factor. Smaller S factor corresponds to faster switching rate. It can be calculated from the following equation:

$$S = \frac{dV_{gs}}{dlogI_d} \tag{3}$$

The sub-threshold swing is related to the interface trap density D_{it}, as shown in the following equation:

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{qs}{\ln(10)kT} - 1\right) - \frac{C_b}{q^2} \tag{4}$$

Hence the change of the interface trap density can be derived from the change of sub-threshold swing. In turn the state of gate oxide layer can be deduced by observing the change of the sub-threshold swing characteristics. The results have been measured and shown in Figures 8 and 9. Also included are the forward conduction characteristics of the body diode in which V_{gs} is set to −3 V to keep the channel off.

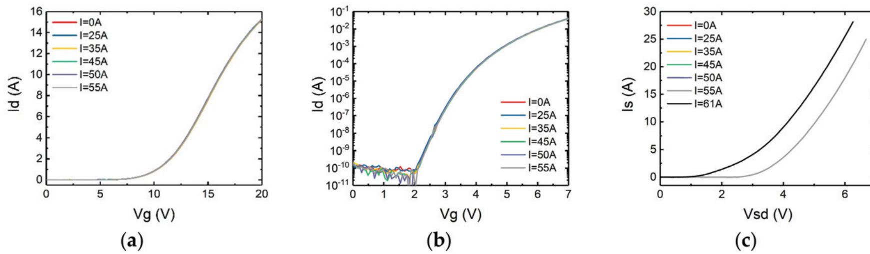


Figure 8. (**a**) Transfer characteristics, (**b**) sub-threshold swing characteristics, (**c**) forward conduction characteristics of the body diode of SCT10N120 after each surge test.

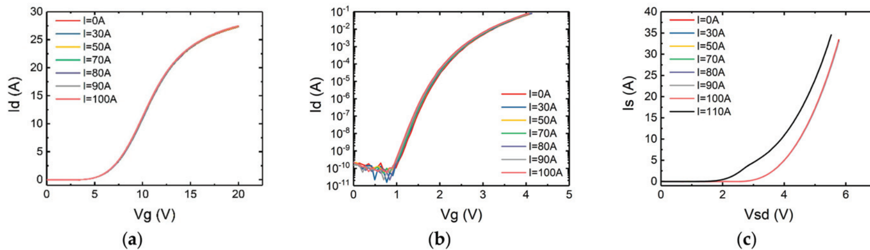


Figure 9. (**a**) Transfer characteristic, (**b**) sub-threshold swing characteristics, (**c**) forward conduction characteristics of the body diode of C2M0160120D after each surge test.

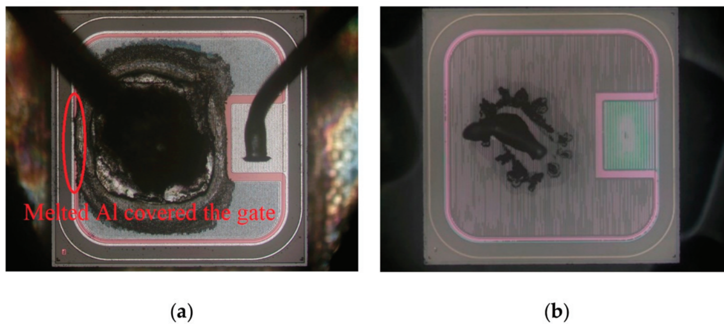
It can be seen from the figures that even applying a surge current very close to the maximum surge current the static characteristics of the devices remain nearly unchanged. Hence it can be concluded

that the damages to the gate oxide layer and the body diode occurred only at the time the maximum surge current was applied.

4.2. Analysis of Failure Mechanism

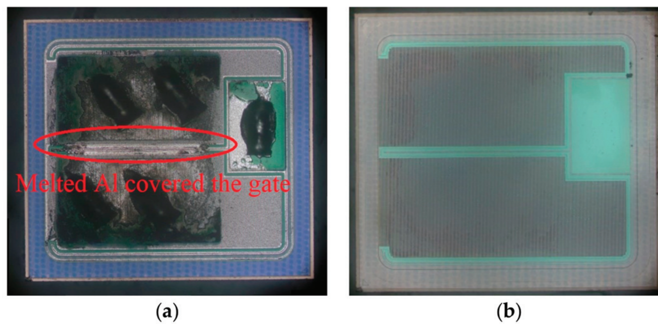
During a surge event, the junction temperatures inside the semiconductor devices can reach extremely high values, possibly several times the maximum rated temperature. It was reported that the main failure mechanism for standard silicon diode and transistor chips within module housings, is the melting of the anode-side metallization [32–34].

To investigate the failure mechanisms of these tested SiC MOSFET devices, anatomy work has been carried out. The following two devices were examined, namely, SCT10N120 (STM) and C2M0160120D (Cree). The anatomical results of the damaged devices are shown in Figures 10 and 11.



(**a**) (**b**)

Figure 10. The anatomy results of STM device SCT10N120 (**a**) decapping, (**b**) removing layers to the substrate layer.



(**a**) (**b**)

Figure 11. The anatomy results of Cree device C2M0160120D (**a**) decapping, (**b**) removing layers to the substrate layer.

Figure 10a is the image of the decapped STM device SCT10N120. The burn mark of the device is very obvious. Removing the layers to the substrate, there is still apparent damage in the substrate layer (Figure 10b). The burned area is concentrated near the bonding wires, indicating that the burnout was caused by the excessive current flowing through the bonding wires.

Figure 11a is the image of the decapped Cree device C2M0160120D. There are also severe burn marks. Compared with the results of SCT10N120, the burn areas of Cree device are more uniform and the degree of burn is lighter. It was found that the Cree device has more bonding wires (four wires) than the STM device (one wire). Therefore, it is possible that multiple bonding wires can spread out current, thus lower the maximum junction temperature and improve the surge performance of devices.

In addition, it is found that the melted Al covers the gate, as marked in the figures. This indicates that Al might have penetrated into the gate and causing the short circuit between the gate and the source.

From the anatomical results, the high temperature caused by excessive current is the main reason for the device failure. The high temperature caused burnout in many areas inside the device and eventually led to the device failure. In order to understand the process of the failure more clearly, the cross section of the damaged cell was cut and observed by SEM. The results are shown in Figures 12 and 13.

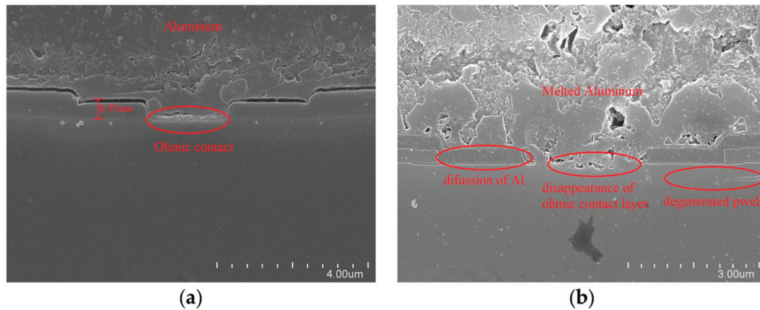


Figure 12. SEM images of SCT10N120 (**a**) before, (**b**) after the device failure.

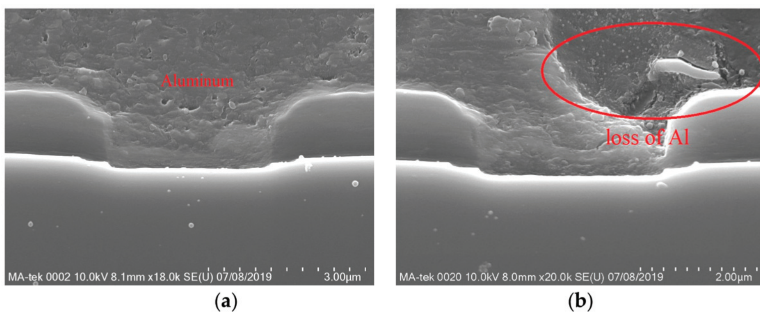


Figure 13. SEM images of C2M0160120D (**a**) before, (**b**) after the device failure.

Device SCT10N120 has been damaged more severely than device C2M0160120D. By comparing the SEM images of SCT10N120 taken before and after the failure, a few different types of device damages are possible.

4.2.1. Aluminum Melted and Diffused into the Interlayer Dielectric

Aluminm (Al) is used to form electrodes in these devices. Firstly, it is observed that Al was melted inside the failed devices. Secondly, it is found that the interlayer dielectric became thinner and its depth is changed from 0.55 µm to 0.36 µm, which indicates that Al may has eroded the interlayer dielectric.

A high temperature can melt Al which could diffuse into the insulator and cause the short circuit of the gate and source. The process is described by the following equation:

$$2\mathrm{Al} + \frac{3}{2}\mathrm{SiO_2} \rightarrow \mathrm{Al_2O_3} + \frac{3}{2}\mathrm{Si} \quad (5)$$

As mentioned in some literature, the product of the above reaction, Si, rapidly dissolves or migrates into Al, leaving fine voids, $(-)_{\mathrm{Al2O3}}$, in Al_2O_3.

$$\mathrm{Al} + \mathrm{Si} \rightarrow \mathrm{Al}:\mathrm{Si} + (-)_{\mathrm{Al_2O_3}} \quad (6)$$

Then, Al will self-diffuse into the voids and fills them,

$$Al + (-)_{Al_2O_3} \rightarrow (Al)_{Al_2O_3} \tag{7}$$

where $(Al)_{Al2O3}$ represents the Al that occupies the Al_2O_3 voids. Thus, the Al can react again with fresh SiO_2 (silicate glass) at the bottom of the Al_2O_3 voids in the process described by Equation (6) [35–37].

In addition, white spots appeared in the interlayer dielectric, indicating that Al has diffused into the interlayer dielectric. It also caused the short circuit of the gate and source.

4.2.2. Ohmic Contact Layer Disappeared

As shown in Figure 12a, there is an ohmic contact layer between the source metal and N+ source area. In Figure 12b, this ohmic contact layer disappears and the boundary between the source metal and N+ source area disappears.

For NMOS, Ni is generally used as an ohmic contact material [38,39]. The ohmic contact layer is formed by rapid annealing at high temperature after the deposition. Because Ni can easily react with SiC to form silicide at high temperature, NiSi and Ni_2Si are the main components in the ohmic contact layer.

Previously Hökelek and Robinson reported that Al started to react with NiSi at 400 °C by decomposing it and forming $NiAl_3$ and Si [40], as shown in the following equation:

$$3Al + NiSi \rightarrow NiAl_3 + Si \tag{8}$$

In reference to the findings of Bartur and Nicolet [41], the disappearance of Ni_2Si can be described as the result of an alternate process consisting of the thermodynamically feasible reaction:

$$6Al + Ni_2Si \rightarrow 2NiAl_3 + Si \tag{9}$$

The eutectic reaction of Si and Al (Equation (9)) enables Al to react with the ohmic contact layer continuously, eventually lead to the disappearance of the ohmic contact layer.

$$Al + Si \rightarrow Al : Si \tag{10}$$

4.2.3. Al Penetrated into SiC

The ohmic contact layer can prevent contact between Al and SiC. However, with the disappearance of the ohmic layer, Al penetrated into SiC regions. In Figure 12b, there is a discontinuous white line at 0.42 µm below the gate showing that Al has penetrated into the device. It is located at the boundary between the Pwell region and the N- drift region. It would affect the contact barrier of the body diode. Thus, the blocking performance of body diode would be affected.

In comparison, device C2M0160120D only exhibits the loss of Al, indicating Al has melted during the test. However, no penetration of Al into SiC regions has been found. That explains why the body diode of C2M0160120D can still have the reverse blocking capability after the test.

Therefore, the above analysis further reveals the failure regions and mechanisms of the device. When a large surge current flowed into the device, the device quickly heated up. The metal of the source electrode melted, eroded the interlayer dielectric then made the gate and the source contact each other. This eventually led to the short circuit between the gate and the source. Furthermore, the melted Al penetrated into the ohmic contact layer and made the ohmic contact layer disappear. Penetration of the Al into the body diode P/N junction also compromises its blocking capability.

4.3. Analysis of Simulation Result

In order to verify the findings of the experiments, finite element numeric simulation of the device has been carried out.

4.3.1. Simulation Setting

The simulation was completed by Silvaco TCAD, the device structure was generated by Devedit, and the surge simulation was completed by Mixmode. The structure of the SiC MOSFET C2M0080120D is shown in Figure 1. The structure parameters of the device are listed in the Table 1. The physical models used in simulation are shown in Table 5.

Table 5. Physical models used in simulation.

Model	Model Used in Simulation	Notes
Carrier Statistics Models	Fermi-Dirac	Reduced carrier concentrations in heavily doped regions (statistical approach).
	Bandgap Narrowing(BGN)	Important in heavily doped regions. Critical for bipolar gain. Use Klaassen Model.
Mobility Models	Lombardi (CVT) Model	Complete model including N, T, E//, and $E_{\perp}$ effects. *
Recombination Models	Shockley-Read-Hall(SRH)	Uses fixed minority carrier lifetimes.
	Auger	Direct transition of three carriers. Important at high current densities.
Impact Ionization Model	Selberherr's Model (Impact selb)	Recommended for most cases. Includes temperature dependent parameters.

* T is lattice temperature, N is the dopant concentration, E// is parallel electric field, and $E_{\perp}$ is perpendicular electric field.

To verify the simulation setting, the transfer characteristic of the device has been simulated and compared with the experimental results in Figure 14a. It can be seen that the curves match each other. Also shown in Figure 14b is the simulation and experimental results of the body diode forward conduction characteristics. The results are very similar.

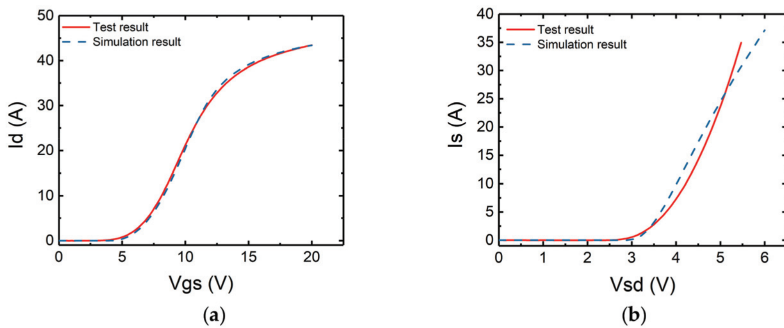


Figure 14. Comparison of (**a**) transfer characteristics, (**b**) body diode characteristics, between simulation and test result.

4.3.2. Surge Simulation Results and Analysis

Based on the device structure parameters listed in Table 1, the device was simulated and results were obtained. The input current was a sinusoidal current, with a 20 ms period.

The Channel Non-Conducting Mode

Atlas is not capable of directly simulate the device failure discussed in the previous sections, as it is mainly caused by some chemical reactions and the melting movement of aluminum at high temperature. Nevertheless, it is possible to simulate the temperature distribution inside the device when the surge occurs.

Mixed mode thermal simulation of the device has been carried out, and the results were obtained and shown in Figure 15.

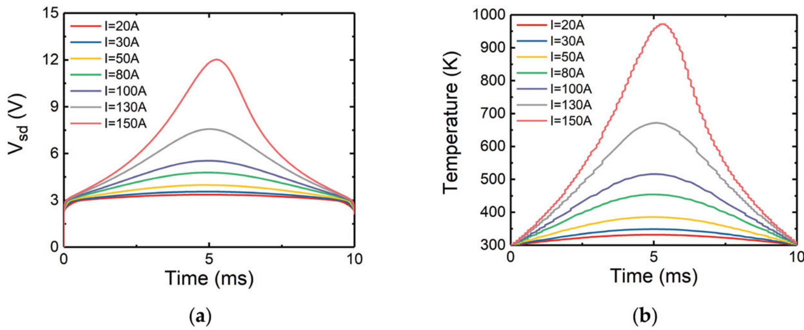


Figure 15. When the channel is non-conducting, the simulated (**a**) source-drain voltage, (**b**) maximum temperature, with time.

Plotted in Figure 15a is the variation of V_{sd} with time inside the device. Initially, there is a voltage jump. This phenomenon matches the experimental results, as shown in Figure 4. In the channel off mode, only the body diode is conducting, and the body diode will not conduct until the threshold voltage is reached. Therefore, there is a voltage jump in the beginning.

Figure 15b shows the change of maximum temperature inside the device with time under different surge current conditions. It can be seen that the trend of the maximum temperature is roughly consistent with that of the voltage. When the current peak value increases, the maximum temperature rises gradually. It can also be found that the temperature rises faster with the increase of current peak value.

The Channel Conduction Mode

The simulated curve of V_{sd} with time in the channel conduction mode is shown in Figure 16a. In Figure 16a, there is an obvious turning point on the voltage curve. In the channel conduction mode, at low current peak value the current flows through the channel. However, as the surge current increases, V_{sd} exceeds the body diode threshold voltage and the body diode conducts current as well. In the experiments, this turning point is not so obvious due to the influence of the parasitic capacitance and inductance. Shown in Figure 16b is the variation of internal maximum temperature with time in the channel conduction mode. The curve is similar to the case when the channel is not conducting.

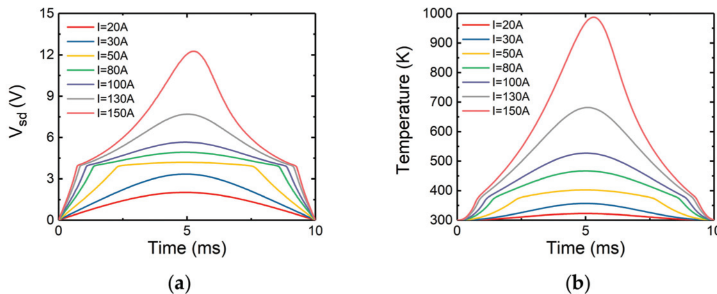


Figure 16. When the channel is conducting, the simulated variation of (**a**) source-drain voltage, (**b**) maximum temperature versus time.

The current densities in the body diode region and the channel when the channel was conducting have been simulated to find out the reasons why channel conduction had little effect on the device surge tolerance. The simulation results are shown in Figure 17. At low current peak value, the current

flows through the channel only. When the on-set voltage of body diode is reached, a portion of the current was transferred to the body diode region. It can be noticed that the slope of the current density flowing through the channel is decreased. Finally, the current density in the body diode becomes greater than the current density in the channel. Shown in Figure 17b are the current flowlines inside the device at t = 5 ms. The number of current flowlines is proportional to the current density. It can be seen that the number of the current flowlines in the body diode region is much more than that in the channel. From Figure 17, it is found that when the current is large enough, the current mainly passes through the body diode region.

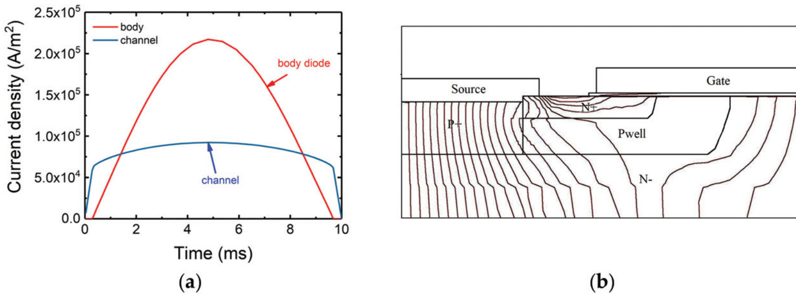


Figure 17. (**a**) Current density of body diode region and channel versus time. (**b**) Current flowlines in device when time = 5 ms.

It is found in the previous sections that the surge failure in this study is mainly caused by the high junction temperature. The maximum junction temperatures versus the time under channel conduction and non-conduction modes are compared in Figure 18. It can be seen that the maximum temperatures on conduction mode are slightly higher than that on the non-conduction mode. Therefore, it can be concluded that no matter the channel is conducting or not, the maximum junction temperatures inside the device are similar. As a result, the surge tolerance is approximately equal. This is mainly due to the fact that, when the current is big enough, the body diode current dominates against the MOS channel current. It also can be seen that, with the increase of the current, the maximum temperature inside the device could exceed the melting point of Al (933 K) and lead to the melting of Al.

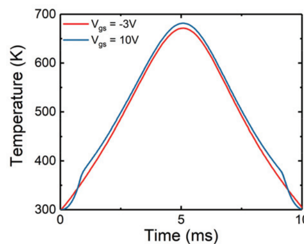


Figure 18. Comparison of the maximum temperature under channel conduction and non-conduction modes when I_s = 130 A.

5. Conclusions

In summary, the reverse conduction surge reliability of several 1200 V SiC MOSFETs has been tested in the channel conduction and non-conduction modes in this paper. Device failures under these circumstances have been investigated in detail. Two types of failure characterized by different behavior after the failure have been found. It is demonstrated that during the surge event the excessive heat

causes the melting of Aluminum and its subsequent reaction with and penetration into the SiC device and dielectric layers. Open-cover anatomy and 2-D numerical simulation confirms such mechanisms.

By increasing the surge current gradually until failure, it is found that the maximum surge currents that the devices can withstand are similar for both channel conduction and non-conduction modes.

The performance change of the device after failure is mainly reflected in two aspects: The first is the short circuit between the gate and the source, the other is the performance change of the body diode. Although the threshold voltages of the body diodes in all devices have been lowered after the failure, the reverse blocking characteristics of the body diodes are different. The reverse blocking capability of Cree's devices represented by C2M0160120D remain essentially unchanged, while other devices represented by SCT10N120 lost their reverse blocking capability after the surge failure. Then, the static characteristics of the device have been tested after each surge current was applied to help understanding the process of the failure. It is found that almost no damage occurred to the gate oxide and the body diode region until the maximum surge current was applied.

The open-cover anatomy of the two devices has been carried out. Both devices have burn marks, but the degree of damage is lighter for the Cree device. Increasing the number of bonding wires can spread the current more evenly across the chip and relieve damage caused by high temperature. By observing the cross section of the damaged cell, it is found that when the surge failure occurs, the source metal melts and penetrates into the interlayer dielectric and the P-well region, leading to the failure of the device.

Silvaco finite element numerical simulation has been employed to study the variation of the internal temperature and current density during the surge tests. In the simulation, it is found that when the surge current reaches a large value, the current mainly flows through the body diode. Therefore, whether the channel conducts or not has limited effect on the surge capability. This conclusion is consistent with the experimental results.

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References

1. Chow, T.P.; Tyagi, R. Wide bandgap compound semiconductors for superior high-voltage power devices. In Proceedings of the 5th International Symposium on Power Semiconductor Devices and ICs, Monterey, CA, USA, 18–20 May 1993; pp. 84–88. [CrossRef]
2. Chow, T.P.; Tyagi, R. Wide bandgap compound semiconductors for superior high-voltage unipolar power devices. *IEEE Trans. Electron. Devices* **1994**, *8*, 1481–1483. [CrossRef]
3. Chow, T.P.; Si, C.; Ga, N. High-voltage power switching devices. *Mater. Sci. Forum* **2000**, *338*, 1155–1160. [CrossRef]
4. Casady, J.B.; Johnson, R.W. Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review. *Solid-State Electron.* **1996**, *39*, 1409–1422. [CrossRef]
5. Saremi, M. modeling and Simulation of the Programmable Metallization Cells (pmcs) and Diamond-Based Power Devices. Ph.D. Thesis, Arizona State University, Tempe Campus, AZ, USA, 2017.
6. Aminbeidokhti, A.; Dimitrijev, S.; Hanumanthappa, A.K.; Moghadam, H.A.; Haasmann, D.; Han, J.; Xu, X. Gate-voltage independence of electron mobility in power AlGaN/GaN HEMTs. *IEEE Trans. Electron Devices* **2016**, *63*, 1013–1019. [CrossRef]
7. Aminbeidokhti, A.; Dimitrijev, S.; Hanumanthappa, A.K.; Moghadam, H.A.; Haasmann, D.; Han, J.; Xu, X. The power law of phonon-limited electron mobility in the 2-D electron gas of AlGaN/GaN heterostructure. *IEEE Trans. Electron. Devices* **2016**, *63*, 2214–2218. [CrossRef]

8. Kimoto, T.; Kosugi, H.; Suda, J.; Kanzaki, Y.; Matsunami, H. Design and fabrication of resurf MOSFETs on 4H-SiC and 6H-SiC. *IEEE Trans. Electron. Devices* **2005**, *52*, 112–117. [CrossRef]
9. Wondrak, W.; Held, R.; Niemann, E.; Schmid, U. SiC devices for advanced power and high-temperature applications. *IEEE Trans. Ind. Electron.* **2001**, *48*, 307–308. [CrossRef]
10. Palanisamy, S.; Fichtner, S.; Lutz, J.; Basler, T.; Rupp, R. Various structures of 1200V SiC MPS diode models and their simulated surge current behavior in comparison to measurement. In Proceedings of the 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Prague, Czech Republic, 12–16 June 2016; pp. 235–238. [CrossRef]
11. Kowalsky, J.; Simon, T.; Geske, M.; Basler, T.; Lutz, J. Surge Current Behaviour of Different IGBT Designs. In Proceedings of the PCIM Europe 2015, International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 19–21 May 2015; pp. 1–10.
12. Basler, T.; Lutz, J.; Jakob, R.; Brückner, T. Surge current capability of IGBTs. In Proceedings of the International Multi-Conference on Systems, Sygnals & Devices, Chemnitz, Germany, 20–23 March 2012; pp. 1–6. [CrossRef]
13. Basler, T.; Lutz, J.; Jakob, R. IGBTs conducting diode-like surge currents. In Proceedings of the 2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD), Waikoloa, HI, USA, 15–19 June 2014; pp. 103–106. [CrossRef]
14. Radhakrishnan, R.; Cueva, N.; Witt, T.; Woodin, R.L. Analysis of forward surge performance of sic schottky diodes. *Mater. Sci. Forum* **2018**, *924*, 621–624. [CrossRef]
15. Hilsenbeck, J.; Treu, M.; Rupp, R.; Rüschenschmidt, K.; Kern, R.; Holz, M. Investigations on surge current capability of SiC schottky diodes by implementation of new pad metallizations. *Mater. Sci. Forum* **2010**, *645*, 673–676. [CrossRef]
16. Banu, V.; Godignon, P.; Jordá, X.; Alexandru, M.; Millan, J. SiC schottky diode surge current analysis and application design using behavioral SPICE models. In Proceedings of the CAS 2012 (International Semiconductor Conference), Sinaia, Romania, 15–17 October 2012; pp. 359–362. [CrossRef]
17. León, J.; Perpiñà, X.; Banu, V.; Montserrat, J.; Berthou, M.; Vellvehí, M.; Jordà, X. Temperature effects on the ruggedness of SiC schottky diodes under surge current. *Microelectron. Reliab.* **2014**, *54*, 2207–2212. [CrossRef]
18. Hofstetter, P.; Bakran, M.M. Predicting Failure of SiC MOSFETs under short circuit and surge current conditions with a single thermal model. In Proceedings of the IEEE 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe), Riga, Latvia, 17–21 September 2018; pp. 1–9.
19. Sadik, D.P.; Heinig, S.; Jacobs, K.; Johannesson, D.; Lim, J.K.; Nawaz, M.; Dijkhuizen, F.; Bakowski, M.; Norrga, S.; Nee, H.P. Investigation of the surge current capability of the body diode of SiC MOSFETs for HVDC applications. In Proceedings of the European Conference on Power Electronics & Applications, Karlsruhe, Germany, 5–9 September 2016; pp. 1–10. [CrossRef]
20. Rodrigues, R.; Zhang, Y.; Jiang, T.; Aeloiza, E.; Cairoli, P. Surge current capability of SiC MOSFETs in AC distribution systems. In Proceedings of the IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Atlanta, GA, USA, 31 October–2 November 2018; pp. 331–337.
21. Carastro, F.; Mari, J.; Zoels, T.; Rowden, B.; Losee, P.; Stevanovic, L. Investigation on diode surge forward current ruggedness of Si and SiC power modules. In Proceedings of the European Conference on Power Electronics & Applications, Karlsruhe, Germany, 5–9 September 2016; pp. 1–10. [CrossRef]
22. Shan, Y.; Yunfei, G.; Shuairong, D.; Xiong, X.; Gang, D. Comparative Investigation of Surge Current Capabilities of Si IGBT and SiC MOSFET for Pulsed Power Application. *IEEE Trans. Plasma Sci.* **2018**, 1–6. [CrossRef]
23. Hofstetter, P.; Bakran, M.M. Comparison of the surge current ruggedness between the body diode of sic mosfets and si diodes for igbt. In Proceedings of the 10th International Conference on Integrated Power Electronics Systems (CIPS 2018), Stuttgart, Germany, 20–22 March 2018; pp. 1–7.
24. Jiang, X.; Zhai, D.; Chen, J.; Yuan, F.; Li, Z.; He, Z.; Wang, J. Comparison study of surge current capability of body diode of SiC MOSFET and SiC schottky diode. In Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, USA, 23–27 September 2018; pp. 845–849.
25. Yamamoto, S.; Nakao, Y.; Tomita, N.; Nakata, S.; Yamakawa, S. Development of 3.3 kV SiC-MOSFET:Suppression of forward voltage degradation of the body diode. *Mater. Sci. Forum* **2014**, *4*, 778–780. [CrossRef]
26. Imaizumi, M.; Miura, N. Characteristics of 600, 1200, and 3300 V planar SiC-MOSFETs for energy conversion applications. *IEEE Trans. Electron. Devices* **2014**, *62*, 390–395. [CrossRef]

27. Hull, B.; Allen, S.; Zhang, S.; Gajewski, D.; Pala, V.; Richmond, J.; Ryu, S.; O'Loughlin, M.; Van, B.E.; Cheng, L.; et al. Reliability and stability of SiC power mosfets and nextgeneration SiC MOSFETs. In Proceedings of the IEEE Workshop on Wide Bandgap Power Devices and Applications, Knoxville, TN, USA, 13–15 October 2014; pp. 139–142. [CrossRef]
28. Sadik, D.; Lim, J.; Ranstad, P.; Nee, H. Investigation of long-term parameter variations of SiC power MOSFETs. In Proceedings of the 17th European Conference on Power Electronics and Applications, Geneva, Switzerland, 8–10 September 2015; pp. 1–10. [CrossRef]
29. Callanan, R.; Rice, J.; Palmour, J. Third quadrant behavior of SiC MOSFETs. In Proceedings of the 28th Annual IEEE Applied Power Electronics Conference and Exposition, Long Beach, CA, USA, 17–21 March 2013; pp. 1250–1253. [CrossRef]
30. Hunger, T.; Schilling, O.; Wolter, F. Numerical and experimental study on surge current limitations of wire-bonded power diodes. In Proceedings of the PCIM Europe 2007, Nuremburg, Germany, 22–24 May 2007.
31. Schroder, D.K. *Semiconductor Material and Device Characterization*; John Wiley & Sons, Inc.: Hoboken, NJ, USA, 2006; pp. 370–372. [CrossRef]
32. Heinze, B.; Lutz, J.; Rupp, R.; Holz, M. Surge current ruggedness of silicon carbide Schottky and merged-PiN-Schottky Diodes. In Proceedings of the 20th International Symposium on Power Semiconductor Devices, Orlando, FL, USA, 18–22 May 2008; pp. 245–248. [CrossRef]
33. Silber, D.; Robertson, M.J. Thermal effects on the forward characteristic of silicon PiN diodes at high pulse currents. *Solid State Electron.* **1973**, *16*, 1337–1346. [CrossRef]
34. Fichtner, S.; Lutz, J.; Basler, T.; Rupp, R.; Gerlach, R. Electro-thermal simulations and experimental results on the surge current capability of 1200 V SiC MPS diodes. In Proceedings of the International Conference on Integrated Power Electronics Systems, Nuremberg, Germany, 25–27 February 2014; pp. 1–5, ISBN 978-3-8007-3578-5.
35. Berger, W.M.; Keen, R.S.; Schnable, G.L. Reliability phenomena in aluminum metalizations on silicon dioxide. In Proceedings of the 4th Symposium on the Physics of Failure in Electronics, Chicago, IL, USA, 16–18 November 1965; pp. 1–31. [CrossRef]
36. Black, J.R. Electromigration of Al-Si alloy films. In Proceedings of the 15th International Reliability Physics Symposium, San Diego, CA, USA, 18–20 April 1978; pp. 257–261. [CrossRef]
37. Tanimoto, S.; Ohashi, H. Reliability issues of SiC power MOSFETs toward high junction temperature operation. *Phys. Status Solidi A* **2009**, *206*, 2417–2430. [CrossRef]
38. Roccaforte, F.; Via, F.L.; Raineri, V. Ohmic Contacts to SIC. *Int. J. High Speed Electron. Syst.* **2005**, *15*, 781–820. [CrossRef]
39. Kakanakov, R.; Kassamakova-Kolaklieva, L.; Hristeva, N.; Lepoeva, G.; Zekentes, K. Thermally stable low resistivity ohmic contacts for high power and high temperature SiC device applications. In Proceedings of the 23rd International Conference on Microelectronics. Proceedings (Cat. No. 02TH8595), Nis, Yugoslavia, 12–15 May 2002. [CrossRef]
40. HKelek, E.; Robinson, G.Y. Aluminum/nickel silicide contacts on silicon. *Thin Solid Films* **1978**, *53*, 135–140. [CrossRef]
41. Bartur, M.; Nicolet, M.A. Thermal oxidation of nickel disilicide. *Appl. Phys. Lett.* **1982**, *40*, 175–177. [CrossRef]

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Design of 400 V Miniature DC Solid State Circuit Breaker with SiC MOSFET

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Abstract: Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) have the advantages of high-frequency switching capability and the capability to withstand high temperatures, which are suitable for switching devices in a direct current (DC) solid state circuit breaker (SSCB). To guarantee fast and reliable action of a 400 V DC SSCB with SiC MOSFET, circuit design and prototype development were carried out. Taking 400V DC microgrid as research background, firstly, the topology of DC SSCB with SiC MOSFET was introduced. Then, the drive circuit of SiC MOSFET, fault detection circuit, energy absorption circuit, and snubber circuit of the SSCB were designed and analyzed. Lastly, a prototype of the DC SSCB with SiC MOSFET was developed, tested, and compared with the SSCB with Silicon (Si) insulated gate bipolar transistor (IGBT). Experimental results show that the designed circuits of SSCB with SiC MOSFET are valid. Also, the developed miniature DC SSCB with the SiC MOSFET exhibits faster reaction to the fault and can reduce short circuit time and fault current in contrast with the SSCB with Si IGBT. Hence, the proposed SSCB can better meet the requirements of DC microgrid protection.

Keywords: silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs); solid state circuit breaker (SSCB); prototype; circuit design

1. Introduction

Direct current (DC) microgrids have elicited increasing attention in recent years, because they have a simple structure and are easy to control [1,2]. However, the safe and stable operation of a DC microgrid is inseparable from the effective protection technology [3]. When a short circuit occurs, fault current will rise instantly to a considerable extent. The equipment in the power system will suffer from huge electro-thermal stress, which seriously affects the operational reliability of the system [4,5]. Therefore, a circuit breaker is required to isolate the fault. Existing circuit breaker techniques can be classified into three types: mechanical circuit breaker, hybrid circuit breaker, and solid state circuit breaker [6–10]. The function of a mechanical circuit breaker is achieved by a mechanical switch. Although the mechanical circuit breaker can handle high current, electric arcing caused contact erosion reduces the lifetime and the disadvantage of long break time further limits its application. A hybrid circuit breaker is composed of a mechanical switch and parallel power devices. The current flows into the mechanical switch under normal working condition and transfers into the semiconductor switch under fault condition. The loss of a hybrid circuit breaker is minimal, but the control of a hybrid circuit breaker is complex. A solid state circuit breaker (SSCB) is composed of power devices

and related circuits to realize the interruption of fault current. The fault clearing time of an SSCB is short, but the drawback of an SSCB lies in its loss. By comparison, an SSCB responds rapidly to the fault and produces no arc when cutting off the current. Besides, without the interaction of mechanical switch and power switch, the control of an SSCB is not complex and the reliability is relatively high. Therefore, an SSCB can better meet the fast and reliable protection requirements in DC microgrid, and has received extensive concern.

The commonly used devices in SSCBs are Silicon (Si)-based power devices [9,11–14]. However, the performance of traditional Si devices has reached its limitation [15]. With the improvement of wide-bandgap semiconductor technology and its application in SSCBs, the performance of SSCBs can be further improved. Compared with Si devices, wide-bandgap semiconductor Silicon Carbide (SiC) devices exhibit further excellent properties. The comparison of material properties is provided in Table 1 [16]. Wider bandgap and higher thermal conductivity indicate that SiC devices can withstand higher temperature than Si devices, which reduces heat dissipation requirement of an SSCB. Higher electron velocity guarantees faster switching speed, higher frequency characteristics, and higher current density of SiC-based power devices. The aforementioned advantages enable SiC devices to operate faster and withstand higher temperature than Si devices, which break through the limitation and improve the fault response capability of Si-based SSCB [17,18].

Table 1. Material properties of Si and SiC.

Parameter	Si	SiC
Bandgap/eV	1.1	3.2
Thermal Conductivity/(W/(cm·°C))	1.3	4.6
Electron Velocity/(10^7 cm/s)	1	3

Among SiC power devices, SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) exhibit the most promising prospects [19,20], but study on SSCBs with SiC MOSFET is still in its infancy. Zhou et al. [21] introduced a digital SSCB with SiC MOSFET to identify inrush current, but the fault clearing time was long, which is adverse to the equipment protection in the power system. Ren et al. [22] focused on solving the inconsistency voltage distribution on cascaded SiC MOSFETs in SSCB in high voltage direct current (HVDC) transmission application, while the detailed design of SSCB was not given. Zhang et al. [23] proposed a changeable delay time protection method for SSCB with SiC MOSFET. However, the high requirements to parameter calculation and complicated design make the SSCB hard to realize. Therefore, to achieve quick and reliable action of the SSCB and to make the SSCB easy to realize in application, detailed design of the SSCB with SiC MOSFET should be carried out.

In this study, a 400 V DC microgrid was adopted as the application background. The topology and structure of an SSCB with SiC MOSFET were introduced. The design of the SSCB was described in detail, including device selection, gate driver, fault detection circuit, energy absorption circuit, and snubber circuit. Finally, a prototype of the DC SSCB with SiC MOSFET was developed, tested and compared with Si insulated gate bipolar transistor (IGBT). Experiment results proved that the designed SSCB with SiC MOSFET can operate reliably in case of failure and can reduce voltage spike during the turn-off period. In addition, the designed SSCB exhibits fast interrupting characteristics, which provide guidance for improving the performance of SSCB and the application of SSCB with SiC MOSFET.

2. Topology of the SSCB with SiC MOSFET

Figure 1a demonstrates the topology of the SSCB with SiC MOSFET. As illustrated in the figure, the SSCB with SiC MOSFET is composed of a SiC MOSFET switch, a drive circuit, a fault detection circuit, an energy absorption circuit, and a snubber circuit. The functions of the power device are to conduct current and to cut off the circuit when fault occurs. The drive circuit is used to send control signals to the power device to turn it on or off. The fault detection circuit can immediately detect

the faults and react. The energy generated during a fault period is absorbed and dissipated by the energy absorption circuit. The snubber circuit is used to suppress the voltage spike induced by circuit inductance in the initial turn-off stage to protect the voltage on the device from exceeding the rated voltage. The structure of the SSCB is depicted in Figure 1b to specifically show its components and further explain the working principle of the SSCB. The gate driver is connected to the SiC MOSFET by gate resistance R_g. The fault detection circuit detects variations in gate voltage. R_1 and R_2 are divider resistances. The function of energy absorption circuit is realized by using a metal-oxygen-varistor (MOV), and the snubber circuit is achieved by simply using MOV_in instead of the commonly used resistance-capacitor (RC) or resistance-capacitor-diode (RCD) circuit [24]. L_1 and L_2 are the parasitic inductances.

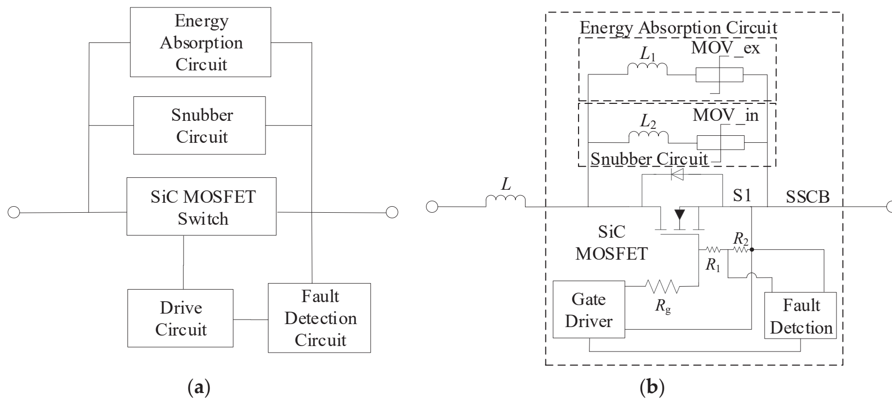

Figure 1. (**a**) Topology of the solid state circuit breaker (SSCB) with SiC metal-oxide-semiconductor field-effect transistor (MOSFET); (**b**) Structure of the SSCB with SiC MOSFET.

The working principle of the SSCB of SiC MOSFET can be explained as below: S1 conducts and current flows through SiC MOSFET under normal working condition. The resistance of MOV_in and MOV_ex are high, and no current flows into the snubber circuit and the energy absorption circuit. When abnormal state occurs, the fault current increases rapidly and causes the change of gate voltage. Through logical judgement and comparison, a turn-off signal is sent to gate driver to turn off the SiC MOSFET. Simultaneously, the voltage on SSCB reaches to the breakdown voltage of MOV, the resistance of MOV immediately drops to a very small value and the voltage on SSCB is clamped. First, MOV_in is triggered to operate to suppress the voltage spike in the early turn-off stage. Then, MOV_ex operates and because of the voltage difference between MOV_in and MOV_ex, the fault current transfers to energy absorption circuit. During this time, the voltage on MOV_ex is higher than the DC-link voltage. MOV_ex in absorbs the energy and fault current attenuates gradually. When the current reaches to zero, the SSCB stops working and fault is cleared.

3. Design of the SSCB with SiC MOSFET

3.1. Device Selection

The designed SSCB is used in a 400 V DC microgrid. A high induced voltage V_L is generated at the early turn-off period due to the fast switching speed and the existence of parasitic inductance in the circuit. Therefore, the SiC MOSFET is required to withstand the sum voltage of DC-link voltage V_{DC} and V_L. V_L is determined by the parasitic parameters in the circuit and change rate of the current. In consideration of the magnitude of the inductance in circuit board (less than 0.2 μH) and the di/dt for SiC MOSFET in turn-off stage (1–3 A/ns) [25], the induced voltage V_L may reach 200 V or above. Therefore, the withstand voltage of the device is preferably guaranteed to have larger margin in

application [21,26]. Considering the SSCB can be used under high current condition, devices with high rated current can be selected. To date, the major manufacturers of SiC MOSFETs are CREE (Durham, NC, USA) and ROHM (Kyoto, Japan). Both manufacturers have products with relatively high rated current: C2M0080120D of 36 A, SCT2080KE of 40 A. However, the device must have a stronger short circuit withstand capability to assure the reliability of the SSCB. According to the study of Wang et al. [27], the comparison of short circuit withstand time (SCWT) and critical energy of the 1200 V/80 mΩ CREE and ROHM SiC MOSFET are made in Table 2. The SCWT of ROHM SiC MOSFET is higher than CREE SiC MOSFET under same DC-link voltage or temperature. In addition, the critical energy of ROHM product is also greater than CREE product. Thus, the 1200 V/80 mΩ ROHM SiC MOSFET performs better than CREE SiC MOSFET in harsh condition. Accordingly, SCT2080KE, with the rated voltage of 1200 V and rated current of 40 A is selected as the switching device of the SSCB.

Table 2. Comparison of the 1200 V/80 mΩ CREE and ROHM SiC MOSFET.

Device	Temperature = 25 °C, V_{DC} = 600 V		Temperature = 200 °C, V_{DC} = 400 V	
	SCWT/µs	Critical Energy/J	SCWT/µs	Critical Energy/J
CREE	3.5	1.2	4.7	1.3
ROHM	4.7	1.6	5	1.4

3.2. Drive Circuit

The suitable drive circuit is the prerequisite for ensuring the satisfactory operation of the SSCB with SiC MOSFET. To assure the fast switching speed, it is necessary to select the proper gate voltage. In addition, the design of the drive circuit must also consider the value of gate resistance, the selection of driver chip.

3.2.1. Gate Voltage

Gate voltage is crucial to develop the excellent characteristics for the SiC MOSFET. Figure 2 shows the relationship between gate voltage and on-state resistance. When gate voltage is low, on-state resistance is relatively high, which will result in large on-state loss. After reaching a certain value, on-state resistance can be considerably reduced. Hence, a higher gate voltage is generally applied. In addition, gate voltage affects the switching characteristics of the device. The device switches faster with the increase in gate voltage, but the voltage should not be excessively high in case of oscillation. Moreover, a high gate voltage can adversely affect the reliability of the gate oxide, thereby resulting in device failure.

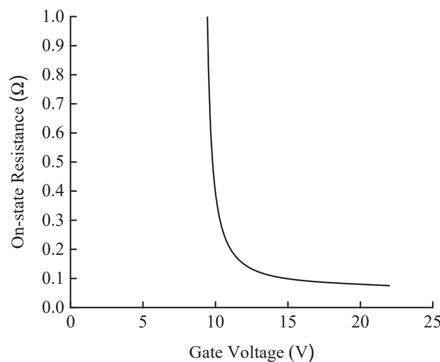

Figure 2. Relationship between gate voltage and on-state resistance of the SiC MOSFET.

A negative gate voltage is generally required to reliably turn off the SiC MOSFET. The higher the voltage, the faster the device can turn off. Similarly, a large negative voltage adversely affects the reliability of the gate oxide. Based on the preceding analysis and combined with the datasheet provided by manufacturer, gate voltage is recommended to be −5/18 V.

3.2.2. Gate Resistance

Gate resistance must be considered in the design of the drive circuit. If the gate resistance is large, then oscillation during the switching process can be suppressed, but the turn-on and turn-off speed will be slow. This condition may increase the loss of the device. By contrast, if the gate resistance is small, then the switching speed accelerates, which easily leads to current and voltage oscillation. However, the loss of the device will decrease. According to the analysis of Li et al. [28] and after repeated testing, gate resistance is determined to be 10 Ω.

3.2.3. Driver Chip

At present, the driver chips available for SiC MOSFETs on the market are mainly IXYS_609 of IXYS (Milpitas, CA, USA) and ACPL-W346 of Avago (San Jose, CA, USA). The drive capability of IXVYS_609 is relatively stronger, which can provide peak current of 9 A. However, it has no isolation function. The drive capability of ACPL_W346 is weaker than that of IXVYS_609. It can provide a peak current of 2 A and is integrated with an optocoupler isolation. The peak current of 2 A is sufficient for a single SiC device. The drive circuit can be more compact due to the integrated optocoupler isolation, and the volume of the SSCB can be reduced. Therefore, the ACPL_W346 chip is selected. Table 3 lists the main technical parameters of ACPL_W346. The specific design scheme of the driving circuit based on ACPL_W346 is described in [29].

Table 3. Main technical parameters of ACPL-W346.

Parameter	Minimal Value	Maximal Value
Source V_{CC}/V	10	20
Output Current I_{OUT}/A	-	2.5
Working Temperature T/°C	−40	105
Propagation Delay/ns	-	120
Common Mode Restraining Capability/kV·μs^{-1}	50	-

3.3. Fault Detection Circuit

During the fault process, the fault current will cause an evident change in the gate-source voltage because of the existence of the Miller capacitance [30]. Thus, the fault can be detected by the change of gate-source voltage. Figure 3 shows the schematic diagram of the fault detection circuit based on gate-source voltage variation.

As shown in Figure 3, the fault detection circuit is composed of clamping circuit, fault detection section, latch circuit, logic control circuit, and reset circuit. The clamping circuit is used to suppress the rise in gate voltage and avoid the overvoltage harm to the gate oxide. The divided gate-source voltage is sent to the differential operational amplifier, whose output is connected to the inverting input of the comparator, and the reference signal is connected to the non-inverting input. If the divided voltage exceeds the reference voltage, then the comparator output signal level switches from high to low. The SR latch circuit outputs a high level and remains. After sending the signal to the inverter, the signal logic reverses. The signal is then sent to the AND gate. During this time, even if the drive control signal is at a high level, the signal level of the AND gate output still remains low. This signal is the input signal of the drive circuit. In this way, the SSCB operates and the SiC MOSFET is turned-off. Figure 4 shows the sequence chart of the fault detection circuit under fault condition.

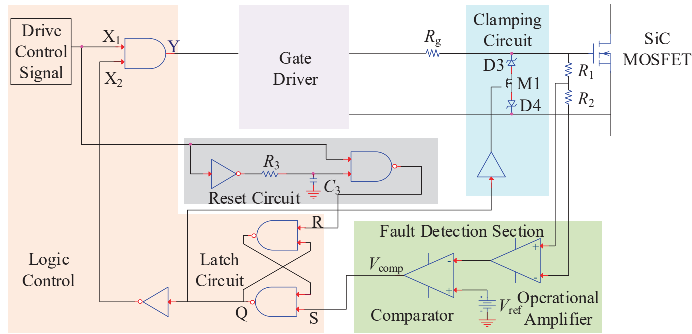

Figure 3. Schematic diagram of fault detection circuit.

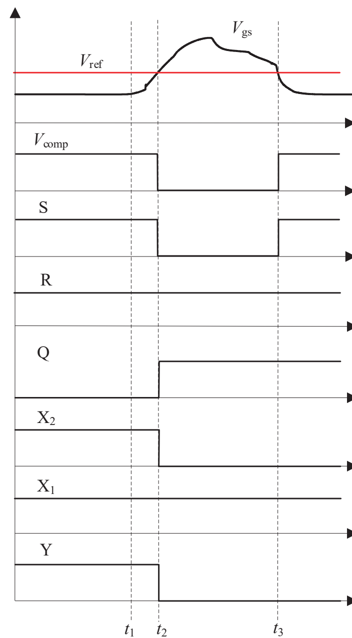

Figure 4. Sequence chart of fault detection circuit under fault condition.

3.4. Design of the Energy Absorption Circuit

During the fault clearing period, the energy stored in the parasitic inductance of the circuit is dissipated by the energy absorption circuit, and the function is achieved by MOV_ex. The voltage on SSCB is clamped to Vmov because of the clamping function of MOV. The voltage on inductance L can be expressed by:

$$V_L = V_{\mathrm{MOV}} - V_{\mathrm{DC}}, \tag{1}$$

where, V_{DC} is the DC-link voltage. To simplify the analysis, the change rate of fault current is assumed to be linear based on the simulation and test results in [31–33]. The inductance current, namely the current of SSCB, can then be calculated as follows:

$$i_L = I_{\mathrm{max}} - \frac{V_{\mathrm{MOV}} - V_{\mathrm{DC}}}{L} t, \tag{2}$$

where I_{max} is the peak current. When SSCB starts to operate, the current will gradually attenuate to zero from its peak value. By setting i_L = 0, the total working time of SSCB t_s can be obtained.

$$t_s = \frac{I_{max} L}{V_{MOV} - V_{DC}} \tag{3}$$

The absorbed energy in the energy absorption circuit can then be achieved by:

$$\begin{aligned} W_{MOV_ex} &= \int_0^{t_s} V_{MOV} \cdot i_L dt \\ &= \int_0^{t_s} V_{MOV} \cdot (I_{max} - \frac{V_{MOV} - V_{DC}}{L} t) dt \\ &= \frac{1}{2} (\frac{V_{DC}}{V_{MOV} - V_{DC}}) L I_{max}^2 \end{aligned} . \tag{4}$$

Since the inductance in the circuit is low (μH level), the energy that needs to be absorbed is small although the short circuit current is high. Thus, an ordinary MOV can meet the requirement of the design. In this study, V_{DC} is 400 V. After looking up the product model, 14D511K is selected as the MOV_ex. Main parameters of 14D511K are listed in Table 4.

Table 4. Main parameters of 14D511K.

Allowable DC Operating Voltage	Breakdown Voltage	Maximal Clamping Voltage	Maximal Absorbed Energy	Power
415 V	510 V	845 V	125 J	0.6 W

3.5. Design of the Snubber Circuit

To suppress the voltage spike, MOV_in is used in the snubber circuit. The fault current will flow into MOV_in first due to smaller parasitic resistance in the snubber circuit. Then, the current will quickly transfer to MOV_ex and MOV_ex will continue to absorb the energy. Thus, MOV_in only works during the early turn-off stage and absorbs minimal energy. However, the voltage of MOV_in affects the peak voltage of SSCB, and the selection of MOV_in is related to MOV_ex. Figure 5 illustrates the simulated relationship of absorbed energy and peak voltage to voltage ratio. With the increase of breakdown voltage ratio of MOV_in and MOV_ex, MOV_in absorbs less energy, while the voltage overshoot of SSCB increases. When voltage ratio is greater than 1.3, the snubber circuit absorbs minimal energy and barely changes. Considering that the energy MOV_in absorbs and the peak voltage can be suppressed effectively, the breakdown voltage of MOV_in can be 1.3 times that of MOV_ex. Since the breakdown voltage of MOV_ex is selected to be 510V, 05D681K with the breakdown voltage of 680V is chosen. The main parameters are provided in Table 5.

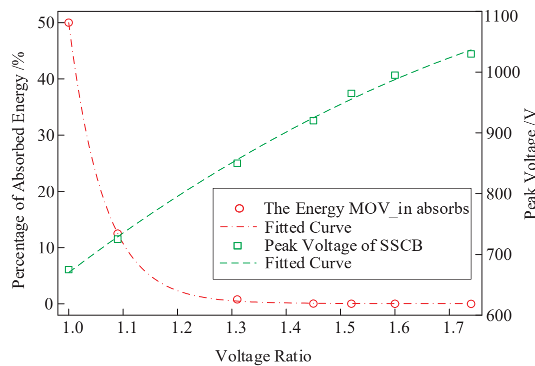

Figure 5. Absorbed energy and peak voltage at varying voltage ratio.

Table 5. Main parameters of 05D681K.

Allowable DC Operating Voltage	Breakdown Voltage	Maximal Clamping Voltage	Maximal Absorbed Energy	Power
560 V	680 V	1120 V	21 J	0.1 W

4. Testing on the SSCB Prototype with SiC MOSFET

Based on the structure of Figure 1b, the prototype of the SSCB with SiC MOSFET was developed and is shown in Figure 6a. The SSCB is composed of a SiC MOSFET, a gate driver, a fault detection circuit, an energy absorption circuit, and a snubber circuit. Gate driver uses the ACPL-W346 driver chip. Fault detection circuit is based on the schematic diagram in Figure 3. Energy absorption circuit is composed of MOV (14D511K) to absorb the energy. Snubber circuit is composed of MOV (05D681K) to suppress the voltage spike in the early turn-off period. The fault simulation circuit is shown in Figure 6b, where S1 is the SSCB prototype. Switch S2, which is parallel with the load, is another SiC MOSFET that controls on and off of the circuit. Load is represented by a 100 Ω resistance. Voltage-stabilizing capacitor C is 560 µF, and DC-link voltage is 400 V. First, S1 is on while S2 is off. The system is under normal working condition. After 5 µs, a turn-on signal is sent to S2, placing the system in a short circuit state, and the current rapidly increases. To prevent the abnormal state caused by the malfunction of SSCB, S1 is forcibly turned off after 3 µs of short circuit. The sequence of the control signals is shown in Figure 7.

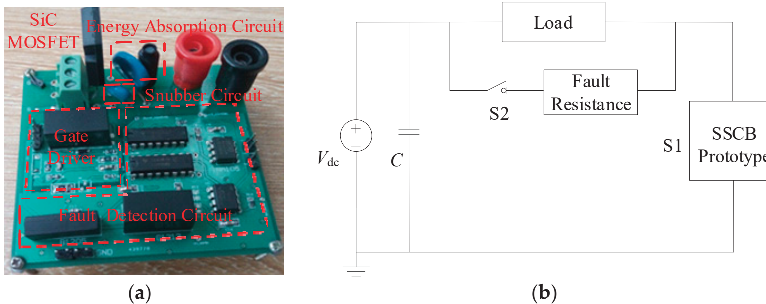

Figure 6. (**a**) SSCB prototype with SiC MOSFET and (**b**) fault simulation circuit.

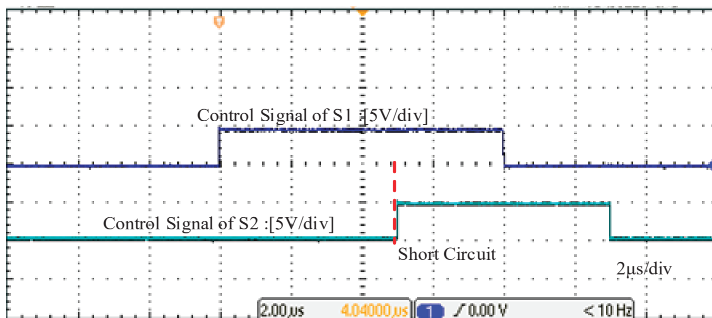

Figure 7. Sequence of control signals of S1 and S2.

Figure 8 presents the test results of the fault detection circuit. When short circuit happens, gate voltage evidently rises. The differential operational amplifier can detect the change and react immediately. A turn-off signal is sent to the gate driver subsequently.

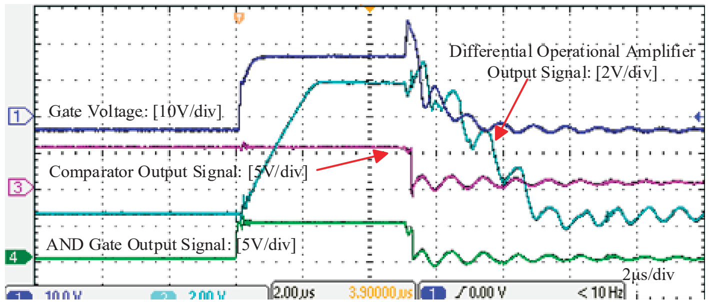

Figure 8. Waveforms of gate voltage change and test results of the fault detection circuit.

Figure 9 shows the test results of the SSCB under the fault. The purple curve is the current waveform, whereas the blue curve is the voltage waveform. Figure 9a,b illustrate the cases where the snubber circuit is disconnected and connected to the circuit, respectively. When the snubber circuit is not connected, the peak voltage of SSCB during short circuit is 800 V, and oscillation is acute. Voltage spike can be suppressed to 750 V and the oscillation can be greatly restrained due to the existence of the snubber circuit. In addition, the peak fault current is approximately 80 A and the fault clearing time is about 720 ns. Therefore, the SSCB with SiC MOSFET can interrupt the current rapidly, and prevent the device from being exposed to high energy, long time shock, which provides protection for the device and improves the reliability of the system.

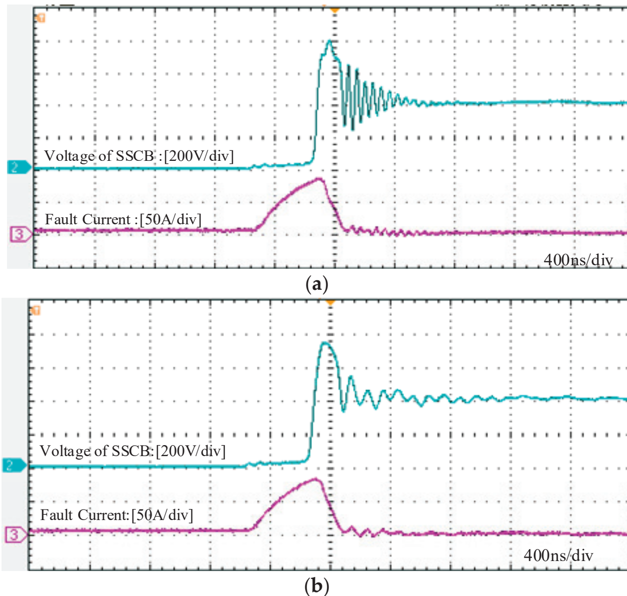

Figure 9. Waveforms of the fault current and voltage of the SSCB with SiC MOSFET: (**a**) without a snubber circuit and (**b**) with a snubber circuit.

This study also does a test on an SSCB with Si IGBT, whose driver chip is TX-DA962D6 by LMY electronics, integrated with the desaturation detection function. Figure 10 shows the experimental result. The purple and blue curves represent the current waveform and voltage waveform, respectively. As shown in the figure, the fault clearing time is 2.8 µs and the fault current is up to 300 A. Both of

these values are nearly four-fold those of the SSCB with SiC MOSFET. Such high current with such long time will exert huge electro-thermal stress on device and equipment in the system.

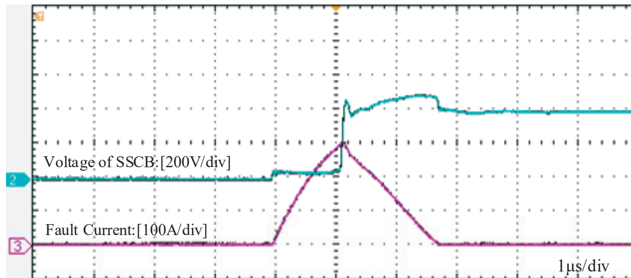

Figure 10. Waveforms of fault current and voltage of the SSCB with an Si insulated gate bipolar transistor (IGBT).

In summary, by using an SiC MOSFET as the switching device, the designed SSCB prototype is evidently faster than SSCB with Si IGBT, which can cut off the fault current within 1 µs. The proposed SSCB with SiC MOSFET is distinguished by the fault detection circuit and the simplicity of the snubber circuit. On one hand, the fault detection method used in an Si-based SSCB is extended to an SSCB with SiC MOSFET because of the existence of a Miller capacitor in the SiC MOSFET. The fault can be detected rapidly and effectively based on the variation in gate voltage. On the other hand, by replacing the RC or RCD snubber circuit with MOV, the complicated design of parameters can be avoided and voltage spike can be suppressed as well. The detailed design in this study makes the realization of SSCB with SiC MOSFET easier and less complicated, providing reference for design and improvement of SSCB.

5. Conclusions

In order to realize the fast and reliable fault isolation in DC microgrid, the topology and structure of a 400 V miniature DC SSCB with SiC MOSFET are introduced. The design of the SSCB prototype is described in detail, including the selection of the device, drive circuit, current detection circuit, energy absorption circuit, and snubber circuit. The experimental results demonstrate that the SSCB with SiC MOSFET can immediately detect and interrupt the fault within 720 ns, peak current value of 80 A. Compared with the SSCB with Si IGBT, the proposed SSCB evidently has shorter interruption time and causes less thermal stress on the device.

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References

1. Bifaretti, S.; Zanchetta, P.; Watson, A.; Tarisciotti, L.; Clare, J.C. Advanced Power Electronic Conversion and Control System for Universal and Flexible Power Management. *IEEE Trans. Smart Grid* **2011**, *2*, 231–243. [CrossRef]
2. Dragičević, T.; Lu, X.; Vasquez, J.C.; Guerrero, J.M. DC Microgrids—Part II: A Review of Power Architectures, Applications, and Standardization Issues. *IEEE Trans. Power Electron.* **2016**, *31*, 3528–3549. [CrossRef]

3. Yang, J.; Fletcher, J.E.; O'Reilly, J. Short-Circuit and Ground Fault Analyses and Location in VSC-Based DC Network Cables. *IEEE Trans. Ind. Electron.* **2012**, *59*, 3827–3837. [CrossRef]
4. Salomonsson, D.; Soder, L.; Sannino, A. Protection of Low-Voltage DC Microgrids. *IEEE Trans. Power Deliv.* **2009**, *24*, 1045–1053. [CrossRef]
5. Munasib, S.; Balda, J.C. Short-circuit protection for low-voltage DC microgrids based on solid-state circuit breakers. In Proceedings of the 2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Vancouver, BC, Canada, 27–30 June 2016; IEEE: Piscataway, NJ, USA, 2016; pp. 1–7.
6. Shukla, A.; Demetriades, G.D. A Survey on Hybrid Circuit-Breaker Topologies. *IEEE Trans. Power Deliv.* **2015**, *30*, 627–641. [CrossRef]
7. Meyer, J.-M.; Rufer, A. A DC Hybrid Circuit Breaker with Ultra-Fast Contact Opening and Integrated Gate-Commutated Thyristors (IGCTs). *IEEE Trans. Power Deliv.* **2006**, *21*, 646–651. [CrossRef]
8. Franck, C.M. HVDC Circuit Breakers: A Review Identifying Future Research Needs. *IEEE Trans. Power Deliv.* **2011**, *26*, 998–1007. [CrossRef]
9. Kempkes, M.; Roth, I.; Gaudreau, M. Solid-state circuit breakers for Medium Voltage DC power. In Proceedings of the 2011 IEEE Electric Ship Technologies Symposium, Alexandria, VA, USA, 10–13 April 2011; IEEE: Piscataway, NJ, USA, 2011; pp. 254–257.
10. Shen, Z.J.; Miao, Z.; Roshandeh, A.M. Solid state circuit breakers for DC micrgrids: Current status and future trends. In Proceedings of the 2015 IEEE First International Conference on DC Microgrids (ICDCM), Atlanta, GA, USA, 7–10 June 2015; IEEE: Piscataway, NJ, USA, 2015; pp. 228–233.
11. Sano, K.; Takasaki, M. A Surgeless Solid-State DC Circuit Breaker for Voltage-Source-Converter-Based HVDC Systems. *IEEE Trans. Ind. Appl.* **2014**, *50*, 2690–2699. [CrossRef]
12. Schmerda, R.; Cuzner, R.; Clark, R.; Nowak, D.; Bunzel, S. Shipboard Solid-State Protection: Overview and Applications. *IEEE Electr. Mag.* **2013**, *1*, 32–39. [CrossRef]
13. Schmitt, S. MOSFET Selection and Drive Strategies for DC Solid State Circuit Breakers. In Proceedings of the PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 20–22 May 2014; IEEE: Piscataway, NJ, USA, 2014; pp. 1–6.
14. Vemulapati, U.; Arnold, M.; Rahimo, M.; Antoniazzi, A.; Pessina, D. Reverse blocking IGCT optimised for 1 kV DC bi-directional solid state circuit breaker. *IET Power Electron.* **2015**, *8*, 2308–2314. [CrossRef]
15. Takayanagi, R.; Taniguchi, K.; Kaneko, S.; Kanai, N.; Kumada, K.; Hori, M.; Ikeda, Y.; Maruyama, K.; Kawamura, I. 3.3kV All-SiC Module for Electric Distribution Equipment. In Proceedings of the 2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia), Niigata, Japan, 20–24 May 2018; IEEE: Piscataway, NJ, USA, 2018; pp. 3396–3400.
16. Millán, J.; Godignon, P.; Perpiñà, X.; Pérez-Tomás, A.; Rebollo, J. A Survey of Wide Bandgap Power Semiconductor Devices. *IEEE Trans. Power Electron.* **2014**, *29*, 2155–2163. [CrossRef]
17. Handt, K.; Griepentrog, G.; Maier, R. Intelligent, compact and robust semiconductor circuit breaker based on silicon carbide devices. In Proceedings of the 2008 IEEE Power Electronics Specialists Conference, Rhodes, Greece, 15–19 June 2008; IEEE: Piscataway, NJ, USA, 2008; pp. 1586–1591.
18. Sato, Y.; Tanaka, Y.; Fukui, A.; Yamasaki, M.; Ohashi, H. SiC-SIT Circuit Breakers with Controllable Interruption Voltage for 400-V DC Distribution Systems. *IEEE Trans. Power Electron.* **2014**, *29*, 2597–2605. [CrossRef]
19. Östling, M. Silicon carbide based power devices. In Proceedings of the 2010 International Electron Devices Meeting, San Francisco, CA, USA, 6–8 December 2010; IEEE: Piscataway, NJ, USA, 2010; pp. 13.3.1–13.3.4.
20. She, X.; Huang, A.Q.; Lucía, Ó.; Ozpineci, B. Review of Silicon Carbide Power Devices and Their Applications. *IEEE Trans. Ind. Electron.* **2017**, *64*, 8193–8205. [CrossRef]
21. Zhou, Y.; Feng, Y.; Liu, T.; Shen, Z.J. A Digital-Controlled SiC-Based Solid State Circuit Breaker with Soft-Start Function for DC Microgrids. In Proceedings of the 2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Charlotte, NC, USA, 25–28 June 2018; IEEE: Piscataway, NJ, USA, 2018; pp. 1–7.
22. Ren, Y.; Yang, X.; Qiao, L.; Zhang, F.; Wang, L. A novel solid-state DC-breaker based on cascaded SiC MOSFETs. In Proceedings of the 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, USA, 26–30 March 2017; IEEE: Piscataway, NJ, USA, 2017; pp. 824–828.

23. Zhang, Y.; Liang, Y.C. Over-current protection scheme for SiC power MOSFET DC circuit breaker. In Proceedings of the 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, USA, 14–18 September 2014; IEEE: Piscataway, NJ, USA, 2014; pp. 1967–1971.
24. Shin, D.; Sul, S.-K.; Sim, J.; Kim, Y.-G. Snubber Circuit of Bidirectional Solid State DC Circuit Breaker Based on SiC MOSFET. In Proceedings of the 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, USA, 23–27 September 2018; IEEE: Piscataway, NJ, USA, 2018; pp. 3674–3681.
25. Wada, K.; Ando, M. Limitation of DC-side stray inductance by considering over voltage and short-circuit current. In Proceedings of the 2013 15th European Conference on Power Electronics and Applications (EPE), Lille, France, 2–6 September 2013; IEEE: Piscataway, NJ, USA, 2013; pp. 1–8.
26. Shen, Z.J.; Sabui, G.; Miao, Z.; Shuai, Z. Wide-Bandgap Solid-State Circuit Breakers for DC Power Systems: Device and Circuit Considerations. *IEEE Trans. Electron. Devices* **2015**, *62*, 294–300. [CrossRef]
27. Wang, Z.; Shi, X.; Tolbert, L.M.; Wang, F.; Liang, Z.; Costinett, D.; Blalock, B.J. Temperature-Dependent Short-Circuit Capability of Silicon Carbide Power MOSFETs. *IEEE Trans. Power Electron.* **2016**, *31*, 1555–1566. [CrossRef]
28. Li, H.; Munk-Nielsen, S. Detail study of SiC MOSFET switching characteristics. In Proceedings of the 2014 IEEE 5th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Galway, Ireland, 24–27 June 2014; IEEE: Piscataway, NJ, USA, 2014; pp. 1–5.
29. Download Reference Designs|Wolfspeed, KIT8020-CRD-8FF1217P-1: 1200V MOSFET EVALUATION KIT. Available online: https://www.wolfspeed.com (accessed on 20 April 2015).
30. Lu, B.; Sharma, S.K. A Literature Review of IGBT Fault Diagnostic and Protection Methods for Power Inverters. *IEEE Trans. Ind. Appl.* **2009**, *45*, 1770–1777.
31. Ren, Y.; Yang, X.; Zhang, F.; Wang, F.; Tolbert, L.M.; Pei, Y. A Single Gate Driver Based Solid-State Circuit Breaker Using Series Connected SiC MOSFETs. *IEEE Trans. Power Electron.* **2019**, *34*, 2002–2006. [CrossRef]
32. Martin, W.A.; Deng, C.; Fiddiansyah, D.; Balda, J.C. Investigation of low-voltage solid-state DC breaker configurations for DC microgrid applications. In Proceedings of the 2016 IEEE International Telecommunications Energy Conference (INTELEC), Austin, TX, USA, 23–27 October 2016; IEEE: Piscataway, NJ, USA, 2016; pp. 1–6.
33. Lei, F.; Rui, G.; Fang, Z.; Xiao, Y.; Fan, Z. Development of a 10kV solid-state DC circuit breaker based on press-pack IGBT for VSC-HVDC system. In Proceedings of the 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), Hefei, China, 22–26 May 2016; IEEE: Piscataway, NJ, USA, 2016; pp. 2371–2377.

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Transient Simulation for the Thermal Design Optimization of Pulse Operated AlGaN/GaN HEMTs

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Abstract: The thermal management and channel temperature evaluation of GaN power amplifiers are indispensable issues in engineering field. The transient thermal characteristics of pulse operated AlGaN/GaN high electron mobility transistors (HEMT) used in high power amplifiers are systematically investigated by using three-dimensional simulation with the finite element method. To improve the calculation accuracy, the nonlinear thermal conductivities and near-junction region of GaN chip are considered and treated appropriately in our numerical analysis. The periodic transient pulses temperature and temperature distribution are analyzed to estimate thermal response when GaN amplifiers are operating in pulsed mode with kilowatt-level power, and the relationships between channel temperatures and pulse width, gate structures, and power density of GaN device are analyzed. Results indicate that the maximal channel temperature and thermal impedance of device are considerably influenced by pulse width and power density effects, but the changes of gate fingers and gate width have no effect on channel temperature when the total gate width and active area are kept constant. Finally, the transient thermal response of GaN amplifier is measured using IR thermal photogrammetry, and the correctness and validation of the simulation model is verified. The study of transient simulation is demonstrated necessary for optimal designs of pulse-operated AlGaN/GaN HEMTs.

Keywords: AlGaN/GaN HEMTs; thermal simulation; transient channel temperature; pulse width; gate structures

1. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) have recently been researched intensively and are considered prospective for high-power RF applications, owing to the advantages such as wide bandgap, high breakdown voltage, and high electron mobility [1–4]. However, high power applications require high power densities in the active region of GaN devices, which leads to highly localized Joule self-heating and potentially high peak temperatures. The localized self-heating of two dimensional electron gas in the conducting channel limits the highest output power density and decreases its reliability. Therefore, the self-heating effect is a main factor that limits the power density of GaN HEMTs [3–6]. To exploit the full potential of GaN devices, especially high-power amplifiers, a great concern is the thermal management both from a performance point of view and more importantly to ensure adequate device reliability [2–8].

For the high-power amplifiers used in radar and communication system, the GaN HEMTs are often operated in pulsed mode, although performance is typically pulse width for the purpose of thermal management, and to maintain the operating channel temperature within a safe limit to avoid thermally activated degradation of the device performance. Meanwhile, the relation between typically pulse width and channel temperature is influenced by thermal design of GaN HEMTs, including the

structure of gates and the power density. Previous works on thermal management in GaN HEMTs has been made, but those researches were focused on self-heating effect with different substrate materials, near-junction region thicknesses, and interfacial layers. However, thorough understanding of the effects of pulse width, gate structures, and power density on channel temperatures have not been well addressed, which are desirable for optimal implementation of GaN HEMT used in high-power amplifiers [2,4,7–11]. Meanwhile, these effects can hardly be predicted by measurements because of the limits of the spatial and temporal resolution. Therefore an accurate transient thermal analysis method is highly desired.

In this paper, we analyze the transient thermal characteristics of pulse-operated AlGaN/GaN HEMT used in high power amplifiers. The relationships between channel temperatures and pulse width, gate structures, and power density of GaN amplifiers with kilowatt-level power are analyzed using the finite element method implemented by the commercial simulation software (COMSOL). The simulation details such as the geometry of the multi fingers GaN HEMTs and material properties are presented in Section 2. The numerical results and discussion in Section 3 focus on illustrating the heat spreading effect and optimizing thermal design. Finally, the experimental test for the thermal design of GaN amplifier is shown in Section 4, and some conclusions are drawn in Section 5.

2. Device Details and Simulation Methods

The geometry of the GaN HEMT power amplifiers is shown in Figure 1a. The layer structure of GaN chip consists of an AlGaN barrier, a GaN buffer, an interface of a GaN/SiC, and a SiC substrates to improve calculation accuracy (Figure 1b). In addition, the chip is soldered to a CuMo heat sink with an AuSn joint for efficient thermal management. The length and width of heat sink are defined as twice the sizes of the chip, in order to avoid the effect of thermal simulation model of GaN HEMTs, which is affected by the large size ratio of chip and heat sink, and thus that the calculation accuracy is not affected when the length and width of heatsink are two times the size of chip in simulation model [12]. In order to estimate the relationships between channel temperatures and pulse width, gate structures, and power density of GaN amplifiers, the geometric and operating parameters are designed as Table 1. The active area is defined as the heat sources region of all gates determined by gate pitch spacing and total gate width (Figure 1c). The power density is an important index for the pulse operated device in product application, and it is determined by dividing the total power by total gate width, the total power defined as thermal dissipated power divided by power efficiency. The pulse period is the product of pulse width and its duty cycle. All the variables are shown in Table 1.

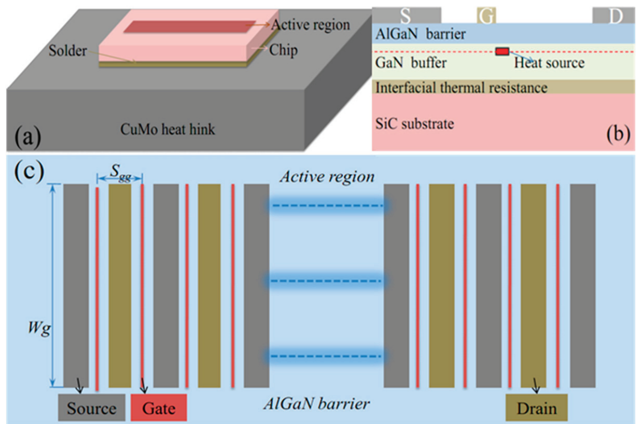

Figure 1. (**a**) Schematic diagram of the actual module for GaN amplifiers; (**b**) the cross section of chip; (**c**) the top active region.

Table 1. Geometric and working parameters of the designed device.

Definition	Value	Definition	Value
Length of chip	4000 μm	AlGaN barrier thickness	20 nm
Width of chip	860 μm	GaN buffer thickness	2.0 μm
Length of heat hink	8000 μm	SiC substrate thickness	80 μm
Width of heat hink	1720μm	Solder thickness	20 μm
Heat sink thickness	1000 μm	Pulse period	200 μs
Power efficiency	50%	Pulse width	Variables
Total power	2550 W	Power density, and gate pitch spacing	Variables
Active area of heat sources region	1.104 mm^2	Gate fingers, and gate width	Variables

The calculations are carried out by the three-dimensional finite element method with COMSOL multiphysics. Here, to improve the calculation accuracy, the nonlinear thermal conductivities of materials, operating conditions, and multilayer physical structures of GaN chip are considered and treated appropriately in our numerical analysis. For the nonlinear thermal conductivities of materials, temperature-dependent thermal conductivities of AlGaN, GaN, and SiC materials of near-junction region of GaN chip have been introduced into the model by employing Kirchhoff's transformation, with these thermal parameters of the device shown in Table 2 [3,12–15]. Operating conditions such as the thermal accumulation, the environmental issues around the GaN amplifier, and heat transfer of the CuMo heat hink are considered, the themo-electro effect is considered as the source of thermal accumulation. The natural convection is applied on the external surfaces of GaN amplifier, and the bottom of the heat sink is set as an isothermal surface plane with constant temperature of 333.15 K (ambient temperature). Meanwhile, this model takes into account the multilayer physical structure factors of the near-junction region, including details of AlGaN barrier, GaN buffer, interfacial layer of GaN/SiC and SiC substrate layers. However, it is challenging to introduce all these parameters simultaneously into the simulation model since it might cause some problems such as the size effect, huge amounts of simulation grid, and failure of convergence, especially for transient simulation.

Table 2. Thermal parameters used in the simulation.

Material	Thermal Conductivity (W/m·K)	Material	Thermal Conductivity (W/m·K)
AlGaN	$25 \times (T/300)^{-1.44}$	SiC	$387 \times (T/293)^{-1.49}$
GaN	$150 \times (T/300)^{-1.42}$	CuMo	167
AuSn	57	-	-
Interfacial thermal resistance		10 K·m^2/GW	

In this paper, some theoretical hypotheses are applied to solve the confliction relation between calculating precision and feasibility under transient simulation for pulse-operated AlGaN/GaN HEMT used in kilowatt-level power amplifiers. First, to avoid huge amounts of simulation grid and achieve feasibility of three-dimensional calculation, the themo-electro effect of GaN amplifier was simplified into heat sources of which the cross section of the model is illustrated in Figure 1b, and the heat sources represent the constant heat flux generated by dissipated power directly under the gates, and the length and width of cross section of heat sources is designed as 0.5 μm and 0.1 μm based on the size of gates of GaN chip (the length of gates is 0.25 μm). Second, to solve the size effect between the chip and the packaging, the gate/drain/source multi-layer metallization was omitted because of small-structural complexity effect [3,4,16]. And the AlGaN barrier material with the 20 nm thickness was supposed to a thin layer, the thin layer had only heat transfer characteristics. Meanwhile, the interface of GaN/SiC is a thick AlN nucleation layer with 20 nm thickness that involves intricate resistance mechanisms, including defects, dislocations, and interfacial disorders, these mechanisms seriously damage the thermal property, therefore heat spreading capacity of this interface of GaN/SiC was represented as a single effective interface thermal resistance in our model. Finally, to reduce the total computing time, only a quarter of device was simulated, because of their structural symmetry [3,12–21].

3. Simulation Results and Discussion

3.1. Transient Channel Temperature in Pulsed Operation

The analyses of transient channel temperature were carried out by the power density of 26.56 W/mm within four pulse repetition periods. A pulse width of 5 μs was used with the pulse period of 200 μs, and the values of gate pitch spacing, gate width and total gate width are 11.5 μm, 342.86 μm, and 96 mm, respectively. The first observation in Figure 2a is that the thermal response changes rapidly with the sudden power rise because of the Joule heating, the trend is that the channel temperature rises instantly at the start, and then continues to rise in approximate linearity with the increase of load power time throughout the ON-state portion. At the OFF-state, the channel temperature reduces immediately as power returns to 0 W, which drops to 25% temperature increment ($\Delta T_{\max}$ = maximal channel temperature—ambient temperature) when the time was 8.5 μs, then the channel temperature drops slowly until the next ON-state.

Meanwhile, as the inset Figure 2b presents, the thermal response is same in different pulse repetition periods, but the channel temperature is increased by the rise of pulse repetition period, particularly the maximal channel temperature is at the end of the pulse (ON-state) because of heat accumulating effect. The maximal channel temperatures are 289.7 °C, 296.2 °C, 299.5 °C, and 301.7 °C with the rise of pulse repetition period, respectively. The explanation is that thermophysical properties of chip materials will reduce because of the nonlinear thermal conductivities of materials, and this leads to the increase of heat accumulation with the rise of pulse repetition period. Meanwhile, the increment of maximal channel temperature is reduced from 6.5 K to 2.2 K, meaning that heat accumulating effect will gently reach saturation in the next several or longer pulse repetition periods, and the channel temperature will be balanced.

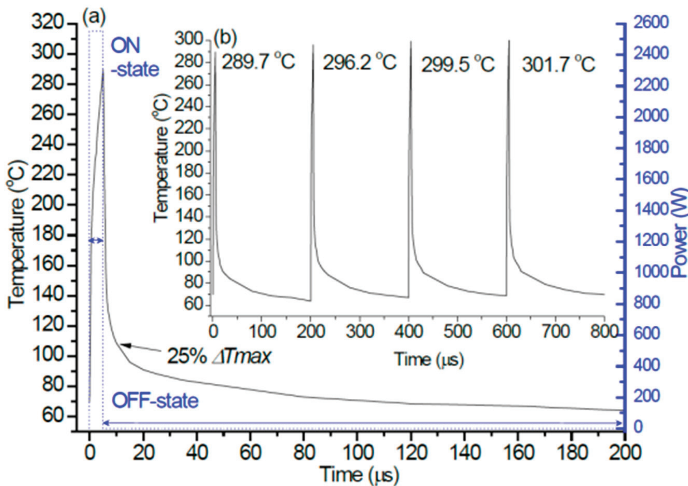

Figure 2. (**a**) Transient channel temperature with pulsed-mode power during one pulse period; (**b**) periodic transient pulses temperature

In addition, the temperature distribution under the time as 605 μs is shown in Figure 3, and the result shows that the heat mainly focuses on the region of active area. The paths of heat transfer are directly reflected in isothermal surfaces as shown in Figure 3 (magnification), and most of the heat is directly spread into SiC substrate through GaN buffer layer, then continued to transfer downward, and those heat ultimately gets extracted by the CuMo heat hink through the AuSn joint layer.

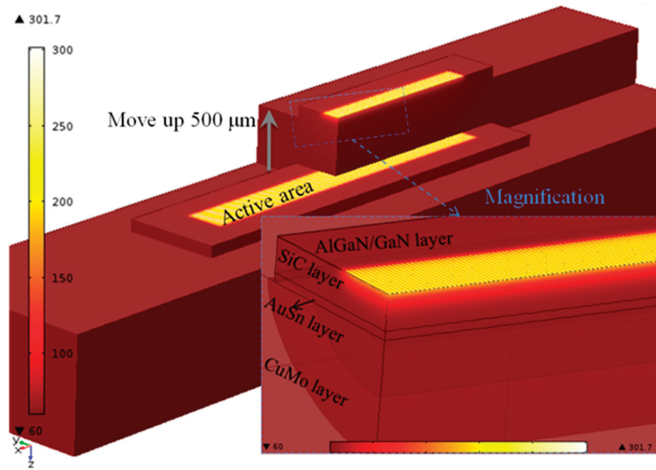

Figure 3. Temperature distribution and isothermal surfaces of device.

3.2. The Pulse Width Effect

Thermal investigation on pulse width was carried out by varying the pulse width from 1 μs to 9 μs at the pulse period of 200 μs, these values are based on the performance indicators of our GaN HEMT power amplifier in the practical application. The values of gate pitch spacing, gate width, and total gate width are 11.5 μm, 342.86 μm, and 96 mm, respectively, and the power density is 26.56 W/mm. The results indicate the channel temperatures are seriously affected by pulse width as shown in Figure 4a. Especially in the ON-state, it means load pulsed power time shown in Figure 2a, corresponding to 1 μs, 3 μs, 5 μs, 7 μs, and 9 μs respectively in Figure 4a, the trends of the channel temperatures of different pulse width have been essentially same in the load power time, and the channel temperature has been normalized to the maximal temperature increase at the end of the respective pulse, this means that the greater the pulse width the higher the maximal channel temperature. At the OFF-state, the channel temperatures reduce immediately, and the times ($t_{0.25}$) when the channel temperature drops to 25% temperature increment are 1.4 μs, 4.8 μs, 8.5 μs, 12 μs, and 15.5 μs, respectively. The cooling ratio of $t_{0.25}$ divided by the pulse width are 1.4, 1.6, 1.7, 1.7, and 1.7, respectively. This demonstrates that there exists a critical saturation for the cooling ratio with the increasing of the pulse width. It is noteworthy that the thermal impedance of device increases with the rise of pulse width shown in the inset Figure 4b, the relation between pulse width and duty cycle is also decided by the formula in the inset Figure 4b, and we find that this increase (ΔZ) of thermal impedance becomes smaller and presents nearly a linear approximation of the exponential function when the duty cycle is more than 2.5%. This suggests that the thermal impedance of device is relatively high sensitivity to duty cycle.

Meanwhile, the heat accumulating effect on the pulse width is analyzed, as shown in Figure 5, within four pulse repetition periods. The maximal channel temperatures were calculated in four pulse repetition periods with different duty cycles. Results indicate that there is almost no change (ΔT) of the maximal channel temperature in four pulse repetition periods when the duty cycle is 0.5%, but the change (ΔT) goes up sharply with the duty cycle increase, and the trend of the ΔT becomes small gradually as the pulse period going on. This demonstrates that the duty cycle has a larger impact on the heat accumulating effect for the device in pulsed operation, but an optimal duty cycle should exist for the contradiction between large duty cycle applications and little heat accumulating effect.

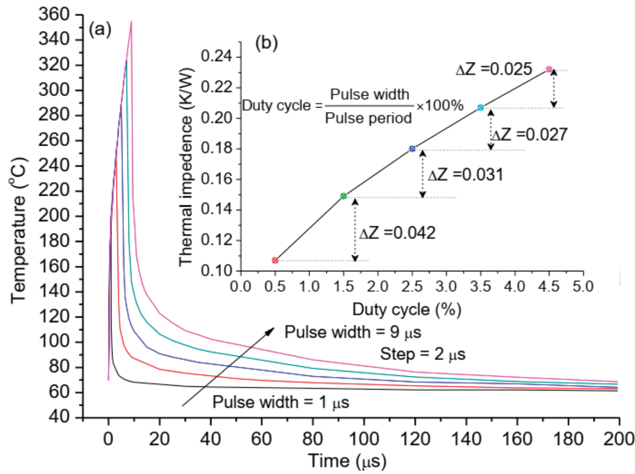

Figure 4. (**a**) Dependence of transient channel temperature on pulse width during one pulse period; (**b**) the impact of duty cycle on thermal impedance of device; the pulse width is 1 μs, 3 μs, 5 μs, 7 μs, and 9 μs, respectively, according to the duty cycle of 0.5%, 1.5%, 2.5%, 3.5%, and 4.5%.

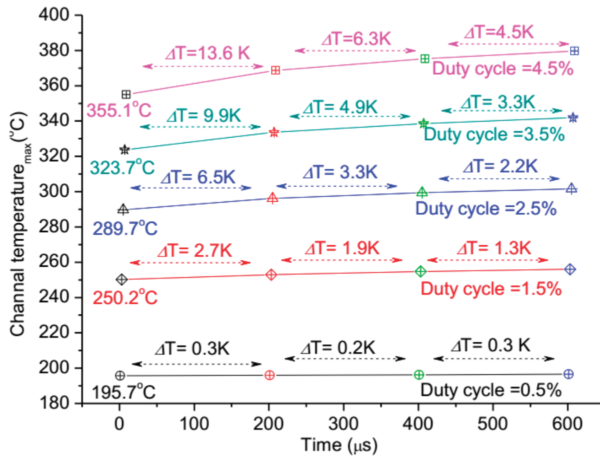

Figure 5. The impact of pulse width on maximal channel temperature during four pulse repetition periods.

3.3. The Gate Structures Effect

To consider the gate structures (the changes of gate width and gate fingers) effect, we keep the power density and pulse width as 26.56 W/mm and 5 μs respectively, meaning that the total gate width and gate pitch spacing is also a constant value which is 96 mm and 10 μm, respectively, and this represents that the length and width of active region is controlled when the active area of heat sources region is fixed. The thermal investigation on gate structures effect was carried out by varying the gate width (*Wg*) from 400 to 300 μm (Figure 6), and according to 240, 260, 280, 300, and 320 gate fingers (*Wn*), respectively. The results of transient simulation are shown Figure 6 in one pulse period (200 μs). We find that the trends of channel temperatures for all five gate structures are the same, and the channel temperature variations are the same in the over pulse period. This result indicates the changes of gate fingers and gate width have no effect on the channel temperature of the device when the total gate

width and active area is also a constant value, significantly, meaning that the surface profile of active area are free to control for thermal design of GaN HEMT device. This is very important for electric and thermal collaborative design of high power GaN device, and provides more space for electric design.

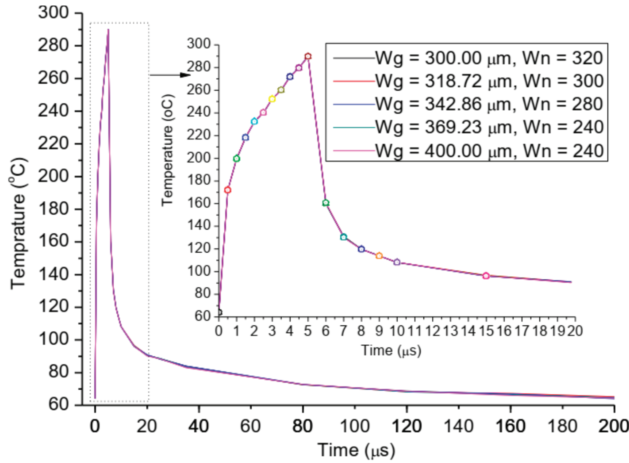

Figure 6. The relationships between transient channel temperature and the changes of the gate width and gate fingers, Wg is the width of a single gate, and Wn is the numbers of gate fingers.

3.4. The Power Density Effect

The change of power density means that the total gate width will change, because that they are interrelated when the total power and the active area of heat sources region are kept fixed at predetermined value in Table 1. The power densities are designed as 33.50 W/mm, 29.98 W/mm, 26.56 W/mm, 23.24 W/mm, and 19.58 W/mm, respectively, which correspond to the values of total gate width as 76.115 mm, 85.029 mm, 96.001 mm, 109.715 mm, 130.287 mm, respectively, and the gate pitch spacing (*Sgg*) are about 14.5 µm, 13 µm, 11.5 µm, 10 µm, and 8.5 µm, respectively, the gate width is fixed as 342.86 µm. The results, as shown in Figure 7, present that the trends of the influence on the channel temperature by the power density (*Pd*) are basically similar in one pulse period, but the degree of the influence increases greatly with the rise of power density throughout the ON-state portion. At the OFF-state, the channel temperatures reduce immediately in 0.5 µs as power returns to 0 W, and the values of channel temperatures in different power density are near when the time is more than 9 µs, but still the more the power density, higher the channel temperature.

Besides, the thermal impedance of device is analyzed, as shown in Figure 8, and we observe that the thermal impedance (Z_{th}) is a linear approximation of the exponential function with respect to the power density and the gate pitch spacing, and the linear fitting equation is: $Z_{th} = 0.062 + 0.0045 \times P_{\mathrm{d}}$. Results demonstrate that power density can extremely affect the channel temperature of the device when the total power, active area, and gate width are also constant values, meaning that we can reduce the channel temperature by the combined contribution of decreasing the power density and gate pitch spacing for the thermal design of GaN HEMT device.

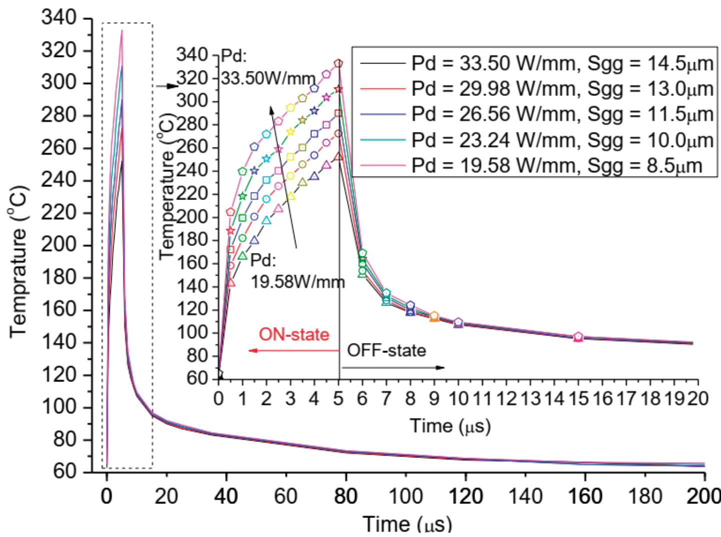

Figure 7. The relationships between transient channel temperature and the changes of power density and gate pitch spacing.

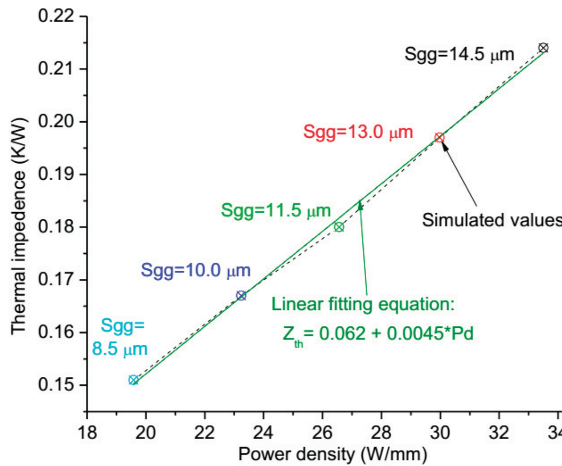

Figure 8. The impact of power density on thermal impedance of device.

4. Experimental Test

A GaN amplifier with kilowatt-level power has been designed based on the above thermal analysis, the power density and gate pitch spacing are designed as 19.58 W/mm and 8.5 μm in order to gain low channel temperature, when total power and active area of heat sources region are kept fixed at a predetermined value, as shown in Table 1. The value of gate width of single gate and total gate width is and 342.86 μm 130.287 mm, respectively. We have the IR thermal photogrammetry, and use the 15× infrared objective for high spatial resolution. The channel temperature of the GaN amplifier operated with a pulse width of 5 μs had been measured by the initial model of the infrared microscope. The transient thermal response and the test position of the GaN amplifier is shown in Figure 9, and the simulation of the GaN amplifier is shown in Figure 7. The experiment result shows that the maximal channel temperature is 202.19 °C, the experimental value is below the simulate value

(252.11 °C shown in Figure 7), around 80.19%. The deviation between calculated and tested data is about 20%, this is primarily due to the low temporal and spatial resolution, surface temperature of IR thermal photogrammetry, and the correctness and validation of the simulation model is demonstrated. Meanwhile, comparison of transient thermal response of the GaN amplifier under experiment and simulation shows that the trends of channel temperatures are basically similar in one pulse period. But, the experimental value of the maximal channel temperature has shown "style drift," meaning that the maximal channel temperature is not at the end of the pulse, mainly because of low resolution in time and surface temperature of IR thermal photogrammetry. The accuracy and precision in the microsecond range of temperature measurements is always a difficult subject in this field.

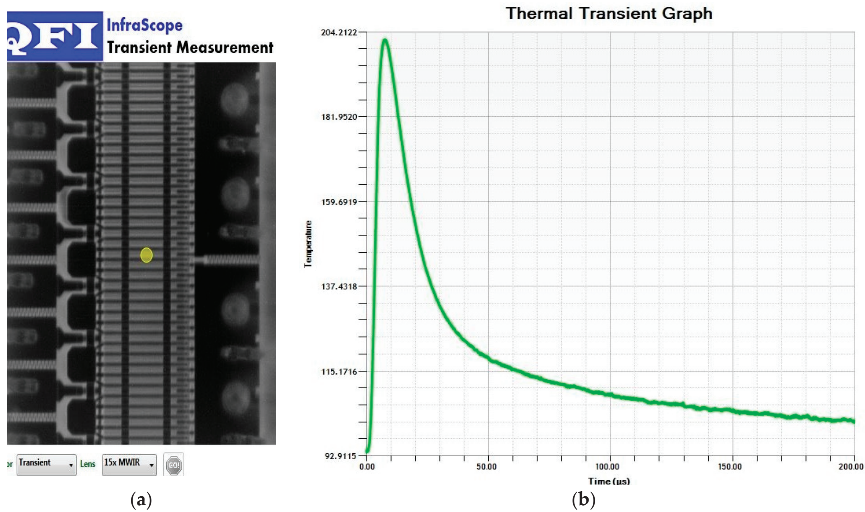

Figure 9. (**a**) The test position of GaN amplifier; (**b**) the transient thermal response of the GaN amplifier under 5 µs pulse width measured by IR thermal photogrammetry.

5. Conclusions

A theoretical transient thermal model based on the finite element analysis is presented to understand the relationships between the channel temperatures and pulse width, gate structures, and power density of GaN amplifiers operating at kilowatt-level power. Thermal response in pulsed operation indicates that the channel temperature sharply rises and goes up linearly until the end of pulse, while it reduces immediately within the tenth of the pulse width as power returns to 0 W at the OFF-state. In the meantime, the periodic transient pulse temperature and the temperature distribution are shown to be the reason of heat accumulating effect. The simulation results of pulse width effect show that the channel temperature rises with the increase of the duty cycle but in a decreasing trend, and there is an optimal duty cycle for heat accumulating effect in stable period pulses. Meanwhile, the power density shows certain influence on channel temperature, hence we can reduce the maximal channel temperature by the combined contribution of decreasing the power density and gate pitch spacing for the thermal design. Furthermore, when the total gate width and active area remain constant, note that the changes of gate fingers and gate width have no effect on the channel temperature when the total gate width and active area show constant values, therefore, the surface profile of active area are free to control for thermal design of GaN HEMT device. Finally, the correctness and validation of the simulation model are demonstrated by thermal test of IR photogrammetry.

Author Contributions: H.G. performed the research and wrote the paper. All authors contributed to the modeling, designing, thermal testing, and editing of the manuscript. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Amano, H.; Baines, Y.; Beam, E.; Borga, M.; Bouchet, T.; Chalker, P.R.; Charles, M.; Chen, K.J.; Chowdhury, N.; Chu, R.; et al. The 2018 GaN power electronics roadmap. *J. Phys. D Appl. Phys.* **2018**, *51*, 163001. [CrossRef]
2. Baczkowski, L.; Jacquet, J.C.; Jardel, O.; Gaquière, C.; Moreau, M.; Carisetti, D.; Brunel, L.; Vouzelaud, F.; Mancuso, Y. Thermal characterization using optical methods of AlGaN/GaN HEMTs on SiC substrate in RF operating conditions. *IEEE Trans. Electron Devices* **2015**, *62*, 3992–3998. [CrossRef]
3. Guo, H.; Kong, Y.; Chen, T. Thermal simulation of high power GaN-on-diamond substrates for HEMT applications. *Diam. Relat. Mater.* **2017**, *73*, 260–266. [CrossRef]
4. Michael, F.; Patrick, M.; Avram, B. Modeling thermal microspreading resistance in via arrays. *J. Electron. Packag.* **2016**, *138*, 010909.
5. Pavlidis, G.; Pavlidis, G.; Heller, E.R.; Moore, E.A.; Vetury, R.; Graham, S. Characterization of AlGaN/GaN HEMTs using gate resistance thermometry. *IEEE Trans. Electron Devices* **2017**, *64*, 78–83. [CrossRef]
6. Chou, H.P.; Cheng, S.; Cheng, C.H.; Chuang, C.W. Thermal behavior investigation of cascode GaN HEMTs. In Proceedings of the 3rd International Conference on Industrial Application Engineering, Kitayushu, Japan, 28–31 March 2015.
7. Nigam, A.; Bhat, T.N.; Rajamani, S.; Dolmanan, S.B.; Tripathy, S.; Kumar, M. Effect of self-heating on electrical characteristics of AlGaN/GaN HEMT on Si (111) substrate. *AIP Adv.* **2017**, *7*, 085015. [CrossRef]
8. Jones, J.P.; Heller, E.; Dorsey, D.; Graham, S. Transient stress characterization of AlGaN/GaN HEMTs due to electrical and thermal effects. *Microelectron. Reliab.* **2015**, *55*, 2634–2639. [CrossRef]
9. Ishizaki, T.; Yanase, M.; Kuno, A.; Satoh, T.; Usui, M.; Osawa, F.; Yamada, Y. Thermal simulation of joints with high thermal conductivities for power electronic devices. *Microelectron. Reliab.* **2015**, *55*, 1060–1066. [CrossRef]
10. Asubar, J.T.; Yatabe, Z.; Hashizume, T. Reduced thermal resistance in AlGaN/GaN multi-mesa-channel high electron mobility transistors. *Appl. Phys. Lett.* **2014**, *105*, 053510. [CrossRef]
11. Darwish, A.; Bayba, A.J.; Hung, H.A. Channel temperature analysis of GaN HEMTs with nonlinear thermal conductivity. *IEEE Trans. Electron Devices* **2015**, *62*, 840–846. [CrossRef]
12. Schwitter, B.K.; Parker, A.E.; Mahon, S.J.; Fattorini, A.P.; Heimlich, M.C. Impact of bias and device structure on gate junction temperature in AlGaN/GaN-on-Si HEMTs. *IEEE Trans. Electron Devices* **2014**, *61*, 1327–1334. [CrossRef]
13. Bertoluzza, F.; Delmonte, N.; Menozzi, R. Three-dimensional finite element thermal simulation of GaN-based HEMTs. *Microelectron. Reliab.* **2009**, *49*, 468–473. [CrossRef]
14. Chen, X.P.; Donmezer, F.N.; Kumar, S.; Graham, S. A numerical study on comparing the active and passive cooling of AlGaN/GaN HEMTs. *IEEE Trans. Electron Devices* **2014**, *61*, 4056–4061. [CrossRef]
15. Wang, A.; Tadjer, M.J.; Anderson, T.J.; Baranyai, R.; Pomeroy, J.W.; Feygelson, T.I.; Hobart, K.D.; Pate, B.B.; Calle, F. Impact of intrinsic stress in diamond capping layers on the electrical behavior of AlGaN/GaN HEMTs. *IEEE Trans. Electron Devices* **2013**, *60*, 3149–3156. [CrossRef]
16. Guo, H.; Han, P.; Chen, T. Study of thermal simulation technology for GaN power device. *Res. Prog. SSE* **2017**, *37*, 176–181.
17. Agarwal, G.; Kazior, T.; Kenny, T.; Weinstein, D. Modeling and analysis for thermal management in gallium nitride HEMTs using microfluidic cooling. *J. Electron. Packag.* **2017**, *139*, 1–11. [CrossRef]
18. Heller, E.; Crespo, A. Electro-thermal modeling of multifinger AlGaN/GaN HEMT device operation including thermal substrate effects. *Microelectron. Reliab.* **2013**, *75*, 45–50. [CrossRef]
19. Donmezer, N.; Islam, M.; Yoder, P.D. The impact of nongray thermal transport on the temperature of AlGaN/GaN HFETs. *IEEE Trans. Electron Devices* **2015**, *62*, 2437–2444. [CrossRef]

20. García, S.; Torre, I.; Mateos, J.; González, T.; Pérez, S. Impact of substrate and thermal boundary resistance on the performance of AlGaN/GaN HEMTs analyzed by means of electro-thermal Monte Carlo simulations. *Semicond. Sci. Technol.* **2016**, *31*, 065005. [CrossRef]
21. Denu, G.A.; Mirani, J.H.; Fu, J. FEM thermal analysis of Cu/diamond/Cu and diamond/SiC heat spreaders. *AIP Adv.* **2017**, *7*, 035102. [CrossRef]

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Improved MRD 4H-SiC MESFET with High Power Added Efficiency

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Abstract: An improved multi-recessed double-recessed p-buffer layer 4H–SiC metal semiconductor field effect transistor (IMRD 4H-SiC MESFET) with high power added efficiency is proposed and studied by co-simulation of advanced design system (ADS) and technology computer aided design (TCAD) Sentaurus software in this paper. Based on multi-recessed double-recessed p-buffer layer 4H–SiC metal semiconductor field effect transistor (MRD 4H-SiC MESFET), the recessed area of MRD MESFET on both sides of the gate is optimized, the direct current (DC), radio frequency (RF) parameters and efficiency of the device is balanced, and the IMRD MESFET with a best power-added efficiency (PAE) is finally obtained. The results show that the PAE of the IMRD MESFET is 68.33%, which is 28.66% higher than the MRD MESFET, and DC and RF performance have not dropped significantly. Compared with the MRD MESFET, the IMRD MESFET has a broader prospect in the field of microwave radio frequency.

Keywords: 4H-SiC; MESFET; IMRD structure; power added efficiency

1. Introduction

Nowadays, as the device size continues to decrease, the process difficulty increases significantly, both the power consumption and non-ideal effects are significant. The first-generation semiconductor Si and other materials are close to their theoretical limits in performance, while 4H Silicon Carbide (4H-SiC) has a wide band gap (3.26 eV), high thermal conductivity (4.9 W/(cm·K)), high breakdown electric field (4 MV/cm) and low dielectric constant (9.7), high electron saturation drift speed (2.7×10^7 cm/s), and exhibits superior performance compared to 3C-SiC, 6H-SiC, Si, GaAs, and so on. Based on the excellent characteristics of 4H-SiC, 4H-SiC metal semiconductor field transistors (4H-SiC MESFETs) are expected to be applied to various semiconductor fields [1–3]. However, current research on 4H-SiC MESFET mainly includes breakdown voltage, saturation drain current, electron saturation drift speed, frequency characteristics etc. [4–10]. There are a variety of ways to improve device performance, such as the use of double-recessed gates [4], recessed buffers and diffusion regions [5,6], doping distribution modification [7,8], silicon-on-insulator (SOI) technology [9,10] and so on, which can significantly improve device performance. At the same time, there is little research on efficiency [11,12]. For non-conventional 4H-SiC-based FETs, the characteristics of the device can be studied using numerical simulations [13–17].

In this paper, we reported a 4H-SiC MESFET with improved multi-recessed double-recessed p-buffer layer (IMRD) structure. Traditional 4H-SiC MESFETs have been experimentally verified. Many experimental results have been reported so far [18,19], but they are all fixed structures, and the effect of structural parameters on the results has not been studied. Based on multi-recessed 4H–SiC MESFETs with double-recessed p-buffer layer (MRD 4H-SiC MESFET) [20], we adopt a new design method optimized by technology computer aided design (TCAD) simulation and verified in advanced design system (ADS) software. The IMRD MESFET has both the excellent performance of MRD MESFET and

better power-added efficiency (PAE) and provides a new idea for high-power operational amplifier design at the device level.

2. Device Structure and Description

Figure 1a,b are the cross-sectional views of the MRD MESFET and the IMRD MESFET, respectively. In Figure 1a, the MRD MESFET contains a high-purity semi-insulating substrate (SI-Substrate), a p-type buffer layer (P-Buffer), an n-type channel layer (N-Channel), and two doped n-type cap layers (Source and Drain), the Nickel Schottky gate has a work function of 5.1 eV. By high energy ion implantation and high temperature annealing processes, two recessed areas are formed on both sides of the gate. The main difference between the two devices is the recessed regions on both sides of the gate. The length and width on both sides are L_1 = 0.15 μm, L_2 = 0.2 μm, H_1 = 0.1 μm and H_2 = 0.1 μm, other parameters are shown in Table 1. In the optimized IMRD MESFET, L_1 = 0.5 μm, L_2 = 0.2 μm, H_1 = 0.15 μm and H_2 = 0.2 μm, and the other parameters are consistent with the MRD MESFET.

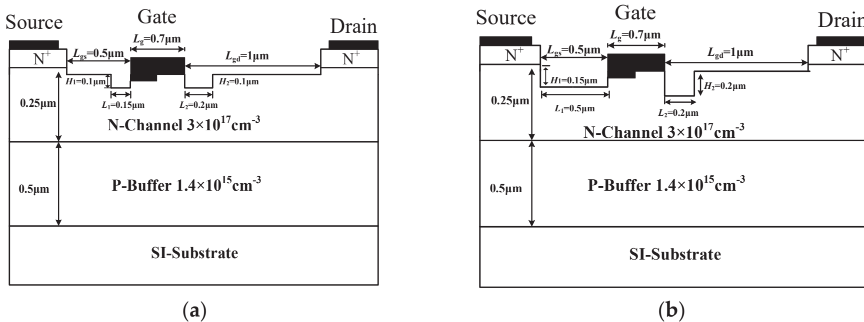

Figure 1. Schematic cross sections of the (**a**) MRD 4H-SiC metal semiconductor field effect transistor (MESFET), (**b**) improved multi-recessed double-recessed p-buffer layer (IMRD) 4H-SiC MESFET.

Table 1. Common parameters of the two structures.

Parameters	Values
P-Buffer Concentration	1.4×10^{15} cm^{-3}
N-Channel Concentration	3×10^{17} cm^{-3}
N-Cap layers Concentration	2×10^{19} cm^{-3}
L_{gs}	0.5 μm
L_{gd}	1.0 μm
L_s	0.5 μm
L_d	0.5 μm
L_g	0.7 μm
N-Channel Thickness	0.25 μm
P-Buffer Thickness	0.5 μm
Device Area (without SI-Substrate)	1 μm × 3.5 μm

The 2D TCAD simulator, Sentaurus is used in this paper. The simulation temperature is set to 300 K. A 5.1 eV Nickel Schottky gate work function is applied. The main model used in the simulation are Mobility (Enormal Doping Dep HighFieldsaturation (GradQuasiFermi)), Recombination (Auger SRH (DopingDep)), Incomplete Ionization, Effective Intrinsic and Density (BandGapNarrowing (OldSlotboom)) [21]. The interface state has a great impact on the device, in this paper, the gate of the two devices are formed by a metal-to-SiC contact to form a Schottky contact, so the gate does not have to consider the interface state. When the MESFET is passivated with a material such as Si_3N_4 or SiO_2, the performance is slightly degraded. When verifying the conventional 4H-SiC MESFET, Si_3N_4 was used as the passivation layer. When Si_3N_4 is used as the passivation layer, the device performance is

reduced by less than SiO_2 [22,23]. As a theoretical analysis, the influence of passivation on the device is not considered here. After obtaining the simulation results, the obtained model parameters are used in the ADS software to measure the PAE of the two devices. In the ADS simulation, the bias conditions of the device are shown in Figure 2. Direct current (DC) voltage Vg1 is −3.5 V, Vdd is 28 V, input power Pavs is 24 dBm, and frequency f is 1.2 GHz.

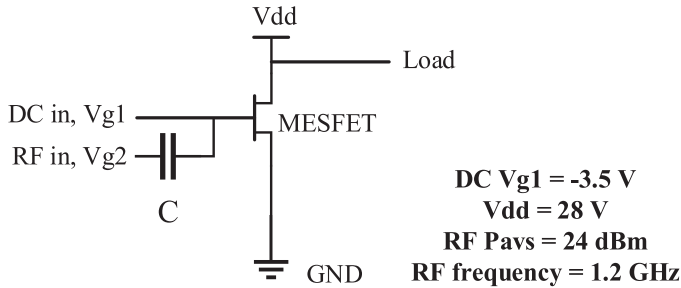

Figure 2. One Tone Load Pull Schematic for power-added efficiency (PAE) measurements.

3. Results and Discussion

3.1. Effect of the Length and Height of the Recessed Regions on the PAE

The effect of the length and height of the recessed regions on PAE is shown in Figure 3. When a parameter changes, the remaining parameters are the default values in Figure 1a. We can see in Figure 3a, when L_1 increases, PAE also increases. When L_1 reaches 0.5 μm, PAE reaches a maximum value; when L_2 is less than 0.1 μm, the PAE increases with L_2. When L_2 reaches 0.2 um, PAE reaches a maximum value. When L_2 is larger than 0.1 μm, PAE decreases with the increase of L_2. In Figure 3b, the trend of the effect of H_1 and H_2 on PAE agrees well. When H_1 and H_2 are less than 0.2 μm, PAE of H_1 and H_2 increase with the increase of H_1 and H_2. When H_1 and H_2 reach 0.2 μm, PAE of H_1 and H_2 reach the maximum value. When H_1 and H_2 are larger than 0.2 μm, PAE of H_1 and H_2 decrease as H_1 and H_2 increases.

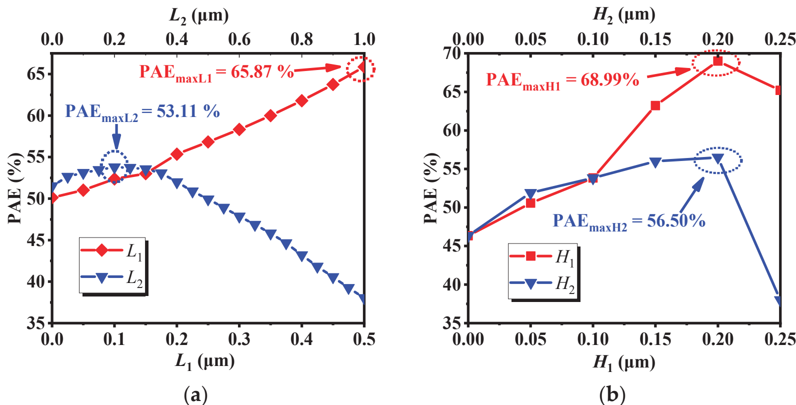

Figure 3. The effect of the (**a**) length and (**b**) height on PAE.

3.2. Optimized Results and Mechanism Discussion

Through further analysis of the results obtained in 3.1, we found that between L_1, L_2, H_1 and H_2 there is a relatively independent relationship. When L_2, H_1 and H_2 take different values, the trend of PAE with L_1 is almost the same as Figure 3a. The maximum value of PAE is found in L_1 = 0.5 μm.

In addition, for L_2, H_1 and H_2, the maximum value of PAE are found in L_2 = 0.2 µm, H_1 = 0.2 µm and H_2 = 0.2 µm. Based on the above results, L_1 = 0.5 µm, L_2 = 0.2 µm, H_1 = 0.2 µm and H_2 = 0.2 µm were selected as the optimal structural parameters, and the optimized device was obtained. The main parameters of the device are shown in Table 2. It can be seen from the table that although its saturated drain current I_{dsat} is too small, which is 35.2% lower than that of the MRD MESFET, and the DC characteristics are greatly weakened, its PAE reaches 70.85%, which is 33.40% higher than that of the MRD MESFET.

Table 2. Comparison of performance parameters of the two structures.

Parameters	MRD MESFET	IMRD MESFET
I_{dsat} (mA/mm)	358.97	233.02
g_m (mS/mm)	73.45	56.37
V_t (V)	−5.81	−6.89
C_{gs} (pF/mm)	0.128	0.13
C_{gd} (pF/mm)	0.39	0.02
Power-added efficiency (PAE) (%)	53.11	70.85

Figure 4 shows the effect of the length and height on I_{dsat}. It can be seen from Figure 4a that when L_1 = 0.5 µm and L_2 = 0.2 µm, the decline of I_{dsat} is small; In Figure 4b, it can be clearly seen that when H_1 is less than 0.15 µm, I_{dsat} decreases, but the value of decrease is not very large. When H_1 is greater than 0.15 µm, I_{dsat} drops sharply. Similarly, for H_2, when H_2 is less than 0.2 µm, the decrease of I_{dsat} is not large. When H_2 is larger than 0.2 µm, the decline of I_{dsat} is more obvious. The main cause of the weakening of the DC characteristics is that the thickness of the channel region becomes extremely thin, resulting in narrowing the channel of most electrons, and thus the DC characteristics are deteriorated. Based on the results above, L_1 = 0.5 µm, L_2 = 0.2 µm, H_1 = 0.15 µm and H_2 = 0.2 µm were selected as structural parameters, and the PAE was measured to be 68.33%. After optimization, the PAE of the IMRD MESFET is 28.66% higher than that of the MRD MESFET.

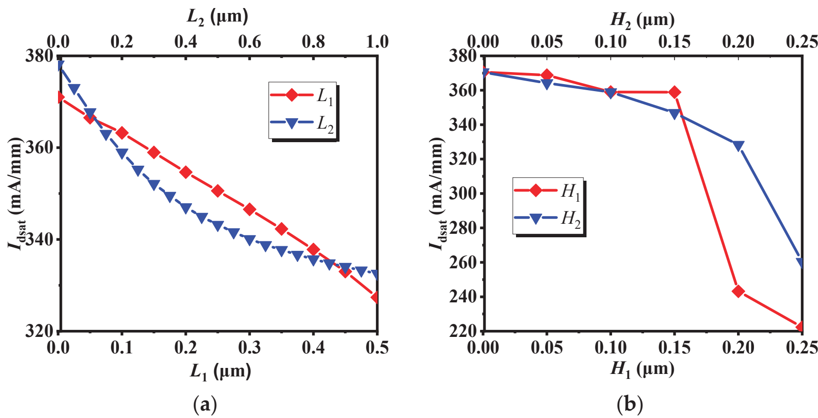

Figure 4. The effect of the (**a**) length and (**b**) height on I_{dsat}.

Figure 5 illustrates the effect of recessed region parameters (L & H) on V_t, Gm_{max}, C_{gs} and C_{gd}, the transconductance Gm_{max}, its physical meaning is the first-order partial conductance of the output drain current and the input voltage, C_{gs} is the gate-source capacitance, and C_{gd} is the gate-drain capacitance. In combination with Figure 3, it can be seen from Figure 5a,c,e that as L_1 increases, the threshold voltage V_t, the transconductance Gm_{max}, the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} decrease, but the PAE gradually increases; when L_2 increases, V_t increases first, then tends to be stationary, Gm_{max} gradually decreases, the change trend of C_{gd} and C_{gs} are about

the same. When L_2 is less than 0.1 μm, the changes of C_{gs} and C_{gd} are relatively stable. When L_2 is larger than 0.1 μm, C_{gs} and C_{gd} are gradually increased. Combined with Figures 3a and 5a,c,e, it can be found that the effects of C_{gs} and C_{gd} on PAE are obvious. It can be seen from the bias conditions of Figure 2 that C_{gs} and C_{gd} affect the input impedance and output impedance respectively, and the power consumed by the capacitor is proportional to the size of the capacitor. According to the definition of PAE, these two capacitors affect the input power and output power, so these two capacitors have a greater impact on the PAE. Similarly, in conjunction with Figure 3, it can be seen from Figure 5b,d,f that, when H_1 is less than 0.2 μm, as H_1 increases, V_t, Gm_{max}, C_{gs} and C_{gd} decrease, while PAE increases. When H_1 is larger than 0.2 μm, PAE decreases with H_1. For H_2, when H_2 increases gradually, V_t and Gm_{max} also decrease gradually, but when H_2 is less than 0.05 μm, C_{gs} and C_{gd} decrease with increasing H_2. When H_2 is greater than 0.05 μm, the change of C_{gs} and C_{gd} are relatively stable. When H_2 is less than 0.2 μm, PAE increases with the increase of H_2. When H_2 is greater than 0.2 μm, PAE decreases as H_2 increases. Combined with Figures 3b, 4b and 5b,d,f, although the capacitances C_{gs} and C_{gd} have a greater influence on PAE, as the H_2 increases, the conductive channel of the device still decreases. When the thickness of the conductive channel is less than 0.05 μm, the conductive channel is extremely thin, and its conductive properties are greatly weakened. At this time, both the AC signal and the DC signal will be greatly attenuated in the channel, resulting in a decrease in output power. Under the combined action of several factors, the PAE decreases as H_2 increases.

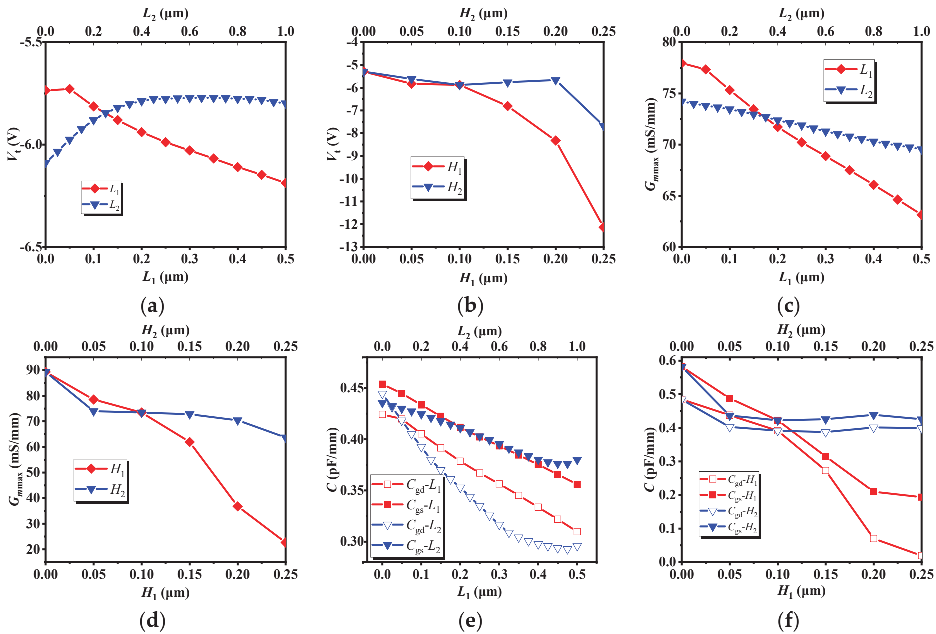

Figure 5. The effect of recessed region parameters on V_t, Gm_{max} and C_{gs}. (**a**) V_t-*L*. (**b**) V_t-*H*. (**c**) Gm_{max}-*L*. (**d**) Gm_{max}-*H*. (**e**) *C*-*L*. (**f**) *C*-*H*.

The power-added efficiency (PAE) is the difference in output and input power in place of radio frequency (RF) output power in the drain efficiency equation, which takes power gain G_p into account.

$$\mathrm{PAE} = \frac{P_{out} - P_{in}}{P_{dc}} = \eta_c(1 - \frac{1}{G_p}) \quad (1)$$

η_c is the drain efficiency and represents the ratio of output power to DC input power. In order to obtain a higher PAE, a larger power gain G_p is required. It can be seen from the equivalent circuit

diagram of the device, the size of the PAE is determined by these parameters together. For the threshold voltage V_t, only when the absolute value of V_t is reduced, can small voltage make the channel turn on. When the input voltage is constant, the smaller the absolute value of the threshold voltage is, the larger the channel current is, and the larger the output power P_{out} is, so that the PAE becomes larger. When Gm_{max} is reduced, its DC characteristic will also decrease. Since the input voltage is constant, the decrease of Gm_{max} causes the bias current I_d to decrease, so that the P_{dc} is reduced, according to the definition of PAE, the decrease of P_{dc} will cause the increase of PAE. The gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} have a greater influence on the PAE, in the equivalent circuit, C_{gs} and C_{gd} are in the input loop and output loop respectively. Because of the larger C_{gs} in the bias, the more AC input energy it consumes, the larger the C_{gd}, the smaller the AC output power of the load is. In addition, as the channel becomes thinner and thinner, it affects both the capacitance and the carrier's passage through the channel region. Although the PAE increases as the capacitance decreases, the extremely thin channel also makes the DC and AC characteristics affected seriously. From the analysis of 3.1–3.3, when the structural parameters of the device are changed, in order to obtain the optimal PAE, it is necessary to weigh the various parameters and find the optimal structural parameters on the premise that the other performance is guaranteed. Perhaps the above design process will sacrifice a small part of the performance, but the efficiency is greatly improved, achieving energy saving and emission reduction, which is very beneficial to the construction of green earth.

4. Conclusions

An improved MRD 4H-SiC MESFET with high power added efficiency is analyzed and studied by co-simulation of ADS and TCAD Sentaurus software in this paper. Based on MRD 4H-SiC MESFET, we optimize the MRD MESFET on both sides of the gate. In the recessed area, the DC, RF parameters and efficiency of the device are weighed, and the IMRD MESFET with the best PAE is finally obtained. The results show that the saturation drain current Idsat of the IMRD MESFET is 311 mA, the threshold voltage V_t is −6.99 V, the maximum transconductance Gm_{max} is 46.37 mS, the gate-source capacitance C_{gs} is 0.218 pF, and the gate-drain capacitance C_{gd} is 17.9 fF. The PAE is 68.33%, which is 28.66% higher than the MRD MESFET, and DC and RF performance have not dropped significantly. This paper proposes to lay a device-level theoretical basis and design method for further energy-efficient RF power amplifier.

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References

1. Murugapandiyan, P.; Ravimaran, S.; William, J. DC and microwave characteristics of Lg 50 nm T-gate InAlN/AlN/GaN HEMT for future high power RF applications. *AEU Int. J. Electron. Commun.* **2017**, *31*, 163–168. [CrossRef]
2. Prasad, D.A.; Komaragiri, R. Performance comparison of 4H-SiC MESFETs. In Proceedings of the 2013 Annual International Conference Emerging Research Areas and 2013 International Conference on Microelectronics, Communications and Renewable Energy (AICERA/ICMiCR), Kanjirapally, India, 4–6 June 2013; pp. 1–5.
3. Kesilmis, Z.; Avc, M.; Aksoy, M. *An Operational Transconductance Amplifier with 45 nm FINFET Technology*; CiteSeerX Scientific Literature Digital Library, Penn State University's School of Information Sciences and Technology: University Park, PA, USA, 2011.
4. Zhu, C.L.; Tin, C.C.; Zhang, G.H.; Yoon, S.F.; Ahn, J. Improved performance of SiC MESFETs using double-recessed structure. *Microelectron. Eng.* **2006**, *83*, 92–95. [CrossRef]
5. Jia, H.; Ma, P.; Luo, Y.; Yang, Z.; Wang, Z.; Wu, Q.; Hu, M. A novel 4H-SiC MESFET with double upper gate and recessed p-buffer. *Superlattices Microstruct.* **2016**, *97*, 346–352. [CrossRef]

6. Orouji, A.A.; Shahnazarisani, H.; Anvarifard, M.K. Simulation analysis of a novel dualtrench structure for a high power silicon-on-insulator metal–semiconductor field effect transistor. *Mater. Sci. Semicond. Process.* **2014**, *31*, 506–511. [CrossRef]
7. Aminbeidokhti, A.; Orouji, A.A. A novel 4H-SiC MESFET with modified channel depletion region for high power and high frequency applications. *Phys. E Low Dimens. Syst. Nanostruct.* **2011**, *44*, 708–713. [CrossRef]
8. Moghadam, H.A.; Orouji, A.A.; Mahabadi, S.E.J. Employing reduced surface field technique by a P-type region in 4H-SiC metal semiconductor field effect transistors for increasing breakdown voltage. *Int. J. Numer. Model. Electron. Netw. Devices Fields* **2013**, *26*, 103–111. [CrossRef]
9. Naderi, A.; Heirani, F. A novel SOI-MESFET with symmetrical oxide boxes at both sides of gate and extended drift region into the buried oxide. *AEU Int. J. Electron. Commun.* **2018**, *85*, 91–98. [CrossRef]
10. Mohammadi, H.; Naderi, A. A Novel SOI-MESFET with Parallel Oxide-Metal Layers for High Voltage and Radio Frequency Applications. *AEU Int. J. Electron. Commun.* **2017**, *83*, 541–548. [CrossRef]
11. Jia, H.; Hu, M.; Zhu, S. An Improved UU-MESFET with High Power Added Efficiency. *Micromachines* **2018**, *9*, 573. [CrossRef] [PubMed]
12. Jia, H.; Zhu, S.; Hu, M.; Tong, Y.; Li, T.; Yang, Y. An improved DRBL AlGaN/GaN HEMT with high power added efficiency. *Mater. Sci. Semicond. Process.* **2019**, *89*, 212–215. [CrossRef]
13. Singh, J.; Kumar, M.J. A Planar Junctionless FET Using SiC With Reduced Impact of Interface Traps: Proposal and Analysis. *IEEE Trans. Electron Devices* **2017**, *64*, 4430–4434. [CrossRef]
14. Della Corte, F.G.; Pezzimenti, F.; Bellone, S.; Nipoti, R. Numerical simulations of a 4H-SiC BMFET power transistor with normally-off characteristics. *Mater. Sci. Forum* **2011**, *679*, 621–624. [CrossRef]
15. Lien, W.C.; Damrongplasit, N.; Paredes, J.H.; Senesky, D.G.; Liu, T.J.K.; Pisano, A.P. 4H-SiC N-Channel JFET for Operation in High-Temperature Environments. *IEEE J. Electron Devices Soc.* **2014**, *2*, 164–167. [CrossRef]
16. Pezzimenti, F. Modeling of the steady state and switching characteristics of a normally-off 4H-SiC trench bipolar-mode FET. *IEEE Trans. Electron Devices* **2013**, *60*, 1404–1411. [CrossRef]
17. Jaikumar, M.G.; Karmalkar, S. Calibration of Mobility and Interface Trap Parameters for High Temperature TCAD Simulation of 4H-SiC VDMOSFETs. *Mater. Sci. Forum* **2012**, *717*, 1101–1104. [CrossRef]
18. Chen, Z.; Deng, X.; Luo, X.; Zhang, B.; Li, Z. Improved Characteristics of 4H-SiC MESFET with Multi-recessed Drift Region. In Proceeding of the 2007 International Workshop on Electron Devices & Semiconductor Technology, Beijing, China, 3–4 June 2007.
19. Elahipanah, H. Record gain at 3.1 ghz of 4h-sic high power rf mesfet. *Microelectron. J.* **2011**, *42*, 299–304. [CrossRef]
20. Jia, H.; Pei, X.; Sun, Z.; Zhang, H. Improved performance of 4H-silicon carbide metal semiconductor field effect transistors with multi-recessed source/drain drift regions. *Mater. Sci. Semicond. Process.* **2015**, *31*, 240–244. [CrossRef]
21. *Sentaurus Device User Guide*, version L-2016.03; Synopsys Inc.: Mountain View, CA, USA, 2016.
22. Tenedorio, J.G.; Terzian, P.A. Effects of Si_3N_4, SiO, and polyimide surface passivations on gaas mesfet amplifier RF stability. *IEEE Electron Device Lett.* **1984**, *5*, 199–202. [CrossRef]
23. Charache, G.W.; Akram, S.; Maby, E.W.; Bhat, I.B. Surface passivation of gaas mesfets. *IEEE Trans. Electron Devices* **1997**, *44*, 1837–1842. [CrossRef]

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Novel High-Energy-Efficiency AlGaN/GaN HEMT with High Gate and Multi-Recessed Buffer

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Abstract: A novel AlGaN/GaN high-electron-mobility transistor (HEMT) with a high gate and a multi-recessed buffer (HGMRB) for high-energy-efficiency applications is proposed, and the mechanism of the device is investigated using technology computer aided design (TCAD) Sentaurus and advanced design system (ADS) simulations. The gate of the new structure is 5 nm higher than the barrier layer, and the buffer layer has two recessed regions in the buffer layer. The TCAD simulation results show that the maximum drain saturation current and transconductance of the HGMRB HEMT decreases slightly, but the breakdown voltage increases by 16.7%, while the gate-to-source capacitance decreases by 17%. The new structure has a better gain than the conventional HEMT. In radio frequency (RF) simulation, the results show that the HGMRB HEMT has 90.8%, 89.3%, and 84.4% power-added efficiency (PAE) at 600 MHz, 1.2 GHz, and 2.4 GHz, respectively, which ensures a large output power density. Overall, the results show that the HGMRB HEMT is a better prospect for high energy efficiency than the conventional HEMT.

Keywords: GaN; HEMT; high gate; multi-recessed buffer; power density; power-added efficiency

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1. Introduction

Wide-bandgap semiconductor materials exhibit many attractive properties far beyond the capabilities of silicon, such as high critical breakdown electric field strength, carrier drift velocity, high thermal conductivity, and large carrier mobility. Therefore, power electronic devices based on wide-bandgap semiconductor materials such as diamond, silicon carbide (SiC), and gallium nitride (GaN) will have higher resistance to high voltages, and lower on-resistance and radiation resistance than silicon devices [1–4]. Recently, GaN devices became a research hotspot of high-frequency and high-power devices and systems with its large forbidden band width, high electron saturation speed, high breakdown voltage, and anti-irradiation [5–9]. The wide-bandgap semiconductor device GaN high-electron-mobility transistor (GaN HEMT) has the advantages of high frequency, high power density, high withstand voltage, and high efficiency; thus, it is used in civil communication, Internet of things, petroleum exploration, aerospace, and so on [10,11]. However, traditional GaN HEMTs are unable to meet the current demand. At present, most research on GaN HEMTs is based on peripheral circuits to regulate and compensate transistors to achieve better output characteristics [12]. However, such designs often lead to shortcomings such as poor transistor withstand voltage, large parasitic capacitance, and a narrow transconductance saturation region, which have a great influence on important performance parameters such as output power and power-added efficiency of the device.

Based on the conventional GaN HEMT, a novel AlGaN/GaN HEMT with a high gate and a multi-recessed buffer (HGMRB HEMT) is proposed in this paper for high-energy-efficiency applications. Compared with its conventional counterpart, the high gate and multi-recessed buffer structure changes the electric field distribution, the gate source capacitance, and the transconductance parameters of the HEMT.

2. Device Structure and Description

Figure 1 shows the device structure of the conventional HEMT (a) and the HGMRB HEMT (b). The source and drain of both devices are N^+ heavily doped with a doping concentration of 1×10^{20} cm^{-3} and have the same 40 nm AlN nuclear layer and SiC substrate layer with a lateral width of 6.5 µm. The self-heating effect is one of the main reasons for restricting GaN devices. It not only affects the output power, but also affects the reliability of the device. Many methods for reducing the self-heating effect were reported, such as changing the substrate material [13,14]. In this paper, SiC is used as the substrate, which greatly reduces the self-heating effect. Compared with the conventional HEMT, the barrier region of the proposed HGMRB HEMT is 5 nm lower than the source, drain, and gate electrodes, forming a high gate. The barrier region between the source/drain and the high gate has a height of 20 nm. The buffer layer height of both devices is 3 µm. The buffer layer of the HGMRB HEMT forms two left and right recessed regions. The widths of the recessed regions are 0.5 µm and 1.5 µm, respectively, and the depth is 4 nm.

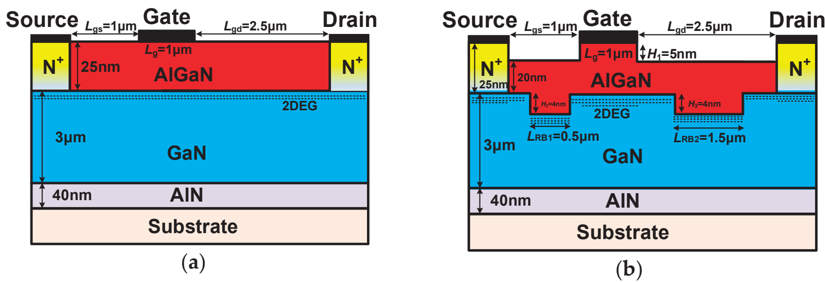


Figure 1. Schematic cross sections of the (**a**) conventional high-electron-mobility transistor (HEMT), and (**b**) proposed HEMT with a high gate and a multi-recessed buffer (HGMRB).

In the proposed new structure, the distribution of the electric field can reduce the electric field peak at the edge of the gate electrode and reduce the electron injection effect near the gate, and the current collapse effect can be alleviated. Therefore, the effect of surface state on device performance is improved. The negative impact of damage caused by etching on device performance is slight under the existing process equipment conditions. In metal-oxide-semiconductor (MOS) devices, carriers flow through the channel region. If the channel region is very narrow, quantum effects need to be considered; however, in the proposed HEMT, electrons flow mainly under the recessed region, rather than in the recessed region. The recessed regions in this paper are mainly used to change the capacitors (C_{gs}, C_{gd}, and so on) and the two-dimensional electron gas distribution of the device. Therefore, there is no need to consider the quantum effect.

3. Results and Discussion

The novel AlGaN/GaN HEMT with a high gate and a multi-recessed buffer was simulated using the TCAD Sentaurus software, and the physical model and key parameters used in the simulation are shown in Table 1. By measuring the traditional HEMT, the values of carrier mobility μ, N_c, and N_v were obtained, and other material parameters were default values. The mobility defines the carrier mobility models, which include electron mobility degradation due to high doping. The thermodynamic model extends the drift–diffusion approach to account for electrothermal effects under the assumption that charge carriers are in thermal equilibrium with the lattice. The effective intrinsic density triggers the bandgap-narrowing effect in highly doped regions using the specified model OldSlotboom. Shockley–Read–Hall (SRH) recombination is activated within the recombination. The Fermi activates the carrier Fermi statistics. Incomplete ionization must be considered when impurity levels are relatively deep compared to the thermal energy (kT). The solution model is coupled {Poisson electron

hole}, and the initial temperature is set to 300 K by default in simulations [15]. In the ADS software, the EE_HEMT model [16] was used. The criterion of breakdown was BreakCriteria {Current (Contact = "Drain" Absval = 1×10^{-4})}. In order to get a more accurate calculation result, the number of iterations was set to 50, and the error reference of the electron was set to 1×10^{-3}. The parameters in the EE_HEMT model were obtained from the TCAD simulations, known literature, and technical manuals, the gate was the input terminal, and the drain was the output terminal, in the different frequency bands of 600 MHz, 1.2 GHz, and 2.4 GHz. The simulation results obtained using Synopsys TCAD Sentaurus and ADS software show that the new structure has better RF characteristics and greater power-added efficiency (PAE).

Table 1. Key parameters used in simulation.

Physical Model	Descriptions	Key Parameters
Mobility	Carrier mobility	μ = 1.300e + 03 $cm^2/(Vs)$
Thermodynamic	Lattice heat capacity	c_v = 3.0 $J/(K{\cdot}cm^3)$
	Lattice thermal conductivity	κ = 1.3 W/(K·cm)
Effective intrinsic density	$n_i(T) = N_C(T) \times N_V(T)$ exp $(E_g(T)/(2kT))$ $n_{i,eff} = n_i \times \exp \times (E_{bgn}/(2kT))$	$N_C = T^{3/2} \times 4.5 \times 10^{14}$ $N_V = T^{3/2} \times 8.9 \times 10^{15}$
Shockley–Read–Hall (SRH) recombination	$\tau = \tau_{min} + (\tau_{max} - \tau_{min})/(1 + (N/N_{ref})$	τ_{min} = 0.0000 s τ_{max} =1.0000 × 10^{-9} s N_{ref} = 1.0000 × 10^{16} cm^{-3}
Fermi	$E_g = E_{g0} + \alpha \times T_{par}{}^2/(\beta + T_{par}) - \alpha \times T^2/(\beta + T)$	E_{g0} = 3.47 eV α = 7.40 × 10^{-4} eV/K β = 6.00 × 10^2 K T_{par} = 0.0000 K

3.1. Direct Current (DC) Characteristics

It can be seen from Figure 2 that, under a large drain bias, a large current will cause the crystal lattice to heat up, forming a self-heating effect. When V_{gs} = 0 V, the effect of self-heating on the output characteristics is more obvious; thus, the self-heating effect must be considered. The drain saturation current of the HGMRB HEMT is slightly smaller than that of the conventional HEMT. At V_{gs} = 0 V and V_{ds} = 20 V, the maximum drain saturation currents of the HGMRB HEMT and conventional HEMT were 550.26 mA/mm and 609.32 mA/mm, respectively, which were reduced by 59 mA/mm, whereby the saturated drain current of the new structure was 9.68% lower than the conventional structure. Similarly, when V_{gs} = 0 V and V_{ds} = −1 V, the saturated drain current of the new structure was 11.73% lower than the conventional structure Since the HGMRB structure is used, there are two recessed regions in the channel region, and the discontinuous channel region hinders the channel current; the deeper the recess depth of the buffer region is, the smaller the channel current will be. At the same time, the Two-dimensional electron gas (2DEG) concentration of the channel region is proportional to the thickness of the barrier layer. The barrier layer of the HGMRB structure will be smaller than the conventional HEMT, resulting in a decrease in channel current. Combining the two points above, the maximum drain saturation current of HGMRB was slightly smaller than that of the conventional HEMT. In order to keep the channel current from dropping significantly, two recesses were formed in the buffer region, and the depth of the recessed region was not particularly large.

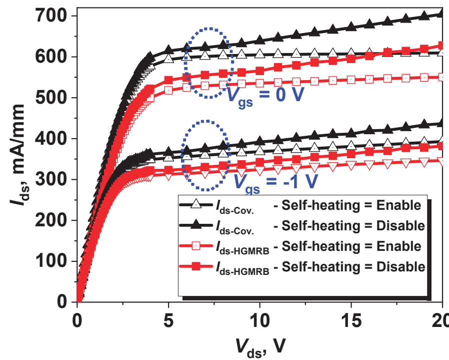


Figure 2. Output characteristics under different values of gate bias for the conventional HEMT and HGMRB HEMT including self-heating.

Figure 3 shows the transfer characteristics and transconductance curves of the conventional HEMT and the HGMRB HEMT at V_{ds} = 20 V. It can be seen from Figure 3 that the threshold voltages V_t of the conventional HEMT and the HGMRB HEMT were −3.41 V and −3.50 V, respectively. As the gate voltage approached 0 V, the drain currents of both HEMTs gradually increased, and the drain current value of HGMRB was smaller than that of the conventional HEMT. Since the magnitude of the threshold voltage is related to the thickness of the barrier layer under the gate, when the thickness of the barrier layer is the same, the depletion region formed under the gate is almost uniform; thus, the turn-on voltages of the two devices are almost identical.

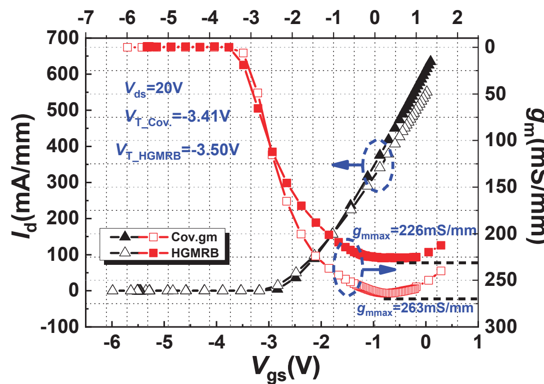


Figure 3. Transconductance and transfer curve with gate voltage at V_{ds} = 20 V.

According to the definition of transconductance g_m, transconductance refers to the ratio between the change value of the current at the output end and the change value of the input terminal voltage. The first-order derivation of the transfer curve is shown in Figure 3. From the figure, the voltage control range of the HGMRB HEMT was slightly stronger than that of the conventional HEMT, but the maximum transconductance g_{mmax} was 37 mS/mm smaller than the conventional HEMT. Due to the existence of a recessed area on the surface of the buffer layer where the channel region was located, the channel region was not flat, and the maximum saturated drain current was reduced; however, the existence of the recess could increase the thickness of the barrier layer above the recess, resulting in an increase in 2DEG, and this kept the maximum drain saturation current from being too low.

Figure 4 shows the breakdown characteristics of the device at $V_{gs} = V_t$, where the break criterion is that the absolute value of the gate is 1×10^{-7} A. The results show that the breakdown voltages (V_b) of the conventional HEMT and HGMRB HEMT were 210 V and 245 V, respectively, with the breakdown voltage increasing by 16.7%. When the high drain voltage was applied, a high electric field was formed at the edge of the gate, such that, when the drain voltage reached a certain value, breakdown occurred at the position of the gate of the GaN HEMT near the drain side. Figure 5 shows the electrostatic potential distribution of the two devices, where it can be seen that the equipotential line distribution on the right side of the gate of the conventional HEMT ($x > 3$) changed to dense firstly and then to sparse, while, in the HGMRB HEMT, the equipotential lines on the right side of the gate ($x > 3$) were more evenly distributed and were not particularly dense, which effectively slowed down the electric field concentration near the gate, enabling the HGMRB HEMT to withstand larger drain voltages and improve the breakdown voltage of the device.

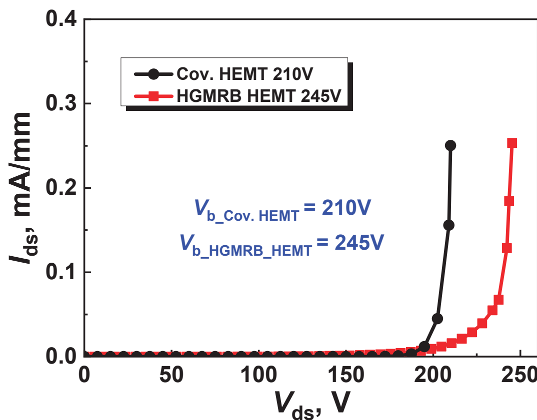


Figure 4. Breakdown characteristics of the two devices at $V_{gs} = V_t$.

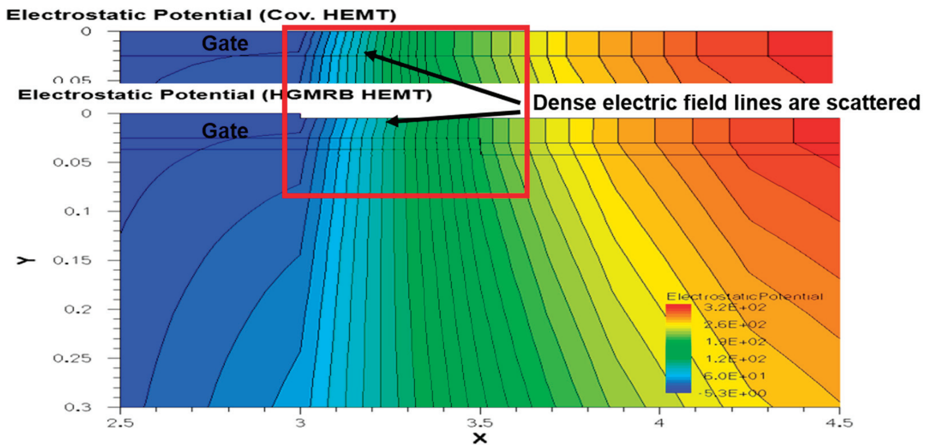


Figure 5. Electrostatic potential distribution of the conventional HEMT and proposed HGMRB HEMT.

3.2. RF Characteristics

The device was biased as shown in Figure 6. The gate was the input terminal in the different frequency bands, and the drain was the output terminal. Figure 7 shows the curve of the gate source capacitance (C_{gs}) and alternating current (AC) transconductance versus frequency for the two devices with V_{gs} = 0 V and V_{ds} = 20 V. Under this bias condition, the DC operating point of the device was better, which is beneficial to obtain more accurate parameters. The simulation results show that when the frequency was 1 GHz, the C_{gs} values of the conventional HEMT and HGMRB HEMT were 2794.49 pF/mm and 2410.57 pF/mm, respectively, and the C_{gs} value of the new structure was about 506 pF/mm lower than the conventional structure. Due to the existence of the high gate, when V_{gs} = 0 V, the depletion region could only diffuse vertically downward [17], while the depletion region under the conventional structure gate diffused to both the source and the drain, and the capacitance area increased [18]. The simulation results show that the depth of the depletion region below the gate of the new structure was deeper than that of the conventional structure. According to the definition of the parallel plate capacitor [19], the gate capacitance of the new structure can be lower than that of the conventional structure.

$$C = \frac{\varepsilon_0 S}{4\pi k d} \tag{1}$$

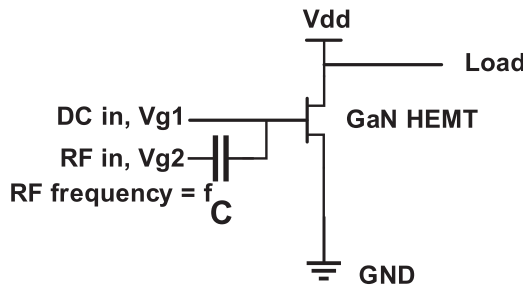


Figure 6. One-tone load-pull schematic for measurements.

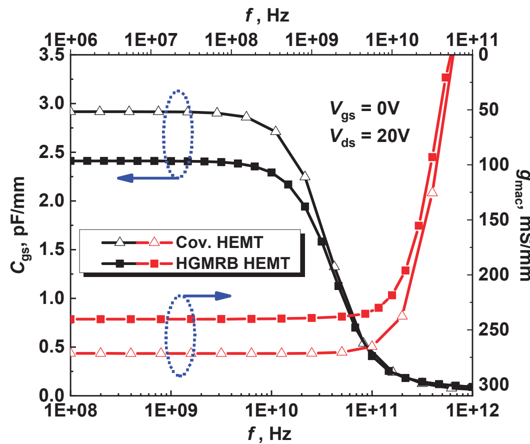


Figure 7. Gate-source capacitance (C_{gs}) and transconductance (g_m) versus frequency of the two devices at V_{gs} = 0V, V_{ds} = 20V.

From the AC transconductance curves of the two structures, it can be seen from the figure that the AC transconductance value of the conventional HEMT device was 31.00 mS/mm higher than that of the HGMRB HEMT at V_{gs} = 0 V and V_{ds} = 20 V, and the AC transconductance peak of the HGMRB HEMT was 240.31 mS/mm. The transconductance peak value under DC conditions was 10.30 mS/mm, and the AC peak transconductance of the conventional HEMT device increased by 14.00 mS/mm.

In AC conditions, the RF signal loaded on the gate periodically changed with frequency, such that the channel output current also changed periodically. When the frequency signal change period exceeded the time constant, the channel current could be changed in the future in the same signal period, resulting in a decrease in current and a decrease in the AC transconductance value under high-frequency conditions.

In order to obtain the cutoff frequency and maximum oscillation frequency of the HGMRB HEMT device, a two-port network was used for small-signal S-parameter simulation, in which V_{gs} = 0 V and V_{ds} = 20 V. Figure 8 shows the simulation results of the small-signal high-frequency characteristic curves of the two structures, where h_{21} is the small signal current gain of the device, maximum available gain (MAG) is the maximum gain of the device, and U is the unilateral power gain of the device. When h_{21} dropped to 0 dB, the cutoff frequency of the HGMRB HEMT and the conventional HEMT device was almost the same, and the cutoff frequency f_t was about 14.2 GHz. The cutoff frequency f_t is inversely proportional to the gate source capacitance C_{gs} and is proportional to the transconductance g_m. Since the transconductance and the gate source capacitance of the HGMRB HEMT were simultaneously reduced, the drop in the transconductance peak of the device and the decrease in the capacitance of the gate source were offset by the effect of f_t; thus, the cutoff frequency of the new structure hardly changed. When the unilateral gain U and the maximum achievable gain MAG dropped to 0 dB, the maximum oscillation frequencies f_{max} of the HGMRB HEMT and the conventional HEMT were about 66 GHz and 57 GHz, respectively, whereby the new structure was 15.78% higher than the traditional structure. It can be seen from Equation (3) that the HGMRB HEMT device itself had a smaller gate resistance value without changing f_t, thus increasing f_{max}.

$$f_t \approx \frac{g_m}{2\pi C_{gs}} \quad (2)$$

$$f_{max} = \frac{f_t}{2} \cdot \sqrt{\frac{R_{ds}}{R_g}} \quad (3)$$

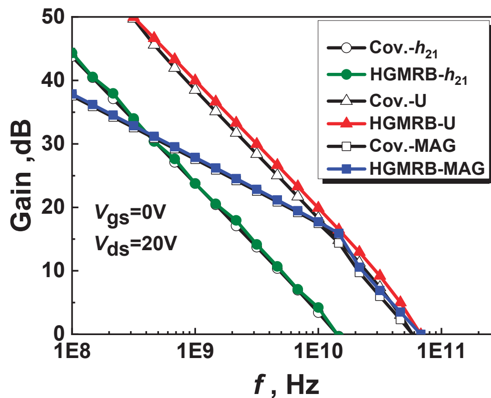


Figure 8. Small-signal high-frequency characteristic curve of two devices at V_{gs} = 0 V, V_{ds} = 20 V.

The device structure parameters described in Table 2 were obtained by simulation verification of Sections 3.1 and 3.2, and these parameters were brought into the EE_HEMT model of the ADS software, and the energy efficiency verification was performed at different frequencies. The DC offset was $V_{gs} = -4$ V and $V_{ds} = 20$ V.

Table 2. Parameters of the conventional high-electron-mobility transistor (HEMT), and proposed HEMT with a high gate and a multi-recessed buffer (HGMRB).

Parameters	Conventional HEMT	HGMRB HEMT
I_{dsat} (mA/mm)	609.32	550.26
V_b (V)	210.00	314.00
g_m (mS/mm)	263.00	226.00
V_t (V)	−3.41	−3.50
C_{gs} (fF/mm)	2916.49	2410.57

3.3. Verification of High Energy Efficiency

Figure 9a shows the output power (P_{out}) and power-added efficiency (PAE) as a function of input power (P_{in}) for the HGMRB HEMT and conventional HEMT under $V_{gs} = -4$ V and $V_{ds} = 20$ V bias conditions at 600 MHz operating frequency. The results show that the power-added efficiency (PAE) of the HGMRB HEMT was always greater than the conventional HEMT. When the input power was 32 dBm, the output power of the HGMRB HEMT reached 42.92 dBm, the output power density was 9.8 W/mm, the power gain was 10.9 dB, and the power-added efficiency reached the maximum value of 90.8%, which was higher than the maximum additional efficiency of the conventional HEMT. When the operating frequency was increased to 1.2 GHz, the P_{out} and the PAE as a function of the input power P_{in} are shown in Figure 9b. When the input power was 32 dBm, the PAE of the HGMRB HEMT reached 87.0%, the P_{out} reached 42.93 dBm, and the power gain was 10.9 dB. At 1.2 GHz, the power output capability and power-added efficiency of the HGMRB HEMT were like those at 600 MHz, but the HGMRB HEMT had greater efficiency. Figure 9c shows the P_{out} and the PAE as a function of P_{in} at 2.4 GHz, $V_{gs} = -4$ V, and $V_{ds} = 20$ V. Due to the smaller gate source capacitance of the HGMRB HEMT, its advantages in saturated output power began to increase as the operating frequency continued to increase. When the input power reached 26 dBm, the PAE of the device was maximum, about 85.0%, and the P_{out} was 41.55 dBm. When the P_{out} was saturated, the output power was 41.95 dBm and the saturated output power density was 7.7 W/mm. The output power of the HGMRB HEMT was always greater than that of the conventional HEMT.

Through the above analysis of the HGMRB HEMT and conventional HEMT, the HGMRB output power and PAE were always greater than conventional HEMT at the same input power. Because the HGMRB HEMT had the advantage of smaller gate source capacitance, when the frequency increased, the device's advantages in power gain and PAE began to fully be reflected.

Table 3 shows the performance of the various parameters of the device at different frequencies in detail. Through the above analysis, HGMRB HEMT and conventional HEMT, HGMRB output power and PAE are always greater than conventional HEMT at the same input power, and because HGMRB HEMT has smaller gate-source capacitance advantages, along with frequency increased, the device's advantages in power gain and PAE began to fully be reflected.

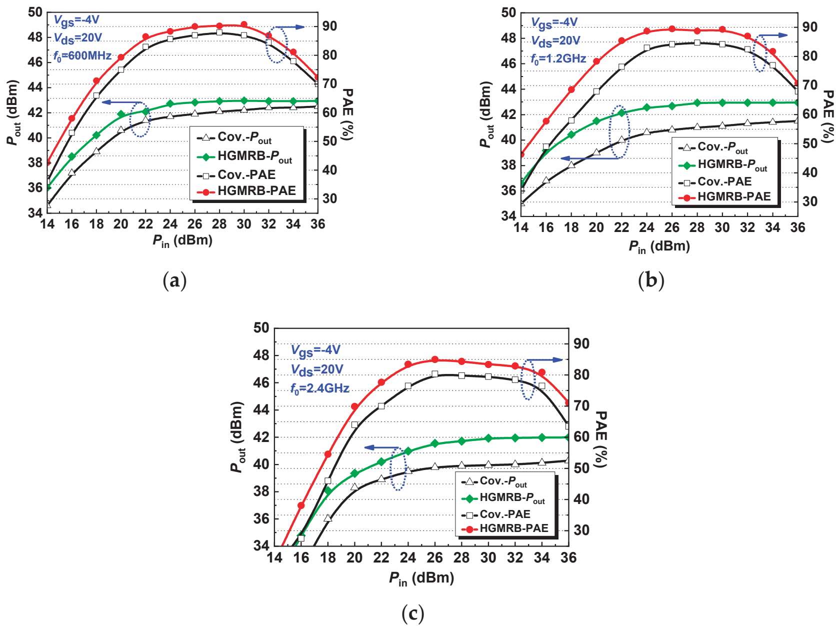


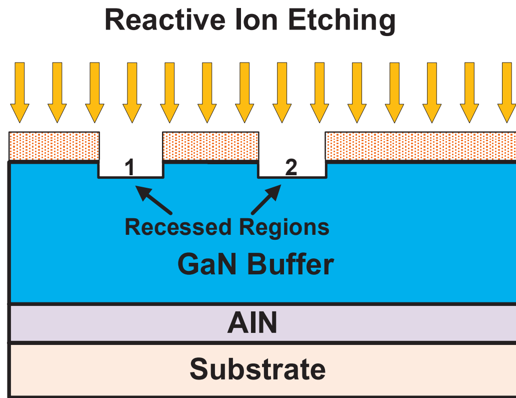
Figure 9. Large-signal performance of the two devices at different frequencies: (**a**) 600 MHz, (**b**) 1.2 GHz, and (**c**) 2.4 GHz.

Table 3. Comparison of output characteristics between the two structures at different frequencies. PAE—power-added efficiency.

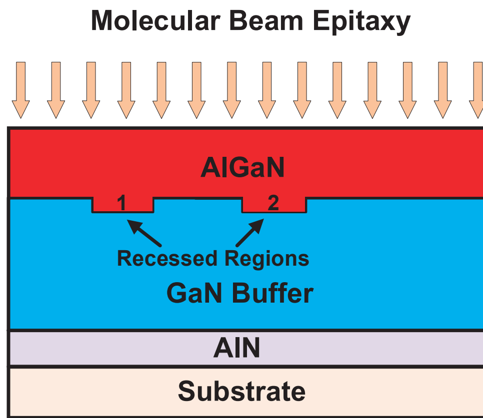
Parameters	HGMRB HEMT			Conventional HEMT		
	600 MHz	1200 MHz	2400 MHz	600 MHz	1200 MHz	2400 MHz
Power density (W/mm)	9.8	9.8	7.7	8.7	6.7	5.0
Gain (dB)	10.9	10.9	9.9	10.4	9.3	8.0
PAE at saturation (%)	86.9	87.0	82.9	84.5	82.5	78.5
The maximum PAE (%)	90.8	89.3	84.4	88	84.7	80.3

3.4. Key Process Steps for HGMRB HEMT

A feasible key fabrication process is shown in Figure 10. Differing from the conventional HEMT process, a high gate and a multi-recessed buffer should be grown in the process below. Firstly, in Figure 10a, reactive ion etching (RIE) was used in the upper surface of the GaN layer of the device, and two recessed regions 1 and 2 were etched. Secondly, in Figure 10b, the AlGaN barrier layer was grown by molecular beam epitaxy (MBE). During the film growth process, the Al content, the impurity dose, and the overall thickness of the barrier layer were controlled in the barrier layer. Thirdly, in Figure 10c, reactive ion etching (RIE) was used. Photolithography was performed on both sides of the upper surface of the AlGaN layer of the device, and two recessed regions 3 and 4 were etched to form a high gate. Then, in Figure 10d, the source, drain, gate, and ohmic contact processes were formed the same as those of the conventional GaN HEMT, where the negative impact of damage caused by etching on device performance was slight under the existing process equipment conditions.



(**a**)



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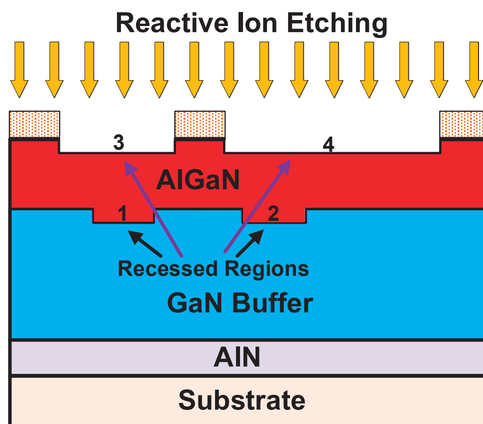
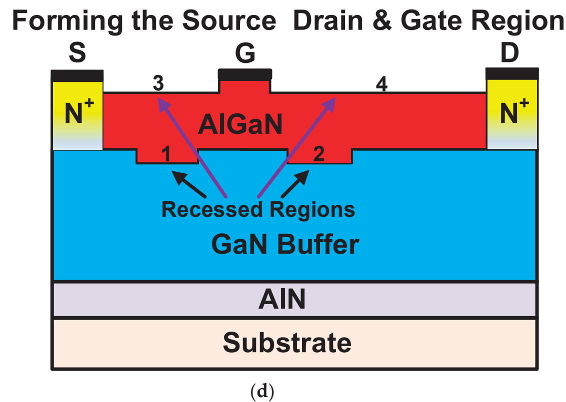


(**c**)

Figure 10. *Cont.*



(**d**)

Figure 10. Key processes to fabricate the HGMRB HEMT. (**a**) Reactive ion etching is used to form the two recessed regions 1 and 2. (**b**)The AlGaN barrier layer is grown by molecular beam epitaxy. (**c**) Reactive ion etching is used to form the two recessed regions 3 and 4, and a high gate is obtained. (**d**) Source, drain, gate, and ohmic contact processes are formed.

4. Conclusions

In this paper, a novel AlGaN/GaN HEMT with a high gate and a multi-recessed buffer for high-energy-efficiency applications was proposed and investigated using TCAD Sentaurus and ADS simulations. Although the maximum drain saturation current and transconductance slightly decreased, the breakdown voltage increased by 16.7%, the gate source capacitance dropped by 17% and the new structure had better gain and higher energy efficiency than the conventional HEMT. The output power density and PAE of the HGMRB HEMT were greater than those of the conventional HEMT in different frequency bands. The results show that the HGMRB HEMT is a better prospect for high energy efficiency than the conventional HEMT.

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Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Saremi, M. Modeling and Simulation of the Programmable Metallization Cells (PMCs) and Diamond-Based Power Devices. Ph.D. Thesis, Arizona State University, Tempe, AZ, USA, March 2017.
2. Saremi, M.; Hathwar, R.; Dutta, M.; Koeck, F.A.; Nemanich, R.J.; Chowdhury, S.; Goodnick, S.M. Analysis of the reverse I-V characteristics of diamond-based PIN diodes. *Appl. Phys. Lett.* **2017**, *111*, 043507. [CrossRef]
3. Jamali Mahabadi, S.E.; Moghadam, H.A. Comprehensive study of a 4H–SiC MES–MOSFET. *Phys. E: Low-Dimens. Syst. Nanostruct.* **2015**, *74*, 25–29. [CrossRef]
4. Moghadam, H.A.; Dimitrijev, S.; Han, J.; Haasmann, D.; Aminbeidokhti, A. Transient-Current Method for Measurement of Active Near-Interface Oxide Traps in 4H-SiC MOS Capacitors and MOSFETs. *IEEE Trans. Electron Devices* **2015**, *62*, 2670–2674. [CrossRef]
5. Razavi, S.M.; Zahiri, S.H.; Hosseini, S.E. Recessed insulator and barrier AlGaN/GaN HEMT: A novel structure for improving DC and RF characteristics. *Pramana* **2017**, *88*, 58. [CrossRef]
6. Lu, Y.; Ma, X.; Yang, L.; Hou, B.; Mi, M.; Zhang, M.; Zheng, J.; Zhang, H.; Hao, Y. High RF Performance AlGaN/GaN HEMT Fabricated by Recess-Arrayed Ohmic Contact Technology. *IEEE Trans. Electron Devices* **2018**, *39*, 811–814. [CrossRef]

7. Zheng, X.; Feng, S.; Zhang, Y.; He, X.; Wang, Y. A New Differential Amplitude Spectrum for Analyzing the Trapping Effect in GaN HEMTs Based on the Drain Current Transient. *IEEE Trans. Electron Devices* **2017**, *64*, 1498–1504. [CrossRef]
8. Hao, R.; Li, W.; Fu, K.; Yu, G.; Song, L.; Yuan, J.; Li, J.; Deng, X.; Zhang, X. Breakdown Enhancement and Current Collapse Suppression by High-Resistivity GaN Cap Layer in Normally-Off AlGaN/GaN HEMTs[J]. *IEEE Trans. Electron Devices Lett.* **2017**, *38*, 1567–1570. [CrossRef]
9. Abbate, C.; Busatto, G.; Iannuzzo, F.; Mattiazzo, S.; Sanseverino, A.; Silvestrin, L.; Tedesco, D.; Velardi, F. Experimental study of Single Event Effects induced by heavy ion irradiation in enhancement mode GaN power HEMT. *Microelectron. Reliab.* **2015**, *55*, 1496–1500. [CrossRef]
10. Micovic, M.; Brown, D.F.; Regan, D.; Wong, J.; Tang, Y.; Herrault, F.; Santos, D.; Burnham, S.D.; Tai, J.; Khalaf, I.; et al. High Frequency GaN HEMTs for RF MMIC Applications. In Proceedings of the 2016 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 3–7 December 2016.
11. Benvegnù, A.; Laurent, S.; Jardel, O.; Muraro, J.L.; Meneghini, M.; Barataud, D.; Meneghesso, G.; Zanoni, E.; Quéré, R. Characterization of Defects in AlGaN/GaN HEMTs Based on Nonlinear Microwave Current Transient Spectroscopy. *IEEE Trans. Electron Devices* **2017**, *64*, 2135–2141. [CrossRef]
12. Lidow, A.; Strydom, J.; De Rooij, M.; Reusch, D. *GaN Transistors for Efficient Power Conversion*; John Wiley & Sons: Hoboken, NJ, USA, 2014.
13. Weimann, N.G.; Manfra, M.J.; Hsu, J.W.P.; Baldwin, K.; Pfeiffer, L.N.; West, K.W.; Chu, S.N.G.; Lang, D.V.; Molner, J.R. AlGaN/GaN HEMTs grown by molecular beam epitaxy on sapphire, SiC, and HVPE GaN templates. In Proceedings of the IEEE Lester Eastman Conference on High Performance Devices IEEE, Newark, DE, USA, 8–8 August 2002.
14. Fujishiro, H.I.; Mikami, N.; Hatakenaka, M. Monte Carlo study of self-heating effect in GaN/AlGaN HEMTs on sapphire, SiC and Si substrates. *Phys. Stat. Solidi C* **2005**, *7*, 2696–2699. [CrossRef]
15. *Sentaurus Device User Guide*, version L-2016.03; Synopsys Inc.: Mountain View, CA, USA, 2016.
16. Angilent Technologies. *ADS Documentation, User Manuals*; Version 2016; Keysight Technologies: Santa Rosa, CA, USA, 2016.
17. Jia, H.; Luo, Y.; Wu, Q.; Yang, Y. A novel GaN HEMT with double recessed barrier layer for high efficiency-energy applications. *Superlattices Microstruct.* **2017**, *111*, 841–851. [CrossRef]
18. Jia, H.; Zhang, H.; Luo, Y.; Yang, Z. Improved multi-recessed 4H–SiC MESFETs with double-recessed p-buffer layer. *Mater. Sci. Semiconduct. Process.* **2015**, *40*, 650–654. [CrossRef]
19. Russell, S.; Sharabi, S.; Tallaire, A.; Moran, D.A. RF Operation of Hydrogen-Terminated Diamond Field Effect Transistors: A Comparative Study. *IEEE Trans. Electron Devices* **2015**, *62*, 751. [CrossRef]

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Vertical Field Emission Air-Channel Diodes and Transistors

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Abstract: Vacuum channel transistors are potential candidates for low-loss and high-speed electronic devices beyond complementary metal-oxide-semiconductors (CMOS). When the nanoscale transport distance is smaller than the mean free path (MFP) in atmospheric pressure, a transistor can work in air owing to the immunity of carrier collision. The nature of a vacuum channel allows devices to function in a high-temperature radiation environment. This research intended to investigate gate location in a vertical vacuum channel transistor. The influence of scattering under different ambient pressure levels was evaluated using a transport distance of about 60 nm, around the range of MFP in air. The finite element model suggests that gate electrodes should be near emitters in vertical vacuum channel transistors because the electrodes exhibit high-drive currents and low-subthreshold swings. The particle trajectory model indicates that collected electron flow (electric current) performs like a typical metal oxide semiconductor field effect-transistor (MOSFET), and that gate voltage plays a role in enhancing emission electrons. The results of the measurement on vertical diodes show that current and voltage under reduced pressure and filled with CO_2 are different from those under atmospheric pressure. This result implies that this design can be used for gas and pressure sensing.

Keywords: vacuum channel; mean free path; vertical air-channel diode; vertical transistor; field emission; particle trajectory model; F–N plot; space-charge-limited currents

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1. Introduction

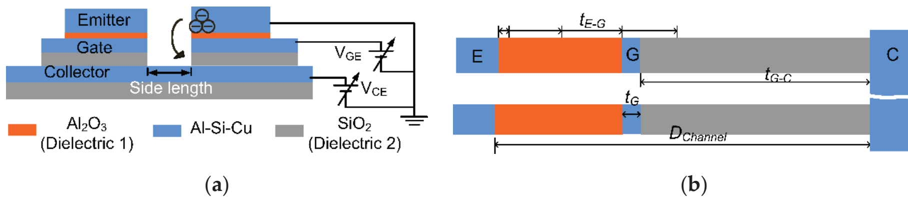
Several potential candidates for low-loss and high-speed electronic transistors beyond complementary metal oxide semiconductors (CMOS) have been proposed. Two-dimensional materials, such as graphene and transition metal dichalcogenide, were considered for next generation transistors [1–3]. Vacuum channel transistors have also been considered candidates because they are 10 times faster than silicon-based transistors [4]. The nature of vacuum channels enables the devices to function at elevated temperatures and radiation levels. A variety of structures in building vacuum channel transistors have been proposed in recent years [4–14], although vacuum transistors were first proposed to build circuits a few decades ago [15]. Generally, if the transport distance of a field emission (FE) is greater than the submicroscale, a vacuum condition is required to prevent carrier scattering, due to collision with moving particles in an ambient environment, and to achieve ballistic transport [16–19]. In addition, such a distance (or longer) generally requires a high driving voltage, which is impractical in large-scale integrated circuits [20]. Several studies have reported that FE devices with a transport distance as small as the nanoscale enable devices to operate at low voltages [5,6,21,22]. Therefore, reducing the transport distance to smaller than the mean free path (MFP) allows devices to operate in atmospheric pressure [5–7,11–13] and function under a small voltage that is suitable for practical circuits. The benefits of using 2D materials can be exploited with a vacuum channel device for low-leakage and high-speed applications [23].

Nanoscale FE air channel devices are generally categorized into horizontal, vertical, and all-around gate, depending on the related locations of emitter collectors and gates. Nanoscale horizontal electron emission air channel devices generally require advanced lithography technology or a trimming approach to define transport distance [4–7,10–14]. By contrast, vertical electron emission air channel devices define transport distance on the basis of the thicknesses of metal-dielectric stacked films [8,9]. Thin films stacked by atomic layer deposition provide an approach for specifying the transport distance of electron emission. The emission zone can be determined by the width of an open cavity on stacked films [7–9]. Gates in vacuum channel transistors are required for modulating tunneling current like in the conventional solid-state transistors. The bottom or surrounding gates of the horizontal and vertical FE transistors generally locate the gates between emitters and collectors so that the gate electric field can effectively modulate emission current [4,6–9,11–14,18]. However, several studies showed that an increase in the gate electric field can still influence the emission current when gate electrodes are above the route of electron emission [10]. The distance between the gate and the emitter can influence the turn-on voltage and controllability on the emission current for a microscale vacuum channel transistor [16–19]. However, the role of gates in vertical transistors has not been well studied. A nanoscale FE transistor can perform differently from a microscale FE one because electrons can be intercepted by coplanar gates under a nanoscale distance [13]. This paper used the finite element modeling to predict electron trajectory and determine the optimal gate location in a vertical vacuum channel transistor. Hence, carrier scattering in air, which may be difficult to find by the current simulation, must be considered in practical FE devices. The other aims of this paper were to fabricate a vertical diode with a transport distance near the MFP (~68 nm) in atmospheric pressure and to discuss carrier scattering under atmospheric and other ambient pressures.

2. Experiment

2.1. Modeling of Vertical Vacuum Channel Transistors

The schematic of a vertical vacuum channel transistor includes stacked layers of emitters, an emitter-gate dielectric (Dielectric 1), a gate, a gate-collector (Dielectric 2), and a bottom collector (Figure 1a). The etched well allows emission electrons to be ejected from the top emitter and collected by the bottom collector through the application of voltage potential (V_{CE}). The application of gate potential (V_{GC}) can modulate the route and the final speed of the electron emission. The side length of the square well is 2 μm, that is, the total emission width is four times the side width. The thicknesses of the emitter-to-gate (Dielectric 1), gate, and gate-to-collector (Dielectric 2) are $t_{E\text{-}G}$, t_G, and $t_{G\text{-}C}$, respectively (Figure 1b). The four transistors with different $t_{E\text{-}G}$ were investigated, namely, EG_3 ($t_{E\text{-}G}$ = 3 nm), EG_10 ($t_{E\text{-}G}$ = 10 nm), EG_20 ($t_{E\text{-}G}$ = 20 nm), and EG_30 ($t_{E\text{-}G}$ = 30 nm) (Table 1). The channels of transport distance ($D_{channel}$) from emitter to collector are nearly the same (~60 nm). The modeling software COMSOL (5.2, COMSOL Inc., Stockholm, Sweden) is used to model particle trajectory and electric field. The particle trajectory model assumes only a 1 nm thickness window on the lower edge of the emitter because the edges of electrodes present the highest electric fields [24]. The window releases the finite electrons (400 particles) to graphically present tracing electrons. The collector counts the collected electrons with different V_{CE} and V_{GC}. The Keithley 2400 current–voltage source meter is used for electrical characterization. The software by COMSOL is used to model the electric fields and particle trajectory in the vertical channel transistors. The material outside the device is air.



(**a**) (**b**)

Figure 1. (**a**) Schematic of the vertical vacuum channel transistor composed of stacked layers of emitters (Al-Si-Cu), a gate dielectric (Al_2O_3), a gate (Al-Si-Cu), a dielectric (SiO_2), and a bottom collector (Al-Si-Cu). (**b**) Transport distance of channel ($D_{Channel}$) made up of the thicknesses of dielectric between the emitter and the gate ($t_{E\text{-}G}$), gate (t_G), and dielectric between the gate and the collector ($t_{G\text{-}C}$) between the emitter (E) and the collector (C).

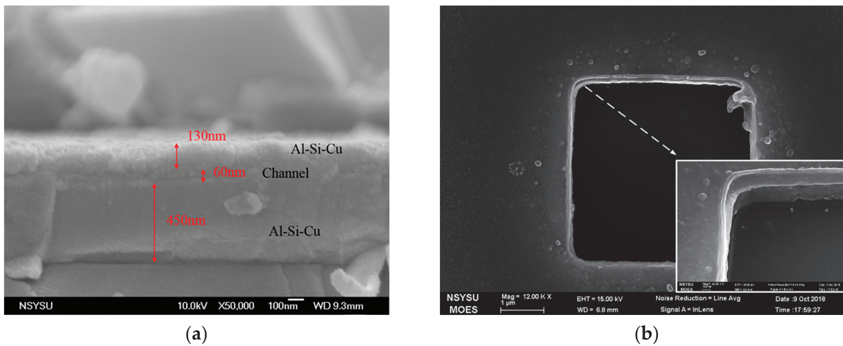
Table 1. Four simulated transistors noted by EG_3, EG_10, EG_20, and EG_30, whose transport distance of the channel ($D_{Channel}$) is the sum of the thickness of emitter-to-gate ($t_{E\text{-}G}$), gate (t_G), and gate-to-collector ($t_{G\text{-}C}$).

Dimensions of Transistors	EG_3	EG_10	EG_20	EG_30
$D_{Channel}$ (nm)	63	60	60	60
$t_{E\text{-}G}$ (nm)	3	10	20	30
t_G (nm)	20	20	20	20
$t_{G\text{-}C}$ (nm)	40	30	20	10

2.2. Fabricated Vertical Field Emission Diodes and Experimental Measurement

The fabrication of the vertical air channel diodes deposits 1 µm SiO_2 for the isolation of devices from a Si p-type (111) substrate. The photo masks define the diode-probing areas of the collector and emitter made of an Al-Si-Cu alloy, in which Al accounts for 99.5% of the metal. The SiO_2 thin film is sandwiched by the top and bottom Al-Si-Cu alloy layers. SiO_2 thickness is roughly the transport distance of electron emission because the electric field is concentrated at the edge of the metal. The cross-section of the stacked thin films indicates that the thicknesses of the top and bottom Al-Si-Cu films are 130 nm and 450 nm, respectively (Figure 2a). Square wells of 2 µm × 2 µm and 4 µm × 4 µm are etched so that electrons are transmitted from the top emitter to the collector that is located on the bottom of the well (Figure 2b). The tilt view of the etched well presents the profiles of the Al-Si-Cu layers (inset of Figure 2b). The MFP is the average distance at which a particle travels between two successive collisions. Therefore, a SiO_2 thickness of 60 nm is applied to enhance sensibility at varying ambient pressures. Transport distance in air is presumed to be approximately equal to the MFP.

The devices were wire-bonded on a printed circuit board and were measured in a customized vacuum chamber (Figure 3). The electric signals were connected to the measurement units outside the chamber via wire ports. The gas inlet of the chamber was connected to a gas feedthrough to allow external gases to flow into the chamber. A dry pump was attached to the chamber, allowing a minimum pressure of 10 mTorr.



(**a**) (**b**)

Figure 2. (**a**) Cross-sectional deposited stacked thin films, in which the thickness of the SiO2 (distance of electrons), the top (emitter), and the bottom (collector) Al-Si-Cu alloy are 60, 130, and 450 nm, respectively. (**b**) Top view of the micrograph of the etched cavity and tilt view (inset) showing the profile of the stacked thin films.

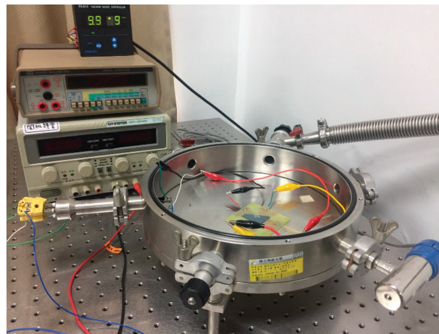


Figure 3. Customized vacuum chamber facilitated with a wire port, vacuum pump, gas inlet, pressure regulator, and pressure indicator used to measure the devices under different pressure levels.

3. Results and Discussion

3.1. Current Density Modeling of Field Emission Diodes

Space charges under high and low electric fields differ owing to the polarity of space charges. Charges in the high field are governed by the F–N theory, whereas those in the low field are governed by the space-charge-limited current. The Fowler–Nordheim (F–N) equation predicts the current density (J) generated from a small surface area of metal based on the electric field (E):

$$J = k_1 \frac{\mathrm{E}^2 \beta^2}{\phi} \cdot \exp\left(-k_2 \frac{\phi^{1.5}}{\beta\, \mathrm{E}} \right), \tag{1}$$

where $k_1 = 1.54 \times 10^{-6}$ A·eV/V^2; $k_2 = 6.83 \times 10^9$ (V/m)·eV$^{1.5}$ are constants [20]; field enhancement factor β is related to geometric design, materials, and usage [25]; ϕ is work function of the metals. However, the electric field for the current coplanar electrodes (E to C) is not uniformly distributed. The metal electrode corner near the dielectric exhibits the highest electric field from the modeling [24]. Thus, the distance of the electric takes the shortest distance of the field emission. Figure 4a shows the metals with a lower work function that also exhibit a higher current density (J). Figure 4b presents the distance that significantly influences the J because the short transport distance renders a strong E.

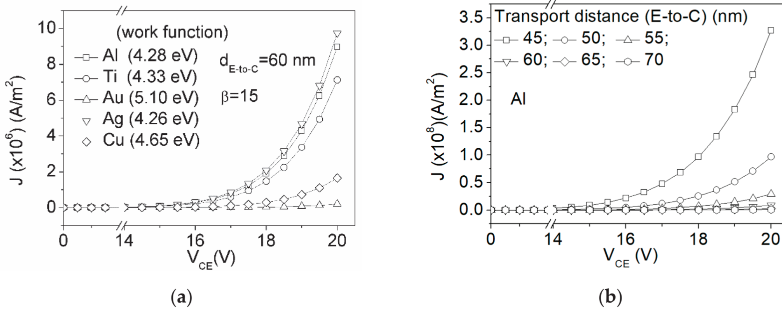
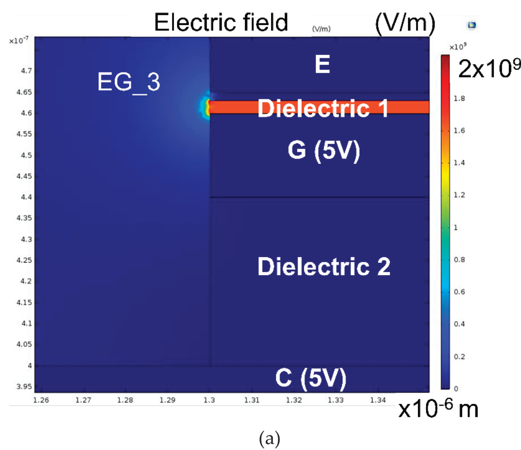


Figure 4. Electric current density (*J*) as a function of applied voltage (V_{CE}) for a high electric field applying the Fowler–Nordheim equation for (**a**) metals that exhibit different work functions (ϕ) and (**b**) different transport distances by using Al metal.

3.2. Finite Element Modeling on Vertical FE Transistors

The optimal position located between an emitter and gate was investigated by applying the distribution of electric fields with different (E-to-G) distances of 3 nm (EG_3), 10 nm (EG_10), 20 nm (EG_20), and 30 nm (EG_30), with $V_G = V_C = 5$ V grounding the emitter, as presented in Figure 5a–d, respectively. The color scales of the four figures are unified, so the colors in the simulation correspond to the values in the figures. The significant difference in the electric field among the figures occurred only on Dielectric 1 and the air between the gate and emitter, whereas the electric field near Dielectric 2 and the surrounding area makes little difference because the electric field is the gradient of potential difference. Dielectric 1 and its vicinity bear a high difference between its emitter and gate, whereas Dielectric 2 and its vicinity bear a small difference. The EG_3 exhibits the highest electric field near Dielectric 1 among the modeled devices. This result implies that the electric field and current density can be substantial at a small (Dielectric 1) thickness. The electric field distribution is consistent with the finding that the sharp edge of an emitter and collector delivers a high-density emission current [5]. This sharp emitter can also lead to the lowering of threshold voltage from non F–N to F–N behavior [13]. Figure 6 presents the electric current (I_E) as a function of V_{GE} for the four transistors. EG_3 exhibits the highest I_E and the steepest slope, i.e., the smallest subthreshold slope. The modeling results preliminarily conclude that the gate of a vertical transistor should be close to the emitter, i.e., Dielectric 1 should be as thin as possible, to obtain a high-drive current and low current leakage.



(a)

Figure 5. *Cont.*

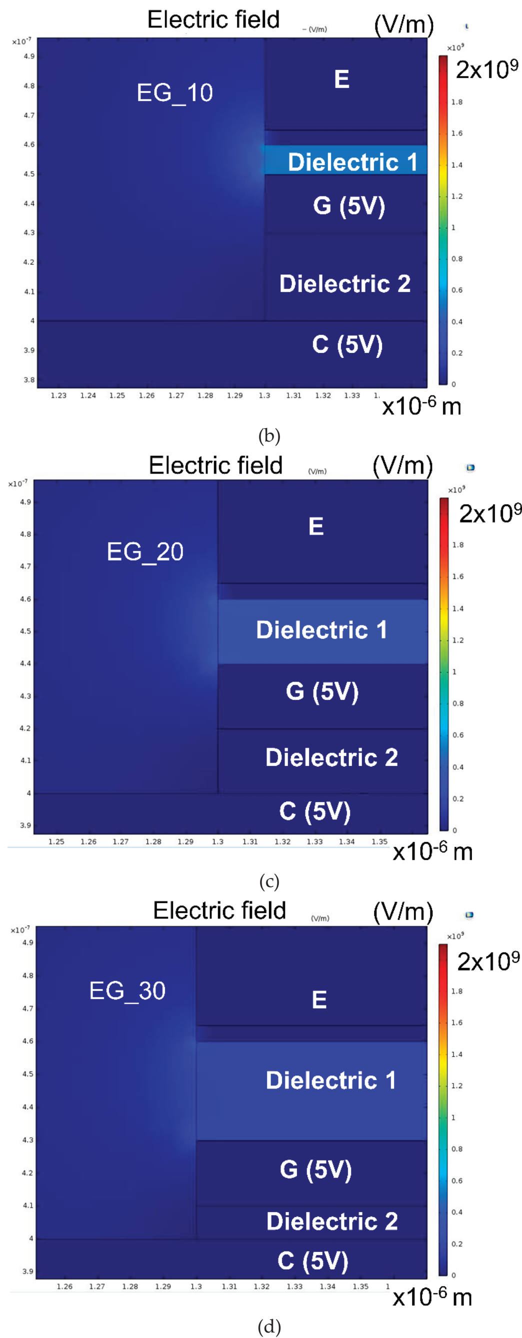


Figure 5. Colors to present electrical fields for (**a**) CG_3, (**b**) CG_10, (**c**) CG_20, and (**d**) CG_30, with $V_G = V_C = 5$ V. The color bars are scaled on the same degree.

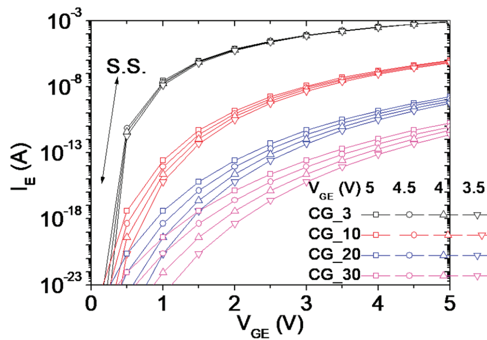


Figure 6. Simulated electric current (I_E) as a function of voltage (V_{GE}) for V_{CE} = 5, 4.5, 4, 3.5 V for CG_3, CG_10, CG_20, and CG_30.

The particle trajectory by COMSOL can present the tracing route by using the Monte Carlo scattering model. The electrons are accelerated and their final speeds increase with the tracing distance. Given that the metal edge renders the highest electric field [24], this simulation assumes that electrons are ejected from an area limited to 1 nm at the edge of the emitter. A finite number of electrons are projected from the geometric boundary of the emitter. The tracing routes of the electrons shift with gate bias. The cross-sectional view of the model (EG_3) shows that the electrons are accelerated because of the presence of an electron field when the electric potential on the collector (V_{CE}) is applied (Figure 7a). Thus, the speeds of the electrons increase along with tracing routes, as indicated by the colors. The bottom collector of the well gathers electrons in the 3D graph (inset of Figure 7a). However, the tracing routes of the electrons are bent down with the application of gate potential (V_{GE}) (Figure 7b). The 3D view shows that the tracing routes are short (inset of Figure 7b) and that the final speeds are smaller than those observed without gate bias (V_{GE}).

The electric current is counted from a limited number of electrons from the emitter and those accumulated on the collector. The collection of electrons is influenced by V_{CE} and V_{GE}. The collection rate at V_{CE} of 0 is only 2% when the V_{GE} = 5 V (Figure 8a). The collection rate significantly increases with V_{CE} (<1.5 V) and saturates when V_{CE} is higher than 1.5 V. The electron flow related to its gate-to-collector electric field is similar to the operation of MOSFETs. The simulation shows that gate potential can substantially enhance the electron flow, similarly to field emission devices [16–20] (Figure 8b). For example, the collector electric current at V_{GE} = 5 V is about five times of that at V_{GE} of 3.5 V. This result indicates that the eliminated gate dielectric of the current vertical field emission devices can perform like typical MOSFETs.

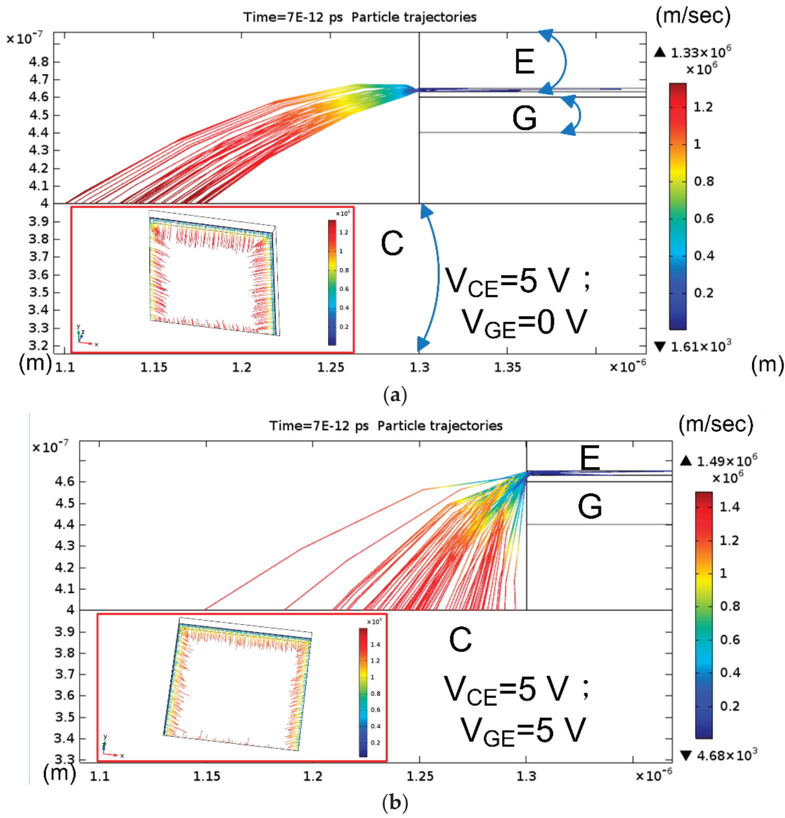


Figure 7. Tracing modeling of the electron trajectories of cross-sectional and three dimentional views (inset) for CG_3 with application of (**a**) V_{CE} = 5 V; V_{GE} = 0 V (**b**) V_{CE} = 5 V; V_{GE} = 5 V.

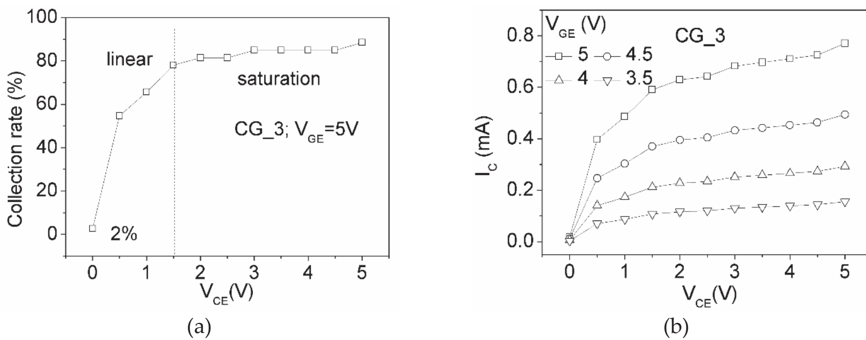


Figure 8. (**a**) Modeling the collection rate of emitted electrons of CG_3 at V_{GE} = 5 V and (**b**) collected electric current (I_C) at V_{CG} = 3.5, 4, 4.5, or 5 V.

3.3. Measurement of Field Emission Vertical Air Channel Diodes

The vertical air channel diodes use the top Al-Si-Cu alloy thin film around the well as the emitter. Thus, the emission zone is proportional to the side length. Although the electric field may not evenly distribute on the metal, the measured current is still roughly proportional to the metal area (Figure 9).

For example, the measured electrical current for the well with a 4 μm side length is 58.1 μA, whereas that of a well with a 2 μm side length is 24.6 μA at 10 V. Both of the curves exhibit F–N behavior in high electric fields (low $1/V_{CE}$) and non F–N behavior in low electric fields (high $1/V_{CE}$) (inset of Figure 9).

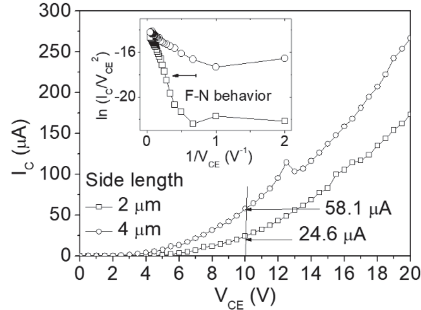


Figure 9. Current–voltage plots of the air channel diodes whose side lengths of the wells are 4 and 2 μm.

The mechanism of tunneling current is described by the F–N plot under high electric field. Based on Equation (1), the negative slope of $\ln(I_C/V_{CE})$ as a function of $1/V_{CE}$ is proportional to the emission distance (*d*) (Equation (2)), and the slope of F–N plot is as follows:

$$slope\ (\mathrm{F.N}) = -\frac{k_2\phi^{1.5}d}{\beta}, \tag{2}$$

Although the slope can determine the work function of the metals [26], β reaches a nonlinear value with increasing V_{CE}. When d = 60 nm, ϕ = 4.28 eV, and the slope is −135.2 by the regression analysis (Figure 10a), the calculated β is approximately 26.8. The linear scale of current–voltage exhibits an exponential relationship (inset of Figure 10a) and is similar to the theory presented in Figure 4a,b. By contrast, the space charge limit current equation can be used in FE at a low electric field [27,28]. The predicted current density (*J*) considers the following space charge effect:

$$J = \frac{I_E}{S} = \frac{4\varepsilon_0}{9}\sqrt{2\frac{e}{m_e}}(\frac{{V_E}^{3/2}}{d^2}), \tag{3}$$

where I_E and S are the emitted current and the surface inner area, respectively. The e and m_e are the magnitude of charge and the mass of the electron, respectively. d is the transport distance. The measurement exhibits that the collecting current (I_C) is aligned with the three-halves power law related to applied voltage (Figure 10b).

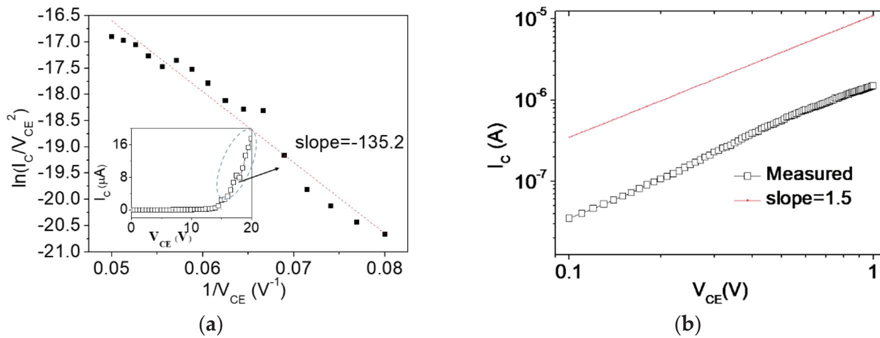


Figure 10. (**a**) F–N plot of the high electric potential part (V_{CE}) range where the slope is −135.2 by the regression method and linear scale of current–voltage plot (inset), and (**b**) logarithm current–voltage plot possessing the characteristic of three-half power on a low electric potential part (V_{CE}) range governed by a space-charge limited current.

The proposed device was measured in the closed chamber (Figure 2) for the evaluation of the impact of the collision of the electrons emitted with ambient gases. The chamber was pumped down to a base pressure and fed with CO_2 from a gas inlet. Then, changes in electric current due to carrier scattering at different ambient environments were evaluated. The measured I_C with fed CO_2 is obviously lower than that under reduced and ambient pressure (Figure 11). This result is consistent with the MFP theory that the collision of field-emitted electrons may differ at different ambient pressure levels and sizes of molecules. The emitted electrons under reduced pressure have less probability of scattering than those in environments with filled CO_2 and atmospheric pressure. Therefore, a high electric current (I_C) is collected from the measurement. This result suggests that current emission distance is critical to the sensing of pressure change and molecular size in air because microscale FE devices typically require vacuum environments to operate [16–20]. For example, the MFP ranges from 0.1 mm to 100 mm at a pressure under 0.8–800 m-Torr. The distance can be extremely long for a miniature device and renders tracing routes difficult to control.

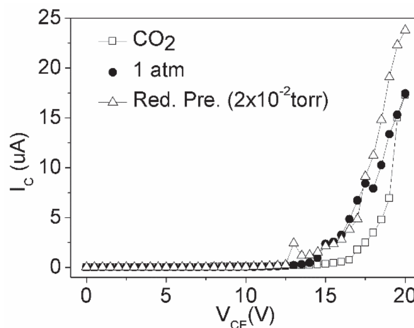


Figure 11. Current–voltage plots for a vertical channel diode with filling CO_2, atmospheric pressure, and reduced pressure of 10 m-torr.

4. Conclusions

Modeling on air channel FE diodes shows that current density increases when metals of low work function are used and substantially increases with emission distance. The particle trajectory model indicates that the thickness of a gate dielectric should be eliminated in the design of a vertical transistor so that high drive current and low current leakage can be achieved. The behavior of the

current–voltage plots related to the application of gate potential is similar to typical MOSFETs from the particle trajectory model. This phenomenon occurs because the transistor, with a short emitter-to-gate distance, exhibits better control on electron emission and a strong electric field near the gate. Although the implementation of a vertical transistor may be limited by the thicknesses of stacked thin films and carrier scattering in air, vertical diodes are fabricated to empirically verify the impact of carrier scattering in air. The measured vertical air channel diodes show that field emission distance (~60 nm that is near MFP) is sensitive to ambient gases and pressure. The measurement results roughly meet the theory of F–N and space-charge-limited current for high and low electric fields; therefore, this current design may be utilized for gas and pressure sensors.

Author Contributions: Conceptualization, W.-T.C.; methodology, W.-T.C.; software, H.-J.H. and P.-H.P.; validation, H.-J.H. and P.-H.P.; formal analysis, H.-J.H. and W.-T.C.; investigation, W.-T.C. and H.-J.H.; resources, W.-T.C.; data curation, H.-J.H.; writing—original draft preparation, H.-J.H.; writing—review and editing, W.-T.C.; visualization, W.-T.C.; supervision, W.-T.C.; project administration, W.-T.C.; funding acquisition, W.-T.C.

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References

1. Giannazzo, F.; Greco, G.; Roccaforte, F.; Sonde, S.S. Vertical transistors based on 2D materials: status and prospects. *Crystals* **2018**, *8*, 70. [CrossRef]
2. Chavarin, C.A.; Strobel, C.; Kitzmann, J.; Bartolomeo, A.D.; Lukosius, M.; Albert, M.; Wolfgang Bartha, J.; Wenger, C. Current modulation of a heterojunction structure by an ultra-thin graphene base electrode. *Materials* **2018**, *11*, 345. [CrossRef]
3. Bartolomeo, A.D.; Urban, F.; Passacantando, M.; McEvoy, N.; Peters, L.; Iemmo, L.; Luongo, G.; Romeo, F.; Giubileo, F. A WSe_2 vertical field emission transistor. *Nanoscale* **2019**, *11*, 1538–1548. [CrossRef]
4. Han, J.W.; Meyyappan, M. The device made of nothing. *IEEE Spectr.* **2014**, *51*, 30–35. [CrossRef]
5. Han, J.W.; Moon, D.I.; Meyyappan, M. Nanoscale vacuum channel transistor. *Nano Lett.* **2017**, *17*, 2146–2151. [CrossRef]
6. Liu, M.; Fu, W.; Yang, Y.; Li, T.; Wang, Y. Excellent field emission properties of VO_2(A) nanogap emitters in air. *Appl. Phys. Lett.* **2018**, *112*, 093104. [CrossRef]
7. Srisonphan, S.; Jung, Y.S.; Kim, H.K. Metal–oxide–semiconductor field-effect transistor with a vacuum channel. *Nature Nanotech.* **2012**, *7*, 504–508. [CrossRef]
8. Park, I.J.; Jeon, S.G.; Shin, C. A new slit-type vacuum channel transistor. *IEEE Trans. Elect. Devices* **2014**, *61*, 4186–4191. [CrossRef]
9. Shen, Z.; Wang, X.; Wu, S.; Tian, J. A new kind of vertically aligned field emission transistor with a cylindrical vacuum channel. *Vacuum* **2017**, *137*, 163–168. [CrossRef]
10. Jones, W.M.; Lukin, D.; Scherer, A. Practical nanoscale field emission devices for integrated circuits. *Appl. Phys. Lett.* **2017**, *110*, 263101. [CrossRef]
11. Han, J.-W.; Oh, J.S.; Meyyappan, M. Cofabrication of vacuum field emission transistor (VFET) and MOSFET. *IEEE Trans. Nanotechnol.* **2014**, *13*, 464–468. [CrossRef]
12. Nirantar, S.; Ahmed, T.; Ren, G.; Gutruf, P.; Xu, C.; Bhaskaran, M.; Walia, S.; Sriram, S. Metal–air transistors: semiconductor-free field-emission air-channel nanoelectronics. *Nano Lett.* **2018**, *18*, 7478–7484. [CrossRef] [PubMed]
13. Chang, W.T.; Pao, P.H. Field Electrons Intercepted by Coplanar Gates in Nanoscale Air Channel. *IEEE Trans. Electron. Devices* **2019**, *66*, 3961–3966. [CrossRef]
14. Kim, J.; Kim, J.; Oh, H.; Meyyappan, M.; Han, J.W.; Lee, J.S. Design guidelines for nanoscale vacuum field emission transistors. *J. Vac. Sci. Technol. B* **2016**, *34*, 042201. [CrossRef]

15. Gray, H.F.; Campisi, G.J.; Greene, R.F. A vacuum field effect transistor using silicon field emitter arrays. In Proceedings of the 1986 International Electron Devices Meeting, Los Angeles, CA, USA, 7–10 December 1986; pp. 776–779. [CrossRef]
16. Subramanian, K.; Kang, W.P.; Davidson, J.L.; Ghosh, N.; Galloway, K.F. A review of recent results on diamond vacuum lateral field emission device operation in radiation environments. *Microelectron Eng.* **2011**, *88*, 2924–2929. [CrossRef]
17. Rakhshandehroo, M.R.; Pang, S.W. Field emission from gated Si emitter tips with precise gate–tip spacing, gate diameter, tip sharpness, and tip protrusion. *J. Vac. Sci. Technol. B* **1997**, *15*, 2777–2780. [CrossRef]
18. Hsu, H.; Kang, W.P.; Raina, S.; Huang, J.H. Nanodiamond vacuum field emission device with gate modulated transistor characteristics. *Appl. Phys. Lett.* **2013**, *102*, 203105. [CrossRef]
19. Lan, Y.C.; Lee, C.T.; Chen, S.H.; Lee, C.C.; Tsui, B.Y.; Lin, T.L. Simulation study of carbon nanotube field emission display with under-gate and planar-gate structures. *J. Vac. Sci. Technol. B* **2004**, *22*, 1244–1249. [CrossRef]
20. Kang, W.P.; Davidson, J.L.; Wisitsora, A.; Wonga, Y.M.; Takalkar, R.; Holmes, K.; Kerns, D.V. Diamond vacuum field emission devices. *Diam. Relat. Mater.* **2004**, *13*, 1944–1948. [CrossRef]
21. Lenzlinger, M.; Snow, E.H. Fowler nordheim tunneling into thermally grown SiO_2. *J. Appl. Phys.* **1969**, *40*, 278–283. [CrossRef]
22. le Fèbre, A.J.; Abelmann, L.; Lodder, J.C. Field emission at nanometer distances for high-resolution positioning. *J. Vac. Sci. Technol. B* **2008**, *26*, 724–729. [CrossRef]
23. Xu, J.; Gu, Z.; Yang, W.; Wang, Q.; Zhang, X. Graphene-based nanoscale vacuum channel transistor. *Nanoscale Res. Lett.* **2018**, *13*, 311. [CrossRef] [PubMed]
24. Talaat, M.; El-Zein, A. A numerical model of streamlines in coplanar electrodes induced by non-uniform electric field. *J. Electrostat.* **2013**, *71*, 312–318. [CrossRef]
25. Schwettman, H.A.; Turneaure, J.P.; Waites, R.F. Evidence for surface-state-enhanced field emission in RF superconducting cavities. *J. Appl. Phys.* **1974**, *45*, 914–922. [CrossRef]
26. Chung, M.S.; Yoon, B.G. Analysis of the slope of the Fowler–Nordheim plot for field emission from n-type semiconductors. *J. Vac. Sci. Technol. B* **2003**, *21*, 548–551. [CrossRef]
27. Child, C.D. Discharge from Hot CaO. *Phys. Rev. (Ser. I)* **1991**, *32*, 492–511. [CrossRef]
28. Butcher, M.; Neuber, A.A.; Cevallos, M.D.; Dickens, J.C.; Krompholz, H. Conduction and breakdown mechanisms in transformer oil. *IEEE Trans Plasma Sci.* **2006**, *34*, 467–475. [CrossRef]

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A Smart Floating Gate Transistor with Two Control Gates for Active Noise Control

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Abstract: A smart floating gate transistor with two control gates was proposed for active noise control in bioelectrical signal measurement. The device, which is low cost and capable of large-scale integration, was implemented in a standard single-poly complementary metal–oxide–semiconductor (CMOS) process. A model of the device was developed to demonstrate the working principle. Theoretical analysis and simulation results proved the superposition of the two control gates. A series of test experiments were carried out and the results showed that the device was in accordance with the basic electrical characteristics of a floating gate transistor, including the current–voltage (I–V) characteristics and the threshold characteristics observed on the two control gates. Based on the source follower circuit, the experimental results proved that the device can reduce interference by more than 29 dB, which demonstrates the feasibility of the proposed device for active noise control.

Keywords: floating gate transistor; control gate; CMOS device; active noise control

1. Introduction

There is growing interest in detecting chemical or bioelectrical signals with solid-state sensors in a complementary metal–oxide–semiconductor (CMOS) process [1,2]. One of the major classes of solid-state sensors is based on the field-effect transistor (FET) [3–5]. The multiparametric nature and intrinsic signal amplification ability of FETs make them capable of achieving well beyond what is possible with two terminal devices. The ion-sensitive field-effect transistor (ISFET) [6,7] is an important branch of FET and has attracted great research interest regarding chemical signal detection due to its small size, capability of mass fabrication, and fast response time. The organic thin-film transistor (OTFT) [8–10] is another meaningful branch and has been extensively studied for bioelectrical signal detection. For example, a sensing platform based on floating gate OTFTs is used for bioelectrical signal sensing [11–14]. The working principle of a floating gate organic charge-modulated field-effect transistor (OCMFET) is shown in Figure 1a, where the sensing area is part of the floating gate exposed to the surrounding bioelectrochemical environment to detect signals, and the control gate is used to set the working point with the control capacitor, as shown in Figure 1b. Ionic or cell charge variations occurring in close proximity to the sensing area cause a charge separation in the floating gate, which leads to a modulation of the charge carrier density inside the channel of the transistor, as shown in Figure 1c [15]. The OCMFET device can detect signals in the frequency range of cell electrical activity (10–1000 Hz) and can work without any external reference electrode. However, the floating gate and sensing area are integrated as a whole and can only detect charge signals, which is not suitable for detecting voltage signals because the voltage signal on the floating gate fixes the working point of the device. In addition, it is difficult for the device to suppress interference, which is important for small signal detection.

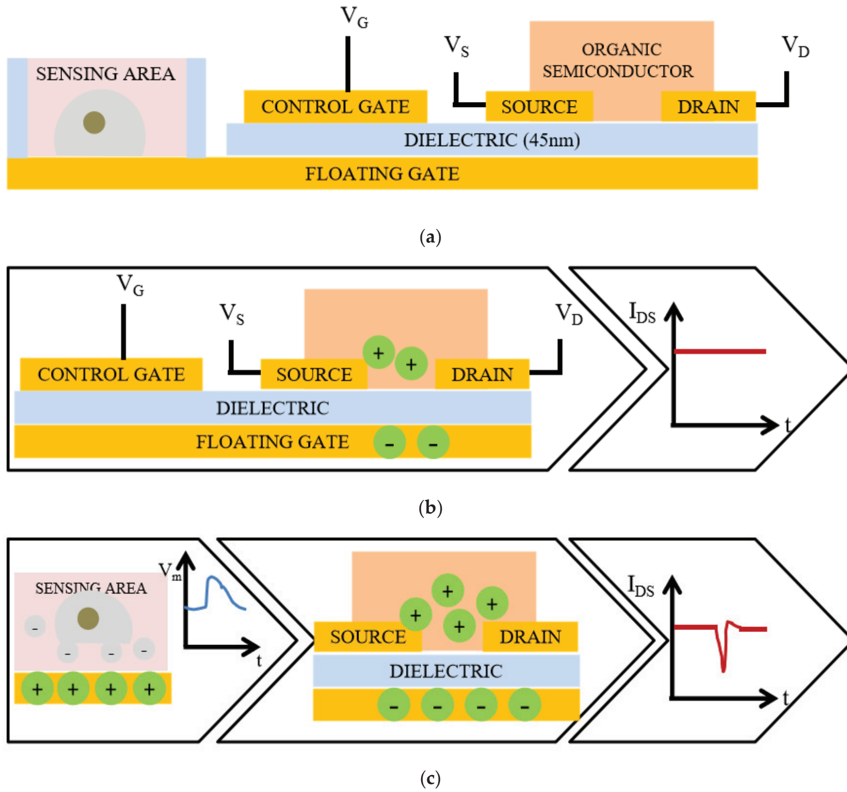


Figure 1. Working principle of a floating gate organic charge-modulated field-effect transistor (OCMFET). (**a**) Cross section of the device, where the floating gate is exposed to the surrounding bioelectrochemical environment as the sensing area. (**b**) The setting of the working point by applying the appropriate V_G. (**c**) The charge sensing and modulation principle of the device, where the charge variations occurring in close proximity to the sensing area cause a charge separation in the floating gate, which leads to modulation of the charge carrier density inside the channel of the transistor and variation of the output current.

In order to detect voltage signals, some modifications must be made, such as separating the sensing area and the floating gate. Moreover, the detected signal is accompanied by some interference and the interference can also modulate the channel charge. To suppress the interference actively, the active noise control (ANC) concept has been introduced, which cancels the unwanted primary interference by using a secondary source for signal superposition [16–18]. Generally, two input ports are required to achieve active noise control, where one input port is used for primary source detection and another for secondary source input [19]. Therefore, we have proposed a smart floating gate transistor with two control gates (called an ANC device), which is characterized by active noise control and a low-cost standard CMOS process.

Firstly, the physical model of the proposed device was developed to demonstrate the working principle, and the layout of the device was implemented in a standard single-poly CMOS process. Secondly, simulation results are illustrated to show the ANC performance based on the proposed device. Finally, the experimental electrical characterizations of the fabricated device are provided, which demonstrate the feasibility of the device for active noise control applications.

2. ANC Device

2.1. Device Structure

The proposed ANC device is based on an evolution of a single-poly metal–oxide–semiconductor field-effect transistor (MOSFET) and the cross section of the proposed ANC device is shown in Figure 2, including a source region (S), a drain region (D), a bulk region (B), a floating gate (FG), and two control gates (CG_1 and CG_2). Two heavily doped N+ regions are generated on a P-type bulk to serve as the source and the drain, and two N- or P-type physically isolated wells are generated beside the bulk to serve as the two control gates CG_1 and CG_2, respectively. The floating gate is generated by a single-poly layer, which is isolated from the bulk and the two control gates by a dielectric layer. The floating gate overlaps the bulk and the two control gates, which leads to the coupling capacitors. The channel current of the proposed device is controlled with two control gates by the coupling capacitors with the floating gate. In application, control gates CG_1 and CG_2 are connected to two standard PADs to receive voltage signals. The source, drain, and bulk are connected to three standard PADs for the normal working condition setting.

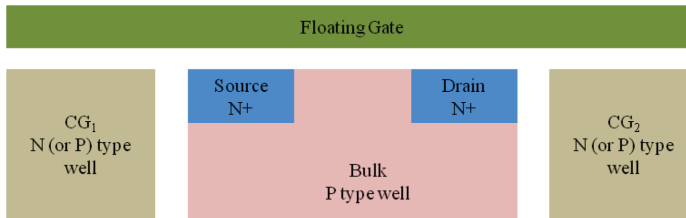


Figure 2. Cross section of the proposed active noise control (ANC) device based on an evolution of a single-poly metal–oxide–semiconductor field-effect transistor (MOSFET), including a source region (S), a drain region (D), a bulk region (B), a floating gate (FG), and two control gates (CG_1 and CG_2).

2.2. Device Model

The equivalent schematic diagram of the proposed ANC device is shown in Figure 3a, where C_{FC_1}, C_{FC_2}, C_S, C_D, and C_B are the capacitors between the floating gate and the control gate CG_1, the control gate CG_2, the source, the drain, and the bulk region, respectively. Considering that the charge Q of the floating gate should be equal to 0, the simple model of the proposed device is expressed in Equation (1) [20]:

$$Q = 0 = C_{FC1}(V_{FG} - V_{CG1}) + C_{FC2}(V_{FG} - V_{CG2}) + C_S(V_{FG} - V_S) + C_D(V_{FG} - V_D) + C_B(V_{FG} - V_B) \quad (1)$$

where V_{FG} is the potential on the floating gate; V_{CG_1} is the potential on the control gate CG_1; V_{CG_2} is the potential on the control gate CG_2; and V_S, V_D, and V_B are the potentials on the source, the drain, and the bulk, respectively. Defining the total capacitors C_T as the sum of the capacitors of C_{FC_1}, C_{FC_2}, C_S, C_D, and C_B, the potential on the floating gate due to capacitive coupling can be expressed as

$$V_{FG} = \frac{C_{FC1}}{C_T} V_{CG1} + \frac{C_{FC2}}{C_T} V_{CG2} + \frac{C_S}{C_T} V_S + \frac{C_D}{C_T} V_D + \frac{C_B}{C_T} V_B. \quad (2)$$

For C_S and C_D being far less than C_T, and the bulk being grounded, Equation (2) can be simplified as

$$V_{FG} = \frac{C_{FC1}}{C_T} V_{CG1} + \frac{C_{FC2}}{C_T} V_{CG2}. \quad (3)$$

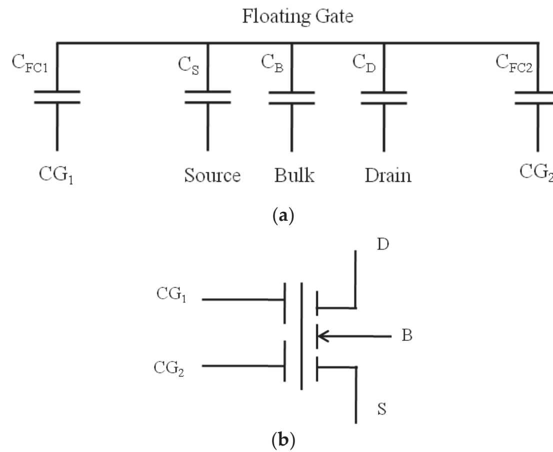


Figure 3. (**a**) The simple model of the equivalent schematic diagram of the proposed ANC device, where $C_{FC_1}, C_{FC_2}, C_S, C_D,$ and C_B are the capacitors between the floating gate and the control gate CG_1, the control gate CG_2, the source, the drain, and the bulk region, respectively. (**b**) Symbols for the ANC device with five terminals.

Generally, CG_1 and CG_2 are equivalent in terms of electrical characteristics and one of them is always set to zero for measurement of the threshold voltage, so the threshold voltages and conductivity factors of the floating gate and control gates CG_1 and CG_2 satisfy the following relationships:

$$V_T^{FG} = \frac{C_{FC1}}{C_T} V_T^{CG1} = \frac{C_{FC2}}{C_T} V_T^{CG2} \tag{4}$$

$$\beta^{FG} = \frac{C_T}{C_{FC1}} \beta^{CG1} = \frac{C_T}{C_{FC2}} \beta^{CG2} \tag{5}$$

where V_T^{FG} is the threshold for the floating gate, $V_T^{CG_1}$ is the threshold for control gate CG_1, $V_T^{CG_2}$ is the threshold for control gate CG_2, β^{FG} is the conductivity factor for the floating gate, β^{CG_1} is the conductivity factor for control gate CG_1, and β^{CG_2} is the conductivity factor for control gate CG_2.

Accordingly, the transformed current–voltage (I–V) equations of the proposed ANC device in the triode region (TR) and the saturation region (SR) can be expressed by

$$\begin{gathered} \mathrm{TR}\ |V_{DS}| < \tfrac{C_{FC1}}{C_T}\left|V_{CG1} + \tfrac{C_{FC2}}{C_{FC1}}V_{CG2} - \tfrac{C_T}{C_{FC1}}V_S - V_T^{CG1}\right| \\ I_D = \beta^{CG1}\left[\left(V_{CG1} + \tfrac{C_{FC2}}{C_{FC1}}V_{CG2} - \tfrac{C_T}{C_{FC1}}V_S - V_T^{CG}\right)V_{DS} - \tfrac{1}{2}\tfrac{C_T}{C_{FC1}}V_{DS}^2\right] \end{gathered} \tag{6}$$

$$\begin{gathered} \mathrm{SR}\ |V_{DS}| \geq \tfrac{C_{FC1}}{C_T}\left|V_{CG1} + \tfrac{C_{FC2}}{C_{FC1}}V_{CG2} - \tfrac{C_T}{C_{FC1}}V_S - V_T^{CG1}\right| \\ I_D = \tfrac{\beta^{CG1}}{2}\left(\tfrac{C_{FC1}}{C_T}\right)\left(V_{CG1} + \tfrac{C_{FC2}}{C_{FC1}}V_{CG2} - \tfrac{C_T}{C_{FC1}}V_S - V_T^{CG1}\right)^2 \end{gathered} \tag{7}$$

which show the relationship between I_D and V_{CG_1}, V_{CG_2}, V_S, and V_D. In Equation (7), I_D in the saturation region is not affected by V_{DS}, which is greatly convenient for reading the output signal of the ANC device. Assuming I_D to be a constant value and the source voltage V_S to be the output signal, the signal of the control gate is easily obtained by measuring the output voltage V_S. This readout method is called the source follower method, where the voltage of source V_S can be expressed by the voltage of two control gates as

$$V_S = \frac{C_{FC1}}{C_T} V_{CG1} + \frac{C_{FC2}}{C_T} V_{CG2} - \sqrt{\frac{2I_D}{\beta^{CG1}} \left(\frac{C_{FC1}}{C_T} \right)} - \frac{C_{FC1}}{C_T} V_T^{CG1}. \quad (8)$$

Normally, one control gate is used to set the DC operation point of the device and works as the secondary source input, and the other control gate is used to detect the effective signal with background interference. The subsequent circuits extract the interference from the output signal V_S and actively generate an inverse interference for secondary input. Thus, the secondary interference on one control gate and the primary interference on the other control gate work together to cancel each other and, finally, output the effective signal in V_S, with the interference being as small as possible.

According to the equivalent schematic diagram of the proposed ANC device shown in Figure 3a and the standard symbols for MOS transistors, the symbols for the proposed ANC device are shown in Figure 3b, which has five terminals of drain (D), source (S), bulk (B), control gate (CG_1), and control gate (CG_2).

2.3. Device Layout

The proposed ANC device was implemented in a standard 0.18 µm single-poly CMOS process. Figure 4 shows the layout and cross section of the proposed ANC device, where AA is the active area, SN is the N+ implantation for source and drain, SP is the P+ implantation, GT is the polysilicon gate, NW is the N-type well, DNW is the deep N-type well, CT is the contact area, and M1 is the metal one. As shown in Figure 4, two control gates were formed in two N-type wells without special isolation from the P-type bulk. CG_1 is an N-MOSC, while CG_2 is a P-MOSFET with a common source, drain, and substrate. The two different structures both modulated the charges in the floating gate by the coupling capacitors. The coupling capacitor was determined by the overlap area between the floating gate and the control gate. The design parameters of the ANC device are listed in Table 1, where L is the abbreviation for the length and W is the abbreviation for the width of the areas shown in Figure 4a.

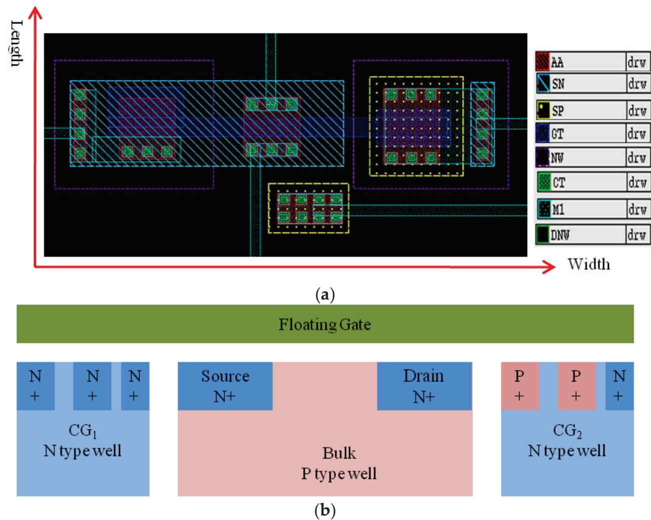


Figure 4. (**a**) Layout of the proposed ANC device, where AA is the active area, SN is the N+ implantation for the source and drain, SP is the P+ implantation, GT is the polysilicon gate, NW is the N-type well, DNW is the deep N-type well, CT is the contact area, and M1 is the metal one. (**b**) Cross section of the layout, where CG_1 is a N-MOSC and CG_2 is a P-MOSFET with a common source, drain, and substrate.

Table 1. The design parameters of the device.

Device	Length (µm)	Width (µm)
CG_1	1.375	2.01
MOS	0.67	2.03
CG_2	1.35	2.00

3. Simulation Results

A simulation schematic based on the proposed ANC device is shown in Figure 5. The device is equivalent to a standard MOSFET M_0 and two capacitors C_0 and C_1, where capacitors C_0 and C_1 can be seen as the coupling capacitors C_{FC_1} and C_{FC_2}, and MOSFET M_0 is equivalent to the combination of the floating gate, the source, the drain, and the p-bulk. Inputs IN_1 and IN_2 are equivalent to the control gates CG_1 and CG_2. Two resistors R_1 and R_2 were used to provide the bias potential for the gate. The device was operated in the source follower mode under the saturation state. The values of two capacitors C_0 and C_1 were set to 24 fF according to the parameters of CG_1 and CG_2, as shown in Table 1, calculated as Equation (9). The saturation current based on the standard MOSFET M_0 was calculated as Equation (10), where V_{GS} is the potential difference between the gate and the source, and V_T is the threshold for the MOSFET device. Signals IN_1 and IN_2 are two sinusoidal wave signals with inverse phase and the same frequency and amplitude. The voltages of nodes G, D, and S were measured and the results are shown in Figure 6. From 0 to 3.5 ms, signal IN_2 was a DC signal, only signal IN_1 modulated the gate voltage with a certain attenuation, and the source voltage followed the gate voltage. After 3.5 ms, signals IN_1 and IN_2 both modulated the gate voltage. When the primary interference was detected by input end IN_1, the source follower structure output the similar primary interference, and subsequent circuits actively generated an inverse secondary interference for input end IN_2, which led to an effective signal without the primary interference at the source output by the superposition of two input signals. As a result, the source voltage was a DC voltage without the input sinusoidal signal, which showed the good performance of active noise control.

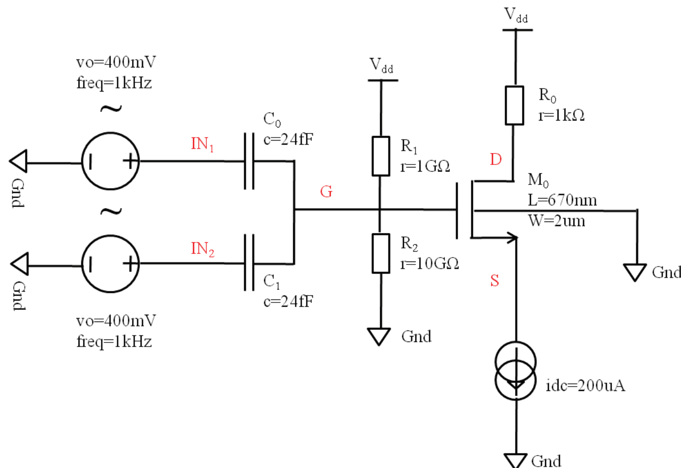


Figure 5. A simulation schematic based on the proposed ANC device with a standard MOSFET M_0 and two capacitors C_0 and C_1, where capacitors C_0 and C_1 can be seen as the coupling capacitors C_{FC_1} and C_{FC_2}; MOSFET M_0 represents the combination of the floating gate, the source, the drain, and the p-bulk; inputs IN_1 and IN_2 are equivalent to the control gates CG_1 and CG_2; and two resistors R_1 and R_2 are used to provide the bias potential for the gate.

$$C = WLC'_{ox} = WL\frac{\varepsilon_{\mathrm{r(ox)}}\varepsilon_0}{t_{ox}} = 1.35 \times 10^{-4}cm \times 2 \times 10^{-4}cm \times \frac{3.9 \times (8.85 \times 10^{-14}F/cm)}{4 \times 10^{-7}cm} = 23.3fF \quad (9)$$

$$\begin{aligned} I_D &= \frac{W\mu C'_{ox}}{2L}(V_{GS} - V_T)^2 \\ &= \frac{2\times10^{-4}cm\times500\mathrm{cm}^2/V\cdot s}{2\times0.67\times10^{-4}cm} \times \frac{3.9\times(8.85\times10^{-14}F/cm)}{4\times10^{-7}cm} \times (1.8V - 0.5V - 0.7V)^2 \\ &= 232\mu A \end{aligned} \quad (10)$$

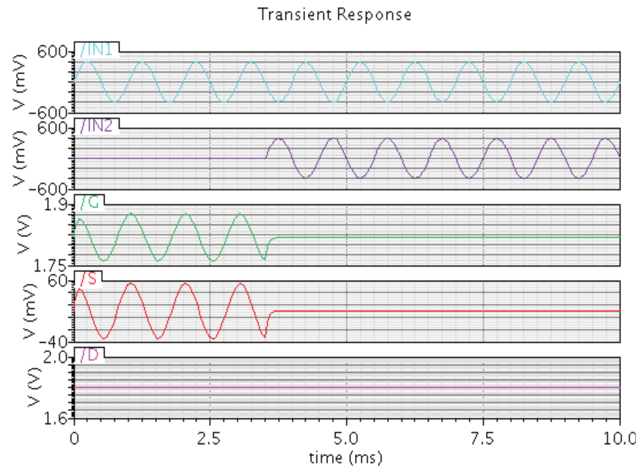


Figure 6. Simulation result of the proposed ANC device, where signals IN_1, IN_2, G, S, and D are the measured voltages from the red node IN_1, IN_2, G, S, and D shown in Figure 5, and signals IN_1 and IN_2 are simulated as the primary interference and secondary interference, respectively. From 0 to 3.5 ms, only signal IN_1 modulates the gate voltage with a certain attenuation and the source voltage follows the gate voltage. After 3.5 ms, signals IN_1 and IN_2 both modulate the gate voltage and the source voltage becomes a DC voltage without noise.

4. Experimental Results

4.1. I–V Characteristics

The proposed ANC device was fabricated in a 0.18 µm single-poly CMOS process and the performance was measured with the Keithley 4200 Semiconductor Characterization System. To test the capability of each control gate to modulate the charge carrier density of the device channel, one of the two control gates was set to zero voltage and the other was input with a scanning voltage, while the source and the bulk were grounded and the drain was set to 0.5 V. Figure 7a shows the I_D–V_G characteristics of the device, where the blue line is for control gate CG_1 and the red line is for control gate CG_2, which shows that each control gate was able to modulate the device and the threshold voltages were within a reasonable range.

Figure 7b and c show the I_D–V_D curves for control gates CG_1 and CG_2, respectively. When the control gate voltage was not large enough, a high drain voltage caused a secondary increase of the drain current. For comparison, the I_D–V_D curve for a standard MOSFET with the same gate size as that of the ANC device is shown in Figure 7d. It can be seen that when the gate voltage of the standard MOSFET is less than 0.2 V, the current I_D increases again after saturation, which is a characteristic similar to that of the proposed device. This may be caused by reverse breakdown of the pn junction

between the drain and the substrate because most of the increasing current comes from the substrate end, which can easily happen when the gate voltage is far below the threshold voltage. When the gate voltage becomes higher, a deeper depletion region is generated below the channel, which connects to the depletion region below the drain region and protects the pn junction from breakdown. Fortunately, in active noise control detection applications, the device is always turned on in the saturation state, which will not cause serious secondary increase.

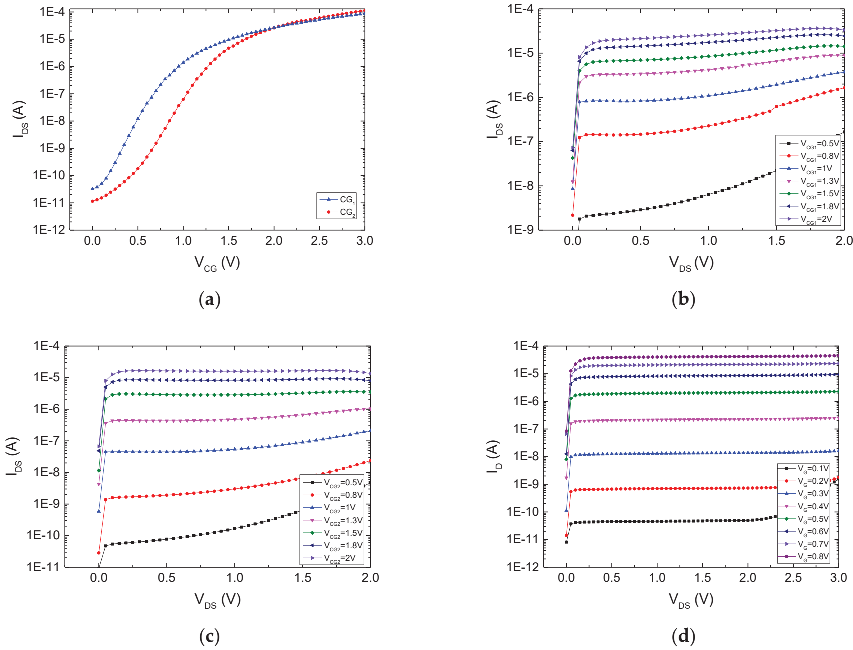


Figure 7. Current–voltage (I–V) characteristics of an ANC device and a standard MOSFET. (**a**) The I_D–V_G characteristics of an ANC device show that each control gate can modulate the device and the threshold voltages are within a reasonable range. (**b**) I_D–V_D characteristics for control gate CG_1. (**c**) I_D–V_D characteristics for control gate CG_2. (**d**) I_D–V_D characteristics of a standard MOSFET.

4.2. Device Threshold Characteristic

The basic structure of the proposed ANC device was a 1.8 V MOSFET with a channel length of 0.67 μm and a channel width of 2.03 μm. The designed overlap area between control gate CG_1 and the floating gate was slightly bigger than that between control gate CG_2 and the floating gate. In the measurement, one of the control gates was grounded and the other was for threshold scanning. The threshold voltage for each control gate is illustrated clearly in Figure 8. The average threshold voltage for CG_1 was 0.95 V and that for CG_2 was 1.3 V.

As discussed in the section on the device model, the threshold relationships satisfy Equation (4). According to the parameters in Table 1, the estimated threshold voltages of the two control gates should almost be the same value, but the measurement result was inconsistent. However, it can be seen from the layout that the real capacitor of CG_1 was larger than that of CG_2, which explains why the threshold voltage of control gate CG_1 was smaller than that of control gate CG_2.

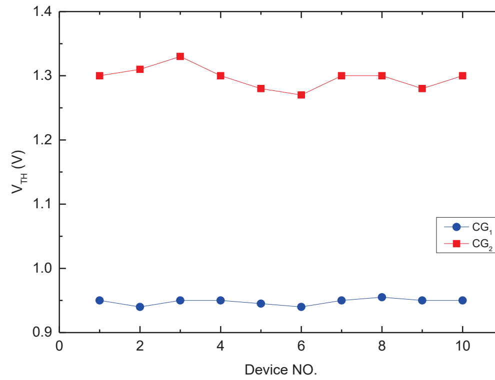
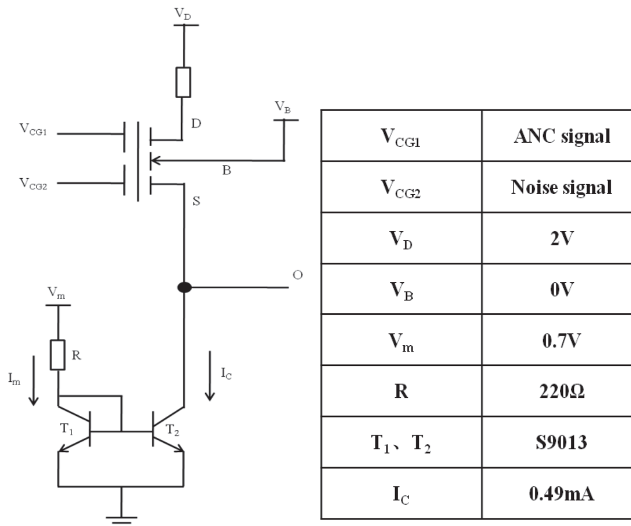


Figure 8. The threshold voltages for two control gates of 10 devices, where the average threshold voltage for CG_1 is 0.95 V and that for CG_1 is 1.3 V.

4.3. ANC Experimental Verification

The circuit with source follower mode is shown in Figure 9, where a current mirror, composed of two transistors T_1 and T_2 and a resistor R, was used to provide a constant saturation current I_C, and V_D was set to 2 V to ensure that the device was in the saturation state.



V_{CG1}	ANC signal
V_{CG2}	Noise signal
V_D	2V
V_B	0V
V_m	0.7V
R	220Ω
T_1、T_2	S9013
I_C	0.49mA

Figure 9. The circuit with source follower mode, where a current mirror, composed of two transistors T_1 and T_2 and a resistor R, is used to provide a constant saturation current I_C, and V_D is set to 2 V to ensure the device is in the saturation state.

To characterize the background noise of the proposed ANC device in the circuit system, control gate CG_2 was grounded and control gate CG_1 was applied with a standard sinusoidal signal (with a 3.3 V DC bias), shown as the black line in Figure 10. The output signal V_S was sampled and analyzed as the blue line, shown in Figure 10. The output signal curve was fitted by a sinusoidal function. The mean square of the residual expressed in Equation (11) represents the background noise of the device in the circuit system, where V_{bn} is the background noise, N is the number of sampled points, y_{real} is

the sampled output signal, and y_{fit} is the fitted signal as mentioned above. The absolute value of the background noise was less than 0.33 mV for N being 1000, which shows the feasibility of the device in detecting small biosignals. It should be noted that the background noise can be reduced further by integrating all circuits in the same CMOS process.

$$V_{\text{bn}} = \sqrt{\frac{\sum_{i=1}^{N} \left(y_{\text{real},i} - y_{\text{fit},i}\right)^2}{N}}. \tag{11}$$

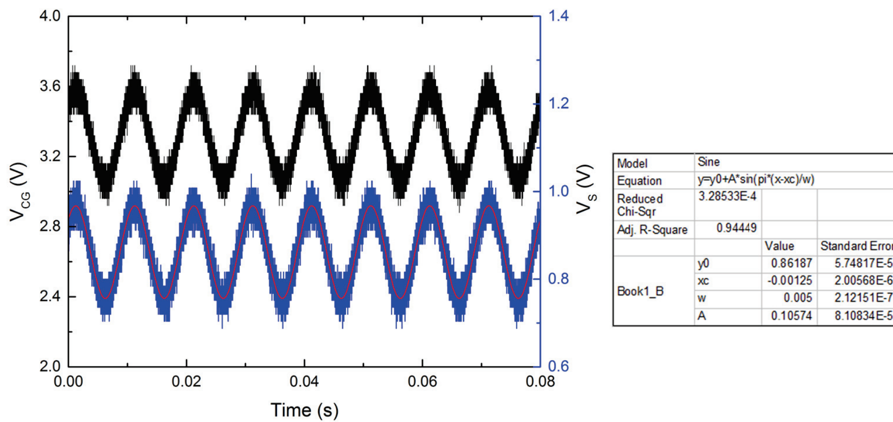


Figure 10. Characterization of device background noise in the circuit, where control gate CG_1 is applied with a standard sinusoidal signal (with a 3.3 V DC bias) as shown with the black line, and the output signal V_S is shown with the blue line and fitted by a sinusoidal function as the red line with the fitting parameters given in the insets. The absolute value of the background noise is less than 0.33 mV.

In Figure 11, the pink line is the signal on control gate CG_1, the red line is the signal on control gate CG_2 (both corresponding to the left axis), and the blue line is the output signal V_S, corresponding to the right axis. V_{CG_2} is an input sinusoidal wave signal, considered as the primary interference. V_{CG_1} is the secondary interference relevant to the primary interference from V_{CG_2}. The measured signal V_S as function of time is shown in Figure 11, which was in good agreement with expectations. As shown in Figure 11a, the output signal V_S followed the superposition of signals V_{CG_2} and V_{CG_1}, as calculated in Equation (8). When the active noise control system was turned on, the ANC signal on CG_1 was adjusted by the subsequent feedback circuits to a signal with an inverse phase from the primary interference on CG_2. The amplitude of the ANC signal was modified by adjusting the gain of the subsequent circuits manually until the output signal V_S became as small as possible. Feedback system design is a large subject area and there are many kinds of specific circuit forms for feedback system implementation. One kind of feedback circuit for an ANC system consists of a bandpass filter and an inverting amplifier. The bandpass filter extracts the interference from the output signal and the inverting amplifier generates an inverse interference for secondary input. Figure 11b shows the result of the ANC system, where the input interference amplitude was 0.255 V and the output interference amplitude after ANC was 0.009 V. Therefore, the circuits can attenuate the interference by greater than 29 dB. The device has proved to be feasible and reliable for active noise control application. Moreover, the device works at ultra-low voltages and without any external reference electrode, and it also provides the capability of large-scale integration at a low cost for fabrication in a standard single-poly CMOS process.

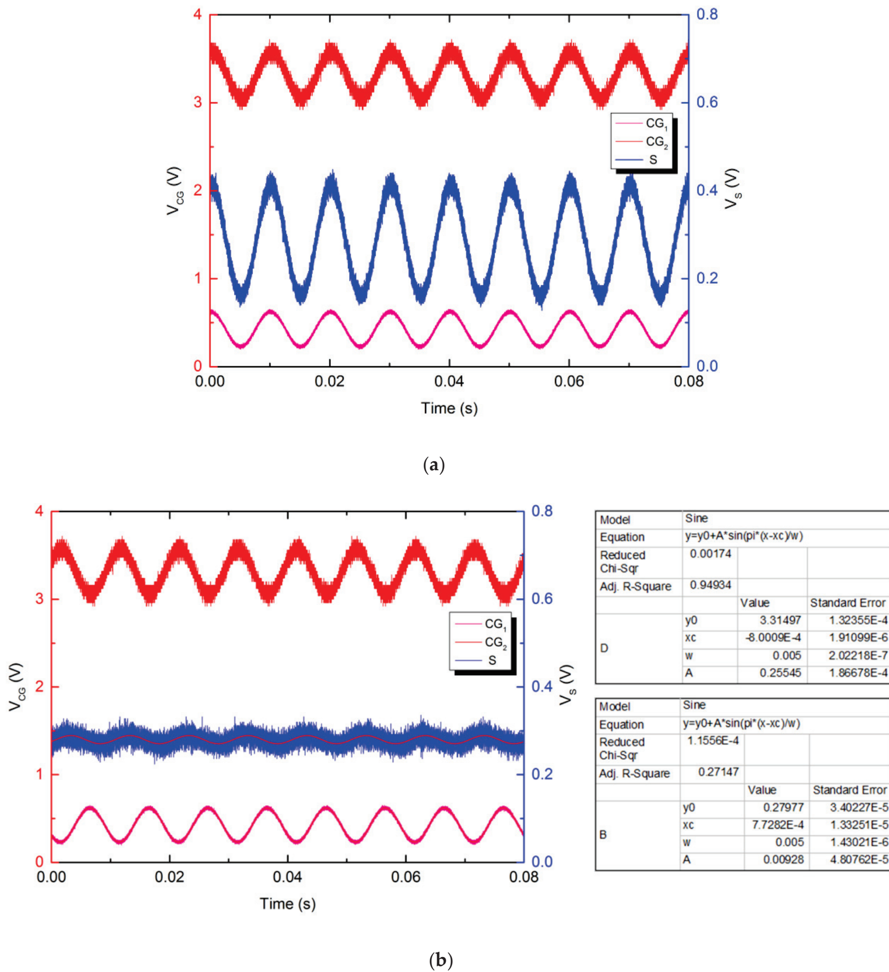


Figure 11. The measured voltage as a function of time, where the pink line is the signal on control gate CG_1, the red line is the signal on control gate CG_2, the blue line is the output signal V_S, and the input interference on control gate CG_2 and the output signal are fitted by a sinusoidal function respectively with the parameters given in the insets. (**a**) Without active noise control, the output signal V_S follows the superposition of signals V_{CG_2} and V_{CG_1} as calculated. (**b**) With active noise control, the output signal V_S is 9 mV and has a 29 dB attenuation for the input interference of 255 mV.

5. Conclusions

A smart floating gate transistor with two control gates was proposed for active noise control in bioelectrical signal measurement. A model of the device was developed and analyzed to demonstrate the working principle of the electrical behavior. Theoretical analysis and simulation results proved that the superposition of the two control gates can be reflected at the source end. To verify the feasibility of the proposed ANC device, a device with a novel structure was designed and fabricated in a standard 0.18 µm single-poly CMOS process. A series of test experiments were carried out and the results showed that the devices were in accordance with the basic electrical characteristics of floating gate transistors, including the I–V characteristics and the threshold characteristics observed on two control

gates. Based on the source follower circuit, the experimental results proved that the device can reduce interference by more than 29 dB, and that is possesses the outstanding characteristic of low-cost, large-scale integration for fabrication in a standard single-poly CMOS process.

Future work will be directed toward fabricating the readout circuit of the proposed device and the subsequent circuit for secondary input in a standard single-poly CMOS process to enhance the large-scale integration ability and reduce the background noise further.

Author Contributions: All authors conceived of and designed the device and experiments; C.M. and C.Y. performed the experiments; H.M. analyzed the data; L.Z. and F.Y. contributed materials and analysis tools; C.M. wrote the paper; L.Z. revised the paper.

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Conflicts of Interest: The authors declare no conflict of interest

References

1. Barbaro, M.; Bonfiglio, A.; Raffo, L. A charge-modulated FET for detection of biomolecular processes: conception, modeling, and simulation. *IEEE Trans. Electron Devices* **2006**, *53*, 158–166. [CrossRef]
2. Meyburg, S.; Stockmann, R.; Moers, J.; Offenhäusser, A.; Ingebrandt, S. Advanced CMOS process for floating gate field-effect transistors in bioelectronic applications. *Sens. Actuator B-Chem.* **2007**, *128*, 208–217. [CrossRef]
3. Zhang, Q.; Subramanian, V. DNA hybridization detection with organic thin film transistors: Toward fast and disposable DNA microarray chips. *Biosens. Bioelectron.* **2007**, *22*, 3182–3187. [CrossRef]
4. Zhang, X.H.; Lee, S.M.; Domercq, B.; Kippelen, B. Transparent organic field-effect transistors with polymeric source and drain electrodes fabricated by inkjet printing. *Appl. Phys. Lett.* **2008**, *92*, 243307. [CrossRef]
5. Kergoat, L.; Piro, B.; Berggren, M.; Pham, M.C.; Yassar, A.; Horowitz, G. DNA detection with a water-gated organic field-effect transistor. *Org. Electron.* **2012**, *13*, 1–6. [CrossRef]
6. Jimenez-Jorquera, C.; Orozco, J.; Baldi, A. ISFET Based Microsensors for Environmental Monitoring. *Sensors* **2009**, *10*, 61–83. [CrossRef] [PubMed]
7. Moser, N.; Rodriguez-Manzano, J.; Lande, T.S.; Georgiou, P. A Scalable ISFET Sensing and Memory Array with Sensor Auto-Calibration for On-Chip Real-Time DNA Detection. *IEEE Trans. Biomed. Circuits Syst.* **2018**, *12*, 390–401. [CrossRef] [PubMed]
8. Ogier, S.D.; Matsui, H.; Feng, L.; Simms, M.; Mashayekhi, M.; Carrabina, J.; Terés, L.; Tokito, S. Uniform, high performance, solution processed organic thin-film transistors integrated in 1 MHz frequency ring oscillators. *Org. Electron.* **2018**, *54*, 40–47. [CrossRef]
9. Krammer, M.; Borchert, J.W.; Petritz, A.; Karner-Petritz, E.; Schider, G.; Stadlober, B.; Klauk, H.; Zojer, K. Critical Evaluation of Organic Thin-Film Transistor Models. *Crystals* **2019**, *9*, 85. [CrossRef]
10. Liao, C.; Yan, F. Organic Semiconductors in Organic Thin-Film Transistor-Based Chemical and Biological Sensors. *Polym. Rev.* **2013**, *53*, 352–406. [CrossRef]
11. Lai, S.; Viola, F.; Cosseddu, P.; Bonfiglio, A. Floating Gate, Organic Field-Effect Transistor-Based Sensors towards Biomedical Applications Fabricated with Large-Area Processes over Flexible Substrates. *Sensors* **2018**, *18*, 688.
12. Spanu, A.; Viola, F.; Lai, S.; Cosseddu, P.; Ricci, P.C.; Bonfiglio, A. A reference-less pH sensor based on an organic field effect transistor with tunable sensitivity. *Org. Electron.* **2017**, *48*, 188–193. [CrossRef]
13. Demelas, M.; Lai, S.; Casula, G.; Scavetta, E.; Barbaro, M.; Bonfiglio, A. An organic, charge-modulated field effect transistor for DNA detection. *Sens. Actuator B-Chem.* **2012**, *171–172*, 198–203. [CrossRef]
14. Lai, S.; Barbaro, M.; Bonfiglio, A. Tailoring the sensing performances of an OFET-based biosensor. *Sens. Actuator B-Chem* **2016**, *233*, 314–319. [CrossRef]
15. Spanu, A.; Lai, S.; Cosseddu, P.; Tedesco, M.; Martinoia, S.; Bonfiglio, A. An organic transistor-based system for reference-less electrophysiological monitoring of excitable cells. *Sci. Rep.* **2015**, *5*, 8807. [CrossRef] [PubMed]

16. Zhang, L.; Tao, J.; Qiu, X. Active control of transformer noise with an internally synthesized reference signal. *J. Sound Vib.* **2012**, *331*, 3466–3475. [CrossRef]
17. Zhang, L.; Wu, L.; Qiu, X. An intuitive approach for feedback active noise controller design. *Appl. Acoust.* **2013**, *74*, 160–168. [CrossRef]
18. Gan, W.S.; Mitra, S.; Kuo, S.M. Adaptive feedback active noise control headset: implementation, evaluation and its extensions. *IEEE Trans. Consum. Electron.* **2005**, *51*, 975–982. [CrossRef]
19. Tseng, W.K.; Rafaely, B.; Elliott, S.J. Combined feedback–feedforward active control of sound in a room. *J. Acoust. Soc. AM.* **1998**, *104*, 3417–3425. [CrossRef]
20. Pavan, P.; Bez, R.; Olivo, P.; Zanoni, E. Flash memory cells-an overview. *Proc. IEEE* **1997**, *85*, 1248–1271. [CrossRef]

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A 45 nm CMOS Avalanche Photodiode with 8.4-GHz Bandwidth

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Abstract: Photodiode is one of the key components in optoelectronic technology, which is used to convert optical signal into electrical ones in modern communication systems. In this paper, an avalanche photodiode (APD) is designed and fulfilled, which is compatible with Taiwan Semiconductor Manufacturing Company (TSMC) 45-nm standard complementary metal–oxide–semiconductor (CMOS) technology without any process modification. The APD based on 45 nm process is beneficial to realize a smaller and more complex monolithically integrated optoelectronic chip. The fabricated CMOS APD operates at 850 nm wavelength optical communication. Its bandwidth can be as high as 8.4 GHz with 0.56 A/W responsivity at reverse bias of 20.8 V. Its active area is designed to be 20 × 20 μm^2. The Simulation Program with Integrated Circuit Emphasis (SPICE) model of the APD is also proposed and verified. The key parameters are extracted based on its electrical, optical and frequency responses by parameter fitting. The device has wide potential application for optical communication systems.

Keywords: CMOS compatible technology; avalanche photodiode; SPICE model; bandwidth; high responsivity; silicon photodiode

1. Introduction

As one of the promising photoelectric sensors, avalanche photodiode (APD) breaks the limitations of electrical interconnects, which results in high-speed, dense, and low-power interconnects [1]. It has become one of the research hotspots in the field of optical communication in recent years [2]. Avalanche photodiodes are widely used in optical communication systems and optical interconnection equipment, such as local area network, chip-to-chip, and board-to-board interconnect [3]. As one of them, 850 nm optical interconnects are actively being investigated, because 850 nm can be easily available as light sources in the high-speed optical interconnects [4,5]. The monolithically integrated high speed 850 nm wavelength silicon APDs based on standard complementary metal–oxide–semiconductor (CMOS) technology are particularly attractive because of significant advantages in cost, power, and performance that CMOS technology brings [6].

However, the optical absorption coefficient of silicon is fairly low at 850 nm. Since in standard CMOS technology, the silicon substrate is thicker than the penetration depth of light, which generates a large number of carriers in the silicon substrate and diffuses around [6]. Secondly, the maximum support voltage is reduced as the CMOS technology shrinks, which limits the reverse bias voltage for the integrated APDs [7].

Several approaches have been proposed to overcome the deficiencies and improve the performance of CMOS silicon technology. In [8], Huang et al. fabricated a silicon photodiode in standard 0.18 μm CMOS technology. The basic structure of proposed photodiode is formed by multiple p-n diodes with shallow trench isolation (STI) between p and n region. The fabricated photodiode demonstrates the −3 dB bandwidth of 1.6 GHz and a high responsivity of 0.74 A/W. In order to reduce the limit of

bandwidth, Lee [9] proposed a spatially modulated avalanche photodiode (SM-APD), which showed a bandwidth of 12 GHz and responsivity of 0.03 A/W. Iiyama et al. fabricated a triple-well structure Si photodiode with standard 0.18 μm CMOS process [10]. The N+ and P+ layers are alternatively arranged and then the electrodes are interdigital structure. The device shows a 10 GHz bandwidth with 0.05 A/W responsivity [10]. Deep N-well CMOS technology can greatly improve the electrical isolation performance between different circuit blocks, which is especially important for integrating RF-to-baseband mixed-mode circuits in a single chip. The device with Deep N-well structure can substantially increase the cut-off frequency. In the paper [11], Chou et al. used extra bias on the Deep N-well in standard CMOS technology, which achieved a high bandwidth (8.7 GHz) with a responsivity of 0.05 A/W under a 11.45 V bias.

In this paper, a P-well/Deep N-well APD based on 45 nm CMOS technology is proposed. The light current, dark current, responsivity, and photodetection frequency response are measured based on the fabricated APD device. The results show that the fabricated APD presents a high responsivity and a high bandwidth. The 8.4 GHz bandwidth is available at 850 nm with 0.56 A/W responsivity. Finally, the key parameters of APD are extracted from the frequency response. A SPICE model is established for future integrated circuit design and simulation.

2. Design and Analysis of CMOS Compatible Avalanche Photodiode (APD)

P-well/Deep N-well structure is considered to be the most suitable structure for fabricating CMOS photodiodes [12]. J. Goy et al. compared various photodiode structures, such as N-well/P-substrate structure, N+/P-substrate structure, and N+/P-well structure. The results indicated that the P-well/Deep N-well structure can improve the responsivity while reducing the parasitic capacitance [12].

Two types of APDs, with different active areas, 20 × 20 μm^2 and 50 × 50 μm^2, are fabricated, separately. Figure 1 shows the schematic structure of the 20 × 20 μm^2 CMOS APD device. The size of 50 × 50 μm^2 device is proportional to the 20 × 20 μm^2. The design is compatible with TSMC 45 nm standard CMOS technology without any process modification or special substrate. The APD is realized by vertical P-well/Deep N-well with shallow trench isolation (STI).

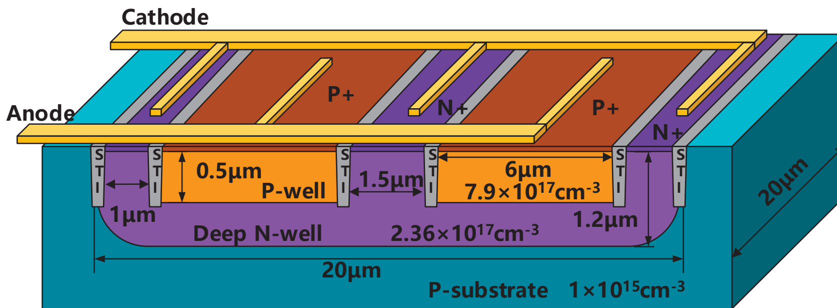


Figure 1. Structure of the designed complementary metal–oxide–semiconductor (CMOS) avalanche photodiode.

The contribution of slow diffusion photo-generated carriers in the P-substrate region can be excluded by the Deep N-well [13]. Moreover, the P-substrate is grounded or connected to a negative potential, which can effectively absorb slow diffusion photo-generated carriers. As a result, the P-well/Deep N-well shows a better performance in photodetection bandwidth than N-well/P-substrate photodiode.

When the reverse bias voltage is high, the electric field of the p-n junction increases rapidly. Because of curvature effect, the local electric field is increased, which makes the edge of the photodiode easily to breakdown [14]. It has a detrimental effect on the stability and performance of CMOS photodiodes. The most common method to prevent photodiode edge breakdown is to use a guard ring structure [15]. In this paper, STI with width of 0.15 μm is used as the guard ring (the junction depth is about 0.5 μm).

The STI can improve the reverse bias by mitigating the premature edge breakdown during avalanche. A high reverse bias provides better avalanche gain and higher responsivity.

To investigate its characteristics, a 100 µW, 850 nm, 10 Gb/s VCSEL modulated by Agilent E8257D signal generator is used as the light source. Figure 2 shows I-V characterizations of the APDs under light and dark environments, separately. All APDs show very low dark currents, which being less than 0.1 nA before the avalanche breakdown. Due to the influence of the STI structure, the avalanche breakdown voltage is increased from 14.5 V to 21.5 V. When the reverse bias approaches the avalanche breakdown voltage of 21.5 V, the dark current begins to increase sharply because of the occurrence of the avalanche breakdown. The 50 × 50 µm^2 APD active area is larger than 20 × 20 µm^2, so the photocurrent of 50 × 50 µm^2 APD is also larger.

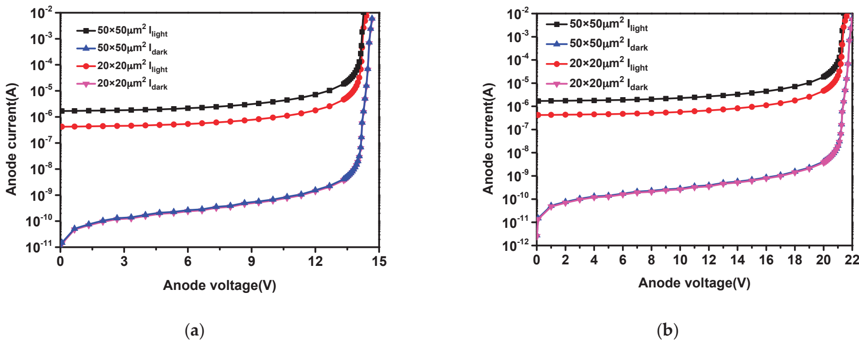


Figure 2. Electrical responses of the avalanche photodiodes (APDs) with different sizes (**a**) without shallow trench isolation (STI); (**b**) with STI.

Responsivity is defined as the photocurrent per incident optical power, which is determined by the current under illumination minus the dark current [16]. Figure 3 shows the avalanche gain, and the responsivity obtained from the measured I-V characterization. The dark current will increases to the same level as the photocurrent when the avalanche breakdown occurs. In order to reduce the influence of the dark current noise, the operating point should be slightly less than 21.5 V. Considering all the related aspects, the operating point is set to be 20.8 V, and the gain is about 23 dB. Due to the STI structure, the reverse bias is significantly improved. As the reverse bias increases, the photocurrent and the responsivity of APDs are improved obviously. When the reverse bias voltage is 20.8 V, the responsivity of the APD with area of 50 × 50 µm^2 is 0.59 A/W. On the same condition, the responsivity of the APD with area of 20 × 20 µm^2 is 0.56 A/W.

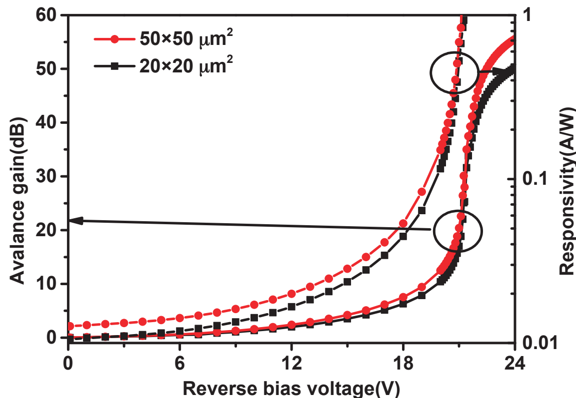


Figure 3. Optical responses of the APDs.

Figure 4 shows the frequency response of the two APDs with different active areas. The bandwidth of 50 × 50 μm^2 is much lower than that of 20 × 20 μm^2. With the increasing of the active area, the parasitic capacitance and the carrier transit time increase accordingly, which deteriorates the frequency property. The APD with active area of 20 × 20 μm^2 shows a bandwidth of 8.4 GHz at a reverse bias of 20.8 V.

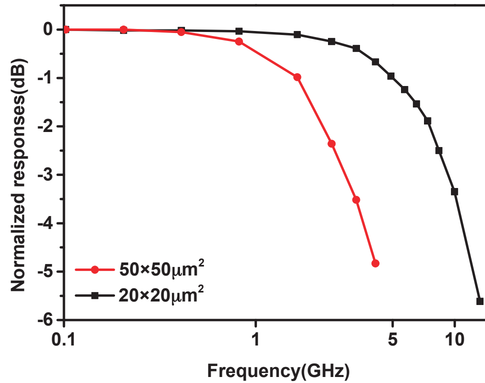


Figure 4. The frequency response of the fabricated APDs.

3. The SPICE Model of the CMOS APD

In order to better understand the photodetection frequency response characterization of the CMOS APD, the SPICE model is set up in the section. We have adjusted and optimized the SPICE model proposed in reference [16] to fit the proposed structure in the paper. The values of the key parameters are extracted from the results of Figures 2–4 by parameter fitting. For the parameter fitting, the initial value comes from the theoretical equation and then is manually modified. Figure 5 shows the updated SPICE model based on the detailed structure of the device. The active part is composed by an inductor and a resistor in series, a resistor in parallel and a capacitor. The capacitor C denotes the capacitance of the depletion region. Resistor R_l denotes the resistance of the depletion region [17]. Inductor L_a indicates the phase delay between the current and voltage caused by the impact ionization [17]. Series resistor R_a indicates reverse saturation current and field-dependent velocity [17]. R_{nw} indicates the Deep N-well resistance. R_{sub} indicates the substrate resistance. C_{sub1} denotes the capacitance between Deep N-well and P-substrate [18]. R_{sub} and C_{sub2} are caused by the parasitic effects of P-substrate [18]. The effect of the photo-generated slow carrier transit time is denoted by the current source f_{tr} [16].

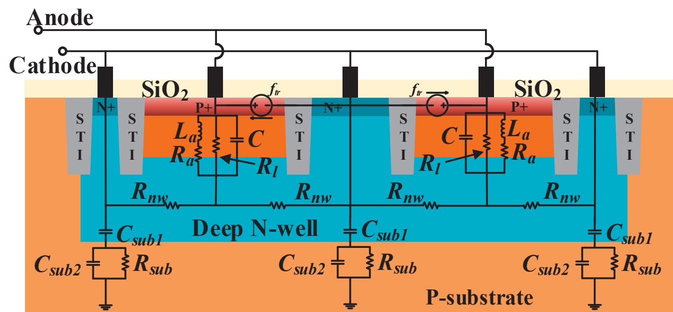
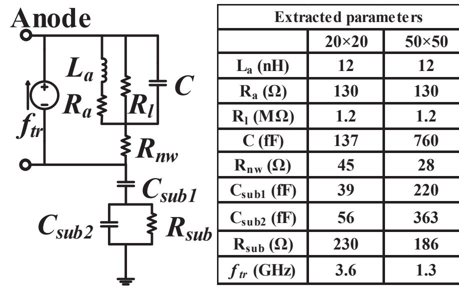


Figure 5. Simulation Program with Integrated Circuit Emphasis (SPICE) model of the CMOS APD.

Figure 6 shows the extracted parameter values for the simulation. The values of L_a, C, and R_{nw} are calculated by the following equations.

$$L_a = \tau_a/(2\alpha' I_0),\ C = \varepsilon_s A/W_D,\ R_{nw} \approx W_d/2A\varepsilon_s v_s$$

where τ_a is the transit time across the avalanche region, α' is the derivative of the ionization coefficient with respect to the electric field, I_0 is the bias current, ε_s is the semiconductor permittivity, A is the cross sectional area, W_D is the depletion region width, W_d is the drift region width, and v_s is the saturation [19].

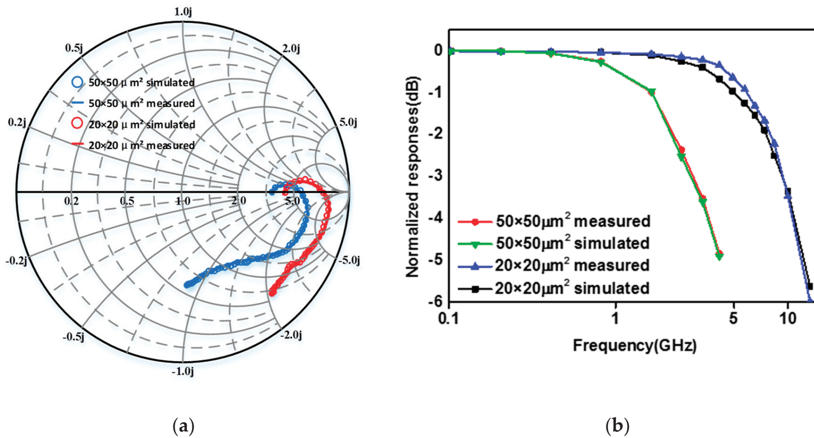


Extracted parameters		
	20×20	50×50
L_a (nH)	12	12
R_a (Ω)	130	130
R_l (MΩ)	1.2	1.2
C (fF)	137	760
R_{nw} (Ω)	45	28
C_{sub1} (fF)	39	220
C_{sub2} (fF)	56	363
R_{sub} (Ω)	230	186
f_{tr} (GHz)	3.6	1.3

Figure 6. SPICE model and the extracted parameters of the APD.

The f_{tr} is estimated as $f_{tr} \approx (1/(2\pi\tau_{tr}))$, and τ_{tr} is expressed as $\tau_{tr} \approx 4L^2/(\pi^2 D)$, where L is the diffusion length, D is the diffusion coefficient [20]. Later, these parameters will be re-corrected by the parameter fitting of the measured reflection coefficients and the frequency response.

The reflection coefficients were measured by a vector network analyzer (Agilent E8362B) under a 100 µW, 850 nm, 10 Gb/s optical signal. From the measured reflection coefficients (shown in Figure 7a), Y-parameters and Z-parameters were calculated. R_a and R_l were extracted by the calculated Z-parameters. R_a and R_l were also re-corrected by parameter fitting. Then using ADS to perform parameter fitting of SPICE model to obtain the values of other parameters and manually modify them.



(**a**) (**b**)

Figure 7. Comparison of the reflection coefficient and the frequency response between the measured and the simulated ones (**a**) reflection coefficients; (**b**) frequency response.

The extracted parameters for R_l, L_a, and R_a are the same for all prepared devices. R_l is defined as the voltage to current ratio near 0 V. The slope of the I-V characterization for all APD is shown in Figure 2, making R_l the same for prepared devices. L_a does not vary with device area at the same bias voltage, because the prepared APDs have the same avalanche multiplication characteristics based on the P-well/Deep N-well junction and guard ring as shown in Figure 2.

R_a denotes the series resistance associated with the avalanche inductor L_a, which determines the quality factor of the avalanche inductance [17]. It is not directly related to the device area. The junction capacitance C is proportional to the area. C_{sub1} and C_{sub2} are also proportional to the area. R_{nw} and R_{sub} do not change much because the increase in lateral resistance makes up for the decrease in vertical resistance.

Figure 7 shows the difference between experiment and simulation of the reflection coefficients and frequency response characterization, respectively. Based on the comparison shown in Figure 7, the simulation result based on the SPICE model coincides with the experiment ones, showing the accuracy of the proposed SPICE model.

Table 1 shows the comparison of the performance of various silicon photodetectors fabricated with standard CMOS technology. Our 20 × 20 μm^2 CMOS APD shows the responsivity with 0.56 A/W and a photodetection bandwidth of 8.4 GHz at a reverse bias voltage of 20.8 V.

Table 1. The performances of various silicon photodetectors.

Parameters	Ref. [9]	Ref. [11]	Ref. [16]	Ref. [21]	This Work
Technology	0.13 μm	0.18 μm	0.13 μm	0.13 μm	45 nm
Structure	P+/N-well SM-APD	Multiple N+/P-sub APD	P+/N-well APD	N+/P-well APD	Double P-well/Deep N-well APD
Area (μm^2)	5 × 5	50 × 50	10 × 10	30 × 30	20 × 20
Bandwidth (GHz)	12	8.7	7.6	3.5	8.4
Responsivity (A/W)	0.03	0.05	0.48	3.92	0.56
Gain	10.6	62.3	15.4	18.8	23
Bias voltage (V)	9.7	11.45	10.25	10	20.8

4. Conclusions

In this paper, an avalanche photodiode is designed and implemented based on 45 nm standard CMOS technology without any process modification. The fabricated CMOS APD shows a high response and high light detection bandwidth. Two types of CMOS APDs with different active areas are prepared, and their I-V characterization, photodetection frequency responses are examined. By reducing the active area from 50 × 50 μm^2 to 20 × 20 μm^2, the optical detection bandwidth of the prepared APD is increased to 8.4 GHz due to the decreased transit time, and the responsivity achieved 0.56 A/W. At the same time, the SPICE model of the fabricated CMOS APD device is set up for future circuit design and simulation. The key parameters based on the actual structure and the measurements are extracted. The simulation results show the accuracy of the proposed SPICE model. The proposed CMOS APDs are very useful for achieving high responsivity, and high speed 850 nm integrated optical receivers based on the standard CMOS technology.

Our future work will focus on reducing the bias voltage and power consumption of the device, while improving its photoelectric detection performance. Improving the light absorption, optimizing the doping concentration and doping depth can further improve the photoelectric detection performance of the device. Light absorption can be increased by adding an anti-reflection layer on the surface of the device. The optimization of doping concentration and doping depth requires more experiments to explore. On the other hand, optimizing the structure and parameters of the design to suit different wavelengths of photoelectric detection is also one of our future research directions.

Author Contributions: Resources, Q.Q. and P.Y.; Writing—original draft preparation, W.Z.; Writing—review and editing, W.Z. and Y.J.; Funding acquisition, P.Y. and Y.J. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Tavernier, F.; Steyaert, M.S.J. High-Speed Optical Receivers with Integrated Photodiode in 130 nm CMOS. *IEEE J. Solid-State Circuits* **2009**, *44*, 2856–2867. [CrossRef]
2. Kostov, P.; Gaberl, W.; Hofbauer, M.; Zimmermann, H. Integrated 180 nm CMOS phototransistors with an optimized responsivity-bandwidth-product. In Proceedings of the Photonics Conference, Burlingame, CA, USA, 23–27 September 2012.
3. Kim, Y.S.; Jun, I.S.; Kim, K.H. Design and Characterization of CMOS Avalanche Photodiode With Charge Sensitive Preamplifier. *IEEE Trans. Nucl. Sci.* **2008**, *55*, 1376–1380. [CrossRef]
4. Woodward, T.K.; Krishnamoorthy, A.V. 1-Gb/s integrated optical detectors and receivers in commercial CMOS technologies. *Sel. Top. Quantum Electron. IEEE J.* **1999**, *5*, 146–156. [CrossRef]
5. Sale, T.E.; Chu, C.; Hwang, J.K.; Koh, G.H.; Nabiev, R.; Tan, L.C.; Giovane, L.M.; Murty, R.M.V. Manufacturability of 850nm data communication VCSELs in high volume. *Proc. SPIE Int. Soc. Opt. Eng.* **2010**, *7615*, 761503–761510.
6. Lee, M.J.; Choi, W.Y. Performance Optimization and Improvement of Silicon Avalanche Photodetectors in Standard CMOS Technology. *IEEE J. Sel. Top. Quantum Electron.* **2017**, *24*, 1–13. [CrossRef]
7. Atef, M.; Polzer, A.; Zimmermann, H. Avalanche Double Photodiode in 40-nm Standard CMOS Technology. *IEEE J. Quantum Electron.* **2013**, *49*, 350–356. [CrossRef]
8. Huang, W.K.; Liu, Y.C.; Hsin, Y.M. A High-Speed and High-Responsivity Photodiode in Standard CMOS Technology. *IEEE Photonics Technol. Lett.* **2007**, *19*, 197–199. [CrossRef]
9. Lee, M.J. First CMOS Silicon Avalanche Photodetectors with Over 10-GHz Bandwidth. *IEEE Photonics Technol. Lett.* **2015**, *28*, 276–279. [CrossRef]
10. Iiyama, K.; Shimotori, T.; Gyobu, R.; Hishiki, T.; Maruyama, T. 10 GHz bandwidth of Si avalanche photodiode fabricated by standard 0.18 µm CMOS process. In Proceedings of the Conference on Optical Fibre Technology, Melbourne, VIC, Australia, 6–10 July 2014.
11. Chou, F.P.; Wang, C.W.; Li, Z.Y.; Hsieh, Y.C.; Hsin, Y.M. Effect of Deep N-Well Bias in an 850-nm Si Photodiode Fabricated Using the CMOS Process. *IEEE Photonics Technol. Lett.* **2013**, *25*, 659–662. [CrossRef]
12. Goy, J.; Courtois, B.; Karam, J.M.; Pressecq, F. Design of an APS CMOS Image Sensor for Low Light Level Applications Using Standard CMOS Technology. *Analog Integr. Circuits Signal Process.* **2001**, *29*, 95–104. [CrossRef]
13. Yang, G.; Cansizoglu, H.; Polat, K.G.; Ghandiparsi, S.; Kaya, A.; Mamtaz, H.H.; Mayet, A.S.; Wang, Y.; Zhang, X.; Yamada, T. Photon-trapping microstructures enable high-speed high-efficiency silicon photodiodes. *Nat. Photonics* **2017**, *11*, 301–308.
14. Kang, H.S.; Lee, M.J.; Choi, W.Y. Si avalanche photodetectors fabricated in standard complementary metal-oxide-semiconductor process. *Appl. Phys. Lett.* **2007**, *90*, 63. [CrossRef]
15. Zul, A.F.M.N.; Iiyama, K.; Gyobu, R.; Hishiki, T.; Maruyama, T. Optimizing silicon avalanche photodiode fabricated by standard CMOS process for 8 GHz operation. In Proceedings of the International Conference on Telematics & Future Generation Networks, Kuala Lumpur, Malaysia, 26–28 May 2015.
16. Lee, M.J.; Choi, W.Y. Area-Dependent Photodetection Frequency Response Characterization of Silicon Avalanche Photodetectors Fabricated With Standard CMOS Technology. *IEEE Trans. Electron Devices* **2013**, *60*, 998–1004. [CrossRef]
17. Wang, Y.C. Small-signal characteristics of a read diode under conditions of field-dependent velocity and finite reverse saturation current. *Solid-State Electron.* **1978**, *21*, 609–615. [CrossRef]
18. Ahn, Y.; Han, K.; Shin, H. A New Physical RF Model of Junction Varactors. *Jpn. J. Appl. Phys.* **2003**, *42*, 2110–2113. [CrossRef]
19. Sze, S. *Physics of Semiconductor Devices*, 2nd ed.; Wiley-Interscience: New York, NY, USA, 1981; p. 1981. [CrossRef]
20. Wang, G.; Tokumitsu, T.; Hanawa, I.; Sato, K.; Kobayashi, M. Analysis of high speed p-i-n photodiode S-parameters by a novel small-signal equivalent circuit model. *IEEE Microw. Wirel. Compon. Lett.* **2002**, *12*, 378–380. [CrossRef]
21. Nayak, S.; Ahmed, A.H.; Sharkia, A.; Ramani, A.S.; Mirabbasi, S.; Shekhar, S. A 10-Gb/s −18.8 dBm Sensitivity 5.7 mW Fully-Integrated Optoelectronic Receiver With Avalanche Photodetector in 0.13- um CMOS. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2019**, *66*, 3162–3173. [CrossRef]

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Simulation Study of Surface Transfer Doping of Hydrogenated Diamond by MoO_3 and V_2O_5 Metal Oxides

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Abstract: In this work, we investigate the surface transfer doping process that is induced between hydrogen-terminated (100) diamond and the metal oxides, MoO_3 and V_2O_5, through simulation using a semi-empirical Density Functional Theory (DFT) method. DFT was used to calculate the band structure and charge transfer process between these oxide materials and hydrogen terminated diamond. Analysis of the band structures, density of states, Mulliken charges, adsorption energies and position of the Valence Band Minima (VBM) and Conduction Band Minima (CBM) energy levels shows that both oxides act as electron acceptors and inject holes into the diamond structure. Hence, those metal oxides can be described as p-type doping materials for the diamond. Additionally, our work suggests that by depositing appropriate metal oxides in an oxygen rich atmosphere or using metal oxides with high stochiometric ration between oxygen and metal atoms could lead to an increase of the charge transfer between the diamond and oxide, leading to enhanced surface transfer doping.

Keywords: surface transfer doping; 2D hole gas (2DHG); diamond; MoO_3; V_2O_5

1. Introduction

Diamond has many electronic applications, such as microwave electronic devices [1], bipolar junction transistor [2], and Schottky diodes [3]. However, one of the most promising areas for diamond industrial application is high-performance field effect transistors (FETs) in the production of high frequency and high-power electronic devices [4]. Its properties potentially enable devices that are beyond the scope of current systems in terms of operating frequency, power handling capacity, operating voltage, thermal robustness, and operating environment. This is due to the fact that the diamond has a wide band-gap of 5.5 eV, a thermal conductivity five times greater than 4H–SiC of 24 W/cm·K (for CVD diamond), a high breakdown field of 20 $W{\cdot}cm^{-1}$, and high hole and electron carrier velocities of 0.8×10^7 cm/s and 2.0×10^7 cm/s, respectfully; making it a superior new candidate for high frequency and high power devices [5–9]. However, the primary issue that has inhibited the application of diamond in the production of mature electronic devices is the lack of a suitably efficient and stable doping mechanism. It is well known that conventional substitutional doping is difficult to achieve in diamond in comparison to other semiconductor materials, such as Si and III-Vs [10]. It is possible to dope diamond with some atoms; however, boron being the most common and successful. Boron doping has its limitations; however, the hole mobility deteriorates as the doping concentration increases and when the doping concentration rises above 3.9×10^{21} cm^{-3} the diamond takes on semi metallic properties [11,12].

Surface Transfer Doping (STD) provides an alternative doping strategy that overcomes the intrinsic limitations that are associated with substitutional doping in diamond and, hence, presents a potential solution for the production of viable electronic devices [13,14]. For STD to occur in diamond, there are

two main prerequisites: hydrogen termination of the diamond surface (H-diamond) and an electron accepting material in intimate contact with the H-diamond surface. The hydrogen termination gives the diamond surface a negative electron affinity, which facilitates the transfer of electrons from the diamond valance band to the surface electron accepting material, creating a quasi two-dimensional sub-surface hole gas (2DHG) in the diamond.

Figure 1 shows the current model for the band bending mechanism in H-diamond when it comes into intimate contact with an electron acceptor material.

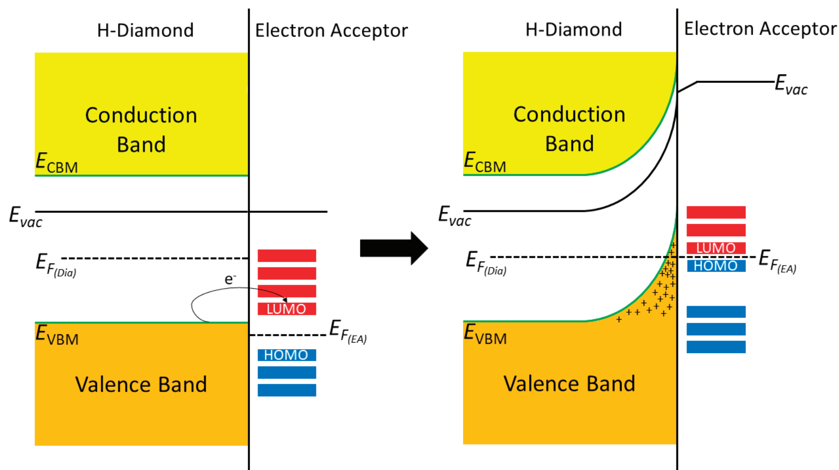

Figure 1. Band diagrams showing the interaction of hydrogen terminated diamond with a surface electron acceptor material.

In the earliest developments of STD, the electron acceptor material was provided by molecules in the atmosphere that spontaneously adsorbed onto the surface of hydrogen-terminated diamond [15]. However, the lack of control over the adsorption of the atmospheric species, and the fact they are readily desorbed by elevated temperatures and fabrication processes, led to research into alternative electron acceptors that are controllable, more stable, and provide improved performance. The first experimental work to use alternative surface electron acceptors was by Strobel et al., who used high electron affinity molecules C_{60} and $C_{60}F_{48}$ in 2004 and 2005, respectively [16,17], with Edmonds et al. revisiting the use of $C_{60}F_{48}$ in 2012 [18]. In 2007, Qi et al. implemented the use of the strong electron withdrawing molecule F_4-TCNQ as the surface acceptor to induce STD in H-diamond reporting areal hole density of 1.6×10^{13} cm^{-2} [19]. However, these alternative dopants were found to result in lower carrier concentrations than atmospheric adsorbates and were unstable at elevated temperatures, despite offering improved controllability of adsorbate on the H-diamond surface. High electron affinity metal oxides have been utilised as surface acceptor materials in order to improve the device stability and enhance the carrier concentration in the surface transfer doped H-diamond. Two of the metal oxides that have been shown in previous experimental studies to improve the performance and stability of STD in H-diamond are MoO_3 and V_2O_5 [13,14,20–27].

Figure 2 presents a schematic diagram and the conceptual idea showing that when a metal oxide with suitably high electron affinity (~4.3 eV) is deposited on an H-diamond surface, electrons from just below the surface of the diamond will transfer to the metal oxide creating the 2DHG in the diamond. The higher the number of electrons extracted from the diamond substrate to the electron acceptor material, the higher the hole concertation of the 2DHG, which, in turn, reduces resistance and increases maximum current in electrical devices. Hence, it is desirable to maximise the charge transfer density from the diamond to the electron acceptor. Such an optimization of charge transfer is

highly challenging when utilising randomly adsorbed species from ambient air on to the H-diamond surface. The species also prove to be unstable at elevated temperatures and offer poor device reliability. Therefore, the optimisation of the composition and structure of thin metal oxide films as alternative electron acceptor layers provides greater potential for engineering the STD process in diamond, and it can result in more robust thermal stability and device reliability.

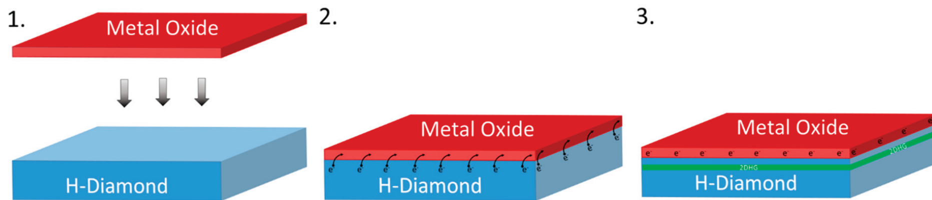

Figure 2. The creation of the two-dimensional sub-surface hole gas (2DHG) just below the diamond surface after interfaced with a suitable metal oxide.

When compared to the progress and publication of experimental work, there has been little theoretical investigation into the STD of H-diamond. In the past, ab-initio and Density Functional Theory (DFT) first principal studies have been carried out to model the types of interactions and transfer doping that occurs in the atmosphere by modelling molecules, such as HCl, NH_3, H_2O, NO_2, NO, and O_3 on H-diamond [28–30]. Until very recently, there has been a lack of theoretical investigation into metal oxide and H-diamond interfaces. Xiang et al. and Xing et al. investigated the STD between H-diamond and molecules of CrO_3 and MoO_3, respectively, while using DFT methods. The publications reported estimated carrier concentrations of 4.7×10^{13} cm^{-2} and 9.83×10^{13} cm^{-1} for MoO_3 and CrO_3 molecules, correspondingly [27,31].

In this work, we present DFT simulations of STD in H-diamond using automictically thin surface layers of both MoO_3 and V_2O_5 in order to investigate these charge transfer processes and obtain detailed scientific understanding of the charge transfer phenomena in such kind of systems. The interfaces of (100) α-MoO_3 and (100) V_2O_5 with 2×1-(100) H-diamond have been modelled and resultant STD analysed with a view to better understanding and optimising STD in the diamond. Although similar DFT studies have already been reported for CrO_3 and MoO_3 molecular clusters on diamond, this work models extended crystalline thin film structures that could better represent real experimental conditions.

2. Materials and Methods

All of the calculations were carried out with Quantumwise Atomistix ToolKit (ATK) software (2017, Copenhagen, Denmark) while using the DFT method [32]. Generalised Gradient Approximation (GGA) exchange correlation was used for the geometry optimisations of all systems and obtain the total energies of the interfaced systems and the individual component parts i.e. H-diamond and the oxide layer in question. For all geometry optimisations, a force tolerance of 0.01 eV/Å was used. GGA-1/2 exchange correlation was used for all electronic structure calculations. The pure DFT method is well known for underestimating the bandgap of semiconductors. Therefore, the DFT-1/2 method was used to obtain a more accurate electronic description of the systems. The DFT-1/2 method is a semi-empirical approach that can overcome the error that local and semi-local exchange correlation density functionals inherently have when working with semiconductors and insulators. It works by correcting the self-interaction error of DFT by cancelling out the electron-hole self-interaction energy by defining an atomic self-energy potential [33]. However, the DFT-1/2 method is not suitable for calculating properties that depend on total energy; hence, we used GGA for the geometry optimisations and calculating adsorption energies. The Perdew, Burke, and Ernzerhof (PBE) functional was chosen

for all calculations, because of the good match with experimental data (around 5.5 eV) regarding the value on the band gap in bulk diamond, as shown in Table 1.

Table 1. Bandgaps produced for bulk diamond by different functionals using Generalised Gradient Approximation (GGA)-Half exchange correlation. Perdew, Burke, and Ernzerhof (PBE) was chosen, because it agreed with the experimental value of 5.5 eV.

Functional	Bulk Diamond Bandgap (eV)
BLYP	5.83
BP86	5.68
BPW91	5.63
PBES	5.42
PW91	5.62
RPBE	5.64
XLYP	5.86
PBE	5.59

A Monkhorst-Pack scheme with an $8 \times 8 \times 1$ k-point density (Å) mesh was used for the Brillouin zone integration. An iteration control tolerance of 0.0001 with a density cut off of 1×10^{-6} was used for all calculations with a medium basis set. The number of pseudo-atomic orbitals in a medium basis set is typically comparable to that of a double-zeta polarized (DZP) basis set [34]. The pseudopotential is SG15 and the density mesh cut-off is 185Ha, which gives high accuracy with a medium computational efficiency.

The H-diamond, MoO_3, and V_2O_5 were created and geometry optimised individually by allowing all of the atoms to fully relax. After this optimisation, the H-diamond and the metal oxide structures were interfaced and a geometry optimisation process was performed by fixing the diamond structure while allowing for the oxides to move as a rigid body in all directions. The interface distances were corrected for counterpoise basis set superposition error and Van der Waals interactions. In this way, the computational cost is significantly reduced, as the surface atoms of the two structures were not fully relaxed independently. When the oxides were interfaced with the 2×1-(100) H-diamond, a strain of <1% was placed on the MoO_3 and 1.02% was placed on the V_2O_5.

3. Results

3.1. MoO_3: H-Diamond Interface

Figure 3 compares diamond, hydrogen terminated diamond and MoO_3 band structures and Density of States (DOS) obtained from the unit cell and super cell DFT simulations. The lattice parameters of the three systems in Figure 3, are: (a) bulk diamond—face centered cubic a = 3.574 Å, (b) hydrogen terminated diamond—super cell lattice type a = 2.527 Å, b = 10.108 Å, c = 27Å (the unit cell for the hydrogen terminated 2×1 diamond is a = 2.527 Å, b = 5.054 Å and it is in agreement with the experimental values of 2.52 Å and 5.04 Å [35]), MoO_3—simple orthorhombic a = 3.962 Å, b = 13.86 Å, c = 3.697 Å. The data that are presented in Figure 3a,b show that, when diamond is hydrogen terminated, the band gap is slightly reduced at the surface due to surface gap states at the valance band maximum (VBM) and conduction band minimum (VBM), because of the presence of hydrogen atoms—the most prominent additional bands from the C–H interaction at the VBM have been highlighted in green in Figure 3b. This is due to the bonding and antibonding C–H states at the VBM and CBM [36]. Although the band gap of the system has been reduced to 4.50 eV, which is shown in Figure 3b, the projected DOS plot for the carbon atoms in the bulk of the structure shows their band gap remains ~5.5 eV. The first two valance sub-bands in Figure 3b, which clearly have higher energies in comparison to the other sub-bands, arise from the interaction of the first layer of carbon with the adjacent hydrogen atoms. If these two sub-bands are ignored the band gap for diamond remains ~5.5 eV.

The band gap of 2.84 eV that is obtained for MoO_3 (Figure 3c) is comparable to reported experimental values of 3.2 eV and 2.8 eV for bulk and polycrystalline MoO_3, respectfully, obtained by absorption spectra measurements [37]. Thermally evaporated MoO_3 (as utilised in previous experimental work [20,26]) forms an amorphous film and, therefore, does not have a well-defined crystal structure. In our simulations, the MoO_3 is built as a perfect crystal and it is most likely the reason that the band gap obtained from the DFT is underestimated in the comparison to the reported experimental values.

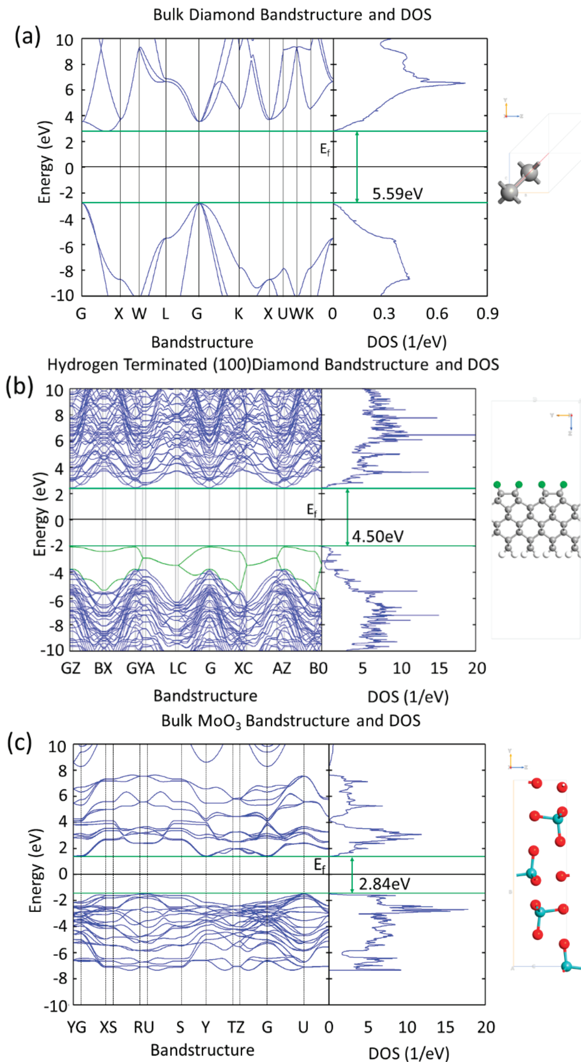

Figure 3. (**a**) Bandstructure and Density of States (DOS) of bulk diamond showing a band gap of 5.59 eV, (**b**) bandstructure and DOS of hydrogen terminated (100) diamond showing a reduced band gap of 4.50 eV due to the highlighted green hydrogen atoms, and (**c**) bandstructure and DOS of bulk MoO_3 showing a band gap of 2.84 eV.

We calculated the optical spectrum of bulk diamond and plotted the dielectric constant to compare our results to a recent theoretical study by Xiang et al and experimental data published by Philipp and Taft to further validate the reliability of our calculation parameters [31,38]. The comparison plots for the real and imaginary parts of the dielectric constant in Figure 4 shows that our DFT method produces results that are in good agreement with other published theoretical work and experimental data.

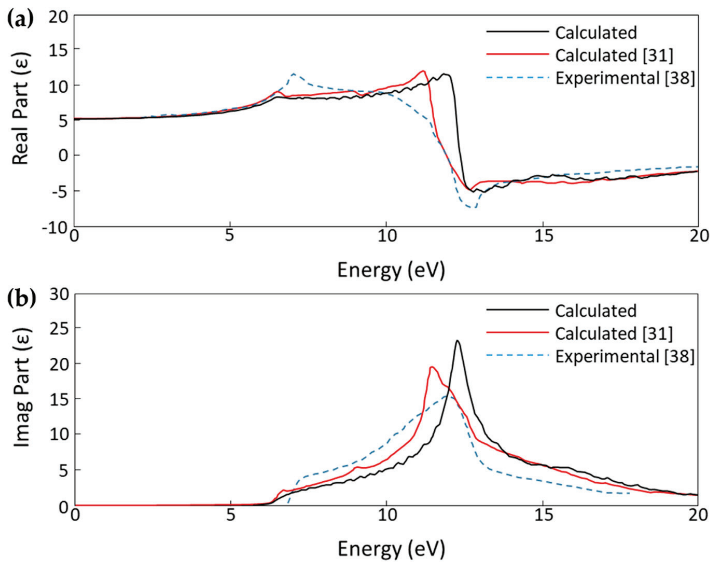

Figure 4. (**a**) Real part and (**b**) imaginary part of the calculated dielectric constant (ε) plots for bulk diamond comparing our calculated results with calculated results by Xiang et al. and experimental results by Philipp and Taft [31,38].

After the H-diamond and MoO_3 units had been fully geometrically optimised, they were interfaced with a strain of <1% being placed on the MoO_3. To geometrically optimise the interface separation, the H-diamond atoms were fixed, while the MoO_3 atoms were kept rigid, allowing for the oxide to move as one unit in the x, y, and z directions. The lattice parameters for the super cell were a = 60.861 Å, b = 7.581 Å, and c = 30.962 with a vacuum of 19 Å.

Figure 5 shows the projected Density of States (PDOS) for the '1s' electron shells of the hydrogen and the '2p' electron shells of the carbon atoms before and after the H-diamond has been interfaced with MoO_3. From the top plot of Figure 5 is clear that, the pure bulk H-diamond still has a band gap of around ~5.5 eV.

The PDOS diagram reveals that, when the H-diamond is in contact with the MoO_3, there is a shift of the PDOS to higher energies and the Fermi Level (E_F) is in contact with the valence states. Moreover, the band gap of the diamond remains constant, but states of the Valance Band Maximum (VBM) have crossed the Fermi Level, which in turn means that charge transfer has occurred, as previously occupied states within the H-diamond are now vacant. This demonstrates that the electrons transferred from the diamond surface to the MoO_3 layer, leaving the hole accumulation layers, as expected from the STD model. Or, in other words, the shift of the E_F from the middle of the bandgap toward the VBM also indicates p-type doping of the H-diamond. This is consistent with the recent experimental and simulation results that were published by other groups [27].

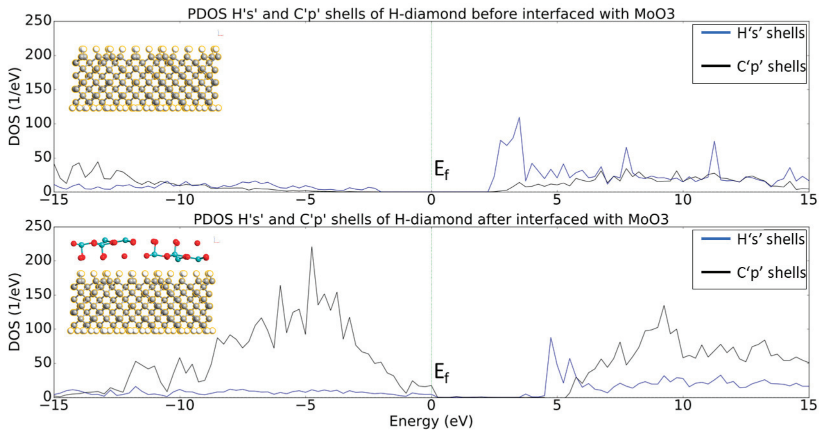

Figure 5. Projected Density of States (PDOS) plots of Hs and Cs shells before and after the H-diamond is interfaced with the oxide. The images inset are two-dimensional (2D) cuts in the middle of the systems just to show what atoms are being projected in the PDOS plots.

The PDOS plot presented in Figure 6 shows the opposite trend regarding the band structure in comparison to the PDOS data for the diamond, which is consistent with the discussion in the previous paragraph. More specifically, the Mo_d and O_p shells have increased states that lie below the Fermi level after the MoO_3 has been interfaced with the H-diamond, indicating that there has been charge transfer at the interface. Indeed, this charge transfer corresponds to an acceptance of electrons by the metal oxide from the diamond substrate.

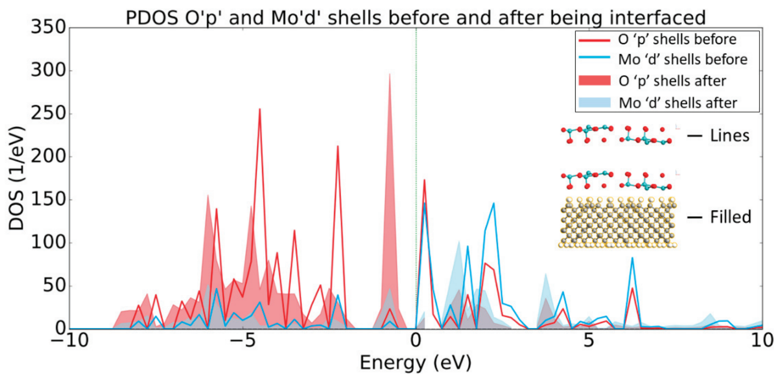

Figure 6. PDOS plot of O_p and Mo_d shells before (lines) and after (filled) being interfaced with the H-diamond. Inset are two-dimensional (2D) crops of the systems being shown in the PDOS, showing that the line and filled plots denote the MoO_3 before and after being interfaced, respectfully.

Additional to the PDOS data, we have analyzed the Mulliken charges and electron density differences of the interfaced system. The analysis of the Mulliken electron population of the system presented in Table 2 showed that electron density had transferred from the first four layers of the H-diamond to the MoO_3, with negligible change to the electron density of the atoms deeper within the diamond. Consistent with the results that are presented in Table 2 is the image in Figure 7, which shows the electron density change for the MoO_3:H-diamond interface. The green regions show where there is a loss of electron density and thus the accumulations of holes, and the purple regions show

where there is an increase in electron density. The electron density difference isosurface shows that there is a hole accumulation that occurs near the surface of the diamond, while most of the electron density gained by the MoO_3 clearly migrates to the oxygen atoms. Figure 7 and Table 2 are clear representations that the H-diamond loses electrons from the layers closest to the surface, showing that a 2DHG created by surface transfer doping has been formed in the H-diamond. Most of the charge transferred to the MoO_3 migrates to the oxygen atoms, rather than the molybdenum atoms with a total transfer of 3.6 electrons from the H-diamond to the MoO_3. Moreover, these results are in very good agreement with work by K. Xing et al., where they also demonstrate electron transfer from the H-diamond to the oxide [27].

Table 2. The calculated Mulliken charges for the MoO3-doped diamond surface.

Material	Before Adsorption	After Adsorption	Change in Mulliken Charge
H-Diamond	1680.0	1676.4	−3.6
MoO_3	767.9	771.5	3.6
Mo	286.7	288.2	1.5
O	481.2	483.3	2.1
Surface H Layer	48.4	38.2	−10.2
First Carbon Layer	198.9	203.0	4.1
Second Carbon Layer	188.7	190.8	2.1
Third Carbon Layer	189.8	190.3	0.5
Bottom H Layer	95.5	95.0	−0.5

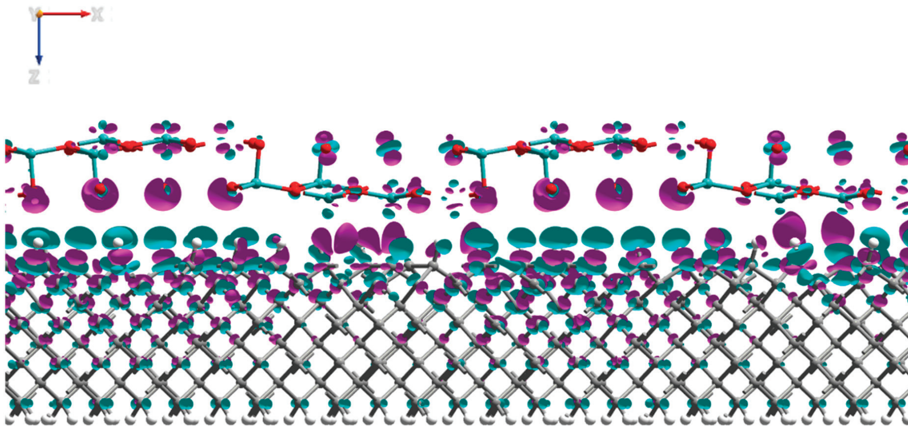

Figure 7. Side view of the MoO_3:H-diamond interface structure showing the electron density differences. The purple regions represent electron accumulation and the green regions represent electron depletion (hole accumulation). The isosurface values are ±0.002 $Bohr^{-3}$.

Of the total electron density transferred to the oxide film, the oxygen atoms gain 2.1 electrons and the molybdenum atoms gain 1.5 electrons. The carrier concentration of the H-diamond would be ~6×10^{13} cm^{-2}, given that the surface area of the system was ~60 Å × 10 Å, calculating the charge transfer per cm^2. This is within the range of previously reported experimental carrier concentrations for MoO_3 that was deposited on the surface of H-diamond substrates of 4×10^{12}–1×10^{14} cm^{-2} [20–22,25,26]. Additionally, it is in very good agreement with the extracted from in-situ four-probe measurements hole density value of 2.7×10^{13} cm^{-2} and calculated charge transfer per unit cell of 4.7×10^{13} cm^{-2} for a monolayer coverage of MoO_3, reported by K. Xing et al [27].

Hence, to summarise, our simulations and analysis reveal that the MoO_3 attracts electrons from the hydrogen terminated diamond in the interfaced system and there is charge transfer between the diamond and the oxide and, as a result, the diamond is p-type and the oxide is n-type doped.

3.2. V_2O_5: H-Diamond Interface

In order to further verify our findings regarding charge transfer to MoO_3, we have performed simulations of another oxygen rich oxide experimentally shown to produce STD in H-diamond—V_2O_5 [13,23–26]. We utilized the same H-diamond cell used for the H-diamond:MoO_3 system and interfaced it with a fully relaxed V_2O_5 unit cell, placing a strain of 1.02% on the V_2O_5 to create the H-diamond:V_2O_5 interface. The super cell lattice parameters were a = 39.231 Å, b = 12.636 Å, c = 50, with a vacuum of 36 Å. The interface was optimised by the same process that was used for the H-diamond:MoO_3 interfacial distance and position.

Figure 8 depicts the bandstructure and DOS calculated for bulk V_2O_5. The band gap calculated is 2.76 eV, which is comparable to the optical bandgap of 2.8 eV reported for 100 nm thick thermally evaporated V_2O_5 films [39].

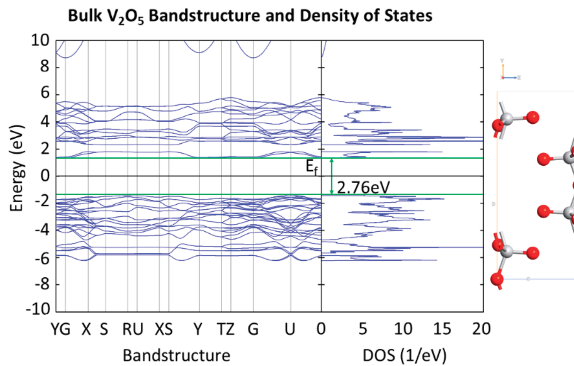

Figure 8. Bandstructure and DOS of bulk V_2O_5 showing a band gap of 2.76 eV.

Figure 9 shows the PDOS for the '1s' electron shells of the hydrogen and the '2p' electron shells of the carbon atoms before and after the H-diamond has been interfaced with V_2O_5. When H-diamond is interfaced with V_2O_5 there is a shift of the PDOS of the diamond to higher energies with some states now crossing the Fermi Level (E_F). Indeed, this is very similar to the observed trend when the H-diamond is interfaced with MoO_3, where the VBM is in contact with the E_F. This suggests that the diamond has lost electrons as states in the diamond that were occupied before being interfaced, are now vacant. The gap between the VBM and CBM remains the same as the diamond's bulk band gap value. Additionally, Figure 9 reveals a similar trend regarding the DOS movement to the results that are shown in Figure 5. Indeed, the E_F has moved closer to VBM, which indicated that there has been charge transfer at the interface and that the H-diamond has been p-type doped.

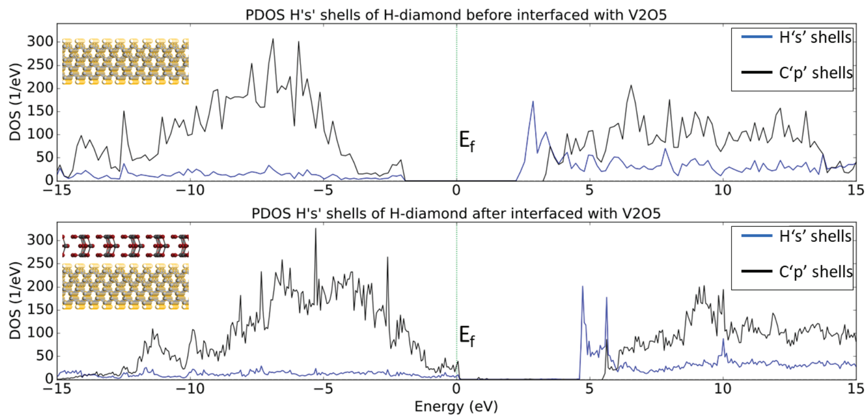

Figure 9. PDOS plots of Hs and Cs shells before and after the H-diamond is interfaced with V_2O_5. The images inset are 2D cuts in the middle of the systems just to show what atoms are being projected in the PDOS plots.

The PDOS presented in Figure 10 shows that the O_p and V_d shells have increased states that lie below E_F after being interfaced with the H-diamond, much in the same way that the O_p and Mo_d shells did. This result suggests that the Vanadium Pentoxide acts in a similar way to the Molybdenum Trioxide to create a 2DHG in the H-diamond when in direct contact with the metal oxide.

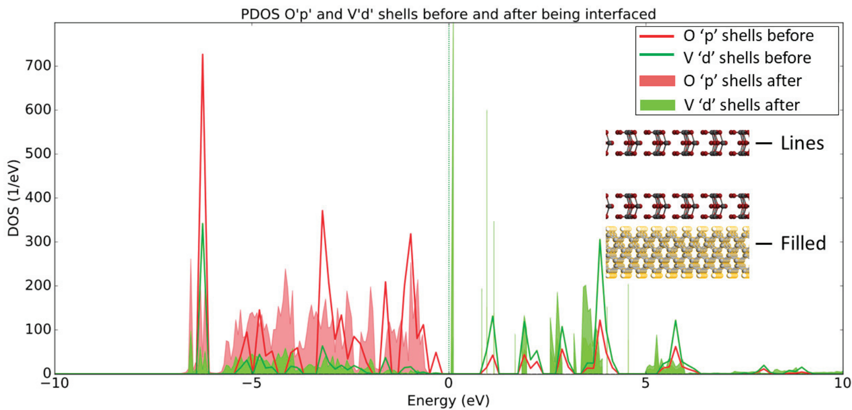

Figure 10. PDOS plot of O_p and V_d shells before (lines) and after (filled) being interfaced with the H-diamond. Inset are 2D crops of the systems being shown in the PDOS, showing that the line and filled plots denote the MoO_3 before and after being interfaced, respectfully.

When the Mulliken electron population (Table 3) of the interfaced system was compared to the charges of the H-diamond and V_2O_5 individually, it showed that there was a charge transfer of 5.1 electrons from the top four layers of the H-diamond to the oxide, again with negligible transfer propagating from deeper within the H-diamond (Figure 11), showing a 2DHG, as observed with the MoO_3.

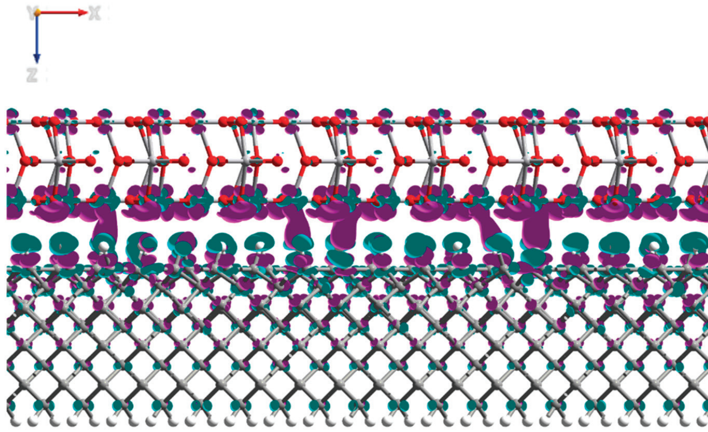

Figure 11. Side view of the V_2O_5:H-diamond interface structure showing the electron density differences. The purple regions represent electron accumulation and the green regions represent electron depletion (hole accumulation). The isosurface values are ±0.0025 $Bohr^{-3}$.

Table 3. The calculated Mulliken charges for the MoO3-doped diamond surface.

Material	Before Adsorption	After Adsorption	Change in Mulliken Charge
H-Diamond	2519.9	2514.8	−5.1
V_2O_5	1343.6	1348.7	5.1
V	520.4	520.6	0.2
O	823.2	828.1	4.9
Surface H Layer	72.4	55.2	−17.2
First Carbon Layer	298.4	305.4	7.0
Second Carbon Layer	283.0	287.1	4.1
Third Carbon Layer	284.7	285.8	1.1
Bottom H Layer	143.3	142.7	−0.6

Similar to the MoO_3, most of the charge transferred migrated to the O atoms in the V_2O_5 as opposed to the V atoms, with an electron density gain of 4.9 and 0.2 for the O and V atoms, correspondingly, see Table 3. Although there was slightly more charge transfer than was observed for MoO_3, the supercell for the V_2O_5:H-diamond system is slightly larger. This meant, when considering the surface area of the system, the calculated carrier concentration per cm^2 created by the V_2O_5 was 2.17×10^{13} cm^{-2}, which, in turn, is slightly less than the carrier concentration seen with MoO_3. The experimental carrier concentration of H-diamond with a thin film of V_2O_5 thermally deposited on the surface, by means of Hall measurements, is measured to be 1.8×10^{13} cm^{-2} [13]. Previous experimental result on H-diamond:V_2O_5 of reported values in the range of 1.8×10^{13} cm^{-2}–1.1×10^{14} cm^{-2}, agree with the carrier concentration we have obtained from our DFT simulations [23–26]. Hence, our results demonstrate that V_2O_5 acts as highly efficient surface acceptor for modulating the carrier concentration and, hence, surface conductivity of the hole conducting channel on diamond.

3.3. MoO_3 and V_2O_5 Comparison

Figure 12 presents an energy band diagram for H-diamond, MoO_3, and V_2O_5 materials relative to the vacuum level (E_{VAC}). In terms of the relation of the VBM in diamond and CBM positions of the oxides both oxides should interact similarly with the diamond substrate. For an adsorbate to accept electrons and, therefore, inject holes into the H-diamond it must have a CBM that lies below the VBM of the H-diamond. The CBM of both oxides are at approximately the same energy level below the VBM

of the diamond and, therefore, it is expected that both oxides will yield similar results when they are interfaced with H-diamond.

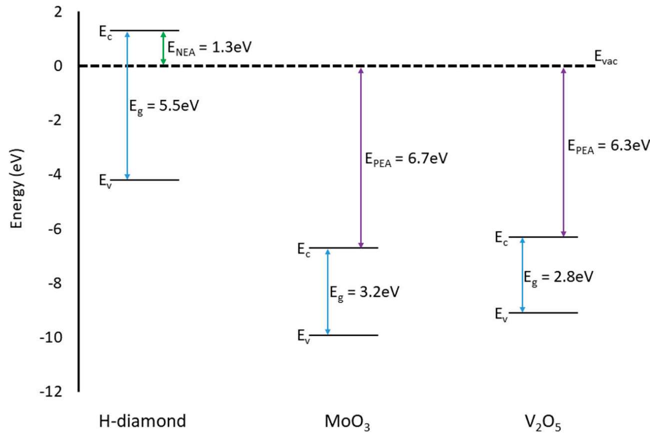

Figure 12. Energy band diagram showing the VBM and CBM positions for H-diamond (left hand side), MoO_3 (middle), and V_2O_5 (right hand side) [30,40,41].

To evaluate the interaction between the H-diamond and the oxides, adsorption energies for both oxides were calculated using the following formula:

$$E_{adsorption} = E_{H-diamonds/oxide} - E_{H-diamond} - E_{oxide} \quad (1)$$

$E_{H\text{-}diamond/oxide}$ is the total energy of the interfaced H-diamond and oxide system. $E_{H\text{-}diamond}$ and E_{oxide} are the energies of the individual components of the interfaced system. Therefore, the adsorption energy is the difference in energy between the whole interfaced system and each individual component: H-diamond and the oxide. The adsorption energies for both oxides, as listed in Table 4, were negative values, which indicate that both processes are driven by a favorable exothermic reaction. Hence, both oxides can be physically absorbed (physisorption) on the diamond surface. We believe that the process is physisorption instead of chemical absorption, because the only one 1s H electrons and the free 2p electron from the C atoms from the diamond surface form a stable covalent bond. Hence, there is no free electron for the H atom to create a chemical bond with either the transition metal or the oxygen from the metal oxide.

Table 4. Adsorption energies corresponding to the two different oxides on H-diamond.

Adsorbate	Adsorption Energy (eV)
MoO_3	−2.94
V_2O_5	−6.41

However, it can also be said that the adsorption energy is not responsible for increased charge transfer, given that the adsorption energy of the MoO_3 is more than two times weaker than the V_2O_5, yet promotes greater charge transfer at the interface. It appears that the most important factor in the amount of charge transfer between H-diamond and the two oxides is the amount of O atoms present in the metal oxide, since, in both cases, this is where the majority of the electron density transferred at the interface migrates. Hence, our result would indicate that, in order to improve the charge transfer and, in turn, increase the carrier concentration in the H-diamond, it would be advantageous to use oxides that have a higher oxygen concentration.

Moreover, metal oxide films are usually deposited onto H-diamond in a vacuum, which can lead to the formation of oxygen deficient amorphous oxide films. Therefore, we hypothesise that depositing the oxides in an oxygen rich atmosphere or using oxides that have a higher oxygen concentration could lead to increased charge transfer and enhanced STD.

4. Discussion

In this work, we investigated models for the surface transfer doping effect induced in hydrogen-terminated diamond when interfaced with MoO_3 and V_2O_5. We simulated the interfaces of the hydrogen-terminated (100) diamond surface with (100) MoO_3 and (100) V_2O_5 while using DFT calculations. The PDOS data show there is a shift of the VBM and CBM bands when the H-diamond is interfaced and, thus, a transfer of electrons from the H-diamond to the metal oxides. MoO_3 and V_2O_5 are both found to readily act as electron acceptors and create a 2DHG in the H-diamond. The carrier concentration in the H-diamond has been calculated using DFT simulations to be 6×10^{13} cm^{-2} and 2.17×10^{13} cm^{-2} for MoO_3 and V_2O_5, respectfully, which are similar to the previously reported experimental values. These values are in good agreement with the range of experimental and simulation studies reported thus far, but underestimate the highest 2DHG carrier concentration values reported to date for these systems. Further refinement of these models to account for variation in surface morphology and hydrogen/oxygen coverage of the diamond surface as well as crystallinity/stoichiometry of the oxide layers will allow for finer optimisation of these models and provide a deeper understanding of the complex charge transport mechanisms at the hydrogen-terminated diamond surface.

However, from these simulations, it is clear that the oxygen atoms play a major role in the amount of charge transfer from the hydrogenated diamond to the metal oxide layers as the majority of the electron density transferred from the diamond migrates to the oxygen atoms. These results suggest that either depositing the metal oxide layers in an oxygen-rich atmosphere to reduce oxygen deficient oxide layers, or the investigation of new acceptor adsorbates with higher oxygen concentrations could lead to improved surface transfer doping in diamond. Moreover, our simulations show that, after depositing MoO_3 and V_2O_5 on the H-diamond surface, the metal oxides show metallic behaviors due to the fact that the Fermi level is inside of the valence band. This observation is consistent with very recent experimental work that was conducted at low temperature, which proves that that MoO_3/V_2O_5 doped H-diamond systems will show a metallic behavior rather than carrier freeze out at cryogenic temperature regime [42]. Hence, this allows for the observation of some exotic quantum transport phenomena, such as phase-coherent backscattering.

Author Contributions: Conceptualization, J.M.; methodology, J.M.; software, J.M. writing—original draft preparation, J.M.; writing—review and editing, V.P.G.; supervision, V.P.G.; funding acquisition, V.P.G. All authors have read and agreed to the published version of the manuscript.

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References

1. Trew, R.J.; Yan, J.; Mock, P.M. The potential of diamond and SiC electronic devices for microwave and millimeter-wave power applications. *Proc. IEEE* **1991**, *79*, 598–620. [CrossRef]
2. Willander, M.; Friesel, M.; Wahab, Q.-U.; Straumal, B. Silicon carbide and diamond for high temperature device applications. *J. Mater. Sci. Mater. Electron.* **2006**, *17*, 1. [CrossRef]
3. Wort, C.; Balmer, R. Diamond as an Electronic material. *Mater. Today* **2008**, *11*, 22–28. [CrossRef]
4. Liu, J.; Ohsato, H.; Wang, X.; Liao, M.; Koide, Y. Design and fabrication of high-performance diamond triple-gate field-effect transistors. *Sci. Rep.* **2016**, *6*, 34757. [CrossRef] [PubMed]

5. Russell, S.; Sharabi, S.; Tallaire, A.; Moran, D.A.J. RF Operation of Hydrogen-Terminated Diamond Field Effect Transistors. *IEEE* **2015**, *62*, 751–756.
6. Kitabayashi, Y.; Kudo, T.; Tsuboi, H.; Yamada, T.; Xu, D.; Shibata, M.; Matsumura, D.; Hayashi, Y.; Syamsul, M.; Inaba, M.; et al. Normally-Off C–H Diamond MOSFETs With Partial C–O Channel Achieving 2-kV Breakdown Voltage. *IEEE Electron Device Lett.* **2017**, *38*, 363–366. [CrossRef]
7. Isberg, J. Diamond Electronic Devices. *AIP Conf. Proc.* **2010**, *1292*, 123–128. [CrossRef]
8. Hirama, K.; Takayanagi, H.; Yamauchi, S.; Jingu, Y.; Umezawa, H.; Kawarada, H. High-performance p-channel diamond MOSFETs with alumina gate insulator. In Proceedings of the 2007 IEEE International Electron Devices Meeting, Washington, DC, USA, 10–12 December 2007; pp. 873–876.
9. Kawarada, H.; Yamada, T.; Xu, D.; Tsuboi, H.; Kitabayashi, Y.; Matsumura, D.; Shibata, M.; Kudo, T.; Inaba, M.; Hiraiwa, A. Durability-enhanced two-dimensional hole gas of C-H diamond surface for complementary power inverter applications. *Sci. Rep.* **2017**, *7*, 42368. [CrossRef]
10. Zhou, D.; Krauss, A.R.; Qin, L.C.; McCauley, T.G.; Gruen, D.M.; Corrigan, T.D.; Chang, R.P.H.; Gnaser, H. Synthesis and electron field emission of nanocrystalline diamond thin films grown from N2/CH4 microwave plasmas. *J. Appl. Phys.* **1997**, *82*, 4546–4550. [CrossRef]
11. Yokoya, T.; Nakamura, T.; Matsushita, T.; Muro, T.; Takano, Y.; Nagao, M.; Takenouchi, T.; Kawarada, H.; Oguchi, T. Origin of the metallic properties of heavily boron-doped superconducting diamond. *Nature* **2005**, *438*, 647. [CrossRef]
12. Ekimov, E.A.; Sidorov, V.A.; Bauer, E.D.; Mel'nik, N.N.; Curro, N.J.; Thompson, J.D.; Stishov, S.M. Superconductivity in diamond. *Nature* **2004**, *428*, 542. [CrossRef]
13. Crawford, K.G.; Cao, L.; Qi, D.; Tallaire, A.; Limiti, E.; Verona, C.; Wee, A.T.S.; Moran, D.A.J. Enhanced surface transfer doping of diamond by V_2O_5 with improved thermal stability. *Appl. Phys. Lett.* **2016**, *108*, 042103. [CrossRef]
14. Ren, Z.; Zhang, J.; Zhang, J.; Zhang, C.; Yang, P.; Chen, D.; Li, Y.; Hao, Y. Research on the hydrogen terminated single crystal diamond MOSFET with MoO3 dielectric and gold gate metal. *J. Semicond.* **2018**, *39*, 074003. [CrossRef]
15. Maier, F.; Riedel, M.; Mantel, B.; Ristein, J.; Ley, L. Origin of Surface Conductivity in Diamond. *Phys. Rev. Lett.* **2000**, *85*, 16. [CrossRef] [PubMed]
16. Strobel, P.; Riedel, M.; Ristein, J.; Ley, L. Surface transfer doping of diamond. *Nature* **2004**, *430*, 439–441. [CrossRef]
17. Strobel, P.; Riedel, M.; Ristein, J.; Ley, L.; Boltalina, O. Surface transfer doping of diamond by fullerene. *Diam. Relat. Mater.* **2005**, *14*, 451–458. [CrossRef]
18. Edmonds, M.T.; Wanke, M.; Tadich, A.; Vulling, H.M.; Rietwyk, K.J.; Sharp, P.L.; Stark, C.B.; Smets, Y.; Schenk, A.; Wu, Q.H.; et al. Surface transfer doping of hydrogen-terminated diamond by C60F48: Energy level scheme and doping efficiency. *J. Chem. Phys.* **2012**, *136*, 124701. [CrossRef] [PubMed]
19. Qi, D.; Chen, W.; Gao, X.; Wang, L.; Chen, S.; Loh, K.P.; Wee, A.T.S. Surface Transfer Doping of Diamond (100) by Tetrafluoro-tetracyanoquinodimethane. *J. Am. Chem. Soc.* **2007**, *129*, 8084–8085. [CrossRef]
20. Russell, S.; Cao, L.; Qi, D.; Tallaire, A.; Crawford, K.; Wee, A.; Moran, D.A.J. Surface transfer doping of diamond by MoO3: A combined spectroscopic and Hall measurement study. *Appl. Phys. Lett.* **2013**, *103*, 20. [CrossRef]
21. Vardi, A.; Tordjman, M.; Alamo, J.A.d.; Kalish, R. A Diamond:H/MoO3MOSFET. *IEEE Electron Device Lett.* **2014**, *35*, 1320–1322. [CrossRef]
22. Tordjman, M.; Saguy, C.; Bolker, A.; Kalish, R. Superior Surface Transfer Doping of Diamond with MoO3. *Adv. Mater. Interfaces* **2014**, *1*, 1300155. [CrossRef]
23. Colangeli, S.; Verona, C.; Ciccognani, W.; Marinelli, M.; Rinati, G.V.; Limiti, E.; Benetti, M.; Cannata, D.; Pietrantonio, F.D. H-Terminated Diamond MISFETs with V2O5 as Insulator. In Proceedings of the 2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Austin, TX, USA, 23–26 October 2016; pp. 1–4.
24. Verona, C.; Arciprete, F.; Foffi, M.; Limiti, E.; Marinelli, M.; Placidi, E.; Prestopino, G.; Rinati, G.V. Influence of surface crystal-orientation on transfer doping of V2O5/H-terminated diamond. *Appl. Phys. Lett.* **2018**, *112*, 181602. [CrossRef]

25. Verona, C.; Ciccognani, W.; Colangeli, S.; Limiti, E.; Marinelli, M.; Verona-Rinati, G. Comparative investigation of surface transfer doping of hydrogen terminated diamond by high electron affinity insulators. *J. Appl. Phys.* **2016**, *120*, 025104. [CrossRef]
26. Crawford, K.G.; Qi, D.; McGlynn, J.; Ivanov, T.G.; Shah, P.B.; Weil, J.; Tallaire, A.; Ganin, A.Y.; Moran, D.A.J. Thermally Stable, High Performance Transfer Doping of Diamond using Transition Metal Oxides. *Sci. Rep.* **2018**, *8*, 3342. [CrossRef] [PubMed]
27. Xing, K.; Xiang, Y.; Jiang, M.; Creedon, D.L.; Akhgar, G.; Yianni, S.A.; Xiao, H.; Ley, L.; Stacey, A.; McCallum, J.C.; et al. MoO3 induces p-type surface conductivity by surface transfer doping in diamond. *Appl. Surf. Sci.* **2020**, *509*, 144890. [CrossRef]
28. Young, H.X.; Yu, Y.; Xu, L.F.; Gu, C.Z. Ab initio study of molecular adsorption on hydrogenated diamond (001) surfaces. *J. Phys. Conf. Ser.* **2006**, *29*, 145–149. [CrossRef]
29. Kim, Y.-H.; Zhang, S.B.; Yu, Y.; Xu, L.F.; Gu, C.Z. Dihydrogen bonding, p-type conductivity, and origin of change in work function of hydrogenated diamond (001) surfaces. *Phys. Rev. B* **2006**, *74*, 075329. [CrossRef]
30. Rivero, P.; Shelton, W.; Meunier, V. Surface properties of hydrogenated diamond in the presence of adsorbates: A hybrid functional DFT study. *Carbon* **2016**, *110*, 469–479. [CrossRef]
31. Xiang, Y.; Jiang, M.; Xiao, H.; Xing, K.; Peng, X.; Zhang, S.; Qi, D.-C. A DFT study of the surface charge transfer doping of diamond by chromium trioxide. *Appl. Surf. Sci.* **2019**, *496*, 143604. [CrossRef]
32. ToolKit, A. *Atomistix ToolKit*; Series Atomistix ToolKit 2: Copenhagen, Denmark, 2017.
33. Ferreira, L.G.; Marques, M.; Teles, L.K. Slater half-occupation technique revisited: The LDA-1/2 and GGA-1/2 approaches for atomic ionization energies and band gaps in semiconductors. *AIP Adv.* **2011**, *1*, 032119. [CrossRef]
34. Smidstrup, S.; Markussen, T.; Vancraeyveld, P.; Wellendorff, J.; Schneider, J.; Gunst, T.; Verstichel, B.; Stradi, D.; Khomyakov, P.; Vej-Hansen, U.; et al. QuantumATK: An Integrated Platform of Electronic and Atomic-Scale Modelling Tools. *J. Phys. Condens. Matter* **2019**, *32*, 015901. [CrossRef]
35. Tsuno, F.T.; Imai, T.; Nishibayashi, Y.; Hamada, K. Naoji Epitaxially Grown Diamond (001) 2×1/1×2 Surface Investigated by Scanning Tunneling Microscopy in Air. *Jpn. J. Appl. Phys.* **1991**, *30*, 1063. [CrossRef]
36. Furthmüller, J.; Hafner, J.; Kresse, G. Structural and Electronic Properties of Clean and Hydrogenated Diamond (100) Surfaces. *Europhys. Lett. (EPL)* **1994**, *28*, 659–664. [CrossRef]
37. Santosh, K.C.; Longo, R.C.; Addou, R.; Wallace, R.M.; Cho, K. Electronic properties of MoS2/MoOx interfaces: Implications in Tunnel Field Effect Transistors and Hole Contacts. *Sci. Rep.* **2016**, *6*, 33562. [CrossRef]
38. Philipp, H.R.; Taft, E.A. Optical Properties of Diamond in the Vacuum Ultraviolet. *Phys. Rev.* **1962**, *127*, 159–161. [CrossRef]
39. Mauger, A.; Julien, C.M. V_2O_5 Thin Films for Energy Storage and Converstion. *AIMS Materials Science* **2018**, *5*, 349–401. [CrossRef]
40. Melskens, J.; van de Loo, B.; Macco, B.; Black, L.; Smit, S.; Kessels, M.M. Passivating Contacts for Crystalline Silicon Solar Cells: From Concepts and Materials to Prospects. *IEEE J. Photovolt.* **2018**, *8*, 373–388. [CrossRef]
41. Jens, M.; Antoine, L.K. Electronic structure of molybdenum-oxide films and associated charge injection mechanisms in organic devices. *J. Photonics Energy* **2011**, *1*, 1–7. [CrossRef]
42. Xing, K.; Creedon, D.L.; Yianni, S.A.; Akhgar, G.; Zhang, L.; Ley, L.; McCallum, J.C.; Qi, D.-C.; Pakes, C.I. Strong spin-orbit interaction induced by transition metal oxides at the surface of hydrogen-terminated diamond. *Carbon* **2020**. [CrossRef]

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