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Silicon Nanodevices

Edited by
Henry H. Radamson and Guilei Wang

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About the Editors

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Henry H. Radamson received Ph.D. degree in semiconductor materials from Linköping University in Sweden in 1996. He joined KTH Royal Institute of Technology in Stockholm in 1997 as senior scientist. In 2016, he became full professor in Chinese Academy of Science in Beijing and since 2017, he is foreign expert in China. In 2019, he became manager of Optoelectronics Innovation Center in Guangzhou. Henry Radamson is a member of European Academy of Sciences since 2020. His research field is nanomaterials, and nanodevices towards integration of electronics and photonics.

He is author of two books: Monolithic Nanoscale Photonics-Electronics Integration in Silicon and Other Group IV Elements, Elsevier 2014 & CMOS past, present, and future, Elsevier, 2018.

Henry Radamson is a member of Executive Committee in European Material Research Society (EMRS) where has also organized several symposiums.

Henry Radamson is in Editorial board of Springer-Nature and he has been Guest Editor for the *Nanomaterials* journal.

He has been also awarded several times for his teaching efforts by Chinese Academy of Sciences and European academy.

Guilei Wang

Guilei Wang, a professor at the Beijing Superstring Academy of Memory Technology. He used to work as a professor at the Institute of Microelectronics, Chinese Academy of Sciences. So far, more than 120 research papers have been published in international journals. He has completed more than 100 patents and patent applications. He has published 1 English book (Guilei Wang: Investigation on SiGe Selective Epitaxy for Source and Drain Engineering in 22 nm CMOS Technology Node and Beyond) and 1 SiGe epitaxy chapter. He has delivered invited talks and short courses in several prestigious international conferences and academic institutions. He served as a member of the Technical Programme Committee (TPC) of the 2018 European Materials Research Society (E-MRS) Spring Conference. He is a guest editor for Nanomaterials and reviewers for the journals. He has won the "E-MRS Young Scientist", "Springer Excellent Doctorate Thesis", and "Excellent Member of the Youth Innovation Promotion Association of the Chinese Academy of Sciences" awards. His research interests focus on nanomaterials for microelectronic and semiconductor quantum computing technologies.

Preface to ”Silicon Nanodevices”

Si nanodevices is a hot topic in the current technology. The start of Moore's law and the following of technology roadmap to scale down the transistors is one of the most important objectives in the semiconductor industry. As our research is proceeding towards to the unknown frontiers, the boundary in different parts of science is emerging together. Therefore, we have chosen a series of research articles in electronics and photonics to highlight the material synthesis and device manufacturing.

The editors would like to acknowledge valuable discussions with and material from all the authors and the valuable supports and help from Guangdong Greater Bay Area Institute of Integrated Circuit and System, Beijing Superstring Academy of Memory Technology, Institute of Microelectronics, Chinese Academy of Sciences.

Henry H. Radamson and Guilei Wang
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Editorial

Special Issue: Silicon Nanodevices

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In recent years, nanodevices have attracted a large amount of attention due to their low power consumption and fast operation in electronics and photonics, as well as their high sensitivity in sensor applications. For example, following Moore's law and the technology roadmap, the structure of transistors has been scaled down by a constant factor in order to obtain lower power consumption. Today, the scaling down of CMOS technology is focusing more on low voltages and cost-effective processes to match the requirements of mobile phone chips [1].

As a result of CMOS evolution, a lot of integration difficulties have been overcome, enabling the architecture of CMOS technology to change from planar or 2D to 3D. During this technology development, many issues, e.g., contact resistance, defects and reliability, have arisen and have been solved, which could affect device performance [2,3]. As an approach at the end of the technology roadmap (3 nm node), Si channel material is being changed to SiGe or Ge material, and even III-V materials could be integrated in the future. This is due to their material properties, as they have significantly higher carrier mobilities of $-40{,}000$ cm^2 V^{-1} s^{-1} for InGaAs (for electrons) and 1900 cm^2 V^{-1} s^{-1} for Ge (for holes) compared to silicon, which has 1400 cm^2 V^{-1} s^{-1} for electrons and 450 cm^2 V^{-1} s^{-1} for holes [1]. In many cases, these are processed to be fin-like or nanowire transistors on insulator substrates. Special attention is paid to All Gate Around (GAA) transistors in vertical or horizontal directions. In such cases, GeSi/Ge multilayers are grown, and later, GeSi can be selectively etched to reach a nano-scale channel [4]. What is interesting is the choice of our transistor design beyond Moore's era. Meanwhile, as a future type of computation that could be used when Moore's Law ends, quantum computing is gaining considerable attention from academic and industrial communities. Group IV material devices will be an important aspect of quantum computing.

Currently, photonic and sensor devices have also attracted a large amount of interest. For example, materials are required for emissions in the infrared and terahertz range with high responsivity and low dark currents [5–7]. Therefore, many studies are seeking methods to decrease the defect density, in particular in device processing. The main goal is to find a monolithic solution where a material can be used for both photonic and electronic components on the chip. Ge and GeSn are materials that are recognized as excellent candidates as optoelectronic materials [8–12].

In this field, nanodevices are manufactured in 3D, and the emergence of electronics and photonics is inevitable. It is obvious that the complexity of our society requires technology to become more complicated in its design. In the future, electronic–photonic designs will be our ultimate goal in nanotechnology.

This Special Issue presents the fabrication and characterization of group IV nanostructures, nanodevices and nanosensors and their integration with photonics. The issue also covers optoelectronic materials and defect engineering as well as characterization.

Conflicts of Interest: The author declares no conflict of interest.

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Four-Period Vertically Stacked SiGe/Si Channel FinFET Fabrication and Its Electrical Characteristics

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Abstract: In this paper, to solve the epitaxial thickness limit and the high interface trap density of SiGe channel Fin field effect transistor (FinFET), a four-period vertically stacked SiGe/Si channel FinFET is presented. A high crystal quality of four-period stacked SiGe/Si multilayer epitaxial grown with the thickness of each SiGe layer less than 10 nm is realized on a Si substrate without any structural defect impact by optimizing its epitaxial grown process. Meanwhile, the Ge atomic fraction of the SiGe layers is very uniform and its SiGe/Si interfaces are sharp. Then, a vertical profile of the stacked SiGe/Si Fin is achieved with $HBr/O_2/He$ plasma by optimizing its bias voltage and O_2 flow. After the four-period vertically stacked SiGe/Si Fin structure is introduced, its FinFET device is successfully fabricated under the same fabrication process as the conventional SiGe FinFET. And it attains better drive current I_{on}, subthreshold slope (SS) and I_{on}/I_{off} ratio electrical performance compared with the conventional SiGe channel FinFET, whose Fin height of SiGe channel is almost equal to total thickness of SiGe in the four-period stacked SiGe/Si channel FinFET. This may be attributed to that the four-period stacked SiGe/Si Fin structure has larger effective channel width (W_{eff}) and may maintain a better quality and surface interfacial performance during the whole fabrication process. Moreover, Si channel of the stacked SiGe/Si channel turning on first also may have contribution to its better electrical properties. This four-period vertically stacked SiGe/Si channel FinFET device has been demonstrated to be a practical candidate for the future technology nodes.

Keywords: stacked SiGe/Si; epitaxial grown; Fin etching; FinFET

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1. Introduction

High-mobility SiGe or Ge channel p-type Fin field effect transistor (FinFET) or gate-all-around (GAA) devices have been demonstrated to be a valid option as performance booster for future technology nodes [1–3]. The low-Ge-content SiGe channel will be implemented firstly on the FinFET owing to its advantages of higher hole mobility, better negative bias temperature instability (NBTI) reliability than silicon and more compatible with present silicon platform [4,5]. So far, a SiGe channel can be integrated in FinFET architectures in multiple ways, e.g., by shallow trench isolation (STI) last scheme [6] or by STI first strategy [7] or epitaxial cladding of Si Fins [8]. However, a high quality of low-Ge-content SiGe epitaxial grown on Si substrate is still a challenge task to solve the epitaxial thickness limit of SiGe film and the threading dislocations (TD) defects. This is because its theoretical critical thickness value is only ~10 nm [9]. Compared with the stable low-Ge-content SiGe layer, the thickness of metastable SiGe layer on Si can reach ~100 nm, but its quality is more easily affected by the following high temperature, implantation, and other processes. The other challenge about SiGe Fin channel is that it has relatively high interface trap charge (N_{it}) at the interfacial layer (IL)/SiGe channel due to the undesired GeO_x formation [10]. The passivation techniques of SiGe layer, such as Si-cap, O_3 low temperature oxidation,

selective GeO_x-Scavenging, and fluorine/nitrogen plasma treatment, have been studied and the experimental demonstration on low-N_{it} SiGe gate stack have been reported [11–15]. However, these passivation techniques may have compatibility problems with a state-of-the-art FinFET. Therefore, a high quality of low-Ge-content SiGe channel FinFET fabrication is still a challenge task and there are limited reports disclosing process details.

In this report, to solve the epitaxial thickness limit and the high interface trap density of SiGe channel FinFET, a four-period vertically stacked SiGe/Si multilayer with the thickness of each SiGe layer less than 10 nm grown on Si substrate is demonstrate by optimizing the epitaxial process. Then, an optimized stacked SiGe/Si Fin etching process with $HBr/O_2/He$ plasma is also introduced to attain a perfect profile. Finally, the four-period vertically stacked SiGe/Si channel FinFET is successfully fabricated and it achieves better drive current I_{on}, subthreshold slope (SS) and I_{on}/I_{off} ratio performance compared with the conventional SiGe channel FinFET under the similar fabrication process.

2. Materials and Methods

P-type FinFET device with a four-period vertically stacked SiGe/Si channel was fabricated on 8-inch p-type (100) wafers. Its fabrication flow is shown in Figure 1, where the fundamental differences with the conventional SiGe channel FinFET process are the stacked SiGe/Si Fin introduction (indicated with red color).

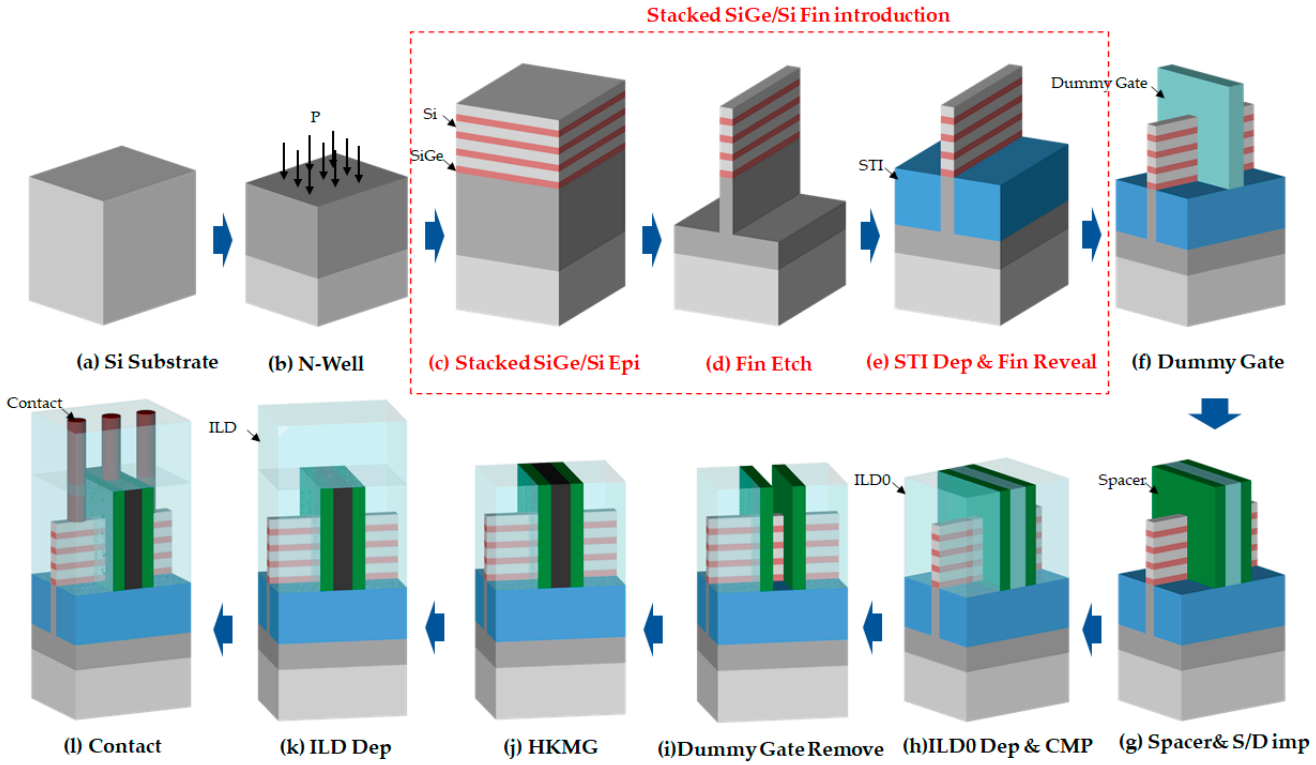


Figure 1. Fabrication flow of four-period stacked SiGe/Si Channel FinFET device.

After a standard nWell formation, four-period stacked SiGe/Si multilayer were epitaxially grown by reduced-pressure chemical vapor epitaxial deposition. Then, the vertical Fin pattern with stacked SiGe/Si multilayer on the top of Si substrate were formed by a spacer image transfer (SIT) technique under an optimal $HBr/O_2/He$ plasma. After STI filling and planarization, a low temperature of 850 °C for 30 s STI densification anneal and 1:100 diluted HF solution Fin reveal was implemented to attain a stacked SiGe/Si Fin formation [16]. Then, a low temperature SiO_2 deposition and dummy gate patterning were performed. After spacer 1 and spacer 2 definition, lightly doped drain (LDD) and source and drain (S/D) implantation was implemented with B and BF_2 dopant respectively. A

low temperature dopant activation of 850 °C for 30 s was performed to keep the stacked SiGe/Si Fin stability [16]. Inter layer dielectric (ILD) deposition and CMP was employed to exposure the dummy gate. A standard tetramethylammonium hydroxide (TMAH) solution at 70 °C was used to remove the dummy poly gate with high selectivity to the underlying oxide on the stacked SiGe/Si Fin. After removal of this oxide, an in-situ low temperature O_3 passivation treatment at 300 °C for 1 min was employed and the Al_2O_3/HfO_2 high-k (HK) dielectric and TiN-based/W metal gate (MG) stack were deposited by the atomic-layer-deposition (ALD) tool. Finally, the standard FinFET following processing was employed to complete the stacked SiGe/Si channel FinFET device fabrication.

3. Result and Discussion

3.1. Epitaxial Growth of Stacked SiGe/Si Multilayer

After a standard HF-last clean, to maintain the well doping profile and attain an excellent surface of the Si substrate, a H_2 pre-bake treatment of 825 °C for 5 min is performed. The epitaxial growth of stacked SiGe/Si multilayer is prepared using dichlorosilane (DCS) and GeH_4 as SiGe layer precursors and SiH_4 as Si layer precursor at 650 °C in H_2 ambient, respectively. And a four-period stacked SiGe/Si is fabricated successfully on the Si substrate by appropriately exchanging the sequences of introduced gases.

The crystalline microstructure of the four-period stacked SiGe/Si multilayer epitaxial grown on Si substrate is detected by high resolution X-ray diffraction (HRXRD, Bruker, Tel Aviv, Israel) in the vicinity of the (004) Bragg peak with a Cu peak radiation. Its $\omega - 2\theta$ HRXRD scan result is shown in Figure 2. It is worth to note that a series of obvious high-intensity satellite peaks are found, indicating that the epitaxial layers of the four-period stacked SiGe/Si multilayer are under strained due to the lattice constant mismatch of Si and SiGe. Moreover, the presence of small-intensity thickness fringes is the characteristic of high quality of the stacked SiGe/Si multilayer.

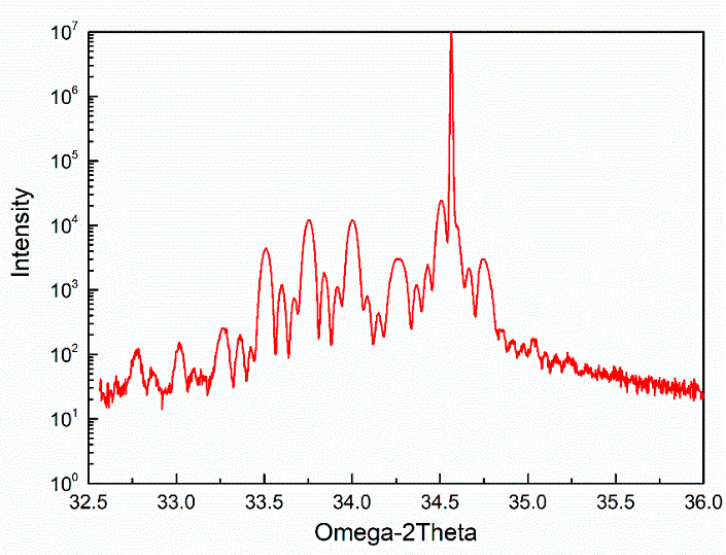
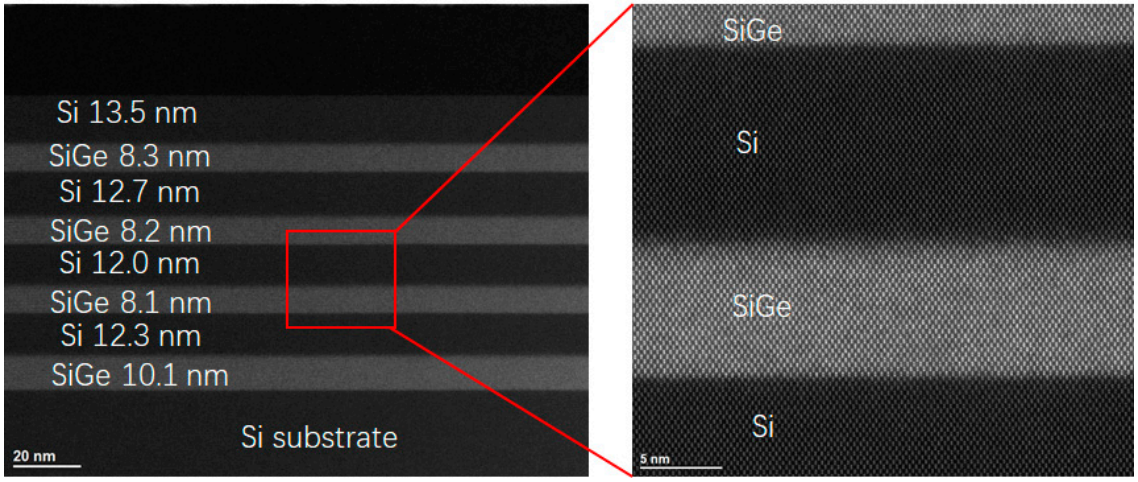


Figure 2. HRXRD spectra result on the four-period stacked SiGe/Si multilayer epitaxial grown on Si substrate.

In addition, its high-angle annular dark field scanning transmission electron microscopy (HAADF-STEM, FEI Talos, Brno, Czech Republic) analysis results are shown in Figure 3. It is found that there are no misfits at the SiGe/Si interfaces, nor threading dislocations crossing the stacked SiGe/Si epitaxial film. Therefore, a high crystal quality four-period stacked SiGe/Si multilayer with thin and distinct interfaces between SiGe and Si is successfully prepared. Meanwhile, the thickness of SiGe from top to bottom is 8.3, 8.2, 8.1 and 10.1 nm under the same time of epitaxial grown. Namely, the thickness

of bottom SiGe is ~2 nm thicker than that of others. It is known that the epitaxial rate is strongly dependent on the crystallization of under-layer, that is, the epitaxial rate might be decreased if multi-crystallization occurs in the under-layer.



(**a**) (**b**)

Figure 3. (**a**)Cross-section HAADF-STEM images of four-period stacked SiGe/Si multilayer; (**b**) its magnified images at the SiGe/Si interfaces.

Subsequently, EDX (FEI Talos, Brno, Czech Republic) line scan analysis of Ge and Si elements is also performed to determine the interfacial morphologies, and atomic fraction of the SiGe/Si layers for the four-period stacked SiGe/Si multilayer. The result is shown in Figure 4. It can be observed that the Ge atomic fraction of the SiGe layers from top to bottom are 23.2%, 23.5%, 23.8%, and 24.5%, respectively. Moreover, the width of transition layer of Si and SiGe are within 1.5 nm. Therefore, very uniform Ge atomic fraction of the SiGe layers with sharp SiGe/Si interfaces are achieved.

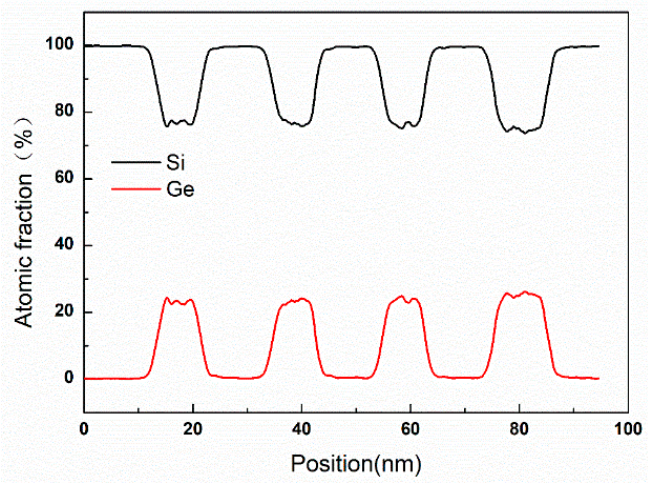
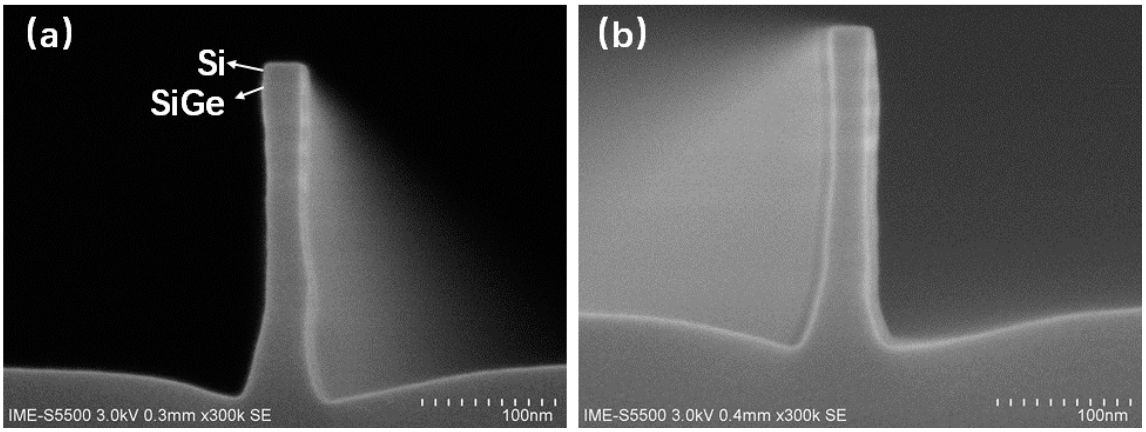


Figure 4. EDX line scan analysis of Ge and Si elements across the four-period stacked SiGe/Si multilayer.

3.2. Stacked SiGe/Si Fin Etching

Based on previous SiGe Fin etching result, HBr-based plasma is chosen as the etching gas for the four-period stacked SiGe/Si multilayer. Figure 5 presents the profiles of Si substrate/four-period stacked SiGe/Si multilayer Fin produced by $HBr/O_2/He$ plasma under different bias voltage and O_2 flow. The other etching process conditions are as

follows: top power of 350 W, pressure of 6 mTorr, HBr flow of 110 sccm, He flow of 50 sccm. A more vertical profile of the Si substrate/four-period stacked SiGe/Si multilayer Fin structure can be achieved as its bias voltage increase from −70 V to −90 V and its O_2 flow increasing from 2.2 to 2.5 sccm. This is because that increasing the bias voltage can attain a larger ion bombardment effect and slightly increasing O_2 flow can help promote passivation films formation on the stacked SiGe/Si Fin sidewall and preserve its profile during etching.



(**a**) (**b**)

Figure 5. Scanning electron microscope (SEM) images of Fin profile under $HBr/O_2/He$ plasma under (**a**) bias voltage of −70 V and O_2 flow of 2.2 sccm, (**b**) bias voltage of −90 V and O_2 flow of 2.5 sccm.

3.3. FinFET Device Fabrication

After these above newly developed epitaxial growth and etching technologies are implemented, the results of following major fabrication process of the four-period stacked SiGe/Si channel FinFET device are shown in Figure 6. Figure 6a presents the cross-sectional SEM image of the Fin reveal structure post STI recess by 1:100 diluted HF solution. It is found that the STI is well controlled and the stacked SiGe/Si Fin on the top of the Si has been revealed. Figure 6b shows the top view SEM image of stacked SiGe/Si channel FinFET device after gate formation with critical dimension (CD) of ~25 nm. And conformal spacer 1 and spacer 2 in Figure 6c are realized at two sides of dummy gate. Figure 6d,e present a top view of stacked SiGe/Si channel FinFET device after dummy gate CMP and dummy gate removal. As can be seen from the images, the surface of ILD is very smooth, and a dummy poly gate is successfully removed with a stacked SiGe/Si channel exposure in the open gate trench. After dummy gate removal, an in-situ low temperature O_3 passivation treatment at 300 °C for 1 min and the Al_2O_3/HfO_2 and TiN/TaN/TiN//W are implemented as HK and MG, respectively. Figure 7 shows cross-sectional transmission electron microscopy (TEM) image for the four-period stacked SiGe/Si channel under the HK/MG stack at the end of fabrication processing. And its HAADF-STEM and EDS mapping results are shown in Figure 8. It is found that a perfect four-period stacked SiGe/Si channel Fin structure with stable SiGe and Si layers is realized and the multilayer HK/MG are well wrapped around. At the same time, the Fin height of SiGe channel is 80.6 nm and the CD is 20 nm.

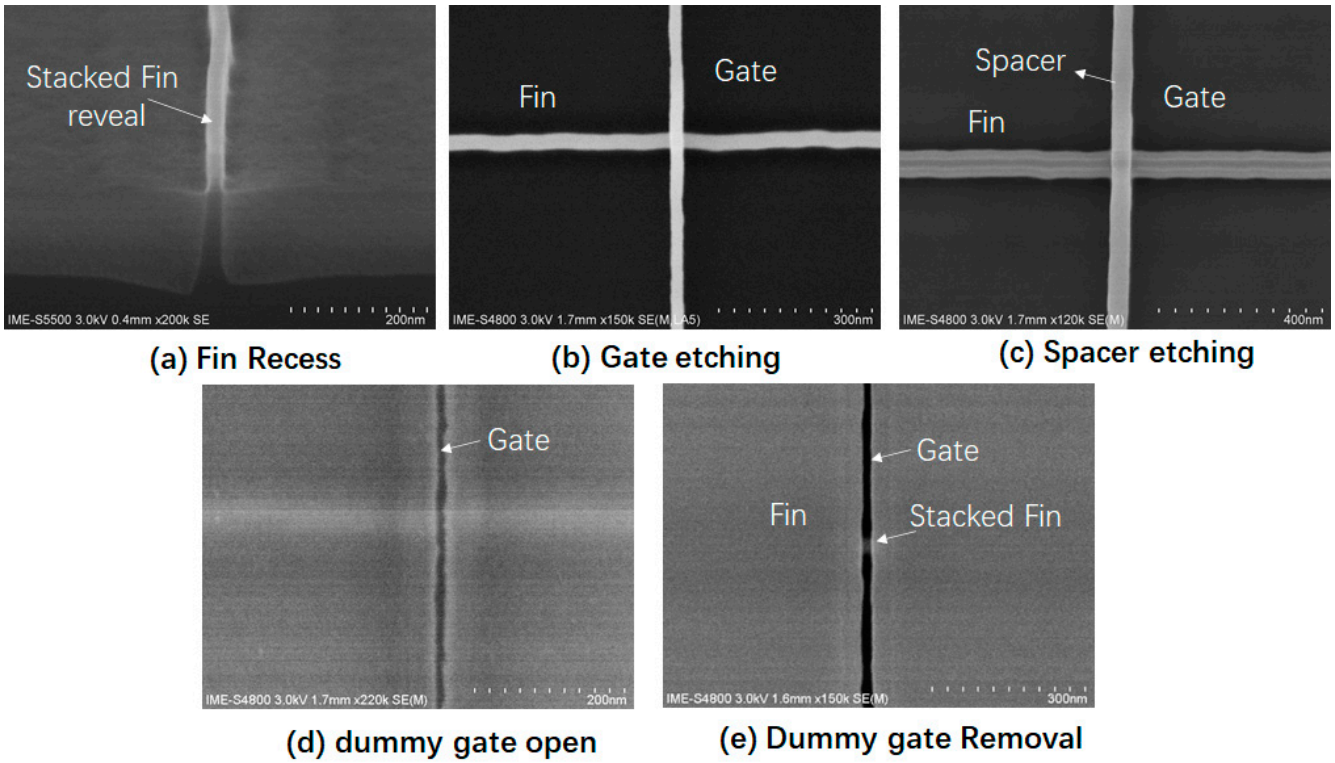


Figure 6. SEM images of stacked SiGe/Si channel FinFET device at different fabrication stages: (**a**) Fin reveal post STI recess, (**b**) dummy gate formation, (**c**) spacer formation, (**d**) poly gate open by CMP, (**e**) dummy gate removal.

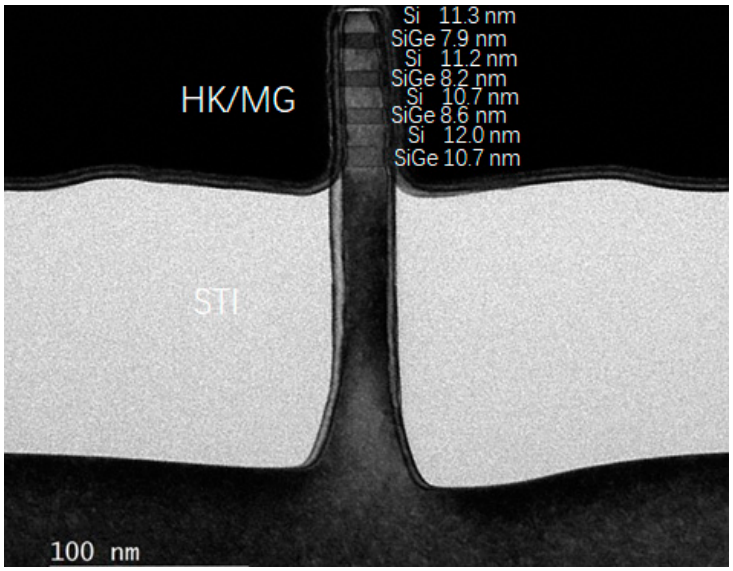


Figure 7. TEM result of four-period stacked SiGe/Si channel FinFET under the HK/MG stack at the end of fabrication processing.

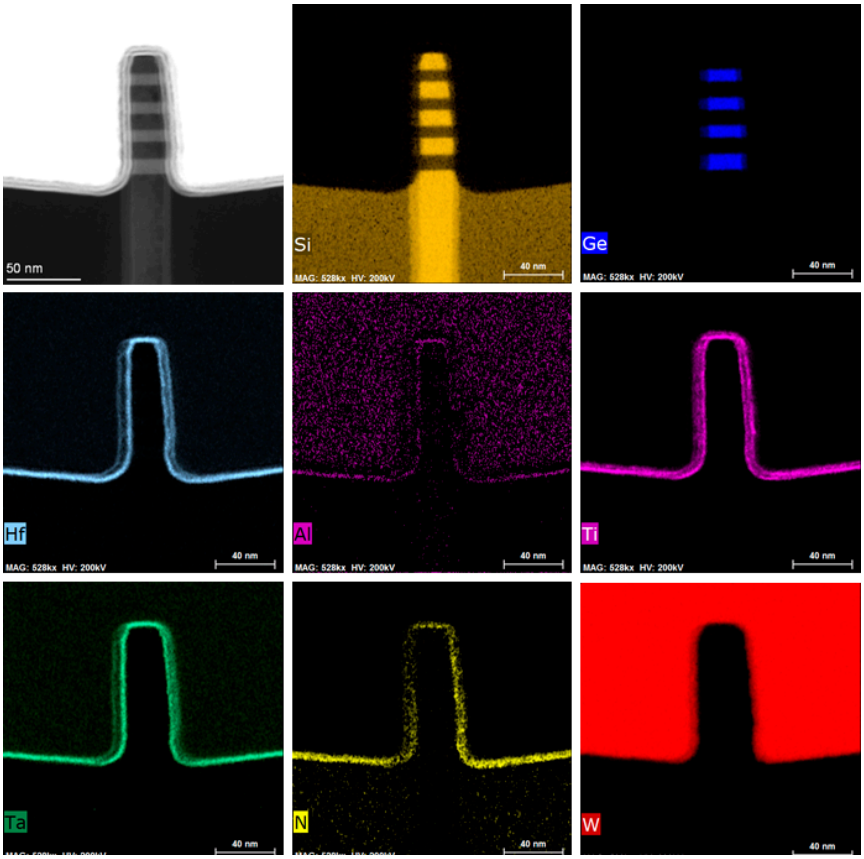


Figure 8. HAADF-STEM and EDS mapping results of the four-period stacked SiGe/Si channel FinFET under the HK/MG stack at the end of processing.

3.4. Electrical Performance

As a comparison, the conventional SiGe channel FinFET is also fabricated under the similar fabrication process.

As shown in Figure 9, the Fin height of its SiGe channel is 33 nm and the CD is 19.5 nm. The Fin height of SiGe channel is almost equal to total thickness of SiGe in the four-period stacked SiGe/Si channel FinFET. Moreover, the CD and profile of Fin of these two kinds of FinFET device are almost comparable. Therefore, these two kinds of FinFET device have almost the same footprint.

Figure 10 shows the I_{DS}-V_{GS} curves for the four-period stacked SiGe/Si channel FinFET and conventional SiGe channel FinFET. Compared with conventional SiGe channel FinFET, the I_{on}, SS and I_{on}/I_{off} ratio of the four-period stacked SiGe/Si channel FinFET under the same footprint show obvious benefit. And their electrical characteristic data are summarized in Table 1. Its I_{on} under $V_{DS} = V_{GS} = -0.8$ V increases 1.6 times, improved from 13.3 μA to 21.2 μA, and its I_{on}/I_{off} ratio can be improved from 1×10^5 to 1×10^6 due to the increase of I_{on} and the decrease of I_{off} at the same time. At the same time, the threshold voltage (V_{tsat}) extracting at I_{on} of 1×10^{-9} A can be improved from +0.38 V to +0.16 V. In addition, four-period stacked SiGe/Si channel FinFET is easier to obtain a better SS characteristic than the conventional SiGe FinFET under the same unoptimized O_3 passivation process. Its SS can be improved from 149 mV/dec to 90 mV/dec. The better SS characteristic should be related to the four-period stacked SiGe/Si Fin structure and it also can help to increase the I_{on} and decrease the I_{off}. The better SS can be attributed to the following two reasons: first, the stacked SiGe/Si with each layer SiGe of 8–10 nm in the stable stage may maintain a better quality and surface interfacial performance during the whole fabrication process compared with the the conventional SiGe of 33 nm in the metastable stage; second, the Si channel of the stacked SiGe/Si channel may turn on first

due to its lower D_{it}. Moreover, the larger Ion can be attributed to the increasing of effective channel width (W_{eff}) because the W_{eff} of four-period stacked SiGe/Si Fin is 181 nm and the W_{eff} of conventional SiGe Fin is only 85.5 nm.

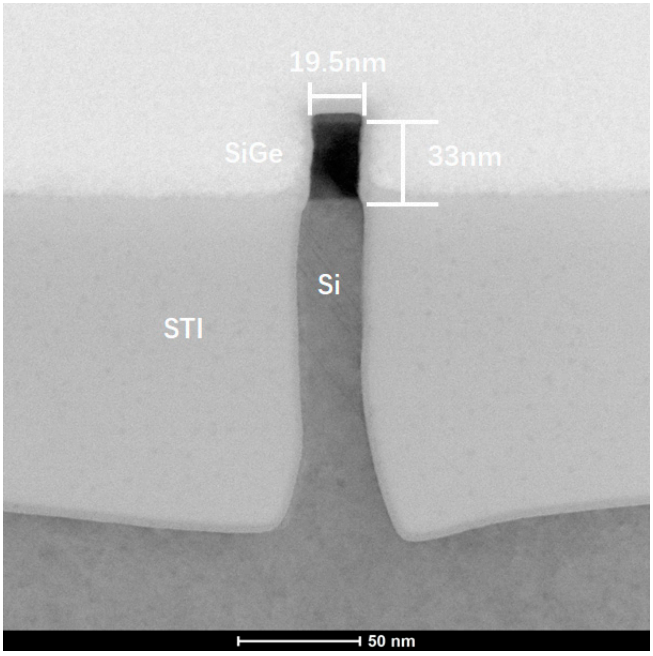


Figure 9. TEM result of the conventional SiGe channel Fin profile.

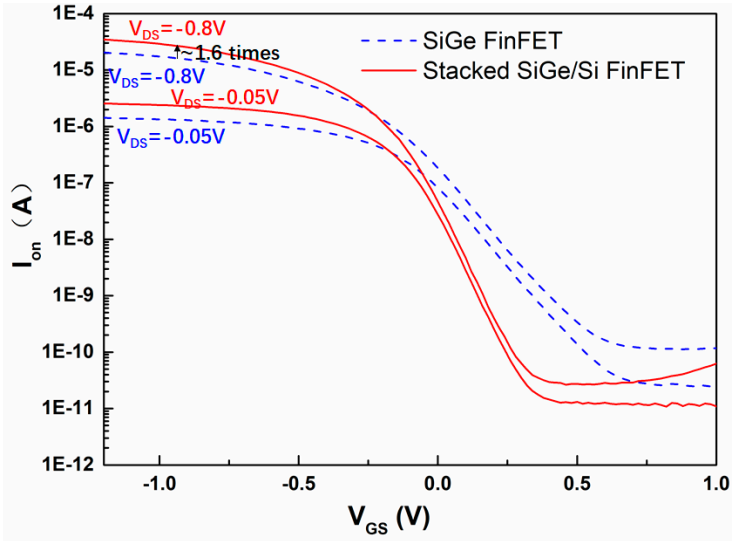


Figure 10. I_{DS}-V_{GS} characteristics of the four-period stacked SiGe/Si channel FinFET and conventional SiGe channel FinFET under the similar fabrication process.

Table 1. Electrical characteristic comparison of the four-period stacked SiGe/Si and conventional SiGe channel FinFET.

Category	Ion (μA)	SS (mV/dec)	V_{tsat} (V)	I_{on}/I_{off}
Conventional SiGe channel FinFET	13.3	149	0.38	1×10^5
Four-period stacked SiGe/Si channel FinFET	21.2	90	0.16	1×10^6

This four-period stacked SiGe/Si channel FinFET has been demonstrated to be a practical candidate for the future technology nodes. However, it is important to emphasize

that these results are preliminary for the four-period stacked SiGe/Si channel FinFET, and there is still much room to improve its electrical characteristic, such as its SS and V_{tsat}. Therefore, we will employ the interfacial passivation, and gate stack engineering to further optimize its electrical performance in the future.

4. Conclusions

In a summary, a four-period vertically stacked SiGe/Si FinFET device was successfully fabricated by optimizing its epitaxial grown and Fin etching process. Compared with the conventional SiGe channel FinFET under the same footprint, its I_{on} increases 1.6 times, I_{on}/I_{off} ratio increases 1 order and SS can be improved from 149 to 90 mV/dec because the four-period stacked SiGe/Si Fin structure has larger W_{eff} and may maintain a better quality and surface interfacial performance during the whole fabrication process. Therefore, this device has been demonstrated to be a practical candidate for future technology nodes. Moreover, considering the compatibility of fabrication process, it also can be use as the I/O device for the vertically stacked Gate-All-Around horizontal nanowire/sheet technology if a thicker gate stack is employed and the channel release step is skipped.

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An Operation Guide of Si-MOS Quantum Dots for Spin Qubits

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Abstract: In the last 20 years, silicon quantum dots have received considerable attention from academic and industrial communities for research on readout, manipulation, storage, near-neighbor and long-range coupling of spin qubits. In this paper, we introduce how to realize a single spin qubit from Si-MOS quantum dots. First, we introduce the structure of a typical Si-MOS quantum dot and the experimental setup. Then, we show the basic properties of the quantum dot, including charge stability diagram, orbital state, valley state, lever arm, electron temperature, tunneling rate and spin lifetime. After that, we introduce the two most commonly used methods for spin-to-charge conversion, i.e., Elzerman readout and Pauli spin blockade readout. Finally, we discuss the details of how to find the resonance frequency of spin qubits and show the result of coherent manipulation, i.e., Rabi oscillation. The above processes constitute an operation guide for helping the followers enter the field of spin qubits in Si-MOS quantum dots.

Keywords: Si-MOS; quantum dot; spin qubits; quantum computing

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1. Introduction

As early as 1982, the famous physicist Feynman proposed that quantum computers can simulate problems that cannot be solved by classical computers [1]. Then, in 1994, Shor proposed the well-known quantum prime factor decomposition algorithm that can be used to crack classic RSA encrypted communications [2], and in 1996, Grover devised the quantum search algorithm which uses only $O(\sqrt{N})$ evaluations of the function [3]. After that, Loss and DiVincenzo proposed the Loss–DiVincenzo quantum computer in 1998 [4] and then in 2000, DiVincenzo presented the DiVincenzo Criteria for physical implementation of quantum computing [5]. These findings set off a wave of quantum computing research.

In this wave, researchers tried to build quantum computers in various systems. Trapped ions [6,7], nuclear magnetic resonance (NMR) [8,9], superconducting loops [10,11], nitrogen vacancy center [12,13], semiconductor quantum dots [14,15], and other systems have enabled the manipulation of single and two qubits and have demonstrated simple quantum algorithms. Among them, silicon quantum dots (QDs) have emerged as promising hosts for qubits to build a quantum processor due to their long coherence time [16,17], small footprint [18], potential scalability [19,20], and compatibility with advanced semiconductor manufacturing technology [21].

In recent decades, silicon QDs have engaged research participants all around the world and have developed fast. In 2012, a long-time singlet–triplet oscillation was realized in silicon double quantum dots (DQD) [22]. Then, high-quality single-spin control was developed in silicon QDs [16,23]. After that, a two-qubit controlled gate in silicon QDs was experimentally implemented [24–27]. Nowadays, the single-qubit operations of spin qubits achieve fidelities of 99.9% [28,29], the two-qubit operation fidelities are above 99% as reported [30], the spin–photon coupling rates are more than 10 megahertz [31–33], and the qubit operation temperature is higher than 1 kelvin [34,35]. In the meantime, experiments on other properties of silicon QDs, including valley states [36–38], orbital states [39], and noise spectra [40,41], have been carried out. Furthermore, experimental approaches and techniques for characterizing features of QDs from other systems, e.g., charge stability diagrams [42–44], random telegraph signals (RTS) [45–48], Elzerman readout [49,50], Pauli spin blockade (PSB) readout [51,52], electron spin resonance (ESR) [53,54], and electron dipole spin resonance (EDSR) [55,56], have been applied in silicon QDs as well. In addition, several reviews [57–59] and guides on fabrication [60] have been reported. However, the process from silicon QD to qubit manipulation is still challenging.

In this article, we give a brief introduction of how to realize a single spin qubit from QDs in a Si-MOS structure. First, we introduce the gate-defined DQD in an isotopically enriched ^{28}Si-MOS structure and the low-temperature measurement circuits. Second, by applying these circuits, we investigate the basic properties of silicon QD devices, i.e., charge states, excited orbital states, valley splitting, lever arms, electron temperature, tunneling rate, and noise spectrum. Then, we introduce two mainstream spin-state-readout methods named as the Elzerman readout and the PSB readout. Finally, we use the rapid adiabatic passage to find out the resonance frequency of the spin qubits and apply the Rabi pulsing schemes to coherently manipulate the spin qubit.

2. Materials and Methods

2.1. Spin Qubit Devices

Spin qubits are hosted in a pair of metal-oxide-semiconductor (MOS) dots with isotopically enriched silicon. By using the high vacuum activation annealing technique, we improve the mobility of Si-MOS devices by a factor of two, reaching 1.5 $m^2/(V{\cdot}s)$ [61]. In this work, we use a DQD that has a similar structure (Ref. [38]) and was fabricated in our lab's clean room. As shown in Figure 1a, the aluminum electrodes are vaporized on top of the silicon oxide by electron beam evaporation techniques. Between every two layers of the electrodes, an insulating layer of aluminum oxide is formed by thermal oxidation. Figure 1b shows that the electrons are confined in the potential wells and the DQD is formed by applying voltages to the electrodes [62]. In the quantum well, a single electron can tunnel between the two QDs by biasing the electrodes' voltages. The entire structure consists of a DQD and a single-electron transistor (SET) sensing the charge states in DQD.

2.2. Measurement Circuits

There are three main types of measurement circuits commonly used to characterize the properties of DQDs, as shown in Figure 2a,c,e:

- Figure 2a: Transport measurements based on a lock-in amplifier. The AC excitation is added to the SET source (S_1) by connecting the lock-in amplifier to an external 1000:1 voltage divider, and finally reaches S_1 at approximately 50 μV, with a lock-in frequency generally between 70 and 1000 Hz. In addition, the drain (D_1) is connected back to the lock-in amplifier to demodulate the signal and obtain the currents.
- Figure 2c: Charge detection based on the lock-in amplifier. The bias voltage at S_1 is connected to a Stanford Research Systems Isolated Voltage Source (SIM 928) through a 1000:1 voltage divider, reaching S_1 at around 500 μV, while the AC excitation of the lock-in amplifier (output at approximately 0.5 to 1.5 mV) is connected to LP through an analog summing amplifier (SIM 980, bandwidth of approximately 1 MHz).

- Figure 2e: Charge detection based on a current-voltage amplifier. The source-drain bias is the same as Figure 2c, except no excitation is applied to the LP and D_1 is connected to a current-voltage amplifier; here, we use a Femto DLPCA200, connected to a voltage amplifier (SIM 910), an analog filter (SIM 965), and finally to a voltmeter (Agilent 34410) for signal measurement or to a PCI-based waveform digitizer (ATS 460), oscilloscope, etc. for the real-time observation of electron tunneling.

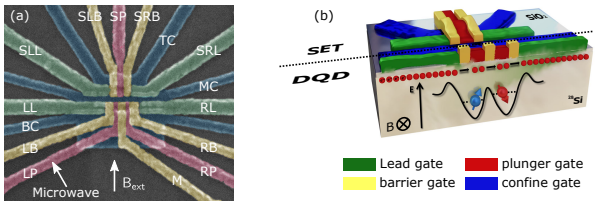

Figure 1. (**a**) Scanning electron micrograph image of a typical Si-MOS DQD. An SET, which is used as a charge sensor, is confined by the top confine gate (TC), middle confine gate (MC), left barrier gate (SLB), and right barrier gate (SRB) and is tuned by the plunger gate (SP). A DQD is composed of a left lead gate (LL), right lead gate (RL), left barrier gate (LB), middle gate (M), right barrier gate (RB), left plunger gate (LP), and right plunger gate (RP) and is confined by a bottom confine gate (BC) and middle confine gate (MC). We tune the left and right QD via the LP and RP, respectively. The tunneling rate of the QDs can be tuned by the LB and RB. The spin of electrons in the left QD is controlled by applying a microwave pulse to the LP. The right white arrow indicates the direction of an in-plane external magnetic field. (**b**) Cross-sectional view of a 3D model of the device. Electrodes for different functions are distinguished by different colors. The SET and DQD are on each side of the dotted line. The electrons in the DQD are located under the plunger gates.

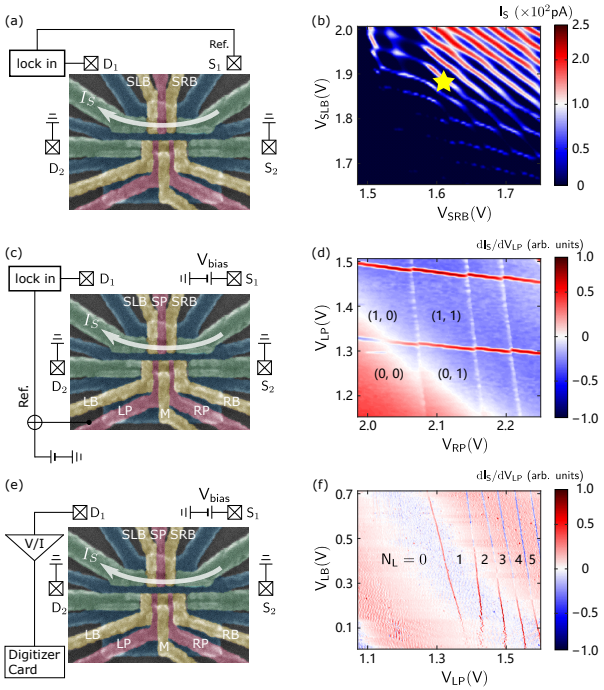

Figure 2. The three different measurement circuits. The white arrow above the SET indicates the direction of the current (I_S). (**a**,**b**) Measurement circuit diagram of the SET using the lock-in amplifier and the Coulomb peak diagram obtained by scanning the voltage of the SET barrier gates (SRB and SLB). The yellow star identifies a sensitive SET position. (**c**,**d**) Measurement circuit diagram of the DQD and the charge stability diagram of the DQD obtained by scanning the RP and LP. (**e**,**f**) Measurement circuit diagram for measuring the DQD using a current-voltage amplifier and the corresponding charge stability diagram of the left QD.

3. Results

3.1. Basic Properties of Silicon QDs

3.1.1. Charge Stability Diagram

Obtaining the QD charge stability diagram by the charge detection method is one of the most basic QD characterization methods [42–44]. As shown in Figure 2a–d, according to the method of measuring QDs using the modulation signal of the lock-in amplifier introduced in Section 2, the source (S_2) and drain (D_2) of the DQD are grounded. We set the voltages of the SLB and SRB near a Coulomb peak so that the SET works sensitively at this position, which is identified by the yellow star in Figure 2b. Then, a voltage of 2.60 V is applied to the LL and RL to ensure that the channel of DQD is turned on. After that, we measured the charge stability diagrams with different gate voltages to obtain the DQD electron occupation numbers and tunneling properties of the left QD. Figure 2d shows the charge stability diagram of the last few electrons in the DQD. The numbers in this figure indicate the electron occupation on the left and right QD. The slope is relatively symmetric with respect to the two electrodes. This indicates that two QDs are formed under electrodes LP and RP. When scanning the voltage of LB and LP, there are continuous electron tunneling lines observed, which correspond to the left QD. As shown in Figure 2f, the tunneling line of the last few electrons in the left QD becomes more invisible when the voltage of LB decreases. This is because a decrease in the LB voltage reduces the tunneling rate of the left QD to the reservoir of D_2.

3.1.2. Detection of Orbital Excited States in Silicon QDs

The orbital excited state in silicon QDs is several meV above the ground state, and it can be detected by the pulsed-voltage spectroscopy method [39,63]. Based on the measurement circuit in Figure 2c, we change the modulation signal output from the lock-in amplifier to a square waveform generated by an external arbitrary waveform generator that is synchronized with the lock-in amplifier. By zooming in and remapping, the single tunneling lines in Figure 3a split into pairs of lines in Figure 3b. As shown in Figure 3c, the principle of the pulsed-voltage spectroscopy method is illustrated. When the voltage of LP is set at the position of the blue square in Figure 3d, the electron can tunnel into the ground state of the QD. As the voltage increases, the energy level of the excited state gradually approaches the amplitude window of the square wave. When the excited state enters the window, the electron can tunnel into the excited state, so that another transport line appears parallel to the left line, identified by the green circle in Figure 3d. According to Figure 3d and the extracted lever arm of LP (α_{LP}, which will be discussed in Section 3.1.3), which is 0.33 meV/mV, the calculated energy of excited state is 1.3 meV.

3.1.3. Detection of Valley States in Silicon QDs

In solid-state physics, due to the six-fold degeneracy at the bottom of the conduction band of silicon, the energy levels at the bottom of the six conduction bands are named as the valley level. In the case of two-dimensional electron gas, the six-fold degeneracy is split into a four-fold degeneration and a double-fold degeneration. Due to the existence of the interfacial electric field, the quadruple degenerate and the double degenerate split further and form valley-level splits [57]. Unlike the orbital state, the splitting energy of the two lowest valley states (E_{VS}) in silicon QDs is similar to the Zeemen splitting energy (E_Z) under the applied magnetic field in our experiment [36–39,64,65]. Therefore, it is important to determine the splitting energy of the valley state. A commonly used method is to measure the electron tunneling line at different magnetic fields. Here, we tune the energy level of the first four electrons by changing the magnetic field of which the direction of is along the surface of the device and perpendicular to the one-dimensional channel formed by the QD, as shown in Figure 1a. Figure 4a shows the transition lines of the first four electrons in the device in Ref. [38]. The voltage of the first transition line of the QD decreases as the magnetic field increases, while the fourth line increases. Differently,

the second transition line increases first and then decreases, and the third line is reversed to the second line.

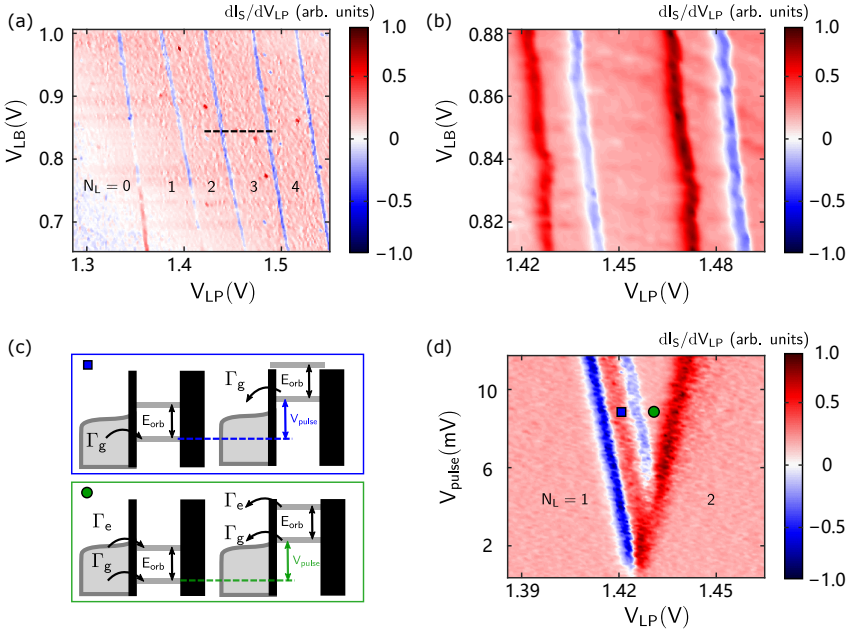

Figure 3. (**a**) Charge stability diagram of the QDs obtained by scanning the LB and LP voltages. (**b**) Zoom in on the QD charge stability diagram after applying a square pulse with a frequency of 687 Hz and an amplitude of 20 mV. (**c**) Schematic diagram of the square pulse spectrum measurement of the excited orbital state. When the LP voltage increases, the tunneling line of the electron in the excited state appears. (**d**) Diagram of the excited orbital state obtained by scanning the amplitude of the square pulse and the LP voltage.

We use the principle of minimum energy to simply explain this phenomenon, as shown in Figure 4b. When filling the first electron, the electron will be filled to the lowest energy level. As the magnetic field increases, E_Z increases, so the energy level of filling the first electron decreases. When filling the second electron, the first electron has been filled to the bottom level. In accordance with the principle of minimum energy, the second electron should be filled with the second-lowest level, but this second-lowest energy level depends on the magnetic field. When the magnetic field is small, the second-lowest energy state is the valley state v_- with spin state up, and vice versa. As shown in Figure 4b, the energy states of the third and fourth electron are mirror-symmetrical to the second and first electrons, respectively. It is obvious from Figure 4b, the position of the kink point is exactly where E_{VS} is equal to E_Z, so by using the position of the kink point and the Bohr magneton (μ_B), we can obtain:

$$E_{VS} = g\mu_B B_{\text{kink}} \tag{1}$$

According to Figure 4a, the E_{VS} of the second electron is 170 μeV, and the E_{VS} of the third one is 245 μeV. The difference between the E_{VS} of these two electrons is caused by the different LP voltages [38].

Additionally, we can estimate α_{LP} by:

$$\alpha_{LP} = \frac{g\mu_B \Delta B}{2\Delta V_{LP}} \tag{2}$$

Therefore, the lever arms of the first four electrons are shown in Table 1:

Table 1. Lever arm α_{LP} for the first four electrons.

Electron Number	Lever Arm α_{LP} (meV/mV)
1	0.33
2	0.32
3	0.31
4	0.34

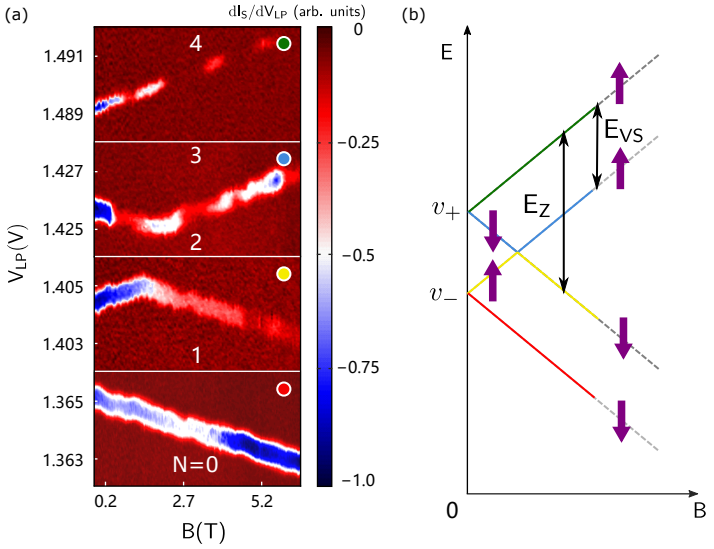

Figure 4. The magnetic spectrum and the corresponding diagram of the energy state for different electron numbers in the QDs. (**a**) The dependence of different electron tunneling lines on the magnetic field, where N = 0, 1, 2, 3, and 4 refer to the number of electrons in the QD. The slopes of the first four electron tunneling lines reveal the lever arms of LP for the first four electrons. (**b**) Energy state diagram of E_Z as a function of the magnetic field. The ordinate is the state energy, and the abscissa is the order of the magnetic field. The purple arrow indicates the direction of the spin. The arrow with E_{VS} represents the energy of the valley splitting.

3.2. Real-Time Observation of Electron Tunneling in Silicon QDs

The characterization of the orbital state, spin state, and valley state in QDs is based on steady-state measurement. However, to detect more properties of electrons, such as tunneling rate, electron temperature, noise spectrum, spin state, etc., we also need the ability to observe the tunneling process of electrons in QDs in real time [45–48]. The measurement circuit of real-time detection has been introduced in Section 2, as shown in Figure 2e. Next, we introduce the measurement results of tunneling rate, electron temperature, noise spectrum, and spin state, respectively.

3.2.1. RTS and the Measurement of Electron Temperature

When we align the electrochemical potential of the first electron in the QD with the Fermi surface of the electron reservoir, the electrons will continuously tunnel in and out of the QD (see the green circle in Figure 5a,b). At this time, on the oscilloscope or digitizer, we can see the signal as shown in the inset of Figure 5b. Since tunneling events happen randomly, we call the observed signal a RTS.

Ideally, electrons tunnel only when the electrochemical potential in the QD is aligned with the Fermi surface of the electron reservoir. However, in practice, due to the limited electron temperature, the Fermi surface of the electron reservoir will have a certain broadening. Therefore, changes in the electron tunneling events can be observed when the LP voltage is changed. The insets in Figure 5b show that when the electrode voltage increases, the electrochemical potential in the QD decreases, so the probability of the electrons occu-

pying the energy state in the QDs gradually increases and vice versa. By fitting the Fermi distribution to the electron occupancy, we can extract the electron temperature. The specific form of the Fermi distribution function we used here is the following [48]:

$$N = \frac{1}{\exp[\alpha_{LP}(V_{LP0} - V_{LP})/(k_B T) + 1]} \tag{3}$$

where k_B represents the Boltzmann constant, α_{LP} has been calculated in Table 1, V_{LP0} and T are fitting parameters. By fitting this equation, the electron temperature of approximately 224 mK is obtained.

3.2.2. Measurement of the Tunneling Rate

For the RTS, we can mark the time of electron tunneling from the reservoir to the QDs as t_{on}, and the time of electron tunneling from the QDs to the reservoir as t_{off}. By counting the distribution of t_{on} and t_{off} over a long period of time, we can actually determine the time of electron tunneling in and out of the reservoir [45].

Here, we introduce another method based on RTS. As shown in Figure 5c, by applying a square waveform on the LP, the signal will also switch between low and high levels with an approximate square wave period. Figure 5d illustrates that the rising and falling edges of the signal are slower, unlike the square wave from the AWG. Excluding the bandwidth limitation of the SET, the width of the edges represents the electron tunneling times t_{on} and t_{off}. By fitting the rising and falling edges exponentially, we can obtain the exact tunneling time values: $t_{on} = 3.45$ ms and $t_{off} = 3.23$ ms.

3.2.3. Noise Spectrum

When observing the real-time electron tunneling signal, there will inevitably be noise interference. Analyzing the noise spectrum can help us analyze the source of the noise and then suppress the noise. Figure 6a shows a typical noise spectrum of a QD system but does not include the noise introduced by the measurement system. The QD system suffers from charge noise [29], random telegraph noise (RTN) [40] and nuclear noise [66] at low frequencies. Johnson Nyquist noise and phonon noise are relatively large at high frequencies and affect the spin relaxation time.

Figure 6b shows the noise spectrum under the different device conditions given in Ref. [38]. The red line is the noise spectrum when the QD is connected. This noise conforms to the law of 1/f. In fact, this is typical charge noise from the QD. The green line is the noise spectrum when the QD is not connected and almost overlaps with the red line above 10 Hz, indicating that the noise above 10 Hz does not come from the QD. The blue line is the noise spectrum when the amplifier input is open, indicating that the noise above 10 Hz comes from the DC line. Compared with Ref. [41], the noise from the QD is low enough for the measurement of the qubit. On the other hand, the capacitance and resistance of the DC line is the main reason for this high-frequency noise. To further reduce the noise source, we can switch to a coaxial line with a smaller capacitance in the future.

3.3. Spin State Readout

After being able to detect the QD charge state and control and measure the tunneling of electrons through a simple square waveform, we now introduce two of the most commonly used methods for spin-to-charge conversion: the Elzerman readout [49,50] and PSB readout [14,51–53].

3.3.1. Elzerman Readout

The process of the Elzerman readout is shown in Figure 7a. We set the voltage to locate the Fermi surface of the electron reservoir between the energy state of the electrons with different spin states. Therefore, the spin-up electrons can tunnel to the electron reservoir (after a period of time to load spin down electrons from the electron reservoir), while the spin down electrons cannot. Since the signal of SET responds to the two events of

electron tunneling in and out of the QD, a square wave is formed in the signal of the SET. By observing the change in the current, it can be determined whether electron tunneling occurs; then, it can be determined whether the spin state of the electron is up.

Figure 7b shows a series of the measured SET current signal while reading the spin state. The signal in the top panel has a square pulse, which corresponds to a spin up state. The signal in the bottom panel does not have such a pulse and indicates a spin down state. Based on the above process, we have achieved a single-shot readout of the electron spin state.

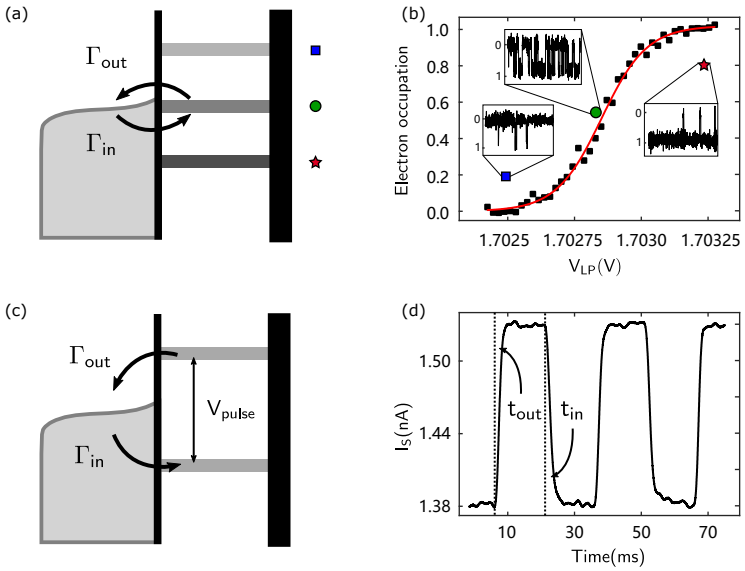

Figure 5. Measurement of the electron temperature and tunneling rate. (**a**) Schematic diagram of different positions of the QD energy state and the Fermi surface of the electron reservoir. (**b**) The probability of electron occupation probability. The electron temperature can be fitted as 223.8 ± 0.8 mK. The inset shows RTS for different electron occupation situations: the circle, square and star marks correspond to the alignment, negative bias and positive bias, respectively. (**c**) Electron tunnel in the QD when the voltage is high and vice versa. (**d**) The average current of the electron tunneling by applying a square wave with a 30 ms period. The average current decays exponentially with the tunnel time, and is characteristic of a Poisson process. A single exponential fitting can be used to obtain t_{on} and t_{off}.

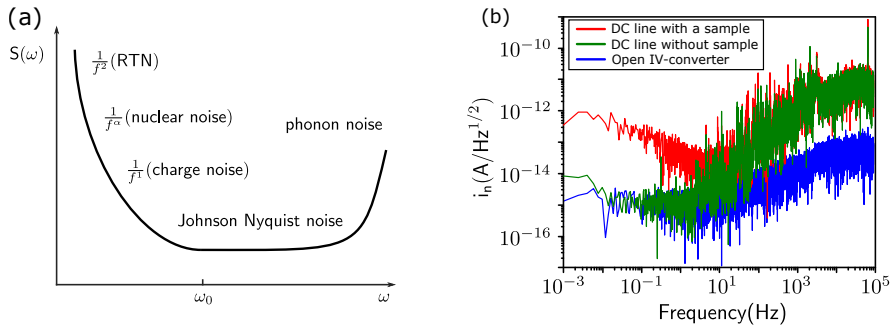

Figure 6. Measurement of the noise spectrum in silicon QD. (**a**) Typical noise spectrum of a silicon QD; the noise from the measurement system is not included. Here, ω_0 is the spin resonance frequency. (**b**) The noise spectrum is measured by a dynamic signal analyzer (SR785) in our system and the spectrum contains three conditions: DC line with a sample, DC line without sample and open I–V converter.

3.3.2. PSB

For the PSB readout, we first need to know the double spin eigenstates; the singlet (S) and triplet (T, include T_0, T_+ and T_-) states:

$$S = \frac{|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle}{\sqrt{2}}, T_0 = \frac{|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle}{\sqrt{2}}, T_+ = |\uparrow\uparrow\rangle, T_- = |\downarrow\downarrow\rangle \quad (4)$$

When there is no magnetic field, the singlet state is the ground state. The three-spin triplet state energies degenerate, which is referred to as the T state. This T state is an excited state. Now, we consider two charge states in a DQD: (1,1) and (0,2). For the (0,2) state, there are two electrons in one QD. According to the Pauli exclusion principle, the spin wave function of the electrons in the T state is symmetric, so two electrons must occupy different orbital states. Therefore, S(0,2) and T(0,2) are non-degenerate, as shown in Figure 7c,d. Δ_{ST} is the energy difference between S(0,2) and T(0,2). However, for the (1,1) state, two electrons are located in their respective QDs, thus avoiding the Pauli exclusion principle and two electrons can occupy one orbital state. Therefore, S(1,1) and T(1,1) are almost degenerate, as shown in Figure 7c,d.

Based on these energy states, we now introduce the PSB readout. As shown in Figure 7c, when a negative bias is applied (the Fermi surface of the source is higher than the drain), electrons in the source can first tunnel to the S(1,1) or T(1,1) state. When tunneling to the S(1,1) state, the electron can continue to tunnel to S(0,2) and then reach the drain to form current. When tunneling to the T(1,1) state, the electron cannot continue to tunnel to S(0,2) due to the PSB, and T(0,2) is higher than T(1,1), so the electron cannot enter any (0,2) charge states, and the current is suppressed. Figure 7d shows the positive bias condition. The Fermi surface of the source is lower than the drain. The electrons in the drain tunnel to the S(0,2) state, and then through the S(1,1) state to the source to form a current. No blockade occurs in the process, so there is current in the entire bias triangle region. In addition, for the PSB readout, we can use the SET to sense the charge states in DQD, and the operating temperature can be raised to higher than 1 kelvin [34,35].

3.3.3. Measurement of Spin Lifetime

After being able to perform a single-shot measurement to read the spin state, we can use the same waveform to measure the spin lifetime (T_1) [50]. The process of a typical single-shot readout is shown in Figure 8a. First, we reduce the voltage for electron evacuating from the QD; this is also referred to as "empty". Then, we raise the voltage so that electrons can tunnel from the electron reservoir to the QDs, which is also called "load". At this time the spin state of the electron in QD is random. Finally, we carefully reduce the voltage to locate the Fermi surface of the electron reservoir between the energy state of different spin electrons to "read" the spin state. We count the number of spin relaxation events for different load time periods. Figure 8b illustrates that the probability of the spin up state ($P_\uparrow$) decreases exponentially, so the T_1 can be obtained by fitting the exponential function.

3.4. Manipulation of the Spin Qubit

Now that we are able to read the spin state via the single-shot readout method, we introduce the manipulation of the spin qubit. There are two mainstream manipulation methods: ESR [16,53,54] and EDSR [23,52,55,56,67,68]. The ESR can be achieved by applying an alternating magnetic field B_1(5–50 μT) perpendicular to the external magnetic field B_{ext} (typically 150–1500 mT) via an antenna structure. For EDSR, we apply an alternating electric field combined with spin-orbit coupling to flip the spin. However, the natural spin–orbit coupling in silicon is weak, so we need micromagnets to introduce a gradient magnetic field to construct synthetic spin-orbit coupling. The advantages of EDSR include a fast spin flip rate, low heating, ease of fabrication, etc. However, the additional magnetic field from the micromagnets makes it difficult to find the resonance frequency $\gamma_e(B_{\text{ext}} + B_1)$ of the qubit. Therefore, we introduce rapid adiabatic passage to solve this problem.

3.4.1. Rapid Adiabatic Passage

We use frequency chirped microwave bursts, and when the excitation frequency passes through the resonance frequency, the electron spin is inverted (see Figure 9b) [23,55,56]. Figure 9a shows the principle of the rapid adiabatic passage process. In the reference frame rotating at the resonance frequency, the Hamiltonian of the system is the following [56]:

$$H(t) = \frac{1}{2}\frac{\partial}{\partial t}(\Delta\nu)t\sigma_z + \nu_1\sigma_x \tag{5}$$

Here, $\Delta\nu$ is the microwave frequency detuning from the resonance frequency, and ν_1 is the spin flip rate.

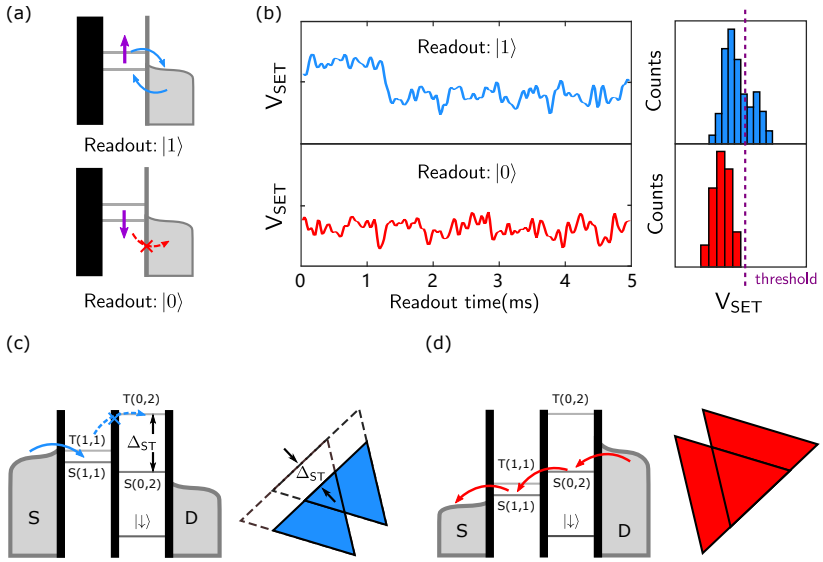

Figure 7. Spin-charge conversion. (**a**) Schematic diagram to read the spin state by the Elzerman readout. The spin-up electrons can tunnel out because the energy is higher than the Fermi surface of the electron reservoir and vice versa. (**b**) The measurement result of the spin state is read out by the Elzerman method in our experiment. When the electron in spin-up state tunnels out, there is a high level in the signal. The electron in spin-down state cannot tunnel out, so the signal remains at a low level. (**c**) Schematic diagram of the energy state and corresponding measurement results of the electron transition current with a negative bias. Δ_{ST} is the energy difference between the S and T states. When the energy detuning is less than Δ_{ST}, PSB occurs. (**d**) Schematic diagram of the energy state with a positive bias. Here, no PSB occurs.

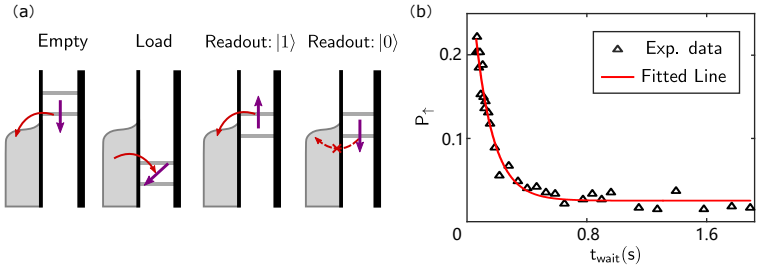

Figure 8. Schematic diagram and measurement result of T_1. (**a**) Schematic diagram of a single-shot readout for T_1 measurement. (**b**) Measured spin up probability ($P_\uparrow$) as a function of waiting time (t_{wait}). The fitting result of T_1 is 335 ± 5 ms for the left QD.

We use the Landau–Zener theory to solve this time evolution of a two-level system that is described by a linearly time-dependent Hamiltonian. The probability of adiabatic transition from one eigenstate to the other is given by [56]

$$P = 1 - \exp\left(-4\pi^2 \frac{\nu_1^2}{\left|\frac{\partial}{\partial t}(\Delta\nu)\right|}\right) \tag{6}$$

An electron spin in the $|\downarrow\rangle$ state will flip to the $|\uparrow\rangle$ state if the microwave frequency sweeps across the resonance frequency. To satisfy the adiabatic evolution condition, the sweep rate $\left|\frac{\partial}{\partial t}(\Delta\nu)\right|$ cannot be too fast compared with ν_1.

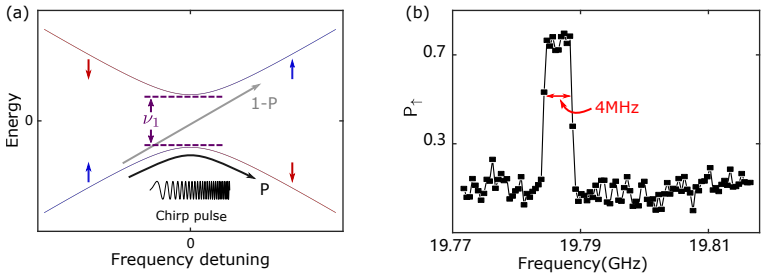

Figure 9. Schematic explanation and measurement result of rapid adiabatic passage. (**a**) Schematic explanation of rapid adiabatic passage in the rotating reference frame. (**b**) $P_{\uparrow}$ as a function of microwave frequency with a 0.5 ms burst time and a 4 MHz frequency modulation depth.

3.4.2. Rabi Oscillation

After calibrating the resonant frequency through the rapid adiabatic passage, we now use a single-frequency microwave combined with a single-shot readout to manipulate the qubit [54,56], as shown in the inset of Figure 10b. Figure 10a shows the Rabi pulsing scheme. First, we increase the voltage so that electrons in the $|\downarrow\rangle$ or $|\uparrow\rangle$ state cannot tunnel from the QDs to the electron reservoir. We apply the microwave pulse before the next stage to flip the electron spin. Then, as mentioned in Section 3.3.3, we carefully decrease the voltage to locate the Fermi surface of the electron reservoir between the energy states of different spin electrons to "read" the spin state. At the end of the "read" phase, the electron spin state will be $|\downarrow\rangle$ no matter the spin state at the beginning. Figure 10b shows the result of a Rabi oscillation. As the microwave duration time increases, the spin of the qubit continuously flips between $|\downarrow\rangle$ and $|\uparrow\rangle$ states. The amplitude of oscillation decreases with time due to noise. We fit the Rabi oscillation with the function $P(t) = A \cdot \exp\left(-t/T_2^{\text{Rabi}}\right) \cdot \sin(f_{\text{Rabi}} t)$. Here, $f_{\text{Rabi}} = 1.256 \pm 0.003$ MHz represents the spin flip rate, and $T_2^{\text{Rabi}} = 5.4 \pm 0.4$ µs represents the influence of the noise in Figure 10b.

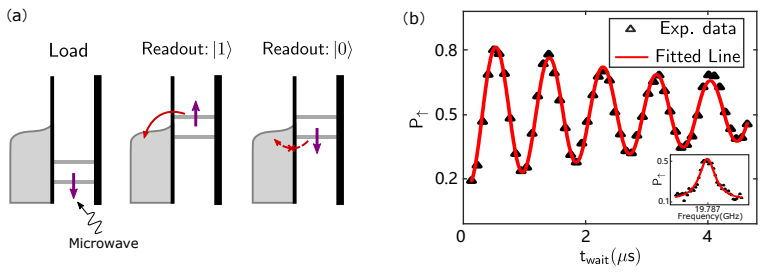

Figure 10. Schematic diagram and measurement result of Rabi oscillation. (**a**) Schematic diagram for Rabi oscillation. (**b**) $P_{\uparrow}$ as a function of t_{wait}. The inset shows $P_{\uparrow}$ as a function of microwave frequency around the resonance frequency $\nu = 19.787$ GHz.

4. Conclusions

In this paper, we provide an operation guide of Si-MOS QDs for spin qubits. First, we introduce the structure of the devices and the measurement circuit. Next, we show the charge stability diagram and detect the orbital and valley states. Then, we use a digitizer to detect the RTS and measure electron temperature and tunneling rate. Moreover, we introduce two commonly used methods, the Elzerman readout and the PSB readout, and use the single-shot readout method to measure the T_1. Finally, we give a brief introduction of ESR and EDSR, use rapid adiabatic passage to calibrate the resonance frequency of the spin qubit, and show the result of the Rabi oscillation. For future directions, researchers may be interested in hybrid qubits coupling [33], hot qubits [34,35], cryogenic control [69,70], foundry-fabrication [71,72], high fidelity readouts [73,74], and qubit number expansion [75].

Author Contributions: R.-Z.H., R.-L.M., M.N., X.Z. and H.-O.L. performed the experiments. R.-L.M. and M.N. fabricated the sample. G.C., K.W. and Y.Z. helped analyze the data. Z.-Z.K., G.L. and G.-L.W. prepared the silicon wafer. H.-O.L., R.-Z.H., X.Z., R.-L.M., M.N. and G.-P.G. designed the experiment, provided theoretical support, and analyzed the results. H.-O.L. and G.-P.G. supervised the project. R.-Z.H. and H.-O.L. wrote the manuscript, with input from all authors. All authors have read and agreed to the published version of the manuscript.

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Investigate on the Mechanism of $HfO_2/Si_{0.7}Ge_{0.3}$ Interface Passivation Based on Low-Temperature Ozone Oxidation and Si-Cap Methods

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Abstract: The interface passivation of the $HfO_2/Si_{0.7}Ge_{0.3}$ stack is systematically investigated based on low-temperature ozone oxidation and Si-cap methods. Compared with the $Al_2O_3/Si_{0.7}Ge_{0.3}$ stack, the dispersive feature and interface state density (D_{it}) of the $HfO_2/Si_{0.7}Ge_{0.3}$ stack MOS (Metal-Oxide-Semiconductor) capacitor under ozone direct oxidation (pre-O sample) increases obviously. This is because the tiny amounts of GeO_x in the formed interlayer (IL) oxide layer are more likely to diffuse into HfO_2 and cause the $HfO_2/Si_{0.7}Ge_{0.3}$ interface to deteriorate. Moreover, a post-HfO_2-deposition (post-O) ozone indirect oxidation is proposed for the $HfO_2/Si_{0.7}Ge_{0.3}$ stack; it is found that compared with pre-O sample, the D_{it} of the post-O sample decreases by about 50% due to less GeO_x available in the IL layer. This is because the amount of oxygen atoms reaching the interface of $HfO_2/Si_{0.7}Ge_{0.3}$ decreases and the thickness of IL in the post-O sample also decreases. To further reduce the D_{it} of the $HfO_2/Si_{0.7}Ge_{0.3}$ interface, a Si-cap passivation with the optimal thickness of 1 nm is developed and an excellent $HfO_2/Si_{0.7}Ge_{0.3}$ interface with D_{it} of 1.53×10^{11} $eV^{-1}cm^{-2}$ @ $E-E_v = 0.36$ eV is attained. After detailed analysis of the chemical structure of the $HfO_2/IL/Si\text{-}cap/Si_{0.7}Ge_{0.3}$ using X-ray photoelectron spectroscopy (XPS), it is confirmed that the excellent $HfO_2/Si_{0.7}Ge_{0.3}$ interface is realized by preventing the formation of Hf-silicate/Hf-germanate and Si oxide originating from the reaction between HfO_2 and $Si_{0.7}Ge_{0.3}$ substrate.

Keywords: $HfO_2/Si_{0.7}Ge_{0.3}$ gate stack; ozone oxidation; Si-cap; interface state density; passivation

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1. Introduction

High-mobility channel materials and novel device architectures, such as FinFETs (Fin Field-Effect Transistor) and nanowire FETs, are proposed to address the demand for scaling CMOS (Complementary Metal-Oxide-Semiconductor) technology [1,2]. In contrast to other potential materials, such as germanium (Ge) or III–V materials, silicon germanium (SiGe) is considered the most promising channel material for PMOS due to its tunability of band gaps and high hole mobility [3]. However, one of the main challenges in integrating SiGe into the novel devices is obtaining a high-quality interlayer (IL) between high-k gate oxide and SiGe substrate.

To control the interface quality, many methods have been extensively explored, such as plasma (N_2 or NH_3) nitridation passivation [4,5], sulfur passivation [6], thermal oxidation [7,8], low-temperature ozone passivation [9–12] and Si-cap passivation [13]. Among them, low-temperature ozone passivation with low thermal budge and Si-cap passivation with excellent properties of interface are considered the most promising passivation methods. For example, the interface state density (D_{it}) of 2.2×10^{12} $eV^{-1}cm^{-2}$

is attained by using a low-temperature ozone oxidation to passivate the interface of $Al_2O_3/Si_{0.7}Ge_{0.3}$[11],and the D_{it} of 2×10^{11} $eV^{-1}cm^{-2}$ for the interface of $HfO_2/Si_{0.8}/Ge_{0.2}$ is realized by using a Si-cap passivation method [14]. However, the technique and mechanism of interface passivation of the HfO_2/SiGe via low-temperature ozone oxidation or Si-cap method still needs further investigation.

In this paper, we fabricated $HfO_2/IL/Si_{0.7}Ge_{0.3}$ gate stacks MOS capacitors by utilizing low-temperature ozone oxidation and Si cap passivation methods. We carefully compared their electrical properties, and the chemical structure of $HfO_2/IL/SiGe$ gate stacks. It is found that the post-HfO_2-depositon (post-O) ozone indirect oxidation is a better choice than a step-by-step procedure (pre-O) method in terms of D_{it} reduction. More importantly, the optimal Si cap method can realize a lower D_{it} of 1.53×10^{11} $eV^{-1}cm^{-2}$ @ $E-E_v$ = 0.36 eV by preventing the formation of Hf-silicate/Hf-germanate and Si oxide originating from the reaction between HfO_2 and $Si_{0.7}Ge_{0.3}$ substrate.

2. Materials and Methods

After standard HF-last cleaning, the 30 nm $Si_{0.7}Ge_{0.3}$ layer was epitaxially grown in a reduced pressure chemical vapor deposition system (ASM E2000 plus, Amsterdam, The Netherlands) on an 8-inch Si substrate. The low-temperature ozone passivation or Si-cap passivation was employed to passivate the interface of $HfO_2/Si_{0.7}Ge_{0.3}$. For low-temperature ozone passivation samples, the ozone oxidation can occur on the $Si_{0.7}Ge_{0.3}$ surface directly (step-by-step procedure (pre-O)) or post HfO_2 deposition (post-O). The ozone oxidation was carried out in 10% O_3/O_2 mixture ambience with the pressure of 3.1 Torr in an atomic-layer-deposition (ALD) chamber (Beneq TFS 200 system, Espoo, Finland). The temperature of the ozone oxidation was 300 °C. For Si-cap passivation, a Si-cap layer was in situ formed on the epitaxial $Si_{0.7}Ge_{0.3}$ layer in the same chamber. After the passivation treatment, the W/TiN or $W/TiN/HfO_2$ gate stack was deposited as the gate stack of MOS capacitors. Finally, $W/TiN/HfO_2/IL/Si_{0.7}Ge_{0.3}$ MOS capacitors were annealed in the forming gas (10% H_2, 90% N_2) at 350 °C for 30 min.

The chemical structures of the $HfO_2/IL/Si_{0.7}Ge_{0.3}$ stacks were studied by X-ray photoelectron spectroscopy (XPS), which was carried out in a Thermo Scientific ESCALAB 250xi (Waltham, MA, USA) system with a photon energy of 1486.7 eV (Al Kα source). The photoelectron emission take-off angle was 90° relative to the sample surface and the pass energy was 15 eV. Moreover, TEM (Transmission Electron Microscope) and EDX (Energy Dispersive X-Ray Spectroscopy) Mapping analysis were performed by using FEI Talos F200X (Hillsboro, MI, USA) to verify the gate stack lattice structure and element content. Multi-frequency capacitance-voltage (C-V) along with conductance-voltage (G-V) measurements were measured using a Keysight 4990 A (Santa Rosa, CA, USA), and leakage-voltage (I-V) was measured using an Agilent B-1500 semiconductor analyzer.

3. Results and Discussion

3.1. Low-Temperature Ozone Oxidation Passivation of $HfO_2/Si_{0.7}Ge_{0.3}$ Interface

In our previous work, the low-temperature ozone oxidation passivation method has been studied in detail based on $Al_2O_3/Si_{0.7}Ge_{0.3}$ gate stacks. It was found that oxidation time played an important role to obtain a high-quality interlayer (IL) and should be at least 5 minutes. Otherwise, the unoxidized Ge atoms would be trapped in the IL, causing the IL as well as the relevant electrical properties to deteriorate. Moreover, increasing oxidation time would result in an increase in the ratio of Si^{4+} to Si^{3+} of the oxide interlayer, which can help decrease the D_{it} [15]. Thus, we chose 30 min as the oxidation time, which has proven to be an optimal experimental condition, to passivate the $HfO_2/Si_{0.7}Ge_{0.3}$ interface in this work.

Figure 1a,b depicts the multi-frequency (1 kHz to 1 MHz) C-V characteristics of $W/TiN/Al_2O_3/IL/Si_{0.7}Ge_{0.3}$ (Al_2O_3 sample) and $W/TiN/HfO_2/IL/Si_{0.7}Ge_{0.3}$ (HfO_2-pre-O sample) MOS capacitors treated with 30 min ozone direct oxidation, respectively. The flat band voltages (V_{fb}) are also shown in the figures. The frequency dispersion features

of the C−V curves observed at gate biases smaller than the V_{fb}, are caused by trapping and de-trapping of holes at traps with energies between approximately mid-gap and the $Si_{0.7}Ge_{0.3}$ valence band edge, corresponding to the depletion of the $Si_{0.7}Ge_{0.3}$ substrate. Comparing Figure 1b with Figure 1a, it is observed that the dispersion feature increases considerably. The energy distributions of the interface state density (D_{it}) were extracted using the conductance method [16], and given in their respective inset in Figure 1. We can see that both of the D_{it} of the two samples decreases along with SiGe band gap energy and the maximum D_{it} values appear near the valence band edge (E_v). However, the maximum value increases from 3.96×10^{12} $eV^{-1}cm^{-2}$ for the Al_2O_3 sample to 2.67×10^{13} $eV^{-1}cm^{-2}$ for the HfO_2-pre-O sample. According to our previous work [17], it is known that for 300 °C/30 min ozone oxidation, about 54% of the Ge atoms of the outermost atomic layer of $Si_{0.7}Ge_{0.3}$ can be oxidized in the initial stage of oxidation. No more Ge atoms would take part in the oxidation process as the oxidation time increases. The GeO_x and SiO_x thickness of the formed oxide layer are estimated to be 0.15 nm and 0.72 nm, respectively. Compared with Al_2O_3, GeO_x is more likely to diffuse into HfO_2 and cause the HfO_2/SiGe interface to deteriorate [18]. Therefore, the increased D_{it} of the HfO_2-pre-O sample can be attributed to tiny amounts of GeO_x in the formed oxide layer.

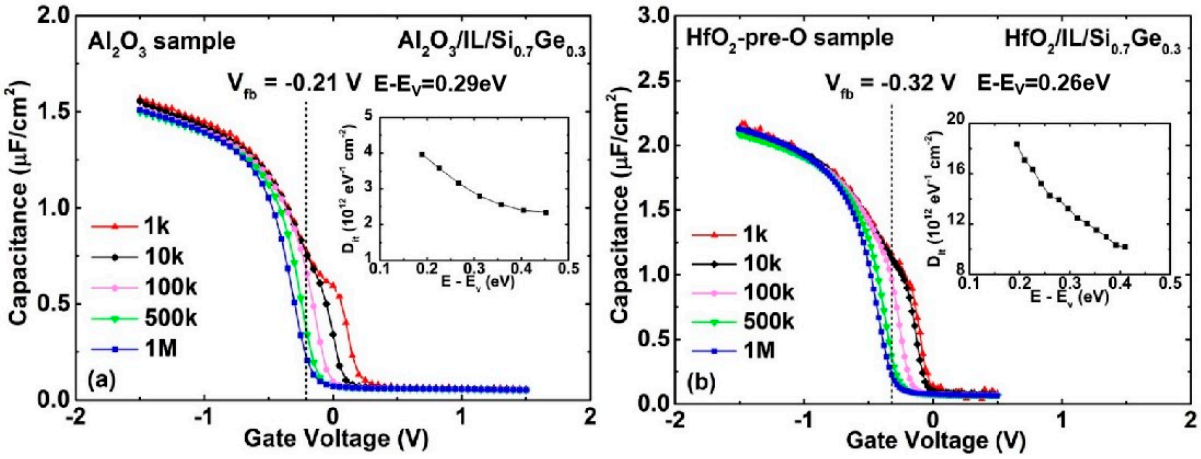

Figure 1. Multi-frequency C-V characteristics of (**a**) Al_2O_3 sample (**b**) HfO_2-pre-O sample with 30 min oxidation time (direct). The insets are their respective energy distributions of D_{it}.

Figure 2 depicts the multi-frequency (1 kHz to 1 MHz) C-V characteristics of W/TiN/HfO_2/IL/$Si_{0.7}Ge_{0.3}$ (HfO_2-post-O sample) MOS capacitor treated with 30 min ozone indirect oxidation, in which the ozone oxidation was carried out after the deposition of HfO_2. The corresponding energy distributions of D_{it} is also given in the inset. Compared with Figure 1b, an obvious improvement in the frequency dispersion feature is observed, and the D_{it} value decreases by about 50%. We infer that the improvement may arise from the following two factors. First, due to the barrier effect of the HfO_2 layer on the diffusion of the oxidizer, the amount of oxygen atoms reaching the interface becomes fewer. Because silicon oxidation is more favorable than germanium oxidation in view of thermodynamic considerations [19], germanium atoms are hardly oxidized in this case. Therefore, almost no GeO_x would diffuse into HfO_2 layer. In addition, the IL thickness of the HfO_2-post-O sample is smaller than that of the HfO_2-pre-O sample, which means the amounts of the Ge atoms accumulating at the IL/SiGe interface decrease accordingly. The experimental results prove that the post-O method is a promising technology to realize an HfO_2/IL/SiGe gate stack with small D_{it}.

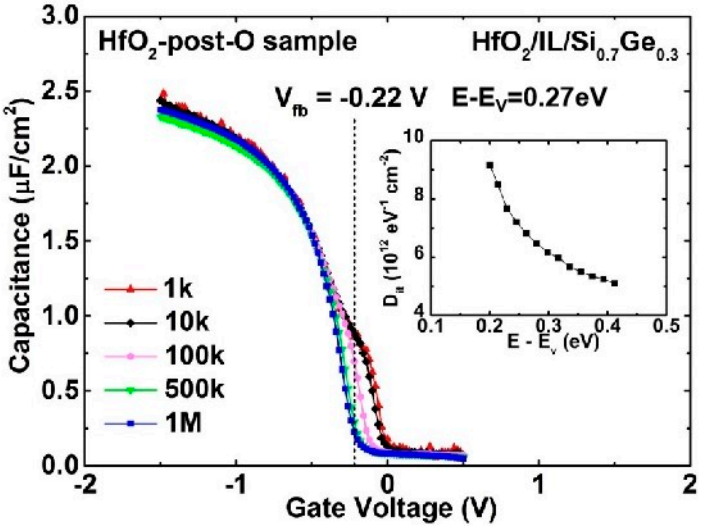

Figure 2. Multi-frequency C-V characteristics of HfO_2-post-O sample with 30 min oxidation time (indirect). The corresponding energy distributions of D_{it} is given in the inset.

The Al_2O_3 sample, HfO_2-pre-O sample and HfO_2-post-O sample were compared on capacitance equivalent oxide thickness (CET) at −1.5 V bias voltage in accumulation. The CETs of each are 2.28 nm, 1.5 nm and 1.37 nm respectively. Comparing the Al_2O_3 sample with the HfO_2, the CET of the Al_2O_3 sample is bigger. The HfO_2-post-O sample decreased the CET, compared to the HfO_2-pre-O sample. This is supposed to be related to the diffusion of GeO_x. In general, the diffusion of GeO_x is less in Al_2O_3 and HfO_2-post-O. Using the post-O method can limit the diffusion of GeO_x in HfO_2. The diffusion of GeO_x affects not only the CET but also the leakage current.

Figure 3 shows the gate Leakage of the Al_2O_3 sample, HfO_2-pre-O sample and HfO_2-post-O sample. Because GeO_x is not easily diffused in Al_2O_3, the leakage current is minimal for the Al_2O_3 sample. Comparing with the HfO_2-pre-O sample, the leakage current HfO_2-post-O sample can be reduced by an order of magnitude.

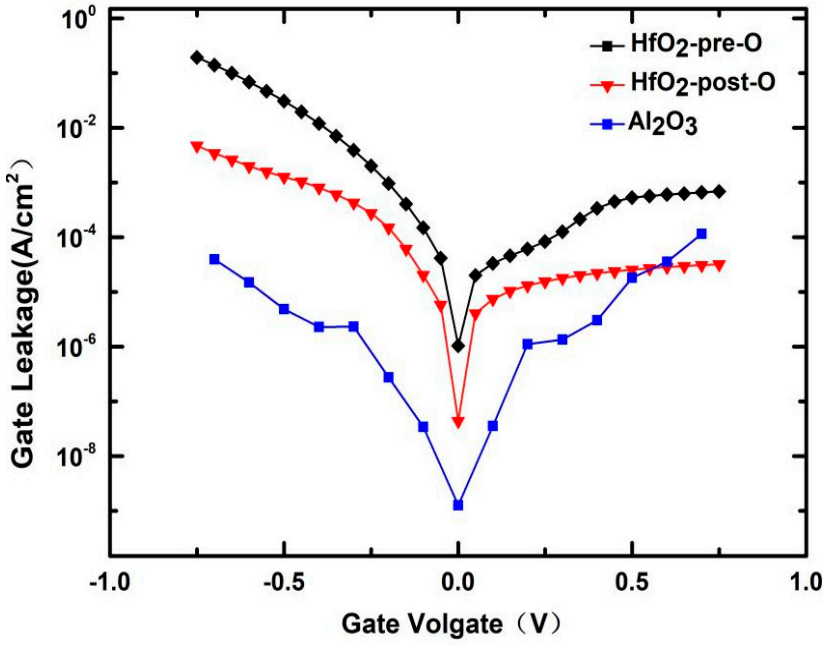

Figure 3. Gate leakage of Al_2O_3 sample, HfO_2-pre-O sample and HfO_2-post-O sample.

3.2. Si-Cap Passivation of $HfO_2/Si_{0.7}Ge_{0.3}$ Interface

To further reduce the D_{it} of the $HfO_2/Si_{0.7}Ge_{0.3}$ interface, Si-cap passivation is in situ performed on the $Si_{0.7}Ge_{0.3}$ layer with different thicknesses. It is found that if the Si cap thickness is larger than or equal to 2 nm, there is a step observed in its C-V curve because a second channel is formed in the Si cap layer. This can be avoided by further thinning of the Si cap layer to 1 nm. Moreover, multi-frequency C-V curves (1 kHz to 1 MHz) of the $W/TiN/HfO_2/IL/Si\text{-}cap/Si_{0.7}Ge_{0.3}$ MOS capacitor with 1 nm Si-cap are measured and shown in Figure 3. It is worthy to note that the frequency dispersive feature is obviously improved compared with the above ozone passivation. However, the CET of the Si-cap sample from Figure 4 may be inaccurate due to the large gate leakage in the accumulation region. In addition, it can be seen that the carriers are mainly confined in the $Si_{0.7}Ge_{0.3}$ layer under this optimal Si-cap thickness due to its large valance band offset. For quantitative analysis, the D_{it} of 1.53×10^{11} $eV^{-1}cm^{-2}$ @ $E-E_v$ = 0.36 eV is attained by using the conductance method. Meanwhile, HRTEM, Si and Ge element EDX mapping of the $W/TiN/HfO_2/IL/Si\text{-}cap/Si_{0.7}Ge_{0.3}$ MOS capacitor with 1nm Si-cap is also implemented and shown in Figure 5. It is found that there is a ~0.6 nm Si capping on the $Si_{0.7}Ge_{0.3}$ with a smooth and high-quality interfacial layer. The reduction of Si cap thickness of 0.4 nm is due to the oxidation of Si cap layer in the process of MOS capacitor fabrication. Therefore, 1-nm Si-cap in situ epitaxial grown is chosen as the optimal Si-cap thickness.

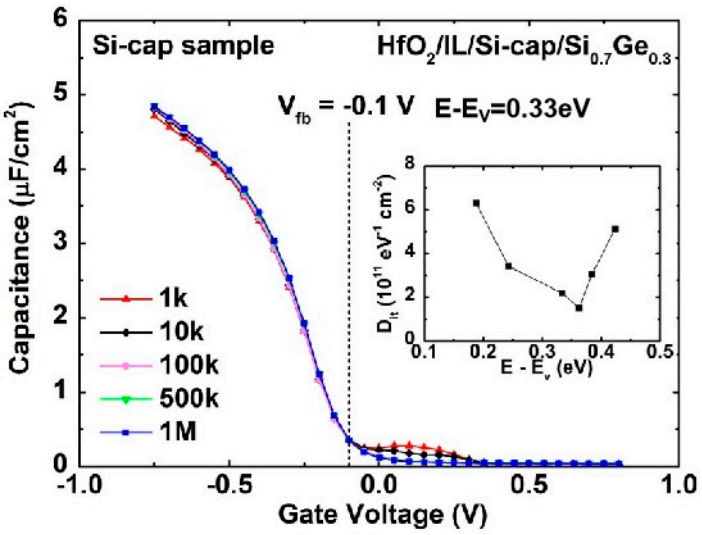

Figure 4. Multi-frequency C-V characteristic of $W/TiN/HfO_2/IL/Si\text{-}cap/Si_{0.7}Ge_{0.3}$ MOS capacitor with 1 nm Si-cap.

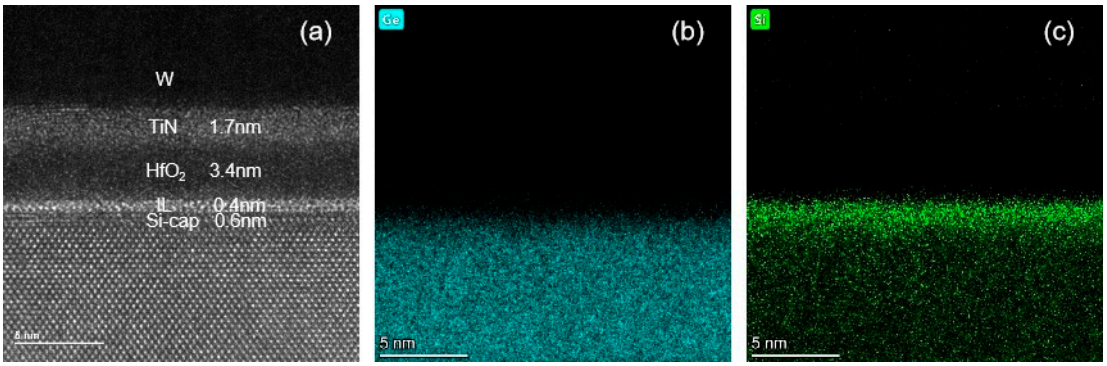

Figure 5. (**a**) HRTEM, (**b**) Ge, and (**c**) Si element EDX mapping of the $W/TiN/HfO_2/IL/Si\text{-}cap/Si_{0.7}Ge_{0.3}$ MOS capacitor with 1 nm Si-cap.

For the purpose of investigating the chemical structure of the HfO_2/IL/Si-cap/$Si_{0.7}Ge_{0.3}$ gate stack (Si-cap sample), X-ray photoelectron spectroscopy (XPS) technology is implemented. The chemical structure of the HfO_2/$Si_{0.7}Ge_{0.3}$ gate stack (SiGe sample), in which HfO_2 is deposited on $Si_{0.7}Ge_{0.3}$ directly, is also analyzed as a control sample. Gaussian-Lorentzian line shapes are used for deconvolution of all the spectra after standard Shirley background subtraction [20]. Figure 6a,b shows the Hf 4f core-level spectra of the Si-cap sample and SiGe sample, respectively. The spectra are both fitted with two component peaks. For the Si-cap sample (shown in Figure 6a), the Hf 4f spectrum consists of a main component at 16.8 eV related to the Hf-O bands in HfO_2, and a second component shifted by ~0.9 eV to higher binding energy, which is from the Hf-O-Si and/or Hf-O-Ge bonds. Because the electro-negativities of the Hf second neighbors (i.e., Si and Ge) are similar, it is difficult to distinguish the two contributions of Hf-O-Si and Hf-O-Ge bonds by XPS. It is worth noting that for the SiGe sample (shown in Figure 6b), the areal intensity of Hf-O-Si/Hf-O-Ge is much more than that of Hf-O. This suggests that a large portion of HfO_2 would react with SiGe to form Hf-silicate/Hf-germanate during the HfO_2 ALD deposition process. In addition, no feature of lower banding energy (14.3 eV–14.8 eV) is detected, indicating that no metallic Hf-Si and/or Hf-Ge are formed in the two samples.

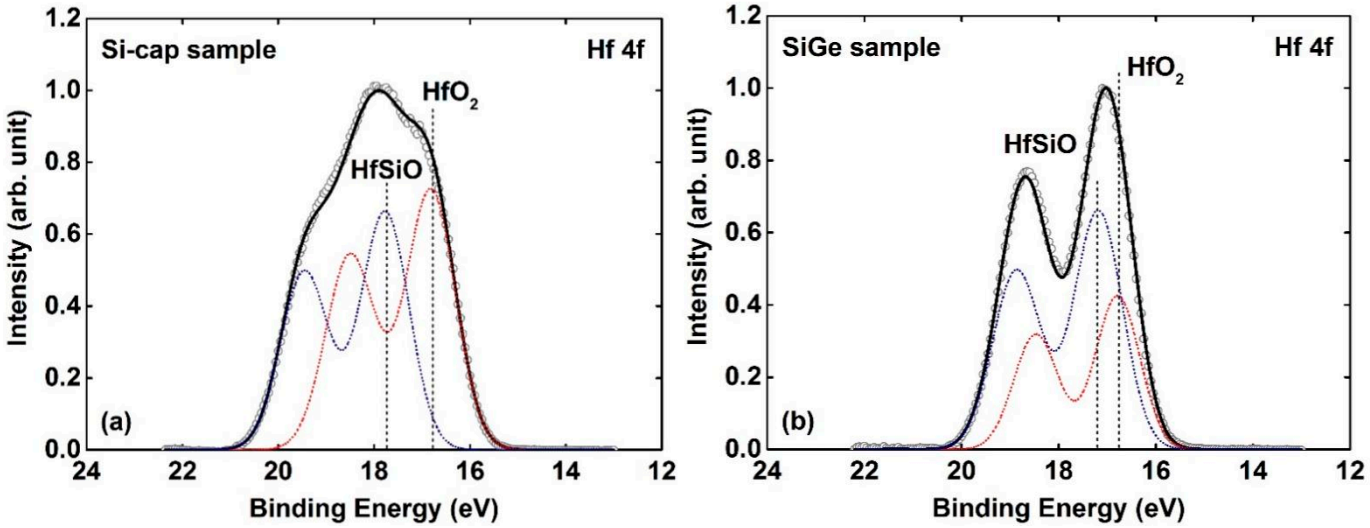

Figure 6. The fitted Hf 4f core-level spectra of (**a**) Si-cap sample and (**b**) SiGe sample. The blue and red dot lines denote the Hf 4f photoelectron from Hf-O-Si and/or Hf-O-Ge bonds and Hf-O bonds in HfO_2, respectively.

Figure 7a,b shows the Si 2p core-level spectra of the Si-cap sample and the SiGe sample, respectively. The spectra are decomposed into four component peaks i.e., Si 2p photoelectron from SiGe (~99.7 eV), SiO_x (~101.2 eV), HfSiO (~102.8 eV), and SiO_2 (~103.9 eV). For the Si-cap sample (shown in Figure 7a), the high-binding energy shoulder (101 eV~105 eV) contains few amounts of Si oxide (SiO_x and SiO_2) and Hf-silicate (HfSiO). When compared with the Si-cap sample, an obvious increase in the areal intensity of the high-binding energy shoulder (101 eV~105 eV) can be observed for the SiGe sample, and there is no peak corresponding SiO_x. Figure 8a,b shows the O 1s core-level spectra of the SiGe sample and Si-cap sample, respectively. The spectra are fitted by the O 1s of SiO_x (~532.8 eV), HfSiO (~532.08 eV) and HfO_2 (~531 eV). We can see that the O 1s photoelectron mainly originates from HfO_2 for the Si-cap sample, while that of the SiGe sample is mainly from SiO_x and HfSiO. This is consistent with the previous discussions about Hf 4f and Si 2p spectra. All of these results indicate that the interfacial region of the HfO_2/SiGe (SiGe sample) is a composite of large amounts of HfSiO (and/or HfGeO) and Si oxide (SiO_2). In other words, Si-cap can prevent the formation of Hf-silicate/Hf-germanate and Si oxide originating from the reaction between HfO_2 and SiGe substrate, and obtain an excellent HfO_2/SiGe interface.

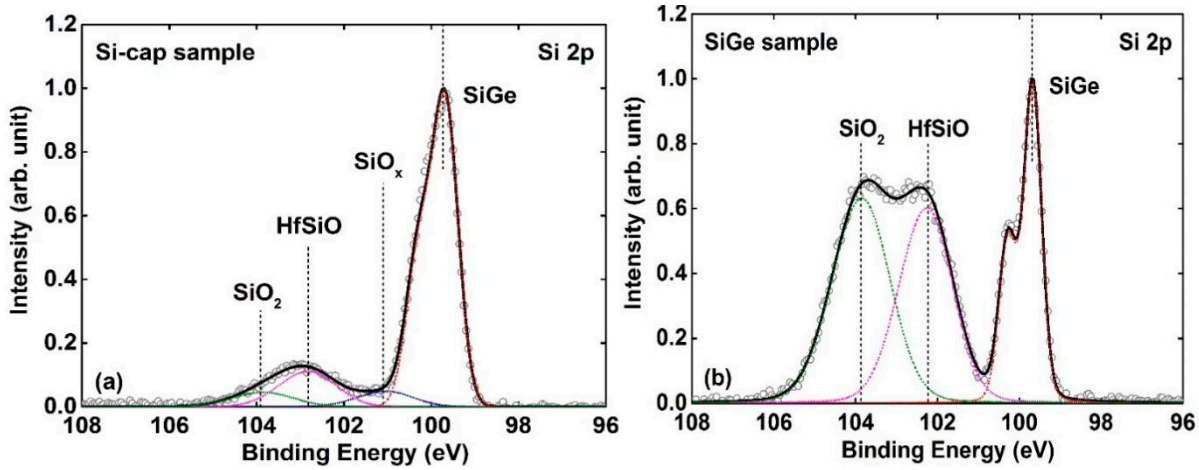

Figure 7. The fitted Si 2p core-level spectra of (**a**) Si-cap sample (**b**) SiGe sample. The red, blue, magenta, and green dot lines denote the Si 2p of SiGe, SiO_x, HfSiO, and SiO_2, respectively.

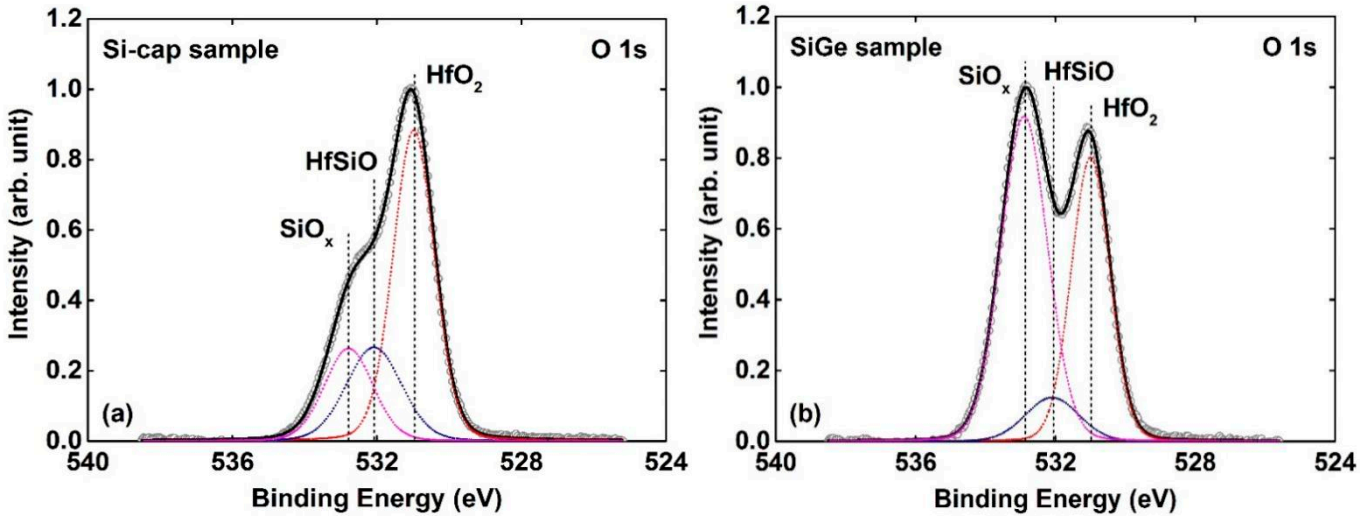

Figure 8. The fitted O 1s core-level spectra of (**a**) Si-cap sample (**b**) SiGe sample. The red, blue, and magenta dot lines denote the O1s photoelectron from HfO_2, HfSiO, and SiO_x, respectively.

4. Conclusions

In summary, the interface passivation of the $HfO_2/Si_{0.7}Ge_{0.3}$ stack is systematically investigated based on low-temperature ozone oxidation and Si-cap methods. Compared with pre-O method, the D_{it} of the post-O sample decreases by about 50% due to less GeO_x available in the IL layer. However, the D_{it} of the $HfO_2/IL/Si_{0.7}Ge_{0.3}$ gate stack still has room to be further optimized. Finally, an excellent $HfO_2/Si_{0.7}Ge_{0.3}$ interface with a D_{it} of 1.53×10^{11} $eV^{-1}cm^{-2}$ @ $E-E_v = 0.36$ eV is attained under the optimal Si cap method by preventing the formation of Hf-silicate/Hf-germanate and Si oxide from the reaction HfO_2 and $Si_{0.7}Ge_{0.3}$ substrate.

Author Contributions: Conceptualization, X.M., Y.W. and Y.L.; methodology, Q.Y., X.M., H.W., Y.W., G.W., J.Z., W.L., X.W., J.Y., Y.L. and W.W.; investigation, Q.Y., X.M., Y.W. and Y.L., data curation, Q.Y., X.M., H.W., Y.W. and Y.L.; writing original draft preparation, Q.Y., X.M., Y.W. and Y.L.; writing review and editing, X.M., Y.W., Y.L. and J.Z.; supervision, J.Y., Y.L. and W.W.; project administration, Y.L. and W.W.; funding acquisition, W.W. All authors have read and agreed to the published version of the manuscript.

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Epitaxial Growth of Ordered In-Plane Si and Ge Nanowires on Si (001)

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Abstract: Controllable growth of wafer-scale in-plane nanowires (NWs) is a prerequisite for achieving addressable and scalable NW-based quantum devices. Here, by introducing molecular beam epitaxy on patterned Si structures, we demonstrate the wafer-scale epitaxial growth of site-controlled in-plane Si, SiGe, and Ge/Si core/shell NW arrays on Si (001) substrate. The epitaxially grown Si, SiGe, and Ge/Si core/shell NW are highly homogeneous with well-defined facets. Suspended Si NWs with four {111} facets and a side width of about 25 nm are observed. Characterizations including high resolution transmission electron microscopy (HRTEM) confirm the high quality of these epitaxial NWs.

Keywords: in-plane nanowire; site-controlled; epitaxial growth; silicon; germanium; nanowire-based quantum devices

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1. Introduction

Si and Ge nanowires (NWs) have potential applications for high-performance transistors [1,2] and for disruptively quantum computation technology [3–6]. The controllable growth of NW arrays in wafer-scale remains the major challenge for large scale integration. The top-down method by patterning and etching can precisely fabricate NWs in wafer-scale but also induce additional defects during the nanofabrications. For instance, IMEC has previously reported the vertically stacked horizontal Si NWs with selective etching of Si/SiGe multilayer fin structures [1]. Moreover, by selectively etching Si, stacked SiGe NWs were obtained to improve the channel mobility [7]. However, the top-down fabrication introduces atomic surface roughness and damages, which deteriorate the carrier mobility of the NWs [8].

Alternatively, the self-assembled growth of NWs via a vapor-liquid-solid (VLS) mechanism can form high quality NWs with a sharp interface [9,10]. A mobility of 730 $cm^2(Vs)^{-1}$ [11] and a ballistic conduction up to several hundred nanometers [12] were reported in such {111}-oriented Ge/Si core/shell NWs. Compared to the {111}-oriented NWs, {110}-oriented Ge/Si core/shell NWs have substantially enhanced hole mobility as high as 4200 $cm^2(Vs)^{-1}$ at 4 K [13]. Although, the VLS-grown Si and Ge NWs have recently presented single crystalline with controllable orientation [14–18], the out-of-planar geometry has not been compatible with the well-established planar device processing technology. Ex-situ assembly methods such as contact printing and capillary assembly have been developed to align the NWs on a target substrate [19,20], however, for such VLS-grown NWs, the precise positioning at a large scale is a challenge. Another challenge of the VLS-grown NWs is the poor size-controllability (including both length and diameter), which is considered to reduce the collective properties of NWs.

Combining top-down nanofabrication and bottom-up self-assembly, we have recently demonstrated site-controlled growth of Ge hut wires on trench-patterned Si (001) substrate [21]. The Ge hut wires have a height of 3.8 nm with sharp {105} facets specifically

oriented along <100> directions with high scalability. They are grown under a relatively high growth temperature where Si and Ge intermixing leads to a reduced Ge composition in the wires. Therefore, it is desirable to obtain epitaxial Si and Ge NWs with controllable size, orientation, and composition. In this work, we epitaxially grow {110}-orientated in-plane Si, SiGe, and Ge NWs on pre-patterned Si NW arrays. The pre-patterned Si NWs with an inverted trapezoidal structure are obtained through nanofabrications. On such pre-patterned Si NWs, homogeneous Si NWs with controllable sizes are epitaxially grown by molecular beam epitaxy. Furthermore, we demonstrate the formation of the conformal SiGe NWs and Ge NWs with {113} facets on the diamond-shaped Si NWs with {111} facets and truncated Si NWs. By transmission electron microscopy (TEM) characterizations, we investigate the material properties of the NWs mentioned above, which exhibit a high quality.

2. Materials and Methods

A CMOS-compatible top-down method was explored here to define the planar Si NW arrays on 200 mm Si (001) wafers. Figure 1 describes the fabrication process: a SiO_2 grating structure is firstly prepared along <110> direction on Si wafer by plasma enhanced vapor deposition, deep ultraviolet lithography, and reactive ion etching. Such SiO_2 grating structure is used as a hard mask for the subsequent wet etching of Si. The SiO_2 grating structure has periods that range from 360 to 440 nm with a constant duty cycle of nearly 1:1 and a depth of 150 nm. After dipping for 5 s in a buffered HF solution (7:1) to remove the native oxide on the exposed Si, a diluted tetramethylammonium hydroxide aqueous solution (TMAH 5%) is used to create the planar Si NWs at 75 °C. The SiO_2 hard mask is finally removed in diluted HF solution.

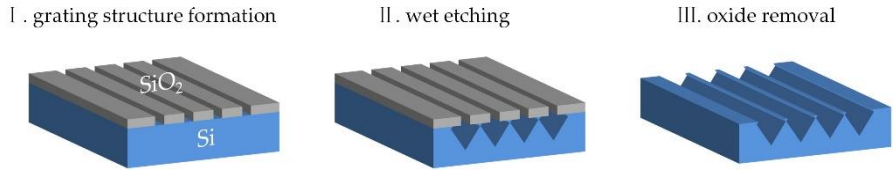

Figure 1. Schematic of process flow for the trapezoidal Si nanowire (NW) array.

By obtaining these pre-patterned Si NWs, we then studied the direct epitaxial growth of Si NWs, SiGe NWs, and Ge/Si core/shell NWs inside a SiGe molecular beam epitaxy system (Octoplus 500 EBV, MBE-Komponenten, Weil der Stadt, Germany). The patterned wafer was cleaved into 10 × 10 mm^2 small samples before dipping in a diluted HF solution for deoxidation and hydrogen passivation. To reduce the thermal instability of these tiny pre-patterned NWs, a low-temperature dehydrogenation was performed at 500 °C. The Si epitaxial NWs were obtained after homoepitaxial growth of Si at growth temperatures from 380 °C to 480 °C with a growth rate of 1 Å/s.

The SiGe NWs and Ge NWs were grown on the Si epitaxial NW after deposition 20 nm Si layer at 450 °C and 380 °C, respectively. The SiGe NWs were obtained by depositing 10 nm $Si_{0.5}Ge_{0.5}$ and 10 nm Si at 350 °C, where the growth rate of Si and Ge was 0.5 Å/s. The Ge NWs were obtained by depositing 2 nm Ge at 300 °C with a growth rate of 0.3 Å/s. The Ge/Si core/shell NWs were further formed after the deposition of 3 nm Si capping layer at 300 °C.

Focus ion-beam (FIB) system (NanoLab Helios 600i, FEI, Hillsboro, USA) equipped with high-resolution field-emission scanning electron microscope (SEM) was employed to elucidate the morphology of NWs and prepare the TEM lamellae. Before the FIB-milling, the NW sample was coated with 5 nm Ti and 50 nm Au for protection. TEM was performed to verify the quality of these epitaxial NWs, using a JEOL 2100 plus, operating at 200 kV.

3. Results and Discussion

3.1. Planar Trapezoidal Si NW Arrays

TMAH solution provides anisotropic wet etching for Si, with selectivity more than 1:10 between the Si {111} and Si {100} planes [22]. Therefore, {111}-faceted V-grooves were fabricated along the <110> direction, as shown in the SEM images (Figure 2a,b). In Figure 2a, on the tips of the Si V-grooves, we observed a Si hourglass figure with inverted {111} facets contributing to the SiO_2 hard mask. With optimized etching conditions, the formation of Si NWs with an inverted triangular or trapezoidal shape are achieved. Multiple widths of Si NWs ranging from 20 nm to 40 nm can be fabricated simultaneously on 200 mm Si (001) wafer by varying the pattern sizes. Figure 2a shows trapezoidal Si NWs with a minimum width of approximately 20 nm, while still preserving good uniformity, as confirmed by the surface SEM images, as shown in Figure 2b. The average width of the neck is approximately 3 nm, as shown in the inset of Figure 2a, expected to be facilely isolated by thermal oxidation [23,24]. The lengths of NW arrays are defined ranging from 2 μm up to 2 mm, suggesting a large aspect ratio (length: width) of nearly 10^5.

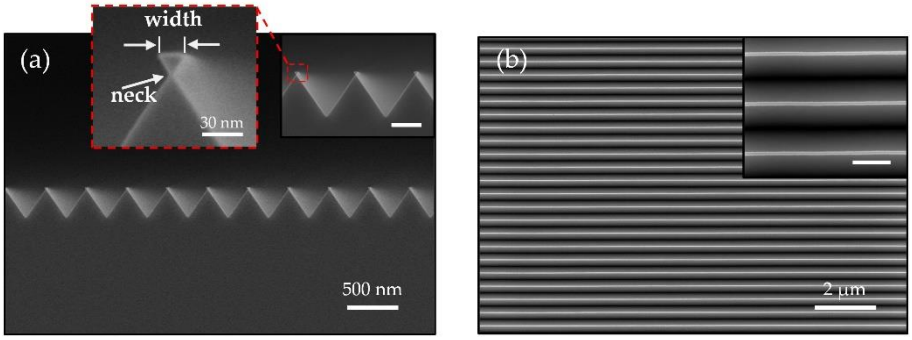

Figure 2. (**a**) Cross-sectional view and (**b**) top view SEM images of the Si NW array with an average wire width of 19 nm. Insets: zoom-in SEM images of the NWs. Scale bar of insets: 300 nm.

3.2. Homoepitaxy of Si NWs

Figure 3a presents a typical NW array by homoepitaxially grown Si on pre-patterned trapezoidal Si NWs. They are highly uniform. The width of these epitaxial Si NWs can be tuned from 30 nm to 50 nm by simply changing the growth conditions. Figure 3b shows the cross-sectional SEM image of epitaxial NWs obtained after the deposition of 20 nm Si layer on 30 nm wide pre-patterned Si NWs at 380 °C. Although only 20 nm Si were deposited at 380 °C, the epitaxial NW evolved rapidly toward the {111}-faceted morphology and a small Si (001) terrace with a width less than 10 nm on the top was left, driven by the reduction of surface energy. We observe a truncated {111}-faceted Si NW with a Si (001) terrace on the top (Figure 3b). By depositing 20 nm Si at 380 °C on a 40 nm wide pre-patterned NW array, a Si (001) terrace with enlarged width of approximately 17 nm was obtained (Figure 3c). If we increase the growth temperature to 450 °C, the Si (001) terrace will evolve into two symmetric Si (111) facets (Figure 4a), which leads to a 33 nm wide diamond-shaped NW. By keeping the growth temperature at 450 °C, when the Si layer is increased to 50 nm, the average width of diamond-shape Si NWs enlarges to approximately 48 nm (Figure 4b). The NWs are characterized by high-resolution TEMs (HRTEMs). Figure 4c provides a cross-sectional HRTEM image of a single Si NW obtained at the identical growth conditions to those in Figure 4b. The green dashed line in Figure 4c represents the interface between the epitaxial layer and the initial hourglass structure (pre-patterned trapezoidal Si NW). The inset of Figure 4c provides a zoom-in HRTEM image of the epitaxial interface labeled in Figure 4c, showing a perfect arrangement of Si atoms. Atoms deposited on the Si hourglass structure diffuse upwards to the shoulder areas to reduce the surface area, as illustrated by black arrows.

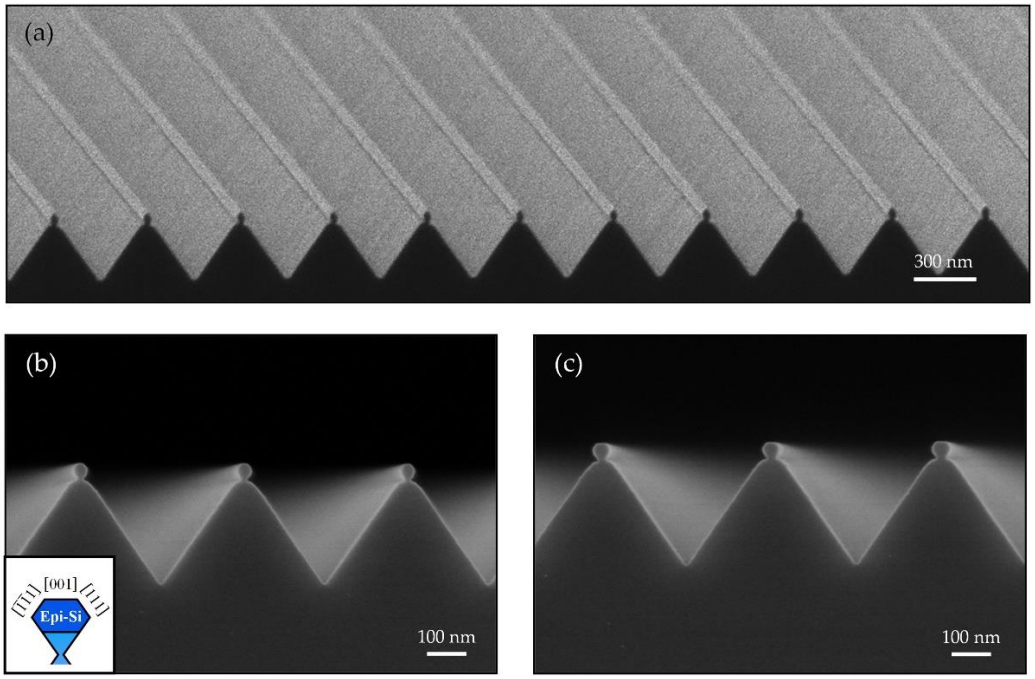

Figure 3. (**a**) Tilted SEM image showing the NW array of epitaxial Si on pre-patterned trapezoidal Si NWs. SEM images of epitaxial Si NWs obtained after the deposition of 20 nm Si at 380 °C on 30 nm wide pre-patterned trapezoidal NWs (**b**) and on 40 nm wide pre-patterned NWs at 380 °C (**c**). Inset of (**b**) schematically shows the truncated {111}-faceted cross-section.

Although the pre-patterned trapezoidal NWs are thermally stable at the aforementioned low-temperature epitaxy, we note that a high-temperature dehydrogenation process at more than 600 °C will deform the pre-patterned Si NWs. The thermal instability becomes remarkable for Si NWs with smaller dimensions [25,26], as we find that the pre-patterned NWs with a size of about 20 nm in Figure 2a deform into discrete Si beads only after 500 °C dehydrogenation. Similar phenomena have been previously reported on an isolated Si NW as Plateau–Rayleigh instability (PRI) [27,28], while the critical temperature reported is much higher at 775 °C for a Si NW with 100 nm diameter. In our case, the root causes of thermal instability are not just dominated by PRI, also strongly influenced by the fragile narrow Si necks as well as the surface diffusion between NWs and patterned V-grooves.

The supporting Si neck of the hourglass structure can significantly affect the thermal instability of the NW growth with small dimensions. Here, we then study the possibility of creating suspended NWs. Figure 5a shows a typical 2 μm long suspended Si trapezoidal NW with a sub-20 nm average width. The supporting Si necks are removed by similar fabrication method mentioned above with over-etched conditions. Absence of the neck, such suspended structure can avoid the diffusion between the NW and the V-groove more effectively. After the growth of the 20 nm Si layer, although the gap between the NW and the pre-patterned V-groove appears to be unclear in the SEM picture (Figure 5b), TEM characterization in Figure 5c has verified that still retains the suspended configuration and forms {111}-faceted diamond-shaped NW with a side width of about 25 nm. Overall, the suspended Si NW exhibit enhanced thermal stability and homogeneity with four {111} facets at small dimensions, which can be considered as an ideal isolated one-dimensional NW system. But these suspended Si NWs are limited to a few micrometers in length, due to insufficient mechanical strength.

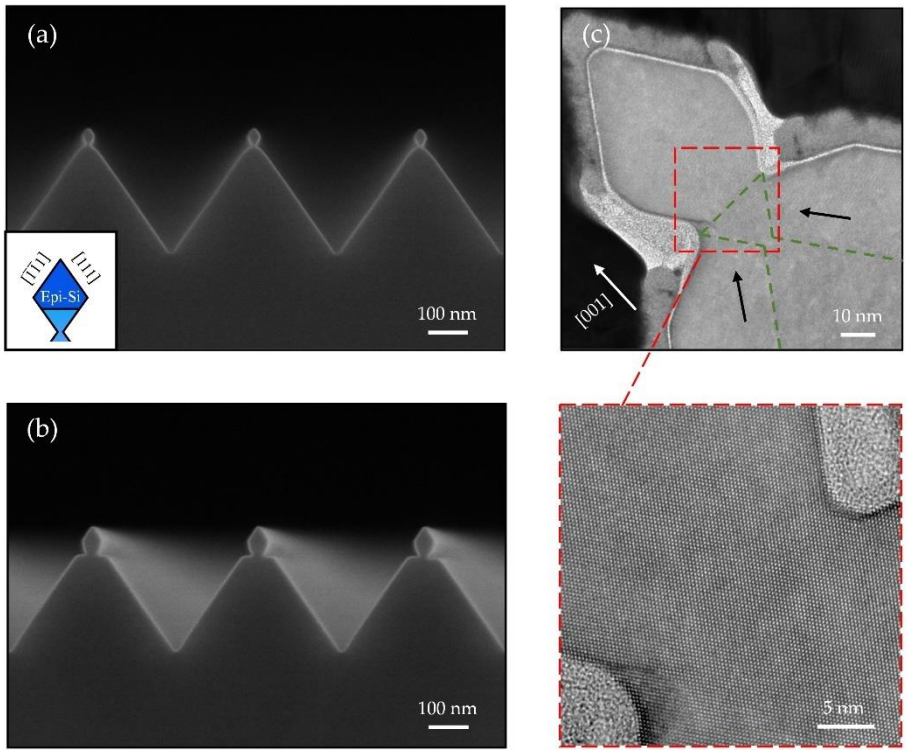

Figure 4. Cross-sectional SEM images of epitaxial Si NWs obtained after the deposition of 20 nm (**a**) and 50 nm (**b**) of Si at 450 °C on 30 nm wide pre-patterned trapezoidal NWs. Inset of (**a**) schematically shows the fully {111}-faceted cross-section. (**c**) Cross-sectional transmission electron microscopy (TEM) image of an epitaxial NW in (**b**), projected toward <110> direction. The interface of epitaxially formed Si NW and initial hourglass structure (pre-patterned Si NW) is sketched in green dashed line. The two shoulder areas marked in black are obtained by atomic diffusion during deposition. Inset of (**c**) shows a zoom-in high resolution transmission electron microscopy (HRTEM) confirming the perfect interface.

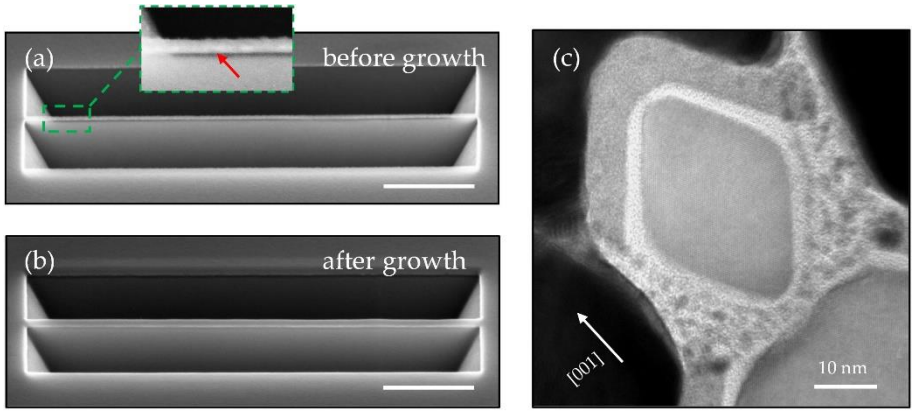

Figure 5. Suspended Si NW before (**a**) and after epitaxy (**b**). They both have a straight structure without distortion. Scale bar: 400 nm. (**c**) Cross-sectional HRTEM showing the high-quality diamond with four {111} facets after epitaxy. The red arrow in the inset of (**a**) highlights the suspended structure.

The size distributions of both the pre-patterned trapezoidal NW and epitaxial NWs were investigated. Figure 6a–c presents the SEM images of the pre-patterned NW and the epitaxial NWs obtained after the deposition of 20 and 50 nm-thick Si, respectively. After epitaxial growth, the rough surface of the pre-patterned NW has been significantly modified by forming atomic {111} facets. As illustrated in Figure 6d, the average width

of pre-patterned trapezoidal NWs is 29.8 nm with relative standard deviation of 6.4%. By depositing a 20 nm (50 nm)-thick Si layer, the epitaxially formed Si NWs exhibit average widths of 35.8 nm (46.0 nm), and the relative standard deviation of the width distribution is reduced to 3.9% (2.9%).

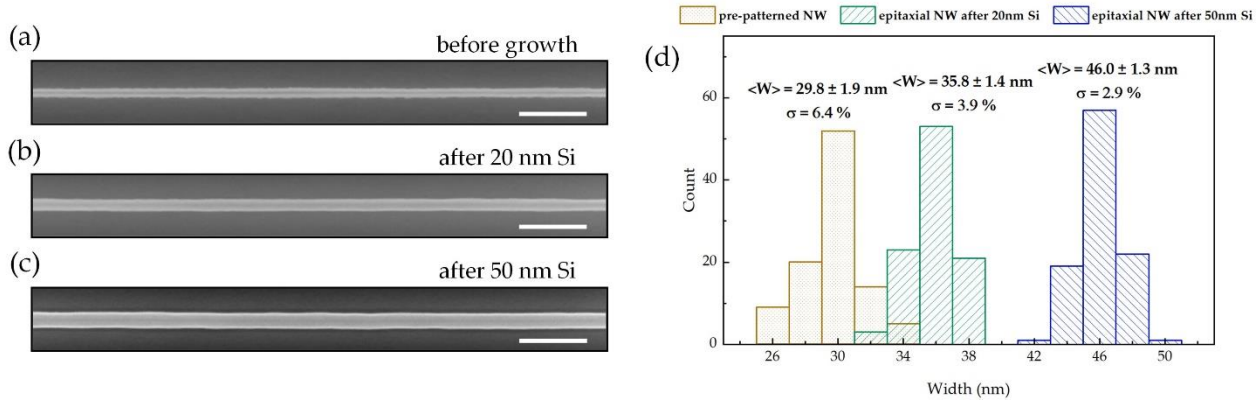

Figure 6. (**a–c**) SEM images of a 30 nm wide pre-patterned trapezoidal NW, epitaxial NWs after the deposition of 20 nm Si and 50 nm Si, respectively. Scale bar: 200 nm. (**d**) Statistical histogram showing the width distribution of 30 nm wide pre-patterned NWs, epitaxial NWs after the deposition of 20 nm and 50 nm Si layer. The average width <W> and relative standard deviation σ of the NWs are quoted.

3.3. Epitaxy of SiGe NWs

The epitaxial Si NWs provide platform for the subsequent growth of SiGe and Ge NWs. As mentioned, the SiGe NWs are obtained after the deposition of 10 nm $Si_{0.5}Ge_{0.5}$ and 10 nm Si layer at 350 °C on the {111}-faceted Si NW. We should note that all the thicknesses of the epitaxial layer mentioned in this work are referred to as-grown layer thickness on flat substrate. Here, the actual $Si_{0.5}Ge_{0.5}$ thickness that was deposited on the {111} facets should be 5.77 nm. The SEM images in cross-sectional view (Figure 7a,b) and top view (Figure 7c,d) indicate that these SiGe NWs are highly uniform. Attributed to the high Ge content in the SiGe layer, we can directly distinguish the SiGe layer in the magnified SEM image as shown in Figure 7b, where the SiGe layer has a brighter contrast.

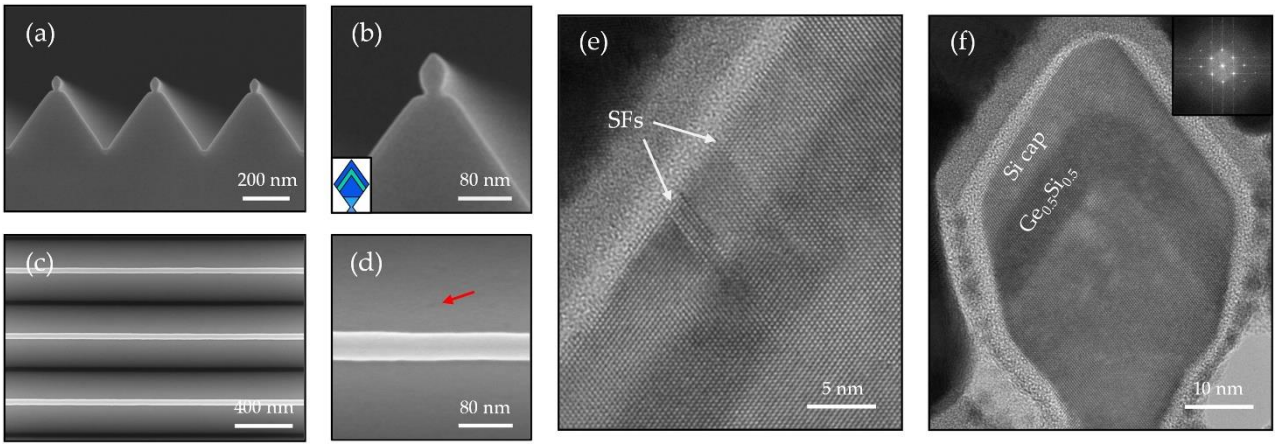

Figure 7. (**a**) Cross-sectional and (**c**) top view SEM images of the $Si_{0.5}Ge_{0.5}$ NW array and (**b**,**d**) the corresponding zoom-in images. The brighter contrast presenting in (**b**) results from the $Si_{0.5}Ge_{0.5}$ layer, where highlights in green in the schematic inset. The red arrow in (**d**) points to a strain-induced defect at the V-groove area. (**e**) Cross-sectional TEM image of SiGe at the V-groove area, showing that stacking faults (SFs) are generated from the interface and penetrate to the surface along the {111} gliding plane. (**f**) Cross-sectional HRTEM of a $Si_{0.5}Ge_{0.5}$ NW. Inset: FFT analysis of the SiGe/Si NW, showing a single set of spots indicating the SiGe is under fully strained condition.

Due to 2.1% lattice mismatch between $Si_{0.5}Ge_{0.5}$ and Si, misfit dislocations will generate if the SiGe film reaches the critical thickness for pseudomorphic growth. From the magnified planar SEM image (Figure 7d), the red arrow indicates strain-induced defects generated at the Si V-groove, indicating the excessive deposition of the SiGe layer. Figure 7e is a cross-sectional TEM image at the Si V-groove, showing that stacking faults (SFs) have generated from the interface and penetrated to the surface along the {111} gliding plane. In addition, we also observed other types of defects including SFs in parallel to the side-wall, attributed to plastic relaxation [29].

The situation is different for the SiGe NW. Figure 7f is a HRTEM image of directly grown in-plane SiGe/Si NW, with absence of defects, indicating the high crystal quality and conformal growth of the SiGe NW. The inset in Figure 7f is the fast Fourier transform (FFT) pattern of the SiGe/Si NW, showing only a single set of diffraction spots without distinct splitting. The FFT pattern is in-line with the spatial measurement result, indicating the SiGe NW is fully strained on Si NW.

3.4. Epitaxy of Ge/Si Core/Shell NWs

Despite a 4.2% lattice-mismatch between Ge and Si, we have further demonstrated Ge NW growth on the truncated {111}-faceted Si NW, where the average width of the Si (001) terrace is about 17 nm. As mentioned, the Ge NWs are obtained after the deposition of 2 nm Ge with a growth rate of 0.3 Å/s. In order to suppress the intermixing between Ge and Si, the growth is performed at a relatively low temperature of 300 °C [30]. Following a 3 nm Si capping layer deposited at 300 °C, Ge/Si core/shell NW is obtained, which can provide a high-performance one-dimensional hole gas system for exploring hole spin qubits [3,4,21]. Figure 8a,b shows cross-sectional and top view SEM images of the Ge/Si core/shell NW arrays, presenting a uniform morphology and smooth surface of NWs. To note, there are also numbers of strain-induced Ge islands formed on the Si V-grooves.

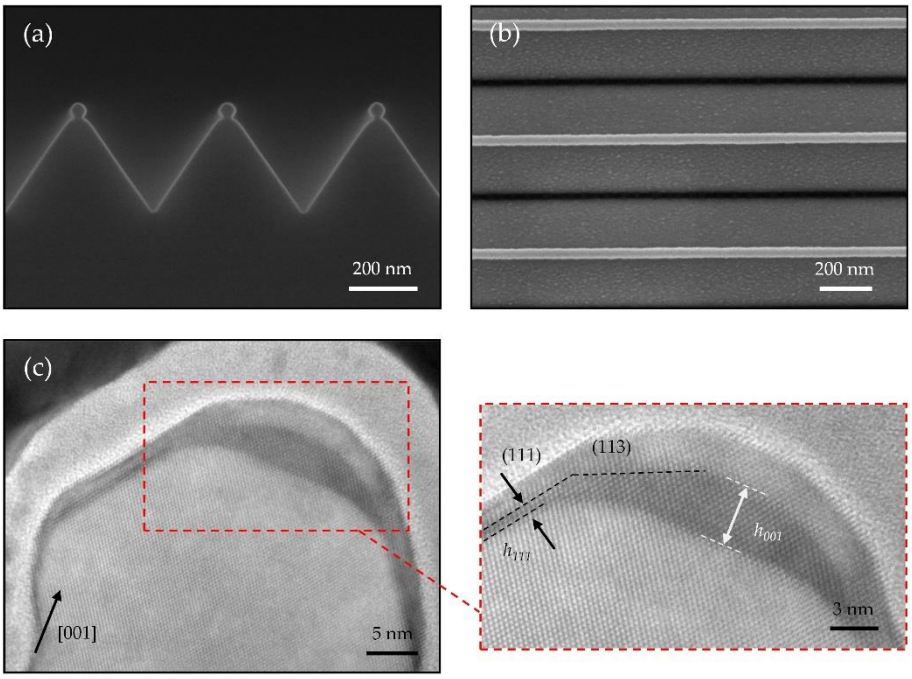

Figure 8. (**a**) Cross-sectional and (**b**) top view SEM images of the Ge/Si core/shell NW arrays. (**c**) Cross-sectional HRTEM image of a Ge/Si core/shell NW. Inset: a zoom-in HRTEM shows the two {113} side facets and the flat (001) top surface.

HRTEM micrograph in Figure 8c shows a typical cross-section of the Ge/Si core/shell NW. The Ge NW is grown on the <110>-oriented Si (001) terrace of the truncated {111}-faceted Si NW. The zoom-in HRTEM image in the inset of Figure 8c presents a trapezoidal geometry of the Ge NW composed of two (113) side facets and a flat (001) top surface. The formation of Ge (113) facets is attributed to the low surface energy, which has been reported in previous works [31–33]. Compared with <100>-oriented Ge hut wires [21,34], these <110>-oriented Ge NWs exhibit a larger aspect ratio of more than 0.2, where the height and width of the Ge NW are about 4 nm and 18 nm, respectively. Comparing the height of the Ge NW on the Si (001) terrace $h_{001} \approx 39.4$ Å and the thickness of the Ge wetting layer on (111) side facets $h_{111} \approx 6.3$ Å, we conclude that there is a significant Ge diffusion from the (111) facet towards the (001) facet. In terms of thermodynamics, Si (001) features higher surface energy than Si (111) [35,36], thus such Ge diffusion toward (001) facet is energetically favored.

Considering the low growth temperature, the intermixing of Ge and Si is strongly suppressed, thus we can expect an almost pure Ge-core in such Ge/Si NWs. Furthermore, atomically sharp interfaces between the Ge-core and the Si-shell are observed in the inset of Figure 8c, which further confirms the negligible intermixing between Ge and Si.

4. Conclusions and Perspectives

In summary, homogenous planar diamond-shaped Si NW arrays (30–50 nm in width) have been achieved on pre-patterned {111}-faceted Si arrays via direct epitaxial growth. Morphologies and dimensions of these NWs are controllable, while they can also be tuned under certain growth conditions. Suspended Si NWs exhibit diamond-shaped cross-section with four Si {111} facets. Furthermore, the SiGe NWs can be conformally grown on the {111}-faceted Si NWs. Additionally, {113}-faceted Ge NWs along [110] direction are also obtained after the deposition of 2 nm Ge on the truncated Si NWs. HRTEMs reveal the high quality of these epitaxial NWs.

The in-plane and site-controllable epitaxial NWs hold promise as the platform for the next generation of devices that require addressability and scalability. The Si and SiGe NWs have potential applications for high-perform transistors [7,23]. Moreover, the [110]-oriented Ge/Si core/shell NWs are expected to have a high mobility and a strong spin-orbit coupling [37,38] for the manipulation of hole spin qubits. Additionally, we believe this method is also applicable to obtain planar nanowires in other material systems with controllable size and orientation, such as III–V compound materials. However, the large V-groove poses a challenge for device fabrication, which needs to be addressed in future research work.

Author Contributions: Conceptualization, J.-J.Z.; methodology, J.-H.W. and J.-J.Z.; formal analysis, J.-H.W., T.W., and J.-J.Z.; investigation, J.-H.W., T.W., and J.-J.Z.; resources, J.-J.Z.; data curation, J.-H.W.; writing—original draft preparation, J.-H.W.; writing—review and editing, T.W. and J.-J.Z.; project administration, J.-J.Z.; funding acquisition, J.-J.Z. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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Investigation on $Ge_{0.8}Si_{0.2}$-Selective Atomic Layer Wet-Etching of Ge for Vertical Gate-All-Around Nanodevice

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Abstract: For the formation of nano-scale Ge channels in vertical Gate-all-around field-effect transistors (vGAAFETs), the selective isotropic etching of Ge selective to $Ge_{0.8}Si_{0.2}$ was considered. In this work, a dual-selective atomic layer etching (ALE), including $Ge_{0.8}Si_{0.2}$-selective etching of Ge and crystal-orientation selectivity of Ge oxidation, has been developed to control the etch rate and the size of the Ge nanowires. The ALE of Ge in p^+-$Ge_{0.8}Si_{0.2}$/Ge stacks with 70% HNO_3 as oxidizer and deionized (DI) water as oxide-removal was investigated in detail. The saturated relative etched amount per cycle (REPC) and selectivity at different HNO_3 temperatures between Ge and p^+-$Ge_{0.8}Si_{0.2}$ were obtained. In p^+-$Ge_{0.8}Si_{0.2}$/Ge stacks with (110) sidewalls, the REPC of Ge was 3.1 nm and the saturated etching selectivity was 6.5 at HNO_3 temperature of 20 °C. The etch rate and the selectivity were affected by HNO_3 temperatures. As the HNO_3 temperature decreased to 10 °C, the REPC of Ge was decreased to 2 nm and the selectivity remained at about 7.4. Finally, the application of ALE in the formation of Ge nanowires in vGAAFETs was demonstrated where the preliminary I_d–V_{ds} output characteristic curves of Ge vGAAFET were provided.

Keywords: vertical Gate-all-around (vGAA); p^+-$Ge_{0.8}Si_{0.2}$/Ge stack; dual-selective wet etching; atomic layer etching (ALE)

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1. Introduction

As the continuous scaling down of complementary metal-oxide-semiconductor (CMOS) technology nodes, novel device designs and high-mobility channel materials have been under investigation [1–8]. Vertical nanowire GAAFET is a powerful candidate for the 3 nm process, since its superiority in the short channel effects (SCEs) control [9,10] and can greatly reduce the gate pitch and increase the device integration density [11,12]. In addition, Ge is one of the most promising channel materials for pMOS due to its high carrier mobility and excellent bandgap [13]. Therefore, vertical GAAFETs with Ge as channel material have become an ideal choice for next era CMOS technology.

For vertical GAA devices, a new structure of vertical sandwich GAAFETs (VSAFETs) with Si source/drain and SiGe channel has been proposed [14,15]. The main process flow of VSAFETs is shown in Figure 1, the selective etching of the channel is a key step in the formation of vertical nanostructures. And the dimension of the channel is determined by selective etching. For the formation of Ge vertical nanowires, several selective etching methods have been reported, including dry etching with Cl_2 or CF_4 RF plasma [16–18] or

mixtures of Cl_2/HBr [19] and wet etching with H_2O_2 (HNO_3) [20] or TMAH [21] or other alkaline solutions [22] or mixtures of $HF/H_2O_2/CH_3COOH$ [20,23]. SiGe/Ge multilayer structures have been used to release with SiGe sacrificial layer etching to fabricate Ge nanowires in the lateral GAA device [19,24]. However, the above-mentioned methods for forming Ge nanowires are all continuous etching methods, and the etching depth is time-dependent. They achieve high selectivity and high etch rate at the cost of repeatability. At and beyond the 3 nm technology node, the gate, and channel of vGAAFETs need to be precisely aligned and the size controlled at the atomic-scale to achieve good device performance. In order to form Ge channels with self-aligned gate structure in VSAFETs, Ge was required to be laterally released to nano-scale size with source/drain-selective etching of Ge. Atomic layer etching (ALE) [25–27] is a promising technology that can remove ultra-thin materials through at least one self-limiting reaction step to achieve lower atomic-scale process variation. At present, the ALE for isotropic selective etching of SiGe to Si [28–30] has been reported, ALE for isotropic selective etching of Ge to GeSi has not been extensively reported. However, the ALE is not universal, and the selective ALE method depends on the recipe and it is difficult to achieve.

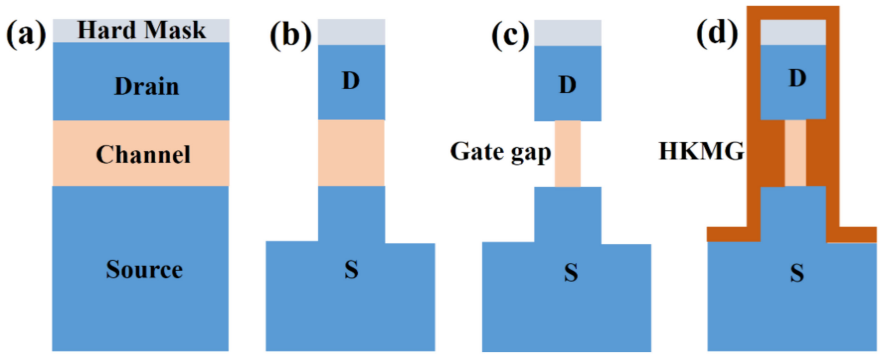

Figure 1. Schematic diagram of the basic flow of vertical Gate-all-around FET (vGAAFETs). (**a**) Sandwich structure and hard mask growth, (**b**) lithographic patterning and plasma anisotropic etching, (**c**) channel isotropic selective etching to form laterally depressed channels and gate gaps, (**d**) gate gaps filling with high-k metal gate (HKMG).

In this work, a developed wet dual-selective ALE process with selective etching of Ge and crystal-orientation selectivity of Ge oxidation was proposed. Based on the principle of atomic layer etching (ALE) and the oxidation–removal reaction of HNO_3 and deionized (DI) water, the characteristics of $Ge_{0.8}Si_{0.2}$-selective ALE of Ge at different temperatures were investigated systematically. The ALE process with a focus on the selective etching of Ge in p^+-$Ge_{0.8}Si_{0.2}$/Ge multilayers with 70% HNO_3 as oxidizer and DI water as oxide removal. The saturated relative etched amount per cycle (REPC) and selectivity at different HNO_3 temperatures between Ge and p^+-$Ge_{0.8}Si_{0.2}$ were investigated in detail. The application of ALE in the formation of Ge nanowires in VSAFETs was demonstrated.

2. Materials and Methods

The samples were performed on 200-mm p-type Si (100) wafers with a resistivity of 8–12 Ohm·cm. The high-quality epitaxial p^+-$Ge_{0.8}Si_{0.2}$/Ge vertical heterostructure multilayers started with a Ge buffer layer growth by ASM E2000 (ASM, Munich, Germany) plus RPCVD on Si wafers [20]. Dichlorosilane (SiH_2Cl_2), germane (10% GeH_4 in H_2), and diborane (1% B_2H_6 in H_2) were utilized as gas precursors for Si, Ge, and B, respectively. $Ge_{0.8}Si_{0.2}$ layers were in-situ doped with boron (concentration: 1.0×10^{19} cm^{-3}). The growth parameters and boron content have been carefully optimized to avoid boron precipitates in the $Ge_{0.8}Si_{0.2}$ layers [31]. The Ge buffer layer was grown with a two-step growth of low-high temperature (400 °C and 650 °C), and then a post-growth in situ annealing was applied at 820 °C in H_2 ambient [32]. Then, the p^+-$Ge_{0.8}Si_{0.2}$/Ge stacks were grown at 500 °C using an adjusted gas source with H_2 as a carrier gas. Then, a hard

mask with 30 nm SiN and 50 nm SiO_2 was deposited with plasma enhanced chemical vapor deposition (PECVD) on the epitaxial p^+-$Ge_{0.8}Si_{0.2}$/Ge stack layers. Finally, the p^+-$Ge_{0.8}Si_{0.2}$/Ge stack fins were patterned by I-line optical lithography and fabricated by using HBr-based dry anisotropic etching. Afterward, the samples were cut into small slices to facilitate the etching experiments.

There were three kinds of samples to estimate the etch rate and selectivity between Ge and p^+-$Ge_{0.8}Si_{0.2}$, as shown in Figure 2a–c. The etch rate of Ge (100 nm) and p^+-$Ge_{0.8}Si_{0.2}$ (300 nm) films with (100) flat surfaces were expressed by the etch rate per cycle (EPC). In order to measure the relative etch rate and selectivity of Ge and p^+-$Ge_{0.8}Si_{0.2}$ with ALE, a structure with (110) sidewall was fabricated and keep p^+-$Ge_{0.8}Si_{0.2}$/Ge/p^+-$Ge_{0.8}Si_{0.2}$/Ge/p^+-$Ge_{0.8}Si_{0.2}$ at 120 nm/50 nm/75 nm/50 nm/75 nm, and p^+-$Ge_{0.8}Si_{0.2}$ with boron dopant concentration of 1.0×10^{19} cm^{-3}. And the thickness and composition of the samples were kept constant among repetitive experiments. The prepared p^+-$Ge_{0.8}Si_{0.2}$/Ge stack structure is shown in Figure 2c. The relative total etched amount (tunnel depth) and GeSi loss are shown in the insert view, selective etching of Ge at (111) planes result in a lateral angle of 54.7°. The etch selectivity between p^+-$Ge_{0.8}Si_{0.2}$/Ge stacks with (110) sidewall is estimated by (tunnel depth + GeSi loss)/GeSi loss [28]. The relative etched amount per cycle (REPC) was calculated as the tunnel depth divided by the number of etching cycles. The flow diagram of ALE is shown in Figure 2d, the steps in the dashed frame are one cycle of ALE, including 70% HNO_3 oxidation, deionized (DI) water rinsing, and repeating the number of cycles until the required etching amount was reached. Before etching experiments, the samples were immersed in diluted BOE (dBOE, 49 wt% HF and 40 wt% NH_4F with volume ratio of 1:7) for 5 min to remove the natural oxide. During the experiments, the volume of the nitric acid solution was constant at 2 L, and the DI water was with overflow rinsing. As high-concentration nitric acid is easier to decompose, the experimental process requires a high-precision density meter to monitor the concentration of HNO_3 solution. In view of the different oxidation mechanism of nitric acid (HNO_3) concentration on Ge, the nitric acid concentration must be maintained at 70% with 5% variation in the ALE experiments compared to the continuous etching of Ge with nitric acid at low concentration. The experimental temperature was kept at 20 °C ± 0.5 °C, and the temperature with variation ±0.5 °C of the HNO_3 solution was controlled by the water bath method of the cryostat at low temperature. The oxidation time t_{ox} of the control recipe is 30 s and the DI water rinsing time (oxide remove time) is set as 1 min to make sure that oxide is removed totally.

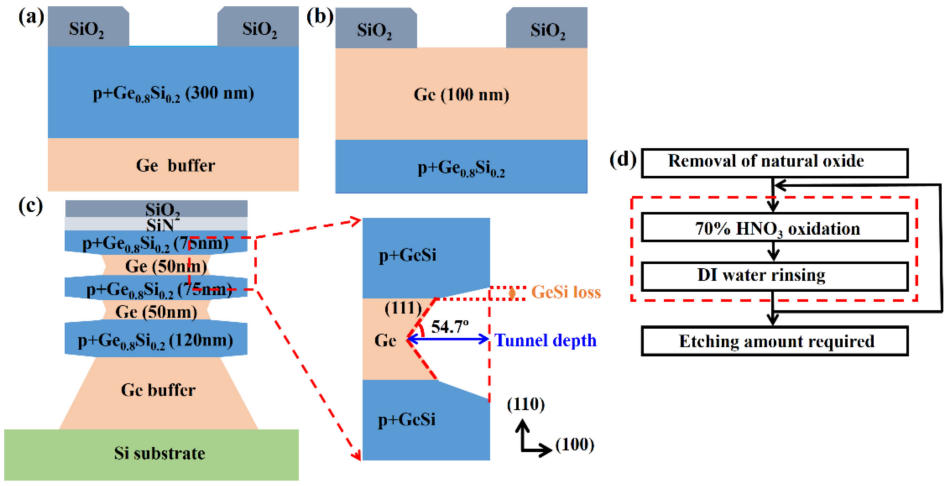

Figure 2. (**a**) Scheme of structure for p^+-$Ge_{0.8}Si_{0.2}$ (**a**) and Ge (**b**) with (100) flat surface; (**c**) scheme of p^+-$Ge_{0.8}Si_{0.2}$/Ge stacks with SiO_2 and SiN as hard mask. The tunnel depth and GeSi loss are indicated in the insert view, selective etching of Ge at (111) planes result in a lateral angle of 54.7°. (**d**) Flow diagram of HNO_3-DI water for p^+-$Ge_{0.8}Si_{0.2}$-selective etching of Ge with ALE.

Scanning electron microscopy (SEM) was used to examine the morphology and etching depth of the samples. Transmission electron microscopy (TEM) characterized the sample to determine the layer profile and evaluate the results of wet etching. Energy dispersive spectroscopy (EDS) was employed to determine the elemental analysis of the etched layers. High-resolution X-ray diffraction (HRXRD) was used to measure the strain relaxation and examine the epitaxial quality. Atomic force microscopy (AFM) measured surface roughness.

3. Results and Discussion

3.1. Dual-Selective Etching Ge to p$^+$-$Ge_{0.8}Si_{0.2}$ with ALE

In order to form Ge channels with self-aligned gate structure in pVSAFETs, Ge was required to be laterally released to nano-scale size with ALE. First, we tried the ALE recipe of selective SiGe to Si in the previous work [28,29], using H_2O_2 and diluted HNO_3 solution as oxidants to oxidize p$^+$-$Ge_{0.8}Si_{0.2}$/Ge stacks. However, due to the water-soluble of GeO_2, GeO_2 generated by the reaction of Ge with H_2O_2 and diluted HNO_3 solution was dissolved in water immediately, resulting in uncontrolled continuous etching [20], these recipes cannot be used as ALE recipes for Ge. Then, we used O_2 plasma and O_3 as oxidants, combined with the etchant for Ge selective etching experiments, but failed with non-selectivity (not shown). Finally, we found that (1) only a high concentration of HNO_3 (70% with 5% variation) as oxidant and DI water as etchant can achieve the selective ALE of Ge to p$^+$-$Ge_{0.8}Si_{0.2}$, and (2) 70% concentrated HNO_3 has crystal-orientation selectivity for the oxidation of Ge, but not for p$^+$-$Ge_{0.8}Si_{0.2}$. The oxidation rate of HNO_3 on Ge surface is inversely proportional to the atomic density of the crystallographic plane, which determines the slower oxidation rate on Ge (111) planes [33,34]. Therefore, the self-saturated selective etching of Ge at (111) planes result in a lateral angle of 54.7°, as shown in the insert view of Figure 3a. Within the experimental error, this angle is equal to the theoretical angle between the (100) and (111) set of planes. A developed dual-selective ALE method, including material selectivity and crystal-orientation selective oxidation, is suitable for the selective etching of Ge in p$^+$-$Ge_{0.8}Si_{0.2}$/Ge stacks.

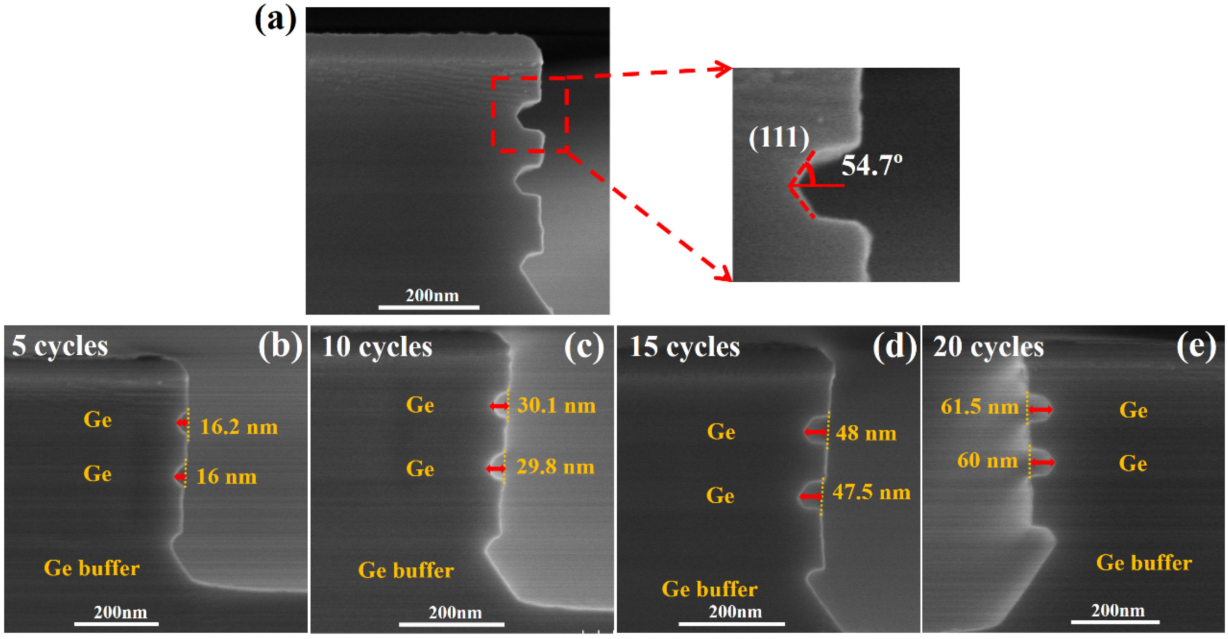

Figure 3. (**a**) The dual-selective etch of Ge at (111) planes result in a lateral angle of 54.7°. The SEM cross-section images of p$^+$-$Ge_{0.8}Si_{0.2}$/Ge multilayers after 70% HNO_3-DI water ALE at (**b**) 5 cycles, (**c**) 10 cycles, (**d**) 15 cycles, and (**e**) 20 cycles. (Oxidation time t_{ox} = 30 s; temperature of HNO_3 = 20 °C).

Due to the ALE separated into two parts: oxidation and oxide remover. The amount of etching is determined according to the amount of oxidation, so the oxidation step is

the key to control the etching rate. First, 70% HNO_3 was used to periodically oxidize the surface of the sample for time t_{ox}, showing a self-limiting surface passivation reaction, and then deionized (DI) water was used to directly remove the oxide. The oxidation of Ge in high-concentration nitric acid can be described as follows [20]:

$$Ge + 4HNO_3 \rightarrow GeO_2 \cdot H_2O + 4NO_2 \uparrow + H_2O \quad (1)$$

In the reaction of high-concentration nitric acid to germanium, the reaction product is $GeO_2 \cdot H_2O$. In the whole reaction process, GeO_2 formed at the germanium-liquid interface diffuses slowly, and enough GeO_2 covers the entire germanium surface and produces passivation to prevent further corrosion of germanium [35]. Compared with ALE of SiGe to Si, the ALE of Ge to p^+-$Ge_{0.8}Si_{0.2}$ did not need another etchant (hydrofluoric acid or dBOE) but only DI water can directly remove oxides. To ensure the stability of the nitric acid concentration during the ALE experiment, the nitric acid concentration needs to be monitored with a high-precision density meter every 5 min. It was found that the concentration of HNO_3 changes by 5% within 1 h during the ALE experiment. When the nitric acid concentration changed more than 5%, that is, the nitric acid concentration is less than 65% (original nitric acid concentration is 70%), the p^+-$Ge_{0.8}Si_{0.2}$/Ge stacks became continuous etching in HNO_3 solution. In order to maintain the stability and repeatability of the ALE experiment, the nitric acid solution was changed every 1 h. It can be seen that the concentration of nitric acid had a great influence on the experimental results. Since nitric acid is exothermic and volatilized when exposed to water, the sample must be dried before the next cycle in nitric acid. In order to verify whether germanium oxide is completely removed in DI water, three comparative experiments were taken at the same time: (1) 70% HNO_3 30 s + DI water cleaning for 1 min, (2) 70% HNO_3 30 s + DI water cleaning for 2 min and (3) 70% HNO_3 30 s + DI water cleaning for 1 min + dBOE immersing for 1 min + DI water cleaning for 1 min. Excluding measurement errors, the Ge etching amounts of these three cleaning conditions were almost the same (not shown), which proved that 1 min of DI water cleaning was sufficient to remove germanium oxide without adding other etching agents. It was also proved that enough water molecules in DI water can pass through GeO_2 to reach the Ge-GeO_2 interface and strip the germanium oxide.

Samples were immersed in concentrated HNO_3 (70%) with oxidation time t_{ox} = 30 s at HNO_3 temperature of 20 °C, and rinsed in DI water for at least 1 min to remove GeO_x effectively. Figure 3b–e shows the SEM cross-section images of p^+-$Ge_{0.8}Si_{0.2}$/Ge stacks after etching with 5 cycles, 10 cycles, 15 cycles, and 20 cycles, respectively. Within the measurement error, the mean relative etching amounts of Ge in p^+-$Ge_{0.8}Si_{0.2}$/Ge stacks were 16.1 nm, 30 nm, 47.8 nm, and 60.8 nm, respectively. The relative etching amount is linearly proportional to the number of etching cycles, and the etch rate per cycle (EPC) is independent of the etching cycle number with the mean value of 3.1 nm.

In p^+-$Ge_{0.8}Si_{0.2}$/Ge stacks, the selective ALE of Ge can be performed smoothly in a 70% HNO_3-DI water system. One is that the Ge layers (atoms) were oxidized preferentially by HNO_3 owing to the weaker Ge-Ge bond energy than those of Ge-Si and Si-Si [36–39]. Second, GeO_2 generated in the Ge layer is soluble in water, while SiO_2 generated by oxidation of the p^+-$Ge_{0.8}Si_{0.2}$ layer is stable and hydrophobic, and GeO_2 far away from the surface cannot be directly dissolved in water because of the passivation of the SiO_2 layer.

The EPC was calculated by dividing the relative etching amounts by the number of etching cycles and this experiment was carried out at HNO_3 temperature of 20 °C. The EPC for Ge and p^+-$Ge_{0.8}Si_{0.2}$ as a function of the oxidation time is shown in Figure 4. The EPC increased with the increase of oxidation time and gradually saturates when the oxidation time exceeds 30 s, indicating that the oxidation of Ge and p^+-$Ge_{0.8}Si_{0.2}$ in concentrated HNO_3 (70%) is quasi-self-limiting. When the oxidation time is 30 s, the etching selectivity between Ge and p^+-$Ge_{0.8}Si_{0.2}$ in (100) flat surface is 6.5, as determined from the two oxidation curves in Figure 4. The EPC of Ge and p^+-$Ge_{0.8}Si_{0.2}$ were 3.7 nm and 0.5 nm, respectively. The etch rate of lateral selective etching of Ge on p^+-$Ge_{0.8}Si_{0.2}$/Ge stacks with (110) sidewall, which is more important in vertical device fabrication, is defined as the

relative etched amount per cycle (REPC). Similarly, as shown in Figure 4, the REPC of Ge in the vertical structure of p^+-$Ge_{0.8}Si_{0.2}$/Ge stacks is fixed at ~3.1 nm. The estimated data in these experiments in Figure 4 show very small etching errors. Therefore, it can be verified that the ALE method is repeatable if the measurement error is taken out.

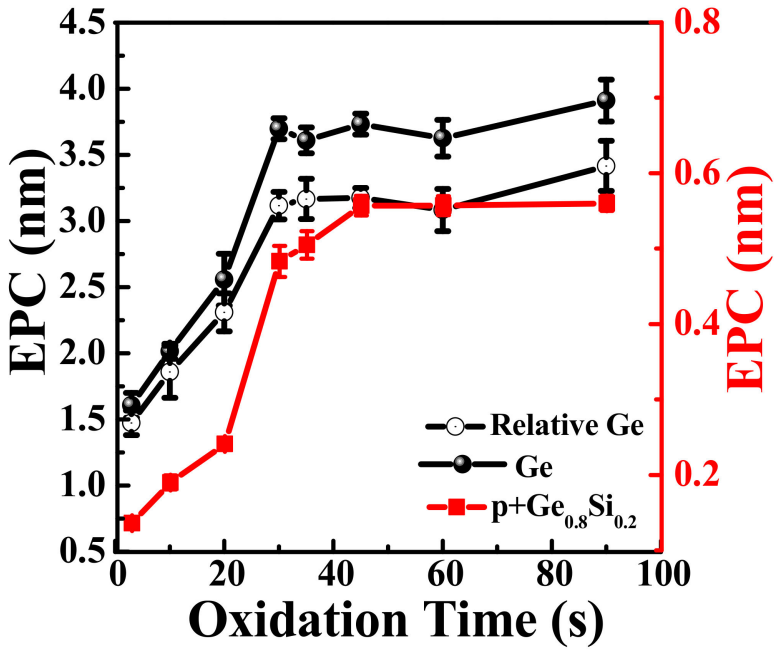

Figure 4. EPCs of ALE with different oxidation time for Ge and p^+-$Ge_{0.8}Si_{0.2}$ (100) planes and Ge selectively etched in p^+-$Ge_{0.8}Si_{0.2}$/Ge stacks. (30 cycles; Temperature of HNO_3 = 20 °C; Experimental data of average values and error bars are shown in the graph).

3.2. Effect of HNO_3 Temperature on Ge ALE

At room temperature (20 °C), the REPC of Ge (3.1 nm) is about 8 times higher than that of REPC of SiGe (0.4 nm) [29]. The etching rate is relatively fast. Since oxidation plays an important role in ALE, the effect of lowering the temperature of the nitric acid solution on the oxidation rate was studied to obtain a lower oxidation rate. Due to the strong corrosiveness of nitric acid, the temperature of the nitric acid solution is cooled by the water bath of the cryostat. In order to explore the effect of low-temperature on the REPC and selectivity between Ge and p^+-$Ge_{0.8}Si_{0.2}$, experiments were carried out at HNO_3 temperature of 5 °C, 10 °C, 15 °C, and 20 °C, respectively. The low-temperature etching morphology was characterized by SEM and TEM. As shown in Figure 5, Ge ALE at 20 °C and 5 °C both exhibit dual-selectivity (material and crystal-orientation selectivity). The TEM results show the clear layering of the p^+-$Ge_{0.8}Si_{0.2}$/Ge stacks and the etching morphology corresponding to the SEM characterization. The oxidation time was t_{ox} = 30 s, where the cycles of 20 °C and 5 °C were 15 cycles and 20 cycles, respectively, and the etching amount of Ge is 50 nm and 36 nm, respectively. Experiments have proved that low temperature can reduce the oxidation rate of nitric acid without changing the etching morphology, which is an effective method to reduce REPC of Ge.

The REPC curves of ALE at different HNO_3 temperatures (20 °C, 15 °C, 10 °C, and 5 °C) in p^+-$Ge_{0.8}Si_{0.2}$/Ge multilayers are shown in Figure 6a. As the temperature of HNO_3 decreased from 20 °C to 5 °C, REPC decreased from 3.1 nm to 1.8 nm. With the HNO_3 temperature reducing to 10 °C, the REPC of Ge was reduced to 2 nm. Similarly, the REPCs at all four temperatures reached saturation when the oxidation time exceeded 30 s, which is the quasi-self-limiting process. Due to the temperature sensitivity of the Ge oxidation reaction, the saturated oxide will be thinner with the lower HNO_3 temperature. The temperature with variation ±0.5 °C was controlled by the water bath of the low-constant temp tank. According to the corrosion model proposed by Seidei [40], its point of view was

to attribute chemical reactions to differences in energy. When the temperature of the HNO_3 decreased, the energy difference between its molecular kinetic energy and the surface activation energy of the sample became smaller, so the oxidation rate became slower.

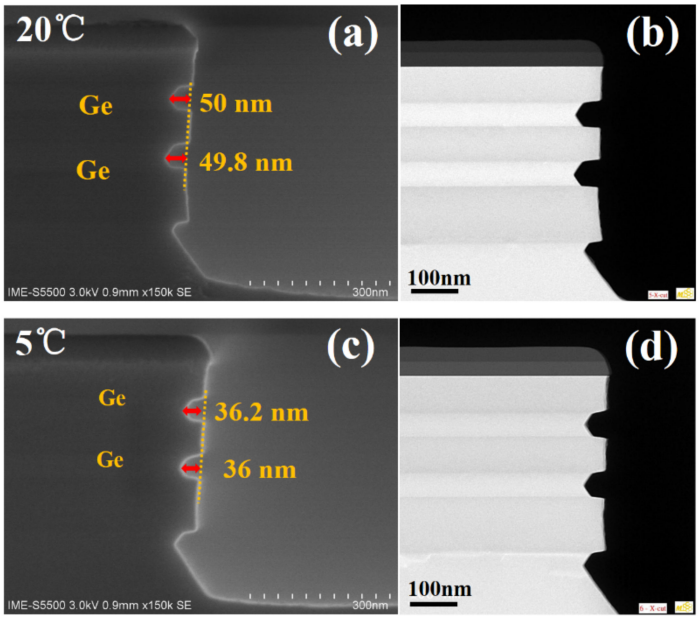

Figure 5. The SEM and TEM images of etching profile of p^+-$Ge_{0.8}Si_{0.2}$/Ge multilayers after ALE at (**a**,**b**) 15 cycles (temperature of HNO_3 = 20 °C); (**c**,**d**) 20 cycles (temperature of HNO_3 = 5 °C). The oxidation time t_{ox} = 30 s.

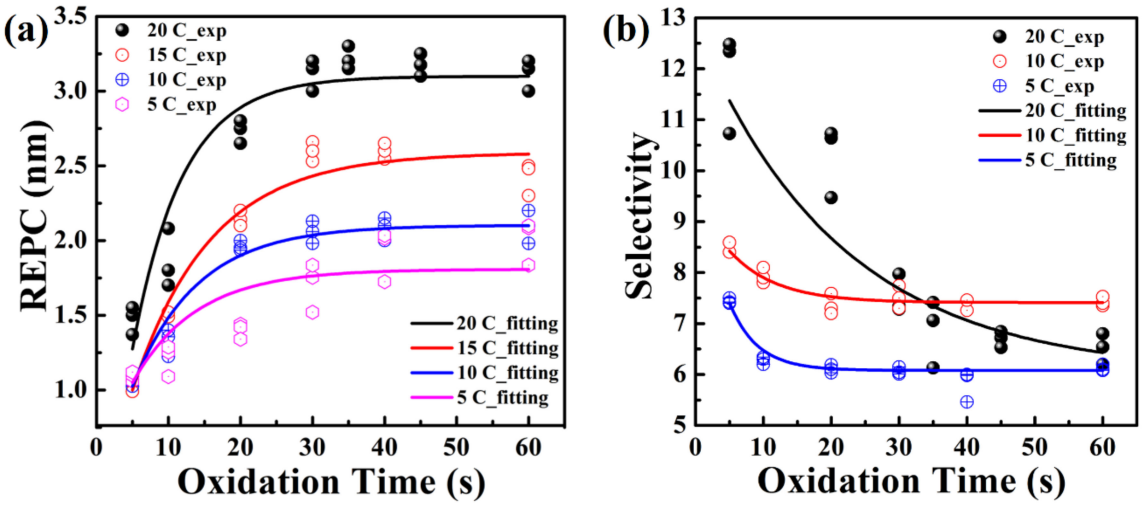

Figure 6. (**a**) The REPC of p^+-$Ge_{0.8}Si_{0.2}$/Ge at different HNO_3 temperatures (20 °C, 15 °C, 10 °C, 5 °C) as a function of oxidation time. (**b**) The selectivity between p^+-$Ge_{0.8}Si_{0.2}$ and Ge at different HNO_3 temperatures (20 °C, 10 °C, and 5 °C) as a function of oxidation time. The scatters and solid lines represent the experimental data and fitting curves of the experimental data.

Figure 6b shows the etching selectivity of p^+-$Ge_{0.8}Si_{0.2}$/Ge stacks at different HNO_3 temperatures (5 °C, 10 °C, and 20 °C). The selectivity is defined as [28]:

$$\text{Selectivity} = \frac{\text{GeSiloss} + \text{Tuneldepth}}{\text{GeSiloss}} \quad (2)$$

where GeSi loss is vertical etching amount of GeSi, which is equal to the horizontal etching amount, and the tunnel depth is the relative total etched amount of Ge to $Ge_{0.8}Si_{0.2}$, as

shown in Figure 2c. The experimental data were obtained by measuring the SEM images of the etching profile in the p^+-$Ge_{0.8}Si_{0.2}$/Ge stacks with (110) sidewalls. The mean values of p^+-$Ge_{0.8}Si_{0.2}$/Ge selectivity at HNO_3 temperatures of 20 °C, 10 °C, and 5 °C were 6.5, 7.4, and 6.1, respectively. The results show that Ge ALE can achieve a high selectivity of Ge to $Ge_{0.8}Si_{0.2}$, independent of HNO_3 temperature. At HNO_3 temperatures of 20 °C, when the oxidation time increased, there was enough time for HNO_3 to destroy and oxidize the Si-Si bonds and Ge-Si bonds. After 30 cycles of ALE, the etching amount of $Ge_{0.8}Si_{0.2}$ became larger, and the EPC became larger accordingly. Thereby reducing the selectivity of Ge to $Ge_{0.8}Si_{0.2}$, and reached saturation when the oxidation time was 45 s. At low temperatures, due to the decrease of the molecular kinetic energy of HNO_3, the selectivity of Ge to $Ge_{0.8}Si_{0.2}$ does not change much with time and reached saturation in about 20 s of oxidation time.

3.3. Structure Characterization and Material Quality Analysis

In order to more accurately characterize the Ge ALE results in this study, the quality of the epitaxial layers and the etching morphology and element analysis of the p^+-$Ge_{0.8}Si_{0.2}$/Ge stack structure were characterized by HRTEM and EDS. Figure 7 shows the cross-section TEM micrograph and elemental analysis of the etched area of p^+-$Ge_{0.8}Si_{0.2}$/Ge stacks with (110) sidewalls with Ge ALE. The results show that the Ge content in the GeSi layer maintains at 80%, and there is no mixing between the layers. The relative etching amount is the same as that characterized by SEM. It was further verified that the selective etching of Ge on (111) planes resulted in a lateral angle of 54.7°. The EDS mapping of Figure 8 shows that the boundaries of the layers are obvious, the thickness of the film is consistent with the design, and there is no obvious element diffusion between the layers. The germanium content of the Ge layer is almost 100%. Si element is distributed in the layers of SiO_2, SIN, and $Ge_{0.8}Si_{0.2}$, O mainly exists in the hard mask of SiO_2.

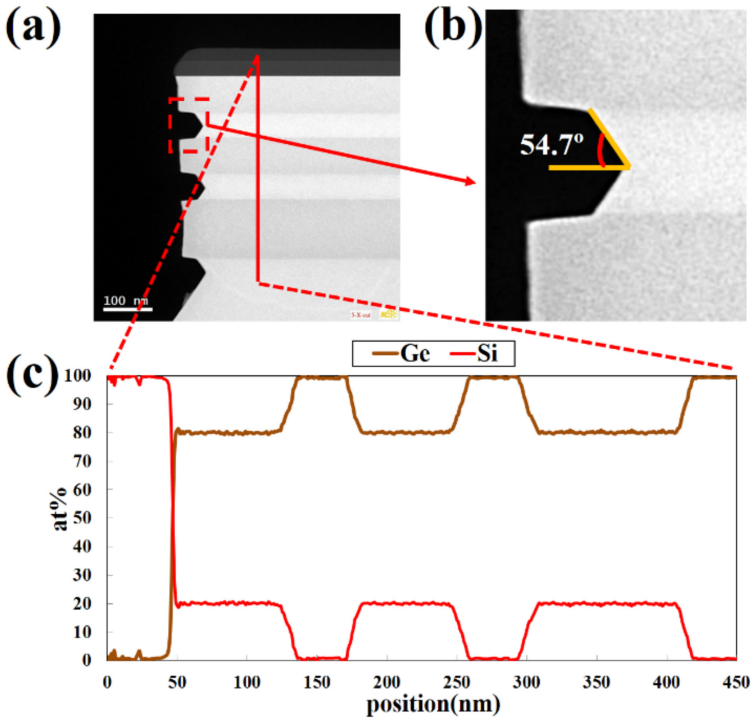

Figure 7. (**a**,**b**) TEM images of etching profile, and (**c**) EDS analysis with line scanning of Si and Ge in vertical orientation of the Ge buffer/p^+-$Ge_{0.8}Si_{0.2}$/Ge stack structure. The selective etching of Ge at (111) planes results in a lateral angle of 54.7°. (20 cycles; temperature of HNO_3 = 15 °C; oxidation time t_{ox} = 30 s).

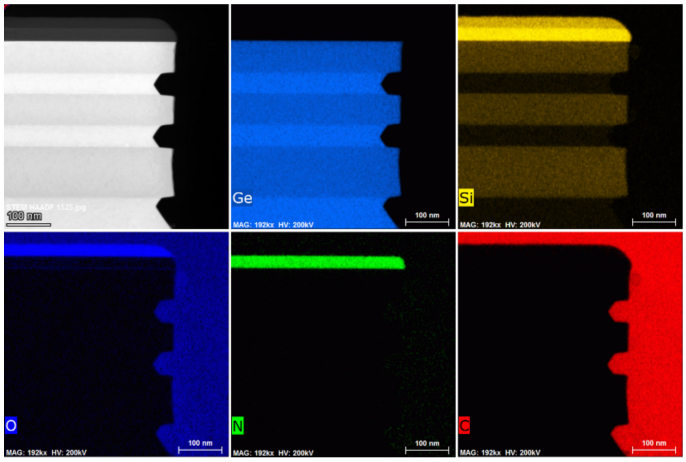

Figure 8. EDS mapping near etching regions with elements Ge, Si, O, N, and C, the sample etching for 15 cycles (oxidation time t_{ox} = 30 s; temperature of HNO_3 = 20 °C).

Crystallinity and strain have a strong impact on channel carrier mobility and device performance, therefore, crystal quality and strain relaxation of the sample before and after the etching steps has been studied. HRXRD is a technique that is widely used for the detection of defects in crystal materials [41]. Figure 9 displays rocking curves (RCs) measured around the (004) reflection on stack samples: as-grown, after vertical stack etch, after ALE at 20 °C, and after ALE at 10 °C. For the as-grown sample, the $Ge_{0.8}Si_{0.2}$ and Ge peaks were intense with low Full-width-of-half-Maximum (FWHM) showing good crystalline quality of $Ge_{0.8}Si_{0.2}$/Ge stack. Since most of the film layer was removed by etching, the intensity of the $Ge_{0.8}Si_{0.2}$ peak was weaker, while the Ge peak was still strong due to the presence of the Ge buffer layer. Compared with the as-grown sample, the $Ge_{0.8}Si_{0.2}$ peak shifts towards the Ge peak after stack etching. This indicates that (tensile-strained) $Ge_{0.8}Si_{0.2}$ is partially relaxed after the vertical etching. Moreover, the Ge peak became asymmetric after vertical etch and the amount of strain in the Ge was minor. No further shift of $Ge_{0.8}Si_{0.2}$ or Ge peak was detected after ALE etching, which indicates that there was no further strain relaxation after lateral etching at 20 °C and 10 °C.

Since Ge will be used as the channel material in vertical GAAFETs, the etched germanium surface can be used as the channel interface. Due to the scattering of the surface roughness, the channel surface roughness will cause gate oxide integrity degradation and mobility degradation. Therefore, it is necessary to measure the surface roughness of Ge that has been etched many times by DI water. Figure 10 shows the AFM images of the flat (100) Ge surface with as-grown epi-Ge, after etching with ALE at HNO_3 temperatures of 20 °C (20 cycles), after etching with ALE at HNO_3 temperatures of 5 °C (20 cycles), and after etching with HF:HNO_3:CH_3COOH mixtures. It was found that the root mean square (RMS) roughness of the ALE process at 20 °C HNO_3 temperatures is 0.85 nm, which is similar to that of the as-grown sample (RMS of 0.67 nm). However, the RMS increases as the temperature of HNO_3 decreases. The roughness is very poor etching with HF:HNO_3:CH_3COOH mixtures. Table 1 shows the comparison of the RMS of flat (100) Ge surfaces of as-grown and different etching processes. It is demonstrated that the surface roughness of ALE is better than chemical continuous etching. The smoothing effect can be explained by a model, where the depressions on the surface asperity are preferentially oxidized, and the protrusions on the asperity are preferentially etched. When the temperature of nitric acid decreases, the oxidizing ability decreases, resulting in uneven surface oxidation. Finally, the height difference between the depressions and the protrusions was increased during the etching, so the surface after the low-temperature treatment is rougher. In summary, we need to make a trade-off between the etching rate and the surface roughness and choose a suitable temperature for ALE etching. Because of the equipment, the preparation process of our devices was mainly carried out at room temperature.

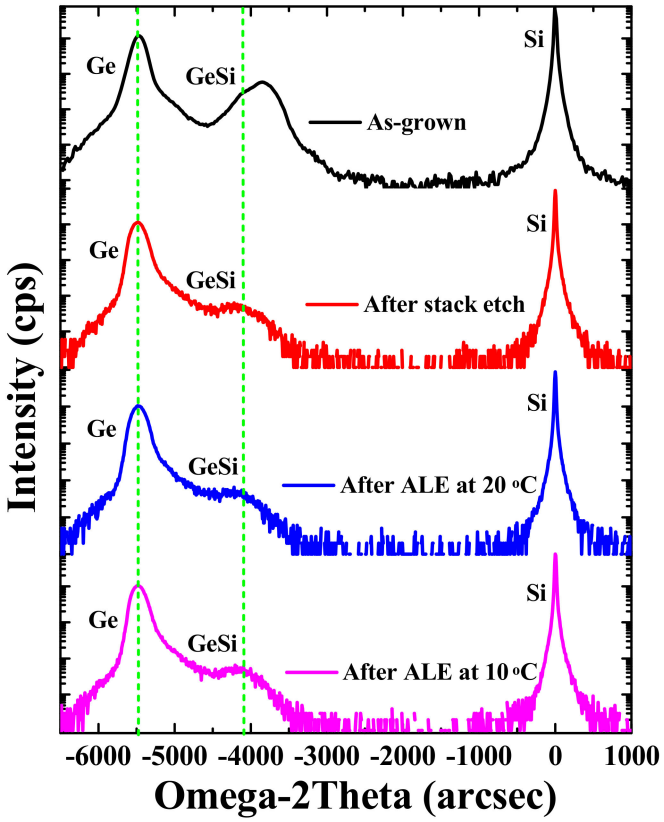

Figure 9. HRXRD rocking curves (RCs) around (004) reflection of stack samples of as-grown, after vertical stack etch, after ALE at 20 °C, and after ALE at 10 °C with 20 cycles.

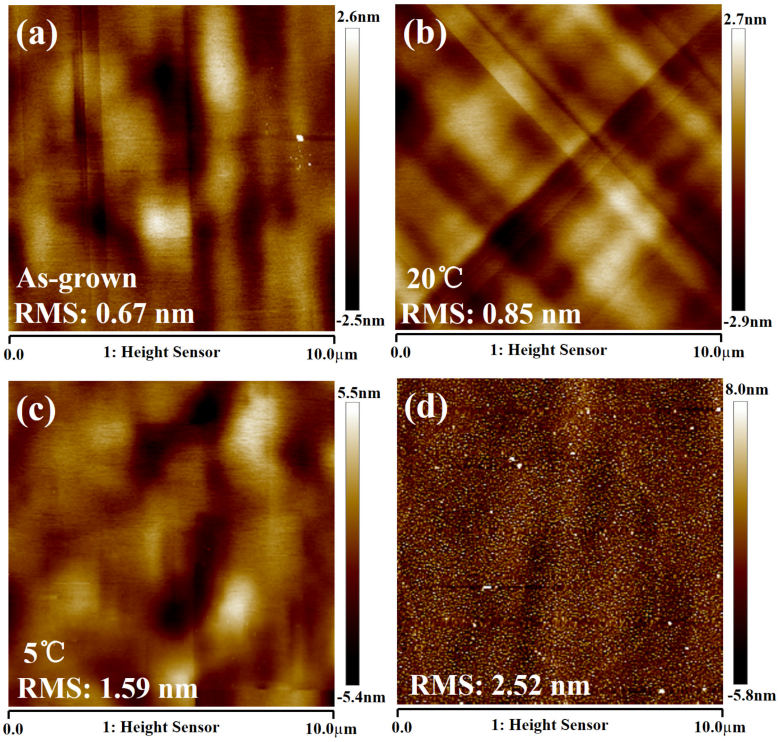

Figure 10. Typical AFM images (10 × 10 μm^2) of flat (100) Ge surfaces before and after the etching process: (**a**) as–grown; (**b**) ALE with 20 cycles (temperature of HNO_3 = 20 °C); (**c**) ALE with 20 cycles (temperature of HNO_3 = 5 °C); (**d**) HF:HNO_3:CH_3COOH mixtures.

Table 1. RMS of flat (100) Ge surfaces with as-grown film and different etching processes.

	As-Grown	20 °C ALE	15 °C ALE	10 °C ALE	5 °C ALE	HF:HNO_3:CH_3COOH
RMS (nm)	0.67	0.85	1.12	1.39	1.59	2.52

3.4. Application of ALE for Ge Vertical Sandwich GAAFETs (VSAFETs)

The ALE of Ge selective to p^+-$Ge_{0.8}Si_{0.2}$ will be adopted in the vertical sandwich GAAFETs (VSAFETs) to form Ge channel nanowire, as mentioned in the introduction. The cross-sectional SEM images of the p^+-$Ge_{0.8}Si_{0.2}$/Ge/p^+-$Ge_{0.8}Si_{0.2}$ sandwich structure forming vertical nanowire are shown in Figure 11a,b. Figure 11a,b respectively show a 40 nm Ge channel with 15 cycles of ALE and a 15 nm Ge channel with 20 cycles of ALE, implying the well-controlled Ge channel size with ALE. Figure 11c,d show the TEM top view for NS with perimeter 185 nm and NW with perimeter 143 nm formed by 30 cycles of ALE, respectively. The TEM top views were cut at the top drain, the brighter part is the channel, and the black part is metal. The vertical nanosheet (NS) and nanowire (NW) shown in Figure 11c,d were obtained on the same wafer, and the channel size and shape are determined by initial dimensions (defined by electron-beam lithography) and the dual-selective ALE.

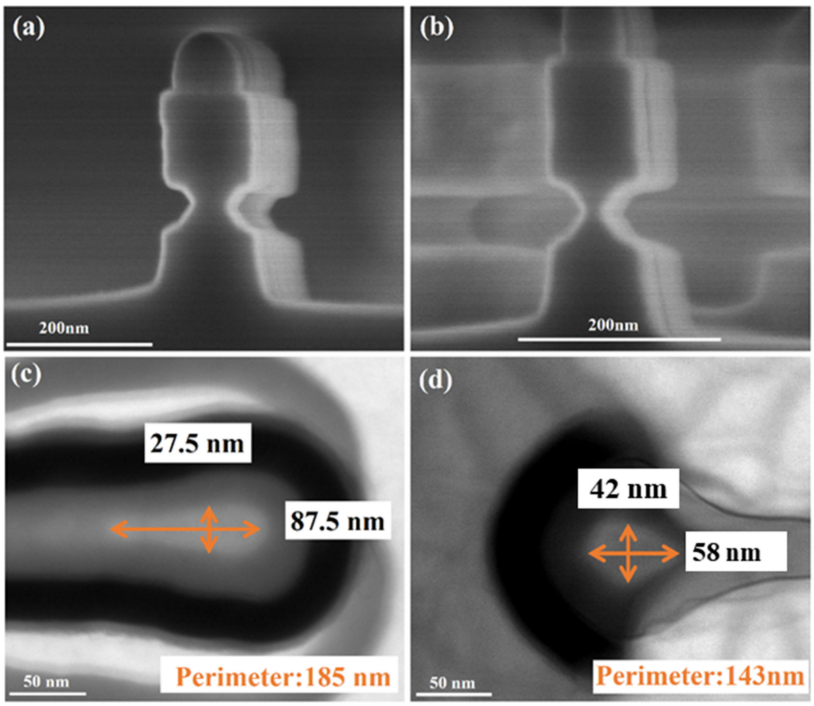

Figure 11. Cross-sectional SEM images of Ge selective etching with ALE, (**a**) 40 nm Ge channel with 15 cycles of ALE, and (**b**) 15 nm Ge channel with 20 cycles of ALE. Cross-sectional TEM top views of Ge VSAFETs: (**c**) NS with perimeter 185 nm, (**d**) NW with a square cross-section with perimeter 143 nm. Oxidation time t_{ox} = 30 s and temperature of HNO_3 = 20 °C.

Figure 12a,b show the cross-sectional SEM and TEM images of the filled high-k metal gate (HKMG) of the gate gap formed by selective etching of the channel with ALE, respectively. Figure 12c shows the TEM image of the gate stack on the side-wall of the hourglass-shaped Ge channel. As shown in Figure 12d–f, the EDX mapping of elements Ge, Si, and W shows sharp contours, proving the absence of element intermixing. The self-saturated dual-selective etch of Ge at (111) planes result in an hourglass-shape with a lateral angle of 54.7°. The current transports along the (111) planes of the hourglass-shaped Ge channel.

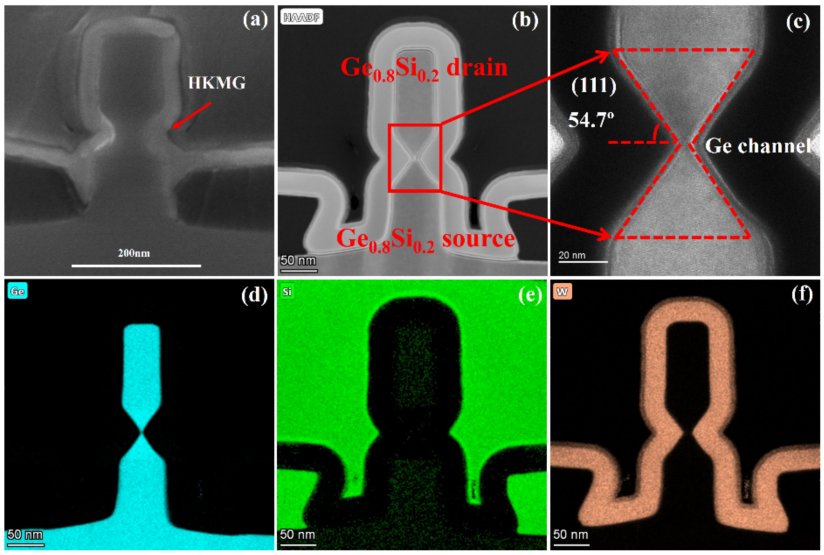

Figure 12. (**a**) SEM and (**b**) TEM images of Ge pVSAFET with gate gaps filling high-k metal gate (HKMG). (**c**) The self-saturated dual-selective etch of Ge at (111) planes result in an hourglass shape with a lateral angle of 54.7°. Energy-dispersive Xray spectroscopy (EDX) mapping of (**d**) Ge (cyan), (**e**) Si (cyan), and (**f**) W (yellow) atoms with sharp contours.

In this stage, a vertical sandwich GAAFET (VSAFET) was processed by ALE method when a Ge nanosheet (NS) with thickness of ~27.5 nm was the channel material as shown in Figure 11c. The process flow of the transistor includes sandwich structure growth, lithographic patterning and plasma anisotropic etching, channel selective etching to form channels, and filling of the high-k metal gate (HKMG) by ALD [14]. Figure 13 illustrates the I_d–V_{ds} output characteristic curve when the I_{on} is 141 μA/um (I_d@V_{ov} = V_{gs} − V_t = −0.6 V, V_{ds} = −1.0 V). It is important to emphasize that these results are preliminary for Ge pVSAFETs, and the device performance will be further studied in the future.

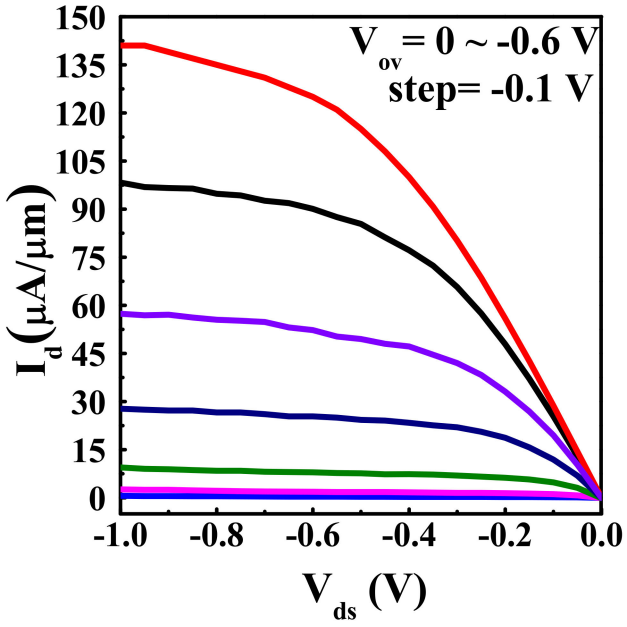

Figure 13. I_d–V_{ds} output characteristic curves for Ge pVSAFET with NS thickness of ~27.5 nm, V_{ov} from 0 to −0.6 V, showing characteristic current saturation behavior. I_d normalizes with the perimeter of NS.

4. Conclusions

In this work, a developed wet dual-selective ALE process with selective etching of Ge and crystal-orientation selectivity of Ge oxidation was proposed. With the oxidation–removal reaction of 70% HNO_3 and deionized (DI) water, the characteristics of $Ge_{0.8}Si_{0.2}$-selective ALE of Ge at different HNO_3 temperatures were investigated systematically. In p^+-$Ge_{0.8}Si_{0.2}$/Ge stacks with (110) sidewalls, the saturated relative etched amount per cycle (REPC) of Ge was 3.1 nm and the saturated etching selectivity was 6.5 at an HNO_3 temperature of 20 °C. The etch rate and the selectivity were affected by HNO_3 temperatures. As the HNO_3 temperature decreased to 10 °C, the REPC of Ge was decreased to 2 nm and the selectivity remained at about 7.4. The Ge channel size in the VSAFETs was well-controlled by ALE. The hourglass-shaped channel of the VSAFETs is formed by the dual-selective ALE of Ge, narrow in the middle and wide close to S/D. Finally, the preliminary I_d–V_{ds} output characteristic curve of Ge pVSAFET was demonstrated.

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Conflicts of Interest: The authors declare no conflict of interest.

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The Effect of Doping on the Digital Etching of Silicon-Selective Silicon–Germanium Using Nitric Acids

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Abstract: Gate-all-around (GAA) field-effect transistors have been proposed as one of the most important developments for CMOS logic devices at the 3 nm technology node and beyond. Isotropic etching of silicon–germanium (SiGe) for the definition of nano-scale channels in vertical GAA CMOS and tunneling FETs has attracted more and more attention. In this work, the effect of doping on the digital etching of Si-selective SiGe with alternative nitric acids (HNO_3) and buffered oxide etching (BOE) was investigated in detail. It was found that the HNO_3 digital etching of SiGe was selective to n^+-Si, p^+-Si, and intrinsic Si. Extensive studies were performed. It turned out that the selectivity of SiGe/Si was dependent on the doped types of silicon and the HNO_3 concentration. As a result, at 31.5% HNO_3 concentration, the relative etched amount per cycle (REPC) and the etching selectivity of $Si_{0.72}Ge_{0.28}$ for n^+-Si was identical to that for p^+-Si. This is particularly important for applications of vertical GAA CMOS and tunneling FETs, which have to expose both the n^+ and p^+ sources/drains at the same time. In addition, the values of the REPC and selectivity were obtained. A controllable etching rate and atomically smooth surface could be achieved, which enhanced carrier mobility.

Keywords: vertical gate-all-around (vGAA); digital etch; quasi-atomic-layer etching (q-ALE); selective wet etching; HNO_3 concentration; doping effect

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1. Introduction

Gate-all-around (GAA) nanowire transistors are ideal candidates for various CMOS applications due to their outstanding gate control, excellent performance, immunity to short-channel effects, and scalability [1–3]. Tunneling field-effect transistors (TFETs) have arisen as promising devices with emerging device concepts by breaking through the subthreshold swing limit of 60 mV/dec for low-power applications [4–6]. GAA nanowire TFETs have become candidates for substitutes for conventional MOS technology, especially in terms of their energy efficiency and scaling due to the better electrostatic control of the tunneling carriers provided by their nanowire structure [7–10]. SiGe channel materials have been introduced due to their excellent bandgap, high mobility, high density of states, and high compatibility with existing CMOS technology [11,12]. In order to precisely define the nanowire diameter and effective gate length, SiGe materials need to be selectively etched with accurate etching depth control and high selectivity for both n^+-Si and p^+-Si for

CMOS and TFET applications, which have to expose both the n^+ and p^+ sources/drains at the same time.

Several techniques have been proposed for selective etching of SiGe, such as mixtures of HNO_3, HF, and H_2O [13–15], as well as solutions of H_2O_2, HF, and CH_3COOH [16,17]. Unfortunately, the wet etching of mixtures is not appropriate for small-sized features due to the high etching rate [18,19]. Vapor etching using gaseous HCl in a chemical vapor deposition (CVD) reactor is also limited because of its high-temperature process, which degrades the sharpness of the junction [20]. Moreover, dry etching using CF_4-based plasma has been extensively researched [21–23]. The disadvantage is that the plasma equipment is more complex and the loading effect is serious [24]. The etching techniques mentioned above involve continuous etching that is controlled by the etching time. Therefore, they do not meet the requirements of nano-scale transistors for process control. Atomic-layer etching (ALE) draws has significantly attracted researchers and the industrial community due to its self-limiting characteristics. The superiority of ALE techniques over other methods is due to the controllable etching rate and excellent variation control [25,26]. It has been employed for the etching of dielectrics [26,27], some nitrides [28], and metals [29,30]. Recently, an isotropic and quasi-ALE (q-ALE) method for Si-selective SiGe was proposed and reported by our group [31,32]. This q-ALE method is based on a cyclic oxidation–etching process in which hydrogen peroxide (H_2O_2) [32] or nitric acid (HNO_3) [31] and buffered oxide etchants (BOEs) are separately used as an oxidant and an oxide remover agent, which is also called digital etching. The experimental etching rate of about 5 A (approximately four monolayers) per cycle accounted for the quasi-self-limited behavior in our q-ALE process [31,32]. This was explained and understood from the perspective of the activation energy, which was extracted by fitting the experimental data with the proposed oxidation model [31]. The works mentioned above mainly focused on the digital etching characteristics of SiGe that is selective of p-type doped Si. However, the digital etching of SiGe that is selective of n-type doped Si and intrinsic Si has not been studied.

In this work, the effect of doping on digital wet etching of SiGe that is selective of Si was investigated systematically. The digital etching was based on a combination of HNO_3 and buffered oxide etchants (BOEs) as an oxidant and an oxide remover agent, respectively. The selectivity characteristics of SiGe for n^+-Si were demonstrated. The effects of different parameters on the selectivity of the etching of germanium–silicon, such as for Si doping, HNO_3 concentration, and SiGe doping, were examined and discussed in detail.

2. Materials and Methods

The substrates were 8 inch p-type Si (100) wafers with a resistivity of 8–12 ohm·cm. The p^+-Si/SiGe/n^+-Si stack layers were grown in an ASM E2000 plus RPCVD reactor (ASM, Munich, Germany). First, after a standard pre-epitaxial cleaning, the wafers were baked at 900 °C in ambient H_2 with a pressure of 20 Torr for 5 min, achieving a pure and smooth silicon surface [32]. Then, the p^+-Si/SiGe/n^+-Si stack layers and p^+-Si/SiGe/i-Si stack layers were grown at 650 °C using an adjusted gas source with H_2 as a carrier gas. Dichlorosilane (SiH_2Cl_2), germane (GeH_4), diborane (B_2H_6), and phosphine (PH_3) were utilized as gas precursors of Si, Ge, B, and P, respectively. The Ge incorporation, P concentration, and B concentration in silicon were achieved by tuning the gas flow and gas pressure. Finally, the epitaxial stack layers were fabricated. Then, a hard mask was deposited on the epitaxial stacked layers, and the pattern was formatted with an optical lithography with an I-line. The Si/SiGe stack layers were etched using hydrogen bromide (HBr)-based dry anisotropic etching. The details of the sample preparation can be found in [32]. Afterwards, the prepared samples were cut into same-sized slices of about 3×3 cm^2 to facilitate the etching experiments.

There were five kinds of Si/SiGe stack layer structures, as shown in Figure 1a–c. Sample I was a laminated structure in which ~300 nm p-type doped Si with a boron dopant concentration of 1.0×10^{20} cm^{-3}, 55 nm intrinsic $Si_{0.72}Ge_{0.28}$, and 120 nm n-type doped Si with a phosphorus dopant concentration of 1.7×10^{19} cm^{-3} were epitaxially grown

in sequence. Bottom p-type doped Si was etched to ~120 nm. The structural diagram is shown in Figure 1a. Sample II was a laminated structure in which ~300 nm p-type doped Si with a boron dopant concentration of 9×10^{19} cm^{-3}, 55 nm intrinsic $Si_{0.72}Ge_{0.28}$, and 120 nm intrinsic Si were grown in situ and in sequence. The structural diagram is shown in Figure 1b. In Sample III, arsenic (As) ion implantation with the energy of 30 keV and dose of 4×10^{15} cm^{-2} was performed on the top intrinsic Si, and then 900 °C spike annealing was carried out to activate arsenic in the top Si. The structural diagram is shown in Figure 1c. This sample was employed to demonstrate the digital etching characteristics of n-type doped Si with the implantation of As. Sample IV was a laminated structure with nine $Si_{0.72}Ge_{0.28}$ layers, as shown in Figure 1d. The n^+-SiGe layers with in situ phosphorus included SiGe layer 1, SiGe layer 2, and SiGe layer 3. The concentrations were 2×10^{19}, 1.3×10^{19}, and 2×10^{19} cm^{-3}, respectively. The intrinsic SiGe layers consisted of SiGe layer 4, SiGe layer 5, and SiGe layer 6. The p^+-SiGe layers with in situ boron included SiGe layer 7 and SiGe layer 8 with a concentration of 4×10^{19} cm^{-3}. SiGe layer 9 was doped with boron with a concentration of 4×10^{19} cm^{-3} and arsenic with a concentration of 4×10^{19} cm^{-3}. The thickness of the SiGe was ~35 nm. The thickness of the Si was ~50 nm. The sample was used for the investigation of the digital etching characteristics of doped SiGe. Sample V was a laminated structure with ~30 nm n^+-Si layers and ~35 nm n^+-SiGe layers with a varying Ge fraction; these layers were alternated, and the sample was used to examine the influence of the Ge mole fraction.

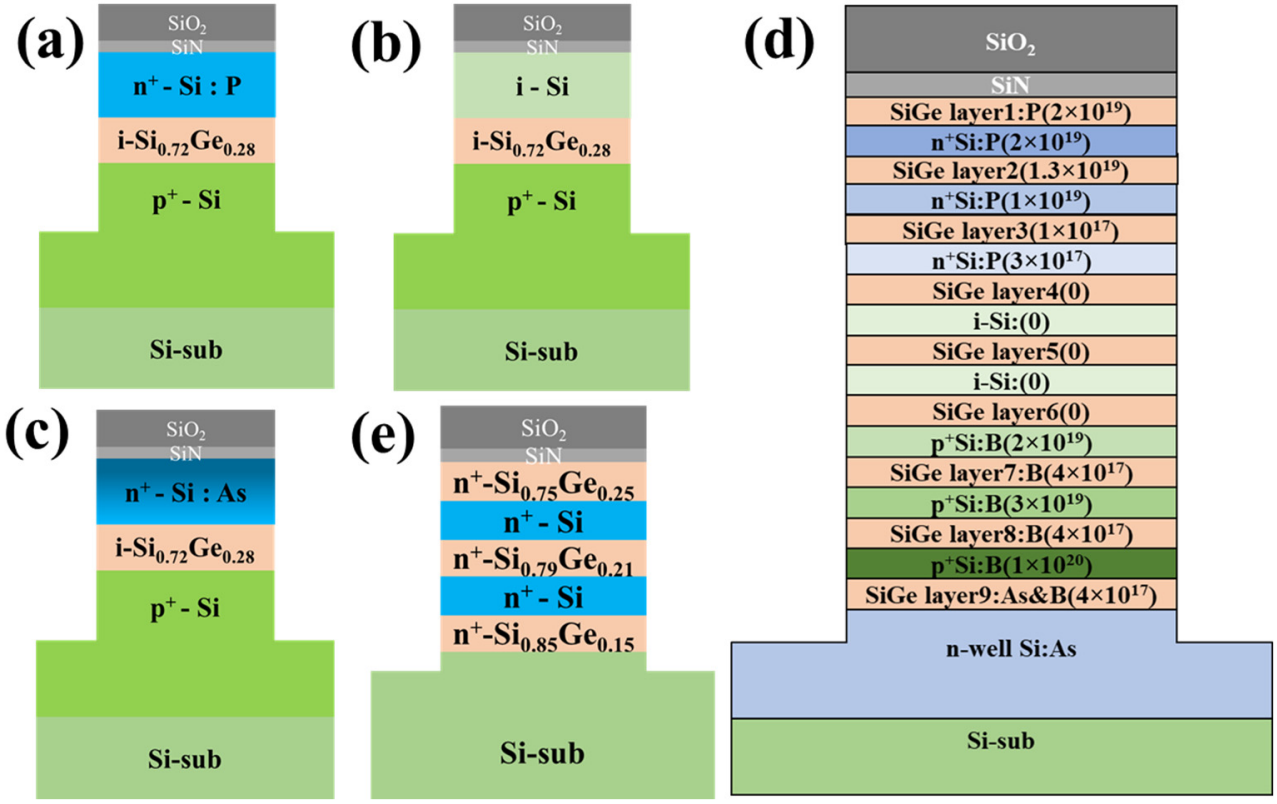

Figure 1. Scheme of the laminated structure with a lateral opening: (**a**) in situ n^+-Si/i-SiGe/p^+-Si; (**b**) i-Si/i-SiGe/p^+-Si; (**c**) implanted n^+-Si/i-SiGe/p^+-Si; (**d**) SiGe/Si multilayers with different doping types; (**e**) SiGe/Si multilayers with different Ge fractions.

The q-ALE process of digital wet etching, including oxidation, deionized (DI) water rinsing, oxide removal, and DI water rinsing, and the investigations on the self-limiting behavior of SiGe etching were described previously [31,32]. The flow is shown in Figure 2. The diluted BOE solutions were utilized for sample pretreatment. The steps within dotted

border, including HNO_3 oxidation, DI water rinsing, oxide removal, and DI water rinsing, were repeated for many cycles until the desired etching amount was reached. The HNO_3 solutions in the experiments were prepared by adjusting the volume of analytical-grade nitric acid (70% (wt/wt)) and the volume of deionized water under the condition that the total volume of the solution was kept constant (2 L). The concentrations of the HNO_3 solutions were monitored with a high-precision density meter. The values of concentrations mentioned in this paper represent mass fractions. The nitric acid solutions were employed for oxidation, and were then cooled to room temperature before use. The oxidation time was set to 60 s. It was long enough to reach saturation with an oxidation time of 27.6 s [31]. The BOE solutions used in the experiments were prepared by diluting the original BOEs (NH_4F 34.8%, HF 6.23%) 50 times with deionized water, and the total volumes of the BOE solutions were kept at 2 L. The BOE solutions were used for oxide removal. HF/BOE concentrations that were too high would damage the Si or SiGe layers. The oxide removal time and DI water rinsing time were fixed at 60 s, which ensured the complete removal of oxides and the non-existent cross-contamination of solutions. The temperature of the control recipe was kept at room temperature (20.5 $\pm$ 0.5 °C). Unless otherwise specified, the oxidation–etching procedure in every experiment was performed for 50 cycles repeatedly. Additionally, the H_2O_2 (30% (wt/wt)) solutions were prepared for the H_2O_2 q-ALE experiments as a comparison with the HNO_3 q-ALE experiments.

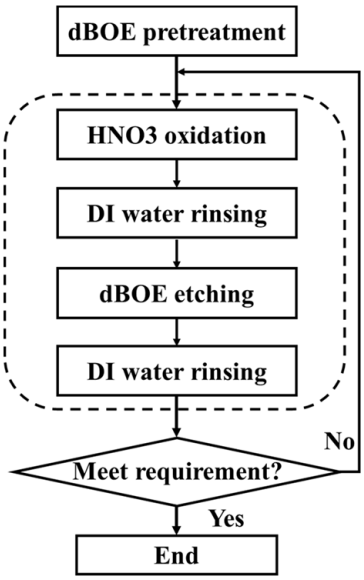

Figure 2. Flow diagram of the main process of digital etching.

The etched morphology of the samples and the etched depth were examined with scanning electron microscopy (SEM) (Hitachi, Tokyo, Japan). Secondary ion mass spectroscopy (SIMS) was used to analyze the doping and mole fraction. Atomic force microscopy (AFM) (Dimension Icon AFM, Bruker, Billerica, MA, USA) was used to measure the surface roughness. High-resolution X-ray diffraction (HRXRD) (Delta-X, Bruker, Billerica, MA, USA) was used to determine the crystallinity and strain relaxation of the Si/SiGe/Si structures.

3. Results and Discussion

3.1. n-Type Doped Si Selectivity with H_2O_2 or HNO_3 q-ALE

The digital etching of SiGe and selectivity of SiGe for p^+-Si were previously identified with H_2O_2-dBOE q-ALE and HNO_3-dBOE q-ALE [31,32]. We chose the above two q-ALE processes to investigate the selectivity of n-type silicon. Figure 3a,b show the SEM cross-section images of Sample I with n^+-Si and in situ phosphorus after etching for 40 cycles with 30% H_2O_2 q-ALE and 40 cycles with 31.5% HNO_3 q-ALE. The relative etching amounts (REAs) of SiGe/p^+-Si with H_2O_2 and with HNO_3 were 18.4 nm (see Figure 3a) and 24.8 nm

(see Figure 3b), respectively. The REPC was calculated by dividing the REA by the number of etching cycles. The REPC with H_2O_2 was 0.46 nm, which was almost identical to the previous results [32]. The REPC with HNO_3 was 0.62 nm, 20% higher than the previous value [31]. This may have been caused by the increase in nitric acid concentration.

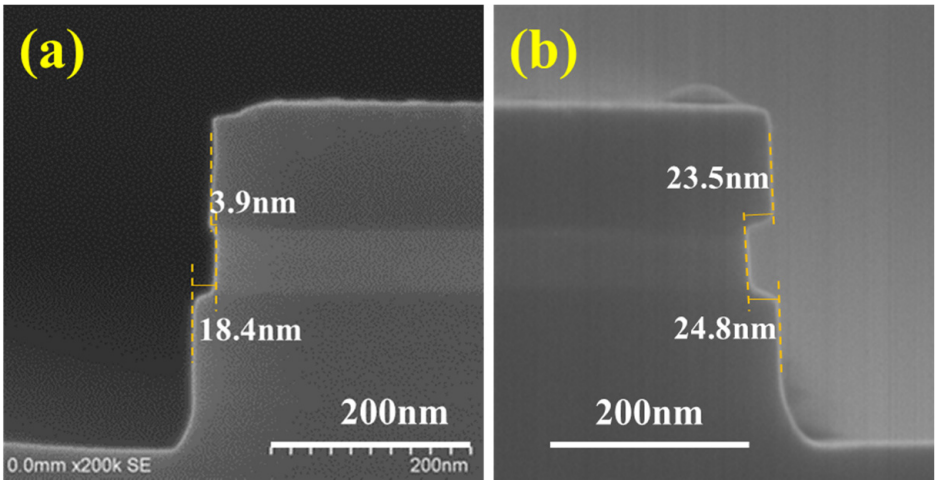

Figure 3. The SEM cross-section images of Sample I after digital etching at 40 cycles with (**a**) 30% H_2O_2-dBOE q-ALE and (**b**) 31.5% HNO_3-dBOE q-ALE.

It is shown in Figure 3a that the REA of SiGe/n^+-Si with H_2O_2 was just 3.9 nm, which is smaller than that of SiGe/p^+-Si, indicating poor selectivity for n^+-Si and the high reactivity of n-Si. Therefore, H_2O_2-dBOE q-ALE was not suitable for p^+-Si/SiGe/n^+-Si structure etching. The differences between n^+-Si and p^+-Si in terms of selectivity and etching rate might be related to the types of carriers or the dopant types. Sample III with the arsenic ion implantation was assessed using 50 cycles with the H_2O_2-dBOE and HNO_3-dBOE q-ALE process. The SEM cross-section images of Sample III are shown in Figure 4a,b. The results are almost consistent. As shown in Figure 4a, with H_2O_2 q-ALE, Sample III exhibited weak selectivity for n^+-Si formed by As implantation. It was demonstrated that the carrier type—instead of dopant type—enhanced the etching rate of n^+-Si in the H_2O_2 q-ALE process. The high concentration of electrons in n^+-Si might accelerate oxide growth in H_2O_2 solutions, which could be explained by the improved relativity of Si-Si back bonds [33].

As shown in Figure 3a,b, the REA of SiGe/n^+-Si with HNO_3 was obviously larger than with H_2O_2, and was close to that of p^+-Si. Similar results are shown in Figure 4a,b. This indicates the excellent selectivity for n^+-Si with the HNO_3 q-ALE process compared with the H_2O_2 q-ALE process, regardless of if in situ doped Si or implanted Si is used. In addition, the etched notch on top of Sample III shown in Figure 4b is assumed to be the result of high dose implantation. Figure 4c shows the SIMS data of boron/arsenic doping and the Ge/Si fraction. The results showed that the dopant concentration was above 1×10^{20} cm^{-3} within a depth of about 100 nm. Such high arsenic doping might lead to local polycrystalline or even amorphous characteristics, which enhance the etching reaction. In addition, a phenomenon that was not easy to observe was that the etching rate of SiGe near the n-type Si was slightly faster than that near the p-type Si. In the arsenic doping profile shown in Figure 4c, the arsenic was distributed in the SiGe. This might have been caused by arsenic implantations. However, the boron distribution in SiGe was negligible. It was considered that the digital etching of SiGe is dependent on the doping of SiGe. We will perform an in-depth study in the third part.

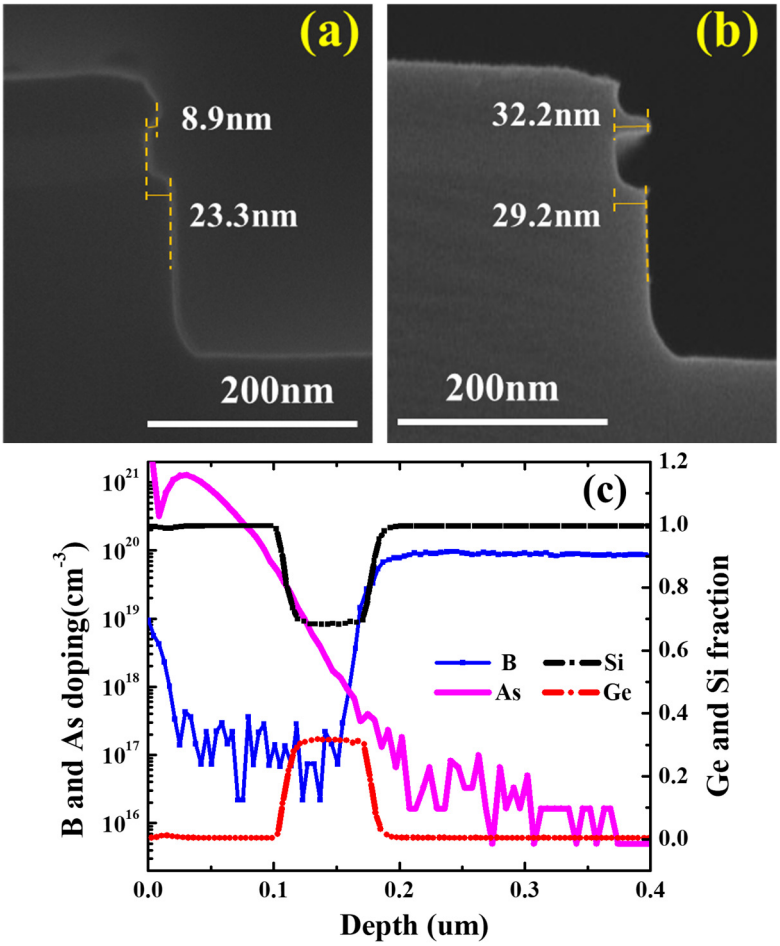

Figure 4. The SEM cross-section images of Sample III after digital etching at 50 cycles with (**a**) 30% H_2O_2-dBOE q-ALE and (**b**) 31.5% HNO_3-dBOE q-ALE. (**c**) SIMS data of boron/arsenic and the Ge/Si mole fraction in Sample III. An abrupt B profile was formed by in situ doped epi, as the profile exhibits a large diffusion into SiGe.

3.2. Effect of Doped Si and HNO_3 Concentration Dependence

In order to explore the effect of doping in silicon on the selectivity of SiGe etching, 31.5% HNO_3 q-ALE experiments were carried out with Sample I and Sample II. The structures of SiGe/n^+-Si, SiGe/p^+-Si, and SiGe/i-Si were included and could be investigated. All of the samples were processed together. Groups of samples including Sample I and Sample II were taken out every 50 cycles. For samples with different doping conditions between the top silicon and bottom silicon, the etching morphologies of the top and bottom silicon might be different. For example, the SEM images of Sample II shown in Figure S1 exhibited different REA values for SiGe/i-Si from those of SiGe/p^+-Si and different i-Si losses with p^+-Si loss.

The structural diagram of the etching morphology is shown in Figure 5. The dashed line in Figure 5 represents the initial envelope lines of the fresh sample. The solid boxes are the envelope lines as they were etched. The angle between the etching slope at the surface of the etched Si and the horizontal direction is θ. Silicon was etched in the vertical and lateral directions. The etching amounts are described as the vertical Si loss (Si loss_v) and lateral Si loss (Si loss_l). As discussed in a previous work [31], the influence of crystal planes on the etching rate was ignored, that is, Si loss_v was almost equal to Si loss_l. The etching amount in the vertical direction could be directly measured. Therefore, the etching amount in the vertical direction is usually regarded as the Si etching amount (Si loss) in the following section. Silicon–germanium was only etched laterally. The etching amount can

be described as the sum of the REA and Si loss_l. The selectivity can be expressed as the ratio of SiGe loss to Si loss, as described in Equation (1).

$$selectivity = \frac{(REA + Si\ loss)}{Si\ loss} = 1 + cot\theta \quad (1)$$

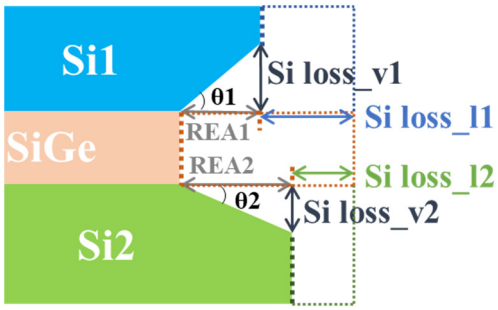

Figure 5. The structural diagram of the etching morphology. The dashed lines represent the initial envelope lines of the fresh sample. The solid boxes are the envelope lines as they were etched.

In addition, in Sample I and Sample II, the diffusion of impurities from silicon to silicon–germanium was negligible, and SiGe could be regarded as intrinsic. The germanium component was fixed in the whole SiGe layer. Therefore, the q-ALE etching of SiGe/Si1 and the q-ALE etching of SiGe/Si2 were independent of each other. The selectivity could be separately calculated by using the Equation (1). According to the angle calculation method and the length calculation method, the values of the selection ratios were very close. This was proved by our experimental data.

Figure 6 shows the dependence of the REA and Si loss on the number of etching cycles for SiGe/n^+-Si, SiGe/p^+-Si, and SiGe/i-Si. The scatters in Figure 6 are the data points obtained through the experiments, and the lines are the curves fitted linearly according to the experimental data. It is shown that the REA of SiGe/n^+-Si, REA of SiGe/p^+-Si, and REA of SiGe/i-Si were highly linear dependent on the number of etching cycles, which was confirmed by the R_square up to 0.975. The Si losses of n^+-Si, p^+-Si, and i-Si were also linearly related to the number of cycles. In the table embedded in Figure 6, the fitting slopes of the REA curves and the Si loss curves represent the REPC and silicon etching amount of each cycle (EPC). It was shown that the REPC of SiGe/p^+-Si was 0.6079 nm, which was close to the REPC value of SiGe/n^+-Si (0.6389 nm). The EPC of p^+-Si was 0.2262 nm, which was also close to the EPC value of n^+-Si (0.2255 nm). The results indicate that the 31.5% HNO_3 concentration had the same etching rate for p^+-Si and n^+-Si. The concentration is expected to be used for the digital etching of p^+-Si/SiGe/n^+-Si stack structures, such as GAA CMOS and TFET applications. Moreover, the slopes in the fitting curves of SiGe/i-Si REA are lower than that of doped Si, suggesting its poor selectivity for i-Si. The EPC of i-Si was 0.3732 nm. It was demonstrated that the etching rate was larger than that of doped Si. It was considered that the doping of silicon contributed to the better selectivity for silicon with the nitric acid etching of SiGe.

Figure 7 shows the selectivity of SiGe/n^+-Si, SiGe/p^+-Si, and SiGe/i-Si. The selectivity was calculated with Equation (1). The experimental data were obtained by measuring the SEM images of Sample I and Sample II with the 31.5% HNO_3 q-ALE process. We carried out the experiments six times on Sample I and Sample II, and six sets of data were obtained. The mean values of the SiGe/n^+-Si, SiGe/p^+-Si, and SiGe/i-Si selectivity were 3.59, 3.68, and 2.56, respectively. The values of the standard deviations were 0.0759, 0.1228, and 0.2512, respectively. The results show the significant improvements in selectivity for doped Si compared with intrinsic Si. The selectivity of SiGe/n^+-Si and SiGe/p^+-Si was similar—40% larger than that of intrinsic silicon. It was demonstrated that doped Si was more difficult to etch in the process of digital etching, which might be due to the oxidation difficulty in the HNO_3 solutions. Moreover, it was observed that the variation in SiGe/n^+-Si was larger

than that in SiGe/p^+-Si. This indicates that it is more susceptible to process factors, such as concentration monitoring and solution preparation. The selectivity might be sensitive to the actual HNO_3 concentration.

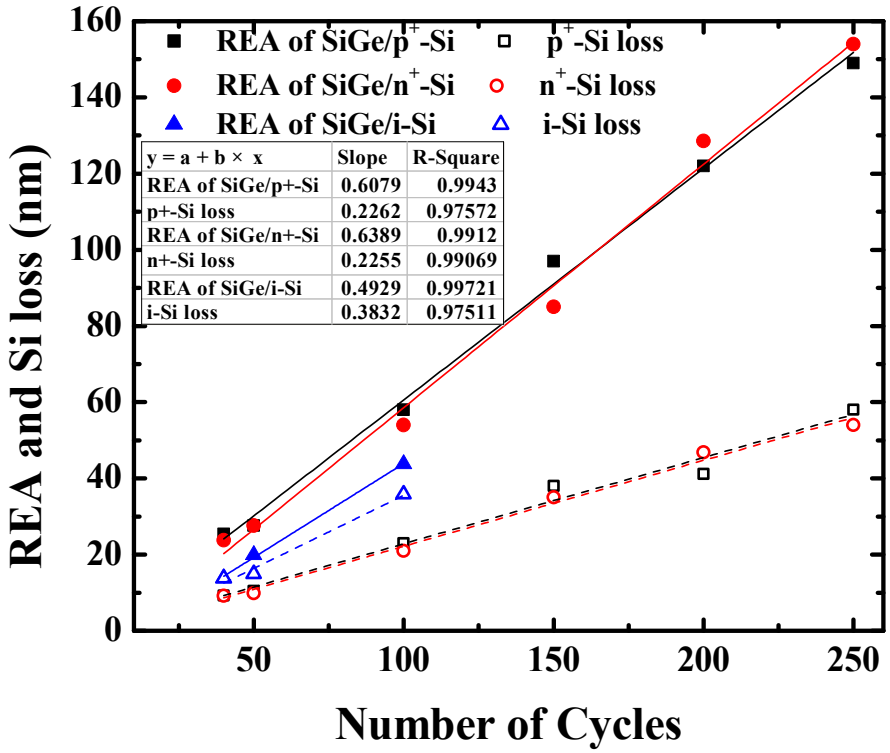

Figure 6. Dependence of the REA and Si loss on the number of etching cycles for SiGe/n^+-Si, SiGe/p^+-Si, and SiGe/i-Si. The scatters are the experimental data, and the lines are the linear fitting curves of the experimental data. The slopes represent the REPC and silicon etching amounts for each cycle (EPC).

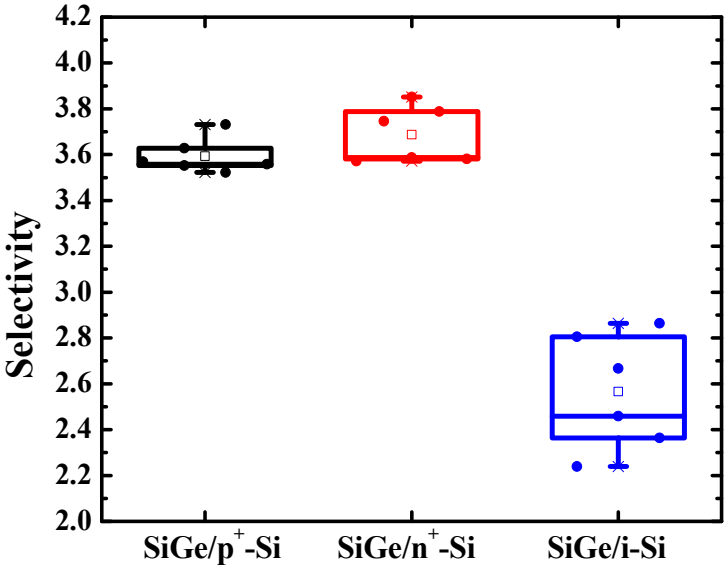

Figure 7. Box plot of the selectivity of SiGe/n^+-Si, SiGe/p^+-Si, and SiGe/i-Si. The means and the standard deviations are 3.59, 3.68, and 2.56 and 0.0759, 0.1228, and 0.2512, respectively. Significant improvements in the selectivity for doped Si were observed. The selectivity of SiGe/n^+-Si and SiGe/p^+-Si was similar, but the variation in SiGe/n^+-Si was larger.

In order to explore the effect of nitric acid concentration, we carried out digital etching experiments on Sample I and Sample II with different HNO_3 concentrations. Figure 8 shows the REPC of SiGe/n^+-Si, SiGe/p^+-Si, and SiGe/i-Si as a function of HNO_3 concentration. As described in Figure 8, with the increase in HNO_3 concentration, the REPC of SiGe/p^+-Si increased and became saturated at 0.61 nm/cycle with the 29.5% HNO_3 concentration. The appearance of saturation is helpful for the stability of the process. However, to achieve accurate etching control for small-sized devices, a controllable etching rate is expected. Moreover, when the concentration was lower than 26.5%, the etched surface of SiGe was very rough, as shown in (Supporting Information, Figure S2a). In the case of high concentrations, damage occurred on the etched surface, as shown in (Supporting Information, Figure S2c). The critical concentration might be between 47.5% and 52%, and the 52% concentration exceeded this limit, resulting in etching damage as shown in (Supporting Information, Figure S2c,d). Therefore, there is a tradeoff between the controllable etching rate, high etching control, small process variations, and excellent etched surfaces when choosing a HNO_3 concentration for the digital etching of SiGe that is selective of p^+-Si.

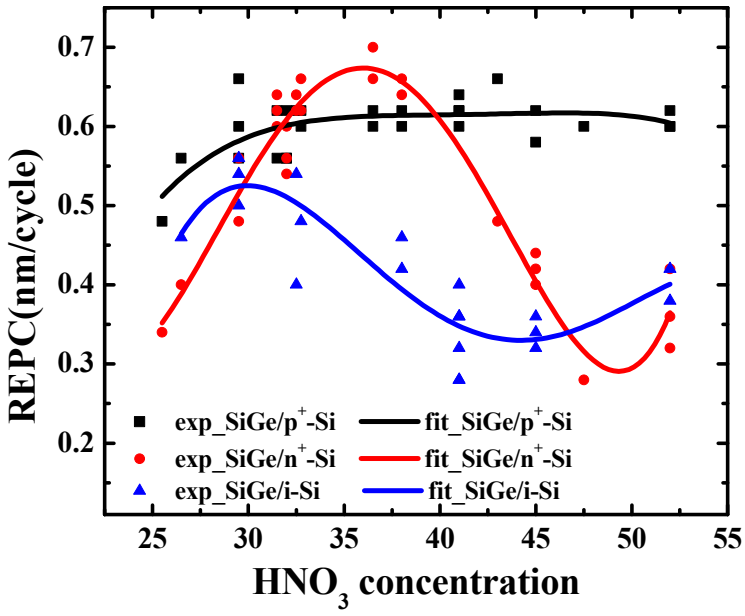

Figure 8. REPC of SiGe/n^+-Si, SiGe/p^+-Si, and SiGe/i-Si as a function of HNO_3 concentration. The dots in the figure are the experimental data, and the lines are the fitting curves of the experimental data. The slopes represent the relative etching amount per cycle (REPC) and the etching amount per cycle (EPC) of silicon.

As discussed above, the concentration range from 26.5% to 47.5% led to an etching morphology with a smooth surface that was free of damage, showing that the study on HNO_3 concentration was meaningful. In this concentration range, it was observed that the REPC of SiGe/n^+-Si had a trend of first increasing and then decreasing. At the concentration of 36.5%, the REPC reached the maximum. The etching rate might be the least influenced by concentration fluctuations. The HNO_3 concentration might be used for the fabrication of GAA transistors due to the small process variations. At the concentrations of 31.5% and 40%, the fitting curves of SiGe/n^+-Si and SiGe/p^+-Si intersected. Despite its identical relative etching rate, the 40% HNO_3 concentration requires a greater nitric acid concentration, thus increasing the cost. It was considered that 31.5% is the most suitable concentration for the digital etching of p^+-Si/SiGe/n^+-Si stack structures, such as for GAA CMOS and TFET applications, which must expose both the n^+ and p^+ sources/drains at the same time.

For the digital etching of SiGe/i-Si, the REPC first increased and then decreased with the increase in HNO_3 concentration. The REPC of SiGe/i-Si reached the maximum, which was equal to that of SiGe/n^+-Si at the 30% HNO_3 concentration. However, there was a large process variation, which is a burden in the control of the etching process. Through many repeated experiments with fine concentration intervals, the HNO_3 concentration relationship can be further verified.

3.3. Effect of Doped SiGe and Ge Fraction Dependence

In the first part, it was observed that the diffusion of arsenic into SiGe might enhance the etching rate of SiGe. Sample IV with in situ doping in SiGe was treated with the 31.5% HNO_3 q-ALE process. To make the effect of doping more obvious and easier to observe, 300 cycles of etching were performed. Figure 9 shows the SEM cross-section images of Sample IV after digital etching at 40, 100, 200, and 300 cycles with 31.5% HNO_3-dBOE q-ALE. It was shown that SiGe layer 1 disappeared at 100 cycles, which might have been due to the etching from the top. The SiGe layer 2 was penetrated horizontally at 200 cycles. It was observed that the remaining SiGe layer 3 at 300 cycles was the lowest. The etching amounts of the intrinsic SiGe layers, including SiGe layer 4, SiGe layer 5, and SiGe layer 6, were almost equal—slightly more than in the p-type SiGe, such as in SiGe layer 7 and SiGe layer 8. The results demonstrate that the relationship of the etching rate with the doping type is: p-type < intrinsic < n-type. The etching rate increased with the increase in n-type dopant concentration. As shown in Figure 9, the remaining amount of SiGe layer 9 doped by almost equal concentrations of arsenic and boron was similar to that of the intrinsic SiGe layers. This indicates the dependence on the carrier type instead of the dopant type. Additionally, it is demonstrated that the etching selectivity between the same doped SiGe and Si always exists regardless of the doping type.

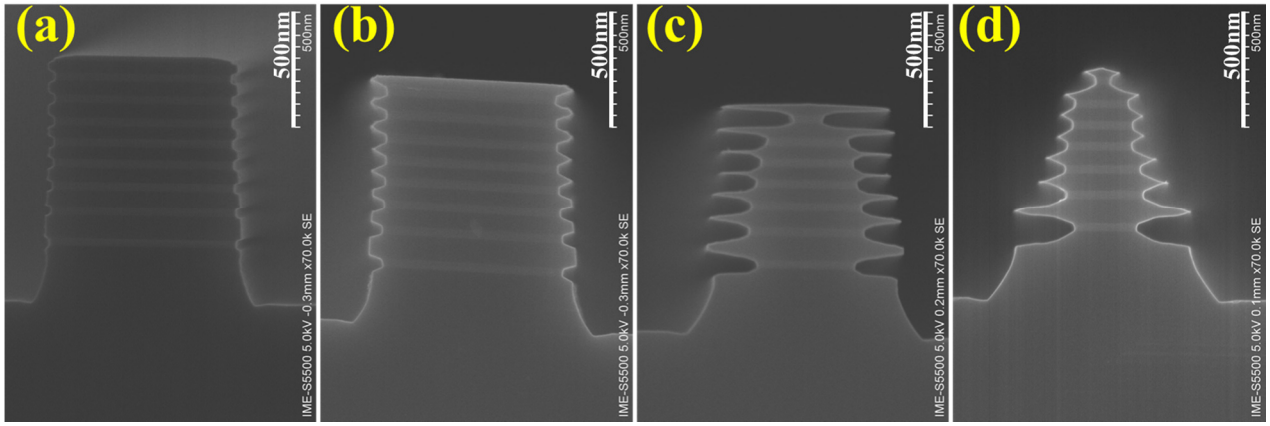

Figure 9. The SEM cross–section images of Sample IV after digital etching with 31.5% HNO_3-dBOE q-ALE at (**a**) 40 cycles, (**b**) 100 cycles, (**c**) 200 cycles, and (**d**) 300 cycles.

To investigate the influence of the Ge fraction on the selectivity and etching rate of n^+-SiGe/n^+-Si, Sample V was etched with 31.5% HNO_3-dBOE q-ALE for 100 cycles. Figure 10 shows the SEM cross-section images of Sample V after digital etching with 31.5% HNO_3-dBOE q-ALE for 100 cycles. As shown in Figure 10, there is a selectivity for n^+-Si in the n^+-SiGe digital etching. The top SiGe might have been etched from the top opening. The REA of the n^+-SiGe increased with the increase in the Ge fraction. This might have been due to the easier hole injection and larger valence band offset [18]. It was demonstrated that increasing the Ge fraction could increase the etching rate of n^+-SiGe and the selectivity of n^+-SiGe/n^+-Si.

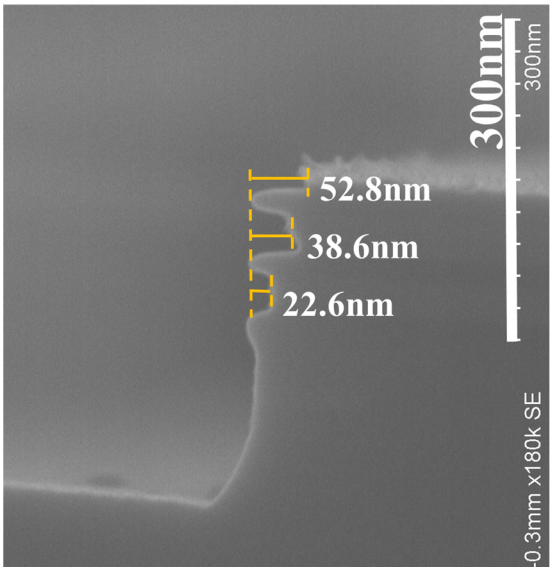

Figure 10. The SEM cross–section images of Sample V after digital etching with 31.5% HNO_3-dBOE q-ALE for 100 cycles.

3.4. Strain and Material Quality Analyses

In order to further determine the strain and material quality of the samples after the etching process, the HRXRD analysis scanning around the (004) diffraction order has been performed on p^+-Si/SiGe/n^+-Si stack layers as grown, after vertical stack etch, and after SiGe q-ALE with 31.5% HNO_3. The HRXRD rocking curves are shown in Figure 11. For the epitaxial growth sample, the SiGe signal was intense, and many fringes were observed around the SiGe peak due to X-ray interference at the SiGe/Si interface, which indicated a high-quality SiGe/Si interface. Therefore, the subsequent etching experiments could be implemented based on the high-quality epitaxial film.

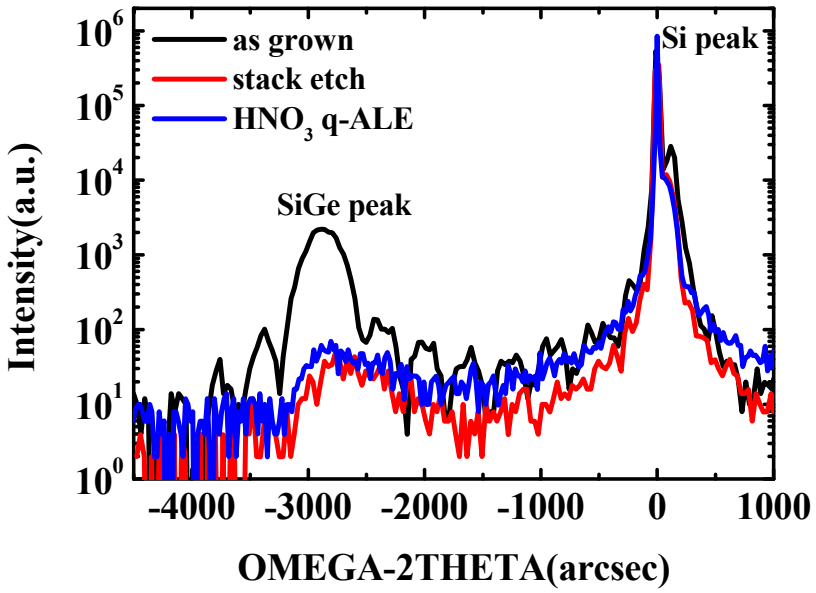

Figure 11. HRXRD rocking curves around the (004) reflection of the as–grown p^+-Si/SiGe/n^+-Si stack layers after vertical stack etching and after 31.5% HNO_3 q-ALE with 50 cycles.

A high full-width at half-maximum (FWHM) is a characteristic of a material's quality [34]. Compared with the epitaxial growth sample, the intensity of the SiGe peak after the etching process was weaker, which might be due to the reduction of SiGe material into

chips after etching. There was also a slight shift of the SiGe peak towards the Si peak, which is an indicator of strain in the SiGe layer. As shown, the SiGe peak of the stack-etched sample was shifted toward the Si substrate peak compared to the SiGe peak of the as-grown sample. This was a result of a strain relaxation induced by the stack-etching process. No continued shift of SiGe peak was detected after SiGe q-ALE etching, indicating that there was no further strain relaxation. This is important point out in the SiGe channel because the energy band and carrier mobility are dependent on the strain.

In vertical GAA CMOS and TFET applications, SiGe is often used as a channel material, and the etched surface can be used as a channel interface. It is necessary to check the surface roughness after it is etched. Figure 12 shows the AFM morphology of the SiGe surface on as-grown epi-SiGe after etched with HNO_3:HF:H_2O mixtures and after etched with q-ALE. It was found that the root mean square (RMS) roughness of the q-ALE process still maintained a comparatively low value after many cycles. The RMS was 0.418 nm at 50 cycles and 0.474 nm at 30 cycles. AFM measurements were performed at many sites. The RMS was always in the range of 0.40 to 0.50 nm. It turned out that the RMS variation was due to differences in the test sites, and there was no dependence on the number of cycles. It was demonstrated that the surface roughness after the HNO_3-dBOE q-ALE process stayed in the range of 0.40 to 0.50 nm and was better than dry [35] and wet chemical continuous etching.

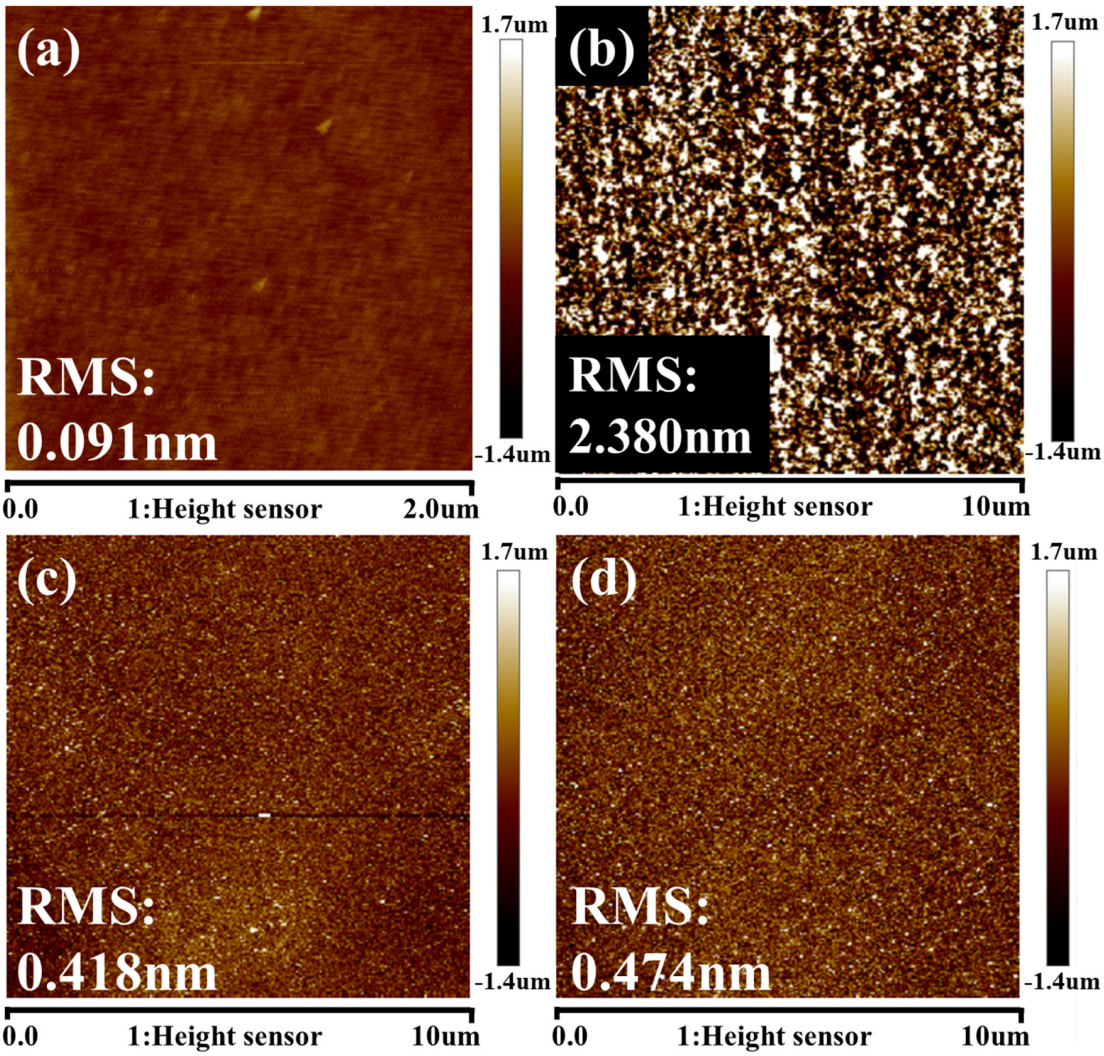

Figure 12. Typical AFM images of flat (100) $Si_{0.72}Ge_{0.28}$ surfaces before and after the etching process: (**a**) as–grown; (**b**) HNO_3:HF:H_2O mixtures; (**c**) q-ALE with 50 cycles; (**d**) q-ALE with 30 cycles.

4. Conclusions

The HNO_3-dBOE q-ALE process consists of alternative HNO_3 oxidation and dBOE oxide removal. Compared with the H_2O_2-dBOE q-ALE process, excellent selectivity for n-type doped Si could be found with HNO_3-dBOE q-ALE. Doping plays an important role in the selective etching of SiGe. The selectivity of SiGe/Si was enhanced by doped Si. In addition, the selectivity for n-type doped Si had a strong dependence on the HNO_3 concentration. The relative etching of n^+-Si reached a maximum at 36.5% HNO_3 concentration, and p^+-Si was saturated at 29.5% HNO_3 concentration. It was found that at 31.5% HNO_3 concentration, identical selectivity levels for p^+-Si and n^+-Si could be achieved. The REPC was 0.6 nm. The etching selectivity was 3.6–40% higher than that of intrinsic Si. The most suitable concentration for digital etching of p^+-Si/SiGe/n^+-Si stack structures, such as for GAA CMOS and TFET applications, which have to expose both the n^+ and p^+ sources/drains at the same time, is considered to be 31.5%. The relationship between the etching rate of doped SiGe and the doping type is: p-type < intrinsic < n-type. The etching rate of doped SiGe could be improved by the Ge fraction. Finally, this technique is a promising process for the fabrication of GAA CMOS transistors and TFETs due to its perfectly controllable etching rate and the resulting atomically smooth surface roughness.

Supplementary Materials: The following are available online at https://www.mdpi.com/article/10.3390/nano11051209/s1, Figure S1: The SEM cross-section images of Sample II after digital etching at 50 cycles: (a) in 30% H_2O_2-dBOE q-ALE (b) 31.5% HNO_3-dBOE q-ALE, Figure S2: The SEM cross–section images of Sample I after HNO_3 digital etching at 50 cycles with varying HNO_3 concentrations: (a) 25.5% HNO_3 concentration (b) 36.5% HNO_3 concentration (c) 52% HNO_3 concentration, the etch damage is marked in the yellow dotted line. (d) significant etch damage at 52% HNO_3 concentration.

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Review

Review of Si-Based GeSn CVD Growth and Optoelectronic Applications

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Abstract: GeSn alloys have already attracted extensive attention due to their excellent properties and wide-ranging electronic and optoelectronic applications. Both theoretical and experimental results have shown that direct bandgap GeSn alloys are preferable for Si-based, high-efficiency light source applications. For the abovementioned purposes, molecular beam epitaxy (MBE), physical vapour deposition (PVD), and chemical vapor deposition (CVD) technologies have been extensively explored to grow high-quality GeSn alloys. However, CVD is the dominant growth method in the industry, and it is therefore more easily transferred. This review is focused on the recent progress in GeSn CVD growth (including ion implantation, in situ doping technology, and ohmic contacts), GeSn detectors, GeSn lasers, and GeSn transistors. These review results will provide huge advancements for the research and development of high-performance electronic and optoelectronic devices.

Keywords: GeSn; CVD; lasers; detectors; transistors

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1. Introduction

Si-based integrated circuits (ICs), which are dominated by Si CMOS technology, have reached their physics limit. The influences of quantum effects, parasitic parameters, and process parameters on data transmission applications are also reaching their limits, as the rapid development of microelectronics has led to higher requirements for data transmission technology. For these reasons, scientists have proposed schemes to integrate optoelectronic devices with microelectronic devices [1–7]. However, Si-based on-chip integrated light source was lacking, and the light sources for existing optoelectronic integrated circuits (OEICs) were all externally coupled; though the coupling efficiency between the edge of the light source and grating coupler was high enough, the lack of an on-chip light source restricted OEICs' applications [8–10]. As such, many research programs started to pay more attention to Si-based monolithic OEIC technology [11–15], which has the following advantages over the baseline technology: (i) it is compatible with mature Si CMOS technology; (ii) has low costs; (iii) has larger wafer sizes and larger scale production; (iv) its partial electrical interconnection can be replaced by optical interconnection, which

can realize high-efficiency, high-speed, and low loss data transmission. Si-based monolithic OEIC technology uses Si-compatible semiconductor technology to integrate optoelectronic devices into Si chips in order to improve chip performance, extend chip function, and reduce costs. Though Si-based photonic devices, such as optical waveguides [16,17], photodetectors [18–20], optical modulators [21–23], and optical switches [24,25], have been successfully developed, it is difficult to achieve high-efficiency emission due to the facts that Si is an indirect bandgap semiconductor and its light emission efficiency is about five orders of magnitude lower than that of direct band gap III–V compound semiconductors. Thus, the need for an Si-based high-efficiency light source represents an important technical bottleneck in the development of Si-based monolithic OEICs. Therefore, looking for a direct bandgap semiconductor material that is compatible with the Si CMOS process is of great significance in the creation of large scale Si-based monolithic OEICs [26–28].

Group IV materials are compatible with the traditional Si CMOS process, and Si, SiGe, and Ge are commonly used as indirect band gap semiconductors despite not being suitable for light emission. Fortunately, tensile strain engineering and Sn-alloying engineering have enabled Ge to become a quasi-direct bandgap or direct bandgap material due to the small bandgap difference between its two minima in conduction bands (only 136 meV). Experimental research has shown an optical gain of 0.24% for tensile-strained n^+-type Ge (the n-type doping level is 1×10^{19} cm^{-3}), which led to the creation of optically injected and electrically injected Ge lasers [29–32]. However, the threshold for a Ge laser is too high, which means that weak tensile-strained n^+-type Ge is not able to supply enough optical gain to achieve low-threshold lasing.

In recent decades, GeSn alloys have demonstrated novel indirect-to-direct bandgap transition, as well excellent carrier transport. Due to their tunable band structures, GeSn materials have become promising candidates to create Si-based OEICs with higher hole mobility, enhanced light absorption, etc. [33–37]. Growing high-quality GeSn layers with relatively high Sn contents has different challenges, e.g., Sn segregation during growth and the poor thermal stability of SnGe layers [38–41]. These issues root from the low solid solubility of Sn in Ge (<1%) and the large lattice mismatch between Si or Ge and GeSn. As early as 1995, the first growth of a GeSn/Ge superlattice was reported using a very low growth temperature in a molecular beam epitaxy (MBE) chamber. Such GeSn layers had an Sn content of 26% [42,43]. Based on these early pioneer works, other growth techniques, such as chemical vapor deposition (CVD) and magnetron sputtering, have been widely used to grow high-quality direct bandgap GeSn materials with high Sn contents [44–49]. Although MBE can grow GeSn materials well, its growth rate is extremely low, which makes it tough to manufacture on a large scale. To achieve a significant impact within the industry, it is very important to develop a commercially available tool to grow high-quality GeSn materials. At a very early development stage of GeSn growth via CVD, SnD_4 and Ge_2H_6 were chosen as the Sn precursors and Ge precursors, respectively. Although there were many foundational studies on GeSn growth via CVD, SnD_4 is a high-cost material with a short lifetime, which makes it incompatible with the industry. For this reason, other precursors such as $SnCl_4$ have been explored. The IMEC and KTH groups pioneered the growing of GeSn layers using commercially available reaction precursors ($SnCl_4/Ge_2H_6$) [50]. A major breakthrough was later demonstrated using the production of commercially available reaction precursors ($SnCl_4/GeH_4$) [51,52]. The limitations of incorporating Sn into Ge have been conquered, and two major breakthroughs for GeSn CVD growth have been reached: (i) a world record high Sn content (22.3%) in bulk GeSn materials with PL emission was observed at room temperature (indicating good material quality), and (ii) SiGeSn/GeSn/SiGeSn multiple quantum well (MQW) structure growth and low-temperature PL intensity were later able to be remarkable enhanced [53–56]. Furthermore, the low costs and widespread availability of these chemicals in large-scale fabrication makes them the best choice for GeSn-based optoelectronic integration into CMOS processing. To make GeSn an efficient N-type or P-type semiconductor material for optoelectronic device application, there is an urgent need to research and develop doping

engineering for GeSn. Currently, doping technologies, such as ion implantation and in situ CVD doping, have been optimized regarding their target doping concentration and doping distributions.

After the successful growth of P^+-Si/i–GeSn/n–GeSn via CVD, Jay Mathews et al. demonstrated the world's first GeSn photodetector with a 2% Sn content in 2009 [57]. The wavelength cutoff was extended to be at least 1750 nm, which means that the GeSn photodetector with a 2% Sn content can cover the entire telecommunication band. Since then, GeSn photoconductor detectors [58–63], and p–GeSn/i–GeSn/n–GeSn heterostructure detectors [64–68] have been demonstrated. Advances in GeSn CVD growth technology have occurred alongside material quality and detector performance improvements, including: (i) the wavelength cutoff for the GeSn photodetector has been progressively broadened from 1800 nm to 2100, 2400, 2600, 2650, and 3650 nm [63]; (ii) based on wafer-bonding technology, the dark current for GeSn photodetector has been suppressed by more than two orders of magnitude [69]; (iii) peak specific detectivity values are now comparable to those of commercial extended-InGaAs detectors (4×10^{10} cm·$Hz^{1/2}$·W^{-1}) at the same wavelength range; (iv) a passivation technique was developed to enhance responsivity and peak specific detectivity [65]; and (v) mid-IR imaging was demonstrated with GeSn photodetectors, and the image quality of the GeSn photodetectors was found to be superior to that of a commercial PbSe detector [63].

Alongside the significant breakthroughs in GeSn growth and detectors, GeSn lasing had also developed to an advanced stage. Recently reported GeSn laser structures have all been grown via the CVD technique. Following the observation of a PL peak with narrowed line widths, a true direct bandgap GeSn material with an Sn content of up to 10% was experimentally demonstrated in 2014 [33]. Encouraged by this major technical breakthrough, researchers used the injection methods such as optical injection with a Ge laser to check the GeSn waveguide, and lasing behavior was clearly observed at a low temperature in 2015 [70]. Following this breakthrough, several types of GeSn lasers [71–82] were demonstrated, though they still suffer from the problems of low-temperature operation and high lasing thresholds. To overcome these difficulties, several methods have been proposed to improve performance, such as greater Sn incorporation into Ge [73,75,76], the use of SiGeSn/GeSn/SiGeSn heterostructures or SiGeSn/GeSn/SiGeSn MQWs as the gain medium [83–86], a modulation doping scheme in SiGeSn/GeSn/SiGeSn MQWs [87], defect management [80], and thermal management [81,82]. Considerable efforts in GeSn lasing research have led to an increased maximum lasing temperature of 270 K [76] due to the amazing discovery of strain relaxation growth mechanism [88]. Near-room-temperature lasing was also observed for a GeSn active medium with a 16% Sn content and high uniaxial tensile strain [77]. A breakthrough regarding the optical pumping threshold was reported in 2020, when a low-Sn-content GeSn material with a high uniaxial tensile strain was utilized as an active medium; continuous wave (CW) lasing was also achieved. However, the lasing temperature only reached 100 K due to the low directness of the active medium [80]. In the same year, electrically pumped GeSn/SiGeSn heterostructure lasers with operation temperatures of up to 100 K were demonstrated [89,90]; this was an essential achievement for Si-based electrically pumped group IV interband lasing.

As a group IV material, GeSn is compatible with Si and can realize the transition from indirect band gap to direct band gap by adjusting its Sn content, which makes it the best substitute for group IV materials in Si-based optoelectronic integration applications. GeSn has an extremely high carrier mobility, so it may also be an ideal materials for transistor applications. Due to the significant development of GeSn CVD growth technology, vertically stacked 3-GeSn-nanosheet pGAAFETs (gate-all-around FETs) [91], GeSn p-FinFETs [92,93], GeSn n-channel MOSFETs [94,95], GeSn/Ge vertical nanowire pFETs [96], GeSn GAA nanowire pFETs [97], and GeSn n-FinFETs [98] have been successfully demonstrated. Additionally, GeSn's direct band gap property was found to effectively improve the tunneling probability of electrons, making an excellent material for TFET preparation [99,100], this opening a new development direction for the integrated circuit after Moore's era. The

discovery of this property has attracted considerable research interest in recent years. Since Sn naturally has low solid solubility in Ge (smaller than 1%), growth of high Sn composition single crystal GeSn is difficult. At present, devices prepared with GeSn materials are still in the research and development stage, so they have not been widely used in production.

To the best of our knowledge, there has yet to be a review article that systematically reported on GeSn material growth and counterpart optoelectronic devices using the CVD technique. UHVCVD [101–104], RPCVD [105–110], PECVD [111–113], LPCVD [114–117], and APCVD [118,119] are discussed in this review, with a focus on identifying processes that can be transferred for the commercial production of GeSn. The objective of this comprehensive review article is to provide readers with a full understanding of the recent experimental advancements in GeSn material growth using CVD, as well as their optoelectronic applications. However, due to the large numbers of publications in this area, the authors of this work only selected articles with significant scientific impacts.

2. Research Progress for GeSn CVD Growth and Its Potential Applications

So far, several types of growth techniques, such as MBE, magnetron sputtering, and CVD have been used to grow GeSn materials. CVD is the dominant growth method in the industry, so more easily transferable. Therefore, we decided to review GeSn CVD growth and its potential applications.

2.1. Potential Applications

A literature survey revealed that GeSn materials have numerous potential applications, including Si-based, integrated, high-efficiency light sources [120–122]; high-mobility electronic devices [92–100]; low-cost, Si-based, high-performance shortwave infrared (SWIR) imaging sensors [63–65]; Si-based photovoltaics [123]; optical signal encoding in the mid-infrared range [124,125]; high-performance logic applications [126,127]; Si-based integrated thermoelectrics as wearable devices [128,129]; Si-based spintronics [130,131]; Si-based integrated reconfigurable dipoles [132,133]; and Si-based quantum computing [134,135] (Figure 1). GeSn-related fundamental research and development applications have also been extensively investigated (Figure 2).

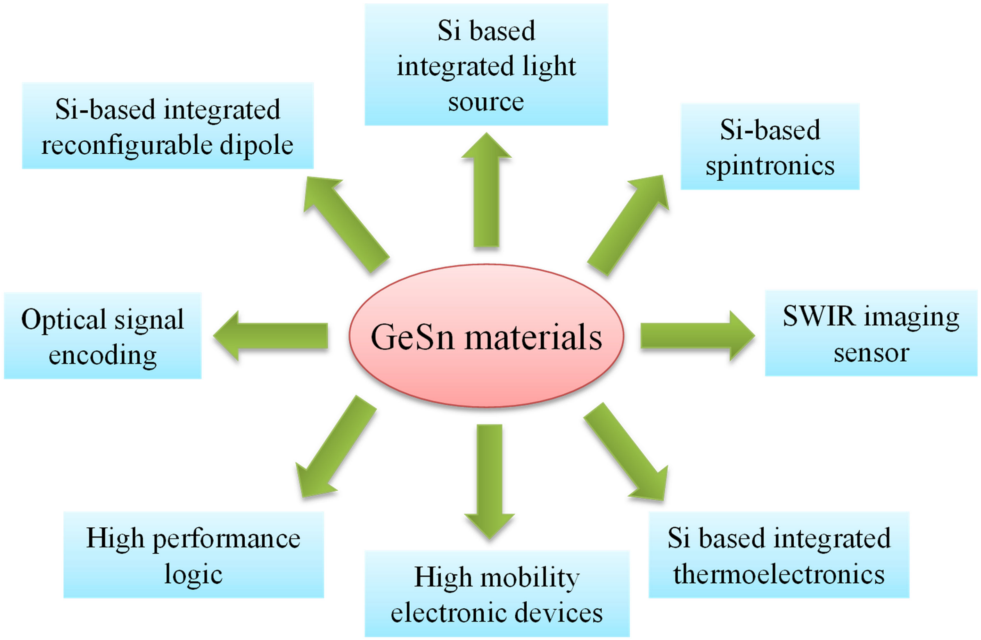

Figure 1. Potential applications of GeSn materials in different research areas.

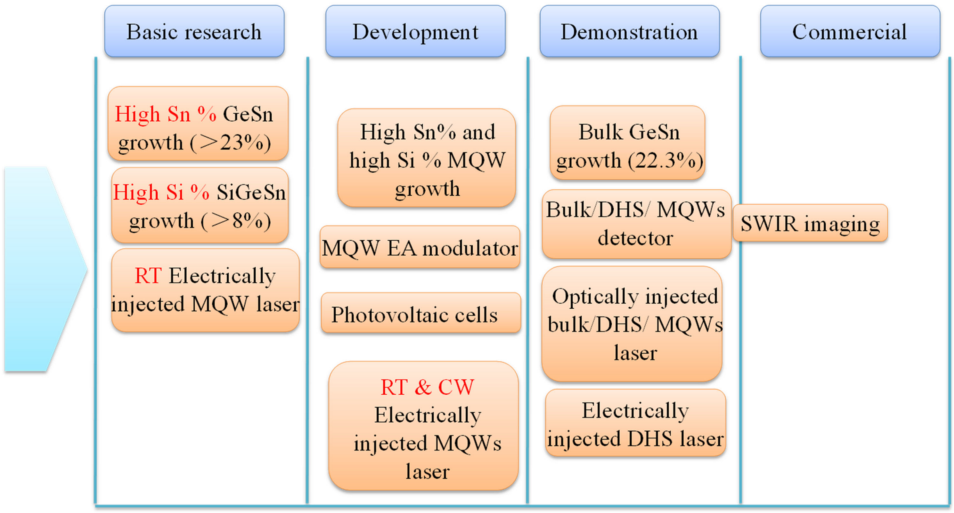

Figure 2. Optoelectronic applications of GeSn as a function of technology readiness level (GeSn transistors, which are still in the technical development stage, are not shown here due to space limitations).

Figure 2 shows the optoelectronic applications of GeSn as a function of technology readiness level. It can be observed that GeSn detectors are getting closer to the low-cost SWIR imaging applications, indicating that GeSn materials have great potential for use in next-generation civilian night-vision and IR cameras [63–65]. However, there are still some technical problems, which are discussed in Section 3. In addition to detectors (which are being rapidly developed), high-quality SiGeSn/GeSn/SiGeSn MQW growth, room-temperature, CW, and electrically injected SiGeSn/GeSn/SiGeSn MQW lasers; MQW electro-absorption (EA) modulators; and photovoltaic cells are in the research and development stage.

2.2. Research Progress for GeSn CVD Growth

In 2001, Kouvetakis's group from Arizona State University (ASU) first reported a GeSn alloy on oxidized and oxidized-free Si using UHVCVD [136]; since then, extensive GeSn CVD growth-related research works have been carried out. In 2003, SnD_4 and SiH_3GeH_3 were used as reaction precursors, and single-phase SiGeSn on a GeSn buffer was first achieved on Si via UHVCVD at 350 °C [137]. To create GeSn materials with higher Sn contents, SnD_4 and Ge_2H_6 were chosen as Sn and Ge precursors, respectively; the experimental results showed that SnD_4 is helpful for low-temperature growth, and its reaction with Ge_2H_6 can create GeSn with an Sn content of up to 25% [138] (Figure 3). The crystallinity, bandgap, lattice constants, optical properties, photoresponses, photocurrents, and Raman scattering results of GeSn materials grown by UHVCVD have been systematically demonstrated [139–144]. In order to grow GeSn at extremely low temperatures, some authors used Ge_3H_8 and Ge_4H_{10} as Ge precursors [145,146]. By using this method, single crystalline GeSn alloys were successfully deposited at temperatures ranging from 300 to 330 °C, the growth rate of the allows was able to meet industrial requirements, and the traditional SK growth mode was avoided. Finally, the authors concluded that Ge_3H_8 is a superior solution to grow GeSn alloys via UHVCVD [145,146]. Compared with previously reported reaction precursors (SnD_4/Ge_2H_6), the growth rate of the SnD_4/Ge_3H_8 combination was found to be improved 3–4 times. For this reason, a 1 μm thick GeSn layer with an Sn content of up to 9% was implemented, and room temperature photoluminescence spectra were observed, indicating that GeSn has great potential to be utilized as a gain medium for a Group IV laser. Later, SiGeSn growth at ultralow temperatures (from 290 to 330 °C) using Ge_4H_{10}, Si_4H_{10}, and SnD_4 were reported [147–149].

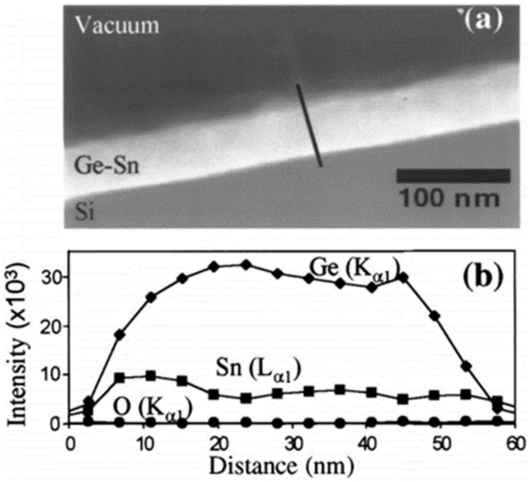

Figure 3. (**a**) Scanning transmission electron microscopy (STEM) image and (**b**) EDX cross-sectional profile of the GeSn with Sn contents of up to 25%. Reproduced with permission from [138], AIP Publishing, 2001.

Although there have been many foundational studies on GeSn growth via CVD investigated, SnD_4 has high costs, is incompatible with the industry, and is unstable at room temperature. For these reasons, other precursors such as $SnCl_4$ have been explored. IMEC and KTH were the first groups to propose GeSn growth using commercially available reaction precursors ($SnCl_4/Ge_2H_6$).

Due to the fact that $SnCl_4$ is liquid at room temperature, these groups evaporated $SnCl_4$ using a bubbler that was connected to an RPCVD chamber. Experimental results showed that defect-free doped and undoped GeSn layers with Sn contents of up to 8% were created using RPCVD at atmosphere conditions. Thermal stability was further determined by annealing at different conditions (400 °C for 10 min, 400 °C for 30 min, 500 °C for 10 min, and 500 °C for 30 min); the (004) omega-2 theta scan of as-grown and annealed $Ge_{0.92}Sn_{0.08}$ samples were compared (Figure 4a). For the sample annealed at 500 °C for 30 min, the diffraction peaks of GeSn and Ge widened and a clear GeSn peak shift was observed, suggesting possible Ge–Sn interdiffusion. To further confirm this assumption, secondary ion mass spectroscopy (SIMS) was conducted. From the SIMS results, the authors concluded that APCVD-grown GeSn with 8% Sn content was stable at the annealing condition of 500 °C for 30 min (Figure 4b). This work paved the way for GeSn growth using both commercially available reaction precursors and CVD production equipment.

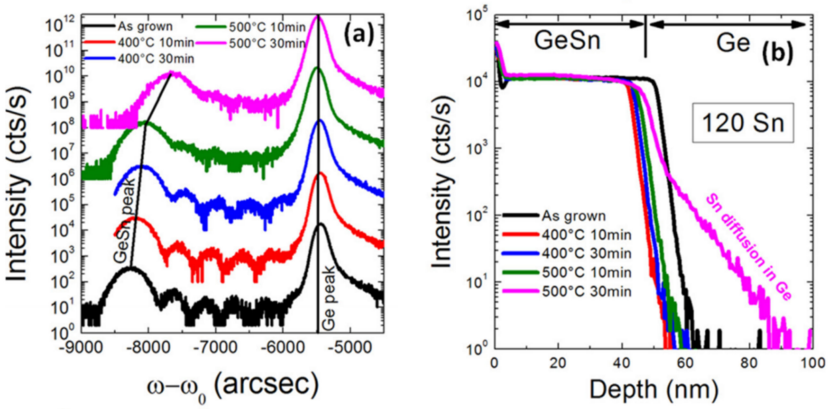

Figure 4. Comparison of (**a**) (004) omega-2 theta scans and (**b**) Sn content profiles of as-grown and annealed $Ge_{0.92}Sn_{0.08}$ samples under different annealing conditions. Reproduced with permission from [150], AIP Publishing, 2011.

Since then, there has been a sharp increase in the scientific knowledge of GeSn CVD growth, as shown by a number of publications (Figure 5a). The number of publications on GeSn CVD growth grew dramatically in 2013 and reaches 19 in 2018 (Figure 5a). The rapid development of GeSn CVD growth techniques has meant that the number of GeSn optoelectronic device publications followed the similar tendency (Figure 5b): (i) following the world's first demonstration of a GeSn detector, GeSn detector-related publications grew from 1 in 2008 to 30 in 2019; (ii) since the world's first demonstration of an optically pumped GeSn laser, publications related to GeSn lasers continually increased from 10 in 2015 to 25 in 2019, and the majority of these laser publications reported experimental results; (iii) there are still few publications regarding GeSn modulators, and a CVD-grown modulator has not been achieved (the majority of the modulator publications have been theoretical investigations).

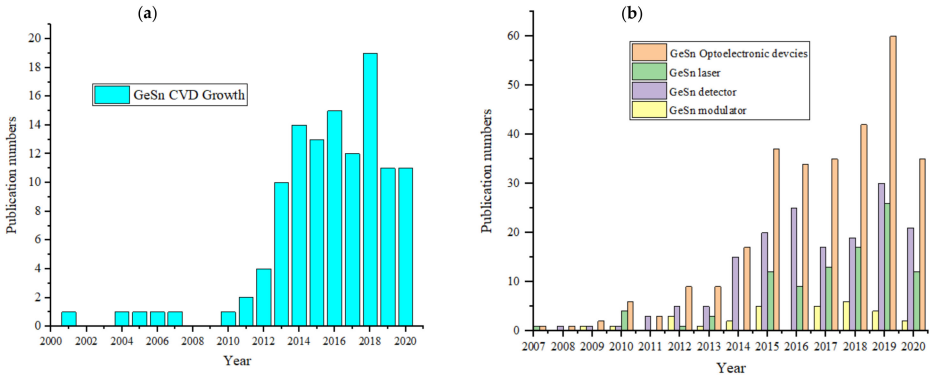

Figure 5. (**a**) Number of publications/year on GeSn materials grown by the CVD technique; (**b**) number of the publications/year on GeSn optoelectronic devices (theoretical calculations and conference proceedings are included).

To help readers to understand the research status of CVD growth techniques, Figure 6 summarizes research on GeSn CVD growth since the introduction of CVD in 2001 in terms of the research institution, growth chamber, year of deposition, and corresponding reference. Figure 6 shows several types of growth chambers, such as UHVCVD (baby color dot), RPCVD (dark color dot), APCVD (red color dot), PECVD (orange color dot), LPCVD (coffee color dot), and RTCVD (green color dot), that have been used to grow GeSn materials. Following pioneer works from ASU and IMEC, research groups from KTH Royal Institute of Technology (KTH), Applied Materials Inc (AM), PGI (Peter Grünberg Institute), and UA (University of Arkansas) started researching GeSn growth using CVD technology in 2013. Since then, research groups from ASM, University of Warwick (UW), National Taiwan University (NTWU), and Université de Montréal (EPM) have also researched GeSn CVD growth. Among all CVD growth technologies, RPCVD growth chamber is most widely accepted due to its commercial availability and more easily transferability (six research groups have used RPCVD chambers to grow GeSn). After the successful demonstration of the low-temperature growth of high-quality Ge on Si using PECVD, plasma-enhanced techniques came to be regarded as promising methods to grow GeSn materials. Thus, plasma-enhanced GeSn growth techniques aroused researchers' attentions from UA and ASU.

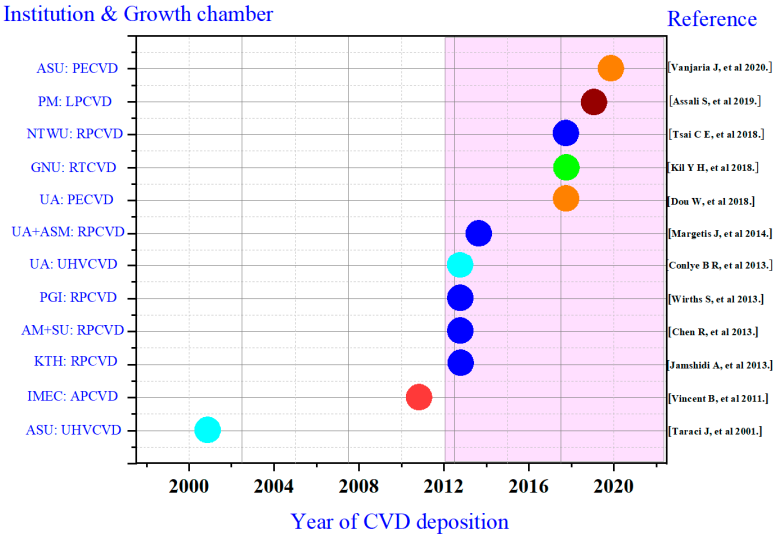

Figure 6. List of GeSn CVD growth papers by different groups.

2.3. GeSn CVD Growth Strategy

To have a full understanding of the GeSn CVD growth strategy, it is necessary to calibrate the Ge growth at low temperatures (below 450 °C). After calibration, the flow rate between Ge precursor and Sn precursor needs to be taken into consideration due to the possible etching effect of the generated Cl* species on the GeSn surface. Therefore, there is a critical flow rate, and the growth rate for GeSn growth has to be high enough to overcome the etching rate. More importantly, the effects of temperature, pressure, carrier gas, and strain relaxation on material growth must be canvassed.

2.3.1. Temperature and Pressure Effect on GeSn Growth

Previous GeSn CVD growth work has demonstrated that Sn content is closely related to growth temperature because the decreasing temperature moves the growth conditions further from equilibrium, thus increasing Sn content. Therefore, we summarize most GeSn CVD growth results in Figure 7. In GeSn growth using the $SnCl_4/GeH_4$ reaction precursor combination, $SnCl_4$ and GeH_4 lose their reactivity at a temperature of 280 °C and growth is totally ceased. Below 285 °C, GeH_4 is not well-adsorbed, which may suggest the generation of GeH_2 and/or 2H. Therefore, the growth temperature for GeSn RPCVD growth with the $SnCl_4/GeH_4$ reaction precursor combination is usually higher than 280 °C. For the Ge_2H_6 and $SnCl_4$ precursor combination, GeSn growth temperature could be as low as 275 °C.

Significantly, UA demonstrated GeSn growth using PECVD with the commercially available GeH_4 and $SnCl_4$; low-temperature growth at 350 °C for GeSn epitaxy on an Si substrate was achieved with an Sn content of up to 6% [113]. By using a 1064 pulsed laser as the light source, a PL signal was also observed at the peak wavelength of 2000 nm, as shown in Figure 8 (Spot III).

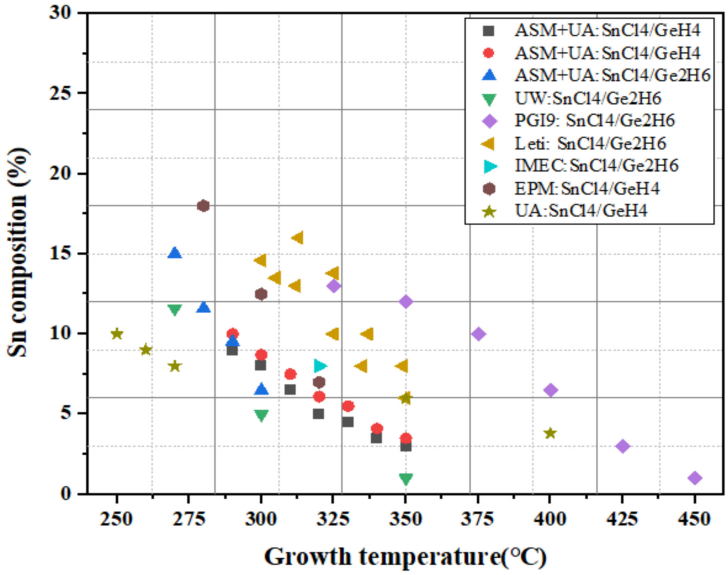

Figure 7. Temperature effect on the Sn content from different research groups (UW, UA, and EPM denote the University of Warwick, University of Arkansas, and Université de Montréal, respectively) [113,115–117,151–156].

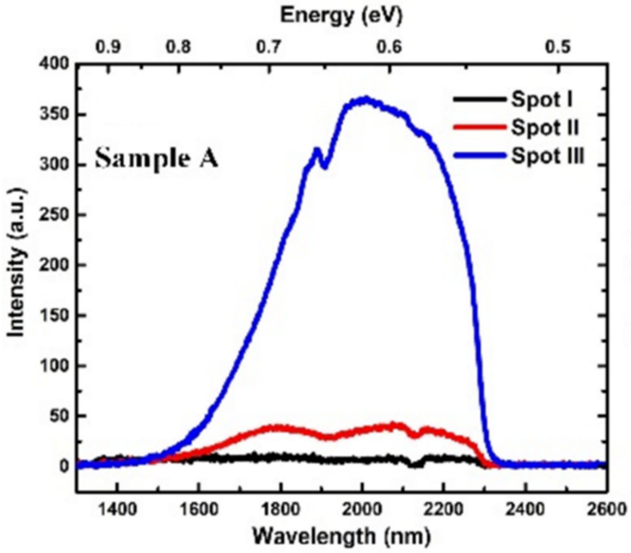

Figure 8. Room-temperature PL spectra for GeSn grown by PECVD technology (the Sn content is 6%). Reproduced from [114], open access by OSA Library, 2018.

Their follow-up work verified that the PECVD system was able to grow a high-Sn-content (>10%, with an PL emission peak at approximately 2100 nm) GeSn layer at ultralow temperatures (250, 260, and 270 °C) [157] (Figure 9). The realization of GeSn PECVD growth at such low temperatures using a $SnCl_4/GeH_4$ precursor combination mainly benefits from plasma-assisted reactivity improvements [157]. With proper growth optimization, the Sn content of the GeSn grown by PECVD should be higher than that of other CVD chambers. Compared to GeH_4, Ge_2H_6 is more reactive and possesses lower growth temperature capabilities, indicating that the reactivity of the Ge-hydride is the only limiting factor for low-temperature GeSn growth. For GeSn RPCVD growth using GeH_4, Sn incorporation was found to drastically decrease at ~285 °C, whereas the growth temperature limit for using Ge_2H_6 was found to be 270 °C [153].

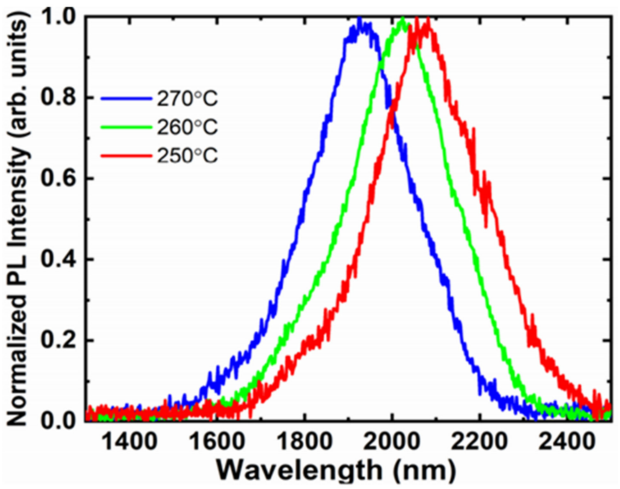

Figure 9. PL spectra for the GeSn grown at temperatures of 250, 260, and 270 °C. Reproduced from [157], open access by ScholarWorks@UARK.

For GeSn growth in a UHVCVD chamber [158–161], growth pressure is usually kept in the range of 1×10^{-4}–2.5×10^{-4} Torr, and Sn content rises with decreasing growth temperatures. Even when different combinations of precursors (SnD_4/Ge_2H_6, SnD_4/Ge_3H_8, and SnD_4/Ge_4H_{10}) are chosen, similar Sn content variation trends are observed (Figure 10). However, growth temperatures with different precursor combinations are varied; the lowest reported growth temperatures for SnD_4/Ge_2H_6, SnD_4/Ge_3H_8, and SnD_4/Ge_4H_{10} are 250, 350, and 150 °C, respectively [145,146,161]. Different from UHVCVD, pressures for GeSn growth in LPCVD and APCVD chambers have been found to range from 10 to 760 Torr [115–117,150]. The surface morphology of a layer GeSn grown by APCVD is shown in Figure 11, where surfaces are milky and pyramidical defects are observed at pressures of 10 and 100 Torr; this issue can solved by further increasing the growth rate (keep the $SnCl_4$ constant and increase the Ge_2H_6 gas flow).

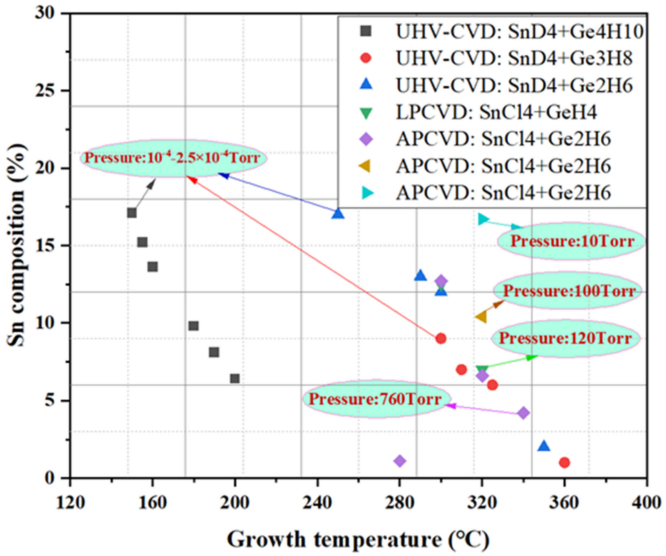

Figure 10. Temperature effect on Sn content from UHVCVD, LPCVD, and APCVD growth.

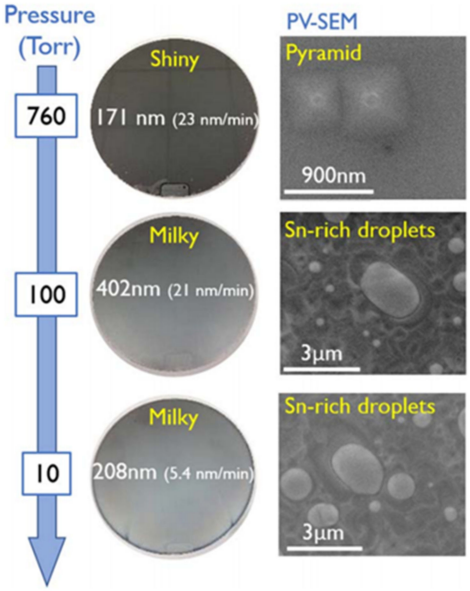

Figure 11. GeSn surface morphology vs. growth pressure (growth temperature: 320 °C; growth pressure: 10, 100, and 760 Torr; precursors: Ge_2H_6 and $SnCl_4$). Reproduced with permission from [119], IOP Publishing, 2018.

For GeSn APCVD growth at a temperature of 320 °C, pressure was found to be a main factor in the growth of high-Sn-content GeSn materials (the achieved Sn contents at 10 and 760 Torr were 16.7% and 6.6%, respectively) [119]. For LPCVD growth at 120 Torr and 320 °C, the Sn content for GeSn was almost the same as that of APCVD.

2.3.2. Carrier Gas Effect on GeSn Growth

The effect of carrier gas on GeSn CVD growth is important and of great significance for the good mixing of precursor gases in a CVD chamber [105,152,153]. In contrast to pure Ge growth, the GeSn CVD growth mechanism has changed due to the introduction of Sn precursors, which have made GeSn CVD growth more complex. In several instances, a thickness reduction or an absence of GeSn occurs when choosing N_2 as the carrier gas; this indicates that the growth rate has already changed and is below the etching rate from HCl. Furthermore, the Sn content of GeSn grown with an N_2 carrier gas is different from that grown with an H_2 carrier gas (Sn% difference is usually approximately 1%; see Figure 12). This Sn content reduction may be mainly attributed to the lower growth rate found when using N_2 as the carrier gas.

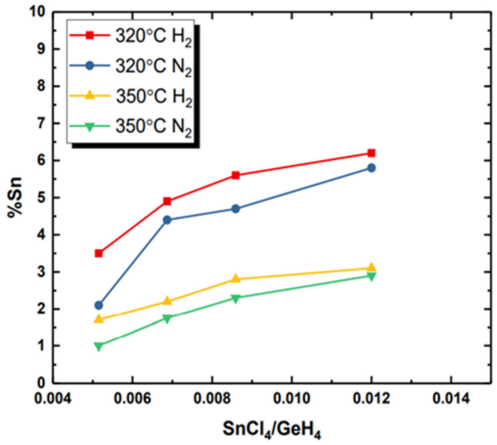

Figure 12. Sn content vs. $SnCl_4/GeH_4$ ratio (growth temperatures: 320 and 350 °C; carrier gases: N_2 and H_2; precursors: GeH_4 and $SnCl_4$). Reproduced from [153], open access by ASU library.

2.3.3. Strain Relaxation Effect on GeSn CVD Growth

F. Gencarelli et al. discovered a composition-dependent strain relaxation mechanism, and they found that high-Sn-content materials show a classical strain relaxation behavior [162]. Their AFM results showed that the island size and density of their low-Sn-content GeSn layers increased with strain relaxation degree (Figure 13) for the following reasons: higher amounts of Sn precursors were needed for high-Sn-content GeSn growth, extra Cl doses were exposed to the surface of GeSn and thus likely avoided Ge–Sn diffusion, Cl atoms could be regarded as the surfactants to mediate the enhancement of island size and density.

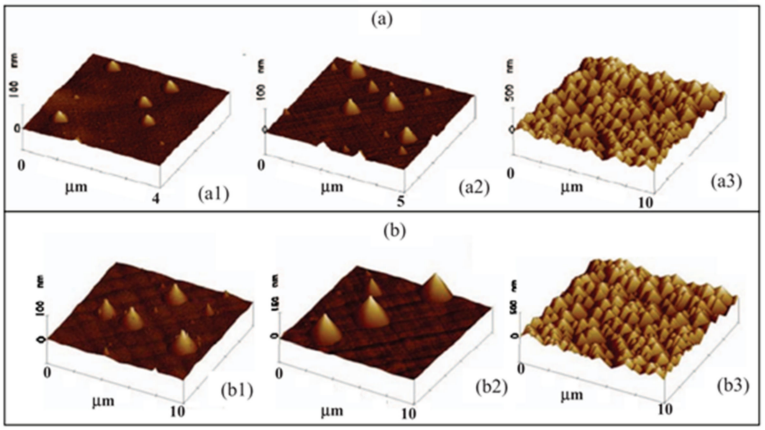

Figure 13. AFM images of (**a**) GeSn with an Sn content of 6.4%; the strain relaxations for (**a1**), (**a2**), and (**a3**) are 8%, 33%, and 75%, respectively. (**b**) GeSn with a strain relaxation of 75%; the Sn contents of (**b1**), (**b2**), and (**b3**) are 12.6%, 8.1%, and 6.4%, respectively. Reproduced with permission from [162], IOP Publishing, 2012.

Later, high-quality GeSn with a world-record high Sn content of 22.3% was crafted after the discovery of strain-relaxation-enhanced (SRE) GeSn CVD growth mechanism [113], thus showing that compressive strain is the primary limiting factor for achieving greater Sn incorporation under an Sn oversaturation condition (Figure 14). In this research, the following growth strategy was proposed: (i) for first GeSn layer growth, they used a growth recipe of 9–12% Sn (the Sn content ranged from 8.8 to 11.9%); (ii) for second GeSn layer growth, they used the same growth recipe, and the $SnCl_4$ flow fraction increased by ~8% compared to the first GeSn layer (the Sn content ranged from 12.5 to 16.5%); and (iii) for third GeSn layer growth, they used the same growth recipe, and the $SnCl_4$ flow fraction increased by ~8% compared to the second GeSn layer. It should be noted that the grading rate of Sn incorporation was well-designed to suppress the growth breakdown. Inspired by the discovery of the SRE GeSn CVD growth mechanism, S. Assali et al. grew a high-quality GeSn layer with 15% Sn using low pressure chemical vapor deposition (LPCVD) in 2018 [115,116].

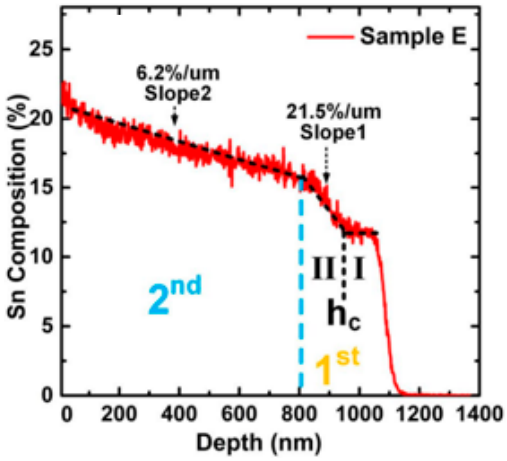

Figure 14. SIMS result for the GeSn sample with an Sn content of up to 22.3% (the maximum Sn contents for regions I, II, and III were 11.9%, 15.5%, and 22.3%, respectively). Reproduced from [113], Springer Nature, open access, 2018.

2.4. Doping for GeSn

Mainstream GeSn doping technologies, such as ion implantation and in situ CVD doping, have been intensively studied for future electronics and photonics applications. Low contact resistivity plays a vital role in the creation of high-performance devices. Table 1 presents a summary of reported B, BF_2^+, and P-doped GeSn via ion implantation in terms of year, institution, Sn content, doping type, doping concentration, activation temperature, and contact metal. Additionally, Tables 2 and 3 present summaries of B-doped GeSn, P-doped GeSn, and As-doped GeSn in terms of year, institution, Sn content, doping type, doping concentration, contact metal, and contact resistivity.

Table 1. Summary of reported B, BF_2^+, and P-doped GeSn via ion implantation in terms of year, institution, Sn content, doping type, doping concentration, activation temperature, and contact metal.

Year	Institution	Sn Content (%)	N-Type	P-Type	Doping Concentration (cm^{-3})	Activation Temperature (°C)	Contact Metal	Ref.
2011	Nagoya University	2–13	——	√	B: 8×10^{19}	350–550	Ni	[163]
2011	CAS-IOS	3	——	√	BF_2^+: ——	400	Al	[164]
2012	NUS and CAS-IOS	2.4	√	——	P: 2.1×10^{19}	400	Al	[165]
2012	NUS and CAS-IOS	4.2	√	√	P: 1×10^{21} BF_2^+: ——	400	Ni	[166]
2012	NUS and CAS-IOS	3–5.3	——	√	BF_2^+: $>1 \times 10^{20}$	300–500	——	[167]
2013	NUS	2.4	√	——	P: 2.1×10^{21}	400	Al	[168]
2013	NUS	4.2	√	√	P: $>1 \times 10^{20}$ BF_2^+: $>1 \times 10^{20}$	400	Ni	[169]
2013	NUS	4.2	√	——	P: ——	450	Ni	[170]
2013	NUS	4.2	√	——	P: ——	400	Ni	[171]

Table 1. *Cont.*

Year	Institution	Sn Content (%)	N-Type	P-Type	Doping Concentration (cm^{-3})	Activation Temperature (°C)	Contact Metal	Ref.
2013	NUS and CAS-IOS	5.3	——	√	BF_2^+: ——	350	Ni and Ni–Pt	[172]
2013	NUS and CAS-IOS	4.1	——	√	BF_2^+: ——	——	——	[173]
2013	Stanford University	7	√	√	P: —— BF_2^+: ——	400	Ti/Ni	[174]
2014	NUS and AM	2.4	√	——	Hot P^+: $>1 \times 10^{20}$	450	Ti/Ni	[175]
2014	NUS and AM	2.6	√	——	P: $>1 \times 10^{20}$	——	——	[176]
2015	CAS-IOS	3.2	√	——	P: 7.64×10^{20}	500	Ni/Al	[177]
2016	Xidian University	4	——	√	BF_2^+: ——	——	Ni	[178]
2016	CAS-IOS	8	——	√	B: ——	300	Ni/Al	[179]
2017	Xidian University	4	——	√	BF_2^+: ——	——	Ni	[180]
2017	National Taiwan University	8	√	——	P: ——	300–350	Ni	[181]
2019	CAS-IOS	6	——	√	BF_2^+: ——	450	Ni/Al	[182]
2020	CAS-IOS	9	√	√	B: —— P: ——	500	Ni Al/Ti/Au	[183]
2020	National Chiao Tung University	2.8	——	√	BF_2^+: ——	400	Al	[184]

2.4.1. Ion Implantation for GeSn

Ion implantation is a widely used technique for doping semiconductor materials, and its advantages include low-temperature operation, precise dose control, good uniformity, and extremely small lateral diffusion. The research and development of GeSn's ion implantation technology is also of great significance for future device application. So far, researchers have carried out extensive research into GeSn ion implantation technology (although most GeSn has been grown in MBE chambers, which are also significant).

Phosphorus has been widely adopted for ion implantation to achieve efficient N-type doping in GeSn layers because its doping concentrations usually ranges from 2.1×10^{19} to 2.1×10^{21} cm^{-3}. For the P-type doping, there are two options: boron and BF_2^+. The highest P-type doping concentration can reach up to 1×10^{20} cm^{-3}.

2.4.2. In Situ GeSn CVD Doping

Optoelectronic devices, such as GeSn LEDs, GeSn lasers, and GeSn detectors, generally need highly doped GeSn for efficient carrier recombination and low contact resistance. Electronic devices, such as GeSn MOSFETs, GeSn TFETs, GeSn FinFETs, and GeSn GAAFETs (gate-all-around), require lower ohmic contacts, higher dopant concentrations, and selective doping. The use of in situ doping technology for GeSn is an attractive route for improving the performance of optoelectronic and electronic devices because it enables the doping of GeSn at low temperatures with a high doping efficiency and selective doping. Indeed, GeSn transitions from an indirect to direct bandgap material with an Sn content as high as 10%, and this property has led to research interest in Si-based, high-efficiency light sources. The first electrically injected GeSn lasers were recently demonstrated with Sn contents of 11% and 15%. It is definitely true that we require better solutions to create direct bandgap, high-quality doped GeSn, and the selection of an appropriate reaction doping gas and the optimization of epitaxial process are vital for this purpose. To this end, the growth of B-doped GeSn, P-doped GeSn, and As-doped GeSn using CVD has been

reported by several institutions, as summarized in Table 2. However, there are several key points to consider: (I) Sn loss occurs for B-doped GeSn CVD growth, indicating that there is a competition between Sn and B atoms [150,185]; (II) excess partial pressure for PH_3 contributes to poor material quality due to P segregation; (III) B_2H_6 partial pressure has no degradation effect on material quality, though it increases the activation doping concentration; (IV) more P could be incorporated into Ge and GeSn by using high order precursors; (V) boron δ-doping layers are helpful for highly doped GeSn growth, and the maximum B concentration can reach up to 1×10^{20} cm^{-3}; and (VI) the doping efficiency of As-doped GeSn is better than that of P-doped GeSn [110].

Table 2. Summary of reported B-doped GeSn, P-doped GeSn, and As-doped GeSn in terms of year, institution, Sn content, doping type, doping concentration, and contact metal.

Year	Institution	Sn Content (%)	N-Type	P-Type	Doping Concentration (cm^{-3})	Contact Metal	Ref.
2009	ASU	2	√	——	P: 1×10^{20}	Cr/Au	[57]
2011	IMEC	8	——	√	B: 1.7×10^{19}	——	[150]
2013	KTH Royal Institute of Technology	9.4	√	√	B: 5×10^{18} P: 1×10^{20}	——	[186,187]
2016	PGI 9	8 and 11	√	√	B: 2×10^{19} P: 1×10^{20}	——	[188]
2016	PGI 9	8.5 and 15	√	√	B: 4×10^{18} P: 7.5×10^{19}	——	[189]
2017	ASM	9	√	——	As: $>2 \times 10^{20}$	——	[110]
2017	ASM and IMEC	1.4	——	√	B: 2×10^{20}	——	[190]
2018	National Taiwan University	10	√	√	B: Sn loss P: No Sn loss	——	[191]
2019	National Taiwan University	>12	——	√	B: $>1 \times 10^{21}$	Ti	[192]
2019	Leti	10 and 15	√	——	P: 5×10^{20}	——	[193]
2020	National Taiwan University	2, 4.7, and 13	——	√	B: 2.1×10^{20} for 2% Sn	Ti	[194]
2020	Leti	6.5	√	√	B: 5.2×10^{19} P: 2.2×10^{20}	——	[195]
2020	National Taiwan University	4.7	——	√	B: 1.9×10^{20}	Ti	[196]
2021	National Taiwan University	9	√	——	P:1.3×10^{20}	Ni	[197]

Table 3. Summary of reported B-doped GeSn, P-doped GeSn, and As-doped GeSn in terms of institution, Sn content, doping type, doping concentration, and contact metal.

Year	Institution	Sn Composition (%)	N-Type	P-Type	Doping Concentration (cm^{-3})	Contact Metal	Contact Resistivity ($\Omega \cdot cm^2$)	Ref.
2014	Institute of Microelectronics, Chinese Academy of Sciences	4	——	——	——	Ni	——	[187]
2018–2020	National Taiwan University	9	√	——	P:1.3 × 10^{20}	Ni	1.5 × 10^{-7}	[191,192,194,196,197]
		2, 4.7, and 13	——	√	B: 2.1 × 10^{20} for 2% Sn	Ti	4.1 × 10^{-10} for 2% Sn	
		4.7	——	√	B: 1.9 × 10^{20}	Ti	1.1 × 10^{-9}	
		>12	——	√	B: >1 × 10^{21}	Ti	4.1 × 10^{-10}	
		10	√	——	P: 1.3 × 10^{20}	Ni	1.1 × 10^{-7}	
		9	√	√	B: 4 × 10^{17} P: ——	Ni	3.8 × 10^{-8}	
2020	Leti	6.5	√	√	B: 5.2 × 10^{19} P: 2.2 × 10^{20}	——	——	[195]
2020	Université de Montréal	11	√	√	B: × 10^{19} As: × 10^{20}	——	——	[198]
2019	University College Cork	8	——	——	——	Ti, Ni, and Pt	——	[199]
2013–2019	NUS	5, 7, and 8	——	√	Ga: 3.4 × 10^{20}	Ti	4.4 × 10^{-10} for 7% Sn	[165–173,200–203]
		8.5	——	√	Ga: 3.2 × 10^{20}	——	——	
		5	——	√	Ga: ——	Ti	9.3 × 10^{-10}	
		5	——	√	Ga: ——	Ni	2 × 10^{-10}	
		5	——	√	Ga: 1.6 × 10^{20}	Ni	1.4 × 10^{-9}	
		2.4	√	——	P: 2.1 × 10^{19}	Al	4 × 10^{-3}	
2012	NUS and CAS-IOS	5.3	——	√	BF_2^+: 5.7 × 10^{20}	Ni	1.6 × 10^{-5}	[204]
2015–2020	CAS-IOS	7	√	——	Sb: 5 × 10^{20}	Ni	1.3 × 10^{-6}	[179,182,183,205,206]
		8	√	——	Sb: 3 × 10^{19}	Ni/Al	6.2 × 10^{-5}	
		7	√	——	Sb: 5 × 10^{19}	Ni	1.3 × 10^{-6}	
		3.2	√	——	P: 7.64 × 10^{19}	Ni/Al	2.26 × 10^{-4}	
		7	——	√	P: 2.44 × 10^{19}	Ni/Al	1.9 × 10^{-6}	

2.4.3. GeSn Ohmic Contact

Among the summarized GeSn contact works is that of Henry. H. Radamson et al., who proposed a novel method to improve the thermal stability of the Ni–GeSn contact. It is well-known that carbon stabilize NiSiGe materials, so after GeSn growth, they implanted C into GeSn. In Figure 15, we can see that the NiGeSn film with C was more uniform than the NiGeSn film without C. Characterization results indicated that the presence of C not only led to the improved thermal stability but also tended to change the preferred orientation of NiGeSn [187]. A comparison work with different contact metals (10 nm of Ni, Ti, and Pt) [199] showed that Ni–GeSn was the most promising candidate due to its low sheet resistance and low formation temperature (below 400 °C). Moreover, Pt–GeSn showed better behavior in terms of thermal stability compared to Ni–GeSn and Ti–GeSn. Because Sn loss occurs during B-doped GeSn CVD growth, it is still challenging to create low contact resistivity p-type GeSn contacts with high Sn contents, a challenge that is particularly critical for GeSn lasers and GeSn TFETs [207,208].

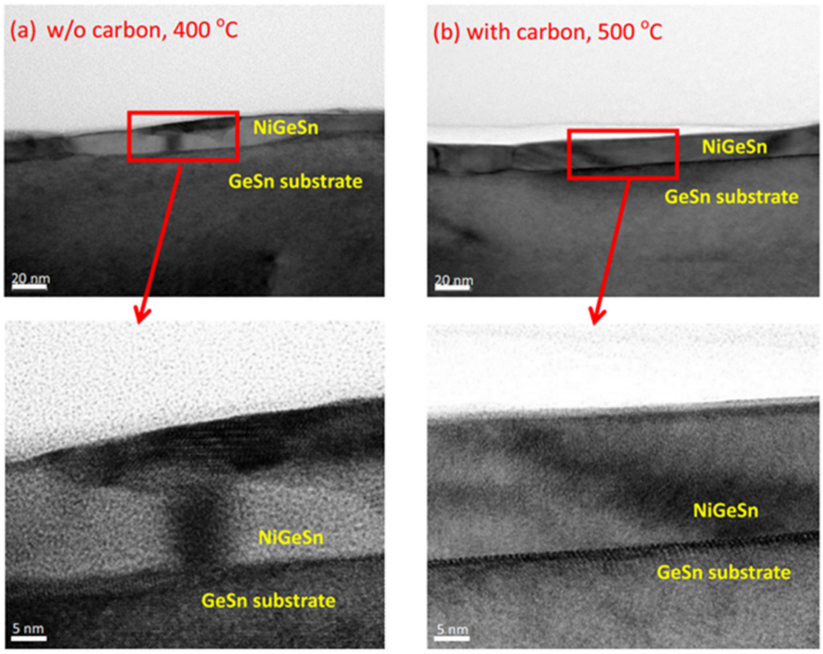

Figure 15. TEM images for Ni–GeSn interface (**a**) annealing at 400 °C without C and (**b**) annealing at 400 °C with C. Reproduced from [187], IOP Publishing, open access, 2015.

3. Research Progress for GeSn Detectors

3.1. GeSn Photoconductive Detector

Photoconductive detector, which can also be defined as metal–semiconductor–metal (MSM) detector, is regarded as the simplest structure to achieve detection. In this type of structure, two Schottky junctions are designed and the total layer structure does not require any doping. Therefore, it can only work at a high bias voltage due to the existence of high contact resistance. However, the capacitance of a photoconductive detector is quite low, which is helpful for high-speed detection. Based on the photoconductive structure, researchers have put great effort into GeSn photoconductive detectors (Figure 16). Table 4 shows the reported performance levels of GeSn photoconductive detectors grown by CVD technology.

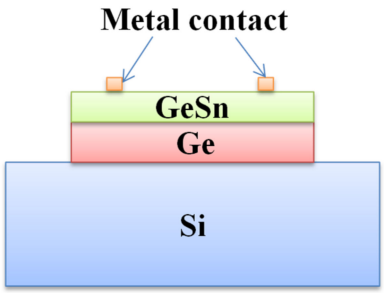

Figure 16. Cross-sectional schematic of a device structure for a GeSn photoconductive detector.

As previously reported, IMEC mastered low-cost and commercially available cutting-edge GeSn growth technology in 2011 (Ge_2H_6/GeH_4 precursor combination) [151]. Subsequently, they further grew a GeSn/Ge MQWs structure, and they also fabricated a photoconductive detector [58]. In 2014, Benjamin, R. Conley et al. reported the temperature-dependent spectral responses and detectivity of GeSn photoconductors with Sn contents ranging from 0.9 to 7% [59]. For a GeSn photoconductor with 7.0% Sn, a maximum wavelength response of 2100 nm was achieved. Experimental results showed that low-temperature responsivity was two orders of magnitude higher than room-temperature responsivity at 1550 nm, and the maximum specific detectivity was 1×10^9 cm·$Hz^{1/2}$/W

at 77 K. In the same year, Benjamin, R. Conley et al. further extended the spectral response using a GeSn layer with 10% Sn [60]. The room-and low-temperature (77 K) wavelength cutoffs for the GeSn detector were found to be 2400 and 2200 nm, respectively. Maximum peak responsivity was observed as 1.63 A/W at 77 K due to photoconductive gain. More importantly, the specific detectivity was increased by about five times compared to the previously reported result (a GeSn photoconductor with 7.0% Sn), indicating that the material quality of the GeSn layer with 10% Sn was greatly improved (Figure 17).

Table 4. Summary of reported GeSn photoconductive detectors in terms of Sn content, GeSn thickness, device structure, wavelength cutoff, and responsivity.

Year	Sn Composition	GeSn Thickness	Structure	Cutoff	Responsivity	Ref.
2012	9%	13 or 20 nm	GeSn/Ge 3QWs	2200 nm	0.1 A/W at 5 V	[58]
2014	0.9%	327 nm	Bulk	1800 nm	——	[59]
	3.2%	76 nm		1900 nm	——	
	7.0%	240 nm		2100 nm	0.18 A/W at 10 V	
2014	10%	95 nm	Bulk	2400 nm	1.63 A/W at 50 V	[60]
2015	10%	95 nm	Bulk	2400 nm	0.26 A/W	[61]
2019	12.5%	140 and 660 nm	Bulk	2950 nm	2 A/W	[63]
	15.9%	250 and 670 nm		3200 nm	0.044 A/W	
	15.7%	165, 585, and 254 nm		3400 nm	0.0072 A/W	
	17.9%	310, 550, and 260 nm		3350 nm	0.0038 A/W	
	20%	450 and 950 nm		3650 nm	0.0067 A/W	
	22.3%	380 and 830 nm		3650 nm	0.0032 A/W	

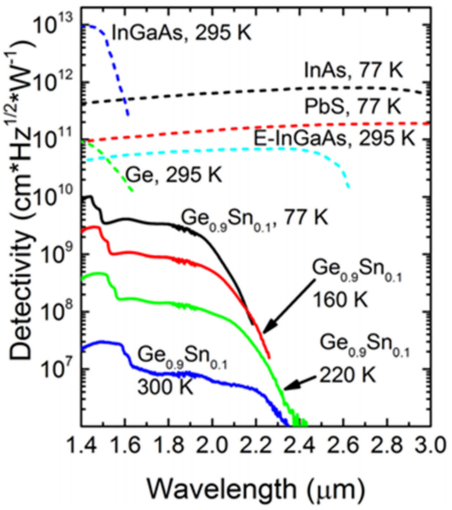

Figure 17. Specific detectivity for a $Ge_{0.9}Sn_{0.1}$ photoconductive detector at temperatures of 77, 160, 220, and 300 K. Reproduced from [60], OSA Publishing, open access, 2014.

In 2019, Huong Tran et al. reported a GeSn photoconductor with high Sn contents (the maximum Sn contents of the top GeSn layer were 12.5%, 15.9%, 15.7%, 17.9%, 20%, and 22.3%) [63]. As the Sn content increased, the cutoff wavelength shifted toward longer wavelength due to the bandgap shrinkage. From 77 to 300 K, the cutoff wavelengths were 3200–3650 nm for the GeSn photoconductor with 22.3% Sn. It is worth noting that this D* value was superior to that of a PbSe detector at the given wavelength range and was comparable to that of a commercial extended-InGaAs detector (4×10^{10} cm·$Hz^{1/2}$·W^{-1}) at the same wavelength range (Figure 18). Even at 300 K, the passivated device showed better results D* than the PbSe detector from 1500 to 2200 nm.

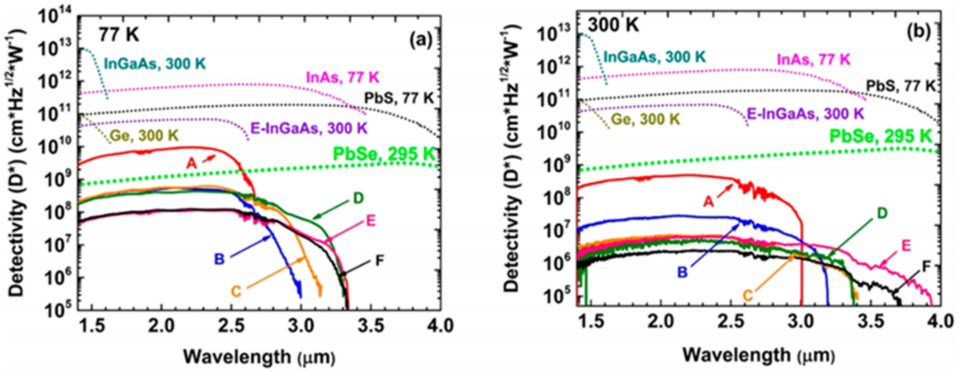

Figure 18. Specific detectivity for a GeSn photoconductive detector at the temperatures of (**a**) 77 K and (**b**) 300 K (the Sn contents for samples A–F were 12.5%, 15.9%, 15.7%, 17.9, 20.0%, and 22.3%, respectively). Reproduced with permission from [63], American Chemical Society, 2019.

To enable a comprehensive overview of the use of GeSn photoconductive materials for infrared detection applications, Figure 19 illustrates the Sn content vs. cutoff wavelength for reported GeSn photoconductive detectors. For GeSn with an Sn incorporation of 0.9–12.5%, the photoconductive detector wavelength coverage was found to range from 1800 to 2950 nm, indicating that GeSn with Sn contents of up to 12.5% or 13% is very promising for SWIR applications. For GeSn with an Sn incorporation of 15.9–22.3%, the photoconductive detector wavelength coverage was found to range from 3200 to 3650 nm, suggesting potential mid wavelength infrared (MWIR) applications. For wavelengths from 3650 to 5000 nm, no detectors have been reported. However, GeSn photoconductive detector performance is limited by current growth technology and Sn distribution uniformity in total layer structures, which causes a low responsivity (the responsivity values are listed in the table above).

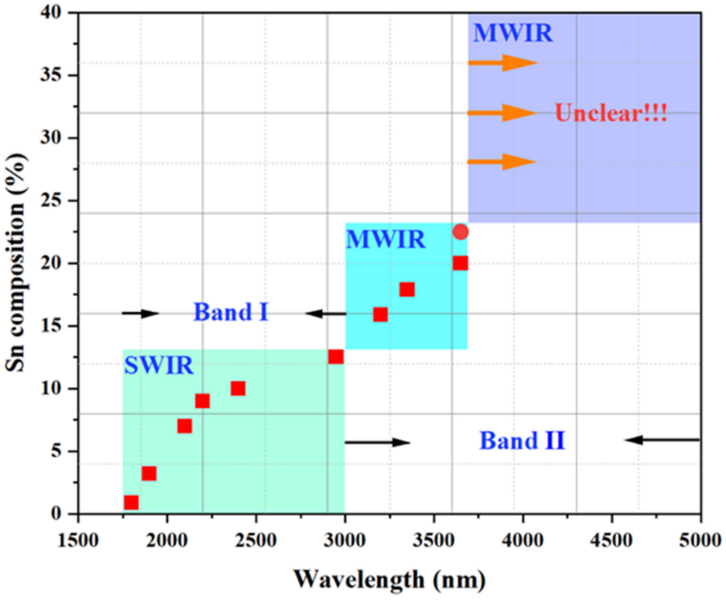

Figure 19. Sn content vs. wavelength of a GeSn photoconductive detector, indicating that GeSn is a promising absorber in SWIR and MWIR detection applications.

3.2. GeSn PIN Detector

The PIN detector is the most common and widely used detector type for Si-based optoelectronics applications. One side of a PIN detector device is for p-type doping, and the other side is for n-type doping; as such, the built-in electric field is able to locate the intrinsic region [18]. A typical cross-sectional schematic diagram of a GeSn PIN detector

is shown in Figure 20, and the major device performance values for reported GeSn PIN detectors are summarized in Table 5.

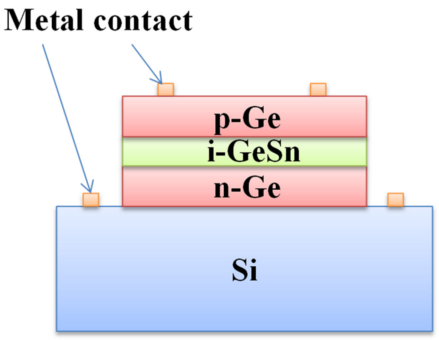

Figure 20. Cross-sectional schematic of typical device structure for a GeSn detector.

Table 5. Summary of reported GeSn PIN detectors in terms of Sn content, GeSn thickness, device structure, wavelength cutoff, and responsivity.

Year	Sn Composition	GeSn Thickness	Structure	Cutoff	Responsivity	Ref
2009	2%	350 nm	n–GeSn/i–GeSn/P-Si	1750 nm	-	[57]
2016	7%	200 nm	p–Ge/i–GeSn/n–Ge	2200 nm	0.15 A/W at 1 V	[62]
	10%	200 nm		2600 nm	0.07 A/W at 1 V	
2018	11%	700 nm	p–Ge/p–GeSn/i–GeSn/n–GeSn/n–Ge	2650 nm	0.32 A/W	[65]
2019	8%	25 nm	p^+–Ge/i-QWs/n^+–Ge	2000 nm	0.2 A/W	[66]

In 2009, Jay Mathews et al. demonstrated the first GeSn photodetector with 2% Sn content; 350 nm $Ge_{0.98}Sn_{0.02}$ was directly grown on a B-doped Si (100) substrate in an UHVCVD system (the carrier concentration in the Si wafer was 4.3×10^{19} cm^{-3}) [57]. Three cycles of post-growth annealing were carried out to decrease the TDDs in $Ge_{0.98}Sn_{0.02}$. Afterwards, n-doped $Ge_{0.98}Sn_{0.02}$ was further deposited, and its carrier concentration was found to be approximately 7.5×10^{19} cm^{-3}. Using the abovementioned layer structure, a circular GeSn photodetector was fabricated. To evaluate the quantum efficiency of the $Ge_{0.98}Sn_{0.02}$ photodetector, the circular mesa was continuously illuminated via a halogen source and 1270, 1300, 1550, and 1620 nm lasers. The $Ge_{0.98}Sn_{0.02}$ detector quantum efficiencies were higher than those in comparable pure Ge device designs processed at low temperatures (Figure 21). Additionally, the wavelength cutoff was extended to at least 1750 nm, which means that a GeSn photodetector with 2% Sn content can cover the entire telecommunication band.

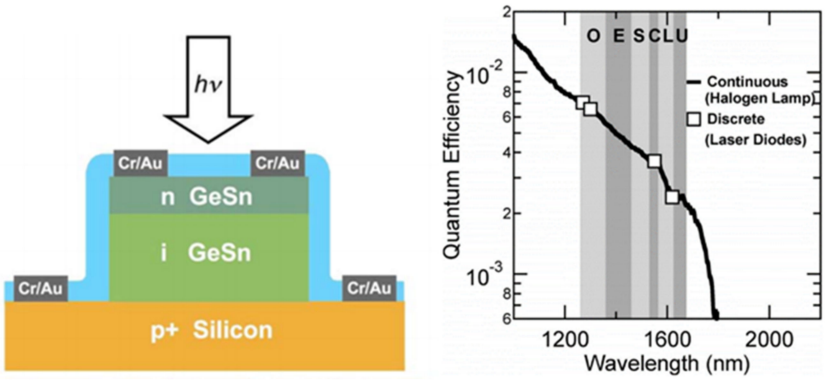

Figure 21. Cross-sectional schematic of a GeSn photodetector and its quantum efficiency as a function of wavelength. Reproduced with permission from [57], AIP Publishing, 2009.

In 2018, Huong Tran et al. fabricated GeSn photodetectors with 700 nm thick GeSn layers using the p–Ge/p–$Ge_{0.91}Sn_{0.09}$/i–$Ge_{0.89}Sn_{0.11}$/n–$Ge_{0.89}Sn_{0.11}$/n–Ge layer structure (all layers were grown by RPCVD) [65]. In order to obtain detailed and accurate external reading of quantum efficiency, all GeSn photodetectors were illuminated with a 2000 nm laser. Room-temperature peak responsivity and external quantum efficiency were measured to be 0.32 A/W at 2000 nm and 20%, respectively. When the GeSn detector was illuminated by a 1550 nm laser, its external quantum efficiency reached up to 22%. Different from the previously reported thin film photoconductor, the thick film photoconductor showed an extended wavelength cutoff (2650 nm) due to the reduced strain relaxation and enhanced light absorption in the thick GeSn film. Nevertheless, the peak specific detectivity for the GeSn detector was compared to other commercial infrared detectors at a wavelength range from 1400 to 3000 nm, which showed that peak specific detectivity of the GeSn detector at 2000 nm was only one order of magnitude lower than that of the extended-InGaAs detector (Figure 22). To improve device performance, Xu S, et al. attempted to create a GeSn/Ge MQW detector [67,68], a GeSnOI detector [69], and a photon-trapping microstructure GeSn/Ge MQW detector [209].

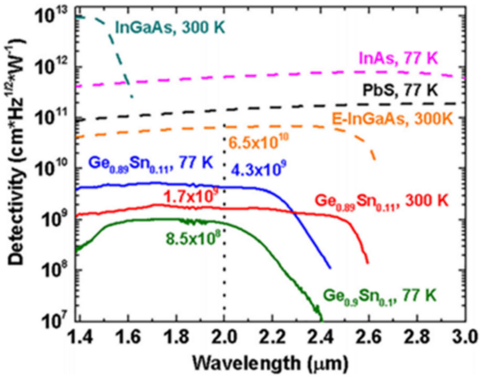

Figure 22. Specific detectivity for a $Ge_{0.89}Sn_{0.11}$ photodetector at the temperatures of 77 and 300 K. Reproduced with permission from [65], AIP Publishing, 2018.

Figure 23 summarize the Sn content vs. cut-off wavelength for a reported GeSn PIN detector. For GeSn with an Sn incorporation of 2–11%, the PIN detector wavelength coverage was found to range from 1750 to 2650 nm, indicating that a GeSn PIN detector is very promising for SWIR applications. Due to the limitations of growth technology, PIN detectors at wavelengths from 2650 to 5000 nm have yet to be reported.

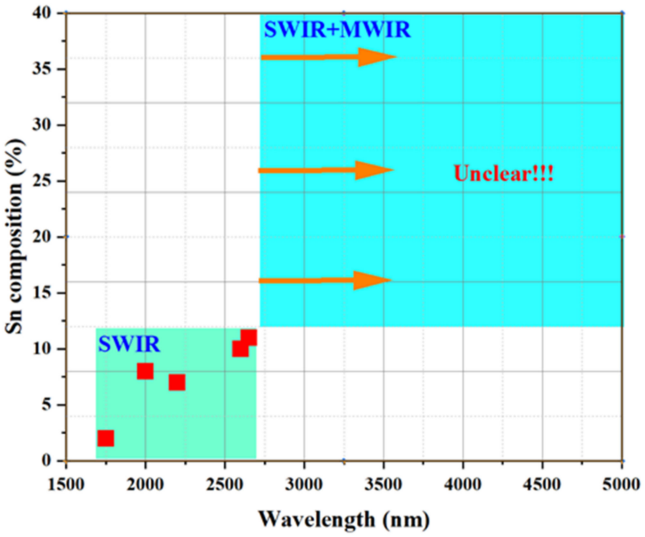

Figure 23. Sn content vs. cut-off wavelength of the GeSn PIN detector.

4. Research Progress for GeSn Lasers

Since Si-based high-efficiency light sources comprise the technical bottleneck for Si-based monolithic optoelectronic integration, researchers have conducted extensive research into Ge and GeSn lasers. Ten years ago, the rapid development of the GeSn CVD growth technique enabled researchers from MIT to demonstrate optically injected and electrically injected Ge lasers at room temperature. The lasing thresholds of these laser devices were very high, which made it difficult to achieve efficient lasing. As a result, more attentions has been paid to the GeSn material due to its direct bandgap property. In this section, we review the latest research on GeSn lasers with different optical cavities, as well as their device performance.

4.1. Optically Injected GeSn Lasers

4.1.1. Optically Injected GeSn Laser with FP Cavity

Based on the GeSn optical gain medium, the world's first optically injected FP cavity GeSn laser was demonstrated at a low temperature [70]. The typical threshold power densities of FP cavity GeSn lasers with cavity lengths of 1 mm, 500 μm, and 250 μm were maintained between 300 and 330 kW/cm^2 (Figure 24a). When the optically injected power density was above its threshold power density, the full width half maximum of the optical emission spectrum was dramatically reduced and the intensity was significantly increased; when the optical injection power density increased to 650 kW/cm^2, the threshold curve tended to be flat (possibly due to a self-heating effect) (Figure 24a). When the optically injected power density increased to 1000 kW/cm^2, the maximum lasing temperature for the GeSn laser with 12% Sn content was 90 K. Figure 24b shows high-resolution laser spectra that indicate the performance of a GeSn laser under multi-mode operation.

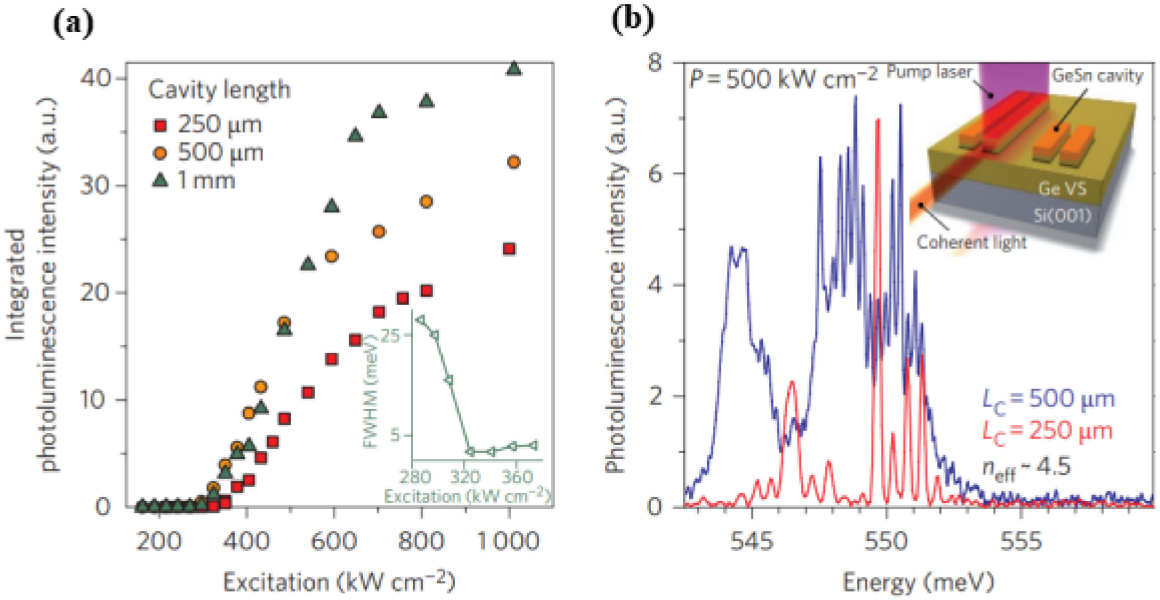

Figure 24. (**a**) Integrated PL intensity vs. excitation power density for a GeSn FP cavity laser with different cavity lengths; (**b**) high-resolution laser spectra for a GeSn laser with cavity lengths of 250 and 500 μm. Reproduced with permission from [70], Springer Nature, 2015.

In 2017, Joe Margetis et al. systematically studied the performance of optically injected GeSn lasers with different Sn contents [73]; the Sn contents of samples A–G were 7.3%, 9.9%, 11.4%, 14.4%, 15.9%, 16.6%, and 17.5%, respectively, and the maximum operation temperatures of samples A–G were 77, 110, 140, 160, 77, 140, and 180 K, respectively (Figure 25). Except for sample A (lower Sn content) and sample E (poor material quality), the samples could be lased at 140 K. It is worth noting that the maximum operation temperature of samples D and G were 160 and 180 K, respectively. The results showed

that the operating temperature of the optically injected GeSn laser was closely related to the Sn content of GeSn, and the GeSn lasers with higher Sn contents possessed higher operating temperature (except for sample F because of its poor material quality). Therefore, increasing the Sn content in GeSn can effectively increase the operating temperature of the laser device. From the theoretical point of view, the main factors that affect the performance of laser devices are material gain, active layer thickness, device surface roughness, and non-radiative recombination. Therefore, there are differences in the operating temperatures of GeSn laser devices with different Sn contents.

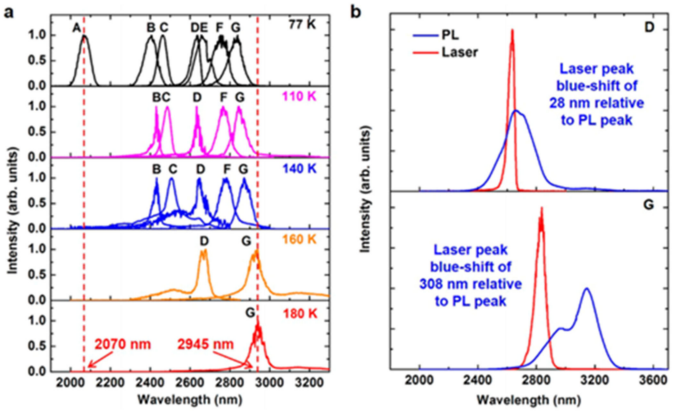

Figure 25. (**a**) GeSn laser spectra for samples A–G; (**b**) comparison of the PL and laser spectra of samples D and G. Reproduced with permission from [73], American Chemical Society, 2017.

Thanks to the discovery of the GeSn strain-relaxation-enhanced growth mechanism [88], researchers were able to increase the Sn content of GeSn to 22.3%. In this layer structure, the GeSn buffer layer is grown with a nominal recipe for 11% GeSn. When the thickness of the 11% GeSn layer reaches its critical thickness, internal strain in the GeSn layer gradually relaxes and more Sn atoms can be incorporated into the Ge lattice. Experimental results showed that the strain relaxation growth mechanism could lead to high-Sn-content GeSn alloys (higher than 22.3%). Later, Wei Dou et al. reported an optically injected bulk GeSn laser with an Sn content of up to 22.3% [75]; both 1064 and 1950 nm pulsed lasers were used for optical injection, and the maximum operating temperatures were 150 and 180 K, respectively (Figure 26).

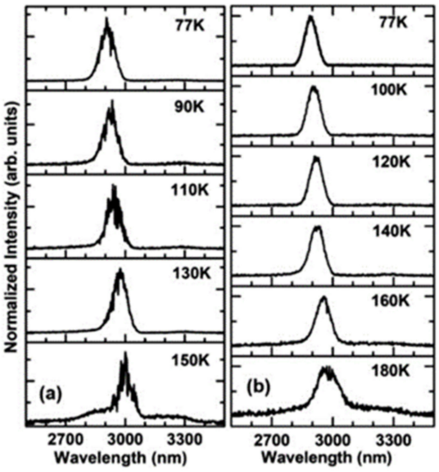

Figure 26. Temperature-dependent lasing spectra for a bulk GeSn laser with an Sn content of up to 22.3%; the optical injection sources were (**a**) a 1064 nm pulsed laser and (**b**) a 1950 nm pulsed laser. Reproduced from [75], OSA Publishing, open access, 2018.

In 2019, Yiyin Zhou et al. researched optically injected GeSn lasers (an Sn content of 20%) with different waveguide widths [76]; 1064 and 1950 nm lasers were used for pulsed optical injection characterization (Figure 27). They concluded that the operation temperature for sample A was lower than those of the other samples (the laser operation temperatures under 1064 and 1950 nm pulsed injection were 120 and 140 K, respectively). Moreover, the threshold for sample A was relatively larger than those of the other samples (at 77 K, the thresholds under 1064 and 1950 nm optical pulsed injection were 516 and 132 kW/cm^2, respectively). When the sample width was wider than 20 μm, the operation temperatures of the laser devices could be increased to 260 and 270 K under 1064 and 1950 nm optical pulsed injection, respectively. The reasons for this are as follows: (i) compared with the side wall surface recombination, free carrier absorption loss and non-radiative recombination were the dominant losses at higher temperatures; (ii) the stripe-shaped optical injection light beam had a Gaussian distribution, which may have resulted in absorption occurring in the middle of a wider waveguide (less absorption at the edge of the waveguide); and (iii) the optical confinement factor for sample D was lower, which led to a higher threshold.

1064 nm pumping	A (5 μm)	B (20 μm)	C (100 μm)	D (planar)
threshold @ 77 K (kW/cm^2)	516	384	356	330
peak position @ 77 K (nm)	2641	2802	2965	2961
max operating temp (K)	120	260	260	260
threshold @ max operating temp (kW/cm^2)	903	2990	6055	9587
peak position @ max operating temp (nm)	2970	3432	3444	3334
1950 nm pumping	**A (5 μm)**	**B (20 μm)**	**C (100 μm)**	**D (planar)**
threshold @ 77 K (kW/cm^2)	132	88	47	74
peak position @ 77 K (nm)	2703	3022	3272	2997
max operating temp (K)	140	270	270	270
threshold @ max operating temp (kW/cm^2)	364	886	796	1105
peak position @ max operating temp (nm)	2780	3414	3462	3354

Figure 27. Summary of laser performance under 1064 and 1950 nm pulsed laser injection (the cavity widths for samples A, B, C, and D were 5 μm, 20 μm, 100 μm, and planar, respectively). Reproduced with permission from [76], ACS Publishing, 2019.

The simplest optical cavity is that of Fabry–Pérot, which consists of two parallel reflecting surfaces that allow coherent light to travel through the whole cavity. Due to the directness difference between GeSn alloys with different contents, we summarize the reported operation temperatures for GeSn with different Sn contents in Figure 28. Operation temperatures were found to increase with more Sn incorporation, indicating that operation temperature is closely related to the directness of GeSn. Different from narrow bulk devices, broad bulk devices (with a cavity width greater than 20 μm) possess higher operation temperatures, possibly due to the following two reasons: (1) they have higher optical gains, and (2) they are wider and thus have higher optical injection efficiencies. However, the operation temperature for a GeSn laser with 22.3% Sn incorporation was found to be the same as that of a GeSn laser with 17.5% Sn incorporation, which means that there were many point defects in the high-Sn-content GeSn layer. For clarification, we also summarize the devices performance for the published FP cavity optically pumped GeSn laser (Table 6).

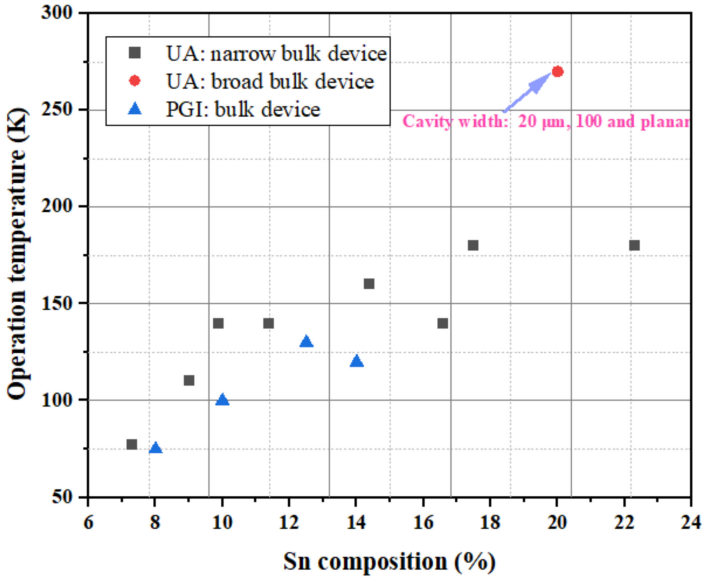

Figure 28. Maximum operation temperature vs. Sn content for optical pumped FP cavity GeSn laser (under pulsed 1064 nm laser) [70,74–76].

Table 6. Summary of the reported optically pumped FP cavity GeSn lasers in terms of structure, Sn content, thickness, cavity width, pumping laser, maximum operation temperature (T_{max}), and threshold.

Year	Structure	Sn (%)	Thickness (nm)	Cavity Width (μm)	Pumping	T_{max} (K)	Threshold (kW/cm^2)	Ref
2015	Bulk	12.6	560	5	Pulsed 1064 nm	90	1000 at 90 K 325 at 20 K	[70]
2016	Hetero	11	260 and 760	5	Pulsed 1064 nm	110	68 at 10 K 166 at 90 K 398 at 110 K	[71]
2017	Bulk	7.3	210 and 680	5	Pulsed 1064 nm	77	300 at 77 K	[73]
		9.9	280 and 850			140	117 at 77 K	
		11.4	180 and 660			140	160 at 77 K	
		14.4	250 and 670			160	138 at 77 K	
		15.9	210 and 450			77	267 at 77 K	
		16.6	160, 680, and 290			140	150 at 77 K	
		17.8	310, 550, and 260			180	171 at 77 K	
2018	Bulk	22.3	380 and 830	5	Pulsed 1064 nm	150	203 at 77 K 609 at 150 K	[75]
					Pulsed 1950 nm	180	137 at 77 K	
2018	QWs	13.8	22 (4×)	——	Pulsed 1950 nm	20	——	[83]
		14.4	31 (4×)	——		90	25 at 10 K 480 at 90 K	
2019	Bulk	20	450 and 970	5	Pulsed 1064 nm	120	516 at 77 K	[76]
				20		260	384 at 77 K	
				100		260	356 at 77 K	
				planar		260	330 at 77 K	
				5	Pulsed 1950 nm	140	132 at 77 K	
				20		270	88 at 77 K	
				100		270	47 at 77 K	
				planar		270	74 at 77 K	

4.1.2. Optically Injected GeSn Laser with WGM Cavity

In 2016, Daniela Stange et al. realized a self-suspending microdisk GeSn laser for the first time [74] (Figure 29). The laser spectrum is shown in Figure 30. It can be seen in the figure that the maximum working temperatures of samples A and B were 80 and 140 K, respectively. Compared with sample B, the lasing spectrum of sample A was blue-shifted

due to its higher content. Although the operation temperature for sample A was lower than that of sample B, the threshold for sample A was lower than that of sample B (the thresholds of samples A and B were 125 and 220 kW/cm^2 at 50 K, respectively).

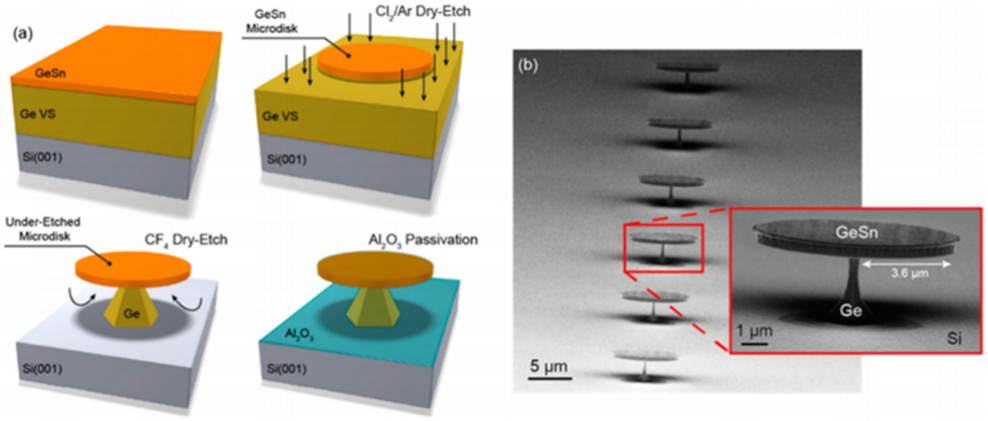

Figure 29. (**a**) Process flow for GeSn microdisk; (**b**) SEM image of GeSn microdisk with an Sn content of 12.5% (diameter was 8 μm). Reproduced with permission from [74], American Chemical Society, 2016.

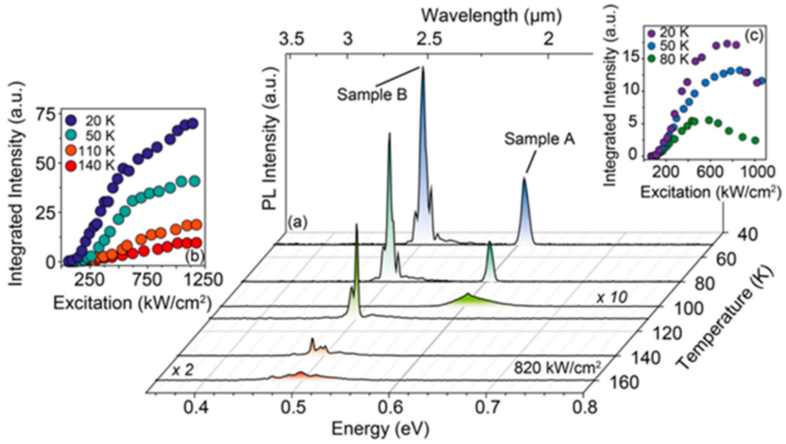

Figure 30. (**a**) Temperature-dependent lasing spectra for samples A and B (the Sn contents for samples A and B were 8.5% and 12.5%, respectively); (**b**,**c**) L–L curves for samples A and B, respectively. Reproduced with permission from [74], American Chemical Society, 2016.

In 2020, Anas Elbaz et al. reported a CW optically injected GeSn microdisk laser with a low Sn content for the first time [80]. Compared with high-Sn-content GeSn, low-Sn-content GeSn has fewer internal point defects and better material quality. After its growth, a low-Sn-content GeSn layer was transferred to an Si substrate with SiN and Al layers. Then, the Si substrate, Ge buffer layer, and defective GeSn layers are removed; only 40 nm, high-quality, low-Sn-content GeSn was left. Finally, the transferred GeSn layer was patterned into independent GeSn/SiN microdisks supported by Al microdisk pillars (Figure 31). The lasing spectrum in Figure 31 shows the continuous wave light injection laser spectrum of a GeSn microdisk with a diameter of 7 μm at 25 K: below the threshold, a light emission spectrum with a wide half-width (red line) was obtained under an optical injection power of 0.5 mW; above the threshold, lasing emission characteristics were obvious under the optical injection power of 6.4 mW. Under the pulsed optical injection and CW light injection, the maximum operating temperatures of the laser device were 90 and 50 K, respectively.

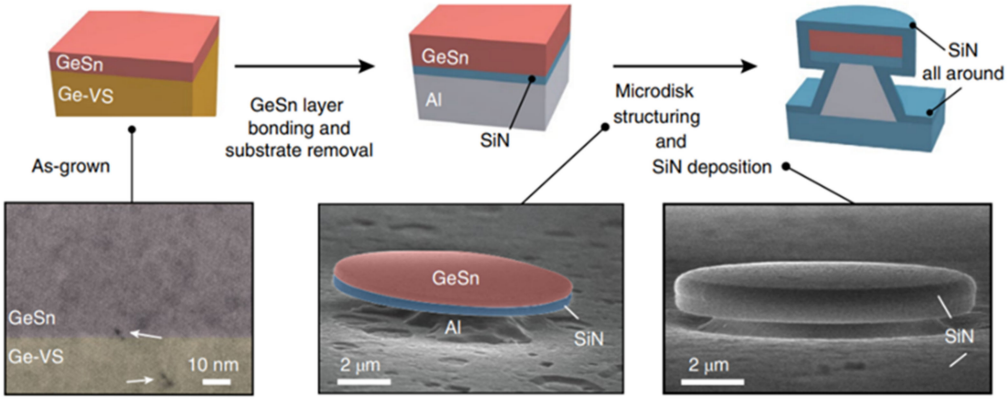

Figure 31. Fabrication process for a GeSn microdisk laser with SiN_x all-around. Reproduced with permission from [80], Springer Nature, 2020.

In 2020, Anas Elbaz et al. created an optically injected GeSn microdisk laser after proper defect management [81,82], indicating that the threshold was greatly reduced compared to that of a GeSn microdisk laser without defect management (the lasing threshold reduction was 1 order of magnitude higher compared to examples in the literature). They also found that the maximum lasing temperature for the optically injected GeSn microdisk laser, with Sn contents ranging from 7% to 10.5%, only weakly depended on Sn content. Apart from the directness of the GeSn active region, the experimental results indicated that nonradiative recombinations and point defects are the main obstacles for high-temperature lasing (Figure 32).

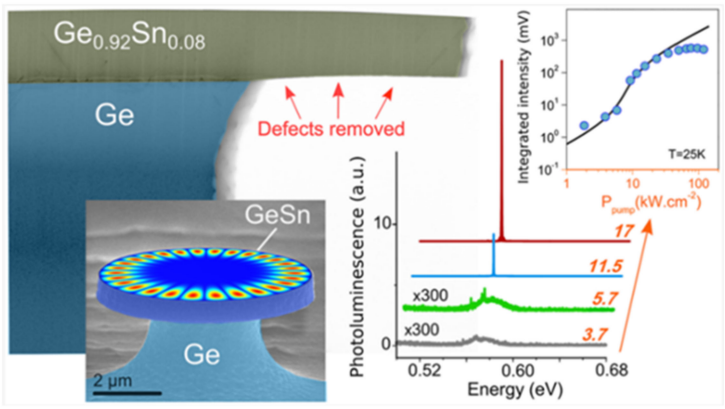

Figure 32. GeSn microdisk laser with removed defects under the disk. Reproduced with permission from [82], American Chemical Society, 2020.

The abovementioned GeSn microdisk laser results show that both pulsed and CW injection have been achieved (Table 7). Especially for CW lasing, this is the most direct evidence to verify that GeSn can withstand a CW injection test. To gain a better understanding of GeSn microdisk lasers, we summarize the operation temperatures for GeSn lasers with different Sn contents in Figure 33. For the pulsed injection, the operation temperature for the GeSn microdisk laser followed a similar trend to that of an FP cavity GeSn laser (the operation temperature increased with Sn content). However, the operation temperature for the heterostructure and quantum well GeSn laser was lower than that of bulk laser, suggesting that there is still room to improve the operation temperatures of heterostructure and quantum well lasers. For CW injection, it seems that operation temperature enhancement is not that sensitive to Sn content, though it brings efficient heat dissipation.

Table 7. Summary of the reported optically pumped WGM cavity GeSn lasers in terms of structure, Sn content, thickness, disk size, pumping laser, maximum operation temperature (T_{max}), and threshold.

Year	Structure	Sn (%)	Thickness (nm)	Disk Size (μm)	Pumping	T_{max} (K)	Threshold (kW/cm^2)	Ref
2016	Bulk	8.5	800	8	Pulsed 1064 nm	90	125 at 50 K	[74]
		12.5	560	8		130	220 at 50 K	
2018	Hetero	16	418	20	Pulsed 1064 nm	230	134 at 15 K	[78]
							375 at 135 K	
							640 at 190 K	
							790 at 230 K	
2018	Hetero	14.5	380	8	Pulsed 1064 nm	100	300 ± 25 at 20 K 250 at 50 K	[84,86]
					Pulsed 1550 nm	120	420 ± 10 at 20 K	
	MQW-A	13.3	22 (10×)		Pulsed 1064 nm	100	35 ± 4 at 20 K	
					Pulsed 1550 nm	120	45 ± 3 at 20 K	
	MQW-B	13.5	12 (10×)		Pulsed 1064 nm	No lasing		
					Pulsed 1550 nm	20	——	
2020	Bonded bulk	5.4	40	9	Pulsed 1064 nm	85	0.8 at 25 K	[80]
				12		100		
				9	**CW 1550 nm**	72	1.1 at 25 K	
2020	Low TDD bulk	7	500	7	**CW 1550 nm**	80–95	10	[81,82]
		8.1		6			8	
		10.5		5			8.9 at 25 K	
				8			11.6 at 25 K	

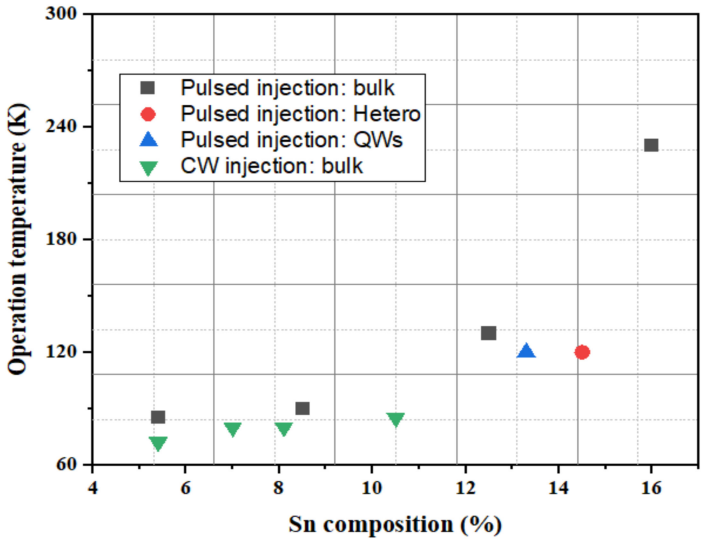

Figure 33. Maximum operation temperature vs. Sn content for an optically pumped WGM cavity GeSn laser (under pulsed 1064 nm laser).

4.1.3. Optically Injected GeSn Laser with Other Microcavities

In addition to those on FP cavity and microdisk cavity GeSn lasers, there have been publications on hexagonal photonic crystal (PC) and micro-bridge GeSn lasers. In 2018, Q.M. Thai et al. reported optically injected GeSn laser with 16% Sn content for the first time [72]. By introducing defects in the photonic crystal defect cavity (such as removing the central hole), the periodic structure around the photonic band gap were able to provide optical feedback to the microcavity. The experimental results showed that the maximum working temperature of the hexagonal photonic crystal GeSn laser was 60 K, and the threshold values at 15 and 60 K were 227 and 340 kW/cm^2, respectively (Figure 34).

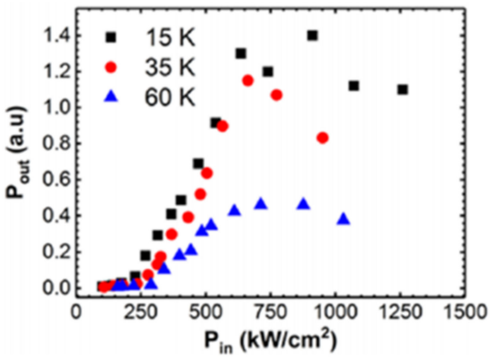

Figure 34. L–L curves for a photonic crystal GeSn laser with an Sn content of up to 16%. Reproduced with permission from [72], AIP Publishing, 2018.

In 2019, Jerémie Chrétien et al. explored a novel approach to create a direct bandgap GeSn material via strain redistribution, thereby controlling band structure and lasing wavelength [77]. Tensile-strained GeSn micro-bridge heterostructures were optically injected using pulsed 1064 and 2650 nm lasers (Figure 35), and the maximum operation temperature for the L = 75 µm micro-bridge structure laser was 273 K, which indicates that the operation temperature was very close to room temperature.

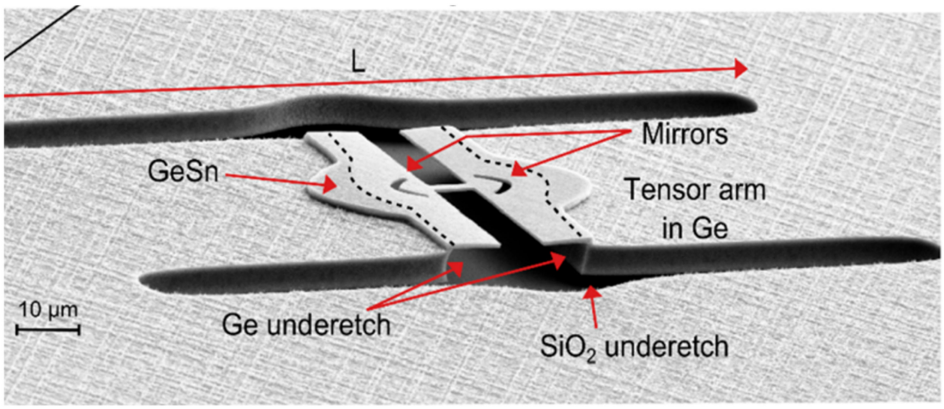

Figure 35. L–L curves for a micro-bridge GeSn laser with an Sn content of up to 16%. Reproduced with permission from [77], American Chemical Society, 2019.

4.2. Electrically Injected GeSn Lasers

Different from optically injected GeSn lasers, electrically injected GeSn lasers are more suitable for practical applications. However, electrically injected GeSn lasers are more challenging to create due to the GeSn active gain medium having to overcome the extra metal absorption loss and more free carrier absorption (FCA) losses. Theoretical predication for the realm of possibility of electrically injected GeSn/SiGeSn lasers can be traced back to ten years ago, when Greg Sun et al. presented modelling and simulation results for an electrically injected SiGeSn/GeSn/SiGeSn double heterostructure laser with an Sn contents ranging from 6 to 12% [210]; they found that this type of laser requires cooling in the temperature range of 100–200 K after taking radiative, nonradiative, and Auger recombinations into consideration. Afterwards, Greg Sun et al. theoretically proposed that the lattice matched that of an $Si_{0.1}Ge_{0.75}Sn_{0.15}/Ge_{0.9}Sn_{0.1}/Si_{0.1}Ge_{0.75}Sn_{0.15}$ MQW laser [211], and they found that modal gain was very sensitive to the QW number in the active region and SiGeSn/GeSn/SiGeSn MQW could operate up to room temperature with a 2300 nm emission wavelength. For the SiGeSn/GeSn/SiGeSn MQW laser with 20 QWs, the optical confinement factor was calculated to be 0.74, and the modal gain was able to exceed 100/cm at a pumping current density of 3 kA/cm^2, which was sufficient to attain room-temperature lasing.

In 2020, Yiyin Zhou et al. reported the first electrically injected FP cavity GeSn/SiGeSn laser on Si with a lasing temperature of up to 100 K; its minimum threshold was approximately 598 A/cm^2 [89,90] (Figure 36). This work was regarded as an essential achievement for Si-based on-chip light source in the development of Si-based OEICs. Later, the effects of cap layer, cap layer thickness, and Sn content in the active region on the operating temperature, threshold, and emission wavelength were further systematically studied [89,90]. Experimental results showed that: (I) an SiGeSn cap had a better optical confinement effect than a GeSn cap; (II) the optical confinement factor was improved via changing the SiGeSn cap layer thickness; and (III) the use of a GeSn laser with an Sn content of up to 15% did not significantly improve device performance.

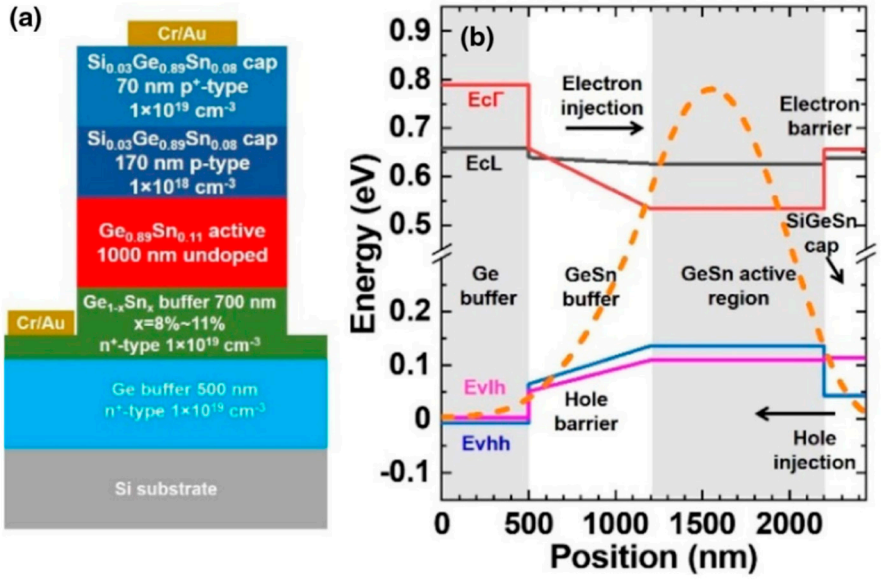

Figure 36. (**a**) Cross-sectional device structure for the first electrically injected FP cavity GeSn/SiGeSn laser; (**b**) calculated band structure and fundamental TE mode profile. Reproduced from [89], OSA Publishing, open access, 2020.

5. GeSn Transistors

In addition to the rapid advancement of GeSn detectors and GeSn lasers grown by CVD technology, there have been some achievements in the field of GeSn transistors due to their mobility properties. In the hyper-scaling era, the quest for high-performance and low-power transistors is continuing and intensifying. One of the key technology enablers of these goals is that of channel materials with high carrier mobility and direct band gap structures [212,213]. GeSn films have emerged as the most promising candidate for next generation nano-electronic devices of computing due to their excellent properties, including ultrahigh hole mobility, band structures with direct and low band gaps, Si-based CMOS compatibility, and low thermal budget, all of which are of great importance for ultrahigh density devices and 3D integration in the hyper-scaling era. Anisotropy at the top of the GeSn valence band makes the effective mass of light hole rapidly decrease with increases of Sn content and the transport capacity rapidly increase. GeSn is a very promising channel material for the next generation pMOSFET, and its hole mobility is even higher than that of Ge. The hole mobility of Ge pMOSFET is increased by more than 10 times with respect to Si devices. In addition, compressive strain can improve the mobility of a GeSn channel by decreasing the effective mass of the hole carrier. GeSn is generally grown on Si substrates using Ge as the buffer layer, and GeSn subjects the Ge buffer layer to compressive strain since the Sn lattice constant is greater than that of Ge. As GeSn materials are compatible with Si-CMOS technology, a few research groups have studied GeSn-based transistors (Table 8 lists the reported transistors with CVD-grown GeSn layers).

Table 8. Summary of reported transistors with GeSn layers grown by CVD technology in terms of institution, transistor type, Sn content, subthreshold swing (SS), I_{on}/I_{off} ratio, and V_{DS}.

Year	Institution	Transistor Type	Sn Composition (%)	SS (mV/dec)	I_{on}/I_{off}	V_{DS} (V)	Refs
2017	University of Notre Dame	Ge/GeSn p-type TFETs	11 and 12.5	215	9.2×10^3	−0.5	[99]
2017	NUS	GeSn FinFET on GeSnOI	8	79	$>10^4$	−0.5	[93]
2017	National Taiwan University	Vertically Stacked GeSn Nanowire pGAAFETs	6 and 10	84	-	−1	[214]
2017	National Taiwan University	GeSn N-FinFETs	8	138	10^3	-	[94]
2018	National Taiwan University	GeSn N-Channel MOSFETs	4.5	180	-	-	[215]
2018	National Taiwan University	Vertically Stacked 3-GeSn-Nanosheet pGAAFETs	7	108	5×10^3	−0.5	[91]
2020	PGI 9	Vertical heterojunction GeSn/Ge gate-all-around nanowire pMOSFETs	8	130	3×10^6	−0.5	[216]

Tunnel-field-effect transistors (TFETs) features subthreshold swings (SS) below 60 mV/decade at room temperature, which also enable a decreased power supply without discounting the off-current. Although Si-TFETs have been reported with SS below 60 mV/decade at low current, band-to-band tunneling (BTBT) is limited by its indirect bandgap property and low SS at high current. Therefore, researchers have investigated GeSn with high Sn contents (12% and 15% Sn incorporation; Figure 37) to create high-performance GeSn TFETs [217]. A higher Sn content enhances device performance, but the subthreshold swing is affected by the increased leakage level. For ultrasmall supply voltages, the device structure should be optimized to improve device characteristics. Using Ge/GeSn heterostructure pTFETs led to the improvements of the BTBT rate. Thus, higher on-current and lower off-current were achieved simultaneously. Christian et al. reported the fabrication and characterization of Ge/GeSn pTFETs (Figure 38), and they recorded a low accumulation capacitance of 3 μF/cm^2 [99]. Moreover, their room-temperature (RT) current–voltage characteristics showed that the Ge/GeSn pTFETs with the 11% Sn content had the highest BTBT current (Figure 39).

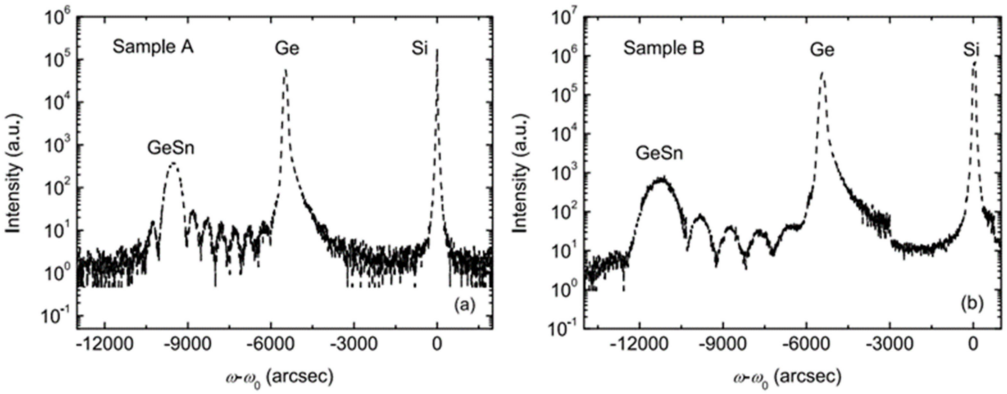

Figure 37. HR–XRD curves for GeSn samples with (**a**) 12% and (**b**) 15% Sn incorporation. Reproduced with permission from [217], IEEE, 2017.

To suppress the short channel effects (SCEs) of multi-gate transistors, Dianlei et al. investigated the p-FinFETs with a CVD-grown GeSn channel [93]. For GeSn p-FinFETs grown on GeSnOI substrates with 8% Sn incorporation (Figure 40), compressive strain and hole mobility were found to be −0.9% and 208 cm^2/V·s, respectively. Record low SS of 79 mV/decade for GeSn p-FETs were also achieved.

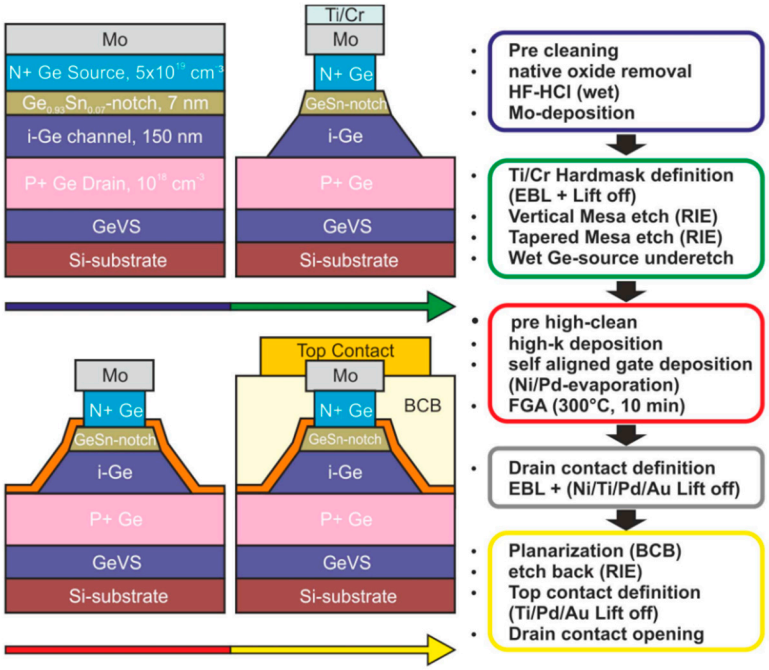

Figure 38. Process flow for Ge/GeSn vertical heterojunction pTFETs. Reproduced with permission from [99], IEEE, 2017.

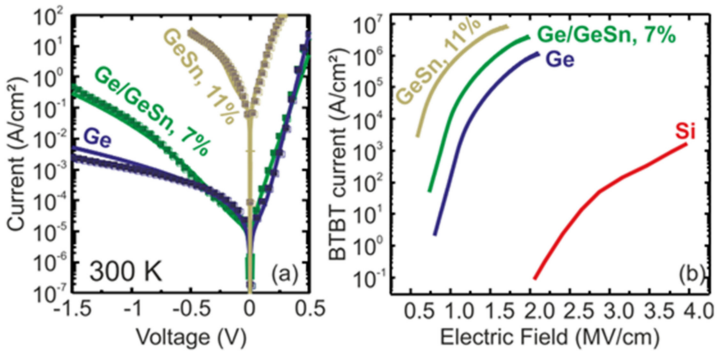

Figure 39. (**a**) RT current–voltage characteristics for GeSn p-i-n diode; (**b**) extracted BTBT current vs. electric field. Reproduced with permission from [99], IEEE, 2017.

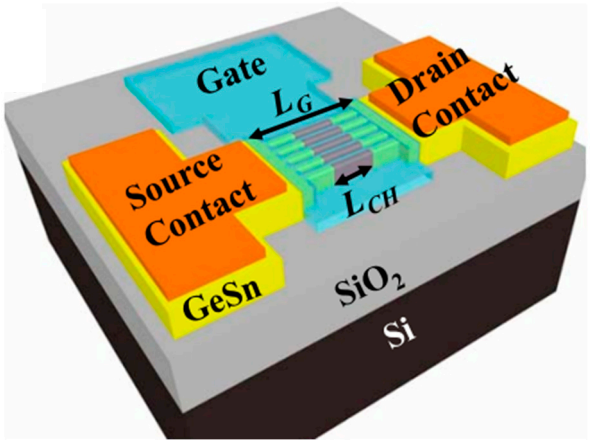

Figure 40. 3D diagram and highlights of the first GeSn FinFETs grown on a GeSnOI substrate. Reproduced with permission from [93], IEEE, 2018.

Compared with FinFETs, gate-all-around (GAA) FETs hold better electrostatic control, which can reduce the SCEs for the gate-length scaling. With down-scaling came the proposition of a vertically stacked Si channel for GAAFETs in order to improve drive current [218,219]. Yu-Shiang Huang et al. systematically investigated the strain response, LF noise, and temperature-dependence properties of vertically stacked GeSn nanowire pGAAFETs [214] (Figure 41). Their experimental results showed that: (I) I_{on} = 1850 μA/μm was improved with higher Sn incorporation; (II) the 6.3% extra enhancement of I_{on} was observed due to the uniaxial compressive strain that occurred when using wafer bending; and (III) the SS for one-nanowire and stacked two-nanowire GAAFETs were 84 and 88 mV/dec, respectively. To further improve the drive current for GAAFETs at a given footprint (Figure 42), vertically stacked 3-GeSn nanosheet pGAAFETs were studied and the I_{on} was increased 1975 μA/μm at V_{DS} = −1 V.

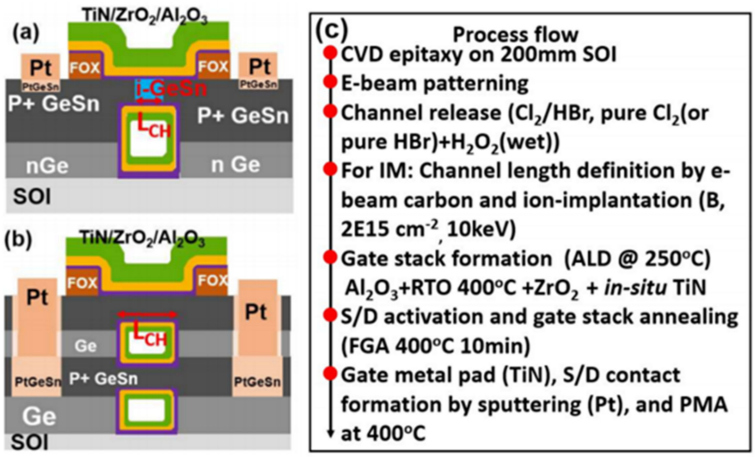

Figure 41. Schematic cross-sectional view of (**a**) single GeSn channel, (**b**) stacked GeSn nanowire pGAAFETs, and (**c**) process flow for devices. Reproduced with permission from [214], IEEE, 2017.

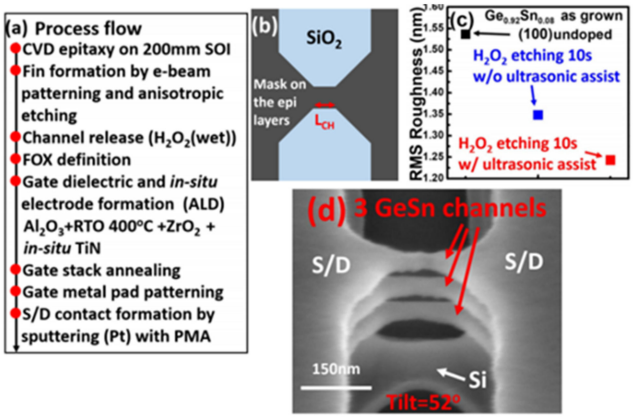

Figure 42. (**a**) Process flow for vertically stacked 3-GeSn nanosheet pGAAFETs; (**b**) top view after the fin formation; (**c**) RMS value for as-grown GeSn; (**d**) SEM image of stacked 3-GeSn nanosheets. Reproduced with permission from [91], IEEE, 2018.

Furthermore, a top–down approach was utilized to fabricate vertical heterojunction GeSn/Ge GAA nanowire pMOSFETs (Figure 43); with proper optimization, a record high I_{on}/I_{off} (3×10^6) was achieved [216].

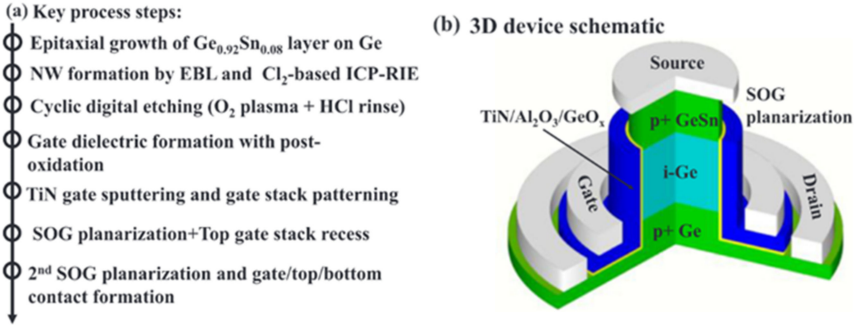

Figure 43. (**a**) Fabrication process and (**b**) 3D schematic of single vertical heterojunction GeSn/Ge GAA nanowire pMOSFETs. Reproduced with permission from [220], Elsevier, 2020.

Similar to the n–Ge material, n–GeSn suffers from a large resistance in metal-n–GeSn contacts mainly due to a strong Fermi pinning effect. To improve the performance of GeSn n-FETs, Yen Chuang et al. researched GeSn n-FinFETs and n-Channel MOSFETs: n^+–GeSn contact; in situ doped n^+–GeSn was grown by CVD, and Ni was employed as the contact metal [94]. With the increasing Sn content and n-type doping level, contact resistivity reduced to 3.8×10^{-8} Ω/cm^2, which may be attributed to the bandgap shrinkage of GeSn (8% Sn incorporation). With the optimized n^+–GeSn contact, the highest drive current and best SS for GeSn n-FinFETs were 108 A/m and 138 mV/dec, respectively (8% Sn incorporation) [91]. To suppress the dopant diffusion for S/D carrier activation, microwave annealing (MWA) was proposed. For GeSn with 4.5% Sn incorporation, GeSn nMOSFETs were found to possess an electron mobility of 440 $cm^2/V{\cdot}s$, suggesting that CVD-grown GeSn and MWA technologies are very promising for GeSn CMOS applications. For higher electron mobility, a 0.46% tensile strain was introduced to $Ge_{0.96}Sn_{0.04}$; due to the introducing of tensile strain, the carrier population in the Γ valley was higher. Thus, the electron mobility of GeSn nMOSFETs was further improved to 698 $cm^2/V{\cdot}s$ [215].

This discussion shows that pTFETs, pFin-FETs, pMOSFETs, nMOSFETs, and vertically stacked nanowire pGAAFETs with CVD-grown GeSn layers have been extensively studied; breaking the bottleneck the n-doped or p-doped GeSn CVD growth technology is one of the main routes forward for high-performance GeSn transistors. Uniformly stacked nanowires or nanosheets with low surface roughness are of great importance for 5 nm CMOS technology nodes and beyond. More importantly, It should be noted that Henry. H. Radamson et al. explored Ni–$(GeSn)_x$ contact formation [220]; the strain dependence, phase formation, and thermal stability of Ni–$(GeSn)_x$ were systematically investigated, and they found that an Sn-rich surface impeded the diffusion of Ni, thus paving the way for the optimization of high-performance nanowire pGAAFETs.

6. Conclusions and Outlooks

In summary, the challenges and progress of GeSn CVD growth technology (including in situ doping technology and ohmic contact formation), GeSn lasers, GeSn detectors, and GeSn transistors were reviewed. Due to growth difficulties, such as the large lattice mismatch between GeSn and Si, the low solubility between Ge and Sn, and phase changes for Sn, more effort must be made in improving the quality of high-Sn-content GeSn materials, GeSn/SiGeSn heterostructures, and GeSn/SiGeSn QWs for high-performance electronic and optoelectronic devices, especially GeSn lasers and GeSn TFETs. Sn distribution uniformity and sharp GeSn/SiGeSn interfaces are the key issues in the development of room temperature, CW electrically pumped GeSn lasers. In addition, research on novel Si-based group IV materials, such as CSiGeSn and CSiGe [221–223], may pave the way for better strain compensation and lattice-mismatched laser structures.

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writing—review and editing, Y.M. and H.H.R. All authors have read and agreed to the published version of the manuscript.

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High Performance p-i-n Photodetectors on Ge-on-Insulator Platform

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Abstract: In this article, we demonstrated novel methods to improve the performance of p-i-n photodetectors (PDs) on a germanium-on-insulator (GOI). For GOI photodetectors with a mesa diameter of 10 μm, the dark current at −1 V is 2.5 nA, which is 2.6-fold lower than that of the Ge PD processed on Si substrates. This improvement in dark current is due to the careful removal of the defected Ge layer, which is formed with the initial growth of Ge on Si. The bulk leakage current density and surface leakage density of the GOI detector at −1 V are as low as 1.79 mA/cm^2 and 0.34 μA/cm, respectively. GOI photodetectors with responsivity of 0.5 and 0.9 A/W at 1550 and 1310 nm wavelength are demonstrated. The optical performance of the GOI photodetector could be remarkably improved by integrating a tetraethylorthosilicate (TEOS) layer on the oxide side due to the better optical confinement and resonant cavity effect. These PDs with high performances and full compatibility with Si CMOS processes are attractive for applications in both telecommunications and monolithic optoelectronics integration on the same chip.

Keywords: GOI; photodetectors; dark current; responsivity

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1. Introduction

Silicon complementary metal oxide semiconductor (CMOS) technology could be used to integrate optical data communication and electrical data computing to achieve electron–photon synergy. Combining the advantages of photons and electrons can overcome some of the bottlenecks which microelectronics technology encounters with the development of Moore's Law, and open more directions for the continuation of Moore's Law [1,2]. Photodetectors (PDs) are the core devices of high-performance electro-optic conversion. Si photodetectors (PDs) are not attractive in optical communication because the cut-off wavelength of their absorption spectrum is 1100 nm. Ge has emerged as a leading contender for optoelectronic devices due to its pseudo-direct bandgap behavior, large absorption coefficient in the near-infrared region, lower cost, and compatibility with CMOS processing compared to III–V materials. This makes Ge PDs very promising in optoelectronic applications.

There are still some practical difficulties to overcome in the research of Ge PDs, especially for the Ge epitaxy on Si. People first attempted to epitaxially grow Ge on Si with a low dislocation density, mainly because the mobility of electrons and holes in Ge is higher than that in Si [3]. For high-quality Ge epitaxy on Si, the greatest challenge is the 4.2% lattice

mismatch ratio between these two elements. This mismatch will result in high surface roughness after growth and high threading dislocation densities in the Ge epitaxial layer, which will hinder the integration of Si and Ge devices and affect device epitaxy on Si [4–6]. SiGe buffer layers were used to reduce the number of threading dislocations in the Ge layer. By carefully adjusting the composition of the SiGe layers, many threading dislocations can be bent or terminated at the heterojunction interfaces, which greatly reduces the dislocation density in the Ge layer [7,8]. A two-step growth method has also been proposed, which can effectively prevent island-like growth, and subsequent annealing can greatly reduce the linear dislocation density [9–11]. Many efforts have been taken to improve the quality of the Ge layer on the Si substrate in order to improve the performance of Ge normal-incident PDs [12], waveguide PDs (WGPDs) [13,14], metal–semiconductor–metal PDs (MSM PDs) [15], etc. However, the fundamental problem of high defective regions at the epitaxial Ge/Si interface has not yet been solved. Various methods have been widely reported to optimize the process of Ge. Compared to the Ge-on-Si structure, the quality of the Ge layer on Ge-on-insulator (GOI) platforms can be significantly improved. During the preparation of GOI substrates, the low-temperature Ge layer with high defect density was removed, resulting in fewer generation/recombination centers in the Ge crystal [16]. In ref [17], the leakage current of Ge p-i-n photodiodes on a GOI substrate with threading dislocation density (TDD) of ~3.2×10^6 cm^{-2} was reduced by 53-fold from one with a TDD of ~5.2×10^8 cm^{-2}. In addition, the introduction of an insulator layer between the Si and Ge can provide better optical confinement for the Ge active layer, enhancing the optical responses of the devices [18]. The direct absorption edge of Ge at 1550 nm limits the application of Ge PD in the C-band (1530–1560 nm) and L-band (1560–1625 nm). In order to achieve high photodetection efficiency in the Ge layer, the optical absorption coefficient must be enhanced by narrowing the direct bandgap energy. An effective approach to narrow the bandgap is to apply enhanced tensile lattice strain. Tremendous efforts have been made to enhance tensile strain in Ge, including the introduction of GeSn [19,20], microbridge structures [21,22], external stressors of SiN_x [23,24], etc. To date, only a few Ge PD photoelectric detection ranges have been extended due to tensile strain on GOI substrates [25–29], and to the best of our knowledge, there is no report on the performance comparison of p-i-n detectors prepared on GOI with different oxide thickness.

In this work, we propose novel methods to improve the p-i-n photodetectors on the GOI substrate. Compared to the PD with low-temperature Ge on the Si substrate, the responsivity of the GOI detector is remarkably improved from 0.32 to 0.5 A/W under 1550 nm wavelength, and from 0.54 to 0.9 A/W under 1310 nm wavelength, increases of 56% and 67%, respectively. The measurement results show that the GOI PDs have lowest dark current of 2.5 nA because of better crystal quality. We also found that the optical performance of the GOI PD could be remarkably improved by integrating a tetraethylorthosilicate (TEOS) layer on the oxide side due to the better optical confinement and resonant cavity effect. We have realized the fabrication and experimental verification of ultra-low dark current and high responsivity GOI photodetectors, for which the detection range can be extended to 1630 nm. This method provides a good foundation for the realization of single-chip optoelectronic integration on large wafers in the future.

2. Materials and Methods

In this study, the Ge layers were deposited on p-type Si (001) 200 mm wafers in a reduced pressure chemical vapor deposition (RPCVD) reactor (ASM Epsilon 2000, Almere, The Netherlands). Ge epitaxy (epi-Ge) was performed in two steps, at 400 °C (low temperature or LT) and 650 °C (high temperature or HT), followed by an annealing of 820 °C for 10 min. The TDD was estimated to be 2.79×10^7 cm^{-2} in the Ge layer. The top 700 nm Ge layer was boron-doped to form P^+-Ge. The growth parameters were carefully optimized to avoid dopant precipitates in the Ge layer [30]. At the same time, a thermal oxide layer of 523 nm was formed on the handle silicon wafer. Later, a 10 nm Al_2O_3 layer was deposited on the epi-Ge wafer to increase the adhesion for bonding. At this stage, two groups of

samples were prepared for bonding; one group was directly bonded to the oxide wafer, but the other one with the TEOS layer was thinned to ~300 nm by chemical mechanical polishing (CMP). Then, the Si of the bonded wafer was removed through a combination of mechanical grinding and wet etching in tetramethylammonium hydroxide (TMAH) solution to form the GOI wafer. Afterwards, a CMP process was applied to remove the defected LT-Ge layer on the top. In these GOI wafers, the final Ge thickness was ~2 μm but the oxide thickness for the sample with no TEOS was 523 nm, whereas for the other one it was ~800 nm. In our experiments, the grown Ge layer on Si was considered as the reference sample.

Finally, a 100 nm thick top n-type Ge layer was formed by ion implantation twice at a dose of 1×10^{15} cm^{-2} and an energy of 18 keV. After each implantation, an annealing treatment at 500 °C in hydrogen for 60 s was performed. The doping level of the n-type layer was estimated as ~2×10^{20} cm^{-3}. The dopant profile of the PIN structure was evaluated by secondary ion mass spectroscopy (Figure 1a).

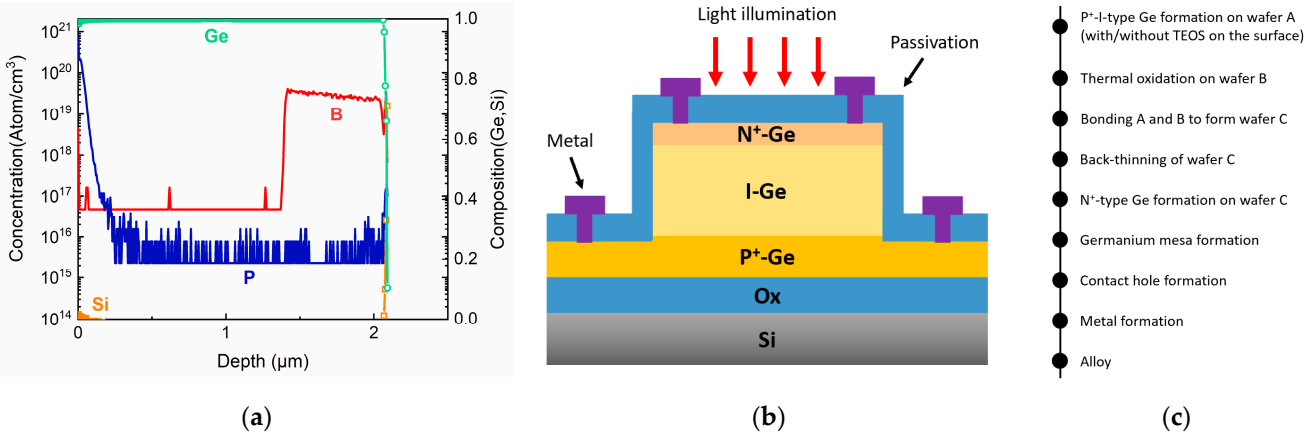


Figure 1. (**a**) SIMS data, (**b**) cross-section schematic, and (**c**) main process flow of GOI p-i-n photodetectors.

Pixels with diameter sizes of 10, 20, 40, 60, 80, and 100 μm were defined and etched down to p-type Ge (bottom contact), followed by a 300 nm thick SiO_2 deposition as a passivation layer by plasma-enhanced chemical vapor deposition (PECVD). After contact, electrode holes were formed by dry etching and wet etching, a 10 nm Ni layer was deposited and rapid thermal annealing (RTA)-treated at 450 °C to form NiGe. The NiGe reduced the contact resistivity to 1.3×10^{-5} Ω·cm^2, which was one of the important factors for low dark current in our detectors. Ni is a better choice compared to Co and Pt, which require higher annealing temperatures which cause dopant diffusion in the detector structure [31–33]. Later, a Ti/TiN/AlCu stack with thickness of 50 nm/10 nm/400 nm was deposited and etched to form metal electrodes. A schematic of the processed detector structure is shown in Figure 1b, and the main process flow of the GOI detector is shown in Figure 1c.

Figure 2a displays the cross-sectional transmission electron microscopy (TEM) (Thermo Fisher Talos, Brno, Czech Republic) image of the entire GOI photodetector with the diameter of 100 μm. An enlargement highlights the lattice arrangement of the Ge layer in Figure 2b. The crystalline quality of Ge layer was high and no obvious threading dislocations were observed, because in our process the defected LT-Ge layer was totally removed, and only the high-quality HT-Ge layer remained. The selected area diffraction (SAD) result of the Ge intrinsic layer is shown in the inset of Figure 2b, which has a very regular arrangement of spots, indicating excellent crystal quality. Figure 2c is an enlarged TEM image at the interface, showing a flat interface with no dislocations between the Ge/Al_2O_3/SiO_2 layers. The materials and processes used for device fabrication can be implemented in a standard CMOS process flow.

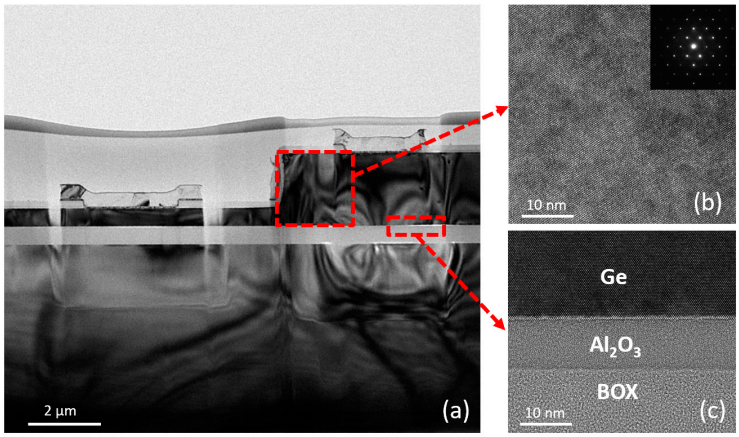
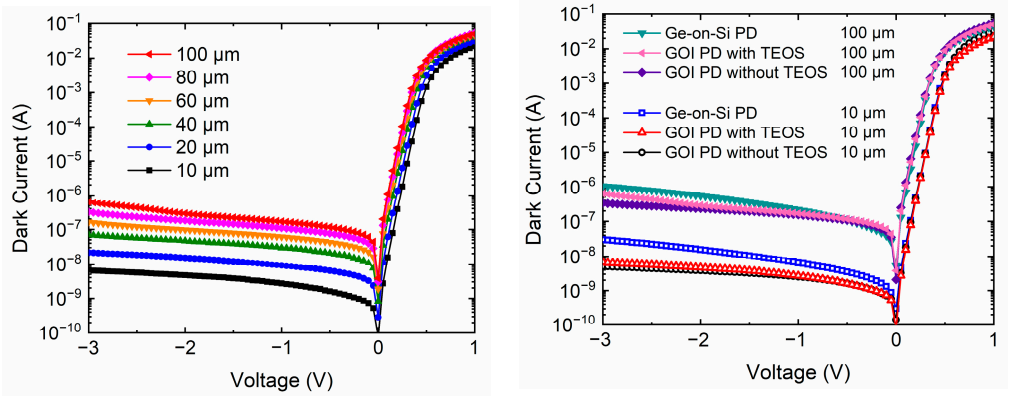


Figure 2. (**a**) Cross-sectional transmission electron microscopy (TEM) image of GOI p-i-n photodetectors. (**b**) High-resolution TEM image with its selected area diffraction (SAD) image (the inset) in the Ge layer, and (**c**) the $Ge/Al_2O_3/SiO_2$ interface.

3. Results and Discussions

3.1. Dark Current

The p-i-n PDs were characterized with respect to their electrical properties. The dark current of the photodiode is not only an indication of material quality, but also determines optical receiver sensitivity [10]. The dark current–voltage characteristics of the devices on GOI with various mesa radii were measured with a Keithley 4200-SCS semiconductor parameter analyzer (Cleveland, OH, USA) at room temperature, as shown in Figure 3a. The dark current curves exhibited a remarkable rectifying behavior with a high on/off current ratio near 10^8 between 1 and −1 V. Figure 3b displays the dark current comparison of GOI PDs and Ge-on-Si PDs with diameters of 10 μm and 100 μm. For Ge-on-Si PD with 10 μm diameter, the dark currents are 6.4, 15.6 and 30.1 nA at −1, −2 and −3 V. The detector on GOI with TEOS with diameter of 10 μm exhibited dark currents as low as 2.7, 4.7, and 6.6 nA at −1, −2, and −3 V. The detector on GOI without TEOS with a diameter of 10 μm exhibited dark currents as low as 2.5, 3.8 and 5 nA at −1, −2 and −3 V. The dark currents of GOI PDs without TEOS were 7.8, 27 and 100 nA for diameters of 20, 40, and 80 μm at −1 V, respectively. The defects/dislocations in the Ge layer increased the trap-assisted tunneling (TAT) leakage current, and carrier tunnels through the center of the Shockley–Read–Hall (SRH) under a relatively high reverse bias [34]. The GOI PDs exhibited ultra-low dark current because of the absence of a defective region compared to Ge-on-Si PDs.



(**a**) (**b**)

Figure 3. Dark currents of (**a**) GOI detectors with diameters of 10, 20, 40, 60, 80, and 100 μm, and (**b**) detectors on three types of substrates with diameters of 10 and 80 μm.

The dark current density (J_{total}) can be divided into the bulk leakage current density (J_{bulk}) and the surface leakage density (J_{surf}) using the following equation [6]:

$$J_{total} = J_{bulk} + 4\,J_{surf}/D \quad (1)$$

Figure 4 displays the total dark current densities (J_{total}) of different photodetectors at −1 V versus 1/D, where D is the mesa diameter of the device. Table 1 shows the dark current density comparison of Ge-on-Si PDs and GOI PDs. Compared with Ge-on-Si PDs, both surface leakage current and bulk leakage current of GOI PDs have been significantly reduced. The J_{bulk} and J_{surf} values of the GOI detector without TEOS extracted from Figure 4 were as low as 1.79 mA/cm^2 and 0.34 μA/cm, respectively. This low bulk dark current density of 1.79 mA/cm^2 is one of the lowest reported dark current density values among the Ge p-i-n photodetectors [35,36], which confirms the excellent Ge crystal quality. The J_{surf} of 0.37 μA/cm indicates excellent surface passivation, resulting in lower surface leakage current.

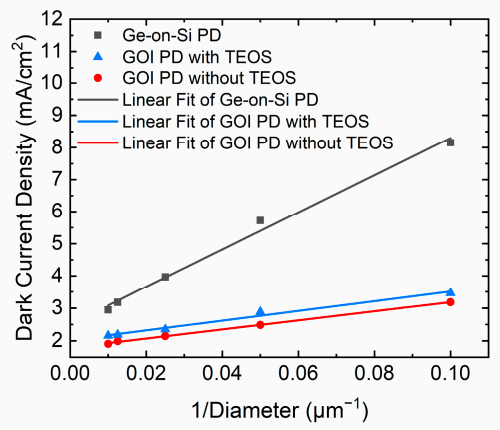


Figure 4. Dark current density (J_{total}) versus 1/D of PDs at −1 V reverse bias.

Table 1. Dark current density comparison of PDs on three types of substrates.

Dark Current Density	Ge-on-Si PD	GOI PD with TEOS	GOI PD without TEOS
J_{bulk} (mA/cm^2)	2.50	2.02	1.79
J_{surf} (μA/cm)	1.45	0.37	0.34

3.2. Responsivity

The photo currents of GOI photodetectors were measured at room temperature using an Agilent B1500A semiconductor parameter analyzer, a probe station, a laser with a wavelength of 1310 nm, and a tunable laser (1500–1630 nm). The photocurrents of the three types of detectors, which are Ge-on-Si PDs, GOI PDs without TEOS, and GOI PDs with TEOS, were measured, respectively. The thickness of the intrinsic Ge layer of all detectors was almost the same (~1.2 μm). The laser output was measured by a calibrated commercial reference detector. The incident light was coupled into the detectors through a single-mode fiber perpendicular to the surface. The spot-size of the fiber was about 3–5 μm. The light power was verified to be 1 mW by a calibrated commercial reference detector. The responsivity parameter is defined as follows:

$$R = I_{ph}/P_o = \eta q\lambda/hc \quad (2)$$

where I_{ph} is the photocurrent, P_o is the optical power incident on the PD, η is the quantum efficiency, q is the electrical charge, λ is incident light wavelength, h is Planck's constant, and c is the speed of light. The responsivity characteristics of different photodetectors under wavelength of 1550 and 1310 nm are shown in Figure 5a. The optical responsivity of

GOI PD without TEOS at 1550 and 1310 nm was 0.43 and 0.7 A/W at −1 V, corresponding to the external quantum efficiencies of 34.4 and 66.3%, respectively. For GOI PD with TEOS, the responsivity at 1550 and 1310 nm was 0.5 and 0.9 A/W at −1 V, corresponding to the external quantum efficiencies of 40 and 85.2%, respectively. The saturation of the optical responsivity values at 0 V bias revealed that the photodetector configuration allowed a complete photogenerated carrier collection without bias. The responsivities of the GOI PDs with TEOS at 1550 nm were 0.50, 0.47, and 0.45 A/W at −1 V, −2 V, and −3V, respectively. The responsivity at λ = 1310 nm was almost constant throughout the reverse bias region, while the responsivity around the band edge (λ = 1550 nm) slightly decreased with the increasing reverse bias because of the Franz–Keldysh effect (FKE) [37].

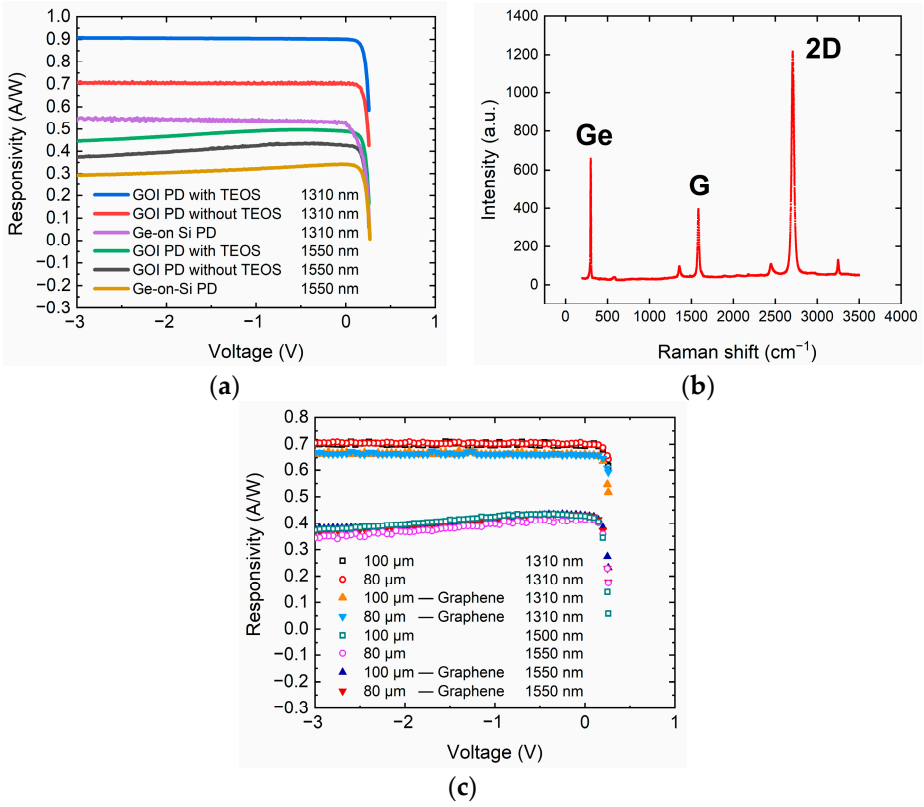


Figure 5. (**a**) Responsivity–voltage characteristics for illuminated PDs with a diameter of 80 μm on three types of detectors. (**b**) Raman spectra of transferred graphene on the detector. (**c**) Responsivity–voltage characteristics for illuminated GOI PDs (without TEOS) with or without graphene on the surface.

In order to improve the performance of Ge PD, an absorption graphene layer was placed on the detector's chip. Raman analysis was performed to confirm the quality of graphene after the transfer process, as shown in Figure 5b. The Ge (≈800 cm^{-1}), G (≈1600 cm^{-1}) and 2D peaks (≈2700 cm^{-1}) with an almost-invisible D peak (≈1300 cm^{-1}) on the SiO_2 indicate that the monolayer graphene was transferred successfully. Figure 5c shows the responsivity characteristics of GOI PDs with or without graphene at 1550 nm and 1310 nm, where 80 and 100 μm are the diameters of the detectors. Although the initial idea behind using graphene was to absorb infrared (IR) radiation, in these measurements, the detector with a graphene layer showed no significant improvements in the responsivity values.

In order to study the high-power characteristics of photodetectors, we used a semiconductor parameter analyzer, a probe station, a 1550 nm laser, and an erbium-doped fiber amplifier (EDFA) to measure the photocurrent under different optical powers at room temperature. The laser output was amplified by the EDFA and introduced on the

top surface of the photodetectors. Figure 6a shows the saturated photocurrent curves of the GOI PDs without TEOS with 80 μm diameter at a bias voltage from 0 to −2 V. The photocurrent gradually increased until it was saturated as the optical power increased. The saturated photocurrent increased with the increase in the bias voltage, because the intensity of electric field became stronger with the increase in the bias voltage and more photogenerated carriers were brought to the electrode, which eventually led to the saturation of the photocurrent [12]. The photocurrents of GOI PDs without TEOS under 100 mW incident light power were 28, 19.3, and 7.6 mA at bias voltages of −2, −1 and 0 V, respectively.

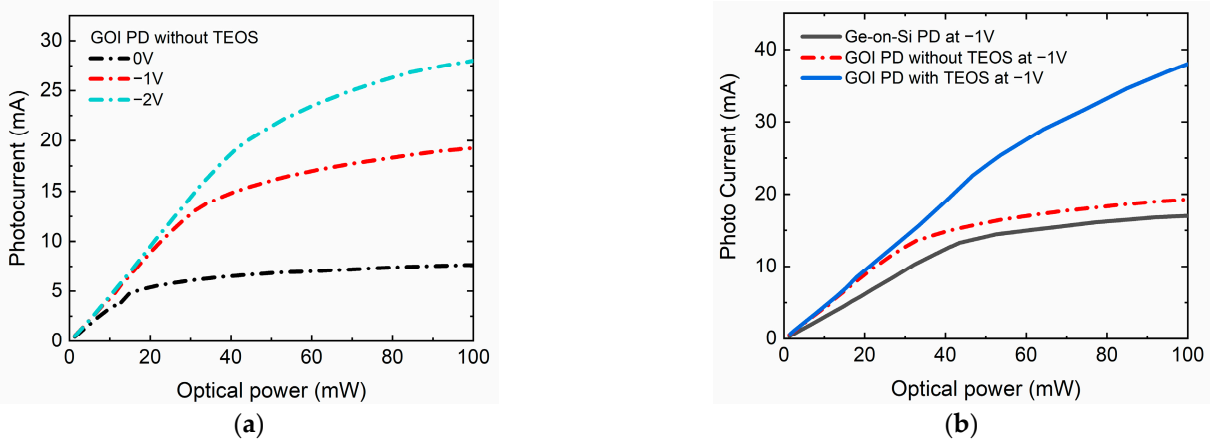


Figure 6. (**a**) Saturated photocurrent curves of the GOI PD without TEOS with 80 μm diameter at bias voltages of 0, −1, and −2 V. (**b**) Saturated photocurrent curves of the normal Ge-on-Si photodetector, GOI PD without TEOS, and GOI PD with TEOS at −1 V.

The high-power characteristics of photodetectors on different types of substrates were investigated, as shown in Figure 6b. The black, red, and blue lines represent the saturated photocurrents curves of the Ge-on-Si PD, GOI PD without TEOS, and GOI PD with TEOS with the same diameter of 80 μm, respectively. Compared to the Ge-on-Si PD, the saturated photocurrent of the GOI PD without TEOS was improved from 17 to 19 mA at −1 V. The saturated photocurrent of the GOI PD with TEOS seemed to be higher than 40 mA when the incident light power exceeded 100 mW, which is twice that of the GOI PD without TEOS at −1 V.

Due to the high refractive contrast between Ge(n~4.2), SiO_2(n~1.45), and Si(n~3.42), the light propagating in the Ge active layer can experience strong reflection at the Ge/insulator/Si interfaces, achieving better optical confinement in the GOI structure [18]. Due to the resonant cavity effect, the light intensity in the GOI active layer is higher than that of Ge on Si under the same light power irradiation, so the photocurrent of GOI PD is higher than that of Ge-on-Si PD. The schematic illustration of the principle of the dielectric mirror with high and low refractive index layers (Ge/Oxide/Si) is shown in Figure 7a. The thicknesses of Ge and SiO_2 are d_1 and d_2. To enhance reflected light inside the Ge layer, A wave and B wave should interfere constructively; this requires the phase difference to be 2π. Thus, d_2 needs to satisfy the following formula [38]:

$$d_2 = m(\lambda/4n) \quad (3)$$

in which m = 1, 3, 5 . . . is an odd integer. λ is the free-space wavelength. n is the refractive index of SiO_2. When m = 2, 4, 6 . . . . is an even-integer, the A wave and B wave will interfere destructively. For wavelengths of 1550 nm, the calculated d_2 for constructive interference could be 801 nm. The thickness of the SiO_2 layer of GOI with TEOS is ~800 nm, which is very close to the calculated result of d_2; therefore, it is more beneficial to form constructive interference in the Ge layer. Furthermore, the GOI with TEOS contained two types of oxide layers, TEOS and thermal oxide. The two-layer oxide structure with slightly different refractive indexes also provided a stronger optical resonant cavity effect for the detector,

as shown in Figure 7b. That is, the GOI PD with TEOS had better optical confinement and stronger resonant cavity effect, resulting in its higher photo current than that of GOI PD with only a thermal oxide thickness of 523 nm. Table 2 shows the effect of different SiO_2 thicknesses of GOI PDs on the light waves in the Ge layer. Thus, to obtain higher responsivity under 1550 nm and 1310 nm, the thickness of the oxide layer of GOI PDs should be accurately formed. In addition, the multi-layer structure can be used to realize the enhancement of the resonant cavity effect.

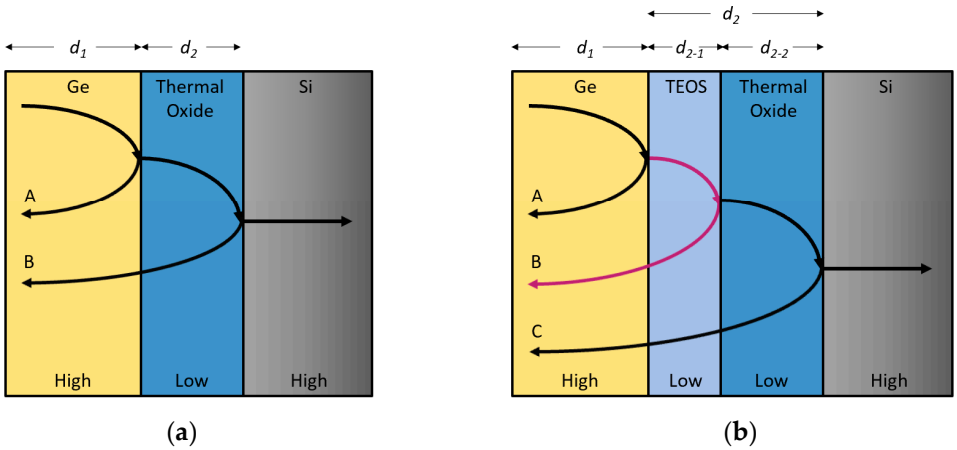


Figure 7. The schematic illustration of the principle of the dielectric mirror with high and low refractive index layers of (**a**) Ge/thermal-oxide/Si, and (**b**) Ge/TEOS/thermal-oxide/Si. Reflected waves A and B interfere constructively if the layer thicknesses d_2 is one-quarter of a wavelength within the layer.

Table 2. The effect of different SiO_2 thicknesses of GOI PDs on the light waves in the Ge layer.

GOI	**Oxide Thickness**		
m value	1	2	3
effect	Constructive	Destructive	Constructive
1550 nm	267 nm	534 nm	801 nm
1310 nm	226 nm	452 nm	678 nm

3.3. Spectral Response

In order to investigate the broad spectral responsivity of the GOI detector, the spectral response of the photodetector was measured using a Nicolet 8700 Fourier-transform infrared spectrometer (FTIR) (Thermo Scientific, Waltham, MA, USA) with a KBr beam splitter and glow-bar source at room temperature. A commercial InGaAs photodetector was used to calibrate spectrum responsivity. Figure 8a shows the spectral response of the GOI PD without TEOS under zero-bias. The optical responsivities of 0.7, 0.43 and 0.028 A/W at −1 V obtained by laser under 1310 nm, 1550 and 1630 nm are also shown for comparison. The trend of spectral response is consistent with that measured by laser. Compared to the other Ge PDs reported previously [18,26,36], this GOI detector achieved high responsivity in a wide spectral range of 1200~1650 nm. The responsivity spectrum of GOI PD showed strong oscillation structures, indicating the effectiveness of the resonant cavity structure to enhance the responsivity. We strongly believe that the responsivity can be further improved: (i) by engineering the cavity length (the thickness of the Ge active layer and oxide layer); and (ii) by optimizing the device process. Moreover, the time-resolved photocurrent response of the GOI PD with a diameter of 80 μm at −1 V under different incident light powers at a wavelength of 1550 nm is shown in Figure 8b. The consistent and repeatable photocurrent responses are observed without noticeable degradation while the incident light is switched with 5 s period. This indicates that our Ge PDs have low defect density and good performance.

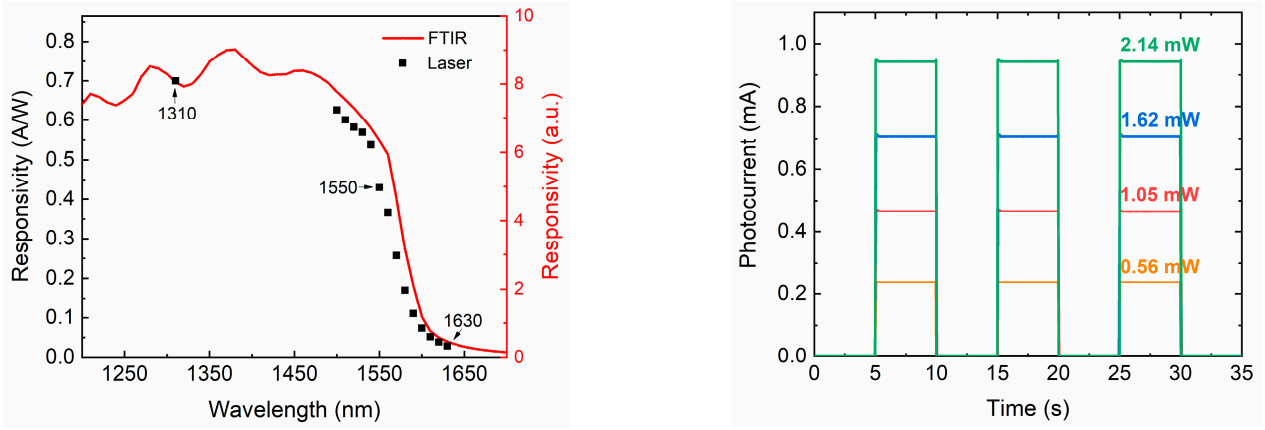


Figure 8. (**a**) The spectral response of GOI photodetectors between 1200 and 1700 nm, and (**b**) time-resolved photocurrent of the GOI photodetector at a wavelength of 1550 nm.

Therefore, we conclude that the GOI PDs are promising candidates for telecommunication applications with their extended photodetection range, enhanced optical responsivity, and complementary metal oxide semiconductor compatibility.

For comparison, an overview of the obtained results of the reported Ge-on-Si p-i-n photodetectors are listed in Table 3. To the best of our knowledge, our GOI p-i-n photodetectors proposed in this study exhibit the best comprehensive performance among the reported results.

Table 3. Performance comparison for the top illuminated Ge p-i-n photodetectors.

Year	Active Area (μm^2)	Dark Current at −1 V (nA)	Dark Current Density at −1 V (mA/cm^2)	Responsivity at 1550 nm (A/W)	Responsivity at 1310 nm (A/W)	Quantum Efficiency (1550 nm/1310 nm)	Ref
2005	$\pi \times 2500$	1728 at −2 V *	22 at −2 V	0.56 at −2 V	0.87 at −2 V	45%/82% *	[39]
2008	20×20	6.8 *	1.7	0.2 at −1 V	0.3 at −1 V	16%/28% *	[35]
2009	$\pi \times 25$	102 *	130	0.05 at −2 V	0.2 at −2 V	4%/19% *	[40]
2010	50×50	990	40	0.13 at −1 V	——	10.4%/—	[10]
2013	$\pi \times 100$	120 *	38.3	0.30 at −1 V	——	24%/—	[11]
2017	$\pi \times 36$	5.2	4.6	0.27 at 0 V	0.59 at 0 V	21.6%/55.8%	[36]
2017	$\pi \times 900$	1329 *	47	0.39 at −2 V	——	31.2%/— *	[27] GOI
2019	$\pi \times 25$	4	5	0.12 at −1 V	——	10%/— *	[41]
2020	$\pi \times 56.25$	450	255 *	0.31 at −1 V	0.52 at −1 V	24.8%/49.2%	[12]
2020	$\pi \times 15625$	280 *	0.57	0.28 at −1 V	——	22.4%/— *	[26] GOI
This work	$\pi \times 25$	6.4	8.1	0.32 at −1 V	0.54 at −1 V	25.6%/51.1%	Ge on Si
This work	$\pi \times 25$	2.5	3.2	0.43 at −1 V	0.70 at −1 V	34.4%/66.3%	GOI WO-TEOS
This work	$\pi \times 25$	2.7	3.4	0.50 at −1 V	0.90 at −1 V	40%/85.2%	GOI W-TEOS

The data have been extracted from the references as indicated. * Data calculated using the referenced material.

4. Conclusions

We have demonstrated a GOI substrate with a high-quality strained Ge layer. Optical devices (PDs) were prepared using a standard CMOS process on these substrates. The optical responsivity of the fabricated GOI p-i-n photodetectors with TEOS at 1550 nm and 1310 nm were 0.50 and 0.90 A/W at −1 V, corresponding to the external quantum efficiencies of 40% and 85.2%, respectively. The GOI p-i-n photodetector with both a thermal oxide and tetraethylorthosilicate (TEOS) layer showed the best optical performance due to its better optical confinement and resonant cavity effect. The GOI PDs without TEOS with a mesa diameter of 10 μm exhibited dark currents as low as 2.5 and 3.8 nA at −1 V and −2 V, and exhibited remarkable rectifying behavior with a high on/off current ratio near 10^8 between 1 and −1 V. These high-performance GOI PDs with extended detection range to 1630 nm indicate that the GOI substrates and devices are ideal for telecommunications and Si-based monolithically integrated optoelectronics compatible with the CMOS process.

5. Patents

The patent of resonant cavity substrate structure for improving the responsivity of photodetector and its method has been submitted.

Author Contributions: Conceptualization, X.Z., G.W. and H.H.R.; Data curation, X.Z., G.W., Y.M., H.L. (Haiou Li) and G.G.; Formal analysis, X.Z., G.W., H.L. (Haiou Li), G.G. and H.H.R.; Funding acquisition, G.W., H.L. (Haiou Li), G.G. and H.H.R.; Investigation, X.Z. and Y.M.; Methodology, X.Z., H.L. (Hongxiao Lin), X.L., Z.K., J.S., J.L., W.X., Y.M., H.L. (Haiou Li) and G.G.; Project administration, G.W., H.L. (Haiou Li), G.G. and H.H.R.; Resources, X.Z., H.L. (Hongxiao Lin), Y.D., X.L., Z.K., J.S., J.L. and W.X.; Software, X.Z., Y.D. and Z.K.; Supervision, G.W., H.L. (Haiou Li), G.G. and H.H.R.; Validation, X.Z., H.L. (Hongxiao Lin), X.L. and J.S.; Visualization, X.Z.; Writing—original draft preparation, X.Z.; Writing—review and editing, Y.M. and H.H.R.. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The data presented in this study are available on request from the corresponding authors.

Conflicts of Interest: The authors declare no conflict of interest.

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MDPI

Review

Review of Highly Mismatched III-V Heteroepitaxy Growth on (001) Silicon

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Abstract: Si-based group III-V material enables a multitude of applications and functionalities of the novel optoelectronic integration chips (OEICs) owing to their excellent optoelectronic properties and compatibility with the mature Si CMOS process technology. To achieve high performance OEICs, the crystal quality of the group III-V epitaxial layer plays an extremely vital role. However, there are several challenges for high quality group III-V material growth on Si, such as a large lattice mismatch, highly thermal expansion coefficient difference, and huge dissimilarity between group III-V material and Si, which inevitably leads to the formation of high threading dislocation densities (TDDs) and anti-phase boundaries (APBs). In view of the above-mentioned growth problems, this review details the defects formation and defects suppression methods to grow III-V materials on Si substrate (such as GaAs and InP), so as to give readers a full understanding on the group III-V hetero-epitaxial growth on Si substrates. Based on the previous literature investigation, two main concepts (global growth and selective epitaxial growth (SEG)) were proposed. Besides, we highlight the advanced technologies, such as the miscut substrate, multi-type buffer layer, strain superlattice (SLs), and epitaxial lateral overgrowth (ELO), to decrease the TDDs and APBs. To achieve high performance OEICs, the growth strategy and development trend for group III-V material on Si platform were also emphasized.

Keywords: III-V on Si; heteroepitaxy; threading dislocation densities (TDDs); anti-phase boundaries (APBs); selective epitaxial growth (SEG)

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1. Introduction

As the big data is coming, continuing rapid development of Internet business, communication network moves toward the direction of high speed and large capacity. To meet the data information transmission requirements of efficient, speedy, and integrated data, very large-scale integrated circuits (VLSI) were developed via continuing miniaturization of the transistor characteristic size according to Moore's law [1]. Si is always considered as the backbone material in the micro- and nano electronic industry owing to its natural abundance, high mobility, larger wafer size, low cost, and mature manufacturing technologies, etc. [2]. However, as the device characteristic size reaches to the sub-7 nm technology node, Si based integrated circuits are suffering from the physical and technological limitations in speed, power consumption, integration, and reliability, which further affect the device performance [3]. At present, two main technical roadmaps were expected to prolong the

Moore's law: (I) "non-silicon" high-mobility materials, such as SiGe, Ge, GeSn, GaAs, InAs, and InGaAs, were gradually extended into CMOS technology; (II) Si-based OEICs were proposed to integrate both photonic devices (such as the laser, optical modulator, optical waveguide, and photodetector) and electronic devices (transistors) on the sole Si wafer, which owns the advantages of faster transmission speed, larger transmission capacity, and low power consumption [4].

For high-mobility "non-silicon" materials, group III-V semiconductors can provide higher electron mobility (electron mobility of GaAs and InAs can reach up to 9000 $cm^2/(Vs)$ and 40,000 $cm^2/(Vs)$, respectively), and are ideal channel material for ultra-high speed and low-power devices, such as the high electron mobility transistor (HEMT) [5,6]. For example, to overcome the downscaling limit of conventional CMOS technology, monolithic integrations of various III-V devices, such as the sub−80 nm E–mode InGaAs/InAs HEMTs [7], InP-based HEMT [8], and AlGaN/GaN HEMT [9], have been proposed, enabling dense three-dimensional (3D) integration, low-power consumption, and high-speed applications [10]. On the other hand, for Si-based OEIC, the Si-based light source is the ultimate obstacle to achieve owing to the fact that Si is an indirect band-gap semiconductor material, and its emission efficiency is very low, which makes it unavailable as the active gain medium for Si-based high-efficient light sources. In contrast, most group III-V materials are definitely suitable for the optoelectronic devices in light-emitting/absorbing devices, including light-emitting diodes (LEDs), lasers, and detectors [11–14], owing to their direct bandgap properties, indicating their stronger photon emission and absorption efficiency in comparison than indirect semiconductors such as Si, Ge [15,16], and GeSn [17]. Thus, taking advantage of the excellent properties of III-V compounds, Si-based III-V CMOS devices and III-V photoelectric devices can further greatly improve the data transmission speed and amount, which effectively reduce integrated electricity and power consumption [18].

To realize the monolithic integration of III-V devices on the Si platform, it is critical to develop the heteroepitaxy technique for group III-V materials on Si [19]. Growth challenges for high-quality III-V heteroepitaxy on Si will cause APBs and TDDs/cracks [20,21]. APBs are caused by a polarity difference between III-V material and Si (surfaces for the III-V material and single Si are polar and non-polar), suggesting that it is prerequisite to prevent the formation of APBs. In case the APBs nucleated at the interface between III-V and Si, which can propagate through whole III-V epilayer, this leads to the devices' manufacturing on Si an impossibility [22]. Another important issue is the TDDs, an issue which is attributed to the mismatch of the lattice constant and thermal expansion coefficient between group III-V material and Si. As a result, both APBs and TDDs can lead to surface roughness, which act as the nonradiative recombination centers and leakage current to destroy the device performance [23]. Hence, the defects management strategy was proposed to decrease the TDDs and APBs for group III-V material, thus improving the device performance. Wafer bonding technologies, such as adhesive bonding [24,25], direct bonding [26], and fusion bonding [27,28], were adopted to form the advanced heterogeneous integration substrate platform. However, wafer bonding induces a high manufacturing cost and low integration density [29]. In addition, it is difficult to realize the graphics technology of alignment and passive devices in subsequent processing [30]. In this regard, growing high-quality III-V semiconductors on Si is the key pathway towards monolithic integration of III-V devices on Si-based OEICs.

The purpose of this review article is providing the types of defects and the mechanism of defects formation in silicon-based III-V heteroepitaxy and the detect solution. Particularly, we update recent advances in the epitaxial growth of large lattice-mismatched III-V materials on Si substrates, especially for GaAs and InP, which are both important materials for optic-device applications. This paper is arranged as follows: Section 2 introduces the fundamental challenges in III-V hetero-epitaxy on the (001) silicon wafer, and we also highlight their defect formation mechanism. Section 3 provides a brief review of growth strategies for the defect solution, including the miscut substrate, buffer layer, Strain super-lattice layers (SLSs), Aspect ratio trapping (ART), and epitaxial lateral over-

growth (ELO). Section 4 elaborates on recent approaches on growing high-quality III-V materials on Si. This includes global hetero-epitaxial thin film growth and selective-area hetero-epitaxy. Finally, we summarize the current status and discuss the potential future of III-V-on-Si heteroepitaxy.

2. Basic Challenges of III-V Hetero-Epitaxy on Si (001)

Heteroepitaxial growth represents a growth where materials with different lattice constants are grown in a stacked order, which is usually named "metamorphic growth" [31]. The relaxed lattice constant of the epitaxial layer is generally different from that of the substrate. To grow high-quality III-V layers on Si, fundamental challenges, such as the lattice mismatch, thermal mismatch, and substrate polarity difference, are the main limitations. Figure 1 shows the bandgap (wavelength) and lattice constants (lattice misfit) for the most commonly used group III-V and group-IV materials [32]. Below each semiconductor material, there are also annotation numbers for their own electron and hole mobilities, from which we can see that III-V semiconductor materials own higher electron mobility than Si, which are more suitable for the high mobility CMOS device. Meanwhile, direct bandgap property of III-V semiconductors made it more conducive to optoelectronic devices compared to the indirect gap of IV materials. However, there is a huge challenge to grow the III-V layer on the Si substrate owing to the highly mismatched nature of III-V and Si. In III-V semiconductors, GaAs (4.1%) and InP (8.0%) have close lattice constants to IV relatively, especially the Ge, which are more likely to realize the heteroepitaxy on the Si substrate. In addition, Ge has the close lattice constant and thermal expansion coefficients to GaAs, which are often used as a buffer layer to grow III-V on Si. This huge mismatch can bring out many defects such as: APBs, TDDs, stacking faults. In this section, the definition of mismatch and the mechanism of defect caused by mismatch will be introduced.

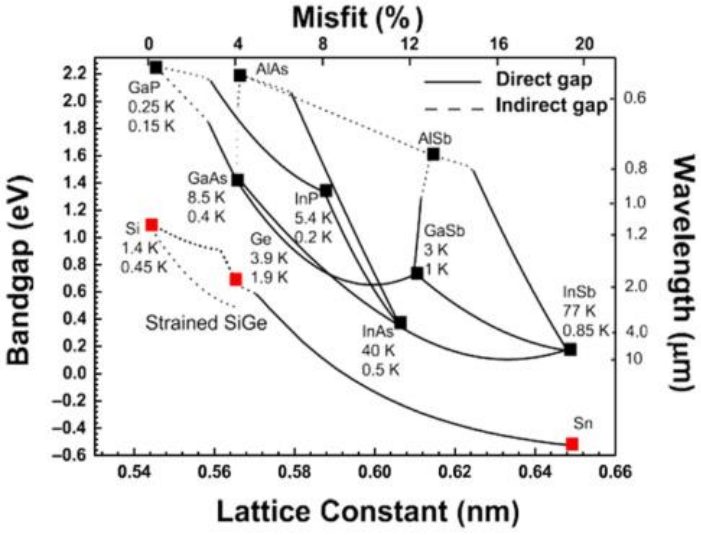

Figure 1. Bandgap (wavelength), lattice constants (lattice misfit), and mobilities for the most commonly used group III-V and group-IV materials. Reprinted with permission from ref. [32]. Copyright 2014 Springer Nature.

Electrical and optical properties of a semiconductor heavily depend on the crystal quality and, hence, defects in the crystal structure. There are several types of defects that can occur in semiconductor crystals, such as structural defects or compositional defects. Considering the spatial extension as a criterion, defects can be classified as 0 D point defects, such as vacancies, 1D line defects, such as misfit dislocations (MDs) or threading dislocations (TDs), 2D planar defects, such as APBs and stacking faults, 3D defects, such as voids. A detailed overview of defects is given by [33,34]. Figure 2 depicts three defect types relevant in this work. Figure 2a depicts a misfit dislocation forming at the interface to

compensate for different lattice constants of the materials. Figure 2b shows the APBs' defect. Homopolar III-III or V-V bonds can form due to the atomic steps grown on the non-polar Si substrate, which lead to the formation of APB. Figure 2c is the stacking faults that can occur during the III-V growth. If the stacking sequence changes in every layer, a zinc-blende (ZB) ABC stacking can be switched to a Wurtzite (WZ) ABAB stacking [35,36], which can impact the optical band gap since some semiconductors exhibit different band gaps for different crystal structures [37] or even change the band gap from indirect to direct or vice versa [38,39]. The heteroepitaxial growth of mismatched III/V on Si introduces additional challenges; hence, the mechanisms of challenges and the defect will be discussed below.

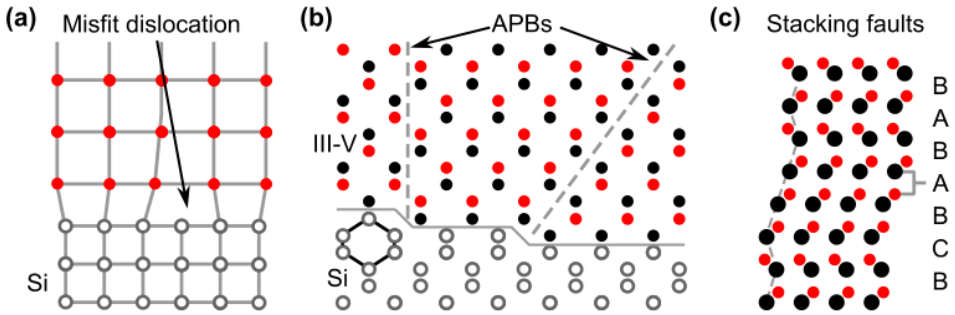

Figure 2. Schematic diagram of three defects (**a**) Misfit dislocation due to lattice mismatch, (**b**) APB at atomic steps of the substrate, (**c**) Stacking faults in the III-V material.

2.1. Lattice Mismatch

One important source of strain in heteroepitaxy is the difference in the lattice constant between different materials, referred to as lattice mismatch. This mismatch introduces strain in the epitaxial layer since it is forced to adapt to the lattice constant of the substrate when it is being deposited on. Eventually, after exceeding a critical thickness, the energy stored as strain will become so huge that the layer will relax. For example, at room temperature, the lattice constants of Si and GaAs were 0.543 nm and 0.565 nm, respectively, and the lattice mismatch was 4.1%. The strain in the heteroepitaxial layer resulting from mismatch is given by [4]:

$$\alpha_m = \frac{\alpha_s - \alpha_o}{\alpha_o} \tag{1}$$

where α_m is the mismatch strain in the epilayer; α_o and α_s are the substrate and overlayer lattice parameters, respectively.

If α_o is greater than α_s, it is a tensile strain; otherwise, it is compressive strain. In an epitaxial layer grown on a foreign substrate, the layer is subjected to biaxial strain in the plane of the substrate (normally the (001), if it is unrelieved, the biaxial strain will translate to a strain in the vertical direction according to:

$$\varepsilon^{\perp} = \varepsilon^{\parallel} \frac{1}{R_B} = \varepsilon^{\parallel} \frac{C_{11}}{2C_{12}} \tag{2}$$

2.2. Thermal Expansion Coefficient Mismatch

Most materials not only have specific lattice constants but also specific coefficients of thermal expansion (CTE). This is highly relevant in heteroepitaxy since epitaxy is normally carried out at a temperature of several hundreds of degrees, which means that the lattices of two different materials will contract to different extents upon cool-down. Going from growth temperature to room temperature, there will be an amount strain introduced in the epitaxial layer according to [40]:

$$\varepsilon_{th} = \int_{T_G}^{RT} \alpha_S - \alpha_0 dT \tag{3}$$

where α_s and α_0 are the thermal expansion coefficients of the substrate and the epitaxial overlayer, respectively, and T_G the temperature at which growth takes place. Since the grown layer is normally more or less relaxed during growth, the introduced thermal strain may lead to formation of dislocations.

When III-V thin film is deposited on a thick substrate, the layer will undergo a formation of misfit dislocations and threading dislocations. After the growth is completed, during the process of lowering the temperature of the wafer, the difference in CTE between the two causes the shrinkage ratio of the two materials to be different, resulting in thermal strain. We assume that during the growth process, it is completely relaxed. After the wafer is cooled down to room temperature, larger CTE (III-V materials) causes greater contraction than the Si substrate, so tensile strain is generated in III-V epitaxy. Nevertheless, the strain caused by the thermal expansion mismatch can be solved through buffer thickness. However, the thermal cracks emerge easily if a thick buffer accumulates too much strain energy when temperature changes. For example, CTE of GaAs (6.6×10^{-6} K^{-1}) is larger than Si (2.3×10^{-6} K^{-1}); the thermal mismatches between Ge, GaAs, and Si are 103%, 105%. Thickness for III-V films on Si is typically below 10 μm [41]. Therefore, huge thermal strain is generated in the thick III-V layer when the temperature drops to room temperature, resulting in thermal cracks through the III-V epitaxial layer. Similar to other defects, the presence of thermal cracks introduces destructive effects on the quality of the III-V epilayer and performance of optoelectronic devices, such as light scattering centers, the electrical leakage path, and a limitation on the total thickness of the epilayer [19]

2.3. Anti-Phase Boundary

Most materials have their own crystal structure and surface primarily. The V group (Si, Ge) has a diamond crystal structure, while III-arsenides and III-phosphides have a zincblende crystal structure which makes the different types of atomic stacking. For example, the diamond crystal structure has its ABAB . . . atomic stacking, but the zincblende crystal structure has its ABCABC . . . atomic stacking. When the III-V layer is grown on the Si substrate, the different types of atomic stacking make the APB defect formation, which arises from the polar on nonpolar nature of the III-V/Si heteroepitaxy and monatomic step of the (001) Si surface [42]. For instance, in the GaAs zincblende structure without defects, Ga atoms should be alternately connected with As atoms. Once the coordination of some atoms in the structure changes so that Ga atoms are no longer connected with As atoms, a two-dimensional structural defect will be formed at the interface where the changes occur, named APB. APBs arise as the existence of steps with odd atomic thickness on the surface of element semiconductor substrates (Si or Ge) and the uneven coverage of group III or V sources during silicon surface pretreatment [43].

In the process of substrate processing, it is impossible to obtain the (001) substrate with a perfect crystalline orientation. In this way, there are certain atomic steps on the actual substrate surface, which is a general monatomic layer height. The causes of APBs are shown in Ge substrate epitaxial GaAs. In the metal-organic chemical vapor phase epitaxy (MOCVD) system, arsenide (As) is pretreated with an arsenic atom (ideal) to grow GaAs on the Ge substrate (001) with the mono-atomic step surface. Due to the presence of the monatomic Ge step, the As atom and Ga atom are arranged alternately in the direction of (001), and GaAs interface with two orientations, and the As-As bond and Ga-Ga bond appear above the step, forming APBs. Figure 3a shows the single-layer steps (or odd layer height steps) to produce two domains in the III-V overlayer with opposite sub lattice allocation, whereas double-layer (or even-numbered) steps do not [44]. Although APBs do not involve partial dislocations, they can still interact with TDDs [45]. APBs are regarded as the non-radiative recombination centers for the optoelectronic devices, which will reduce the life of a few carriers in the device, and increase the scattering of most carriers, thus affecting the device performance. To characterize the influence of APBs on the optical properties, photoluminesce quenching and spectral broadening were usually adopted [46].

Besides, the APBs defect can be observed under SEM or AFM. As an example, irregular and curved boundaries were clearly observed for the SEM image of the as-grown GaAs/Si(100) sample (Figure 3b) [47]. APB is a plane defect, which can prevent the manufacture of Si-based III-V devices. Therefore, achieving APB-free III-V/Si heteroepitaxy is a fundament for following III-V devices' fabrication.

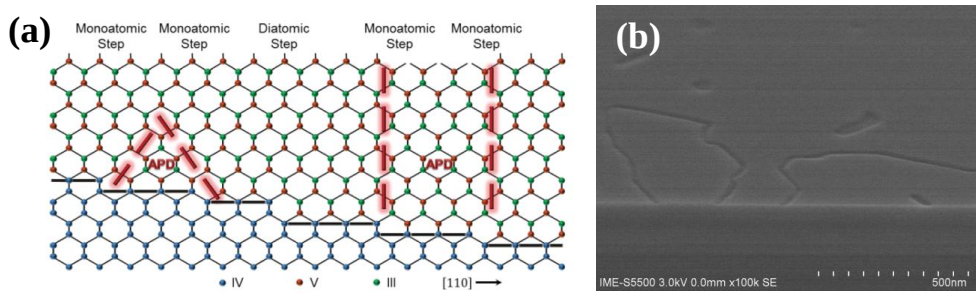

Figure 3. (**a**) (Color online) Schematic showing nonpolar/polar interface between Ge and GaAs. Monoatomic steps on the Ge surface result in APBs, planes of As-As, or Ga–Ga bonds. The APD can either self-annihilate (left) or rise to the surface (right). Diatomic steps on the Ge surface (center) do not result in APD formation. Reprinted with permission from ref. [44]. Copyright 2016 American Vacuum Society. (**b**) SEM plan view images of GaAs/Ge/Si (100) sample with APBs. Reprinted with permission from ref. [47]. Copyright 2021 Springer Nature.

2.4. Threading Dislocation Density

Heteroepitaxy of III/V materials on Si substrates results in the huge strain energy, which is released in the thickness of epitaxy via the formation of MDs along the heterointerface and TDs toward the surface. Thick epitaxy can release the mismatch strain but generates a large number of line defect dislocations. In addition, because of the mismatch TEC of III-V and Si, thick III-V epitaxy also accumulates much strain energy upon temperature cool down, inducing thermal cracks that emerge easily. These thermal cracks case the defects and surface roughness in the epitaxial layer; usually the dislocation density near the interface is as high as 10^9–10^{11}/cm^2 [48,49].

Dislocations are line defects representing a break of symmetry along a line, called the dislocation line, which are defined by a line vector, a Burgers vector describing the distortion of the lattice along the line, and a glide plane on which the dislocation moves. Dislocations can generally be subdivided into edge dislocations and screw dislocations. The fundamental difference between these two dislocation types is that whereas the edge dislocation is perpendicular to the dislocation line vector, the screw dislocation has a Burger vector parallel to the line vector. According to the angle between Burgers and the dislocation line, 90° (edge), 0° (screw), and 60° units are the important dislocations, and the 60° unit is the main dislocation which occurs mostly at the edge of island growth during initial epitaxy. Hence, the defect formation and glide mechanism are discussed. For heteroepitaxy to begin, a two-dimensional film Tc (a few nanometers) was grown on the substrate, allowing plastic relaxation to start. Because of the lager lattice mismatch, TDs will originate from the interface and glide along the slip planes to the surface with the increase in the epitaxy. When many dislocations appear in the same area, dislocation lines are formed by upward extension of multiple obvious dislocations. The entanglement of dislocation lines changes the direction of the dislocation movement. When multiple dislocations are entangled into one, the total number of dislocation lines will decrease, thus reducing the penetrating dislocation generated by upward growth and extension. However, the dislocation entanglement generates new dislocations in different directions, some of which annihilate with epitaxial growth and some penetrate to the surface, increasing the surface dislocation density. In addition, the surface dislocation mainly consists of proliferating dislocation and penetrating dislocation, forming a "dislocation half-loop". Figure 4 shows a sketch of MD formation by the glide of an existing TD from the substrate (I) and by

dislocation half-loop formation (II). This "dislocation half-loop" has a great contribution to the strain release [50].

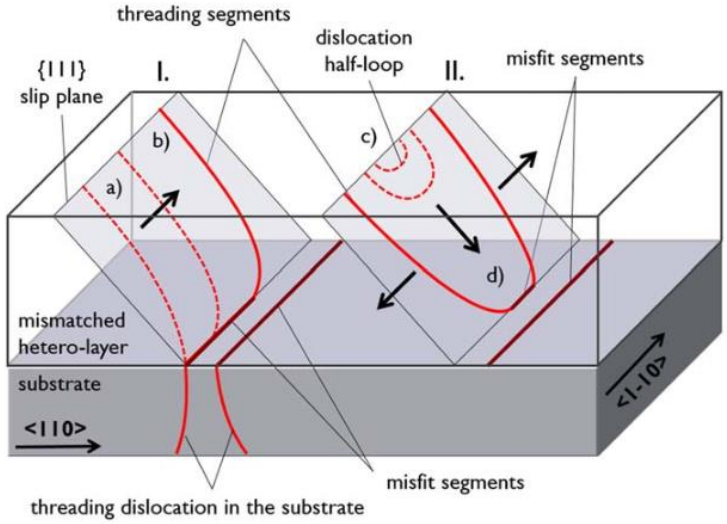

Figure 4. Schematic for the formation of misfit dislocation via threading dislocation glide: (**I**) TDs bend over and glide along the slip planes, (**a**,**b**) and half-loop formation; (**II**) half-loop nucleation at the surface and gliding down to the interface, (**c**,**d**). Reprinted with permission from ref. [50]. Copyright 2018 IOP Publishing.

TDs are one-dimensional crystal dislocations in semiconductor film, which has a serious impact on the properties of semiconductors. The TD is the scattering or absorption center of the carrier or light, which reduces the free path of the electron and greatly reduces the mobility of the carrier. For example, in optoelectronic devices, TDs are the center of non-radiative recombination because the intermediate bandgap energy level in the dislocation core is highly efficient at capturing minority carriers, resulting in a minority load in the material. These defects will form a non-radiative composite center, greatly reducing device lifetime and luminous efficiency. In the case of a semiconductor laser, only a large number of minority carrier reversals are realized in the active layer to obtain an effective gain, and a laser is generated, and it is seen that the reduction in minority carrier lifetime is disadvantageous [51]. In the laser structure, if the minority carrier lifetime is reduced due to dislocations, more injected minority carriers will form a non-radiative recombination before the number of population inversions are sufficient; then, the quality of the laser will fall. Early research work pointed out that for lasers, when the TDD is exceeded, the laser will not work properly due to the reduced lifetime of minority carriers [52]. Therefore, the necessary means to prevent the dislocation from extending upward and reducing TDD in the hetero-epitaxial layer is the main problem of laser fabrication on the basis of the current stage.

TDD is a quantitative parameter which describes the quality of the epitaxial layer. It can be measured by the three common approaches: (1) Etch-pit density (EPD) measurement [53]; (2) X-ray diffraction (XRD) measurement [54]; (3) Transmission electron microscopy (TEM) [55]. In the EPD method, TDD is obtained by calculating the pits at the crystalline region by optical observation or atomic force microscopy (AFM), which is a very easy, quick, and cheap process, but it tends to underestimate the TDD. XRD provides a non-destructive measurement of TDD in the range from 10^5 to 10^9 cm^{-2}. It is possible to calculate the TDD by measuring FWHM of rocking curve widths, because dislocations broaden the rocking curve. TEM measurement enables direct observation of TDs and quantitative analysis in the layer.

2.5. Stacking Faults

Stacking faults (SFs) are planar defects (PDs) representing a disruption in the crystallographic stacking order. In crystals with the Face-Centered Cubic (FCC) type lattice, they normally occur on {111} planes since these have the lowest SF energy. SFs can occur either as an insertion or removal of a crystallographic plane. This may happen either during deposition or by the gliding of a plane from its natural position to another. Joseph et al. [44] investigated the SFs originating from defects or contamination on the surface prior to growth, especially at low T_{sub}, which caused pits on the surface along [110] direction, as shown in Figure 5.

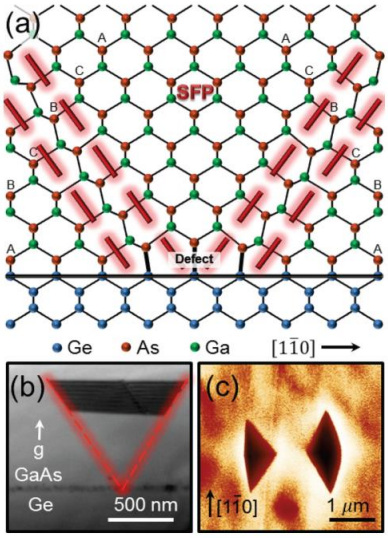

Figure 5. (Color online) (**a**) Schematic down [110] direction showing a SFP that originates from defect or contamination on the Ge surface; (**b**) XTEM with g = 002; (**c**) AFM image for the surface pits. Reprinted with permission from ref. [44]. Copyright 2016 American Vacuum Society.

3. Defect Solution for III-V Hetero-Epitaxy on (001) Silicon Wafer

3.1. Surface Treatment for Si Substrate

The atomic-level Si substrate platform is a basis for the III-V semiconductor devices' manufacture. It is because rough or particle substrates can cause the stacking faults during the heteroepitaxy. To avoid stacking faults, a very clean surface for the Si substrate is very important. The ex-situ process [56] (including cycled HF dip and O_2 plasma treatments) was developed, and film thickness variation (around 0.3 nm) is well reproduced (Figure 6).

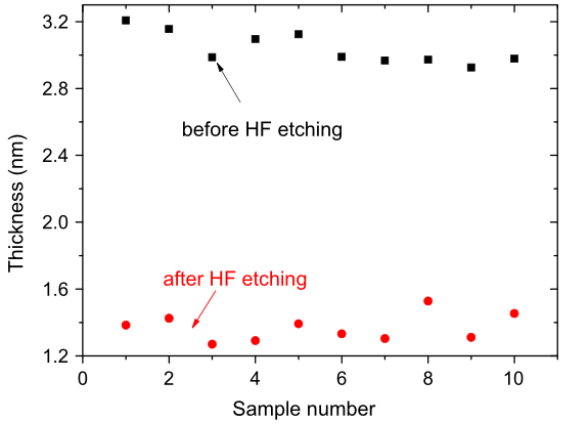

Figure 6. Thickness variation before and after HF 1% bath taken from a single Si substrate. Reprinted with permission from ref. [56]. Copyright 2015 Elsevier BV.

3.2. Process Optimization for III-V Heteroepitaxy Growth

3.2.1. Miscut Si Substrate

There are two main difficulties in heterogeneous growth of silicon-based III-V materials: APBs and TDs. As mentioned in Section 2.3, APBs' defect arises from polar mismatch between the III-V materials and the Si substrate, two alternating (2×1) and (1×2) dimerization on the monatomic steps of the Si (001) surface. In order to avoid anti-phase disorder in the III/V layer, it is important to nucleate on a (001) Si surface with bi-atomic steps. Double steps on the Si (001) surface are desired in order to suppress APBs in subsequently grown III-V epilayers. At present, it is universally acknowledged that the use of miscut Si substrates with various angles from 2° to 6° is effective in suppression of the formation of APBs [57,58]. A miscut Si substrate can make the Si-Si dimmers parallel to the upper terrace, and the double-atomic steps can form predominantly. The step structures of Si (001) and their energetic were studied theoretically by Chadi [59]. To obtain miscut substrates, thermal treatment is usually adopted to initiate the double-step formation, which was verified on Si substrates with a miscut in <110> directions [60]. The high-temperature treatment in As atmosphere using the miscut substrate can make the surface of the silicon substrate form the diatomic step, existing as (1×2) surface reconstruction, and the direction of the As-As dimer or Si-Si is parallel to the direction of surface step. This form is called single-domain surface, which is a stable surface structure. The III-V family layer obtained on this structure is a single-phase structure, thus inhibiting the APBs. However, the formation of a double-atomic step does not always guarantee the APB-free III-V epitaxial layer on Si. To ensure that the Si substrate surface is almost all diatomic steps or only a few single atomic steps, the crucial keys are the diatomic step validation of the Si substrate surface and process optimization. Sakamtoto et al. [61] verified the formation of diatomic steps of the Si surface by high temperature annealing and etched by anisotropy, respectively. Carved and reflection high energy electron diffraction (RHEED) are two ways to prove the Si surface formation of diatomic steps. The mechanism of mono-atomic step transformation to diatomic step transformation on the Si surface under cyclic annealing at high temperature was analyzed by Kawabe [62].

3.2.2. Bulk Hetero-Epitaxial Growth of III-V Thin Films on Si Substrate

TDD is another problem originating from the large lattice mismatch between the III-V and Si substrate. The effective suppression and reduction in TDs can be considered from two directions.

(1). The buffer layer and dislocation barrier layer with a strain field structure are the common method to reduce TD because the strain field generated by them can bend the direction of dislocation extension, thus effectively reducing the penetration depth of dislocation.

Low temperature buffer layer technology is a widely used scheme for heterogeneous epitaxy of silicon-based III-V materials, which can effectively inhibit the generation of dislocation at the interface [63,64]. The low temperature (LT) buffer layer is critical to the quality of III-V materials. III-V materials are generally island nucleated on the Si surface at a low temperature, which is the key factor affecting the nucleation density. When there is high growth temperature of the buffer layer (e.g., 650 °C), nucleation density is small, and large compressive strain causes many defects in the core. In contrast, lowering the temperature decreases the migration performance of surface nucleating atoms and the initial nucleus, thus increasing the nucleation density and reducing the size of the nucleus. The relaxation of the III-V layer at the interface releases strain and reduces the defect density at the top III-V layer [65]. Inserting buffer materials which the lattice constants between Si and III-V groups is an improved method to low TDD. The buffer layer can also be a material with a component gradient or gradual component gradient. For GaAs/Si heteroepitaxy, a wide variety of methods using Ge [66], SiGe [19], GeSnSi [67], InGaP [68] were developed. Among these materials, Ge has been most widely used because of its complete miscibility

with Si, well-developed Ge-on-Si growth technology, and nearly the same lattice constant with GaAs [69].

The graded SiGe component buffer layer can effectively disperse dislocation into different component epitaxial layers to obtain a high-quality top epitaxial layer. These buffer layers can provide a high surface base for III-V epitaxial growth owing to the little mismatch between them, which can improve the quality of the III-V epilayer. In addition, the control of initial nucleation conditions of the buffer layer is also the most critical part to obtain high-quality top layer materials. For example, the lattice constant of GaP is very close to that of Si. After obtaining the high-quality GaP/Si materials, the gradient layer $GaAs_xP_{1-x}$ can be used to obtain the transition to GaAs [70]. However, a very thick Ge buffer layer or graded SiGe buffer for III-V growth on Si causes difficulties for interconnection between the III-V Optical device and existing CMOS devices because of huge step height. Therefore, in order to obtain both lower TDD and a thin structural layer, multiplied superlattice layers are introduced.

Strain superlattice layers (SLs) commonly consist of multiple pairs of two lattice-mismatched layers alternately under compression and tension. If the thickness of each SLs' layer is less than a certain critical thickness (30 nm), which otherwise creates misfit dislocations, each SL accommodates elastic strains caused by lattice mismatch. The strain field of SLs can bend over and force the dislocations propagating upward to move laterally toward the edge of the sample, leading to dislocation coalescence and annihilation. Note that the SLs should have enough lattice mismatch and thickness to generate strain required for bending dislocations. SLs are used to filter dislocation, and dislocation density can be reduced an order of magnitude [71] when $In_xGa_{1-x}As/GaAs$ and $GaAs_{1-x}P_x/GaAs$ SLs structures were inserted between the silicon substrate and III-V material. However, SLs will introduce new strain in the epitaxial layer, which will cause mismatching dislocations from the III-V/Si interface to slip and interact, merge, or vanish**.** These SLs can make the propagating TDs bend over to interfaces and serpentine back and forth between the different superlattice interfaces, which increases the chance of coalescence and annihilation with other dislocations.

In addition, instead of two-dimensional SLs, the self-assembled QDs can be better used as DFLs to decrease TDD. Because the strain-driven self-organized QDs produce a large three-dimensional (3D) strain field around themselves, dislocations around QDs can be bent over and annihilated in a similar way to SLSs' DFLs. Consequently, 3D QDs islands can promote the propagating dislocations to bend over more easily due to the stronger Peach–Koehler forces [72]. Yang et al. [73] proposed and demonstrated the employment of InAs QDs as 3D DFLs in GaAs-based material. Then, Shi et al. [74] reported a four-fold reduction in density of TDs in the InP/Si system by using self-organized InAs/InAlGaAs QDs as DFLs. A number of TDs generated from InP/GaAs and GaAs/Si interfaces propagate toward the top surface, leading to the TDD of 1.3×10^9 cm^{-2}. However, the growth process of quantum dots has relatively high requirements. How to control the growth conditions of quantum dots, or the best quantum dots, is needed to be solved.

(2). During the process of epitaxial growth, controlling and optimizing the growth condition of the epitaxial layer are another method to decrease TDD. Heteroepitaxy growth is a complex process science as it involves issues, e.g., nucleating, temperature, thickness, annealing, so a systematic investigation for III-V heteroepitaxy on Si is necessary. For example, too high initial temperature can induce the forming of 3D islands in in initial nucleation. A high temperature annealing process [75,76] can make defects slip and disappear and too-thick epitaxy and can increase the bow on the wafer [77]. Meanwhile, another measure includes a buffer layer with thermal cycle treatment [78], and other methods have also been developed to decrease the TDD.

Currently, the heteroepitaxy of III-V materials on Si substrates consists of primarily two methods, one is the global area epitaxy and the other is selective epitaxial growth (SEG). Global area epitaxy generally includes silicon-based III-V direct epitaxy of a group of materials and epitaxy using a buffer layer. SEG is a more effective method to reduce

TDD, which can limit the defects in the patterned channel, obtaining a high quality III-V heteroepitaxial layer.

3.2.3. Selective Epitaxial Growth (SEG)

Selective epitaxial growth (SEG) is introduced for the integration of different materials on the same plane or for the realization of high-quality III-V semiconductor layers. This technique is based on a certain purpose graphed Si (or Ge) substrate, locally epitaxial on the III-V layer, graphed as an insulating medium (generally SiO_2). The graphic substrate has the advantages of releasing strain caused by heat mismatch, strong repeatability, and ease of combination with other epitaxial methods, which makes it another promising method. There are two mechanisms for dislocations reduction using graphic substrates: one is aspect ratio trapping (ART); the other is epitaxial lateral overgrowth (ELO).

ART technology is the solution of the epitaxial high-quality III-V family layer in silicon graphics grooves with a height/width ratio greater than 2. It is a method to limit the dislocation at the bottom of the groove by using the limiting effect of the SiO_2 side wall on the dislocation in the groove on the Si graphics substrate through the selection epitaxy. In the groove of this size, the growth plane changes from the original (001) plane to a crystal plane composed of {111} and {113} when the group III-V material was grown [79]. Defects, such as dislocations, also extend along the crystal plane and are limited when dislocations meet the groove insulation wall, thus obtaining a top layer with almost no defects (Figure 7).

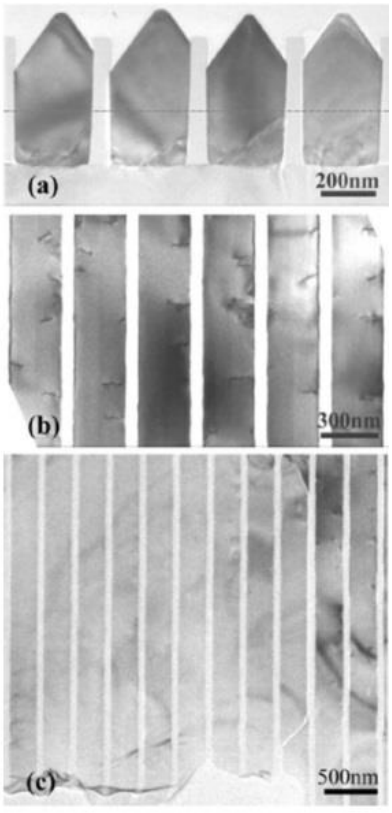

Figure 7. (**a**) Cross-sectional TEM of silicon-based GaAs in the groove in the direction of [110] (the groove width is 270 nm, and the depth to width ratio is 1.8); (**b**) the plane TEM image, the defect is near the insulation wall; (**c**) TEM image of the thinned sample. Reprinted with permission from ref. [79]. Copyright 2007 American Institute of Physics.

ART epitaxy technology has the following advantages: (1) easy to integrate with a variety of high mobility group III-V materials and device structures; (2) it can use the selective epitaxy to achieve the epitaxy growth of Ge materials and group III-V materials between different grooves to achieve the monolithic integration of the Si base; (3) the

graphic substrate of the scheme can be prepared by STI (shallow trench isolation) templates in traditional Si-based microelectronic technology, which is convenient for future large-scale integration; (4) the scheme can be directly in the groove to achieve a high-quality group III-V nano-scale on Si, compared to other nano-material preparation methods; the scheme is more convenient for the next generation of Si based high mobility device preparation and application. The scheme can combine the excellent optoelectric properties of III-V group materials with Si, and has great application potential in the future Si-based monolithic optoelectronic integration.

Epitaxial lateral overgrowth (ELO) is a technique developed to overcome the difficulties with obtaining a high-quality epitaxial layer on a foreign substrate. The idea is to use a substrate of a first material with a thin layer of a second material as a starting point. The layer of second material will be full of defects due to the previously outlined mechanisms. On top of this layer, a mask, normally a dielectric such as SiO_2 or Si_3N_4, is deposited, and openings in the mask are defined by lithography and etched. Growth is then conducted selectively in the openings with no nucleation on the mask (shown in Figure 8a). Once the grown material reaches the height of the mask, it starts growing laterally across the mask without nucleation on it, as shown in Figure 8b. In the laterally grown parts, propagating defects such as threading dislocations and stacking faults will be blocked by the mask and consequently cannot propagate into the layer above the mask.

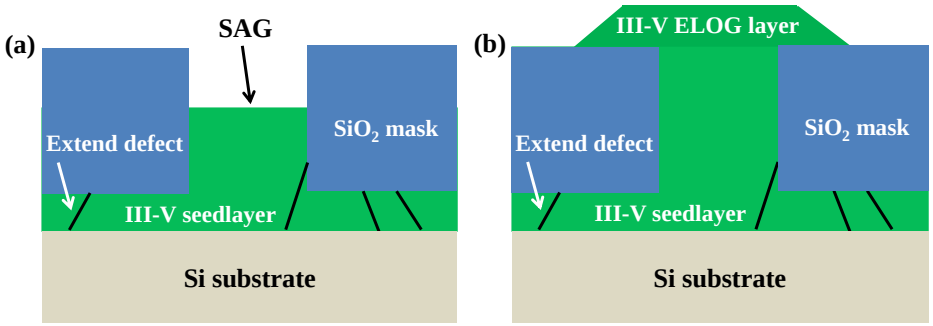

Figure 8. Principle of SAG (**a**) and ELO (**b**) applied to heteroepitaxy of III-V on Si.

It was shown that the angle between the mask openings and the crystallographic direction greatly influences the lateral and vertical growth rates as well as the bounding facet plane [80]. Recently, it was also shown that image forces acting on dislocations close to the mask sidewalls in the openings cause dislocations to bend towards the mask sidewalls, thereby enhancing the filtering effect so that virtually no dislocation propagation though the mask openings occurs [81].

Above all, traditional Si based III-V materials' heteroepitaxy technology described above is still facing a series of problems. For example, the demand of TDD values should be lowered to 10^{-6} cm^{-2}, the RMS surface roughness as low as below 0.5 nm, and compatibility with the traditional CMOS process make it difficult to realize the large-scale integration application of Si-based III-V group devices in the future. Therefore, how to solve the defect of the highly heteroepitaxy mismatch of Si-based III-V group materials is the problem that most scholars are solving at present.

4. Latest Approach of Heteroepitaxy of Si-Based III-V Group Materials

4.1. III-V Thin Films Hetero-Epitaxial Grow on Si Wafer-Scale

Fabricating the optoelectronic devices, a high-quality structure of III-V layers grown on the Si substrate is prerequisite. However, defects such as the APBs and the TDDs, propagating from the heterointerface to the surface, seriously affect the performance of the device. Bulk III-V structure layers are the basis of larger scale optoelectronic devices' fabricating. This section will introduce several methods to achieve TDD-lowering and an APB-free III-V layer on Si substrates, mainly focusing on global epitaxial growth on the bulk Si substrate.

4.1.1. APB-Free of III-V on Miscut Ge/Si Substrates

The APB defect is very obvious, which is derived from the different atomic step between the III-V and Si substrate. However, substrates with a sufficient miscut exhibit a double-stepped terrace structure that can significantly reduce the APB. In 1986, Kawabe [82] grew APB-free of GaAs/Si films on a mis-oriented Si (001) substrate toward (110), which has a better structural quality and luminescence efficiency. Then, the affection of different crystal directions on APB elimination was studied [83,84]. It was suggested that mis-orientation toward (100) is optimum, since it produces steps in the vertical (110) directions, and this assists the formation of edge-type which is fit dislocations that accommodate the misfit more efficiently [85,86]. Then, the influence of different angles of the Si substrate on the inhibition of APB is also discussed. Wanarattikan et al. [87] grew GaAs layers with two-step growth on miscut Ge (001) substrates mis-oriented by big angles between 4° and 6° towards [110] direction. They found that APBs were limited at the 20–30 nm GaAs/Ge interface, while APBs-free 480 nm GaAs regions can be significantly obtained on the 6° miscut Ge (001) substrates with the RMS of 0.9 nm. A higher quality of GaAs with four times the FWHM of the GaAs epilayer than that grow on the normal Si substrate. However, the large angle substrate is not only difficult to manufacture, but also incompatible with the existing silicon manufacturing technology. Figure 9 shows the model of APBs' generation and self-annihilation mechanisms In Figure 9a, an incomplete pre-layer at the initial Ge/Si surface induces the APBs' generation when III-V epitaxy grows on the axis (001) Ge/Si substrate. The Ga and As atoms can be adsorbed on Ge atoms, forming Ga–Ga and As–As bonds along the [1] direction. Instead, the miscut substrate can offer a short terrace length between steps, which is conducive to APDs' annihilation at an initial growth stage. Figure 9b,c are the model of APDs' formation and annihilation.

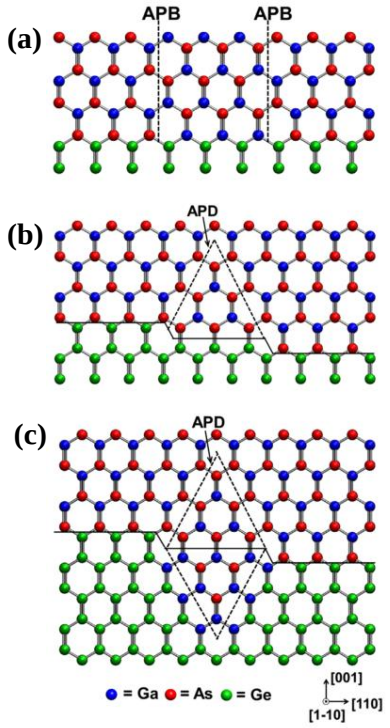

Figure 9. The model of generation and self-annihilation mechanisms of APBs: (**a**) an on-axis Ge (001) substrate and (**b**,**c**) miscut Ge (001) substrates. Reprinted with permission from ref. [87]. Copyright 2015 Elsevier.

Recently, one notably called "exact" Si (001) substrate with a slight mis-orientation (<0.5°) was made to grow APB-free III-V epilayers [88]. Figure 10 shows the GaAs layer was grown on different types of Si substrate. In Figure 10a, a high density of randomly oriented APBs on the GaAs surface with the RMS roughness of 1.6 nm was obtained when

grown on a normal Si substrate. Figure 10b shows the "quasi-normal" Si (001) substrate with a 0.15° after the surface preparation procedure by annealing, presenting a 2 × 1 surface structure and predominant double steps. Based on the double steps of the "quasi-normal" Si (001) substrate, a 150 nm GaAs overlayer was deposited. Figure 10c shows the AFM image of the GaAs surface. We can see the APB-free surface of GaAs with a 0.8 nm RMS value. Above all, it is not necessary to use a large miscut substrate; instead, using this "quasi-nominal" substrate can make the GaAs layers more compatible with the existing silicon manufacturing technology.

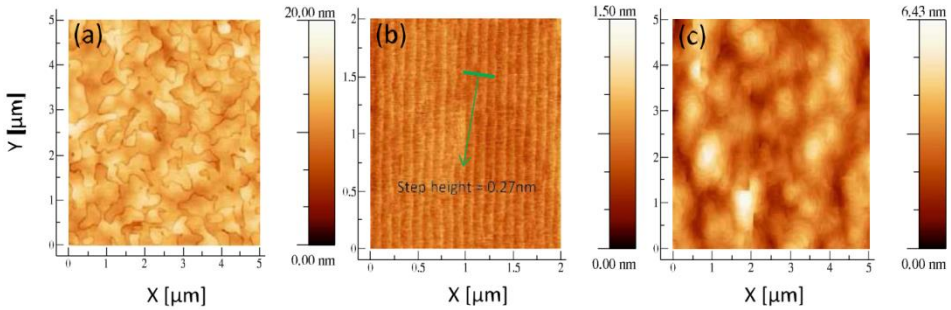

Figure 10. AFM image of (**a**) GaAs grown on un-optimized Si (001): High density of randomly oriented APBs; RMS roughness 1.6 nm; (**b**) 0.15° Si (001) surface after optimized preparation (800–950 °C annealing under H_2). The surface is therefore mainly double-stepped; (**c**) APBs-free GaAs layer grown on optimized 0.15° Si (001): RMS roughness is 0.8 nm. Reprinted with permission from ref. [88].

As for the growth of InP, there is little research on bulk heteroepitaxy due to the large lattice mismatch (8%). M. Grundmann et al. [89] studied the existence or the lack of APB in the InP, providing the information about the presence of single or double atomic steps on the Si, respectively. They found the APBs-free InP could be obtained if it used the 3.8° miscut Si substrate. APBs could be decreased by the miscut substrate, but there were still hillocks on the InP layer.

4.1.2. TDD-Reduction of III-V by Inserting Buffer Layers

TDD is a common problem in heteroepitaxy, which is caused by mismatch of the lattice constant and CTE between different materials. The TDDs extend directly through the epitaxy layer from the interface surface, which greatly affects the performance of devices. For a high-quality III-V layer monolithically grown on Si, achieving a low density of TD is a key issue. In particular, the TDs penetrating an active region of optoelectronic devices significantly degrade their performance.

The forming of TDD begins the initial stage of III-V growth on Si, since the growth begins with the formation of the island on the Si surface. A simple two-step growth has been most widely adopted in III-V heteroepitaxy. The two-step growth starts with low-temperature (LT) growth in the initial stage, then growing the overlayer at typical high temperature (HT). During this growth method, the defects are introduced in the LT step because it can introduce a higher density of islands, which is better for islands coalescing into a continuous layer at HT growth [90]. Although the conventional two-step growth can be used in the process of heteroepitaxy, for Si based III-V heteroepitaxy, the large mismatch of the lattice constant and CET results in a large penetrating dislocation and thermal strain in the epitaxy material. Hence, a wide variety of methods have been extensively studied, including the buffer layer, annealing, three-step growth, and superlattices (SLs). Based on the III part of the growth principle of III-V heteroepitaxy on Si, the big challenge is a large lattice mismatch between them, which induces the quantitative TDD. Therefore, inserting a buffer layer in which the lattice constant and CET are matched with Si and III-V is a popular scheme of Si based III-V heteroepitaxy. This method can effectively suppress the dislocation extension from the bottom to the surface. As we know, Ge is most widely used because of its nearly the same lattice constant and thermal expansion matching between

GaAs and Si. There is much research on optimization of growth process parameters. Yu et al. [64] investigated the growth of GaAs epitaxy on Si substrates with a Ge buffer. Before growing GaAs on the Ge buffer, an arsenic pre-layer was deposited with graded temperature ramped from 300 to 420 °C. Their results display that the TDD of GaAs was significantly reduced by inserting the Ge buffer. They demonstrated a graded-temperature arsenic pre-layer to improve the surface roughness to 1.1 nm, and a low V/III ratio of 20 to suppress the interdiffusion between Ge and GaAs, earning an APB-free GaAs epitaxy with the TDD of 2×10^7 cm^{-2}. Zhou et al. [91] also grew 450 nm GaAs films on miscut Ge-on-Si substrates by MOCVD using a two-step epitaxial method. They found that a 3 nm initial thin buffer layer is critical for the suppression of anti-phase boundaries and threading dislocations. The polishing process is essential to remove the ultrathin LT- GaAs, obtaining a smooth surface for HT-GaAs layer growth. Finally, high-quality GaAs top layers with a low TDD of 2.25×10^5 cm^{-2} and the RMS less than 1 nm were obtained. Figure 11a shows the cross-sectional TEM images of GaAs/Ge/Si. Threading dislocations are restricted at the Ge/Si interface, as shown in Figure 11b. At the same time, heteroepitaxy of GaAs on the Ge surface is not the source for threading dislocation because of the little mismatch between Ge and GaAs. In Figure 11c, APBs were inhibited in the initial thin LT-GaAs buffer layer owing to the double-atomic Ge steps and high temperature annealing (>700 °C) under arsine.

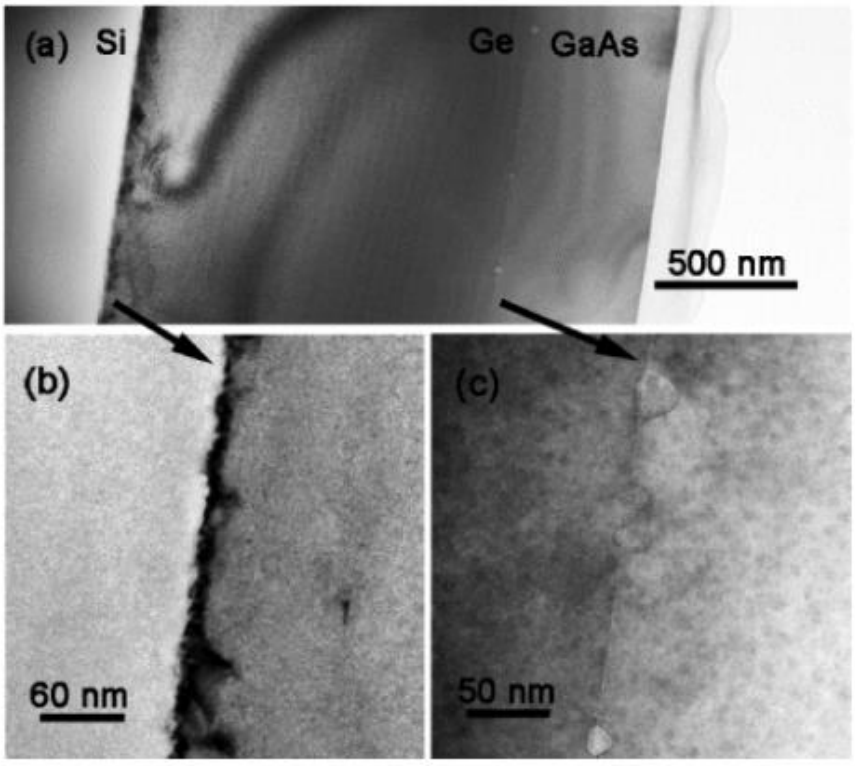

Figure 11. (**a**) Cross-sectional TEM images of GaAs/Ge/Si; (**b**,**c**) are the interface of Ge/Si and GaAs/Ge, respectively. Reprinted with permission from ref. [91]. Copyright 2014 IOP Publishing.

The growth of GaAs is very sensitive to roughness and strain of the buffer layer. Therefore, it is necessary to optimize the Ge buffer layer before III-V epitaxy. Bogumilowicz et al. [77] investigated the effect of the Ge buffer layer with different thickness on the threading dislocations in GaAs epitaxial layers. First, a range of 0.36 and 1.38 μm thickness of the Ge buffer was grown on the miscut Si substrate. The results displayed that increasing the thickness of the Ge buffer results in a decline RMS value of 0.5 nm. Based on this optimized Ge buffer, a smoother 0.27 μm GaAs was obtained with a RMS less than 1 nm and low defect density of 3×10^7 cm^{-2}. However, a thicker Ge + GaAs epitaxial stack produced a linear increase in the wafer curvature, which causes a bow of the substrate. This bow may introduce huge strain inside the wafer, which further deteriorates the surface roughness of GaAs and the

following device performance. Figure 12 shows the surface morphology of GaAs layers grown on different thicknesses of Ge-buffered Si (001) substrates. The thicknesses of the Ge buffer layer are: (a) 357 nm, (b) 764 nm, (c) 1377 nm, respectively. From the scale and the crystallographic directions, Figure 12b presents low APB density and surface roughness; the APBs' linear density decreased rapidly as the thickness of Ge changed: 0.4 μm^{-1} for the 357 nm Ge buffer down to 0.1 μm^{-1} for the 357 nm Ge buffer and less than 0.1 μm^{-1} for 1377 nm Ge. Subsequently, Du et al. [92] also confirmed this conclusion on the influence of Ge thickness variation on the TDD of the GaAs epitaxial layer.

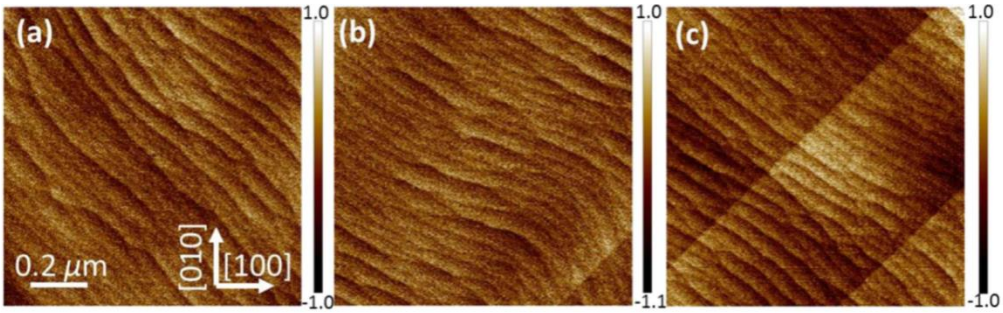

Figure 12. AFM images of GaAs layers grown on Ge-buffered Si (001) substrates. The Ge buffer thickness increased from (**a**) 357 nm up to (**b**) 764 nm and finally (**c**) 1377 nm. Reprinted with permission from ref. [77]. Copyright 2016 Elsevier BV.

4.1.3. TDD-Reduction of III-V by Thermal Annealing

However, the engineered Ge buffer on the Si substrate always exists with large strain, which is difficult for the following GaAs growth. Therefore, the graded $Si_{1-x}Ge_x$ buffer layer was used for GaAs to grow on the Si substrate, owing to offering efficient strain relaxation, and therefore a final Ge cap layer serves as a virtual substrate for GaAs growth. For a graded $Si_{1-x}Ge_x$ buffer grown on Si, a slow increase in Ge composition layers can induce a low number of "glissile" TDs. These effective "glissile" dislocations can increase the segment length of misfit dislocation, which accelerates the strain release. Thereby, the nucleation of new TDs is minimized. Meanwhile, the composition gradient dislocation can bend over and slip during the multilayer and then obtain the upper epitaxial layer with low TDD. Boeckl et al. [93] applied UHVCVD technology to prepare the Ge_xSi_{1-x} buffer layer on the Si substrate, and obtained a GaAs/Si epitaxial layer with a penetrating dislocation density of 10^6 cm^{-2} magnitude. After that, substantial efforts were devoted to achieving artificial $Ge/Ge_xSi_{1-x}/Si$ substrates [94,95]. However, a final Ge layer of composition 100% typically takes 10 μm of epitaxial growth when it is almost fully relaxed theoretically. A thicker buffer layer will not only result in a material consumption, but also be an incompatibility with the small CMOS devices. More important, thermal strain will be introduced during the high temperature ramping down, which increases the roughness of the final product surface [96]. In addition, in order to obtain a smooth surface in rough Ge/GeSi buffers for III-V growth, a chemical-mechanical polishing (CMP) process was used, which can decrease the TDD, but increase the fabrication cost [97].

The thermal annealing (TA) method is indispensable to reduce defect density during growth, enabling thermally activated dislocation migration and thus the annihilation of dislocations. Indeed, the TA-induced reduction of TDD in III-V/Si has been substantially investigated [98–101]. Barrett et al. [101] investigated the post growth annealing (PGA) effect on growing GaAs films on Si (001). He studied the effect of an ex situ post-growth annealing temperature range of 550–700 °C and time on the dislocation density of the GaAs layer. They found that the APB density was reduced ten times when the annealing temperature is above 650 °C. Figure 13 shows the plots of the APB density for different annealing conditions. Obviously, APB density decreases rapidly to a nonzero value after the higher temperature annealing at 650 °C and 700 °C, but for low annealing temperature, the APB density is still large even with a longer annealing time. The mechanism may be

explained by the energetics of APB habit planes. High annealing temperature has sufficient energetics to propel the APB slip on {110} type planes [100].

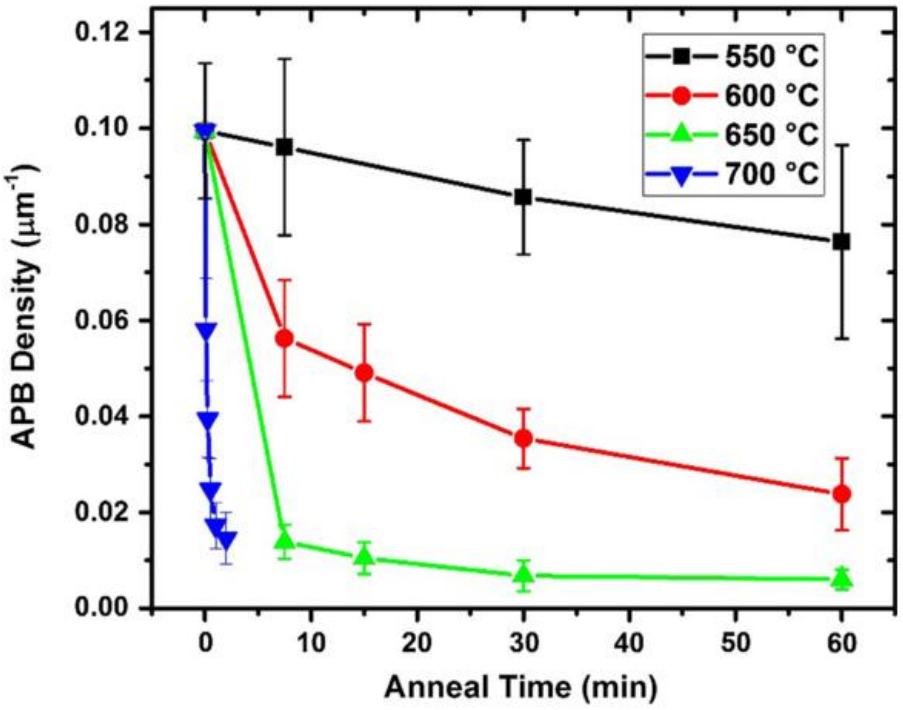

Figure 13. Plot of surface APB densities in the GaAs layer for different annealing conditions. APB density consistently decreases with increasing anneal time and temperature. Reprinted with permission from ref. [101]. Copyright 2019 Springer Nature.

Yet, previously reported annealing temperatures are either thermocouple target temperatures or ambient temperatures in the furnaces. Compared with post annealing, thermal cyclic annealing (TCA) is more conducive to defect elimination and strain relaxation. Callahan et al. [99] investigated the thermal cycle annealing (TCA) effects on the defect reduction in GaAs/Si, and reported that the dislocation density was considerably reduced to 2×10^6 cm^{-c} as the annealing temperature and cycling number increased. His results revealed that the thermally induced stress as a driving force of dislocation motion contributed to the dislocation annihilation, such as coalescence. Meanwhile, based on their numerical analysis, an excellent quality of GaAs layers with a low TDD of 10^5 cm^{-2} would be realized if the thermal cycle annealing is carried out more than 1000 times. Recently, Shang et al. [102] grew a GaAs layer through an in situ thermal cycle annealing (TCA) in the chamber to investigate the effect of TCA times on the reduction in TDD of the GaAs-on-Si template. Figure 14 shows the plot of the TDD with a different TCA process. We can see in Figure 14a that increasing the times of the TCA can reduce the TDD of the GaAs obviously, but a higher TCA of 735 °C enables a minimum TDD of 3.7×10^7 cm^{-2} after 12 cycles of TCA. The mechanism is that times of TCA can prompt the TDs slip, offset or propagate to the edge of the wafer, resulting in a low thermal mismatch strain. However, a higher annealing temperature above 745 °C causes catastrophic degradation of the GaAs surface owing to the formation of a Ga droplet, as shown in Figure 14b. Figure 14c shows the comparison of ECCI images of the surface of GaAs before and after cycles of TCA. It is clearly seen that the TDD was reduced from 4.18×10^8 cm^{-2} to 3×10^7 cm^{-2} after 16 cycles of TCA.

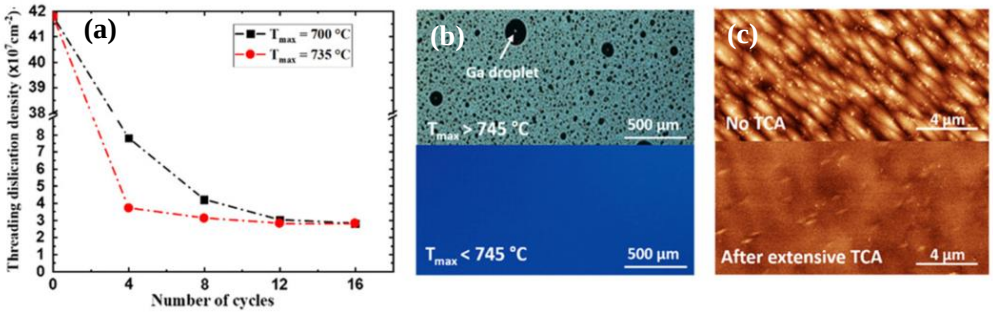

Figure 14. (**a**) TDD of the TCA process of GaAs-on-Si template. The minimum TDD achievable via TCA at the given GaAs thickness is about 3.7 × 10^7 cm^{-2}; (**b**) Nomarski microscope image of the GaAs surface after annealing above and below 745 °C temperature. Gallium droplets are observed when T max is higher than 745 °C; (**c**) ECCI images of the as-grown GaAs with no TCA (top) and after 16 cycles of TCA (bottom). The TDD is about 4.18 × 10^8 cm^{-2} with no TCA and decreases to 3.7 × 10^7 cm^{-2} after extensive TCA. Reprinted with permission from ref. [102].

For the InP/Si, TA has also been applied to improve the crystal quality [103]. However, the effect of thermal annealing on the defect reduction is not as dramatic as in GaAs/Si because the difference in CTE between InP and Si is relatively small; thus, the dislocation motion by thermally driven strain is limited.

4.1.4. TDD-Reduction of III-V by Multi-Step Epitaxial Growth

Multi-step epitaxial growth is a modified conventional two-step growth method, which inserts the Intermediate temperature (IT) layer between the LT and HT layer, and was commonly employed in recent years [104–106]. The two-step growth is a low temperature nucleation layer and high temperature growth layer. The purpose of the low temperature nucleation layer is to ensure sufficient time for the initial three-dimensional fusion to reduce the surface roughness and promote the fusion between the dislocations, thereby limiting the dislocation movement and reducing the penetration depth. However, the instability of the initial nucleation layer in low temperature growth makes harsh growth conditions for the high temperature growth; therefore, it is difficult to grow III-V materials stably with low surface roughness and defect density. Multi-step epitaxial growth such as three-step or four-step, which insert intermediate temperature growth, helps to prevent nuclear island forming in a metastable state from being reconstructed or damaged at high temperature. Wanarattikan et al. [87] studied the effect of the process of two-step growth and one-step growth on GaAs buffer layers using miscut Ge substrates. They designed the two-step growth with: low temperature growth at 470 °C and high temperature growth at 580 °C. Their results presented that compared with the one-step growth process at a temperature of 550 °C, two-step growth of the GaAs process exhibited a lower TDD value by about three times; the lowest APB density is 2.7 × 10^7 cm^{-2}. In following, a multi-step growth process was also studied. Wang et al. [105] demonstrate the three-step growth of GaAs on the Si (001) substrate in a low-pressure metal organic chemical vapor deposition reactor compared with two-step growth. To decrease the TDD further, TCA was also introduced for comparison. They designed their three-step growth process as: a 70 nm-thick initial LT-GaAs nucleation layer was grown at 420 °C, a 300 nm MT-GaAs epilayer grown at 630 °C, and then a 1.5-µm-thick HT-GaAs epilayer grown at 685 °C. Table 1 is different characteristic data of GaAs/Si samples grown with different procedures. Compared with the two-step growth, the TDD and RMS values of GaAs were reduced obviously by three-step growth. Meanwhile, the combination of three-step growth with two TCA steps can further improve the surface morphology and crystal quality of metamorphic GaAs. A TDD of only 1.1 × 10^7 cm^{-2}, EPD of 3 × 10^6 cm^{-2}, and the smallest RMS of 1.8 nm can be obtained via this Combinatorial method.

Table 1. Different characteristic data of GaAs/Si samples grown with different procedures. Reprinted with permission from ref. [105] Copyright 2013 American Vacuum Society.

Samples	Growth Procedure	DCXRD $\omega-$Scan FWHM (arcsec)	RMS Roughness in 10×10 μm^2 (nm)	TDD (cm^{-2})
A1	Two−step growth	327.5	2.9	4.4×10^7
A2	Two−step growth + one TCA step	210.2	2.5	1.9×10^7
B1	Three−step growth	298.2	2.4	3.7×10^7
B2	Three−step growth + one TCA step	184.3	2.0	1.4×10^7
B3	Three−step growth + two TCA steps	164.2	1.8	1.1×10^7

According to the above, although three-step growth can reduce the RMS of the GaAs surface to 1.8 nm, it still cannot meet the requirements of device preparation. In 2021, Du et al. [47] also investigated the three-step growth of GaAs on both 0°—and 6°—miscut Si substrates with an engineered Ge buffer. First, a flatter Ge buffer layer was obtained through CMP, which is more favorable for GaAs growth. The conventional two-step growth process was low temperature at 460 °C, high temperature at 670 °C. The results of the two-step growth displayed a foggy surface of GaAs with the RMS of 3.4 nm. Then, an intermediate temperature at 600 °C was inserted between low and high temperature growth of GaAs to impede the defects to propagate to the HT layer. Figure 15a–d show the GaAs surface morphology of a comparison of the two-step with three-step growth on 0° and 6° miscut Si substrates. The three-step growth process can obviously eliminate the pits (TDs) on both substrates, but APB strips still exist on 0° miscut Si substrates. In other words, APB-free GaAs film with a low TDD of 7.4×10^7 cm^{-2} and RMS of 1.27 nm could be obtained on 6°− miscut Si substrates by three-step growth.

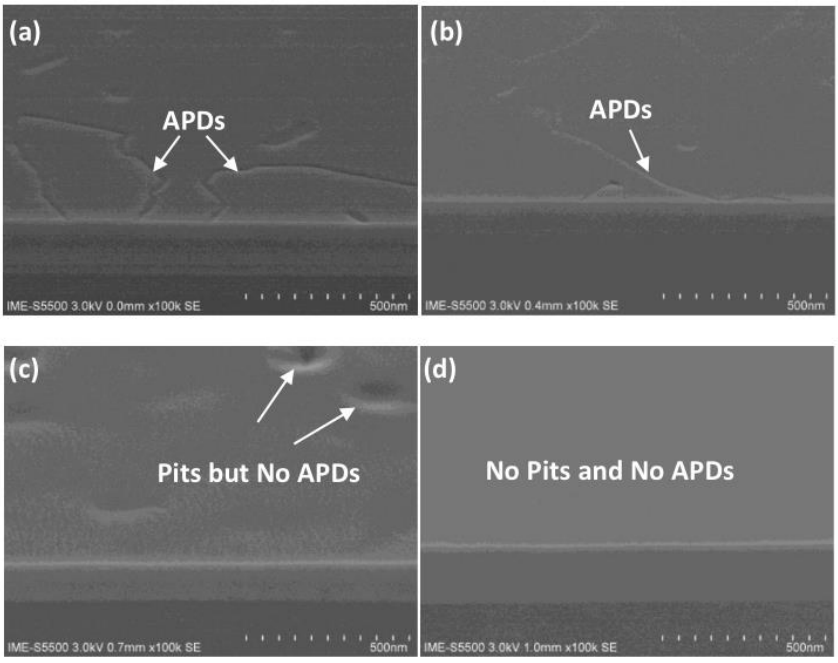

Figure 15. The SEM plan view images of GaAs (**a**) two-step growth on 0° miscut Si substrates and (**b**) three-step growth on 0° miscut Si substrates; (**c**) two-step growth on 6° miscut Si substrate, (**d**) three-step growth on 6° miscut Si substrate. Reprinted with permission from ref. [47]. Copyright 2021 Springer Nature.

For the InP/Si, direct growth of InP on Si produces a much higher TDD than that of GaAs on Si; a two-step growth is difficult to obtain a flat InP surface [107]. However, our group is developing the high-quality InP epitaxial layer on a 200 mm miscut Si platform using the multi-step growth technique, which has an APB-free InP-on-Si substrate. These breakthrough results will be submitted later.

4.1.5. TDD-Reduction of III-V by Inserting Strained-Layer Superlattices Layer

Recently, strain-layer superlattices (SLs) were employed as dislocation filter layers (DFLs) to filter the dislocations' density by bending the dislocation direction with the strong strain field around the quantum well (QW) or 3D quantum diots (QDs) [108–110]. The detail mechanism of dislocation being filtered and eliminated by SLs is explained in part III. Ternary-binary SLSs DFLs are widely used in III-V/Si heteroepitaxy, including InGaAsAs/GaAs, InAlAs/GaAs, InGaAs/InP, and so on [111–114]. For instance, Tang et al. [115] compared InAlAs/GaAs and InGaAs/GaAs (SLSs) as dislocation filter layers to grow 1.3 μm InAs/GaAs quantum dot laser structures on Si substrates. Two types of SLSs are designed as: five-period of 10 nm $In_{0.15}Ga_{0.85}As$/10 nm GaAs and five-period of 10 nm $In_{0.15}Al_{0.85}As$/10 nm GaAs, respectively. Figure 16a–c shows the cross-sectional TEM of low magnification of two different SLs layers. We can see that free dislocations of GaAs layers are visible after the insertion of InAlAs/GaAs SLSs in Figure 16b, but a few dislocations are also exist in GaAs layers after the insertion of InGaAs/GaAs SLSs in Figure 16a. TDD reduction of the GaAs after insertion of different types of SLSs was also characterized by TEM and EPD in Figure 16c, respectively. After three sets of InAlAs/GaAs SLSs, the GaAs sample shows an average defect density of about 2.0×10^6 cm $^{-2}$ while the one with InGaAs/GaAs SLSs has about 5.0×10^6 cm^{-2}. In addition, photoluminescence (PL) also verified that the sample with InAlAs/GaAs SLSs is about two times stronger than that with InGaAs/GaAs SLSs, which means that InAlAs/GaAs SLSs are more effective in blocking the propagation of threading dislocations than InGaAs/GaAs SLSs under the similar growth conditions.

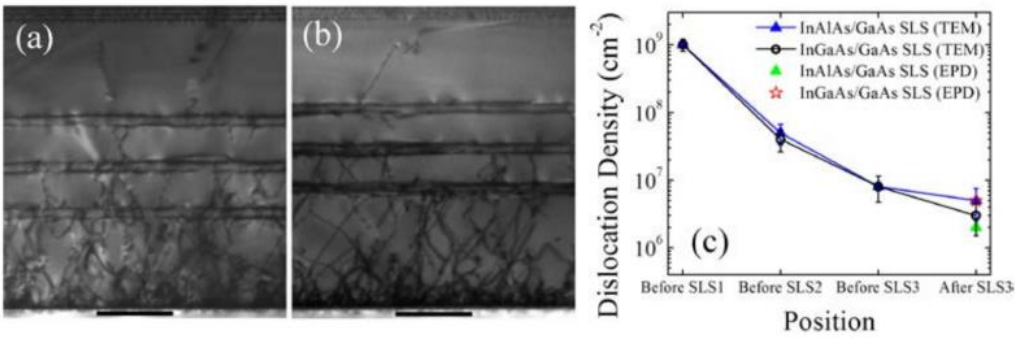

Figure 16. Cross-sectional TEM dark field images of (**a**) InGaAs/GaAs SLS and (**b**) InAlAs/GaAs SLS. (**c**) Reduction in dislocation induced by the SLS layers measured at different positions. Reprinted with permission from ref. [115].

The changing of composition of SLSs materials can affect the band potential barrier, which has an important impact on defects' limitation. Later, Tang et al. [116] investigated the indium composition and thickness of In_xGa_{1-x} As/GaAs SLSs for 1.3 μm QD lasers on Si. They designed the efficacy of indium composition x which were 0.16, 0.18, and 0.20, and the thickness of GaAs were 8, 9, and 10 nm. To improve the effectiveness of InGaAs/GaAs DFLs, two different growth methods were introduced in Figure 17a,b. In growth method I in Figure 17a, a GaAs spacer layer was grown during the period of heating up to 610 °C right after the deposition of InGaAs/GaAs SLSs at 420 °C. In contrast, in growth method II, the GaAs spacer layer was grown after in-situ annealing of the SLSs at 610 °C in Figure 17b. In Figure 17c, the PL peak intensity of the QD laser structure with growth method II was at least three times higher than that with growth method I. This improvement can be attributed to the high-temperature growth of the GaAs spacer layer

and in-situ annealing of SLSs. It is also revealed that the optimized indium composition and GaAs thickness in SLSs were 0.18 and 10 nm, respectively. In Figure 17d, it was shown that the employment of three sets of $In_{0.18}Ga_{0.82}As$/GaAs SLSs DFLs effectively blocked and annihilated the TDs. In addition, the UCSB team [113] grew the GaAs layer on the GaP-engineered Si substrate using $In_{0.1}Ga_{0.9}GaAs$/GaAs strain super-lattices (SLSs). The $In_{0.1}Ga_{0.9}GaAs$/GaAs SLSs can further reduce the penetration dislocation density in the GaAs buffer layer to 7.3 × 10^6 cm^2.

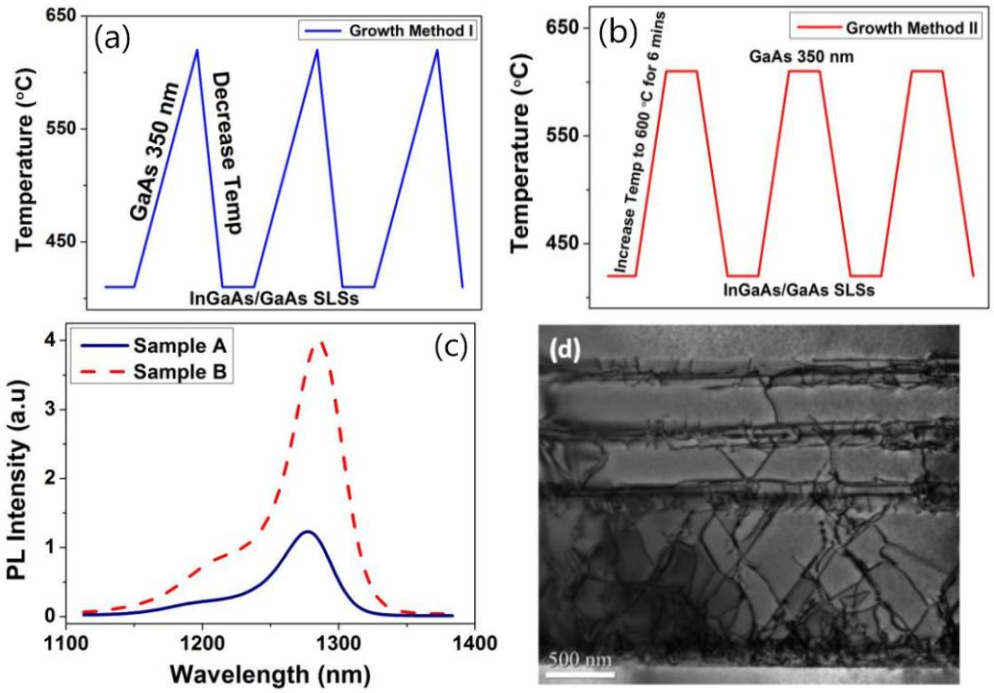

Figure 17. (**a**) Growth method I; (**b**) Growth method II; (**c**) PL spectra measured at room temperature for the two sample; (**d**) Dark-field cross-sectional TEM image of optimized In0.18Ga0.82As/GaAs SLSs DFLs. Reprinted with permission from ref. [116]. Copyright 2016 IEEE.

In the InP/Si platform, the DFLs based on InGaAs/InP, In(Ga)AsP/InP, (In)GaP/InP [117,118] were also commonly adopted. In 2020, Klamkin et al. [107] reported their advanced InP-on-Si virtual substrate which is optimized by inserting $In_{0.73}Ga_{0.27}As$ (13 nm)/InP (19 nm) 10-pair SLSs on the GaAs-on -V-grooved Si (GoVS) template. In this report, InP buffer layers were first grown on the GoVS template using multi-step growth, followed by four sets of InGaAs (13 nm)/InP (19 nm) 10-pair SLSs with 300-nm-thick InP spacer layers. Figure 18a shows the cross-sectional STEM image of the InP-on-Si template and the extracted dislocation density at various growth stages. Six lines are the different growth stages. First, at low temperature growth of InP on the GoVS substrate, many dislocations are visible at the interface of GaAs and InP; the TDD is in the order of 10^{10} cm^{-2}. After the three-step growth of InP (line 2), a large number of TDs are annihilated and coalesced, leading to a reduced defect density of approximately 1.5 × 10^9 cm^{-2}. In following, a higher set of SLSs is inserted to filter dislocations, which can be seen in the image that the TDs decrease after the multi-SLSs insertion. Figure 18b shows the plot of the TDD value with the various growth stages. The dislocation filtering efficiency is enhanced for the higher set of SLSs; the final InP surface TDD is reduced to 1.17 × 10^8 cm^{-2} after four sets of InGaAs/InP DFLs (line 6). The final InP surface morphology was also characterized by ECCI in Figure 18c. APB-free and low TD were present, but few SFs and pinholes appear. The counted densities for TDs, SFs, and pinholes were 6.9 × 10^7 cm^{-2}, 1.1 × 10^7 cm^{-2}, and 3.5 × 10^7 cm^{-2}, respectively. Such pinholes are mainly due to the fact that higher SLSs also introduce new dislocations. It was revealed that InGaAs/InP SLSs can obviously reduce the TDD to 10^7 cm^{-2}, but they formed a rough surface with many hillocks.

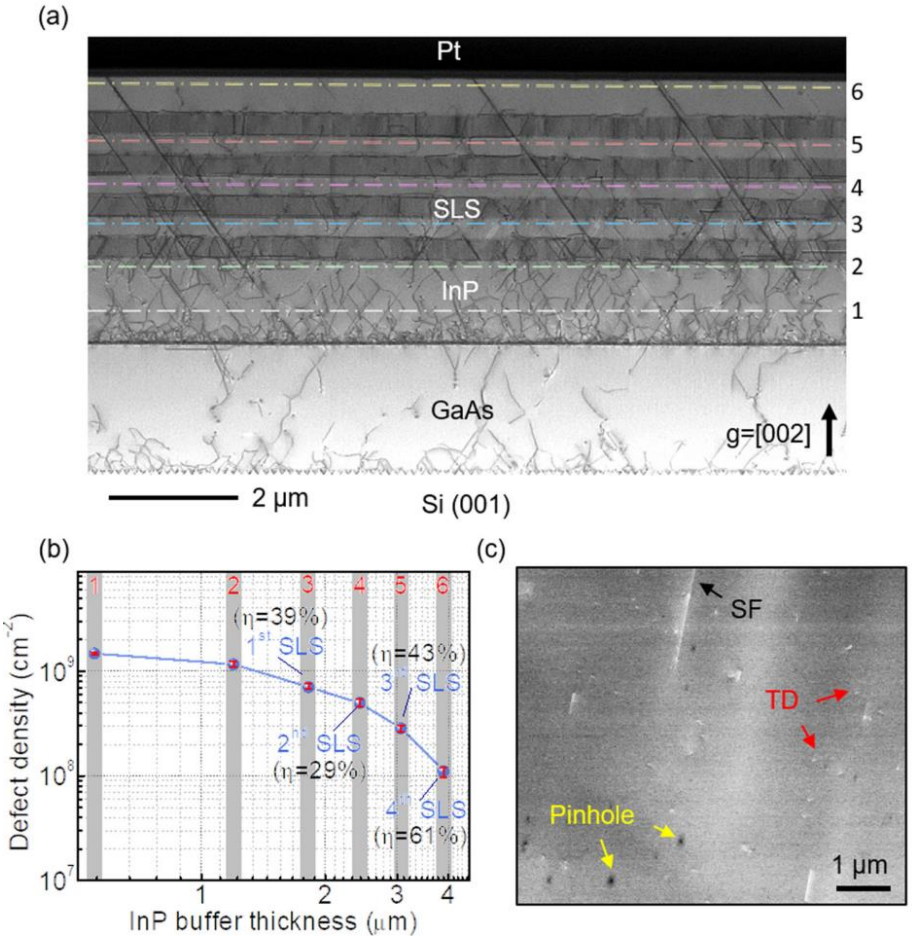

Figure 18. (**a**) Cross-sectional STEM image of the InP-on-Si template to demonstrate the generation and propagation of threading dislocations and stacking faults; (**b**) Extracted dislocation density as a function of the InP buffer thickness at various growth stages. (**c**) Typical ECCI image of the InP surface, where different kinds of defects can be identified and counted. Reprinted with permission from ref. [107]. Copyright 2020American Institute of Physics.

In addition, the self-assembled QDs can be used as DFLs to filter the TD of the InP/Si layer. Because the strain-driven self-organized QDs produce a large three-dimensional strain field around themselves, dislocations around QDs can be bent over and annihilated in a similar way to SLSs DFLs. Shi et al. [119] grew the InP layer on the GaAs-on-Si substrate by inserting optimized multiple InAs/InP QDs as DFLs. They inserted two periods of five-layer InAs/InP QDs dislocation filters to obtain a smoother surface before the subsequent QD stack growth during the HT-InP layer growth. A RMS roughness of 2.88 nm of a binary InP layer can be obtained, minimizing the generation of large InAs islands. Figure 19a shows the cross sectional of InP on planar Si inserted with two periods of five-layer InAs/InP QD DFLs. The structure of InP and the InAs/InP DFLs layer are observed clearly. Figure 19b shows the effect of InAs/InP DFLs on defect elimination by TEM images. It can be seen that the TDD is bent and eliminated by the first five-layer InAs/InP QD DFLs, but sufficient defects can still propagate upward to the top surface. After the second stage of QD DFLs, very few TDs can be detected, and most of the defects are propelled or pinned by the stacked QDs, leading to either annihilation or coalescence of the TDs. Finally, a low defect density of 3×10^8 cm^{-2} was achieved for the InP-on-Si substrate.

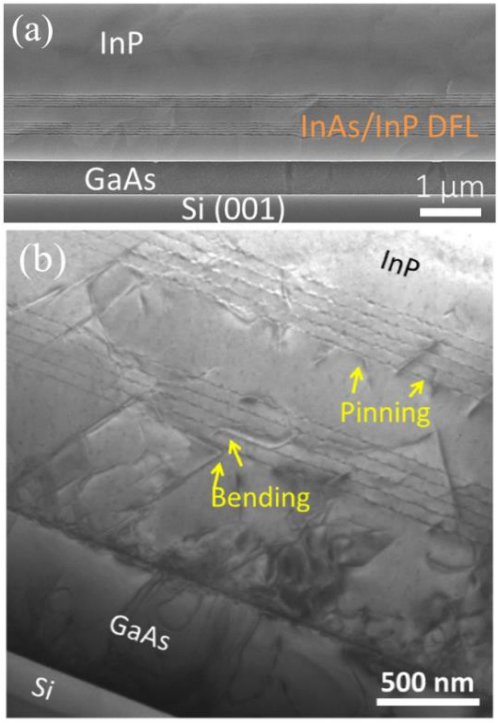

Figure 19. (**a**) Cross-sectional SEM of InP layer grown on planar GaAs/Si by inserting two periods of five-layer InAs/InP QD DFLs; (**b**) cross-sectional TEM images of InP grown on planar GaAs/Si by inserting two periods of five-layer InAs/InP QD DFLs. Reprinteed with permission from ref. [119]. Copyright 2018 AIP Publishing.

Adopting SLSs' dislocation filter to reduce the TDD also was used with the selective epitaxial technology recently. For instance, Norman et al. [120] obtained the GaAs/Si epitaxial layer by SEG; the $In_{0.15}Ga_{0.85}As$ SLSs dislocation filter was grown on the V-groove graphic substrate. ECCI shows a low dislocation density as 2×10^7 cm^{-2}.

4.2. III-V Thin Films Selective Epitaxial Growth on Si Wafer-Scale

However, the miscut Si substrates are not popular in current industrial process flows because of the high consumption and are incompatible with advanced Si manufacturing technologies. Thus, some researchers explore other methods to reduce the problem of APBs in epitaxial GaAs layers on nominally on-axis Si (001) wafers.

Selective epitaxial growth (SEG), allowing the epitaxial layer to grow on the pre-defined region by substrate patterning, offers additional control over the strain relaxation process to control the dislocation. Aspect ratio trapping (ART) is the most common method of SEG owing to the simplicity of design. This epitaxial technology, through a high depth-width ratio, limits the dislocation and other defects originating from the Si surface to the bottom of the groove by using the SiO_2 sidewall, so as to obtain high-quality, dislocation-free III-V materials at the top, which greatly reduces the dislocation density in the materials. The ART template can be made by STI technology from traditional CMOS processes, which can realize the monolithic integration of III-V group materials and Ge materials on the Si substrate.

4.2.1. Aspect Ratio Trapping Technology (ART)

The original concept of ART for epitaxial III-V on the silicon substrate was proposed by Fitzgerald in 1991 [121]. At that time, this idea was called the "epitaxial necking effect": They point out that the {111} crystal plane family is the slip plane in the zinc-blende lattice structure, and the TD is mainly along the {111} plane, which develops a 45° with plane (001). So, when the width of the selected area is less than the thickness of the epitaxial

material, the TD will reach the edge of the material and terminate. The method was firstly revealed in Ge/Si hetero-epitaxy [122] and then applied to III-V/Si epitaxy. Bai et al. [123] introduced the ART method directly to GaAs epitaxy on silicon. They first deposited SiO_2 on silicon with a certain thickness and then etched along the [110] direction to reach a certain surface of the silicon substrate width of grooves. The SiO_2 side wall of the groove limits the development of TD from the GaAs-silicon interface; part of GaAs has almost no defects, as shown in Figure 20. In Figure 20a, a lot of dislocations are visible at the interface of GaAs/Si, and gradually limited within the SiO_2 trenches, then completely terminated within the first 200 nm of GaAs growth. The schematic of initial coalesced GaAs growth and coalesced GaAs growth is shown in Figure 20b.

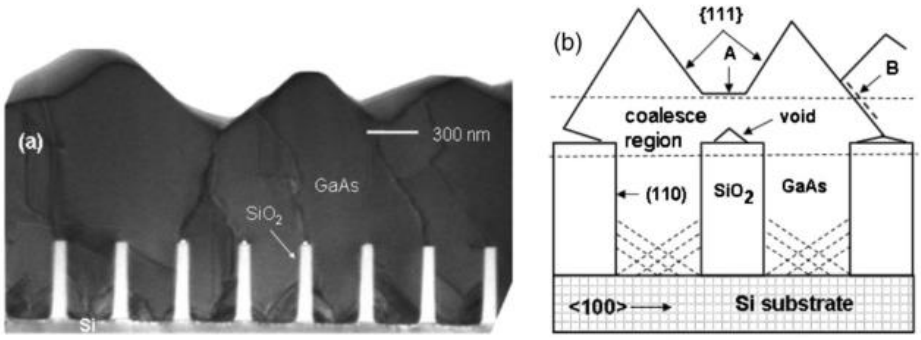

Figure 20. (**a**) Cross-sectional TEM image of GaAs grown on ART patterned Si; (**b**) coalesced GaAs grown and the schematic illustration of coalesced GaAs growth. Reprinted with permission from ref. [123]. Copyright 2008 American Institute of Physics.

Although the above SiO_2 mask can limit the development of TDD, the APBs are still generated, which bring defects to the materials and limits the photoelectric properties. Therefore, TDD and APB are further reduced by introducing a buffer layer. Li et al. [124] investigated the growth of GaAs layers on polished Ge/Si by selective ART. They first grew the Ge layer on the patterned SiO_2 substrate, then deposited GaAs on the SEG Ge buffer layer. Figure 21 shows the layer structure. Their results indicated that APB-free GaAs can be obtained only on a polished SEG Ge buffer layer on the exact (001) Si substrate. Figure 21b shows the APB surface of GaAs when grown on a non-polished SGE Ge buffer layer. In Figure 21c, an APB-free of 1 μm GaAs layer was obtained with the full-width at half-maximum (FWHM) is only 140 arcsec. The significant APB reduction in the GaAs layer was attributed to the nature of SEG-based Ge growth, which results in a virtual miscut Ge surface after CMP. However, hard-to-control asymmetry of GaAs facets and the thicker structural layer are not conducive to device integration which remains a problem.

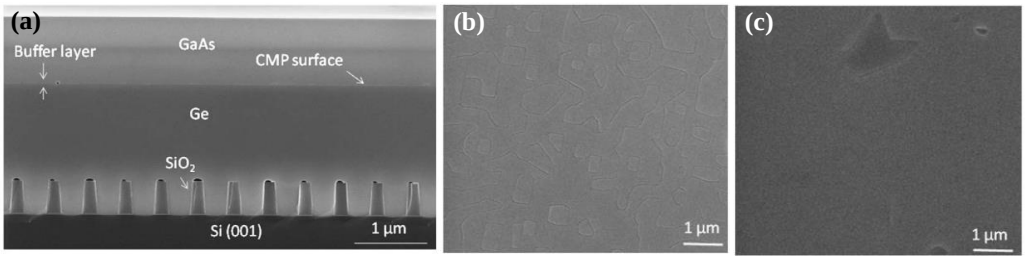

Figure 21. (**a**) Cross-sectional SEM image of GaAs overgrown on polished SEG Ge buffer layer on patterned Si (001) substrate. (**b**) Plane view of GaAs surface grown on exact oriented (001) Ge substrate and (**c**) on polished SEG Ge/Si substrate. Reprinted with permission from ref. [124]. Copyright 2009 Elsevier BV.

In order to resolve this problem, a thin buffer layer is grown in the groove to selectively continued III-V materials. Wang et al. [125] demonstrated the SEG method of high-quality InP layers in submicron trenches on normal Si substrates using a thin Ge buffer layer.

Figure 22 shows the cross-sectional TEM images of the SEG InP layer in 100 nm STI trenches. {111} and {311} facets are visible after the Si process. Then, a thin Ge buffer layer was deposited to form a relatively round surface. This rounded Ge surface removes facets, and the SEG InP grows following the Ge surface in a step flow growth mode; thus, a different crystal orientation can be avoided, which can solve the problem of voids' formation. Meanwhile, an annealing process can prompt the single surface steps of Ge to migrate and merge into double steps, which is essential to avoid any APB formation. In addition, many threading dislocations' TDs are confined at the side of the trench; an APB-free and low TDD InP layer is obtained at the top of the trenches.

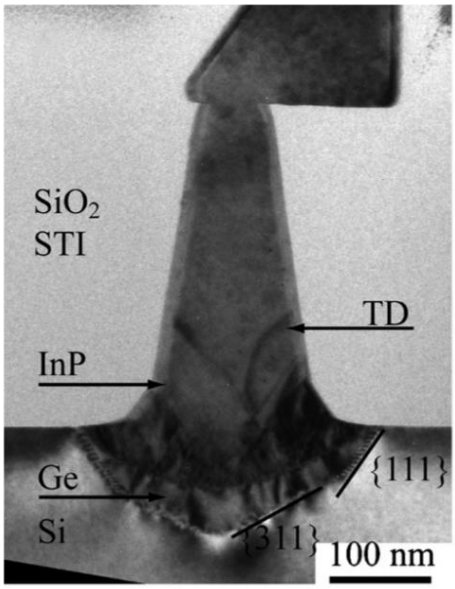

Figure 22. Bright field cross-section TEM images of InP grown in the 100 nm wide STI trenches. {111} and {311} Si facets were obtained after Si etch with HCl vapor. TDs are confined in the bottom of the trenches. Reprinted with permission from ref. [125]. Copyright 2010 American Institute of Physics.

Even though a pre-epitaxial Ge buffer layer is helpful to solve the APB, the quality degradation of III-V materials still cannot be completely eliminated because the diatomic steps cannot form naturally, spontaneously on the Si declination substrate and Ge buffer layer surface. Although the formation of diatomic steps can be promoted by certain pretreatment, it is still not guaranteed that all epitaxial interfaces are diatomic steps. When the III-V materials are deposited in the position without diatomic steps, there will always be possible APBs. The density of defects such as twin planes traveling along the trench direction is fairly high. In 2012, the IMEC group innovatively developed a method to construct natural diatomic step surfaces by pre-etching the silicon substrate at the bottom of the ART method SiO_2 groove into a "V" groove consisting of two {111} faces using an alkaline solution, which can effectively suppress the generation of APB in the III-V epitaxial layer [126]. Growing III-V materials on V-grooved (111) Si surfaces can greatly enhance the quality of epitaxial III-V materials in the ART process [127–134]. There are many advantages by the use of {111} Si V-grooves in the ART growth process. First, APBs can vanish in the V-grooves by the crystallographic alignment between the Si and III-V materials; secondly, compared with the Si (001) plane, little defects will generate when III-V materials nucleate on the Si (111) plane; thirdly, it can selectively grow the active region in any location on the silicon substrate, and the size and position of the active area can be controlled manually. Figure 23 shows the schematic diagrams of the III-V lattice in the "V-shape" of Si. Figure 23a shows III-V lattice in the V-shape of Si with {111} facets along the [110] direction [125], which have the same polarity, but in Figure 23b, a single step on the Si (111) surface is equal to the interplanar spacing of Si {111} planes; such steps might not lead to the formation of APBs in the III−V material.

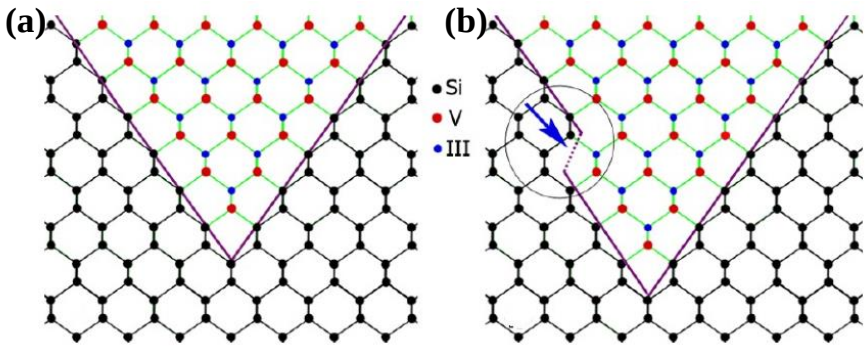

Figure 23. Schematic diagrams of III−V lattice in: (**a**) the "V-shape" of Si with {111} facets; (**b**) a monatomic step on a (111) plane. Reprinted with permission from ref. [126]. Copyright 2012 American Chemical Society.

Tommaso et al. [128] grew GaAs fins in sub-100 nm trenches patterned on Si (001) substrates using the ART approach. They demonstrated the trench bottom geometries in "V" shaped with a consequence of the NH_4OH etch. A 75 nm deep of the "V" shaped groove is formed with the presence of small {113} and (001) facets, which can minimize the interfacial energy and prevent the formation of APBs. Figure 24a–c display bright field STEM images of GaAs-on-V-grooved-Si in directions both perpendicular and parallel to the trenches. All TDs (meandering lines) are found annihilated on the oxide walls and confined at the trench bottom. Few {111} planar defects can be identified, and none of them reach the surface, suggesting the upper part of the inspected GaAs portion is free of defects.

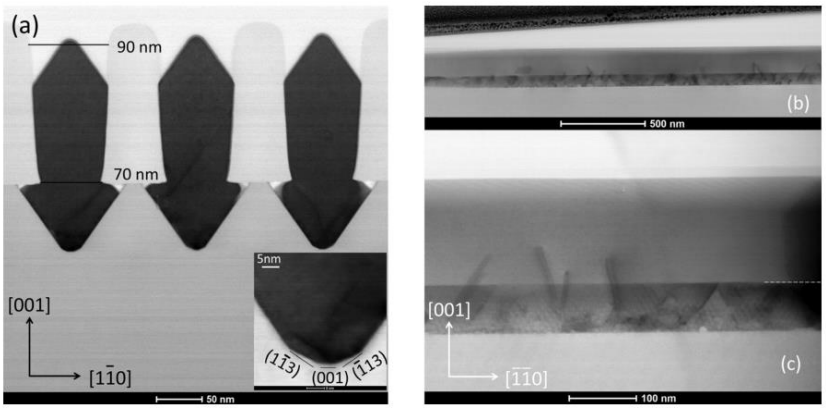

Figure 24. (**a**) Bright field STEM image of GaAs on V-grooved Si. Inset: High magnification bright field STEM image of the trench bottom [113] direction; (**b**,**c**) show low and high magnification bright field-STEM images of a cross section parallel to the trenches Reprinted with permission from ref. [128]. Copyright 2015 American Institute of Physics.

However, the defects of III-V material are also related to the structure of the groove and the growth process. The different aspect ratio also affects the limitation of material defects. Kunert et al. [50] reported that the GaAs fins selectively grow in a V-shaped trench with the aspect ratio of 7.5, 3, 1. Figure 25 shows a cross sectional SEM of the GaAs selectively grown in different ARs. In the case of the ARs being 7.5 and 3, all dislocation defects are trapped and confined inside the STI region in Figure 25b,c. However, for the ARs of 1 in Figure 25d, TD defects are also found above the trench, which indicates that an AR of 1 is not sufficient to block all dislocation. In fact, in these narrow trenches, the InP layer is very defective, with an extremely rough and discontinuous surface. As the surface treatment for wide and narrow trenches is identical, we must conclude that the geometrical confinement within the narrow trenches induces a transition from 2D to 3D growth.

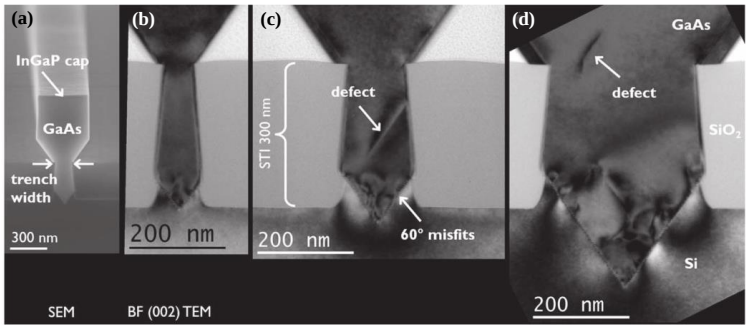

Figure 25. (**a**) a slightly tilted cross SEM image of a GaAs nano-ridge was deposited in 100 nm wide trenches capped with an InGaP cap; cross-sectional bright field TEM images of GaAs were grown in (**b**) 40 nm; (**c**) 100 nm; (**d**) 300 nm trench. Reprinted with permission from ref. [50]. Copyright 2018 IOP Publishing.

In the III-V compounds' semiconductor, InP global epitaxy on the Si substrate is rarely reported due to the difficulty of a huge 8% lattice mismatch. However, based on the advantages of ART technology, growing InP on silicon by the ART approach is common [132,133]. In the first place, the creation of {111}-oriented V-grooved pockets in trenches by this ART approach not only can prohibit the formation of APBs, but also promote strain relaxation via the formation of planar defects such as stacking faults. By designing the shape of the Si substrate, a highly twinned region is forming at the InP/Si interface, enabling a growth of active regions closer to the Si substrate. This twinned region is conducive to the strain relaxation when InP is deposited inside the V-grooved Si pockets. Moreover, InP can serve as a buffer layer for the growth of other III-V semiconductor compounds, such as InGaAs, InGaP. In the past few years, we summarize four growth schemes that were investigated by some researchers in Figure 26. Selective epitaxial growth of InP is deposited in different types of trench (V-grooved or rounded shape trench); different buffer layers (Ge, GaAs) are deposited for the growth of InP.

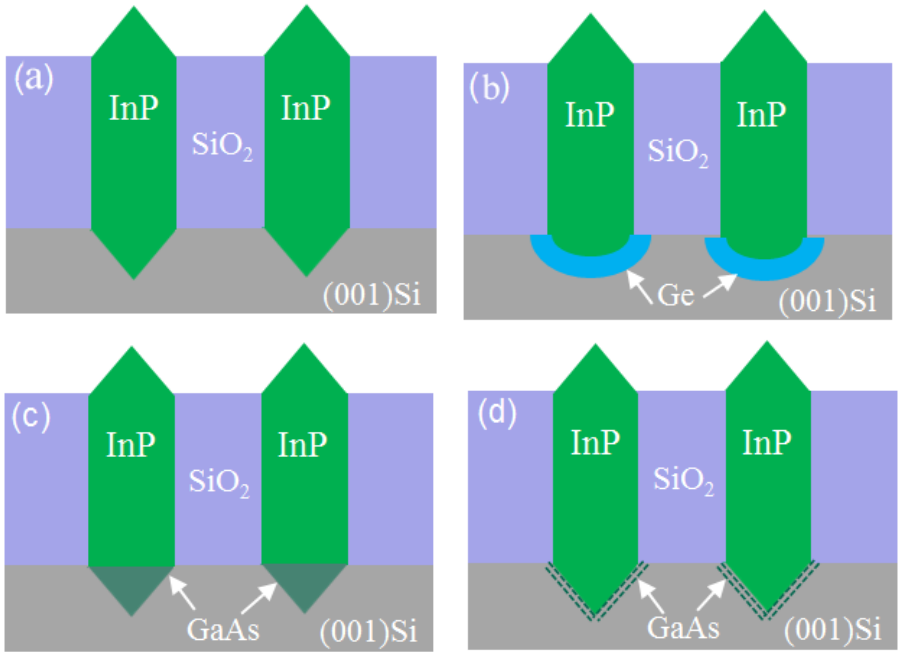

Figure 26. Four epitaxial schemes of InP on patterned Si using ART: (**a**) direct InP epitaxy on V-grooved Si; (**b**) InP on rounded Ge surface; (**c**) InP on a GaAs intermediate buffer filling up the V-grooves; (**d**) InP on a few–nanometer–thick GaAs stress relaxing layer.

Although the creation of {111}-oriented V-grooved pockets in trenches by this ART approach can prohibit the formation of APBs, the weakness of this method is that it is impossible to capture the (111) steering defect along the parallel direction of the groove. This defect can result in stacking fault, twins on the sidewalls, in the upper InP layer, which makes it impossible to obtain large-size plane InP layer. Merckling et al. [134] studied the impact of starting geometry at the bottom STI on the crystalline alignment of the InP layer. They explored the starting geometry at the bottom as rounded etch with Ge buffer versus a crystalline <111> V-groove structure in the Si; the model is in Figure 27a. Rounded Ge structure exhibits different crystallographic facets such as {001}, {111}, and {113}, instead only {111} crystallographic planes on V-groove structure. Different crystallographic facets in rounded Ge surface may provide a nucleation surface with a unique polarity, which is inconducive to grow better nucleation uniformity. Instead, Si V-groove {111} enclosure will provide a surface with a unique polarity. The quality of InP layer was quantitatively characterized by HRXRD. The extracted FWHM value shows broad diffraction peak from InP grown on rounded Ge/Si at 1690 arcsec, while a much narrower diffraction peak from InP grown on "V" shape Si is 540 arc sec. Meanwhile, scanning spreading resistance microscopy (SSRM) was used to measure the local electrical resistance of InP for different process in Figure 27b,c. It is clear that low resistance (high conductivity) of the Ge buffer region is observed in the bottom of the trench, but a much thinner and a higher resistance of the V-groove InP/Si interface. Their SSRM results displayed that the InP grew on a rounded-Ge surface exhibits a low resistance (high conductivity) in the ~10^6 ohms range in Figure 27b, while the resistance is clearly improved to ~5×10^7 ohms range by using a V-groove starting surface in Figure 27c. In other words, higher quality of InP layer was achieved by the use of a V-grooved Si starting surface. In addition, more TDs were generating from the round Si/Ge interface, periodically decorated with misfit dislocations, propagating in the III-V layer.

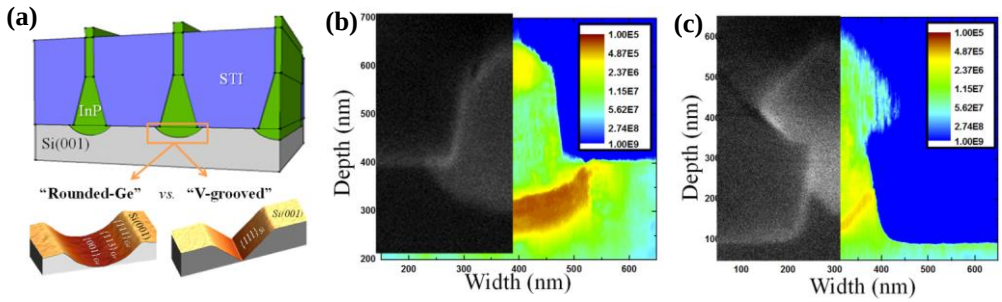

Figure 27. (**a**) Schematics of different starting surface (rounded-Ge and V-grooved Si) for the III-V growth on Si; Room temperature SSRM patterns in W = 80 nm trenches of InP epitaxially grown on **(b)** rounded-Ge and (**c**) V-groove Si starting surface. Reprinted with permission from ref. [134]. Copyright 2014 American Institute of Physics.

By mimicking the metamorphic InP/GaAs buffer on planar Si [135], GaAs and InP have the same crystal structure (sphalerite structure), which can reduce dislocation defects for the InP layer by using GaAs as the buffer layer. Figure 26c illustrates the model of a GaAs intermediate buffer layer. Li et al. [133] grew the high-quality uncoalesced thin films InP by MOCVD in SiO_2 trenches on Si (001) via the ART method. Addition of a V-grooved Si surface to the ART process can more effectively trap misfit defects and APBs at a GaAs/Si intermediate interface as shown in Figure 28. They first directly grew InP in a blanket Si substrate with a different thickness of the GaAs layer. The 30-nm-GaAs buffer was not sufficient to allow misfit dislocations to be trapped in the ART structure. APBs and stacking faults were also observed from the Si surface to the upper InP layer as seen in Figure 28a. In Figure 28b, a thicker 200nm single GaAs buffer can make the stacking faults and twins originate from the InP/GaAs interface along {111}, which effectively inhibited the defects and APBs. Then, V-grooved surfaces at the trench bottom were formed for InP ART. A

V-grooved feature would effectively increase the desired aspect ratio in the ART process and enable GaAs growth inside a pre-defined Si {111} enclosure, which can be expected to promote initial GaAs nucleation uniformity. From Figure 28c, it can be seen that high crystallographic quality of the InP is above the dotted line, where InP is essentially defect free. Figure 28d is the reference of InP global epitaxy on the exact (001) Si substrate, for which various mixed defects exist with high TDDs in the InP layer.

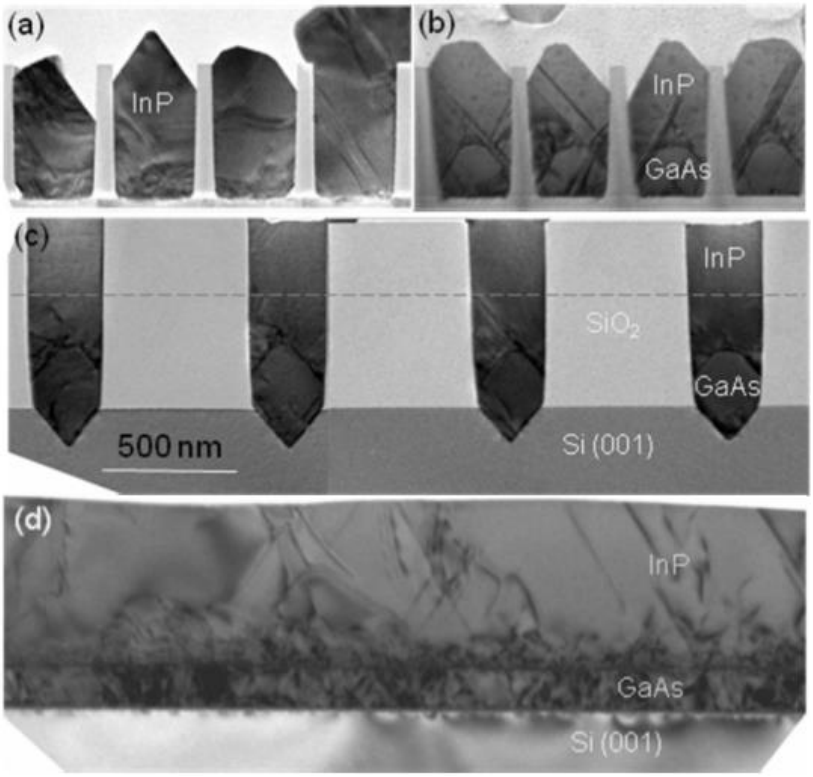

Figure 28. Cross-sectional TEM images of (**a**) InP/GaAs/Si with a 30 nm GaAs buffer layer; (**b**) InP/GaAs/Si with 200 nm intermediate GaAs layer; (**c**) InP/GaAs/Si structure with V-grooved Si surface and modified growth conditions and (**d**) same growth as (**c**) but grown on a Si (001) substrate. All images are to the same scale. Reprinted with permission from ref. [133]. Copyright 2009 IOP Publishing.

Bulk growth and quantum well (QW) are also induced as a dislocation filter to reduce TD in the ART technology further. Zhou [136] grew InP in nanoscale V-grooved trenches on the Si (001) substrate using InGaAs/InP multi-quantum-well by metal organic chemical vapor via the ART method. To obtain the best InGaAs quantum well potential barrier, a 60% In composition of InGaAs/InP MQW was deposited on InP/GaAs buffer layers in nanoscale V-grooved trenches. Figure 29 shows the cross-sectional TEM image of the sample. Highly uniform InGaAs/InP MQWs were visible over different trenches in Figure 29a. Few defects propagated through the GaAs/InP buffer layer to the MQW region in Figure 29b. From the magnification of InGaAs/InP MQW and the InP contact layer part, a clearly identified line and no crystalline defects are observed in Figure 29c. The four periods of 3 nm/6 nm InGaAs/InP QWs are observed with fine periodicity, flat and sharp interfaces in an atomic size, which indicated the highest quality of materials in Figure 29d.

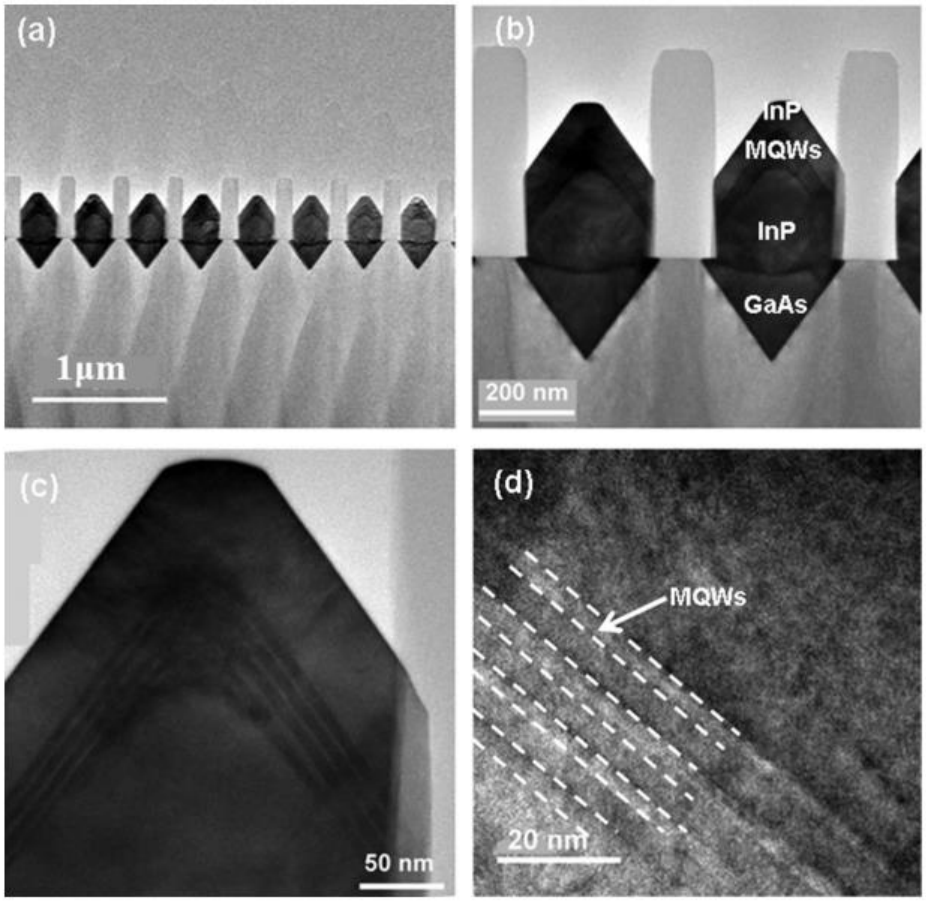

Figure 29. (**a**,**b**) Low magnification cross-sectional TEM image of an InGaAs/InP MQW grown on InP/GaAs buffer layers in nanoscale V-shaped trenches of Si (001) substrate; (**c**) A magnified cross-sectional TEM image of the top part of the sample; (**d**) A high-resolution TEM image taken from the region of side MQW. Reprinted with permission from ref. [136]. Copyright 2016 American Institute of Physics.

The use of {111}-oriented V-grooved pockets in SiO_2 trenches by the ART approach is effective to restrict the generation of APBs and TDs, but the V-groove etched by the KOH solution is not only easy to cause serious damage to the crystal arrangement of the Si surface, but also easy to cause surface contamination by wet etching. In 2019, Wei et al. [130] grew the III-V materials on the V shape bottom of the {111} plane Si substrate by MBE. They first obtained the U-shaped pattern with ridges along [110] direction on the Si (001) substrate in Figure 30a; then, the homoepitaxy of the 550 nm Si layer was conducted by MBE at 600 °C. After that, the (111)-faceted Si hollow structures were achieved on the U-shape patterned Si (001) substrate in Figure 30b. The GaAs layers were deposited on the V shape Si substrate using a two-step method, as shown in Figure 30c. This outgrown (111)-faceted Si hollow structure is considered as a diatomic step to grow the ABP-Free GaAs layer on the GoVS template. More importantly, the thermal strain is released and attributed to this hollow structure. Figure 30d shows a perfect surface with the RMS at 1.3 nm and a low TDD of 7.0×10^6 cm^{-2}. This novel process can solve the problem of incompatibility between the miscut Si substrate and conventional Si substrate used in the CMOS process, which has a great commercial value.

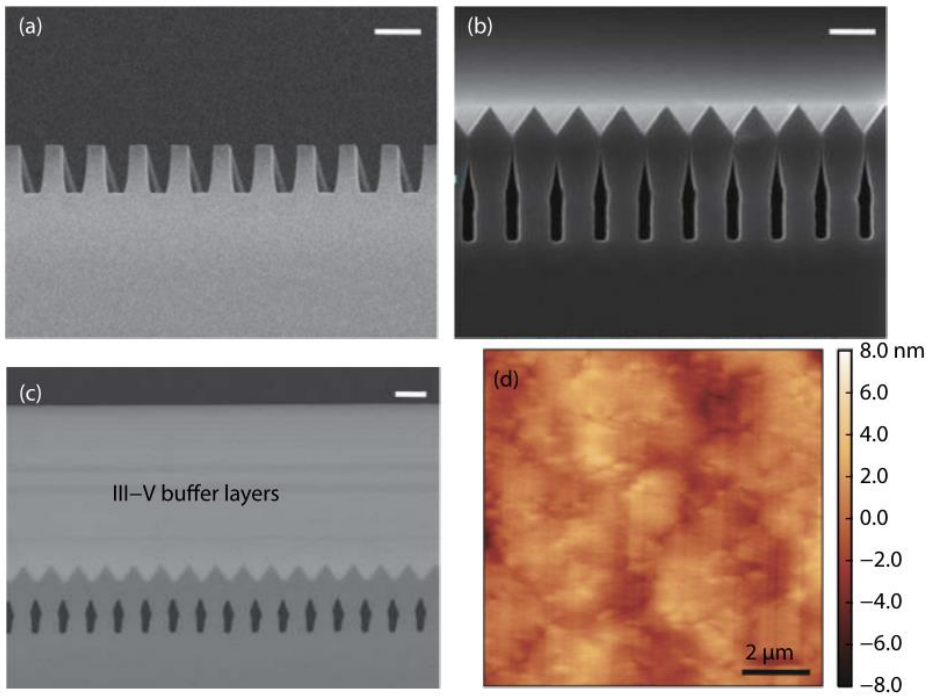

Figure 30. (**a**) Cross-sectional SEM images of U-shape patterned Si substrate; (**b**) Cross-sectional SEM images of homoepitaxy of 550 nm Si on (111)-faceted Si hollow; (**c**) III-V buffer layers on (111)-faceted Si hollow substrate; (**d**) AFM image of III-V buffer layers on Si substrate. Reprinted with permission from ref. [130]. Copyright 2019 IOP Publishing.

From the above Figure 30, it is amazing that the presence of an extra free surface can absorb ~10% thermal strain between Si and GaAs layers, which can obviously reduce the TDD. As we know, the forming of the thermal crack is the thermal strain caused by the large CET of III-V and Si during the cool-down process. Controlling thermally induced strain during the growth is very important to the device fabrication. In order to prevent the crack formation, Saravanan et al. [137] grew GaAs films on a Si/porous Si/Si (SPS) substrate at a low temperature of 450 °C. Their result shows a biaxial tensile stress as low as 1.69 kbar for GaAs/SPS at the 77 K photoluminescence spectra, but with a higher TDD of 10^{11} cm^{-2}. Inserting the buffer layer can decrease the TDD, while thicker buffer layers (~4 μm) can also induce thermal crack. Therefore, the strain compensated layer was introduced to reduce the thermal strain. Takano et al. [138] grew GaAs epilayers on Si substrates by inserting $In_xGa_{1-x}As$ buffer layers via low-pressure metalorganic vapor-phase epitaxy. The TDD of 4.8×10^6 cm^2 for the GaAs layer was achieved by insertion of an InGaAs strained layer. This incomplete strain relaxation in InGaAs layers can compensate the tensile strain due to the large TEC between GaAs and Si materials. However, the compositional buffer layer has some drawbacks, such as several microns in thickness, high cost, and large usage of material. In following, a thinner superlattice (SL) buffer was applied as the strain compensated layer to minimize the thermal crack, and the SL layer can not only facilitate strain relaxation by interaction with misfit dislocations, but also compensate the thermal strain energy from the mismatch of III-V to Si [107,116,136].

Recently, the use of a patterned substrate to minimize the thermal crack was widely developed. As for pre-patterned growth, cracks can be avoided by growth on a small area due to strain relaxation near the pattern edge. As seen from Figure 31, the thermal strain of GaAs is released and attributed to this Si hollow structure; approaches using the Ge on the micropillar patterned Si (001) substrates were also proposed. Zhang et al. [139] grew APB-free GaAs film on employed the {113}-faceted Ge/Si (001) hollow substrate by MBE. First, the fabrication of the {113}-faceted Ge/Si (001) hollow substrate is as follows: the U-shape grating pattern was defined on an on-axis Si (001) substrate by using deep ultraviolet lithography and reactive ion

etching; then, depositing the 60 nm Si buffer on the patterned substrate, a 600 nm Ge layer was grown to achieve the {113}-faceted Ge hollow structures, as shown in Figure 31a. Second, the typical two-step GaAs was grown on the {113}-faceted Ge/Si (001) hollow substrate in Figure 31b. Figure 31c shows the magnification of {113}-faceted Ge and the GaAs interface; few APBs were found at the bottom of the Ge {113} sawtooth structure, but APBs are not observed in the top GaAs layer. Similarly, the {113}-faceted Ge structure can annihilate the APBs at the interface with the {111}-faceted Si structure, which can be considered as a miscut substrate. However, the Ge {113} crystal plane has less miscut than the Si {111} crystal plane, which brings out a trapezoidal shape of APB in ten nanometers of the bottom of the Ge {113}. In following, the 7-μm-thick GaAs layer, which is far beyond the typical value of the cracking thickness, can be grown on the {113}-faceted Ge/Si hollow substrate. They characterized the thermal strain issue by a high-resolution XRD reciprocal space mapping (RSM) performed around (004) and (224) reflections, as shown in Figure 31d,e. From the peak position of RSM, the in-plane strain $\varepsilon_{\parallel}$ of the GaAs and Ge layer were calculated from the extracted calculation of the in-plane lattice constant and out-of-plane lattice constant of the GaAs and Ge. Compared with the lattice constant of bulk GaAs and Ge, the residual thermal strain of Ge is about 89.8% lower than that of the Ge layer on normal Si substrates [140]. The residual thermal strain of GaAs is 29.4% lower than that of the GaAs layer grown on the Ge/Si template [141]. Their results indicated that this hollow structure plays an essential role in thermal strain reduction. With a 400 nm GaAs deposition, a smooth GaAs surface with a RMS of 0.67 nm was acquired, and a low TDD of $5.7 \times 10^6/\mathrm{cm}^2$ was obtained by following InGaAs/GaAs quantum-well DFLs inserting.

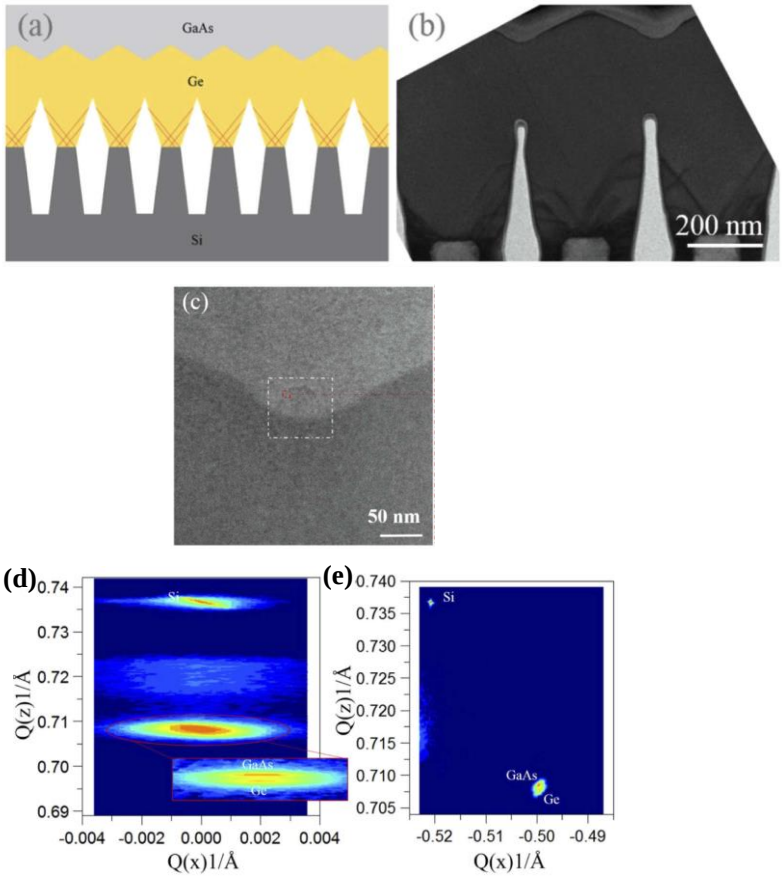

Figure 31. (**a**) The schematic illustration of the GaAs grown on the Ge/Si hollow substrate; (**b**) Cross-sectional TEM image of 600 nm thick Ge layer grown on the hollow patterned (001) Si; (**c**) Zoom-in HADDF image of the interface at the bottom region; high-resolution XRD reciprocal-space mapping around (**d**) (004) and (**e**) (224). Inset of (**c**) Higher resolution (004) map from triple-axis mode. Reprinted with permission from ref. [139].

4.2.2. Epitaxial Lateral Overgrowth (ELO)

Although the ART technique discussed above can effectively solve the APB problem, and block the propagation of crystalline defects using the groove mask, this technique also limits the maximum achievable dimension of III-V epitaxial layers, which are more amenable in some device applications [142]. In order to provide a large film plane for the preparation of III−V devices, the ART technique needs to be continuously optimized so that the SEG III−V materials are epitaxial and grown out of closely spaced trenches, and extend laterally above the oxidation strips until the materials from adjacent grooves merge together to form a continuous high quality epitaxial layer. Recently, an alternative ART technique called Lateral aspect ratio trapping (LART) was developed. As schematically illustrated in Figure 32a, micrometer-scale III-V crystals can be directly grown above the buried oxide layer by this LART method [143]. Compared to the conventional "aspect ratio trapping" approach, the LART approach is changing the direction of the groove, enabling the growth front to the lateral direction. The lateral oxide trenches can be created by dry etch terminated on the buried oxide; then, anisotropic wet etching was processed to form "V" shaped Si. This {111}-oriented Si bevel structure not only prohibits the formation of APBs in the initiating lateral growth of InP layers, but also the propagation of TDD was effectively blocked by the wide lateral SiO_2 trenches, which reveal a high "aspect ratio" in the lateral direction. Figure 32b,c shows a tilted-view SEM image of the SEG InP layer grown on (001) SOI substrates using the LART method. Figure 33b shows an InP-epi "wing" grown using the lateral ART approach, and Figure 33c displays the two symmetrical InP-epi wings. From the SEM images, we can see the Si pedestal sandwiched between the top oxide spacer, and the buried oxide layer features two {111}-oriented surfaces. Starting from the nucleation sites provided by the {111} Si facets, the InP crystal evolves laterally along the [110] direction into wing-structures with two {111} facets. The angle between the two {111} facets is around 110° which indicates a zincblende crystal structure Then, the InP stripes continue laterally to grow inside the long nano-scale SOI trenches resulting in dislocation-free InP crystals right atop the buried oxide layer. In addition, the dimension of III-V nano-ridges can be controlled by changing the thickness of the Si layer on SOI, which is limited by the size of photolithography in the conventional ART approach. This in-plane and close placement of the III-V layer with the Si device layer also facilitates the integration of III-V light emitters with Si-based photonic components.

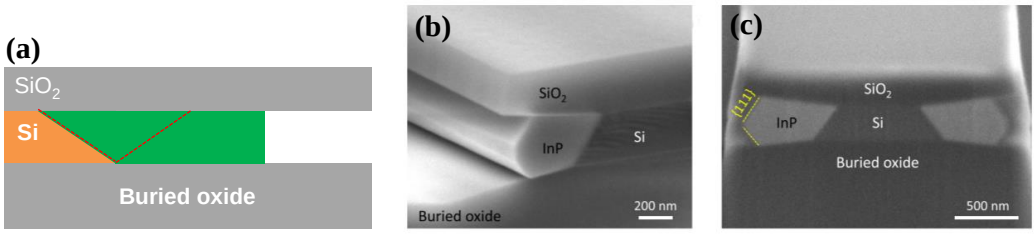

Figure 32. (**a**) The scheme of lateral ART. The red dotted lines denote the confinement of the majority of crystalline defects at the InP/Si interface and the trapping of residual TDs by the top and bottom SiO_2 layers. (**b**) Tilted view SEM image of one InP sandwiched between the top oxide spacer and the buried oxide layer. (**c**) Cross-sectional SEM images of two symmetrical InPs grown using the lateral ART approach. Reproduced with permission from ref. [143]. Copyright 2019 American Institute of Physics.

The above ART methods or lateral ART approach often produce sub-micrometer dimensions of APB-III-V layers, but to expand the dimension of the epitaxial III-V further to tens and even hundreds of micrometers, ART technology needs to be improved. Epitaxial lateral overgrowth (ELO) is an innovative technique to provide large regions of device materials. In the ELO process, a III-V buffer layer is first grown on the Si substrate, then polished by CMP. Microsized SiO_2 stripe patterns are selectively etched to expose the III-V buffer layer for regrowth. Then, the III-V epitaxial layer is vertically regrown through the

opened region of the mask and thereafter can be laterally grown over the mask. Most of TDs in the buffer layer are blocked by the bottom of the mask, but a small number of TDs around the opened region will propagate upwards, as shown in Figure 33a. Therefore, a high crystalline quality and thicker layer can be made by this ELO. For the GaAs on Si, there are many pioneering works reported [144,145]. Tsaur et al. [146] first obtained the single-crystal GaAs layers by means of ELO seeded within stripe openings in a SiO_2 mask over GaAs layers grown on Ge-coated Si substrates. TEM and scanning cathodoluminescence studies indicated that the laterally overgrown GaAs layers have a dislocation density. However, the early reports on ELO for GaAs-on-Si suffered from the limited defect-free region and the mechanical weakness of the laterally grown parts, both of which became severe as the ELO layer was further grown. In 2015, Yunrui et al. [147] demonstrated that the GaAs coalescence layer grew on the patterned 1.8 μm GaAs buffer layer by epitaxial lateral overgrowth using metal-organic chemical vapor deposition. A 410-nm-thick coalesced ELO GaAs layer was obtained with the low root-mean-square surface roughness of 6.29 nm. Figure 33b,c show the SEM images of the growth and evolution of the ELO GaAs layer on the opening trenches. As shown in Figure 33b, the growth front of GaAs is faceted, with (111) B on both sides and (001) on the top. With the deposition time, the overall 410 nm ELO GaAs layer was shown in Figure 33c.

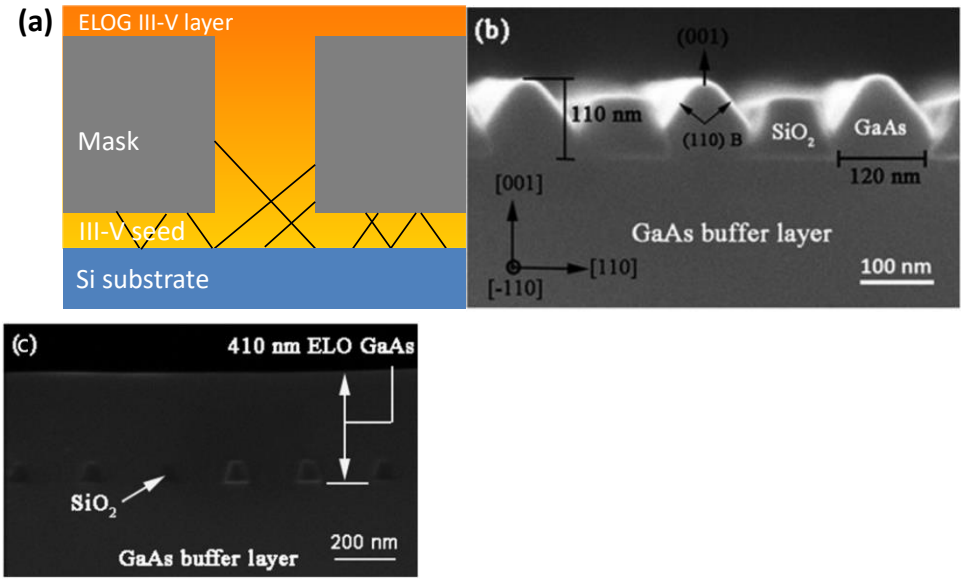

Figure 33. (**a**). Schematics of lateral epitaxial overgrowth (ELO); (**b**) cross-sectional SEM images of the films after the first selective growth stage; (**c**) cross-sectional SEM images of the ELO GaAs layer. Reprinted with permission from ref. [147]. Copyright 2015 American Institute of Physics.

Compared with GaAs-on-Si, ELO techniques are more widely employed [148–150] on InP-on-Si growth, because it is very difficult to obtain low TDDs and large-scale via the direct growth of InP on Si. For the optimization of InP ELO on the (001) Si substrate, Metaferia et al. [151] investigated the ELO of InP from mesh and line openings on the masked InP seed layer on the Si (001) wafer. Their results showed that the coalesced region produced the TDD in a range from 6×10^6 cm^{-2} to 4×10^7 cm^{-2} depending on the thickness of the ELO layer. In their work, the ELO InP layer was grown on a 1.5-μm-thick InP/Si substrate with a 40-nm-thick SiO_2 mask. The mesh and line masks (opening and masking width of 200 nm and 3 μm, respectively), tilted 15°and 30°off the [110] direction, are compared. The quicker coalescence in the mesh opening resulted in better surface roughness at the early growth stage (~10-μm-thick InP layer), but, after an extended growth (~100 μm-thick InP layer), both mesh and line opening cases exhibited a similar surface roughness (RMS roughness of 16~25 nm). It was shown that regardless of both angles (15° and 30°) and masks (mesh and line opening), the TDDs were measured to

be a similar value. The TDD of the 10 µm-thick and 100 µm-thick InP layer was measured to be 2~4 × 10^7 cm $^{-2}$ and 6~7 × 10^6 cm^{-2}, respectively. Han et al. [152] displayed two improved ELO strategies to achieve large-dimension III-V materials with a close proximity to the Si substrates in Figure 34. The first scheme is called conformal growth; III-V films lateral selective epitaxial growth starts from III-V seeds on silicon. In the conformal growth scheme [153], after the III-V films were deposited on the Si substrate, a thin layer of the growth mask is then patterned to form the III-V seeds. Then, the regrown III-V stripes were laterally selectively grown along the initial III-V seeds to extend the large dimension size. Another scheme is named corrugated epitaxial lateral overgrowth (CELO) [154]; short III-V thin film segments were processed as a III-V seeds by bulk III-V film deposition and patterned; then, a thin patterned oxide mask was deposited on III-V seeds for the following homogenous selective regrowth of the InP process. In both strategies, crystalline defects are confined within the seed mesa, while the laterally overgrown III-V is free of any TDs. Figure 34b shows the cross-sectional SEM in [110] view of CELOG InP on Si; defects are confined in the lateral trenches, and no TDS can be found in the CELOG InP layer. These two improved processes can be used for large-dimension III-V layer manufacturing, which could be furthered processed to the subsequent growth of lasers' structures.

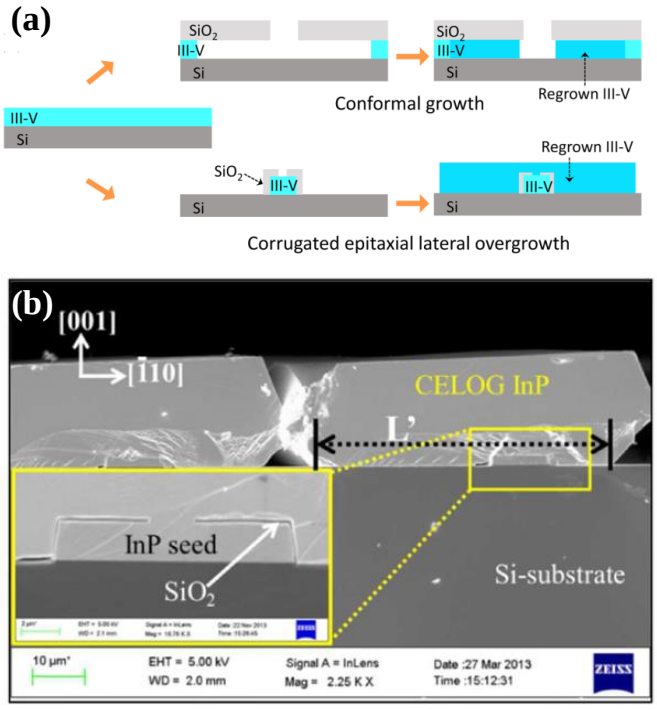

Figure 34. (**a**) Schematic of two improved ELO process; **(b)** cross-sectional SEM in [110] direction view of CELOG InP on Si. Reprinted with permission from ref. [154]. Copyright 2015 IOP Publishing.

Following the above results, in 2020, Omanakuttan et al. [155] fabricated and studied the high crystalline quality of InP by the self-aligned corrugated epitaxial lateral overgrowth (CELOG) method. Figure 35a–d display the InP-seed mesa fabrication process flow. A schematic of the InP-seed mesa was patterned on Si processed for CELOG and is shown in Figure 35e. Through a series of processes: mask deposition, photolithography, and etching, then the CELOG of InP/Si can be obtained by a schematic of Figure 35f. The defective InP seed acts as the CELOG InP growth origination; the threading dislocations propagating from the InP seed can be eliminated by creating dislocation loops for increasing the InP layer thickness. Their results displayed that RMS surface roughness of 2.95 nm obtained for the uniform InP CELOG layer. A higher intensity band edge emission in the cathodoluminescence spectra near-BE band at 892 nm (1.39 eV) and enhanced carrier lifetime (710 ps) of InP are observed above the CELO InP/Si interface compared to the defective seed InP layer on Si, which are attributed to the reduced TDD realized (~3 × 10^8 cm^{-2}) by the CELO

method. For the application of the photonic integrated circuit (PIC), a large dimension and uniform InP layer with ultralow dislocation on Si are desired. The CELOG can be extended to the formation of other large dimensions of III-V/Si heterostructures.

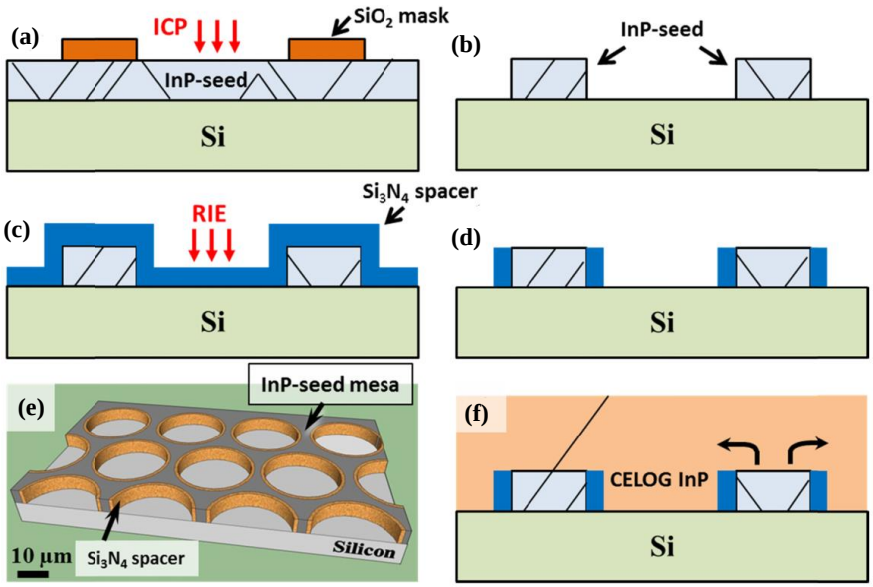

Figure 35. (**a**–**d**) Process of InP-seed mesa fabrication for CELO; (**e**) Schematic of the InP-seed mesa pattern on Si before CELO. The thickness of InP-seed layer is 2 μm, and the distance between the two adjacent circular rings of diameter 30 μm is 5 μm; (**f**) Schematic of the CELO InP/Si cross-section. Reprinted with permission from ref. [155].

In the laterally grown parts, propagating defects such as threading dislocations and stacking faults will be blocked by the mask and consequently cannot propagate into the layer above the mask. ELOG was used to grow GaN [156], as well as InGaAs [157] on Si.

The InAs semiconductor material is a very good candidate for ultra-high-speed electronic and optoelectronic devices, due to its narrow band gap, small electron effective mass, and very high electron mobility (~33,000 cm^2/V s at 300 K). However, the large epitaxial strain generated by the high lattice mismatch (11.4%) and the difference in thermal expansion between InAs and Si, leads to a roughness surface and high TDD, which degrade the electrical and optical properties. At present, growth of thin-film InAs is usually difficult, but direct growth of vertical nanowires can usually accommodate a larger lattice mismatch as compared to thin-film growth [158]. Regarding InAs nanowires, various strategies including vertical VLS growth [159], vertical SEG growth [160,161] have been proposed. Among these techniques, vertical VLS growth has an obvious disadvantage: using Au as the catalyst leads to the formation of deep-level traps with silicon and degrades the device performance, which makes it forbidden in the CMOS fabrication process, so vertical SAE growth was widely developed. In the process of InAs NWs' growth, the morphology of NWs is essential to homogeneous optical and electrical properties. Hertenberge et al. [160] obtained very high yields of ~90 percent of vertically (111)-oriented InAs nanowires selectively grown on the patterned Si(111) substrate. Then, Bjork et al. [161] studied (111)Si (axial) and (1-10)Si (radial) growth of InAs NWs by varying growth duration, temperature, group-III molar flows, V/III ratio, mask material, mask opening size, and inter-wire distance. To achieve uniform nucleation and a high vertical yield of wires, an As-terminated surface and an optimized TMIn flow and V/III ratio are required. Below 520 °C and 540 °C, respectively, the <111> and the <1-10> growth is surface kinetically limited. Their results also indicated that by placing wires in large arrays, it is possible to stop the <1-10> growth rate completely in favor of the <111> growth rate. Recently, Grégoire et al. [162] report that the vertical and high aspect ratio InAs NWs with a hexagonal shape were grown on both GaAs (111)B and Si(111) patterned substrates by selective epitaxial growth (SEG). The

morphology and the quality of InAs NWs' arrays grown on GaAs(111)B and Si(111) were characterized by SEM and photoluminescence measurements in Figure 36a–d, respectively. For NWs grown on GaAs(111)B in Figure 36a, a strong peak at 0.445 eV with a full width at half-maximum (FWMH) of 32meV was observed, while a low peak at 0.413 eV with a FWHM of 34 meV grown on Si was observed, as shown in Figure 36b. A lower PL intensity recorded from InAs NWs grown on Si compared to GaAs is probably due to the lower NW density and diameter. By decreasing the NW diameter, the principal PL peak shifted to a higher energy, confirming the presence of both WZ and ZB phases in InAs NWs grown by SAG-HVPE. These NW arrays exhibited strong PL intensity and optical absorption, which is encouraging for future optical devices.

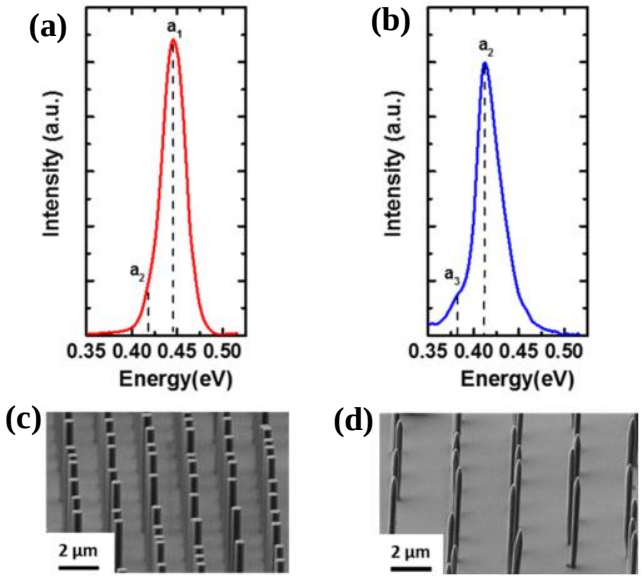

Figure 36. PL spectra at 10 K of InAs NWs grown on (**a**) GaAs (111) B and (**b**) Si (111); (**c**,**d**) Corresponding SEM images. The pitches are, respectively, 2 and 2.5 µm. Reprinted with permission from ref. [162]. Copyright 2021 American Chemical Society.

In the III−V semiconductor, III-antimonide, such as GaSb, has attracted a tremendous amount of research interest. GaSb (0.72 eV) is a direct bandgap material, which can be used as a photodetector of the mid-IR spectrum. Moreover, GaSb exhibited attractive characteristics for p-MOSFETs due to their high bulk hole mobility (over 1000 cm^2/Vs). Similarly, it has great challenges to grow GaSb on Si substrate, due to the large lattice mismatch and thermal mismatch. Recently, there were reports of a GaSb-on-insulator (-OI) by direct wafer bonding [163] and epitaxial layer transfer [164], but these methods remain costly due to the limited sizes of available III−V substrates. However, a one-dimensional (1D) GaSb nanowire (NW) manufactured by selective epitaxial growth (SEG) provides extra benefits for many advanced utilizations, such as the better stress relaxation, capability of the advanced gate stacking integration, more efficient light adsorption and trapping. For the GaSb NWs' application in electronic devices, a well-controlled nanowire-like morphology with a small diameter (several tens of nanometers) is essential. Yang et al. [165] grew very thin and uniform GaSb NWs with diameters down to 20 nm by the use of a sulfur surfactant. This GaSb NWs were configured into transistors and exhibited impressive electrical properties with the peak hole mobility of ~200 cm^2/Vs, better than any mobility value reported for a GaSb nanowire device. To control the GaSb crystal shape and dimension deeply, an alternative to the SEG technique known as template-assisted selective epitaxy (TASE) was developed [166,167]. Borg et al. [167] investigated a monolithic integration of high-mobility horizontal GaSb NWs on the SOI substrate by TASE. They found that a high degree of morphological control allows for GaSb nanostructures with critical dimensions down to 20 nm. Figure 37a displays a SEM image of an exemplary array of

GaSb nanostructures outside the templates. The exposed front GaSb surface, at which the crystal grows, typically forms a large {111} facet often with two smaller and opposing {110} facets (see Figure 37c,d). Because of the polar nature of the GaSb zinc-blende crystal structure, nonequivalent 180° rotations of the crystal lattice can occur upon nucleation on the nonpolar Si. This results in two distinct orientations of the growth facets as illustrated in Figure 37d. Meanwhile, the GaSb growth is governed by excess Sb present on the GaSb surface, leading to a strong growth rate dependence on the V/III ratio and temperature. Hall/van der Pauw measurements are conducted on 20-nm-thick GaSb nanostructures, revealing high hole mobility of 760 $cm^2/(V\ s)$.

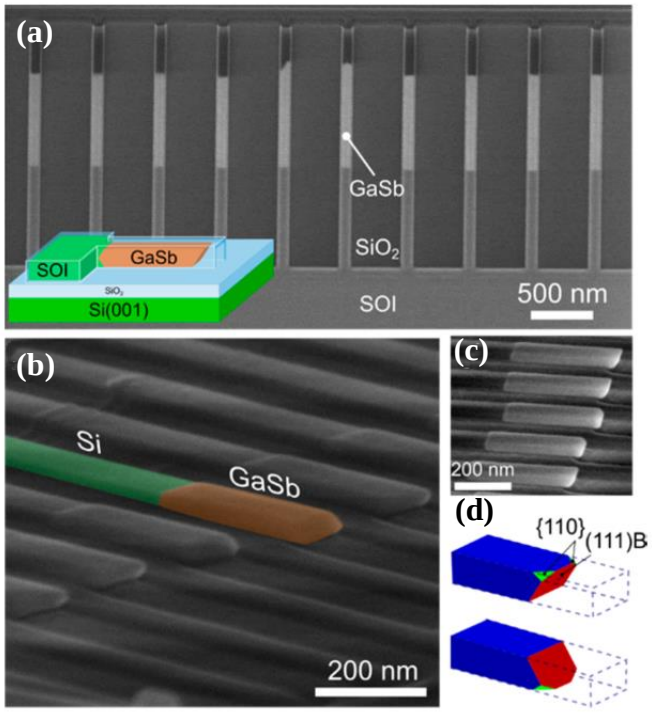

Figure 37. (**a**) SEM image of an array of horizontal GaSb nanostructures integrated coplanar with a SOI layer using TASE. The inset shows an illustration of the layer structure. (**b**,**c**) Tilted SEM images of GaSb nanostructures. (**d**) Schematic illustration highlighting the typical faceting observed at the growth front of the GaSb crystals. Reprinted from ref. [167]. Copyright 2017 American Chemical Society.

In summary, the APB problem can be solved by a miscut Ge/Si substrate, {113}-faceted Ge/Si (001) hollow substrate in the global epitaxial method, and {111}-oriented V-grooved in the ART method. However, high quality III−V heteroepitaxy with low TDD on Si is crucial to the monolithic integration of III−V devices on Si-based PICs. Table 2 is the summary of the reported TDD and RMS values of GaAs, InP in the growth of the substrate, epitaxy method, buffer materials, process in these years. In terms of material growth quality, the TDD of the GaAs layer as low as $10^7\ cm^{-2}$ can be achieved by inserting the superlattice via global epitaxy. Then, the 8-inch GaAS-O-I substrate can be realized in our group soon. However, few research projects report on the preparation of other III−V epitaxy methods on the Si substrate. For selective epitaxial growth (SEG), many III−V semiconductors such as InP, InCaP, InAs, GaSb, etc. can be grown by the ART method. A TDD of $10^6\ cm^{-2}$ of the InP layer was obtained in the V-grooves patterned Si substrate. In terms of application, the high-quality and stress-controlled large-size III-V epitaxial layer grown by global epitaxy is more conducive to the preparation of Si-based OEIC. On the contrary, the III-V nanowire arrays fabricated by the SEG method can produce the monolithic integration of III-V nanodevices on silicon substrates. Especially for a smaller

size of CMOS electronic devices, several tens of nanometers of III-V NWs are considered optimal for high-performance tunnel-FETs.

Table 2. Summary of reported TDD value of III-V materials in terms of substrate, epitaxy method, buffer, procedure.

Year	Substrate	Epitaxy Method	Buffer	Procedure	III-V Materials	TDD (cm^{-2})	RMS (nm)	Refs.
2011	0° Si	Global	Ge	two-step growth	GaAs	2×10^7	1.1	[70]
2011	4° Si	Global	Ge	two-step growth	GaAs	1.8×10^7	—	[64]
2013	0° Si	Global	—	three-step growth+ TCA	GaAs	1.1×10^7	0.73	[113]
2014	Ge	Global	—	two-step growth	GaA	2.7×10^7	0.7	[93]
2015	6° Ge	Global	—	two-step growth	GaAs	—	0.6	[97]
2016	0° Si	Global	Ge	two-step growth	GaAs	3×10^7	0.5	[98]
2018	0° Si	Global	Ge	$In_{0.18}Ga_{0.82}As$/GaAs SLSs	GaAs	2.3×10^6	—	[121]
2019	0° Si	ART	Si	(111)-faceted Si hollow	GaAs	7.0×10^{6}	1.3	[138]
2020	0° Si	ART	Ge	{113}-faceted Ge/Si hollow substrate.	GaAs	5.7×10^6	0.67	[145]
2021	0° Si	Global	CMP-Ge	three-step growth	GaAs	7.4×10^7	1.27	[53]
2018	0° Si	Global	Ge	InAs/InP QD DFLs	InP	3×10^8	2.88	[127]
2011	0° Si	ELO	—	two-step growth	InP	4×10^8	—	[158]
2019	0° Si	CELOG	—	two-step growth	InP	3×10^8	2.95	[162]
2020	0° Si	Global	—	$In_{0.73}Ga_{0.27}As$/InP SLSs	InP	4.5×10^7	2.38	[115]

5. Conclusions and Outlooks

High-quality III-V heteroepitaxy on the Si substrate is crucial to the Si-based optoelectronic integration circuits (OEICs). In this work, we reviewed the three major challenges of the Si based IIII-V heteroepitaxy: (1) anti-phase boundaries (APB); threading dislocation (TD); (3) stacking faults (SF). Meanwhile, the mechanism and theoretical model of three kinds of defects are also deeply analyzed, which is convenient for readers to understand its development process in detail. In order to solve each issue, a wide variety of strategies is discussed. The bulk and high quality of III-V structure layers are the basis of larger scale optoelectronic devices' fabricating. For global epitaxy, the offcut Si substrates can easily suppress the formation of APBs, but it is incompatible with the integration of CMOS manufacturing. To reduce the TDDs, a lot of methods, including the buffer layer, annealing, multi-step growth, defect filter layers, and so on, were developed. In this, the thick layer and high annealing process can lead the new defects as stacking faults and thermal cracks, resulting in the low TDD of 10^6 cm^{-2} for GaAs, and a higher TDD (~10^7 cm^{-2}) of InP-on-Si due to a larger lattice mismatch (~8%) between InP and Si. For selective epitaxial growth (SEG), {111}-oriented V-grooved pockets in SiO_2 trenches by the ART approach are effective to restrict the generation of APBs and TDs, but the solution-etched V-groove is not always uniform and easily damages the crystal arrangement of the Si surface, which obviously affects the defects' distribution. In addition, the ART method also limits the maximum achievable dimension of the epitaxial III-V materials. Epitaxial lateral overgrowth (ELO) is an innovative technique to provide large regions of device materials, especially for plane-InP growth on Si. Moreover, other III-V semiconductors, such as InAs, GaSb, which have high mobility but larger mismatches with the Si substrate, can be fabricated in small-size Nanowires (NWs) by the ART method, representing potential applications as the channel material integrated on Si substrates to MOSFETs devices.

Even though major obstacles for III-V-on-Si heteroepitaxy, such as APBs, TD, stacking faults, are resolved now, the quality of III-V layers on on-axis Si is still unsatisfactory for the deployment on the PICs or ICs. Currently, we can obtain the low TDD of 10^6 cm^{-2}, but it still challenging to reduce the TDD to native substrates (~10^4 cm^{-2}). Therefore, further effects need to be devoted to improving the quality of the III-V layer on Si to realize the integrated III-V on the Si-based platform fully. The Epitaxial Lateral Overgrowth (CELO) is

an innovative process for large-scale high-quality Si-based III-V epitaxial layers; systematic research and process optimization are still needed to improve the materials' quality and device performance further. In addition, the bounding of III-V-O-I can thin the LT low-quality layer, which can fabricate the high-performance optoelectronic devices. Therefore, based on the current research, efforts should continue to be devoted to resolving the TDDs and the compatibility of integration techniques with large-volume CMOS manufacturing.

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Core-Shell Dual-Gate Nanowire Charge-Trap Memory for Synaptic Operations for Neuromorphic Applications

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Abstract: This work showcases the physical insights of a core-shell dual-gate (CSDG) nanowire transistor as an artificial synaptic device with short/long-term potentiation and long-term depression (LTD) operation. Short-term potentiation (STP) is a temporary potentiation of a neural network, and it can be transformed into long-term potentiation (LTP) through repetitive stimulus. In this work, floating body effects and charge trapping are utilized to show the transition from STP to LTP while de-trapping the holes from the nitride layer shows the LTD operation. Furthermore, linearity and symmetry in conductance are achieved through optimal device design and biases. In a system-level simulation, with CSDG nanowire transistor a recognition accuracy of up to 92.28% is obtained in the Modified National Institute of Standards and Technology (MNIST) pattern recognition task. Complementary metal-oxide-semiconductor (CMOS) compatibility and high recognition accuracy makes the CSDG nanowire transistor a promising candidate for the implementation of neuromorphic hardware.

Keywords: short-term potentiation (STP); long-term potentiation (LTP); charge-trap synaptic transistor; band-to-band tunneling; pattern recognition; neural network; neuromorphic system

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1. Introduction

Modern day computer architectures suffer from the Von Neumann bottleneck where the separation of memory and processing units impose a fundamental limit on the maximum achievable processing speeds. In addition, the high levels of energy consumption in the conventional computing architecture are a major drawback especially for data intensive applications like big data analytics, machine learning etc. The human brain on the other hand has a highly energy efficient design where the storage and processing are carried out locally using a hugely parallel network of neurons and synapses [1,2]. Neuromorphic systems are gaining research attention due to their potential to design computer chips that can mimic the human brain in merging memory and processing [1,2]. The brain functions (observation, reorganization, learning, and memorization) are performed by neurons (computing elements) and synapses (memory elements) [1,2]. In the neuromorphic system, an artificial synaptic device plays a key role in linking the artificial neurons and modulating the connection strength (synaptic weight) between neurons [3–15]. In order to realize brain-like computing, different types of artificial synaptic devices have been proposed for artificial intelligence applications [3–22]. The major applications for these artificial synaptic transistors are neuromorphic in-memory computing chip, artificial sensory perception, humanoid robotics, memorize, and recognize massive and unstructured data through parallel and power-efficient ways [3–22]. Charge tapping/de-trapping based artificial synapse are favorable for in-memory computing applications due to their stable analogue conductance state and nonvolatile characteristic [12].

Among these electronic artificial synapses, two terminal non-volatile memory devices such as resistive random access memory (RRAM) and phase change memory (PCM) are strong candidates due to their small form factor [5,6,21,22]. However, due to variability and reliability issues in these devices, the recognition rate undergoes fast degradation.

These issues can be resolved with synaptic devices based on complementary metal-oxide-semiconductor (CMOS) field-effect transistors (FET) [15–20]. These FET-based electronic synaptic devices operate with a charge trap layer, which is an attractive candidate with many advantages, (i) low synaptic current; (ii) good reliability; (iii) high integration density; (iv) a large conductance window; and (v) process compatibility with CMOS [15–20]. These FET-type devices show the feasibility of artificial synapse but may have difficulties in scaling due to short channel effect and band-to-band tunneling in nanoscale regime. These effects degrade the performance of a synaptic transistor and reduces state retention. These issues can be resolved with multigate transistors [23]. Among these transistors, gate all around (GAA) transistor shows the better performance due better controllability over the gate [23,24]. Recently, a novel GAA transistor utilizing a nanotube with a core gate has been proposed to improve the gate controllability and enhance the device performances with same effective silicon film thickness [24–28] and also deal with better scaling over the nanowires [24,25].

Therefore, in this work, we emulate biological synaptic properties such as short-term potentiation (STP), long-term potentiation (LTP), and long-term depression (LTD) in an artificial synaptic device with a novel core-shell gate all around transistor. In neuromorphic systems, STP plays a key role in learning mechanism of the human brain [1,2]. STP is observed due to floating body effect (non-volatile characteristic) and LTP and LTD is observed due to trapping and detrapping of the holes from the nitride layer (volatile characteristic). In order to evaluate the inference capabilities of the proposed synaptic device, the weights (conductance values) extracted from the LTP/LTD characteristics of the device are utilized for pattern recognition using a simulated artificial neural network. The designed neural network recorded a high degree of recognition accuracy of 92.28% for the synaptic device.

2. Device Design Strategies and Models Calibration

Figure 1a–c show the schematic representation of the core-shell dual-gate (CSDG) nanowire transistor in 3D and biological synapse, 2D and top view, respectively. The simulated device dimensions and parameters are optimized and illustrated in Table 1. The device consists of two gates (core (inner) and shell (outer) gate) in gate all around or surrounded gate manner, which helps to accumulate the carriers from the silicon film and makes the deeper potential well for charge storage [24–28]. The dual gate in the device increases the gate controllability and shows better scalability [24–28]. In this work, core gate with thinner oxide (SiO_2 of 2 nm), which is responsible for the floating body effect for STP while thicker oxide (SiO_2 of 6 nm/nitride of 4 nm/SiO_2 of 2 nm (O/N/O)) is utilized for charge trapping to show LTP and LTD operations [17]. The device is simulated with the Silvaco ATLAS (Santa Clara, CA, USA) simulation tool with calibrated models. The physical simulation models are calibrated with experimental transfer characteristics of gate all around and double gate inversion mode transistor as shown in Figure 2a,b, respectively.

Table 1. Device specification for CSDG device as synapse.

Device Parameters	Values
Gate length (L_g)	100 nm–50 nm
Silicon core channel radius (T_{Si})	20 nm
Tunneling oxide thickness (T_{TOX})	2 nm (SiO_2)
Nitride layer thickness (T_{NOX})	4 nm (Si_3N_4)
Blocking oxide thickness (T_{BOX})	6 nm (SiO_2)
Oxide thickness (T_{OX})	2 nm (SiO_2)
Core-gate workfunction ($\phi_{m,Core}$)	4.6 eV
Shell-gate workfunction ($\phi_{m,Shell}$)	4.8 eV
Channel doping (N_A)	10^{15} cm^{-3}
Source/drain doping (N_D)	10^{20} cm^{-3}

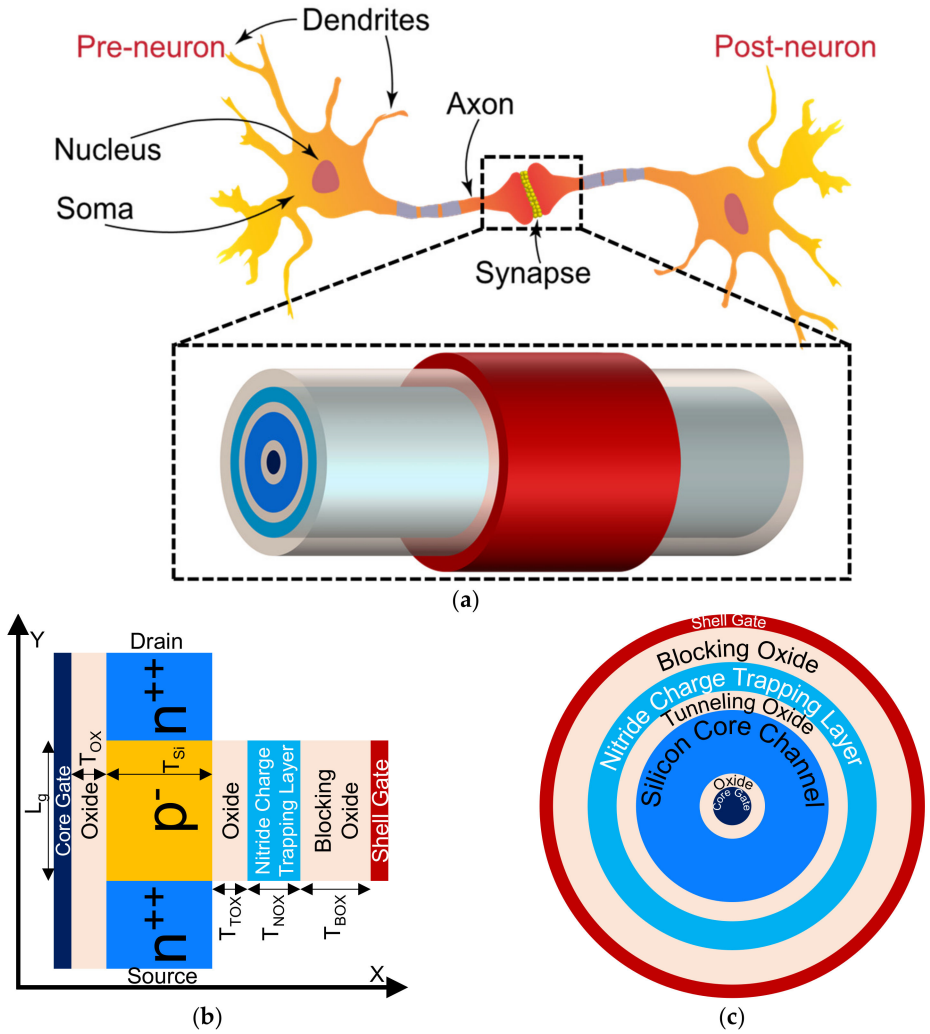


Figure 1. (**a**) Schematic representation of biological synapse and 3D illustration of core-shell dual-gate (CSDG) nanowire transistor. Schematic representation in (**b**) 2D and (**c**) top view of CSDG nanowire transistor for artificial synapse device.

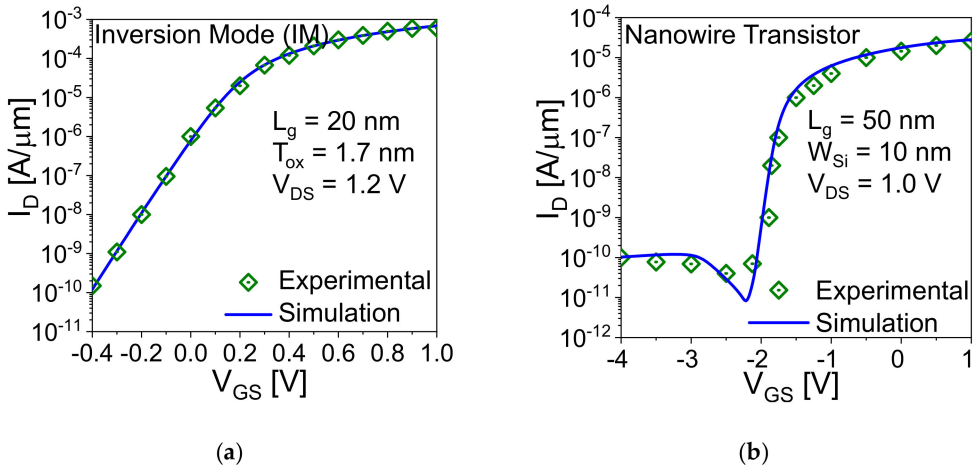


Figure 2. Comparison of simulated transfer characteristic with experimental (**a**) double-gate inversion mode [29] and (**b**) nanowire transistor [30].

Synaptic transistor operations (STP, LTP, and LTD) are based on charge generation, recombination, trapping, and detrapping of charge from the device [15–17]. In order to

generate the charge in the device, non-local band-to-band-tunneling (BTBT) and impact ionization models are incorporated while for trapping and detrapping the charge from the nitride layer, a macro model (DYNASONOS) is embedded in the simulation, along with hot carrier injection, Fowler–Nordheim (F–N) tunneling, and Poole–Frenkel emission models have also been activated. Other physical models are also incorporated such as the Fermi–Dirac statistics model, concentration-dependent, Shockley–Read–Hall generation, and recombination model, Auger recombination model, density gradient quantum effect, bandgap narrowing model, concentration and temperature-dependent carrier lifetime model, Lombardi's mobility model.

3. Results and Discussion

Thanks to core-shell dual gate nanowire transistor, which creates a deeper potential well for charge storage and enhances the retention characteristic of a capacitorless dynamic random access memory (1T DRAM) cell [31]. In this work, the biasing and timing schemes are optimized to achieve STP, LTP, and LTD in the device and mimic the core-shell dual gate transistor as an electronic synapse. The working principle of the device as synapse is based on floating body effect and charge trapping and de-trapping from the nitride layer [15–17,32,33]. These operations are based on band-to-band-tunneling, impact ionization, hot carrier injection, and F–N tunneling in the device [15–17,19,32,33]. In this work, program operation is based on the BTBT mechanism due to its low power consumption and better reliability issue. In order to achieve the transition from STP to LTP at $\geq$ 10th pulse, core-gate voltage is optimized with fixed drain voltage of 1.4 V and shell gate voltage of -1.0 V. Achieving STP in the device not only shows the capability for both STP and LTP, but also consumes lower voltage for LTP operation [19]. The reason for the optimization of the core-gate voltage is that band-to-band-tunneling in the device takes place near the channel and drain due to thinner oxide for core-gate. Figure 3a,b show the transfer characteristics of the device with independent gate operation, respectively. It is clearly observed from Figure 3a (drain current-core-gate voltage) that at lower gate voltage, drain current is increasing due to tunnelling between channel and drain compared to Figure 3b (drain current-shell-gate voltage).

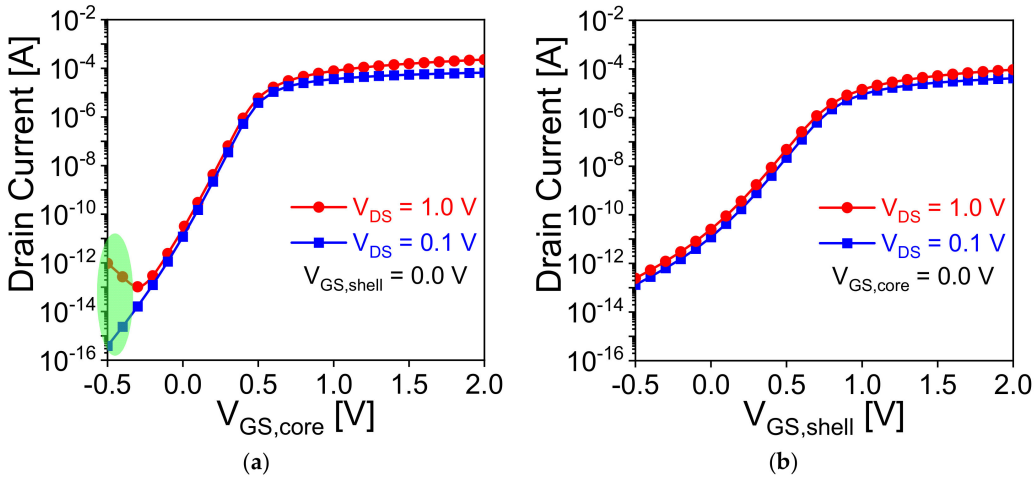


Figure 3. Dual-gate operations of the synaptic memory device. Transfer characteristics at V_{DS} = 0.1 V and 1 V. (**a**) I_D-$V_{GS,core}$ curves at $V_{GS,shell}$ = 0 V. (**b**) I_D-$V_{GS,shell}$ curves at $V_{GS,core}$ = 0 V. L_g = 100 nm and T_{Si} = 20 nm.

Figure 4a shows the voltage waveform during potentiation operation to find the optimized bias with fixed drain and shell gate voltage. A repetitive pulse with pulse and interval width of 2 µs are applied to mimic the device as synapse and shows the transformation from STP to LTP through trapping the charge in the nitride layer. To achieve efficient neuromorphic computational functions, 35 consecutive pulses are applied

to stimulate potentiation and, then 35 pulses for depression. Figure 4b,c show the variation of electric field (E field) and energy band diagram, respectively, with different core-gate voltages (−0.1 V, −0.2 V, and −0.3 V). The E field and energy band diagram extracted 1 nm below core gate oxide. CB and VB indicate the conduction and valence band energies. Figure 4b,c reveal that increase in core-gate voltage (in negative magnitude) increases the E field and reduces the tunneling width between the core-gate and drain junctions, which helps to enhance the tunneling in the device and generates more electron hole pairs. The generated holes are stored in the lower potential region, and furthermore, these stored holes trigger the impact ionization in the device and start trapping the holes in the nitride layer. In Figure 4c, the barrier between source and channel is lower for $V_{GS,core}$ of −0.3 V compared to lower gate bias. This confirms that the stored holes contribute positive potential and trigger impact ionization in the device and achieves transition at lower pulse as shown in Figure 4d. Figure 4d shows the variation of trapped charge in the nitride layer during potentiation pulse. Similarly, in the case of LTD, shell gate voltage plays a crucial role to de-trap the holes from the nitride layer. Figure 5a shows the voltage waveform during the depression operation to de-trap the charge. Figure 5b shows the energy band diagram of the device during depression operation with different shell gate voltage. Increase in shell gate voltage increases the F–N tunneling probability in the device and starts de-trapping the trapped charges from the nitride layer as shown in Figure 5c.

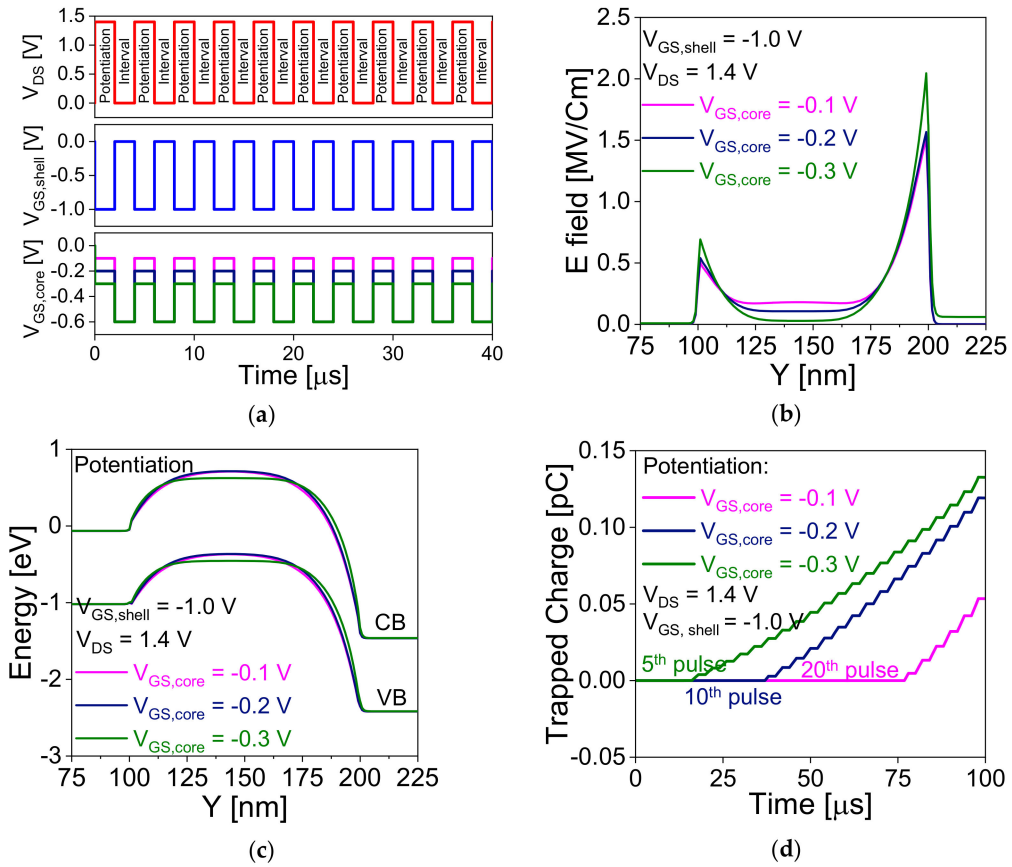


Figure 4. Potentiation operation. (**a**) voltage waveform during potentiation operation. Variation of (**b**) electric field (E filed) and (**c**) energy band diagram with core-gate voltage along the y-direction. (**d**) Variation of trapped charge for different $V_{GS,core}$. E field and energy band diagram are extracted 1 nm below of the core gate oxide.

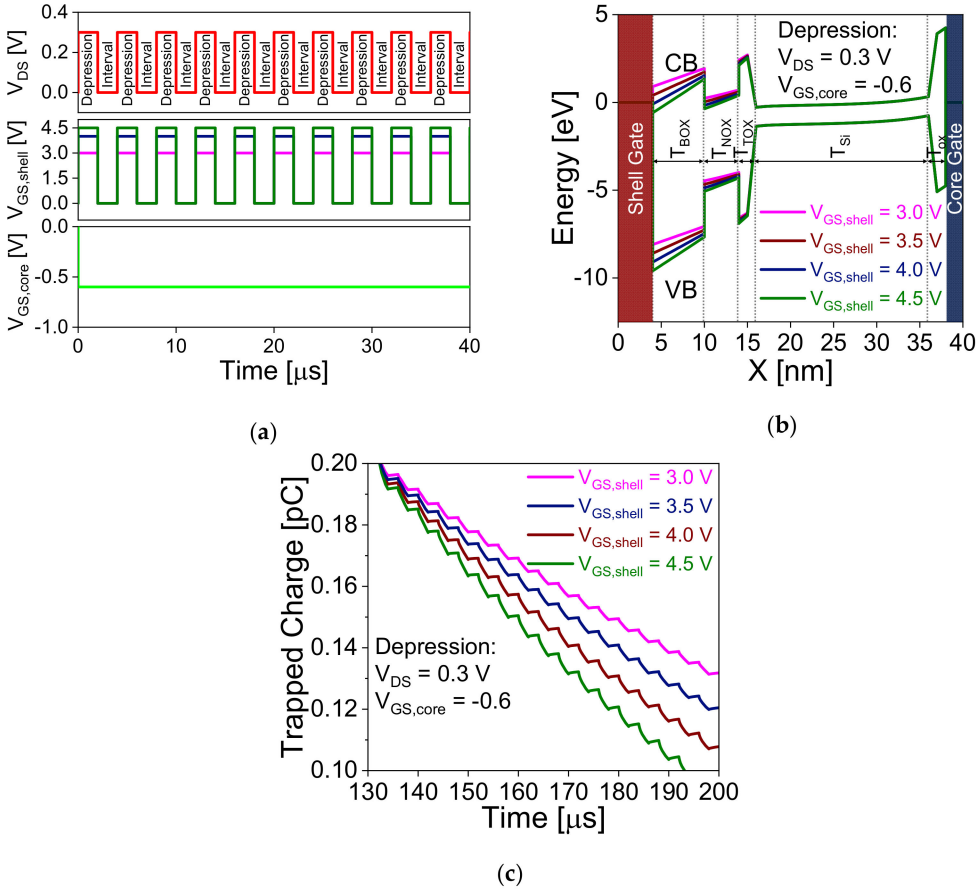


Figure 5. Depression. (**a**) voltage waveform during depression operation. Variation of (**b**) energy band diagram with core-gate voltage along the *x*-direction. (**c**) variation of trapped charge for different $V_{GS,shell}$.

Figure 6a,b show the transient analysis and trapped charge in the nitride layer of the device during potentiation and depression operation, respectively. During potentiation, a repetitive pulse start trapping the holes in the nitride layer due to hot hole injection and F-N tunnelling at lower bias, which shows the transformation from STP to LTP at the 10th pulse. At the 10th pulse, a sharp transition is observed in the drain current and nitride layer, which confirms that the device is in LTP state. Figure 7a–d show the contour plots of impact ionization rate in the device and charge trapped in the nitride layer during potentiation operation at different pulses (1st pulse, 5th pulse, 10th pulse, and 20th pulse). Initially (1st pulse) for STP, the BTBT mechanism is utilized to generate the holes in the device by applying drain voltage (V_{DS}) = 1.4 V, core gate voltage ($V_{GS,core}$) = −0.2, and shell gate voltage ($V_{GS,shell}$) = −1.0 V. The generated holes are accumulated at a lower potential region and electrons start drifting towards the drain side. Further, on increasing the number of repetitive pulses, electrons obtain sufficient energy to trigger the impact ionization in the device and generates more number of electrons-holes pairs in the device. At the 10th pulse, the generated holes get sufficient energy to get trapped in the nitride layer due to F–N tunneling even at lower bias. At the 20th pulse, it can be observed that impact ionization rate is constant while trapped charge in the nitride layer is increasing with increase in pulse. This confirms that after the 10th pulse, generated holes with the energy at the Fermi-Dirac distribution tail have higher probabilities of injection into nitride layer due to hot hole injection. De-trapping the holes from the nitride layer is performed through F–N tunnelling. LTD operation is performed by applying a lower drain bias, V_{DS} = 0.3 V, $V_{GS,core}$ = −0.6, and higher $V_{GS,shell}$ = 4.0 V.

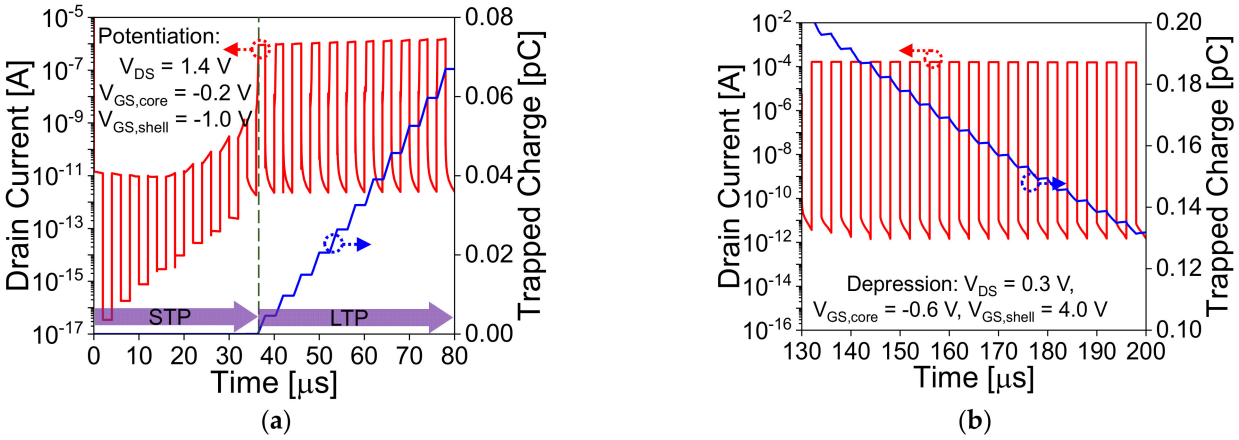


Figure 6. Transient analysis and trapped charges in the nitride layer during (**a**) potentiation and (**b**) depression. A sharp transition in current and trapped charges in the transient analysis of potentiation shows the transformation from short-term potentiation (STP) to long-term potentiation (LTP).

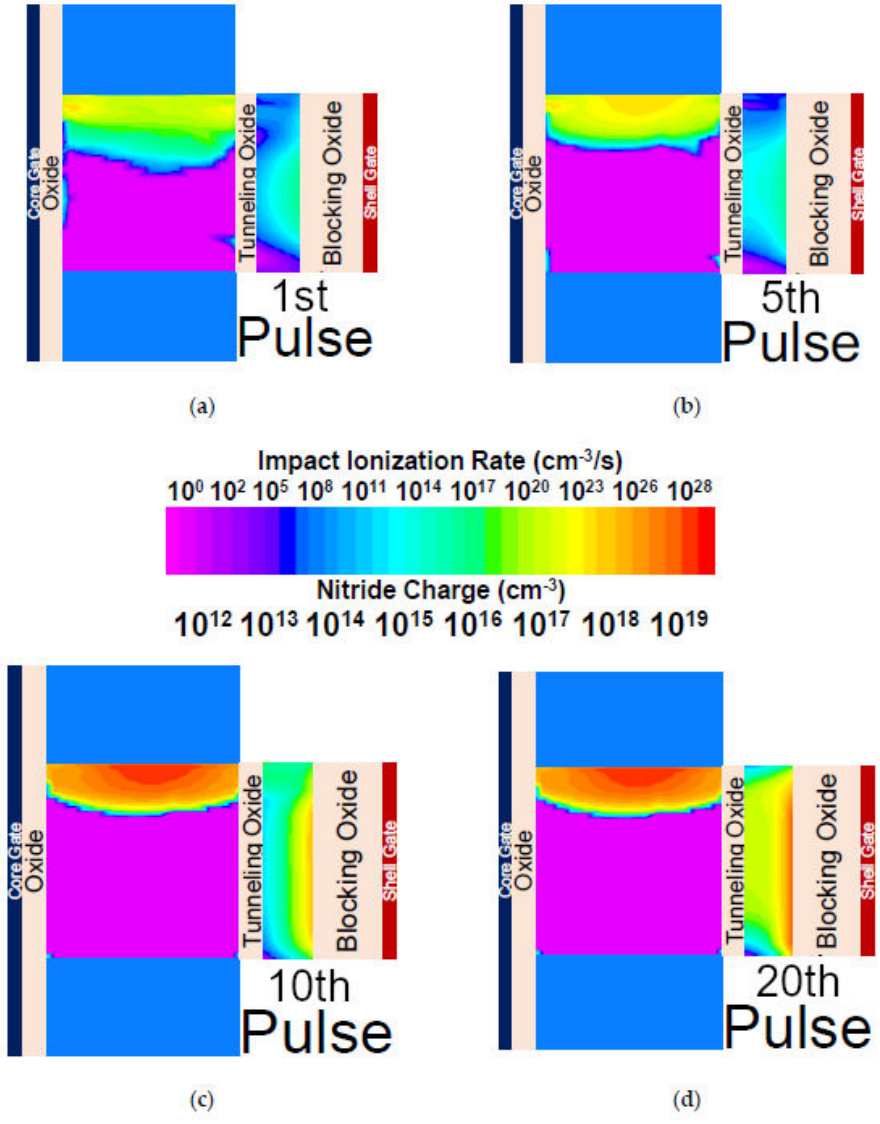


Figure 7. Contour plots of Impact Ionization and charge trapped in the nitride layer during potentiation at (**a**) 1st, (**b**) 5th, (**c**) 10th, and (**d**) 20th pulse.

The transformation from STP to LTP can also be observed from the transfer characteristics (Figure 8a,b) and transient analysis (Figure 8c,d) of the device during inference (read) operation. Inference in the biological brain is analogous to the read operation in an artificial synaptic transistor. To avoid the disturbance and for non-destructive read a lower bias is applied. Figure 8a,b show the drain current—shell gate voltage curve at $V_{DS} = V_{GS,core} = 0.1$ V for different pulses of potentiation and depression, respectively. In the case of potentiation operation, as shown in Figure 8a the transfer characteristics of the device are unchanged during STP states (from 0 to 9th pulse) while from the 10th pulse (LTP), threshold voltage (V_{TH}) is decreasing with increase in pulse due to increase in trapped charge in the nitride layer (Figures 4d and 6a).

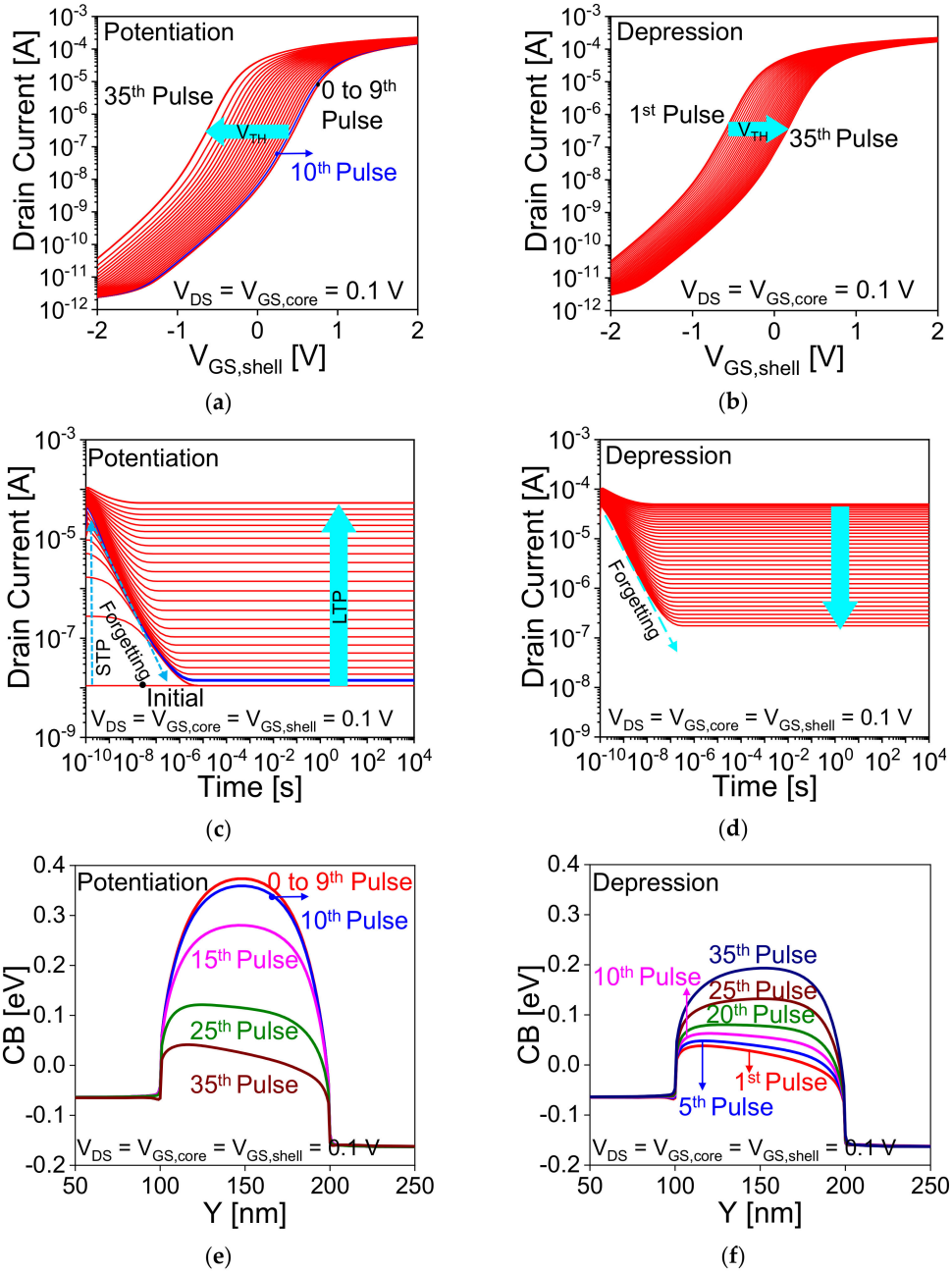
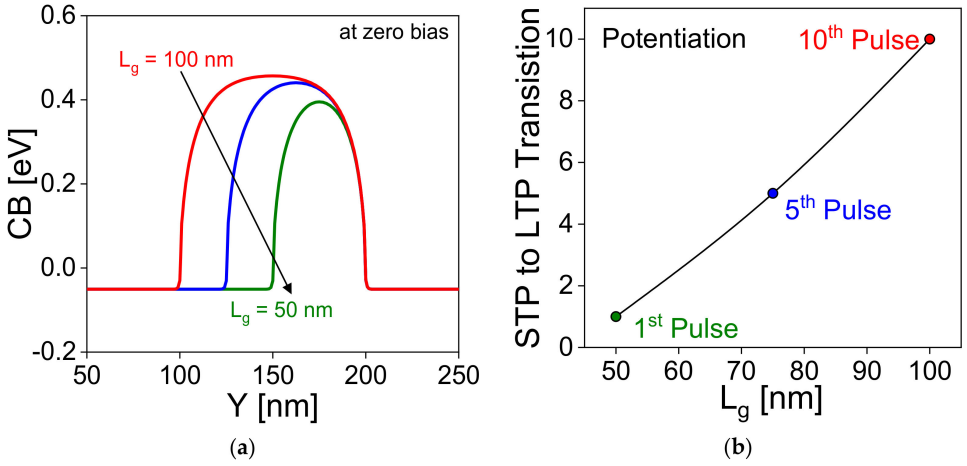


Figure 8. Transfer characteristics of the device during inference (read) operation for (**a**) potentiation (**b**) depression at different pulses. Transient analysis during read operation for (**c**) potentiation (**d**) depression at different pulses. Variation in conduction band (CB) during inference operation for different (**e**) potentiation and (**f**) depression pulses.

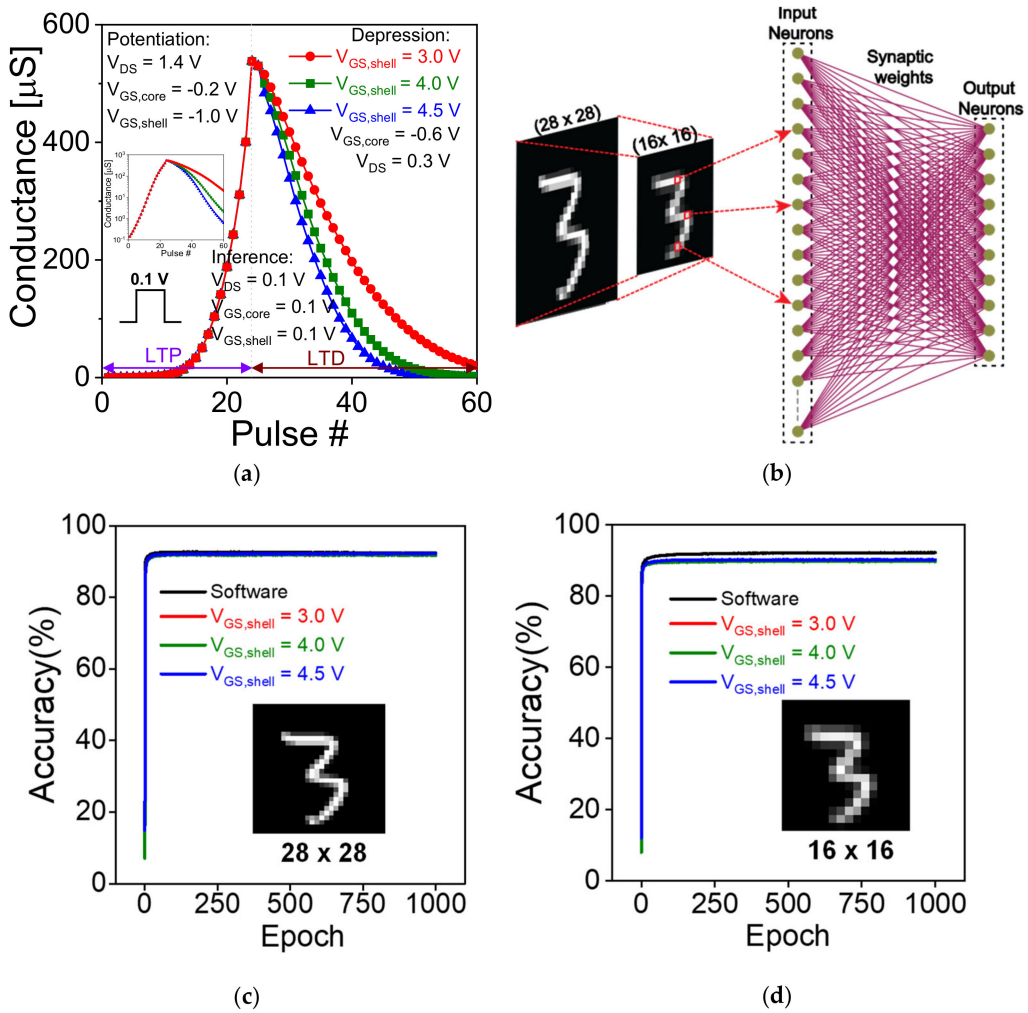
The trapped charges in the nitride layer lower the V_{TH} due to the increase in channel potential (lower the barrier for electron), and hence increases the drain current (higher weight) with increase in pulse. Figure 8e,f show the CB energy diagram during inference operation for different potentiation and depression pulses, respectively. Conduction band energies are extracted at below 1 nm of oxide/nitride/oxide (O/N/O) at $V_{DS} = V_{GS,core} = V_{GS,shell} = 0.1$ V. The same is sensed from Figure 8c for STP that drain current increases for a short time and start decreasing (forgetting) due to recombination of carriers during interval in the device, and thus approaches to the initial level (no pulse (device is at equilibrium condition)). For LTP (from the 10th pulse), current is higher than the STP current and retained up to 10^4 s due to trapped holes in the nitride layer, which helps to increase the channel potential during inference operation. These results (Figure 8a,c) confirm that this CSDG nanowire transistor is capable of both STP and LTP functions. In the case of LTD, the reverse process is observed, increase in repetitive pulse reduces the channel potential (increases the barrier as shown in Figure 8f) of the device due to de-trapping the holes from the nitride layer (Figures 5c and 6b), and hence increases the threshold voltage (lower weight) of the device as shown in Figure 8c. The same is illustrated in Figure 8d, increase in pulse reduces the current due to recombination of the carriers in the device, and thus current approaches to the initial state with increasing pulse.

Figure 9a shows the conduction band (CB) diagram at zero bias condition for different gate length (100 nm, 75 nm, and 50 nm). Reduction in gate length reduces the storage area for floating based memory, which reduces the retention time [34–39]. The operation of this synaptic transistor is based on the floating body effect, and charge trapping/de-trapping from the nitride layer. Thus, reduction in gate length reduces the minimum required potentiation pulses by which STP-to-LTP transit occurs as a function of gate length. Downscaling of gate length increases the electric field between the channel and source/drain junctions, which increases the tunneling in the device, and thus, minimum number of pulses are required for the STP-to-LTP transition decreases as shown in Figure 9b. As we scale down the device dimensions, the potentiation behaviour of the device remains the same except for the reduction in pulse number required for STP to LTP transition. Figure 10a shows the variation of conductance (weight) value of LTP and LTD operations with different pulses, respectively. In inset of Figure 10a shows the conductance value in logarithmic scale. From Figure 6b, it is evident that the conductance value for LTP operation is relatively linear compared to the LTD state because the charge trapped in the nitride layer is increasing logarithmically with an increase in the number of pulses (Figures 4d and 6a). In the case of LTD operation, conductance value is estimated with different shell gate voltage ($V_{GS,shell}$ of 3.0, 4.0, and 4.5 V). This shows that for shell gate voltage of 4.5 V, more number of holes are de-trapped from the nitride layer, and thus reduces the conductance value abruptly. For shell gate voltage of 4.0 V, the conductance is linear compared to 3.0 and 4.5 V because the amount holes de-trapped rate from the nitride layer is lower. Although an increase in $V_{GS,shell} > 4.5$ V (increasing the F–N tunneling probability), increases the memory window during depression but degrades the conductance value abruptly. In the same way, the LTP weight can also be modulated, and it is more prominent by core gate voltage ($V_{GS,core}$) because the tunneling is govern by ($V_{GS,core}$). Thus, to obtain the linear conductance value, voltages during operations (potentiation, depression, and inference) need to be optimized. The linearity in the conductance of the LTP and LTD curves affects the inference accuracy of the neural network because it is related to the degree of the synaptic weight change.



(**a**) (**b**)

Figure 9. Downscaling of gate length. (**a**) Variation of CB energy. (**b**) number of pulses required for the transformation from STP to LTP. CB and VB indicate conduction and valence band, respectively.



(**a**) (**b**) (**c**) (**d**)

Figure 10. (**a**)Variation in conductance value for Long term potentiation (LTP) and Long-term depression (LTD) characteristics of the CSDG device (**b**) schematic of the single layer neural network with the CSDG transistor as the synapse for Modified National Institute of Standards and Technology (MNIST) digit recognition. Digit recognition accuracy (%) as a function of the number of training epochs at three distinct depression voltages of the synaptic device for (**c**) 28 × 28 and (**d**) 16 × 16 MNIST dataset. Inset of (**c**,**d**) shows the MNIST image of digit "3" in 28 × 28 and 16 × 16 resolutions, respectively.

Finally, to investigate the learning and inference capabilities of the proposed synaptic device for hardware-based neural networks (HNN), we have simulated a single layer neural network (NN) [40] consisting of one input layer and one output layer as shown in Figure 10b. The synaptic weights (conductance values) obtained from the Potentiation/Depression data in Figure 10a was used for off-chip training of the NN. The designed NN was used to classify image data from a Modified National Institute of Standards and Technology (MNIST) dataset which consists of 60,000 training images and 10,000 test images of handwritten digits from "0" to "9". All the images are in grayscale format with a resolution of 28 × 28 pixels. The normalized pixel intensities in the interval [0,1] are linearized to form a column matrix with 784 elements which is then fed to the input of the NN. The input values (x_i) undergo vector matrix multiplication [27] with the corresponding weight values (w_{ij}) and is summed up to form $\sum_{i,j} w_{ij}x_i$ at each of the output neurons. i and j denote the number of input nodes and output nodes, respectively. The output at each of these neurons is then transformed using a rectified linear unit (ReLU) activation function. The output neuron with the highest probability for a particular input image is considered as the corresponding prediction from the NN. In the present work, we have also trained the NN using a 16 × 16 downscaled version of the MNIST dataset, so that the effective number of input nodes is reduced to 256. Figure 10c,d shows the variation of accuracy of digit recognition with the number of epochs for the 28 × 28 MNIST dataset using randomly initialized weight distribution (software-based) and device weights extracted for 3 distinct values of depression voltages ($V_{GS,shell}$) i.e., 3.0 V, 4.0 V and 4.5 V. The final accuracy of digit recognition for the weight update from devices with $V_{GS,shell}$ = 3.0 V, 4.0 V and 4.5 V after 1000 epochs was 91.88%, 91.91% and 92.28% respectively which is very close to the ideal software based NN accuracy of 92.36%. This high accuracy in image recognition reveals that the proposed synaptic device is highly suited for neuromorphic inference applications. Similarly, 16 × 16 MNIST images were used for the devices with $V_{GS,shell}$ = 3.0 V, 4.0 V and 4.5 V yielding an accuracy of 89.94%, 89.65% and 90.17% respectively. In comparison to the software-based recognition accuracy of 92.25%, there is only a marginal drop in accuracy for these devices, which indicates the high reproducibility of our synaptic devices for inference applications requiring reduced input data.

4. Conclusions

In this work, we have simulated a novel core-shell dual gate nanowire transistor as an artificial synaptic transistor with calibrated simulation models. The dual gate helps to achieve a deeper potential well for charge retention of the device. The analysis highlights that the combination of floating body effect and charge trapped in the nitride achieves short-term potentiation and long-term potentiation and depression. The results of the CSDG nanowire indicate the following.

1. Transformation from STP to LTP occurs at the 10th pulse and it can be modulated through core gate voltage ($V_{GS,core}$) because the tunneling is governed through $V_{GS,core}$.
2. The trade-off between change in threshold voltage, and linearity in, conductance is observed during depression operation.
3. We can investigate the learning and inference capabilities of the proposed synaptic device for hardware based neural networks (HNN).
4. A reliable and consistent digit recognition accuracy of 92.28% is achieved by a single layer neural network on the MNIST dataset.

Furthermore, the analysis highlights the feasibility of the proposed synaptic device for inference applications pertinent to neuromorphic computing.

Author Contributions: Design and optimization of the synaptic device structure, validation of the synaptic operation schemes by device simulation, and preparation of the manuscript draft, M.H.R.A.; design of the artificial neural network based on the proposed synaptic transistor array, evaluation

of the system accuracy, and preparation of the manuscript draft, U.M.K.; conception of the device structure and operation schemes, orientation of the directions of this research, organization of the workflow managing the overall research projects, and preparation of the final manuscript, S.C. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The data presented in this study are available on request from the corresponding author.

Conflicts of Interest: The authors declare no conflict of interest.

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nanomaterials

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Article

Organotrialkoxysilane-Functionalized Prussian Blue Nanoparticles-Mediated Fluorescence Sensing of Arsenic(III)

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Abstract: Prussian blue nanoparticles (PBN) exhibit selective fluorescence quenching behavior with heavy metal ions; in addition, they possess characteristic oxidant properties both for liquid–liquid and liquid–solid interface catalysis. Here, we propose to study the detection and efficient removal of toxic arsenic(III) species by materializing these dual functions of PBN. A sophisticated PBN-sensitized fluorometric switching system for dosage-dependent detection of As^{3+} along with PBN-integrated SiO_2 platforms as a column adsorbent for biphasic oxidation and elimination of As^{3+} have been developed. Colloidal PBN were obtained by a facile two-step process involving chemical reduction in the presence of 2-(3,4-epoxycyclohexyl)ethyl trimethoxysilane (EETMSi) and cyclohexanone as reducing agents, while heterogeneous systems were formulated via EETMSi, which triggered in situ growth of PBN inside the three-dimensional framework of silica gel and silica nanoparticles (SiO_2). PBN-induced quenching of the emission signal was recorded with an As^{3+} concentration (0.05–1.6 ppm)-dependent fluorometric titration system, owing to the potential excitation window of PBN (at 480–500 nm), which ultimately restricts the radiative energy transfer. The detection limit for this arrangement is estimated around 0.025 ppm. Furthermore, the mesoporous and macroporous PBN-integrated SiO_2 arrangements might act as stationary phase in chromatographic studies to significantly remove As^{3+}. Besides physisorption, significant electron exchange between Fe^{3+}/Fe^{2+} lattice points and As^{3+} ions enable complete conversion to less toxic As^{5+} ions with the repeated influx of mobile phase. PBN-integrated SiO_2 matrices were successfully restored after segregating the target ions. This study indicates that PBN and PBN-integrated SiO_2 platforms may enable straightforward and low-cost removal of arsenic from contaminated water.

Keywords: prussian blue nanoparticles; organotrialkoxysilane; silica beads; arsenite; arsenate; water decontamination

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1. Introduction

Large numbers of people in Bangladesh and India are exposed to arsenic contamination in potable water. Metallurgical, agricultural, and industrial processes result in the discharge of arsenic into soil and water [1,2]. Long-term exposure to arsenic, even at low concentrations, can lead to oncological, immunological, neurological, and endocrine effects [3]. The World Health Organization recently set an arsenic limit of 10 µg/L for drinking water (Holm, 2002) [4]. Natural water predominantly contains the inorganic species arsenate [$HAsO_4^{2-}$, As(V)] and arsenite [AsO_2^{-}, As(III)]. Inorganic As(III) was noted to be more toxic (10 times), mobile, and water-soluble (4–10 times) than As(V) [5]. The conversion rate of As(III) (arsenite) to As(V) (arsenate) in oxygenated water is a slow process, which depends on certain specific conditions [6]. Consequently, there is an alarming need to develop novel methods for sensing and removal of arsenic from drinking water [7].

Prussian blue nanoparticles (PBN) contain metal in two different oxidation states, Fe^{+3} and Fe^{+2}; these materials are known for their advanced peroxidase mimetic activity [8–10].

The charge transfer between the two iron species is responsible for the deep blue color of the complex [11]. Bi-metallic coordination compound PBN are a well-known inorganic material for electrocatalytic applications [12–15]. Several reports demonstrated the formation of mixed metal analogues, which involve straightforward replacement of the ferric/ferrous ion with another metal having a similar chemical state [16–18]. The properties of Prussian blue complex can be readily modified depending upon the nature of the constituent metal pair. Iron hexacyanoferrate synthesized via traditional synthetic routes (e.g., co-precipitation and electrosynthesis) do not exhibit appropriate processability for technical applications. We processed PBN from a single precursor involving the active role of the organotrialkoxysilane, which not only controlled the nucleation and solubility but also provided stability to the contents of reaction medium [19]. In addition, the PBN made from a single precursor were found to act as a light quenching material [20]; the photoactivity of the materials was examined using fluorescence imaging. Earlier studies show that organotrialkoxysilanes such as 3-aminopropyltrimethoxysilane (APTMS) allow the conversion of a single precursor, potassium hexacyanoferrate, to Prussian blue; this material was used for electrocatalytic detection of dopamine [21]. We further examined the use of another organotrialkoxysilane, 2-(3,4-epoxycyclohexyl) ethyltrimethoxysilane (EETMSi), in the presence of cyclohexanone for the controlled synthesis of PBN as a light quenching material.

Several methods, including iron oxide-coated sand, manganese greens, and iron ores, were previously described for arsenic removal [22]. Spectrophotometric and fluorometric methods have been previously studied to estimate the trace amounts of arsenite in water [23–25]. PBN, which include iron of two different oxidation states in a metal framework, may undergo specific interactions with As(III). Thus, we examined the fluorescence quenching ability of the PBN in the presence of arsenic(III). A novel result based on fluorescent sensing of arsenic was recorded, indicating the interaction between PBN and arsenic(III). PBN within a matrix were subsequently studied for use in arsenic removal.

Silica (SiO_2) beads are a non-toxic and inexpensive matrix, which may be used as a template to synthesize PBN using organotrialkoxysilane. PBN were inserted into mesoporous SiO_2; the PBN became embedded in the accessible SiO_2 pores. The PBN@SiO_2 was used for As(III) removal and its subsequent oxidation into arsenate through an interaction with the iron species in the material. This adsorption–oxidation process was demonstrated with PBN@SiO_2 under different pH conditions to analyze the efficacy of the oxidant system. The high uptake efficiency of PBN@SiO_2 (95%) indicated that this material is attractive for use in As(III) removal. XPS, ICP, and HPLC techniques were used to detect and quantify As(III) species. The PBN@SiO_2 was separated easily through centrifugation; this recycled material also showed As(III) removal activity. The proposed As(III) removal process is more cost effective over those reported to date. The ability to recycle PBN@SiO_2 adds to the economic viability of this process.

2. Experimental Section

2.1. Materials

Potassium ferricyanide was purchased from Merck India (Bengaluru, Karnataka, India). Silica beads (50 μm) and silica nanoparticles (200 nm) were purchased from Sigma-Aldrich (Bengaluru, Karnataka, India). Sodium arsenite was purchased from S D Fine-chem Limited (Mumbai, Maharashtra, India), and Azure-B was obtained from Sisco Research Laboratories Pvt. Ltd. (Mumbai, Maharashtra, India). 2-(3,4-epoxycyclohexyl)ethyltrimethoxysilane (EETMSi) and cyclohexanone were obtained from Sigma-Aldrich (Bengaluru, Karnataka, India). In addition, the remaining chemicals were of analytical grade and procured from commercial sources. The working solution of As(III) was freshly prepared with Milli-Q water using sodium arsenite ($NaAsO_2$) and stored in a dark freezer. Milli-Q water was used throughout the experiment to avoid interference from contaminants.

2.2. Synthesis of PBN, PBN@SiO_2 and PBN@MSNP Mediated through EETMSi

2.2.1. EETMSi-Mediated Formation of PBN

The synthesis of PBN was accomplished using [2-(3,4-Epoxycyclohexyl)ethyl]trimethoxysilane(EETMSi) and cyclohexanone from the single precursor potassium ferricyanide via chemical reduction. The homogeneous colloidal sol of Prussian blue nanoparticles (PBN) was prepared by adding 20 µL of EETMSi (0.1 M) to 100 µL of potassium ferricyanide (0.03 M) under stirring conditions. Subsequently, 20 µL of cyclohexanone was added to the reaction mixture; this mixture was kept in an oven at 343 K for 8 h. The blue-colored colloidal suspension of PBN was characterized byX-ray diffraction (XRD), Transmission electron micrpscopy (TEM), etc.

2.2.2. EETMSi-Mediated Formation of Prussian Blue Nanoparticles Modified Silica (PBN@SiO_2)

Mesoporous silica was used to obtain PBN-confined mesoporous silica (PBN@SiO_2). Typical synthesis involved a multistep procedure as follows: At first, 10 mg of mesoporous silica beads were suspended in 100 mL of EETMSi (1.2 M) aqueous solution under constant stirring conditions. After 3 h, un-adsorbed EETMSi was extracted with methanol, followed by centrifugation. 200 mL of potassium ferricyanide [$K_3Fe(CN)_6$] aqueous solution (0.03 M) was added to the alkoxysilane-modified SiO_2 suspension under vigorous stirring conditions (800 rpm). Cyclohexanone was added to the alkoxysilane-modified $K_3Fe(CN)_6$@SiO_2 suspension under vigorous stirring and left to stand in oven at 338 K overnight. The unreacted $K_3Fe(CN)_6$ and unabsorbed PBN were removed via washing (five times) with methanol/water (2:1) solvent. The residual material was collected after centrifugation; a drying step was subsequently performed.

2.2.3. EETMSi-Mediated Formation of PBN@MSNPs

Mesoporous silica nanoparticles (MSNPs) were used to prepare Prussian blue nanoparticle-embedded mesoporous silica nanoparticles (PBN@MSNP). Ten milligrams of mesoporous silica nanoparticles (average particle size 200 nm and pore size 6 nm) were suspended in 100 mL of EETMSi (1.2 M) aqueous solution under stirring conditions. After 3 h, un-adsorbed EETMSi was removed with methanol, followed by centrifugation. Two hundred milliliters of potassium ferricyanide aqueous solution (0.03 M) were added to the alkoxysilane-modified MSNP suspension under vigorous stirring conditions (800 rpm). Cyclohexanone was added to the alkoxysilane-modified $K_3Fe(CN)_6$@MSNPs suspension under continuous stirring and left to stand in oven at 338 K overnight. The unreacted $K_3Fe(CN)_6$ and unabsorbed PBN were removed via washing (five times) with methanol/water (2:1) solvent. The residual material (PBN@MSNPs) was collected after centrifugation; a drying step was subsequently performed.

2.3. Materials Characterization

The particle size and morphology of as-synthesized PBN/PBN@SiO_2 and PBN@MSNP were analyzed using high-resolution transmission electron microscopy (HRTEM) with 800 and 8100 instruments (Hitachi, Tokyo, Japan) at an acceleration voltage of 200 kV. The topographical properties of as-synthesized PBN over SiO_2 were analyzed using a field emission scanning electron microscopy instrument (FEI (S.E.A.) Pte Ltd., Singapore). The elemental confirmation and mapping analyses were accomplished with an EDX attachment (Oxford Instruments plc, Abingdon, UK). A Rigaku X-ray diffractometer (Rikagu, Tokyo, Japan) with Cu Ka radiation (λ = l.5406 A^0) was used to evaluate diffraction data. The XRD analysis was performed over the scan range of 10–90° for PBN. FTIR spectra were recorded on an ALFA-ATR Fourier transform infrared spectrometer (Bruker, Ettington, Germany). XPS analysis was performed using an ESCA/AES System (Surface Nano Analysis, GmbH, Berlin, Germany), which was equipped with an Al-Kα (1486.6 eV) X-ray source operating at a power of 385 W and a PHOBIOS 150 3D energy hemispherical analyzer with a delayline detector (SPECS Surface Nano Analysis GmbH, Berlin, Germany). The C-1s peak (284.5 eV)

was used as an internal reference to calibrate the absolute binding energy. The quantitative detection of elements was performed through ICP techniques. Fluorescence analysis was performed using a 7100 spectrophotometer (Hitachi, Tokyo, Japan). Arsenic speciation was performed using high-performance liquid chromatography (HPLC) with a Shim-packed GIST C18 chromatography column encompassing a hydrophobic (non-polar) stationary phase (column length = 75 mm, inner diameter = 7.6 mm) for the determination of all species. Ammonium phosphate solution was used as an eluent for the entire HPLC experiment. The HPLC mobile phases of ammonium phosphate solution with pH 6.9 were prepared by mixing monobasic ($NH_4H_2PO_4$) and dibasic ($(NH_4)_2HPO_4$) salt solutions with an appropriate ratio.

2.4. Fluorometric Method

A fluorometric method was used for the determination of As(III) species. Fluorescein (Flo) was used as a probe molecule (λex = 480 nm, λem = 510 nm) for the estimation of As(III) species. The fluorescence experiment was performed under neutral pH (6.8) conditions using Milli-Q water. Different concentrations of As(III) standard solution (10 ppm to 320 ppm) were prepared by adding appropriate amounts of sodium arsenite to Milli-Q water. The result was obtained using the effective concentration of Flo, PBN, and As(III).

3. Results and Discussion

3.1. Organotrialkoxysilane-Mediated Synthesis of PBN Analogs

Organotrialkoxysilane with an amine functional group, APTMS, in the presence of cyclohexanone was previously used for the controlled conversion of a single precursor, $K_3[Fe(CN)_6$, into Prussian blue nanoparticles under ambient conditions [20]. Subsequently, 2-(3,4-epoxycyclohexyl) ethyltrimethoxysilane (EETMSi) was used to make PBN in the absence of cyclohexanone [9]. Although the process enabled efficient conversion of single precursor, $K_3[Fe(CN)_6$, into Prussian blue nanoparticles, the duration was substantially longer. Accordingly, we attempted to use cyclohexanone along with EETMSi to obtain PBN from a single precursor pathway. Indeed, the process enabled the rapid formation of PBN, as shown in Figure 1; additional details on this process are provided below.

3.1.1. PBN as a Homogeneous Suspension

Slow decomposition under hydrothermal conditions via single precursor synthesis readily produced a blue-colored solution of PBN. The TEM micrographs in Figure 1A,B revealed well-dispersed nanocubes of PBN with an average diameter of 30 nm. The histogram (inset of Figure 1A) shows broad size distribution of crystalline nanoparticles, ranging between 27 and 53 nm. The average width of nanoparticles may be altered by modifying the EETMSi/Fe^{3+}/cyclohexanone feed ratio and thermal conditions. Accordingly, we investigated the role of EETMSi in combination with a ketonic reducing agent. The EDX and TEM data provided information on the chemical composition and nanoparticle structure, respectively. Figure 1D shows the contributions to the EDX spectrum from the Fe Kα peak at 6.4–7.0 keV and 0.9 keV, the Cu peak at 7.8–9.0 keV, and the Si peak at 7.057 keV; Fe peak and the peaks for N, O, and C are also noted. The XRD spectrum shown in Figure 1E reveals nearly all the planes assigned to 2θ values as per JCPDS # 73-0687, 17.4° (200), 24.7° (220), 35.3° (400), 39.6° (420), and 43.7° (422), 50.0° (440), 53.9° (600), 57.2° (620), 66.1° (640), and 68.9° (642).

3.1.2. PBN Confined in Mesoporous Silica (PBN@SiO_2)

We also attempted to insert PBN into mesoporous silica through the synergistic action of EETMSi and cyclohexanone; the product is represented as PBN@SiO_2. Mesoporous silica with a particle size of 50 micrometers and a pore diameter of 6 nm was used for the synthetic insertion of PBN; these materials have use in column chromatography. SEM micrographs in Figure 2A–C show the topographical features of PBN@SiO_2 and the narrow size distribution of the PBN in the SiO_2 matrix. Figure 2D shows the EDX data for

PBN@SiO_2, which shows a silicon content of 31.9% elemental weight; the inset of Figure 2A shows photographic images of mesoporous SiO_2 (I) and PBN@SiO_2 (II). The XRD spectra of as-made PBN@SiO_2 and mesoporous SiO_2 are shown in Figure 2E(a–b). The results for as-made PBN@SiO_2 and mesoporous SiO_2 demonstrate a broad peak, which is assigned to the 101 plane of amorphous SiO_2 (Figure 2E(a)); additional peaks for as-made PBN@SiO_2 are assigned to 220, 220 and 400 lattice planes of crystalline PBN. After exposure to the EETMSi-mediated PBN-laden formulation, an alteration in the SiO_2 pore size was detected via BET analysis (Table 1).

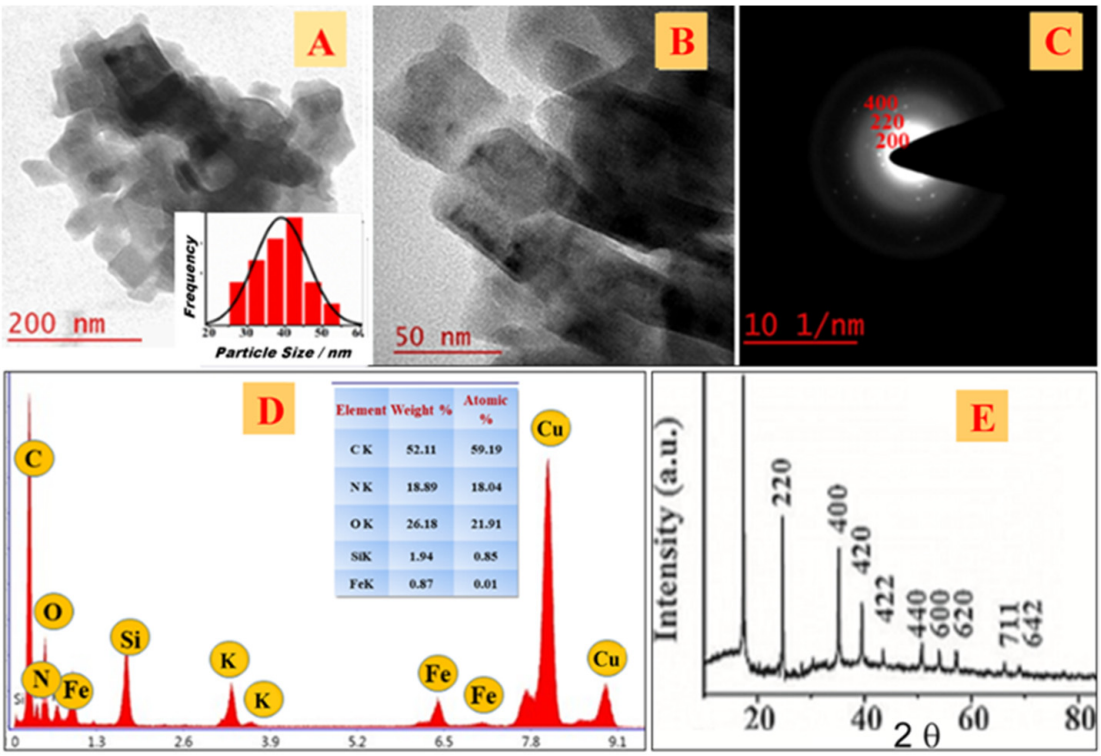


Figure 1. TEM images of PBN at different magnifications (**A**,**B**). Bar histogram displaying the particle size distribution curve of the nanoparticles (inset of Figure 1A). SAED pattern of as-synthesized particles (**C**), EDX profile with all the anticipated elements (**D**), XRD of EETMSi-functionalized PBN (**E**).

Table 1. Parameters calculated from BET nitrogen gas adsorption isotherm.

Sample Name	Surface Area $\times 10^4$ cm^2/g	Pore Size (nm)
SiO_2 Bead	474.8	6.1
PB@SiO_2 Bead	426.8	4.3

3.1.3. PBN-Doped Mesoporous Silica Nanoparticles (PBN@MSNP)

We also undertook the synthetic incorporation of PBN within mesoporous silica nanoparticles. Silica nanoparticles (MSNP) with an average particle size of 200 nm and a pore size of 6 nm were used for this purpose. The porous nanocomposite was obtained primarily in two steps: (a) surface functionalization of the matrix by EETMSi, followed by (b) the uniform distribution of metal precursor throughout the network and subsequent reduction to form nanoscale particles. The in situ growth of PBN was pH controlled. The soluble Fe^{3+} species easily adhered to the pore channels in the presence of capping agent EETMSi. The HRTEM micrograph of bare MSNPs (Figure 3a(A)) shows a porous skeleton of spherical morphology. Figure 3a(B) shows PBN inside the mesoporous silica nanoparticles (encircled in red) [26]. The selected area electron diffraction (SAED) pattern of the corresponding hybrid nanoparticle assembly (PBN@MSNP) is shown in Figure 3a(C).

The zeta potential value was obtained from dynamic light scattering (DLS) data to understand the solution stability of particles. As shown in Figure 3a(D), the value of zeta potential is nearly −23 mV (i.e., towards the negative side); hence, the PBNPs are also negatively charged.

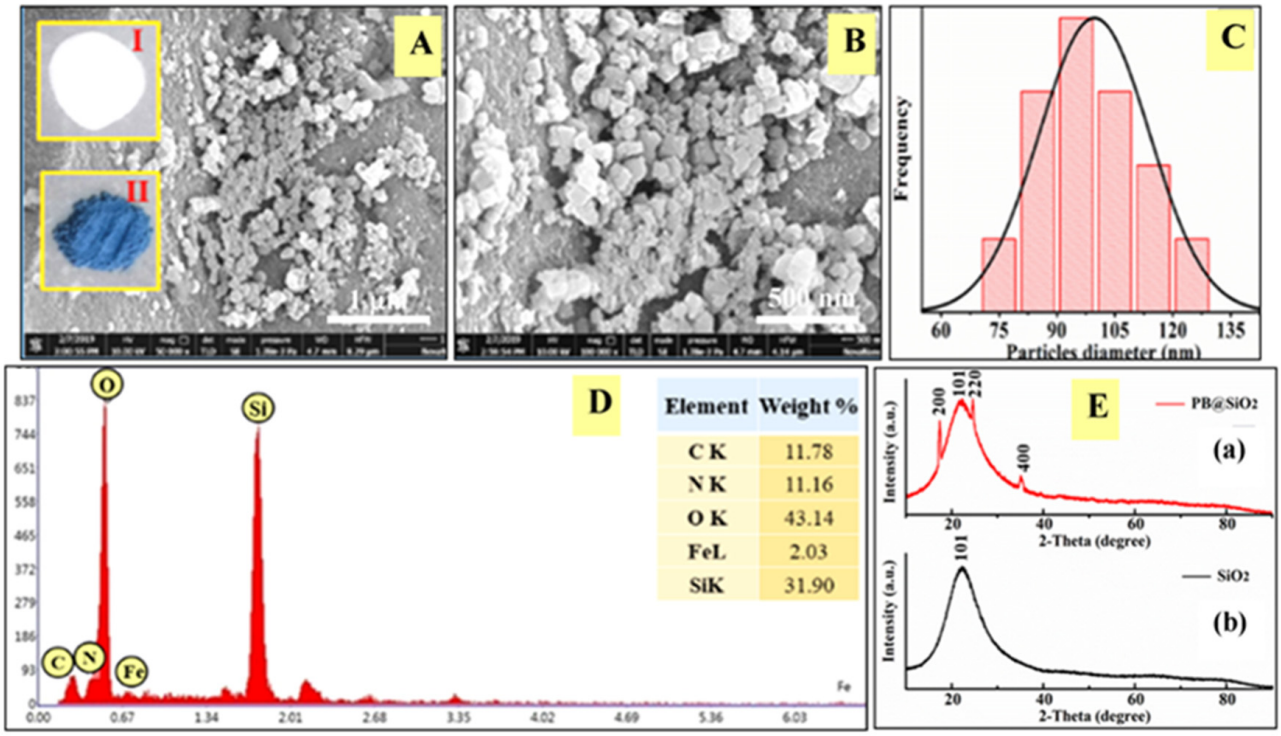


Figure 2. (**A**,**B**) HRSEM images of PBN@SiO_2 at two different magnifications. Inset of (**A**) shows photographic images of mesoporous silica (I) and PBN-inserted mesoporous silica (II). (**C**) The particle size distribution of PBN within mesoporous silica. (**D**) The EDX spectrum of PBN-inserted mesoporous silica. (**E**) XRD spectra of SiO_2 (**a**) and PBN@SiO_2 (**b**).

The EDX spectrum of PBN@MSNPs is shown in Figure 3a(E). The EDX mapping of the organotrialkoxysilane-functionalized PBN@MSNPs with the elemental composition of (B) carbon, (C) nitrogen, (D) oxygen (E) iron, and (F) silicon is shown in Figure 3b. The crystallographic data for as-prepared PBN@MSNPs and blank MSNPs are shown in Figure 3a(F). The peaks indexed at 2θ values of 17.6° (200), 24.3° (220), and 37.8° (400) indicated the successful insertion of crystalline PBN within the SiO_2 matrix; per JCPDS # 73-0687, 17.4° (200), 24.7° (220), 35.3° (400), 39.6° (420), and 43.7° (422), 50.0° (440), 53.9° (600), 57.2° (620), 66.1° (640), 68.9° (642), and 77.2° (820) can be indexed as the PB cubic space group Fm3m.

3.2. FTIR Analysis of PBN@SiO_2

The peak at 2086 cm^{-1} in the FTIR spectrum (Figure 4A of PBN may be attributed to the CN stretching mode of the Fe(II)-C-N-(III)Fe moiety in PBN. The broad bands at 3402 cm^{-1} and 1642 cm^{-1} in the spectrum correspond to OH-stretching and H_2O bending mode of the interstitial water molecule, respectively, within the PBN lattice. The strong band near 2885–2990 cm^{-1} corresponds to the C-H stretching vibration of sp^2-hybridized carbon in cyclohexanone.

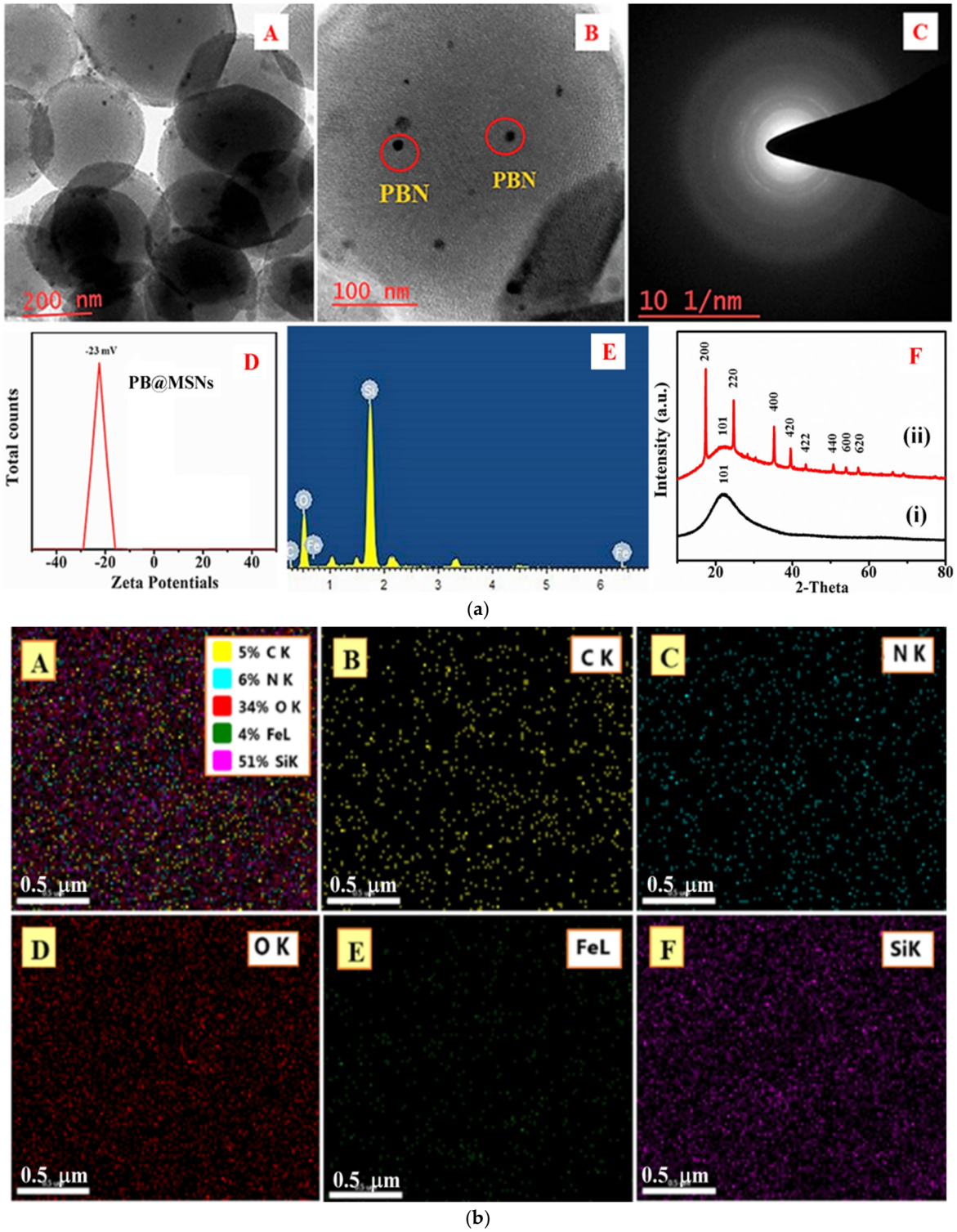


Figure 3. (**a**) (**A**) HRTEM image of organotrialkoxysilane-functionalized Prussian blue nanoparticles (PBN@MSN), (**B**) micrograph showing the magnified view of bulk-confined PBN (encircled in red) in mesoporous silica, (**C**) SAED pattern of the corresponding hybrid nanoparticle assembly (PBN@MSN), (**D**) stability profile of PBN@MSN in terms of zeta potential measurement, and (**E**) EDX spectrum of PBN@MSNP. (**F**) XRD profile for MSNPs (i) and as-synthesized PBN@MSNPs (ii). (**b**) (**A**) Mapping analysis of organotrialkoxysilane-functionalized Prussian blue nanoparticles with elemental composition (**B**) carbon, (**C**) nitrogen, (**D**) oxygen (**E**) iron, and (**F**) silicon.

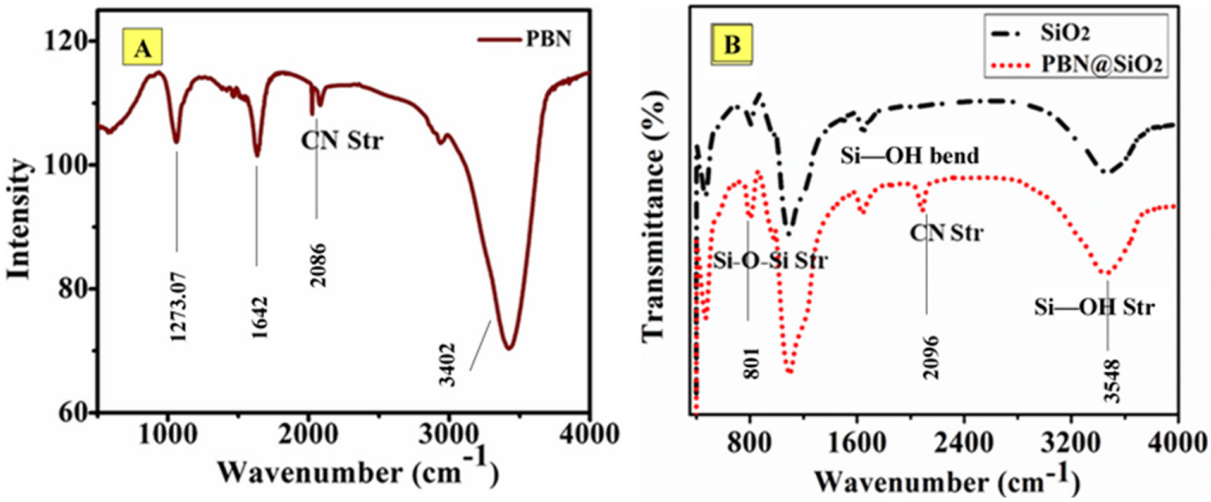


Figure 4. (**A**) FTIR spectrum of as-synthesized PBN; (**B**) FTIR spectra of (black line) SiO_2 and (red line) as-synthesized PBN@SiO_2.

The broad bands centered at 3548 cm^{-1} and at 1632 cm^{-1} are assigned to the stretching and bending vibrations of silanol groups (Si–OH), respectively, in the silica beads [27]. The bands at 1093 cm^{-1} and 801 cm^{-1} in the spectrum are associated with the anti-symmetric and symmetric stretching modes (Si–O–Si) of SiO_4 units. The prominent peak at 2096 cm^{-1} (Figure 4B is attributed to the stretching mode of Fe(II)-CN-(III)-Fe moiety in PBN [28] and indicates the successful formation of nanoparticles over SiO_2.

3.3. Fluorometric Study

3.3.1. Effect of the Addition of As(III) on the Fluorescent Intensity of Fluorescein

Since PBN have already been established as light quenching material, the PBN-mediated fluorescence quenching of fluorescein was evaluated. The impact of As(III) on fluorophore activity was studied via adding a different concentration of As(III) solution to a fixed Flo concentration. Subsequently, 0.01 mL of As(III) (10–320 ppm) and 10 µL of Flo solution (0.2 mM) were transferred into 2 mL of Milli-Q water and allowed to stand for 2 min at room temperature prior to fluorescence analysis. The fluorescence intensity of Flo was found to be enhanced as the function of As(III) (Figure 5A,B). At a lower As(III) concentration, a less pronounced enhancement phenomenon was observed. This result revealed that the extent of the interaction between Flo molecule and As(III) occurred to a higher extent at a higher As(III) concentration (up to 1.5 fold). The emission intensity was found to enhanced three-fold when the concentration of As(III) was elevated from 0.05 ppm to 2 ppm (effective concentration).

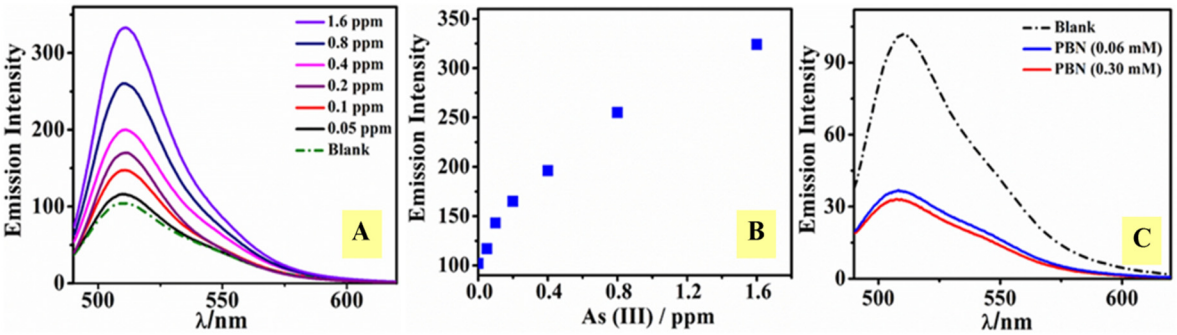


Figure 5. Fluorescence emission spectra of Flo (blank) in the presence of different As(III) concentrations from 0.05 ppm to 1.6 ppm (**A**). Plot of fluorescence intensity of Flo (0.2 mM) after exposure to a variable concentration (0.05–1.6 ppm) of As(III) (**B**). Effect of PBN addition (0.06 mM, 0.3 mM) over Flo (0.2 mM) fluorescence (**C**).

3.3.2. Interaction of Fluorophore with PBN

PBN were employed to observe the effect of the nano-sized particles over Flo. A constant amount of PBN nanosol (0.3 mM) was added to a known concentration of Flo (0.2 mM); the mixture was allowed to stand at room temperature for 2 min. The results revealed that PBN quenched the fluorescence property of Flo as shown in Figure 5C. Furthermore, the effect of PBN concentration over the emission intensity of Flo was investigated. Mixtures containing various concentrations of PBN with Flo were used to understand the interaction of nanoparticles with the fluorophore. The mixtures (i) PBN (0.06 mM) with Flo (0.2 mM) and (ii) PBN (0.3 mM) with Flo (0.2 mM) were evaluated. It was shown that EETMSi functionalized PBN acted as a quencher for Flo since the intensity of the fluorophore was found to diminish in the presence of PBN (Figure 5C). On increasing the concentration of PBN from 0.06 mM to 0.3 mM, only a small reduction in the emission intensity was observed (Figure 5C).

3.3.3. Effect of As(III)/PBN System over Flo Intensity

To understand the active role of PBN over As(III) interaction, we performed two experiments. In the first experiment, different concentrations of As(III) varying from 0.05 ppm to 1.6 ppm (effective concentration) were added to the fixed content of Flo (0.3 mM); the Flo-As(III) system was then exposed to a constant amount of PBN (0.3 mM) (as shown in Figure 6). In the second experiment, PBN (0.3 mM) were initially added to the Flo solution (0.2 mM); a variable concentration of As(III) between 0.05 ppm and 1.6 ppm (effective concentration) was then added to the PBN-Flo system (Figure 7). The substantial fluorescence quenching of the Flo-As(III) system in the presence of PBN was calculated using the relation F_0/F, where F_0 and F denote the fluorescent intensity of the Flo-As(III) system in the absence and in the presence of PBN, respectively (Figure 8A). Similarly, the substantial fluorescence quenching of the Flo system in the presence of PBN was calculated using the relation F_0/F, where F_0 denotes the fluorescence intensity of the Flo system in the absence of PBN and As(III), and F denotes the fluorescence intensity of Flo in the presence of PBN and As(III) (Figure 8B).

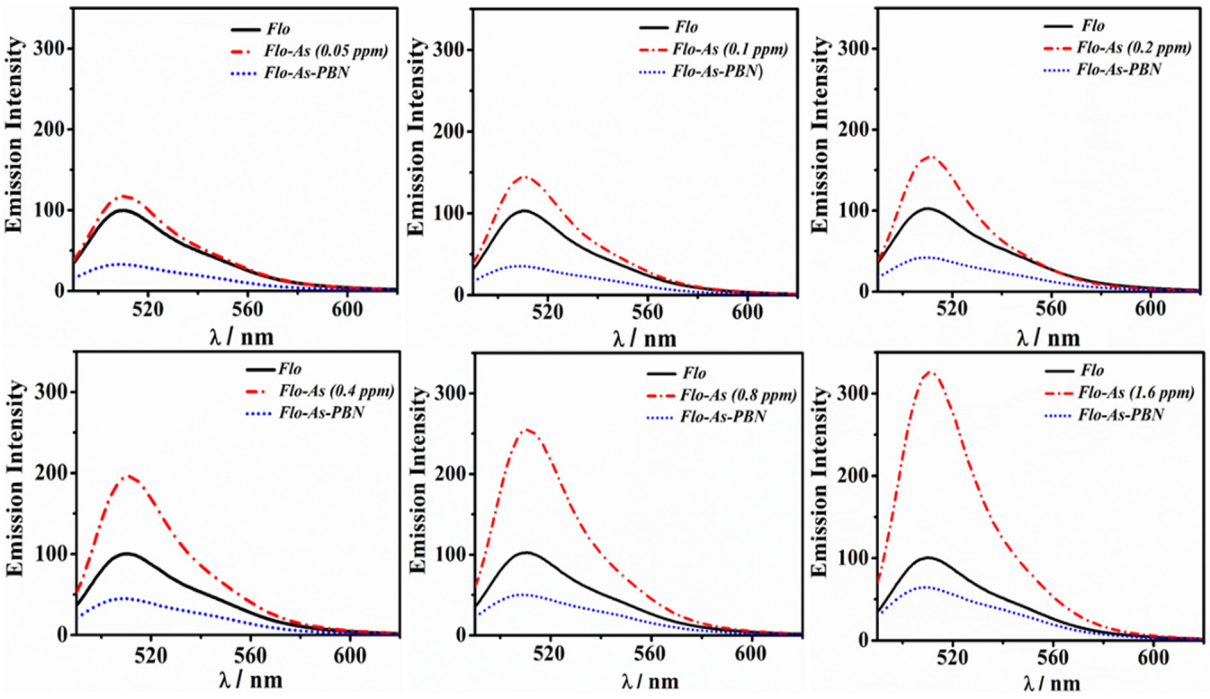


Figure 6. Study of the impact of PBN addition (10^{-1}) over the emission intensity of Flo-As(III) system by varying the As(III) solution (0.05–1.6 ppm) and keeping a constant concentration of Flo (0.2 mM) and PBN (0.3 mM).

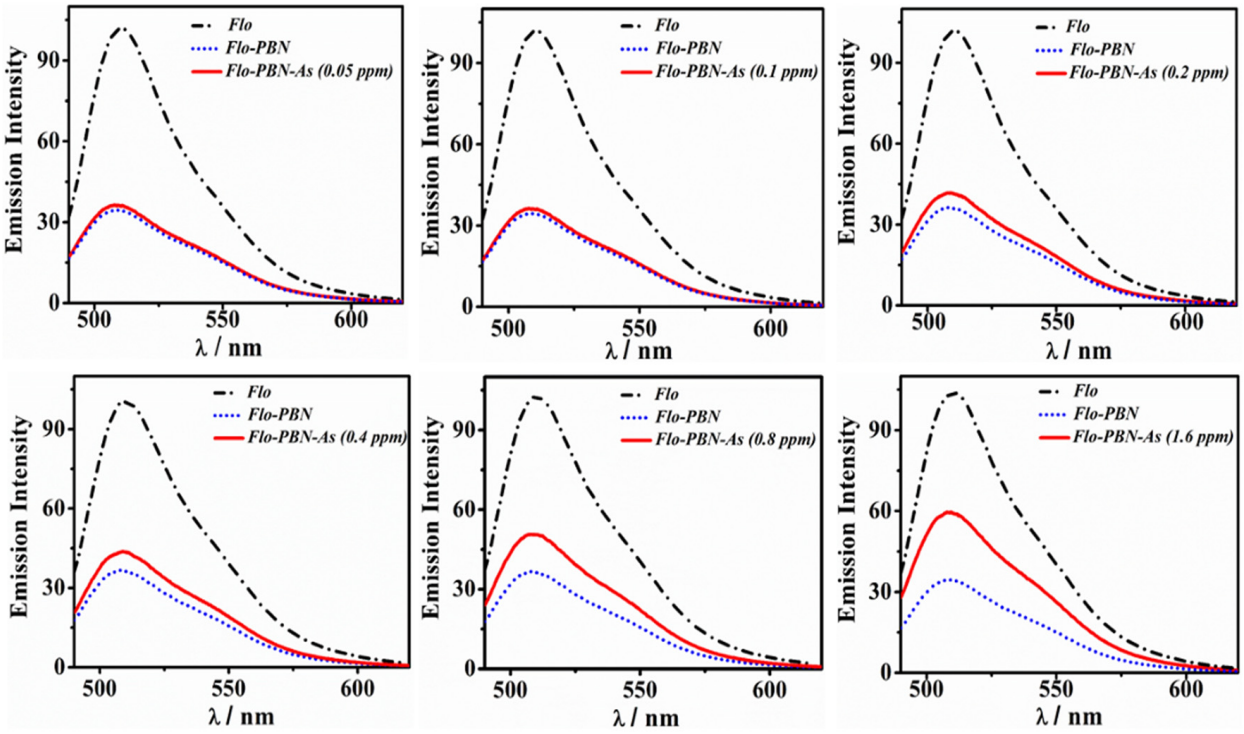


Figure 7. Study of the influence of As(III) addition over the emission spectra of the quenched Flo-PBN system by adding different concentrations of As(III) solution (0.05–1.6 ppm) and keeping a constant concentration of Flo (0.2 mM) and PBN (0.3 mM).

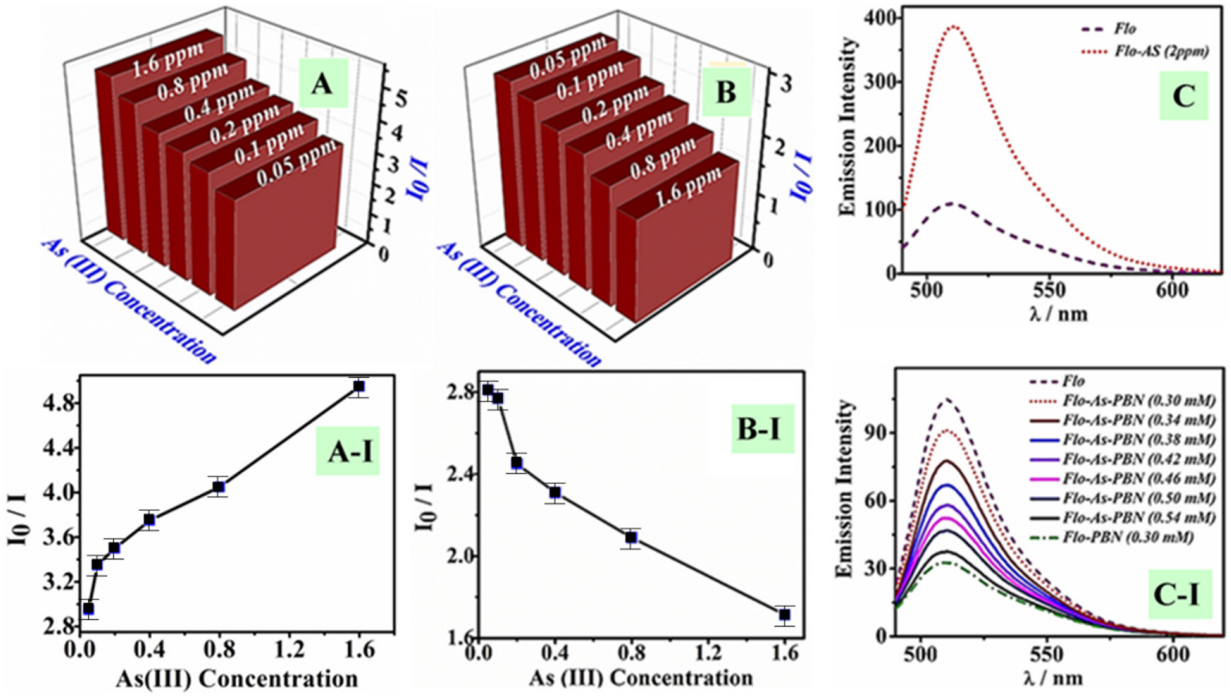


Figure 8. Bar diagram displaying fluorescence quenching (FQ) with respect to the variable concentration (effective concentration) of As(III) for the PBN@Flo-As(III) system (**A**) and the As(III)@PBN-Flo system (**B**). Plots of fluorescence intensity of the Flo-PBN system with respect to a variable content of As(III), showing concentration-dependent fluorescence quenching in both circumstances (**A-I**,**B-I**), with error bars representing the standard deviation. Emission spectra displaying the effect of adding 2 ppm of As(III) to the emission intensity of Flo (**C**). The required amount of PBN for complete quenching by adding various amounts of PBN to the Flo-As(III) system (**C-I**) and Flo.

It was observed that As(III) interacted predominately with the available quantity of the PBN moiety; the residual available As(III) was associated with the rise in emission intensity after interacting with Flo (Figure 8C-I). The subsequent addition of PBN achieved maximum quenching after interacting with available As(III), as displayed in Figure 8C-I. This result indicates that 0.54 mM PBN was sufficient to obtain complete interaction with 2 ppm arsenite. A similar concentration of 2 ppm of As(III) was added to the Flo-PBN system, which contained both PBN and Flo. The results (Figure 8A-I and Figure 8B-I) showed a decrease in fluorescent intensity of Flo-As(III) and Flo as a function of PBN; PBN altered the fluorescence influencing properties of As(III). It is surmised that Prussian blue interacted with As(III) more efficiently than the Flo-As system throughout the fluorescence process. A separate experiment was performed to discover the PBN loading for complete removal of As(III) from a concentration of 2 ppm (effective concentration). For this study, primary emission spectra of Flo-As(III) were recorded while adding As(III) aqueous solution (2 ppm) to the blank solution containing Flo (0.2 Mm) only (Figure 8C). A similar concentration of 2 ppm of As(III) was added to the Flo-PBN system, which contained both PBN.

3.4. As(III) Decontamination from Aqueous Solution Using PBN@SiO_2

The heterogeneous PBN@SiO_2 system was studied in order to understand the dynamic interaction occurring between As(III) and PBN. Accordingly, inexpensive and non-reactive silica beads were used for the modulation of active PBN in the formulation of the heterogeneous matrix. Heterogeneous methods are considered to play an influential role in catalysis due to their straightforward separation and large-scale applicability. For As(III) decontamination, the as-synthesized PBN@SiO_2 (0.05 g) was successfully packed in a column of 10 mm diameter. The standard As(III) solution (10 ppm) was prepared via adding an appropriate amount of sodium arsenite salt in Milli-Q water; 10 mL of the solution was passed through the PBN@SiO_2 enclosed column. The fluorescence analysis of separated supernatant (PBN@SiO_2 processed) was performed using Flo (0.2 mM) under similar conditions. In this study, 10 µL of as-eluted supernatants (PBN@SiO_2 processed and unprocessed As(III) solution) were added separately with Flo and left to stand at room temperature for 2 min. Their emission spectra were recorded to understand PBN@SiO_2 interactions with As(III). Unprocessed As(III) solution was observed to enhance the emission intensity of Flo many-fold (Figure 9A) as compared to the PBN@SiO_2 processed As(III) solution (Figure 9B).

PBN@SiO_2 was shown to significantly remove the As(III) from the contaminated solution. The ICP analysis of PBN@SiO_2 processed As(III) aqueous solution was performed to quantify the arsenic concentration in the solution. The result showed 0.0018 ppm arsenic (As) content for the PBN@SiO_2 processed As(III) solution. In addition, 0.13 ppm Fe content was also detected in the processed As(III) solution. The ICP analysis indicated that some of the iron species of PBN ($[Fe^{III}[Fe^{II}(CN)_6]$) leached out with the eluent during interaction with the As(III) species. To investigate the presence of active iron species in the eluent, we studied the addition of ferrous sulfate with active ferrous species (Fe^{+2}) to the colorless supernatant eluent. During this process, we added the ferric chloride-containing active ferric species to the colorless supernatant eluent. We observed that colorless supernatant changed immediately to an intense blue color (resembling the Prussian blue color) when ferric chloride was added. However, no such changes were observed when ferrous sulfate (containing Fe^{+2}) was added.

We performed a fluorometric experiment in which supernatant (SN) was employed to observe its modulation of the Flo fluorescence properties. Fluorescent emission spectra were recorded after adding Flo (10 µL) to 10 µL of PBN@SiO_2 processed supernatant (SN). A small change in intensity (I_o = 102.23) was observed with respect to the Flo (I_o = 98.74) as seen in Figure 9C (1 and 2). A study that involved adding ferric chloride to the Flo-supernatant (Flo-SN) mixture showed that the Flo fluorescence property was quenched (I = 31.73) when compared to Flo (I = 98.74), as shown in Figure 9C (3). Supernatant-

containing ferrocyanide species had an instant interaction with the added ferric chloride, which instantly converted into PBN.

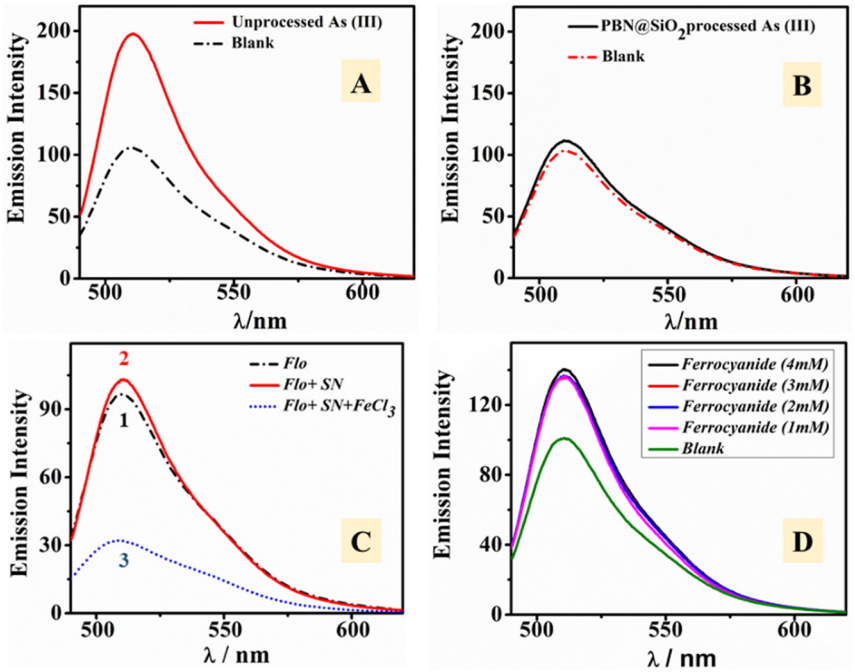


Figure 9. Fluorescence emission spectra of Flo with unprocessed (**A**) and PBN@SiO_2 processed (**B**) As(III) solution. Identification of ferrocyanide species in supernatant on the addition of ferric chloride via fluorescence quenching (**C**). Study of the effect of ferrocyanide species (1–4 mm) over Flo emission spectra (**D**).

To analyze the role of the residual ferrocyanide species in the supernatant over the emission spectra, a fluorescence experiment centered on the ferrocyanide concentration was conducted. We prepared and added different amounts (1 mM to 4 mM) of ferrocyanide solution to a constant amount of Flo (0.2 mM) to analyze the influence of the solution over the Flo emission intensity. Ferrocyanide acted as a weak enhancer (Figure 9D). These results indicate that the As(III) was supposed to undergo oxidation into arsenate in the presence of PBN. The iron species in the PBN undergo reduction into Fe^{+2} throughout the As(III) removal process. On the addition of active ferric species to the supernatant, an immediate reaction leads to the formation of PBN after the interaction with residual ferrous species. The collected PBN@SiO_2 was characterized with XPS to observe the significance of arsenic treatment over the PBN@SiO_2 phase (as discussed in a subsequent section). Moreover, the resultant eluent was collected into separate vials and underwent HPLC analysis for the detection of arsenic species.

3.5. HPLC Results on PBN@SiO_2 Treated Arsenic(III)

All the separated species were noted in the ion-chromatogram at their respective retention time such as arsenobetaine (AsB) at 2.17/2.42/2.55 min, dimethylarsinic acid (DMA) at 3.57 min, As(III) at 3.8/3.9 min, and As(V) at 7.7 min. The chromatogram shown in Figure 10A–D was obtained as the result of HPLC separation of the arsenic species after treatment with PBN@SiO_2 at different pH values (2.2–8.5). HPLC analysis illustrates that the removal efficiency of As(III) ((Figure 10A) by PBN@SiO_2 increased from 33.52% (Figure 10B) to 59.90% (Figure 10C) with a pH increase from 2 to 6.5; this improved to 95.13% (Figure 10D) under a mild alkaline condition (pH-8.5). The ion chromatogram results also showed an insignificant peak at a retention time of 7.35 min ((Area% = 1.4) at pH = 6.5 and (Area% = 9.09) at pH = 8.5), which was associated with leaching of As(V) in an aqueous solution during the oxidation–adsorption process. All of the arsenic

species (As(III), DMA, AsB) identified at various retention times along with their relative concentration in a HPLC environment are shown in Table 2.

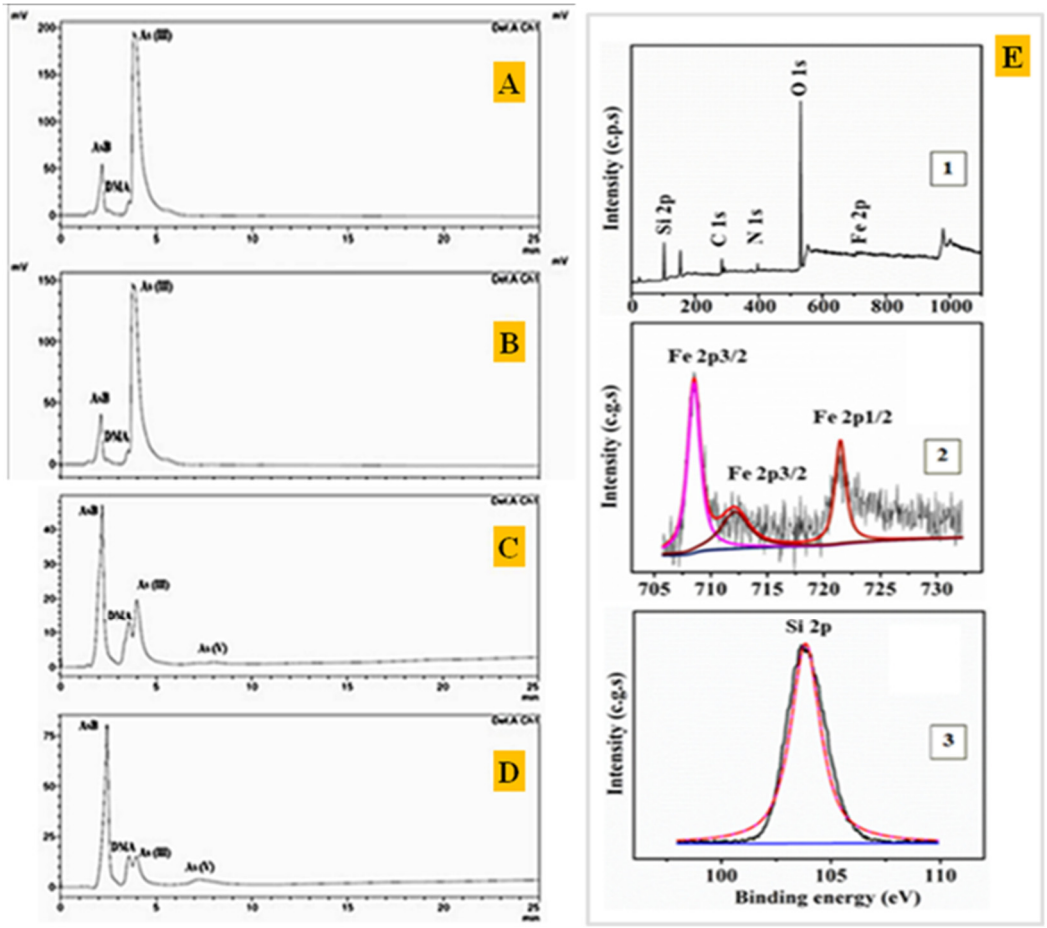
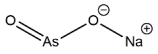
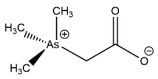
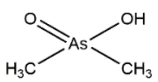


Figure 10. Ion chromatogram obtained during HPLC speciation of species present in the sample. (**A**) Standard As(III) (5 ppm) solution at pH = 6.5). (**B**) Standard As(III) sample (5 ppm) after PBN@SiO_2 treatment in acidic medium (pH = 2). (**C**) As(III) standard solution (5 ppm) after PBN@SiO_2 treatment in neutral medium (pH = 6.5). (**D**) As(III) standard sample (5 ppm) after PBN@SiO_2 treatment in alkaline medium (pH = 8.5). (**E**) XPS analysis of PBN@SiO_2. (**1**) A complete survey scan with all recognized species. (**2**) Fe^{2+} and Fe^{3+} species XPS peak in PBN@SiO_2. (**3**) Identified Si(IV) chemical states in SiO_2.

Table 2. All arsenic species (As(III), DMA, AsB) identified at different retention times along with their relative concentration during HPLC.

Species	Description	Molecular Formula	Height (%)	Area (%)	System pH	Retention Time	Figure
As^{III}	Sodium arsenite ($NaAsO_2$)		47.1	57.03	2.2	3.86 min	Figure 10B
			23.86	30.65	6.8	3.97 min	Figure 10C
			6.91	5.23	8.5	3.95 min	Figure 10D
AsB	Arsenobetaine (AsB)		45.56	34.39	2.2	2.55 min	Figure 10B
			58.29	49.74	6.8	2.17 min	Figure 10C
			70.02	56.95	8.5	2.42 min	Figure 10D
DMA	Dimethylarsinic acid (DMA)		6.85	4.21	2.2	3.58 min	Figure 10B
			15.81	16.21	6.8	3.57 min	Figure 10C
			13.45	11.79	8.5	3.57 min	Figure 10D

AsB, which frequently existed in the zwitterionic form due to the interaction between the positively charged arsenic and the negatively charged carboxylic group, starts to migrate immediately after interacting with the hydrophobic C18 Shim-pack column. However, As(III) is a neutral species (pKa = 9.2) up to a pH of 8, which eluents slowly with the solvent front. Consequently, negatively charged DMA and As(V) species feasibly eluent by a variety of interactions (e.g., H bonding and ion-exchange) along with hydrophobic effects. The obtained result was acquired after a total run time of 25 min and repeated twice to minimize the experimental error.

3.6. XPS Analysis of PBN@SiO_2

XPS survey scans indicated the presence of Si, O, Fe, and C in blank PBN@SiO_2 and As, Si, O, Fe, and C in As(III)-PBN@SiO_2. The peaks were assigned as follows: Fe $2p_{3/2}$—708 eV; Fe $2p_{3/2}$—713 eV; Fe $2p_{1/2}$—722 eV; As(III) 3d—44.2 eV and As(IV) 3d—47 eV, respectively. The peak position of the Si 2p spectrum corresponds to a binding energy of 103.63 eV and shows the characteristics of Si(IV) in a SiO_2-type compound [29].

3.6.1. Fe(II) and Fe(III) Identification in PBN@SiO_2

After peak fitting, the spectrum can be de-convolved into three peaks. Figure 10E shows the XPS peaks centered on binding energies of 721.27 and 708.34 eV for Fe $2p_{1/2}$ and Fe $2p_{3/2}$, respectively; these features are characteristic of the Fe^{+2} moiety in Prussian blue. In addition, a spectrum shows a peak at a binding energy of 712.12 eV, which corresponds to Fe^{+3} species. The position of these peaks is in good agreement with the results in the literature for the characteristic Fe^{+3} and Fe^{+2} components of Prussian blue compounds [30].

3.6.2. As(III)-PBN@SiO_2 and As(V)-PBN@SiO_2

The cation As(III) and the oxidized species As(V) detected on the PBN@SiO_2 substrate with XPS after a decontamination process are shown in Figure 11. The binding energy values (in eV) for O (1s), Si (2p), Fe (2p), and N (1s) in PBN@SiO_2 and As-PBN@SiO_2 are listed in Table 3. The XPS survey scan as shown in Figure 11D shows peaks at a binding energy of 49.03 eV, which are associated with the presence of As(V) and indicate the successful sorption of As(V) by PBN@SiO_2 [31]. The other peak located at 43.23 eV is associated with the adsorption of As(III) over SiO_2 prior to the oxidation process [32]. However, the peak positions observed for the Fe^{+3} and Fe^{+2} core level (2p) spectra of PBN@SiO_2 are shifted slightly to a lower binding energy relative to the unreacted and unabsorbed PBN@SiO_2 species. This shift in the peaks for Fe^{2+} $2p_{3/2}$ (binding energy of 708.19 eV) and Fe^{2+} $2p_{1/2}$ (binding energy of 721.42 eV) may be attributed to arsenic adsorption [33]. The shift in the peak position (with a reduction in intensity) of Fe^{+3} $2p_{3/2}$ (binding energy of 712.86 eV) relative to pure PBN@SiO_2 suggests the reduction of the material during arsenic oxidation [34]. The position of the characteristic peak of Fe^{+2} (binding energy of 55.04 eV, 3p) remained unchanged throughout the As(III) oxidation and adsorption process [31]. A peak emerged at a binding energy of 398.99 eV, which was attributed to the presence of nitrogen in the environment. Alterations in the peak position of PBN@SiO_2 relative to that of As-PBN@SiO_2 were associated with chemical adsorption by PBN@SiO_2 of arsenic species.

Table 3. XPS data of PBN@SiO_2 and Arsenic-PBN@SiO_2.

Sample	Si(2p)	O	Fe^{+3}	Fe^{+2}	Fe^{+2}	N	As(III)	As(V)
		1s	$2p_{3/2}$	$2p_{1/2}$	$2p_{3/2}$	1s	3d	3d
PBN@SiO_2	103.63	532.62	712.12	721.27	708.34	397.07	-	-
As-PBN@SiO_2	103.49	531.99	712.86	721.42	708.19	397.05 and 398.99	43.23	49.03

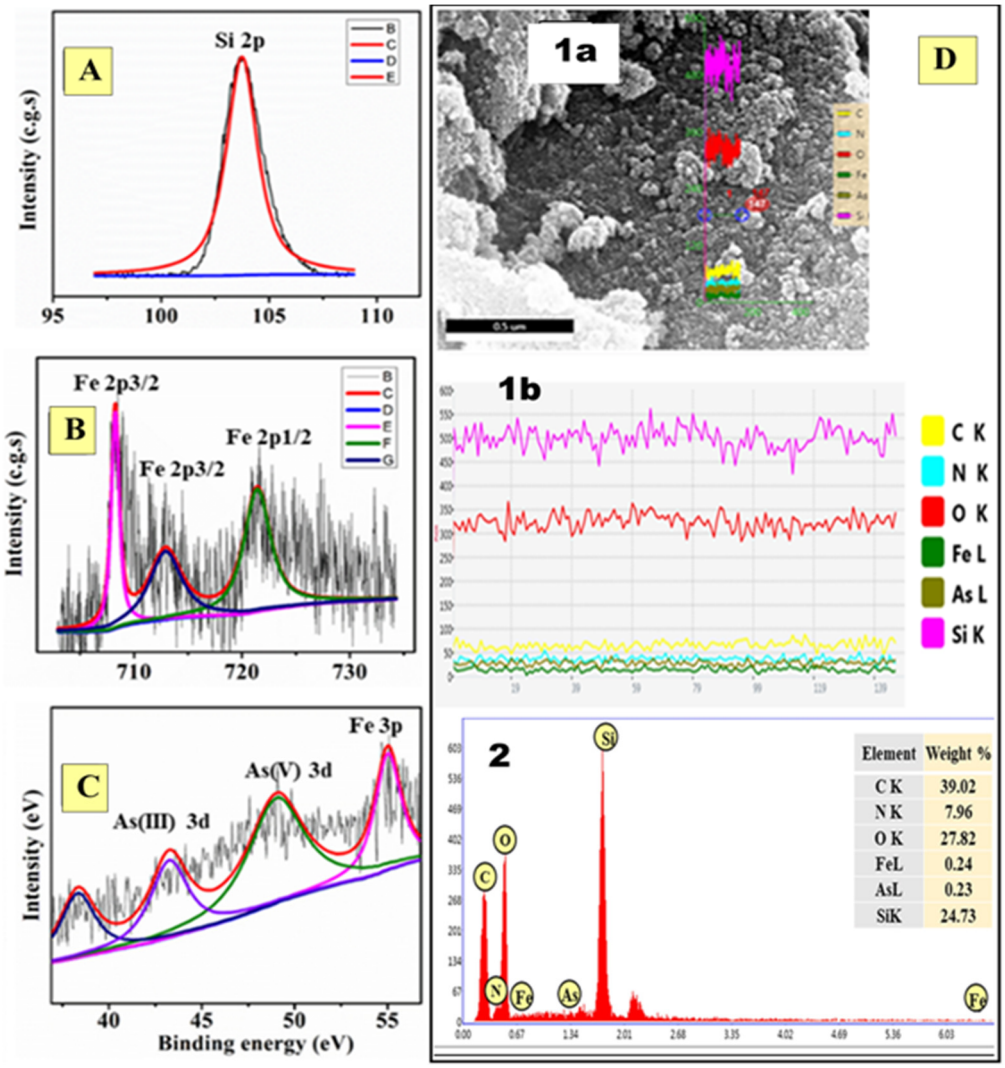


Figure 11. X-ray photoelectron spectrum of As-PBN@SiO_2 after arsenic exposure. (**A**) Identified Si(IV) chemical states in SiO_2. (**B**) Fe^{2+} and Fe^{3+} species XPS peak in PBN@SiO_2. (**C**) Arsenic species (As(V) and As(III)) at PBN@SiO_2. (**D**) (**1a**,**1b**) EDX line scan measurement comprised of an inner SiO_2 and an outer ferric hexacyanoferrate with As(III) enrichment over the PBN@SiO_2 surface. (**2**) EDX analysis shows all of the anticipated elements.

3.7. Effect of pH on Arsenic Removal

The results in Figure 10 illustrate the effects of pH on the removal of As(III) using PBN@SiO_2. As can be observed, As(III) removal was dependent on pH; the greatest removal efficiency occurred under moderate pH (pH = 6–9) and was found to diminish at highly acidic pH (pH < 3). As reported earlier, surfaces of silica beads were positively charged in highly acidic conditions and acquired a negative charge in the pH range of 3–10 [35]. Subsequently, moderate pH was found to be favorable for a sorbent surface since decreased protonation is supposed to enlarge the attraction force between the negatively charged PBN@SiO_2 surface and the positively charged As(III) cationic species. This result is similar to earlier findings by Gupta et al. who reported a significant increase in As(III) adsorption onto iron oxide-coated quartz sand with an increase in pH from 4.5 to 7.5 [36]. At a highly acidic pH (<3), repulsion occurred between the positively charged adsorbent sites and the adsorbate species (As^{+3}), which prevented the adsorption and arsenic oxidation processes. No substantial rise in As(III) removal efficiency was observed with an elevation in pH.

3.8. Analysis of PBN@SiO_2 Surface through SEM-EDX after As(III) Remediation

After the As(III) removal process, the PBN@SiO_2 surface was analyzed using SEM. The result showed the change in morphology of PBN (cubic to spherical) after arsenic interaction (Figure 11E). The EDX results suggest that the material is comprised of an inner SiO_2 chemistry and an outer ferric hexacyanoferrate ($Fe^{+3}[Fe^{+2}(CN)_6]$) chemistry, with some As(III) enrichment over the PBN@SiO_2 surface. The presence of the anticipated elements was confirmed through EDX analysis.

3.9. Recyclability and Proposed Mechanism

It has been well established that Prussian blue is comprised of Fe metal in Fe^{+2} (low spin) and Fe^{+3} (high spin) states, which are linked via CN bridges. Prussian blue can undergo reduction to what is known as Prussian white (Fe^{II}–C≡N–Fe^{II}) or oxidation to what is known as Prussian yellow (Fe^{III}–C≡N–Fe^{III}) [37,38]. Reduction of Prussian blue to Prussian white on the surface of silica gel was found to facilitate the As(III) oxidation to As(V) and their subsequent removal. Conversion of Fe^{3+} to Fe^{+2} was shown during the decontamination in PBN and validate the altered chemical environment due to arsenic interactions. The addition of ferric chloride to the white-blue colored arsenite-treated PBN@SiO_2 residue instantly generated a blue color; this phenomenon is attributed to the conversion of hexacyanoferrate $\left[Fe^{II}(CN)_6\right]$ species of $K_2[Fe^{II}Fe^{II}(CN)_6]$ into Prussian blue $\left(K[Fe^{III}Fe^{II}(CN)_6\right])$ through the interaction with ferric species (ferric chloride). The reaction during Prussian blue synthesis has been shown as:

$$4K_2[Fe^{II}Fe^{II}(CN)_6] + 4FeCl_34\left(K[Fe^{III}Fe^{II}(CN)_6\right]) + 4KCl$$

The variation of surface charge of SiO_2 with a change in pH was found to be the fundamental framework for PBN activity over the course of arsenic removal.

3.10. Mechanism of PBN Based Fluorescence Sensing of As(III)

The findings as shown in Figures 4–6 revealed an analyte-dependent intervalence transition in iron hexacyanoferrate $[Fe^{III}{}_4[Fe^{II}(CN)_6]_3]$ between Fe^{2+} and Fe^{3+} as shown below:

$$Fe^{2+} + Fe^{3+} + \text{light energy} \rightarrow Fe^{3+} + Fe^{2+}$$

The intervalence transition may be evaluated based on changes to the absorption spectrum. The fluorescein–PBN interaction is associated with fluorescence resonance energy transfer as recently described [39,40]; this material is capable of quenching the emitted fluorescence of fluorescein. When PBN undergo interaction with As(III), there is a conversion of PBN into Prussian white nanoparticles, followed by a conversion of As(III) to As(V); thus, the quenching ability is lost. The Prussian white nanoparticles can further be converted into PBN after treating the same with acid as discussed above. This scheme provides an effective and inexpensive method for PBN-mediated removal of As(III) udermvisible light.

3.11. Characterization of Recyclable PBN@SiO_2

After arsenic elimination, the recycled PBN@SiO_2 was investigated with XRD, SEM, and FTIR to understand the effect of the recycling process on PBN@SiO_2 morphology, size, and crystallinity. An SEM image of the recycled PBN@SiO_2 is shown in Figure 12. More spherical-shaped than cube-shaped particles were observed; the aggregation of PBN with no precise shape was also observed. XRD analysis demonstrated a shifting inward of the peak position (θ) as compared with the unused PBN@SiO_2. The presence of anticipated elements was identified via EDX analysis. In addition, characteristic CN stretching in PBN was noted; this feature was noted at a considerably lower wavenumber (2054 cm^{-1}), which is attributed to particle aggregation [39]. The PBN characteristics before and after the recycling process as obtained from XRD, SEM, and FTIR analysis are listed in Table 4.

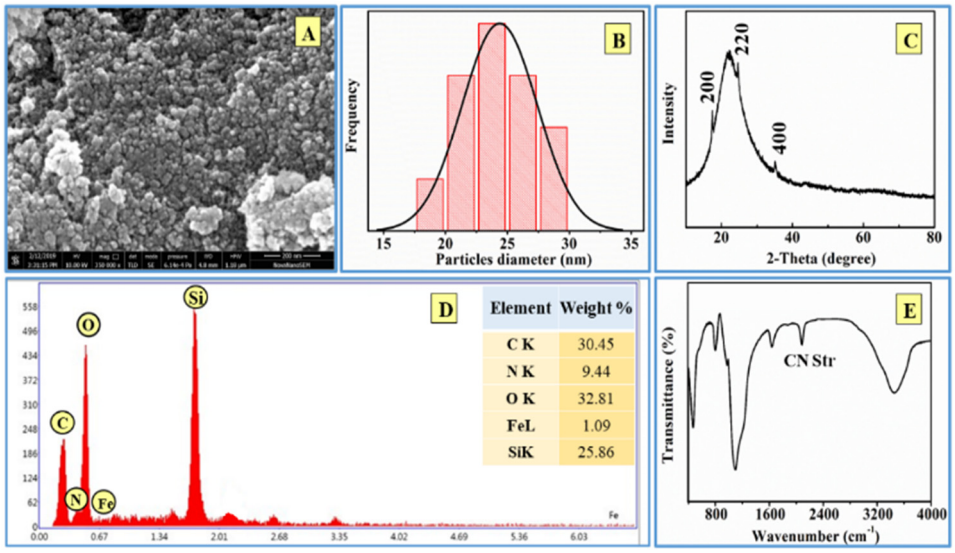


Figure 12. Analysis of recycled PBN@SiO_2 following acid treatment. (**A**) An alteration in nanoparticle morphology as identified through SEM imaging, (**B**) A decrease in particle size (26 nm) as calculated from the displayed histogram, (**C**) Minor shift in peak position with similar planes as identified through XRD analysis, (**D**) Spectrum with the entire anticipated element as detected by EDX, (**E**) Shift in CN stretching peak observed using FTIR.

Table 4. Table with HRSEM, XRD and FTIR data displaying the variations between unused and recycled PBN@SiO_2.

Analysis	Property	Unused PBN@SiO_2	Recycled PBN@SiO_2
HRSEM	Shape	Nanocubic (82%) and Spherical (18%)	Nanocubic (19%) and Spherical (81%)
HRSEM	Size	70–20 nm	17–26 nm
XRD	2-Theta (Planes)	17.6 (200), 24.3 (220), 37.83 (400)	17.4 (200), 24.6 (220), 35.12 (400)
FTIR	CN Str.	2096 cm^{-1}	2054 cm^{-1}

4. Conclusions

PBN are a light-sensitive material that is processed through functional alkoxysilane- and cyclohexanone-mediated conversion of a single precursor, potassium hexacyanoferrate. The synthetic incorporation of PBN within mesoporous silica (PBN@SiO_2) was also studied; the morphology of these particles was characterized using TEM, SEM, XRD, and XPS. The as-made PBN were studied as a fluorescent quencher. The quenching ability of the materials is found to be a function of arsenic(III) concentration; this result suggested a novel application of PBN for fluorescence sensing of arsenic. In addition, XPS studies confirmed that arsenic is adsorbed on PBN@SiO_2 as arsenite (As(III)) and arsenate (As(V)) irrespective of the initial oxidation state of the material; this result indicated a novel application of PBN for the removal of arsenic(III) from a given sample.

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Informed Consent Statement: Informed consent was obtained from all subjects involved in the study.

Data Availability Statement: Data supporting reported results can be found in the laboratory of Prof. Prem C Pandey of IIT(BHU). https://iitbhu.ac.in/dept/apc/people/faculty.

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Flexible Carbon Nanotubes Confined Yolk-Shelled Silicon-Based Anode with Superior Conductivity for Lithium Storage

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Abstract: The further deployment of silicon-based anode materials is hindered by their poor rate and cycling abilities due to the inferior electrical conductivity and large volumetric changes. Herein, we report a silicon/carbon nanotube (Si/CNT) composite made of an externally grown flexible carbon nanotube (CNT) network to confine inner multiple Silicon (Si) nanoparticles (Si NPs). The in situ generated outer CNTs networks, not only accommodate the large volume changes of inside Si NPs but also to provide fast electronic/ionic diffusion pathways, resulting in a significantly improved cycling stability and rate performance. This Si/CNT composite demonstrated outstanding cycling performance, with 912.8 mAh g^{-1} maintained after 100 cycles at 100 mA g^{-1}, and excellent rate ability of 650 mAh g^{-1} at 1 A g^{-1} after 1000 cycles. Furthermore, the facial and scalable preparation method created in this work will make this new Si-based anode material promising for practical application in the next generation Li-ion batteries.

Keywords: silicon; yolk−shell structure; anode; lithium-ion batteries

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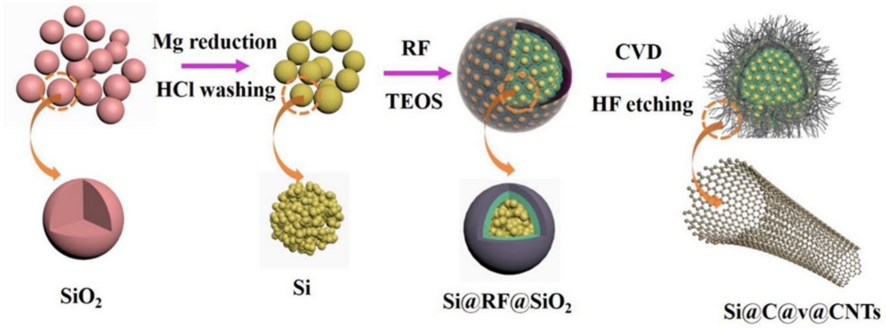
1. Introduction

Silicon (Si) is the most promising anode candidate in lithium-ion batteries (LIBs) due to its high theoretical specific capacity (~4200 mAh g^{-1}) and cut-price [1–4]. However, the large volume changes (over 400% expansion after full lithiation) induced poor structural stability and continuous breaking and regenerating of the solid-electrolyte interphase (SEI) cause's short working life for Si-based anodes [5–7]. Moreover, the low electrical conductivity of the Si limits its rate performance under high current densities [8–10]. Up till now, introducing a reserved void space and conductive framework into silicon-based materials has been regarded as the most effective strategy to fundamentally improve the electrochemical behavior of Si-based anodes [11–13]. The introduced reserved space can buffer the huge changes in volume of Si during cycling, leading to the enhanced structural integrity and cycling stability [14–16]. Additionally, the conductive framework within the composites increases the overall conductivity of the electrodes, resulting in the high-rate capacities under high current densities [17–20].

Among various Si-based composites, the yolk-shelled Si/carbon (Si/C) composites are the most promising candidate because of their distinctive advantages over the existing Si-based composites in terms of cycling stability and rate behavior [21–24]. Many previous reports confirmed the effective structure [25–27]. For these yolk-shelled Si/C composites,

the Si-yolk was encapsulated within a hollow C-shell with reserved space between the Si-yolk and the C-shell. Therefore, the volume changes of inner Si-yolk can be accommodated by the void space and confined within the hollow C-shell, leading to increased structural stability and limited formation of the outer generated SEI film [25–27]. However, the introduced void space limits the conductive contact between Si-yolk and C-shell and further decreases the tap density of the composite [28–30]. Carbon nanotubes (CNTs) with excellent mechanical properties and high electrical conductivity are regarded as another hopeful carbon matrix to increase the overall behavior of Si-based materials [31–36]. Currently, most of the reported Si/CNT anodes are synthesized by directly using expensive commercialized CNTs to mix with Si nanoparticles (Si NPs), causing increased production cost [37–39]. Moreover, it is difficult to achieve the uniform distribution between CNTs and Si NPs due to their large surface area [40,41]. Currently, new Si/CNT anodes composites have been developed via a chemical vapor deposition (CVD) process, which provides distinguished structural stability and electrochemical performance, enhances the overall conductivity of the electrode, and increases the safety of the battery [32,42]. Moreover, it is remaining a great challenge to prepare promising Si/CNT composites with low-cost methods while preserving the unique volume change containment functionality of Si/C yolk–shell structures.

Herein, we overcome these obstacles by developing new Si/CNTs anodes (Scheme 1). Si NPs were successively double-coated with rigid carbon and silica layers (Si@C@SiO_2) to better encapsulate the incorporated multiple Si NPs to realize good safety levels. Furthermore, the SiO_2 coating layer on the outer surface of Si@C@SiO_2 further provided active position for in situ CNTs grown via a CVD method, resulting in a new Si/CNT composite. For this new Si/CNT, the flexible CNT networks were grown on the surface of Si@C@SiO_2 particles. Therefore, the aggregation for both the CNTs and Si NPs can be significantly suppressed due to the external in-situ grown CNTs networks. Additionally, compared with the traditional yolk-shell structure, the CNT networks and the carbon coating shell effectively increase the conductive contact, not only between the inner Si-yolks and CNT networks but also among different Si/CNT microparticles, leading to increased electronic conductivity and rate capacities. Moreover, the overall structural stability and integrity of this new Si/CNT can also be enhanced by flexible porous CNT networks and rigid carbon coating [42].



Scheme 1. Schematic illustration of the preparation of the Si@C@v@CNTs.

2. Materials and Methods

2.1. Synthesis of Si NPs

All reagents in this paper were purchased from Sinopharm Co (Shanghai, China). The nano-sized silica (SiO_2) spheres were firstly synthesized by the well-established Stöber method. In the following magnesiothermic reduction (MR) process, Mg powders (99%) and the obtained SiO_2 spheres were uniformly mixed and placed in one side of a crucible boat. After that, a certain amount of NaCl (AR) (SiO_2:NaCl = 1:10) was placed in the other side of the crucible boat. The crucible boat was then placed in the center of the tube furnace (OTF-1200X, Shenzhen kejing-zhida Co, Shenzhen, China) and increased to 700 °C

under an Ar/H_2 (95:5 vol. %) flow and retained for 6 h. After cooling down to normal condition, the obtained sample was dispersed in 1 M HCl for several hours to remove NaCl and byproduct MgO. The final porous Si NPs powders were obtained after a wash and vacuum dry.

2.2. Synthesis of Si@RF@SiO_2

The above prepared Si NPs were modified with 3-aminopro-pyltrimethoxysilane (APTES) (AR) to positively charge the surfaces. In total, 0.4 g Si NPs were uniformly dispersed in 300 mL ethanol (AR), containing 4 mL of APTES, and stirred for 5 h to obtain APTES-Si NPs. The above APTES-Si NPs was re-dispersed in an alkaline mixture of 150 mL deionized water and 30 mL ethanol, containing 1 mL of aqueous ammonia (AR) under magnetic stirring for 30 min. After that, 0.6 g resorcinol (AR) and 0.8 mL formaldehyde (AR) were separately added to the reaction system and continued stirring for 10 h to form a homogeneous phenolic resin (RF) coating layer under room temperature. The Si@RF powders were obtained via centrifugation treatment of the reaction solution. For the SiO_2-coated Si@RF composite (named Si@RF@SiO_2), 400 mg Si@RF was mixed with 1.5 mL tetraethyl orthosilicate (TEOS) (AR) hydrolysis under alkaline condition to form SiO_2 coating layer on the outer surface of Si@RF.

2.3. Synthesis of Si@C@v@CNTs

Carbon nanotubes were grown in situ via a CVD method using Iron(III) nitrate nonahydrate (AR) as the catalyst (Fe) and acetylene (5%) as carbon precursors at 900 °C for 2 h under Ar/H_2 in a tube furnace. The catalyst was loaded on the precursor microspheres of Si@RF@SiO_2 prior to the deposition procedure to ensure that the CNTs could be grown in situ on the active positions during the CVD process. Finally, the SiO_2 coating layer was removed with dilute hydrofluoric acid (AR) solution and followed by centrifugation treatment and ethanol washing. After removing the SiO_2 sacrificial coating layers, the final composite was named Si@C@v@CNTs ("v" stands for "void"). For comparison purposes, the Si@C@v@C ("v" stands for "void") without in-situ grown CNTs was also synthesized via the same CVD method but in the absence of a $Fe(NO_3)_3{\cdot}9H_2O$ catalyst, and the Si@v@CNT without an inner carbon layer was also synthesized via the same CVD method in the absence of the RF-layer.

2.4. Characterizations

The XRD patterns of samples were obtained via a DX-2007 X-ray diffraction (XRD) experiment apparatus (λ = 1.5418 Å) (Dandong Haoyuan Instrument Co, Dandong, China) to confirm the phases and crystallinity. The Si content of composites was characterized by a thermogravimetric analyzer (TGA4000) (NSK LTD, Tokyo, Japan) at a heating rate of 10 °C min^{-1} in air atmosphere. The nitrogen adsorption/desorption isotherm curves were obtained via a Micromeritics ASAP-2020M nitrogen adsorption/desorption apparatus (Best Instrument Technology Co, Beijing, China) to confirm the porosity character. The micro-structures and morphologies of the materials were collected via a JSM-6700F scanning electron microscope (SEM) (JEOL, Tokyo, Japan) with an IE300X energy-dispersive X-ray spectrometer and a JEM-2100F transmission electron microscope (TEM) (JEOL, Tokyo, Japan). X-ray photoelectron spectroscopy (XPS) curves were obtained by applying an electron spectrometer (ESCALab250) (Thermo Fay, Boston, MA, USA) to analyze the surface of composites. Raman spectra was collected with a Raman spectrometer (JobinYvon HR800) (Renishaw, London, UK).

2.5. Electrochemical Measurements

The CR2016 coin-type cells were assembled in the glove box under inert atmosphere conditions without water and oxygen to test the electrode performance by using polypropylene films as separators (the thickness of the separator was 25 μm) to separate the working and counter electrodes (lithium wafer) in an electrolyte. The electrolyte was the 1 M $LiPF_6$

dissolved in the solvent of ethylene carbonate and dimethyl carbonate (the amount of the electrolyte used in assembling the coin-type cell was 70 μL). The working electrode was made by coating the slurry of the above active materials containing a proportional conductive carbon black and polyvinylidene fluoride (PVDF) binder on the copper foil (the mass loading of the electrode was about 1.2 mg cm^{-2}), which was then dried under a 120 °C vacuum oven for 14 h (the thickness of the active electrode layer was about 20 μm). Finally, the copper foil was cut into wafers with a uniform size of 1 cm. The galvanostatic cycling measurements were conducted by a CT 2001A battery tester at determinate voltage windows. Cyclic voltammogram (CV) tests were performed by using an electrochemical workstation within a fixed voltage range and scan rate.

3. Results and Discussions

Figure S1 shows the XRD patterns of reduced Si NPs, Si@RF, and Si@RF@SiO_2. Three sharp diffraction peaks, which are located at 2θ values of 28.4, 47.2, and 56.1°, were attributed to the planes of (111), (220), and (311) for the crystal Si phase, respectively (JCPDS NO. 27-1402), indicating that the amorphous SiO_2 synthesized by the well-established Stöber method were fully reduced to crystalline Si in the MR process [43]. Another broad peak at ∼25° corresponded with the amorphous carbon and silica coming from the double coat with RF and silica layers. As shown in Figure 1a, for Si@C@v@CNTs and Si@v@CNTs, after the CVD process, CNT grown in situ across Si-CNPs and the diffraction peak at ∼25° was observed, corresponding to the (002) plane of the crystalline carbon [40]. Figure 1b displays the Raman spectra of Si@C@v@CNTs, Si@v@CNTs, and Si@C@v@C. The sharp peak at about 500 cm^{-1} could be appointed to the Si peaks. Additionally, the weak peaks at about 1345 cm^{-1} (D-band) and 1595 cm^{-1} (G-band) could be associated with the vibration modes of sp^3-bonded carbon atoms in amorphous carbon and sp^2-bonded carbon atoms in typical graphite, respectively [44]. As calculated, the I_D/I_G was 0.98, 0.96, 0.95 for Si@C@v@C, Si@v@CNTs, and Si@C@v@CNTs, respectively. Si@C@v@CNTs had a relatively higher graphitization degree due to the microcrystalline structure of CNTs. Thermogravimetric analysis (TGA) was tested to confirm the proportion of carbon and silicon for the samples (Figure 1c). The weight losses occurred from 500 to 800 °C were ascribed to the carbon combustion and calculated to be 54.3%, 70.6%, and 85.9% for Si@C@v@C, Si@v@CNTs, and Si@C@v@CNTs, respectively. As the temperature continued to rise, Si NPs were further oxidized, leading to a weight increase in the TGA curves. The Si content in the three samples were 45.7%, 29.4%, and 14.1% for Si@C@v@C, Si@v@CNTs, and Si@C@v@CNTs, respectively. Compared with the other two samples, high C and CNT content in Si@C@v@CNTs provided more electric contact between particles, thus enhanced overall electronic conductivity and superior performance could be expected. The elemental compositions and valence states in the composites were determined by X-ray photoelectron spectroscopy (XPS) spectra. Figure 1d reveals the whole spectrum of Si@C@v@CNTs, confirming the coexistence of Si, C, and O. The high-resolution spectrum of Si 2p is shown in Figure 1e. Three peaks of Si-Si (98.6 eV), Si-C (101.6 eV), and Si-O (102.98 eV) originated from monatomic Si, residual silica, or slight oxidation of the Si NPs [45]. In addition, the high-resolution C 1s and O 1s in Figure S2 shows that the peak at 283.75 eV was related to the graphite-like sp^2 hybridized carbon and another peak at 283.3 eV was assigned to C-O. The O 1s peak at 537 eV may be attributed to adsorbed oxygen and the residual silica layer [46].

The Brunauer−Emmett−Teller (BET) specific surface area and pore volume for the samples are illustrated in Table S1. Compared with Si@C@v@C, the Si@C@v@CNTs had a relatively higher BET specific surface area of 106.98 m^2 g^{-1}, with a pore volume of 0.3212 cm^3 g^{-1}. We believe that the higher surface area was mainly due to the existence of reserved void space and in-situ grown CNT networks. The nitrogen adsorption–desorption isotherm curve of the samples is displayed in Figure 1f. All the curves had a distinct hysteresis loop, suggesting the existence of a mesoporous structure [47]. The pore size distribution curve (Figure S3) shows a diverse pore structure between 2 and 10 nm, which

incorporate a series of micro- and mesopores derived from CNT networks [48]. Furthermore, these multiple pore structures not only afford fast and shortened electronic/ionic diffusion pathways but also absorb the huge expansion in volume inside Si NPs during cycling, resulting in a significantly enhanced overall structural integrity and electrochemical performance.

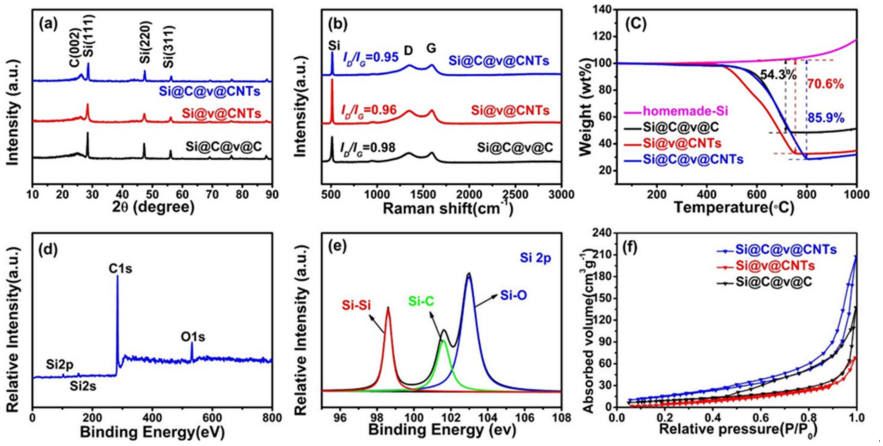


Figure 1. XRD patterns (**a**), Raman spectra (**b**), and thermogravimetric analysis (TGA) curves (**c**) of Si@C@v@C, Si@v@CNTs, and Si@C@v@CNTs; X-ray photoelectron spectroscopy (XPS) of Si@C@v@CNTs (**d**), High-resolution XPS spectrum of Si 2p (**e**), and N_2 adsorption-desorption isotherms curves of Si@C@v@C, Si@v@CNTs, and Si@C@v@CNTs (**f**).

Figure 2 shows the scanning electron microscopy (SEM) images of the structural evolution of Si@C@v@CNTs at different synthesis stages. The SEM image of SiO_2 spheres firstly synthesized by the well-established Stöber method is shown in Figure 2a. The pristine SiO_2 spheres present a monodispersed spherical shape with a uniform diameter of approximately 300 nm. After the Mg-reduction process, porous Si NPs with well-preserved monodispersed spherical morphology were successfully prepared (Figure 2b). Figure 2c,d show the SEM images of Si@RF and Si@RF@SiO_2. The diameters of as-prepared Si@RF and Si@RF@SiO_2 precursors were increased to 400 nm and 500 nm, respectively, indicating the successful coating of RF and SiO_2 layers on the Si cores, resulting in Si@C@SiO_2 particles. Figure 2e,f reveals a large amount of tangled CNTs with various diameters in the range of 50–100 nm externally grown in situ across the Si@C@SiO_2 particles. The multiple Si NPs were well supported by the in-situ generated flexible porous CNTs networks, contributing to better electric contact, not only between the inner Si-yolks but also among the Si-CNT microparticles. Figure 2g reveals the uniform elemental distribution of the Si, C, and Fe in Si@C@v@CNTs. It is clearly observed the Si-yolks were well coated by the outer C-shell and distributed across the flexible CNT networks. Figure S4 shows the SEM images of Si@C@v@C. The observed wrinkles over the entire surface confirm the full encapsulation of Si@C@SiO_2 by the carbon layer. The SEM images of Si@v@CNTs in Figure S5 reveal the similar tangled CNTs with Si@C@v@CNTs.

Figure 3a–c shows the transmission electron microscopy (TEM) images of homemade SiO_2 and reduced Si NPs. The high-resolution TEM image (HRTEM), taken from one of the Si NPs, reveals that the obtained Si NPs had high crystallinity [49,50]. The TEM images of Si@RF and Si@RF@SiO_2, as shown in Figure 3d–e, confirm that the Si NPs were well wrapped by the RF carbon-SiO_2 double coating layers. The TEM and HRTEM images of Si@C@v@CNTs presented in Figure 3f–i confirm CNTs grown in situ on the outer layer of the Si@RF NPs with a void between the two. The carbon layer derived from RF was about 5 nm and could accelerate electron transfer between Si NPs and CNTs, leading to enhanced structural stability. The void generated due to the etching of SiO_2 could effectively alleviate the expansion of the inner Si NPs. According to the TEM images of a single CNT shown in Figure S6, the outer diameter of this single CNT was approximately 35 nm and the tube

wall was 12 nm. The TEM image of Si@C@v@C in Figure S7 shows that the Si NPs were well wrapped with double carbon layers. The TEM images of Si@v@CNTs in Figure S8 confirms that existence of similar CNTs grown to Si@C@v@CNTs but without of a carbon layer on the Si NPs.

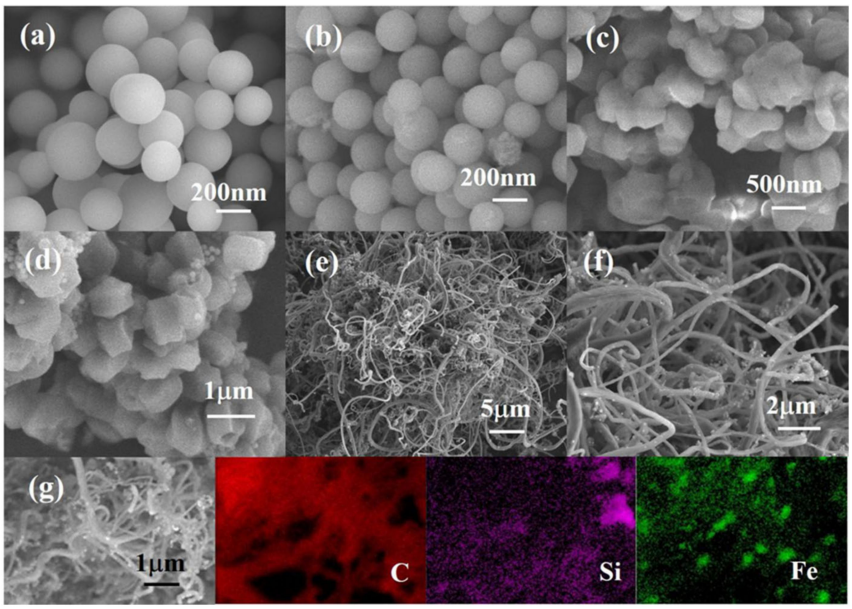


Figure 2. SEM images of SiO_2 nanoparticles (NPs), synthesized by the well-established Stöber method (**a**), reduced Si NPs in the magnesiothermic reduction (MR) process (**b**), SEM images of the in-process samples: Si@RF (**c**), Si@RF@SiO_2 (**d**), Si@C@v@CNTs (**e**,**f**). (**g**) the elemental mapping results of Si@C@v@CNTs.

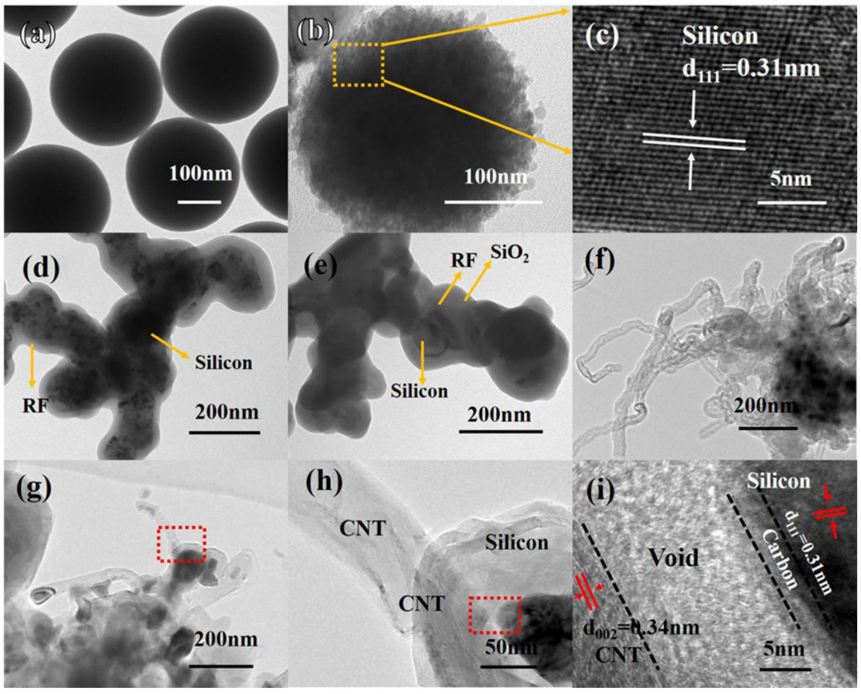


Figure 3. Transmission electron microscope (TEM) images of SiO_2 NPs synthesized by the well-established Stöber method (**a**), reduced Si NPs in the MR process (**b**), high resolution TEM (HRTEM) images of Si NPs (**c**), TEM images of Si@RF (**d**), Si@RF@SiO_2 (**e**), and Si@C@v@CNTs (**f**–**h**), and HRTEM images of Si@C@v@CNTs (**i**).

The cyclic voltammetry (CV) curve of Si@C@v@CNTs exhibited the typical electrochemical properties of Si-based anode materials (as shown in Figure 4a). In the first cathodic branch (lithiation), a distinct broad peak between 0.5 and 0.8 V was ascribed to the generated solid-electrolyte interphase (SEI) film. However, this peak disappeared after the first lithiation, suggesting the generation of the firm and stable films during the first cycle [51]. The lithiation peak at 0.18 V can be appointed to the lithiation process of Si. In the following anodic branch (delithiation), the peaks located at 0.34 and 0.5 V were ascribed to the dealloying process from Li_xSi to amorphous Si [52]. Figure 4b shows the initial charge–discharge profiles of the materials at 100 mA g^{-1}. The disappearance of the voltage plateaus between 0.5 and 0.8 V after the first cycle also confirms the generation of stable SEI films, which is in accordance with the CV results in Figure 4a [44]. The initial discharge and charge capacities were 2698.4 and 1684.2 mAh g^{-1} for Si@C@v@C, 2546.5 and 1760.6 mAh g^{-1} for Si@v@CNTs, and 2350.1 and 1787.0 mAh g^{-1} for Si@C@v@CNTs at 100 mA g^{-1}, corresponding to the initial coulombic efficiencies (ICE) of 62.41, 69.14, and 76.04%, respectively. Figure S9 shows the galvanostatic charge–discharge curves of Si@C@v@CNTs during the first five cycles at 100 mA g^{-1}. After the first cycle, the CE increased to 92.73% in the following cycling test and reached 96.04% after the fifth cycle. Most importantly, the voltage plateaus during the cycling test was well-maintained, suggesting improved electrochemical utilization of the active electrode materials. The cycling behavior in Figure 4c shows the charge capacities at 100 mA g^{-1} for Si@C@v@C.

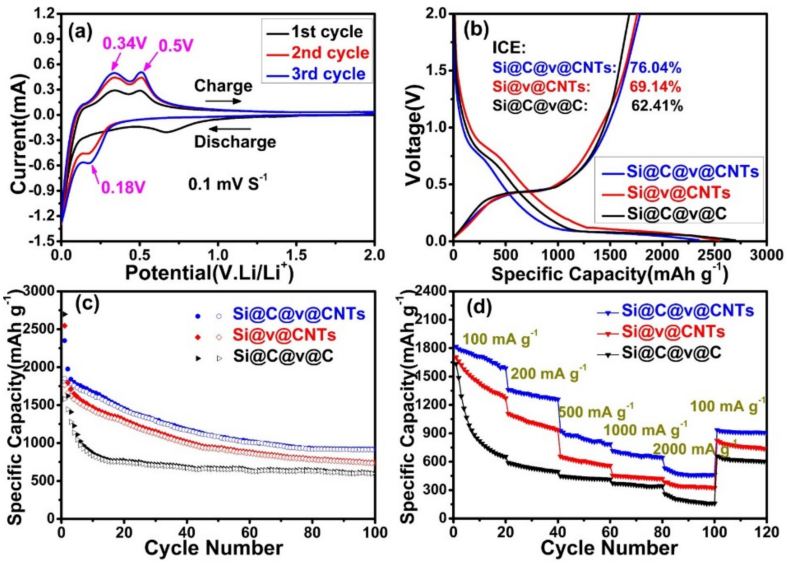


Figure 4. Electrochemical properties: cyclic voltammetry for the first three cycles of Si@C@v@CNTs at a scan rate of 0.1 mV s^{-1} between 0–2.0 V (**a**), the initial discharge–charge curves at 100 mA g^{-1} (**b**), cycling performances at 100 mA g^{-1} (**c**), the rate performances (**d**) of Si@C@v@C, Si@v@CNTs, and Si@C@v@CNTs.

Si@v@CNTs and Si@C@v@CNTs were 598.7, 736.1, and 912.8 mAh g^{-1} after 100 cycles, respectively, indicating that the Si@C@v@CNTs were endowed with the best cycling behavior. Therefore, the outer in-situ grown CNT networks can significantly improve the cycling behavior and structural integrity of the inside-coated Si NP anodes. Figure 4d shows the rate performances of Si@C@v@C, Si@v@CNTs, and Si@C@v@CNTs performed at a series of different current densities. As expected, Si@C@v@CNTs present the best rate ability, even at high current densities. Very high reversible capacity of 907.7 mAh g^{-1} was maintained when the current density was back to 100 mA g^{-1}, suggesting an excellent rate ability of Si@C@v@CNTs. Furthermore, a high reversible capacity of 650 mAh g^{-1} was retained for Si@C@v@CNTs at high 1 A g^{-1} after 1000 cycles (Figure 5a). Therefore, it can be concluded that the introduced void space and porous CNT networks can absorb the

huge volume expansion inside Si NPs, leading to enhanced overall structural stability and integrity [52–54]. In addition, the CNT networks and inner rigid carbon coating provided more sufficient conductive contact to fast electronic/ionic diffusion pathways, resulting in significantly improved cycling stability and rate performance [55–57]. Figure S10 shows the SEM images of Si@C@v@CNTs after 1000 cycles at 1 A g^{-1}. No cracking can be detected for Si@C@v@CNTs, and all the active materials were still well adhered to the current collector without exfoliation (Figure S10a,b). In addition, the morphology was well maintained in Si@C@v@CNTs after the long cycling test. (Figure S10c). Figure 5b shows the schematic illustration of lithiation and delithiation processes.

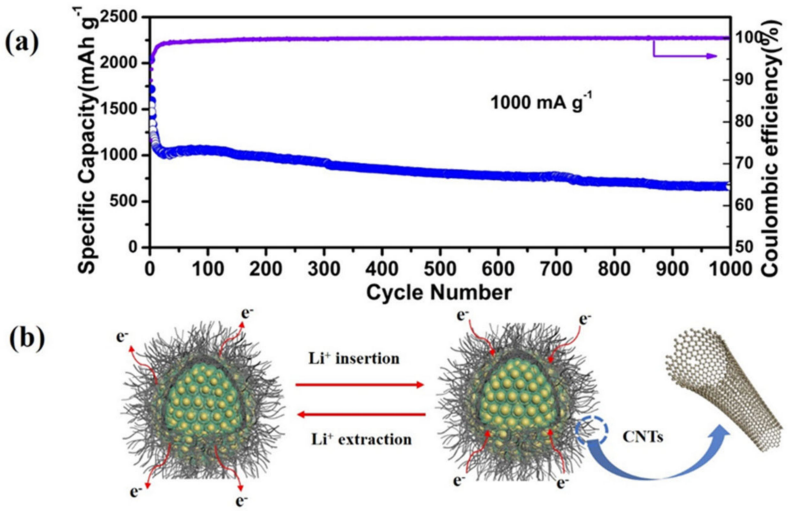


Figure 5. Cycle performance of Si@C@v@CNTs at a current density of 1000 mA g^{-1} (**a**) and a schematic illustration of lithiation and delithiation processes (**b**).

Moreover, we fabricated a full cell with our Si@C@v@CNTs as the anode and $LiNi_{0.6}Co_{0.2}Mn_{0.2}O_2$ (NCM622) as the cathode (Si@C@v@CNTs//NCM622). The voltage profiles of NCM622 are shown in Figure S11. The NCM622 cathode exhibited a stable reversible capacity of 160 mAh g^{-1} with a flat charging/discharging plateau at about 3.5 V. Referring to the voltage profiles of the Si@C@v@CNTs anode and the NCM622 cathode from half cells, the working potential range for the full cell was set between 2 and 4 V. The cycling performance of Si@C@v@CNTs//NCM622 is shown in Figure S12. The full cell displays a reversible capacity of 92 mAh g^{-1} at 100 mA g^{-1} after 100 cycles, indicating potential cycling stability for commercial viability.

4. Conclusions

In summary, we synthesized a yolk-shelled structured silicon/carbon nanotube composite for high performance lithium storage application. This novel Si-based anode was made of an external grown flexible CNT network to confine the inner multiple Si NPs. The in-situ generated outer CNT networks not only accommodated the huge changes in volume space inside Si nanoparticles but also provided fast electronic/ionic diffusion pathways, resulting in markedly improved cycling stability and rate ability. Furthermore, the facial and scalable preparation method created in this work could make this new Si-based anode material promising for practical application in next generation Li-ion batteries.

Supplementary Materials: The following are available online at https://www.mdpi.com/2079-4991/11/3/699/s1. Figure S1: XRD patterns of reduced Si NPs in the MR process, Si@RF, and Si@RF@SiO_2. Figure S2: XPS spectrum of C1s (a) and O1s (b) of Si@C@v@CNTs. Figure S3: The pore size distribution curve of Si@C@v@C, Si@v@CNTs, and Si@C@v@CNTs. Figure S4: SEM images of Si@C@v@C. Figure S5: SEM images of Si@v@CNTs. Figure S6: TEM images of a single CNT. Figure S7: TEM images of Si@C@v@C. Figure S8: TEM images of Si@v@CNTs. Figure S9: The first five discharge-charge curves of Si@C@v@CNTs at current density of 100 mA g^{-1}. Figure S10: Digital photograph (a), SEM image of Si@C@v@CNTs after the cycling test at 1.0 A g^{-1} (b,c). Figure S11: Charge/discharge profiles of NCM626 between 2.0–4.3 V. Figure S12: The electrochemical performance of the full cell using Si@C@v@CNTs as anode and $LiNi_{0.6}Co_{0.2}Mn_{0.2}O_2$ (NCM622) as cathode at the current density of 100 mA g^{-1}. Table S1: The Brunauer-Emmett-Teller (BET) surface area, pore volume and average pore size of the samples.

Author Contributions: Conceptualization, J.L. and Z.P.; methodology, N.H., and Z.P.; software, X.W.; validation, C.Z., J.Q., and G.L.; formal analysis, X.L.; investigation, N.H.; resources, X.Z.; data curation, N.H.; writing—original draft preparation, N.H.; writing—review and editing, N.H., X.Z., and L.Z.; supervision, X.Z.; project administration, X.Z. and Z.P. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The data presented in this study are available on request from the corresponding author.

Conflicts of Interest: The authors declare that they have no competing interests.

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