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Advanced Interconnect and Packaging

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Unlike transistors, the continuous downscaling of feature size in CMOS technology leads to a dramatic rise in interconnect resistivity and concomitant performance degradation. At nanoscale technology nodes, interconnect delay and reliability become the major bottlenecks faced by modern integrated circuits. To resolve these interconnect problems, various emerging technologies, including airgap, nanocarbon, optical, and through-silicon via (TSV), have been proposed and investigated. For example, by virtue of TSV technology, dies can be stacked to increase the integration density. More importantly, 3D integration and packaging also offer the most promising platform to implement "More-than-Moore" technologies, providing heterogeneous materials and technologies on a single chip. The "Advanced Interconnect and Packaging" Special Issue seeks to showcase research papers on new developments in advanced interconnect and packaging, i.e., on the design, modeling, fabrication, and reliability assessment of emerging interconnect and packaging technologies. Additionally, there are two interesting papers on carbon nanotube interconnects and interconnect reliability issues.



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