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A Proof-of-Concept Open-Source Platform for Neural Signal Modulation and Its Applications in IoT and Cyber-Physical Systems

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Abstract: This paper presents the design, implementation, and characterization of a digital IoT platform capable of generating brain rhythm frequencies using synchronous digital logic. Designed with the Google SkyWater 130 nm open-source process design kit (PDK), this platform emulates Alpha, Beta, and Gamma rhythms. As a proof of concept and the first of its kind, this device showcases its potential applications in both industrial and academic settings. The platform was integrated with an IoT device to optimize and accelerate research and development efforts in embedded systems. Its cost-effective and efficient performance opens opportunities for real-time neural signal processing and integrated healthcare. The presented digital platform serves as a valuable educational tool, enabling researchers to engage in hands-on learning and experimentation with IoT technologies and system-level hardware–software integration at the device level. By utilizing open-source tools, this research demonstrates a cost-effective approach, fostering innovation and bridging the gap between theoretical knowledge and practical application. Furthermore, the proposed system-level design can be interfaced with various serial devices, Wi-Fi modules, ARM processors, and mobile applications, illustrating its versatility and potential for future integration into broader IoT ecosystems. This approach underscores the value of open-source solutions in driving technological advancements and addressing skills shortages.

Keywords: IoT devices; cyber-physical systems; emerging technologies; open-source synthesis tools; applied artificial intelligence; IoT for healthcare; skill shortage in chip design; open-source chip design

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1. Introduction

1.1. Context

The integration of brain decoding technologies with IoT and CPS signifies a major advancement in both personal and clinical applications. The integrated embedded device described in this paper, designed to generate and modulate neural rhythms, represents a significant contribution to developing an IoT platform targeted for applications such as the brain–computer interface (BCI). Enhanced signal processing capabilities could enable seamless interaction with IoT networks and CPS, allowing brain activity to control a range of connected devices directly. In CPS, which merges computational and physical processes, advanced neural decoding devices provide more intuitive and responsive interfaces. For instance, individuals with paralysis could utilize BCIs to manage smart environments with unprecedented precision [1].

Similarly, linking brain signals to IoT devices enables users to adjust home automation systems, operate assistive technologies, or interact with smart healthcare devices through thought alone [2]. This integration enhances user experience and improves independence for individuals with disabilities. The synergy between brain decoding technologies and IoT can foster adaptive systems that respond to real-time neural data, such as smart homes adjusting lighting or temperature based on the user's emotional or cognitive state [3].

The rapid evolution of IoT devices underscores the need for cost-effective and accelerated design at the chip level. Traditional chip design methods involve high costs and lengthy development time due to expensive proprietary tools and complex fabrication processes [4]. The Google SkyWater 130 nm open-source PDK addresses these challenges by reducing development costs and time-to-market [5]. This paper employs Tiny Tapeout, a platform designed to make chip production accessible and cost-effective [6]. Utilizing open-source tools and PDKs eliminates the need for restrictive licenses and NDAs operating on remote cloud servers. This approach aligns with the evolving digital chip design landscape, emphasizing accessibility and cost efficiency, particularly in educational settings [7]. Google's recent initiative to promote complete open-source manufacturing through collaborations with Efabless and SkyWater Technology has significantly democratized chip design. By utilizing the SkyWater 130 nm PDK, designers can access advanced manufacturing techniques without the prohibitive costs associated with semiconductor fabrication. The platform supports approximately 400 open-source designs on a single chip with 24 GPIO pins, which are then mounted on a demonstration board for thorough testing. The chip designers receive a datasheet and access to an online project index, allowing exploration of designs beyond their own and enhancing the educational and research value of the platform. This model promotes affordability by sharing the costs of chip packaging and circuit board manufacturing, making it particularly beneficial for rapid proof of concept designs. Each tile on the chip measures approximately 160×100 μm^2 and supports around 1000 logic gates. It is envisaged that analog and mixed-signal capabilities will be included in future designs, which is an essential requirement for real-time signal sensing in AI-enabled IoT devices, broadening the scope for experimentation. This aligns with the broader focus on digital chip design for academic research prototyping and educational purposes, such as the prototype application for reproducing brain rhythms, by providing a practical and engaging tool for researchers.

Making use of these open-source tools in IoT and CPS applications could facilitate integration with sensors, autonomous vehicles, and advanced healthcare technologies [8]. Furthermore, recent technological advancements underscore the importance of semiconductor design and fabrication, particularly low-power, high-efficiency devices in IoT and CPS [9]. Neuromorphic engineering is another important aspect of rapid prototyping, which aims to replicate neural systems in hardware. It offers solutions to traditional software-based models that could effectively be mapped with speed and energy efficiency and could significantly benefit from this initiative [10–13]. In this research, the proposed digital device designed using Google SkyWater 130 nm technology, capable of generating brain rhythms, illustrates the viability of cost-effective IoT device implementation. This system-level design demonstrates the viability of future advanced neural signal processing and applications in real-time for IoTs.

Previously, the high cost of proprietary design tools has been a barrier to semiconductor innovation. According to [14], more than a trillion semiconductors are produced annually, and the global semiconductor market is projected to reach a total value of USD 1 trillion by 2030. By adopting open-source tools such as the Google SkyWater 130 nm PDK, researchers can achieve cost-effective chip design and fabrication, reducing financial barriers, fostering innovation, and aligning with the need for scalable and economically viable solutions [15]. The semiconductor global supply chain during the COVID-19 pandemic in 2021 exposed vulnerabilities, emphasizing the need for a skilled workforce to address these challenges. The semiconductor industry faces skill shortages globally that impact its ability to innovate and respond to emerging needs [16]. Addressing these skill gaps through educational initiatives and training programs is imperative for advancing technology and ensuring industry resilience. Recent efforts and investments such as the UK's GBP 1 billion investment strategy [14], the European Chips Act investment forecast of more than EUR 43 billion [17], and the Chinese CNY 47 billion for chips investment have been announced [18]. These serious efforts and investments reflect a global recognition of semiconductor technology's strategic importance, underscoring how open-source solutions

can enhance innovation and efficiency in semiconductor design and fabrication, promising smarter and more responsive systems that improve quality of life and operational efficiencies [19].

1.2. Motivations and Contributions

As elaborated in the Section 1.1 of this paper, the importance of research efforts and skills in IoTs at the device level is imperative and timely. With emerging applications in AI-enabled IoT devices, the complexity of such devices will increase, and to keep up with the pace of technology, this work fills the gap by proposing efficient and cost-effective solutions in IoT system design. The rapid advancement and widespread adoption of these technologies require the need for digital chips that not only meet high performance and reliability standards but are also developed quickly and affordably.

Traditional chip design cycles pose significant challenges, including the high cost of development tools and associated licenses, which far exceed the budgetary constraints of higher education institutions, and secondly, extended development cycles restrict rapid prototyping and innovation. To address these challenges, this study demonstrates the use of the Google SkyWater 130 nm open-source PDK as an alternative to conventional chip design strategies and associated tools.

The primary objectives of this research are twofold: first, to demonstrate how open-source tools can simplify and expedite the chip design process and integrate with the IoT ecosystem, making it more accessible and economically viable. Secondly, to showcase the practical implementation of these tools through the development of a digital platform capable of generating brain rhythms that could potentially be used for future developments in treating neurological disorders. The digital IoT platform proposed in this study demonstrates a small-scale prototype within IoT applications, thereby fostering innovation while reducing development costs. By integrating the proposed IoT platform with various serial devices and Wi-Fi modules, the case study illustrates its potential for real-time processing and adaptive control systems. This research thus forth addresses the critical issue of skill shortages and resource limitations in IoT device development due to the constraints elaborated in the Section 1.1 of this paper.

By promoting the use of open-source tools and emphasizing the importance of skill development, this research contributes to advancing technology cost-effectively and helps mitigate skill gaps. The global emphasis on semiconductor technology, as reflected in recent investments and legislative actions, aligns with the goal of this research, which is to enhance chip design capabilities and leverage open-source solutions to drive innovation. This approach not only supports the development of cutting-edge IoT technologies but also provides a scalable and adaptable framework for future advancements in the field. The primary objectives and significant contributions of this paper are as follows:

1. Demonstrate the use of the Google SkyWater 130 nm open-source PDK as an alternative to conventional chip design for IoT device development;
2. Demonstrate open-source tools to simplify and expedite the chip design process and integrate with the IoT ecosystem;
3. Showcase the practical implementation with a small-scale prototype capable of generating brain rhythms;
4. Demonstrate the use of an open-source mobile application interfaced with an ARM Cortex-M0 processor and Wi-Fi module.

The rest of this paper is organized as follows:

Section 2 presents the software and hardware design, the development of an IoT device, its characterization, and mobile app integration. Sections 3 and 4 thoroughly discuss the research presented in this paper, as well as its limitations, followed by the conclusion in Section 5.

2. Materials and Methods

Brain rhythms are represented as continuous analog signals using sinusoidal functions. The general mathematical representation of a continuous sinusoidal waveform is given by Equation (1).

$$x(t) = A.\, sin\ (2\pi ft + \varphi) \tag{1}$$

where x(t) is the amplitude of the signal at time t, A denotes the peak amplitude, f is the frequency in Hertz (Hz), and φ, represents the phase shift in radians. This continuous function captures the smooth oscillations of brain rhythms over time. To represent these continuous signals in a digital system, they must be discretized into a series of digital samples. This process involves sampling the continuous signal at regular intervals and quantizing the amplitude values to fit within a finite digital range. The digital representation of a signal is governed by the sampling theorem, specifically the Nyquist–Shannon sampling theorem, which states that $F_s \geq 2{\cdot}f_{max}$, where F_s is the sampling frequency and f_{max} is the highest frequency component in the signal. This theorem ensures that the signal can be accurately reconstructed from its samples without aliasing, which occurs when high-frequency components are misrepresented as lower frequencies. To discretize the analog signal, we sample it at intervals of T_s, the sampling period, where $T_s = 1/f_s$.

Thus, the discrete-time signal $x[n]$ can be expressed by Equation (2).

$$x[n] = A.sin(2\pi f.n.Ts + \varphi) \tag{2}$$

where n is an integer index representing each discrete time step. Quantization is the process of mapping these continuous amplitude values to a finite set of discrete values, which is determined by the number of bits used in the digital representation. Therefore, with b bits of resolution, the amplitude is quantized into 2^b levels, and each sample is assigned one of these levels. In practical terms, if the continuous analog signal has a frequency component f of 50 Hz, and the chosen sampling frequency f_s is 1000 Hz, the sampling period T_s is 1/1000 s. For a signal with a period T = 1/f, the number of samples per period is given by Equation (3).

$$\text{Samples per period} = f_s \times T = f_s/f \tag{3}$$

This ensures that each cycle of the continuous signal is accurately captured by the discrete samples. For digital chip design, representing brain rhythms as discrete pulses allows the implementation of digital systems that can process and analyze these signals in real time. The digital pulses approximate the analog waveform by converting continuous variations in amplitude and time into a series of discrete values, making it feasible to integrate these signals into digital hardware. The transition from analog to digital representation involves approximating the continuous waveform with a sequence of digital values, facilitating efficient processing and analysis in digital circuits. This approach is essential for implementing brain rhythm simulations on digital chips, enabling real-time applications in neurotechnology and cyber-physical systems.

2.1. Software Design and Implementation

This section of the paper presents a case study demonstrating the practical applications of a custom-designed chip capable of generating these rhythms using open-source tools. By leveraging the Google Skywater 130 nm technology, the study illustrates how such a chip can be used for real-time modulation of brain signals, offering a cost-effective approach to advancing research and therapeutic interventions in neurotechnology. The Alpha, Beta, and Gamma rhythms were first simulated in software by using Python on Thonny design suite (Windows 10, Python 3.10.11, Tk 8.6.13) running on intel i7@1.87 GHz quad core.

Different brain rhythms, such as Alpha, Beta, and Gamma, represent various patterns of electrical activity in the brain, each associated with different cognitive and physiological states. Alpha rhythms, typically observed during relaxed wakefulness, range from 8 to 13 Hz and are crucial for calming the mind. Beta rhythms, ranging from 13 to 30 Hz, are

associated with active thinking and focus, while Gamma rhythms, from 30 to 100 Hz, are linked to higher cognitive functions such as problem-solving and perception. The simulated waveforms are shown in Figure 1.

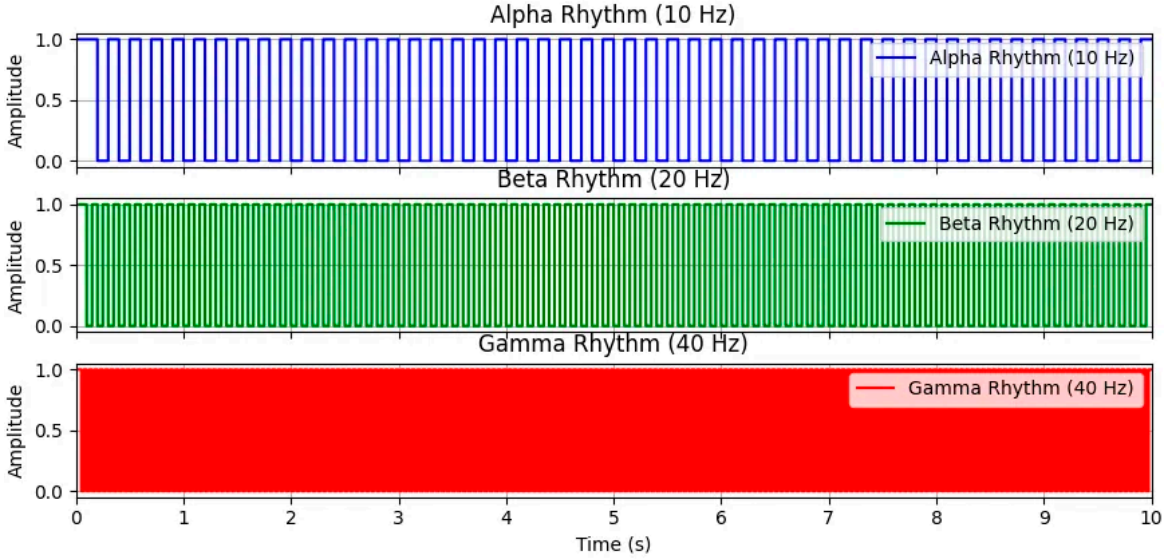

Figure 1. Simulated brain rhythms.

Figure 1 illustrates digital step signals for three distinct brain rhythm frequencies: Alpha, Beta, and Gamma. The purpose of the simulation is to demonstrate the variations in these rhythms, including how they are sampled and represented digitally. The sampling frequency used was 1000 Hz. This rate is crucial for accurately capturing the characteristics of the signal. In practical terms, this means that each second of the signal is divided into 1000 discrete points. Retrospectively, for the Alpha rhythm, which has a period of 100 milliseconds, there are 1000 samples in one second, so each cycle of the Alpha rhythm is represented by 100 samples.

The top plot in Figure 1 represents the Alpha rhythm at 10 Hz and shows that this rhythm completes one full cycle every 100 milliseconds. This slower oscillation is reflected in the plot as longer periods between transitions. The 1000 Hz sampling rate ensures that these transitions are captured with adequate detail, providing a clear depiction of the Alpha rhythm. The middle plot illustrates the Beta rhythm at 20 Hz. This rhythm has a shorter period of 50 milliseconds, meaning that each cycle occurs more frequently than the Alpha rhythm. The plot shows these more frequent transitions, with the Beta rhythm completing a full cycle every 50 milliseconds. The sampling rate of 1000 Hz is still sufficient to accurately represent these faster transitions. The bottom plot displays the Gamma rhythm at 40 Hz. This rhythm oscillates even more rapidly, with a period of just 25 milliseconds. The plot captures these rapid changes, highlighting the short time intervals between each transition. The high sampling frequency of 1000 Hz is essential here to ensure that the quick oscillations of the Gamma rhythm are accurately depicted. In all three subplots, the x-axis represents time in seconds. The x-axis is scaled consistently across all plots to allow direct comparison of the different rhythms.

The total duration shown in each plot is 10 s, which covers multiple cycles of each rhythm, offering a comprehensive view of how each rhythm behaves over time. The y-axis in each plot represents amplitude, showing the signal's high and low states. The step function in the plots depicts these transitions, where each rhythm alternates between a high state and a low state. The plots include labels and titles to specify the type of rhythm and its frequency, with the x-axis labeled as "Time (s)" and the y-axis labeled as "Amplitude". Overall, the figure demonstrates how different brain rhythms are represented digitally, highlighting the importance of a sufficient sampling frequency to capture the details of both slow and fast oscillations. The consistent sampling rate of 1000 Hz across all

rhythms ensures that each rhythm is accurately captured, providing a clear and detailed visualization of their characteristics.

Similar to Alpha, Beta, and Gamma rhythms, Delta and Theta rhythms are crucial brainwave patterns with distinct physiological and cognitive roles. Delta rhythms, characterized by frequencies between 0.5 and 4 Hz, are predominantly associated with deep sleep and are believed to facilitate restorative processes and memory consolidation [20]. The plot shown in Figure 2 generates and visualizes two types of brain rhythms, Delta and Theta, over 10 s using a sampling frequency of 1000 Hz. To create the time axis, an array is generated that spans from 0 to 10 s in 1-millisecond intervals. This array provides a detailed time scale for the x-axis, allowing each sample point to be accurately plotted. For signal generation, the Delta rhythm has a frequency of 2 Hz, which translates into a pulse occurring every 500 samples, while the Theta rhythm has a frequency of 5 Hz, resulting in a pulse every 200 samples. These specific frequencies determine the spacing and duration of each pulse in the signals. In the top subplot, the Delta rhythm is depicted with green step plots, showing periodic pulses every 500 samples. This creates a pattern reflecting the rhythm's lower frequency. The bottom subplot displays the Theta rhythm in red step plots, with pulses occurring every 200 samples, illustrating the higher frequency of this rhythm.

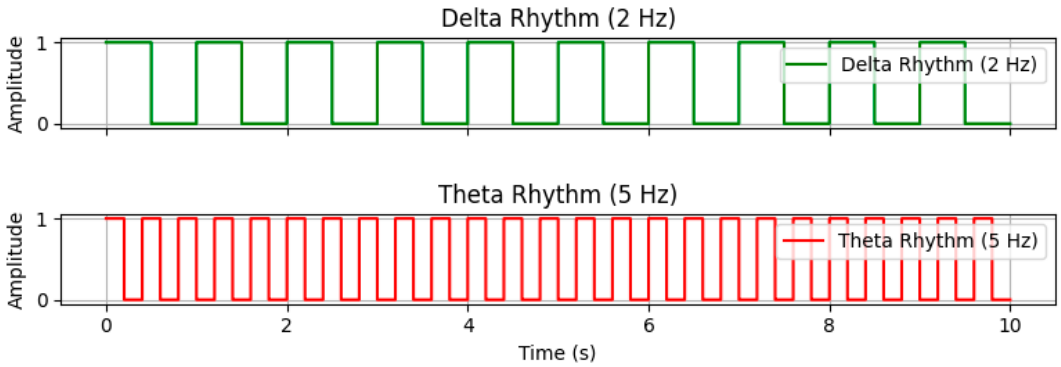

Figure 2. Delta and Theta rhythm.

Unlike regular brain rhythms reported in neuroscience, epilepsy is a neurological disorder characterized by recurrent seizures caused by abnormal electrical activity in the brain. Seizures often manifest as distinct changes in the brain's electrical rhythms, which can be observed using electroencephalography (EEG). These rhythms, categorized into different frequency bands, play a crucial role in understanding and managing epilepsy. The plots shown in Figure 3 visualize pulse signals at various frequencies, simulating chaotic behavior similar to that observed in epileptic seizures. This approach is essential in understanding how different frequency components interact to model complex neurological patterns.

The sampling frequency, set at 1000 Hz, ensures a high-resolution representation of the pulse signals. With a total duration of 10 s, this results in 10,000 samples, creating a detailed time series for analysis. The time array is generated to span this duration with 1-millisecond intervals between samples, providing an accurate depiction of the pulse signals over time. The top plot illustrates a pulse signal with a low frequency of 2 Hz. Here, the x-axis represents time in seconds, while the y-axis shows the amplitude of the signal, which alternates between 0 and 1. At 2 Hz, the signal completes a cycle every 0.5 s, resulting in a repetitive pattern of pulses. Low-frequency oscillations, such as those in the Delta (0.5–4 Hz) and Theta (4–8 Hz) bands, are associated with various brain states. Delta waves are linked with deep sleep, while Theta waves are observed during lighter sleep and certain cognitive processes [20]. This plot captures the lower end of these oscillatory patterns, providing insight into baseline brain activity. The second plot depicts a pulse signal with a medium frequency of 5 Hz. The time axis and amplitude axis follow the same conventions, but at 5 Hz, the signal completes a cycle every 0.2 s. This creates a more frequent pulse pattern compared to the 2 Hz signal. Medium-frequency oscillations, such as those in the Theta range, are often observed during cognitive tasks and can reflect

transitional brain states. In epilepsy, these frequencies may appear during seizures or abnormal brain activity [21]. This plot demonstrates the contribution of medium-frequency components to overall brain dynamics. The third plot (from the top) shows a pulse signal with a high frequency of 15 Hz. The signal oscillates every 0.067 s, leading to a densely packed pulse pattern. High-frequency oscillations, including Beta (13–30 Hz) and Gamma (30–100 Hz) bands, are associated with heightened neural activity and various cognitive functions. They are also relevant in the context of epileptic seizures, where high-frequency bursts can indicate increased seizure activity [22].

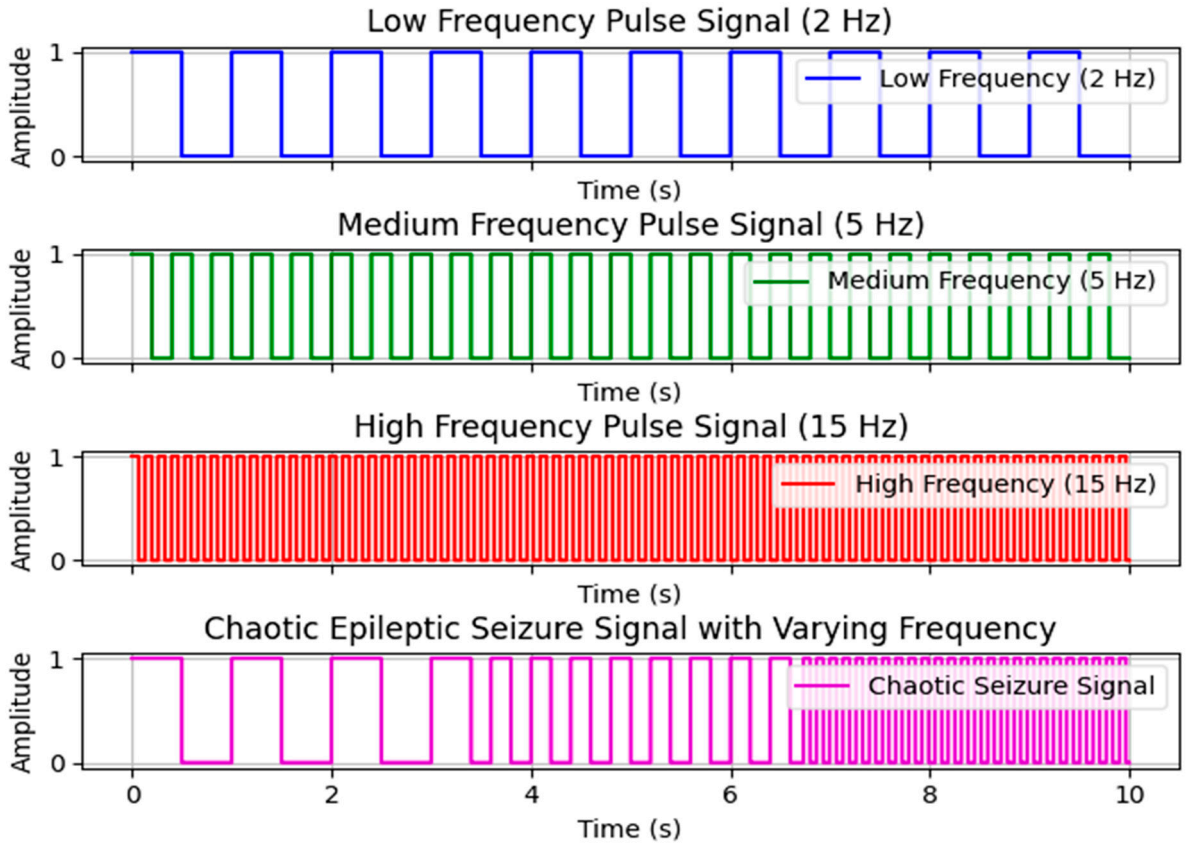

Figure 3. Pulse signals simulating brain activity and seizure patterns.

This plot illustrates how high-frequency components are represented, which is important for understanding the impact of rapid oscillations during seizures. The bottom-most plot presents a chaotic pulse signal with dynamically varying frequency. The *x*-axis shows time, and the *y*-axis indicates the amplitude of the signal, which changes to simulate seizure-like behavior. The signal begins with a low frequency, transitions to a medium frequency, and then shifts to a high frequency. This modulation reflects the complex and dynamic nature of epileptic seizures, where frequency and amplitude fluctuate unpredictably due to the rapid synchronization and desynchronization of neural activity. In actual seizures, the brain's normal rhythms are disrupted, leading to irregular and high-amplitude bursts of activity [21].

This chaotic behavior in the plot offers a visual representation of the erratic nature of seizure activity, providing valuable insights into the dynamics of neural oscillations during epilepsy. The generated plots effectively illustrate how different frequency components and their combinations can model brain activity and epileptic seizures. By varying the frequency dynamically, the chaotic signal captures the unpredictable nature of seizures, enhancing our understanding of these complex neurological phenomena. This simulation serves as a valuable tool for analyzing seizure activity and offers a foundation for further research into the dynamics of epilepsy. Furthermore, such simulations can enhance the development

of methods for seizure detection and modulation, providing practical applications for real-time monitoring and therapeutic interventions [22].

2.2. Hardware Design and Implementation

Digital counters are fundamental components in digital electronics, used to count pulses or events, and are employed in this study to generate periodic waveforms, including various brain rhythms such as Alpha, Beta, Gamma, Delta, and Theta rhythms. These counters operate by incrementing their count with each clock pulse and can be tailored to produce specific frequencies by adjusting the counting range and clock frequency. In this study, synchronous counters were utilized to generate periodic signals corresponding to these brain rhythms.

The basic operation involves a counter that increments with a clock signal and generates an output pulse when a designated count is reached. This pulse can then be used to create waveforms with the desired frequencies. To produce the Alpha rhythm at 10 Hz, with a clock frequency of 1 kHz, the counter produces an output pulse every 100 clock cycles. Therefore, a counter with 100 stages, or a modulus of 100, is employed, which is implemented as a 7-bit counter with additional logic to reset at 100 counts. This design ensures that a pulse is generated each time the counter reaches 100. For the Beta rhythm at 20 Hz, also with a 1 kHz clock frequency, the counter needs to generate a pulse every 50 clock cycles. Thus, a counter with 50 stages or a modulus of 50 is used. This is implemented with a 6-bit counter, producing a pulse whenever the counter reaches 50. To achieve the Gamma rhythm at 40 Hz, the counter must output a pulse every 25 clock cycles. A counter with 25 stages, or a modulus of 25, is used, which is implemented with a 5-bit counter. This setup generates a pulse each time the counter reaches 25. Each of these counters is designed with an appropriate number of flip-flops to match its modulus.

For the Alpha rhythm, seven D-flip-flops were used, as this is sufficient for the modulus of 100. For the Beta rhythm, six flip-flops are adequate, and for the Gamma rhythm, five flip-flops are used, as $2^5 = 32$ is enough for the modulus of 25. Each counter is connected to a 1 kHz clock source, with flip-flops arranged in series and logic gates employed to decode the count and generate the output pulse. These digital counters and their waveforms are designed to be implemented on a chip using the Google Skywater 130 nm node with open-source tools.

This open-source approach allows for the development and fabrication of the chip at a lower cost, fostering innovation and accessibility in academic settings with limited resources to budget and tools. The digital waveforms produced by these counters are characterized as periodic pulses, demonstrating the rhythm frequencies. For instance, the Alpha rhythm's waveform displays a pulse every 100 clock cycles, the Beta rhythm shows a pulse every 50 clock cycles, and the Gamma rhythm reveals a pulse every 25 clock cycles. These waveforms are depicted as digital step functions, highlighting the periodic nature and frequency of each brain rhythm. In each design, the D flip-flops are connected in a series configuration to form a binary counter. The clock input drives the flip-flops, and the output from the last flip-flop is used to determine when the counter reaches the specified count. A comparator was employed to detect the specific count value and generate an output pulse. The reset logic ensures that the counter restarts after reaching the designated count, maintaining periodic waveform generation.

A synthesis view of the circuit diagram simulated by Yosys 0.38 [23] is shown in Figure 4. The circuit was simulated with Icarus Verilog 12.0, and simulations are shown in Figure 5. An overall flowchart from design specification to implementation, including GDS generation and final chip characterization, is shown in Figure 6. As shown in Figure 4, square boxes represent cells. Outputs are shown on the right, while input ports are shown on the left. The first line of text inside the box indicates the cell name for internal cells. The second line specifies the cell type. Internal cell types start with a dollar sign. Diamond-shaped nodes represent wires that are not ports (blue wires interface), whereas octagon-shaped nodes represent ports (purple wires interface). Elliptical nodes are constant

drivers (green wires interface and standard paths), and their labels follow the format <width>'<bits>. Boxes with rounded corners and labels such as 4:0–4:0 are used to break out and re-combine nets from buses (olive wire control signal). These boxes help manage and reorganize signal connections within a bus structure.

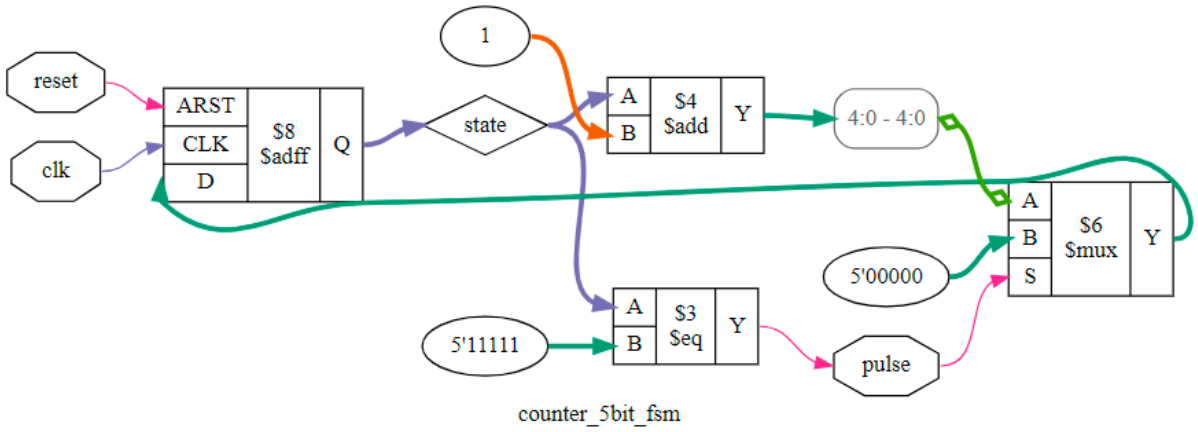

Figure 4. Hardware synthesis circuit diagram for a 5-bit counter to emulate Gamma rhythms.

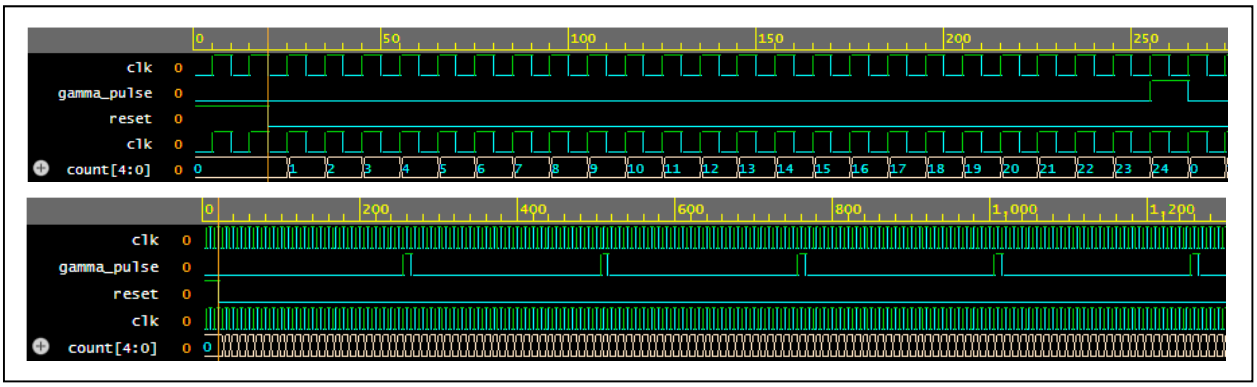

Figure 5. Gamma rhythm simulated with Icarus Verilog 12.0 to verify the functionality of the circuit.

To calculate computational latency for software simulations and hardware synthesis, unlike commercial tools, the open-source tools used in this study provide very limited automated options. In this work, an HP ProBook laptop was used with Intel(R) Core i7-10510U CPU @ 1.80 GHz, four cores, and eight logical processors with 8 GB RAM. Given the complexity of the code, computational latency is negligible. The computational latency for software simulations was recorded as 6 milliseconds for various brain rhythms generation. For hardware simulations, Yosys, an open-source tool, does not provide built-in functions for measuring synthesis time; however, a time counter in Verilog is included. The CPU user time was recorded as 0.03 s, and the system time as 0.01 s. Hence, the total elapsed time for the synthesis of the FSM using Yosys was recorded as 40 milliseconds. A screenshot of the calculated time is shown below.

```
End of script. Logfile hash: 17a1c523c1, CPU: user 0.03s system 0.01s, MEM: 10.96 MB peak
Yosys 0.38+113 (git sha1 91fbd5898, clang++ 14.0.0-1ubuntu1.1 -fPIC -Os)
Time spent: 84% 1x show (0 sec), 4% 8x opt_expr (0 sec), ...
Finding SVG file...
./.yosys_show.svg
[2024-10-20 16:08:32 UTC] Opening circuit diagram...
Done
```

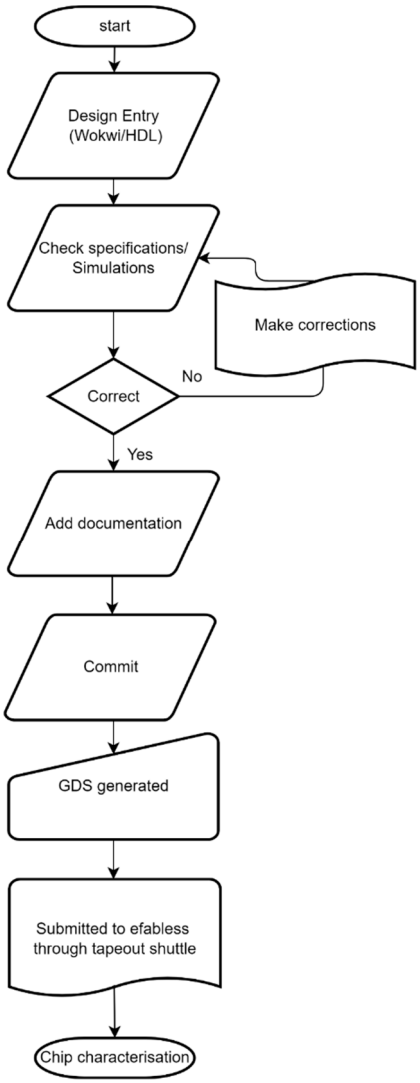

Figure 6. Chip design simulation and submission flow with open-source tools.

Similarly, Yosys does not provide a built-in power analysis tool; however, the power consumption could be estimated using the demo board's 3.3 V IO supply voltage and 4 mA drive strength. For the low-frequency digital circuit, static power consumption is considered negligible, and dynamic power consumption can be estimated using the following expression, as shown in Equation (4).

$$P_{dynamic} = C_{load} \times V^2 \times f \tag{4}$$

The load capacitance could be estimated by Equation (5).

$$C_{load} \approx \frac{I_{drive}}{V \times f} \tag{5}$$

For 1 kHz operating frequency, 3.3 V IO supply voltage, and 4 mA drive strength, the load capacitance is ≈1.21 uF. Hence, the dynamic power consumption is estimated at 42 mW.

2.3. Chip Layout

The digital chip was developed using the Wokwi and GitHub templates [24,25] with the Google Skywater 130 nm process, which is a fully open-source PDK, to ensure accessibility for educational and research purposes [26,27]. The chip features multiple digital counters, each configured to generate specific brain rhythm frequencies. The complete

chip layout of all designs, as rendered in GDS, is depicted in Figure 7a [27]. The chip is packaged in a 64-pin QFN, and the chip layout of the design presented in this paper is shown in Figure 7b. The design detailed in this paper utilized a single tile, which measures 160 × 100 μm^2. The total cell utilization is shown in Table 1.

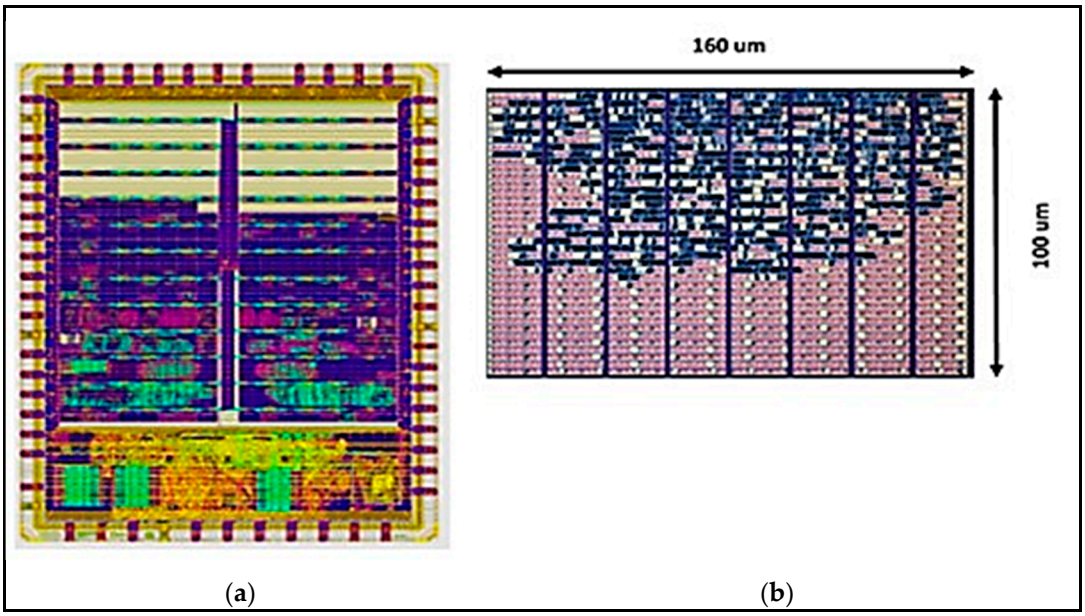

Figure 7. (**a**) GDS renderer for overall designs and (**b**) chip layout of the proposed design (160 × 100 um).

Table 1. Total cell usage.

Category	Count
Inverter	
Tap	287
Flip-Flops	246
Buffer	171
AND	50
Misc.	39
Combo Logic	26
NOR	10
OR	10
Multiplexer	2

In total, 596 cells were used, which was 32.45% of the total logic available.

2.4. Chip Verification

The chip was tested using the Commander app via a serial port alongside an 8-channel logic analyzer. The IO pins on the breakout board were connected to a Saleae logic analyzer [28] tool to detect and verify various brain rhythms. The breakout board and connection setup are illustrated in Figure 8. The chip characterization and the resulting waveforms are displayed in Figure 9. To ensure accurate testing and characterization, the setup involved configuring the serial app to interface with the chip through the serial port, while the Saleae logic analyzer provided detailed waveform analysis through its 8-channel interface. This setup allowed for comprehensive verification of the chip's ability to generate and replicate the targeted brain rhythm frequencies.

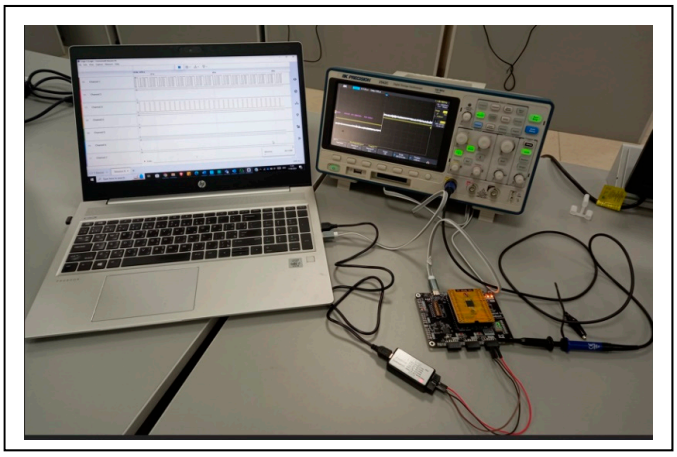

Figure 8. Chip connection with a serial logic analyzer for chip characterization.

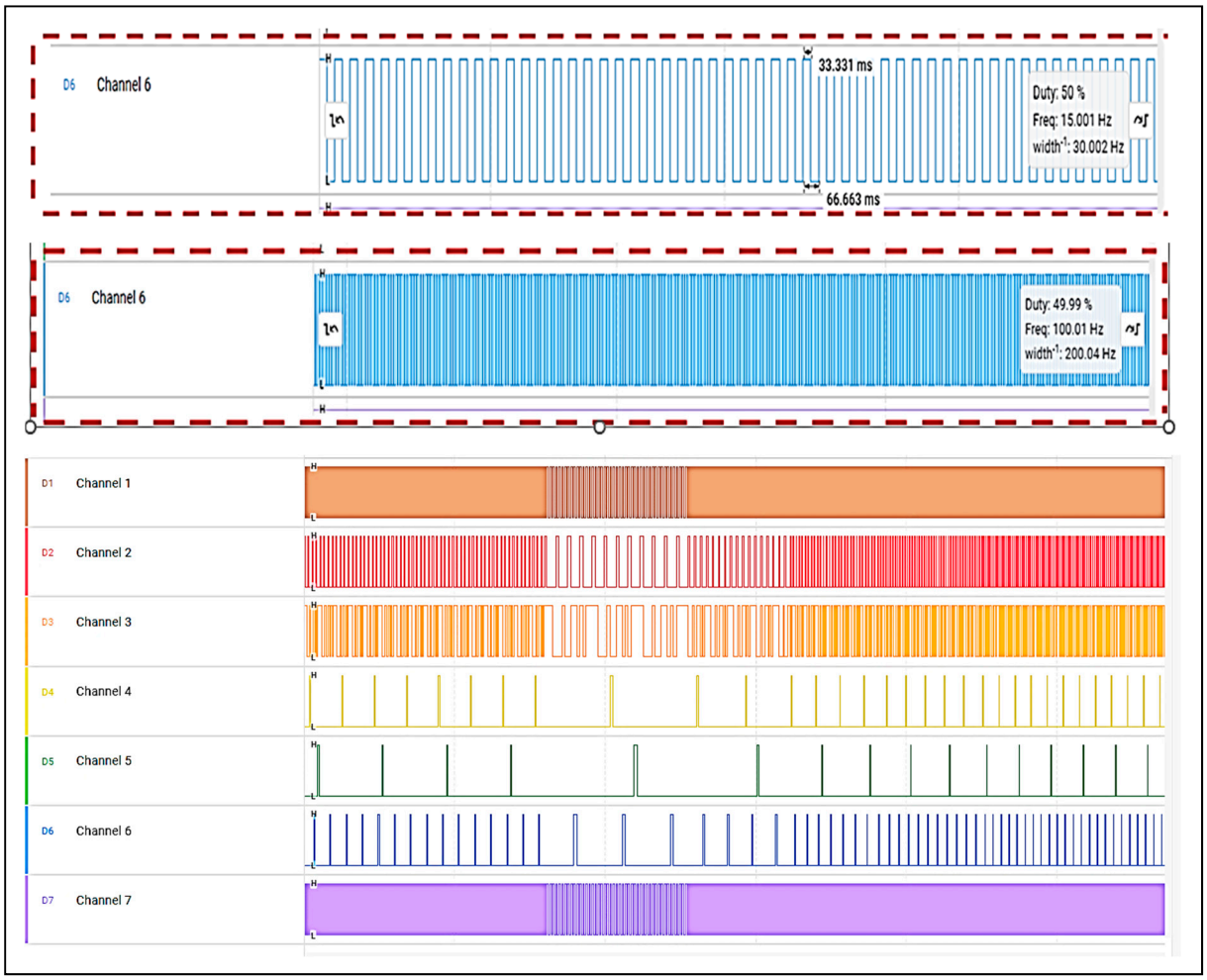

Figure 9. Multiple channels show the required frequencies generated by the chip.

The results reported demonstrated the chip's performance and functionality in generating the expected rhythms, confirming its effectiveness for its intended applications. The detailed connection schematics and breakout board layout, as depicted in Figure 8, facilitated the testing process and supported the successful validation of the chip.

2.5. IoT Connectivity with Mobile App Interface

To enhance the functionality of the open-source customized platform for brain rhythm generation, an open-source Blynk mobile application was integrated with the platform [29]. The Blynk app was developed to remotely control the Wi-Fi module integrated into an Arduino board. This integration demonstrates how the platform can be extended into an integrated IoT ecosystem, allowing wireless control of modulating brain rhythms. By introducing this IoT feature, we can illustrate how IoT-enabled wireless communication modules interact with the custom-designed brain rhythm chip, enabling real-time control and monitoring, as illustrated in Figures 10 and 11.

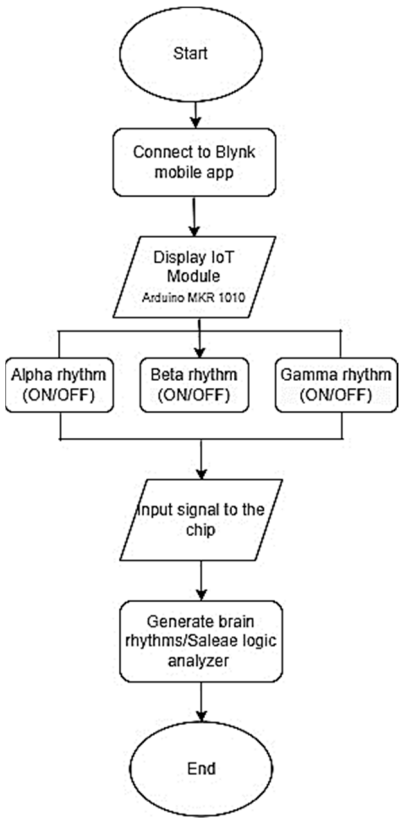

Figure 10. Mobile app interface with the MKR Wi-Fi 1010 IoT module.

The integration was achieved by setting up an Arduino board (MKR WIFI 1010) [30] with a Wi-Fi module, which facilitated wireless communication between the Blynk mobile app and the brain rhythm chip. The Arduino board was programmed using the Arduino IDE, and code was developed that allowed the Arduino to receive commands from the Blynk app and transmit them to the brain rhythm chip via the GPIO pins, as shown in Figure 10. The Wi-Fi module was configured to connect to a local wireless network, enabling communication between the mobile app, Arduino board, and the brain rhythm chip. In the code implementation, the SAMD21 Cortex-M0+ module connected to the local Wi-Fi network using authentication tokens from the Blynk app. The mobile app sent control commands to the Arduino via the Wi-Fi module, which were then relayed to the brain rhythm chip. The Blynk app's switches were mapped to virtual pins (2, 3, and 4), which allowed the user to select different brain rhythm frequencies (such as Alpha, Beta, and Gamma) connected through the Arduino IoT board to the input pins of the daughter board. When the user selects the virtual switch, it sends a signal through the SAMD21 Cortex-M0+ microcontroller to the GPIO pins to trigger the corresponding output on the chip, as illustrated in Figure 11.

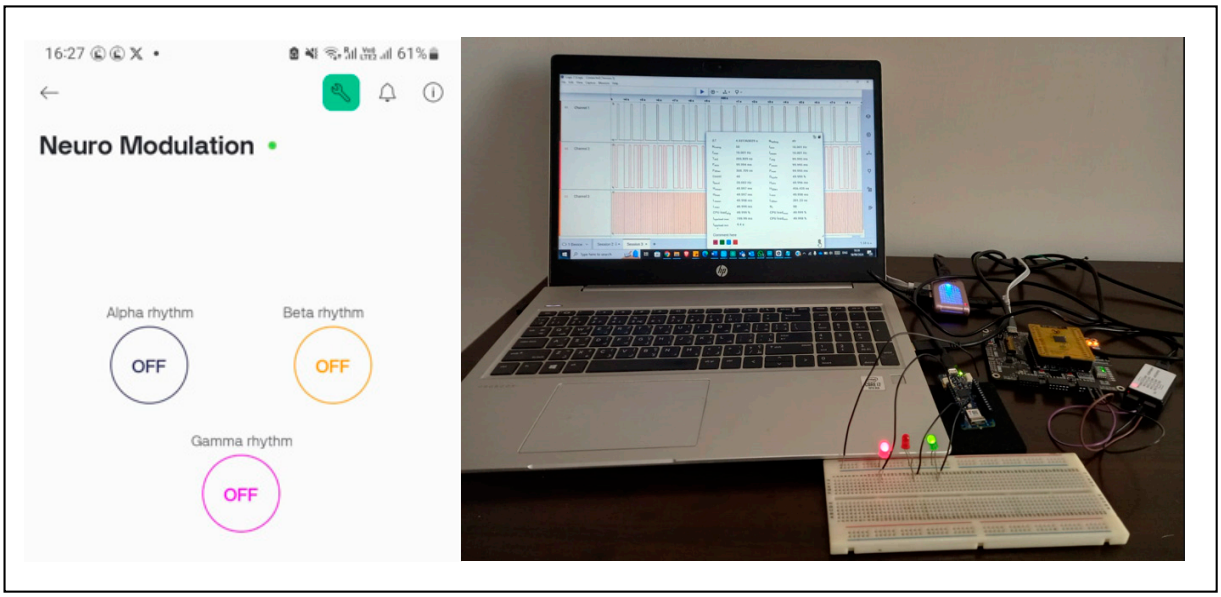

Figure 11. Blynk mobile app interface with the MKR 1010 IoT board with chip interface and Saleae logic analyzer.

This setup allows for smooth interaction between the mobile app and the hardware, resulting in a fully functional IoT-enabled brain rhythm modulator. The Blynk mobile app was configured with user-friendly interfaces to instantiate different frequencies, emulating brain rhythms wirelessly. This user interface enables quick and easy control over the chip's output, making the system accessible for further research in IoT-enabled neural signal modulation. The platform successfully demonstrated the ability to wirelessly switch between different brain rhythms without manual reconfiguration, showcasing its flexibility and robustness, as shown in Figure 12.

The proposed IoT platform, combined with the Blynk app interface and a custom-designed chip developed with all open-source tools, serves as a novel platform for learning and research. It enables researchers to gain practical experience with IoT, hardware–software integration, and system design. The simplicity of the app interface makes it easy for researchers to experiment with IoT-enabled devices. This approach also fosters innovation, allowing engagement with cutting-edge technologies in a meaningful way. In addition to its educational benefits, the integration offers scalable possibilities for industrial applications. Combining IoT, and real-time brain rhythm generation, as a prototype opens the door to applications in smart healthcare solutions, adaptive control systems, and real-time neural signal processing. The computational latency and low power aspects pave the way for standalone IoT applications, as alluded to in Section 2.2.

The designed chip was interfaced with an Arduino MKR Wi-Fi 1010 powered by the SAMD21 Cortex-M0+ 32-bit ARM microcontroller, offering efficient performance with low power consumption, making it ideal for IoT applications. It integrates the NINA-W102 module (based on ESP32) for Wi-Fi and Bluetooth connectivity, supporting 2.4 GHz networks while maintaining energy efficiency for battery-powered applications. The author acknowledges the use of Grammarly 14.1202.0 and ChatGPT 4 mini in the process of translating and improving the clarity and quality of the English language in this manuscript.

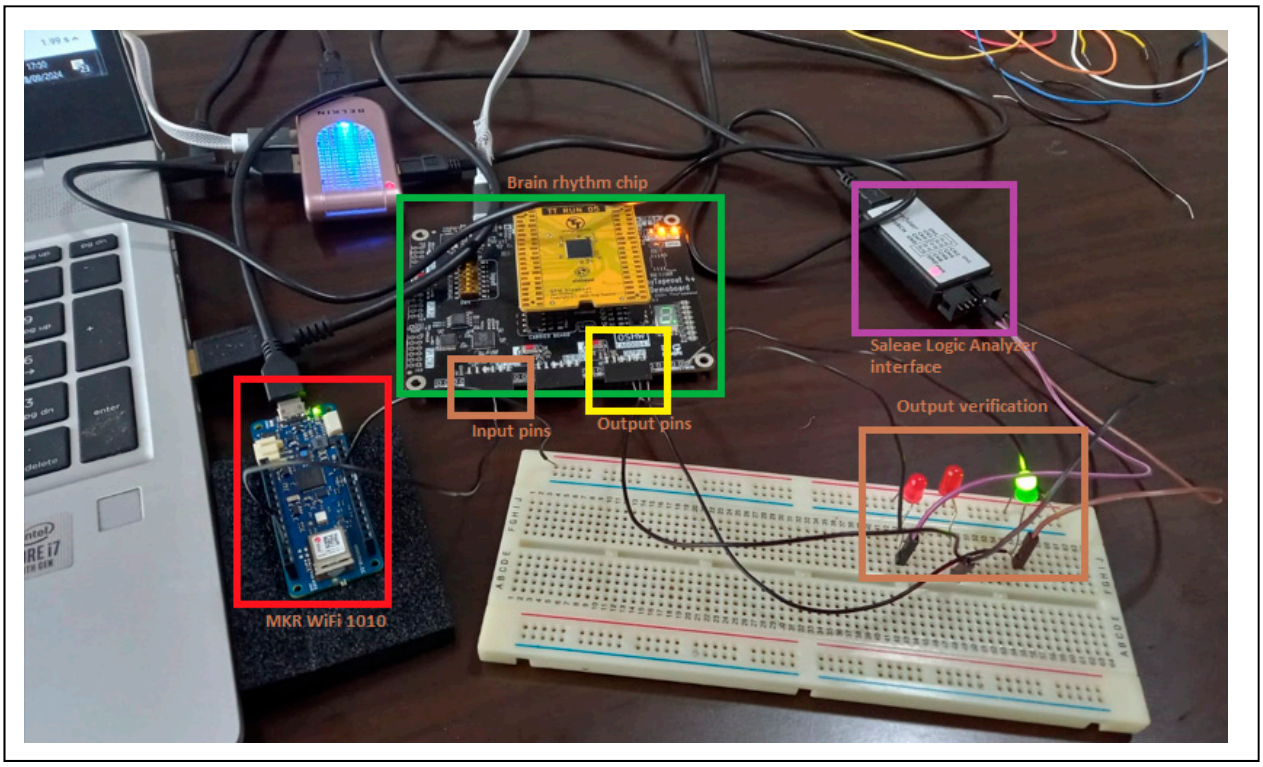

Figure 12. Test setup with MKR Wi-Fi board interface with the chip and Saleae logic analyzer for chip verification.

3. Discussion

Alpha rhythms are typically associated with relaxed wakefulness, being most prominent when a person is calm but awake. Abnormalities in Alpha rhythms during seizures can indicate altered brain states or the onset of seizure activity. Monitoring these rhythms provides valuable insights into baseline brain activity and potential deviations that might precede or accompany seizures. By identifying these disruptions early, healthcare providers can better predict and manage seizures, improving patient outcomes. Beta rhythms, on the other hand, are linked to active cognitive processing and motor functions. In the context of epilepsy, alterations in Beta rhythms can signal heightened brain excitability or the propagation of seizure activity. Disruptions in Beta rhythms during seizures can aid in identifying and localizing seizure foci, which is critical for targeted therapeutic interventions. Accurate analysis of these rhythms can help in the development of more effective treatment strategies and enhance our understanding of the complex mechanisms underlying seizure activity.

The chip designed to generate these fundamental brain rhythms demonstrates a viable option for academic research. By simulating and generating Alpha, Beta, and Gamma rhythms, the chip creates a controlled environment for studying their roles in epilepsy. When used alongside EEG data, this chip enables researchers and clinicians to compare generated rhythms with actual brain activity, thereby enhancing the accuracy of seizure detection and localization. Continuous generation of these rhythms can help identify deviations indicative of potential seizures, facilitating earlier intervention and more effective treatment.

Furthermore, the chip's ability to generate and modulate specific brain rhythms opens up exciting potential therapeutic applications. For instance, it can be utilized in closed-loop neurostimulation systems, where the chip generates compensatory rhythms to counteract abnormal brain activity. This approach could help stabilize brain activity and mitigate seizures, offering a new avenue for therapeutic intervention. Beyond its application in epilepsy research, the integrated platform holds promise for a wide range of IoT applications. In intelligent transportation systems, real-time neural processing could

enhance decision-making and improve safety by integrating neural data with vehicular control systems. In industrial IoT, such chips can advance monitoring and control systems, leading to more efficient and responsive operations. The design and implementation of this chip using open-source tools underscore the importance of democratizing access to advanced technology.

Open-source platforms allow for cost-effective experimentation and innovation, particularly valuable for university students and researchers. By reducing the barriers to entry for advanced chip design, open-source tools play a crucial role in fostering the next generation of engineers and researchers, contributing to the advancement of technology and science on a global scale. Recent studies have highlighted the benefits of using open-source tools to streamline chip design. For instance, authors in [31] explore the financial and operational advantages of open-source design tools for IoT chips, demonstrating a reduction in design costs and a faster time-to-market. However, their work primarily focuses on hardware design aspects and lacks detailed implementation scenarios. Similarly, authors in [32] discuss the role of open-source hardware in alleviating chip shortages through 3D printable breakout adapters, which reduce design costs and aid faster prototyping. Their work showcases how open-source tools can be vital in distributed manufacturing models for IoT and electronics design. Authors in [33] provide an overview of IoT architecture, protocols, and data formats, proposing a reference architecture and reviewing popular data layer protocols and formats. The article also highlights the importance of gateways in ensuring compatibility between IoT devices and platforms. Additionally, it surveys both commercial and open-source IoT platforms, noting the heterogeneity of open-source options. The article also includes a summary of relevant free and open-source projects, making it a valuable resource for IoT system deployment.

Retrospectively, the author of this paper proposes the use of end-to-end open-source tools for IoT development at the device level, with no commercial tools involved. The proposed platform is a novel, cost-effective, easily implementable solution for generating brain rhythms while also serving as an educational resource for hands-on experience with applied IoT technologies. The proposed work in this paper addresses several gaps, such as by using the Google SkyWater 130 nm open-source PDK, demonstrating a cost-effective chip design solution with a development cost of approximately USD 150 per tile, significantly lower than traditional proprietary tools [34]. Further IoT applications have been reported in the literature [35–39]; however, none of these reported studies offer an end-to-end solution for IoT development. The approach presented in this paper not only reduces financial and temporal costs but also accelerates time-to-market, making advanced chip design integrated with IoT capability more accessible. Hence, the proposed research offers a valuable contribution that bridges the gaps identified, providing practical implementations and supporting educational initiatives in the IoT and semiconductor industry.

4. Future Work and Limitations

Open-source IoT development and applications entail several focus areas. In applications related to neural signal processing, integrating complex neural models could enhance the capabilities of the proposed IoT platform, making it more valuable for research on brain function and disorders. While the Google SkyWater 130 nm technology does facilitate open-source device development, it also imposes limitations, such as a tile size of approximately 160×100 μm^2, which supports around 1000 logic gates. This size is relatively small and restricts large designs, thereby limiting the complexity of the designs that can be implemented. If users wish to add more tiles, the cost of the device increases retrospectively. Furthermore, existing open-source hardware synthesis tools do not offer automated power and speed calculations; they require the netlist to be analyzed by other tools, which restricts design automation at the system level. Addressing these constraints will be crucial for future research, aiming to expand the chip's functionalities for broader applications in neuroscience, IoT, and cyber-physical systems.

5. Conclusions

This paper successfully demonstrates the design, implementation, and characterization of a digital platform capable of generating various brain rhythms using the Google SkyWater 130 nm PDK. The platform not only emulates key brain rhythms but also provides a versatile solution for integration into IoT and CPS, offering real-time neural signal processing and adaptive control system capabilities. By utilizing open-source tools, this approach presents a cost-effective method for both industrial applications and academic research, fostering hands-on experimentation and bridging the gap between theoretical knowledge and practical skills in hardware–software integration. Furthermore, its compatibility with serial devices, mobile applications, and Wi-Fi modules enhances its versatility, ensuring future scalability within broader IoT ecosystems. This work underscores the potential of open-source technology in advancing both educational and industrial initiatives, highlighting its value for future research and innovation in neural signal processing and IoT platforms. Nonetheless, as highlighted in Section 4 of this paper, this work provides a significant opportunity for academics and researchers to explore further applications and address the skills shortage. Retrospectively, it will require strong commitments from academic and research institutions, as well as governments, to recognize the urgent needs and opportunities this discipline offers. Additionally, there should be more focus on developing open-source tools and democratizing the toolchain and chip fabrication to fully benefit from the technological advancements.

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Conflicts of Interest: The author declares that at the time the paper was published, they had no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. The work was entirely self-funded. An indirectly related patent is pending at the American University of Ras al Khaimah, Research Office, UAE.

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