A 3-to-5 V Input, 80 Peak-to-Peak Voltage (Vpp) Output, 2.75% Total Harmonic Distortion Plus Noise (THD+N), 2.9 µF Load Piezoelectric Actuator Driver with Four-Switch Buck–Boost

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Abstract: As human–computer interaction has become increasingly popular, haptic technology has become a research topic of great interest, since vibration perception, as a type of haptic feedback, can enhance user experience during an interaction. However, the high power consumption of existing drivers makes them unsuitable for use in portable devices. In this paper, a bidirectional four-switch buck–boost converter (FSBBC) and Proportional–Integral (PI)–Proportional (P) feedback control are proposed to implement a driver in a high-capacitance piezoelectric actuator which is capable of recovering the energy stored in the high-capacitance load and increasing efficiency. The FSBBC offers an extended input voltage range, rendering significant technological advantages in diverse applications such as automobiles, laptops, and smartphones. By implementing specific control strategies, the FSBBC not only outperforms conventional buck–boost converters in boosting performance, but also ensures that the output and input voltages retain the same polarity. This effectively addresses the polarity inversion challenge inherent to traditional buck–boost circuits. Within the FSBBC, the significant reduction in voltage stress endured by the MOSFET effectively minimizes system costs and size and enhances reliability. The proposed system was simulated in Simulink, which was combined with testing on a field-programmable gate array (FPGA). The driver is capable of driving capacitors of up to 2.9 µF, with 80 Vpp output and 2.75% total harmonic distortion (THD) observed in the test.

Keywords: piezoelectric actuator; bidirectional four-switch buck–boost converter; digital PID; FPGA

1. Introduction

Vibration feedback is a haptic interaction method, which is a key method for human–computer interaction. Wearable devices—particularly, smart watches and sports bracelets—have entered many people’s daily lives, and vibration effects play a crucial role in giving consumers useful information. Piezoelectric actuators also have several advantages over conventional vibration actuators, including quick response times, broad driving bands, high vibration intensities, delicate and realistic vibration experiences, low acoustic noise, low power requirements, and small size [1–3]. Additionally, piezoelectric actuators have capacitive loads, which allows for bidirectional flow of energy, which increases efficiency [4]. They can be widely used to provide high-quality vibration feedback effects in low-power, small-footprint systems.

At present, actuators made of piezoelectric ceramic fall into two main categories: operational amplifier-type and PWM switching-type actuators. Series of amplifier-type actuators, which typically use Class A, Class B, and Class A–B operational amplifiers to drive piezoelectric actuators, have been developed by Texas Instruments [5] and Maxim Integrated [6]. Operational amplifiers were in a dominant position during the early development stage of piezoelectric actuator drivers because of their simplicity [7–9]. Wireless
optical power-transfer technology, based on operational amplifiers, was proposed to overcome the limitations in conventional wired electrical connections, to improve the flexibility and mobility of actuators for micro-robots [10]. However, because piezoelectric actuators have capacitive loads and operational amplifiers cannot recover the energy stored within the actuators, efficiency is reduced [11]. Additionally, operational amplifiers suffer from large power losses and bulky heat sinks.

Switching amplifiers have advantages over operational amplifiers; for example, they are small, lightweight, and highly efficient. Switching power supplies are perfect for creating miniature circuits because they mix passive parts and active semiconductor switches to transfer energy frequently and effectively between the power supply and the load. A single-inductor, highly integrated, bidirectional, high-voltage actuator driver was proposed with low power consumption and total harmonic distortion (THD) [12]. It is a boost circuit and cannot provide buck functions in some high-voltage application scenarios, for example, 48 V in-vehicle power supply systems. Additionally, capacitive DC–DC converters were proposed, and various voltage conversion ratios can be obtained, which can significantly reduce power consumption in comparison with hard-switched drivers [13]. However, because their output voltage can only rise multiplicatively, they cannot produce arbitrary waveforms.

In this study, we propose a piezoelectric actuator driver grounded on a bidirectional four-switch buck–boost converter (FSBBC) integrated with PI–P feedback control. Table 1 presents a comparative analysis of boost, buck–boost, and FSBBC. Distinguished by its broader input voltage adaptability, FSBBC showcases significant technological advantages over standard converters. This adaptability is particularly beneficial in diverse applications such as automotive electronics, laptop power management, and addressing the dynamic power requirements of contemporary smartphones. FSBBC integrates specialized control strategies, enabling it to not only outperform traditional buck–boost converters—equivalent to the “boost” circuit—in terms of boosting performance, but also to maintain the same polarity between output and input voltages. This stands in contrast to the polarity inversion issues often faced by conventional buck–boost circuits. Delving deeper into the design intricacies of the FSBBC, one can observe a notable alleviation in the voltage stress exerted on the MOSFET components. Such mitigation translates into tangible benefits, paving the way for reduced system costs and a more compact footprint. More crucially, this design refinement augments the overall reliability of the system. This enhanced reliability proves paramount in critical applications, especially in sectors like medical, aviation, and military.

Table 1. Comparison of different circuit structures.

<table>
<thead>
<tr>
<th></th>
<th>Boost</th>
<th>Buck–Boost</th>
<th>Four-Switch Buck–Boost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase Shift of the Input and Output</td>
<td>no</td>
<td>reverse</td>
<td>yes</td>
</tr>
<tr>
<td>Boost Capability (Vo/Vin)</td>
<td>$\frac{1}{D}$</td>
<td>$D$</td>
<td>same</td>
</tr>
<tr>
<td>MOS Voltage Stress</td>
<td>$V_o$</td>
<td>$V_o + V_i$</td>
<td>$V_o$ or $V_i$</td>
</tr>
</tbody>
</table>

$D$ represents the duty cycle.

The rest of the paper is organized as follows: the architecture and closed-loop feedback are introduced in Section 2, the stability analysis and parameter determination are conducted in Section 3, the hardware implementation and test results are shown in Section 4, and the conclusion is presented in Section 5.

2. Proposed Method

Generally, the output of a DC–DC converter is constant and its output value is determined by the duty cycle. In this study, a four-switch buck–boost circuit is proposed as the major driving circuit, and a full-bridge circuit is used to expand the voltage waveform to form a larger peak-to-peak voltage, as shown in Figure 1.
The overall block of the suggested driver is shown in Figure 2. The ADC samples’ voltage and current signals are then used as inputs for the digital closed-loop feedback. Next, voltage and current dual closed-loop processing is performed to generate the duty cycle of the PWM signal, which then drives the MOSFETs for the operation.

2.1. Four-Switch Buck–Boost Circuit

The simplest approach is to allow Q1 and Q4 to switch simultaneously as a pair of MOSFETs, while Q2 and Q3 switch simultaneously as another pair of MOSFETs. However, the biggest drawback of this approach is that all four MOSFETs should switch every cycle; hence, losses are large and common-mode noise is also large.

However, the four-switch buck–boost circuit shown in Figure 3 can be considered as a series of buck and boost circuits. If we define Q1 and Q2 as buck units, Q3 and Q4 as boost units, and \( d_1 \) and \( d_2 \) as the duty cycles of buck and boost units, respectively, the average voltage at points A and B in Figure 3 are

\[
\bar{V}_A = d_1 V_{in}
\]

\[
\bar{V}_B = (1 - d_2) V_0
\]
The following derivation can be constructed using the voltage–second balancing principle, wherein the inductor energy storage is zero for each switching cycle in the steady state and the inductor current is constant, that is, the inductor current changes to zero for each switching cycle:

\[
\overline{V_L(t)} = L \frac{di_L(t)}{dt}
\]

\[
\int_0^{T_s} v_L(t) \, dt = \int_0^{T_{on}} v_L(t) \, dt + \int_{T_{on}}^{T_s} v_L(t) \, dt
= v_L T_{on} + v_L (T_s - T_{on})
= 0
\]

Hence, Equation (5) is obtained. Then, Equations (1) and (2) are brought in, and Equation (6) is obtained, which indicates that the output voltage can be regulated by \(d_1\) and \(d_2\). Because \(d_1\) and \(d_2\) can be controlled independently, the four-switch buck–boost converter has various control schemes.

\[
\overline{V_A} = \overline{V_B}
\]

\[
V_o = \frac{d_1}{1 - d_2} V_{in}
\]

As the MOSFETs allow current to flow in both directions, the circuit runs forward when current travels from the power supply to the load. It is in forward buck mode if the output voltage is lower than the supply voltage. As \(d_2\) should be as tiny as feasible [14], the minimum \(d_2\) is equal to zero. Meanwhile, this also enables the system output to be lower than the input voltage. In this scenario, the four-switch buck–boost functions in buck mode. If asynchronous rectification is chosen, then Q1 is controlled by \(d_1\), Q2 is in the disconnected state throughout the switching cycle (conducted by the parallel diode), Q3 is on, and Q4 is open. Thus, the use of MOSFET for Q2 conduction greatly reduces the conduction loss; thus, the synchronous rectification method should be used.

When the output voltage is close to the input voltage, the circuit has a brief transition state between the buck and boost modes, in which the four MOSFETs turn on and off in a switching cycle. This helps to smooth the transition from buck mode to boost mode. However, because this mode’s lifespan is so brief, the associated loss is also minimal.
The circuit enters forward boost mode when the output voltage is much higher than the input voltage. Q3 and Q4 are controlled by $d_2$ and $(1 - d_2)$, respectively, whereas Q1 and Q2 remain unchanged.

The circuit is in reverse buck mode when current flows back from the load to the supply side and the output voltage is higher than the supply voltage. Although the current direction is different, reverse buck mode and forward boost mode are actually rather similar. Similarly to the above, there is a brief buck–boost mode as a transition. And then, the circuit enters reverse boost mode when the output voltage is significantly less than the input voltage.

2.2. PI–P Feedback

A dual closed-loop control has been proposed to improve the dynamic characteristics of the system and increase the accuracy with which the output can follow the reference waveform changes. Because the design in this study is a voltage-based PWM converter, it is ultimately necessary to control the change in the duty cycle, that is, to control the increase or decrease in the output voltage. Therefore, by adding a current loop, this duty cycle adjustment process makes the result more appropriate, and the current loop can also play the role of current limiting [15].

Specifically, it consists of an outer loop that is used to control the voltage and an inner loop that is used to control the current; this combination is called a voltage and current dual closed loop. The voltage outer loop consists of the output voltage as input, and the current inner loop uses the inductor current as input. Together with the PID, they form a feedback control system. This not only improves the stability and dynamic characteristics of the system, but also ensures safe operation of the system. In the system, the voltage loop utilizes Proportional–Integral (PI) compensation to eliminate steady-state errors, enhancing both steady-state accuracy and system stability. The current loop, by regulating the inductor current, further augments this system stability. However, introducing PI control into the current loop would increase the system order, potentially compromising its stability and reliability. Figure 4 shows a simplified schematic diagram.

![Figure 4. Voltage and current dual closed loop.](image_url)

3. Stability Analysis and Simulation

3.1. Root–Locus Diagram

According to the transfer function in Equation (7) and the system block diagram shown in Figure 5, the open-loop transfer function $G_3(s)$ of the system can be obtained [16], where $G_1(s)$ denotes the voltage regulator’s transfer function (PI), $G_2(s)$ denotes the current regulator (P), $G_{id}(s)$ denotes the duty cycle’s transfer function to the inductor current, and $G_{vi}(s)$ denotes the inductor current’s transfer function to the output voltage. The root trajectory of the system can then be plotted, using MATLAB for further analysis.
After an in-depth analysis of the system’s transfer function, it is revealed to be a fourth-order system with four poles. However, only two dominant poles have a significant impact on the system’s performance. As a result, it can be simplified to a second-order system. Within a second-order system, the typical optimal damping ratio is 0.707. With a damping ratio of 0.707, the system’s frequency response exhibits a relatively gentle rise and fall slope, endowing the system with favorable frequency characteristics.

The changes to the root trajectory of $P_v$, with initial parameters $P_i = 8$ and $I_v = 100$, are shown in Figure 6a. When the value of $P_v$ is less than 146, the root trajectory is located on the left-hand side of the s-plane and the system is stable at this time. As $P_v$ increases, damping decreases, and, to obtain more suitable damping, the value of $P_v$ can be determined to be in the range of 0.4.

The root trajectory of the $I_v$ variation, with initial values $P_v = 0.5$ and $P_i = 8$, is shown in Figure 6b. Again, the value of $I_v$ is chosen under the assumption that the system is stable and well-damped. However, a larger value of $I_v$ leads to a stronger integral effect of the controller, which can accelerate elimination of the steady-state error in the system. The range of 150 is used to determine the value of $I_v$.

The changes to the root trajectory of $P_i$, with starting parameter values of $P_v = 0.5$ and $I_v = 100$ is shown in Figure 6c. The dominant pole gradually moves away from the origin as $P_i$ increases within a certain range, and system performance improves. The value range of $P_i$ is determined to be approximately 16, according to the case of better damping, because the root route is entirely located on the left-hand side of the s-plane.
3.2. Simulation

Each parameter still has a range of values that satisfy the constraint of stability, and various values have various effects on the system, which are categorically explained below and validated in a simulation carried out using Matlab with the circuit shown in Figure 1. The first category is how the system is impacted by the voltage outer loop’s scale factor. Because it is difficult to multiply a fraction in a digital circuit implementation but easy to obtain the negative power of 2 by simply shifting to the right, the scale factor of the outer voltage loop is set to 0.25, 0.5, or 1. Table 2 shows the actual output voltage and THD for various scale factors of the outer voltage loop when the driving requirement is 100 nF load capacitance, 200 Vpp driving voltage, and 100 Hz waveform frequency. From this, the THD decreases significantly as the scale factor of the voltage outer loop increases, which is in line with the fact that a larger scale factor leads to faster correction of deviation, but the maximum voltage does not have a particularly obvious change pattern.

Table 2. Comparison of simulation results of scale factors for different voltage outer loops.

<table>
<thead>
<tr>
<th>Voltage Outer Loop Proportionality Factor</th>
<th>Actual Voltage (Vpp)</th>
<th>THD</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25</td>
<td>190</td>
<td>1.75%</td>
</tr>
<tr>
<td>0.5</td>
<td>198</td>
<td>0.96%</td>
</tr>
<tr>
<td>1</td>
<td>196</td>
<td>0.74%</td>
</tr>
</tbody>
</table>

For a system driven with a 100 nF load capacitance, 200 Vpp driving voltage, and 100 Hz waveform frequency, Table 3 displays the actual output voltage and THD for various voltage outer loop integration factors. It is clear from the table that the voltage outer loop integration factor has little bearing on the system’s output. In voltage loop control, integral compensation can eliminate steady-state errors. However, an excessively large integral term might lead to issues such as integral saturation, integral wind-up, system overshoot, and prolonged system response times. Conversely, if the integral term is too small, significant steady-state errors may arise. Therefore, a relatively suitable value of the integral term is chosen.

Table 3. Comparison of simulation results of integration coefficients for different voltage outer loops.

<table>
<thead>
<tr>
<th>Voltage Outer Loop Integration Factor</th>
<th>Actual Voltage (Vpp)</th>
<th>THD</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>198</td>
<td>0.96%</td>
</tr>
<tr>
<td>150</td>
<td>197</td>
<td>1.06%</td>
</tr>
<tr>
<td>300</td>
<td>198</td>
<td>1%</td>
</tr>
</tbody>
</table>

Finally, for the proportionality coefficient of the current inner loop, Table 4 shows the actual output voltage and THD corresponding to various proportionality coefficients of the current inner loop when the driving requirement is 100 nF load capacitance, along with 200 Vpp driving voltage and 100 Hz waveform frequency. From the table, as the integration coefficient of the circuit’s inner loop increases, the output result of the system deteriorates, and a larger the proportionality coefficient is not better.

Table 4. Comparison of simulation results for different scale factors of the current inner loop.

<table>
<thead>
<tr>
<th>Current Inner Loop Proportionality Factor</th>
<th>Actual Voltage (Vpp)</th>
<th>THD</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>198</td>
<td>0.96%</td>
</tr>
<tr>
<td>12</td>
<td>194</td>
<td>1.02%</td>
</tr>
<tr>
<td>16</td>
<td>192</td>
<td>1.21%</td>
</tr>
</tbody>
</table>

A simulation was run for the four-switch buck-boost-based drive system proposed in this paper, where the PI-P settings that provided the best THD effects were chosen from Tables 2–4. The output voltage peaked near 198 V and the signal’s THD was 1.42% when
the input voltage was 3.3 V while driving a 100 nF capacitor with a reference waveform of 200 Vpp and a 200 Hz digital sine wave, as illustrated in Figure 7a.

The reference waveform frequency decreased to enhance the THD because the vibration strength caused by high voltage was more noticeable than that caused by high frequency in terms of intuitive vibration feeling. The output peak-to-peak voltage was close to 198 V; the reference waveform was a 200 Vpp, 100 Hz digital sine wave signal; and the signal’s THD was 0.74%, as shown in Figure 7b.

The input voltage was increased from 3.3 V to 12 V, and use of the proposed approach on a vehicle was simulated. The reference waveform was still a 200 Vpp, 100 Hz digital sine wave signal, and the capacitive load was changed to 1 F because the vehicle application had a large capacitive load. The peak-to-peak output voltage was close to 192 V and the THD of the detected signal was 1.2%, as shown in Figure 7c.

In addition to producing sine waves, the driver is also capable of producing triangle waves. A 200 Vpp, 100 Hz triangle wave with output voltage peaks close to 98 V and 196 V is shown in Figure 8a as an example. Additionally, as illustrated in Figure 8b, the driver can mix a sine wave and triangular wave.
The input reference waveform’s amplitude and frequency were changed, and then a simulation was attempted with various piezoelectric ceramic sizes. Small ceramic capacity is typically used in low-power products, such as portable products, whereas large ceramic capacity is typically used in high-drive products, such as automotive products. Additionally, varying the output waveform’s amplitude and frequency can produce various vibration effects and improve the vibratory feedback sensation. Table 5 presents the findings. The drive voltage and frequency were appropriately reduced, to allow the system to handle the load as it grew. As the load increased, the output waveform became more distorted.

Table 5. Simulation results for different cases.

<table>
<thead>
<tr>
<th>Ceramic Capacities (µF)</th>
<th>Drive Voltage (Vpp)</th>
<th>Waveform Frequency (Hz)</th>
<th>THD</th>
<th>Actual Voltage (Vpp)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>200</td>
<td>&lt;=100</td>
<td>0.96%</td>
<td>198</td>
</tr>
<tr>
<td>0.1</td>
<td>200</td>
<td>&lt;=200</td>
<td>1.74%</td>
<td>197</td>
</tr>
<tr>
<td>0.2</td>
<td>180</td>
<td>&lt;=200</td>
<td>1.60%</td>
<td>176</td>
</tr>
<tr>
<td>0.4</td>
<td>150</td>
<td>&lt;=150</td>
<td>2.00%</td>
<td>148</td>
</tr>
<tr>
<td>0.8</td>
<td>150</td>
<td>&lt;=120</td>
<td>2.60%</td>
<td>118</td>
</tr>
<tr>
<td>1</td>
<td>120</td>
<td>&lt;=200</td>
<td>2.70%</td>
<td>118</td>
</tr>
<tr>
<td>2.2</td>
<td>120</td>
<td>&lt;=150</td>
<td>4.40%</td>
<td>118</td>
</tr>
<tr>
<td>3.6</td>
<td>100</td>
<td>&lt;=150</td>
<td>3.24%</td>
<td>99</td>
</tr>
<tr>
<td>4.4</td>
<td>100</td>
<td>&lt;=120</td>
<td>3.18%</td>
<td>99</td>
</tr>
</tbody>
</table>

4. Implementation and Measured Comparison

4.1. System Implementation

The system is divided into two parts: the driver circuit and the digital feedback control; the driver circuit was built with discrete devices, and feedback control was implemented using an FPGA.

In this study, a Zynq-7010 FPGA chip was used for implementation. To ensure that the THD of the output waveform remained within acceptable bounds and to circumvent excessive energy losses, the controller was configured to set the ADC sampling frequency at 1 MHz, aligned with the system’s switching frequency of 1 MHz. A diminished switching frequency could lead to a compromised THD in the output waveform. Conversely, an excessively high switching frequency might escalate the system’s energy consumption, thereby diminishing efficiency. The Zynq-7010 chip has a dual 12-bit sampling rate of 1 Mbps ADC, which met the design requirements, and its dual-channel nature meant that it could collect voltage and current signals simultaneously. The final verification of the entire system is shown in Figure 9.

At the same time, in the actual system tests, as shown in Figures 9 and 10, a piezoelectric actuator was connected. The test results met our expectations.

Figure 9. Hardware experimental platform.
4.2. Test Results and Comparison

As illustrated in Figure 10, the measured oscilloscope data were imported into MATLAB for examination. An output waveform is shown in Figure 10a for a load capacitance of 100 nF and reference waveform of a 150 Vpp, 100 Hz sine wave signal. The distortion level of the output waveform was lowered by a reduction in the voltage amplitude. The THD obtained from the analysis in Simulink was 12.50%.

A second output waveform is shown in Figure 10b for a load capacitance of 2.9 µF and reference waveform of an 80 Vpp, 90 Hz sine wave signal. The THD derived from the Simulink study was 2.75%.

Table 6 shows a comparison of the measured performance of the proposed design with other piezoelectric actuator drivers. In work (1), i.e., the case in which the reference waveform was 80 Vpp and 90 Hz, it drove a larger load capacitor and, thus, could be used under high driving requirements. When work (2) was used to increase the output voltage when driving a small-load capacitor, there was a larger THD, so the THD needs to be further optimized.

Table 6. Performance comparison.

<table>
<thead>
<tr>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage (V)</td>
<td>3.6</td>
<td>3.6</td>
<td>3.6</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Inductance value (µH)</td>
<td>100</td>
<td>4.7</td>
<td>10</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Load capacitance (µF)</td>
<td>0.1</td>
<td>0.1</td>
<td>0.68</td>
<td>2.9</td>
<td>0.1</td>
</tr>
<tr>
<td>Frequency (Hz)</td>
<td>150</td>
<td>150</td>
<td>130</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>Output voltage (Vpp)</td>
<td>100</td>
<td>100</td>
<td>80</td>
<td>80</td>
<td>150</td>
</tr>
<tr>
<td>THD (%)</td>
<td>0.33</td>
<td>1.12</td>
<td>1</td>
<td>2.75</td>
<td>14.14</td>
</tr>
</tbody>
</table>

5. Conclusions

In this paper, a four-switch buck–boost and voltage–current dual closed-loop piezoelectric actuator driver was proposed. The model’s stability was analyzed, the PI controller’s
parameter range was determined, and the effects of the PI controller parameters on the system’s output waveform were discussed. The simulation results, obtained using Simulink, show that the peak-to-peak voltage can reach up to 200 V, and the highest frequency can reach 200 Hz. The THD is below 1%, demonstrating the feasibility of the theoretical design. In the FPGA experiment, the driver can achieve a peak-to-peak voltage of 80 V and THD of 2.75% when driving a large-load capacitor of 2.9 µF. When driving a 100 nF capacitor, the peak-to-peak voltage reaches 200 V, demonstrating its capability to drive large-load capacitors and generate high-voltage outputs.

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References

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