

Article

Design and Real-Time Validation of a Three-Phase Inverter Using an Interleaved Synchronous Super-Lift Luo Converter for Aircraft Power Systems

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Abstract

This paper examines a 24 kVA three-phase inverter supplied by a set of four synchronous Super-Lift Luo DC–DC converters (ISSLLC) connected in parallel to a common DC link. The converters boost a 28 V DC input to approximately 400 V, which then feeds a 115 V, 400 Hz inverter intended for aircraft electrical systems. The overall system was modeled analytically, simulated using PLECS, and validated in real time on a Typhoon HIL platform. In both simulation and HIL, the DC link remained low ripple, and the inverter delivered well-balanced three-phase output voltages. The measured total harmonic distortion was 0.77%, and the power factor was close to unity, staying within MIL-STD-704F limits. The agreement between the simulation and HIL results confirms the precision and real-time feasibility of the proposed ISSLLC-based inverter for aerospace and other high-gain, high-efficiency applications.

Keywords: Super-Lift Luo converter; interleaved converters; aircraft power systems; three-phase inverter; high-gain DC–DC conversion; hardware-in-the-loop simulation

1. Introduction

Size and weight are critical design considerations in the aviation industry, where compact solutions with equivalent performance are generally favored despite higher costs. Using 400 Hz instead of the common 50/60 Hz AC frequency greatly reduces the size of passive components. As a result, power supplies, motors, transformers, and inverters have smaller dimensions, and power transmission lines are reduced. Following the Second World War, the aerospace industry set 400 Hz as the standard frequency, and this continues with the US Military Standard MIL-STD-704F [1,2]. Today, because of the increased use of electronic devices in modern aircraft, nonsymmetrical and nonlinear loads are common in avionics systems. This increase has triggered more complex harmonic generation and made power control more complex [3]. Moreover, the evolving need for control in aerospace systems has required advanced control approaches with higher bandwidth to effectively manage these complex loads [4]. Recent aerospace-oriented inverter studies have therefore focused on compact, high-frequency AC power systems operating at 400 Hz, with particular emphasis on power density, harmonic mitigation, and compliance with aircraft power quality standards. Multilevel inverter structures for aircraft ground power and propulsion applications have been reported to enhance waveform quality, reduce switch count, and maintain compliance with aircraft power-quality standards [5–7]. Compact GaN-based



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inverter implementations for 115 V, 400 Hz avionic systems have also demonstrated high efficiency and lightweight realization [8]. Resonant and isolated single-stage inverter architectures have further been proposed to reduce component count and switching losses while maintaining galvanic isolation in aerospace platforms [9]. These developments highlight the ongoing effort toward compact and high-performance inverter solutions for modern aircraft systems.

This paper presents an innovative solution to the efficiency, weight, and harmonic distortion problems faced by conventional aircraft power systems. The main contribution of this study is not limited to system-level integration. The novelty lies in the application of an interleaved synchronous Super-Lift Luo DC–DC converter to a high-power 400 Hz three-phase aerospace inverter, combined with analytical modeling and stability verification of the overall system. Unlike conventional boost-based or transformer-isolated solutions, the proposed structure achieves high voltage gain with reduced DC-link ripple and low harmonic distortion, while maintaining a transformerless and weight-efficient architecture suitable for aviation applications. This system is particularly relevant in the context of the More Electric Aircraft (MEA) initiative, which aims to replace traditional hydraulic and pneumatic systems with electrical systems to improve performance and reduce maintenance needs [10]. Within this framework, high step-up and weight-optimized inverter architectures have been investigated for high-frequency aircraft power systems [11]. The proposed interleaved synchronous Super-Lift Luo converter (SLLC)-based 24 kVA three-phase inverter is characterized by high power density and low harmonic distortion (<2%). The stability of the system is theoretically proven by state-space modeling and experimentally verified by PLECS simulations and Typhoon HIL tests. Similar trends toward high-density and experimentally validated inverter solutions for aerospace and aircraft ground power applications have been reported in recent literature, highlighting the relevance of compact converter–inverter architectures for modern avionics systems. The findings provide a scalable solution suitable for both existing auxiliary power units (APUs) and the integration of renewable energy sources.

The interleaved design helps reduce the ripple of the input current, which is crucial to maintain a stable power supply in aircraft systems [12,13]. The interleaved topology of the DC–DC converter significantly reduces the input current ripple, as demonstrated by Denholm et al. [14]. Their proposed interleaved two-channel design achieves a peak-to-peak input current ripple of less than 1.5%, which minimizes fuel cell degradation and improves system reliability. This characteristic is particularly advantageous for inverters that require a stable DC-link voltage with low ripple.

The design of interleaved converters also allows for better thermal management and reduced electromagnetic interference [15–17]. Interleaved DC–DC converters exhibit superior thermal performance compared to conventional topologies, as demonstrated by Alavi et al. [15]. Their analysis shows that the floating interleaved boost converter achieves significantly lower junction temperatures (e.g., 62 °C for IGBTs) due to reduced current stress per channel, enhancing reliability and lifespan. Such thermal and EMI advantages are particularly critical in aerospace environments, where stringent reliability and electromagnetic compatibility requirements must be satisfied.

Systems using interleaved converters have achieved efficiencies that exceed 96% to 98% due to optimized switching and conduction strategies [18–20]. However, potential disadvantages include increased complexity in control strategies and design, which may complicate implementation in aircraft inverters [21]. Consequently, practical realization of interleaved architectures requires careful coordination between control design, real-time implementation, and hardware constraints.

Interleaved topologies allow for better current sharing among channels, which reduces the size of filter inductors and capacitors [22,23], thus improving the power density of the inverter. The use of a single inductor in some interleaved inverter designs simplifies the architecture while maintaining a high power density [24]. However, efficiency issues may arise in this type of interleaved topology. For instance, a study demonstrated an interleaved converter achieving 94.6% efficiency at full load [25] while another study, which has a different kind of interleaved topology, achieved a peak efficiency of 95.6% [26]. These results indicate that the choice of interleaving strategy and component configuration directly influences efficiency and scalability in high-power inverter systems.

The Super-Lift Luo converter is an advanced DC-DC converter derived from the buck-boost converter, designed to efficiently elevate low photovoltaic voltage to a higher level with minimal voltage and current ripple, and has recently gained attention in high step-up and high power-density power conversion research, making it suitable for various applications [27–30]. Simulations have also been carried out for electric vehicle applications as DC-DC converters, resulting in increased efficiency and reduced voltage fluctuations [31,32]. However, despite its favorable electrical characteristics, its application in aerospace power systems has received very limited attention. Similarly, the literature contains no studies on aviation using the Super Lift Luo converter other than simulations [33].

The design and development of a three-phase 24 kVA inverter with an interleaved synchronous Super-Lift Luo converter for aeronautical power systems involves integrating high-power conversion technologies to meet the specific needs of aerospace applications. The system aims to maximize efficiency, reduce ripple, and ensure high-performance stability in various operating conditions. This work therefore addresses a clear gap in the existing literature by extending the application of the Super-Lift Luo converter toward aerospace-grade inverter systems validated under real-time operating conditions.

2. Methodology

2.1. Super Lift Luo Converter

The Super-Lift Luo converter (SLLC) is a transformerless DC-DC converter topology that uses a step-up voltage conversion mechanism to achieve high voltage gain. Built on the classic Luo converter family, this structure adds an additional voltage-boosting capacitor stage, as shown in Figure 1, to geometrically increase the output voltage. As a result, higher output voltages can be achieved at lower switching rates (duty cycle) compared to traditional boost or Luo converters.

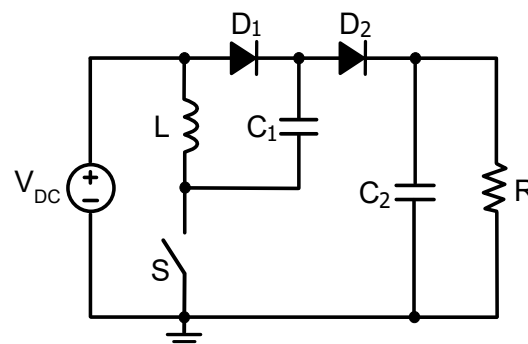


Figure 1. Circuit diagram of the Super-Lift Luo converter.

Figure 1 illustrates the main functional elements of the proposed SLLC stage. The input inductor L provides energy buffering and shapes the input current, enabling continuous-energy transfer between switching intervals. The capacitors C_1 and C_2 act as voltage-lift (energy storage) capacitors: they are charged during the appropriate switching state and

then series-assist the input source during energy transfer, thereby achieving high step-up gain while reducing voltage/current ripple. The diode(s) in the power path ensure unidirectional energy transfer and provide electrical isolation between the output and the source during the charging interval. Finally, the active switch (or synchronous switch) governs the two operating states and controls the energy flow, while the output-side filter capacitor maintains the DC-link/output voltage by attenuating switching ripple.

The SLLC has a structure that operates with two switching states. When the switch is closed, the input voltage charges both the inductor and the voltage boost capacitor, while the output side is isolated from the circuit via a diode. When the switch is in the open position, the energy stored in the inductor is released and combined with both the input voltage and the previously charged capacitor to be transferred to the output. In this way, the system manages to increase the output voltage without using a transformer. This architecture eliminates the disadvantages associated with transformers, such as weight, volume, and electromagnetic noise, making it particularly suitable for applications requiring high efficiency, low EMI, and compact design, such as aviation. In continuous conduction mode (CCM) and under ideal conditions, the voltage gain of the SLLC used in this study is given by the following Equation (1);

$$\frac{V_o}{V_{in}} = \frac{2 - D}{1 - D} \quad (1)$$

where V_o is the output voltage, V_{in} is the input voltage, and D is the duty cycle. This gain expression defines the relationship between the converter's duty cycle value and the output voltage, and demonstrates the basic operating principle of the system. However, this theoretical gain can only be achieved in practice if the appropriate component values are selected. Therefore, the correct sizing of the passive elements in the Super-Lift Luo converter topology is critical for both obtaining the desired output voltage and ensuring stable and efficient operation of the system.

In this context, it is necessary to first size the super-lift capacitor (C_1) responsible for energy transfer. These capacitors carry high currents during the switching period by entering a charge-discharge cycle and directly affect the system gain. The value of these capacitors can be calculated using the following Equation (2), depending on the average current passing through them, the switching frequency, and the allowed voltage ripple:

$$C_1 = \frac{I \cdot D}{f_s \cdot \Delta V_C} \quad (2)$$

The C_2 capacitor at the output performs the system's filtering function and reduces high-frequency oscillations in the output voltage by damping sudden changes in the load current. A similar formula is used for this capacitor, but the current and voltage variables in the formula are redefined according to the system's output values as I_{out} and ΔV_o for the calculation.

Finally, the inductor value (L) is determined by the following Equation (3) to ensure that the converter operates in continuous conduction mode and to limit current oscillations:

$$L_1 = \frac{V_{in} \cdot D}{f_s \cdot \Delta I_L} \quad (3)$$

These formulas provide a reference for choosing the elements used in the converter in a systematic way and can be adapted to specific application requirements and design tolerances.

2.2. Interleaved and Synchronous Operation

The structure shown in Figure 2 features an interleaved power conversion structure consisting of four Super-Lift Luo-type DC-DC converters. These converters operate using

synchronous switching logic, and the output of each is connected to a common DC bus line. The structure is based on the principle of four parallel converters that target the same voltage level, which are activated sequentially with a defined switching-phase displacement.

Each switch group is triggered with a time delay of one-fourth of the carrier period (90° electrical phase), thereby spreading the input current of the four converters over time and improving the system's overall voltage and current profile. It should be noted that the control signal waveforms illustrated in Figure 2 are intended to describe the operating principle and switching sequence of the proposed control strategy. In practice, by using an appropriate switching device, correct gate-driving circuitry, and a real-time controller with sufficient bandwidth, the control signals can closely approach the depicted waveforms. Nevertheless, minor deviations from the ideal shapes may occur due to sampling delays, quantization effects, and non-ideal switching behavior in real-time implementations such as HIL experiments. These deviations do not affect the correctness of the switching operation or the overall control performance.

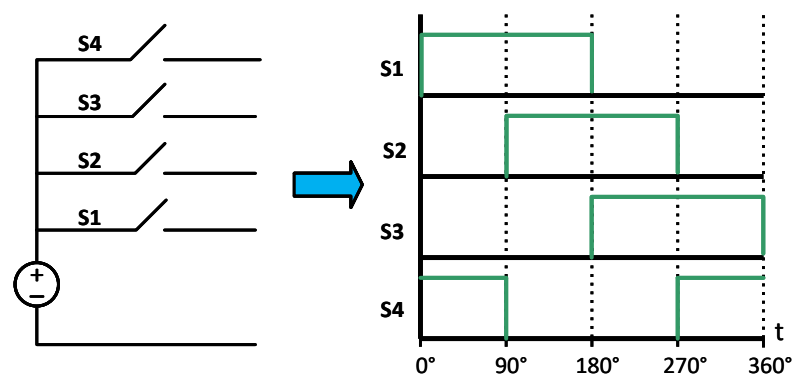


Figure 2. Four-channel interleaved operation. The time axis is normalized in degrees. 360° corresponds to one full switching period (T).

This temporal distribution provided by the interleaved topology reduces sudden current changes caused by switching and suppresses both electromagnetic interference (EMI) effects and output fluctuations by reducing the amplitude of high-frequency harmonic content. Additionally, synchronous rectification is achieved by using MOSFETs instead of diodes in each converter, which reduces transmission losses and increases system efficiency. The time-spreading of each converter's duty cycle also balances thermal load sharing, reducing thermal stress on components and enhancing system reliability in the long term. The ripple-minimizing effect is represented in Figure 3 and is investigated in the Section 3.

Interleaving the converter reduces input current ripple (see Figure 3) while increasing the effective switching frequency at the DC link. As a result, the size of the passive components can be reduced without adversely affecting system stability. Such features are particularly relevant for aircraft electrical power systems, where strict limitations on weight, volume, and thermal performance apply. Moreover, sharing the current among interleaved phases leads to a more uniform thermal profile and lowers the electrical stress on individual semiconductor devices. In the context of 400 Hz aerospace power systems, the proposed interleaved SLLC-based structure therefore offers a practical balance between compactness, efficiency, and reliable DC-link operation under varying load conditions, while preserving fault-tolerant operation through the interleaved structure.

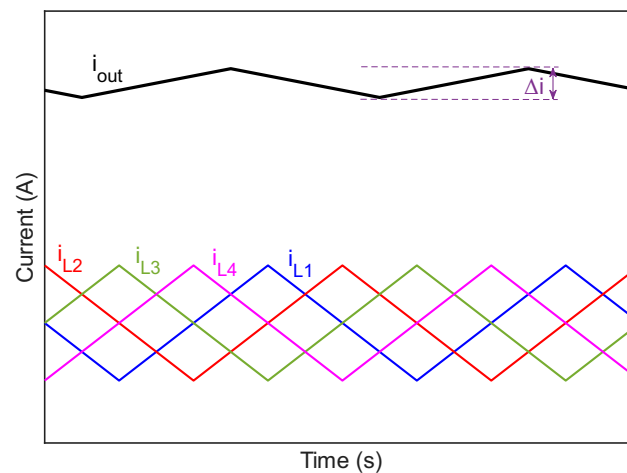


Figure 3. Four-channel interleaved operation ripple minimization.

2.3. Control Design

The control strategy for the proposed Interleaved Synchronous Super-Lift Luo converter (ISSLLC) is based on a small-signal dynamic model. For control design, it is necessary to determine how small changes in the duty ratio affect the output voltage. This sensitivity is obtained by differentiating the equation given in Equation (1) with respect to D as represented in Equation (4);

$$\frac{\partial V_o}{\partial D} = \frac{V_{in}}{(1-D)^2} \quad (4)$$

This derivative represents the DC gain of the small-signal control-output transfer function. When passive elements L , C_1 , and C_2 are included in the average state-space model and linearized around the operating point, the following general form is obtained as displayed in Equation (5):

$$G_{vd}(s) = \frac{V_{in}}{(1-D)^2} \cdot \frac{1 + s \cdot \frac{L}{R(1-D)^2}}{1 + s \cdot \left[\frac{L}{R(1-D)^2} + \frac{C_1 R}{1-D} \right] + s^2 \cdot \frac{L(C_1 + C_2)}{(1-D)^2}} \quad (5)$$

Based on this model, a PI (proportional–integral) controller was designed to regulate the output voltage. The PI structure was selected to ensure zero steady-state error for step changes in load or reference, while providing sufficient phase margin for stable operation. The proportional term shapes the loop gain to achieve the desired crossover frequency, and the integral term increases the low-frequency gain to eliminate steady-state error.

The controller parameters were selected to ensure stable operation and sufficient robustness of the overall system. A bandwidth separation strategy was adopted, in which the inner current control loops were designed with a significantly higher bandwidth than the outer voltage control loop, thereby minimizing loop interaction and ensuring adequate phase margin. The controller design is based on the derived small-signal model of the proposed converter, and stability is verified through time-domain simulations and real-time HIL experiments. Furthermore, the controller tuning explicitly accounts for the location of the dominant double pole ω_0 and the right-half-plane zero $\omega_{z,RHP}$, with the crossover frequency selected to be below 20% of $\omega_{z,RHP}$ to preserve closed-loop stability.

3. Results

This section presents the results of a 24 kVA three-phase inverter system based on the ISSLLC. The section provides a description of the converter and inverter design, the component selection process, and the control strategy used. Simulation studies conducted in the PLECS environment analysed the steady-state and dynamic performance of the system under different operating conditions, and the simulation results were verified in real time through hardware-in-the-loop validation tests conducted on the Typhoon HIL platform. The comparison of interleaved and noninterleaved structures focuses on output voltage stability and ripple reduction.

3.1. Simulations

To verify the analytical design presented in Section 2, the proposed interleaved synchronous Super-Lift Luo converter was modelled in PLECS. The simulation setup replicates the target operating conditions of the aircraft electrical system, including the high step-up requirement from a low-voltage DC source to the regulated DC bus feeding a three-phase inverter. All passive and active component values were determined according to the design equations in the previous section, ensuring consistency between analytical predictions and simulation results.

3.1.1. Circuit Design

The proposed DC–DC conversion stage is implemented as a four-channel interleaved synchronous Super-Lift Luo converter to achieve the high step-up ratio required for converting $V_{in} = 28$ V DC to $V_{out} = 400$ V DC. In the interleaved configuration, each channel shifts 90 degrees to reduce the ripple in both the input and output currents, increase the response time, and evenly distribute the thermal stress across the switching devices. The use of synchronous MOSFET switches instead of diodes minimises conduction losses and improves overall efficiency, particularly at high output voltages. Figure 4 shows the complete schematic of the converter.

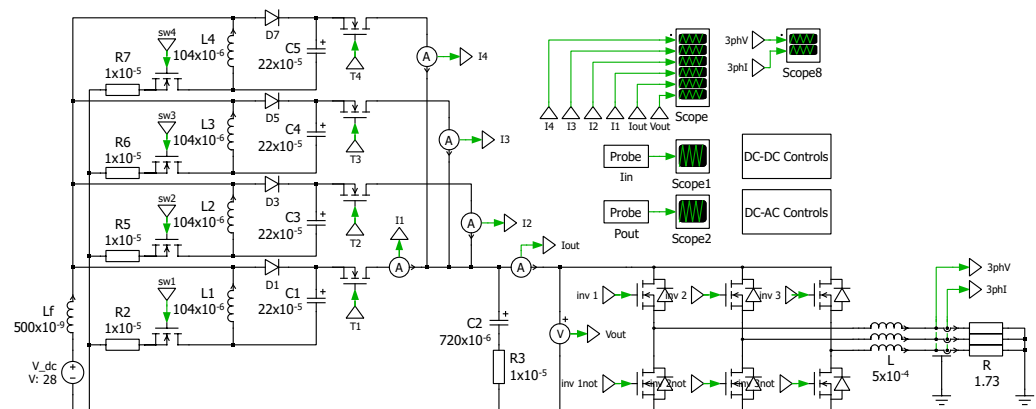


Figure 4. Simulation topology of the inverter showing the four interleaved DC–DC converters and the 3-phase inverter stages.

Each channel comprises an input inductor $L_{1,2,3,4} = 104 \mu\text{H}$, a primary lift capacitor $C_{1,3,4,5} = 220 \mu\text{F}$, and a bulk output capacitor $C_2 = 2200 \mu\text{F}$. The interleaving effect reduces the equivalent inductance in the small-signal averaged model to Equation (6).

$$L_{eq} = \frac{L_{channel}}{N} = \frac{104 \mu\text{H}}{4} = 26 \mu\text{H} \quad (6)$$

where $N = 4$ is the number of channels. While the small-signal model uses L_{eq} the physical design retains the higher per-channel inductance value of $104 \mu\text{H}$ to suppress individual

channel current ripple, reduce peak inductor currents, and improve EMI performance. This also ensures that each inductor operates well below its saturation limit during transient load conditions.

The bulk output capacitor C_2 is sized to stabilise the DC bus voltage under load transients and to minimise low-frequency voltage ripple. The value of C_1 is determined based on voltage lift requirements and its role in shaping the converter's double pole and zero locations, as detailed in the analytical model in Section 2.

The load is modelled as the DC equivalent of the three-phase inverter's rated output. Given a per-phase resistance of $1.73 \, \Omega$ at $115 \, V_{\text{rms}}$, the total load power is approximately

$$P_{\text{total}} \approx 22.9 \, \text{kW}, \quad (7)$$

corresponding to an equivalent DC-side resistance of

$$R_{\text{dc}} = \frac{V_{\text{out}}^2}{P_{\text{total}}} \approx 6.9767 \, \Omega. \quad (8)$$

This load representation is used in both steady-state and small-signal simulations to ensure realistic voltage and current waveforms. In addition to the nominal rating point ($R_{\text{dc,nom}} = 6.98 \, \Omega$, corresponding to 22.9 kW at $115 \, V_{\text{rms}}$ per phase), a conservative operating point ($R_{\text{dc,test}} = 6.67 \, \Omega$) was intentionally employed in the load-transient and validation studies. This reflects the slightly elevated AC-side RMS voltage ($118\text{--}120 \, V_{\text{rms}}$) used to emulate practical conduction and switching losses, resulting in an active power of approximately 24 kW at near-unity power factor. The inverter apparent power rating remains at 24 kVA, and all results comply with MIL-STD-704F.

3.1.2. Control Design and Switching Models

The control strategy is implemented in two sequential stages: the front-end DC–DC converter and the back-end DC–AC inverter.

In the DC–DC stage, the converter employs a voltage-mode control scheme with a continuous *PI* (Proportional–Integral) controller. The output voltage is sensed and scaled by a gain factor of $1/400$, producing the feedback signal. This is compared with the reference command to generate the error signal e , which is processed by the *PI* controller as seen in Equation (9) below.

$$PI(s) = K_p + \frac{K_i}{s}, \quad (9)$$

with $K_p = 0.2$ and $K_i = 70$. The *PI* output u regulates the duty cycle command of the interleaved channels. To implement switching, the *PI* output is compared with a high-frequency triangular carrier waveform, generating PWM signals for synchronous operation of the four interleaved channels. Interleaving shifts the phase of each PWM signal by 90° , thereby reducing both input and output current ripple. Current feedback is additionally scaled ($10/915 \times 0.001$) to observe the summed inductor currents and verify current-sharing symmetry. This ensures robust operation under dynamic load conditions and suppresses EMI by distributing switching harmonics, as shown in Figure 5.

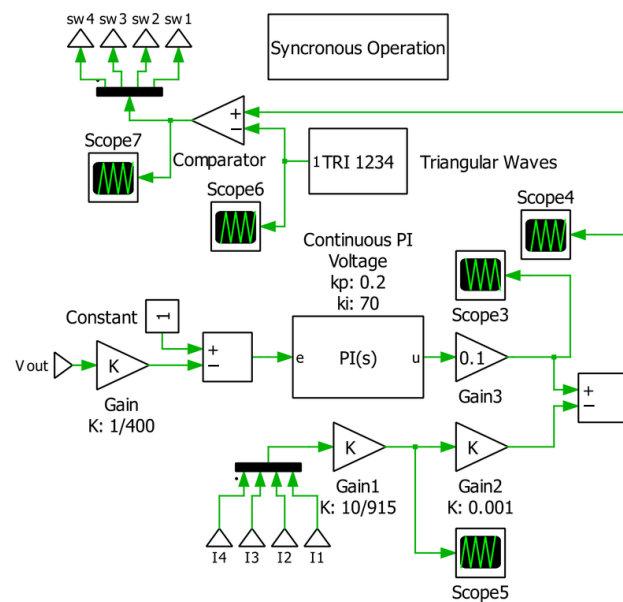


Figure 5. Control block diagram of the DC–DC converter stage.

In the DC–AC stage, the regulated DC bus is converted into a balanced three-phase AC output. The modulation strategy employs sinusoidal pulse-width modulation (SPWM), where three sinusoidal reference signals, phase-shifted by 120° , are compared against a high-frequency triangular carrier waveform ($f_c = 50$ kHz). The resulting comparator outputs generate the gate signals for the inverter switches, producing three-phase voltages at $f = 400$ Hz. Logical operators ensure that complementary switch pairs are driven with appropriate dead-time insertion to prevent shoot-through (Figure 6).

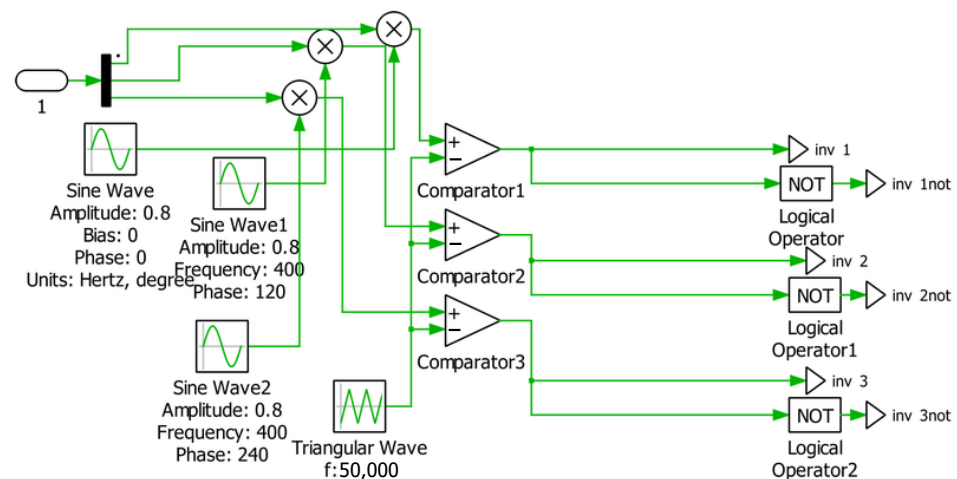


Figure 6. SPWM-based inverter modulation scheme.

A secondary feedback loop regulates the root-mean-square (RMS) values of the three-phase output voltages and currents. The RMS values of the line voltage and current are measured, scaled, and compared with their respective references. The resulting error is processed by a continuous PID controller of the form shown in Equation (9), with tuned gains of $K_p = 0.2$ and $K_i = 50$. The controller output adjusts the modulation index of the SPWM process, thereby maintaining the desired amplitude of the inverter's three-phase output under varying load conditions. This feedback structure is illustrated in Figure 7.

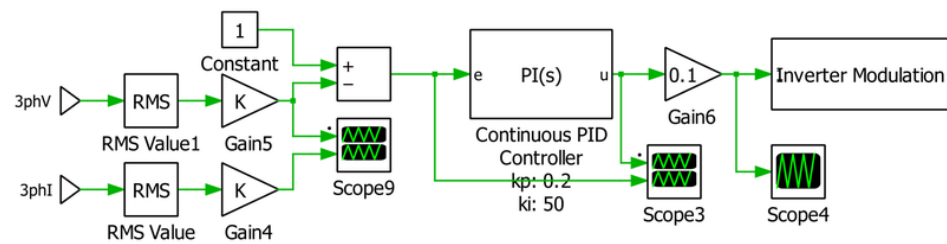


Figure 7. RMS feedback loop with continuous PID controller for the DC–AC stage.

The two control stages are interconnected through the regulated DC bus. The DC–DC converter ensures that the intermediate bus voltage remains stable under source and load disturbances, effectively decoupling the input supply from the inverter dynamics. This regulated DC bus then serves as the input to the DC–AC inverter stage, providing a stiff voltage source for high-quality AC waveform generation. In this way, the first stage establishes the required operating conditions for the inverter, while the second stage focuses on delivering sinusoidal three-phase voltages to the load in compliance with aerospace power quality standards.

3.1.3. DC–DC Stage Simulation Results

The simulation results of the DC–DC converter are summarised in Figures 8 and 9. The inductor currents in Figure 8 clearly demonstrate the effect of interleaving. During start-up (left), the four channel currents rise smoothly and reach steady state within approximately 0.25 s. According to MIL-STD-704F, airborne DC power buses must return to within $\pm 6\%$ of their nominal value within 0.5 s following a transient disturbance. The observed settling time is significantly faster than this requirement, indicating robust regulation. At steady-state (right), the channel currents are shifted by 90° , resulting in balanced current sharing and substantial ripple cancellation. The measured effective ripple current is reduced to about 0.6 A compared to the theoretical 2.5 A for a single-channel case, confirming the benefit of interleaving in both ripple reduction and EMI performance.

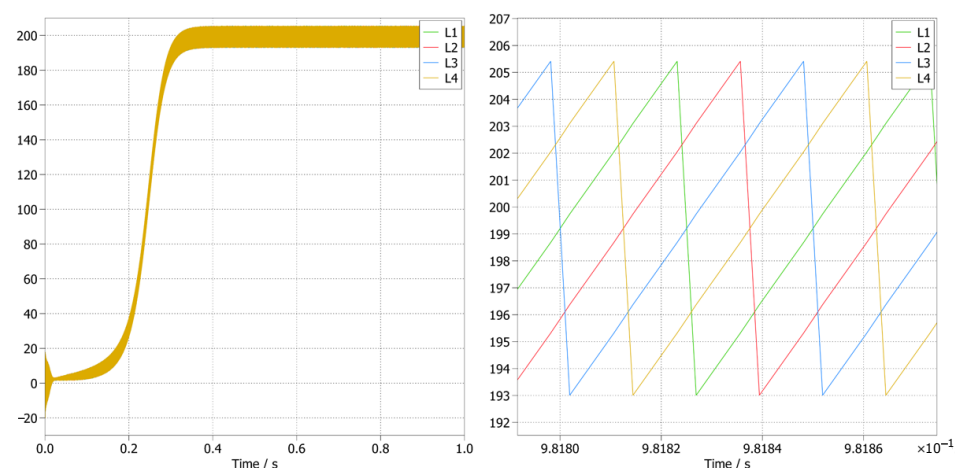


Figure 8. Inductor currents of the four interleaved channels: start-up transient (left) and steady-state interleaving (right).

The corresponding output voltage behaviour is shown in Figure 9. During start-up (left), the bus voltage settles at the reference value of 400 V in less than 0.25 s, which is well within the 0.5 s recovery window mandated by MIL-STD-704F. Under steady-state conditions (right), the measured ripple is approximately 0.9 V peak-to-peak, which is less than 0.03% of the nominal 400 V. This is more than an order of magnitude lower than the 1% ripple limit specified in MIL-STD-704F, thereby validating the design of the bulk output

capacitor and the interleaving scheme. These results confirm that the DC–DC converter provides a stiff and well-regulated DC bus, establishing the necessary operating conditions for the subsequent DC–AC inverter stage.

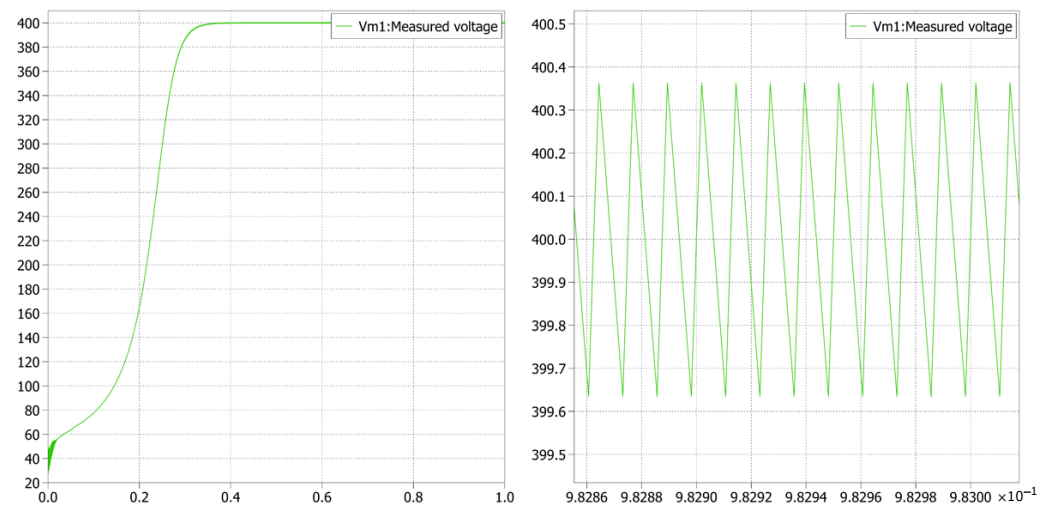


Figure 9. Output voltage of the DC–DC converter: start-up regulation (left) and steady-state ripple (right).

The output current ripple of the proposed four-channel interleaved converter was measured to be approximately 0.1 A. This reduction is due to the ripple cancellation effect of interleaving. For an N -channel interleaved converter, the effective ripple magnitude can be estimated as seen in Equation (10).

$$\Delta I_{\text{out}}(N) = \Delta I_{\text{channel}} \cdot \left| \frac{\sin(N\pi D)}{N \sin(\pi D)} \right|, \quad (10)$$

where D is the duty ratio and $\Delta I_{\text{channel}}$ is the inductor current ripple of a single channel. In the present case, $N = 4$ and the measured value is $\Delta I_{\text{out}} \approx 0.1$ A. Without interleaving ($N = 1$), the same converter operating at 20 kHz would exhibit a ripple of approximately $\Delta I_{\text{out}} \approx 0.4$ A. Thus, the interleaved structure reduces the effective current ripple by nearly a factor of four while simultaneously increasing the ripple frequency from $f_s = 20$ kHz to $Nf_s = 80$ kHz, greatly improving output filtering is shown in Figure 10.

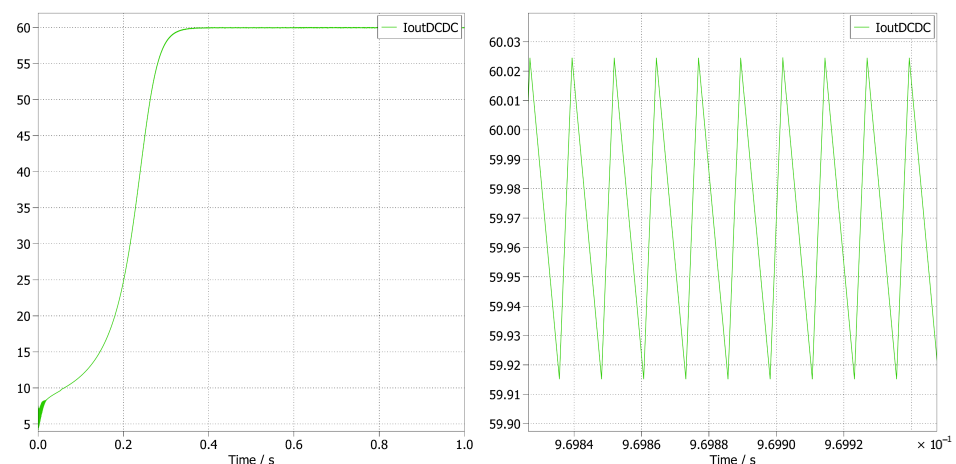


Figure 10. Output current waveform of the interleaved DC–DC converter, showing a ripple of approximately 0.1 A.

3.1.4. Load–Transient Performance

To assess the dynamic performance of the converter, single-step load changes were applied from the conservative test baseline $R_{eq} = 6.67 \, \Omega$ ($I_{FL} \approx 60 \, \text{A}$) to new load levels corresponding to $\pm 25\%$ and $\pm 50\%$ variations. The numerical results of the single-step transient tests are summarized in Table 1. After the step, the converter continued operation at the new steady-state load. The limits of MIL-STD-704F require the output voltage to recover within $\pm 6\%$ of nominal in less than 0.5 s.

Table 1. Single-step transient tests from nominal load.

Load Step	ΔI (%)	$R_{eq} \, (\Omega)$	Observed V_{out} Response
6.67 $\rightarrow$ 8.89	−25	8.89	$\approx 3\text{--}4\%$ undershoot, $t_{settle} \approx 0.20 \, \text{s}$
6.67 $\rightarrow$ 5.33	+25	5.33	$\approx 5\%$ overshoot, $t_{settle} \approx 0.25 \, \text{s}$
6.67 $\rightarrow$ 13.3	−50	13.3	$\approx 8\text{--}10\%$ undershoot, $t_{settle} \approx 0.30 \, \text{s}$
6.67 $\rightarrow$ 4.44	+50	4.44	$\approx 12\text{--}15\%$ overshoot, $t_{settle} \approx 0.35 \, \text{s}$

The graphical results are summarized in Figure 11, where the four panels correspond to the following cases:

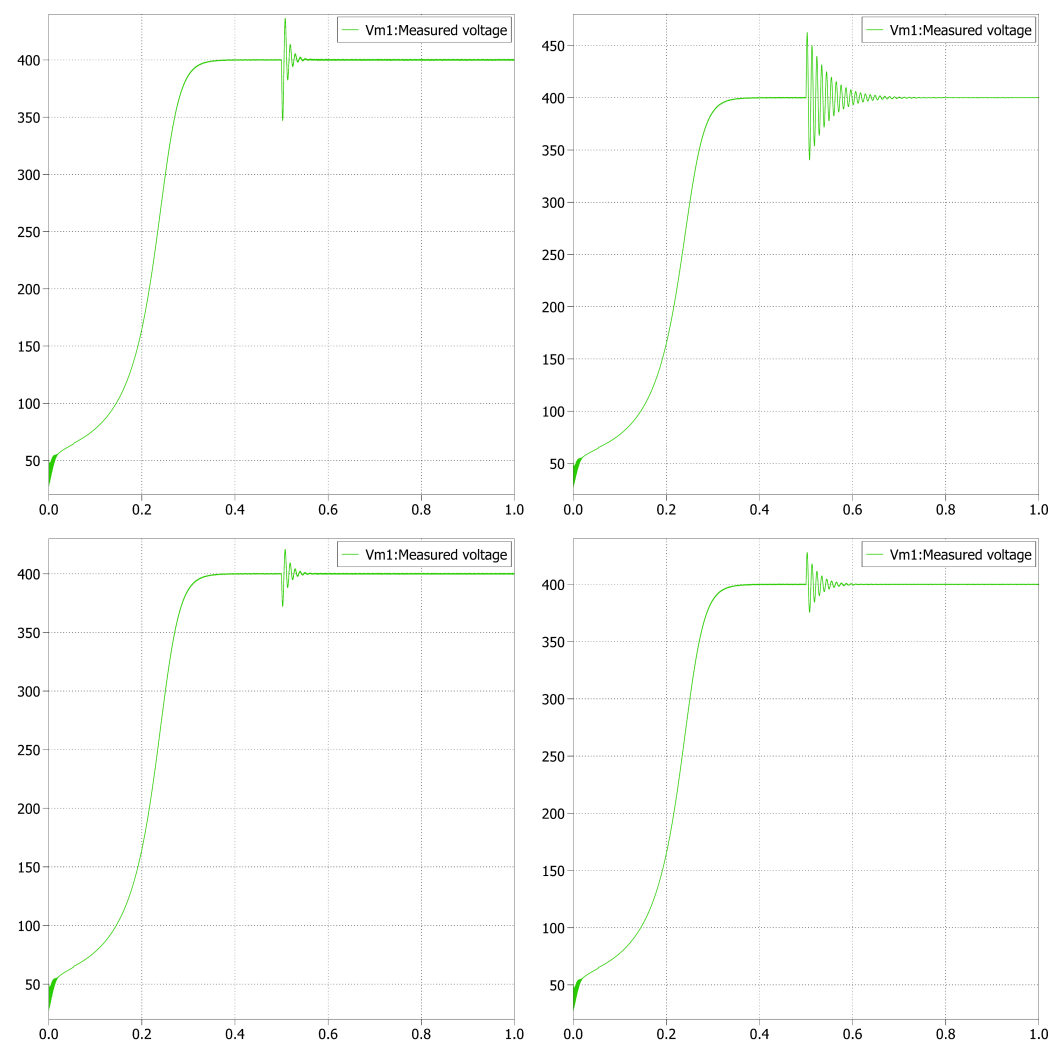


Figure 11. Single-step load transient responses of the interleaved DC–DC converter. Top row: $\pm 25\%$ load changes; Bottom row: $\pm 50\%$ load changes.

- Top-left: $6.67 \rightarrow 8.89 \Omega$ step (-25% load current). The bus voltage shows a small undershoot of about $3\text{--}4\%$ before settling.
- Top-right: $6.67 \rightarrow 5.33 \Omega$ step ($+25\%$ load current). The bus exhibits $\sim 5\%$ overshoot and stabilizes in ~ 0.25 s.
- Bottom-left: $6.67 \rightarrow 13.3 \Omega$ step (-50% load current). The voltage dips by about $8\text{--}10\%$, then recovers within ~ 0.3 s.
- Bottom-right: $6.67 \rightarrow 4.44 \Omega$ step ($+50\%$ load current). This worst-case scenario yields $\sim 12\text{--}15\%$ overshoot, but the voltage still returns to the $\pm 6\%$ band within ~ 0.35 s.

In all cases, the converter recovered well within the 0.5 s requirement of MIL-STD-704F, demonstrating robust control performance. The interleaved structure further ensured that the output current ripple remained around 0.1 A, significantly lower than a single-channel counterpart.

3.2. DC–AC Stage Performance

The second stage of the proposed power conversion system is the three-phase DC–AC inverter, which converts the regulated 400 V DC bus into a balanced AC output suitable for aircraft applications. This stage employs a SPWM strategy to generate three sinusoidal phase voltages with 120° displacement at the standard 400 Hz frequency. The phase-to-neutral RMS voltage is regulated to approximately 120 V, corresponding to 208 V line-to-line, in accordance with the steady-state voltage tolerance specified for 400 Hz aircraft power systems in MIL-STD-704F. The choice of 120 V in simulation accounts for resistive and conduction losses expected in hardware implementation, ensuring that the delivered voltage under practical conditions settles near the nominal 115 V. This section presents the simulated AC output waveforms and evaluates their compliance with the voltage, frequency, and harmonic distortion requirements specified by MIL-STD-704F.

3.2.1. AC Output Waveforms and Settling

After start-up, the three phase voltages rapidly converge to steady state as illustrated in Figure 12 (left panel). In steady state (right panel), the phase-to-neutral RMS is ≈ 120 V for all phases and the line-to-line RMS is ≈ 208 V. The measured fundamental is $f \approx 399.3$ Hz, and the output THD is $\approx 1.27\%$, comfortably below the 5% limit. The steady-state voltage, frequency, and THD values are summarized in Table 2.

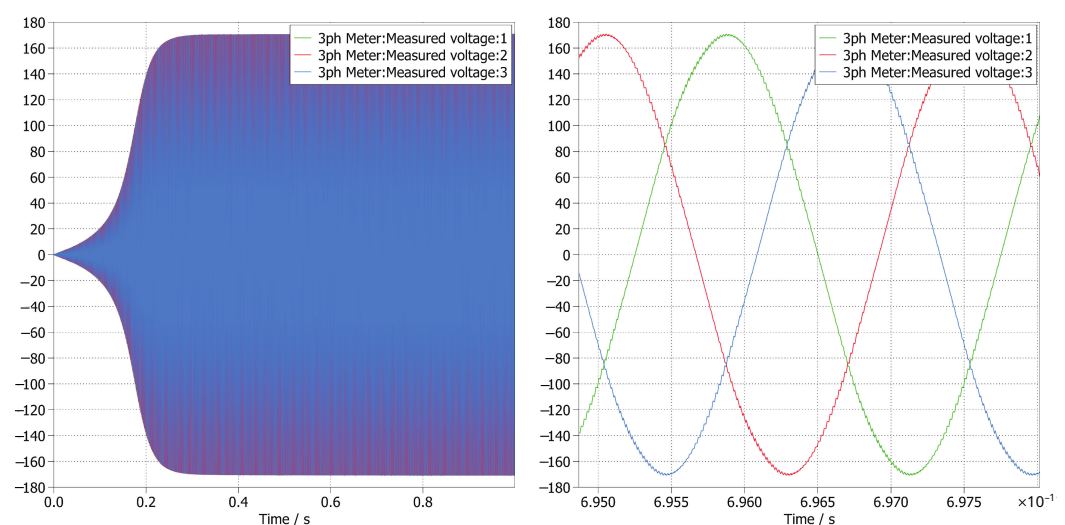


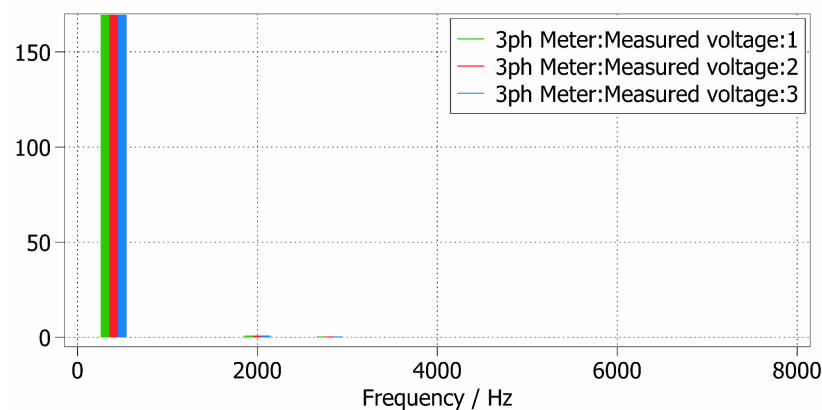
Figure 12. Three-phase inverter output: start-up and settling (left) and steady-state waveforms (right).

Table 2. Steady-state AC output summary (phase-to-neutral and line-to-line).

Quantity	Value	MIL-STD-704F Limit	Compliance
Phase RMS (V_a , V_b , V_c)	119.8/119.9/119.9 V	120 V ($\pm 5\%$)	Yes
Line RMS (V_{ab} , V_{bc} , V_{ca})	207.5/207.8/207.6 V	208 V ($\pm 5\%$)	Yes
Fundamental frequency	399.3 Hz	400 Hz ($\pm 1\%$)	Yes
THD (phase voltage)	1.27%	$\leq 5\%$	Yes

3.2.2. Harmonic Analysis and Power Quality

The harmonic spectrum of the inverter output voltages is shown in Figure 13. The fundamental component at $f \approx 400$ Hz is clearly dominant and has an RMS value of about 120 V. Higher order harmonics remain at low levels and the THD is about 1.27%. The obtained value is in the acceptable range as MIL-STD-704F allows up to 5% THD. The three phases show almost identical spectra, indicating good balance and phase symmetry.

**Figure 13.** Harmonic spectrum of the three-phase inverter output voltages (phase-to-neutral). The fundamental at 400 Hz dominates, while higher-order harmonics remain strongly attenuated.

3.2.3. Power Factor Analysis

At the inverter output (point of common coupling, PCC), the three-phase power factor (PF) was evaluated from the apparent power ratio:

$$PF = \frac{P_{avg}}{S}, \quad (11)$$

where P_{avg} is the average active power and S is the apparent power.

The measured phase RMS voltages were $V_A = 119.95$ V, $V_B = 120.07$ V, $V_C = 119.88$ V, and the corresponding RMS currents were $I_A = 69.34$ A, $I_B = 69.41$ A, $I_C = 69.30$ A. The slight differences observed among the three phase values are mainly caused by interleaving effects, initial condition asymmetries, and numerical discretization inherent to the simulation environment. Since each phase is initialized independently, minor transient deviations may occur during startup and dynamic conditions. These differences are not structural and are effectively mitigated under steady-state operation by the closed-loop control system. The per-phase active powers were

$$P_A = 8.317 \text{ kW}, \quad (12)$$

$$P_B = 8.334 \text{ kW}, \quad (13)$$

$$P_C = 8.307 \text{ kW}. \quad (14)$$

This yields a total active power of

$$P_{\text{tot}} = 24.958 \text{ kW}, \quad (15)$$

and a total apparent power of

$$S_{\text{tot}} = 24.958 \text{ kVA}. \quad (16)$$

Consequently, the three-phase power factor is

$$\text{PF} \approx 0.999\text{--}1.000. \quad (17)$$

The detailed phase RMS values and calculated power factors are summarized in Table 3. Given the very low distortion observed in the harmonic analysis, the total PF is essentially displacement-limited ($\text{PF} \approx \cos \varphi$) and comfortably satisfies the typical aircraft acceptance criteria ($\text{PF} \geq 0.95$) under rated load. The corresponding phase voltage and current waveforms are shown in Figure 14, clearly indicating the near-unity displacement factor.

Table 3. Phase RMS values and PF.

Phase	V_{rms} (V)	I_{rms} (A)	P (kW)	PF
A	119.95	69.34	8.317	0.999–1.000
B	120.07	69.41	8.334	0.999–1.000
C	119.88	69.30	8.307	0.999–1.000
Total	–	–	24.958	0.999–1.000

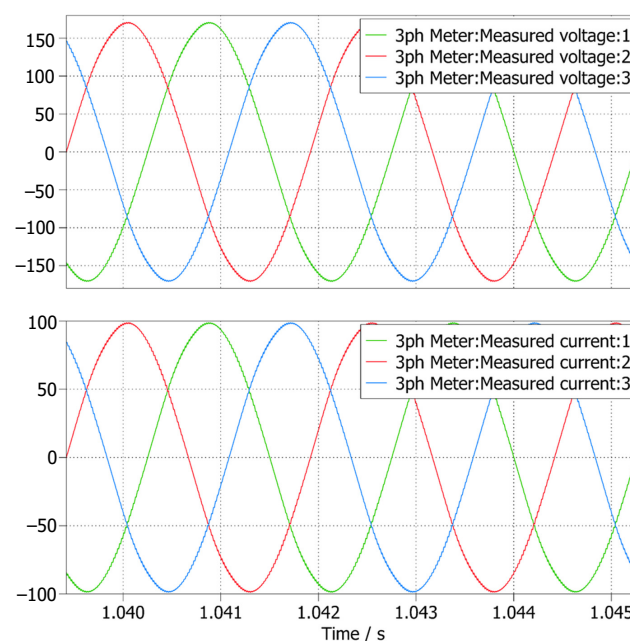


Figure 14. Phase voltages and currents at the PCC, showing the near-unity displacement factor ($\text{PF} \approx 1$).

3.3. Hardware-in-the-Loop (HIL) Setup

To evaluate the practical behavior of the proposed interleaved synchronous Super-Lift Luo converter based inverter, a hardware-in-the-loop (HIL) implementation was carried out using the Typhoon HIL real-time platform, as shown in Figure 15. The complete power conversion structure, including the four-channel interleaved DC–DC stage and the three-phase inverter, was modeled within the HIL environment. This setup enables the

interaction between the DC–DC and DC–AC stages to be viewed in a controlled and reliable experimental setup under dynamically changing operating conditions. This is particularly beneficial in power electronics systems where full-scale laboratory testing may pose safety hazards or infrastructure constraints.

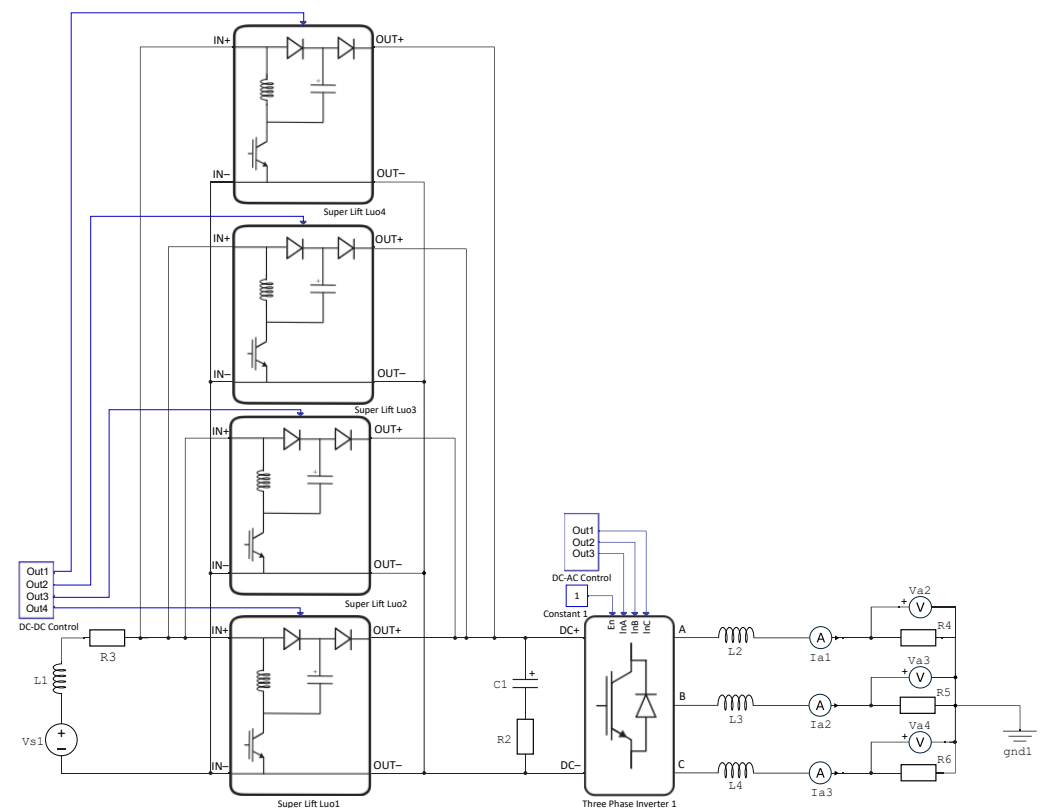


Figure 15. Schematic of the interleaved synchronous Super-Lift Luo converter-based three-phase inverter implemented in the Typhoon HIL platform.

All control algorithms were implemented in the Typhoon HIL Control Center and executed in real time. The PWM generation, interleaving logic, and voltage-current feedback loops were evaluated using a fixed simulation step of $1\ \mu\text{s}$, which provided consistent timing throughout the control execution. The DC–DC converter switching frequency was set to 20 kHz for each interleaved channel, with appropriate carrier phase displacement applied between channels to reduce input current ripple and distribute thermal stress. The three-phase inverter was operated with sinusoidal PWM at a switching frequency of 50 kHz and an output fundamental frequency of 400 Hz. Voltage and current regulation were performed utilizing PI controllers in accordance with the previously described analytical design.

The HIL setup was primarily used to examine whether the stability, transient response, and ripple behavior observed in conventional time-domain simulations are preserved when the system is operated under real-time constraints. In addition, power-quality indicators such as voltage regulation, harmonic distortion, and power factor were evaluated in real-time operation. Moreover, transient events and parameter variations could be investigated without the risk associated with physical hardware testing. A direct comparison between simulation results and HIL measurements provides confidence in the practical applicability of the proposed converter topology and control strategy for aerospace power system applications. Full-power experimental implementation is considered a logical continuation of this work.

3.3.1. HIL Validation

Figure 16 shows the inductor current waveforms (I_{L1} – I_{L4}) of the four interleaved Super-Lift Luo converter channels together with the regulated DC output voltage obtained from the HIL study. A 90° phase shift between adjacent channels ensures an even current distribution among the four stages during operation. Although the peak-to-peak ripple of each inductor current is approximately 10 A, the combined ripple observed at the DC bus remains below 1 A due to the ripple-cancellation effect inherent to the interleaved topology. This balanced current sharing not only reduces input ripple but also promotes improved thermal distribution and overall electromagnetic compatibility of the converter.

The lower part of Figure 16 shows the DC bus voltage waveform obtained from the HIL study. The output voltage stays close to $V_{DC} \approx 404$ V, with a ripple level below 0.2% of the nominal value. This result is in good agreement with the simulation outcomes. The observed voltage stability indicates compliance with the steady-state and transient limits defined by MIL-STD-704F, while confirming that the PI-based voltage controller provides effective voltage regulation.

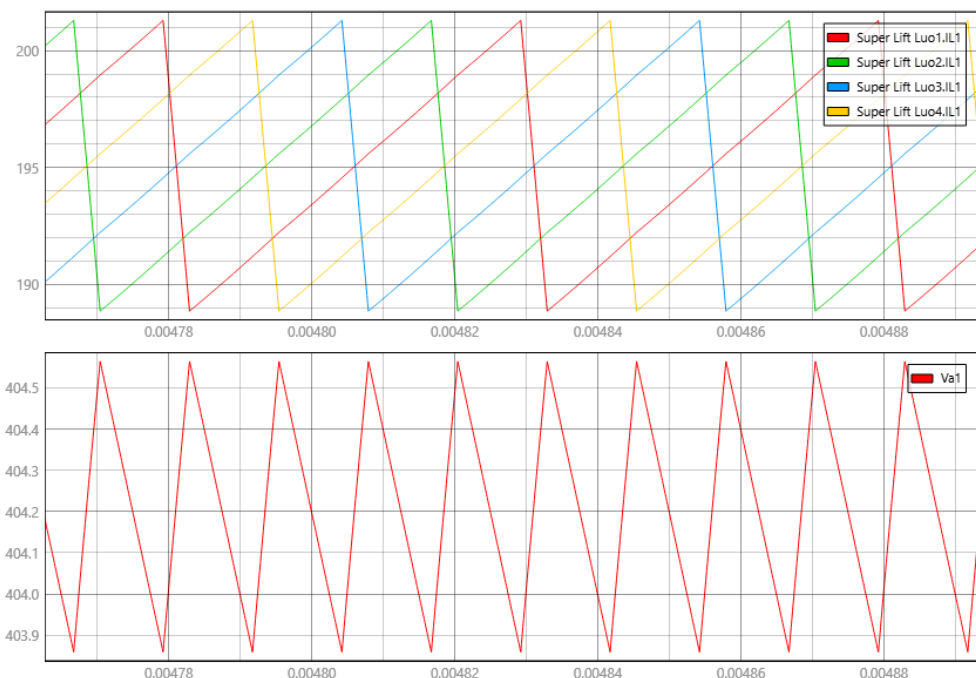


Figure 16. HIL results for the DC–DC conversion stage: (top) inductor currents of the four interleaved Super-Lift Luo converter modules; (bottom) regulated DC bus voltage.

3.3.2. DC–AC Stage Performance and Control Verification

The three-phase inverter is supplied by the regulated DC bus generated by the interleaved SLLC stage and is controlled using sinusoidal PWM with complementary gating and dead-time protection. The HIL results shown in Figure 17 indicate balanced three-phase currents and phase-to-neutral voltages. The fundamental output frequency is approximately 400 Hz, remaining within the ± 10 Hz tolerance specified by MIL-STD-704F. The measured phase voltage peak is $V_{pk} \approx 162.6$ V, corresponding to a phase RMS value of $V_{rms} \approx 115$ V, which results in a line-to-line RMS voltage of $V_{LL} \approx \sqrt{3} V_{rms} \approx 199$ V.

The phase currents have similar magnitudes and are separated by 120° , with no noticeable shift with respect to the corresponding phase voltages. No DC offset or phase asymmetry can be identified in the measured current waveforms. The distortion level is low, which is in line with the harmonic analysis results, where the total harmonic distortion

remains well below the 5% limit. During real-time operation, the inverter maintains balanced phase behavior with stable voltage regulation.

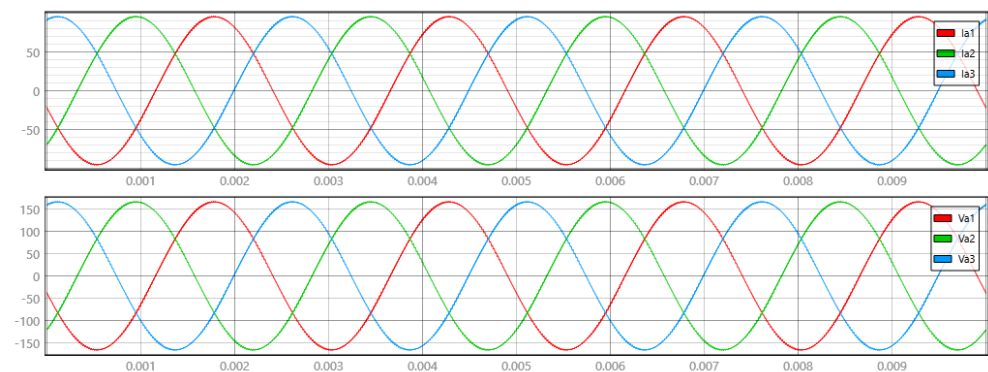


Figure 17. HIL results for the DC–AC inverter: (**top**) balanced three-phase currents; (**bottom**) phase-to-neutral voltages with $V_{pk} \approx 162.6$ V ($V_{rms} \approx 115$ V) at 400 Hz.

3.3.3. Power Quality and Power Factor (HIL Results)

The power quality of the real-time inverter output was assessed by analyzing the phase-A voltage waveform in the frequency domain. The harmonic spectrum is presented in Figure 18, plotted on a logarithmic scale to clearly show the very low amplitude of higher-order components. The fundamental frequency appears at 400 Hz with an amplitude of $V_1 = 165.8$ V ($V_{rms} = 117.3$ V). All harmonic components above the fundamental remain well below 1% of the main component amplitude. The third, fifth, and seventh harmonics are each under 0.1%, resulting in a total harmonic distortion of

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \times 100 = 0.77\%. \quad (18)$$

Such an extremely low THD demonstrates that the inverter produces a highly sinusoidal output voltage, fully complying with the $THD \leq 5\%$ criterion specified in MIL-STD-704F. The nearly zero phase displacement between voltage and current waveforms yields an overall power factor of approximately

$$PF = \cos \varphi \times \frac{1}{\sqrt{1 + (THD/100)^2}} \approx 0.999. \quad (19)$$

Hence, the inverter delivers almost purely active power to the load, confirming the effectiveness of the control strategy in real-time operation. The close numerical agreement between the simulation and HIL results (PF and THD differences below 0.2%) validates the accuracy of the real-time implementation.

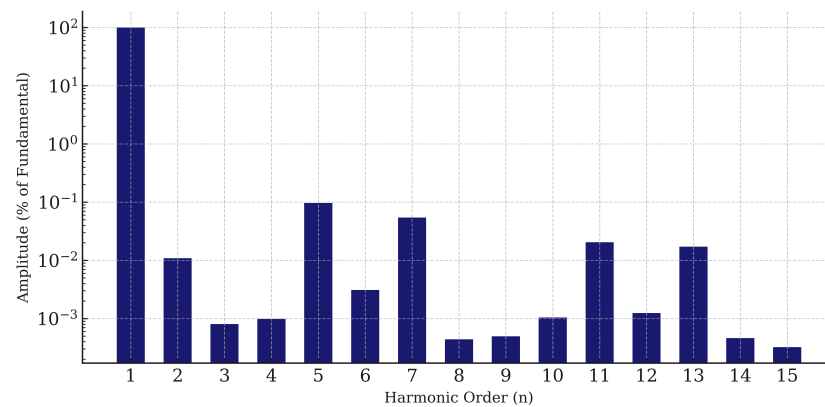


Figure 18. FFT spectrum of the phase-A output voltage obtained from the HIL test, showing a dominant 400 Hz fundamental, THD = 0.77% and PF $\approx$ 0.99.

3.4. HIL Overall Summary

The HIL validation comprehensively confirms the accuracy and real-time feasibility of the proposed ISSLLC based inverter system. The DC–DC stage achieved a regulated output of $V_{DC} \approx 404$ V with an output current ripple below 1 A, demonstrating the effective current sharing and ripple cancellation of the four-channel interleaved topology. The subsequent DC–AC inverter stage produced balanced three-phase voltages at 400 Hz with RMS values of approximately 115 V per phase and perfectly sinusoidal waveforms.

The FFT analysis of the HIL-measured output voltage (Figure 18) indicates a fundamental component of 165.8 V and a total harmonic distortion of 0.77%, which is well below the 5% limit specified in MIL-STD-704F. The inverter also operated with a displacement factor close to unity ($\cos \varphi \approx 1$) and a total power factor of approximately 0.999, supplying almost all the active power to the load. Both the dynamic and steady-state responses were consistent with the results obtained from the PLECS offline model, with deviations in voltage amplitude, THD, power factor, and frequency remaining under 0.2%.

To place the proposed approach in context, its performance can be qualitatively compared with representative baseline converter solutions commonly used in aerospace and high-frequency power systems, such as conventional boost-based, transformer-isolated, and multilevel inverter topologies. Compared to classical boost converters, the proposed interleaved synchronous SLLC structure achieves higher voltage gain with reduced DC-link ripple, which directly benefits inverter stability and harmonic performance. In contrast to transformer-isolated solutions, the proposed topology eliminates magnetic isolation stages, leading to reduced weight and volume while maintaining compliance with 400 Hz aerospace power requirements. Furthermore, the interleaved architecture contributes to improved transient response and current sharing, enabling high efficiency and low harmonic distortion. These findings are further supported by the HIL results, which validate that the proposed converter and control strategy satisfy the demanding power-quality requirements of 115 V, 400 Hz aircraft electrical systems, confirming their suitability for real-time embedded aerospace applications and compliance with MIL-STD-704F.

4. Conclusions

This study investigated the design, modeling, and real-time validation of a 24 kVA three-phase inverter based on an interleaved synchronous Super-Lift Luo converter for aircraft 115 V, 400 Hz power systems. The presented structure combines the high voltage gain of the Super-Lift Luo converter with the current-sharing and ripple-reduction characteristics of interleaving. The use of synchronous rectification contributes to reduced conduction losses and improved efficiency.

The interleaved DC–DC stage distributes power among four channels, reducing current stress and supporting stable DC-link regulation from a 28 V input to approximately 400 V. The cascaded PI control structure enables consistent voltage regulation under steady-state and transient conditions.

Hardware-in-the-Loop testing showed close agreement with the PLECS simulations. The inverter achieved a regulated three-phase output of 115 V, 400 Hz with a total harmonic distortion of only 0.77% and a power factor of 0.999, indicating almost purely active power delivery. The close agreement between PLECS and HIL results (less than 0.2% deviation) validates both the converter model and the control implementation in real time.

The results indicate that the proposed ISSLLC-based inverter meets the steady-state and transient power-quality requirements defined by MIL-STD-704F for aircraft electrical systems. The topology provides a promising solution for next-generation more-electric aircraft, and its modular structure allows adaptation to other high-gain, high-efficiency applications such as renewable energy interfaces and electric propulsion systems.

Although the experimental cases presented in this study are in the kVA power range, the proposed interleaved synchronous Super-Lift Luo converter based inverter is conceptually scalable to higher power levels. The interleaved architecture facilitates current sharing and thermal balancing, which are essential for high-power operation. Nevertheless, scaling to significantly higher power ratings would require advanced semiconductor devices, reinforced thermal management, and modular system design, which are considered to be future research directions.

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Abbreviations

The following abbreviations are used in this manuscript:

AC	Alternating Current
DC	Direct Current
DC–DC	Direct Current to Direct Current
DC–AC	Direct Current to Alternating Current
DoD	Depth of Discharge
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FFT	Fast Fourier Transform
HIL	Hardware-in-the-Loop
ISSLLC	Interleaved Synchronous Super-Lift Luo converter
MEA	More Electric Aircraft
MIL-STD-704F	Military Standard for Aircraft Electric Power Characteristics
PF	Power Factor
PI	Proportional–Integral
PLECS	Piecewise Linear Electrical Circuit Simulation
PWM	Pulse Width Modulation
RMS	Root Mean Square
SLLC	Super-Lift Luo converter
SSLLC	Synchronous Super-Lift Luo converter
SPWM	Sinusoidal Pulse Width Modulation
THD	Total Harmonic Distortion

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