

Article

# Time Resolution Improvement Using Dual Delay Lines for Field-Programmable-Gate-Array-Based Time-to-Digital Converters with Real-Time Calibration

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Received: 8 December 2018 ; Accepted: 18 December 2018 ; Published: 21 December 2018



**Abstract:** This paper presents a time-to-digital converter (TDC) based on a field programmable gate array (FPGA) with a tapped delay line (TDL) architecture. This converter employs dual delay lines (DDLs) to enable real-time calibrations, and the proposed DDL-TDC measures the statistical distribution of delays to permit the calibration of nonuniform delay cells in FPGA-based TDC designs. DDLs are also used to set up alternate calibrations, thus enabling environmental effects to be immediately accounted for. Experimental results revealed that relative to a conventional TDL-TDC, the proposed DDL-TDC reduced the maximum differential nonlinearity by 26% and the integral nonlinearity by 30%. A root-mean-squared value of 32 ps was measured by inputting the constant delay source into the proposed DDL-TDC. The proposed scheme also maintained excellent linearity across a range of temperatures.

**Keywords:** field-programmable gate array (FPGA); time-to-digital converter (TDC); tapped-delay line (TDL); dual delay lines (DDL); run-time calibration; differential non-linearity (DNL)

## 1. Introduction

Time-to-digital converters (TDCs) are vital components in numerous scientific applications, such as positron emission tomography (PET) [1–6], time-of-flight (ToF) image sensors [3–7], and light detection and ranging (LiDAR) [8–10]. Especially in ToF imaging and LiDAR applications, high-resolution TDCs affect overall performance. Field programmable gate array (FPGA)-based TDC designs have become notably popular thanks to their programmability and the short times required to generate designs [11–22]. The tapped delay line (TDL) is the simplest FPGA-based structure in TDC designs. Time resolution and linearity are crucial to FPGA-based TDCs; however, the dedicated elements used in FPGAs often result in a lack of uniformity in delay cells, which in turn can undermine time linearity [12]. Therefore, a great deal of research has gone into the development of calibration methods to overcome nonuniform cell delay in FPGA-based TDL-TDCs [13–22].

Time resolution and time linearity are crucial issues in any FPGA-based TDC design. In 1997, Kalisz et al. presented a calibration method for an FPGA-based TDC implemented with a QuickLogic pASIC FPGA device. The TDC can reach a time resolution of 200 ps, and the conversion range of this TDC is 43 ns [13,14]. Dedicated carry lines of an FPGA are used as delay cells to perform time interpolation within the system clock period and to realize fine time measurements [15]. A TDC with calibration implemented in an Altera EP1K50TC144-1 FPGA has a resolution of 65 ps; a TDC implemented in a Xilinx XC2V4000-6BF957 FPGA has a resolution of 46.2 ps. The authors also utilized the dedicated resources of FPGA devices to design TDCs on FPGA platforms [16,17]. Another factor

that affects the time linearity in FPGA-based TDC designs is the presence of ultra-wide bins (UWB) when dedicated resources are used in the FPGA device. Thus, because wave union TDCs divide the original bin size, they can deal with UWB effects and improve the time linearity [18–21]. However, the wave union method is not applicable to high-end FPGAs, in particular the Xilinx UltraScale FPGA that is manufactured with 20-nm process technology. Therefore, the authors proposed a dual-sampling TDL architecture and a bin decimation method for Xilinx UltraScale FPGAs that could make the delay elements as small and uniform as possible, so that the implemented TDCs can achieve high time resolutions beyond the intrinsic cell delay [23,24]. Recently, selected, divided, or interpolated versions of the delay bin have become more popular to manage the nonuniform delay cells in FPGA-based TDCs, and thus to improve the time resolution and time linearity [22–31].

Two-stage inner interpolation methods that employ an eight-phase clock and an equivalent time coding delay line within a 28-nm FPGA chip were reported [25]. Although such methods enable high time resolution, the designs are highly complex. Nonetheless, time histogram bin counts have been used to calibrate nonlinearity in TDL-TDC delay bins [26–31], and two-sample-sums and two-sample-differences of a quantized histogram can be used to minimize the influence of nonlinear quantization on the histogram [26]. Unfortunately, the quantization-and-nonlinearity minimization method depends on a highly complex mathematical analysis [26]. A multi-path delay line can select the most equal cell as a delay bin in an FPGA device to improve its linearity [27]. A merged delay line was also presented to delay the UWB effect [28]. Unfortunately, the methods in [27,28] must pre-run the code density test to obtain the time information of each bin, then re-design the TDC according to that time information during the calibration. Thus, the process is remarkably time consuming and impractical, especially in real-time systems. A simpler approach was proposed in [29], wherein a code density test was used to calibrate the delay cell, and the conversion output bit was adjusted to improve differential non-linearity (DNL) and integral nonlinearity (INL) values. Nonetheless, that nonlinearity correction was still processed in the same manner as an off-line program-based correction. In [30], the auto-calibration circuit was implemented in a single FPGA; however, the calibration was only run when the FPGA was started. This underlines the importance of developing a straightforward system that can be used to implement run-time corrections to resist environmental effects. In [31], the authors presented a dual-phase tapped delay line with on-the-fly calibration, implemented on a 40-nm FPGA. The results demonstrated that the characteristics of the delay cell tend to change at different temperatures. During a temperature shift from 10–50 °C, their TDC with on-the-fly calibration maintained a 12.8-ps root-mean-squared (RMS) standard uncertainty [31]. Several works have presented delay cells that are sensitive to environmental changes, especially temperature effects [13,14,16,19,23,24,30,31]. Moreover, a comparison is listed in Table 1, which presents the performance of the proposed DDL-TDC compared with existing works.

**Table 1.** Comparison with FPGA-based TDCs. LSB, least significant bit.

| Method    | Structure | FPGA              | Dynamic Range | RMS (ps) | LSB (ps) | DNL (LSB)     | INL (LSB)     | Calibration Method |
|-----------|-----------|-------------------|---------------|----------|----------|---------------|---------------|--------------------|
| [13,14]   | VDL       | pASIC (0.65 μm)   | 43 s          | 129      | 200      | [−0.47, 0.44] | [−0.2, 1.28]  | Off-line           |
| [16]      | TDL       | Virtex-5 (65 nm)  | 50 ns         | 24.2     | 17       | [−1.00, 3.55] | [−2.99, 2.58] | Off-line           |
| [23]      | TDL       | UltraScal (20 nm) | 2 ns *        | 4.2      | 3.29     | ---           | [--, 2]       | Off-line           |
| [25]      | TDL       | Virtex-5 (65 nm)  | 42 s          | 20       | 2.5      | ---           | ---           | Off-line           |
| [28]      | TDL       | Virtex-5 (65 nm)  | 6 ns *        | 28.9     | 50       | [−0.47, 0.62] | [−0.87, 0.68] | Off-line           |
| [29]      | TDL       | Virtex-5 (65 nm)  | 6 ns *        | —        | 60       | [−0.54, 0.24] | [−0.66, 0.65] | Off-line           |
| [30]      | TDL       | Virtex-5 (65 nm)  | 6 ns *        | —        | 46.9     | [−0.68, 1.04] | [−4.27, 2.27] | Real-time *        |
| [31]      | TDL       | Virtex-6 (40 nm)  | 1.6 ns *      | 12.8     | 10       | [−1.00, 1.91] | [−2.20, 3.93] | Real-time          |
| This Work | TDL       | Virtex-5 (65 nm)  | 6 ns *        | 32       | 46.9     | [−0.64, 0.92] | [−7.12, 4.18] | Real-time          |

VDL: Vernierdelay line; TDL: tapped delay line; FPGA: Field-Programmable-Gate-Array; RMS: root-mean-squared; LSB: least significant bit; DNL: differential non-linearity; INL: integral nonlinearity.  
\* Only calibrate at the start of the TDC. \* The dynamic range for the fine time counter.

This study proposes a novel architecture that employs two TDLs for an FPGA-based TDC, referred to as a dual delay line (DDL) TDC. This architecture can be implemented within the calibration circuit of an FPGA chip to enable calibration operations in real time. A finite state machine (FSM) is used to manage both the calibration delay line and the conversion delay line, which allows (1) nonuniform delay cells to be calibrated and (2) time differences to be converted based on data held in calibration mapping memory. Experimental results demonstrated the superiority of the proposed DDL-TDC over conventional TDL-TDCs in terms of time linearity and maximum INL and DNL values, despite variations in temperature. This makes the proposed DDL-TDC highly robust for the measurement of time differences in a broad range of external environments.

The remainder of this paper is organized as follows. The proposed FPGA-based DDL-TDC is outlined in Section 2. Details concerning the TDL-TDC, FPGA platforms, and DNL calibration circuits are presented in Section 2. Experiments aimed at evaluating the proposed scheme are described in Section 3. Conclusions are drawn in Section 4.

## 2. Design of the Proposed DDL-TDC

### 2.1. Method of TDL-TDC

TDL is the most popular structure used in TDC implementation (Figure 1); however, a lack of uniformity in delay cells tends to undermine time linearity, particularly in FPGA-based TDC devices. Figure 1 shows the architecture of the TDL-TDC, and the histogram illustrates the time distribution of the delay cell in the delay chain. It is easy to observe that the delay cell cannot reach an equal delay time in the chain. This impairs the linearity of the TDC; we want to correct this nonlinearity effect in this work. A calibration method is presented in [29], which provides a simple bin calibration scheme for FPGA-based TDC designs. Thus, the uniformity delay cell in an FPGA-based TDC can be calibrated, and the linearity can be improved. Unfortunately, the method addressed in [29] calibrated the TDC output by using a software program after the TDL-TDC output had been measured. Thus, that scheme cannot calibrate the uniform delay cell immediately in a run-time conversion. Unlike off-line methods, such as that proposed in [29], we adopted a statistical approach to the calibration of an FPGA-based TDC [30] to address the topic of time linearity in real time.

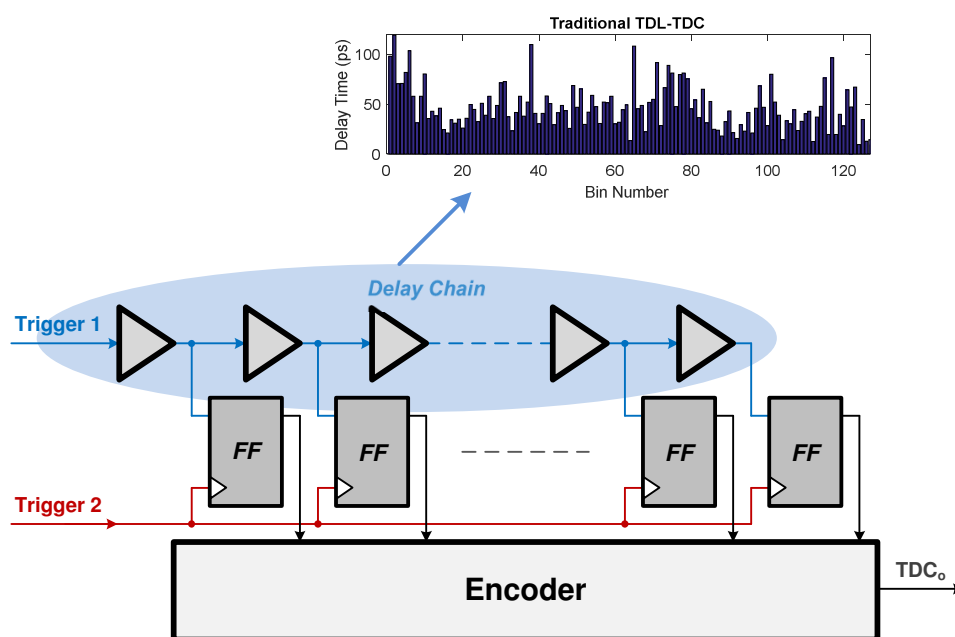


Figure 1. Architecture of TDL-TDC.

## 2.2. Calibration of TDL-TDC

As the code density test is adapted, the time distribution of each delay cell can be expressed as follows:

$$t_1 = \frac{h_1}{C}T, \quad (1)$$

$$t_2 = \frac{h_2}{C}T, \quad (2)$$

$$\vdots$$

$$t_M = \frac{h_M}{C}T, \quad (3)$$

where  $h_i$  indicates the number of hits for the  $i^{\text{th}}$  delay cell,  $C$  is the total hits of this calibration run,  $T$  is the range of the calibration signal, and  $M$  delay cells are allocated in this chain. The time conversion is calculated from the cells when the signal is reached. As the signal reaches the  $N^{\text{th}}$  cell, the time conversion result  $T_N$  can be expressed as follows:

$$T_N = \sum_{j=1}^N (t_j). \quad (4)$$

The TDC conversion output can be further expressed through the quantization operation  $Q(\bullet)$ :

$$TDC_c = Q\left(\sum_{j=1}^N (t_j)\right). \quad (5)$$

Based on Equation (5), the time conversion can be obtained according to the hit distribution of each cell, which is called the code density statistical calibration. Because the statistical bin calibration requires considerable time to obtain the time distribution of each delay cell in the chain, two delay lines are adopted in the proposed DDL-TDC to reach run-time calibration. Thus, the calibration can alternate between these two delay lines. These two delay lines are assigned to dedicated fast lookahead carry logic, referred to as CARRY4 cells in the Xilinx Vertix-5 FPGA [32], in two vertical lines by using the commands RLOC and LOC of the Xilinx ISE 14.7 software (Xilinx Int., San Jose, CA, USA) tool. The dedicated fast lookahead carry logic (CARRY4) has a small time delay in the Vertix-5 FPGA logic resource, which can obtain higher time resolution than other logic resources. In each CARRY4, four delay cells are implemented, and 512 delay cells are allocated in each vertical delay line. Figure 2 illustrates the layout of the two delay chains in the FPGA chip and the details of the CARRY4 cells.

## 2.3. Architecture of DDL-TDC

Figure 3 illustrates the architecture of the proposed DDL-TDC, in which two TDLs are incorporated in the calibration circuit and a real-time FSM is implemented upstream of the TDL-TDC output. The proposed FSM has two calibration mapping memories; these memories control the two delay lines to do calibration or run TDC conversion. For this reason, the DDL-TDC can run calibration and conversion based on the control signal from the proposed FSM. Figure 4 presents a flowchart for two FSMs that manage calibration and output. The calibration FSM (*FSM Cal*) has three states:

- **Init:** As the TDL enters calibration mode, the FSM transitions to the *Init* state. In this state, calibration memory will be reset to zero for all addresses, and the system begins to run code density counts. The calibration memories, *Cal\_Mem A* and *Cal\_Mem B*, include 512 8-bit words; thus, 9-bit addresses must be reset.
- **Cal\_Run:** Code density counts are run in this state to calibrate the time distribution corresponding to the delay line that will be calibrated. For this,  $2^{17}$  counts are run for the *Cal\_Run* state to obtain the time distribution based on the code density test scheme [33].

- Cal\_Num*: After *Cal\_Run*, the *Cal\_Num* sums the hit counts for each delay cell. Then, the time distribution can be converted to time delay. These items of time information are stored within the calibration memory ((*Cal\_Mem A* or (*Cal\_Mem B*)) appropriate for the relevant cell delay. Thus, the TDC output code can be calibrated from this calibration mapping memory.

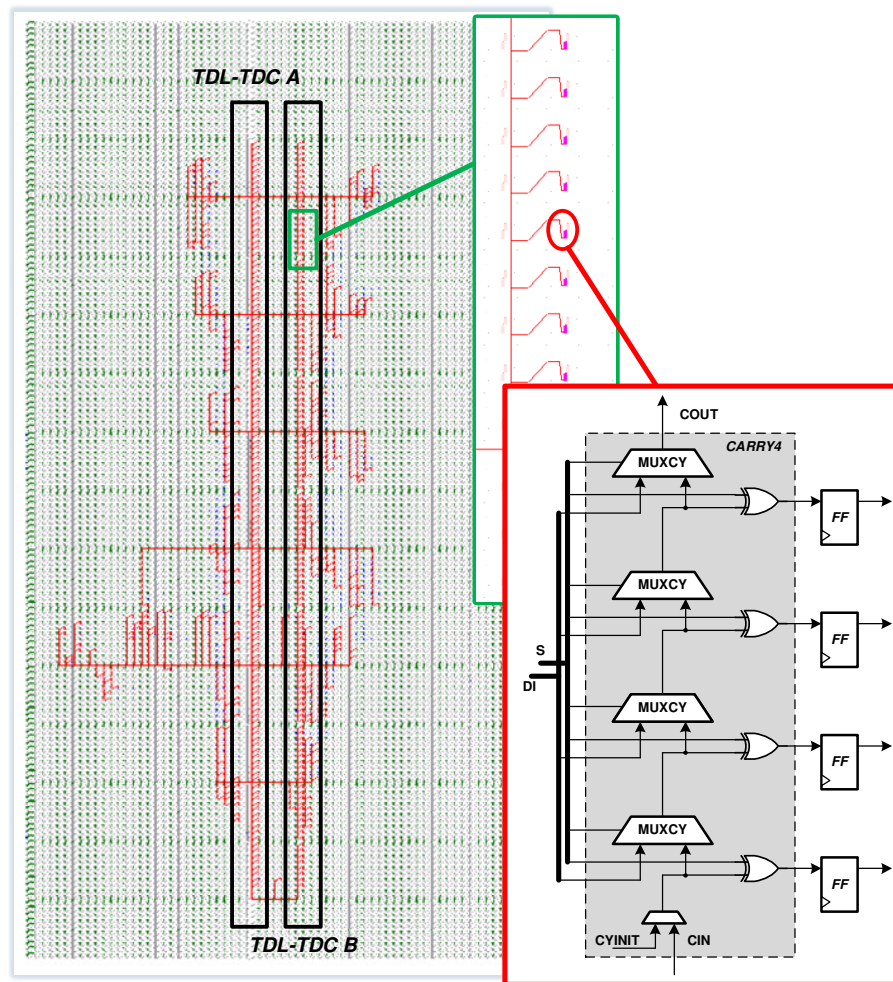


Figure 2. Layout view of two delay chains in the proposed FPGA-based DDL-TDC.

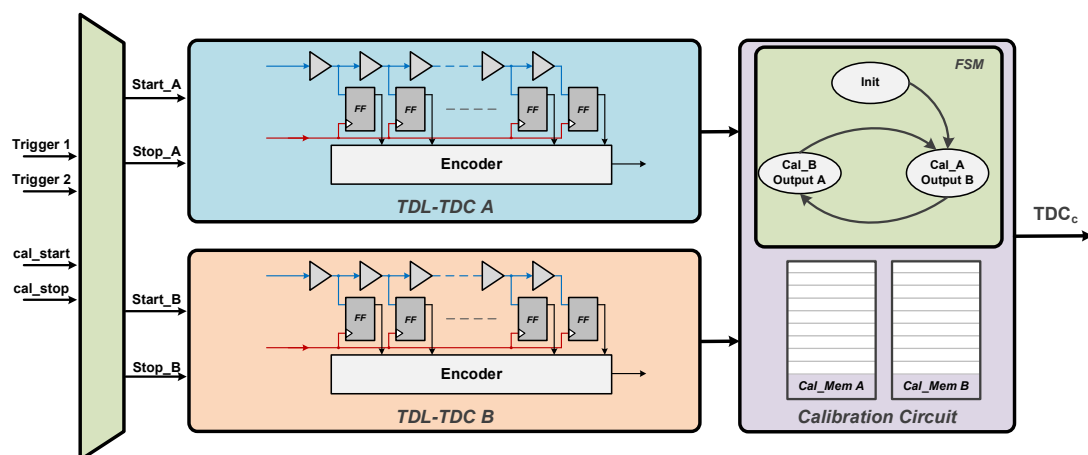


Figure 3. Architecture of DDL-TDC.

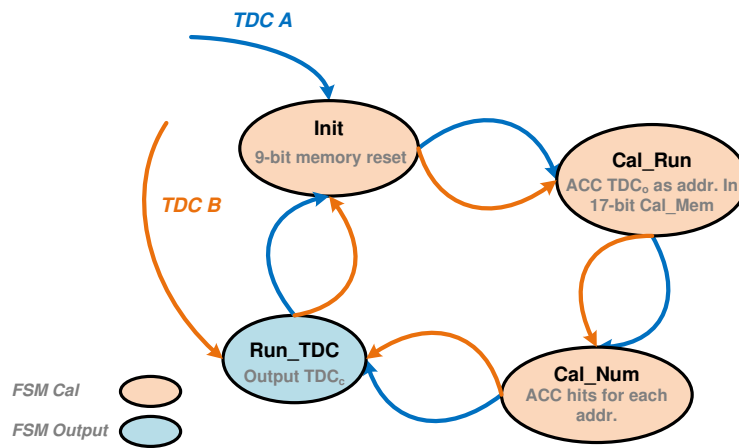


Figure 4. Finite state machine used in DDL-TDC.

The conversion FSM (*FSM Output*) includes just one state (*Run\_TDC*), in which the time delay is converted into digital code based on data in the calibration memory. According to *FSM Cal* and *FSM Output*, the proposed TDC can always calibrate the delay cell. TDL-A runs DNL calibration and updates calibration mapping codes in the calibration memory *Cal\_Mem A*, while TDL-B simultaneously performs conversions based on *Cal\_Mem B*. Following the calibration of TDL-A, TDL-B calibrates the DNL and updates the mapping code in *Cal\_Mem B*, while TDL-A simultaneously runs the conversion. The proposed DDL calibration circuit is able to perform calibrations in real time and shows excellent performance in terms of time linearity.

2.4. Calibration Flow of DDL-TDC

Figure 5 illustrates the timing diagram of the proposed DDL calibration. In the beginning, the TDL-A takes  $2^9 = 512$  cycles to reset *Cal\_Mem A* and then uses  $2^{17} = 131,072$  cycles to count the hits of code density testing in the *Cal\_Run* state of the TDL-A calibration FSM. Finally, TDL-A uses  $2^9 = 512$  cycles to obtain the calibration map and stores the parameter in *Cal\_Mem A*. For these  $(2^9 + 2^{17} + 2^9)$  cycles, TDL-TDC A executes calibration, and TDL-TDC B runs the time conversion at the same time. The operation changes for the next  $(2^9 + 2^{17} + 2^9)$  cycles; in those cycles, the TDL-TDC A runs time conversion, and the TDL-TDC B executes calibration. As TDL-TDC A executes the calibration, *cal\_start* and *cal\_stop* connect to *Start\_A* and *Stop\_A*; the input signals *Trigger 1* and *Trigger 2* connect to the input signals of TDL-TDC B (*Start\_B* and *Stop\_B*). In this work, we chose 6 ns as our clock period. Thus, the calibration time of TDL-TDC A is  $(2^9 + 2^{17} + 2^9) \times 6 \text{ ns} = 792,576 \text{ ns} \approx 0.8 \text{ ms}$ . In this 0.8 ms, TDL-TDC A executes the calibration, and TDL-TDC B runs the time conversion. However, in the next 0.8 ms, TDL-TDC B executes the calibration, and TDL-TDC A runs the time conversion. Consequently, the proposed DDL-TDC performs calibration every 0.8 ms. This time is short enough to adapt to changes in the environment; the ongoing conversion is suitable for ToF LiDAR applications.

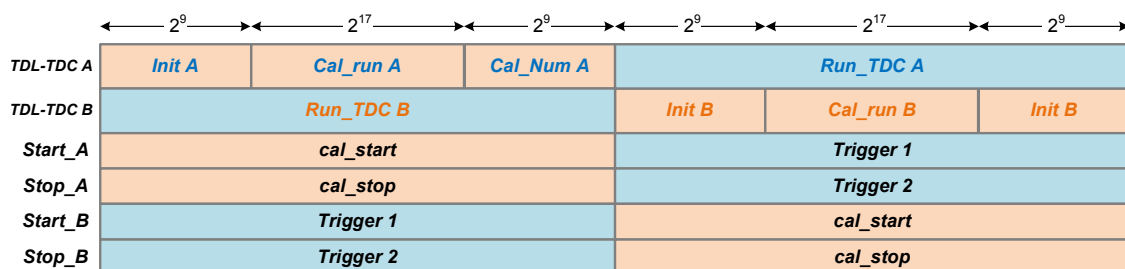


Figure 5. Timing flow of the calibration in the proposed DDL-TDC.

### 3. Experiment Results and Discussion

#### 3.1. Experiment Setup

To demonstrate the proposed FPGA-based DDL-TDC, our proposed DDL-TDC architecture was implemented on a Xilinx XC5VLX110T FPGA chip by using a Xilinx ISE 14.7 tool to synthesize the RTL Verilog code and do placement and routing to evaluate its performance in terms of time linearity. Figure 6 shows the experimental setup of the proposed DDL-TDC measured system. For this, *Trigger 1* and *Trigger 2* 166-MHz clock signals were generated using Agilent (Agilent Technologies, Santa Clara, CA, USA) 81130A signal generators with two asynchronous sources. Calibrations *cal\_start* and *cal\_stop* were respectively generated using two on-board oscillators from 100-MHz and 200-MHz clocks that employed discrete on-chip phase-locked loops (PLL) to generate two 166-MHz clock signals. Based on a clock signal of 166 MHz, the time conversion range was 6 ns. The resource utilization of the proposed DDL-TDC is shown in Table 2. The DDL-TDC required an additional 2% of the slice registers, 3% slice LUTs, 5% occupied slices, two PLLs, and two block RAM units, which caused a light resource overhead relative to the TDL-TDC, and the power consumption of the DDL-TDC was increased by only 7% relative to the TDL-TDC. The 6-ns interval was chosen in this work because we measured the average delay time for a vertical CARRY4 delay chain. The common technique to set the (average or total) delay of the cells is to lock the total delay of the line to a reference. For this circuit, 6 ns was a suitable delay time for 512 delay cells. A longer time would not have been suitable because the delay cells would not have worked in a single vertical chain. A smaller time would not have been suitable because the conversion range would have been too small. Thus, we chose 6 ns (166 MHz) as the clock cycle in this work. This was only suitable for the particular FPGA in this work. If a different FPGA were used, a different frequency would be expected.

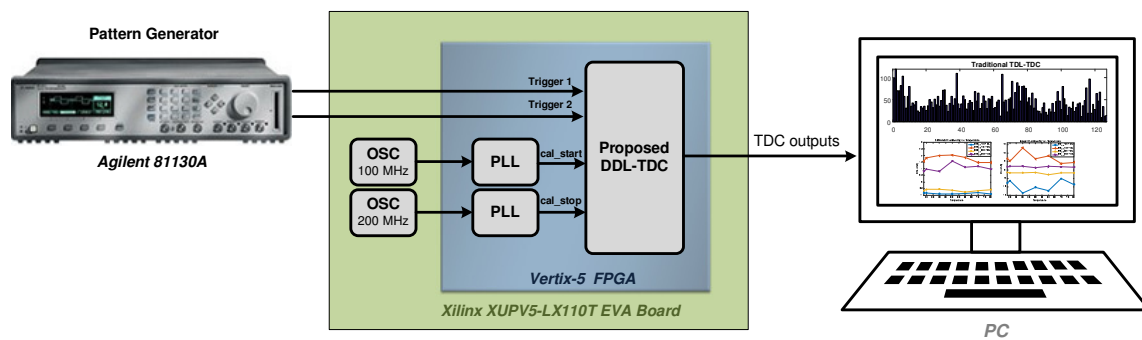


Figure 6. Experimental setup of the proposed DDL-TDC measured system.

Table 2. FPGA resource utilization and power consumption of the DDL-TDC.

| Resources       | Available | TDL-TDC<br>(No Calibration) |             | DDL-TDC<br>(Real-Time Calibration) |             |
|-----------------|-----------|-----------------------------|-------------|------------------------------------|-------------|
|                 |           | Used                        | Utilization | Used                               | Utilization |
| Slice Registers | 69,120    | 1023                        | 1%          | 2147                               | 3%          |
| Slice LUTs      | 69,120    | 1567                        | 2%          | 4107                               | 5%          |
| Occupied Slices | 17,280    | 473                         | 2%          | 1342                               | 7%          |
| PLL_ADVs        | 6         | 0                           | 0%          | 2                                  | 33%         |
| Block RAM/FIFO  | 148       | 0                           | 0%          | 2                                  | 1%          |
| Total Power     |           | 1.507 W (100%)              |             | 1.606 W (107%)                     |             |

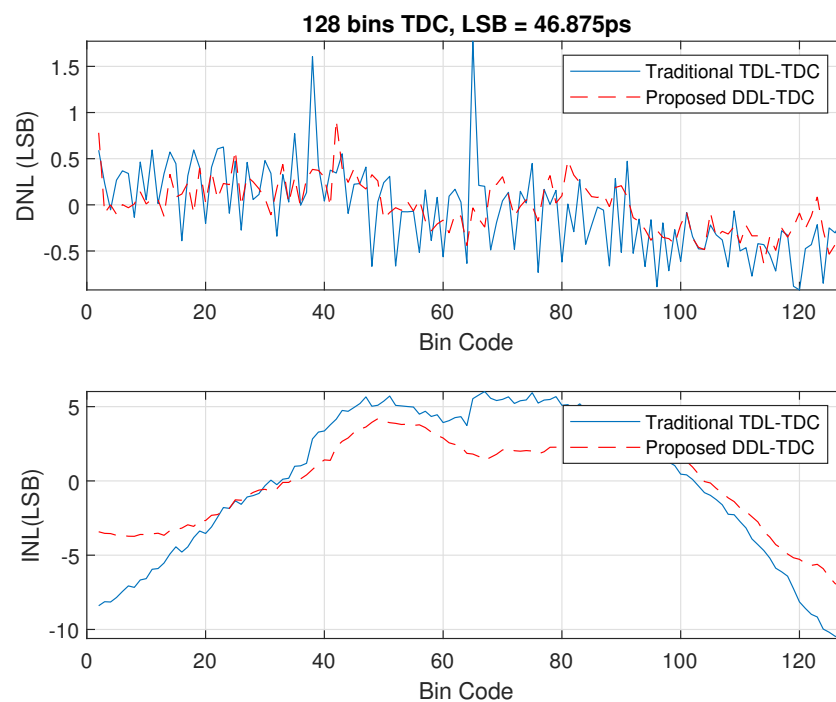
#### 3.2. Results and Discussion

The proposed DDL-TDC output 7-bit ~ 5-bit digital code over a conversion range of 6 ns, such that the least significant bit (LSB) of the DDL-TDC was 46.875 ps (= 6 ns/128) ~ 187.5 ps (= 6 ns/32). Figures 7–9 compare DNL and INL values from a traditional TDL-TDC (without any calibration) and from the proposed DDL-TDC (with real-time calibration) for the LSBs of 46.875 ps, 93.75 ps,

and 187.5 ps, respectively. The ranges of DNL and INL values were  $[-0.64, 0.92]$  and  $[-7.12, 4.18]$  for 46.875 ps,  $[-0.50, 0.44]$  and  $[-3.35, 2.06]$  for 93.75 ps, and  $[-0.47, 0.35]$  and  $[-1.34, 1.03]$  for 187.5 ps. Table 3 shows the linearity improvement of the DDL-TDC compared with the TDC-TDC, which is presented as percentages without any calibration. The DDL-TDC clearly outperformed TDL-TDC in terms of INL and DNL. These results clearly demonstrate the efficacy of DDL-TDC in terms of time linearity.

**Table 3.** Linearity improvements for the proposed DDL-TDC and TDL-TDC.

| LSB       | DNL Improvements | INL Improvements |
|-----------|------------------|------------------|
| 46.875 ps | 31%              | 30%              |
| 93.75 ps  | 46%              | 30%              |
| 187.5 ps  | 26%              | 41%              |



**Figure 7.** INL/DNL values obtained using the proposed DDL-TDC with 7-bit digital output.

To verify the time resolution of the proposed DDL-TDC, a constant time interval was fed as *Trigger 2*, which was constantly delayed by the *Trigger 1* signal. Figure 10 presents the histogram of the measured data after performing  $10 \times 2^{17}$  measurements of the constant delay time. The measured mean time was 252.8 ps, and the RMS value was 32.41 ps. Thus, the single-shot precision of DDL-TDC was  $22.9 \text{ ps} = 32.41 / \sqrt{2} \text{ ps}$ . For various temperatures, Figure 11 also illustrates the RMS values for real-time calibration TDC (DDL-TDC) and for the TDL-TDC with a constant mapping calibration table in software. The proposed DDL-TDC exhibited considerable robustness against fluctuations in temperature, as indicated by the RMS values in Figure 11. Consequently, the proposed DDL-TDC not only improved DNL and INL performance but also achieved high-resolution measurements in an FPGA-based TDC design.



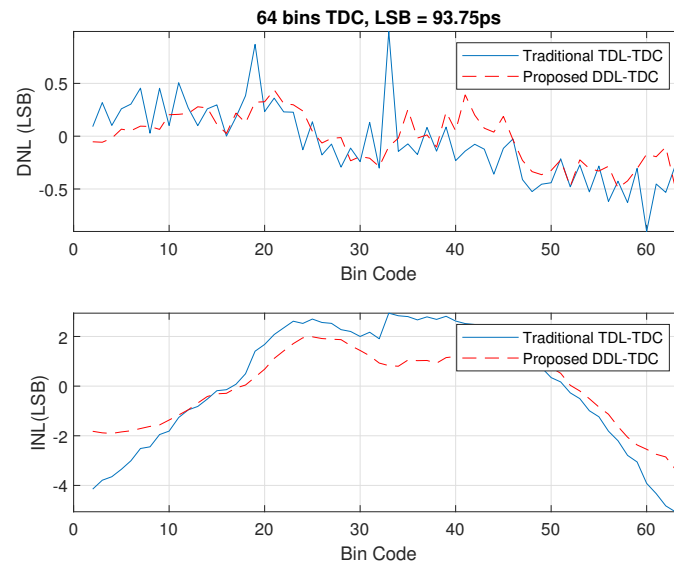


Figure 8. INL/DNL values obtained using the proposed DDL-TDC with 6-bit digital output.

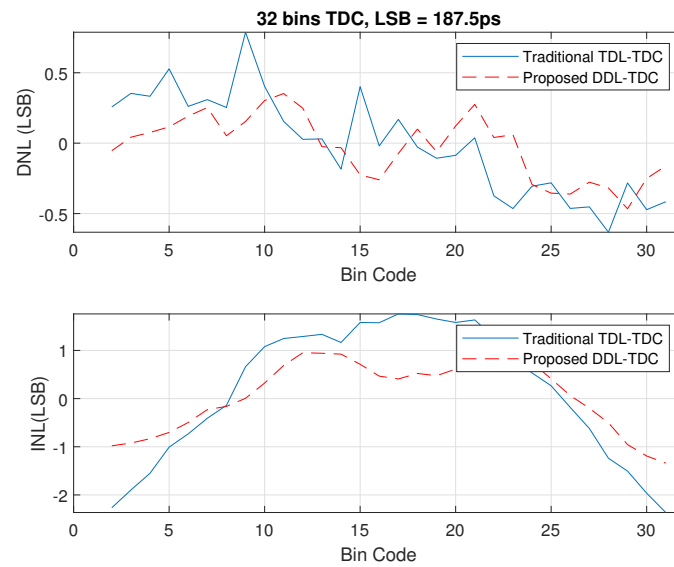


Figure 9. INL/DNL values obtained using the proposed DDL-TDC with 5-bit digital output.

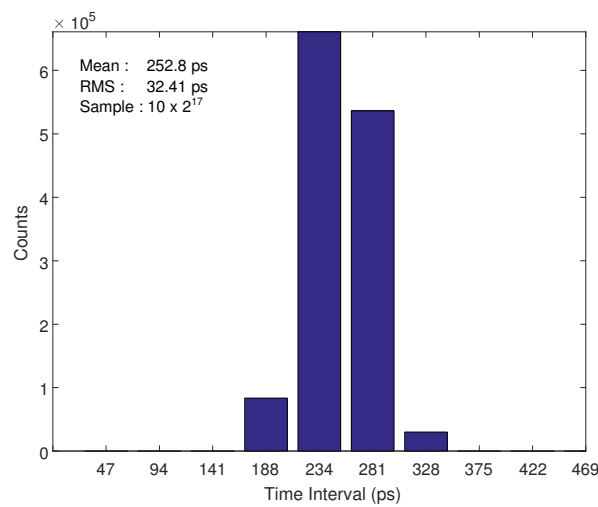
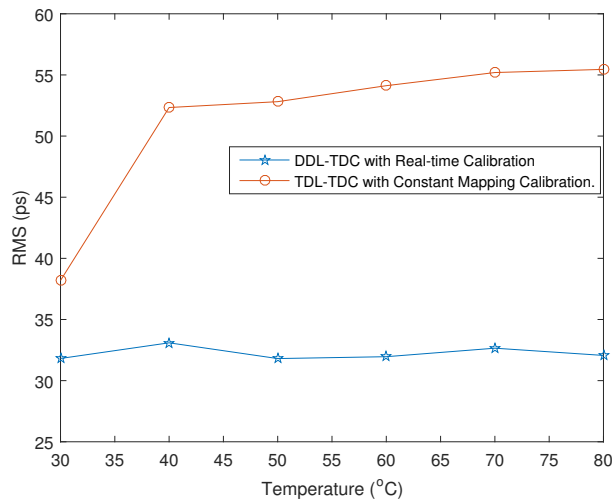


Figure 10. Measurements of constant delay for the proposed DDL-TDC.



**Figure 11.** RMS values obtained at various temperatures with 7-bit digital output.

In addition, the proposed DDL-TDC achieved high-resolution and high-linearity measurements. Thus, the time conversion range was only 6 ns, but a 32-ps resolution time was achieved for high-resolution measurements. The DDL-TDC could be augmented with an additional coarse counter to increase the conversion range for some applications that might require larger conversion range measurements. However, the fine time measurements would still use the DDL-TDC to maintain the high-resolution measurements.

#### 4. Conclusions

This paper proposes an FPGA-based DDL-TDC, which uses FSMs to calibrate the delay in each TDC delay cell to minimize DNL values. The two delay lines in the DDL circuit perform calibrations alternately, which allows calibrations to be made in real time. Experimental results demonstrated the efficacy of the proposed DDL-TDC in terms of DNL and INL values. The proposed scheme enables this DDL-TDC to manage dedicated nonuniform delay distribution in FPGA and thereby maintain a high degree of linearity in real time.

**Funding:** This research was funded by the Ministry of Science and Technology of Taiwan grant number 107-2221-E-182-066 and Chang Gung Memorial Hospital-Linkou grant number CMRPD2H0051, CIRPD2F0013, and CMRPD2G0312.

**Acknowledgments:** The authors would like to thank the Particle Physics and Beam Delivery Core Laboratory of the Institute for Radiological Research, Chang Gung University/Chang Gung Memorial Hospital, Linkou, for their assistance.

**Conflicts of Interest:** The author declare no conflict of interest.

#### References

1. Moses, W.W.; Buckley, S.; Vu, C.; Peng, Q.; Pavlov, N.; Choong, W.; Wu, J.; Jackson, C. OpenPET: A Flexible Electronics System for Radiotracer Imaging. *IEEE Trans. Nucl. Sci.* **2010**, *57*, 2532–2537. [[CrossRef](#)]
2. Sportelli, G.; Belcari, N.; Guerra, P.; Spinella, F.; Franchi, G.; Attanasi, F.; Moehrs, S.; Rosso, V.; Santos, A.; Del Guerra, A. Reprogrammable Acquisition Architecture for Dedicated Positron Emission Tomography. *IEEE Trans. Nucl. Sci.* **2011**, *58*, 695–702. [[CrossRef](#)]
3. Aguilar, A.; Garcia-Olcina, R.; Leiva, I.; Martinez, P.A.; Martos, J.; Soret, J.; Suarez, A.; Torres, J.; Benlloch, J.M.; Gonzalez, A. Optimization of a Time-to-Digital Converter and a coincidence map algorithm for TOF-PET applications. *J. Syst. Arch.* **2015**, *61*, 40–48. [[CrossRef](#)]
4. Junnarkar, S.S.; O'Connor, P.; Vaska, P.; Fontaine, R. FPGA-Based Self-Calibrating Time-to-Digital Converter for Time-of-Flight Experiments. *IEEE Trans. Nucl. Sci.* **2009**, *56*, 2374–2379. [[CrossRef](#)]
5. Yousif, A.S.; Haslett, J.W. A Fine Resolution TDC Architecture for Next Generation PET Imaging. *IEEE Trans. Nucl. Sci.* **2007**, *54*, 1574–1582. [[CrossRef](#)]

6. Marino, N.; Baronti, F.; Fanucci, L.; Saponara, S.; Roncella, R.; Bisogni, M.G.; Guerra, A.D. A Multichannel and Compact Time to Digital Converter for Time of Flight Positron Emission Tomography. *IEEE Trans. Nucl. Sci.* **2015**, *62*, 814–823. [[CrossRef](#)]
7. Ronchini Ximenes, A.; Padmanabhan, P.; Charbon, E. Mutually Coupled Time-to-Digital Converters (TDCs) for Direct Time-of-Flight (dTOF) Image Sensors. *Sensors* **2018**, *18*, 3413. [[CrossRef](#)]
8. Li, X.; Yang, B.; Xie, X.; Li, D.; Xu, L. Influence of Waveform Characteristics on LiDAR Ranging Accuracy and Precision. *Sensors* **2018**, *18*, 1156. [[CrossRef](#)]
9. Zhang, C.; Lindner, S.; Antolovic, I.M.; Wolf, M.; Charbon, E. A CMOS SPAD Imager with Collision Detection and 128 Dynamically Reallocating TDCs for Single-Photon Counting and 3D Time-of-Flight Imaging. *Sensors* **2018**, *18*, 4016. [[CrossRef](#)]
10. Adamo, G.; Busacca, A. Time Of Flight measurements via two LiDAR systems with SiPM and APD. In Proceedings of the 2016 AEIT International Annual Conference (AEIT), Capri, Italy, 5–7 October 2016; pp. 1–5.
11. Wang, H.; Zhang, M.; Liu, Y. High-Resolution Digital-to-Time Converter Implemented in an FPGA Chip. *Appl. Sci.* **2017**, *7*, 52. [[CrossRef](#)]
12. Wu, J. Several Key Issues on Implementing Delay Line Based TDCs Using FPGAs. *IEEE Trans. Nucl. Sci.* **2010**, *57*, 1543–1548. [[CrossRef](#)]
13. Kalisz, J.; Szplet, R.; Pasierbinski, J.; Poniacki, A. Field-programmable-gate-array-based time-to-digital converter with 200-ps resolution. *IEEE Trans. Instrum. Meas.* **1997**, *46*, 51–55. [[CrossRef](#)]
14. Kalisz, J.; Szplet, R.; Pelka, R.; Poniacki, A. Single-chip interpolating time counter with 200-ps resolution and 43-s range. *IEEE Trans. Instrum. Meas.* **1997**, *46*, 851–856. [[CrossRef](#)]
15. Song, J.; An, Q.; Liu, S. A high-resolution time-to-digital converter implemented in field-programmable-gate-arrays. *IEEE Trans. Nucl. Sci.* **2006**, *53*, 236–241. [[CrossRef](#)]
16. Favi, C.; Charbon, E. A 17ps time-to-digital converter implemented in 65nm FPGA technology. In Proceedings of the ACM/SIGDA International Symposium on Field Programmable Gate Arrays, Monterey, CA, USA, 22–24 February 2009; pp. 113–120.
17. Aloisio, A.; Branchini, P.; Cicalese, R.; Giordano, R.; Izzo, V.; Loffredo, S.; Lomoro, R. High-Resolution Time-to-Digital Converter in Field Programmable Gate Array. In Proceedings of the Topical Workshop on Electronics for Particle Physics, Naxos, Greece, 15–19 September 2008; pp. 383–387.
18. Wu, J.; Shi, Z. The 10-ps wave union TDC: Improving FPGA TDC resolution beyond its cell delay. In Proceedings of the IEEE International Symposium Circuits and Systems, Como, Italy, 5–9 October 2008; pp. 3440–3446.
19. Bayer, E.; Traxler, M. A High-Resolution (<10 ps RMS) 48-Channel Time-to-Digital Converter (TDC) Implemented in a Field Programmable Gate Array (FPGA). *IEEE Trans. Nucl. Sci.* **2011**, *58*, 1547–1552.
20. Zhang, M.; Wang, H.; Liu, Y. A 7.4 Ps FPGA-Based TDC with a 1024-Unit Measurement Matrix. *Sensors* **2017**, *17*, 865. [[CrossRef](#)]
21. Wang, J.; Liu, S.; Zhao, L.; Hu, X.; An, Q. The 10-ps Multitime Measurements Averaging TDC Implemented in an FPGA. *IEEE Trans. Nucl. Sci.* **2011**, *58*, 2011–2018. [[CrossRef](#)]
22. Tontini, A.; Gasparini, L.; Pancheri, L.; Passerone, R. Design and Characterization of a Low-Cost FPGA-Based TDC. *IEEE Trans. Nucl. Sci.* **2018**, *65*, 680–690. [[CrossRef](#)]
23. Wang, Y.; Liu, C. A 4.2 ps Time-Interval RMS Resolution Time-to-Digital Converter Using a Bin Decimation Method in an UltraScale FPGA. *IEEE Trans. Nucl. Sci.* **2016**, *63*, 2632–2638. [[CrossRef](#)]
24. Wang, Y.; Liu, C. A 3.9 ps Time-Interval RMS Precision Time-to-Digital Converter Using a Dual-Sampling Method in an UltraScale FPGA. *IEEE Trans. Nucl. Sci.* **2016**, *63*, 2617–2621. [[CrossRef](#)]
25. Chaberski, D. Time-to-digital-converter based on multiple-tapped-delay-line. *Measurement* **2016**, *89*, 87–96. [[CrossRef](#)]
26. Chaberski, D.; Zielinski, M.; Grzelak, S. The new method of calculation sum and difference histogram for quantized data. *Measurement* **2009**, *42*, 1388–1394. [[CrossRef](#)]
27. Chen, Y.H.; Lu, C.W.; Chang, T.Y.; Hsia, C. A High Resolution FPGA-Based TDC with Nonlinearity Calibration. In Proceedings of the IEEE International Symposium on Instrumentation & Measurement, Sensor Network and Automation, Sanya, China, 25–28 August 2012; pp. 44–47.

28. Chen, Y.H. A High Resolution FPGA-based Merged Delay Line TDC with Nonlinearity Calibration. In Proceedings of the IEEE International Symposium on Circuits System, Beijing, China, 19–23 May 2013; pp. 2432–2435.
29. Chen, Y.H. A counting-weighted calibration method for a field-programmable-gate-array-based time-to-digital converter. *Nucl. Instrum. Methods Phys. Res. Sect. A* **2017**, *854*, 61–63. [[CrossRef](#)]
30. Chen, Y.H. Run-time calibration scheme for the implementation of a robust field-programmable gate array-based time-to-digital converter. *Int. J. Circuit Theory Appl.* **2018**. [[CrossRef](#)]
31. Won, J.Y.; Kwon, S.I.; Yoon, H.S.; Ko, G.B.; Son, J.W.; Lee, J.S. Dual-Phase Tapped-Delay-Line Time-to-Digital Converter With On-the-Fly Calibration Implemented in 40 nm FPGA. *IEEE Trans. Biomed. Circuits Syst.* **2016**, *10*, 231–242. [[CrossRef](#)] [[PubMed](#)]
32. Xilinx. *Virtex-5 FPGA User Guide*, version 5.4; UG 190; Xilinx Inc.: San Jose, CA, USA, 2012.
33. Seo, Y.H.; Kim, J.S.; Park, H.J.; Sim, J.Y. A 1.25 ps Resolution 8b Cyclic TDC in 0.13  $\mu\text{m}$  CMOS. *IEEE J. Solid-State Circuits* **2012**, *47*, 736–743. [[CrossRef](#)]



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