

Article

Optimum Layout of Low Power LC-Based Digitally Controlled Oscillator for Bluetooth Low Energy in a 4G/5G LTE System

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Abstract: This paper presents an optimum layout method of a low-power, digitally controlled oscillator (DCO) for a Bluetooth low-energy (BLE) transceiver in a 4G/5G LTE system. For the optimal LC-based DCO layout, three different layouts, including different g_m cell locations and an Al metal layer, were implemented, and performance was compared and verified for BLE application. The implemented neck DCO (NDCO), where the g_m cell is located in the neck of the main inductor, showed superior performance compared to other layouts in terms of low phase noise and low power consumption. The designed NDCO had a low phase noise of -116.1 dBc/Hz at 1 MHz with a 0.5 mW power consumption. The supply voltage and oscillation frequency range were 0.8 V and 4.7–5.7 GHz, respectively, and the NDCO designed with the optimal layout had a good figure-of-merit of -192.6 dBc/Hz.

Keywords: bluetooth low energy (BLE) transceiver; digitally controlled oscillator (DCO); g_m cell; layout; IoT; 4G/5G LTE; embedded system



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1. Introduction

Bluetooth low-energy (BLE) applications are wireless, home area network (WHAN)-based technologies for communication with a short transmission distance in 5G/Internet of Things (IoT) wireless technology [1]. These systems require a low-power, all-digital phase locked loop (ADPLL) circuit, with many studies demonstrating improved low power and low phase noise performance using these circuits [2–5]. The performance of all-digital PLLs, including frequency resolution, low phase noise, and low power consumption, is determined by the digitally controlled oscillator (DCO) [2], because the DCO block is a sub-block circuit in the ADPLL and is important in terms of power consumption, phase noise, and oscillation frequency range. Recently, DCOs were widely employed because of their fast design time, efficient chip area, and low cost [2]. The layout of a typical DCO requires a design that reflects on/off parasitic capacitance switching in the capacitor bank, high-Q inductor in the LC tank, parasitic components on the layout, and the burden of a large control circuit area, which were previously studied in the literature [2–5].

A low-power, high-resolution DCO was designed using a current reuse structure and a multistage capacitor reduction technique. However, in a multistage capacitor using a unit variable capacitor, it is difficult to implement a small capacitor for high resolution and it is sensitive to parasitic effects [4]. Previous studies [5–8] on DCOs focused on optimizing the circuit or structures. The performance-enhancing technologies of circuit and structure optimization require a large die area due to the large inductor and capacitor array (LC tank), and a control circuit to ensure a wide oscillation frequency range and excellent phase noise performance. Additional parasitic components were generated due to the connecting metal lines required in the layout, resulting in poor performance of the DCO. The g_m cell required to compensate for these parasitic components is a design consideration to improve the DCO performance. However, the g_m cell location was designed inconsistently (the

DCO connected to the tail of the LC tank or the DCO at the neck of the inductor) and did not present optimum conditions for excellent performance.

In this paper, we present a DCO design layout based on the measurement results for layout optimization using g_m cell locations and an Al metal layer. When the g_m cell is located after the main inductor and the capacitor bank, it is difficult to predict the performance of the DCO due to the parasitic line inductance generated between the main inductor and the capacitor bank. The rest of this paper is organized as follows: Section 2 describes the advantages and disadvantages of each g_m cell location. Section 3 covers the LC-based DCO design and configuration of the capacitor bank with the optimum layout. Section 4 describes the tests of the DCOs used to verify the key idea of this paper, and discusses measurement results and considerations. Finally, Section 5 is the conclusion of this paper.

2. Layout Issues of Low-Power LC-Based DCO

2.1. Determine Location of g_m Cell

In terms of phase noise performance, the voltage swing of the LC tank can be described as tank energy. A low noise-to-carrier ratio (NCR) describes the relationship with tank energy as:

$$\frac{(V_n^2)}{(V_{tank}^2)} = \frac{1}{E_{tank}} \quad (1)$$

where V_n is the noise voltage, V_{tank} is the voltage swing level, and E_{tank} is the energy of the LC tank. As shown in Equation (1), as E_{tank} increases, V_n , the noise factor, should be reduced. The phase noise at the offset frequency is:

$$L\{F_{offset}\} = \frac{g_L^2}{I_{bias}} \quad (2)$$

where F_{offset} is the offset frequency of the oscillation frequency and g_L is a loss of the inductor. To reduce the phase noise and power consumption, g_L should reduce the loss of the inductor, as shown in Equation (2). The inductor in the LC tank, which affects the phase noise and output signal power, was designed with various types of inductor for high-Q design [6,7]. A high-Q inductor using the embedded wafer level ball grid array (eWLB) package inductor was implemented due to its excellent phase noise and higher voltage swing, but its power consumption was large [6]. Conversely, the 3D helical inductor was smaller and low-power, but did not have excellent phase noise with a low Q-value [7]. The design of the inductor was critical, but the layout with a small coupling capacitor and a small metal resistance increased the area of the inductor because it was designed with a wide metal layer and little mutual coupling between metals. However, chips in low-cost applications have limitations on chip size, making it impossible to use a relatively large inductor. Therefore, an optimal-sized inductor must be designed that includes appropriate losses, and a large g_m cell structure must be selected that can compensate for the losses. Here, the capacitor in the LC tank had a high Q and could be neglected.

In LC-based oscillator design, as shown in Figure 1, Complementary metal-oxide-semiconductor (CMOS) architectures are conventionally employed for low power consumption because they can have double the g_m compared with other architectures, such as N type MOSFET (NMOS)- and P type MOSFET (PMOS)-type g_m -cell architecture. Fabricated DCOs also adopt a complementary architecture for low power consumption and use bonding-wire degeneration inductors (L_s) to reduce chip area instead of using spiral tail inductors.

The left side of Figure 1 shows a schematic of a DCO with three capacitor banks, i.e., the most significant bit (MSB) bank, the least significant bit (LSB) bank, and the fine bank. The largest switched capacitor is located near the main inductor for linear frequency change and chip area efficiency. In the layout of the DCO on the right side of Figure 1, the NMOS- and PMOS-type g_m cells can be placed in either the tail of the capacitor bank or

the neck of the inductor. The DCO located at the tail of the capacitor bank is the tail-DCO (TDCO) and the DCO located at the neck of the inductor is the neck-DCO (NDCO).

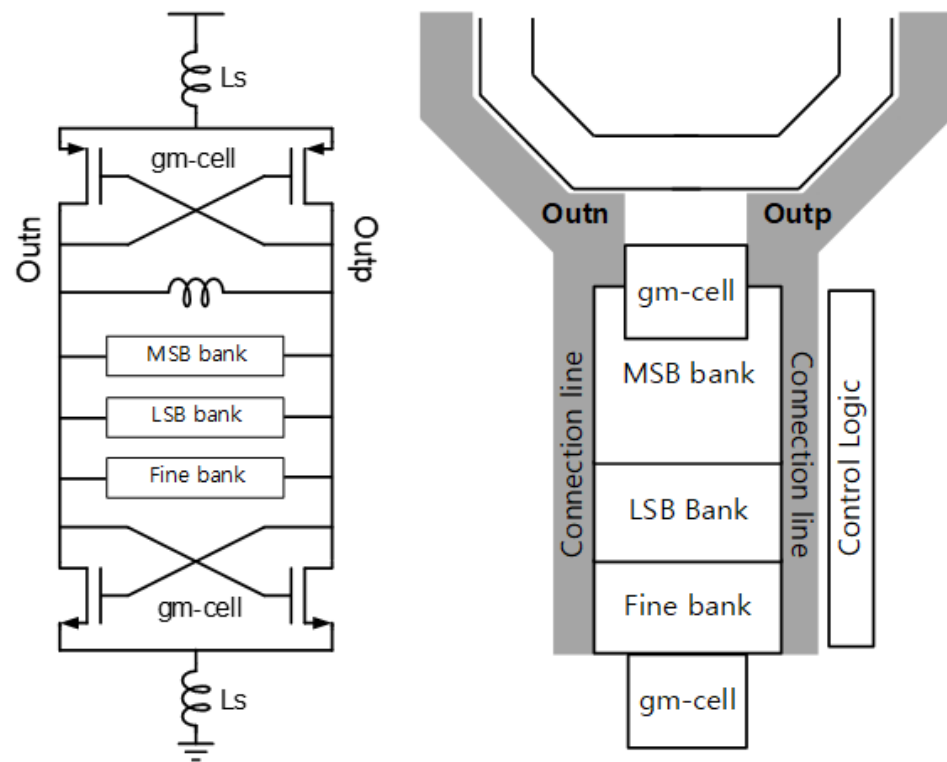


Figure 1. The general CMOS complementary digitally controlled oscillator (DCO) architecture and layout.

The LC resonant circuit is the key circuit that determines the oscillation frequency of the DCO, and consists of a main inductor and a bank of capacitors for frequency selection. The maximum frequency of the DCO is oscillated under the condition that all switches in the capacitor bank are turned off, and the minimum frequency is oscillated under the condition that all switches in the capacitor bank are turned on. Figure 2a shows the TDCO with the g_m -cell circuit after the main inductor and capacitor banks. This creates an additional parasitic inductance between the main inductor and capacitor banks in the designed LC resonant circuit. As shown in Figure 2a, the maximum frequency shifts to a lower oscillation frequency under the condition that all switches are turned off by the added parasitic inductance. In the case of parasitic resistance and capacitance, ultra-thick metal (UTM) layers with small sheet resistance have small parasitic resistance values, and the parasitic capacitance is also ignored as a CMOS vertical structure between the ultra-thick metal (UTM) and substrate. Therefore, the tuning range of the oscillation frequency of the TDCO is reduced, and should be sufficiently considered in DCO design. However, the layout arrangement of the drive buffer can maintain symmetry with differential output signals.

Conversely, in Figure 2b, the g_m -cell circuit of the NDCO is located in the middle of the main inductor and capacitor bank. This excludes the parasitic line inductance generated between the inductor and capacitor bank because all switches of the capacitor banks are turned off by high impedance. So, the DCO without parasitic line inductance has an oscillation frequency range with an LC resonant circuit, as designed. However, phase mismatch between differential signals can occur due to the asymmetry of the drive buffer connection.

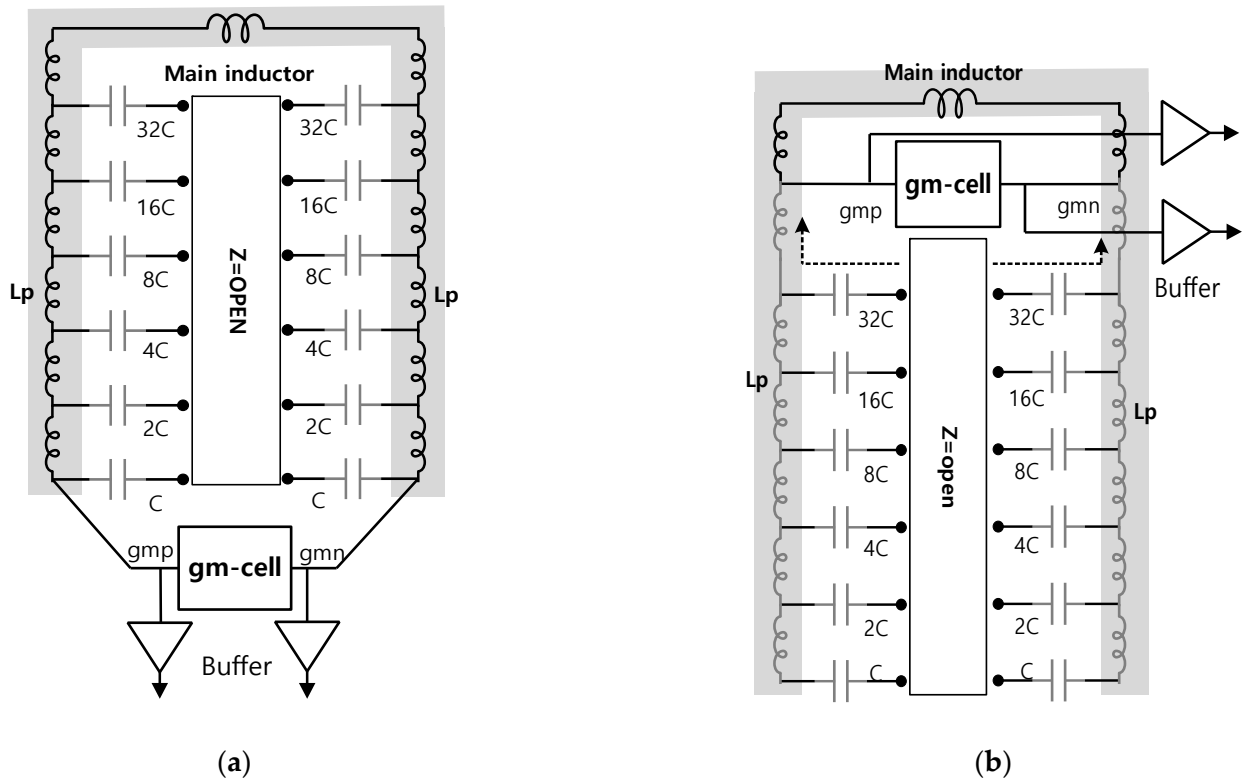


Figure 2. Equivalent circuit of a DCO including parasitic line inductance (L_p): (a) g_m cell is located in tail of the capacitor bank; (b) g_m cell is located in the neck of the inductor.

2.2. Layout Method for High-Linear-Frequency Control

The high-frequency DCO is one sensitive circuits where oscillation frequency can be changed by parasitic components generated in the layout. In particular, the parasitic components of routing metal are some of the important design parameters to be considered in the DCO because it is difficult to design an LC resonance circuit that can be linearly adjusted according to the parasitic line inductance (L_p).

$$\omega_{DCO}^2 = \frac{1}{(L_s + L_p)(C_{var} + C_p)} \quad (3)$$

where L_s is the main inductor and C_{var} and C_p are the capacitor and parasitic capacitance of the switching capacitor in the capacitor bank, respectively. Here, the ratio between the maximum frequency and the minimum frequency can be expressed as:

$$\frac{\omega_{DCO,minfreq.}^2}{\omega_{DCO,maxfreq.}^2} = \frac{C_p(L_s + L_p)}{C_{var}(L_s + L_p) + L_s} \quad (4)$$

In Equation (4), the oscillation frequency of the DCO shifts according to the parasitic inductance. In addition, it has a nonlinear oscillation frequency due to the different parasitic inductances according to the position of the switches. The capacitor bank, including a linear capacitor unit, has a nonlinear oscillation frequency due to unexpected parasitic line inductance. As a method for minimizing the parasitic component of the routing metal, an ultra-thick metal (UTM) layer or Al metal layer commonly used metal options due to their low resistivity. In addition, a previous study [9] showed that using aluminum (Al) is a suitable method to reduce the parasitic inductance in LC resonance circuits.

For example, as shown in Figure 2a, the TDCO layout effectively reduced the parasitic inductance component using an Al metal layer. The capacitor bank circuit was covered by the Al metal layer to reduce the parasitic line inductance between the main inductor and

the capacitor bank. It shortened the parasitic inductance, as shown in Figure 3. Capacitor banks, including short-circuit effects, have the desired oscillation frequency range due to parasitic inductance reduction. To verify this effect, we compared and verified the effect on reducing parasitic inductance by adding Al metal to the TDCO layout. For accurate parasitic extraction, an electromagnetic (EM) simulator can be used. However, this process requires a long simulation run-time and a complex setup. For accurate prediction of the results, implementation and simulation must be synchronized. Therefore, we compared the performance of the Al metal layer using actual fabrication and measurement without using EM simulation.

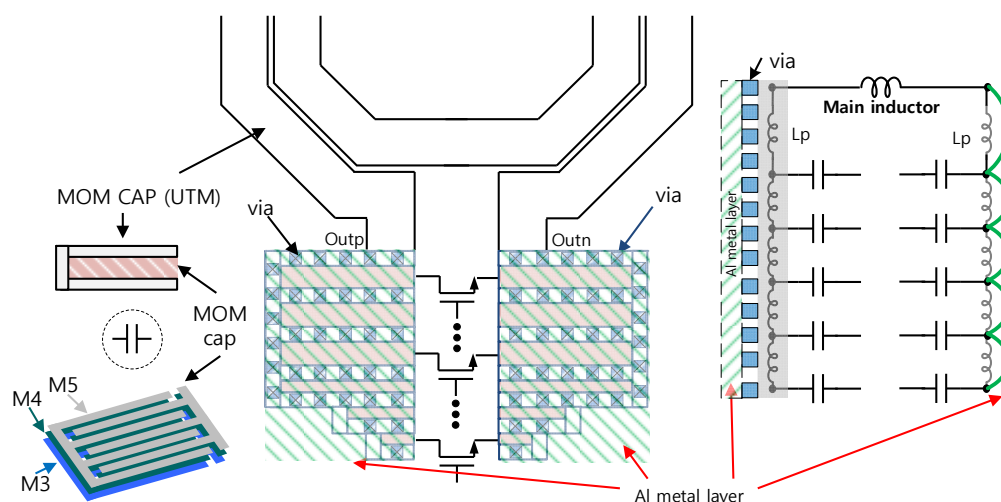


Figure 3. Layout and equivalent circuit using a metal Al layer.

3. DCO Design

Figure 4 shows a simplified schematic with three capacitor banks, i.e., the MSB, LSB, and fine bank. All capacitor banks were designed with unit-weighted instead of binary-weighted structures to ensure linearity in the frequency step. Even though the area of the unit-weighted capacitor bank is slightly larger than that of the binary capacitor bank, it presents many merits in terms of linearity and flexibility in design [10]. For example, to change the capacitor required for linear oscillation frequency control, all unit capacitor sizes in the capacitor bank were changed, maintaining constant the ratios of capacitor sizes, such as unit $\times 1$, $\times 2$, $\times 4$, and $\times 8$ [10]. However, in the unit-weighted structure, the optimum capacitor unit value considering the parasitic components generated in the layout can be individually applied to optimize performance. For linearity and reliability, the unit capacitor contains inverter logic to bias the source and gate of the switch. Assuming a voltage swing (V_{pp}) of 0.8 at the output node and a supply voltage for the inverter logic of 1.2 V, when the switch was turned off, the turn-off-resistance of the switch was a few mega ohms, and the V_{gs} of the switch produced a voltage swing from -1.6 to -0.8 V based on the 1.2 V supply. Ensuring the V_{gs} reliability of a low-voltage threshold (LVT) switch with low turn-on resistance is difficult, therefore, a thick-oxide metal-oxide semiconductor FET (MOSFET) switch was used for the large signal swing of the DCO. However, the thick-oxide MOSFET switch increases the turn-on resistance and layout area, which complicates the design of the capacitor bank. To solve the reliability problem [8], if it is possible to supply a voltage lower than 1.2 V on the source voltage, an LVT switch with a low turn-on-resistance can be used. For this purpose, the supply voltage of the source inverter was 0.8 V, the same as the voltage of the DCO, and a different supply voltage from the inverter voltage for the gate was applied, as shown in Figure 4. This helped to improve the linearity and reliability of the DCO through a simple configuration power separation scheme. To reduce the mismatch between unit capacitors, the unit capacitor and control circuit should be

arranged separately in the layout. This separation makes the arrangement conditions of all unit capacitors the same.

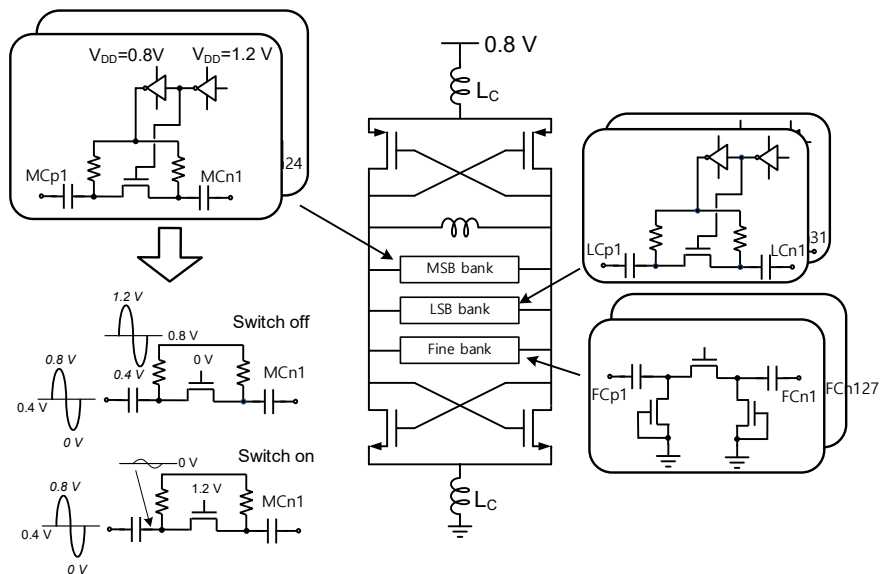


Figure 4. Structure and operation principle of the switch and control circuit for tuning the capacitor in a capacitor bank.

Figure 5 depicts a useful method for reducing the mismatches between unit capacitors. In this design, the electrical control part and the unit capacitor cells were separated. The circles in Figure 5 represent a unit capacitor cell, which consisted of a switch, two capacitors, and two DC-blocking resistors. All these unit cells were located inside the capacitor dummy guard. The dummy was composed of unit cells that were the same size as those used for oscillation frequency tuning. This capacitor dummy layout was a layout technique for making all the coupling effects generated by the metal layer the same. In addition, the control logic blocks were located as far as possible outside the dummy for separation. When the electrically isolating layout was adopted, the randomness of the oscillation frequency was reduced, as shown in earlier studies of fabricated DCOs [8]. This layout method was applied to all capacitor banks, such as the MSB, LSB, and fine frequency tuning banks.

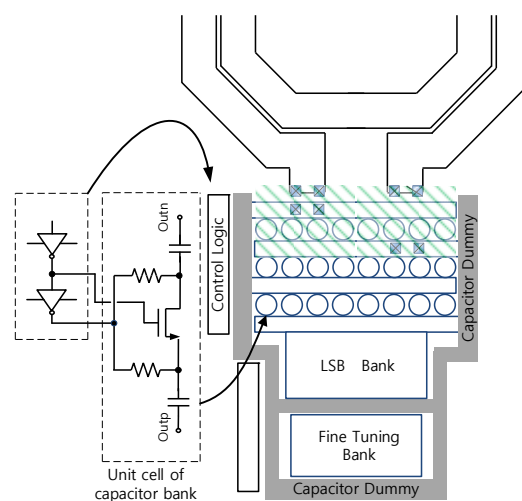


Figure 5. Layout for high isolation between the unit capacitor cell and the control circuit.

4. Implementation and Measurement Results

To verify the effect of the proposed layout methods, three DCOs were implemented in then 55 nm CMOS process, as shown in Figure 6, and measured by a digitally controlled, embedded system. The DCOs were designed with the same inductor, capacitor banks, g_m cell, and output buffers. The NDCO on the left of Figure 6 had a g_m cell in the neck of inductor and the TDCO in the middle had a g_m -cell in the tail of the capacitor bank. The Al-metal DCO (AIDCO) on the right of Figure 6 had a g_m cell in the tail of the capacitor bank, which was applied to the Al metal layer for high linear frequency tuning.

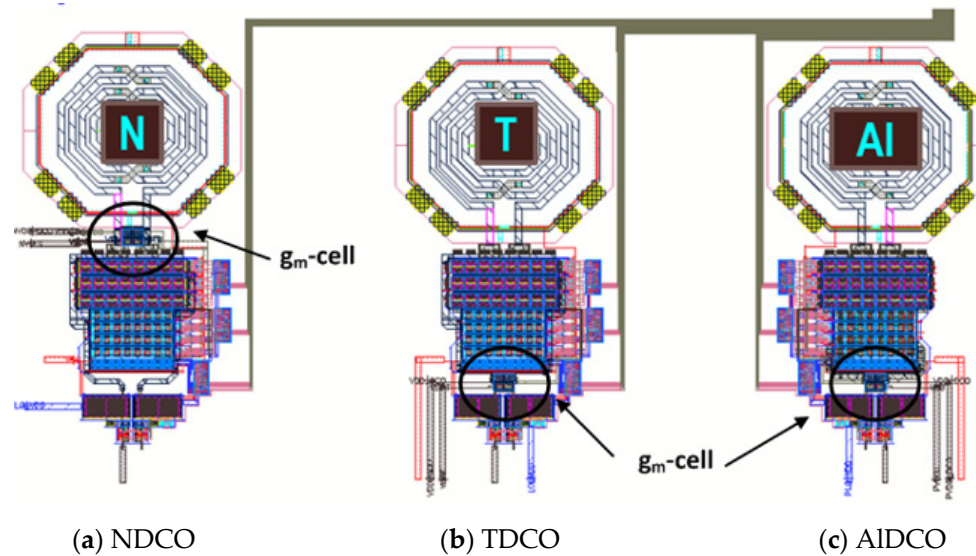


Figure 6. The layout of the designed DCOs.

Figure 7 shows a chip picture of the designed DCOs. The NDCO and TDCO were designed with a layout area of $0.072 \mu\text{m}^2$ and the AIDCO with a layout area of $0.06 \mu\text{m}^2$, all integrated into one chip for comparison. For accurate performance comparison, the main inductor, capacitor bank, and g_m cell in the DCO were used identically.

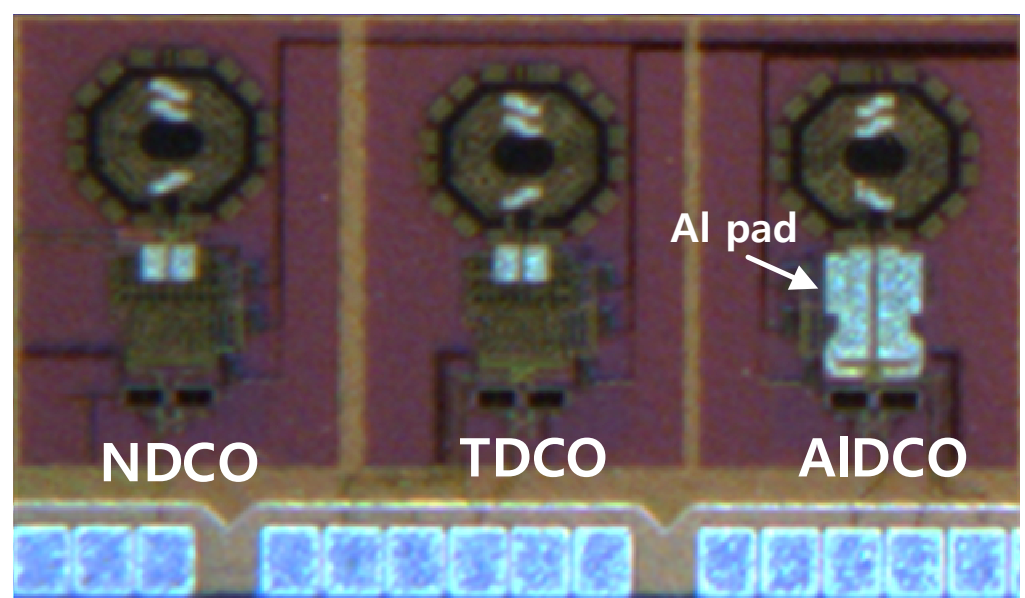


Figure 7. The die photo of the designed DCOs.

Figure 8 shows the oscillation frequency range and the change in frequency according to the digital code. As shown in Figure 8a, the difference of measured maximum oscillation frequency was only 23 MHz between NDCO and TDCO. However, AIDCO presented a 347 MHz difference in maximum oscillation frequency compared to NDCO. The oscillation frequency range of NDCO and TDCO was about 923 MHz, and AIDCO was measured as having an oscillation frequency range of 775 MHz. Figure 8b shows the slope of the frequency according to the digital code. AIDCO showed a relatively linear frequency change compared to NDCO and TDCO, as expected, due to the additional AI layer. However, the maximum oscillation frequency was 148 MHz lower than that of other DCOs. In general, capacitor banks have small capacitor values at low digital codes. It becomes difficult to attain linear frequency control given the parasitic inductance of the layout. As shown in Figure 8b, the AIDCO produced a linear result at a relatively low digital code compared to the other DCO layouts. The results showed that the additional AI metal layer produced a linear frequency change effect but had a lower maximum frequency due to the parasitic capacitor generated between the capacitor banks. As such, when designing a DCO using an AI metal layer, a sufficient frequency margin should be considered.

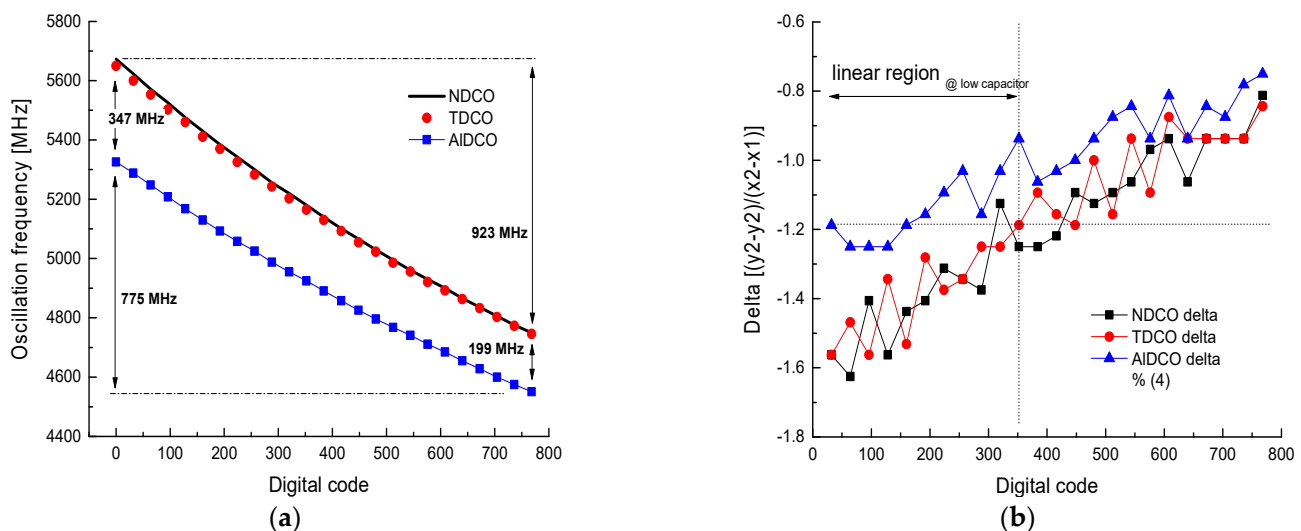


Figure 8. Measurement of three test DCOs: (a) oscillation frequencies and (b) linear frequency control.

Figure 9 shows the phase noise of the designed NDCO at 4.8 GHz. The DCO exhibited low phase noise of -116.1 dBc/Hz at 1 MHz with a 0.8 V supply voltage. The overall performance of the DCOs can be represented by a figure-of-merit (FoM) as follows [11]:

$$FoM = -PN(f_{offset}) + 20 \log \left(\frac{f_0}{f_{offset}} \right) - 10 \log \left(\frac{P_{DC}}{1mW} \right) \quad (5)$$

The FoM of the designed NDCO was superior to that of the other DCOs. Since the NDCO had a g_m cell in the neck of the inductor, the Q-factor of main inductor degraded less than that of the tail of the capacitor bank. The high Q-factor of the LC-tank resulted in the high performance of the NDCO.

Table 1 compares the performance of the measured DCOs, showing that the DCO consumed less power and had superior phase noise compared to existing designs, with a high FoM index.

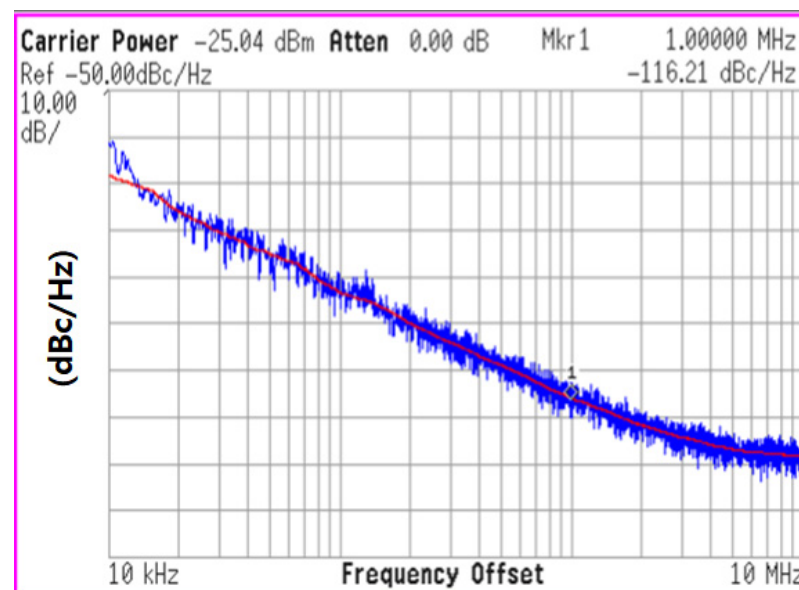


Figure 9. Measurement result of phase noise in an NDCO.

Table 1. Summary of performances of designed DCOs and comparison with previous works. FoM, figure-of-merit.

Parameter	NDCO	TDCO	AIDCO	JSSC 2014 [12]	JSSC 2015 [13]
Frequency (MHz)	4750–5673	4746–5650	4551–5326	4450–7100	4400–5400
Tuning range (%)	17.8%	17.4%	15.6%	45.8%	20.4%
Current (mA) with 0.8 V supply voltage	0.66	0.73	0.75	N/A	N/A
PD * (mW) with 0.8 V supply voltage	0.5	0.58	0.6	1.2	1.65
Phase noise (dBc/Hz) at 4.8 GHz	−116 at 1 MHz	−114 at 1 MHz	−113.5 at 1 MHz	−104 at 1 MHz	−120 at 1 MHz
FoM (dBc/Hz)	192.6	190	189	180	193
CMOS process	55 nm		65 nm		
Area (mm ²)	0.07		0.06		0.19

* PD: power dissipation.

5. Conclusions

In this paper, the optimal g_m cell position for the performance of the DCO and an Al metal layer for linear frequency control were implemented and compared using the 55 nm CMOS process. The fabricated DCOs presented different oscillation frequency ranges, phase noises, and power consumptions depending on their layout. According to the results, the DCO's layout for BLE seems to be suitable for NDCOs, with the g_m cell located at the neck of the inductor and a frequency tuning range of 17.8%, power consumption of 0.5 mW, and excellent noise performance of 116 dBc/Hz. For the TDCO, power consumption and phase noise of 0.58 mW and 114 dBc/Hz were recorded, respectively. The AIDCO for linear frequency control showed relatively poor performance, with 0.6 mW power consumption and 113.5 dBc/Hz phase noise, but showed a linear frequency change compared to the other DCOs.

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