Dual-Mode Control Scheme to Improve Light Load Efficiency for Dual Active Bridge DC-DC Converters Using Single-Phase-Shift Control

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Abstract: In vehicle-to-grid (V2G) applications, dual active bridge (DAB) converters are commonly used as the power interface because they offer high efficiency, galvanic isolation, and bidirectional power flow. For the DAB control strategy, phase-shift control is the mainstream, especially the single-phase-shift (SPS) method because of its ease of implementation. However, due to the phase shift, a DAB converter operated under this control method has relatively high backflow power, resulting in poor efficiency. The SPS control method has the drawback of high backflow power, especially at light loads. Thus, this paper proposes a new dual-mode control scheme to improve the light load efficiency of DAB converters by taking advantage of the pulse-width modulation (PWM) strategy in combination with the conventional SPS strategy for DAB converters based on load conditions. In other words, when the DAB converter operates under light load conditions, the PWM control strategy is used to avoid considerable backflow power. A prototype DAB converter with a power rating of 1 kW under a switching frequency of 100 kHz interfacing a DC bus (400 V) and a battery pack (50 V) is designed and implemented to verify the feasibility of this control strategy. A detailed analysis of the working principle and design parameters of the proposed converter is provided in this paper. Experimental results show that the highest efficiency of the proposed converter at light loads (10–200 W) was 96.2% for the forward power conversion and 97.3% for the backward power conversion.

Keywords: dual-mode control; dual active bridge converter; single-phase-shift; pulse-width modulation

1. Introduction

Nowadays, countries around the world are constantly seeking ways to utilize energy efficiently and reduce environmental impacts associated with carbon emissions. One of the most popular solutions today is using the smart grid, which provides a sustainable, reliable, economical, and environmentally friendly power grid [1]. The ability to connect electric vehicles (EVs) to the grid is one of the key features of a smart grid, which reduces emissions and fossil energy consumption. In a smart grid, EVs can be regarded as mobile energy storage. By connecting EVs to the grid, the overall energy utilization rate can be improved.

Since power electronics technology has evolved rapidly in recent years, DC/DC converters have been widely used in EVs, energy storage systems, energy conversion systems, DC distributed power systems, and power transmission systems. Moreover, DC-DC converters even appear in applications such as inverters [2]. One of the most popular
topologies used in the DC/DC converter is the dual active bridge (DAB). Due to the attractive characteristics such as zero-voltage switching (ZVS) of all power switches, near-minimal voltage and current stress, galvanic isolation with bidirectional power flow, low number of passive components as well as a high voltage conversion ratio [3–9], the DAB converter is widely used as the power interface for EVs in V2G systems. A DAB converter topology typically consists of a high-frequency transformer and two active full-bridge rectifiers, as shown in Figure 1. The DAB converter has bidirectional energy transmission characteristics, and it is commonly controlled by phase-shift control to change its transferred power.

![Figure 1. The DAB converter topology.](image)

There are numerous phase-shift control methods applied to DAB converters. Generally, they can be categorized as SPS control, extended-phase-shift (EPS) control, dual-phase-shift (DPS) control, and triple-phase-shift (TPS) control. Among these control methods, the SPS control method is the most widely used due to its advantages, such as ease of implementation, simple algorithms used, soft switching capabilities, etc. In the SPS control method, diagonally opposite switches on each full-bridge are controlled to create a leading or lagging phase of the primary side voltage relative to the secondary side voltage of the transformer to control power flow direction and magnitude. The phase difference between the voltages on the primary side $V_P$ and the secondary side $V_S$, the so-called phase-shift angle, $\theta$, is the only variable that can be controlled, as shown in Figure 2.

![Figure 2. Control waveforms of SPS control.](image)

When the control signal of the full-bridge rectifier on the primary side of the transformer is ahead of the control signal of the full-bridge rectifier on the secondary side of
the transformer, the energy is transferred from the DC bus to the energy storage (battery pack). Conversely, when the control signal of the full-bridge rectifier on the secondary side of the transformer precedes that of the full-bridge rectifier on the primary side of the transformer, energy is transferred from the energy storage to the DC bus. With the aim of achieving ZVS for power switches, auxiliary inductor \( L_s \) serves as a means of transferring and storing energy.

However, the disadvantage of SPS is the occurrence of backflow power caused by the circulating current. There are periods during the power transfer process when the transformer’s primary side voltage \( V_p \) and inductor current \( i_{LK} \) are in opposing directions, causing the energy stored in auxiliary inductor \( L_s \) to return to the input (DC bus), as shown in Figure 3. As the transmission power remains constant, the greater the backflow power, the greater the required forward transmission power. The backflow power also leads to higher current stress on the power switches, causing an increase in conduction loss and the magnetic loss of the transformer, resulting in lower converter efficiency, especially at light loads.

![Figure 3. Backflow power in SPS control.](image)

For better efficiency of DAB converters at light load, several control strategies were developed, such as EPS control [10,11] or series resonant dual-active bridge (SRDAB) converters [12,13]. EPS control can effectively reduce the current stress and reactive power and thus increase the system efficiency, but the phase-shift degrees of freedom also increase. This control method adds another degree of freedom to the converter by adjusting the time sequence between the gate signals of diagonal power switches to enhance flexibility. Ref. [10] proposed a minimum-backflow-power under extended-phase-shift control (MEPS) strategy to minimize the backflow power and improve the efficiency in a wide operating range. Ref. [11] presented a three-degree-of-freedom control method for DAB converters to achieve full load range ZVS under a wide voltage range. However, in practice, control complexity is high because of the number of coupled variables, making it difficult to implement. In terms of resonant converters, Ref. [12] introduced a symmetrical CLLC resonant tank on the DAB with pulse frequency modulation (PFM) control to achieve soft switching during bidirectional power conversion. In [13], a dual-bridge series resonant DC-DC converter (DBSRC) developed by modifying the topology of the traditional DBSRC was introduced. The proposed circuit presents higher voltage gain, a wider soft-switching region, and larger output power than the traditional DBSRC. However, the resonant converter commonly uses variable frequency control methods, which generate higher harmonics. As a result, the converter requires the use of more complex designed EMI suppression filters. To improve efficiency at light loads while taking advantage of the large power transmission capacity of SPS control, a fixed-frequency dual-mode control strategy is proposed in this paper, enabling the DAB converter to switch the operation mode based on the load. For example, the DAB converter operating at light loads is controlled by using PWM control. Nevertheless, when the converter is under medium-to-full
load, the DAB converter is controlled by using the SPS control. Table 1 shows a comparison of the related studies.

Table 1. Comparison of the DAB converter with different control strategies.

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>Topology</td>
<td>DAB</td>
<td>DAB</td>
<td>SRDAB</td>
</tr>
<tr>
<td>Control strategy</td>
<td>Dual-mode PWM-SPS</td>
<td>MEPS</td>
<td>PFM</td>
</tr>
<tr>
<td>Transformer type</td>
<td>Conventional transformer</td>
<td>Solid-state transformer</td>
<td>Conventional transformer</td>
</tr>
<tr>
<td>Prototype power rating</td>
<td>1 kW</td>
<td>200 W</td>
<td>1 kW</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>100 kHz</td>
<td>20 kHz</td>
<td>70–150 kHz</td>
</tr>
<tr>
<td>Maximum efficiency</td>
<td>97.30%</td>
<td>approx. 90.00%</td>
<td>94.60%</td>
</tr>
</tbody>
</table>

This paper is structured as follows:

Section 1 introduces the DAB converter topology and its control strategies. This section also briefly mentions the purpose of this study and the paper structure. Section 2 describes the operation of the dual-mode control strategy for the DAB converter, along with its related circuit analysis. Section 3 presents the design procedure of the prototype converter. Section 4 establishes the power loss model of the converter. In section 5, the experimental results prove the feasibility of the proposed dual-mode control strategy for the DAB converter. Moreover, the experimental data show that the light load efficiency of the proposed control strategy is higher than that of the traditional SPS control strategy. Section 6 concludes the paper.

2. Operating Principle of the Proposed Dual-Mode Control Strategy for the DAB Converter

The operating principle of the proposed dual-mode control strategy for the DAB converter breaks down into two parts: light load and medium-to-full load.

Since forward power conversion and backward power conversion operate similarly, the analysis will focus on the forward power conversion (power transferred from the DC bus to the battery pack). Figure 4 depicts the structure of the DAB converter for analysis. The components are defined as follows:

1. $S_1$, $S_2$, $S_3$, and $S_4$ are power switches of the high voltage full-bridge.
2. $S_5$, $S_6$, $S_7$, and $S_8$ are power switches of the low voltage full-bridge.
3. $D_1$, $D_2$, $D_3$, and $D_4$ are the intrinsic diodes of power switches $S_1$, $S_2$, $S_3$, and $S_4$ of the high voltage full-bridge, respectively.
4. $D_5$, $D_6$, $D_7$, and $D_8$ are the intrinsic diodes of power switches $S_5$, $S_6$, $S_7$, and $S_8$ of the low voltage full-bridge, respectively.
5. $C_{oss1}$, $C_{oss2}$, $C_{oss3}$, and $C_{oss4}$ are the parasitic capacitances of power switches $S_1$, $S_2$, $S_3$, and $S_4$ of the high voltage full-bridge, respectively.
6. $C_{oss5}$, $C_{oss6}$, $C_{oss7}$, and $C_{oss8}$ are the parasitic capacitances of power switches $S_5$, $S_6$, $S_7$, and $S_8$ of the low voltage full-bridge, respectively.
7. $L_M$ is the magnetizing inductance of the transformer.
8. $L_k$ is the sum of transformer leakage inductance and auxiliary inductance.
9. $V_{DCbus}$ is the voltage of the DC bus (high-voltage side).
10. $V_{Bat}$ is the voltage of the battery pack (low-voltage side).
2.1. Light Load

Under light load conditions, the proposed DAB converter adopts the PWM control to drive two full-bridges, which lowers the loss of backflow power and improves the efficiency of the DAB converter. Figure 5 demonstrates the theoretical waveforms of the proposed control strategy for the DAB converter in PWM mode under light load conditions.

State 1 ($0 \leq t \leq t_1$):
As shown in Figure 5, due to the discharge of energy stored in $C_{OSS1}$, $C_{OSS4}$, $C_{OSS5}$, and $C_{OSS8}$ to zero during the dead time in the previous state, switches $S_1$, $S_4$, $S_5$, and $S_8$ are
turned on with ZVS at $t = t_0$. Since $L_M$ and $L_K$ have not discharged their stored energy completely, currents $i_{LM}$ and $i_{LK}$ keep flowing in the same direction as their previous state until their stored energy is discharged to zero. The detailed current path is shown in Figure 6a.

State 2 ($t_0 < t \leq t_1$):

As shown in Figure 5, at $t = t_0$, switches $S_1$, $S_4$, $S_5$, and $S_6$ remain on. The energy stored in $L_K$ has been discharged to zero, causing $L_K$ to change its state from discharging to charging. Nevertheless, the energy stored in $L_M$ has not been discharged to zero. In this case, $V_{DCbus}$ will charge $L_K$ and combine with the $L_M$, transferring the energy to the low-voltage side to provide the load. The detailed current path is shown in Figure 6b.

State 3 ($t_1 < t \leq t_2$):

As shown in Figure 5, at $t = t_1$, switches $S_1$, $S_4$, $S_5$, and $S_6$ remain on. At this time, $L_M$ has discharged its stored energy to zero, thus transitioning from discharge to charge energy. $V_{DCbus}$ charges inductors $L_M$ and $L_K$, as well as supplies energy to the load. The detailed current path is shown in Figure 6c.

State 4 ($t_2 < t \leq t_3$):

At $t = t_2$, switches $S_1$, $S_4$, $S_5$, and $S_6$ are turned off. The period from $t_3$ to $t_4$ is the dead time of the high- and low-voltage side switches. At this time, currents $i_{LM}$ and $i_{LK}$ flow in the same direction. The high-voltage side current discharges $C_{oss2}$ and $C_{oss3}$ to charge $C_{oss1}$ and $C_{oss4}$, combining with $L_M$ to transfer energy to the low-voltage side. The low-voltage side...
side current discharges $C_{OSS6}$ and $C_{OSS7}$, charging $C_{OSS5}$ and $C_{OSS8}$, and providing energy to the load. The detailed current path is shown in Figure 6d.

Note that after the energy stored in $C_{OSS2}$, $C_{OSS3}$, $C_{OSS6}$, and $C_{OSS7}$ has been discharged to zero, intrinsic diodes $D_2$, $D_3$, $D_6$, and $D_7$ conduct the current during the remainder of this state. The detailed current path is shown in Figure 6e.

State 5 ($t_4 \leq t \leq t_5$):
As shown in Figure 5, due to the discharge of energy stored in $C_{OSS2}$, $C_{OSS3}$, $C_{OSS6}$, and $C_{OSS7}$ to zero during the dead time in state 4, switches $S_2$, $S_3$, $S_6$, and $S_7$ are turned on with ZVS at $t = t_4$. Since $L_M$ and $L_K$ have not discharged their stored energy completely, currents $i_{LM}$ and $i_{LK}$ keep flowing in the same direction as their previous state until their stored energy is discharged to zero. The detailed current path is shown in Figure 6f.

States 6 to 8 work the same way as states 2 to 4; the only difference is that switches $S_2$, $S_3$, $S_6$, and $S_7$ take the place of switches $S_1$, $S_4$, $S_5$, and $S_8$. Therefore, there will be no further explanation.

2.2. Medium-to-Full Load

As the load condition changes from light load to medium-to-full load, the SPS control is used to operate the DAB converter, controlling the direction and magnitude of the transferred power. Figure 7 demonstrates the theoretical waveforms of the proposed control strategy for the DAB converter in SPS mode under medium-to-full load conditions.

State 1 ($t_0 \leq t \leq t_1$):
As shown in Figure 7, due to the discharge of energy stored in $C_{OSS1}$ and $C_{OSS4}$ to zero during the dead time in the previous state, switches $S_1$ and $S_4$ are turned on with ZVS at $t = t_0$. Since inductor $L_K$ has not discharged its stored energy completely, current $i_{LK}$ keeps flowing in the same direction as that in the previous state until the energy stored in $L_K$ is discharged to zero. The detailed current path is shown in Figure 8a.
State 2 ($t_1 \leq t \leq t_2$):
As shown in Figure 7, at $t = t_1$, switches $S_1$, $S_4$, $S_5$, and $S_7$ remain on. The energy stored in $L_s$ has been discharged to zero, causing $L_s$ to change its state from discharging to charging. At this time, $V_{DCbus}$ charges $L_s$. Therefore, current $i_s$ changes its direction and increases linearly. The detailed current path is shown in Figure 8b.

State 3 ($t_2 \leq t \leq t_3$):
As shown in Figure 7, at $t = t_2$, switches $S_1$ and $S_4$ remain on, switches $S_5$ and $S_7$ are turned off. The period from $t_2$ to $t_3$ is the dead time of the low-voltage side switches. At this time, the low-voltage side current discharges $C_{oss1}$ and $C_{oss2}$, charging $C_{oss3}$ and $C_{oss5}$, and providing energy to the load. The detailed current path is shown in Figure 8c.

Figure 8. (a–g) The current flow path of the DAB converter in SPS control mode.
Note that after the energy stored in \( C_{OSS5} \) and \( C_{OSS8} \) has been discharged to zero, intrinsic diodes \( D_5 \) and \( D_8 \) conduct the current during the remainder of this state. The detailed current path is shown in Figure 8d.

State 4 (\( t_3 \leq t \leq t_4 \)):
As shown in Figure 7, switches \( S_1 \) and \( S_4 \) remain on. Due to the discharge of energy stored in \( C_{OSS5} \) and \( C_{OSS8} \) to zero during the dead time in the previous state, switches \( S_5 \) and \( S_8 \) are turned on with ZVS at \( t = t_3 \). The detailed current path is shown in Figure 8e.

State 5 (\( t_4 \leq t \leq t_5 \)):
As shown in Figure 7, at \( t = t_4 \), switches \( S_5 \) and \( S_8 \) remain on, while switches \( S_1 \) and \( S_4 \) are turned off. The period from \( t_4 \) to \( t_5 \) is the dead time of the high-voltage side switches. At this time, the high-voltage side current discharges \( C_{OSS2} \) and \( C_{OSS3} \), charging \( C_{OSS1} \) and \( C_{OSS4} \) and transferring energy to the low-voltage side to provide the load, and then flows back to \( V_{DCbus} \). The detailed current path is shown in Figure 8f.

Note that switches \( S_5 \) and \( S_8 \) remain on in this state. After the energy stored in \( C_{OSS2} \) and \( C_{OSS3} \) has been discharged to zero, intrinsic diodes \( D_2 \) and \( D_3 \) conduct the current. The detailed current path is shown in Figure 8g.

States 6 to 10 operate similarly to states 1 to 5, but there are some notable points as follows:
Switches \( S_2, S_3, S_5, \) and \( S_8 \) in state 6 and state 7 operate the same way as switches \( S_1, S_4, S_6, \) and \( S_7 \) in state 1 and state 2.
Switches \( S_2, S_3, S_6, \) and \( S_7 \) in states 7, 8, 9, and 10 operate the same way as switches \( S_1, S_4, S_5, \) and \( S_8 \) in states 2, 3, 4, and 5.
Therefore, there will be no further explanation.

3. Design of the DAB Converter Prototype

This paper employs a digital signal processor (DSP) to process the feedback signal from feedback circuits and control the mode switching, as shown in Figure 9.

![Figure 9. Block diagram of the proposed dual-mode control for the DAB converter.](image_url)

The DSP program updates its input regularly by sampling the output voltage and current via the ADC module. These values serve to calculate the output power \( P_O \). The
DSP program compares the $P_o$ value with a threshold value (200 W for forward conversion or 100 W for backward conversion) for mode switching. Based on the comparison result, the mode selector function will choose the suitable operation mode. A duty-cycle value or phase-shift value is calculated and sent to the PWM module, depending on the mode selected. There are two cases: when the energy is transferred from the $V_{DCbus}$ to $V_{bat}$, $V_{bat}$ would be an output voltage. In this case, the voltage value from feedback circuit B and the current value from current sensor B will be used to calculate output power $P_o$. On the other hand, when energy is transferred from $V_{bat}$ to the $V_{DCbus}$, the voltage value from feedback circuit A and the current value from current sensor A will be used to calculate output power $P_o$.

The DAB converter prototype was designed in accordance with the design parameters in Table 2.

**Table 2. Design parameters of the DAB converter prototype.**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary voltage, $V_{DCbus}$</td>
<td>400 V</td>
</tr>
<tr>
<td>Secondary voltage, $V_{bat}$</td>
<td>50 V</td>
</tr>
<tr>
<td>Maximum output power, $P_o$</td>
<td>1 kW</td>
</tr>
<tr>
<td>Maximum power, $P_{max}$</td>
<td>4.5 kW</td>
</tr>
<tr>
<td>Switching frequency, $f_{sw}$</td>
<td>100 kHz</td>
</tr>
<tr>
<td>Maximum phase-shift, $D_{max}$</td>
<td>0.2</td>
</tr>
<tr>
<td>Voltage ripple, $\Delta V_{DCbus}, \Delta V_{bat}$</td>
<td>&lt;5%</td>
</tr>
</tbody>
</table>

The rated power is 1 kW. The voltage of the high-voltage side is 400 V, and that of the low-voltage side is 50 V. For the high-voltage side of the converter, MOSFET SCT3080ALGC11, produced by ROHM Semiconductor (Kyoto, Japan), was selected for the power switch. On the other hand, MOSFET IRFP4321PBF, produced by Infineon (Neubiberg, Germany), was chosen for the power switches on the low-voltage side.

The flow chart diagram of the design process for energy storage components is given in Figure 10.

![Figure 10. Design flow chart for energy storage components.](image-url)
3.1. Transformer Selection

In order to achieve bidirectional power transfer, the DC bus voltage and the battery voltage are used as design criteria. Formula (1) is used to obtain the turns ratio.

$$n = \frac{N_P}{N_S} = \frac{V_{DCbus}}{V_{bat}} = 8$$  \hfill (1)

The transformer part number PC95PQ50/50Z-12, produced by TDK (Tokyo, Japan), is used as the high-frequency transformer of the proposed DAB prototype. The core is MnZn PC 95 ferrite core, and the coil former is PQ 50/50. According to the specifications provided by TDK, the effective cross-sectional area of the core is

$$A_e = \frac{1.8}{8} \text{ cm}^2.$$  \hfill (2)

By using the temperature characteristics curve of the transformer, it can be known that the saturation magnetic flux density of the iron core is about 410 mT at the temperature of 100 °C. To avoid the saturation of the transformer core, the maximum magnetic flux density $B_{max}$ is designed to be 0.31 times the saturation value, that is, 127 mT to ensure the normal operation of the transformer \[14, 15\]. Since the transformer voltage is the square wave, the form factor $K_f$ is 4. Finally, Formulas (2) and (3) are used to obtain the number of turns required for the high-voltage side winding, $N_P$ is 24 turns, and for the low-voltage side winding, $N_S$ is 3 turns.

$$N_P = \frac{V_{DCbus} \times 10^4}{B_{max} \times K_f \times A_e \times f_{sw}} \cong 24 \text{ turns}$$  \hfill (2)

$$N_S = \frac{N_P}{n} \cong 3 \text{ turns}$$  \hfill (3)

3.2. Inductor Selection

Formula (4) shows that the phase-shift ratio $D$ varies with the maximum power transfer $P_{Max}$ of the DAB converter \[16\].

$$P_{Max} = D(1 - D) \frac{n \times V_{DCbus} \times V_{bat}}{f_{sw} \times L_K}$$  \hfill (4)

Therefore, it is necessary to take the phase-shift ratio value into account in the design of the inductor. Operating at the maximum power transfer point ($D = 0.5$) can maximize the ZVS range. However, the DAB converter operating at this value increases the backflow power loss. Thus, this paper chooses a phase-shift ratio of 0.2.

This phase-shift ratio value is substituted into Formula (4) and then rewritten as Formula (5). The proposed DAB prototype is designed with maximum power is 4.5 times its rated power. Substitute all parameters into Formula (5) to obtain the inductance value.

$$L_K = \frac{0.16 \times n \times V_{DCbus} \times V_{bat}}{f_{sw} \times P_{Max}} \cong 57 \mu\text{H}$$  \hfill (5)

3.3. Output Capacitor Selection

Output capacitors are commonly used to regulate and filter output voltage output. Equivalent series resistance (ESR) inside the capacitor affects the output voltage ripple. Increasing the RMS value of the capacitor current leads to more loss dissipated across the ESR of capacitance. Taking these factors into account, the output capacitor was selected to keep the ripple voltage below 5% as a design requirement. This paper calculates the capacitance of capacitors $C_1$ and $C_2$, respectively, using Formula 6 and Formula 7 \[16\], where the ripple of the $V_{DCbus}$ ($\Delta V_{DCbus}$) is 6 V, and the ripple of $V_{bat}$ ($\Delta V_{bat}$) is 0.75 V.

$$C_1 = \frac{P_{DCbus}}{2 \times f_{sw} \times V_{DCbus} \times \Delta V_{DCbus}} \cong 2.0833 \mu\text{F}$$  \hfill (6)
\[ C_2 = \frac{P_{\text{bat}}}{2 \times f_{\text{sw}} \times V_{\text{bat}} \times \Delta V_{\text{bat}}} \approx 133.333 \mu F \]  \hspace{1cm} (7)

Considering the non-ideal case and the requirement for bidirectional power conversion, one 100 \( \mu F \)/450 V capacitor was chosen for the high-voltage side, and three 120 \( \mu F \)/63 V capacitors in parallel were selected for the low-voltage side.

4. Power Loss Model of the DAB Converter

Efficiency is related to transferred power and power losses. By taking into account the power switch losses, transformer losses, and inductor losses, a power loss model was built to verify the practical measured power efficiency.

4.1. Power Switch Losses

In this paper, the power switch is considered the ideal switch. Therefore, the power losses of the intrinsic diode can be ignored. Generally, power switch losses are divided into switching and conduction losses [17]. Switching loss, which is duty-cycle dependent, occurs during the turning on and turning off time of the power switch. Steady-state losses caused by a power switch can be calculated as follows:

The turn-on loss can be described as:

\[ P_{\text{SW(on)}} = \frac{V_{DS} \times I_p \times T_r \times f_{\text{sw}}}{6} \]  \hspace{1cm} (8)

where \( V_{DS}, I_p, T_r \) refer to the drain voltage, peak current, and rising time of the power switch, respectively.

The turn-off loss can be described as:

\[ P_{\text{SW(off)}} = \frac{V_{DS} \times I_p \times T_f \times f_{\text{sw}}}{6} \]  \hspace{1cm} (9)

where \( T_f \) refers to the falling time of the power switch.

The switching losses can be expressed as:

\[ P_{\text{SW,loss}} = P_{\text{SW(on)}} + P_{\text{SW(off)}} \]  \hspace{1cm} (10)

The gate drive loss can be calculated by using Formula (11).

\[ P_{\text{Gate}} = \frac{(C_{\text{iss}} + C_{\text{rss}}) \times V_{GS}^2}{2 \times T} \]  \hspace{1cm} (11)

where \( C_{\text{iss}} \) and \( C_{\text{rss}} \) refer to the input capacitance and reverse transfer capacitance of the power switch, respectively. \( V_{GS} \) is the gate-source voltage of the switch, and \( T \) is the switching period.

The conduction loss of the power switch can be calculated by using Formula (12).

\[ P_{\text{Cond}} = I_{\text{rms}}^2 \times R_{DS(on)} \]  \hspace{1cm} (12)

where \( I_{\text{rms}} \) refers to the RMS drain current, and \( R_{DS(on)} \) is the conduction resistance.

The total power losses of the power switch can be expressed as Formula (13).

\[ P_{\text{Loss(SW)}} = P_{\text{SW,loss}} + P_{\text{Gate}} + P_{\text{Cond}} \]  \hspace{1cm} (13)

4.2. Transformer Losses

The transformer losses consist of copper losses and core losses. The core loss can be calculated by using Formula (14).

\[ P_{\text{Coreloss(TR)}} = P_{\text{CV(Tr)}} \times V_{e(Tr)} \]  \hspace{1cm} (14)

where \( P_{\text{CV(Tr)}} \) refers to the core loss density, and \( V_{e(Tr)} \) refers to the effective core volume of the transformer, respectively.
The copper loss of the transformer can be calculated as Formula (15).

\[ P_{\text{Copper loss}(\text{Tr})} = I_{\text{rms(}\text{Pri})}^2 \times R_{\text{Copper}(\text{Pri})} + I_{\text{rms(}\text{Sec})}^2 \times R_{\text{Copper}(\text{Sec})} \]  

(15)

where \( I_{\text{rms(}\text{Pri})} \) and \( I_{\text{rms(}\text{Sec})} \) refer to the RMS value of the primary side and secondary side current, respectively. \( R_{\text{Copper}(\text{Pri})} \) and \( R_{\text{Copper}(\text{Sec})} \) refer to the resistance of the primary side and secondary side winding, respectively.

The total power losses of the transformer can be expressed as Formula (16).

\[ P_{\text{Loss}(\text{Tr})} = P_{\text{Core loss}(\text{Tr})} + P_{\text{Copper loss}(\text{Tr})} \]  

(16)

4.3. Inductor Losses

Similarly to transformers, the inductor power losses consist of copper losses and core losses. The core loss can be calculated by using Formula (17).

\[ P_{\text{Core loss}(\text{In})} = P_{CV(\text{In})} \times V_{e(\text{In})} \]  

(17)

where \( P_{CV(\text{In})} \) refers to the core loss density, and \( V_{e(\text{In})} \) refers to the effective core volume of the inductor, respectively.

The copper loss of the inductor can be calculated as Formula (18).

\[ P_{\text{Copper loss}(\text{In})} = I_{\text{rms(In)}}^2 \times R_{\text{Copper(In)}} \]  

(18)

where \( I_{\text{rms(In)}} \) represents the RMS value of inductor current, and \( R_{\text{Copper(In)}} \) represents the inductor winding resistance.

The total power losses of the inductor can be expressed as Formula (19).

\[ P_{\text{Loss(In)}} = P_{\text{Core loss(In)}} + P_{\text{Copper loss(In)}} \]  

(19)

4.4. Total Power Losses

Total power losses of the converter can be considered as the sum of switch losses, transformer losses, and inductor losses. Total power losses can be derived as follows:

\[ P_{\text{Loss Total}} = P_{\text{Loss(SW)}} + P_{\text{Loss(Tr)}} + P_{\text{Loss(In)}} \]  

(20)

5. Experimental Results

As a practical demonstration of the proposed dual-mode control strategy, a prototype DAB converter with a power rating of 1 kW was built and tested. The image of the actual circuit experimental platform is presented in Figure 11.
In this experiment, the prototype converter uses a DSP TMS320F28335 produced by Texas Instruments (Dallas, USA) as a digital controller to implement the proposed dual-mode control strategy. The proposed dual-mode DAB converter prototype has the specifications shown in Table 3:

Table 3. Specifications of the proposed DAB converter prototype.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary voltage, $V_{DCbus}$</td>
<td>400 V</td>
</tr>
<tr>
<td>Secondary voltage, $V_{bat}$</td>
<td>50 V</td>
</tr>
<tr>
<td>Transformer turns ratio, $n$</td>
<td>24:3</td>
</tr>
<tr>
<td>Maximum output power, $P_{max}$</td>
<td>1 kW</td>
</tr>
<tr>
<td>Switching frequency, $f_{sw}$</td>
<td>100 kHz</td>
</tr>
<tr>
<td>Maximum phase-shift, $D_{max}$</td>
<td>0.2</td>
</tr>
<tr>
<td>Magnetizing inductance, $L_{M}$</td>
<td>1.2 mH</td>
</tr>
<tr>
<td>Leakage inductance, $L_{K}$</td>
<td>57 $\mu$H</td>
</tr>
<tr>
<td>High-voltage side capacitor, $C_1$</td>
<td>100 $\mu$F</td>
</tr>
<tr>
<td>Low-voltage side capacitor, $C_2$</td>
<td>360 $\mu$F</td>
</tr>
</tbody>
</table>

Experimental data describing the bidirectional power conversion of the proposed DAB converter are divided into two categories: the measured waveforms of the forward power conversion mode (power flow from the high-voltage side to the low-voltage side) and the measured waveforms of the backward power conversion mode (power flow from the low-voltage side to the high-voltage side).

5.1. Forward Power Conversion Mode

According to the load conditions, the proposed DAB converter operates in PWM mode at light load (output power below 200 W), as shown in Figures 12 and 13. In PWM mode control, the gate signals $V_{GS1}$ and $V_{GS3}$ on the high-voltage side are synchronized with gate signals $V_{GS5}$ and $V_{GS7}$ on the low-voltage side. Thus, the DAB converter has the switching characteristics of a synchronous rectifier, as shown in Figures 12a and 13a. In addition, it can be seen from Figure 12b that when the output power is 10 W, the duty cycle of gate signal $V_{GSI}$ is approximately 45.7%, and the RMS value of inductor current $i_{LK}$ is 278 mA. When the output power increases to 200 W, the duty cycle of the gate signal $V_{GSI}$ increases to 47.1%, and the RMS value of inductor current $i_{LK}$ is 739 mA, as shown in Figure 13b.

![Figure 12](image-url)

**Figure 12.** Experimental waveforms of the prototype converter operating in forward power conversion mode (at 10 W output power): (a) waveforms of gate signals $V_{GSI}$, $V_{GS5}$, $V_{GS7}$, and inductor current $i_{LK}$; (b) waveforms of gate signals $V_{GSI}$, $V_{GS5}$, and $i_{LK}$. 
When the output power increases above 200 W, the operating mode of the proposed DAB converter changes from PWM mode to SPS mode, as shown in Figures 14 and 15. The SPS controls the turn-on time of switches, causing the phase-shift between the high-voltage side switches and low-voltage side switches, thereby controlling the direction and magnitude of power flow. When \( V_{GS1} \) leads \( V_{GS5} \), power flows from the high-voltage side to the low-voltage side, as illustrated in Figures 14a and 15a. When the output power is 300 W and 1 kW, the RMS value of inductor current \( i_{Lx} \) is 852 mA and 2.81 A, respectively, as shown in Figures 14b and 15b.
5.2. Backward Power Conversion Mode

Since the main control object in this mode is changed to the low-voltage side, the main control signals are $V_{GS5}$, $V_{GS6}$, $V_{GS7}$, and $V_{GS8}$. At light load (output power below 100 W), the DAB converter operates in PWM mode, as shown in Figures 16 and 17. In PWM mode control, gate signals $V_{GS5}$ and $V_{GS7}$ on the low-voltage side are in phase with gate signals $V_{GS1}$ and $V_{GS3}$ on the high-voltage side. Thus, the DAB converter has the switching characteristics of a synchronous rectifier, as shown in Figures 16a and 17a. According to Figures 16b and 17b, when the output power is 10 W and 100 W, the duty cycle of gate signal $V_{GS7}$ is approximately 43.44% and 46.29%, and the inductor current $i_{LK}$ is 269 mA and 298 mA, respectively.

![Figure 16](image1.png)

Figure 16. Experimental waveforms of the prototype converter operating in backward power conversion mode (at 10 W output power): (a) waveforms of gate signals $V_{GS1}$, $V_{GS3}$, $V_{GS5}$ and $V_{GS7}$; (b) waveforms of gate signals $V_{GS5}$, $V_{GS7}$ and inductor current $i_{LK}$.

![Figure 17](image2.png)

Figure 17. Experimental waveforms of the prototype converter operating in backward power conversion mode (at 100 W output power): (a) waveforms of gate signals $V_{GS1}$, $V_{GS3}$, $V_{GS5}$ and $V_{GS7}$; (b) waveforms of gate signals $V_{GS5}$, $V_{GS7}$ and inductor current $i_{LK}$.

When the output power increases above 100 W, the operating mode of the proposed DAB converter changes from PWM mode to SPS mode. Note that at this time, gate signal $V_{GS1}$ lags behind gate signal $V_{GS5}$, as shown in Figures 18a and 19a. When the output power is 200 W and 1 kW, the RMS value of inductor current $i_{LK}$ is 595 mA and 2.84 A, respectively, as shown in Figures 18b and 19b.
Figure 18. Experimental waveforms of the prototype converter operating in backward power conversion mode (at 200 W output power): (a) waveforms of gate signals \( V_{GS1}, V_{GS3}, V_{GS5} \) and \( V_{GS7} \); (b) waveforms of gate signals \( V_{GS5}, V_{GS7} \) and inductor current \( i_{LK} \).

Figure 19. Experimental waveforms of the prototype converter operating in backward power conversion mode (at 1 kW output power): (a) waveforms of gate signals \( V_{GS1}, V_{GS3}, V_{GS5} \) and \( V_{GS7} \); (b) waveforms of gate signals \( V_{GS5}, V_{GS7} \) and inductor current \( i_{LK} \).

5.3. Load Transient Testing for the Proposed DAB Converter

Experiments on the step load response of the proposed converter in bidirectional power conversion are shown in Figures 20 and 21. Figure 20 shows the experimental waveforms in the forward power conversion mode. According to Figure 20a, the distortion level of battery voltage is approximately 12 V when the step load changes from 10 W to 1 kW, and it takes about 300 ms to reach a steady state. Conversely, the distortion level of battery voltage is approximately 2 V when the step load changes from 1 kW to 10 W, and it takes about 200 ms to reach a steady state, as shown in Figure 20b. Figure 21 shows the experimental waveforms in the backward power conversion mode. When the step load changes from 10 W to 1 kW, the distortion level of the DC bus voltage is approximately 5 V, and it takes around 10 ms to reach a steady state, as shown in Figure 21a. Conversely, when the step load changes from 1 kW to 10 W, the distortion level of the DC bus voltage is around 5 V, and it takes about 120 ms to reach a steady state, as shown in Figure 21b.
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Figure 20. Step load response of prototype converter operating in forward power conversion mode: (a) load change from 10 W to 1 kW; (b) load change from 1 kW to 10 W.

Figure 21. Step load response of prototype converter operating in backward power conversion mode: (a) load change from 10 W to 1 kW; (b) load change from 1 kW to 10 W.

Figures 22 and 23 are waveforms of the mode switching of the proposed DAB converter. This paper sets the mode switching point at 200 W for forward power conversion, so the output power is selected from 150 W to 300 W for measurement. According to Figure 22a, it takes approximately 60 μs for the converter to reach a steady state without oscillation when the output power increases from 150 W to 300 W. Conversely, when the output power changes from 300 W to 150 W, the converter takes approximately 100 μs to reach a steady state without oscillation, as shown in Figure 22b.

Figure 22. Waveforms of mode switching (in forward power conversion): (a) load change from 150 W to 300 W; (b) load change from 300 W to 150 W.
For backward power conversion, the mode switching point (threshold value) is set at 100 W, so the output power is selected from 10 W to 200 W for measurement. A steady state time of about 60 μs is observed when the output power increases from 10 W to 200 W in Figure 23a. Conversely, when the output power decreases from 200 W to 10 W, the converter reaches a steady state after 120 μs, as shown in Figure 23b. It is worth noting that under the above test conditions, the converter does not oscillate. Therefore, the dual-mode control strategy proposed in this paper is feasible.

5.4. Efficiency Comparison Curve

Figure 24 shows the efficiency comparison between the DAB converter using the dual-mode control strategy proposed in this paper and a DAB converter using the traditional SPS control strategy. It can be seen from the figure that the light load efficiency of the DAB converter using the dual-mode control strategy is better than that of the DAB converter using the traditional SPS strategy. In particular, in the forward power conversion mode, the maximum efficiency of the proposed control strategy is 10% higher than that of the traditional SPS strategy, as shown in Figure 24a. In the backward power conversion mode, the maximum efficiency of the proposed control strategy is 5% higher than that of the traditional SPS control strategy, as shown in Figure 24b.

The characteristic of the SPS control is that high backflow power when operating at light loads reduces the converter efficiency. The light-load efficiency of the proposed dual-
mode converter is enhanced because the converter operates in PWM mode to minimize backflow power. Experimental results verify that the dual-mode control strategy proposed in this paper improves the light load efficiency of the DAB converter compared with the traditional SPS control strategy. Table 4 shows a comparison of the related studies with the proposed dual-mode control strategy in terms of efficiency. Table 5 also shows the calculation for the power loss of the proposed dual-mode DAB converter at a load of 100 W.

<table>
<thead>
<tr>
<th></th>
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<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>Light load (10% of power rating)</td>
<td>93.34%</td>
<td>n/a</td>
<td>approx. 86%</td>
</tr>
<tr>
<td>Medium load (50% of power rating)</td>
<td>93.04%</td>
<td>approx. 88%</td>
<td>approx. 92%</td>
</tr>
<tr>
<td>Full load (100% of power rating)</td>
<td>92.59%</td>
<td>approx. 90%</td>
<td>93.25%</td>
</tr>
</tbody>
</table>

6. Conclusions

This paper proposes a dual-mode control strategy for addressing the disadvantage of conventional SPS control applied to DAB converters. In dual-mode control, PWM and SPS techniques are combined and switched depending on the load. Under light load conditions, the DAB converter is controlled by the PWM control method. During medium-to-full load conditions, on the other hand, the DAB converter is controlled by the SPS method. The experimental results indicate that the converter can achieve the highest efficiency of 96.267% when operating in the forward power conversion mode (power flow from the high-voltage side to the low-voltage side), and 97.331% when operating in the backward power conversion mode (power flow from the low-voltage side to the high-voltage side). Furthermore, there is no oscillation when switching back and forth between operating modes.

Author Contributions: Conceptualization, J.-M.W. and T.N.T.T.; methodology, W.-Y.C. and J.-M.W.; software, T.N.T.T., W.-Y.C. and J.-M.W.; validation, T.N.T.T., W.-Y.C. and J.-M.W.; resources, J.-M.W.; writing—original draft preparation, J.-M.W. and T.N.T.T.; writing—review and editing, J.-M.W. and T.N.T.T. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the Ministry of Science and Technology, R.O.C., (grant numbers: MOST 110-2622-E-150-002 and MOST 111-2221-E-150-009).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.
Acknowledgments: The authors are grateful for the support of Power Electronics Research Laboratory members during the execution of this study. Further, we would like to express sincere gratitude to all anonymous reviewers for their time and expertise, which significantly improved our paper’s academic and professional quality.

Conflicts of Interest: The authors declare no conflict of interest.

References