Optimization of Data Acquisition System Based on Electrical Impedance Tomography in Dredging Engineering

Ning Liu, Shihong Yue * and Yibo Wang

School of Electrical and Information Engineering, Tianjin University, Tianjin 300072, China; ning2506@tju.edu.cn (N.L.); wyb1130@tju.edu.cn (Y.W.)
* Correspondence: shyue1999@tju.edu.cn

Abstract: Electrical impedance tomography (EIT) is an advanced visualization detection technique with non-invasive, radiationless, and fast-response characteristics. As an important means in dredging engineering, EIT-based measurement can realize the estimate and computation of key flow parameters such as the flow velocity and solid phase fraction of solid-liquid two-phase flow in a pipe. Despite progress, both the data acquisition rate and the signal-to-noise ratio (SNR) of the existing EIT system are too low to meet many practical requirements. In this study, efforts are made concerning the EIT acquisition system by optimizing the sensor array, data acquisition system, and data communication module. Experimental results show that (1) the optimized system has an SNR of 73 dB, which is about 40% higher than the original system, and (2) the optimization of data transmission methods can achieve a maximum allowable transmission rate of 316.4 Mbps, sufficient to support data transmission over 1000 frames per second. Consequently, the key problems of the existing EIT acquisition system are substantially overcome.

Keywords: electrical impedance tomography; data acquisition system; signal-to-noise ratio; data acquisition rate

1. Introduction

Electrical impedance tomography (EIT) is an advanced detection technique that solves electrical parameter distribution over all pixels in a detection field [1]. By measuring the electrical signals at the field’s boundaries, the target objects within the measured field can be visually reconstructed by various pixel greyscales. Since EIT has advantages, such as its radiationless, non-invasiveness, fast response, and low cost, it has received increasing attention in many important applications [2].

The data acquisition system plays an important role in the EIT detection process. The earliest acquisition system is a single row of 16 electrode sensors called Sheffield Mark I [3]. The excitation frequency of the system is 50 kHz, and the data acquisition frame rate is 12.5 fps. Later, Mark II and Mark 3.5a were developed based on this system, and the new system achieved a signal-to-noise ratio (SNR) of 55 dB [4,5]. Holder et al. designed a multi-frequency excitation system with excitation frequencies ranging from 225 Hz to 65 kHz based on the Mark I system, which aimed to design brain imaging for changes in electrical impedance during brain activity [6]. Ryan et al. presented a set of EIT systems for detecting breast cancer, with a digital signal process (DSP) as the core master component of the system [7]. Harsh et al. conducted the Kyung Hee University (KHU) Mark 2.5 multi-frequency EIT system, which modified the central control unit to a field programmable gate array (FPGA) [8]. The proposal of the new scheme optimized the digital design after greatly reducing system artifacts and maximizing system performance.

Recently, the research group attached to Tianjin University designed a 16-electrode EIT measurement system for lung function detection, with an imaging speed of 30 fps [9]. Afterward, modifications were made to the original system, and a dual-mode measurement...
system based on FPGA was introduced, with an SNR of 74 dB. They also presented an EIT hardware system based on a controller area network (CAN) bus, which expands the frequency of the excitation signal to 10 MHz [10]. Introducing the multi-period undersampling technique enables it to extract more imaginary part information of impedance. The existing EIT system has achieved certain real-time accuracy and has been applied in practical engineering [11]. Compared with traditional EIT devices, the EIT system in this article integrates three functions: flow measurement, solid phase content measurement, and visualization while possessing high measurement accuracy and real-time performance [12,13].

EIT has taken effects in estimating and measuring the key parameters in dredging engineering, but the low spatial resolution limits its in-depth and further applications. Essentially, two key problems remain unsolved as follows:

1. **Signal-to-noise rate (SNR):** To ensure the accuracy of measurement data, higher requirements of SNR have been put forward. However, the existing EIT data acquisition system cannot keep a high SNR under arbitrary conditions. The acquisition and processing system of EIT must be improved;

2. **Acquisition rate:** There is still significant room for enhancing the real-time performance of the measurement system, and the length of a single measurement cycle directly affects the data quality between the measurement results and the distribution of the medium in the pipe. Improving the EIT acquisition rate is a significant prerequisite for ensuring the accuracy of measurement results.

In this study, we propose an optimization EIT design by solving the two main problems in the existing EIT system. The SNR is improved by optimizing measurement circuits and data transmission characteristics. The EIT acquisition rate is improved by optimizing the analog-to-digital conversion module and data communication module. At the same time, the digital phase-sensitive demodulation technique is used to ensure the real-time performance of the EIT system. The simulation and real experimental results show that compared to traditional EIT systems, the proposed design in the study can greatly improve the SNR and data acquisition rate.

## 2. Materials and Methods

### 2.1. EIT System Structure

The composition of the FPGA-based EIT system is shown in Figure 1. Firstly, the excitation electrical signal is applied to the electrode array on the sensor to obtain the electrical parameters of the tested field. The response electrical signal is measured through a data acquisition system and sent to the data processing system of the upper computer. The upper computer calculates and analyzes the measurement data through software algorithms, thereby achieving the estimation of key flow parameters within the measured field and achieving the integration of concentration and flow measurement.

![Figure 1. EIT system composition.](image-url)
According to the measuring process, the workflow of the EIT acquisition process in this study is shown in Table 1.

<table>
<thead>
<tr>
<th>Table 1. Workflow of the EIT acquisition process.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Step 1: Generate a digital sine wave from FPGA.</td>
</tr>
<tr>
<td>Step 2: Drive an external DA conversion chip to generate an AC signal.</td>
</tr>
<tr>
<td>Step 3: Load filtered smooth signal to the sensor electrode.</td>
</tr>
<tr>
<td>Step 4: Measure the current signal and convert it into a digital signal through an AD conversion chip.</td>
</tr>
<tr>
<td>Step 5: Transfer the digital signal to FPGA for demodulation to obtain its amplitude.</td>
</tr>
<tr>
<td>Step 6: Process the data collected by the EIT system through the upper computer.</td>
</tr>
</tbody>
</table>

The existing EIT system has a collection speed of 60 fps, an SNR of 52 dB, and a system signal frequency of 80 kHz [14]. Data acquisition is the core composition of any EIT system. Its performance directly determines the detection quality in dredging engineering.

2.2. Improvement of SNR

The flow object composition in the dredging pipe is complex, and due to interference from other electromagnetic components, many electromagnetic signals are carried in the measurement field, which leads to a large amount of high-frequency and low-frequency noise in the measurement circuit. Therefore, it is necessary to conduct spectral analysis in the measurement circuit to observe the frequency distribution of the noise and add corresponding filters to eliminate related noise. At the same time, selecting appropriate electrode materials and transmission signal lines can also reduce external interference to a certain extent. Our study will propose two methods to improve the SNR of EIT.

(1) **Optimization of the measurement circuit**

After the excitation signal is added to the sensor, the obtained current signal is transmitted to the FPGA for demodulation through the measurement circuit. The measurement signal carries relevant information about the field conductivity distribution. Due to the complexity of signals in the field of dredging pipes, measurement signals may carry various noise frequencies. Therefore, a series of signal processing circuits must be added to the measurement circuit to obtain high-precision measurement signals.

AD8129 is selected as the cross-resistance amplifier. The signal amplified by AD8129 in the measurement circuit can be observed through an oscilloscope. It is seen that this signal contains higher-order harmonics much higher than 80 kHz. After discrete Fourier transform (DFT) verification, it was observed that this higher-order harmonic signal is approximately in the frequency band of 4 MHz. The structure of the measurement circuit and the DFT results are shown in Figure 2. Where \( I_X \) is the current to be measured, \( R_O \) is the resistance value of the sensing resistor, and \( U_O \) is the partial voltage of the sensing resistor. Therefore, we chose a second-order Salley–Kelly low-pass filter and set its cutoff frequency to 3 MHz. The structure and filtering effect are shown in Figure 3, and it can be seen that most of the noise signals in the measurement signal have been filtered out at this time.
Figure 2. Measurement circuit and DFT result. (a) Measurement circuit; (b) DFT result.

Figure 3. Filter structure and filtering effect. (a) Filter structure; (b) Filtering effect.

(2) Electrode and transmission line

The sensor electrodes are composed of metal materials arranged at equal intervals inside the pipe or container. They are used to release and obtain electrical signals and are key media for establishing sensitive fields in the measured field domain. These electrode arrays directly affect the potential and equipotential lines of the detection field and have a significant impact on the reconstruction of the conductivity distribution in the measured field [15]. Therefore, sensors used in dredging engineering have high requirements for the materials and manufacturing processes of electrodes and pipes. The internal schematic diagram is shown in Figure 4.

Figure 4. EIT sensor structure.
The electrode material must have good conductivity and stable chemical properties. Under the excitation of sinusoidal electrical signals, if the excitation frequency is too low, the polarization reaction on the electrode surface is severe; if the excitation frequency is too high, electromagnetic induction and "connection impedance" will create strong noise [16–19]. The sensor array of the EIT system is directly in contact with the medium inside the pipe. When an electrical signal is added to any electrode, the electrode will undergo a certain chemical reaction with the substances, thereby affecting the size of the measured value. In the dredging industry, solid materials must be transported through pipes a few kilometers away for reclamation. To cope with the high pressure inside the pipe, electrode materials need to have a certain compressive strength higher than 2.6 MPa. The commonly used materials for electrodes are shown in Table 2.

Table 2. Characteristics of electrode materials at room temperature.

<table>
<thead>
<tr>
<th>Material</th>
<th>Resistivity (Ω·m)</th>
<th>Yield Strength (MPa)</th>
<th>Electrochemical Characteristics</th>
<th>Price (RMB/ton)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper</td>
<td>1.72 × 10⁻⁸</td>
<td>343</td>
<td>Strong stability and corrosion resistance</td>
<td>62,980</td>
</tr>
<tr>
<td>Titanium</td>
<td>4.2 × 10⁻⁷</td>
<td>300</td>
<td>Good stability and corrosion resistance</td>
<td>62,210</td>
</tr>
<tr>
<td>Carbon</td>
<td>3.5 × 10⁻⁶</td>
<td>9.3</td>
<td>Non-metallic, corrosion-resistant</td>
<td>2000</td>
</tr>
<tr>
<td>Tungsten</td>
<td>5.48 × 10⁻⁸</td>
<td>-</td>
<td>Strong stability and corrosion resistance</td>
<td>116,000</td>
</tr>
<tr>
<td>Stainless steel</td>
<td>7.3 × 10⁻⁷</td>
<td>207</td>
<td>Moderate stability, not resistant to corrosion</td>
<td>15,625</td>
</tr>
</tbody>
</table>

After comparing the electrode material characteristics mentioned above, titanium was ultimately used as the electrode material instead of traditional stainless steel. Due to the relatively low electrical resistivity and high yield strength of titanium metal, it has good electrochemical stability while meeting lower prices.

In practice, the transmission signal line between the pipe and the data acquisition system is also highly affected by electromagnetic signals generated by other equipment, and these interference sources will directly affect the accuracy of the data collected by the equipment. Therefore, the signal line needs to use a single-core shielded wire with a shielding layer, which can prevent external interference sources from affecting the excitation and measurement signals and also block the path of the signal line, radiating electromagnetic waves outward. The composition of the shielding wire is shown in Figure 5.

![Composition of shielding wire.](image)

Figure 5. Composition of shielding wire.

2.3. Improvement of Acquisition Rate

The signal acquisition rate of a data acquisition system is mainly determined by the single cycle time of the system, i.e., the time to obtain a set of measured values. The main factors affecting the single cycle time of the system include the signal frequency released by the FPGA and the transmission rate of the communication module.

(1) Analog-to-digital conversion optimization

Phase-sensitive demodulation is the most crucial step in obtaining measured values in FPGA. This step requires that the sampling frequency of the A/D module and the D/A module should be consistent. The number of single-cycle semaphores output by analog-to-digital conversion is determined by the sampling frequency of the analog-to-digital conversion chip and the frequency of the analog signal.

\[ n = \frac{f_s}{f} \]  (1)
where $f$ is the frequency of the analog signal, $f_s$ is the sampling frequency, and $n$ is the number of single-cycle semaphores. The number of different single-cycle semaphores directly determines the final effect of digital-to-analog conversion. The more single-cycle semaphores, the higher the similarity between the output digital signal and the analog signal.

The system has a high demand for signal frequency. The sampling frequency of the A/D and D/A modules must be increased to obtain a higher signal frequency and ensure the current number of single-cycle semaphores. The current sampling frequency of the system is 10 MHz, which is directly provided by FPGA. The highest sampling frequency of the D/A chip AD9764 is 125 MHz, and the highest sampling frequency of the A/D chip AD9240 is 10 MHz.

The current sampling frequency is the highest sampling frequency of AD9240, so the AD9240 chip directly limits the signal frequency of the data acquisition system. Based on the above analysis, it is necessary to replace the A/D conversion chip to improve the signal frequency of the data acquisition system. The common parameters of low-voltage analog-to-digital conversion chips are shown in Table 3.

Table 3. Performance parameters of common analog-to-digital conversion chips.

<table>
<thead>
<tr>
<th>Chip</th>
<th>Maximum Sampling Rate (MSPS)</th>
<th>Packaging Type</th>
<th>Resolution Ratio/Bit Wide (bit)</th>
<th>SNR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD9240</td>
<td>10</td>
<td>MQFP-44</td>
<td>14</td>
<td>78.5</td>
</tr>
<tr>
<td>AD9244</td>
<td>65</td>
<td>LQFP-48</td>
<td>14</td>
<td>75.3</td>
</tr>
<tr>
<td>LTC2239</td>
<td>80</td>
<td>QFN-32</td>
<td>10</td>
<td>61.6</td>
</tr>
<tr>
<td>ADS4149</td>
<td>250</td>
<td>VQFN-48</td>
<td>14</td>
<td>72.2</td>
</tr>
</tbody>
</table>

Considering sampling frequency, cost, accuracy, and other conditions, a 14-bit high-speed analog-to-digital converter AD9244 was ultimately adopted. Its peripheral circuit design is shown in Figure 6.

Figure 6. Design of peripheral circuit for AD9244 analog-to-digital conversion module.

(2) Communication protocol optimization

As one of the key components of the data collection system, the reliability, stability, and real-time performance of the data transmission system will directly affect the performance of the entire system [20]. For an electrical imaging system with $n_0$ electrodes in a single
cross-section, the voltage value between each two electrodes is measured after the sensitive field is established, and then the image is reconstructed. The number of measurements required to reconstruct an image is

$$n_1 = n_0(n_0 - 1)$$  \hspace{1cm} (2)

Because each measurement data contains 16 bits of real and imaginary data, the number of bytes required to reconstruct an image is

$$n_2 = 2n_1$$  \hspace{1cm} (3)

Therefore, for the existing 16-electrode system, the data required to reconstruct an image is 480 B. In addition, each frame of data will also include a frame header and a frame footer, resulting in a data volume of 504 B per frame.

Currently, the data transmission methods commonly used in EIT data collection systems both domestically and internationally include USB, RS-232/485, Ethernet, Firewire, Peripheral Component Interconnect (PCI) interface, etc. [21–23]. The maximum transmission rates and characteristics of the various transmission methods mentioned above are shown in Table 4.

**Table 4. Comparison of data transmission methods.**

<table>
<thead>
<tr>
<th>Data Transmission Method</th>
<th>Rate</th>
<th>Distance</th>
<th>Characteristic</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB2.0</td>
<td>480 Mbps</td>
<td>5 m</td>
<td>Low-cost, widely used</td>
</tr>
<tr>
<td>RS-232/485</td>
<td>115,200 bps</td>
<td>1200 m</td>
<td>Simple but low-speed</td>
</tr>
<tr>
<td>Ethernet(IEEE 802.3ab)</td>
<td>1 Gbps</td>
<td>Hundreds of kilometers</td>
<td>Relatively complex, capable of remote communication</td>
</tr>
<tr>
<td>Firewire(IEEE 1394c-2006)</td>
<td>800 Mbps</td>
<td>4.5 m</td>
<td>Less CPU usage, reliability, and high-cost</td>
</tr>
<tr>
<td>PCI(PCI-X 3.0)</td>
<td>4266 MB/s</td>
<td>-</td>
<td>Belongs to the local bus</td>
</tr>
</tbody>
</table>

The existing EIT system uses RS-232 serial port transmission and can only support transmission rates up to tens of frames per second. This results in the system’s data collection rate being limited by the data transmission method. The existing serial communication can no longer meet the system’s requirements for real-time and reliability. A transmission rate of over 1000 frames per second can meet the real-time requirements of the system [24]. Since the amount of data per frame is 504 B, the transmission rate of the data transmission interface should be greater than 504 kB/s, which is 4.032 Mbps when converted to Baud. Except for RS-232/485, all other transmission methods in Table 4 can meet the transmission speed requirements. Due to the low development cost and good universality of USB2.0, USB2.0 was chosen for the EIT data collection system.

We adopted the CY7C68013A chip from Cypress’s EZ-USB FX2LP series. CY7C68013A is a USB2.0 control chip from Cypress, which includes a high-speed USB2.0 communication protocol and compatible 8051 control. This chip contains 16 KB of internal RAM, allowing firmware programs to run directly without the need for additional memory. CY7C68013A integrates four first-in, first-out (FIFO) internally, with a total size of 4 K bytes. Users can set them to work in master or slave mode. CY7C68013A contains an I2C interface for connecting to external EEPROMs. Users first download the written firmware program to the EEPROM. When CY7C68013A is powered on and started, it will automatically read the EEPROM program and start running in the internal RAM. The internal structure of CY7C68013A is shown in Figure 7.
The data communication between FPGA and USB chips is achieved by reading and writing FIFO data from the four ports (EP2, EP4, EP6, EP8) of CY7C68013A. The FPGA is the main device, and the port of CY7C68013A is the slave device. The slave FIFO can operate in synchronous or asynchronous mode. Due to the internal clock of the chip being 48 MHz and the clock of the EIT system being 50 MHz, the slave FIFO is set to operate in asynchronous mode.

The firmware program of CY7C68013A was completed in the Keil uVision development environment. Through the firmware program, configure the dual function IO of CY7C68013A to Slave FIFO mode, pin FLAGA to indicate the empty flag of EP2 port, FLAGB to indicate the full flag of EP2 port, and FLAGC to indicate the full flag of EP6 port. Additionally, ports 2 and 4 are configured as Bulk outputs, while ports 6 and 8 are configured as Bulk inputs. Burn the generated iic file into the chip's EEPROM to ensure that the power on the program is not lost.

The reading and writing timing diagram of the chip is shown in Figure 8. The read-and-write control of the chip is implemented by two state machines, and its program is written in Verilog. The state transition diagram of the reading and writing process is shown in Figure 9.

![Internal structure diagram of CY7C68013A](image)

**Figure 7.** Internal structure diagram of CY7C68013A.

![Reading and writing the timing diagram of the chip](image)

**Figure 8.** Reading and writing the timing diagram of the chip. (a) Read; (b) Write.
2.4. Digital Phase-Sensitive Demodulation Technique

Without considering environmental interference and noise effects, the sine excitation signal output by the data acquisition system may change in amplitude and phase when passing through the measured field domain, while the frequency and waveform remain unchanged. Therefore, the basic form of the discrete signal of $V_m(i)$ that represents the magnitude of voltage received by FPGA can be expressed as

$$V_m(i) = A \sin(2\pi i/N + \theta)$$  \hspace{1cm} (4)

where $A$ is the amplitude of the sine wave, and $N$ represents the number of sampling points of the AD converter within one excitation signal cycle. Obviously, such a digital signal sequence requires processing to obtain the sine wave amplitude required for image reconstruction. Taking the maximum value point $V_{\text{max}}$ in a cycle as the value of $A$ is a simple and effective method. However, this method will result in extremely low noise immunity, and any noise that causes a change in the maximum value will have a significant impact on the results. Another method is to directly transmit the amplitude of these discrete signals to the upper computer, which utilizes its powerful data processing function for calculation. However, this requires transmitting $N$ data per cycle, which is very detrimental to the real-time performance of the system.

To address the above issues, digital phase-sensitive demodulation technology is adopted, which converts the discrete signal into a sine wave amplitude through multiplication accumulation and coordinate conversion in FPGA and then transmits it to the upper computer. This method has good anti-interference performance. Due to the parallel execution of instructions in FPGA and the need to transmit only one data to the upper computer, it has almost no impact on the real-time performance of the system.

In Equation (4), $V_m$ represents the voltage to be measured. Assuming $V_{re}$ represents the real part of $V_m$ and $V_{im}$ represents the imaginary part of $V_m$, they can be represented as

$$V_{re} = \frac{2}{N} \sum_{i=0}^{N-1} V_m(i) \times \sin \frac{2\pi i}{N} = A \cos \theta$$ \hspace{1cm} (5)

$$V_{im} = \frac{2}{N} \sum_{i=0}^{N-1} V_m(i) \times \cos \frac{2\pi i}{N} = A \sin \theta$$ \hspace{1cm} (6)

Therefore, the amplitude of $V_m(i)$ can be expressed as

$$A = \sqrt{V_{re}^2 + V_{im}^2}$$ \hspace{1cm} (7)

According to the above formula, digital phase-sensitive demodulation is achieved using the Multiply Accumulate (MAC) and Coordinate Rotation Digital Computer (CORDIC) modules in FPGA. The designed module block diagram is shown in Figure 10.
Figure 10. Module diagram of digital-phase sensitive demodulation.

$V_m(n)$ represents the discrete voltage value to be measured after AD conversion. Two MACs are used to perform cross-correlation operations with the reference signals $\sin(n)$ and $\cos(n)$, respectively, to obtain the real and imaginary values. Take the output of MAC as the input of CORDIC and perform modulus calculation to obtain the amplitude of the signal to be tested. Using digital phase-sensitive demodulation technology effectively ensures the real-time performance of the system and improves the data acquisition speed.

3. Results

3.1. Experiment on Static Objects

To test the optimization effect of the proposed scheme on the EIT acquisition system, static experiments were conducted to test the SNR of the current system using the optimized EIT acquisition system. The output waveform frequency of the FPGA DDS IP core is set to 160 kHz, and the sampling frequency of AD9764 and AD9244 is set to 20 Mhz. At this time, the excitation frequency of the entire system is 160 kHz. The inner diameter of the static water basin device is 16 cm, and the liquid phase background is tapping water with a conductivity of 260 $\mu$S/cm. The entire testing device is shown in Figure 11.

Figure 11. Experimental device for the test of static objects.
Set the excitation size to 2 V and continuously collect 1000 sets of measurement values in the pure water. After performing SNR analysis on the current system using continuous multiple sets of measurement data, the calculation formula for SNR is as follows:

$$SNR = 20 \log \left( \frac{\sigma_x}{\bar{x}} \right)$$  \hspace{1cm} (8)

where $\sigma_x$ represents the standard deviation of the measured values and $\bar{x}$ represents the average of the measured values.

The measurement value sequence consists of 480 measurements, and they are shown in Figure 12. To measure the anti-interference ability of the entire EIT system, it is necessary to calculate the SNR of the EIT acquisition system for 480 measurements separately and then calculate the expected values of all results to obtain the SNR of the entire system. The SNR of some measured values is shown in Table 5.

![Figure 12. Measurement value sequence.](image)

**Table 5. SNR situation of some measured values.**

<table>
<thead>
<tr>
<th>Measurement Data Number</th>
<th>$\bar{x}$</th>
<th>$\sigma_x$</th>
<th>SNR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>898</td>
<td>0</td>
<td>80.0656</td>
</tr>
<tr>
<td>182</td>
<td>410.98</td>
<td>0.0408</td>
<td>72.3976</td>
</tr>
<tr>
<td>283</td>
<td>293</td>
<td>0</td>
<td>/</td>
</tr>
<tr>
<td>290</td>
<td>197.9950</td>
<td>0.0705</td>
<td>68.9652</td>
</tr>
<tr>
<td>327</td>
<td>236.98</td>
<td>0.0408</td>
<td>75.0986</td>
</tr>
<tr>
<td>396</td>
<td>180.9900</td>
<td>0.0995</td>
<td>65.1967</td>
</tr>
<tr>
<td>442</td>
<td>174.0016</td>
<td>0.0407</td>
<td>72.5998</td>
</tr>
<tr>
<td>473</td>
<td>169.9983</td>
<td>0.0408</td>
<td>72.3976</td>
</tr>
</tbody>
</table>

From Table 5, it can be seen that the SNR of most measured values is above 65 dB, and some measured values have no fluctuations in 1000 sets of data, with a standard deviation of 0, indicating a good SNR. When calculating the expected SNR of all measured values, the parameter with an SNR of “/” is set to 100 dB, resulting in an SNR of 73 dB for the current system. Compared to other EIT systems, both domestically and internationally, it can reach a higher level [25,26]. The EIT system in the article is optimized based on our previous work. The original EIT system has an SNR of 52 dB. The comparison results show that the optimized EIT measurement system has significantly improved SNR.

3.2. Simulation Results

Simulate the reading and writing process of the communication module using Modelsim simulation software, and the simulation results are shown in Figure 13. Among them, USB_ADDR is an addressing signal for FIFO. When the values of this signal are 00 and 10,
the communication module performs read and write functions, respectively. The results of the simulation experiment indicate the feasibility of the USB2.0 communication used in this simulation.

![Simulation Results](image1)

**Figure 13.** Communication module reading and writing simulation results. (a) Write; (b) Read.

After compiling the Verilog program and burning it into FPGA, the EZ-USB Interface was used as a communication tool for data communication. The results showed that USB2.0 communication based on CY68013A could be successfully applied to existing EIT devices.

The communication speed of the communication module is the most concerning issue. To test the actual communication speed of the communication module in this study, the upper computer program Streamer provided by Cypress company was used to test the USB transmission speed. After connecting the main control circuit board of the system to the computer using a USB transmission cable, open the Streamer to establish the connection. After selecting the corresponding read and write ports, the operator can initiate data transmission and monitor the transmission speed in real-time through the Streamer. The test results are shown in Figure 14, with a transmission rate of 40,500 KB/s, which is 316.4 Mbps; The receiving rate is 45,000 KB/s, 351.6 Mbps. Based on the calculation of the frame rate in Section 2, it can be seen that the optimized communication method can allow data transmission over 10,000 frames per second, greatly improving the system’s data acquisition rate.

![Transmission & Receiving Rates](image2)

**Figure 14.** Data transmission and reception rate monitoring results. (a) Transmission Rate; (b) Receiving rate.

4. Conclusions

To improve the performance of the data acquisition system used in dredging engineering, in this study, we propose an optimization scheme. To enhance the anti-interference and real-time performances, the sensor array, data acquisition system, and data communication module in the system are optimized to improve the SNR and data acquisition
rate. Experimental results show that the optimized system has an SNR of 73 dB and a data transmission rate of 316.4 Mbps, which outperforms the existing system. Therefore, the proposed optimization scheme can extend the EIT applicable range owing to the improvement of the measuring quality.

Further work is focused on integrating multiple excitation modes into a system to cope with complex measuring conditions.

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