Article

QCA-Based Secure RAM Cell Structure Using Logic Transformation and Cell Interaction with Signal Reliability and Energy Dissipation in Quantum Computing

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Abstract: A RAM cell, one of the components that greatly affects the performance of quantum computing, outputs mostly stored values on quantum-dot cellular automata (QCA) as they are. Currently, a problem is that the stored value may be initialized according to the selection input. To solve this problem, circuits that separate the stored value from the output value have recently been designed, but most of them have long latency, large areas, and many plane structure intersections, resulting in unstable signals. Therefore, in this paper, we propose a new secure QRAM (QCA-based RAM) cell logic by analyzing and modifying the existing cell logic in nanotechnology. We initially propose 2-to-1 multiplexers based on cell interaction, and a QRAM cell is proposed based on our multiplexer and an optimized QRAM cell logic diagram. Compared with existing designs, the proposed circuits produce superior results in terms of circuit performance and energy dissipation. Additionally, the operation of our multiplexers is verified mathematically using physical proof. The secure QRAM cell proposed in this paper does not have the initialization problem based on the selection input that is present in some existing circuits, thus it is very easy to design an extension to $N \times N$ RAM, and it has high signal stability, reliability, connectivity, and scalability because there is no intersection.

Keywords: quantum computing; nanotechnology; quantum-dot cellular automata RAM; signal reliability; cell interaction; low-power dissipation

1. Introduction

CMOS is the semiconductor technology used in most of today's integrated circuits. The performance of CMOS has been improved by increasing the density of circuits; however, the speed of development of CMOS circuits is slowing due to physical limitations. Therefore, next-generation circuit technology to replace CMOS is being developed to solve this problem [1–6]. Quantum-dot cellular automata (QCA) is a next-generation digital nanocircuit design technology that does not use transistors [7,8]. Circuits designed with QCA have lower power, faster speed, and higher signal transmission stability than circuits designed with the CMOS technology [9–13]. Therefore, QCA is attracting attention from many research communities as an excellent next-generation circuit technology to replace CMOS [14,15].

In QCA, various circuits can be designed based on digital logic, including memory essential for computers. Representatively, RAM, ROM, CAM, and registers have been proposed, and currently, research is focused on designing registers and RAM [16–25]. The conventionally proposed QCA-based RAM cells have a disadvantage in that values stored in most circuits are initialized according to a selection input. This is because the value stored in the RAM cell and the actual output value are treated identically, greatly affecting scalability.

When RAM has multiple selection input lines, all the lines, except the line whose signal value is 1, transmit a signal of 0, hence, apart from the RAM cell that receives the signal of 1, the rest of the cells do not store values and are initialized. Therefore, when designing the RAM, only one selection input line has to be used. In the end, the corresponding circuits were designed with only 1 × N RAM, and N × N RAM cannot be designed using multiple select input lines due to scalability problems [16–20].

As a solution for designing an N × N type RAM, some studies have recently been carried out to design the stored values and output values differently [21–24]. These RAM cells can be designed to be extended to N × N type RAM like CMOS-based RAM cells. However, these RAM cells have a problem in that signal transfer is unstable due to the use of many planar structure intersections. In particular, the recently proposed circuit [22] uses a large number of planar intersections, thus the signal is unstable and the circuit does not operate properly.

The proposed 2-to-1 multiplexer is designed with a single clock and can satisfy the real clocking system with simple wiring clock control. We show a typical clocking design by fitting MXLR to 3 × 3 square bins so that the proposed circuits can potentially satisfy current real clocking systems. The contributions of this study can be summarized as follows:

- We design a planar 2-to-1 multiplexer circuit using cell interactions.
- We propose a RAM cell logic diagram that separates stored values and output values.
- Based on the proposed multiplexer and logic diagram, we propose a secure QCA-based RAM cell with excellent scalability.
- We show that the proposed structures can work well in a real clocking system by simply adjusting the clocking of the wire.
- The performance of the proposed circuit and existing circuits is verified and compared using QCADesigner.
- In addition, circuits are measured and compared with energy dissipation using QCAPro.
- The proposed multiplexer is mathematically verified through physical proof.

This paper is organized as follows. Section 2 explains the basic knowledge on QCA, the previously proposed multiplexer circuits, and the logic diagrams and circuits of RAM cells. Section 3 proposes the 2-to-1 multiplexers and the RAM cells designed based on them and provides the real clocking design by fitting our scheme in 3 × 3 square bins. In Section 4, the performances of the proposed circuit and existing circuits are compared. First, the circuits are compared based on the number of cells, area, delay time, and cost; the amount of energy dissipation in each circuit based on the tunneling energy of the RAM cells is also compared. Then, the multiplexer is mathematically verified using physical proof. Finally, Section 5 provides a summary and conclusion of the work.

2. Related Works

In this section, the basic description of the QCA circuit design, physical proof, and introduction of the existing multiplexer and RAM cell are provided.

2.1. Background on QCA

A quantum cell (hereafter referred to as QCA cell), which is the basic unit of the QCA circuit, has four quantum dots and consists of two floating electrons inside the quantum cell [25–27]. These electrons can move between the quantum dots, but they are located opposite each other because a repulsive force is generated that pushes them away from each other [28–31].

The electron position has two types of arrangements and depending on the type, it can have a polarization of +1 (binary logic 1) or −1 (binary logic 0), as shown in Figure 1a [4]. In addition, electrons inside different cells also generate a force that pushes them away from each other, causing the polarization of adjacent cells to be the same [32]. This is called QCA wiring and the value is passed from the INPUT cell to the right (Figure 1b).

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Figure 1. Two polarization states of the QCA basic cell: (**a**) P = +1 (binary 1), P = −1 (binary 0); (**b**) QCA cell-based wiring.

Figure 2 shows the basic gates composed of QCA cells. Figure 2a shows a 3-input majority vote gate. It consists of three input cells (A, B, C) and one output cell (OUT), and outputs two or more identical values among the three input values as a result [33,34]. Figure 2b,c show that the polarization of one input cell is fixed to −1 (or +1) in the 3-input majority gate of Figure 2a, and AND or OR operations are performed, respectively [35]. Figure 2d is a rotated 3-input majority vote gate, which is rotated 45° from the normal cell in the center in the cross-shaped cell arrangement of Figure 2a. Figure 2d can also be used by transforming it into an AND/OR gate as shown in Figure 2b,c [36].
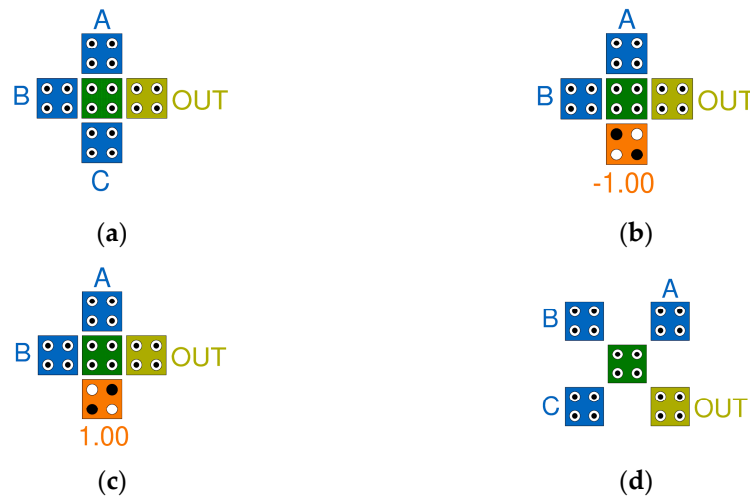
Figure 2. QCA basic gates: (**a**) 3-input majority gate; (**b**) AND gate; (**c**) OR gate; (**d**) rotated 3-input majority gate.

2.2. Typical 2-to-1 Multiplexer

A multiplexer is a circuit that outputs only one signal among several input signals based on a selected input value. A multiplexer is used as a key element in various circuits. A D-latch, which is a key circuit of a RAM cell that can generate a loop section, can be designed using a multiplexer. A D-latch can be designed simply by deleting one input cell of the multiplexer and extending and connecting the wiring of the output cell to that location. Therefore, the multiplexer is a key circuit in the design of RAM cells. There are two types of conventionally proposed 2-to-1 multiplexers: a majority gate-based design using three majority gates and one inverter, and a design based on interactions between electrons inside the cell. Figure 3 shows a multiplexer based on a majority vote gate among the previously proposed QCA 2-to-1 multiplexers. Figure 3a,b shows circuits proposed by Iqbal et al., and Sen et al., respectively, and both are designed based on a 3-input majority vote gate and are designed for stable signal transmission rather than circuit size [37,38]. Figure 3c,d shows circuits proposed by Ahmad et al., and Rezai et al. The area of the circuits is greatly reduced using a combination of the rotated 3-input majority gate in Figure 2d and the general 3-input majority gate [39,40]. Jain et al., also used the rotated gate based on a multilayer structure [41], while Vahabi et al. proposed a cell-interaction-based multiplexer with minimal area but latency in 2023 [42].
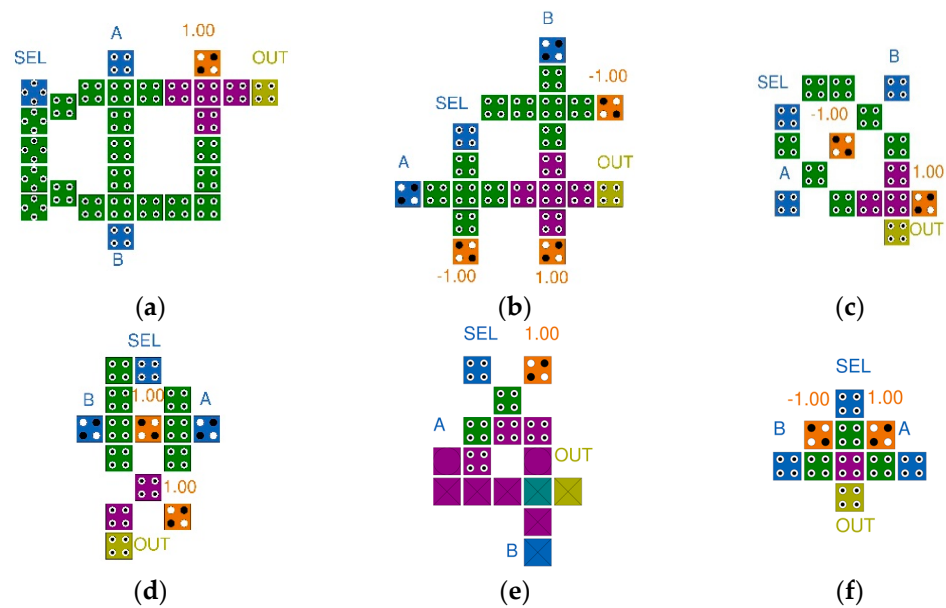
Figure 3. Typical QCA 2-to-1 Multiplexers: (**a**) circuit developed by Iqbal et al. [37]; (**b**) circuit developed by Sen et al. [38]; (**c**) circuit developed by Ahmad et al. [39]; (**d**) circuit developed by Rezai et al. [40]; (**e**) circuit developed by Jain et al. [41]; (**f**) circuit developed by Vahabi et al. [42].

2.3. Physical Proof

Physical proof is a mathematical method that confirms which polarization is correct through each potential energy, assuming that the polarization of the QCA cell whose polarization has not been determined is +1 or −1 [37–41]. Assuming the polarization of electrons in a specific QCA cell, the potential energy interacting with the electrons in the cell and adjacent cells is calculated, and then the sum is calculated. The total sum of potential energies when the polarization of the cell is −1 and +1 is calculated, and the values are compared to determine whether the electrons in the cell are disposed of with the polarization having lower energy. As an example of a majority voting gate, assuming that the polarization of the center cell is −1 or +1, the potential energy is calculated by measuring the distance between the electrons inside input cells A, B, and C and the electrons placed inside the center cell. After adding all these values and comparing them, the polarization on the side with the lower value can be determined as the polarization of the center cell.

2.4. Typical RAM Cell

Figure 4 shows logic diagrams of recently proposed RAM cells. Figure 4a is a logic diagram based on a majority vote gate, and this type of RAM cell has been most frequently proposed [17]. A 5-input majority vote gate is used to store values and is characterized by resetting to 0 (RESET) or setting to 1 (SET) depending on whether the values of SET and RESET are equal. Figure 4b is a multiplexer-based RAM cell logic diagram that selects either SET/RESET or IN as the input value based on the SEL function and then selects and outputs the input value or stored value based on the R/W value [20]. Figure 5 shows the logic diagrams of a RAM cell that can be expanded to an N × N RAM among previously proposed circuits. Figure 5a was proposed by Mubarakali et al. [21] and used four AND gates, one OR gate, and one multiplexer. Figure 5b is the logic diagram proposed by Heydari et al. [22], designed using four AND gates, one OR gate, and one majority vote gate.
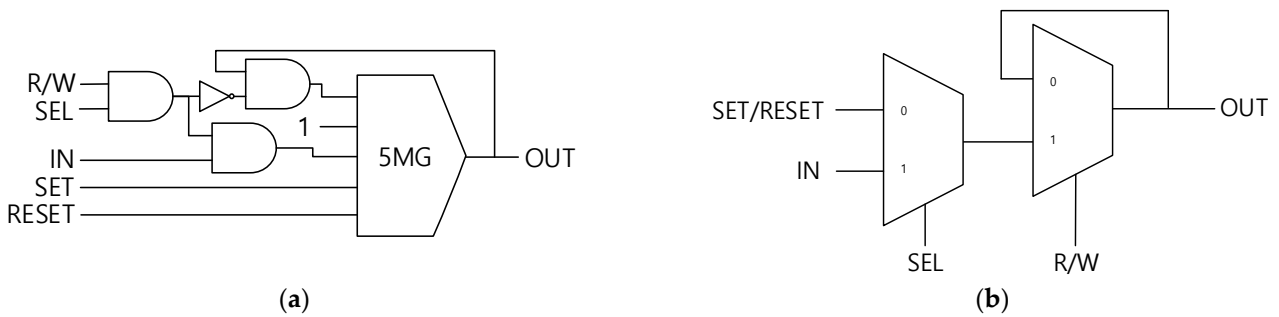
Figure 4. Typical logic diagrams of non-expandable RAM cells: (**a**) 5-input majority vote gate-based RAM cell [17]; (**b**) multiplexer-based RAM cell [20].
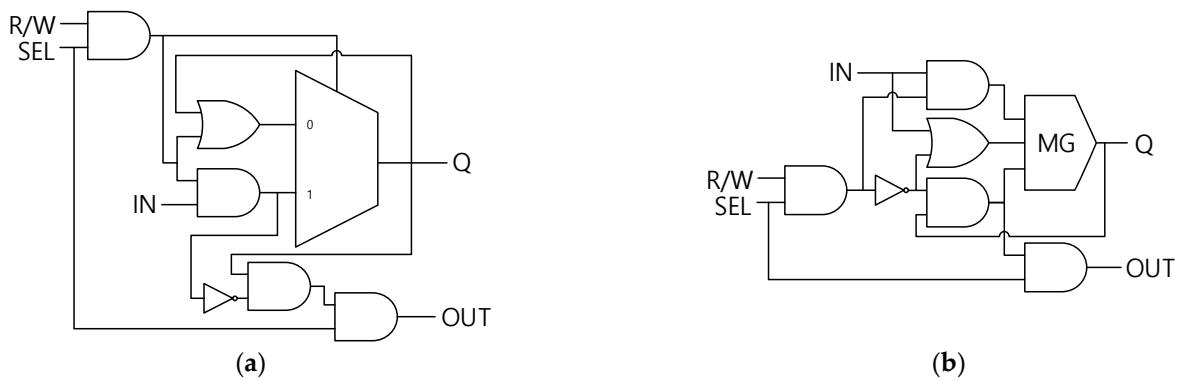

Figure 5. Typical logic diagrams of expandable RAM cells: (**a**) logic diagram proposed by Mubarakali et al. [21]; (**b**) logic diagram proposed by Heydari et al. [22].

Figure 6 shows the previously proposed QCA RAM cells. Figure 6a is a RAM cell designed by Majeed et al. using a 5-input majority vote gate as a D-latch [17]. The circuit connects SEL (Select) and R/W (Read/Write) with an AND gate to transmit a selection signal to a 5-input majority vote gate. If both SET and RESET values are 1 or 0, the corresponding circuit stores and outputs 1 or 0, regardless of other input values. When the values of SET and RESET are different and SEL = R/W = 1, that is, when the corresponding RAM cell is activated and the Write function is executed, the value of IN is output and saved. Conversely, if at least one of the SEL and R/W values is 0, the previously stored value is output.

Figure 6b is a QCA RAM cell designed by Sasamal et al. using a rotated 3-input majority gate [20]. This circuit was designed based on a multiplexer implemented using a rotated 3-input majority gate, and one of the two multiplexers was modified to be a D latch. This circuit selects the value to be updated by IN or SET/RESET based on the value of SEL and transmits it to the D latch and outputs and stores the value to be updated based on the value of R/W, or outputs the previously stored value.

The above two circuits cannot be used to design N x N type RAM because the value to be stored and the value to be output are the same. Figure 6c is a QCA RAM cell proposed by Mubarakali et al. [21]. Figure 6c shows the modification and design of the multiplexer into a D latch, but the values to be stored and the values to be output are set differently. This means that when SEL = 0, the stored value is not initialized and is continuously stored, and N × N RAM can be designed using this function.
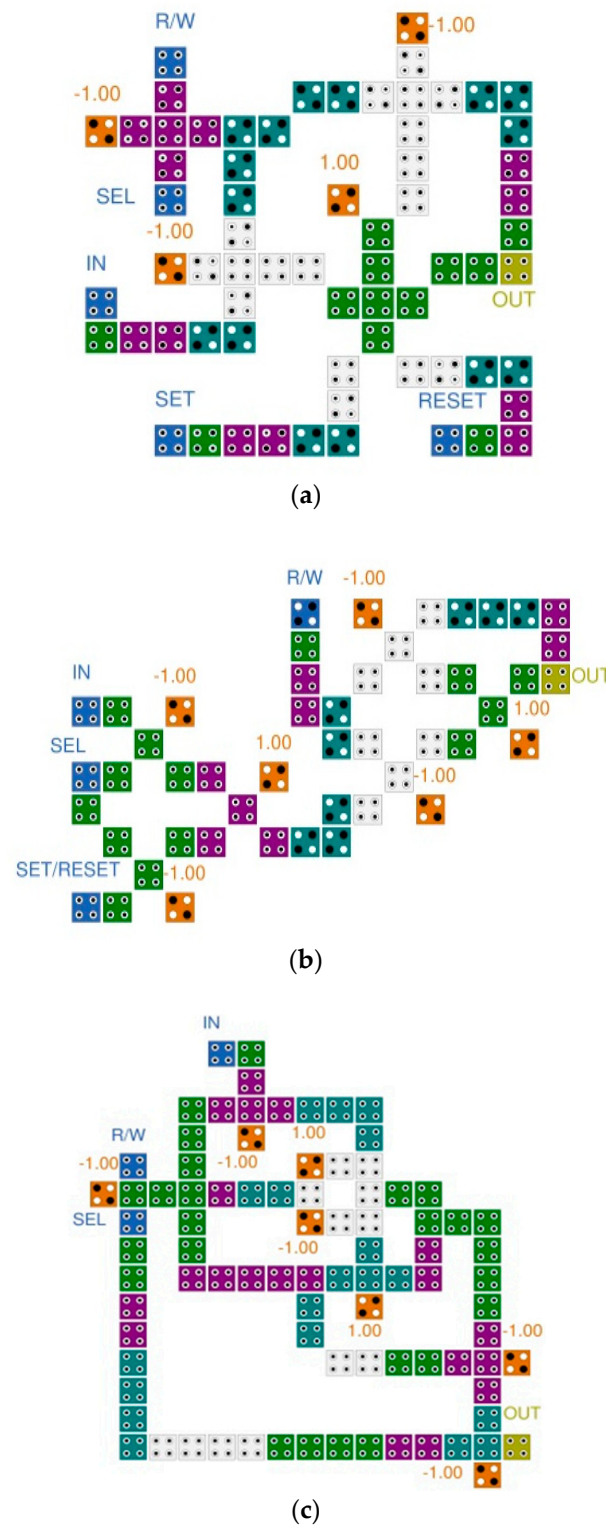
(**a**)

(**b**)

(**c**)

Figure 6. Typical QCA RAM cell: (**a**) circuit developed by Majeed et al. [17]; (**b**) circuit developed by Sasamal et al. [20]; (**c**) circuit developed by Mubarakali et al. [21].

3. Proposed QCA Circuits

In this section, the proposed 2-to-1 multiplexers and QCA RAM cell with logic transformation are described.

3.1. Proposed 2-to-1 Multiplexer

Figure 7 shows the QCA 2-to-1 multiplexers proposed in this study. The proposed multiplexers are circuits designed through interactions between electrons inside cells. They are designed to minimize the number of cells, space used, and delay time. Both consist of 13 cells, have an area of 0.01 μm^2, and a latency of 0.25 clock cycles. In both circuits, the signal propagates through the inverter twice and the signal of one fixed cell is attenuated based on the value of SEL, the signal of the other fixed cell is strengthened, and the value is transmitted to the output cell. The proposed multiplexers are easy to connect with other circuits and have good scalability because the input and output cells are arranged on one side.
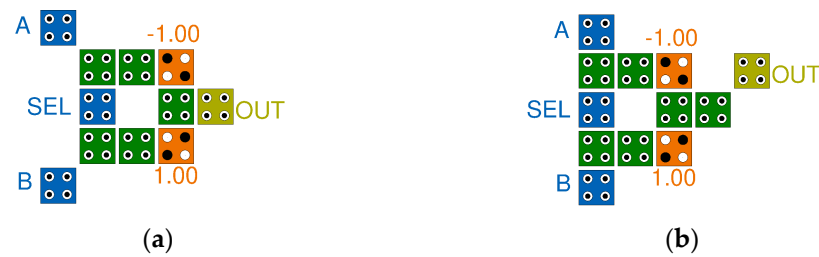

(**a**)   (**b**)

Figure 7. Proposed QCA 2-to-1 multiplexer: (**a**) multiplexer for connection (MXC); (**b**) multiplexer for loop (MXL).

Figure 7a is a connection-type multiplexer that has a symmetrical structure in which input and output cells are evenly distributed on both sides. Therefore, any expansion circuit can be used without a loop section. Figure 7b is a modified circuit that can be used when designing an extension circuit with a loop section. Since the output cell is placed above the center, it is convenient to connect the output cell OUT and the input cell A to create a loop section.

3.2. Proposed QCA RAM Cell

Table 1 is a truth table of RAM cells used in digital circuits. It has three input values—SEL, R/W, and IN—and an output value, OUT. Q_{t-1} is the value of Q_t stored in the RAM cell at the previous time step, and Q_t is the value stored in the current RAM cell. If SEL = 0, OUT outputs 0, and Q_t does not change its value. When SEL = 1, read/write functions are performed based on the value of R/W, and when R/W = 0, read functions are performed. At this time, Q_t maintains the value as it is and OUT outputs the value of the stored value Q_{t-1}. Conversely, if R/W = 1, the write function is performed, while at this time, Q_t and OUT output the value of IN. Based on the truth table in Table 1, the expression of the output value is summarized as (1) and (2).

Table 1. Truth table for the RAM cell memory unit.

SEL	R/W	IN	Q_{t-1}	Q_t	OUT
0	X	X	X	Q_{t-1}	0
1	0	X	0	$0(Q_{t-1})$	$0(Q_{t-1})$
1	0	X	1	$1(Q_{t-1})$	$1(Q_{t-1})$
1	1	0	X	0	0(IN)
1	1	1	X	1	1(IN)

$$OUT = SEL \times R/W \times IN + SEL \times \overline{R/W} \times Q_{t-1} \qquad (1)$$

$$Q_t = SEL \times R/W \times IN + \overline{SEL \times R/W} \times Q_{t-1} \qquad (2)$$

As shown in Equation (1), the most important input value in the selected RAM cell is R/W. Since the resulting value changes based on R/W, Equation (1) can be modified to

Equation (3). In addition, since the circuit operates when SEL = 1 and the output value when SEL = 0, OUT = 0, Equation (3) can be replaced with Equation (4). Equation (2) can be transformed into Equation (5) using the same principle.

$$OUT = SEL \times MUX(R/W, IN, Q_{t-1}) \tag{3}$$

$$OUT = SEL \times MUX(SEL \times R/W, IN, Q_{t-1}) \tag{4}$$

$$Q_t = MUX(SEL \times R/W, IN, Q_{t-1}) \tag{5}$$

Figure 8 is a proposed RAM cell logic diagram based on Equations (4) and (5), designed using a multiplexer and two AND gates. The corresponding logic diagram is designed to minimize the number of gates, and is very simplified compared with the existing logic diagram.
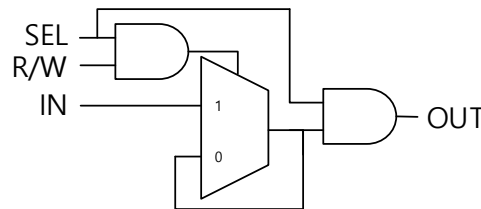

Figure 8. Proposed logic diagram of QCA RAM cell.

Figure 9 shows the QCA RAM cell proposed in this paper. It consists of a 2-to-1 multiplexer, a 3-input majority gate, and a rotated 3-input majority gate, shown in Figures 2 and 7. First, an input value IN or a stored value is output through cell Q using a multiplexer. The output value Q is connected to the input of the multiplexer or connected to the input cell SEL and the AND gate. At this time, if SEL = 1, Q is output to cell OUT, and if SEL = 0, the binary value 0 is output. Figure 9a,b show designs based on MXC and MXL. MXLR is designed to be suitable for making loop structures, and MXCR has low spatial density. Meanwhile, the proposed 2-to-1 multiplexer is designed with a single clock and can satisfy the real clocking system with a simple wiring clock control. Figure 10 shows a typical clocking design by fitting MXLR to 3 × 3 square bins so that the proposed circuits can potentially satisfy current real clocking systems [43,44].
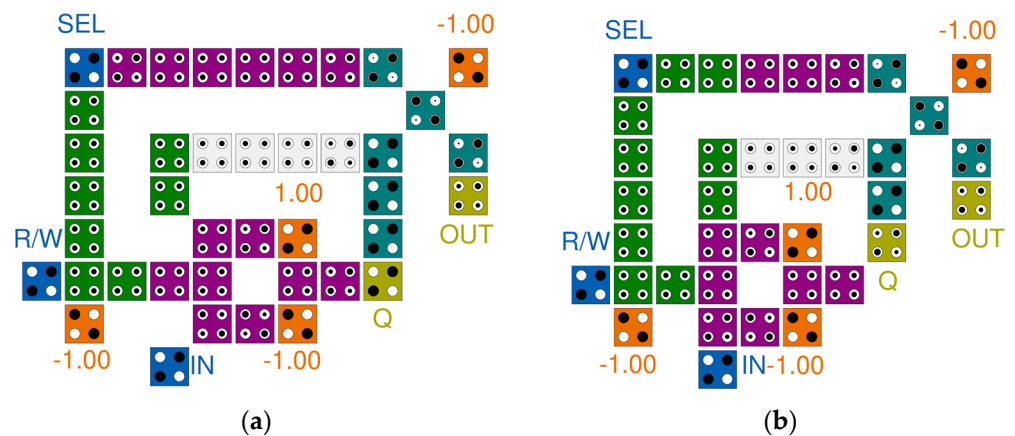

Figure 9. Proposed QCA RAM cell: (**a**) MXC-based RAM cell (MXCR); (**b**) MXL-based RAM cell (MXLR).
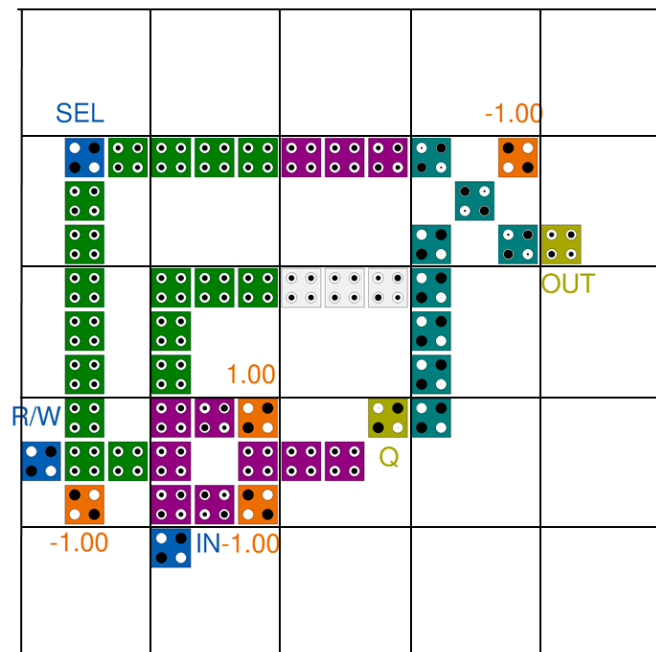
Figure 10. Real clocking for proposed MXLR using 3 × 3 square bins.

4. Analysis and Discussion

4.1. Simulation Results and Performance Analysis

Table 2 is the truth table of a 2-to-1 multiplexer. It has three input values—SEL, A, and B—and one output value, OUT. If SEL = 0, the value of B is output, and if SEL = 1, the value of A is output. Figure 11 is the simulation result of the proposed 2-to-1 multiplexer, and it can be confirmed that both MXC and MXL operate normally. In this study, all circuits were simulated using QCADesigner 2.0.3, and coherence vector simulation engine. The tested parameters were set as shown in Table 3 [45].

Table 2. Truth table for a 2-to-1 multiplexer.

SEL	A	B	OUT
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Table 3. Simulation parameters.

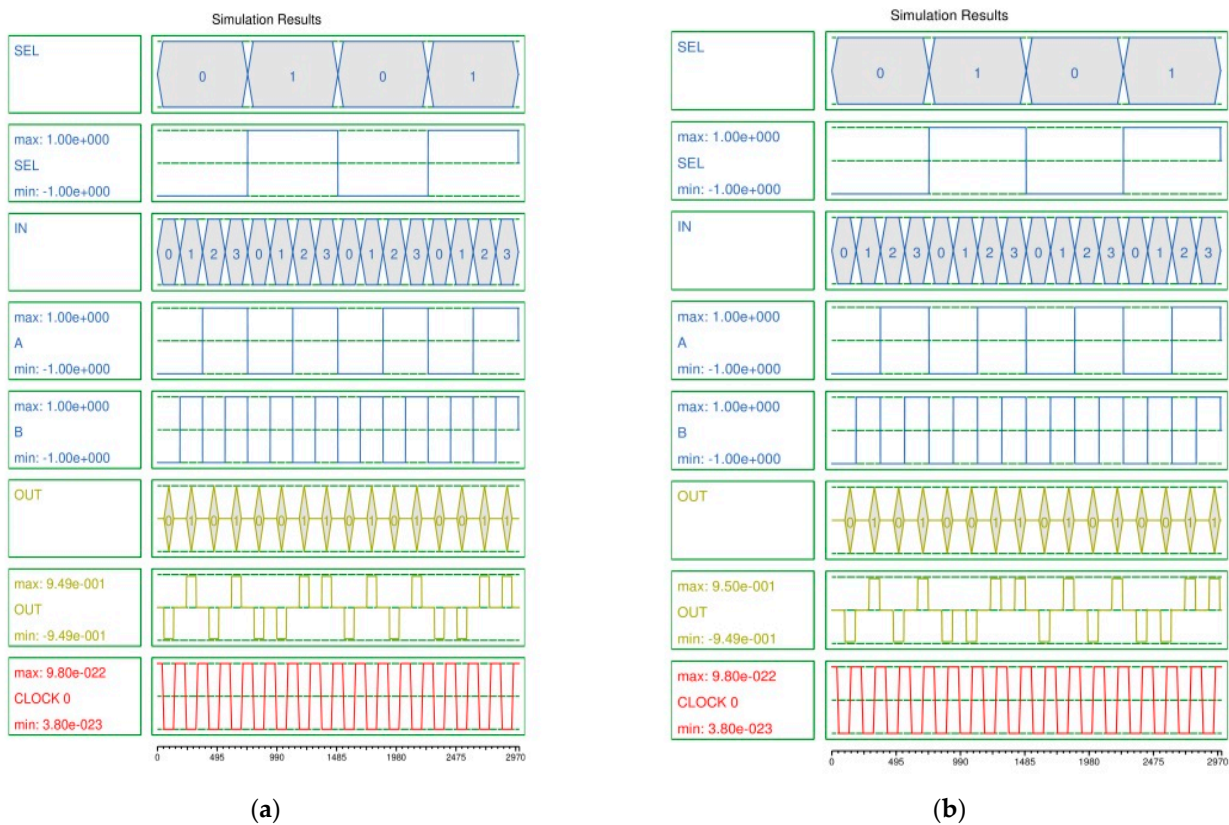| Parameters	Coherence Vector
Cell size	18 nm
Dot diameter	5 nm
Cell separation	2 nm
Layer separation	11.5 nm
Clock high	9.8×10^{-22} J
Clock low	3.8×10^{-23} J
Clock shift	0
Clock amplitude factor	2.0
Relative permittivity	12.9
Temperature	1 K
Relaxation time	1.0×10^{-15} s
Time step	1.0×10^{-16} s
Radius of effect	80 nm

Figure 11. Simulation results of proposed 2-to-1 multiplexers: (**a**) MXC, (**b**) MXL.

Figure 12 shows the simulation results of the proposed RAM cells. If the selected input cell SEL = 0, 0 is output from the output cell OUT. When SEL = 1 and input cell R/W = 0, that is, when performing the read function, the stored value, 1, is output. Conversely, when SEL = 1 and R/W = 1, that is, when performing the write function, 0 and 1, the values of the input cell IN, are sequentially output. Both MXLR and MXCR add one cell before the output cell (OUT) for signal stability and reliability.

Table 4 shows comparisons between the QCA 2-to-1 multiplexer and previously proposed 2-to-1 multiplexers. The comparison standards are the number of cells, the number of fixed inputs, the circuit area, and latency. The AT^2 is calculated by multiplying the area of the circuit by the square of the latency [43]. The proposed multiplexers show remarkable performance improvements compared with existing majority vote gate-based multiplexers [37–41] and recent cell-interaction-based multiplexers [42]. AT^2 reduced from a minimum of 83% to a maximum of 92% compared with the existing majority gate-based circuit. A cost reduction of 69% or more compared with the latest cell-interaction-based circuit was confirmed.

Table 4. Comparison of the performance of 2-to-1 multiplexers.

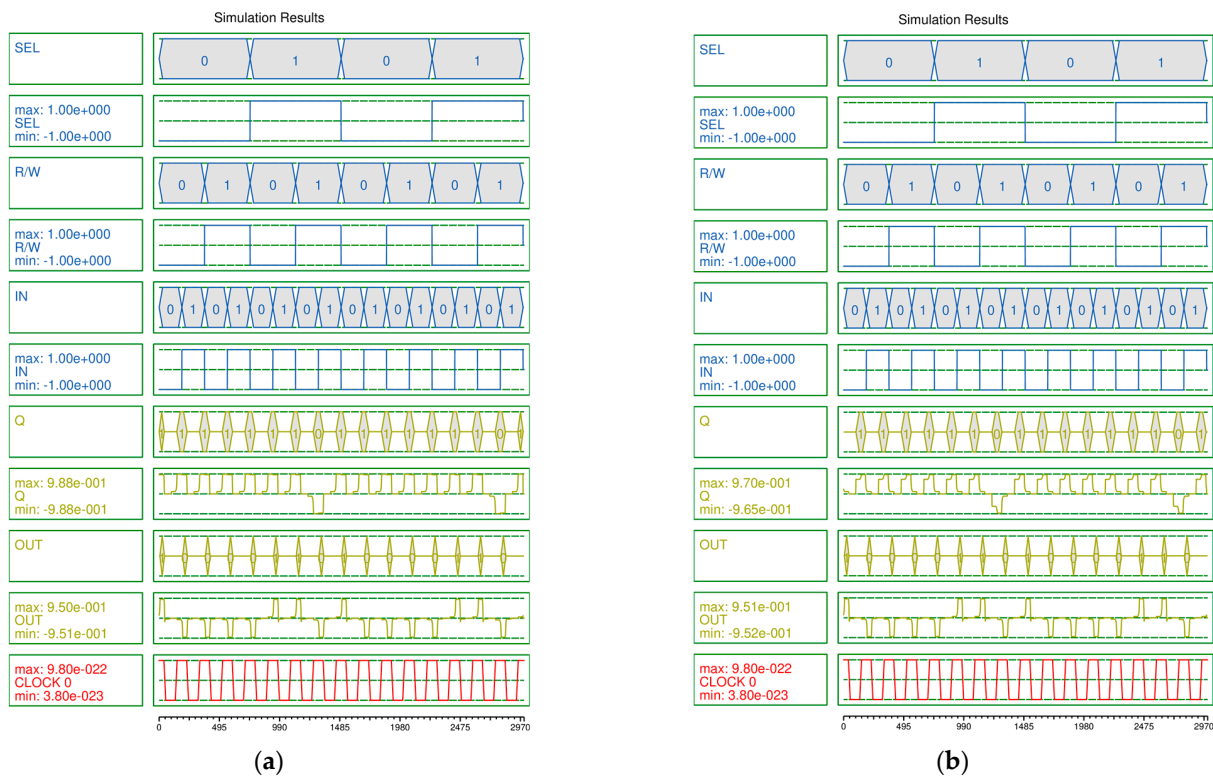| Circuit	Cell Count (# of Fixed Inputs)	Area (nm^2)	Latency (Clock Cycle)	AT^2 (Area $\times$ Latency^2)	Crossover
[37]	28 (1)	24,564	0.5	6141	Coplanar
[38]	23 (3)	24,964	0.5	6241	Coplanar
[39]	16 (2)	13,924	0.5	3481	Coplanar
[40]	15 (2)	15,524	0.5	3881	Coplanar
[41]	20 (1)	13,524	0.75	7607	Multilayer
[42]	10 (2)	7644	0.5	1911	Coplanar
MXC	11 (2)	9604	0.25	600	Coplanar
MXL	12 (2)	9604	0.25	600	Coplanar

Figure 12. Simulation results of the proposed RAM cells: (**a**) MXCR, (**b**) MXLR.

Table 5 is a performance table for QCA RAM cells, comparing recently proposed RAM cells. Compared to circuits [21,22], which separate stored and output values, the proposed circuit reduces the number of cells by 59.77%, the area by 66.6%, and latency by 57.14% and 40%, respectively. In addition, compared to the circuit in [19], which has the highest overall performance, 40.67% of the cell count and 57.14% of the area are reduced, and the AT^2 is reduced by 57.14%.

Table 5. Comparison of the performance of QCA RAM cells.

Circuit	Cell Count (# of Fixed Inputs)	Area (μm²)	Latency (Clock Cycle)	AT² (Area × Latency²)	Cost$_{II}$
[16]	108 (4)	0.11	1.25	0.171875	669
[17]	67 (4)	0.06	1.25	0.093750	754
[18]	92 (3)	0.10	1.5	0.225000	2046
[19]	59 (6)	0.07	0.75	0.039375	434
[20]	75 (6)	0.10	1.5	0.225000	950
[21]	87 (7)	0.09	1.75	0.275625	2781
[22]	87 (5)	0.09	1.25	0.140625	950
[23]	71 (4)	0.06	1.25	0.093750	859
[24]	94 (4)	0.08	1.25	0.125000	577
MXCR	41 (4)	0.03	1.00	0.030000	298
MXLR	37 (4)	0.03	0.75	0.016875	183

For a more objective performance evaluation, the cost function discussed in reference [23,43] has been applied.

$$Cost_I = \left(M^k + I + C^l \right) \times T^p, \ 1 \leq k, \ l, \ p \qquad (6)$$

where M is the number of majority gates, I is the number of inverters, C is the number of crossovers, and T is the delay of the circuit and k, l, p are the exponential weightings for

majority gate count, crossover count and delay, respectively. All circuits compared here are coplanar structures so there is no need to consider the number of layers.

However, when a 5-input majority gate and a multiplexer using cell interactions were added, we modified the equation to take these into account. The modified equation is shown in Equation (7).

$$Cost_{II} = \left((M_3 + F_1 \times M_5 + F_2 \times M_C)^k + I + C^l\right) \times T^p \tag{7}$$

where F_1 and F_2 are the ratios of the number of cells of the five-input majority and the cell-interaction-based multiplexer under consideration to the number of cells of the 3-input majority gate, and M_C is the number of cell-interaction-based multiplexer. In the most general case, a double weighting is applied to M and C which are associated with both complexity and fabrication difficulty, and a double weighting can be given to the delay as well since the demand for speed in recent circuit designs is increasing [43].

The result of $COST_I$ has the problem of not accurately counting the 5-input majority gate and the cell interaction MUX. The RAM cells in references [16–18,23,24] contain at least one 5-input majority gate, and the RAM cells in references [19–21], MXCR, and MXLR contain at least one cell interaction MUX. Therefore, it is judged that $COST_{II}$ is a more objective and equally compared result ($COST_{II}$ is rounded to one decimal place). As shown in Table 5, the proposed MXLR reduced the cost by a maximum of 93.42%, and it was confirmed that the cost was reduced by 57.83% compared with the circuit in [19], which is the best among the existing studies. As a result, it can be confirmed that the proposed circuits show excellent AT^2 and $COST_{II}$ results.

4.2. Power Dissipation Analysis

QCAPro can handle a large number of cells through a fast approximation-based technique and can calculate switching energy dissipation due to polarization in the QCA circuit [45–47]. Figures 13–15 classify the energy loss of the proposed circuits by energy amount using QCAPro. Average leakage energy dissipation, average switching energy dissipation, and total switching energy dissipation were measured and a temperature value of 2 k was specified as a parameter in QCAPro. The levels of applied energy were designated as 0.5 *Ek*, 1.0 *Ek*, and 1.5 *Ek*, respectively, and comparative analysis was performed.
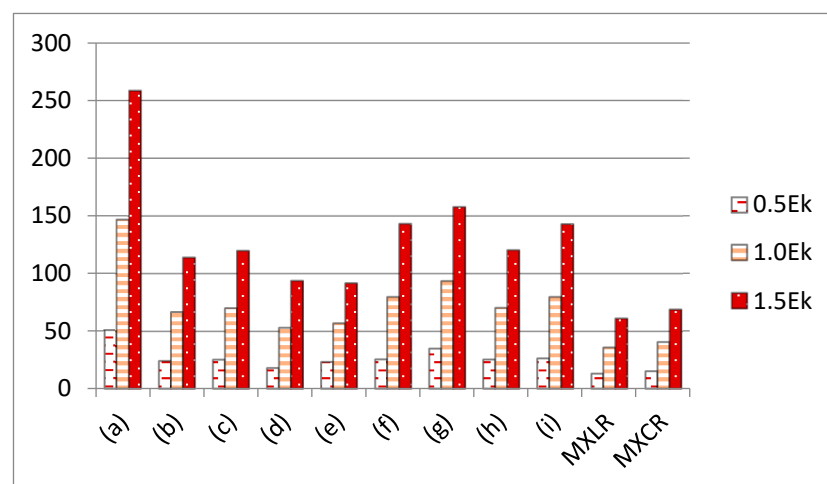

Figure 13. Avg. leakage energy dissipation based on the amount of energy (meV): (a) [16]; (b) [17]; (c) [18]; (d) [19]; (e) [20]; (f) [21]; (g) [22]; (h) [23]; (i) [24].
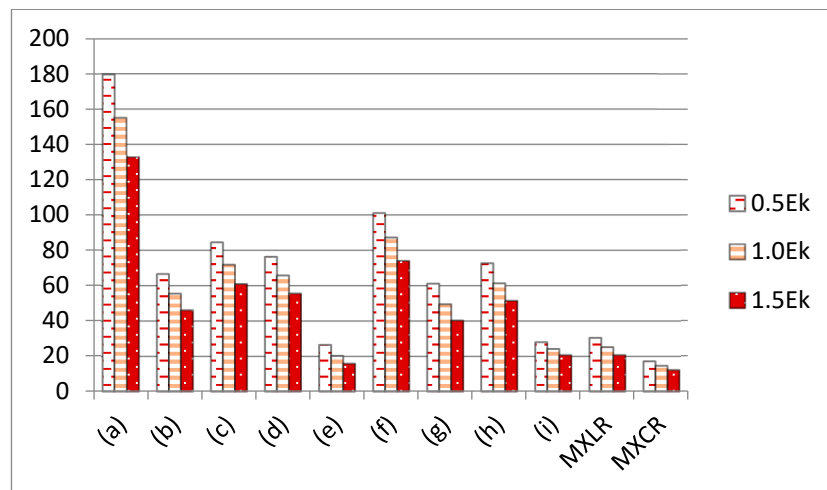
Figure 14. Avg. switching energy dissipation based on the amount of energy (meV): (a) [16]; (b) [17]; (c) [18]; (d) [19]; (e) [20]; (f) [21]; (g) [22]; (h) [23]; (i) [24].
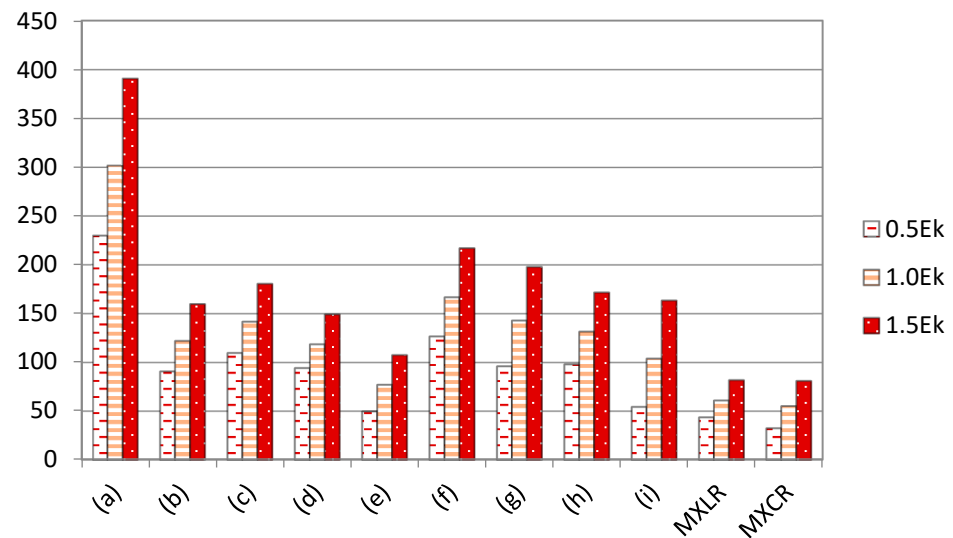

Figure 15. Total switching energy dissipation based on the amount of energy (meV): (a) [16]; (b) [17]; (c) [18]; (d) [19]; (e) [20]; (f) [21]; (g) [22]; (h) [23]; (i) [24].

The results of energy loss analysis showed that both proposed circuits showed lower total energy dissipation compared with conventional RAM cells. The circuit with the best performance was MXCR, which had about 35.04% lower energy dissipation at 0.5 *Ek*, 28.58% at 1.0 *Ek*, and 24.73% lower energy efficiency at 1.5 *Ek* compared with the results of [20], which had the highest energy efficiency among the previously proposed circuits.

MXLR also confirmed that total energy dissipation is far superior to existing circuits. In addition, MXLR has more energy loss when low energy is applied compared with MXCR, but the higher the applied energy, the lower the increase in the average leakage energy and the smaller the switching energy loss, such that the total energy dissipation is relatively low. Therefore, the performance of MXLR outperforms that of MXCR when an energy of 1.5 Ek or more is applied.

Figure 16 shows dissipated power maps that occur when 0.5 Ek of energy is applied to RAM cells. The rectangles represent QCA cells; the darker the color, the greater the amount of energy leakage from the cell.
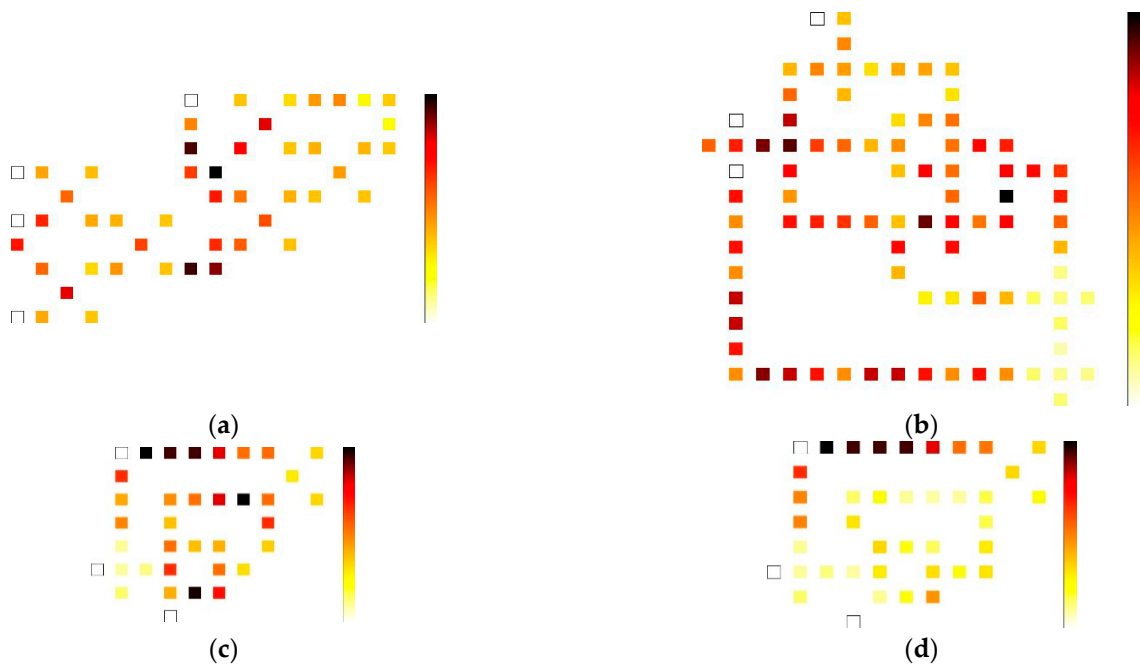
Figure 16. Dissipated power maps of RAM cells (0.5 Ek): (**a**) [20]; (**b**) [21]; (**c**) MXLR; (**d**) MXCR.

4.3. Physical Proof of the Proposed 2-to-1 Multiplexer

Equation (8) is a formula for calculating the potential energy due to the interaction between electrons. *U* is the potential energy, *k* is the Coulomb constant, q_1 and q_2 are the magnitudes of the charge of the electron, and *r* is the distance between the two electrons. At this time, since *k*, q_1, and q_2 are constants, the numerator can be treated as a constant in Equation (8). The corresponding constant value is called *A* and is expressed as in Equation (9). In addition, the potential energy of the cell's electronic configuration is expressed as the sum of the potential energies of two electrons in the cell (U_T) and is shown in Equation (10) [36].

$$U = \frac{kq_1q_2}{r} \tag{8}$$

$$A = kq_1q_2 = 9 \times 10^9 \times \left(1.6^2\right) \times 10^{-38} = 23.04 \times 10^{-29} \tag{9}$$

$$U_T = \sum_{i=1}^{2} U_i \tag{10}$$

Before making a physical proof, some assumptions are necessary. First, it is assumed that all cells are square, with a side length of 18 nm and a distance between cells of 2 nm. Second, the quantum dots of the QCA cell are located at the vertices of the cell, and electrons are also located at the center of the QCA cell. Third, the maximum distance for the interaction between electrons is 80 nm. In other words, if the distance between electrons exceeds 80 nm, they cannot affect each other.

For the multiplexer proposed in this paper to output the value of A, SEL = 1 is required. In order to physically prove this, it is assumed that A, SEL = 1, and B = −1, and physical proof is performed. Figure 17 is physical proof of the proposed multiplexer. There are five cells whose polarization is unknown. Each cell is numbered and the polarization corresponding to each cell is obtained. Since the proposed multiplexer outputs the polarization opposite to that of cell 5, the output value of the multiplexer can be determined by finding the polarization of cell 5. Physical proof was performed using the proposed MXL and showed that left–right reversal does not affect the overall result.
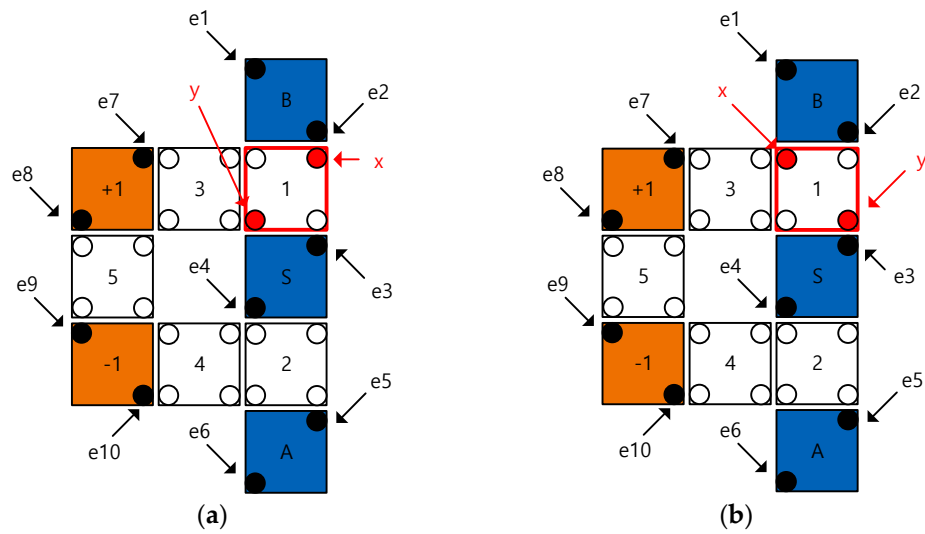
Figure 17. Physical proof of MXL: (**a**) Case 1: cell1 = +1; (**b**) Case 2: cell1 = −1.

The electrons inside the input cell are designated e1 to e6, and the electrons inside the fixed cell are designated e7 to e10. The electrons inside the cell to be obtained are indicated by x and y, and the polarization of cell No. 1 is verified. Figure 17a,b shows the verification process when the polarization of cell 1 is assumed to be +1 or −1.

$$
\begin{aligned}
E_{1X} &= \frac{23.04 \times 10^{-29}}{26.91 \times 10^{-9}} = 8.563 \times 10^{-21} & E_{1Y} &= \frac{23.04 \times 10^{-29}}{38.00 \times 10^{-9}} = 6.063 \times 10^{-21} \\
E_{2X} &= \frac{23.04 \times 10^{-29}}{2.00 \times 10^{-9}} = 1.152 \times 10^{-19} & E_{2Y} &= \frac{23.04 \times 10^{-29}}{26.91 \times 10^{-9}} = 8.563 \times 10^{-21} \\
E_{3X} &= \frac{23.04 \times 10^{-29}}{20.00 \times 10^{-9}} = 1.152 \times 10^{-20} & E_{3Y} &= \frac{23.04 \times 10^{-29}}{18.11 \times 10^{-9}} = 1.272 \times 10^{-20} \\
E_{4X} &= \frac{23.04 \times 10^{-29}}{42.05 \times 10^{-9}} = 5.48 \times 10^{-21} & E_{4Y} &= \frac{23.04 \times 10^{-29}}{20.00 \times 10^{-9}} = 1.152 \times 10^{-20} \\
E_{5X} &= \frac{23.04 \times 10^{-29}}{60.00 \times 10^{-9}} = 3.84 \times 10^{-21} & E_{5Y} &= \frac{23.04 \times 10^{-29}}{45.69 \times 10^{-9}} = 5.042 \times 10^{-21} \\
E_{6X} &= \frac{23.04 \times 10^{-29}}{80.05 \times 10^{-9}} = 2.878 \times 10^{-21} & E_{6Y} &= \frac{23.04 \times 10^{-29}}{60.00 \times 10^{-9}} = 3.84 \times 10^{-21} \\
E_{7X} &= \frac{23.04 \times 10^{-29}}{40.00 \times 10^{-9}} = 5.76 \times 10^{-21} & E_{7Y} &= \frac{23.04 \times 10^{-29}}{28.43 \times 10^{-9}} = 8.105 \times 10^{-21} \\
E_{8X} &= \frac{23.04 \times 10^{-29}}{60.73 \times 10^{-9}} = 4.794 \times 10^{-21} & E_{8Y} &= \frac{23.04 \times 10^{-29}}{40.00 \times 10^{-9}} = 5.76 \times 10^{-21} \\
E_{9X} &= \frac{23.04 \times 10^{-29}}{70.46 \times 10^{-9}} = 3.27 \times 10^{-21} & E_{9Y} &= \frac{23.04 \times 10^{-29}}{45.65 \times 10^{-9}} = 5.047 \times 10^{-21} \\
E_{10X} &= \frac{23.04 \times 10^{-29}}{70.46 \times 10^{-9}} = 3.27 \times 10^{-21} & E_{10Y} &= \frac{23.04 \times 10^{-29}}{45.65 \times 10^{-9}} = 5.047 \times 10^{-21}
\end{aligned}
$$

$$
U_X = \sum_{i=1}^{10} E_{iX} = 1.636 \times 10^{-19} \tag{11}
$$

$$
U_Y = \sum_{i=1}^{10} E_{iY} = 7.171 \times 10^{-20} \tag{12}
$$

First, the potential energy is analyzed when cell 1 = +1. In Figure 17a, the value of the potential energy that x and y have with the adjacent electrons is defined using Equation (11). U_X and U_Y represent the potential energies of x and y, respectively. For example, E_{1x} and E1y refer to the potential energies of two electrons, x and e1 and y and e1 interacting with each other. Therefore, the potential energies of U_X and U_Y when the polarization of cell 1 = +1 can be expressed by Equations (11) and (12), respectively, and the sum of these values is equal to Equation (13). In the same way, in Figure 17b, the potential energy when cell 1 = −1 polarization is equal to (14).

$$
U_T = U_X + U_Y = 1.636 \times 10^{-19} + 7.171 \times 10^{-20} = 2.353 \times 10^{-19} \tag{13}
$$

$$
U_T = U_X + U_Y = 6.901 \times 10^{-20} + 1.679 \times 10^{-19} = 2.369 \times 10^{-19} \tag{14}
$$

The results of the comparison showed that since the potential energy when the polarization of cell 1 = +1 is smaller than the potential energy when the polarization is −1, the polarization of cell 1 is determined to be +1. The polarization of cell 2 is +1 because two cells with the same polarization are adjacent to each other. For the polarization of cell 3, the potential energy generated by the electrons inside the fixed cell +1, −1, input cells S, A, B, and cell 1 and cell 2 is obtained, which is the same as Equations (15) and (16).

$$P = +1 : U_T = U_X + U_Y = 1.02 \times 10^{-19} + 1.035 \times 10^{-19} = 2.055 \times 10^{-19} \tag{15}$$

$$P = -1 : U_T = U_X + U_Y = 1.865 \times 10^{-19} + 2.082 \times 10^{-20} = 3.947 \times 10^{-19} \tag{16}$$

The results of Equations (15) and (16) show that when the polarization of cell 3 is +1, the potential energy is lower, thus the polarization of cell 3 is determined to be +1. The polarization of cell 4 can also be obtained using the potential energy with the 7 cells mentioned above, and the results are obtained using Equations (17) and (18), and the polarization of cell 4 is +1, based on the results. Now, the polarization of cell 5 is obtained through the potential energy generated between the above-mentioned 7 cells, cell 3, and cell 4.

$$P = +1 : U_T = U_X + U_Y = 1.774 \times 10^{-19} + 8.165 \times 10^{-20} = 2.591 \times 10^{-19} \tag{17}$$

$$P = -1 : U_T = U_X + U_Y = 9.956 \times 10^{-20} + 2.108 \times 10^{-19} = 3.103 \times 10^{-19} \tag{18}$$

$$P = +1 : U_T = U_X + U_Y = 2.004 \times 10^{-19} + 2.089 \times 10^{-19} = 4.093 \times 10^{-19} \tag{19}$$

$$P = -1 : U_T = U_X + U_Y = 2.093 \times 10^{-19} + 1.377 \times 10^{-19} = 3.47 \times 10^{-19} \tag{20}$$

The process of obtaining the polarization of cell 5 is as shown in Equations (19) and (20), and the results of potential energy comparisons showed that the potential energy is lower when cell 5 = −1; therefore, the polarization of cell 5 is determined to be −1. The output value of the multiplexer is +1, which is the opposite of the value of cell 5. Therefore, it can be confirmed that the input value operates normally. In the same way, simulation output values for other input values can be verified to operate normally using the physical proof shown above.

5. Conclusions

Among the previously proposed RAM cells, circuits that do not separate the stored value from the output value cannot be designed to be extended to NxN RAM because the stored information is initialized based on the value of the selection signal. In addition, the circuits they separate are inefficient and the output signal is unstable, thus some circuits do not work properly. Therefore, an optimized QCA RAM cell was proposed using the 2-to−1 multiplexer and RAM cell logic diagram proposed in this study. Through the proposed logic diagram, circuit optimization and stable signal transmission were successful, and comparing performance with existing circuits confirmed that it showed excellent performance in terms of delay time and area. In addition, energy dissipation comparisons proved that the proposed circuit has good energy efficiency, and normal operation was verified using a simulation tool. The reliability of the operation of the proposed circuit was also mathematically proved using physical proof. We have shown that real clocking control is possible by adjusting the simple QCA wiring clocking.

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