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Investigations into Higher-Frequency Hysteresis Current Controller for Supraharmonic Hybrid Active Filters

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Abstract: Hysteresis current controllers (HCCs) are extensively used in low-frequency power inverters and active power filters. Very little is known about their strengths and weaknesses when applied at supraharmonic frequencies. The major concern regarding the use of HCCs is their variable and uncontrollable switching frequencies. This results in difficulties in filter design, high switching losses, and the possibility of resonance conditions with power system elements. In this article, investigations are conducted on the application of HCCs in a hybrid filter for a 6 kHz matrix converter (MC)-coupled supraharmonic load. The effects of the MC-coupled load and VSC switches on the HCC's switching frequency are analyzed. A novel mathematical model for obtaining a fixed-frequency HCC is presented. The model is verified in open- and closed-loop HCC control configurations for a three-phase hybrid active power filter (HAPF). Fast Fourier transform (FFT) analysis of the supply current after the implementation of the novel HCC-HAPF showed 2.31% of the 50 Hz fundamental. The analysis is verified in a MATLAB/Simulink environment.

Keywords: hybrid active filter; hysteresis current controller; matrix converter; supraharmonic frequency

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1. Introduction

In recent years, the use of power electronic converters as interfaces for domestic and industrial loads has increased exponentially. Wind power applications, solar photovoltaic generators, electric vehicles, and battery storage chargers are the most common applications of power electronic converters [1]. These self-commutating converters, due to their numerous switching states, have switching frequencies in the kilohertz (kHz) band range and produce switching harmonic frequencies above 2 kHz [2]. Unfortunately, very little research has been conducted, and there are few regulations on such frequency ranges. Supraharmonic frequency is a term describing harmonic frequencies between 2 and 150 kHz and was introduced by the IEEE at their PES conference in 2013 [3]. The presence of supraharmonic frequencies poses threats to power electronic converters [4].

Supraharmonic interference received less attention due to the limited use of fast switching converters in the past [5]. But with the recent high demand for electric vehicles, wireless and fast battery charging stations, variable-speed drives, and electronically controlled lamps [6], there is a need to increase research in this area. Table 1 shows the operating frequency ranges of electronic converters used for selected domestic and industrial loads.

Active power filters are preferred for harmonic compensation due to their compatibility and smaller weight and size [7–10]. Traditional passive filters may not be practical in applications where size and weight are of much concern. The IEEE Std. 519-2022 recommends an acceptable 5% THDi harmonic current distortion. Hence, the average attenuation of a passive filter should be 26 dB during maximum currents and 32 dB during minimum currents. Passive filter components based on the above are too large and bulky in applications where size and weight are of much concern. The minimum weight of a similar

filter with 107 amperes of nominal choke current from the Schneider electronics 'Altivar61' line chokes catalogue for a three-phase source at 380 to 480 V and 50/60 Hz is 16 kg [11], which is too large for applications in aircraft, ships, electric vehicles, etc. Active harmonic filters on their own may not be an economically feasible option for higher-frequency compensation. Hybrid harmonic filters are the most viable option for supraharmonic-frequency compensation [12]. Using hybrid harmonic compensation, the parallel combination of a passive L-C filter and a shunt active power harmonic filter is proposed. With this, the passive filter is designed to attenuate 60% of the supraharmonic frequencies.

Table 1. Operating frequency ranges of electronic converters for selected loads.

Load	Switching Frequency (kHz)
Electric vehicle chargers	15–100
Solar PV inverters	4–20
Power communication lines (PCLs)	9–95
Communication notch oscillations	Up to 10
Industrial size converters	9–150
Street lighting systems	Up to 20
Household electronic devices (LEDs and CFLs)	2–150

The HCC method, due to the stability and faster dynamic responses of HCCs during transient behaviors, is the most preferred pulse width modulation (PWM) control technique for active power filters. However, the variable nature of the HCC switching frequency increases switching oscillations, electromagnetic interference (EMI), and difficulty in active filter design. Most research works are on fixed-frequency HCCs for low-frequency applications [13–16]. The principle of fixed-frequency HCCs is used to define a variable hysteresis band for each leg of the VSC, thereby maintaining a nearly constant switching frequency. The behaviors of HCCs in supraharmonic frequency ranges are unknown, and not enough research has been conducted on this topic. This leaves a knowledge gap related to the feasibility of HCCs for higher-switching-frequency converters as well as the switches appropriate for its realization.

This article bridges this knowledge gap and presents a novel mathematical expression for estimating the maximum switching frequency of an HCC for hybrid active power filters (HCC-HAPF). This article presents an improved model for implementing fixed-frequency HCCs and explores its realization using metal–oxide–semiconductor field-effect transistors (MOSFETs). The dV/dt and dI/dt are analyzed, as they are the major causes of oscillations, overshoots, and EMI during higher-frequency switching.

The objectives and contributions of this study are as follows:

1. To investigate the nature and propagation of the supraharmonic frequencies produced by a 50 kW, 6 kHz MC-interfaced load.
2. To obtain a novel equation for estimating a fixed-frequency hysteresis current controller in higher-frequency applications.
3. To achieve supraharmonic frequency compensation within the recommended standards of IEEE Std. 519-2022 [17] using the HCC-HAPF.

The remainder of this paper is arranged as follows: Section 2 describes reference current generation using the P-Q technique. Section 3 reviews the HCC and derives the novel mathematical expression for the hysteresis current controller. The effects of the load and VSC switches on the switching frequency are also analyzed. The novel expression is tested with a hybrid active filter topology for a 6 kHz MC application, and Section 4 summarizes the simulation results. Section 5 discusses and compares the obtained results. Section 6 concludes the study with future research directions.

2. The MC and Supraharmonics

Several research works [1,3,6,18] have identified the sources of these supraharmonics as power electronic converters with higher switching frequencies. The authors in [1]

presented supraharmonics propagation from electric vehicles with respect to small and low-voltage grids. They concluded that supraharmonic frequencies may result in the tripping of residual current devices and "frequency beating". The authors in [3,6] seek to establish standardization and measurements for supraharmonic applications. They concluded that the emissions from supraharmonic frequencies reduce the efficiency and life expectancy of electrical equipment.

Power electronic converters are also the primary victim of supraharmonic frequencies, as their dynamic performance are crippled, as the authors in [4,5,19,20] explored. The authors in [4,5] explored the power electronic converters and supraharmonics and [17] confirmed the effect of higher harmonic frequencies as the reduction in lifespan of power system devices. The authors in [8] successfully modeled the emissions from supraharmonic devices from the parallel operation of two converters and confirmed that it can be predicted by linear models.

The advantages of the use of MCs supersedes that of the traditional back-to-back converters [21,22]. Paramount is its bi-directional operation and the absence of energy storage elements. Irrespectively, the MC's voltage transfer ratio of 0.867 and supraharmonic input and output frequencies discourages its use. The authors in [23–25] explored power quality issues with the matrix converter and proposed possible active power filters (APF) as a solution. The large switching states of the MC produces discontinuous input currents and voltage spikes in the supply grid. Figure 1 shows the power system connected to an MC interfaced load with the hybrid active power filter between the supply and the load. From Figure 1, the input current is composed of active and reactive powers and the harmonics, as shown in Equation (2). These supraharmonics are propagated into the power system due to the discontinuous currents of the MC [26–29]. Table 2 shows the reviewed literature on the topic.

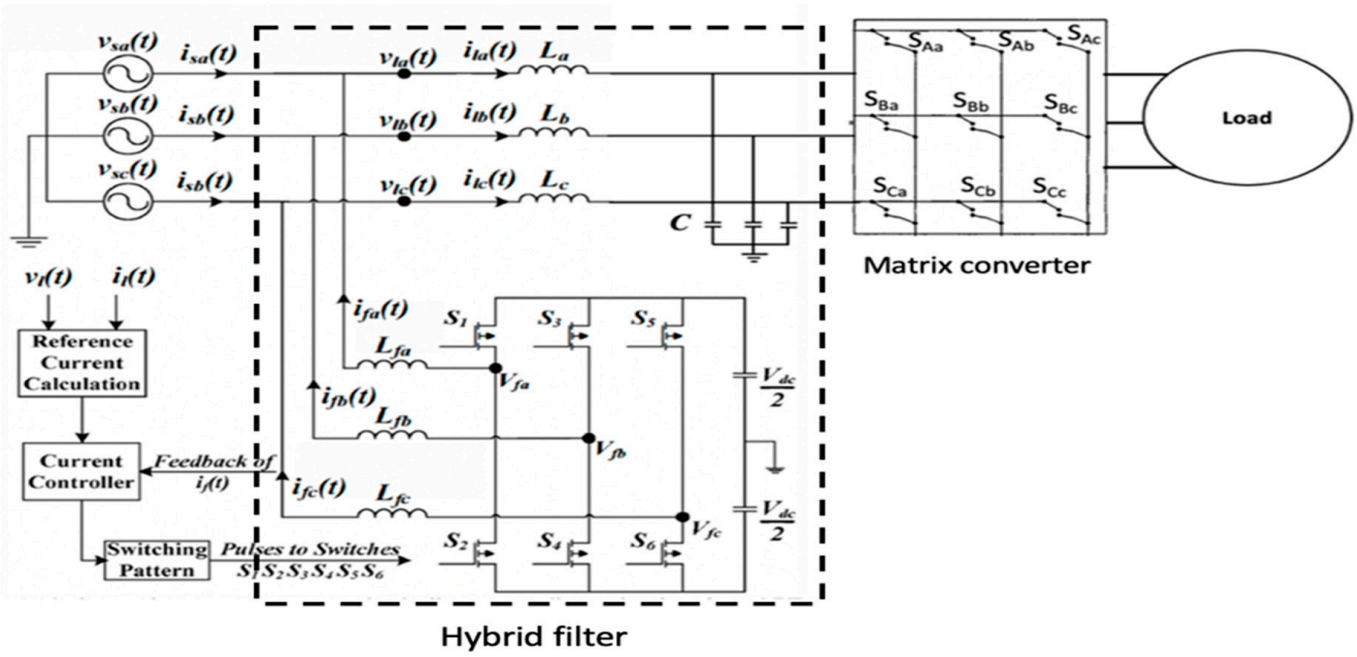


Figure 1. Power system with MC interfaced load and hybrid active power filter in between.

Table 2. Similar works review.

References	Method	Conclusion
[1]	Supraharmonics in electric vehicles	Frequency beating, tripping of residual devices
[3,6,17]	Measurement and standardizations	Reduces life expectancy of electrical equipment
[16]	Supraharmonics in multiple VSCs	Supraharmonics are distributed integer multiple of the switching frequency of VSC
[4,5]	Supraharmonics in power electronic loads and mode of compensation	Power converters are sources of supraharmonics. Zone-phase compensation
[18]	Modelling of EMI from supraharmonic devices	It is possible to model the effects of supraharmonics
[21–23]	Power quality issues with MC and possible solution with active power filters (APF)	Lyapunov control strategy, APF, Shunt and series power filters
[24–27,29]	Supraharmonics in MC	Large switching states of MC causes supraharmonics

If the supply voltage and current are considered as Equation (1) and Equation (2), respectively, then the instantaneous power at the input side of the MC can be expressed as Equation (3). Passive filters are the most recommended solution for MC harmonic attenuation. But resent load dynamics has made passive filter solutions not a feasible option due to compact size and light weight converters being the most required attributes in today's load applications. Active harmonic power filters are economically not recommended for higher frequency compensation. With this, researchers are now focusing on hybrid active power filter solutions consisting of passive R-L-C and shunt active power filters.

$$v_{s(t)} = V_m \sin \omega t \tag{1}$$

$$i_S(t) = i_L(t) = i_0 + i_1 \sin(\omega t + \theta_1) + \sum_{n=5,7.9.11...}^{\infty} i_n \sin(n\omega t + \theta_n) \tag{2}$$

$$P_{L(t)} = i_1 V_m sin^2 \omega t cos\theta_1 + i_1 V_m sin\omega t cos\omega t sin\theta_1 + \sum_{n=3,5,7...}^{\infty} V_m sin\omega t i_n \sin(\omega nt + \theta_n) \tag{3}$$

where

$v_{s(t)}$: supply voltage;
V_m: supply voltage amplitude;
$i_S(t)$: supply current;
$i_L(t)$: load current;
i_0: DC load current component;
i_1: first harmonic component;
ω: supply frequency (50/60) Hz;
n: harmonic number;
$P_{L(t)}$: load power.

Active power filter design always begins with the extraction of the reference current from the load [30–32]. The instantaneous active and reactive power theory (P-Q theory) proposed by the authors in [33] is the most used technique for reference current generation. The principle is to extract the compensational error current from three-phase voltage and current measurements expressed in their alpha/beta domain using a transformation matrix, T, as seen in Equation (4). Ignoring the zero sequence currents, the instantaneous active, p(t), and reactive q(t), powers can be computed with Equation (5). Finally, decomposing p(t) and q(t) into direct and oscillatory components, the reference currents can be calculated from the oscillatory component of the active power, $\widetilde{P}$, and the total reactive power, q, for a partial compensation. The compensational current extracted in Equation (7) is of same amplitude but 180° out of phase with the harmonic load current [34].

$$T = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{4}$$

$$\begin{bmatrix} P(t) \\ q(t) \end{bmatrix} = \begin{bmatrix} v_\alpha(t) & v_\beta(t) \\ -v_\beta(t) & v_\alpha(t) \end{bmatrix} \begin{bmatrix} i^*_{c\alpha}(t) \\ i^*_{c\beta}(t) \end{bmatrix} \tag{5}$$

$$\begin{bmatrix} i^*_{c\alpha}(t) \\ i^*_{c\beta}(t) \end{bmatrix} = \begin{bmatrix} v_\alpha(t) & v_\beta(t) \\ -v_\beta(t) & v_\alpha(t) \end{bmatrix} \begin{bmatrix} -\widetilde{P}(t) \\ -q(t) \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} i^*_{ca} \\ i^*_{cb} \\ i^*_{cc} \end{bmatrix} = T^{-1} \begin{bmatrix} i^*_{c\alpha}(t) \\ i^*_{c\beta}(t) \end{bmatrix} \tag{7}$$

The obtained reference currents are compared with the inverter current, in a closed-loop system, under an appropriate control mechanism to produce gating signals for the VSC. Triangular carrier pulse width modulated (PWM) control and the hysteresis current control strategies are the most applied control techniques for active filters [31]. HCCs are most applied due to their stability, easy implementation, and faster dynamic responses. Irrespectively, HCC controllers are most applied in low-frequency applications, and not very much is known about their responses in higher frequency applications. HCCs are known for their variable switching frequencies, and several research works on obtaining constant switching frequencies have been presented [35–38].

3. The Hysteresis Current Controller

The implementation of the traditional constant bandwidth variable frequency HCC (CBVF-HCC) involves comparing the reference current to the inverter current within the hysteresis band, as seen in Figure 2. The aim is to obtain an error current, $e_r(t)$, as minimum as possible within a hysteresis bandwidth and generate an appropriate gating signal.

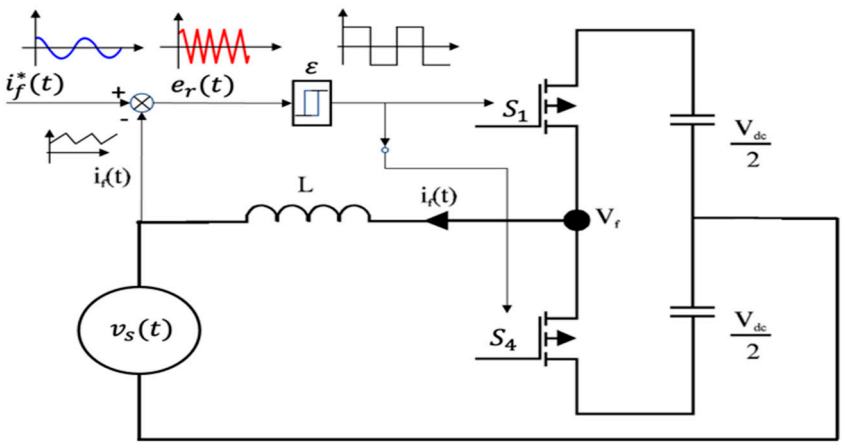


Figure 2. Per phase equivalent of Figure 1 using CBVF−HCC. $v_{s(t)}$: supply voltage; $i_f(t)$: inverter current; $i^*_f(t)$: reference current; ε: hysteresis band current; $e_r(t)$: error current; S_1, S_4 power inverter switches.

Considering a sinusoidal supply voltage with no harmonics, the inverter voltage, V_f, is dependent on the appropriate switching scheme of the inverter switches as well as the modulation index. Under linear modulation mode and considering the current direction in Figure 2, V_f can be generalized as:

$$V_f = (S_1 - S_4) \times \frac{V_{dc}}{2} \tag{8}$$

For Vc = $\frac{V_{dc}}{2}$

$$V_f = \begin{cases} V_C \; for \; S_1 = 1 \\ -V_C \; for \; S_4 = 1 \end{cases} \tag{9}$$

Again, from Figure 2, the following expressions can be obtained for the rate of change in the inverter current and that of the reference current, respectively.

$$\frac{di_f(t)}{dt} = \frac{1}{L}\Big(v_f - v_s(t)\Big) \tag{10}$$

$$\frac{di_f^*(t)}{dt} = \frac{1}{L}\Big(v_f^* - v_s(t)\Big) \tag{11}$$

The error current, $e_r(t)$, is calculated for each phase of the VSC and obtained from Figure 3, where the inverter current tracks the reference current, within the hysteresis bandwidth, to generate gating pulses for the VSC.

$$e_r(t) = \begin{bmatrix} e_{ra} \\ e_{rb} \\ e_{rc} \end{bmatrix} = \begin{bmatrix} i_{fa}^* \\ i_{fb}^* \\ i_{fc}^* \end{bmatrix} - \begin{bmatrix} i_{fa} \\ i_{fb} \\ i_{fc} \end{bmatrix} \tag{12}$$

$$\frac{\Delta e_r}{\Delta t} = \frac{2\varepsilon}{t_1} = \frac{di_f^*(t)}{dt} - \frac{di_f(t)}{dt} \tag{13}$$

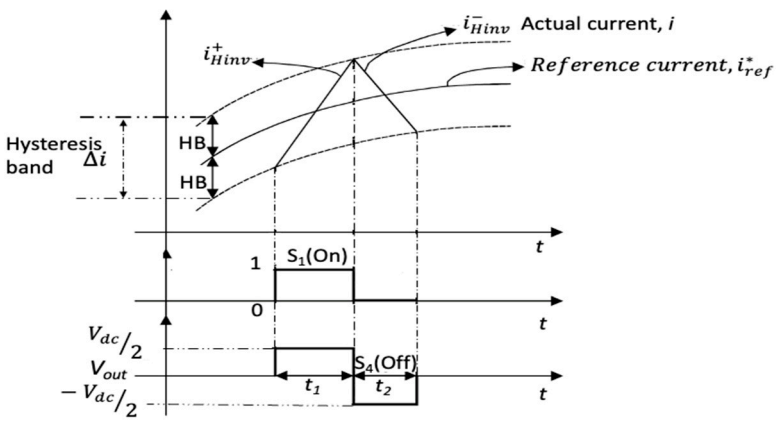


Figure 3. Hysteresis current control bandwidth gate pulses. i^*_{ref}: Reference current; i^+_{Hinv}: Rising inverter current; i^-_{Hinv}: Falling inverter current; Δi/HB: Hysteresis current bandwidth; S_1/S_4: VSC switch 1 and 4; V_{out}: VSC output voltage; V_{dc}: VSC Capacitor voltage.

From Figure 3, the rate of change in the error current can be deduced, for the rising and falling periods, as Equation (14) and Equation (15), respectively. From these, a relation between the hysteresis bandwidth and the switching frequency can be obtained by substituting Equations (14) and (15) into Equation (13).

$$\frac{di_f^+(t)}{dt} = \frac{1}{L}\Big(v_f - v_s(t)\Big) \tag{14}$$

$$\frac{di_f^-(t)}{dt} = -\frac{1}{L}\Big(v_f + v_s(t)\Big) \tag{15}$$

$$\begin{cases} 2\varepsilon = \frac{di_f^*(t)}{dt} \times t_1 - \frac{di_f^+(t)}{dt} \times t_1 \\ -2\varepsilon = \frac{di_f^*(t)}{dt} \times t_2 - \frac{di_f^-(t)}{dt} \times t_2 \end{cases} \tag{16}$$

Equation (16) is the traditional relation for obtaining the hysteresis current error, ε. From the expression, a fixed band is obtained, but variable and uncontrollable switching frequencies will be observed. This results in several challenges in using the HCC controller including difficulties in harmonic filter design due to the uncontrollable nature of the

switching frequency. This article resolves this issue by presenting a novel equation that expresses the maximum instantaneous switching frequency with respect to the error band current.

The basic condition for the successful implementation of this controller is for the rate of change in the reference current to be smaller than that of the inverter current shown in Equation (16). Equations (17)–(21) calculate the hysteresis current bandwidth as well as present an expression for the instantaneous switching frequency of the VCS for a finite time period, T.

$$\frac{di_f^+}{dt} > \frac{di_f^*}{dt} \tag{17}$$

$$t_1 = 2\varepsilon \Big/ \left(\frac{di_f^+}{dt} - \frac{di_f^*}{dt} \right) \tag{18}$$

$$t_2 = 2\varepsilon \Big/ \left(\frac{di_f^*}{dt} - \frac{di_f^-}{dt} \right) \tag{19}$$

If the total period $T = t_1 + t_2$, then the frequency can be obtained as Equation (20), and eventually Equation (21) gives the novel expression. The frequency is to be obtained instantaneously for each sampling time and for each phase.

$$f_{inst} = \frac{1}{T} = \frac{1}{t_1 + t_2} \tag{20}$$

$$f_{inst} = \frac{1}{2\varepsilon} \left(\frac{1}{\frac{1}{\frac{di_f^+}{dt} - \frac{di_f^*}{dt}} + \frac{1}{\frac{di_f^*}{dt} - \frac{di_f^-}{dt}}} \right) \tag{21}$$

where

$i_f^+(t)$: rising current;
$i_f^-(t)$: falling current;
i_f^*: reference current;
f_{inst}: inverter switching frequency;
$\frac{di_f^+}{dt}$ and $\frac{di_f^-}{dt}$: the rising and falling rate of change in inverter current;
$\frac{di_f^*}{dt}$: rate of change in reference current.

3.1. Validation of the Novel Expression

The obtained expression will work for all load types, constant and varying, provided the principles of hybrid filter designs are followed. Irrespectively, the expression was simulated with three reference signals: sinusoidal, square wave and the trapezoidal reference signals considering a supraharmonic frequencies source from an MC interfaced constant load application, although only the results of the trapezoidal reference signal are presented in this article.

Hybrid active filter topology was selected for the compensation due the fact that passive L-C filter solutions will be too bulky and heavy to be implemented in applications where size and weight are important, which is the major target application considered in this article. Active filters, on the other hand, will be too expensive considering the frequency range. The HAPF consists of a passive filter section and an active power filter section with its controls. The passive side of the HAPF was to meet the following requirements.

- Filter input impedance at grid frequency must be less than or equal to the grid impedance and higher at harmonic frequencies.
- Filter current transfer ratio must be low at grid frequency.

The above rules governed the sizing of the passive filter components and resulted in an RLC passive filter selection. The capacitor value was designed based on the reactive power requirements at grid frequency, and the inductor selection was based on the consideration that the voltage drop in the RLC filter must be 5% of the grid voltage. There is a maximum passive filter attenuation of 60% to maintain a smaller size passive filter element. The following equations were used to obtain the passive filter parameters.

$$|H(j\omega)| = \left| \frac{1}{1 - \left(\frac{\omega_{SW}}{\omega_C}\right)^2} \right| \tag{22}$$

$$C_F = \frac{K_C S_{MC}}{3V_s^2 \omega_g} \tag{23}$$

The filter inductance was calculated after obtaining C_F and the cutoff frequency, ω_C, using the following equation.

$$\omega_C = \frac{1}{\sqrt{L_F \times C_F}} \tag{24}$$

For the active side of the HAPF, the main components are the DC capacitance voltage and capacitance value and the coupling inductance value. The reactive power produced by the inverter can compensate the reactive power in the supply when the VSC output voltage is higher than the supply voltage; thus, $V_{inv} > V_s$ under linear modulation mode. The DC capacitance voltage, V_{dc} was obtained as Equation (26) by:

$$m_a = \frac{2\sqrt{2}V_{inv}}{V_{dc}} \tag{25}$$

If $m_a = 1$, then

$$V_{dc} = 2\sqrt{2}V_{inv} = 2\left(\sqrt{2}/\sqrt{3}\right)Vs \tag{26}$$

The selection of the DC capacitance value was based on the instantaneous power exchange between the inverter and the grid during transients. The peak-to-peak ripple voltage of the inverter was assumed to be 15% of the DC bus voltage. Hence, the lost energy in the inverter is compensated for as shown in Equation (27):

$$E = \frac{1}{2}C_{dc}\left(V_1^2 - V_2^2\right) = P \times T = K3V_S I_f aT \tag{27}$$

where $V_2 = V_1 - \Delta V_{ripp}$ and ΔV_{ripp} is the peak-to-peak ripple voltage. V_1 is the DC voltage. If the power rating of the inverter is P, then the energy stored in the capacitor for a period T can be estimated.

The selection of the coupling inductor was based on the peak-to-peak ripple current, i_{ripp}, which was calculated considering the harmonic currents to be 10% of the input current to the MC.

$$L \geq \frac{\frac{2}{3}V_{dc} - V_s \sin(\omega t)}{max\left|\frac{di_L}{dt}\right|} \tag{28}$$

Equation (21) expresses the VSC switching frequency in terms of the hysteresis band current, the rate of change in the both the reference current and that of the inverter current. From Equation (21), the maximum allowable HCC can be measured, and a near constant switching frequency can be obtained under supraharmonic applications. The obtained expression was verified in an open-loop control simulation using the trapezoidal reference signal.

The trapezoidal reference signal was considered as it closely represented the speed of change in the MC harmonic currents. Figure 4 shows the simulation for the trapezoidal reference signal. For a harmonic frequency of 6 kHz, the minimum coupling inductance size

required for the shunt active filter is calculated from equations based on [39] considering a 1 kW 6 kHz converter coupled to a 400 V 50 Hz supply.

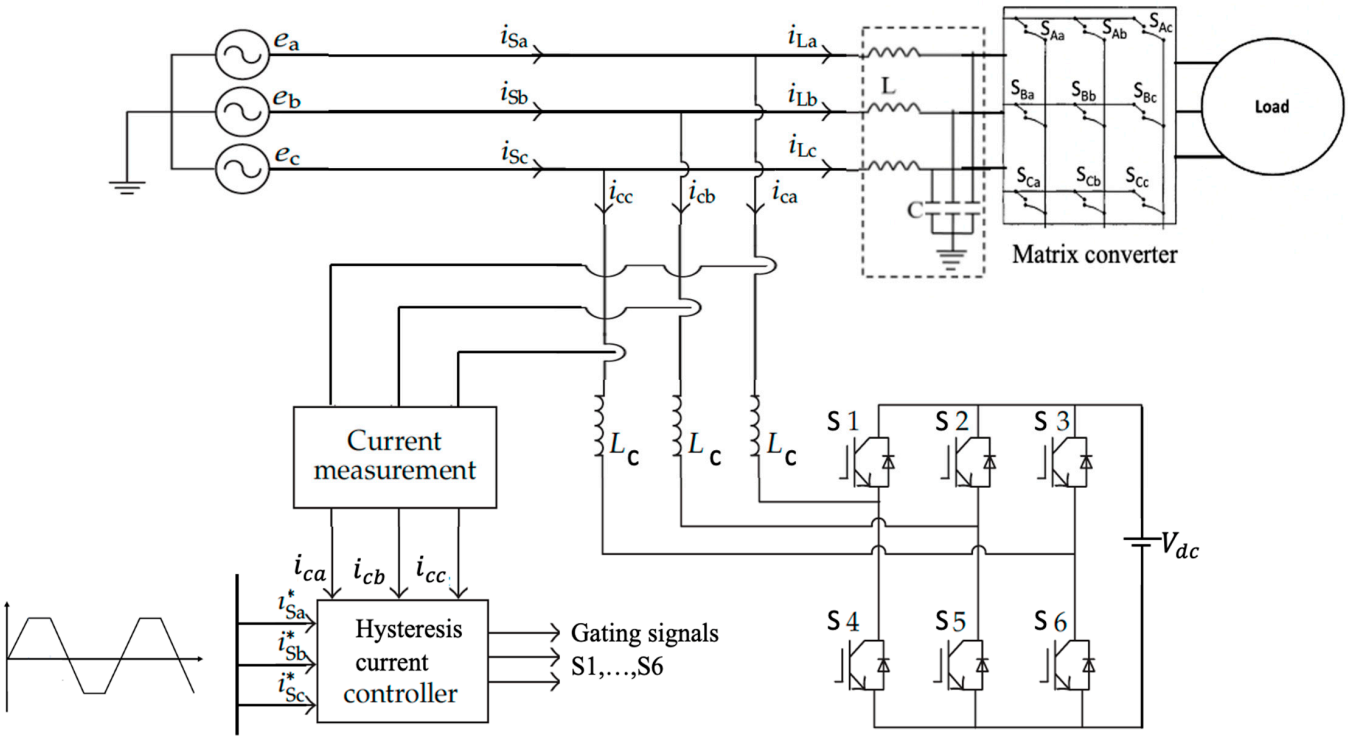


Figure 4. Open-loop schematic diagram of HCC-HAPF for MC input current harmonics elimination. Source: [39].

The maximum current change rate of the VSC and the minimum coupling inductance, L, can be calculated based on Figure 5 for a 6 kHz harmonic frequency at t = $90/\omega$ as Equation (29) using Equation (28).

$$\begin{aligned} max\left|\frac{di_L}{dt}\right| &= \frac{1.44}{0.1\times1.67\times10^{-4}} = 86.23\times10^3 \text{ A/s} \\ L \geq \frac{\frac{2}{3}V_{dc}-V_s\sin(\omega t)}{max\left|\frac{di_L}{dt}\right|} &= \frac{466.667-V_S}{86.23\times10^3} = 0.77 \text{ mH} \end{aligned} \tag{29}$$

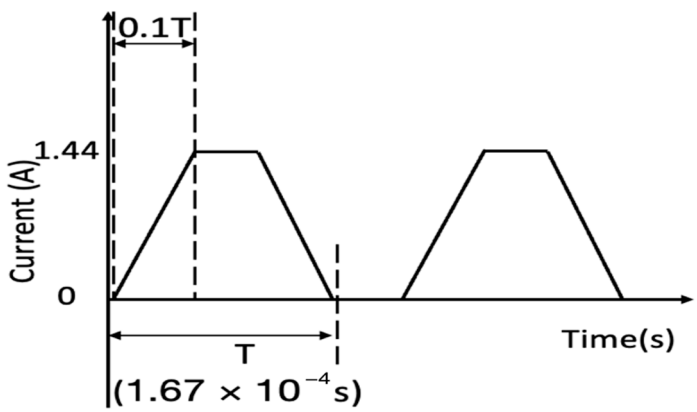


Figure 5. Maximum rate of change in the harmonic load current. Source: [37]. T: total period in seconds; I_f: current in amperes.

With Equation (28), the rate of change in the VSC output current can be calculated using Equations (14) and (15) for the rising and falling currents and the RMS value of the supply voltage.

$$\frac{di_f^+(t)}{dt} = 3.89 \times 10^5 \mathrm{A/s} \qquad \frac{di_f^-(t)}{dt} = -1.43 \times 10^6 \ \mathrm{A/s} \tag{30}$$

For a trapezoidal wave reference current of Figure 6, the rate of change in the reference current, considering the first four terms of a trapezoidal wave equation, can be expressed as Equation (31). The rate of change in the converter current at harmonic frequency of 6 kHz is calculated as Equation (32).

$$\begin{gathered} i_f^* = \frac{8\sqrt{2}}{\pi^2} I_f^* (\sin(\omega t) + \frac{\sin(3\omega t)}{9} - \frac{\sin(5\omega t)}{25} - \frac{\sin(7\omega t)}{49}) \\ \frac{di_f^*}{dt} = \frac{8\sqrt{2}}{\pi^2} I_f^* \omega \left(1 + \frac{1}{3} - \frac{1}{5} - \frac{1}{7}\right) \end{gathered} \tag{31}$$

$$\frac{di_f^*}{dt} = 6.16 \times 10^4 \ \mathrm{A/s} \tag{32}$$

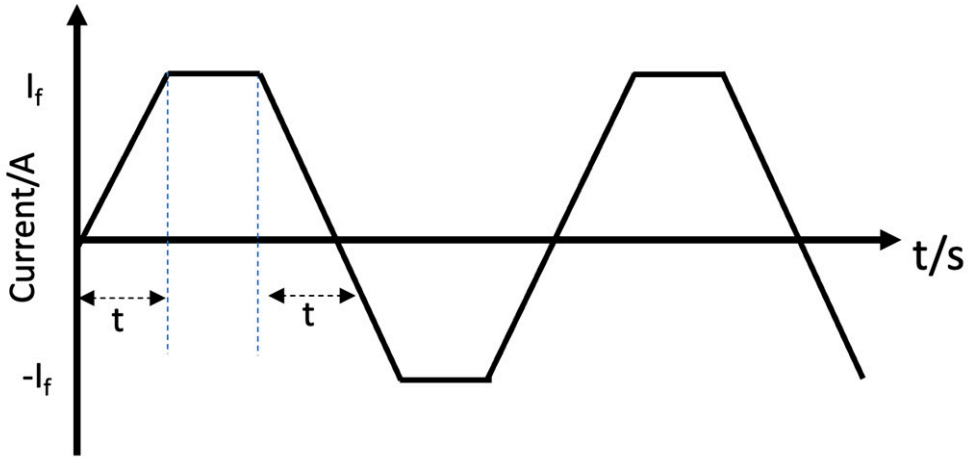
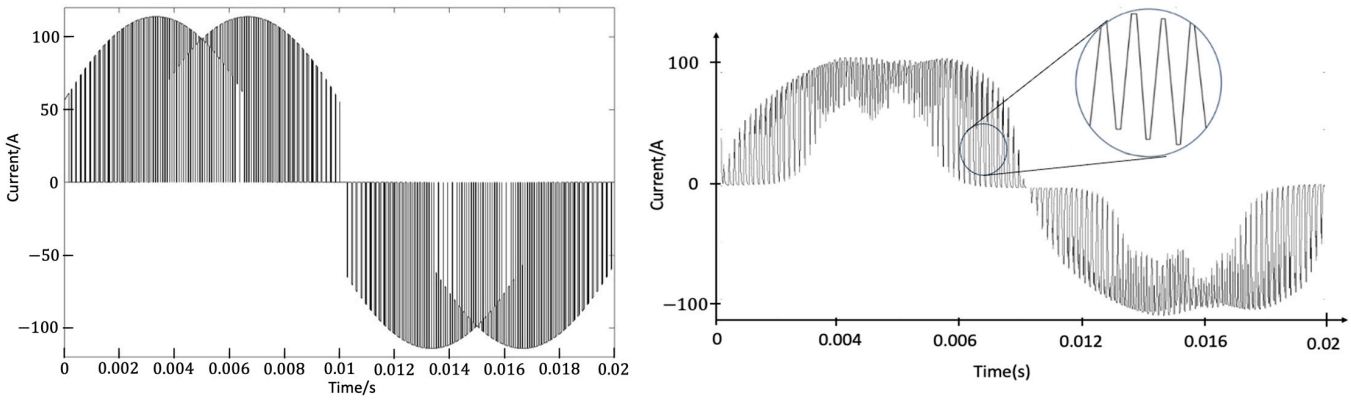


Figure 6. Trapezoidal wave shape reference current. t: rising and falling time in seconds; I_f: current in amperes.

From Equations (30) and (31), the maximum switching frequency for a trapezoidal wave shape reference current can then be obtained as Equation (33).

$$\begin{gathered} f_{inst} = \frac{1}{2\varepsilon}\left(\frac{1}{\frac{1}{3.89\times10^5 - 6.16\times10^4} + \frac{1}{6.16\times10^4 + 1.43\times10^6}}\right) \\ f_{inst} = \frac{131.90}{\varepsilon}\mathrm{kHz} \end{gathered} \tag{33}$$

The trapezoidal reference signal by nature closely represents the matrix converter load current shape as seen in Figure 7 and by the above deductions; an instantaneous switching frequency, based on the parameters used, is 131.9 kHz considering a hysteresis band of 1 A.



(**a**) (**b**)

Figure 7. MC output current shape at 1 kHz switching frequency: (**a**) unfiltered; (**b**) with 60% passive L-C filter attenuation.

3.2. Effects of the Power Rating of the MC on Inverter-Switching Frequency

The effects of the MC power rating on the maximum instantaneous switching frequency of the VSC was analyzed with MC ratings of 10 kW, 50 kW and 100 kW. Each had a 6 kHz frequency on the trapezoidal signal, as it closely represented the MC current shape. For the above converter rating, the appropriate MC input current, I_f, was obtained with Equation (34). For the MC rated capacity, $S_{MC,}$ of 10 kW, the MC input current and the maximum rate of change in the reference current can be obtained from Equations (34) and (35).

$$I_f = \frac{S_{MC}}{400\sqrt{3}} = 14.43 \text{ A} \tag{34}$$

$$\frac{di_f^*}{dt} = \frac{8\sqrt{2}}{\pi^2} I_f^* \omega \left(1 + \frac{1}{3} - \frac{1}{5}\right) = 7.06 \times 10^5 \text{ A/s} \tag{35}$$

The instantaneous frequency of the VSC can be calculated from Equation (35), and the rate of change in the rising and falling inverter current of Equations (30) and (31) is shown as Equation (36).

$$\begin{gathered} \frac{di_f^+(t)}{dt} = \frac{(700-400)}{0.077mH} = 3.88 \times 10^6 \text{ A/s} \\ \frac{di_f^-(t)}{dt} = -\frac{(700+400)}{0.77mH} = -1.47 \times 10^7 \text{ A/s} \\ f_{inst} = \frac{1}{2\varepsilon}\left(\frac{1}{\frac{1}{3.89\times10^6 - 7.06\times10^5} + \frac{1}{7.06\times10^5 + 1.47\times10^7}}\right) \\ f_{inst} = \frac{1.319}{\varepsilon} MHz \end{gathered} \tag{36}$$

Table 3 summarizes the deduction above with a different matrix converter power, S_{MC} at 6 kHz, which is expressed as a ratio of the hysteresis band current. From the table, it can be concluded that the VSC switching frequency is directly proportional to the power of the MC. Hence, an increment in the MC power increases the VSC switching frequency, which proves the theory.

Table 3. Effects of changing MC power, S_{MC}, on the converter switching frequency.

S_{MC}/kW/6 kHz	1	10	50	100
$\frac{di_f^*(t)}{dt}$, A/s	7.06×10^4	7.06×10^5	3.53×10^6	7.06×10^6
$\frac{di_f^+(t)}{dt}$, A/s	3.89×10^5	3.89×10^6	1.94×10^7	3.89×10^7
$\frac{di_f^-(t)}{dt}$, A/s	-1.47×10^6	-1.47×10^7	-7.47×10^6	-14.29×10^8
f_{inst}, MHz	$\frac{0.1319}{\varepsilon}$	$\frac{1.319}{\varepsilon}$	$\frac{6.72}{\varepsilon}$	$\frac{13.19}{\varepsilon}$

Finally, the effects of the hysteresis current error, ε, and the maximum instantaneous switching frequency are analyzed. From Equation (21), the relation between ε and f_{inst} is inversely proportional. The error current was toggled between 0.2 A, 0.5 A, 0.7 A and 1 A at 10 kW MC rated power. Table 4 shows the obtained results.

Table 4. Relationship between hysteresis error current and the VSC switching frequency at S_{MC} (10 kW).

S_{MC}/kW/6 kHz	10			
ε/A	0.2	0.5	0.7	1
f_{inst}/MHz	6.72	2.68	1.92	1.319

4. Simulation Results and Analysis

A simulation of the theory was first conducted in a three-phase, open-loop configuration for the trapezoidal reference signal. A closed-loop simulation of a hybrid active filter for an MC interfaced three-phase load was analyzed. Figure 8 depicts a three-phase voltage source supplying a three-phase MC interfaced load. The HAPF consisted of the parallel combination of a shunt active power filter (SAPF) and a passive L-C filter. Table 5 shows the parameters selected for the simulations of the MC-HAPF in MATLAB/Simulink environment based on equations from an earlier work by the same authors [39]. Irrespectively, non-ideal conditions were included in the simulation to approximate practical implementation for future work.

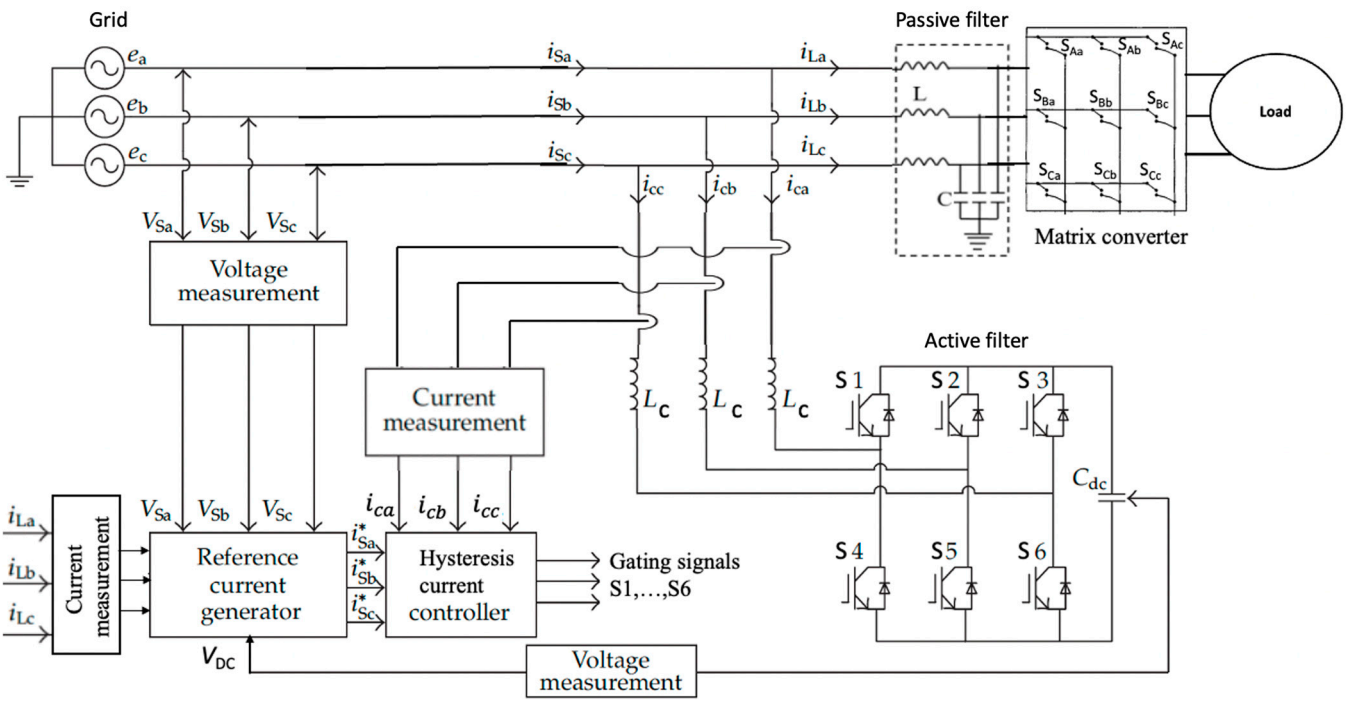


Figure 8. Schematic diagram of closed-loop active filter schematic diagram. Source: [39].

The open-loop setup consisted of a three-phase supply and the MC coupled load as seen in Figure 4 above. The open-loop reference trapezoidal signal was compared to the VSC output current signal in the presence of the hysteresis band. The trapezoidal signal was selected because its rate of change in current closely mimics that of the matrix converters. Table 6 shows the parameters for the trapezoidal reference simulation. The effects of the reference signal's frequency and hysteresis current bandwidth on the switching frequency of the VSC were tabulated and analyzed.

Table 5. Parameters selected for the open-loop configurations.

Parameter	Value
Supply voltage ($V_{L\text{-}L}$)	400 V, 50 Hz
MC rated power, S_{MC}	50 kW
MC switching frequency	6 kHz
LC low-pass filter values, C_{HF}	33 µF
Passive filter inductance, L_{HF}	1.87 mH
Damping resistance, R_{HF}	1 Ω
DC reference voltages	653 V_{min}, 700 V_{max}
DC capacitance	100 µF
Coupling inductance	115 µH

Table 6. Parameters selected for the closed-loop configurations.

Parameter	Value
Supply voltage ($V_{L\text{-}L}$)	400 V, 50 Hz
MC rated power, S_{MC}	50 kW
MC switching frequency	6 kHz
DC capacitor voltage	653 V_{min}, 700 V_{max}
Coupling inductance	115 µH
Reference signal frequency	50 Hz, 6 kHz

The simulation results for the open-loop and closed-loop configurations are shown below. The open-loop current shape and its maximum switching frequency as well as that for the closed-loop hysteresis-controlled MC setup are shown in Figures 9 and 10, respectively.

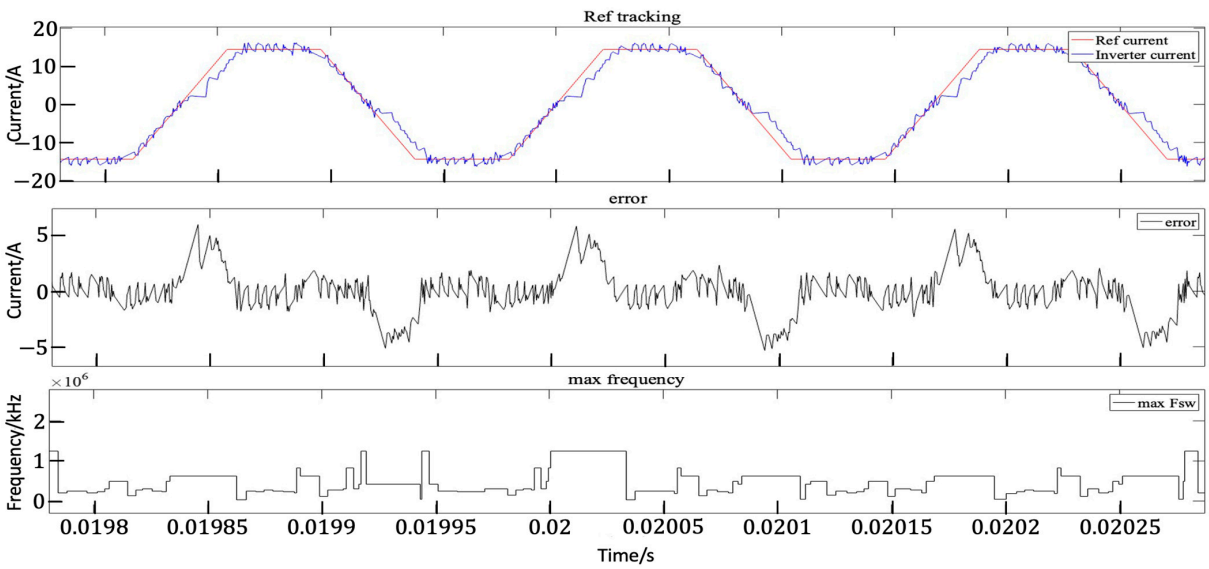


Figure 9. HCC simulation results for reference tracking, error current and maximum-switching frequency for trapezoidal wave reference signal.

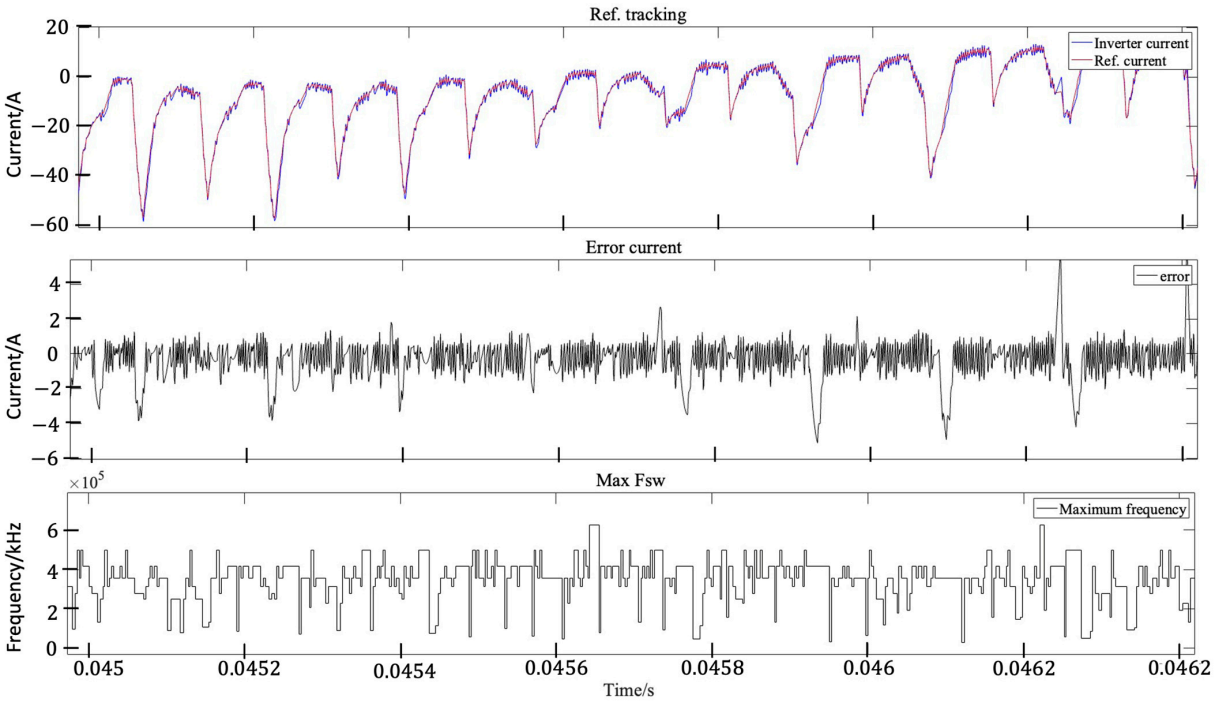


Figure 10. MC-HCC simulation results.

5. Discussion

From Table 7, it was observed that the simulation results followed the calculated results. Also, the results obtained from the MC-HAPF showed a 600 kHz maximum HAPF switching frequency for a 50 kW MC with 6 kHz switching frequency. The implementation of the above active part of the hybrid filter will involve the use of high-switching transistors. An example will be paralleling two IPW60R120P7 or R6030KNZ4 power MOSFETS for this purpose. Insulated gate bipolar transistors, IGBT's, are the most used transistors for inverter design for low frequencies (20 to 100) kHz and higher power applications, while metal–oxide–semiconductor field effect transistors, MOSFETs, are most suitable for low power and higher frequency (in MHz) range applications. However, there is the possibility of paralleling power MOSFETs for high power and frequency applications. From the above simulations, the following deductions were observed:

1. The converter rated power is directly proportional to the maximum attainable active filter hysteresis switching frequency.
2. Again, the maximum hysteresis switching frequency increases with the decrease in the hysteresis bandwidth current.
3. Reference signals with rate of change close to the supraharmonic signal frequency reduces the maximum hysteresis switching frequency of the VSC.

Table 7. Simulation results at hysteresis error current of 1 A.

	Novel Equation		Simulation Results	
MC power, S_{MC}	1 kW	10 kW	1 kW	10 kW
Current ref, I_f/A	1.44	14.44	1.44	14.4
Trapezoidal	131.9 kHz	1.31 MHz	140 kHz	1.3 MHz
MC-HAPF	136.74 kHz	712 kHz	130 kHz	610 kHz

With these observations, the following recommendations are suggested. For higher-frequency applications (6–10 kHz), power MOSFETs are recommended for hysteresis active filter-switching applications. However, to prevent switching loses, it is recommended to maintain a converter rated power below 50 kW. In applications with higher power (above 50 kW)

and relatively lower converter switching frequencies (below 6 kHz), IGBTs are recommended. IGBTs are not recommended for higher frequency applications but are most recommended for lower switching frequency converters. Also, for EMI and oscillations control, the gate resistor of MOSFETS, irrespective of the connected load, needs to be carefully selected as the size of the gate resistors mostly affects the switching frequency of the power MOSFET. Table 8 shows an IGBT and MOSFET data sheet from Infineon and the ST catalog. Further information about the MOSFET switching frequencies is provided in Appendix A.

Table 8. IGBT and MOSFET catalog datasheet.

Parameter	Transistor	
	IGBT (IKW30N60H3)	MOSFET (STW15NB50)
V_{CE} max	600 V	500 V
I (@ 25°) max	60 A	14.6 A
Turn-on delay time	21 ns	24 ns
Turn-off delay time	207 ns	15 ns
Rise time	33 ns	14 ns
Fall time	22 ns	25 ns
Switching frequency, min max	20–100 kHz	20 kHz–12 MHz

The harmonic distribution of the MC coupled load was analyzed, and Table 9 shows the MC input current harmonic distribution obtained after the simulation without any filter, passive or hybrid, at a sampling time of 4×10^{-7} with 50,000 samples per cycle. Without any filter, fast Fourier transform analysis (FFT) of the input current shows the total harmonic distortion of 57.49%, as seen in Figure 11a, with the dominant higher frequency harmonics occurring at the 155th harmonic level, which is close to the MC switching frequency. This further proved the influence of the switching frequency of the MC on the grid.

Table 9. Harmonic distribution of MC input current.

Frequency, Hz	Harmonic Number, h	Percentage of Fundamental %
0	DC	0.23
50	Fnd	100.00
250	5	8.85
350	7	3.28
450	9	0.81
550	11	1.26
650	13	1.66
7550	151	9.36
7600	152	5.59
7700	154	5.23
7750	155	19.21
7850	157	14.58
7900	158	7.91
8000	160	4.45
8500	161	13.06
THD%		57.49

The introduction of the passive L-C filter, as the interface to the MC, reduced the THD of the MC input current to 20.82% with the dominant h155 harmonic reducing to 10% of the fundamental. The passive filter could be designed to achieve more attenuation, but this will increase the size and weight of the filter as well as the reactive power burden and possibly lead to resonance conditions. Figure 11b shows the FFT analysis of the input current when a passive L-C filter was employed.

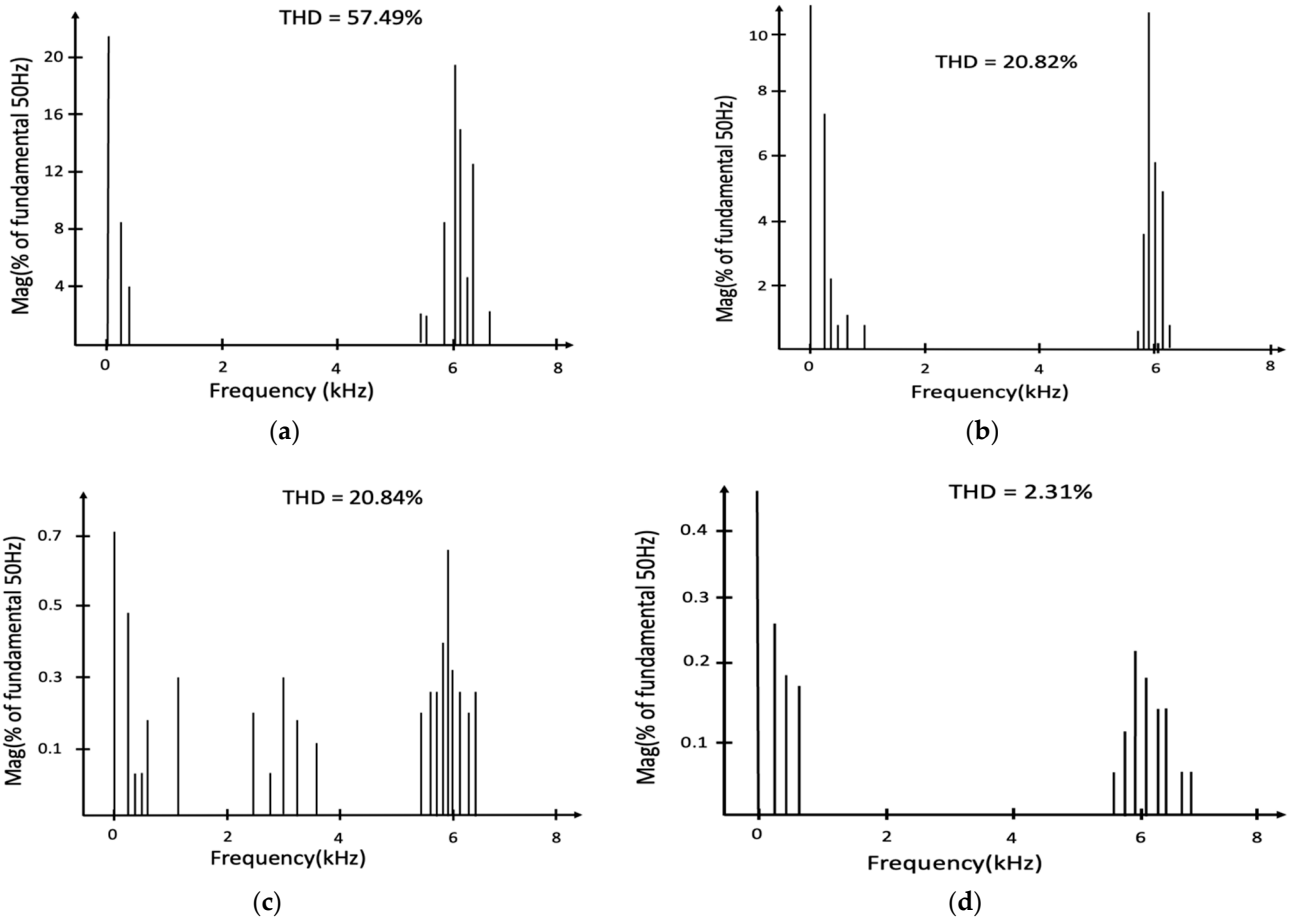


Figure 11. FFT analysis of MC input current (**a**) without filter, (**b**) passive L-C filter only, (**c**) with SAPF only, (**d**) with HAPF.

The implementation of the SAPF as the only filter interface between the MC input current and the supply grid resulted in a THD of 20.84% with h155 as 0.63% from FFT analysis. The SAPF could not achieve further compensation, as a large compensational current must be supplied by the SAPF. The hysteresis current controller maintained a constant switching frequency of 80 kHz for the inverter gating pulses. Figure 11c shows the THD of the MC input current in the FFT window.

The introduction of the HAPF resulted in the overall increase in the RMS value of the fundamental current to 91.8 A. While the passive part of the HAPF attenuated the supraharmonics, the active part of the HAPF compensated the lower frequency harmonics. By this principle, better harmonic compensation was achieved. At the same sampling time and samples per cycle, the THD of the input current under the HAPF was successfully reduced to 2.31%, and the h155 harmonic level compensated to 0.16% of the fundamental 50 Hz. These are within the IEEE Std. 519-2022 standards. Figure 11d shows the FFT analysis of the MC input current when the HAPF was used.

6. Conclusions

Supraharmonics in the power system affects power quality and affects load parameters. Traditional passive and active filters may not be enough to compensate these high-frequency harmonics. This investigation provides filter designers with enough information about the strengths and weaknesses regarding the use of HCCs for active power filters. The obtained novel equation debunks the popular notion of uncontrollable and variable switching frequencies, difficulty in filter design and higher loses associated with HCCs when used as higher frequency inverter current controls. The novel equation can be used to size inverters

for any application. As controller for active filters, the HAPF achieved 0.16% THD of the dominant h155 harmonic level after implementation. Compared to traditional passive filter solutions, the obtained results present a better option for MC high-input current harmonic attenuation, as the size and weight of the filter is much improved. The limitations proposed by [39] pertaining to the crippling of the switching frequency by the HCC have been overcome. Future research is directed toward optimization of the equation and the use of model predictive controllers.

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Nomenclature

C_{DC}	DC link capacitance
C_f	Passive filter capacitance
C_{Hf}	HAPF passive-side capacitance
HAPF	Hybrid active power filter
I_{MC}	Matrix converter current at grid frequency
I_S	Source current
L_f	Passive filter inductance
L_{Hf}	HAPF passive-side inductance
L_C/L_Hinv	SAPF/HAPF coupling inductance
MC	Matrix converter
SAPF	Shunt active power filter
S_{MC}	Rated power of matrix converter
V_S	Source voltage
VSC	Voltage source converter
ω	Base frequency in radian
ω_C	Resonance frequency in radian

Appendix A. Effects of the VSC Switches on Maximum Switching Frequency

MOSFETS are widely used in applications that require higher power density and efficiency due to their higher switching speeds and lower losses [38,39]. Irrespectively, increasing the switching speed naturally induces oscillations, higher frequency harmonics, voltage and current overshoots and even more loses. This challenges the use of the MOSFET in power converters, VSCs and active harmonic filters under supraharmonic frequency applications.

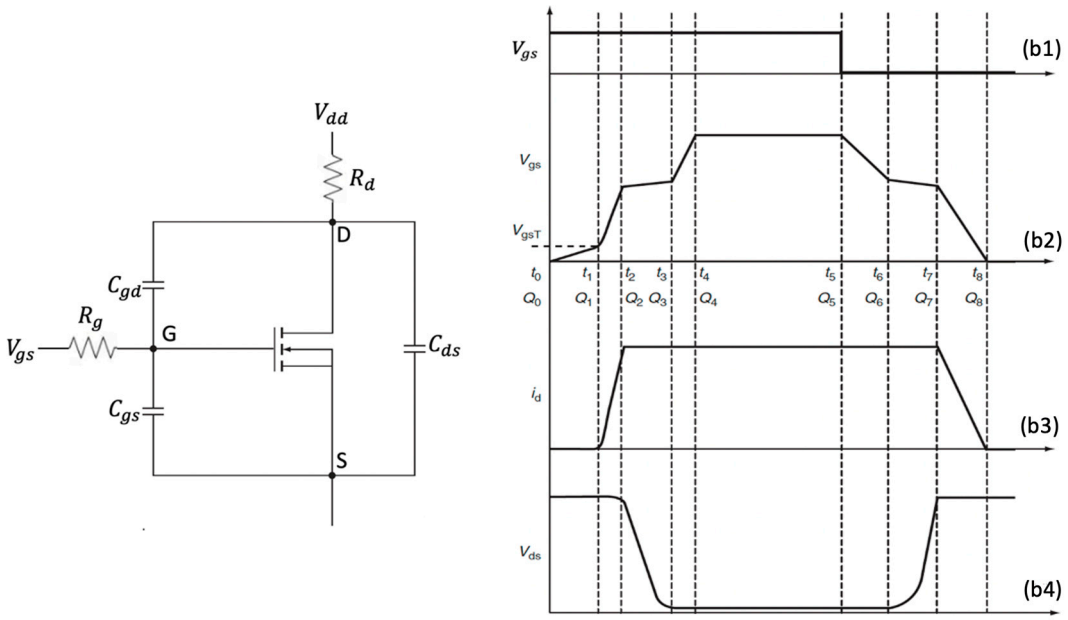
The power MOSFET can be modeled as in Figure A1a which shows the parasitic capacitors; gate-to-source capacitor, C_{gs}, gate-to-drain capacitor, C_{gd}, and drain-to-source capacitor, C_{ds} of a power MOSFET. The gate of the MOSFET is insulated from the substrate; hence, an initial gate current, I_g, is needed to charge both C_{gs} and C_{gd} to turn on the MOSFET. To turn off the MOSFET, the gate drive must be bi-directional to conduct/sink current away from the gate [40–44].

From Figure A1 and considering the initial switching-on stage, the parasitic input capacitances, (C_{gs} + C_{gd}), are charged through the gate resistor, R_g, for a period of t_0 +t_1 =

T_1. The total time delay is dependent on the input capacitance and the logarithmic function of the gate voltage and its threshold. This can be expressed as shown in Equation (A1).

$$T_1 \approx R_g\left(C_{gs} + C_{gd}\right)\ln\left(\frac{V_{gs}}{V_{gs} - V_{gsT}}\right) \tag{A1}$$

The second stage requires raising V_{gs} above the miller plateau. At this stage, the transistor is unblocked and experiences feedback from C_{gd}. The drain voltage drops to its minimum as the drain current increases to its maximum. The total charge, Q_{tot3}, and the equivalent charge, C_{eq}, required through this stage are estimated as Equation (A2) and Equation (A3), respectively. The total delay can be estimated as T_2 in Equation (A5) [45].



(**a**) (**b**)

Figure A1. (**a**) Parasitic capacitance model of the power MOSFET; (**b**) switching characteristics of a power MOSFET. C_{gd}: Gate to drain capacitance; C_{gs}: Gate to source capacitance; C_{ds}: Drain to source capacitance; D: Drain; G: Gate; R_g: Gate resistance; R_d: Load resistance; S: Source; V_{gs}: Gate-to-source voltage; V_{dd}: Transistor voltage source; $Q_{(1\text{-}8)}$: Capacitance charge; V_{gsT}: Gate-to-source threshold voltage; V_{ds}: Drain-to-source voltage; V_{dsmin}: Minimum drain voltage.

$$Q_{tot3} = V_{gs}C_{gs} + C_{gd}\left(V_{gs} + V_{dd}\right) \tag{A2}$$

$$C_{eq} = \frac{Q_{tot3}}{V_{gsmax}} = C_{gs} + C_{gd}\left(1 + \frac{V_{dd}}{V_{gsmax}}\right) \tag{A3}$$

$$\frac{V_{dd}}{V_{gsmax}} = miller\ effect \tag{A4}$$

$$T_2 \approx 0.8C_{gd}\frac{R_g(V_{dd} - V_{dsmin})}{V_{gs} - V_{gsT}(V_{dd} + V_{dsmin})/2R_dS} \tag{A5}$$

For $S:\ \Delta I_d/\Delta V_{gs}$

In the third stage, the V_{ds} drops to its minimum, and the MOSFET is driven in full enhancement mode, and the total time duration is T_3 in Equation (A6).

$$T_3 \approx 3R_g\left(C_{gs} + C_{gd}\right) \tag{A6}$$

T_1+ T_2+ T_3 makes up the total turn on time of the MOSFET, T_{on}.

$$\mathrm{T_{on}} = \mathrm{T_1} + \mathrm{T_2} + \mathrm{T_3}$$
$$T_{on} = \frac{1.6C_{gd}R_gR_dV_{dd}S}{2V_{gs}R_dS - V_{gsT}V_{dd}} + R_g\left(3 + \ln\left(\frac{V_{gs}}{V_{gs} - V_{gsT}}\right)\right)\left(C_{gs} + C_{gd}\right) \tag{A7}$$

At

$$V_{dsmin} \approx 0$$

The total required gate current to turn on the MOSFET can be calculated as shown in Equation (A8).

$$i_g = \frac{C_{eq}V_{gsmax}}{T_{on}} \tag{A8}$$

The next stage is from t_4–t_5, which is characterized by constant values of currents and voltages and equivalent to the saturation stage of a bipolar transistor. The gate current remains zero during t_4–t_5 when the MOSFET is fully on. No charge is required to keep it on.

The fifth stage begins the turn-off stage of the MOSFET. The gate pulse signal becomes zero, and the turn-off sequence is initiated. When the input pulse signal drops to zero, the capacitance $C_{gs} + C_{gd}$ begins to be discharged. It is most important for the appropriate gate driver to be bi-directional. The total time required to discharge can be calculated as Equation (A9).

$$T_4 = R_g\left(\mathrm{C_{gs}} + C_{gd}\right)\ln\left(\frac{V_{gs}}{V_{diss}}\right) \tag{A9}$$

where the discharge voltage is given as Equation (A10).

$$V_{diss} = V_{gsT} + \frac{(V_{dd} - V_{dsmin})}{R_dS} \tag{A10}$$

The MOSFET is discharged from the ohmic region to the off state. The drain-to-source voltage is increased during this time. The total time duration can be given by Equation (A11).

$$T_5 \approx 0.8C_{gd}\frac{R_g(V_{dd} - V_{dsmin})}{V_{\mathrm{gsT}} + (V_{dd} - V_{dsmin})/2R_dS} \tag{A11}$$

In the final stage, C_{gs} is discharged to a full turn-off state, V_{ds} is raised to its initial value and I_d is minimized to zero. The total time delay can be estimated based on R_g and the input capacitances as in Equation (A12).

$$T_6 \approx 3R_g\left(\mathrm{C_{gs}} + C_{gd}\right) \tag{A12}$$

The total off time can be estimated based on the combination of $\mathrm{T_4}$ + $\mathrm{T_5}$ + $\mathrm{T_6}$ as in Equation (A13) at a minimum $\mathrm{V_{dsmin}}$ of 0.

$$T_{off} = \frac{1.6C_{gd}R_gR_dV_{dd}S}{2V_{gsT}R_dS + V_{dd}} + R_g\left(3 + \ln\left(\frac{V_{gs}}{V_{gsmax}}\right)\right)\left(C_{gs} + C_{gd}\right) \tag{A13}$$

The total switching time of the MOSFET can be calculated as T_{on} + T_{off}. The maximum allowable switching frequency based on the above deduction can then be obtained with the inverse of the total switching period. Considering the IRFP450 enhancement mode MOSFET parameters specified in Table A1, the total on and off time delays from Equations (A7) and (A13), the maximum switching frequency can be mathematically estimated as Equation (A14).

Table A1. IRFP450 MOSFET parameters.

Parameter	Value
V_{dd}	500 V
Drain-to-source voltage, V_{ds}	500 V
Drain current, I_d	14 A
Gate-to-source voltage, ±Vgs	20 V
Ciss (Cgs + Cgd)	2600 pF
Coss (Cds + Cgd)	720 pF
Crss/Cgd	340 pF
Cgs	2260 pF
Cds	380 pF
Conductance, S	1–10 mA/V
Gate-to-source threshold voltage, (VgsT)	2–4 V

$$T_{on} = \frac{2.72 \times 10^{-7} R_g R_d S}{40 R_d S - 1500} + 8.22 \times 10^{-9} R_g$$

$$T_{off} = \frac{2.72 \times 10^{-7} R_g R_d S}{6 R_d S + 50} + 7.8 \times 10^{-9} R_g$$

For
S: 1 mA/V
R_g: 3 ΩR_d: 3.57 Ω

$$\begin{gathered} T_{tot} = \frac{8.16\times10^{-7}}{0.12-1500} + \frac{8.16\times10^{-7}}{0.018+500} + 4.8 \times 10^{-8} \\ F_{sw} = \frac{1}{T_{on}+T_{off}} = 20.8MHz \end{gathered} \tag{A14}$$

The obtained maximum frequency, F_{sw}, from Equation (A14) is calculated based on manufacturers data provided on the datasheet of the IRFP450, and operational values will differ. The maximum obtainable frequency was analyzed for various values of R_g and R_d at S = 1 mA/V. Tables A2 and A3 show the results of these variations of the frequency. From Table A3, it can be observed that increasing the gate resistance alleviates the switching frequency, which will eventually reduce oscillations and electromagnetic interferences (EMIs) [44–47]. However, the reduction in switching speed increases switching losses and the on/off time delays.

Table A2. Maximum switching frequency at constant gate resistance, R_g (3 Ω) and variable load resistance, R_d.

Parameter	Value			
R_d	Full load resistance (3 Ω)	10 k Ω	100 k Ω	300 k Ω
F_{sw}	20.8 MHz	18.1 MHz	6.4 MHz	5.6 MHz

Table A3. Maximum switching frequency at constant gate resistance, R_d (3.57 Ω) and variable gate resistance, R_g.

Parameter	Value			
R_g	1 Ω	3 Ω	10 Ω	20 Ω
F_{sw}	62.4 MHz	20.8 MHz	6.2 MHz	3.12 MHz

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