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# Digitalization of Pulse Signal Processing for Ex-Core Instrumentation System in Nuclear Power Plants

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**Featured Application: Proposed research could be useful in condition monitoring activities for neutron detectors and neutron instrumentation systems.**

**Abstract:** Nuclear power plants (NPPs) are globally important sources of clean energy. However, high operation and maintenance (O&M) costs are one of the factors hindering the development of NPPs. In this study, we focused on the development of a digital algorithm for ex-core instrumentation systems (EISs) to reduce O&M costs, given that the digitalization of EISs is not progressing compared with other instrumentation and control systems in NPPs. Specifically, we developed a digital algorithm for pulse signal processing in EISs, which traditionally require a significant amount of hardware and maintenance efforts. Our purposes were to simplify the configuration and reduce the O&M costs associated with pulse signal processing. To validate the algorithm, we used a detector emulator and a research reactor. Additionally, we explored a new approach to reduce the workload associated with a discrimination characteristics test (DCT) in EISs. The results of this study demonstrated that the proposed algorithm is effective in achieving good linearity within ±5% of the span and response performance with a delay time of 5 ms, which are required for EISs. Furthermore, the proposed method for the DCT shows promising results in reducing the time required for the test compared with conventional methods.

**Keywords:** nuclear power plant; instrumentation and control system; digitalization; field-programmable gate array

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**Citation:** Konishi, R.; Sasano, M.; Hayashi, M.; Azuma, T. Digitalization of Pulse Signal Processing for Ex-Core Instrumentation System in Nuclear Power Plants. *Appl. Sci.* **2024**, *14*, 2445. https://doi.org/10.3390/app14062445

Academic Editors: Chia-Hung Lin, Neng-Sheng Pai, Chao-Lin Kuo, Chang-Hua Lien and Gianluigi Ferrari

Received: 31 January 2024
Revised: 8 March 2024
Accepted: 12 March 2024
Published: 14 March 2024

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## 1. Introduction

Nuclear power plants (NPPs) are globally important sources of clean energy that do not emit greenhouse gases. According to the International Atomic Energy Agency (IAEA), global electricity consumption is increasing annually, and it is predicted that by 2050, it will be approximately double that of 2022 [1]. Nuclear power is expected to contribute to both the rapid increase in electricity consumption and the mitigation of global warming, and the construction of new NPPs is planned around the world [2]. While there are multiple types of NPPs, many use pressurized water reactors (PWRs), and most of the plants planned for future construction also use PWRs. Additionally, most of the small modular reactors (SMRs) currently being developed are also based on PWR technology.

From an economic perspective, NPPs face the challenge of higher operation and maintenance (O&M) costs compared with other power sources such as coal, oil, and liquefied natural gas-fired thermal power. The O&M costs of nuclear power are approximately twice as high as those of thermal power generation [3]. Reducing the O&M costs of NPPs is a problem that needs to be solved for the planned expansion and stable operation of NPPs. In the United States, grants have been provided for research on using digital technology to

reduce O&M costs to one-tenth of the conventional level, specifically targeting innovative reactors [4]. It is anticipated that the utilization of digital technology will be essential for reducing O&M costs.

In this study, we focus on ex-core instrumentation systems (EISs), which are essential for PWR plants, both currently in operation and planned for future construction. An EIS monitors the state of the reactor core by detecting neutron leakage from the reactor core with neutron detectors installed outside the reactor and issuing trip signals in case of abnormal conditions, making it a crucial component for PWR operation. However, the digitalization of EISs has been lagging behind other instrumentation and control (I&C) systems. The advantages of digitizing the I&C system include the ability to replace multiple hardware components with software, enabling miniaturization, reducing the number of degraded parts, and facilitating easy replacement. Additionally, utilizing digital technology allows for self-diagnosis, where the system itself can detect faults, leading to significant improvements in maintainability and reliability. While existing I&C systems are being replaced with digital systems, many EISs still remain analog. This is believed to be due to the unique neutron measurement required in nuclear power, as well as the high-speed operation for a safety system. In particular, EISs require rapid response performance compared with other I&C systems [5].

There are several examples of digitalizing EISs. One example is the SPINLINE system developed by Rolls-Royce, which utilizes a calibrated pulse acquisition board with a microcontroller [6,7]. The SPINLINE system processes pulse signals from the neutron detector by combining the calibrated pulse acquisition board with the UC25 N+ processor board [6]. Another example is the DWK250 system developed by Mirion Technologies, which incorporates the NI 21 module to discriminate pulse signals derived from neutrons from other signals such as gamma rays and electrical noise, as well as the NZ21 module for signal processing to generate the count rate [8]. These examples demonstrate the ongoing progress in digitalizing pulse signal processing for EISs.

As previously mentioned, there are few examples of digitalizing pulse signal processing for EISs, all of which use multiple modules for pulse measurement and microprocessors. The IAEA mentioned that techniques utilizing microprocessors have replaced analog techniques used in NPPs because microprocessors have many advantages compared with analog devices. However, microprocessors now have short product life cycles, and applications may become obsolete in a relatively short time due to a lack of replacement parts and support [9]. These indicate that there is room for improvement in terms of reducing hardware quantities and ensuring the continuity of production. Additionally, EISs have redundancy required for the safety system. By digitizing EISs, it is possible to achieve significant cost-savings through reduced hardware requirements. In this study, we aim to further reduce the hardware required for pulse signal processing in EISs by developing a newly devised digital algorithm with a field-programmable gate array (FPGA). FPGAs have attracted attention for their low design and verification costs, resistance to cybersecurity threats, and production continuity. We will explain this algorithm and present the validation results using a detector emulator and a research reactor. Additionally, we will discuss the feasibility of a new approach to reduce the workload associated with the discrimination characteristics test (DCT) for the maintenance of EISs.

## 2. Previous Research

There have been studies regarding the digitalization of EISs [10–12]. Kim et al. [10] proposed methods for processing pulse signals and the mean square value output of a fission chamber (FC) in the digital-signal-processing unit. Mjzoob et al. [11] aimed to digitalize the Intermediate Range (IR). However, the main topic of these studies was the validation of an algorithm for digital processing of an EIS using simulations, and they did not experiment on the basis of actual detector signals. Joo et al. [12] demonstrated the performance of the digital wide-range neutron power measurement channel, including pulse signal processing, using a research reactor. However, the feasibility of achieving the

required high-speed response in an EIS using digital circuits has not been discussed. It is essential to validate the safety functions required for an EIS to be used in commercial power reactors. Therefore, we believe that the verification conducted in this study will be beneficial for advancing the digitalization of EISs.

Figure 1 shows the traditional EIS configuration for PWRs. An EIS has three different ranges, i.e., source range (SR), IR, and power range (PR), to monitor a wide measurement range spanning 12 digits from reactor shutdown and startup to normal operation [13]. The IR and PR process the signal output from the compensated ion chamber (CIC) or uncompensated ion chamber (UIC) by using a logarithmic amplifier or summing amplifier, whereas the SR processes the pulse signal output from the proportional counter (PC) by using several analog modules, i.e., a preamplifier, pulse amplifier, pulse shaper, and logarithmic amplifier. Using many analog modules increases O&M costs and has the potential to limit the continuity of production. Thus, digitalization will greatly benefit the SR in terms of reducing modules and continuing production for plant operation. Another advantage of digitalizing the SR is to improve its maintainability because the number of SR maintenance tests is higher than that for other ranges, e.g., the V-I characteristics test, plateau characteristics test, and DCT. The purpose of the DCT is to set a discrimination level that can distinguish pulse signals derived from neutrons from other signals. The discrimination level may vary due to environmental factors such as noise and the degradation of the detector. Typically, a graph of discrimination characteristics is created by plotting pulse counts at various discrimination levels to determine the appropriate threshold. In a traditional EIS, the pulse shaper includes a discrimination function and generates a rectangular pulse when the original pulse signal exceeds the discrimination level. The scaler-timer then counts the number of rectangular pulses within a specified period to create the graph. However, this traditional method requires multiple changes in discrimination levels and pulse counts to compensate for the loss of pulse height information. To address this issue, we explored an alternative method with digital techniques, which incorporates a peak hold function to capture the maximum pulse height of each original pulse and a software function to create a discrimination characteristics graph directly using the acquired pulse height information.

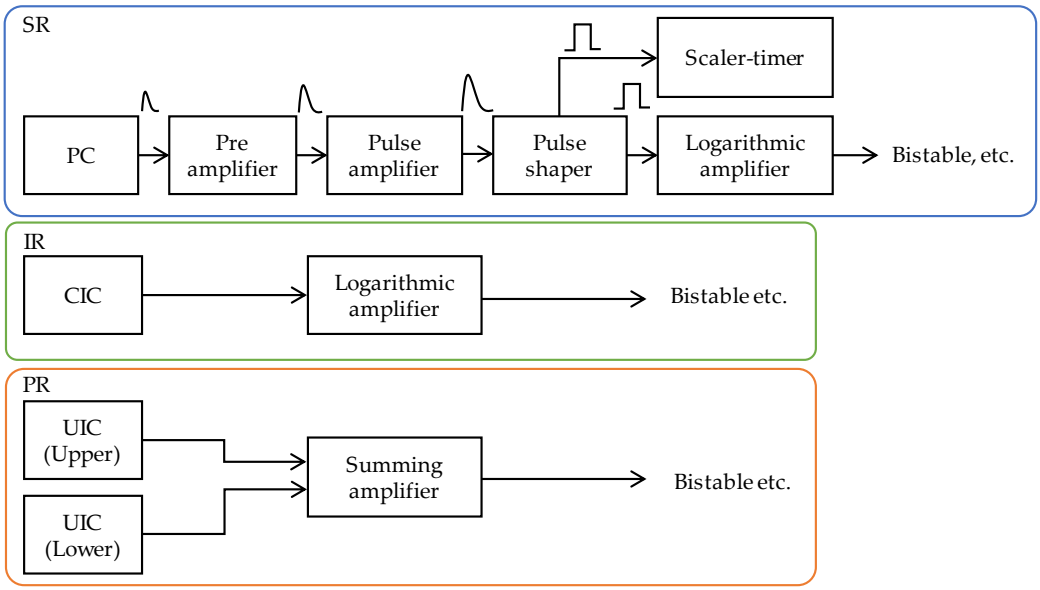



**Figure 1.** Traditional EIS configuration.

## 3. Design of Algorithm

### *3.1. Requirements*

In this study, we will confirm the basic performances of an EIS required for the operation of NPPs, i.e., linearity and response time. The requirements of the digital

algorithm for pulse signal processing in this study are as follows. These requirements are referred to in the latest NPP, AP1000 design control document [5].

- Measurement range is 6 decades of neutron flux: 1 to $10^6$ counts per second (cps);
- Accuracy is within ±10% of the span;
- Response time at reactor trip is within 600 ms;
- In addition to the above, the following points should also be considered:
- The algorithm should be implemented on an FPGA;
- The resource utilization of the algorithm should be kept below 80%.

As mentioned in Section 1, microprocessors, which were traditionally dominant in digital systems, are now considered obsolete technology when considering component replacement. Therefore, it is advisable to utilize the latest technology, such as FPGA. Another advantage of using FPGA is the consideration of Common Cause Failure (CCF), which is one of the requirements to be considered in safety systems of NPPs. Countermeasures for CCF using FPGA have already been recognized by the nuclear regulatory commission [14]. Furthermore, since this study focuses on the basic functionality of EISs as the target of digital algorithms, it is important to design with some margin in resource utilization to anticipate future functional expansions.

### *3.2. Configuration*

FPGAs are important in digitalizing I&C systems in NPPs since they enable high-speed calculations with parallel processing and can be easily replaced when an FPGA device has been discontinued. We used the Digilent (Pullman, WA, USA) FPGA evaluation board Eclypse Z7 [15] equipped with Xilinx's (San Jose, CA, USA) Zynq-7000 combined with the Digilent (Pullman, WA, USA) analog-to-digital converter (ADC) Zmod ADC1410 [16] for the digital algorithm design. Figure 2 shows the configuration of digital pulse signal processing. Since the pulse signals output from a detector such as an FC are extremely short (e.g., 200 ns), the ADC for EISs must have an adequate sampling rate. Table 1 shows the features of Zmod ADC1410. We aimed to convert the analog signal to a digital signal after the preamplifier so that the SR can have a simple configuration with the minimum analog modules. This improves cost-effectiveness, scalability, and maintainability because it reduces modules such as a pulse amplifier, pulse shaper, and logarithmic amplifier indicated in Section 2, and enables easy modification with only code changes. Zynq-7000 consists of a system-on-chip-integrated processing system (PS) and a programmable logic (PL) unit. The PL is equipped with FPGA, and the PS is equipped with a processor. As shown in Figure 2, most processing functions are achieved in the PL, and the PS is only used for communication with the PC.

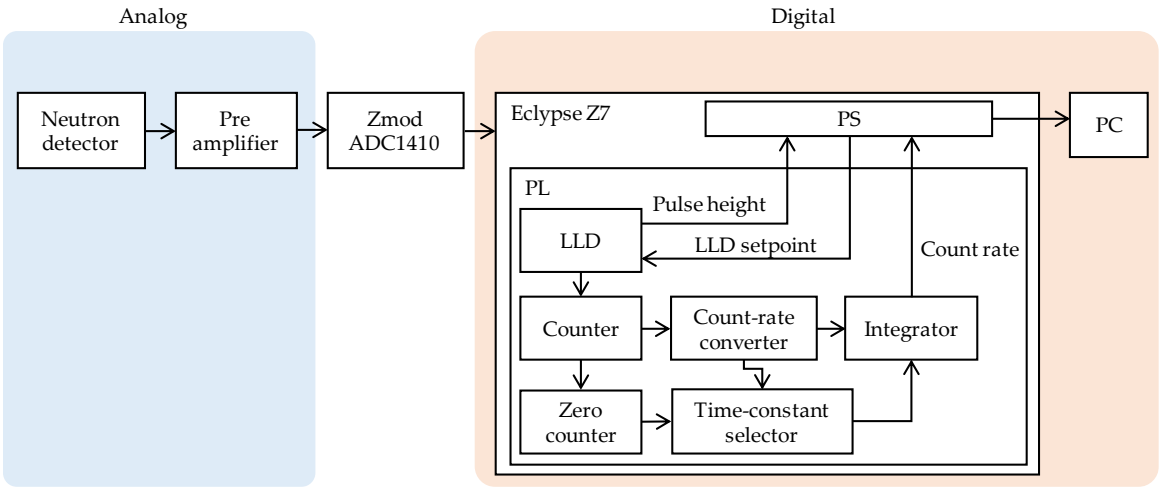



**Figure 2.** Configuration in this study with ADC and FPGA evaluation board.

**Table 1.** Features of Zmod ADC1410 [17].

| Resolution | Input Range | Sample Rate | Input Impedance | Analog Bandwidth |
|---|---|---|---|---|
| 14-bit | ±1 V | 105 MS/s | 1 MΩ | 70 MHz @ 3 dB |

### *3.3. Algorithm for Pulse Signal Processing*

In the PL, we have designed six function blocks: the lower-level discriminator (LLD), counter, count-rate converter, zero counter, time-constant selector, and integrator.

The LLD receives the digital signal that has been converted by the ADC. It discriminates the pulse signal derived from neutrons from other signals, such as gamma rays or electrical noise, using a logic function. This discrimination is based on determining whether the pulse height exceeds a preset threshold. If the pulse height exceeds the threshold, the LLD identifies the signal as being derived from neutrons. The LLD then outputs rectangular pulses depending on the number of signals that exceed the threshold. The LLD also has a peak hold function and outputs the maximum pulse height at each inputted pulse to use in creating the discrimination characteristics graph at the PC.

The counter counts the pulses that are output by the LLD when the signals exceed the threshold every 1 ms.

The zero counter counts the periods when the counter's count is zero every 1 ms to select a time constant in the case of a low count rate.

The count-rate converter converts the pulse counts to a count rate (X) by multiplying a constant coefficient of 1000 ($coef_{const}$) and preset variable coefficients ($coef_{var}$) in lookup tables (LUTs) shown in Figure 3 with the latest counter's output ($C_n$) as represented in Equation (1). The preset variable coefficients are used for inhibiting the fluctuation of neutron and disturbance signals, such as electromagnetic noise, and are controlled with $C_n$ and the previous counter's output ($C_{n-1}$), as shown in Figure 4. The variable coefficients are set with 14 values, ranging from 0.05 to 1, and are selected on the basis of the relationship between $C_n$ and $C_{n-1}$. The initial value is set to 0.05, and if $C_n$ is equal to or greater than 10% but less than 10 times $C_{n-1}$, the variable coefficient increases to the next value, which is 0.2. If this condition continues, the variable coefficient increases up to its maximum value of 1. If $C_n$ is less than 10% or greater than or equal to 10 times $C_{n-1}$, it is reset to the initial value.

$$X = coef_{const} \cdot coef_{var} \cdot C_n \quad (1)$$

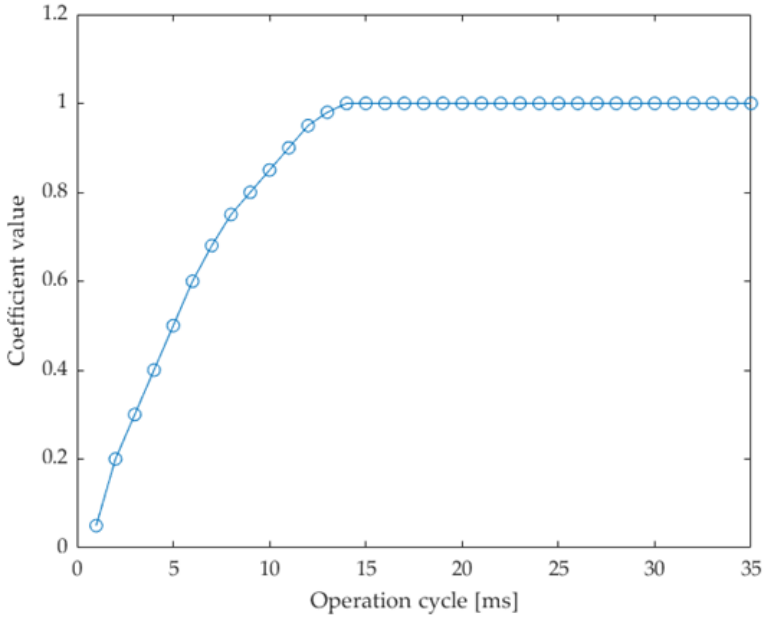



**Figure 3.** Variable coefficient multiplied by the counter's output.

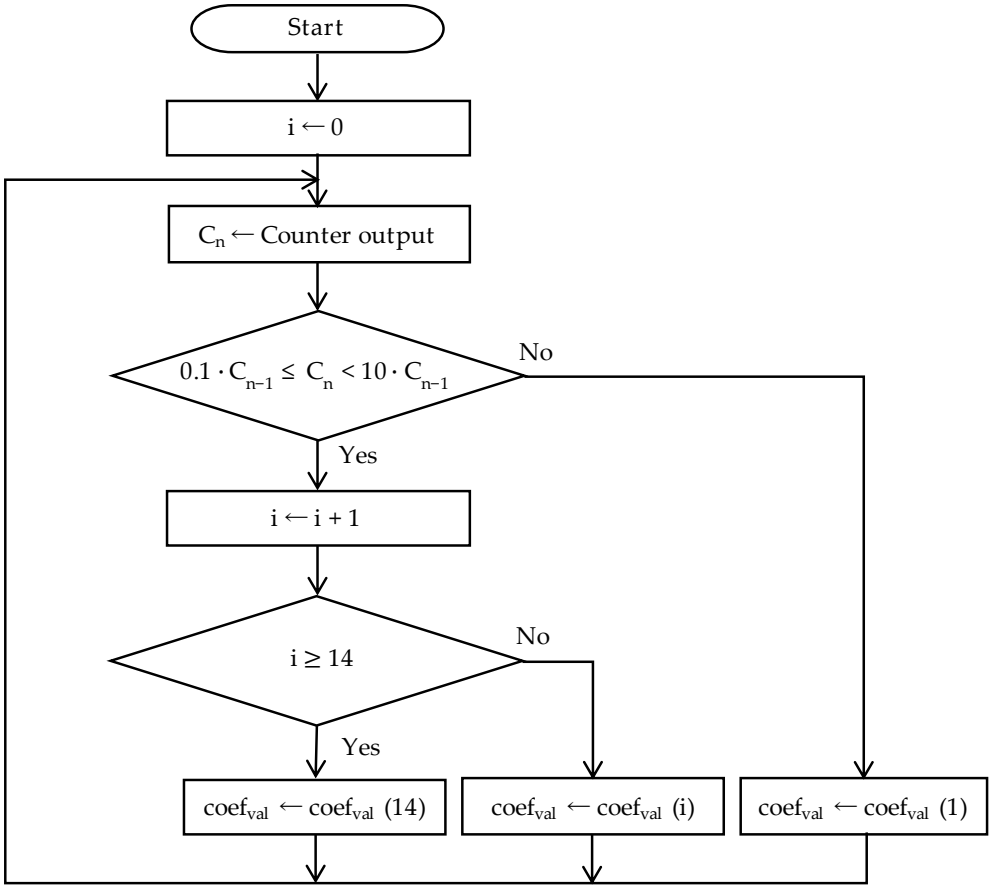



**Figure 4.** Flow chart of selecting variable coefficients.

The time-constant selector automatically selects a preset time constant from the LUTs to be used for the first-order lag calculation implemented in the integrator. The time constants need to be long during a reactor shutdown when there is a relatively low count rate to ensure measurement reliability, but they need to be short under startup to normal operations when there is a relatively high count rate to quickly detect any abnormal change in reactor power. The time-constant selector contributes to this responsiveness by selecting a time constant on the basis of the output from the count-rate converter. Figure 5 shows all time constants set for this study, totaling approximately 200. Time constants $10^3$ to $10^6$ cps, when an output from the count-rate converter will be non-zero, were set on the basis of Equation (2), and time constants for other count-rate ranges when an output from the count-rate converter will be zero or non-zero were set on the basis of Equations (2) and (3).

$$\tau = \frac{1}{2 \cdot n \cdot \sigma^2}, \tag{2}$$

where $\tau$ is a time constant, n is a count rate, and $\sigma$ is the relative standard deviation.

$$n = \frac{1000}{C_0 + 1}, \tag{3}$$

where $C_0$ is the period during which the output from the count-rate converter is zero.

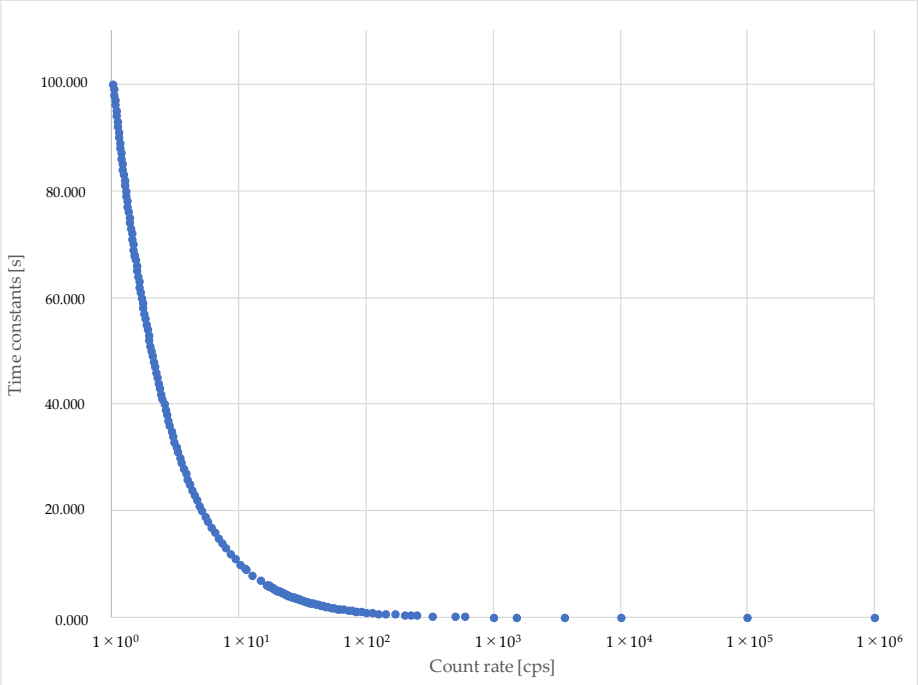



**Figure 5.** Relationship between time constants and count rate.

The integrator implements a first-order lag calculation using Equation (4) with a count rate and time constant from the count-rate converter and the time-constant selector, respectively.

$$Y_i = Y_{i-1} \cdot e^{-\frac{T}{\tau_i}} + \left(1 - e^{-\frac{T}{\tau_i}}\right) \cdot X_i, \quad (4)$$

where $Y_i$ is the output at the i-th sampling time, $Y_{i-1}$ is the output at the previous i-th sampling time, $X_i$ is the output from the count-rate converter at the i-th sampling time, T is the sampling time, and $\tau_i$ is the i-th time constant.

The resource utilization which includes six function blocks and ADC control logics is shown in Table 2. The resource utilization was approximately 30%, indicating that there was sufficient margin available.

**Table 2.** Resource utilization.

| Site Type | Used | Available | Utilization |
|---|---|---|---|
| Slice LUTs | 6999 | 53,200 | 13.16% |
| Slice registers | 6809 | 106,400 | 12.85% |
| DSPs | 7 | 220 | 3.18% |

### *3.4. Application of Discrimination Characteristics Test*

Our proposed method for the DCT is to create a discrimination characteristics graph using collected maximum pulse heights output from the LLD. The Zmod ADC1410 converts pulse signals into 16-bit digital signals. The LLD outputs the maximum value of the pulse signal converted into a digital signal to the PC via the PS. The graph is created by running software developed using MATLAB (R2023a) on the PC. The software lists the maximum values of the pulse signals obtained during a specified period. Next, it searches for addresses, pre-assigned from 1 to 65,535, that match the maximum value of the pulse signal and increments the count value stored at each address whenever the address and maximum value match. After performing the search and count for all data in the list, it generates a total count value by summing up the count values for all addresses. The graph

is created by subtracting the count values stored at each address from the total count value in ascending order of addresses.

## 4. Results and Discussions

### *4.1. Validation Using Detector Emulator*

Figure 6 illustrates the configuration for validation using a detector emulator. The CAEN NDT6800D [18] was used to generate the simulated pulse signals shown in Figure 7.

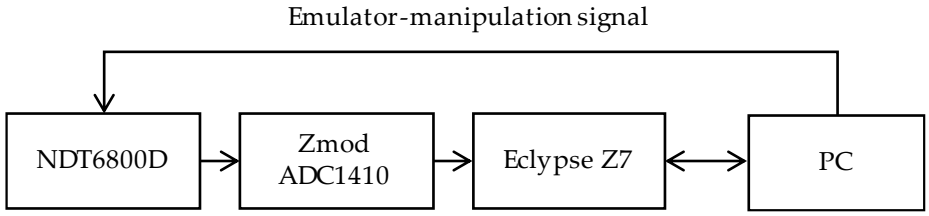



**Figure 6.** Experimental configuration with detector emulator.

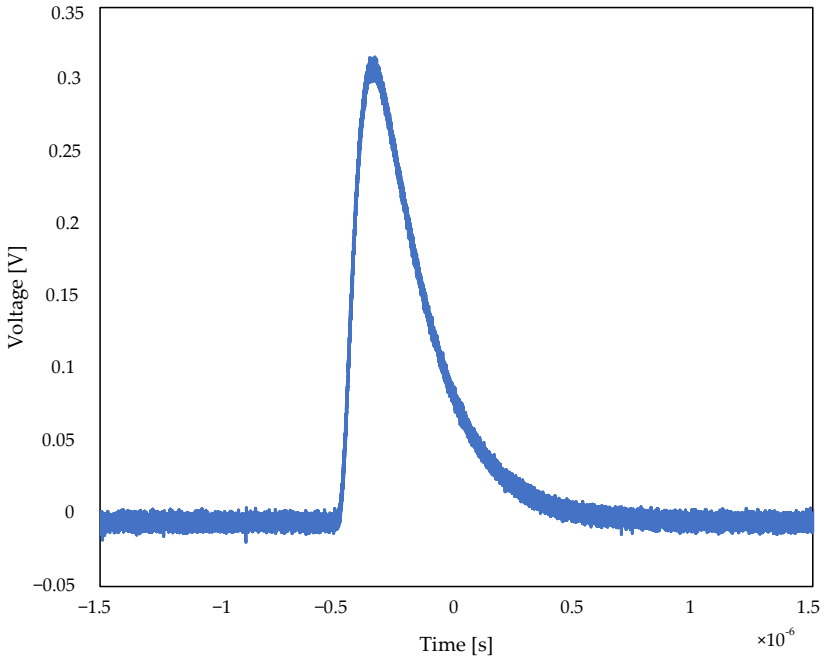



**Figure 7.** NDT6800D output pulse signal.

In this experiment, we validated linearity and response time performance. To validate linearity, the pulse signals generated by the NDT6800D with a range of 1 to $10^6$ cps and a constant or random signal frequency were inputted to the FPGA evaluation board. The random signal frequency was based on a Poisson distribution. The result of linearity validation is shown in Figure 8. We confirmed that FPGA outputs are within ±5% of the span. The result satisfies the requirement mentioned in Section 3.1, indicating that the proposed algorithm demonstrates good linearity performance.

To validate response time, we assumed the trip set point is $10^5$ cps in this experiment, referred to as the traditional PWR [13], and set the input signal by varying the count rate from −10% to +10% of the set point. The result of the response time is shown in Figure 9. The FPGA outputs reached the set point after approximately 5 ms, within the required performance response time mentioned in Section 3.1. This indicates that the proposed algorithm demonstrates rapid response performance.

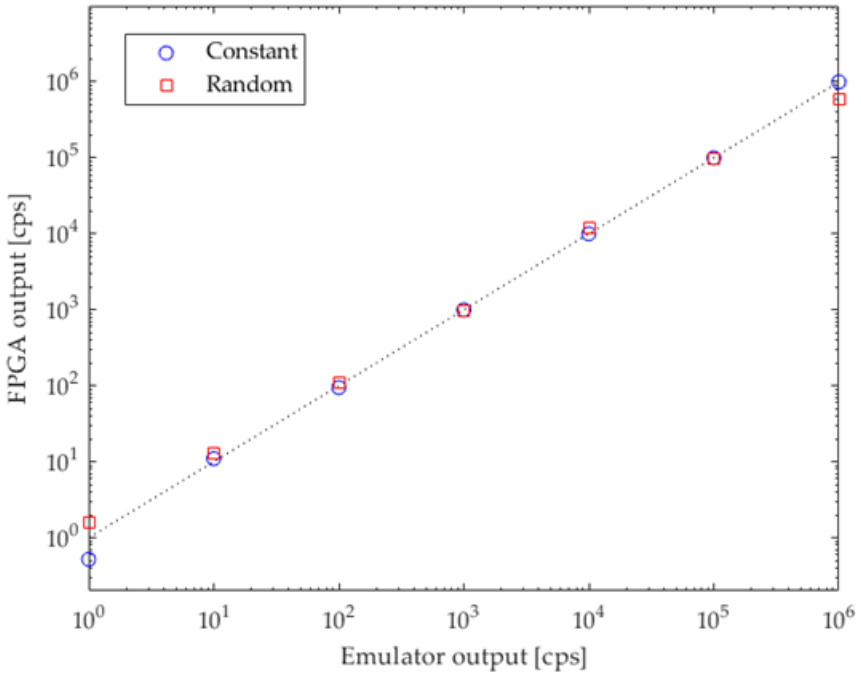



**Figure 8.** FPGA output for emulator output.

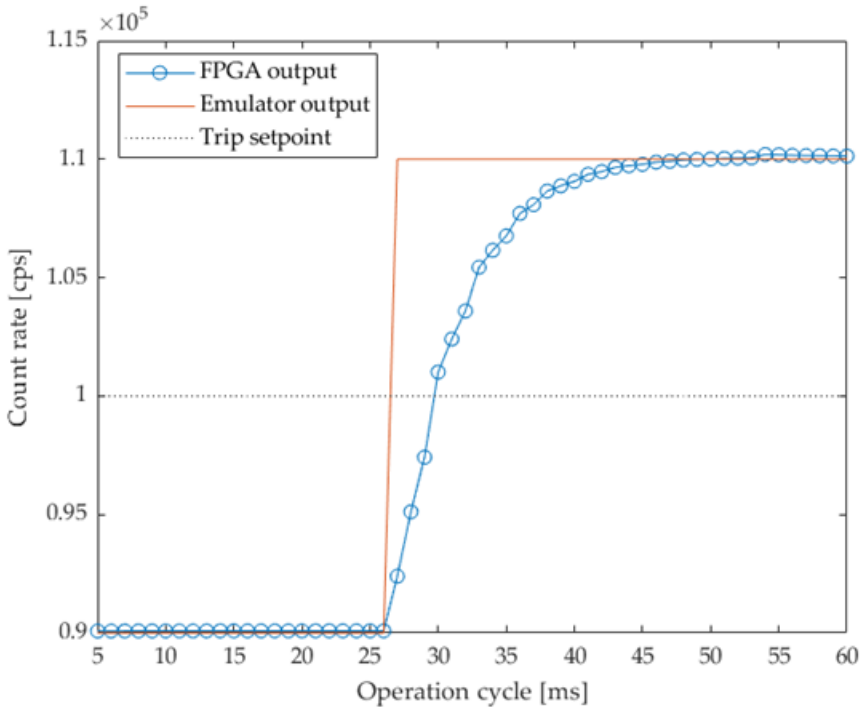



**Figure 9.** Response characteristics of the developed algorithm.

### *4.2. Validation Using Research Reactor*

In this experiment, we validated linearity using the UTR-KINKI Research Reactor designed and produced by the American Standard Corporation (Mountain View, CA, USA) [19] at Kindai University, with the FC as a neutron detector. The configuration of the experiment is shown in Figure 10. The reference signal for a true count rate to be compared with FPGA outputs was measured using the Amptek (Bedford, MA, USA) Digital Multichannel Analyzer MCA-8000D.

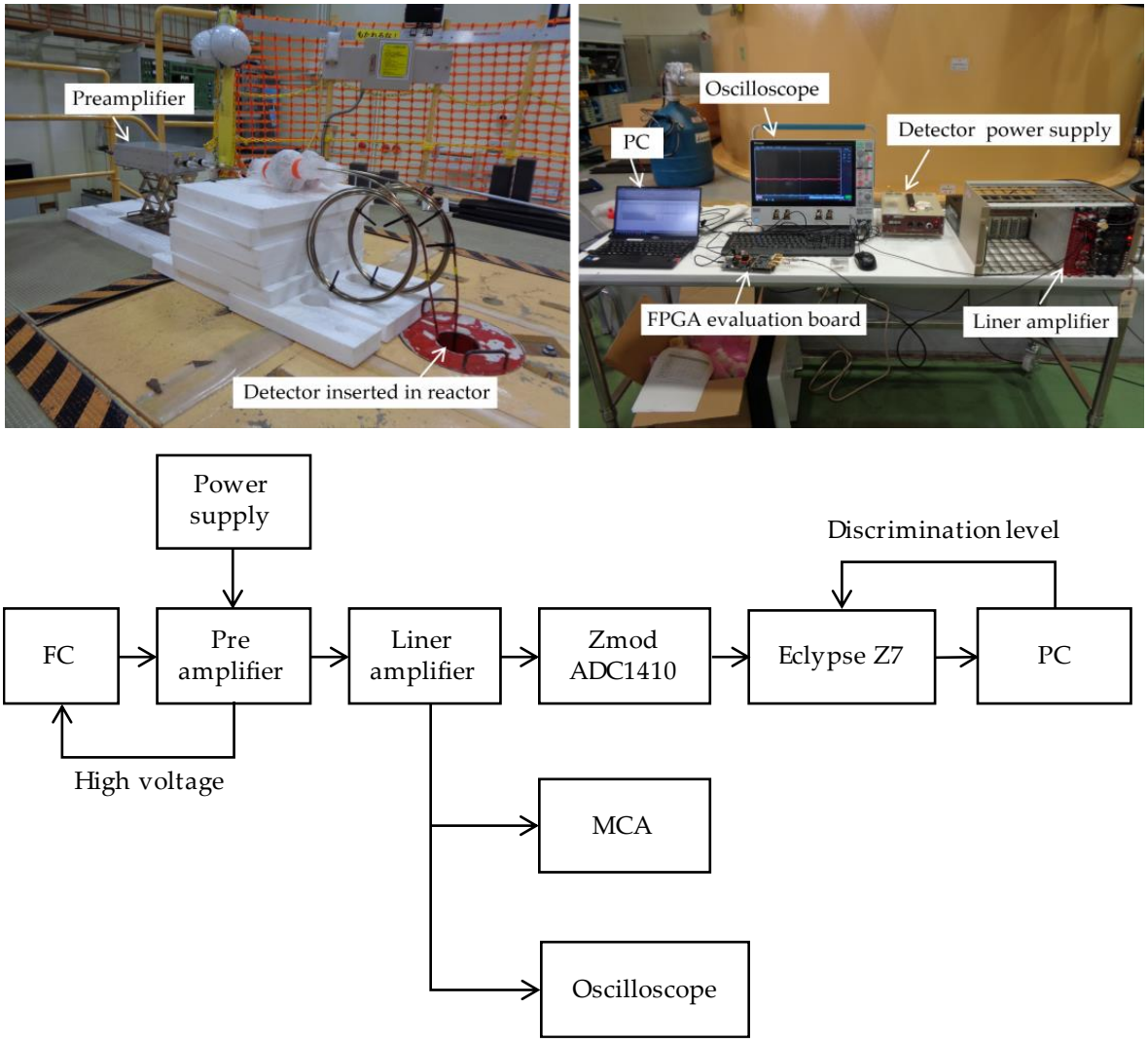



**Figure 10.** Experimental configuration with UTR-KINKI Research Reactor.

The result of linearity is shown in Figure 11. FPGA outputs are within ±2% of the span. The result satisfies the requirement mentioned in Section 3.1, indicating that the proposed algorithm demonstrates good linearity performance. However, for a reactor power of 0.01 W, there is a difference between the FPGA output and MCA output. We suspect that this is due to the limited number of time constants available in the count-rate converter because the number of time constants in $10^3$ from $10^6$ cps is lower than the rest of the range. To investigate this hypothesis, we created a simulation model using MATLAB (R2023a) Simulink and added one additional time constant in the range of $10^4$ to $10^5$ cps. We then conducted verification using this simulation model. Figure 11 shows the results of comparing the original algorithm with the improved algorithm using the simulation model created in MATLAB Simulink. The results of the original algorithm align well with the verification results using the research reactor, confirming the validity of the simulation model. Furthermore, the results of the improved algorithm align well with the values obtained from the MCA-8000D at 0.01 W, demonstrating that the addition of time constants can improve linearity.

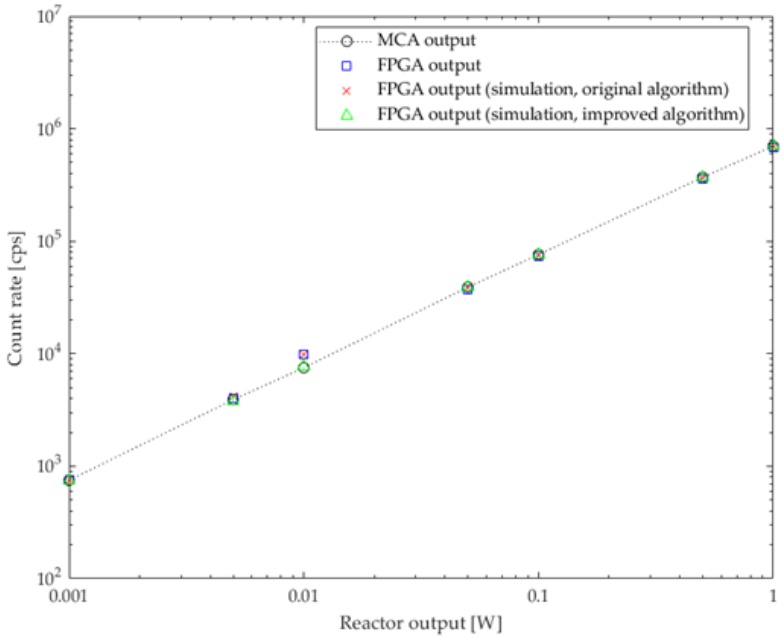



**Figure 11.** FPGA output with respect to reactor output.

### *4.3. Feasibility of a New Discrimination Characteristics Test Method*

In this experiment, we used an FC as a neutron detector. The FC is coated with $UO_2$, a fissile material. When a neutron interacts with the $UO_2$, it produces fission fragments. Since the $UO_2$ emits alpha particles for alpha decay, pulses derived from alpha particles become background noise [20]. Figure 12 shows the discrimination characteristics graph created using the proposed method with pulse heights collected at 0.01 W reactor power. In Figure 12, a region where the counts remain constant between 0.03 V and 0.08 V is obtained, indicating the separation of pulses from alpha particles and neutrons. Figure 13 represents the spectrum of the FC obtained with the MCA-8000D, and the pulses from alpha particles and neutrons are separated around 0.05 V, indicating the validity of the discrimination characteristics graph shown in Figure 12.

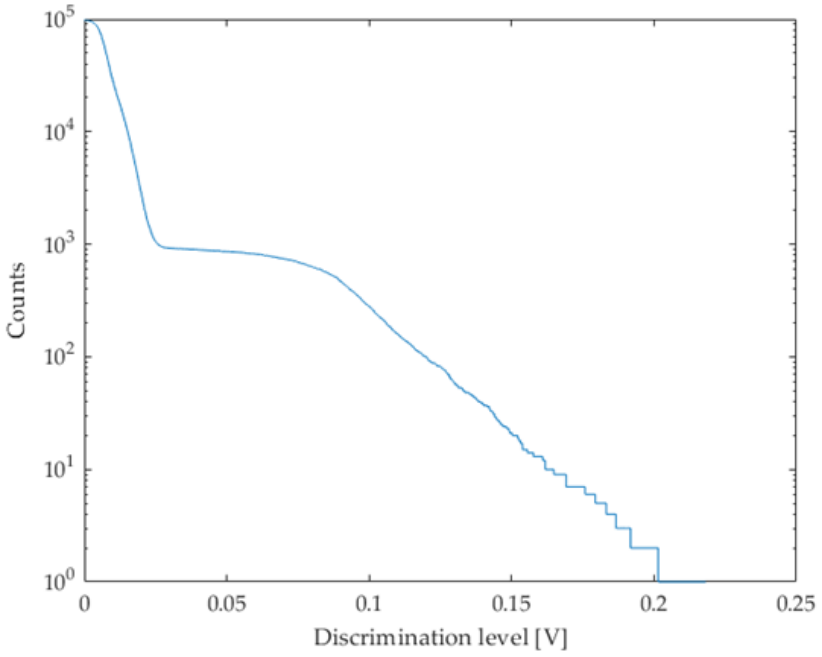



**Figure 12.** Discrimination characteristics graph obtained using the proposed method.

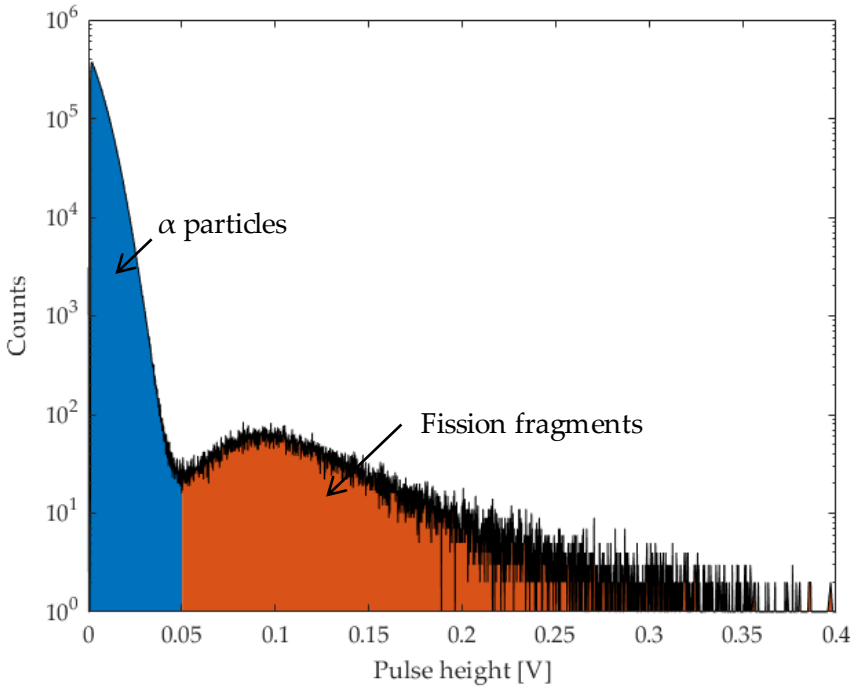



**Figure 13.** FC spectrum obtained using MCA-8000D.

In conventional methods, obtaining the discrimination characteristics graph required changing the discrimination level and collecting counts, which took a considerable amount of time. However, with the proposed method, the graph can be created in a very short time, enabling a reduction in workload for maintenance through the utilization of a digital technique.

## 5. Conclusions

The digitalization of instrumentation and control systems plays a crucial role in reducing operation and maintenance (O&M) costs of nuclear power plants (NPPs). In this study, we focused on ex-core instrumentation systems (EISs), which are essential systems for the safe and secure operation of pressurized water reactor plants. Traditional EISs used in many existing NPPs are composed of multiple analog modules, and particularly in pulse signal processing, many analog modules are required. Therefore, there is a need for digitalization to simplify the configuration and improve maintainability. There are several examples of digitalizing EISs, but they use a microprocessor that is now obsolete. Therefore, state-of-the-art technology is required to digitalize EISs.

We conducted a demonstration study using a field-programmable gate array (FPGA) combined with a high-speed analog-to-digital converter to develop and validate a digital algorithm for efficient pulse signal processing, and explored a new method to enhance the efficiency of maintenance work associated with the discrimination characteristics test (DCT). The validation was conducted using a detector emulator and research reactor. As a result, we confirmed that the proposed algorithm can achieve linearity within $\pm 5\%$ of the span and response performance with a delay time of 5 ms, which are required for EISs, with a simpler configuration than a traditional EIS. Additionally, by creating a discrimination characteristics graph using pulse height information, we expect to be able to conduct the DCT in a shorter time compared with a conventional method. As for the validation of the digital algorithm, we compared the results obtained in the research reactor to simulated outputs using MATLAB Simulink. The simulated outputs align well with the values obtained from the experiment using the research reactor, and we proved that adding a time constant improves linearity.

In conclusion, the digitalization of EISs significantly contributes to reducing O&M costs. The proposed digital algorithm can satisfy the requirements for commercial power reactors and achieve a simpler configuration to improve maintenance. Furthermore, the

advanced DCT method can reduce workload. In addition, the digitalization of EISs has the potential to further reduce O&M costs and improve convenience for users. We plan to conduct further investigations to determine the potential advantages of digitalization, such as advanced pulse discrimination and condition-based monitoring. These advancements have the potential to further enhance the efficiency and effectiveness of EISs, leading to even greater cost savings and operational improvements in NPPs. This study is a crucial first step towards realizing the potential benefits of digitalizing EISs. The progressing of digitalization in EISs, based on this study, will contribute to significant advancements in the developments of NPPs and the mitigation of global warming. On the other hand, the potential disadvantages of digitalization must also be considered. One such disadvantage is the need to address electromagnetic compatibility (EMC). Digitalization can make systems more susceptible to external noise and can also introduce noise from within the system itself. While this study focused on the development and validation of digital algorithms for EISs, it is necessary to conduct EMC mitigation considerations during the stages of system design and detailed circuit design.

**Author Contributions:** R.K. and T.A. conceptualized, designed, and analyzed the system. R.K. and M.S.: software, M.H.: supervision. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research received no external funding.

**Institutional Review Board Statement:** Not applicable.

**Informed Consent Statement:** Not applicable.

**Data Availability Statement:** The raw data supporting the conclusions of this article will be made available by the authors on request.

**Acknowledgments:** The authors would like to express their sincere gratitude to Genichiro Wakabayashi, Tetuo Horiguchi, and Hiroshi Shiga for their great support of the experiment with URT-KINKI.

**Conflicts of Interest:** Authors Ryo Konishi, Makoto Sasano, Masateru Hayashi were employed by the company Advanced Technology R&D Center, Mitsubishi Electric Corporation. Author Tetsushi Azuma was employed by the company Energy System Center, Mitsubishi Electric Corporation. This research was conducted with a research fund from Mitsubishi Electric Corporation. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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