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Uniform Oxide Layer Integration in Amorphous IGZO Thin Film Transistors for Enhanced Multilevel-Cell NAND Memory Performance

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Abstract: In this work, the implementation of HfZrO layers for the tunneling, charge trapping, and blocking mechanisms within the device offer benefits in terms of programmability and data retention. This configuration has resulted in a memory device that can achieve a significant difference in threshold voltage of around 2 V per memory level. This difference is crucial for effectively distinguishing between multiple levels of memory in MLC applications. Additionally, the device operates at low programming voltages below 14 V. Furthermore, the device showcases impressive endurance and data retention capabilities, maintaining a large memory window over extended periods and under varying temperature conditions. The advancement in the a-IGZO-based memory device, characterized by its uniform oxide stacking, presents a viable solution to the industry's requirement for memory storage options that are efficient, dependable, and economical.

Keywords: homogeneous oxide stacking; multilevel-cell (MLC) NAND memory; hafnium-zirconium oxide (HfZrO); charge trap memory (CTM)



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1. Introduction

Over recent years, the evolution of amorphous indium-gallium-zinc oxide (a-IGZO)-based thin film transistors (TFTs), integrating the technology of non-volatile charge trap memory (CTM), has captivated the interest of both academic researchers and industrial practitioners [1]. The main reason for this interest lies in their unique characteristics, such as their ability to achieve high electron mobility, which allows for fast data manipulation; their capacity for optical transparency, which enables the development of transparent electronic devices; and their ability to be manufactured at low temperatures. This adaptability is particularly important for merging with pliable substrates and for the diminution of fabrication expenses. Among the most prominent features of these devices is their exceptional efficiency in programming, marked by considerable variations in threshold voltage (ΔV_{th}), a fundamental requirement for the dependable archiving and retrieval of data within memory frameworks. Extensive research has been conducted to enhance the functionality and efficiency of non-volatile memories by exploring different materials suitable for the charge trap layer, which are different from those used in the tunneling or barrier layers [2,3]. Predominantly, silicon nitride has been selected as the trapping layer [4] owing to its superior capabilities in charge trapping, whereas the construction of tunnel and barrier layers has involved a variety of metal oxides or nitride insulating materials [5]. Opting for distinct materials for each specific layer has facilitated the optimization of individual layer properties, thereby enhancing the cumulative performance of the device. However, the use of multiple materials in this approach presents certain challenges, including discrepancies at interfaces and an increase in the complexity of the manufacturing process [6,7]. Despite these challenges, the implementation of such stratified structures has demonstrably optimized manufacturing workflows within the sector, encouraging

broader acceptance of sophisticated memory technologies. On the other hand, the uniform arrangement of blocking, trapping, and tunneling layers in memory devices has historically been overlooked, mainly because it was believed that a uniform composition might not effectively promote charge trapping [8], which is crucial for the efficient functioning of memory devices. Contrary to this presumption [9], the present study introduces a novel memory device that leverages a uniform oxide stacking methodology, realized through the meticulous calibration of production parameters. Specifically, this device employs uniform HfZrO across the charge trap, blocking, and tunneling layers, facilitating the establishment of multilevel storage mechanisms within the device [10]. HfZrO is highly advantageous due to its deep trap energy levels, making it an excellent alternative to Si₃N₄. It offers improved properties compared to traditional SiO₂ tunneling layers [11,12] because of its energy band offsets and compatibility with low-temperature processing methods. The production of the blocking and tunneling layers is executed using high-temperature sputtering techniques, whereas the trapping layer is synthesized through a low-temperature procedure, ensuring the structural compatibility of the device with an extensive array of substrates [13,14]. Our examination of program/erase (P/E) dynamics showcases a substantial memory window exceeding 4.3 V, delineating the states of full erasure and programming, indicative of the data storage capacity. Furthermore, the device exhibits remarkable data retention, preserving data integrity beyond 10⁵ s, and displays durable endurance characteristics, indispensable for prolonged reliability. Additionally, operating within a low programming voltage threshold, with operational voltages remaining below 14 V, delineates this device as a power-efficient option for memory storage applications. These insights not only corroborate the practicability of fabricating flash memory devices via a homogeneous process growth strategy but also highlight the prospective utility of homogeneous stacking methods in conceptualizing future flash memory technologies. This investigation accentuates the feasibility of streamlining the fabrication process while either maintaining or amplifying the performance of memory devices and reliability, thereby broadening their application across diverse technological domains.

2. Materials and Methods

2.1. Device Fabrication

Figure 1 depicts the schematic structure of the device. The patterning process encompasses the use of traditional photolithography, wet etching, and lift-off techniques. At first, an n⁺-silicon substrate is subjected to a thorough wet etching cleansing procedure to eliminate any present surface oxides and impurities, guaranteeing a perfect base for subsequent additional layers. Subsequently, a 200-nm-thick layer of hafnium oxide (HfO₂) is applied onto the substrate as the back gate (BG) dielectric layer using radio frequency (RF) sputtering techniques. The sputtering process involves using a flow rate of 30/2 sccm of argon/oxygen gas and a working pressure of 4.7 mTorr. The temperature is set at 250 °C during this process. The selection of this method is based on its accuracy and capability to achieve uniform coverage on the substrate. The active region is defined by depositing a 50-nm-thick layer of IGZO onto the substrate using RF sputtering methods. This process involves using an argon flow rate of 20 sccm, maintaining a working pressure of 5 mTorr, and conducting the deposition at room temperature. The target contains In₂O₃, Ga₂O₃, and ZnO in a mole fraction ratio of 1:1:1. After the semiconductor layer is formed, the source and drain (S/D) contacts of the device are created by directly depositing a 200-nm-thick layer of Au/Ti onto the IGZO layer using electron beam (e-beam) evaporation. The S/D contacts are established, and then the necessary layers for tunneling, charge trapping, and blocking are created using HfZrO films with thicknesses of 5 nm, 20 nm, and 30 nm, respectively. The sputtering conditions are carefully calibrated to deposit these layers. The oxygen partial pressure is set at 3.4×10^{-4} torr, while the argon pressure is maintained at 2×10^{-3} torr. The sputtering temperature is set at 300 °C to achieve the ideal HfZrO composition. The charge trapping component is created by reducing the oxygen partial pressure to 8×10^{-5} torr, which improves the memory characteristics of the device by

producing oxygen-deficient oxides. During the last stage of production, a layer of Au/Ti with a thickness of 150 nm is applied using e-beam evaporation to create the floating gate (FG) in an environment with air. The fabricated device is subjected to conventional thermal annealing at a temperature of 400 °C for a duration of 30 min. This process is carried out to eliminate any defects present in the channel layer and gate insulating film, as well as to enhance the interface state between them. The device possesses a channel length (L) of 20 μm and a width (W) of 30 μm .

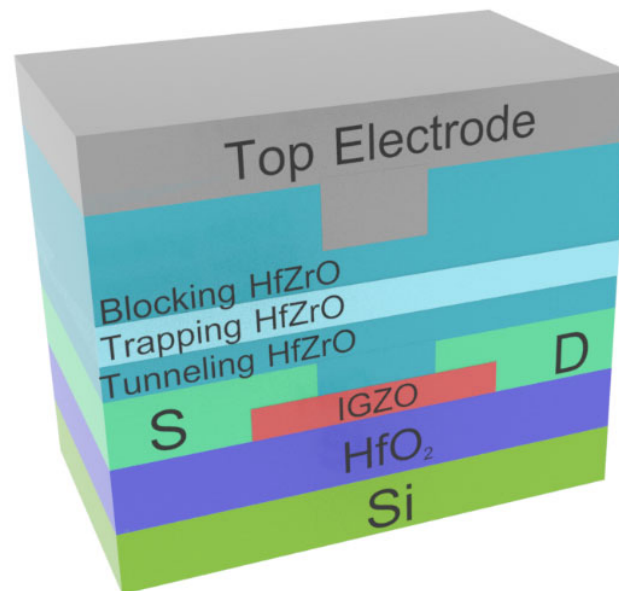


Figure 1. Detailed schematic representation of the layered architecture within the memory device.

2.2. Characterization Methods

The electrical characteristics were thoroughly analyzed using an Agilent 4156B precision semiconductor parameter analyzer. This involves applying voltage to the top gate while keeping the bottom n-doped Si substrate grounded, ensuring accurate and reliable readings. Measurements are conducted within an enclosed space devoid of external factors to prevent any outside influences. During program and erase operations, a voltage is applied to the floating gate (FG), while the bottom gate (BG) is connected to the ground.

3. Results and Discussion

In order to further explore the programming capabilities and charge retention of the recently developed memory device, a series of thorough examinations were conducted. These examinations focused on analyzing the transfer characteristic responses under different programming conditions. The device's ability to undergo significant changes in threshold voltage (ΔV_{th}) when exposed to positive and negative gate biases was examined, demonstrating its responsiveness to various electrical stimuli from the external environment. Measurements taken following short 5 ms programming pulses at various gate voltages provided a comprehensive understanding of the electrical characteristics of the device. The noticeable changes in the drain current versus gate voltage curves ($I_d - V_g$) after applying positive gate pulses highlight the sensitivity and effectiveness of the device in efficiently adjusting the threshold voltage. The increase in programming voltage leads to a concurrent escalation in ΔV_{th} , which is particularly noticeable as it rises from 11 V to 13 V. This highlights the significant level of control that can be achieved over the programming state of the device. The level of control demonstrated suggests the presence of a robust and reliable memory storage system in the device, which enables precise encoding of data by modifying the threshold voltage [15]. Conversely, the adaptability of the device in programming is further confirmed by its performance under negative gate pulses. The $I_d - V_g$ curves exhibit a shift toward the negative direction, which becomes more pro-

nounced as the negative gate bias increases. This confirms the effectiveness of the device in retaining charge, even in reverse electrical situations. The increase in ΔV_{th} from -12 V to -14 V, as shown in Figure 2b, indicates a broad operational range, allowing for flexible methods in memory programming and data archiving strategies [15]. When compared to a conventional a-IGZO TFT that does not have a specialized layer for charge storage and only has a 55 nm single-layer HfZrO as the gate dielectric, there is a significant difference in functional performance. Despite subjecting this standard device to considerably high gate biases of $+30$ V / -30 V over a prolonged ten-minute interval, negligible shifts in ΔV_{th} were observed. This pronounced absence of CTM behavior in the pure TFT configuration vividly underscores the pivotal significance of the HfZrO layer within the enhanced memory device. In the absence of this layer dedicated to charge storage, the device is incapable of sequestering and preserving a sufficient quantity of electrons necessary for satisfying memory operation prerequisites. This juxtaposition clearly accentuates the fabricated memory device's superior capabilities in charge storage and programming efficiency, ascribed to its intricately architected structure that integrates HfZrO as a layer for charge storage. Such a design not only supports the capture of electrons at high density but also guarantees consistency and reproducibility in the programming actions of the device, positioning it as a formidable contender for cutting-edge memory technology applications.

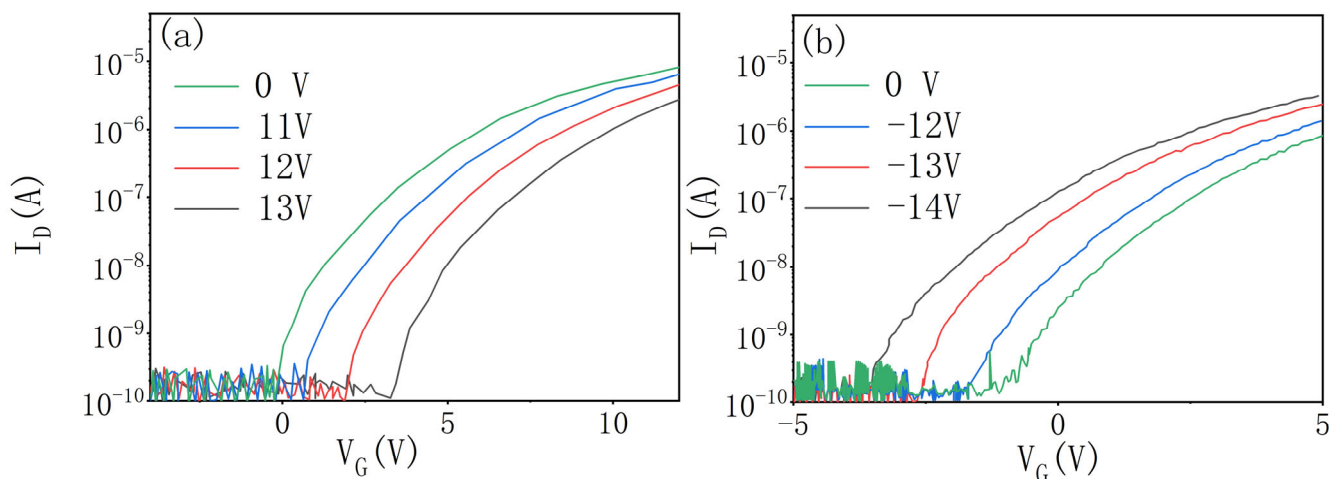


Figure 2. (a) Transfer characteristics observed when the memory device is subjected to a range of positive gate biases, applying such biases for a short programming duration of 5 ms. (b) Transfer characteristics under a spectrum of negative gate biases, also conducted over a programming time of 5 ms.

An investigation was conducted to analyze the fluctuations in threshold voltage (ΔV_{th}) associated with various programming durations, as depicted in Figure 3a. The investigation employed a range of positive voltages, specifically from 11 V to 13 V, represented by a continuous line on the chart. This revealed significant differences in ΔV_{th} across this voltage range. These discrepancies distinctly illustrate the capacity for attaining multilevel attributes within a brief timeframe, extending from 5 ms to 30 ms. This revelation indicates the practicality of deploying multilevel cells (MLCs) that necessitate shorter durations of programming, thereby augmenting both the capacity and efficiency of data storage in memory devices. An increase in the programming voltage leads to a significant increase in the amount of charge injected into the charge trapping layer, which greatly contributes to a higher ΔV_{th} . This suggests that the intensity of the programming voltage, along with the programming span, plays an integral role in bolstering the memory functionalities of the device. Precisely, prolonging the programming interval results in a commensurate rise in ΔV_{th} , owing to the aggregation of an enhanced volume of charge within the charge trapping layer. It is important to understand that achieving a desired ΔV_{th} target of 1.5 V requires different programming durations depending on the voltage polarity. A positive

voltage of 11 V can be programmed in 10 ms, while a negative voltage of -12 V requires a longer period of 30 ms. This observation highlights the exceptional programming efficiency manifested when leveraging a positive gate bias within memory devices [16].

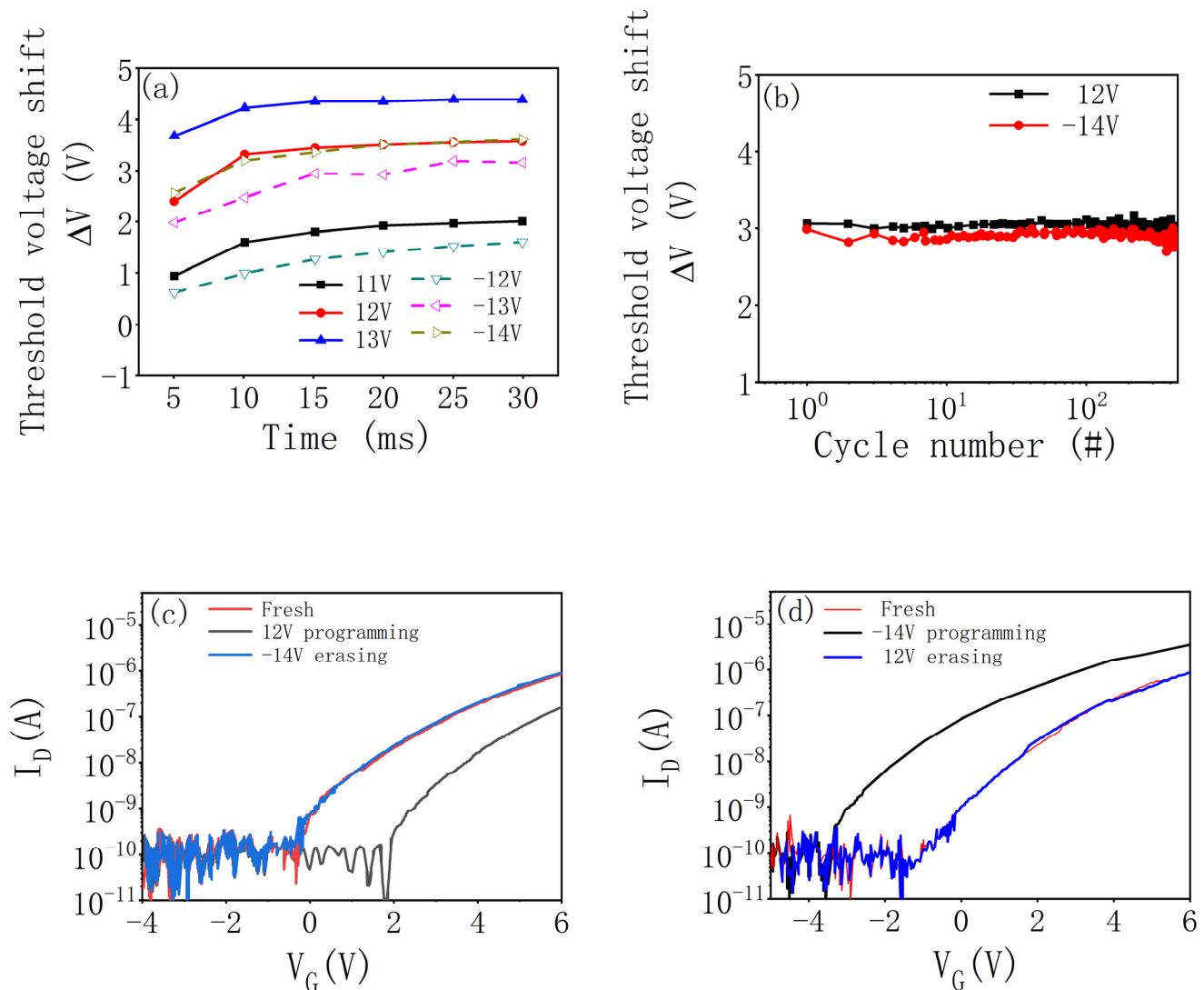


Figure 3. (a) Relationship between the threshold voltage shift (ΔV_{th}) and programming duration, with applied voltages for positive scenarios and for negative ones. (b) Relationship between the absolute value of ΔV_{th} and the quantity of programming/erasing cycles, highlighting results for both a 12 V positive voltage and a -14 V negative voltage. (c) Transfer properties of the memory unit when subjected to a programming sequence at positive 12 V, subsequently followed by an erasure process at negative 14 V. (d) Transfer properties when the memory unit is initially programmed at negative 14 V and then erased at positive 12 V.

In contexts entailing negative voltages, the necessity for both an augmented voltage and an extended duration of programming to replicate the ΔV_{th} observable under positive voltage conditions becomes apparent. This requisite predominantly stems from the intrinsic properties of IGZO as an n-type semiconductor, which impedes the conduction of holes. Consequently, this culminates in a reduction in the efficiency of negative erasure within IGZO TFT memory devices, chiefly due to a scarcity of holes within the channel layer [17]. The facilitation of hole transfer from the channel to the charge storage layer through F–N tunneling is notably hindered under a negatively biased gate. Conversely, the exposition of the device with a positive gate bias unveils its exceptional programming proficiency. For instance, maintaining a programming voltage at 12 V facilitates a notable

augmentation in ΔV_{th} , escalating from approximately 2.4 to 3.7 V as the programming period extends from 5 to 30 ms, mirroring the behavior delineated under a -14 V scenario as exhibited in Figure 3a. To further probe into the program/erase (P/E) dynamics of these memory devices, the influence of P/E cycle frequency on ΔV_{th} was meticulously evaluated. Figure 3b accentuates the results of consecutive P/E operations, where, notably, post 400 P/E cycles, the devices consistently display a stable storage window of about 3 V, irrespective of voltage polarity. This constancy serves as a testament to the devices' fluid switching faculties and their robust electronic program–erase attributes [18]. Figure 3c delineates the transfer characteristics subsequent to the application of a 12 V programming voltage for 10 ms, culminating in a ΔV_{th} of 3.2 V. Conversely, administering a -14 V negative gate pulse for an analogous duration almost restores the $I_d - V_g$ curve to its foundational state, reflective of the device's pristine condition. Moreover, as illustrated in Figure 3d, imposing a -14 V negative bias pulse on the gate for 10 ms induces a leftward deviation in the device. The subsequent application of a positive 12 V bias pulse for the identical duration remarkably reinstates the device to its original state. This observation is particularly salient as it divulges that the P/E action's duration remains uniform across both voltage polarities, furnishing substantial benefits for MLC applications predicated exclusively on voltage bias modifications [19,20].

Figure 4 presents an in-depth examination of the memory's data retention properties at both ambient and elevated temperatures (100°C), meticulously documenting how the device sustains its charge over extended periods. The investigation into retention characteristics spanned an initial duration of 10^5 s, with findings subsequently projected across a decade to ascertain the extent of charge dissipation following prolonged operational periods of the memory device. The changes in threshold voltage of the device were measured at normal room conditions for different states: unprogrammed (fresh), after programming, and after erasing. The measurements were conducted over a period of 10^5 s. In the case of unaltered devices, the variance in threshold voltage (V_{th}) remained notably insignificant throughout the retention assessment period. Conversely, for units subjected to a 12 V programming pulse for a 10-millisecond interval, a discernible contraction in the storage window was recorded, diminishing to 2.87 V in comparison to the unprogrammed state as the duration of retention progressed. Similarly, when components were subjected to a -14 V pulse for the same amount of time, the window size decreased to 2.4 V by the end of the 10^5 s evaluation. This decrease is mainly attributed to the discharge of charge from the amorphous indium-gallium-zinc oxide charge storage layer. These findings collectively underscore the flash memory's robust capacity for data preservation and its exemplary retention attributes. When subjected to a high-temperature environment (100°C), the storage window significantly decreased due to increased charge migration, which directly corresponds to a reduction in defects within the charge trapping layer. Notwithstanding the incremental diminution of the storage window as retention time extended, the device successfully maintains ample storage capacities of 4.4 V and 3.7 V after a decade (3×10^8 s) under both ambient and elevated temperature conditions, respectively. These measurements affirm the practicality of deploying such metrics within the realm of non-volatile flash memory solutions, highlighting their suitability and reliability for long-term data storage applications [21].

Figure 5a illustrates a comparison of specimens with different thickness configurations, providing insight into the complex balance needed to optimize memory device functionality by tailoring layer thickness. The engineering of the tunneling layer presents a crucial balance challenge: it needs to be thin enough to allow charge tunneling, but also thick enough to ensure good charge retention. However, excessive thinness undermines this requirement for thickness. Opting for a 5 nm thickness achieves an ideal compromise, ensuring that the tunneling layer remains adequately slender to support efficient charge transit while preserving the structural integrity vital for the device's consistent performance. The development of the blocking layer adds another dimension of complexity. It is imperative that this layer acts as a robust barrier to prevent undesirable charge injection

from the gate, necessitating both considerable thickness and superior material quality to ensure the effective insulation of the channel [19]. However, an excessively thick blocking layer might inadvertently diminish the efficacy of the electric field between the gate and channel, thus impeding the device's functional efficiency [22].

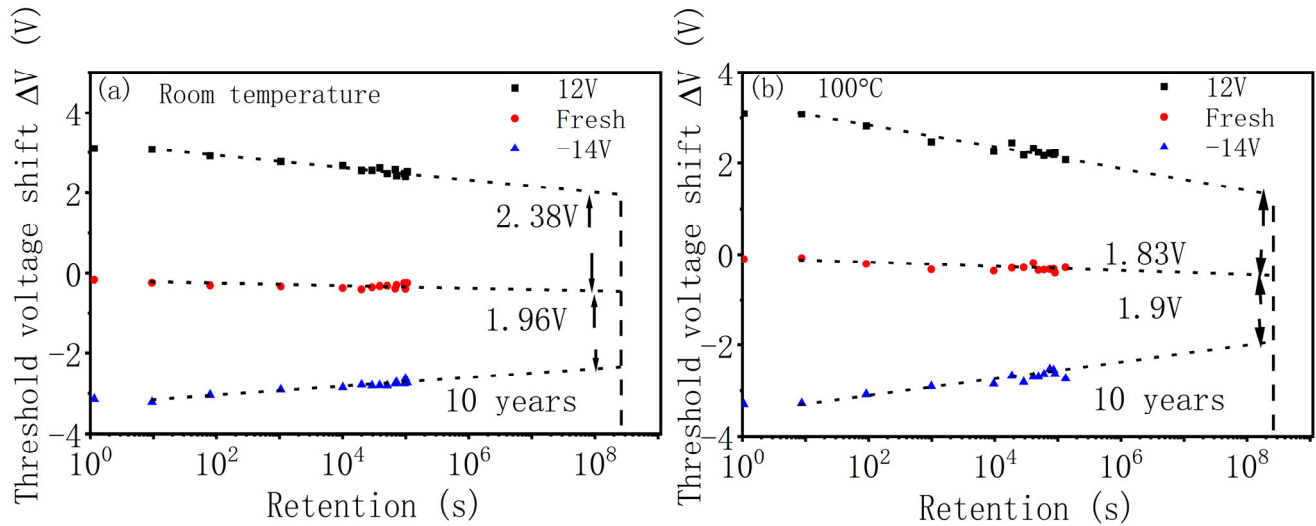


Figure 4. The retention characteristics of memory devices at (a) room temperature and (b) 100 °C.

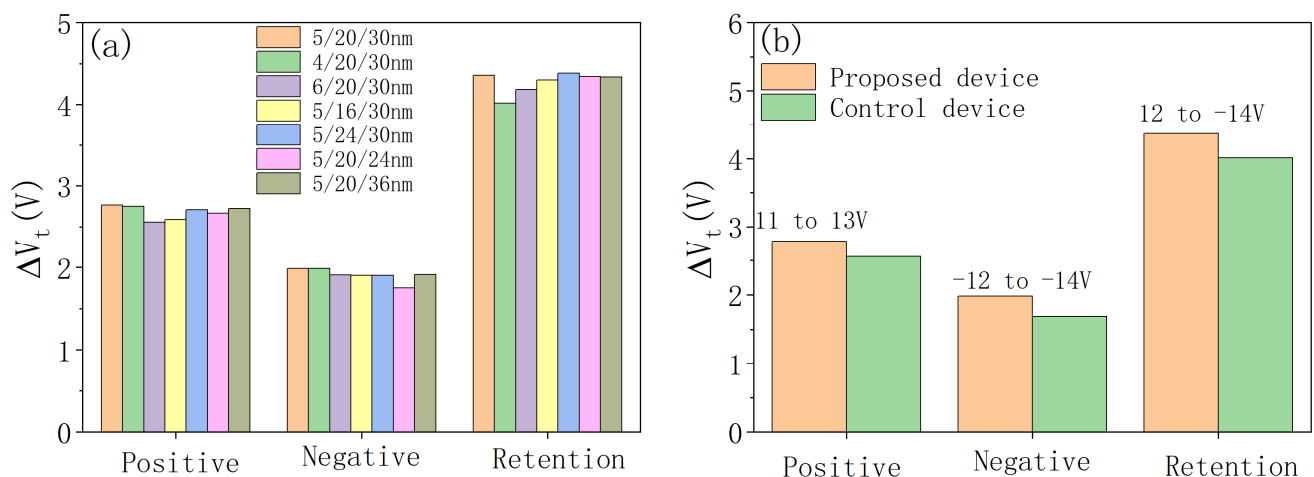


Figure 5. (a) Variations in threshold voltage for devices exposed to positive gate biases from 11 to 13 V and negative biases from −12 to −14 V over a period of 5 ms, along with the anticipated changes in threshold voltage after a decade of retention, considering layers with different thickness configurations. The configuration comprising tunneling, charge trapping, and blocking layers with thicknesses of 5 nm, 20 nm, and 30 nm, respectively, demonstrated the most optimal performance. (b) Threshold voltage shifts in both the devised and comparative control devices under the same conditions of positive and negative gate biases for 5 ms, with projections of these shifts after 10 years of retention, showcasing the enduring efficacy of the proposed device structure.

The formation of the trapping layer, particularly in environments with reduced oxygen levels, leads to a higher density of traps compared to those created in conditions with higher oxygen availability. This situation presents a clear division: increasing the number of traps can improve the memory's ability to store charge, but achieving the best conditions for sputtering without causing too many defects or leakage paths is a difficult challenge. Therefore, if the trapping layer is excessively thin, it may weaken the device's ability to prevent leakage currents, which could potentially jeopardize the stability of the entire system. After thorough deliberation, a configuration of thicknesses measuring 5/20/30 nm

was identified as the optimal choice, delivering the most harmonious performance across the device's array of operational requirements. To highlight the benefits of the memory device proposed in this research, a comparative analysis was conducted against a reference model composed of layers of 5 nm HfZrO/20 nm SiN/30 nm HfZrO. Silicon nitride (SiN) was chosen due to its proven efficacy as a charge trapping material in charge trap memory (CTM) applications [2,23]. As depicted in Figure 5b, experimental evidence supports that our proposed configuration either matches or exceeds the reference model in terms of functional performance. This comparison not only validates the advanced memory device's adept programming capabilities but also its exceptional charge storage capacity. Typically, films created in environments with lower oxygen partial pressures, thus being oxygen-deficient, tend to exhibit higher rates of defects. Although these imperfections slightly decrease the amount of current that leaks, they also encourage the formation of conductive pathways or filaments caused by the presence of oxygen vacancies. Moreover, the specific arrangement of trap energy levels in HfZrO, which are concentrated at important locations, has a significant impact on its ability to support multiple storage levels. This enhances the usefulness of HfZrO as a charge trapping medium with unique benefits. Regarding the impact of gate bias on electron behavior, the ease with which electrons in the IGZO channel's accumulation layer migrate into the charge storage layer through F-N tunneling under a positive bias is noteworthy. This process effectively secures and retains positive charges within the layer. In contrast, the intrinsic properties of a-IGZO as an n-type semiconductor complicate the dynamics of charge under negative bias; the depletion of the channel obstructs the conversion of the a-IGZO channel to the p-type [24]. Nevertheless, the reduced barrier height under such conditions still facilitates electron movement from the charge storage layer back to the IGZO channel via F-N tunneling, thus preserving the memory device's capacity for maintaining positive charge storage amidst adverse biasing scenarios.

4. Conclusions

In conclusion, the investigation of amorphous indium-gallium-zinc oxide memory technology has definitively demonstrated its strong compatibility and effectiveness for utilization in advanced multilevel-unit NAND memory applications. This device utilizes uniformly structured hafnium-zirconium oxide thin films in its key components, including the barrier layer, charge trapping layer, and tunneling layer. As a result, it provides exceptional programmability and erasability, distinguishing itself in the field of memory technologies. The use of these uniform HfZrO thin films not only simplifies the manufacturing process but also improves the device's performance in important aspects. An outstanding accomplishment of this a-IGZO memory device is its capacity to achieve substantial threshold voltage disparities, around 2 volts for every memory level, while functioning at comparatively low programming voltages, specifically below 14 volts. The ability to differentiate between different states with minimal energy consumption is crucial for the efficient functioning of multilevel NAND units. Additionally, the device exhibits strong retention properties, guaranteeing that data remain stable and can be retrieved over long periods of time. This is crucial for dependable memory storage solutions. Moreover, the uniform composition of the oxide stack employed in this device not only streamlines the manufacturing process but also enhances the compatibility of materials, making it advantageous for incorporating the memory technology into different electronic platforms. The use of a consistent material composition throughout the layers of the device simplifies the processing, resulting in reduced production complexities and costs. This makes it a more appealing choice for large-scale manufacturing. Moreover, the homogeneous oxide stack's compatibility with established semiconductor technologies enables the smooth incorporation of a-IGZO memory into present electronic systems, broadening its potential applications in various industries. This research highlights the considerable capacity of a-IGZO memory devices to advance the field of NAND memory technology. The utilization of low operational voltages, coupled with a significant distinction between memory states

and the guarantee of data stability, results in the emergence of a-IGZO memory as a highly promising solution for future memory storage requirements. This technology offers a combination of efficiency, reliability, and compatibility that effectively fulfills the demands of contemporary electronic devices.

Supplementary Materials: The following supporting information can be downloaded at: <https://www.mdpi.com/article/10.3390/app14062588/s1>.

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