

Article

Interleaved Modified SEPIC Converters with Soft Switching and High Power Factor for LED Lighting Appliance

Hung-Liang Cheng , Chun-An Cheng , Chien-Hsuan Chang , En-Chih Chang, Lain-Chyr Hwang * and Yi-Chan Hung

Department of Electrical Engineering, I-Shou University, Kaohsiung City 84001, Taiwan; hlcheng@isu.edu.tw (H.-L.C.); cacheng@isu.edu.tw (C.-A.C.); chchang@isu.edu.tw (C.-H.C.); enchihschang@isu.edu.tw (E.-C.C.); isu11101010m@cloud.isu.edu.tw (Y.-C.H.)

* Correspondence: lain@isu.edu.tw

Abstract: A novel ac/dc LED driver with power factor correction and soft-switching functions is proposed. The circuit topology mainly consists of two modified single-ended primary inductance converters (SEPIC) with interleaved operation. The first half stage of SEPIC operates like a boost converter and the second half stage operates like a buck–boost converter. Each boost converter is designed to operate in discontinuous current mode (DCM) to function as a power factor corrector (PFC). The two buck–boost converters that share a commonly coupled inductor are designed to operate at near boundary conduction mode (BCM). Without using any active clamping circuit, auxiliary switch or snubber circuit, the active switches can achieve zero-voltage switching on, and all diodes achieve zero-current switching off. First, operation modes in steady state are analyzed, and the mathematical equations for design component parameters are derived. Finally, a prototype circuit of 180 W rated power was built and tested. Experimental results show satisfactory performance of the proposed circuit.

Keywords: ac/dc converter; interleaved converter; power factor corrector (PFC); single stage; soft switching



Citation: Cheng, H.-L.; Cheng, C.-A.; Chang, C.-H.; Chang, E.-C.; Hwang, L.-C.; Hung, Y.-C. Interleaved Modified SEPIC Converters with Soft Switching and High Power Factor for LED Lighting Appliance. *Appl. Sci.* **2024**, *14*, 6656. <https://doi.org/10.3390/app14156656>

Academic Editor: Sang Hyuk Im

Received: 28 May 2024

Revised: 22 July 2024

Accepted: 25 July 2024

Published: 30 July 2024



Copyright: © 2024 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

A light-emitting diode (LED) has the advantages of small size, high energy efficiency, long service life, fast response time, good color rendering, environmental friendliness, etc. Nowadays, LEDs have gradually replaced fluorescent lamps and high-intensity gas discharge lamps, and have been widely used in various lighting systems [1–4].

When the input voltage is an ac line voltage source, a large capacitor filter needs to be installed after the rectifier circuit to reduce the ripple of the rectified dc voltage. Since the diode of the rectifier circuit only conducts when the ac voltage is higher than the dc voltage. The conduction time is very short, and the input current is a large pulse inrush current. This results in a low power factor and high total harmonic distortion of current (THDi) [5]. High-order harmonic currents can interfere with control circuits or communication systems and cause malfunctions in measuring instruments and electrical protection equipment. Therefore, advanced countries have formulated strict specifications, such as IEC 61000-3-2 [6] and IEEE 519 [7] to regulate the power factor and THDi of electrical products [8,9]. In order to meet the specifications of power factor and THDi, a power factor corrector (PFC) should be added in front of the original ac/dc converter, so that the LED drivers have a two-stage circuit architecture [10,11]. In order to improve the shortcomings of using more components in a two-stage converter and to reduce the number of energy transfer times in the converter and thereby improve the circuit efficiency, researchers have developed a number of single-stage LED drivers in which the active switches and control circuit are shared by a PFC converter and a dc/dc converter [12–17]. However, in order to serve

as switches for both the PFC converter and the DC/DC converter, some shared switches operate in hard switching.

Hard switching means that the switch cannot operate at zero-voltage switching on (ZVS) or zero-current switching off (ZCS). For active switches, if they cannot operate at ZVS, their parasitic capacitance will generate huge spike currents due to an instant short circuit when they are turned on, and the energy originally stored in the parasitic capacitance will be dissipated inside the switches. For diodes, if they cannot operate at ZCS, a reverse recovery current will be generated when the diodes are turned off. In other words, in addition to huge switching losses, hard switching is also accompanied by high current and high voltage stress. Therefore, hard switching circuits must use switches with high voltage/current specifications to reduce their failure rate. Without the use of higher specification components, the LED drivers with hard switching can only be used in low-power products. The literature [18–20] proposed LED drivers with single-stage topologies. Although they can achieve a high power factor, their energy conversion efficiency is not high because the active switches cannot meet ZVS operation, so they are only suitable for low-power products (9–50 W). In order to solve the hard-switching problem, pulse-width modulation (PWM) converters usually use active clamping or snubber circuits to implement ZVS and/or ZCS [21–24]. However, these soft-switching techniques require the use of additional auxiliary switches, diodes, inductors, and capacitors, which increases circuit costs. In addition, current loops in active clamping or snubber circuits generate additional conduction losses, thereby reducing circuit efficiency. In the literature [25–28], a single-stage topology is obtained by integrating a PWM converter and a resonant converter, where the PWM converter is used as the PFC circuit and the full-bridge or half-bridge resonant converter is used as the DC/DC converter. The resonant converter not only has the advantage of galvanic isolation. By designing the switching frequency to be greater than the resonant frequency of the resonant tank, the resonant tank will present an inductive load, and the active switches can operate at ZVS. However, the resonant converter requires additional rectifier and filter circuits to obtain a smooth DC output voltage, which not only increases the component count but also causes more conduction losses.

This paper proposes an ac/dc converter to drive high-power LEDs, which is obtained by modifying two single-ended primary inductance converters (SEPIC) with interleaved operation. The proposed circuit achieves a high power factor and low THDi and the switch meets soft switching. The other content of this paper is organized as follows. Section 2 proposes the circuit topology and analyzes the steady-state operation mode in detail; Section 3 deduces the mathematical equations for designing circuit component parameters; Section 4 designs, manufactures and experimentally measures the 180 W prototype circuit. Finally, some conclusions are made in Section 5.

2. Proposed LED Driver and Analysis of Steady-State Operation

2.1. Circuit Topology

Figure 1 shows the circuit topology of the high-power factor ac/dc LED driver proposed in this paper. The circuit consists of a low-pass filter (L_f , C_f), a bridge rectifier (D_{r1} – D_{r4}), and two modified SEPIC circuits. One SEPIC circuit includes inductor L_{p1} , diode D_1 , active switch S_1 , dc-link capacitor C_{B1} , flywheel diode D_3 and the primary winding of the coupled inductor T_1 , and the other includes inductor L_{p2} , diode D_2 , active switch S_2 , dc-link capacitor C_{B2} , flywheel diode D_4 and secondary winding of T_1 . Diodes D_{S1} and D_{S2} are the intrinsic body diodes of S_1 and S_2 , respectively. Figure 2 shows the control voltages (v_{GS1} , v_{GS2}) of S_1 and S_2 . They are both square wave voltages with a phase difference of 180 degrees and partially overlap, i.e., both S_1 and S_2 are in conduction for a certain period of time.

Typically, a SEPIC circuit is a single-stage topology using only one active switch. The first half stage of the SEPIC circuit operates like a boost converter and the second half operates like a buck–boost converter. Compared with the traditional two parallel SEPIC circuits, the circuit proposed in this paper has two differences. The first is the addition of

two diodes (D_1, D_2) to avoid the currents in L_{p1} and L_{p2} flowing in the opposite direction. If i_{p1} and i_{p2} have reverse currents, the power factor correction performance will be impaired, and some excess conduction loss will occur. The second point is to use a coupled inductor T_1 instead of two separate inductors for the second half stage of the two SEPIC circuits. T_1 consists of an iron core and two windings with the same number of turns. Unlike traditional SEPIC circuits, which require additional components to enable ZVS operation for active switches. The winding current of the coupled inductor is designed to operate close to the boundary conduction mode (BCM). Based on the principle of magnetomotive force balance, the mutual inductance current will be converted between the two windings and the winding current is used to discharge the store charges in the parasitic capacitance of the active switch to fulfill ZVS operation.

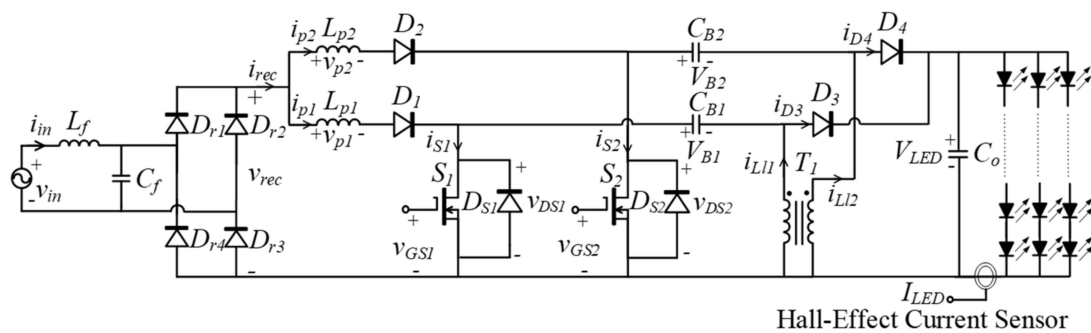


Figure 1. Proposed LED driver.

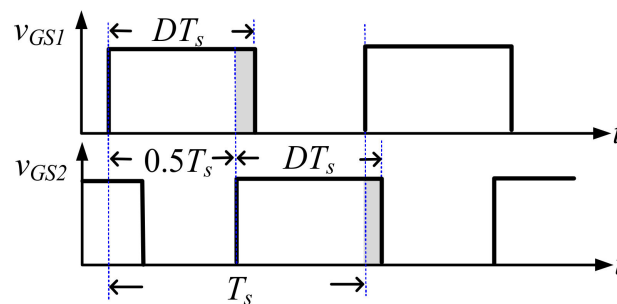


Figure 2. Gate-to-source voltages of S_1 and S_2 .

2.2. Analysis of Operation Mode

The following assumptions are made to simplify the circuit analysis.

- (1) In order to ensure ZCS operation for all diodes, the currents of L_{p1} and L_{p2} are designed to operate in discontinuous-current mode (DCM), and the winding currents of T_1 are all designed to decrease to zero amps.
- (2) All components are considered ideal except for the parasitic capacitance (C_{S1} and C_{S2}) and intrinsic diodes (D_{S1} and D_{S2}) of the S_1 and S_2 .
- (3) The two SEPIC circuits are identical with $L_{p1} = L_{p2} = L_p$, $C_{B1} = C_{B2} = C_B$, $V_{B1} = V_{B2} = V_B$.
- (4) Capacitors C_{B1} , C_{B2} , and C_o are large enough that the voltages across them (V_{B1} , V_{B2} , and V_o) can be regarded as constant.
- (5) The winding resistance and iron loss of T_1 are neglected. The leakage inductance in the primary and secondary windings are equal ($L_{l1} = L_{l2} = L_l$), and the mutual inductance L_m is large enough so that the mutual inductance current is regarded as a constant I_{Lm} .
- (6) S_1 and S_2 are turned on and off at a high frequency (f_s) well above the input line frequency (f_L). Therefore, the rectified input voltage can be regarded as a constant value in each high-frequency cycle.

In steady-state operation, the circuit can be divided into 10 operation modes in each high-frequency cycle according to the status of each component. Figure 3 shows the equivalent circuits for each operation mode, where v_{rec} denotes the voltage after the bridge rectification and R_o denotes the equivalent resistance of the LEDs. In Figure 3, T_1 is represented by a transformer model, where L_{l1} and L_{l2} are leakage inductances and v_T is the voltage across the mutual inductance. For a coupled inductor, the following equation can be derived [29].

$$i_{Ll1} + i_{Ll2} = i_{Lm}, \quad (1)$$

$$v_T = \frac{L_m di_{Lm}}{dt}, \quad (2)$$

Applying Faraday's law to the leakage inductances gives

$$v_{Ll1} + v_{Ll2} = \frac{L_{l1} di_{Ll1}}{dt} + \frac{L_{l2} di_{Ll2}}{dt} = \frac{L_l di_{Lm}}{dt}, \quad (3)$$

Figure 4 shows the schematic waveforms of voltage and current of the main components. The following section describes the details of each operation mode and the derivation of the associated equations.

Before operation Mode 1, both S_1 and S_2 are on. Since S_2 is turned on before S_1 , most of the mutual inductance current i_{Lm} flows in the secondary winding of T_1 through S_2 , that is, $i_{Ll2} \gg i_{Ll1}$. When v_{GS2} changes from high level to low level, S_2 is turned off and the circuit enters operation Mode 1.

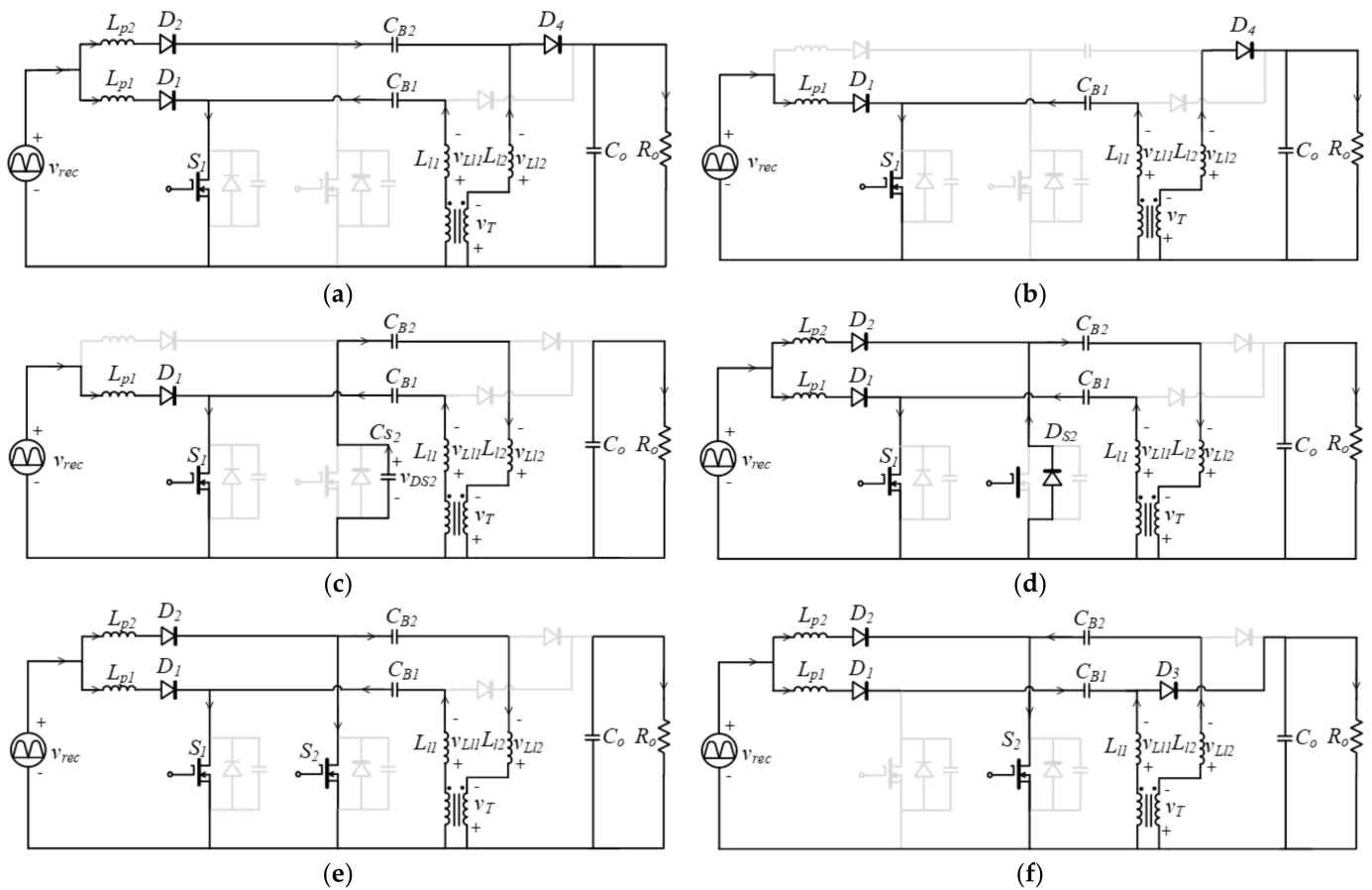


Figure 3. Cont.

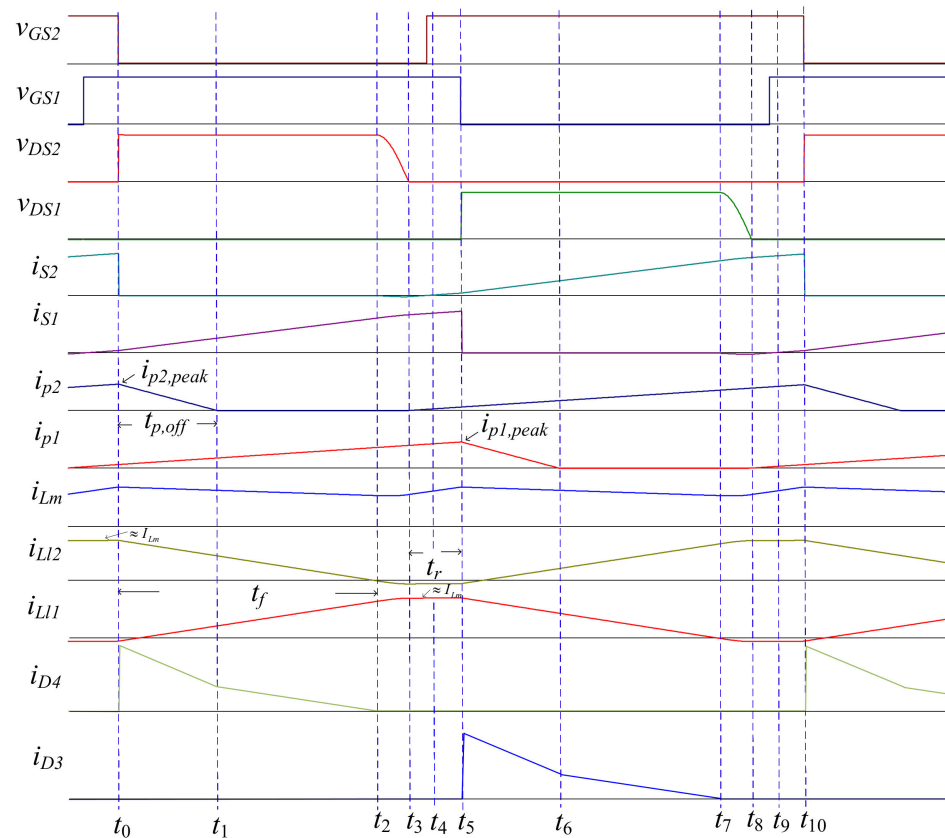
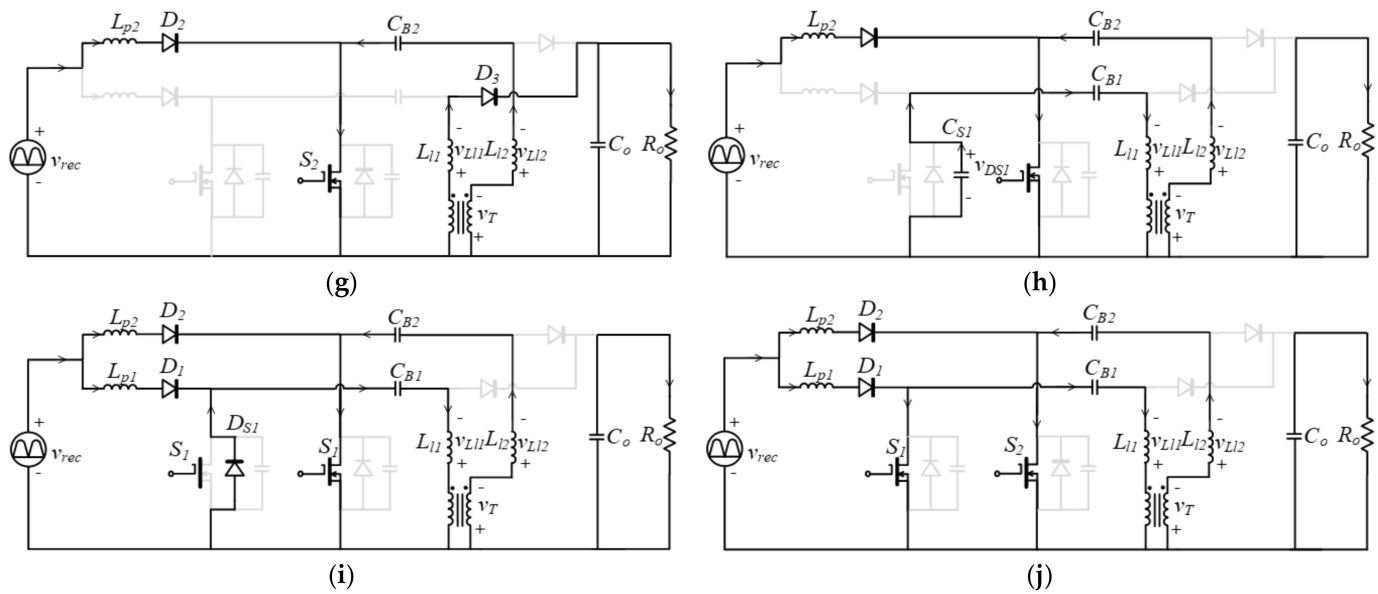


Figure 4. Schematic waveforms.

2.2.1. Operation Mode 1 ($t_0 < t < t_1$)

At the moment before S_2 is turned off, i_{p2} reaches a peak value, denoted as $i_{p2,peak}$. When S_2 is turned off, i_{p2} flows through D_2 to charge C_{S2} , and i_{LI2} also flows into C_{B2} to charge C_{S2} . In practice, the parasitic capacitance is very small. C_{S2} will be quickly charged to $V_B + V_o$. After that, i_{p2} will flow through D_2 , C_{B2} , D_4 , and C_o , while i_{LI2} will flow through

D_4 and C_o , as shown in Figure 3a. The voltages and current equations for L_{p1} and L_{p2} are as follows.

$$v_{p1}(t) = v_{rec}, \quad (4)$$

$$i_{p1}(t) = i_{p1}(t_0) + \frac{v_{rec}}{L_p}(t - t_0), \quad (5)$$

$$v_{p2}(t) = -V_B - V_o + v_{rec}, \quad (6)$$

$$i_{p2}(t) = i_{p2,peak} - \frac{(V_B + V_o - v_{rec})}{L_p}(t - t_0), \quad (7)$$

The current i_{p1} keeps increasing linearly while i_{p2} starts to decrease linearly.

From Figure 3a, the voltage equations of the primary and secondary windings of T_1 are expressed as (8) and (9), respectively.

$$v_{Ll1} + v_T = V_B, \quad (8)$$

$$v_{Ll2} + v_T + V_o = 0, \quad (9)$$

Adding (8) and (9) gives

$$v_{Ll1} + v_{Ll2} + 2v_T = V_B - V_o, \quad (10)$$

Substituting (2) and (3) into (10) yields

$$v_T = \frac{L_m}{L_l + 2L_m}(V_B - V_o), \quad (11)$$

Substituting (11) into (8) and (9), respectively, the leakage inductance voltages can be expressed as follows.

$$v_{Ll1} = \frac{(L_m + L_l)V_B + L_m V_o}{L_l + 2L_m}, \quad (12)$$

$$v_{Ll2} = \frac{-L_m V_B - (L_m + L_l)V_o}{L_l + 2L_m}, \quad (13)$$

Equation (12) shows that v_{Ll1} is positive, so i_{Ll1} starts to rise from a negative value close to zero. After a period of time, i_{Ll1} rises to become positive. Equation (13) shows that v_{Ll2} is negative, and i_{Ll2} starts to decrease from the peak value. In other words, when S_2 is turned off, i_{Ll2} decreases and i_{Ll1} increases, that is, the current originally flowing through the secondary winding of T_1 gradually converts to flow through the primary winding.

The boost converters would be designed to operate in DCM. When i_{p2} declines to zero, D_2 turns off and the circuit enters the next operation mode.

2.2.2. Operation Mode 2 ($t_1 < t < t_2$)

In this mode, the equivalent circuit is shown in Figure 3b. The current i_{p2} remains zero. Equations (4), (5), and (8)–(13) remain unchanged. Therefore, i_{p1} and i_{Ll1} continue to rise, and i_{Ll2} continues to fall. When i_{Ll2} decreases to zero, D_4 turns off and the circuit enters the next operation mode.

2.2.3. Operation Mode 3 ($t_2 < t < t_3$)

In this mode, i_{p2} remains zero while i_{p1} keeps increasing. This mode is the process of discharging C_{S2} from high voltage to zero volts. As shown in Figure 3c, v_{Ll1} and v_{Ll2} can be expressed as follows.

$$v_{Ll1} = V_B - v_T, \quad (14)$$

$$v_{Ll2} = V_B - v_T - v_{DS2}, \quad (15)$$

Adding (14) and (15) gives

$$v_{Ll1} + v_{Ll2} = 2V_B - 2v_T - v_{DS2}, \quad (16)$$

Substituting (2) and (3) into (16) yields

$$v_T = \frac{L_m}{L_l + 2L_m}(2V_B - v_{DS2}), \quad (17)$$

Substituting (17) into (14) and (15) respectively, v_{Ll1} and v_{Ll2} can be expressed as follows.

$$v_{Ll1} = \frac{L_l V_B + L_m v_{DS2}}{L_l + 2L_m}, \quad (18)$$

$$v_{Ll2} = \frac{L_l V_B - (L_m + L_l)v_{DS2}}{L_l + 2L_m}, \quad (19)$$

At the beginning of this mode, v_{DS2} is equal to $V_B + V_o$, (18) and (19) show that v_{Ll1} is positive, and v_{Ll2} is negative. The current i_{Ll1} keeps on rising. On the contrary, i_{Ll2} continues to decrease and becomes negative, i.e., the secondary winding current is reversed, and at this time, T_1 acts as a transformer. During the discharge of C_{S2} , v_{DS2} decreases. Observing (17)–(19), it can be known that v_T and v_{Ll2} increase, and v_{Ll1} decreases. When C_{S2} discharges to zero volts, D_{S2} turns on and the circuit enters operation Mode 4.

2.2.4. Operation Mode 4 ($t_3 < t < t_4$)

Figure 3d shows the equivalent circuit of operation Mode 4. The voltage and current equations of L_{p2} are

$$v_{p2}(t) = v_{rec}, \quad (20)$$

$$i_{p2}(t) = \frac{v_{rec}}{L_p}(t - t_3), \quad (21)$$

The current i_{p2} starts to rise from zero. The voltage equations of the primary and secondary windings of T_1 are

$$v_{Ll1} + v_T = V_B, \quad (22)$$

$$v_{Ll2} + v_T = V_B, \quad (23)$$

Adding (22) and (23) gives

$$v_{Ll1} + v_{Ll2} + 2v_T = 2V_B, \quad (24)$$

Substituting (2) and (3) into (24) yields

$$v_T = \frac{2L_m}{L_l + 2L_m}V_B, \quad (25)$$

Substituting (25) into (22) and (23), respectively, v_{Ll1} and v_{Ll2} can be expressed as follows.

$$v_{Ll1} = v_{Ll2} = \frac{L_l}{L_l + 2L_m}V_B, \quad (26)$$

Equations (25) and (26) show that v_T is positive, and v_{Ll1} and v_{Ll2} are also positive and equal, therefore, i_{Lm} , i_{Ll1} and i_{Ll2} all rise. Because L_m is much larger than L_l , (26) shows that v_{Ll1} and v_{Ll2} are very small, therefore, i_{Ll1} and i_{Ll2} rise slowly.

Observing Figure 3d, it can be noticed that i_{Ll2} has two current paths, one is C_{B2} – T_1 secondary winding– D_{S2} , and the other is C_{B2} – T_1 secondary winding– v_{rec} – L_{p2} – D_2 . Before i_{Ll2} rises from negative to zero, v_{GS2} changes from low level to high level. Because i_{Ll2} is negative, its absolute value becomes smaller during the rise process. At first, the absolute value of i_{Ll2} is larger than i_{p2} . When i_{p2} rises to become larger than the absolute value of i_{Ll2} , S_2 would be turned on and the circuit enters operation Mode 5.

2.2.5. Operation Mode 5 ($t_4 < t < t_5$)

Figure 3e shows the equivalent circuit of this mode. Because D_{S2} is in the on-state before S_2 is turned on, it clamps v_{DS2} at zero volts, therefore S_2 satisfies ZVS. In this mode, i_{p2} has two current loops, which are L_{p2} – D_2 – C_{B2} – T_1 secondary winding– v_{rec} , and L_{p2} – D_2 – S_2 – v_{rec} . D_{S2} is on when the circuit is operating in mode 4 and S_2 is on when the circuit is operating in mode 5. Whether D_{S2} is on or S_2 is on, v_{DS2} is equal to zero volts, so the voltage and current equations for Mode 5 are identical to Mode 4. Hence, i_{p1} and i_{p2} all continue to rise. When v_{GS1} changes from high level to low level, S_1 is turned off and the circuit enters operation Mode 6.

2.2.6. Operation Mode 6 ($t_5 < t < t_6$) ~ Operation Mode 10 ($t_9 < t < t_{10}$)

Figure 3f–j show the equivalent circuits of Mode 6 to Mode 10. The circuit operation principles of Mode 6 to Mode 10 are similar to those of Mode 1 to Mode 5 and will not be described again here. When v_{GS2} changes from high level to low level, S_2 is turned off, and the circuit enters the next high-frequency cycle of operation Mode 1.

3. Mathematical Equations for Parameters Design

3.1. Boost-Typed PFC Converter

From the analysis of the operation mode, it can be known that the voltage across L_{p1} (L_{p2}) is equal to v_{rec} when S_1 (S_2) is on. On the contrary, when S_1 (S_2) is turned off, L_{p1} (L_{p2}) transfers the stored energy to C_{B1} (C_{B2}) and C_o . L_{p1} (L_{p2}) is served as the inductor of a boost converter. In order for the boost converter to operate in DCM throughout the input voltage cycle, $V_B + V_o$ must be high enough to satisfy the following equation.

$$V_B + V_o \geq \frac{V_m}{1-D}, \quad (27)$$

First, k is defined as

$$k \triangleq V_B + V_o / V_m, \quad (28)$$

When the value of k is greater than 2, the power factor can reach more than 0.98 and the output power can be expressed as [30]

$$P_o = \frac{\eta D^2 V_m^2}{L_p f_s} \cdot y, \quad (29)$$

where η represents the circuit efficiency and y is expressed as

$$y = \int_0^\pi \frac{\sin^2 \theta}{1 - \frac{1}{k} \sin \theta} d\theta = \frac{k^3}{\sqrt{k^2 - 1}} \left(1 + \frac{2}{\pi} \sin^{-1} \frac{1}{k} \right) - k^2 - \frac{2}{\pi} \cdot k, \quad (30)$$

3.2. Buck–Boost Converter

Based on the previous assumptions, i_{Lm} can be regarded as a constant value I_{Lm} when L_m is sufficiently large. During Mode 1 and Mode 2, i_{L1} rises and i_{L2} decreases, and it is known that the increase in i_{L1} is equal to the decrease in i_{L2} by (1). Mode 3 describes the process in which the parasitic capacitance of S_2 is discharged from $V_B + V_o$ to zero volts. Because C_{S2} is very small and the drop in i_{L2} is also very small, therefore, at the end of Mode 3, i_{L2} is negative but almost equal to zero. Thus, it is known that the peaks of i_{L1} and i_{L2} are very close to I_{Lm} .

$$i_{L1,peak} = i_{L2,peak} \approx I_{Lm}, \quad (31)$$

Operation Mode 2 ends when i_{L2} decreases to zero. Using (13) and (31), the time required for i_{L2} to decrease from the peak value to zero is equal to

$$t_f = t_2 - t_0 \approx \frac{I_{Lm} L_l (L_l + 2L_m)}{L_m V_B + (L_m + L_l) V_o}, \quad (32)$$

During the period from Mode 1 to Mode 2, v_T is negative and i_{Lm} decreases. On the contrary, during the period from Mode 3 to Mode 5, v_T is positive and i_{Lm} increases. Applying the volt-second balance law of inductance, the average value of v_T is equal to zero. From (11) and (25), we can obtain

$$\overline{v_T} = \frac{L_m (V_B - V_o)}{L_l + 2L_m} \cdot t_f + \frac{2L_m V_B}{L_l + 2L_m} \cdot t_r = 0, \quad (33)$$

where t_r represents the rising time of i_{Lm} . Ignoring the short charging and discharging time of C_{S1} (C_{S2}), we can obtain

$$t_f + t_r \approx 0.5 T_s, \quad (34)$$

Combining (33) and (34), it can be deduced that t_f and t_r are, respectively, expressed as

$$t_f = \frac{V_B}{V_B + V_o} T_s, \quad (35)$$

$$t_r = \left(0.5 - \frac{V_B}{V_B + V_o} \right) T_s, \quad (36)$$

Because both t_r and t_f must be positive values, it can be seen from (36) that the design constraint for realizing the converter proposed in this study is that

$$V_o > V_B, \quad (37)$$

Substituting (35) into (32) yields

$$I_{Lm} = \frac{V_B (L_m V_B + (L_m + L_l) V_o)}{L_l (L_l + 2L_m) (V_B + V_o)} T_s, \quad (38)$$

From the analysis of the operation modes, it can be seen that the output power comes from two paths. One is that L_{p1} (L_{p2}) directly provides energy to the output terminal through D_3 (D_4). The other is that L_{p1} (L_{p2}) first charges C_{B1} (C_{B2}) through D_3 (D_4), and then C_{B1} (C_{B2}) provides energy to the output terminal. The power supplied to the output terminal by each of these two paths is equal to

$$P_1 = \frac{P_o V_o}{(V_B + V_o)}, \quad (39)$$

$$P_2 = \frac{P_o V_B}{(V_B + V_o)}, \quad (40)$$

For a buck-boost converter, when the active switch is turned off, the inductor current flows through the flywheel diode and releases energy to the output. Combining (35) and (38) yields that the average of the descending portions of i_{L1} and i_{L2} added together is equal to

$$\overline{i_{L1, fall}} + \overline{i_{L2, fall}} = 2 \times \frac{t_f I_{Lm}}{2T_s} = \frac{V_B^2 (L_m V_B + (L_m + L_l) V_o)}{L_l (L_l + 2L_m) (V_B + V_o)^2 f_s}, \quad (41)$$

Equation (41) represents the average current delivered to the output by the buck–boost converters. Combining (40) and (41) yields

$$\frac{V_B(L_m V_B + (L_m + L_l)V_o)}{L_l(L_l + 2L_m)(V_B + V_o)f_s} = \frac{P_o}{V_o}, \quad (42)$$

The coupling coefficient of the coupled inductor is defined as

$$k_c \triangleq \frac{L_m}{L_l + L_m}, \quad (43)$$

Combining (42) and (43) yields

$$L_l = \frac{V_B V_o (k_c V_B + V_o)}{(1 + k_c)(V_B + V_o)P_o f_s}, \quad (44)$$

4. Parameters Design and Experimental Results

A 180 W prototype LED driver was built and tested to demonstrate the feasibility of the proposed circuit. The specification of the proposed LED driver is listed in Table 1. The input supply voltage presented in the article is $110 \text{ V}_{\text{rms}} \pm 10\%$, not universal voltage ($85\text{--}264 \text{ V}_{\text{rms}}$). Equation (45) shows the design constraint for the dc-link voltage and the output voltage. The higher the input voltage, the higher the dc-link voltage and the output voltage should be. Compared with other loads, the voltage of each LED is very small. High output voltage means a considerable number of LEDs per string. When there are too many LEDs per string, the design range of the output-rated power will be limited. The load consists of three LED strings connected in parallel, each string consisting of sixty 1 W LEDs. The rated voltage and current of each LED are 3.6 V and 0.28 A, respectively.

Table 1. Specification of the proposed LED driver.

Item	Value
Input voltage, V_{in}	$110 \pm 10\% \text{ V}_{\text{rms}}, 60 \text{ Hz}$
Output voltage, V_{LED}	216 V ($60 \times 3.6 \text{ V}$)
Output current, V_{LED}	0.84 A ($3 \times 0.28 \text{ A}$)
Output power, P_o	180 W
Switching frequency, f_s (at rated power)	50 kHz

4.1. Parameters Design

The considerations and calculations of component parameters are as follows.

A. Choose duty ratio and dc-link voltage.

As shown in Figure 2, the gate–source voltages of S_1 and S_2 should briefly overlap when they are at high levels, that is, the duty cycle is slightly higher than 0.5. However, a high-duty cycle requires a higher dc-link voltage for the PFC converter to operate in DCM. Here, the duty ratio is chosen to be 0.54.

$$D = 0.54$$

The design constraint for dc-link voltage can be obtained by combining (27) and (37), as follows.

$$V_o > V_B > \frac{V_m}{1 - D} - V_o, \quad (45)$$

Considering the 10% variation in the input voltage, the applicable range of the dc-link voltage is calculated as

$$216 > V_B > \frac{110\sqrt{2} \times 1.1}{1 - 0.54} - 216 = 156 \text{ V}$$

Here, the dc-link voltage is chosen to be

$$V_B = 160 \text{ V}$$

B. Calculate PFC inductance.

First, calculate the value of k and the value of y using (28) and (30) in sequence.

$$k = \frac{160 + 216}{110 \times \sqrt{2}} = 2.42$$

$$y = \frac{(2.42)^3}{\sqrt{(2.42)^2 - 1}} \left(1 + \frac{2}{\pi} \sin^{-1} \frac{1}{2.42} \right) - (2.42)^2 - \frac{2}{\pi} \times 2.42 = 0.78$$

Assuming a circuit efficiency of 95%, the PFC inductance can be calculated by using (29).

$$L_p = \frac{0.95 \times (0.54)^2 \times (110 \times \sqrt{2})^2}{180 \times 50 \times 10^3} \times 0.78 = 0.58 \text{ mH}$$

C. Determine the leakage inductance and the mutual inductance of T_1 .

Selecting a coupling coefficient of 0.9, the leakage inductance can be calculated by using (44).

$$L_l = \frac{0.95 \times 160 \times 216 \times (0.9 \times 160 + 216)}{(1 + 0.9) \times (160 + 216) \times 180 \times 50 \times 10^3} = 1.84 \text{ mH}$$

Then, the mutual inductance is calculated to be

$$L_m = 16.54 \text{ mH}$$

4.2. Experimental Results

Table 2 shows the component parameters of the prototype LED driver. In practice, it is not easy to produce a coupled inductor whose mutual inductance and leakage inductance meet the design values at the same time. Therefore, in this prototype circuit, first, a coupled inductor with a mutual inductance equal to 16.54 mH was implemented, and then two small inductors were, respectively, connected in series with the two windings of this coupled inductor. In addition, the sum of the leakage inductance of the coupled inductor and the inductance of each small inductor is equal to 1.84 mH.

Table 2. Component parameter.

Item	Value
Low-pass filter L_f, C_f	$L_f = 0.5 \text{ mH}, C_f = 2 \text{ } \mu\text{F}$
Diodes $D_{r1}-D_{r4}$	MUR460
Diodes D_1-D_2	C3D10060A
PFC inductance L_{p1}, L_{p2}	0.58 mH
DC-link capacitance C_{B1}, C_{B2}	100 μF
Mutual inductance L_m	16.54 mH
Leakage inductance L_{l1}, L_{l2}	1.84 mH
Output capacitance C_o	100 μF
Active switches S_1, S_2	IPW65R080CFD

Figure 5 shows the control voltages of the two active switches. As shown in the figure, the duty cycles of v_{GS1} and v_{GS2} both exceed 0.5, so both S_1 and S_2 are in a conductive state for a certain period of time. Figure 6a shows the inductor current waveforms of two PFC converters for several input voltage cycles. It can be seen that the envelope of the inductor current follows the input voltage to be a sinusoidal waveform. The peak value of the inductor current is high at high input voltage, and vice versa. Therefore, the time required for the inductor current to decrease from a peak value to zero is not the same. When the input voltage is at a high point, it requires more time for the inductor current to decrease from a peak value to zero. It can be concluded that if PFC converters can operate in DCM when the input voltage is at its peak point, then they can operate in DCM throughout the input voltage cycle. Figure 6b shows the expanded waveforms when the input voltage is near the peak value. As shown, the inductor current does decrease to zero. Figure 7a shows the waveforms of input voltage and input current. It can be seen that the input current follows the input voltage and is in phase with the input voltage. A power analyzer was used to measure the power quality of the input line. At rated power operation, the values of the active power, reactive power, and apparent power were 196.7 W, 34.5 Var, and 199.7 VA, respectively. The measured power factor and THDi are 0.985 and 5.27%, respectively. The specifications of the proposed LED were measured. Figure 7b shows the harmonic spectrum of the input current. The current harmonics are compared with the IEC 61000-3-2 Class C standard [6]. It can be seen that all measured current harmonics are below the standard. It verifies that operating a boost converter in DCM can indeed achieve a high power factor and low THDi. Figure 8 shows the current waveforms in the two windings of the coupled inductor. As mentioned in the section on analysis of operation mode, Mode 3 is the time to discharge the parasitic capacitance from high voltage to zero volts, and Mode 4 is the time for the inductor current to rise from zero to greater than the absolute value of the inductor current. Generally, the parasitic capacitance is very small. The typical output parasitic capacitance of the active switch (IPW65R080CFD, Infineon Technologies, Neubiberg, Germany) is 215 pF. Therefore, the time required for Mode 3 and Mode 4 is very short. The mutual inductance current is converted between the primary and secondary windings. When the current in one winding decreases, the current in the other winding increases. Additionally, the winding current will drop to a negative value. Although this negative current is very small, it is enough to release the parasitic capacitance of the MOSFET and allow the active switch to meet ZVS. Figure 9 shows the voltage and current waveforms of the two active switches. It can be seen from these experimental waveforms that before v_{GS1} (v_{GS2}) changes from low to high level, there is a negative current that discharges the parasitic capacitance of the active switch to zero volts. This allows the active switches to be turned on at zero voltage and zero current. Figure 10 shows the LED voltage and current waveforms. The measured LED power is 181 W, which is quite close to the design target values. The circuit efficiency is 92%. In addition, it can be seen that the LED voltage exhibits low-frequency ripples (120 Hz), and the ripple factor is calculated to be approximately equal to 7%. This ripple voltage can be reduced by using larger output capacitance or larger dc-link capacitance. Figure 11 shows the photo of the proposed LED driver test stand.

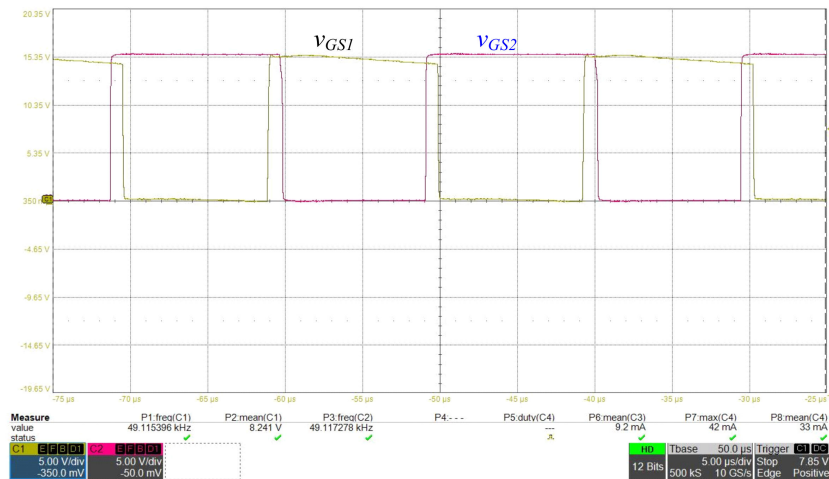
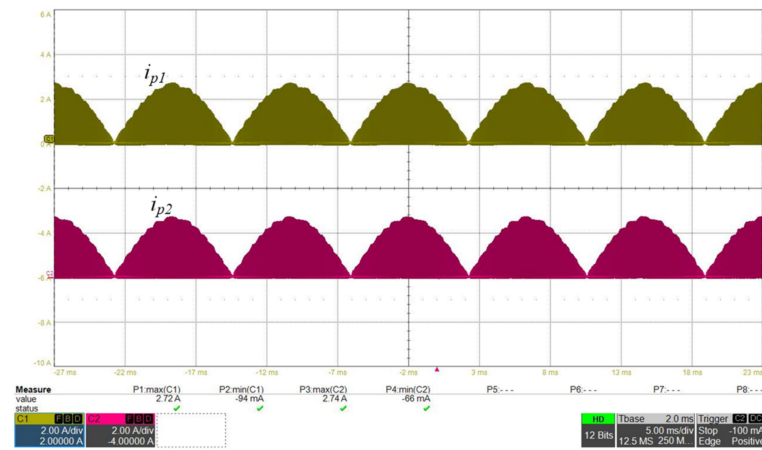
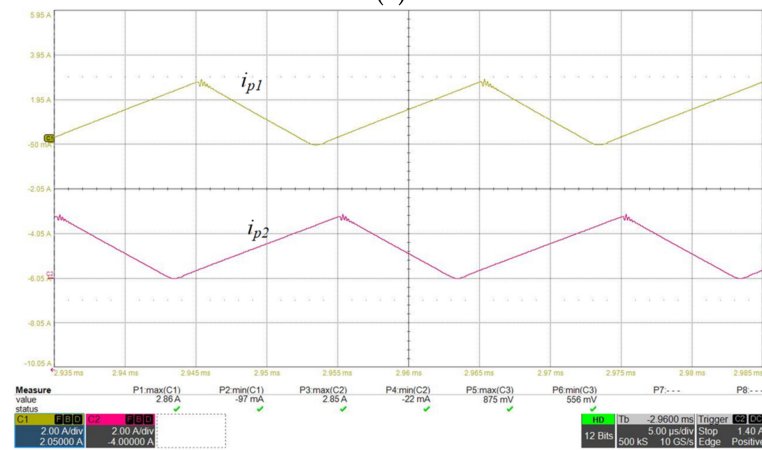


Figure 5. Gate-to-source voltages. (v_{GS1} : 5 V/div, v_{GS2} : 5 V/div, time: 5 μ s/div).

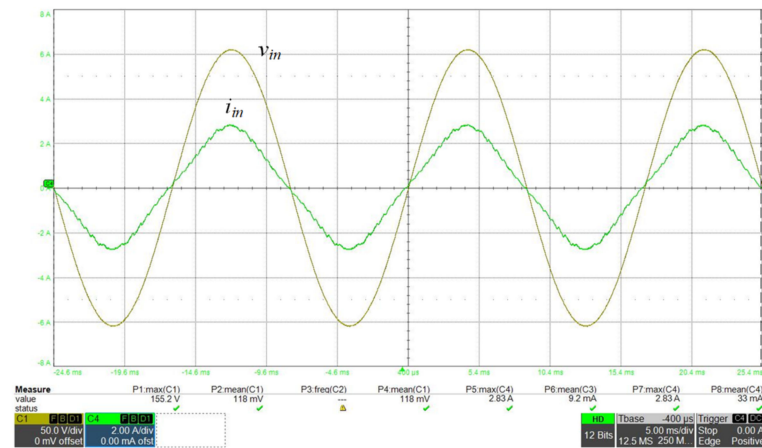


(a)

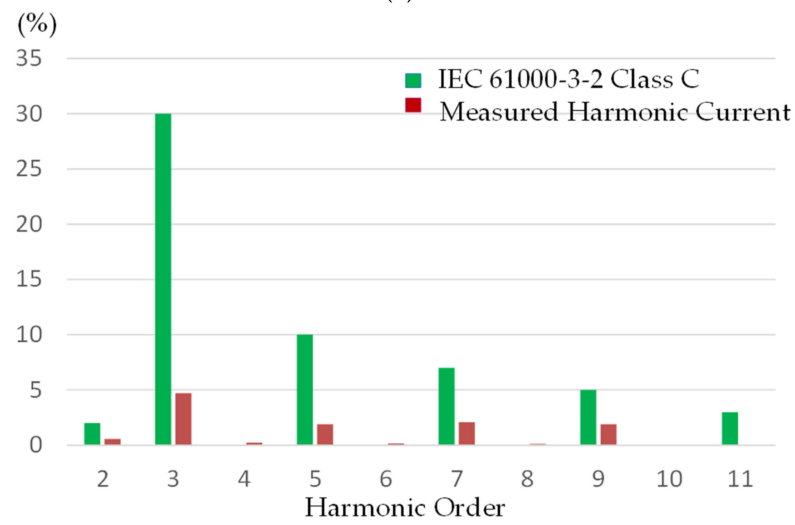


(b)

Figure 6. Inductor currents of the PFC converters. (a) i_{p1} and i_{p2} for several input voltage cycles. (i_{p1} , i_{p2} : 2 A/div, time: 5 ms/div), (b) expanded waveforms of i_{p1} and i_{p2} when the input voltage is near the peak value. (i_{p1} , i_{p2} : 2 A/div, time: 5 μ s/div).



(a)



(b)

Figure 7. (a) Waveforms of the input voltage and current. (v_{in} : 50 V/div, i_{in} : 2 A/div, time: 5 ms/div), and (b) comparison between measured input current harmonics and IEC standard [6].

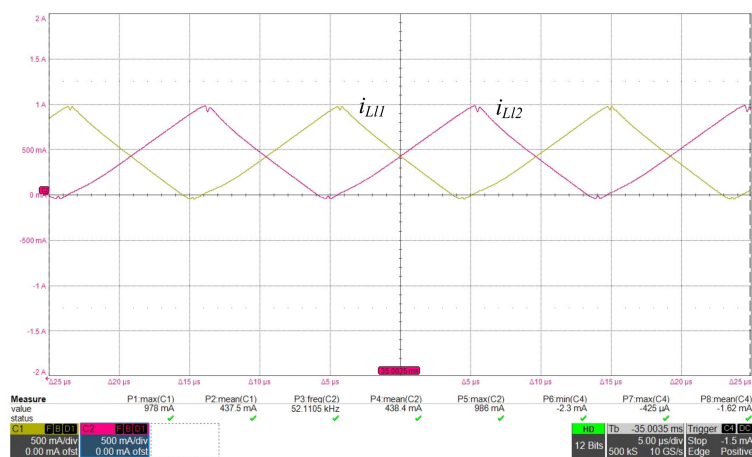
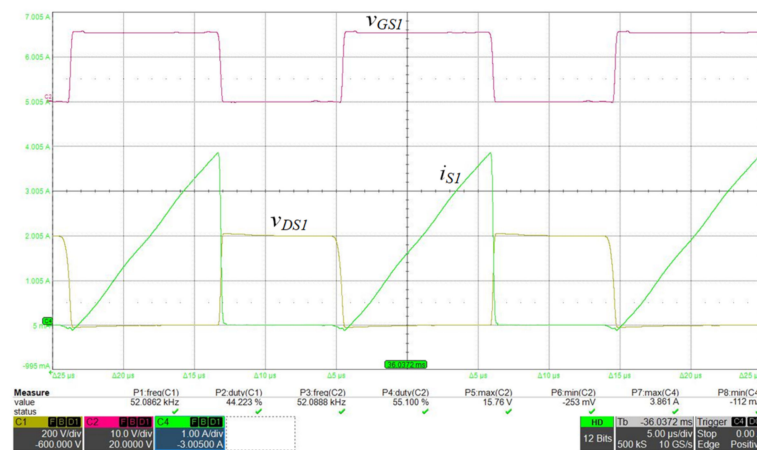
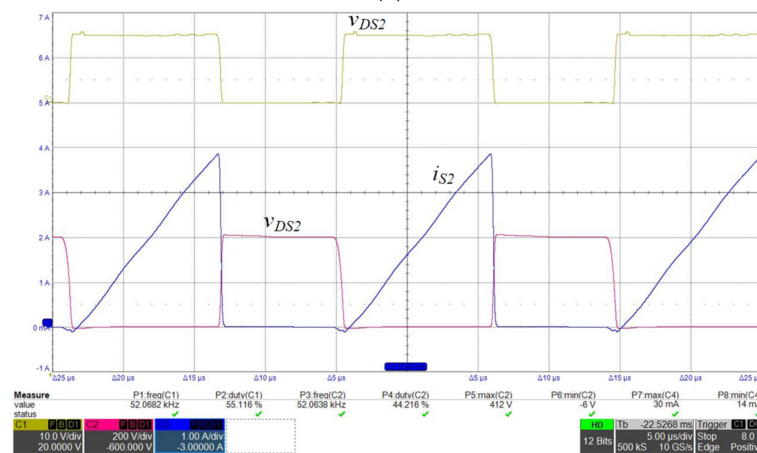


Figure 8. Waveforms of leakage current of T_1 . (i_{L11} , i_{L12} : 0.5 A/div, time: 5 μs/div).



(a)



(b)

Figure 9. Waveforms of S_1 and S_2 . (a) v_{GS1} , v_{DS1} and i_{S1} . (v_{GS1} : 10 V/div, v_{DS1} : 200 V/div, i_{S1} : 1 A/div, time: 5 μ s/div). (b) v_{GS2} , v_{DS2} and i_{S2} . (v_{GS2} : 10 V/div, v_{DS2} : 200 V/div, i_{S2} : 1 A/div, time: 5 μ s/div).

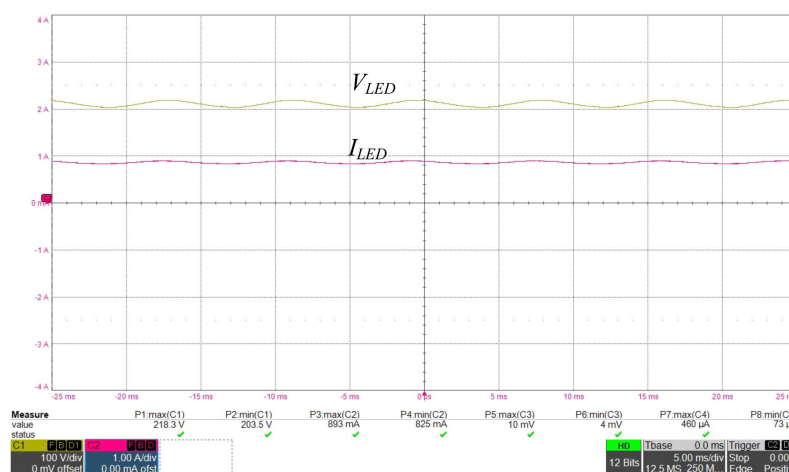


Figure 10. Waveforms of LED voltage and LED current. (V_{LED} : 100 V/div, I_{LED} : 1 A/div, time: 5 ms/div).

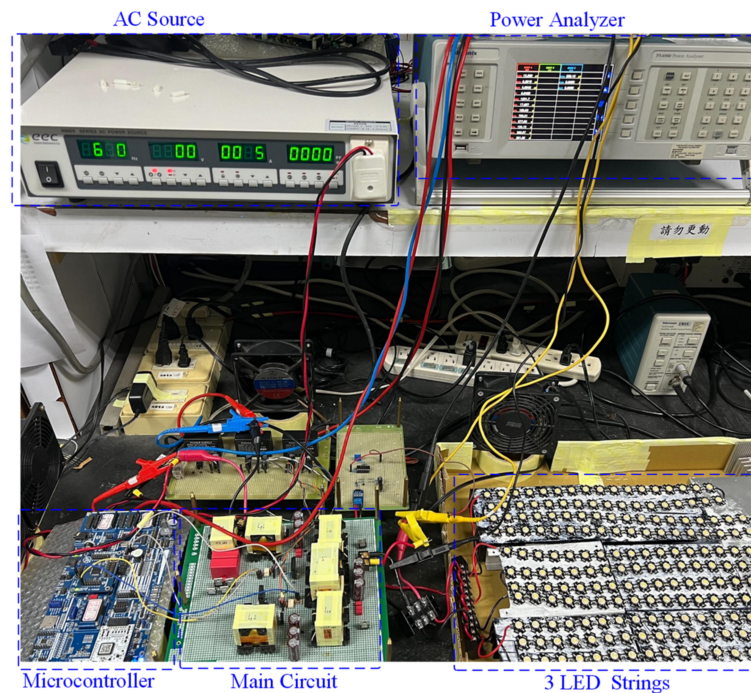


Figure 11. Photo of the proposed LED driver test stand.

5. Conclusions

This paper proposes a new LED driver with a high power factor and low total current harmonic distortion. The circuit architecture consists of two modified SEPICs that share a coupled inductor with two windings. The two SEPICs are interleaved operated, and their active switches have a duty cycle greater than 0.5. In this paper, mathematical equations are derived, and component parameters are designed so that all inductor currents would decrease to zero, allowing all diodes to operate at ZCS. In addition, the winding current of the coupled inductor can completely release the charge of the parasitic capacitance of the active switch, so that the active switch operates at ZVS, which significantly reduces the switching loss. A prototype circuit with a rated power of 180 W is implemented and measured experimentally. The experimental results show that the power factor and THDi are equal to 0.985 and 5.27%, respectively, at rated power operation. The measured efficiency of the circuit is 92%. The experimental results have verified the feasibility of the proposed circuit.

Author Contributions: H.-L.C. conceived the novel circuit topology and wrote the paper. C.-A.C. revised the original circuit and analyzed the circuit operation; C.-H.C. and E.-C.C. derived the mathematical equations and designed the circuit component. and designed parameters of the circuit components; Y.-C.H. carried out the prototype LED driver and measured as well as analyzed experimental results; L.-C.H. performed circuit simulations and revised the manuscript for submission. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding author.

Acknowledgments: This work was supported by the National Science and Technology Council, R.O.C. under Grant NSTC 112-2221-E-214-006.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Zhan, X.; Chung, H.; Zhang, R. Investigation into the use of single inductor for driving multiple series-connected LED channels. *IEEE Trans. Power Electron.* **2017**, *32*, 3034–3050. [\[CrossRef\]](#)
2. Cheng, C.A.; Lee, C.M.; Chang, E.H.; Hou, S.H.; Lan, L.F.; Lin, C.K. A novel integrated electronic lighting driver circuit for supplying an LED projection lamp with high power factor and soft switching characteristics. *Electronics* **2023**, *12*, 4642. [\[CrossRef\]](#)
3. Esteki, M.; Khajehoddin, S.A.; Safaei, A.; Li, Y. LED system applications and LED driver topologies: A review. *IEEE Access* **2023**, *11*, 38324–38358. [\[CrossRef\]](#)
4. Abdelmessih, G.Z.; Alonso, J.M.; Dalla Costa, M.A. Analysis, design, and experimentation of the active hybrid-series-parallel PWM dimming scheme for high-efficient off-line LED drivers. *IET Power Electron.* **2019**, *12*, 1697–1705. [\[CrossRef\]](#)
5. Subjak, J.S.; Mcquilkin, J.S. Harmonics-causes, effects, measurements, and analysis: An update. *IEEE Trans. Ind. Appl.* **1990**, *26*, 1034–1042. [\[CrossRef\]](#)
6. IEC 61000-3-2:2018/AMD2:2024; Amendment 2—Electromagnetic compatibility (EMC)—Part 3-2: Limits—Limits for Harmonic Current Emissions (Equipment Input Current ≤ 16 A Per Phase). International Electrotechnical Commission (IEC): Geneva, Switzerland, 2024. Available online: <https://webstore.iec.ch/en/publication/77736> (accessed on 24 July 2024).
7. IEEE 519-2022; IEEE Standard for Harmonic Control in Electric Power Systems. Institute of Electrical and Electronics Engineers (IEEE): Piscataway, NJ, USA, 2022. Available online: <https://standards.ieee.org/ieee/519/10677> (accessed on 24 July 2024).
8. Arseneau, R.; Ouellette, M. The effects of supply harmonics on the performance of compact fluorescent lamps. *IEEE Trans. Power Deliv.* **1993**, *8*, 473–479. [\[CrossRef\]](#)
9. Christiansen, R. Effect of high levels of harmonics from lighting equipment and system. In Proceedings of the Conference Record of the 1991 IEEE Industry Applications Society Annual Meeting, Dearborn, MI, USA, 28 September–4 October 1991; pp. 1859–1862.
10. Camponogara, D.; Ferreira, G.F.; Campos, A.; Dalla Costa, M.A.; Garcia, J. Offline LED driver for street lighting with an optimized cascade structure. *IEEE Trans. Ind. Appl.* **2013**, *49*, 2437–2443. [\[CrossRef\]](#)
11. Cheng, H.L.; Chang, Y.N.; Cheng, C.A.; Chang, C.H.; Lin, Y.H. High-power-factor dimmable LED driver with low-frequency pulse-width modulation. *IET Power Electron.* **2016**, *9*, 2139–2146. [\[CrossRef\]](#)
12. Cheng, C.A.; Cheng, H.L.; Chung, T.Y. A novel single-stage high-power-factor LED street-lighting driver with coupled inductors. *IEEE Trans. Ind. Appl.* **2014**, *50*, 2821–2826. [\[CrossRef\]](#)
13. Gacio, D.; Alonso, J.M.; Calleja, A.J.; García, J.; Rico-Secades, M. A universal-input single-stage high-power-factor power supply for HB-LEDs based on integrated buck-flyback converter. *IEEE Trans. Ind. Electron.* **2011**, *58*, 589–599. [\[CrossRef\]](#)
14. Alonso, J.M.; Viña, J.; Vaquero, D.G.; Martínez, G.; Osório, R. Analysis and design of the integrated double buck-boost converter as a high-power-factor driver for power-LED lamps. *IEEE Trans. Ind. Electron.* **2012**, *59*, 1689–1697. [\[CrossRef\]](#)
15. Li, Y.C.; Chen, C.L. A novel primary-side regulation scheme for single-stage high-power-factor AC–DC LED driving circuit. *IEEE Trans. Ind. Electron.* **2013**, *60*, 4978–4986. [\[CrossRef\]](#)
16. Cheng, C.A.; Chang, C.H.; Cheng, H.L.; Chang, E.C.; Lin, Y.R.; Lan, L.F. A novel light-emitting diode streetlight driver circuit applied to a direct current-input voltage source. *Sustainability* **2023**, *15*, 10934. [\[CrossRef\]](#)
17. Moon, S.C.; Koo, G.B.; Moon, G.W. A new control method of interleaved single-stage flyback AC-DC converter for outdoor LED lighting systems. *IEEE Trans. Power Electron.* **2013**, *28*, 4051–4062. [\[CrossRef\]](#)
18. Lam, C.W.; Jain, P.K. A high power factor, electrolytic capacitor-less AC-input LED driver topology with high frequency pulsating output current. *IEEE Trans. Power Electron.* **2015**, *30*, 943–955. [\[CrossRef\]](#)
19. Wang, S.; Ruan, X.; Yao, K.; Tan, S.C.; Yang, Y.; Ye, Z. A flicker free electrolytic capacitor-less AC-DC LED driver. *IEEE Trans. Power Electron.* **2012**, *27*, 4540–4548. [\[CrossRef\]](#)
20. Zhang, F.; Ni, J.; Yu, Y. High power factor AC–DC LED driver with film capacitors. *IEEE Trans. Power Electron.* **2013**, *28*, 4831–4840. [\[CrossRef\]](#)
21. Yu, X.; Su, J.; Guo, S.; Zhong, S.; Shi, Y.; Lai, J. Properties and synthesis of lossless snubbers and passive soft-switching PWM converters. *IEEE Trans. Power Electron.* **2020**, *35*, 3807–3826. [\[CrossRef\]](#)
22. Lee, J.H.; Yu, D.H.; Kim, J.G.; Kim, Y.H.; Shin, S.C.; Jung, D.Y.; Jung, Y.C.; Won, C.Y. Auxiliary switch control of a bidirectional soft-switching dc/dc converter. *IEEE Trans. Power Electron.* **2013**, *28*, 5446–5457. [\[CrossRef\]](#)
23. Yun, J.J.; Choe, H.J.; Hwang, Y.H.; Park, Y.K.; Kang, B. Improvement of power-conversion efficiency of a dc-dc boost converter using a passive snubber circuit. *IEEE Trans. Ind. Electron.* **2012**, *59*, 1808–1814. [\[CrossRef\]](#)
24. Lo, Y.K.; Chiu, H.J.; Lin, J.Y.; Wang, C.F.; Lin, C.Y.; Gu, B. Single-stage interleaved active-clamping forward converter employing two transformers. In Proceedings of the 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 17–21 March 2013; pp. 1898–1905.
25. Wang, Y.; Guan, Y.; Huang, J.; Wang, W.; Xu, D. A single-stage LED driver based on interleaved buck–boost circuit and LLC resonant converter. *IEEE J. Emerg. Sel. Topics Power Electron.* **2015**, *3*, 732–741. [\[CrossRef\]](#)
26. Ma, H.; Lai, J.S.; Zheng, C.; Sun, P. A high-efficiency quasi-single-stage bridgeless electrolytic capacitor-free high-power AC–DC driver for supplying multiple LED strings in parallel. *IEEE Trans. Power Electron.* **2016**, *3*, 5825–5836. [\[CrossRef\]](#)
27. Liu, J.; Tian, H.; Liang, G.; Zeng, J. A bridgeless electrolytic capacitor free LED driver based on series-resonant converter with constant frequency control. *IEEE Trans. Power Electron.* **2019**, *34*, 2712–2725. [\[CrossRef\]](#)

28. Filho, O.C.D.S.; Tofoli, F.; Barreto, L.H.S.C.; Oliveira, D.D.S. Single-phase isolated AC–AC symmetrical full-bridge converter. *IEEE J. Emerg. Sel. Topics Power Electron.* **2022**, *10*, 846–855. [[CrossRef](#)]
29. Cheng, H.L.; Hwang, L.C.; Chang, H.H.; Wang, Q.Y.; Cheng, C.A. High-efficiency flicker-free LED driver with soft-switching feature. *Micromachines* **2022**, *13*, 797. [[CrossRef](#)]
30. Liu, K.H.; Lin, Y.L. Current waveform distortion in power factor correction circuits employing discontinuous-mode boost converters. In Proceedings of the IEEE Power Electronics Specialists Conference, Milwaukee, WI, USA, 26–29 June 1989; pp. 825–829.

Disclaimer/Publisher’s Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.