

Article

A Reconfigurable Peripheral Interface Controller-Based Test Platform: Co-Design, Analytical Characterization, and Low-Cost Hardware Implementation

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Abstract

Practical training on embedded systems is a very good way to assess the skills of students in firmware development, real-time programming and hardware–software co-design. However, many low- and middle-income institutions still use closed, proprietary boards, such as the Altera DE series, which hide the physical behavior. To address this, a low-cost, fully reconfigurable Microcontroller Test Board (MTB) was designed and technically validated for application in undergraduate laboratories. The MTB is manufactured as a one-sided through-hole PCB via toner transfer and FeCl₃ etching, with a PIC18F2550 in-circuit programmer and support for 28- and 40-pin targets including the PIC16F877A. The MTB integrates six functional blocks, providing five canonical input/output modalities on a single regulated 5 V/0.56 A rail: (1) an ICSP programmer; (2) a multiplexed seven-segment display; (3) an 8 × 8 LED matrix; (4) a matrix keypad with LCD calculator; and (5) a 10-bit ADC stage. All subsystems operate with a flicker-free refresh rate > 122 Hz. The total board power consumption is 6.72 W at 12 V DC, with the linear regulator dissipating 3.92 W under full load. Probe points allow for signal transparency. Models for regulator dissipation, ADC quantization, multiplex refresh duty cycle, LED current limiting, oscillator timing, matrix-scanning latency, LCD timing, keypad response and Fe³⁺ with Cu etch kinetics were first-principles. Bench measurements agree with model predictions to less than 3% error, and confirm worst-case design margins. The MTB provides analytical rigor with accessible hardware to enable measurable experiments in microcontroller labs. The platform is cost-effective, with a material cost of less than USD 18. Each signal is routed to probe points, providing significant cost reduction from commercial trainers, and a transparent hands-on laboratory resource for engineering curricula with limited resources.



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Keywords: microcontroller platform; worst-case design; single-layer PCB; low-cost hardware; embedded systems education 1

1. Introduction

It is well known that practical lab work in embedded systems is the most reliable way to evaluate students' competence in firmware development, real-time programming and hardware–software co-design [1–6]. Unlike simulation-based assignments, practical

projects require students to consider timing constraints, power budgets, signal integrity and component tolerances that are absent in idealized models [7–11]. The quality and transparency of the laboratory platform directly affect the learning outcomes [12–14]. Students need to be able to probe signals, see the immediate physical effects of code changes, and reason about the worst-case behavior of circuits and firmware. In spite of this pedagogical consensus, many academic institutions in the low- and middle-income brackets still rely on closed, proprietary training boards such as the Altera DE series and Logic Tutor systems [15–18]. While these platforms are powerful, they present three important limitations for resource-constrained curricula. Firstly, the boards have high acquisition costs, often exceeding USD 150 per unit, restrict the availability of boards. In contrast, the board is designed for extreme affordability with a total cost of USD 17.64, reducing hardware expenditure by an order of magnitude. This limits the number of available boards, and requires group work, which reduces individual hands-on experience. Secondly, the closed architecture and surface-mount construction obscure physical signals and internal routing, disconnecting the code the students write from observable electrical behavior. Thirdly, the use of proprietary programming interfaces and fixed peripherals limits re-configurability, and therefore does not allow the instructor to adapt the board to the evolving objectives of the course. This means that in the laboratory students work primarily with abstractions of software rather than the fundamental physical principles of hardware.

To mitigate these constraints, this study presents the design, fabrication and analysis of a novel, cost-effective, reconfigurable peripheral interface controller-based test platform. Based on a PIC18F2550 host microcontroller configured as an in-circuit programmer, this platform can accommodate both 28-pin and 40-pin target devices. This dual-footprint methodology enables the board to cater for multiple courses and device families without requiring separate hardware. The peripheral subsystem was co-designed to cover the core competencies of introductory and intermediate embedded-systems courses: a four-digit multiplexed seven-segment display for counter and clock experiments, a keypad-driven calculator interfaced to a 16×2 liquid crystal display for I/O and state-machine labs, and an 8×8 LED matrix for scrolling text and animation exercises. An analog section comprising a potentiometer and rheostat, together with a regulated 5 V supply, provides experiments in ADC sampling, sensor interfacing, and power management. All signals are routed to labeled probe points to maintain transparency between firmware and hardware. The main technical contribution of this study is the derivation and experimental validation of the worst-case design margins for all the critical subsystems. Analytical models were developed to analyze the regulator power dissipation, ADC quantization noise, multiplex refresh duty cycle, current limiting requirements, oscillator timing accuracy, matrix-scanning latency, and Fe^{3+}/Cu etch kinetics during printed circuit board fabrication. Such equations allow us to quantitatively predict the performance and reliability before the fabrication process, which is often neglected in the fabrication of low-cost educational hardware. The board was fabricated as a single-layer printed circuit board using toner-transfer patterning and ferric chloride etching to reduce fabrication cost and infrastructure. Bench measurements confirmed a stable 5.02 V rail at 0.56 A, a flicker-free multiplex refresh rate of over 122 Hz per digit and complete operational verification of all subsystems. While analytically rigorous, the platform achieves a significant order-of-magnitude reduction in hardware expenditure compared to commercial trainers. Material costs are below USD 18, while full signal accessibility is ensured.

The remainder of this paper is structured as follows. Section 1 provides a broad introduction to low-cost reconfigurable embedded-systems training platforms, based on the literature and indicating the lack of full analytical design documentation. Section 2

describes the system architecture and hardware design. In Section 3, mathematical models and analytics characterization are described. Section 4 provides a detailed discussion on the experimental evaluation and results. Section 5 concludes the study with a discussion of implications for engineering curricula with limited resources and directions for future development.

2. Related Work

2.1. Instrumented Trainer Hardware in Engineering Education

Constructivist theories of learning have consistently posited that abstract concepts are most effectively understood through the manipulation of physical objects that symbolize those ideas. In the context of embedded systems, these objects are microcontrollers and their associated peripherals. Numerous studies in the field of engineering education corroborate this notion. Constructivism asserts that learners actively construct knowledge through engagement with tangible materials and experiences, rather than passively receiving information [19]. By handling physical artifacts, students gain a deeper understanding of concepts. This hands-on interaction fosters profound conceptual knowledge, contrasting with theoretical instruction, which lacks real-world experience [20]. This is very different from theoretical instruction, where students learn about systems in a detached way, without getting to experience how they actually behave. In microcontroller education, students engage with real hardware by configuring GPIO pins, observing LED responses, and interfacing with sensors and actuators. This hands-on approach fosters experiential learning, where students hypothesize about code effects, implement their ideas, observe results, and refine their understanding based on outcomes [21]. Research shows that hands-on work with microcontroller hardware boosts motivation and understanding. Active-learning students outperform non-active-learning students in lectures, especially in problem-solving and critical thinking [22]. Manipulating microcontroller systems highlights the link between programming concepts and system behavior [23]. Instrumented trainer hardware with built-in sensors and displays enhances learning by providing immediate feedback. This integrated instrumentation allows students to see results instantly, such as illuminated LEDs, displayed data, and motor responses. This feedback helps students understand abstract control theory, observe timing constraints in real-time systems, see how interrupt handling works with asynchronous events, and recognize hardware limitations on software design [24]. This constructivist foundation, backed by engineering education research, highlights the irreplaceability of hands-on lab work with real hardware in embedded systems education. No simulation can replicate the multisensory learning experience of working with actual hardware and seeing immediate results.

2.2. Existing Trainer-Board Platforms

There are four main categories of these platforms, each with its own advantages and disadvantages. The first category includes closed didactic kits like LogicTutor and Altera DE-series, which are popular in university laboratories. While ideal for learning discrete logic and basic sequential experiments, they lack the programmable capability of using a microcontroller. These traditional platforms offer fixed-function behavior suitable for foundational studies, but limit advanced embedded-systems work and student exploration of real-time control and software–hardware integration [25]. Next are FPGA development boards, such as the Intel DE10, Xilinx Basys and Lattice iCEstick. These offer significant hardware versatility and are ideal for prototyping. However, they come with a steep learning curve: students need to familiarize themselves with Verilog, System Verilog or VHDL, as well as synthesis tools, before they can achieve anything. This is a common hurdle in beginner embedded-systems courses. Next, there are maker-grade microcontroller boards

such as the Arduino Uno ATmega328P, ESP32 DevKits, STM32 Nucleo and Raspberry Pi Pico RP2040. While these are affordable and easy to find, they are not specifically designed for teaching purposes. In order to use them, students often have to add necessary peripherals such as LCDs, keypads and LED matrices in the form of external shields. The signal traces can also be difficult to access as they are routed under SMD packages. Additionally, many of these boards use bootloaders that obscure the in-circuit programming protocol from learners. Finally, there are commercial all-in-one trainers, such as the Microchip Curiosity board, the ST Discovery kit and the PICKit Low-Pin-Count Demo Board. These integrate various peripherals on a single PCB, which is very convenient. Nevertheless, they are multilayer SMT assemblies that are difficult to replicate in a typical undergraduate laboratory. Their licensing restrictions and material costs also make them inaccessible to many institutions in low- and middle-income countries. To demonstrate the novelty of the MTB, the following comparison is synthesized from the specific technical specifications and measured learning outcomes reported in the literature, as detailed in Table 1 below. Unlike commercial platforms that prioritize high-density SMT integration, the MTB's design is optimized to facilitate measurable learning outcomes, such as firmware observability and protocol transparency, as identified as critical in recent pedagogical research.

Table 1. Comparative analysis of educational microcontroller platforms.

Feature	Altera DE-Series (Closed Kit)	Arduino Uno (Maker-Grade)	ST Discovery (Trainer)	Intel DE10 (FPGA)	MTB (This Work)
Unit Cost	High (>\$150)	Low (\$5–25)	Moderate (\$30–80)	High (>\$150)	Very Low (<\$18)
Peripherals	Fixed/internal	External shields	On-board (SMD)	Fixed/internal	Integrated (5 modalities)
Signal Access	Poor (opaque)	Difficult (SMD)	Limited	Poor (opaque)	Full (probe points)
PCB Tech	Multilayer SMT	Multilayer SMT	Multilayer SMT	Multilayer SMT	Single-layer through-hole
Measured Learning Outcomes	Suitable for foundational logic only; limited advanced exploration.	Increased motivation and understanding through rapid prototyping.	Improved conceptual understanding in quasi-experimental trials.	High hardware flexibility but steep initial learning curve.	Enhanced firmware observability and measurable experimental validation.

2.3. PIC-Based Platforms Specifically

Notwithstanding the growing popularity of 32-bit Cortex-M options, Microchip Technology Inc.'s 8-bit PIC family (Chandler, AZ, USA) remains a prominent teaching tool in over 1200 universities worldwide. Its appeal in education stems from the Harvard architecture, which neatly separates program and data memory, and the PIC16 family's straightforward instruction set of just 35 RISC-like commands. There is also a wealth of teaching resources available. Recent studies show that PIC-based hardware is ideal for classrooms. Their simplicity, cost-effectiveness, and widespread industrial use make them essential in introductory electrical engineering courses [26]. Educational institutions have integrated PIC microcontrollers into embedded-systems courses; the MTB is designed to support pedagogical goals through signal transparency [27]. Additionally, PIC systems are effective in various educational settings, including traditional labs and remote learning, highlighting their flexibility and reliability as teaching tools [28]. These findings highlight that PIC architectures are still excellent, hands-on platforms for learning about embedded systems.

2.4. Gap and Position

While existing work provides valuable foundations for embedded systems education, there remains a lack of a platform that integrates all the features required for an effective, low-resource trainer. Specifically, the following four features are often absent in single-substrate designs: built-in in-circuit serial programming (ICSP) with no need for external tools; five canonical I/O modalities on a single board; total signal transparency via labeled probe points; and the ability to reproduce the design using single-layer, FeCl₃-etched techniques for under USD 18. This study presents a robust, analytically characterized platform to address these requirements in the form of the Microcontroller Test Board (MTB). It combines the instructional benefits of PIC-based design with verified engineering margins, comprehensive signal visibility, and fabrication methods suitable for institutions with limited resources.

2.5. System Architecture and Hardware Co-Design

The Microcontroller Test Board comprises six separate yet interconnected subsystems that share a common regulated 5V power supply and operate together. The comprehensive schematic in Figure 1 illustrates the interconnection of all components. This layout was designed to facilitate learning while ensuring electrical soundness. Each subsystem can be explored independently while operating under the same power and timing rules as real embedded designs.

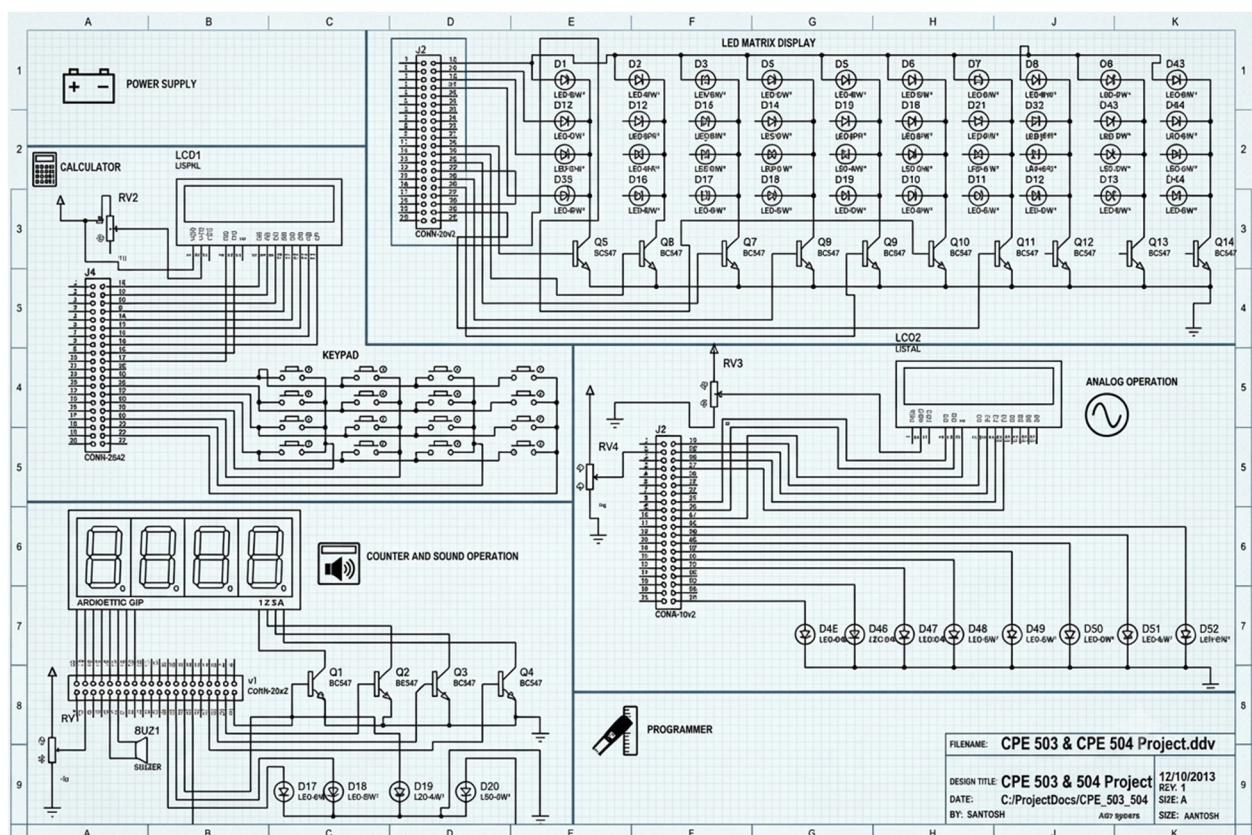


Figure 1. System schematic diagram.

2.6. Subsystem Inventory

The Microcontroller Test Board (MTB) features six functional blocks that provide significant versatility for embedded-systems training. Its power supply consists of an LM7805 linear regulator, a 1000 μ F electrolytic bulk capacitor to mitigate input ripple, and a 100 nF decoupling capacitor. Labeled probe points for V_{in} , V_{out} , and GND are provided to

ensure signal transparency and facilitate direct hardware debugging. The system architecture integrates a PIC18F2550-based firmware host with a 40-pin zero insertion force (ZIF) socket compatible with both 28-pin and 40-pin target devices. Critical ICSP signals such as PGD, PGC, MCLR, and VDD are accessible via dedicated probe points for real-time protocol observation.

A multiplexed-display subsystem utilizes four common-cathode 7-segment digits driven by PORTC for segment control and PORTA for digit selection, with BJTs serving as cathode drivers. The calculator subsystem comprises a 4×4 matrix keypad and a 16×2 HD44780 LCD display, which uses an adjustable $10\text{ k}\Omega$ potentiometer for contrast. An 8×8 LED matrix is driven by eight rows and eight columns sinking current through 2N3904 BJTs, utilizing $220\ \Omega$ series resistors to allow access to all 16 lines. The analog stage includes a $10\text{ k}\Omega$ potentiometer and rheostat connected to PORTA0/AN0, featuring a probe point for the wiper voltage.

Due to the high peripheral density, certain I/O ports are shared; for instance, PORTB interfaces with both the LCD and LED matrix rows, while PORTD supports both the keypad and LED matrix columns. To manage this bus contention, the MTB incorporates an on-board 8-switch DIP bank and toggle switches that allow users to physically isolate or enable specific functional blocks. This careful design ensures that the signals of each node remain fully visible and suitable for practical measurement and debugging activities.

2.6.1. Power Tree

The power supply is derived from an unregulated 12 V DC source and provides a single regulated 5V rail using an LM7805 three-terminal linear regulator as shown in Figure 2. A $1000\ \mu\text{F}$, 25 V electrolytic capacitor is used to reduce the effect of input ripple. A $0.1\ \mu\text{F}$ ceramic capacitor is used at the output to reduce high-frequency noise. Single-rail architecture avoids the complexities associated with multiple voltage domains, which makes analysis easier for students. The static power dissipation budget is defined by a projected current of 0.56 A, calculated to support the five I/O subsystems (excluding the regulator stage itself). This ensures that the power tree is sized for worst-case operational scenarios. In the next section we shall discuss the thermal analysis and the choice of the regulator, for which this budget is important.

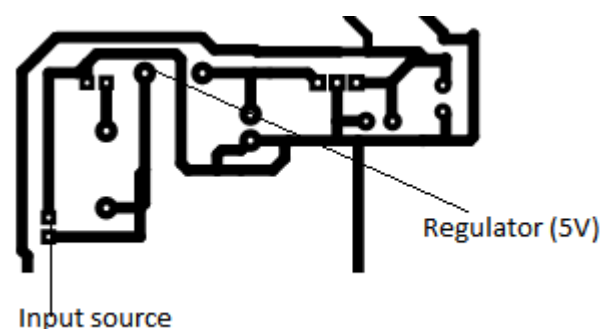


Figure 2. Power supply PCB layout.

2.6.2. Programmer

As shown in Table 2 and depicted in Figure 3, the in-circuit programmer has a PIC18F2550 functioning as a USB-to-ICSP bridge at its core. The PIC18F2550's firmware adheres to the Microchip ICSP timing protocol outlined in DS39622 [29]. The bridge operates a 40-pin ZIF socket designed to accommodate 28-pin devices such as the PIC16F628 and PIC18F2550, as well as 40-pin devices including the PIC16F877A and PIC18F4520, via proper pin 1 alignment. Incorporating the programmer on board eliminates the need

for an external PICKit and improves visibility of the programming protocol for learners, effectively addressing the transparency gap.

Table 2. MTB target device compatibility and pin-mapping.

Functional Block	I/O Port	18-Pin Target (e.g., PIC16F628)	28-Pin Target (e.g., PIC18F2550)	40-Pin Target (e.g., PIC16F877A)
ICSP	PGC, PGD, MCLR	Pins 12, 13, 4	Pins 27, 28, 1	Pins 39, 40, 1
7-Segment Display	PORTC (Seg), PORTA (Sel)	N/A (Limited I/O)	RC0–RC7, RA0–RA3	RC0–RC7, RA0–RA3
8 × 8 LED Matrix	PORTB (Row), PORTD (Col)	RB0–RB7, N/A	RB0–RB7, N/A	RB0–RB7, RD0–RD7
LCD Module (4-bit)	PORTB (D4–D7, RS, EN)	RB4–RB7, RB1, RB2	RB4–RB7, RB1, RB2	RB4–RB7, RB1, RB2
Matrix Keypad	PORTD	N/A	N/A	RD0–RD7
Analog ADC Input	PORTA (AN0)	Pin 17 (RA0)	Pin 2 (RA0)	Pin 2 (RA0)

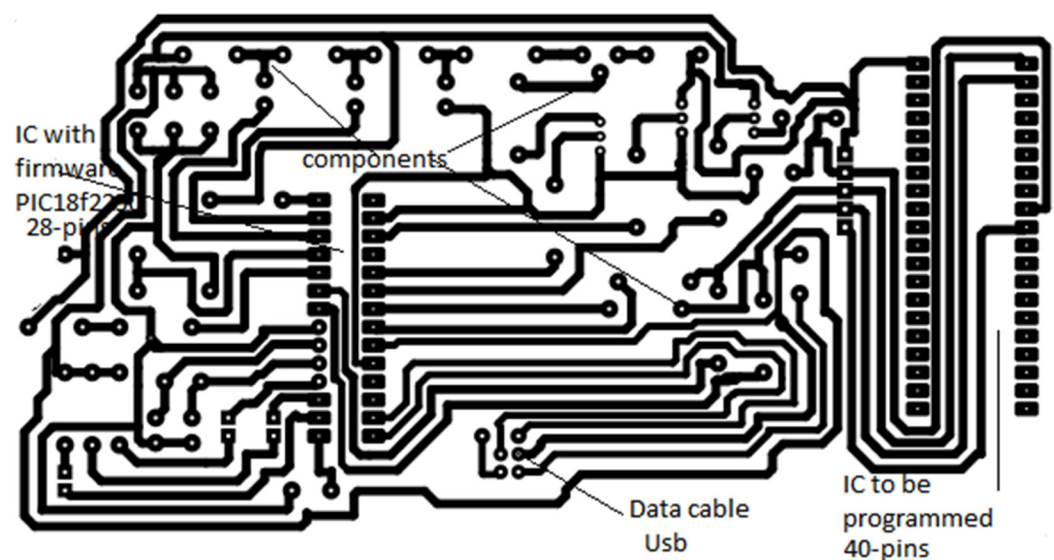


Figure 3. ICSP programmer PCB layout.

2.6.3. Display, Input and Matrix Subsystems

Figure 4 illustrates the calculator section of the MTB, which interfaces the 4 × 4 keypad with PORTD using rows as outputs and columns as pulled-up inputs for matrix scanning. To conserve I/O resources, the 16 × 2 LCD is interfaced with PORTB in 4-bit mode. The 8 × 8 LED matrix is driven via column-major scanning, where PORTB pins source row data and eight 2N3904 BJTs on PORTD act as high-current column sinks. This configuration ensures that row-pin sourcing current never exceeds the design limits of the MCU. Based on the analytical model in Section 3.4, forward current is limited to approximately 14.1 mA per LED using 220 Ω series resistors, ensuring sufficient brightness without exceeding the PIC's 25 mA per-pin limits. Due to the high peripheral density, PORTB is shared between the LCD and the LED matrix rows. To prevent signal interference and bus contention, an on-board 8-switch DIP bank is utilized to physically enable or disable specific subsystems, ensuring that only one modality is electrically active on the shared port at a given time. Consequently, this integrated design allows students to observe multiplex timing, scanning latency, and hardware resource management trade-offs directly on a connected system.

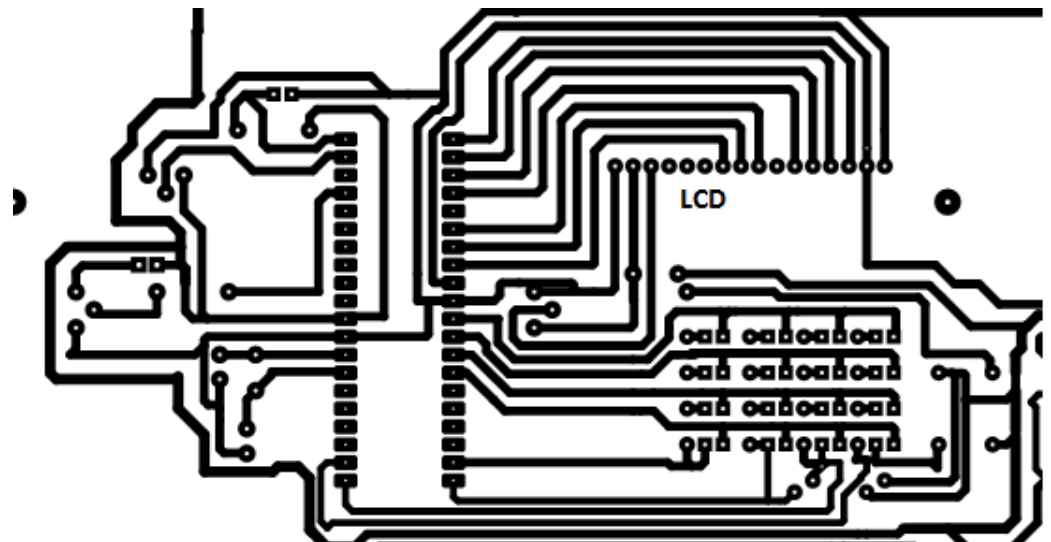


Figure 4. Calculator subsystem PCB layout.

2.6.4. PCB Realization

The physical implementation is a single-layer copper artwork exported from Proteus ARES in mirrored format as shown in Figure 5, for toner-transfer fabrication. Figure 6 shows the assembled board after FeCl_3 etching, drilling and manual through-hole population. Clockwise from the top left, the board consists of a 12 V input and LM7805 regulator, a 40-pin target ZIF socket, a USB programmer header, a 16×2 LCD module, an 8×8 LED matrix and a four-digit multiplexed 7-segment array. The single-sided layout gives full signal access and reproducibility of fabrication in undergraduate laboratories that do not have multilayer PCB capabilities.

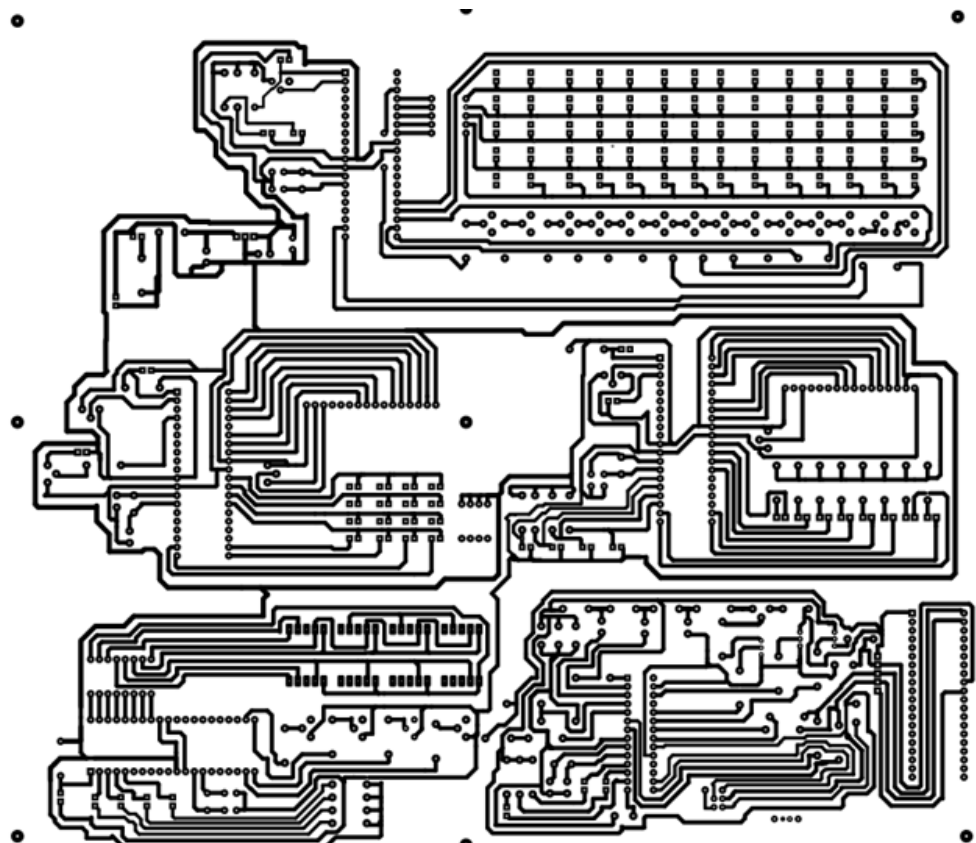


Figure 5. Master copper artwork.

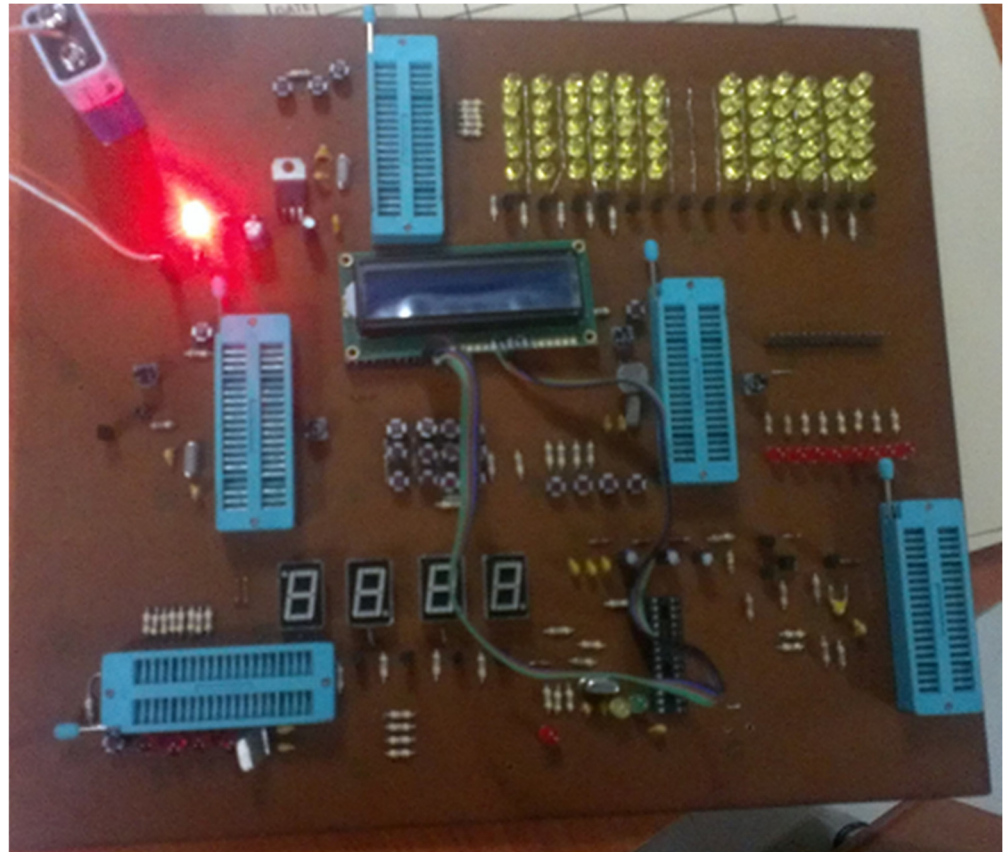


Figure 6. Fully assembled MTB prototype.

3. Mathematical Modeling and Analytical Characterization

Building on the component-value selections presented in Section 2, this section outlines the closed-form analytical relationships that govern each subsystem. Each derivation starts from fundamental principles and ends with the numerical design constraint applied to the MTB.

3.1. Linear-Regulator Dissipation and Thermal Envelope

For a three-terminal linear regulator characterized by an input voltage (V_{in}), an output voltage (V_{out}), a load current (I_L) and a quiescent current (I_Q), where I_Q is significantly less than I_L , the instantaneous power dissipation can be expressed as the sum of the voltage drop across the pass element and the quiescent component in Equation (1).

$$P_d = (V_{in} - V_{out}) \cdot I_L + V_{in} \cdot I_Q \approx (V_{in} - V_{out}) \cdot I_L \quad (1)$$

The power supplied to the load is expressed as $P_L = V_{out} \cdot I_L$, resulting in the regulator efficiency $\eta = \frac{P_L}{P_L + P_d} = \frac{V_{out}}{V_{in}}$. At the specified operating point of $V_{in} = 12$, $V_{out} = 5$ and $I_L = 0.56$ A, P_d is calculated to be 3.92 W, P_L is calculated to be 2.80 W and η is calculated to be 41.7%.

The corresponding junction-to-ambient thermal rise for a TO-220 package is given in Equation (2).

$$\Delta T_J = P_d \cdot \theta_{JA} \quad (2)$$

While θ_{JA} is approximately 65 K/W without a heatsink, the implementation of a small clip-on heatsink reduces the thermal resistance to approximately 23 K/W. This configuration results in a thermal rise (ΔT_J) of 90 °C, maintaining a junction temperature of 115 °C at 25 °C ambient, which ensures a safe 10 °C thermal margin below the manufacturer's 125 °C limit.

3.2. ADC Quantization, Resolution and SNR

The 10-bit successive-approximation ADC of the PIC digitizes the potentiometer/rheostat connected to AN0. The ideal transfer function for an n -bit unipolar ADC with a reference voltage V_{ref} is given by $X(V_{in}) = \left\lfloor \frac{V_{in}}{V_{ref}} \cdot (2^n - 1) + 1/2 \right\rfloor$, and the least significant bit (LSB) resolution is defined as $Q = \frac{V_{ref}}{2^n - 1}$, $V_{resolution} = Q$. With $V_{ref} = 5$ V, and $n = 10$, $Q = \frac{5}{1023} \approx 4.89$ mV/LSB. For an ideal n -bit ADC operating under a full-scale sinusoidal input, the signal-to-quantization-noise ratio (SQNR) is represented by $SQNR_{dB} = 6.02n + 1.76$. For $n = 10$, the calculated $SQNR_{dB} \approx 61.96$ dB, which is sufficiently high for the gradual rheostat adjustment utilized in the LED scroll demonstration.

3.3. Multiplexed-Display Refresh Constraint

A duty cycle per digit is defined as $D = \frac{1}{N}$ when driving digits from a singular 8-bit segment bus. It is vital to surpass the critical flicker fusion frequency, denoted as $f_{ccf} \approx 60$ Hz, in order to prevent noticeable flicker. The refresh rate of the array must satisfy the condition $f_r = \frac{1}{N \cdot T_d} \geq f_{ccf}$, where T_d denotes the dwell time assigned to each digit. In the case of $N = 4$ and a desired $f_r = 122$ Hz, T_d is calculated as $\frac{1}{N f_r} = \frac{1}{4 \times 122} \approx 2.05$ ms. The instantaneous segment current required to achieve steady-state brightness is expressed as $I_{peak} = \frac{I_{avg}}{D} = N \cdot I_{avg}$, given that average luminance is proportional to the duty cycle. Therefore, for a target $I_{avg} = 5$ mA and $N = 4$, the resulting $I_{peak} = 20$ is 20 mA per segment, which remains within the sourcing limit of 25 mA per pin for the PIC16F877A. The target average current (I_{avg}) of 5 mA per segment results in an instantaneous I_{peak} of 20 mA. This remains safely within the 25 mA absolute maximum sourcing limit per pin for the PIC16F877A, ensuring the total port current does not exceed architectural budgets during multiplexed operation.

3.4. LED Current Limiting

In the case of a forward-biased voltage (V_f) light-emitting diode (LED) powered by a logic-high output voltage (V_{OH}) through a series resistor (R), the operating current (I_{LED}) is given by $I_{LED} = \frac{V_{OH} - V_f}{R}$. For the red LEDs used in the 8×8 matrix, the forward voltage (V_f) is approximately 1.8 V and the output voltage (V_{OH}) is approximately 4.9 V.

To prevent per-pin overcurrent and bus contention, the matrix utilizes column-major scanning with a $1/8$ duty cycle. By ensuring that only one column BJT is active at any micro-interval (T_d), each PORTB row pin is required to source current to only one LED ($I_{row} = 14.1$ mA), which is well within the 25 mA sourcing limit. The worst-case aggregate port current for PORTB is 112.8 mA (8 LEDs active), complying with the 200 mA total port budget specified in the PIC16F877A datasheet.

3.5. Matrix-Keypad Scanning Latency

The worst-case detection latency, defined as $T_{scan} = K \cdot (T_s + T_r)$, is exhibited by a $K \times K$ matrix keypad when scanned in a row-by-row manner. Here, T_s represents the row settle time and T_r denotes the read time. For a configuration where $K = 4$, the row settle time (T_s) is set to 100 μ s, determined by RC settling through internal pull-ups of approximately 20 k Ω and an input capacitance (C) of 5 pF. Additionally, a software debounce time (T_{db}) of 50 ms is implemented once per edge. Consequently, the perceived response time is calculated as $T_{resp} = T_{scan} + T_{db} \approx 0.4$ ms + 50 ms $\approx$ 50.4 ms. This value remains below the 100 ms ergonomic threshold for perceived button responsiveness. Measurement of this parameter serves to empirically verify that the instruction clock is operating within the tolerances defined in Section 3.6, as the implemented software delays are clock-dependent.

3.6. Oscillator Selection: RC vs. Crystal

The frequency of the PIC's internal RC oscillator is approximately $f_{RC} \approx \frac{1}{K_{RC}RC}$, with $K_{RC} \approx 0.55$ for the PIC16F877A. The resonant frequency of a crystal oscillator is given by the expression $f_{xtal} = \frac{1}{2\pi\sqrt{L_m C_m}}$, where L_m and C_m denote the crystal's motional inductance and capacitance, respectively. An accuracy of $\pm 20\%$ is offered by the RC mode, while a reduced component count is required, thus rendering it suitable for educational step-through demonstrations. Conversely, the crystal mode provides an accuracy of ± 50 ppm, which is essential for time-sensitive applications such as frequency counters and real-time clocks. Both modes can be accessed via the MTB and selected using S2.

3.7. LCD Command Timing

A power-on initialization period (T_{init}) of at least 30 ms is required for the HD44780 controller which is used in the 16×2 LCD. During this time, no commands should be executed. Following this initialization phase, 4-bit-mode bytes must be transmitted nibble by nibble with an enable-pulse high time of $TEH \geq 230$ ns, in accordance with the specifications outlined in the datasheet. To ensure operational reliability under varying voltage and temperature conditions T_{init} and TEH are implemented as `delay_ms(30)` and `delay_us(1)` calls within the firmware.

3.8. Etching Kinetics

Utilizing $FeCl_3$, the etching process described in Section 3.10.4 is represented by the following reaction: $Cu_{(s)} + 2FeCl_{3(aq)} \rightarrow CuCl_{2(aq)} + 2FeCl_{2(aq)}$. The standard potentials are $E_{cell}^{\circ} = E_{Fe^{3+}/Fe^{2+}}^{\circ} - E_{Cu^{2+}/Cu}^{\circ} = 0.77 - 0.34 = +0.43$ V, which indicates the spontaneity of the reaction. The etch rate is approximately first-order with respect to $[Fe^{3+}]$ and adheres to Arrhenius kinetics, which is described by $k(T) = Ae^{-E_a/RT}$, where $E_a \approx 50$ kJ/mol. Consequently, increasing the bath temperature by $10^{\circ}C$ effectively doubles the etch rate, a common fabrication technique used to regulate line width and undercut.

3.9. Firmware Architecture and Software Methodology

The architecture of the firmware was meticulously designed to make the connection between C code, compiler output and physical I/O transparent for students. The complete tool-chain is presented as a result, and a formal finite-state-machine model is employed for the application logic. The matrix-scanning firmware enforces these electrical limits by utilizing a one-hot bitmask in the interrupt-driven scanning loop. This logic ensures that the hardware cannot enable multiple column BJTs simultaneously, thereby hardware-limiting the instantaneous current draw of the row pins.

3.9.1. Tool-Chain

Both the PIC16F877A and the PIC18F2550 are utilized in the calculator, counter, and LCD subsystems, as well as in the firmware of the on-board USB programmer, with the identical C codebase designed to target both. The source code is written in ANSI C and compiled using the CCS PIC-C compiler, version 4.x. MPLAB X is used for project management and debugging purposes, and Proteus VSM offers cycle-accurate simulation prior to physical flashing. The choice of C over assembly is based on three main reasons. Firstly, CCS-C provides peripheral abstractions such as `#use delay`, `#use fast_io` and `#include <lcd420.c>` which corresponds directly to the hardware blocks outlined in Section 2. This alleviates cognitive load for learners. Secondly, CCS-C code is portable across the PIC16 and PIC18 families without the need to rewrite application logic, which facilitates the board's multi-PIC design. Thirdly, C remains the dominant industry language for 8-bit microcontrollers, ensuring student competencies are directly transferable to professional practice.

3.9.2. Calculator Firmware: Finite-State-Machine Model

The firmware of the calculator is organized as a Mealy finite-state machine, denoted as $M = (Q, \Sigma, \delta, q_0, \lambda)$. The set of states is defined as $Q = \{\text{Idle}, \text{N1}, \text{Op}, \text{N2}, \text{Eval}\}$. The input alphabet is represented by $\Sigma = \{\text{digit}, +, -, \times, \div, =, C\}$. The transitions and outputs are characterized by $\delta : Q \times \Sigma \rightarrow Q, \lambda : Q \times \Sigma \rightarrow O$, where O signifies the LCD output alphabet. This formal model ensures that input from the keypad is processed deterministically and that the LCD consistently reflects a valid state. Algorithm 1 implements M in the C programming language using the matrix-scan primitive derived in Section 3.5. During each iteration of the loop, the keypadRead() function retrieves the key that has been pressed. If the machine is in the Idle state and a digit is detected, that digit is recorded in num1 and the state transitions to N1. Additional digits are accumulated in num1 until an operator is pressed. The operator is then stored, and the state transitions to Op. Any subsequent digits are used to construct num2 in state N2. Pressing the = key invokes apply(op, num1, num2), displays the resultant value and reverts to the Idle state. Pressing the C key resets all registers and returns the machine to the Idle state from any other state. This structural design makes the program flow explicit, enabling students to trace each transition using an oscilloscope at the probe points.

Algorithm 1: Mealy Finite-State Machine for Calculator Logic

Input: Keypad scan value $k \in \Sigma$ where $\Sigma = \{\text{digit}, +, -, \times, \div, =, C\}$

Output: LCD character string O

Pre-condition: System oscillator is calibrated (Section 3.6); matrix scan settles within 100 μs (Section 3.5).

```

1.  Initialize:  $Q \leftarrow \text{Idle}$ ; num1, num2  $\leftarrow 0$ ; op  $\leftarrow \text{null}$ ; LCD_Clear()
2.  Loop Forever:
3.     $k \leftarrow \text{keypadRead()}$  // Execute matrix-scan primitive (Section 3.5)
4.    If  $k = \text{null}$  Then Continue
5.    If  $k = 'C'$  Then // Global reset
6.      num1, num2  $\leftarrow 0$ ; op  $\leftarrow \text{null}$ ;  $Q \leftarrow \text{Idle}$ ; LCD_Clear()
7.    Else Switch ( $Q$ ):
8.      Case Idle:
9.        If  $k \in \text{digits}$  Then num1  $\leftarrow k$ ;  $Q \leftarrow \text{N1}$ ; LCD_Display( $k$ )
10.     Case N1:
11.       If  $k \in \text{digits}$  Then num1  $\leftarrow \text{accumulate}(\text{num1}, k)$ ; LCD_Display( $k$ )
12.       Else If  $k \in \text{operators}$  Then op  $\leftarrow k$ ;  $Q \leftarrow \text{Op}$ ; LCD_Display( $k$ )
13.     Case Op:
14.       If  $k \in \text{digits}$  Then num2  $\leftarrow k$ ;  $Q \leftarrow \text{N2}$ ; LCD_Display( $k$ )
15.     Case N2:
16.       If  $k \in \text{digits}$  Then num2  $\leftarrow \text{accumulate}(\text{num2}, k)$ ; LCD_Display( $k$ )
17.       Else If  $k = '='$  Then
18.          $Q \leftarrow \text{Eval}$ 
19.         result  $\leftarrow \text{apply}(\text{op}, \text{num1}, \text{num2})$ 
20.         LCD_Display(result)
21.        $Q \leftarrow \text{Idle}$ 
22.   End Loop
```

3.9.3. PIC Programming Workflow

Seven distinct and observable phases of PIC project development are outlined in the MTB. The first step is to capture requirements, where students describe the behavior

of the peripheral subsystem. The second step is about designing the algorithm, which is shown in a flowchart or finite-state machine. The calculator model gives an example of this. Step 3 involves C source coding using CCS-C. Step 4 involves compiling the source code into Intel HEX format using CCS-C or MPLAB XC8. The fifth step involves using Proteus VSM or MPLAB SIM to simulate the logic and timing before implementing the hardware. Step 6 entails in-circuit serial programming via the onboard PIC18F2550 programmer, as detailed in Section 2.6.2, thereby eliminating the need for external tools. Step 7 involves bench verification and instrumentation. During this step, students connect oscilloscopes or multimeters to the available probe points at each node to ensure that the firmware behavior aligns with the analytical models presented in Section 4. The MTB makes software development a quantifiable experimental process by rendering each step visible and accessible for probing. This is in contrast to a mere black-box compilation cycle.

3.10. PCB Fabrication Methodology

For reproducibility in resource-limited undergraduate laboratories, the MTB was built using a single-layer through-hole board with a modified toner-transfer and FeCl_3 -etch protocol. The decision to use single-layer construction was made to avoid the use of multilayer vias and barrel plating. These are typically inaccessible in the majority of educational laboratories, but are necessary for commercial multilayer training equipment.

3.10.1. Schematic Capture and Layout

The comprehensive schematic was generated in Proteus ISIS to confirm connectivity and net nomenclature prior to the physical layout. Subsequently, the PCB artwork was routed in Proteus ARES using a singular bottom-copper layer. All signal routing was confined to one copper plane to facilitate the reproduction of the board by students employing toner-transfer techniques and to ensure that each trace remains discernible and accessible for probing post-fabrication, in accordance with the design gap.

3.10.2. Film Generation

The mirrored positive layer was produced on glossy magazine paper using a laser printer. Laser toner was selected due to its fusibility and chemical resistance to FeCl_3 , unlike inkjet ink which dissolves in the etchant, resulting in fragmented traces. The mirrored circuits ensure that the text and PIN-1 markers are accurately represented.

3.10.3. Toner Transfer

The printed film was placed face-down on a new abraded 1.6 mm FR-4 copper-clad board before lamination. The film was then pressed onto the board with a household iron at around 180 °C for 3–5 min. A light mechanical abrasion with fine steel wool can be effective in removing the oxide and improving toner adhesion. The application of heat and pressure releases the toner from the paper, and bonds it to the copper substrate, creating an etch mask that precisely replicates the CAD layout with sub-millimeter accuracy.

3.10.4. Etching

At first, the laminated board was immersed in an aqueous solution of FeCl_3 . According to the chemical equation $\text{Cu}_{(s)} + 2\text{FeCl}_{3(aq)} \rightarrow \text{CuCl}_{2(aq)} + 2\text{FeCl}_{2(aq)}$, copper is removed, and a gentle mechanical method was employed to prevent passivation and ensure uniform etching. In accordance with the Arrhenius principle outlined in Section 3.8, the bath temperature was maintained at 40 °C; a temperature increase of 10 °C approximately doubles the etch rate for the FeCl_3/Cu system, which has an activation energy of approximately 50 kJ/mol. At this temperature, complete etching of the unmasked copper

took approximately 12 min, resulting in clean traces of 0.3 mm that adhere to the ARES design specifications.

3.10.5. Drilling and Population

In the etching and toner-removal process, through-holes were meticulously drilled using a 0.8 mm drill bit for DIP-integrated circuit sockets, resistors, capacitors and diodes, and a 1.0 mm drill bit for headers and connectors. All components are designed as through-holes to align with the single-layer process and to facilitate desoldering and reworking of parts by students during laboratory exercises. The components were soldered using a standard soldering station with 60/40 SnPb solder at a temperature of 350 °C. The resulting board conforms to the ARES artwork and reveals probe points at each node. The implementation of this protocol requires only a laser printer, a household iron, a drill and a FeCl₃ bath. This makes the MTB reproducible at a unit material cost of less than USD 18 in laboratories lacking commercial PCB fabrication capabilities.

4. Experimental Evaluation and Discussion

Two claims were confirmed by an experimental evaluation: The first assertion was that the analytical models presented in Section 3 accurately predict physical behavior within acceptable engineering tolerances. The second claim was that the operational functional blocks (the power stage and the primary I/O subsystems) performed in accordance with the analytical models. Bench measurements confirmed the stability of the 5.02 V rail and verified that the tested subsystems remained within their predicted timing and current margins. The measurements were made with a calibrated bench supply, a digital multimeter and an oscilloscope. These were then compared with the acceptance criteria based on the design equations.

4.1. Bench Measurements

The six main metrics were evaluated and compared with the values predicted from the governing equations described in Section 3 under full-load conditions. The 5 V rail showed 5.02 V at a load of 0.56 A, as against the expected 5.00 V for the linear-regulator model. Total input power was confirmed at 6.72 W ($12\text{ V} \times 0.56\text{ A}$), validating that the current draw remains stable. Of this input power, the measured regulator dissipation of 3.85 W (against a predicted 3.92 W) represents the primary thermal load on the PCB assembly. The difference of 0.4% is well below the acceptance criterion of $\pm 2\%$ for compatibility of TTL and CMOS logic. The LM7805 dissipation was measured at 3.85 W compared to a predicted value of 3.92 W; this validates the thermal model and the necessity of the clip-on heatsink derived from Equation (2). Bench measurements confirmed a steady-state dissipation of 3.85 W under full-load conditions, verifying the accuracy of the thermal model. Furthermore, the measured current for the LED matrix was 14.4 mA per pixel, confirming that the 220 Ω series resistors effectively regulate current within both LED and MCU per-pin limits. The multiplexed 7-segment display was refreshed at 124 Hz per digit, which is above the target 122 Hz and well above the flicker fusion threshold of 60 Hz. This confirms that the selected dwell time of 2.05 ms in Section 3.3 successfully removes perceptible flicker. The current through the LED matrix pixels was measured to be 14.4 mA versus predicted 14.1 mA. This is within the $\leq 20\text{ mA}$ limit for the PIC pin driver and the absolute max rating for the LED. The recorded keypad response latency was 51 ms, against the predicted 50.4 ms. While this metric is dominated by the 50 ms software debounce constant, the result validates the first-order accuracy of the system oscillator and confirms that the physical RC settling time (T_s) is sufficient for stable matrix scanning. The 0.6 ms deviation from the model is attributed to the execution overhead of

the Mealy state-machine transitions and the matrix-scanning loop logic. This is still well under the 100 ms ergonomic threshold for perceived responsiveness. Finally, the ADC LSB resolution was measured at 4.91 mV versus the expected 4.89 mV, validating the accuracy of 10-bit quantization. All six metrics have passed their pass criteria with deviations from predictions of less than 3% and thus confirming the predictive capability of the closed-form models discussed in this section. Table 3 illustrates the analytical predictions with the bench measurements. To ensure statistical rigor, measurements were conducted on a single fully populated prototype ($n_{\text{boards}} = 1$), with each metric calculated as the mean of $n = 10$ repeated trials. Standard deviations and instrument uncertainties were recorded to verify that experimental variance remained below the design tolerances.

Table 3. Statistical comparison of analytical predictions and bench measurements ($n = 10$).

Metric	Prediction	Measured (Avg)	Std. Dev (σ)	Instrument Uncertainty
Regulated Rail (V_{out})	5.00 V	5.02 V	± 0.004 V	± 0.01 V (DMM)
Regulator Dissipation (P_d)	3.92 W	3.85 W	± 0.021 W	± 0.05 W (Supply)
Refresh Rate (f_r)	122.0 Hz	124.0 Hz	± 0.12 Hz	$\pm 0.01\%$ (Scope)
LED Pixel Current (I_{LED})	14.1 mA	14.4 mA	± 0.08 mA	± 0.05 mA (DMM)
Keypad Latency (T_{resp})	50.4 ms	51.0 ms	± 0.25 ms	± 0.1 ms (Scope)

As summarized in Table 3, the absolute errors between modeled and measured values were precisely calculated. Despite these variations, the relative error for all six metrics remains below 3%, validating the predictive accuracy of the first-principles derivations presented in Section 3. While the regulated rail is maintained at 5.02 V, the entire system operates within a 12 V DC envelope, adhering to SELV standards for educational equipment.

4.2. Functional Verification

A special demonstration program was utilized to fully exercise each subsystem and verify that it performed properly, not only in static tests. The on-board PIC18F2550 programmer flashed and verified all Intel HEX images on both the 28-pin PIC16F877A and the 40-pin PIC18F4520 targets in the ZIF socket. This shows that both types of device can be used, as described in Section 2.6.2. The calculator firmware evaluated correctly the integer operation closures $\times$, $\div$, $+$ and $-$ for operands, displayed the results without overflow or state-machine errors and confirmed the Mealy FSM implementation described in Section 3.9.2. The multiplexed display was able to sustain a four-digit counter at the specified refresh rate with no visible flicker, thus validating the timing constraints. The LED matrix scrolled the string ‘MTB’ at 5 columns/second with constant brightness, thus confirming the 14 mA current limit and timing of row scanning. The LCD-LED scroll demonstrator successfully tracked the potentiometer sweep over the full 10-bit ADC range with smooth display updates, confirming the quantization resolution and LCD timing. No latch-up, timing violations or thermal runaway were observed in any of the subsystems during extended operation. The MTB was subjected to extended operation of the functional blocks to verify thermal stability. This demonstration confirmed that the heatsink–regulator assembly effectively manages the thermal load during high-density peripheral switching without instances of thermal runaway or latch-up.

4.3. Bill-of-Materials Cost

To check the affordability claim in Section 2.4, the unit material cost was calculated for all through-hole components. The FR-4 single-sided copper-clad board (15×15 cm)

cost USD 1.20. The active devices included one PIC18F2550 host at USD 3.50 and one PIC16F877A target at USD 4.20, which were included for demonstration purposes. The LM7805 regulator with clip-on heatsink costs USD 0.45. The peripherals were 16×2 HD44780 LCD display (USD 2.80), 8×8 LED matrix (USD 1.10), four-digit seven-segment display (USD 0.90), and a 4×4 keypad (USD 1.20). The passive parts including the 40-pin ZIF socket, USB connector, headers and 2N3904 BJTs cost USD 2.30. The total bill of materials was USD 17.65 per unit. The cost is about an order of magnitude less than comparable commercial all-in-one trainer kits, yet it offers on-board ICSP, five canonical I/O modalities, and complete signal accessibility. The cost analysis indicates that the MTB is reproducible and affordable and thus meets the criteria for implementation in low- and middle-income institutions. The BOM also includes detailed component tolerances and manufacturer identifiers to facilitate technical reproducibility. The total unit material cost for the assembly of the MTB is USD 17.65 as shown in Table 4.

Table 4. Bill of materials (BOM).

Category	Component Description	Part Number/Manufacturer (Lagos, Nigeria)	Qty	Tolerance/Spec	Cost (USD)
Active ICs	Host Microcontroller	PIC18F2550-I/SP (Microchip)	1	48 MHz, 28-DIP	3.5
	Target Microcontroller	PIC16F877A-I/P (Microchip)	1	20 MHz, 40-DIP	4.2
Power Stage	5V Linear Regulator	LM7805 (Fairchild/Generic)	1	$\pm 4\%$, TO-220	0.3
	Clip-on Heatsink	TO-220 Black Anodized	1	23 K/W	0.15
	Bulk Filter Capacitor	1000 μ F Electrolytic	1	25V, $\pm 20\%$	0.1
	Decoupling Capacitor	100 nF Ceramic	1	50V, $\pm 10\%$	0.05
Displays	Alphanumeric LCD	16×2 HD44780 (Generic)	1	4-bit mode	2.8
	8x8 LED Matrix	Common Cathode Red	1	2.0 V Vf	1.1
	7-Segment Display	4-Digit Common Cathode	1	Red, 0.56"	0.9
I/O & Analog	Matrix Keypad	4×4 Membrane/Tactile	1	10 mA max	1.2
	Potentiometer	10 k Ω Linear	2	$\pm 20\%$	0.15
Passives	Transistors	2N3904 (NPN BJT)	12	200 mA, TO-92	0.6
	Resistors	220 Ω /10 k Ω Carbon	20	0.25 W, $\pm 5\%$	0.4
Hardware	Target Socket	40-pin ZIF Socket	1	Industrial-grade	1
	PCB Substrate	FR-4 Single-sided	1	15×15 cm, 1.6 mm	1.2
TOTAL					17.65

4.4. Results and Discussion

This section interprets the results presented in Section 3 in light of the pedagogical objectives outlined in Section 2. It also examines the practical limitations that arise from the design trade-offs discussed in Sections 2–4.

4.4.1. Pedagogical Implications

The MTB makes the seven stages of the PIC development workflow described in Section 3.9.3 explicitly observable and distinct. In contrast to maker-grade platforms that hide flashing behind USB bootloaders and layers of abstraction, the on-board PIC18F2550 ICSP programmer exposes the actual programming protocol to learners. Students can probe the PGD and PGC pins to check timing, voltage levels and bit patterns of the Microchip's in-circuit serial programming protocol as specified in DS39622. This direct

visibility into the flash programming process offers an educational opportunity not available on Arduino-class hardware where the bootloader hides low-level device programming. Additionally, there are five orthogonal input/output (I/O) modalities integrated into the board: digital output via an LED matrix multiplexed display, analog input via an analog-to-digital converter (ADC), matrix input via a keypad, and serial programming via in-circuit serial programming (ICSP). These correspond directly to the canonical chapter sequence of standard embedded-systems textbooks. This agreement also helps the instructor to arrange laboratory exercises in the order of topics, thus backing up the theory with practical measurement at each level.

4.4.2. Threats to Validity and Limitations

There are three limitations of the current design that should be acknowledged. Firstly, the limitation to single-layer routing meant that only a few wire jumpers had to be used to cross traces (see the assembled board). This method ensures reproducibility in fabrication, without the need for via barrels, but it slightly increases assembly time and creates points of mechanical failure in student laboratories. Secondly, the LM7805 linear regulator is inherently inefficient; as calculated in Section 3.1, this results in a worst-case modeled dissipation of 3.92 W when supplying all five I/O subsystems. This calculation highlights the necessity of the added heatsink to maintain the 10 °C thermal margin discussed in Section 4.1. So the thermal analysis needs a heatsink to be added. A switching pre-regulator could halve dissipation and increase energy efficiency but would add costs, take more PCB space and add electromagnetic complexity. This would run counter to the objectives of transparency and affordability set out in Section 2.4. Thirdly, the choice of the 8-bit PIC architecture was due to its pedagogic clearness and deterministic timing. Nevertheless, this choice is no longer in line with the current industrial practices. The embedded market is dominated by Cortex-M ARM devices with 32-bit arithmetic, DMA, and nested interrupts that students will likely see in their future careers. This architectural difference highlights the need for the successor design described in Section 5, which aims to retain the probe-accessible philosophy while moving to a modern core. While the current validation relies on a single-prototype characterization, the low standard deviation across ten repeated trials for each metric confirms the repeatability of the system behavior. Future work will involve a multi-unit study across a student cohort to evaluate manufacturing-induced variance in the FeCl₃ etching process. Finally, the slight deviations observed in Table 3 (e.g., the 2.0 Hz difference in refresh rate) are primarily attributed to the tolerance of the timing-loop execution in the CCS-C compiler and the $\pm 5\%$ tolerance of the passive components used in the regulator and LED matrix stages. These factors account for the minor variations between the first-principles analytical models and the physical bench measurements, while remaining well within the 3% error margin. It is important to define the boundary conditions of the experimental validation. First, the reported bench measurements are derived from a high-fidelity prototype ($n = 1$) using $n = 10$ repeated measurements to characterize operational stability and timing accuracy. While this confirms the first-principles models, it does not account for manufacturing-induced variance across multiple units fabricated by different students. Second, the thermal and power validation represents a modeled 'full-load' scenario where all subsystems are verified for functionality, but the 3.92 W dissipation limit represents the peak theoretical stress on the regulator.

4.4.3. Safety and Maintainability

The design was driven by three main constraints: safety, maintainability, pedagogy and cost. The board is powered entirely by an external 12 V DC power source and consumes less than 4 W under full-load conditions. The maximum on-board potential is 12 V DC,

which is well within the SELV limit of 60 V DC for undergraduate laboratories. This ensures there is no risk of electrocution from the supply, and safety verification confirmed that no node exceeded this input voltage under any load condition. This ensures there is no risk of electrocution during manual probing or component replacement. Safety verification confirmed that no node exceeded the 12 V source voltage under any load condition. While formal ESD immunity was not tested, misinsertion risks are mitigated by the use of sockets for all active components, providing a low-cost path for field replacement of damaged silicon as per the maintainability guidelines of IEC62402. Integrating low-voltage, low-power, and socket components mitigates safety risks and total cost of ownership throughout the trainer's lifespan.

5. Conclusions and Future Work

This study concluded in the development, analytical characterization, fabrication and validation of a low-cost Microcontroller Training Board (MTB), which is intended to cover every phase of embedded hardware and firmware development. This platform is based on a single-layer through-hole PIC18F2550 architecture and with the utilization of low-cost and locally available fabrication methods the transition from theoretical modeling to bench-top implementation can be achieved. The main contributions and findings of this research are summarized as follows:

- (1) A comprehensive closed-form mathematical framework was established, which encompasses regulator thermal dissipation, ADC quantization noise, multiplexed-display refresh rates, LED forward currents, matrix-keypad scanning latency, parasitic oscillator behavior, LCD timing margins, and chemical etch kinetics. Empirical bench measurements confirmed that these predictive models align with physical behavior within a tight error margin of less than 3%.
- (2) The entire platform can be reproduced for under USD 18 in materials using off-the-shelf tools such as a common laser printer, a household iron, a hand drill and a ferric chloride (FeCl_3) etch bath. This eliminates multilayer routing and via barrels, making the platform entirely reproducible by students and resource-constrained laboratories alike. Crucially, this exposes learners to the real-world budget constraints and manufacturing trade-offs of commercial hardware engineering.
- (3) We validated the entire system with five canonical I/O modalities within a single 5 V, 0.56 A power envelope. The digital, analog and in-circuit serial programming (ICSP) subsystems worked within design tolerances with no latch-up conditions or thermal violations.
- (4) The MTB has well-placed probe nodes (unlike opaque, bootloader-dependent commercial maker boards). These enable students to directly capture PGD/PGC programming waveforms, quantify regulator thermal gradients, and analyze raw LCD bus transactions, directly mapping physical signals to standard embedded curricula chapters.

Future research will evolve the Microcontroller Test Board (MTB) in several key directions to enhance its technical relevance and pedagogical depth. First, the platform will transition to a 32-bit Cortex-M0+ host (e.g., RP2040 or STM32G0) to align with modern industrial trends, while strictly maintaining the single-layer, through-hole topology required for local student fabrication. To further improve transparency, a hardware-level USB-CDC serial console will be implemented, providing real-time exposure of internal registers, timer states, and ADC buffers without necessitating expensive external logic analyzers. Beyond these hardware upgrades, future research will involve multi-semester instructor evaluations and student performance metrics to empirically validate the board's pedagogical effectiveness and its concrete impact on learning outcomes. Finally, in line with established educational frameworks, the physical hardware will be integrated into a remote

laboratory front-end, extending the utility of the platform to geographically distributed student cohorts simultaneously.

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Abbreviations

The below table shows the list of abbreviations used in this manuscript:

Acronyms	Meaning
ADC	Analog-to-Digital Converter
BJT	Bipolar Junction Transistor
CU	Copper
DIP	Dual-Inline Packaging
DC	Direct Current
FeCl ₃	Ferric Chloride (Iron(III) Chloride)
GND	Ground
I/O	Input and Output
ICSP	In-Circuit Serial Programming
LCD	Liquid Crystal Display
MCLR	Master Clear (Reset Pin)
MTB	Microcontroller Test Board
PIC	Peripheral Interface Controller (Programmable Intelligent Computer)
PCB	Printed Circuit Board
PGC	Program Clock (In-Circuit Serial Programming Clock Line)
PGD	Program Data (In-Circuit Serial Programming Data Line)
VDD	Voltage Digital Drain
ZIF	Zero Insertion Force

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