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A Reduced-Switch Battery/Supercapacitor Hybrid Energy Storage System for Battery Current Stress Mitigation in Low-Power Electric ATVs

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Abstract

Low-power electric all-terrain vehicles (ATVs) experience repeated acceleration, grade-driving, and regenerative-braking events that impose high transient current demand on the battery pack. This study presents a reduced-switch battery/supercapacitor hybrid energy storage system (HESS) as a battery-current-stress mitigation architecture for low-power electric ATVs. Converter-level hardware tests are used to verify the voltage-regulation capability of a 500 W reduced-switch prototype, whereas vehicle-level Simulink evaluations are used to compare battery-current-stress indicators under representative ATV-oriented cycles. The proposed mode-constrained Db4 allocation strategy assigns the smoother positive demand component to the battery and fast transient and braking-related power components to the supercapacitor. Under the ATV-oriented complex cycle, the proposed HESS limits the battery current to 15 A, reduces the RMS battery current from 19.31 A to 12.45 A, decreases the maximum DC-bus voltage sag from 1.528 V to 0.523 V, and recovers 1.738 Wh of regenerative braking energy in the evaluated model. These results indicate reduced battery-current-stress indicators and improved DC-bus regulation within the evaluated operating range; direct battery aging, thermal, and cycle-life validation are outside the scope of the present work.

Keywords: battery current stress; battery/supercapacitor hybrid energy storage system; electric all-terrain vehicle; reduced-switch topology; mode-constrained power allocation; supercapacitor buffering; regenerative braking; DC-bus voltage control

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1. Introduction

Low-power electric all-terrain vehicles (ATVs) frequently operate under start–stop, climbing, obstacle-crossing, and regenerative-braking conditions. These operating conditions cause rapid variations in traction power demand, which can increase battery current stress and disturb the DC-bus voltage when the onboard storage system relies only on a battery pack. Battery/supercapacitor hybrid energy storage systems (HESSs) provide a practical route for separating energy and power functions in electric vehicles [1,2], where the battery mainly supplies the average power and the supercapacitor (SC) supports short-duration peak power and braking-energy absorption [3].

Representative battery/SC HESS topologies for DC-drive applications are shown in Figure 1 [4,5], including semi-active, dual-active, cascaded semi-active, and reduced-switch switch/diode direct-connect structures. These topologies differ in controllability, DC-link regulation capability, usable SC voltage range, switch count, and implementation cost [6]. For low-power ATVs, the central design challenge is to retain the operating flexibility required for traction and regenerative braking while avoiding excessive power devices, conduction paths, and control burden. Although high-flexibility topologies can provide strong regulation capability, their hardware complexity is not always well matched to compact low-power vehicles.

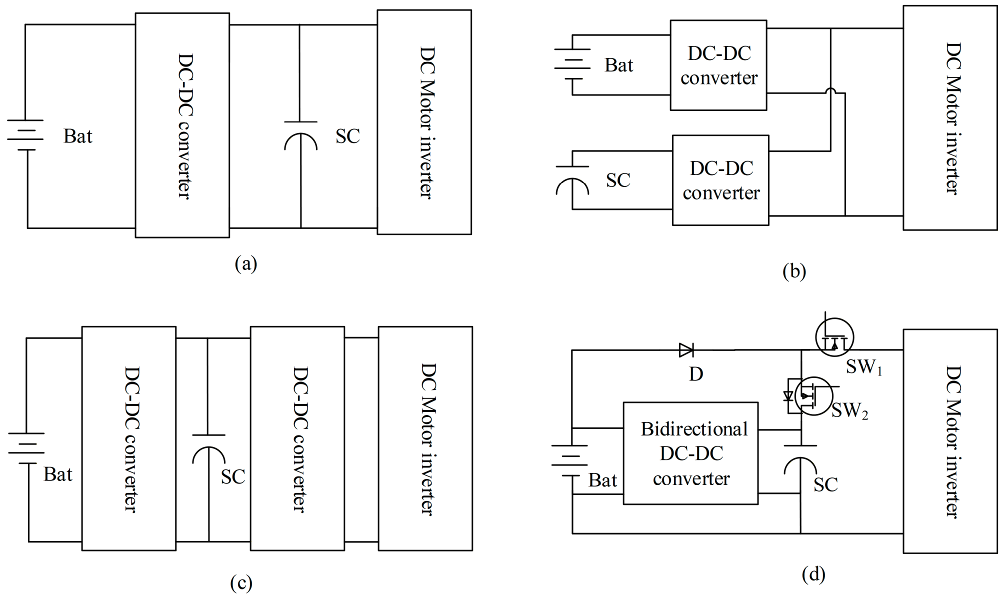

Figure 1. Representative battery/SC HESS topologies: (**a**) semi-active HESS; (**b**) dual-active HESS; (**c**) cascaded semi-active HESS; and (**d**) reduced-switch switch/diode direct-connect HESS.

This work therefore investigates the reduced-switch battery/SC HESS as a battery-current-stress mitigation architecture for low-power electric ATVs. The objective is to evaluate whether the topology and mode-constrained allocation strategy can reduce peak battery current, RMS battery current, battery charge throughput, and resistive-loss indicators while maintaining DC-bus regulation and regenerative-braking functionality.

Beyond the hardware topology, energy management is also critical because the generated power references must remain consistent with the feasible power-flow paths of the selected switching mode [7,8]. A purely frequency-based allocation may produce battery and SC power commands that cannot be implemented under the present switch state, whereas a purely threshold-based mode selector may respond insufficiently to fast transient demand [9].

The contribution of this study is threefold. First, the paper defines a reduced-switch battery/SC HESS implementation with three metal–oxide–semiconductor field-effect transistors (MOSFETs) for low-power electric ATV applications and clarifies its feasible operating modes for traction, regenerative braking, and SC restoration. Second, it combines Db4-based demand-power separation with mode and SOC constraints so that the resulting battery and SC references remain consistent with feasible power-flow paths. Third, it separates converter-level hardware validation from vehicle-level model-based evaluation, allowing the voltage regulation capability of the prototype and the battery-current-stress indicators of the ATV-HESS model to be assessed without conflating the two validation levels.

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The remainder of this paper is organized as follows. Section 2 describes the proposed topology, operating modes, energy-management strategy, converter controller, prototype platform, and simulation model. Section 3 presents converter-level hardware results and vehicle-level model-based evaluation results. Section 4 discusses the engineering implications and limitations, and Section 5 concludes the paper.

2. Materials and Methods

2.1. Low-Power Electric ATV Application Scenario

The target platform is a low-power electric ATV supplied by a 48 V DC bus. The application scenario emphasizes frequent acceleration, short high-load intervals, grade driving, and regenerative braking rather than sustained high-speed cruising. The design therefore prioritizes transient-power buffering, battery-current limitation, safe regenerative-energy absorption, and reproducible converter-level validation on a 500 W prototype.

2.2. Reduced-Switch Battery/Supercapacitor HESS Topology

In the design of HESSs for low-power ATVs, the battery is intended to supply the relatively smooth average power, whereas the supercapacitor is responsible for providing or absorbing the additional transient power demanded by the motor inverter [10]. For compact low-power platforms, reducing the number of controllable switches can simplify the circuit structure, gate-drive requirements, and control implementation. Following these design principles, a simplified cascaded multimode HESS is developed. The configuration of the proposed topology is illustrated in Figure 2. As shown, the system adopts a parallel connection between the battery and the supercapacitor and employs three MOSFET switches (SW1, SW2, and SW3). Additionally, a diode (D) is incorporated to prevent reverse current flow and enhance battery safety.

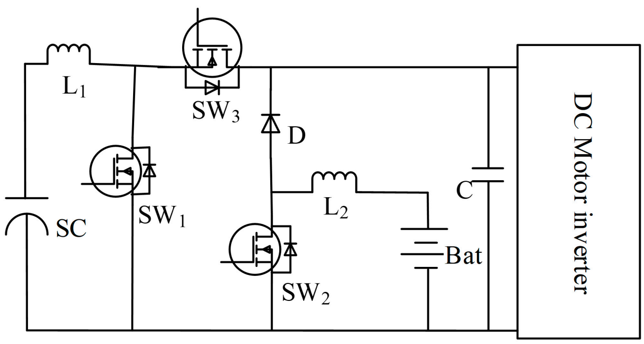

Figure 2. Topology of the proposed reduced-switch HESS.

The proposed simplified cascaded multimode HESS operates as a boost converter when energy flows from the HESS to the motor inverter and as a controlled charging path when regenerative braking energy is recovered from the motor inverter and stored in the supercapacitor. The main advantage of this topology is that it preserves the key power-flow functions required for traction, regenerative-energy absorption, hybrid output, and SC restoration while using fewer controllable switching paths. The detailed efficiency and thermal effects depend on the actual conduction paths, device characteristics, and operating conditions, and are therefore reserved for future experimental characterization.

2.3. Operating Modes and Feasible Power-Flow Paths

The gates of the MOSFETs are driven using a pulse-width modulation (PWM) technique, which generates a square waveform with a fixed switching frequency. By adjusting the duty cycles of the PWM signals applied to the three MOSFETs (SW1, SW2, and SW3), multiple operating modes can be achieved to satisfy the dynamic requirements of ATV operation.

In practical operation, SW3 is used in the operating modes that require an SC-charging path, namely regenerative braking in Mode I and battery-assisted SC restoration in Mode V. It remains off in Modes II–IV, where the HESS supplies positive traction power without charging the SC branch.

For regenerative braking, effective buck-type charging of the SC requires the rectified braking-side DC voltage to exceed the instantaneous SC terminal voltage. When the braking-side voltage is lower than, or close to, the SC voltage, the recoverable SC charging current is naturally limited by the available voltage headroom and the mode-selection logic prevents overcharging.

During normal ATV operation—such as starting, acceleration, idling, or climbing—the HESS delivers positive output power. In this case, SW3 remains completely off (duty cycle = 0), and the system operates in the boost mode. According to the power-distribution strategy, appropriate duty-cycle settings of SW1 and SW2 allow independent boost outputs from the battery and the SC, respectively.

When the SC SOC is sufficiently high, the system operates in an SC-only output mode, in which SW2 and SW3 are turned off and SW1 is pulse-controlled to boost the SC voltage, as shown in Figure 3b. Conversely, when the SC SOC is low and the battery remains available, the battery-only mode is engaged to maintain DC-bus power supply while disabling SC discharge and charging. In this case, SW1 and SW3 are turned off, and SW2 is pulse-controlled to boost the battery output, as illustrated in Figure 3c.

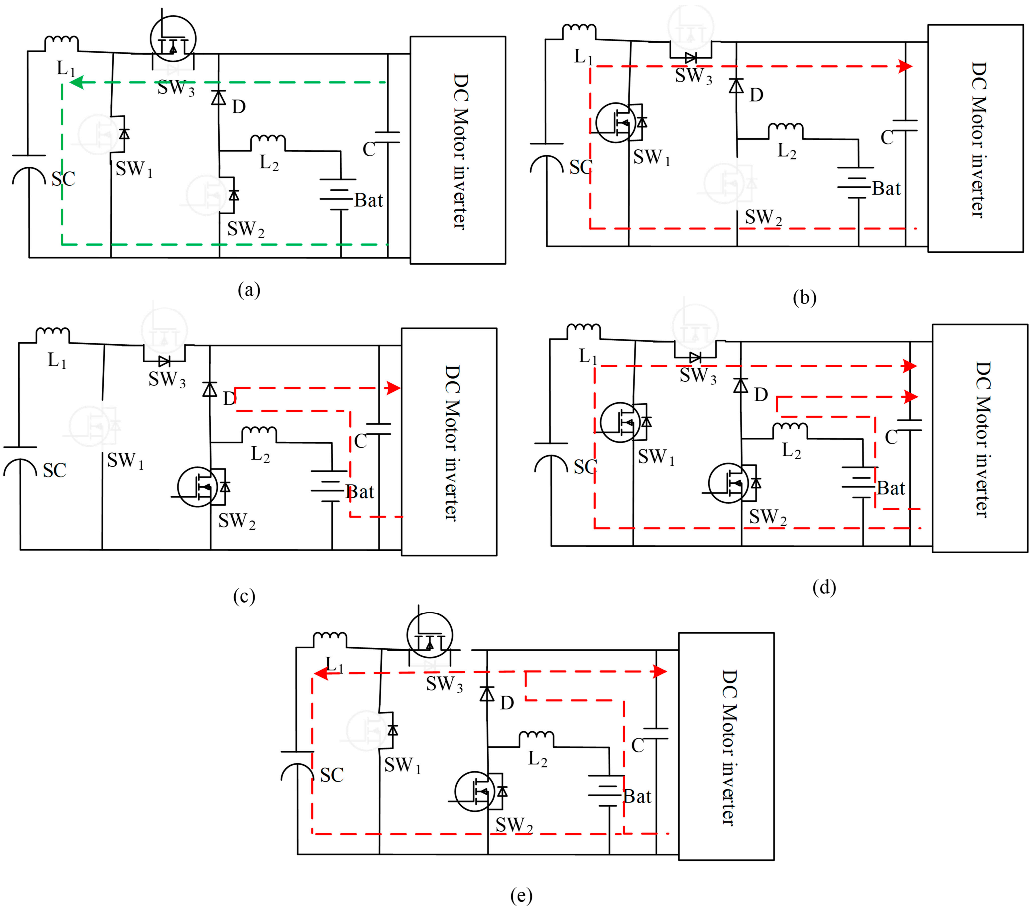

Figure 3. Operating modes of the proposed reduced-switch HESS: (**a**) regenerative-energy absorption; (**b**) SC-only output; (**c**) battery-only output; (**d**) hybrid output; and (**e**) battery output with SC

restoration. Red dashed arrows indicate traction/discharge power-flow paths, and green dashed arrows indicate regenerative or SC-charging power-flow paths.

The combined output mode of the battery and SC serves as the principal operating mode of the proposed reduced-switch HESS, as depicted in Figure 3d. Here, SW3 remains off, while SW1 and SW2 are simultaneously modulated to achieve joint boosting and battery current limitation. The duty-cycle ratios of SW1 and SW2 are determined according to the power-distribution strategy, ensuring that the battery provides the average power and the SC delivers the transient peak power.

When the supercapacitor SOC is low and the traction demand is moderate, the system enters the battery-output with supercapacitor-charging mode, as shown in Figure 3e. In this mode, SW1 is turned off, SW3 provides the SC-restoration path, and SW2 is pulse-controlled so that the battery supplies the load while transferring only the permitted restoration current to the SC. The restoration command is constrained by the DC-bus requirement, the SC current limit, and the SC SOC upper threshold to avoid coupling the load supply and SC charging in an uncontrolled manner.

The operating conditions, switching states, main power-flow paths, and functions of the five modes are summarized in Table 1.

Table 1. Operating modes and switching states of the proposed reduced-switch HESS.

Mode	Condition	SW1	SW2	SW3	Main Power Flow	Function
I	$P_{dem} < 0$ and SC has voltage headroom	Off	Off	PWM	Motor inverter -> SC	Regenerative-energy absorption
II	Battery SOC low, SC SOC sufficient	PWM	Off	Off	SC -> DC bus	SC-only output
III	SC SOC low, battery available	Off	PWM	Off	Battery -> DC bus	Battery-only output
IV	Normal positive demand	PWM	PWM	Off	Battery + SC -> DC bus	Hybrid output
V	SC SOC low and moderate traction demand	Off	PWM	On/PWM	Battery -> load + SC	SC restoration

In Mode V, SW3 provides the SC-restoration path and may remain on or be pulse-controlled according to the required SC-restoration current.

2.4. Mode-Constrained Energy Management Strategy

The energy management system (EMS) is the system-level coordination unit of the proposed HESS [11]. It integrates hardware modules, including the data-acquisition circuit, voltage/current sensing units, and STM32 controller, with software functions including SOC estimation, mode selection, and power allocation. In the vehicle-level evaluation, battery SOC is updated by current integration using the simulated battery current, while SC SOC is calculated from the voltage-squared energy relationship of the SC pack. The SOC values are then used only as control-state variables for mode selection and constraint enforcement, not as direct health indicators. The overall energy-management structure of the proposed reduced-switch HESS is shown in Figure 4.

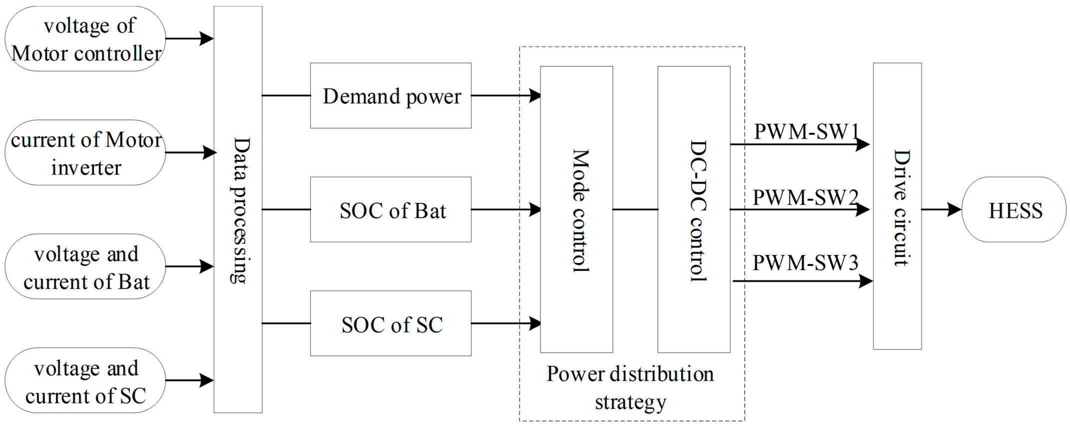

Figure 4. Energy-management structure of the proposed reduced-switch HESS.

The proposed reduced-switch HESS operates in five distinct modes. Selecting an appropriate operating mode that corresponds to the current driving condition is critical to the effectiveness of the power-allocation strategy. Because the energy-flow direction varies among operating modes, mode transitions must be coordinated with the feasible power-flow paths of the circuit. Even within a single mode, the power-distribution ratio between the battery and the supercapacitor may differ depending on instantaneous power demands.

DC–DC converter control is also essential for implementing the selected energy-management command. Once the operating mode is determined, the switching-device control performance directly affects the accuracy and stability of battery/SC power distribution. Therefore, a well-tuned converter controller is required to translate the supervisory power-allocation strategy into stable switch-level operation.

2.4.1. Mode Selection and Power-Flow Constraints

The conventional rule-based mode-selection method typically defines fixed logical thresholds as criteria for determining the operating mode based on the required power demand and the states of the battery and supercapacitor. This approach offers simplicity, real-time performance, and ease of implementation; however, it lacks detailed analysis of the required power, particularly under conditions where both the battery and the supercapacitor operate simultaneously. Recent studies have further incorporated driving-pattern recognition and wavelet-fuzzy energy management into battery-supercapacitor systems to improve power sharing under variable electric-vehicle operating conditions [12].

To enhance the utilization efficiency of the energy storage components, a comprehensive power-allocation strategy is proposed, which jointly considers the battery state, the supercapacitor state, and the instantaneous power demand [13]. First, mode-selection rules are formulated according to the states of the battery and the supercapacitor [14]. Subsequently, wavelet transform analysis is applied to decompose the required power into distinct frequency components, enabling further optimization of the power-allocation process [15].

The mode-selection logic and detailed control rules for the proposed reduced-switch HESS are illustrated in Figure 5. When the demand power is negative, regenerative braking energy is preferentially absorbed by the supercapacitor as long as voltage and SOC headroom are available. When the SC approaches its upper SOC or voltage limit, the admissible SC charging reference is reduced by the constraint projection rather than being applied directly. This treatment keeps the wavelet-based reference consistent with the feasible power-flow path of the selected mode.

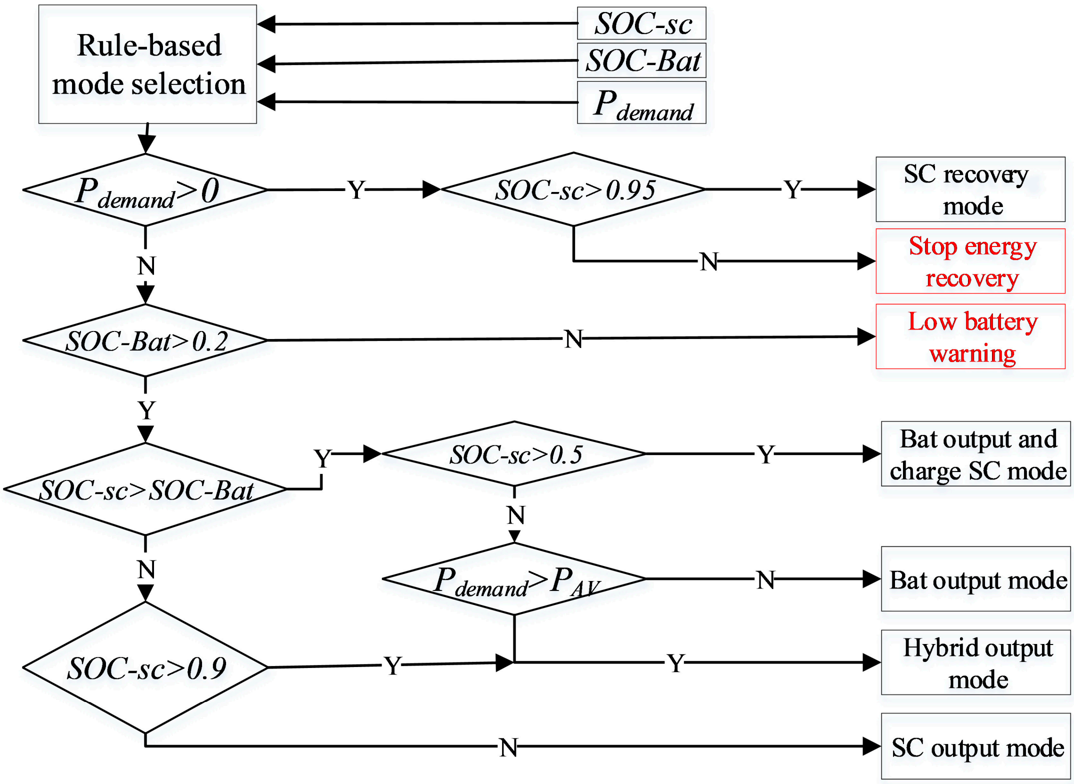

Figure 5. Mode-selection and control rules of the proposed reduced-switch HESS. Red boxes indicate SOC-boundary protection actions.

When the demand power is positive, the mode selection is primarily determined by the SOCs of both the battery and the supercapacitor.

The battery-only mode, supercapacitor-only mode, and battery-output with supercapacitor-charging mode are considered extreme operating conditions, applicable when either the battery or the supercapacitor exhibits low available power. Under normal conditions, the proposed reduced-switch HESS primarily operates in the combined output mode, in which both the battery and the supercapacitor deliver power simultaneously. The specific power contribution of each component in this mode must be further analyzed and allocated according to the real-time power demand to achieve optimal energy utilization.

2.4.2. Db4 Wavelet-Based Power Allocation

The wavelet transform (WT) is adopted to separate the nonstationary ATV demand-power signal into relatively smooth and fast-varying components. In the proposed strategy, WT is not used for strict spectral partitioning but rather to assign the smoother demand component to the battery and the fast transient and braking-related components to the supercapacitor according to their dynamic characteristics.

Among common wavelet bases, including Haar, Daubechies, Coiflets, and Symlets, the Daubechies-4 (Db4) wavelet is selected because the ATV demand-power signal contains abrupt variations during start-up, climbing, and braking events. With compact support, orthogonality, and sensitivity to discontinuities, Db4 is suitable for separating the low-frequency demand trend from fast transient fluctuations in this application.

The decomposition level is set to three as a compromise between separation capability and implementation complexity. In the vehicle-level implementation, the approximation component A3 is interpreted as the low-frequency demand trend, whereas D3, D2, and D1 represent progressively faster transient components. The positive portion of A3 is assigned to the battery, while the faster fluctuating components are assigned to the supercapacitor for transient-power support and regenerative-energy absorption. The preliminary references are then projected onto current, voltage, SOC, and mode constraints before switch commands are generated. Therefore, the reported vehicle-level results should be interpreted as Simulink-based evaluations of the proposed allocation logic. For embedded deployment, the same principle can be implemented through a causal finite-buffer or sliding-window realization, with buffer length, decomposition delay, and computation time selected according to the target controller hardware.

The Db4 decomposition generates intermediate battery and SC power references rather than direct switch commands. These references are constrained by the selected operating mode, SOC limits, current limits, and DC-bus voltage requirements before being converted into PWM commands [16]. This mode-constrained step prevents the controller from requesting battery or SC power paths that are unavailable under the current switching state. The proposed mode-constrained Db4-based battery/SC power allocation procedure is summarized in Algorithm 1.

Algorithm 1. Mode-Constrained Db4-Based Battery/SC Power Allocation

Input: Demand power $P_{dem}(k)$, battery SOC, supercapacitor SOC, DC-bus voltage $V_{dc}(k)$, current limits, voltage limits, and mode thresholds.

1: Determine the admissible operating mode from the signs of $P_{dem}(k)$, battery SOC, supercapacitor SOC, and the headroom available for regenerative braking.

2: Apply a three-level Db4 decomposition to the demand-power sequence and obtain the smooth approximation component and fast detail components.

3: Assign the smooth positive component to the battery reference and assign fast positive transients and braking-related negative power to the supercapacitor reference.

4: Project the preliminary references onto the admissible power-flow paths of the selected mode and enforce battery-current, supercapacitor-current, SOC, and DC-bus voltage constraints.

5: Convert the constrained battery/SC power references into feasible switch-level commands for SW1, SW2, and SW3 in the Simulink model; embedded implementation requires causal buffering and delay assessment.

Output: Mode-consistent battery and supercapacitor power references and switching commands. The algorithm is therefore used in this paper as a mode-consistent allocation procedure for vehicle-level model evaluation, while real-time embedded optimization and experimental latency validation are treated as future implementation tasks.

The mathematical expressions for the Db4 wavelet and its corresponding scaling function are given as follows:

$$C[i] = g_0 s[2i] + g_1 s[2i+1] + g_2 s[2i+2] + g_3 s[2i+3] \quad (1)$$

$$a[i] = h_0 s[2i] + h_1 s[2i+1] + h_2 s[2i+2] + h_3 s[2i+3] \quad (2)$$

where $g_0 = h_3, g_1 = -h_2, g_2 = h_1, g_3 = -h_0$ and $h_0 = \frac{1+\sqrt{3}}{4\sqrt{2}}, h_1 = \frac{3+\sqrt{3}}{4\sqrt{2}}, h_2 = \frac{3-\sqrt{3}}{4\sqrt{2}}, h_3 = \frac{1-\sqrt{3}}{4\sqrt{2}}$.

The Db4 wavelet transform is employed to perform a three-level decomposition of a UDDS-based demand-power signal. This example is intended to illustrate the low-/high-frequency separation process of the proposed wavelet-based power-allocation strategy, rather than to serve as the final vehicle-level validation cycle. The UDDS-based profile includes typical urban-driving features such as repeated start-up, low-speed cruising, acceleration, deceleration, braking, and idling. The decomposition result is shown in Figure 6.

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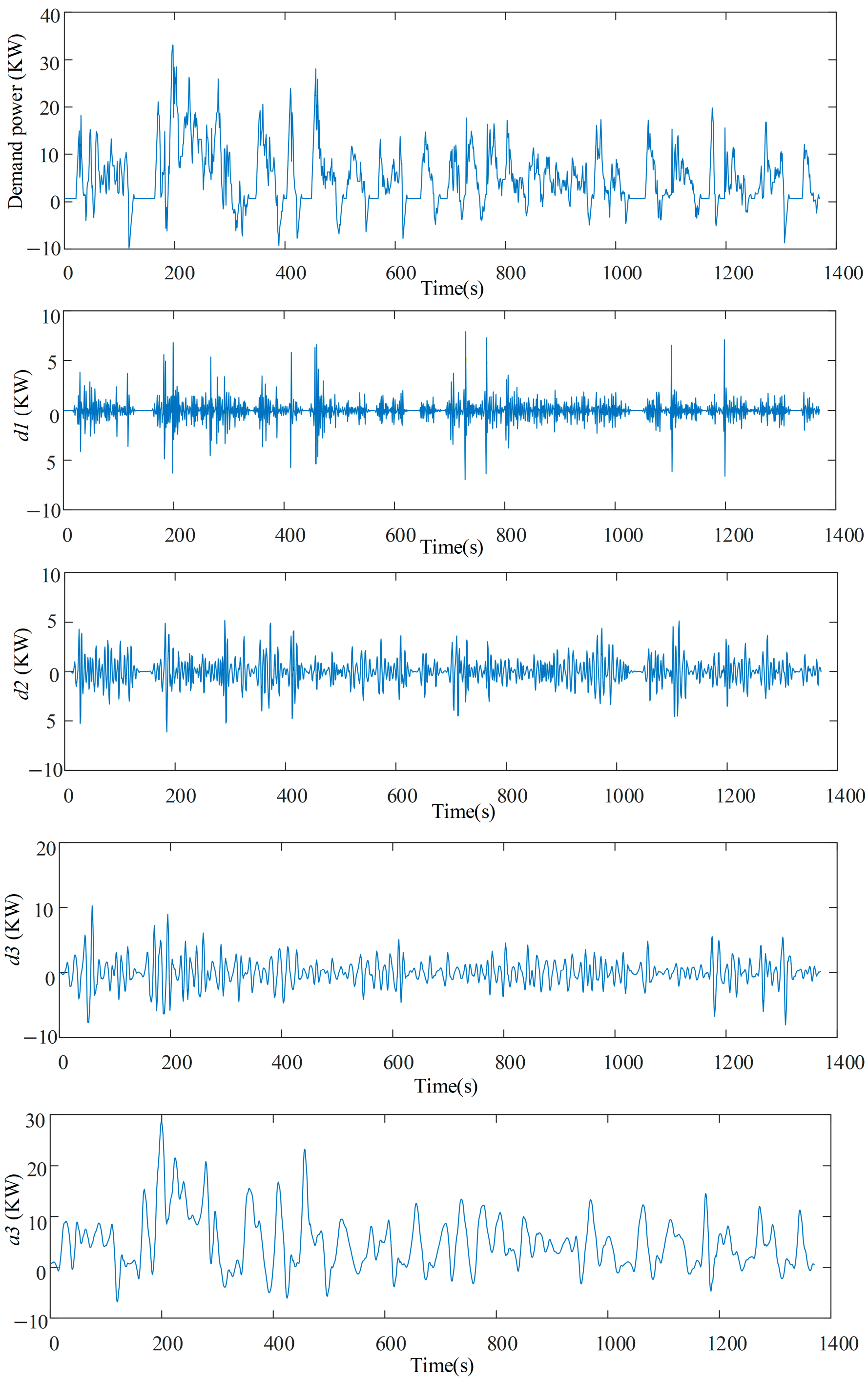

Figure 6. Db4 wavelet decomposition of UDDS-based demand power.

As shown in Figure 6, the approximation component A3 represents the relatively smooth low-frequency trend of the demand power, while D3, D2, and D1 represent progressively faster fluctuating components. In the proposed allocation strategy, the positive part of A3 is assigned to the battery, whereas the high-frequency components and the negative portions associated with braking are assigned to the supercapacitor. It should be noted that these detail components are intermediate decomposition results rather than the final supercapacitor power commands. The final battery and supercapacitor power commands are obtained through the following recombination rules:

$$\begin{cases} P_{\mathrm{Bat}} = a_3^+ \\ P_{\mathrm{SC}} = a_3^- + d_1 + d_2 + d_3 \end{cases} \quad (3)$$

where P_{bat} and P_{sc} denote the power supplied by the battery and the supercapacitor, respectively.

2.5. Converter-Level DC-Bus Voltage Control

When the battery or the supercapacitor supplies power to the load, power transfer is implemented through the DC–DC converter. Therefore, converter control provides the actuator-level basis for the realization of the proposed power-allocation strategy. Because the boost converter exhibits nonlinear dynamics, a conventional proportional–integral controller is insufficient to guarantee the desired transient voltage-regulation performance under rapid start-up and load-disturbance conditions [17,18]. For the proposed reduced-switch HESS, the boost operating mode is the dominant traction-side operating condition; therefore, this section focuses on the control design of the boost converter shown in Figure 7. The controller design is described in terms of state error definition, sliding-surface construction, and stability-constrained parameter selection.

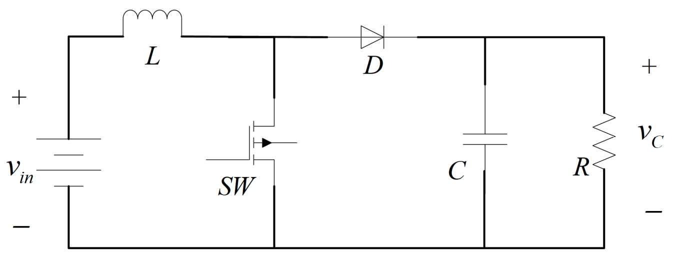

Figure 7. Equivalent DC–DC boost converter.

Following robust tracking and sliding-mode control principles for battery/supercapacitor HESSs in electric vehicles [19,20], the conventional terminal sliding-mode controller is referred to as the baseline TSMC in this study, whereas the improved controller is referred to as the proposed variable-terminal-exponent sliding-mode controller. The proposed controller retains the sliding-mode control framework and introduces a variable terminal exponent to improve the transient response under start-up and load-disturbance conditions.

$$S = i_L(t) + k_1 v_C + k_2 \int_0^t e_v{}^{\gamma} d\tau \tag{4}$$

where S is the sliding surface, $i_L(t)$ is the inductor current, v_C is the output capacitor voltage, e_v is the voltage tracking error, k_1 and k_2 are positive constants, γ is the terminal order and $0 < (\gamma = p/q) < 1$. The controller parameters are selected within a stability-constrained admissible range and are then tuned according to convergence speed, overshoot limitation, and disturbance-rejection requirements.

Selecting the Lyapunov function as

$$V = \frac{1}{2} S^2 \tag{5}$$

To satisfy the Lyapunov reaching condition, S and its time derivative should satisfy $S\dot{S} < 0$ in the vicinity of the sliding surface.

when $u = 1$, $S < 0$, so we need $\dot{S} > 0$

$$\frac{v_{in}}{L} - k_1 \frac{v_C}{RC} + k_2 (v_C - v_{ref})^{\gamma} > 0 \tag{6}$$

when $u = 0$, $S > 0$, so we need $\dot{S} < 0$

$$\frac{v_{in}-v_C}{L}+k_1\left(\frac{i_L}{C}-\frac{v_C}{RC}\right)+k_2(v_C-v_{ref})^{\gamma}<0 \tag{7}$$

By considering the limiting cases of the terminal exponent and the inductor-current state, an admissible range of the controller parameters can be obtained from the Lyapunov sign conditions.

The impact of terminal power γ on the dynamic performance of system control is inconsistent during start-up and load changes. In general, when e_v is near the equilibrium point, it can be seen as $|e_v|<1$, the terminal power leads to $|e_v{}^{\gamma}|>|e_v|$. This means the system state with the nonlinear term e_v^{γ} converges toward the equilibrium point faster than the linear term e_v. In addition, there are many cases where $|e_v|>1$, such as when the start-up, load, or input voltage changes greatly. In this case, the terminal power leads to $|e_v{}^{\gamma}|<|e_v|$. This means the system state with the nonlinear term e_v^{γ} converges toward the equilibrium point slower than the linear term e_v.

To select a practical terminal exponent for the converter controller, the terminal power term is parameterized as

$$\gamma=\frac{1}{\pi}\arctan(ae_v-b)+c \tag{8}$$

where a, b and c are positive real-valued tuning parameters. In this study, they are selected within stability-constrained ranges and then tuned according to the desired transient response and oscillation-suppression requirements of the converter system.

2.6. Prototype Platform and System-Level Simulation Model

To verify the feasibility of the proposed simplified HESS, a 500 W low-power prototype was designed and fabricated. As shown in Figure 8, the prototype integrates the main circuit topology in Figure 2 with auxiliary modules, including an STM32 MCU system, MOSFET driver circuit, voltage/current sensing circuits, auxiliary power supply, and PWM optocoupler isolation circuit.

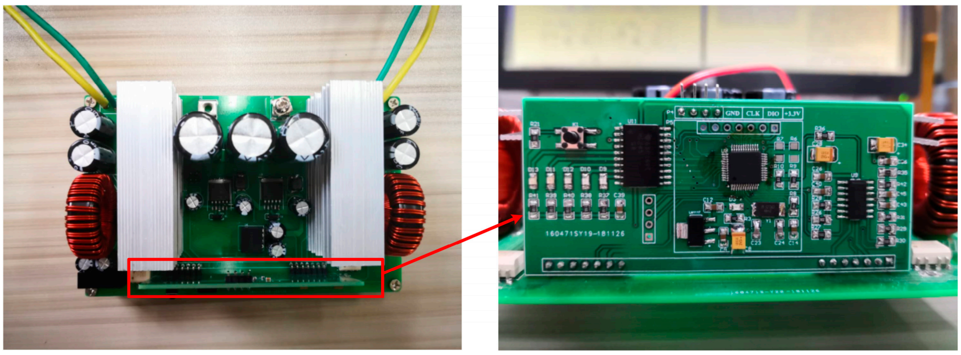

Figure 8. Low-power prototype of the proposed reduced-switch HESS.

The STM32 microcontroller system primarily implements the control of the DC–DC converter. Specifically, three pulse-width modulation (PWM) signals are generated according to the designed control strategy and applied to the MOSFET power switches SW1, SW2, and SW3, thereby enabling mode switching and power distribution. To facilitate circuit hardware testing and software debugging, five mode-indicator LEDs and manual mode-selection switches are incorporated, allowing verification under different operating conditions. Additionally, four I/O ports are reserved for connection with an ARM-based control platform to enable future functional expansion.

The MOSFET driver circuit employs a TLP352 gate driver optocoupler. The voltage and current measurement units are composed of TL084 and OP07CN operational amplifiers, respectively. The current-sensing circuit adopts a second-order amplifier configuration for signal acquisition and isolation, with a maximum measurable current of 30 A. The auxiliary power supply provides operating power for the STM32 system and other active components. The PWM optocoupler isolation circuit is implemented using a 74LVC245 tri-state octal transceiver, pull-down resistors, and optocoupler diodes, which together perform signal isolation and level conversion for the PWM signals output by the STM32.

Based on the low-power prototype, converter-level validation is carried out through DC–DC voltage-regulation tests under start-up and load-disturbance conditions. In addition, the component parameters of the prototype are used to establish a Simulink-based vehicle-level average model for evaluating the proposed energy-management strategy under representative ATV-oriented operating cycles. To clarify the different evidence roles of the converter-level hardware tests and the vehicle-level model-based evaluations, the validation scope is summarized in Table 2. The converter-level prototype test setup is illustrated in Figure 9, and the main system parameters used for the prototype test and vehicle-level simulation are summarized in Table 3.

Table 2. Validation scope of the converter-level hardware tests and vehicle-level model-based evaluation.

Validation Level	Method	Main Object	Verified or Evaluated Content
Converter-level validation	500 W hardware prototype	Reduced-switch DC–DC converter	Start-up response and load-disturbance voltage regulation
Vehicle-level evaluation	Simulink ATV-HESS model	Battery/SC power sharing and EMS	Battery-current-stress indicators, DC-bus regulation, and regenerative-energy behavior

Table 3. Main system parameters.

Component	Parameter	Value
Prototype	Rated power	500 W
DC bus	Reference voltage	48 V
Vehicle	Mass	380 kg
Battery	Type	$LiFePO_4$
Battery	Nominal voltage/capacity	48 V/18 Ah
Battery	Current limit/internal resistance	25 A/0.06 Ω
Supercapacitor	Configuration	8 cells in series
Supercapacitor	Rated voltage	50 V
Supercapacitor	Equivalent capacitance of the SC pack	280 F
Supercapacitor	Current limit/equivalent internal resistance	120 A/0.003 Ω

As shown in Table 2, the converter-level hardware test is used to verify the DC–DC voltage-regulation capability, whereas the vehicle-level Simulink model is used to evaluate energy-management behavior and battery-current-stress indicators. The setup in Figure 9 is not used as evidence for ATV-level road-test or full vehicle-level hardware validation; the subsequent vehicle-level results are model-based Simulink evaluation results.

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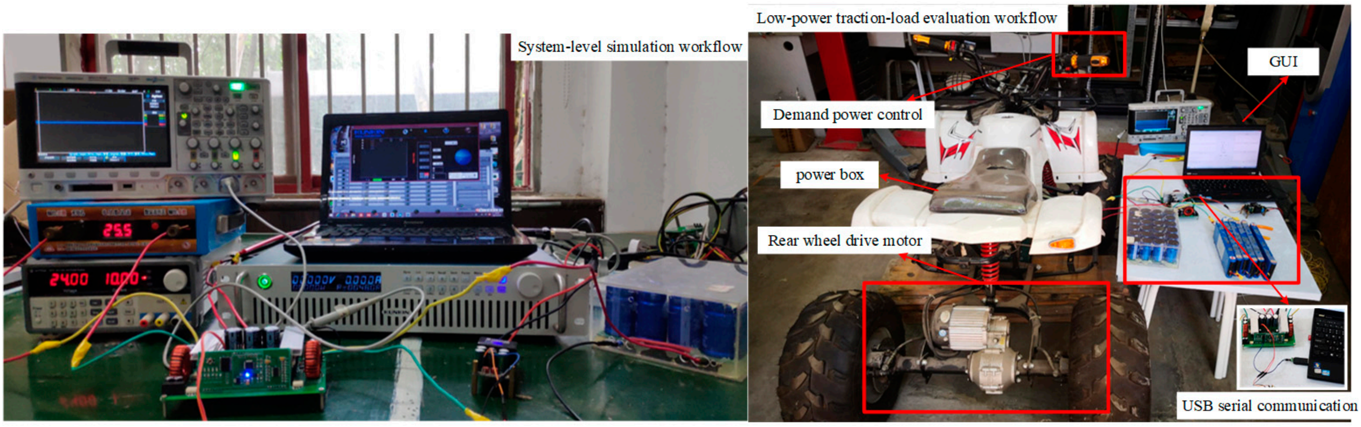

Figure 9. Converter-level prototype test setup of the proposed reduced-switch HESS.

The supercapacitor pack is composed of eight cells connected in series. Its theoretical maximum stored energy can be calculated as

$$E_{\mathrm{SC,max}} = \frac{1}{2} C_{\mathrm{SC,eq}} V_{\mathrm{SC}}^2 \tag{9}$$

For the adopted pack-level parameters of $C_{\mathrm{SC,eq}}$ = 280 F and V_{SC} = 50 V, the theoretical stored energy is approximately 350 kJ, corresponding to about 97.2 Wh. This energy level is suitable for transient peak-power buffering and regenerative-energy absorption rather than sustained traction supply.

The parameters listed in Table 3 are selected to match the hardware prototype and the target low-power ATV application scenario. The converter-level prototype test is used to evaluate the dynamic voltage-regulation performance of the DC–DC converter, whereas the vehicle-level Simulink model is used to evaluate the proposed energy-management strategy and compare different energy-storage configurations. The vehicle-level model includes the battery and supercapacitor equivalent models, DC-bus voltage dynamics, vehicle longitudinal dynamics, wavelet-based power allocation, and operating-mode selection logic. Therefore, the following validation section distinguishes the converter-level hardware measurements from the vehicle-level model-based simulation results.

2.7. Battery-Current-Stress and DC-Bus Evaluation Metrics

To evaluate battery-current-stress mitigation and DC-bus regulation performance, all vehicle-level configurations are assessed over the same driving window. The battery-side indicators include the peak battery current $I_{\mathrm{b,pk}}$, RMS battery current $I_{\mathrm{b,rms}}$, battery charge throughput Q_{through}, and estimated battery resistive-loss energy $E_{\mathrm{loss,b}}$. Here, $I_{\mathrm{b,pk}}$ is defined as the maximum absolute battery current during the evaluated cycle, while $I_{\mathrm{b,rms}}$ represents the RMS value of the battery current.

The battery charge throughput is calculated from the absolute battery current as

$$Q_{\mathrm{through}} = \frac{1}{3600} \int_0^T \left| I_{\mathrm{b}}(t) \right| dt \tag{10}$$

and the estimated battery resistive-loss energy is calculated as

$$E_{\mathrm{loss,b}} = \frac{R_{\mathrm{b}}}{3600} \int_0^T I_{\mathrm{b}}^2(t) dt \tag{11}$$

where $I_b(t)$ is the battery current, R_b is the equivalent internal resistance of the battery pack, and T is the duration of the evaluated cycle. $Q_{through}$ is expressed in Ah, while $E_{loss,b}$ is expressed in Wh. The DC-bus voltage sag, RMS DC-bus voltage deviation, and recovered regenerative braking energy are also reported as system-level indicators. These indicators are used to quantify electrical current stress and regulation performance; they are not treated as direct state-of-health, capacity-fade, or cycle-life measurements. The numerical precision reported in the tables follows the simulation data-export format and the post-processing resolution used for indicator calculation. It should be interpreted as model-based indicator precision rather than vehicle-level hardware measurement accuracy.

3. Results

To evaluate the proposed HESS from a battery-current-stress and system-regulation perspective, the results are organized into six parts. Section 3.1 reports converter-level DC-bus voltage regulation. Section 3.2 evaluates UDDS-based battery-current mitigation. Section 3.3 presents the ATV-oriented complex cycle and supercapacitor buffering behavior. Section 3.4 compares battery-current-stress, DC-bus, and regenerative-energy indicators. Section 3.5 tests sensitivity to the initial supercapacitor SOC. Section 3.6 verifies mode coverage under SOC-boundary conditions.

The converter-level results in Figure 10 are obtained from hardware measurements, whereas the vehicle-level results in Figures 11–16 are model-based Simulink simulation results using the component and vehicle parameters listed in Table 3. The vehicle-level results are therefore interpreted as current-stress and control-performance indicators rather than direct battery-aging measurements.

3.1. Converter-Level DC-Bus Voltage Test

The converter-level prototype test is performed on the 500 W hardware platform to evaluate the DC–DC voltage-regulation performance during start-up and sudden load disturbances. Figure 10 compares the dynamic responses of the baseline TSMC and the proposed variable-terminal-exponent sliding-mode controller under the same prototype conditions.

As shown in Figure 10a, the TSMC-based controller produces an evident start-up overshoot, with the peak voltage reaching approximately 58–60 V before settling near the 48 V reference. In contrast, the proposed controller in Figure 10c reaches the steady-state voltage with a much smaller overshoot. Under the sudden load-change condition shown in Figure 10b,d, both controllers maintain voltage regulation, while the proposed controller shows smaller voltage fluctuation and faster recovery. These results indicate improved transient regulation and disturbance-rejection capability for the boost converter.

3.2. UDDS-Based Battery Current Stress Mitigation

The official UDDS speed trace is adopted as the baseline urban stop-and-go pattern. Because the maximum speed of the original UDDS trace exceeds the rated speed range of the considered low-power electric ATV, the speed amplitude is scaled to 30 km/h while preserving the original UDDS time sequence and frequent acceleration–deceleration characteristics. The scaled velocity is obtained by linearly normalizing the original UDDS speed trace as

$$v_{ATV}(t) = \frac{v_{max,ATV}}{v_{max,UDDS}} v_{UDDS}(t) \tag{12}$$

where $v_{\max,\mathrm{ATV}}$ is set to 30 km/h, and $v_{\max,\mathrm{UDDS}}$ is the maximum speed of the original UDDS trace.

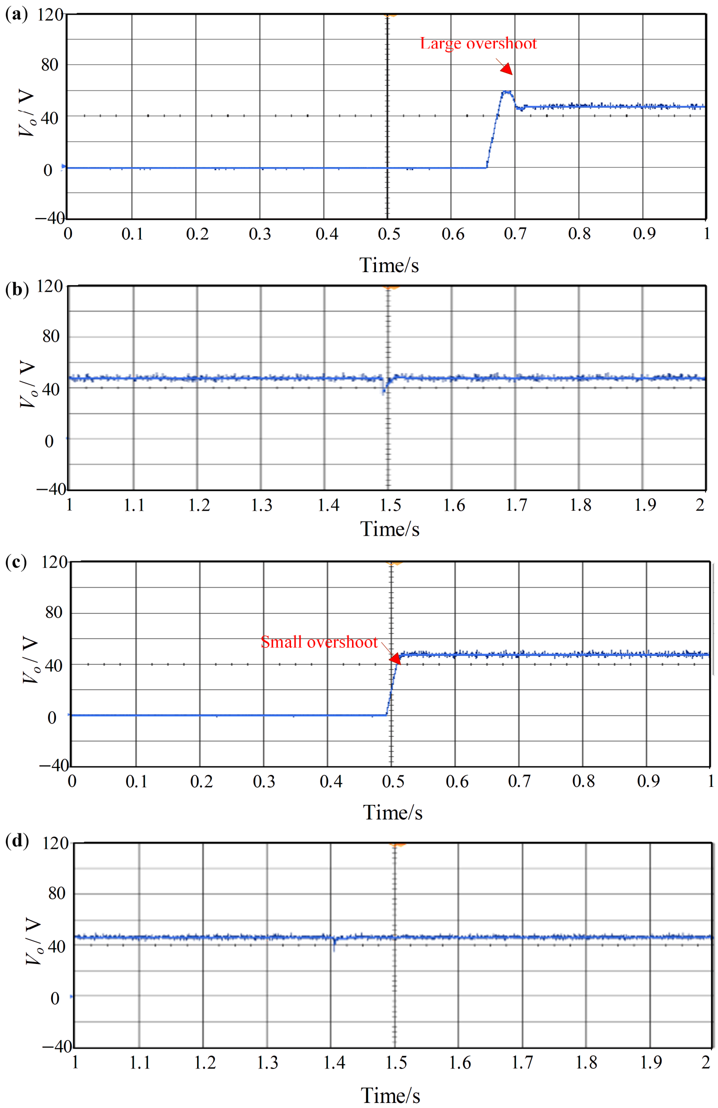

Figure 10. Experimental comparison of the baseline TSMC and the proposed variable-terminal-exponent sliding-mode controller for the boost converter: (**a**) start-up voltage response under baseline TSMC; (**b**) voltage response under baseline TSMC after a sudden load change; (**c**) start-up voltage response under the proposed controller; and (**d**) voltage response under the proposed controller after a sudden load change. The blue curves denote the measured output-voltage responses, the red annotations indicate overshoot-related regions, and the vertical dashed reference lines mark the start-up or sudden-load-change instant.

The traction demand power is calculated from the longitudinal vehicle dynamics model:

$$P_{\mathrm{dem}}(t) = \frac{v(t)}{\eta_{\mathrm{d}}}\left[m\frac{dv(t)}{dt} + mgf_{\mathrm{r}} + \frac{1}{2}\rho C_{\mathrm{d}} A v^2(t) + mg\sin\theta(t) \right] \tag{13}$$

where m is the vehicle mass, f_{r} is the rolling-resistance coefficient, ρ is the air density, $C_{\mathrm{d}}A$ is the equivalent aerodynamic drag area, η_{d} is the drivetrain efficiency, and

$\theta(t)$ is the road slope angle. For the ATV-scaled UDDS-derived cycle, $\theta(t) = 0$. For the ATV-oriented complex cycle, $\theta(t)$ is determined from the prescribed grade profile.

Using this model and the vehicle parameters listed in Table 3, the scaled speed profile is converted into the traction demand power shown in Figure 11a. Unlike the UDDS-based demand-power signal used in Section 2.4.2—only to illustrate the wavelet-decomposition process—the present cycle is an ATV-scaled UDDS-derived urban cycle used for vehicle-level comparative validation. In this cycle, the original UDDS time sequence and stop-and-go characteristics are preserved, while the speed amplitude is scaled to match the rated speed range of the considered low-power ATV.

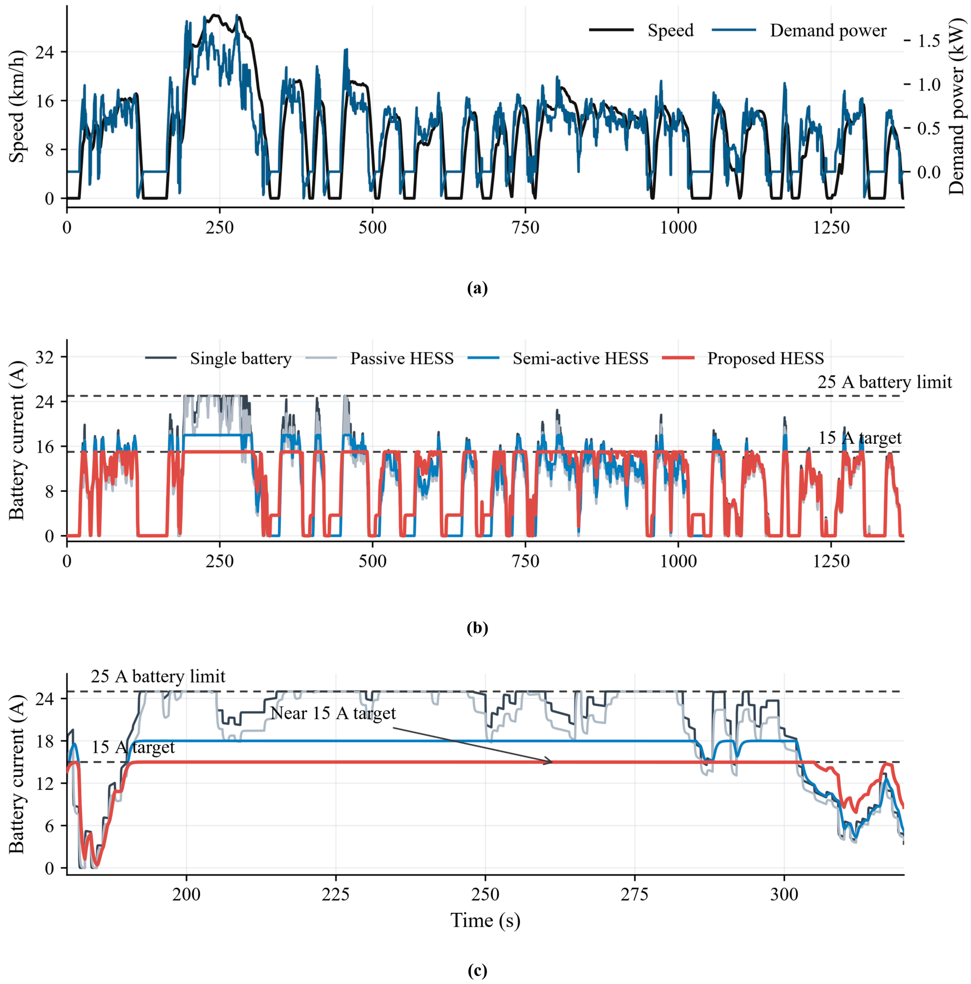

Figure 11. UDDS-based battery current stress mitigation of the proposed reduced-switch HESS: (**a**) ATV-scaled UDDS speed and demand power; (**b**) battery-current comparison among different configurations; and (**c**) enlarged high-demand interval.

The UDDS-based profile in Figure 11a shows the ATV-scaled speed and traction demand power. Figure 11b compares the battery current of the single-battery system, passive HESS, semi-active HESS, and proposed HESS. During the high-demand interval, the single-battery and passive HESS cases approach 25 A, whereas the proposed HESS limits the battery current to approximately 15 A by assigning transient power to the supercapacitor branch. This figure provides the primary UDDS-based evidence that the proposed control strategy reduces battery-current-stress indicators under stop-and-go operation.

3.3. Complex ATV Cycle and Supercapacitor Buffering

In addition to the scaled UDDS-derived cycle, an ATV-oriented complex cycle is constructed to represent operating conditions that are more specific to electric ATV applications. The cycle includes start-up, regenerative braking, uphill driving, and high-load transient segments. The speed, grade, and demand-power profiles of the ATV-oriented complex cycle are shown in Figure 12.

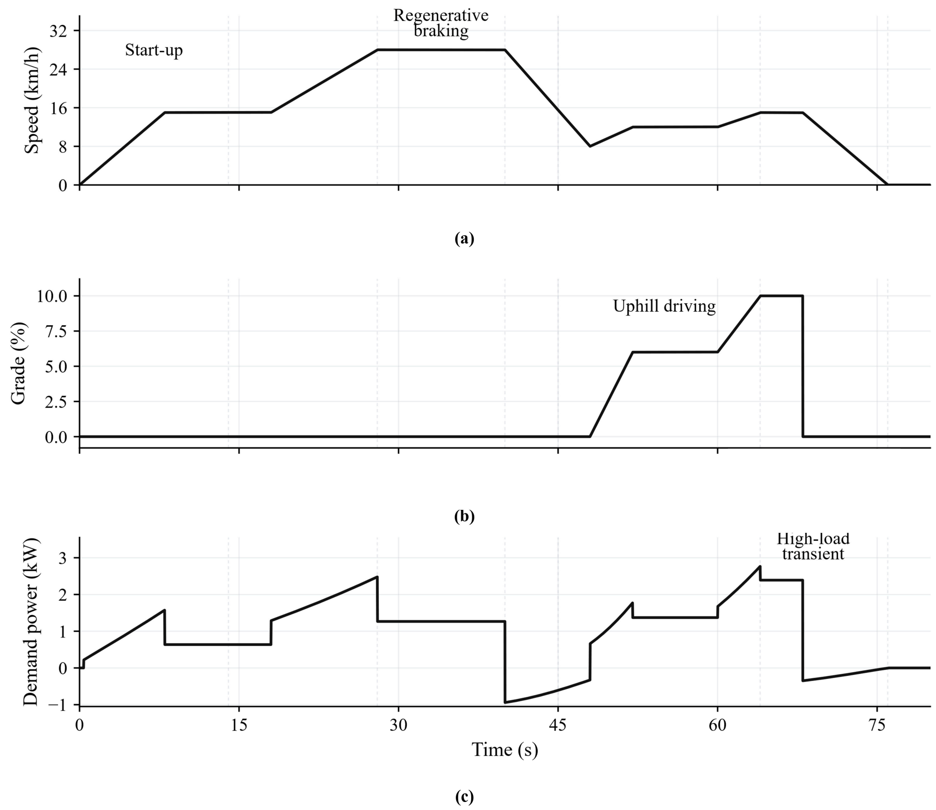

Figure 12. ATV-oriented complex-cycle profile for vehicle-level validation: (**a**) speed profile; (**b**) grade profile; and (**c**) demand-power profile.

The profile in Figure 12 defines the ATV-oriented complex cycle used for vehicle-level battery-current-stress and power-buffering evaluation. The profile includes start-up, braking, grade-driving, and high-load transient segments, so it provides a more application-specific duty cycle than the scaled UDDS trace alone.

Based on this ATV-oriented complex cycle, the power-sharing behavior and mode-constrained operation of the proposed HESS are shown in Figure 13.

The detailed power-sharing result in Figure 13 focuses on the proposed HESS. The supercapacitor branch absorbs fast positive transients and braking-related negative power, while the battery branch follows a smoother baseline reference. This behavior explains the battery-current-stress reduction reported in the following comparative indicators.

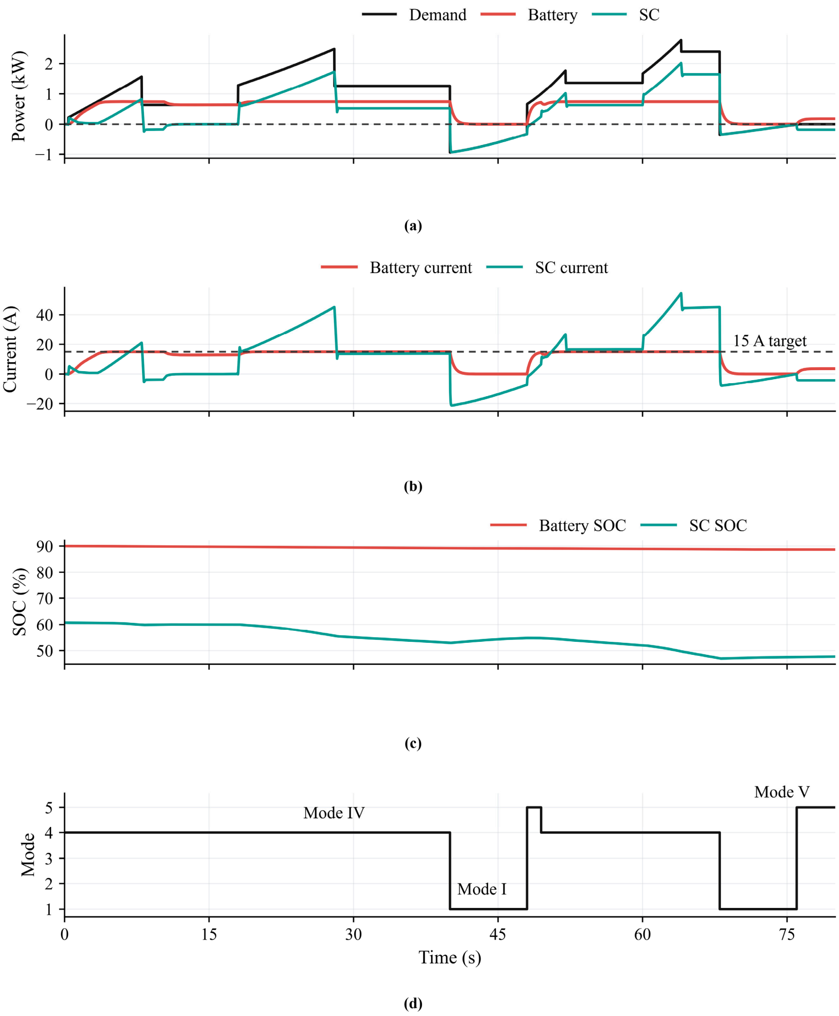

Figure 13. Supercapacitor buffering and mode-constrained power sharing under the ATV-oriented complex cycle: (**a**) power sharing among demand power, battery power, and SC power; (**b**) battery and SC currents; (**c**) battery and SC SOCs; and (**d**) selected operating mode. The dashed horizontal reference lines indicate the zero-power/current reference or the 15 A battery-current target in the corresponding subfigures.

3.4. Comparative Battery-Current-Stress Indicators

To further evaluate battery-current-stress mitigation, four configurations are compared under the same ATV-oriented complex cycle: a single-battery system, a passive HESS, a semi-active HESS, and the proposed reduced-switch HESS. All cases are implemented in the same vehicle-level average-model framework and use the same vehicle coefficients, battery pack, demand-power profile, DC-bus reference, simulation step size, and evaluation indicators. The passive, semi-active, and proposed HESS cases also use the same SC pack parameters. The single-battery case serves as the no-SC baseline. The passive HESS represents an uncontrolled buffering case, in which battery/SC power sharing is determined by branch dynamics and equivalent impedance characteristics. The semi-active HESS serves as an active-control benchmark with an actively regulated SC branch. Its controller is tuned within the same current, voltage, and SOC limits by increasing the SC transient-power contribution until the RMS battery current is reduced without violating the 48 V DC-bus regulation target or the component current/SOC constraints. The proposed HESS represents the low-switch-count mode-constrained solution. Therefore, the comparison focuses on how the energy-storage structure and power-sharing principle affect battery-current-stress indicators, DC-bus regulation, and regenerative-energy behavior under common average-model assumptions.

The comparative battery-current-stress, DC-bus, and regenerative-energy indicators of the four configurations are summarized in Figure 14.

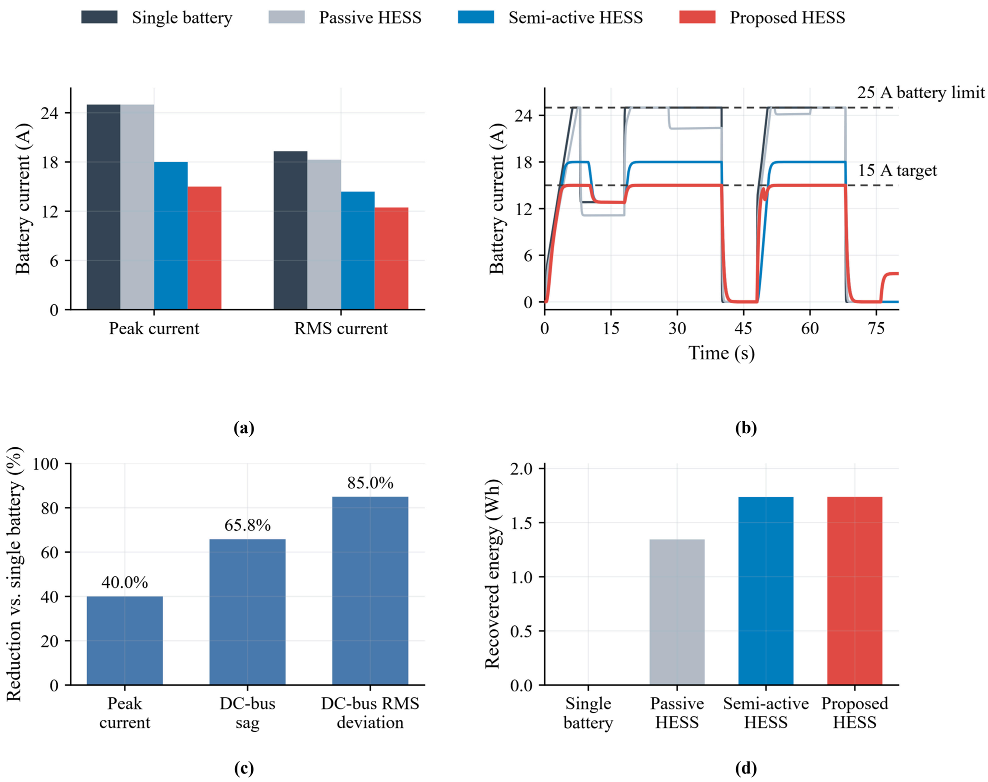

Figure 14. Comparative battery-current-stress, DC-bus, and regenerative-energy indicators under the ATV-oriented complex cycle: (**a**) peak and RMS battery-current indicators; (**b**) battery-current waveform comparison; (**c**) reduction ratios relative to the single-battery baseline; and (**d**) recovered regenerative braking energy.

The comparative dashboard in Figure 14 summarizes the battery-current, DC-bus voltage, and regenerative-energy indicators under the ATV-oriented complex cycle. The proposed HESS reduces the battery current stress compared with the single-battery and passive HESS configurations by transferring fast transient demand to the supercapacitor branch. It also maintains the DC-bus voltage close to the 48 V reference and achieves recovered braking energy comparable to the semi-active HESS benchmark.

The quantitative indicators in Table 4 are calculated over the ATV-oriented complex cycle according to the definitions in Section 2.7. Table 4 retains the core comparison of peak current, RMS current, DC-bus voltage sag, RMS DC-bus voltage deviation, and recovered braking energy.

Table 4. Quantitative comparison under the ATV-oriented complex cycle.

Configuration	$I_{b,pk}$ (A)	$I_{b,rms}$ (A)	$\Delta V_{dc,max}$ (V)	$V_{dc,err,rms}$ (V)	E_{rec} (Wh)
Single battery	25.00	19.31	1.528	0.480	0.000
Passive HESS	25.00	18.28	1.175	0.309	1.345
Semi-active HESS	18.00	14.39	0.643	0.078	1.738
Proposed HESS	15.00	12.45	0.523	0.072	1.738

Note: $I_{b,pk}$, $I_{b,rms}$, $\Delta V_{dc,max}$, $V_{dc,err,rms}$, and E_{rec} denote the peak battery current, RMS battery current, maximum DC-bus voltage sag, RMS deviation of the DC-bus voltage, and recovered regenerative braking energy, respectively.

The quantitative results in Table 4 further support the waveform observations in Figure 14. Compared with the single-battery baseline, the proposed HESS reduces the peak battery current from 25.00 A to 15.00 A and the RMS battery current from 19.31 A to 12.45 A. Table 5 extends this comparison with additional battery-current-stress indicators, including charge throughput and estimated battery resistive-loss energy.

Table 5. Battery-current-stress indicators under the ATV-oriented complex cycle.

Configuration	$I_{b,pk}$ (A)	$I_{b,rms}$ (A)	$Q_{through}$ (Ah)	$E_{loss,b}$ (Wh)	Reduction in $E_{loss,b}$ (%)
Single battery	25.00	19.31	0.359	0.497	0.00
Passive HESS	25.00	18.28	0.338	0.446	10.38
Semi-active HESS	18.00	14.39	0.272	0.276	44.47
Proposed HESS	15.00	12.45	0.242	0.207	58.41

Note: $Q_{through}$ is the absolute battery charge throughput over the cycle. $E_{loss,b}$ is the estimated battery resistive-loss energy using the internal resistance listed in Table 3. The reduction percentage is calculated relative to the single-battery baseline.

Because $E_{loss,b}$ is proportional to $I_b^2 R_b$, it is more sensitive to high-current peaks than the charge-throughput indicator. Compared with the single-battery baseline, the proposed HESS reduces $Q_{through}$ from 0.359 Ah to 0.242 Ah and decreases the estimated resistive-loss indicator from 0.497 Wh to 0.207 Wh, corresponding to a 58.41% reduction. This result supports the conclusion that the proposed HESS reduces the high-current exposure of the battery under the evaluated ATV-oriented complex cycle.

A supplementary cross-cycle robustness summary is provided in Figure S1, where peak battery current, RMS battery current, DC-bus voltage sag, and recovered regenerative energy are compared under three representative operating cycles. In addition, a model-based parameter-sensitivity analysis is provided in Table S1, showing that the reported battery-current-stress and DC-bus indicators remain broadly stable under moderate battery-resistance and traction-demand perturbations in the adopted average-model simulation.

3.5. Supercapacitor Initial-SOC Sensitivity

The influence of supercapacitor initial SOC is evaluated to test whether the proposed current-stress mitigation remains effective when the available supercapacitor energy headroom changes. Three initial SOC values are considered—0.60, 0.75, and 0.90—representing low, nominal, and high initial-energy states within the normal usable SC operating window of the adopted model. More extreme initial SOC values are not used as the main sensitivity cases because very low SC SOC would trigger discharge restriction or restoration-dominant operation, whereas very high SC SOC would reduce regenerative-braking headroom and may lead to braking-energy curtailment.

The corresponding battery-current, SC SOC, DC-bus voltage, and cumulative recovered-energy responses are shown in Figure 15.

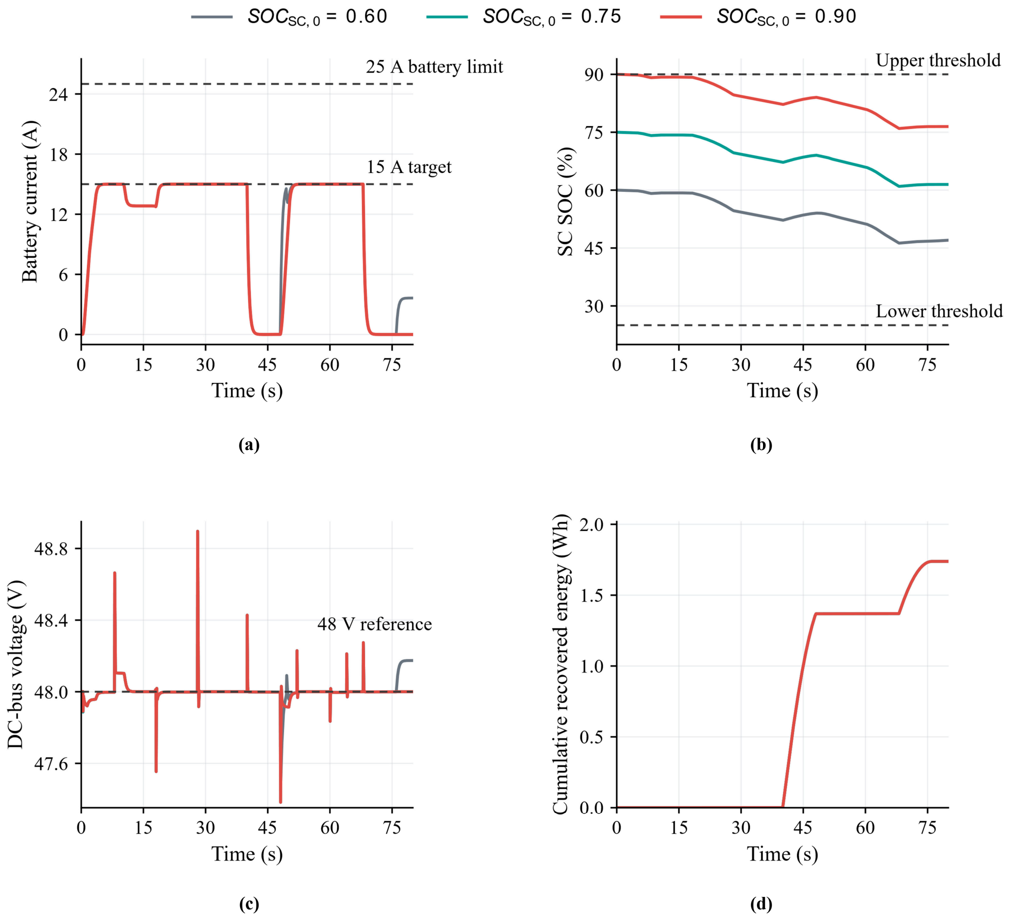

Figure 15. Sensitivity of battery-current-stress and DC-bus indicators to the initial supercapacitor SOC: (**a**) battery current; (**b**) SC SOC; (**c**) DC-bus voltage; and (**d**) cumulative recovered energy.

The sensitivity results in Figure 15 show that the proposed control strategy maintains the 15 A battery-current limit for all tested initial SC SOC values. The main influence of the initial SC SOC appears in the SC SOC trajectory, whereas the battery-current-stress indicators vary only slightly within the simulated initial-SOC range of 0.60–0.90. Therefore, the result is interpreted as limited sensitivity within the evaluated SOC range rather than as a general claim for all SC headroom conditions. The quantitative sensitivity indicators for the three initial SC SOC cases are summarized in Table 6.

Table 6. Sensitivity indicators for different initial supercapacitor SOC values.

Initial SC SOC	$I_{b,pk}$ (A)	$I_{b,rms}$ (A)	$Q_{through}$ (Ah)	$E_{loss,b}$ (Wh)	$\Delta V_{dc,sag,max}$ (V)	E_{rec} (Wh)	SC SOC Variation (%)
0.60	15.00	12.45	0.242	0.207	0.523	1.738	13.738
0.75	15.00	12.31	0.234	0.202	0.618	1.738	14.037
0.90	15.00	12.31	0.234	0.202	0.618	1.738	14.037

Note: The table reports the same current-stress and bus-regulation indicators as Section 2.7. The DC-bus item denotes the maximum voltage sag relative to the 48 V reference, rather than the maximum absolute voltage deviation. The SC SOC variation denotes the difference between the maximum and minimum SC SOC values during the evaluated cycle. These results indicate control robustness within the simulated initial-SOC range and should not be interpreted as direct electrochemical aging performance. The nearly identical battery-side indicators for the initial SC SOC values of 0.75 and 0.90 are caused by the same effective mode sequence and current-limited allocation path. Once sufficient SC voltage and energy headroom are available, the battery current is mainly governed by the 15 A current target and the mode-constrained allocation law rather than by the exact initial SC SOC.

3.6. Mode-Coverage and SOC-Boundary Verification

Because a normal driving cycle may not activate all operating modes, a dedicated mode-coverage test is conducted to verify the logical completeness of the proposed mode-selection strategy. It should be noted that this test is not intended to represent a continuous driving cycle; instead, representative SOC-boundary and power-demand conditions are deliberately imposed to examine whether Modes I–V can be correctly selected. The resulting demand-power profile, SOC boundary conditions, and selected operating modes are shown in Figure 16.

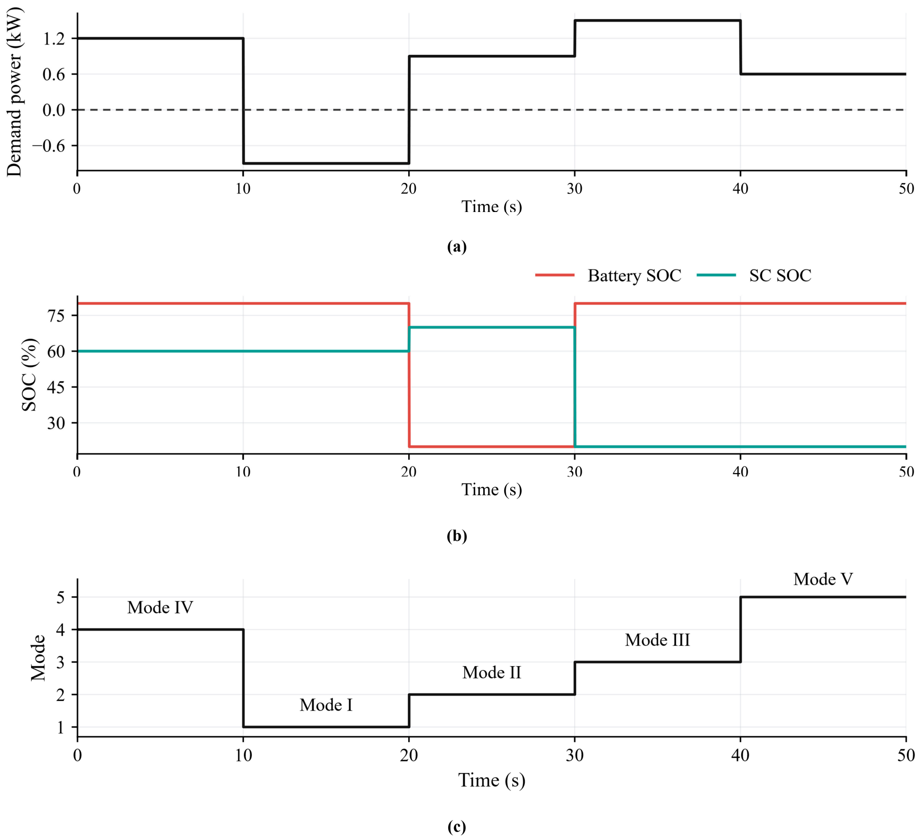

Figure 16. Mode-coverage and SOC-boundary verification of the proposed reduced-switch HESS: (**a**) demand-power profile; (**b**) SOC boundary conditions; and (**c**) selected operating mode.

As shown in Figure 16, the dedicated SOC-boundary test successfully triggers all five operating modes of the proposed HESS. Mode I is activated during the negative demand-power interval, indicating regenerative braking with supercapacitor charging. Mode II is triggered when the battery SOC is low and the supercapacitor has sufficient available energy. Mode III occurs when the supercapacitor SOC is low and the battery remains available. Mode IV represents normal combined output, and Mode V is activated when the battery supplies the load while restoring the supercapacitor energy reserve.

These results confirm that the proposed mode-selection logic covers the prescribed SOC-boundary and power-demand cases in the simulation test. Therefore, Figure 16 is interpreted as a mode-logic coverage check for traction, regenerative braking, and supercapacitor energy restoration, rather than as a continuous real-driving-cycle validation of all modes.

4. Discussion

4.1. Battery Current Stress Mitigation

The main result is the reduction of battery-current stress under ATV-oriented transient-load operation. Under the ATV-oriented complex cycle, the proposed HESS reduces the peak battery current from 25.00 A to 15.00 A and the RMS battery current from 19.31 A to 12.45 A. These quantities are electrical stress metrics; they support the conclusion that the battery current burden is reduced in the evaluated cycles, but they do not by themselves establish capacity-fade, internal-resistance, or cycle-life improvement.

This improvement is mainly produced by the combined effect of transient-power separation, current limiting, and feasible-path projection. The Db4-based allocation assigns the smoother positive demand component to the battery and transfers fast positive transients to the SC branch, thereby reducing high-frequency battery-current excursions and the associated resistive-loss metric. During braking intervals, the negative power component is preferentially absorbed by the SC when sufficient voltage and SOC headroom are available. Because the preliminary power references are projected onto the admissible operating mode and component limits before switch-level implementation, infeasible power commands are avoided, which also helps reduce DC-bus voltage sag under the evaluated transient-load conditions.

The supplementary parameter-sensitivity results in Table S1 further support the consistency of the reported current-stress and DC-bus performance under moderate parameter perturbations in the adopted average-model simulation. The proposed HESS maintains the selected 15 A battery-current constraint, while RMS battery current, charge throughput, DC-bus voltage sag, and recovered braking energy show only small variations. These results indicate that the main current-stress mitigation trend remains stable within the tested uncertainty range.

4.2. Supercapacitor Buffering and SOC Headroom

The supercapacitor branch acts as a transient buffer rather than as the primary energy source. This role is visible in the complex-cycle power-sharing results and in the initial-SOC sensitivity test. For initial SC SOC values of 0.60, 0.75, and 0.90, the proposed HESS maintains the 15 A battery-current target in the simulated cycle, but this conclusion is limited to the tested SOC range. Operation very near the upper SC voltage or SOC threshold would require explicit handling of reduced regenerative headroom and unrecovered braking power. The recovered regenerative energy of 1.738 Wh in the ATV-oriented complex cycle is much smaller than the theoretical maximum SC pack energy of approximately 97.2 Wh because the former corresponds only to the braking intervals within one evaluated driving window, whereas the latter represents the full theoretical energy storage capability of the SC pack. In this cycle, the recoverable energy is limited by braking duration, braking-side power level, instantaneous SC voltage/SOC headroom, and the admissible charging path of the selected operating mode. Therefore, the SC is not intended to be fully charged or deeply cycled in a single cycle; its primary role is to provide transient-power buffering and regenerative-energy headroom.

4.3. Implementation Complexity and Validation Boundary

The reduced-switch structure lowers the number of actively controlled power devices and simplifies mode coordination compared with more flexible HESS topologies. This advantage must be interpreted together with the associated trade-offs: fewer controlled paths can limit regenerative voltage headroom, constrain current sharing, and shift part of the performance burden to mode selection and constraint projection. The present comparison focuses on battery-side current-stress indicators and DC-bus regulation; it does not establish a total system-efficiency or thermal-performance advantage over semi-active alternatives.

From a practical implementation perspective, the reduced-switch architecture is attractive for low-power ATV applications because it reduces the number of actively driven power devices and gate-drive channels. This can simplify packaging and controller implementation compared with more flexible fully active HESS structures. However, commercial deployment would still require full-power prototype verification, thermal design, protection coordination, mechanical packaging, safety certification, and vehicle-level road testing before the proposed architecture could be treated as a production-ready EV energy-storage solution.

4.4. Limitations and Future Work

The present study focuses on the electrical current-stress mitigation, DC-bus regulation, and regenerative-energy behavior of the proposed reduced-switch HESS. Converter-level prototype tests are used to verify the voltage-regulation capability of the hardware implementation, while vehicle-level average-model evaluations are used to quantify battery-current-stress metrics under representative ATV-oriented duty cycles. The converter-level hardware waveforms reported in this study are representative measurements of the prototype voltage-regulation behavior under the tested start-up and load-disturbance conditions. Formal repeatability statistics will be included in subsequent full-power prototype validation. The supplementary sensitivity analysis further supports the consistency of the main electrical metrics under moderate model-parameter perturbations. Building on this basis, future work will extend the evaluation to repeated full-power prototype tests, hardware-in-the-loop implementation, thermal characterization, and aging-aware experiments, so that the current-stress metrics reported here can be further connected with long-term battery degradation behavior.

5. Conclusions

This paper presented a reduced-switch battery/supercapacitor HESS for battery-current-stress mitigation in low-power electric ATVs. The proposed architecture combines five operating modes, mode-constrained Db4-based power allocation, and DC-bus voltage control to assign fast transient and regenerative-braking power components to the supercapacitor while keeping the battery current within the selected constraint in the evaluated cycles.

Under the ATV-scaled UDDS-derived cycle, the proposed HESS limits battery current to approximately 15 A during the high-demand interval. Under the ATV-oriented complex cycle, peak battery current decreases from 25.00 A to 15.00 A and RMS battery current decreases from 19.31 A to 12.45 A. The maximum DC-bus voltage sag decreases from 1.528 V to 0.523 V, while recovered braking energy remains 1.738 Wh.

The additional current-stress indicators show that the proposed HESS reduces battery charge throughput and estimated resistive-loss energy relative to the single-battery baseline. The initial supercapacitor SOC sensitivity test further shows that the proposed allocation strategy maintains the 15 A battery-current constraint for initial SC SOC values of 0.60, 0.75, and 0.90. The nearly identical battery-side indicators observed at $SOC_{sc,0}$ = 0.75 and 0.90 are consistent with the same effective current-limited control path under sufficient SC voltage and energy headroom.

The results demonstrate reduced battery-current-stress indicators and stable DC-bus regulation for the considered ATV-oriented duty cycles, supported by converter-level hardware voltage-regulation tests and supplementary model-based sensitivity checks. By combining a reduced-switch topology, mode-constrained allocation, and prototype-level voltage-regulation verification, this study provides a practical foundation for subsequent full-power prototype evaluation, thermal characterization, vehicle-level implementation, and aging-aware durability assessment.

Supplementary Materials: The following supporting information can be downloaded at: https://www.mdpi.com/article/10.3390/batteries12070248/s1. Figure S1: presents the cross-cycle robustness summary of peak battery current, RMS battery current, DC-bus voltage sag, and recovered regenerative energy under the ATV-scaled UDDS, ATV-oriented complex, and long urban-like cycles. Table S1: presents the supplementary model-based parameter-sensitivity results of the proposed HESS under moderate battery-resistance and traction-demand perturbations.

Author Contributions: Conceptualization, J.W.; methodology, J.W. and S.Z.; software, S.Z. and L.L.; validation, S.Z., M.L. and L.L.; formal analysis, M.L.; investigation, Z.Y. and M.L.; data curation, Z.Y.; visualization, Z.Y. and L.L.; writing—original draft preparation, S.Z.; writing—review and editing, J.W.; supervision, J.W.; funding acquisition, J.W. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The simulation profiles, model parameters, and processed experimental data are available from the corresponding author upon reasonable request.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript: ATV, all-terrain vehicle; Db4, Daubechies-4; DC, direct current; EMS, energy management system; HESS, hybrid energy storage system; MCU, microcontroller unit; PWM, pulse-width modulation; RMS, root mean square; SC, supercapacitor; SOC, state of charge; SMC, sliding-mode control; TSMC, terminal sliding-mode control; UDDS, Urban Dynamometer Driving Schedule.

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