

Article

Rectifying and Photoconductive Responses in Graphene–Double-Insulator–Graphene (GI²G) Structures

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Abstract

Advanced solar energy-harvesting devices, such as optical rectennas, typically use metal–insulator–metal diodes because of the ultrafast response of these diodes at high frequencies. However, the diode performance is limited by weak current–voltage (*I*–*V*) asymmetry and optical losses in metallic electrodes. Graphene offers a promising alternative electrode material owing to its high carrier mobility, broadband optical transparency, and compatibility with nanoscale device architectures. Nevertheless, graphene-based optical rectennas face challenges associated with insufficient diode nonlinearity. In this study, we developed a vertically stacked graphene–double-insulator–graphene (GI²G) tunnel diode. Devices with various junction sizes were fabricated to investigate size-dependent rectifying behavior. A reduced graphene overlap area was defined by electron-beam lithography to introduce asymmetry and increase nonlinear conduction. An Al₂O₃/SiO₂ tunnel barrier composed of dielectrics with different band gaps and electron affinities improved the asymmetric *I*–*V* characteristics. Photoresponse measurements under AM1.5G illumination revealed a clear photocurrent, indicating rectification-related photoresponse. The photoresponse increased with decreasing junction area, which is consistent with enhanced rectification performance in smaller junctions. These results demonstrate that the GI²G tunnel diode provides a promising platform for next-generation energy harvesting and optical sensing applications.

Keywords: graphene; optical rectenna; photoresponse; MIM diode; rectification; energy harvesting



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1. Introduction

The growing demand for advanced solar energy-harvesting technologies has driven efforts to increase the efficiency of energy-conversion systems, which requires new device architectures that enable high energy-conversion efficiency and support technological advances. Thus, new material and devices based on new operating principles are required [1].

Graphene and other low-dimensional materials contribute to advances in solar energy-harvesting because of their remarkable properties, including strong light–matter interactions [2–7], strong nonlinear optical responses [8,9], high carrier mobility [10,11], pressure-induced ferroelectricity [12], and tunable band structures through external fields or chemical treatments [13–15]. Graphene is an attractive low-dimensional material owing to its excellent electrical and optical properties. Consequently, graphene can be used to fabricate high-speed optoelectronic devices [16–24]. However, it remains challenging to

exploit graphene's outstanding properties effectively in practical device architectures. Technological advancements are required in wafer-scale fabrication processes, including the formation of low-resistance ohmic contacts [25], doping techniques for carrier modulation and pn-junction formation [26], the control of interfacial interactions with supporting substrates [11], and the development of low-damage processes [27].

The optical rectenna consists of a nanoantenna and a rectifying diode. The nanoantenna captures visible light, and the diode rectifies the high-frequency electromagnetic component to generate direct current. Research on rectennas originated from a patent filed by Brown in 1969 [28], and a power conversion efficiency of over 90% was later achieved at a microwave frequency of 2.45 GHz [29]. In 1972, Bailey proposed extending power-absorbing antennas, which convert solar energy into direct current, to the visible-light region [30]. Subsequently, Corkish et al. examined the theoretical performance limits of optical rectennas and reported that a conversion efficiency of approximately 85% is theoretically attainable [31]. However, as the operating frequency increases, major challenges arise in optimizing antenna design, reducing device dimensions, minimizing Joule losses in metallic nanostructures, improving diode response speed, and achieving sufficient nonlinear conduction. Consequently, in the terahertz (THz) and higher frequency regions, the practically achievable conversion efficiency decreases to below 1% [32,33].

Improving the diode performance is particularly crucial in developing rectennas for high-frequency operation. Schottky diodes based on GaAs and Si have been studied extensively in the microwave and millimeter-wave regions [34–36]. In contrast, metal–insulator–metal (MIM) structures with ultrafast response have been used in the THz and infrared regions [37–42], because the Schottky diodes used in rectennas exhibit large power loss above 5 THz due to parasitic capacitance. Therefore, MIM tunnel diodes, which enable low-power operation and ultrafast response above 100 THz, have attracted attention as promising devices for optical rectification. Metal–double-insulator–metal tunnel diodes have also been explored to achieve asymmetric I – V characteristics [43]. In the visible region, alternative device architectures, including carbon nanotube electrodes and graphene geometric diodes, have been reported [44–47]. Nonetheless, it remains difficult to produce rectifying diodes that operate stably at frequencies above the THz range because of the intrinsic trade-off between current density and ultrafast rectification. Although MIM diodes exhibit excellent high-frequency response, their symmetric barrier structure and thin insulating layers cause leakage currents, resulting in low direct-current output and a small rectification ratio.

In this work, we developed a vertically stacked graphene–double-insulator–graphene (GI^2G) tunnel diode. The insulator layers consisted of Al_2O_3 and SiO_2 layers with different band gaps and electron affinities, sandwiched between the top and bottom graphene layers. The $\text{Al}_2\text{O}_3/\text{SiO}_2$ bilayer served as a tunnel barrier, minimizing leakage current across the junction. Furthermore, the graphene electrodes were not heavily perturbed by the dielectric stacks, and their high carrier mobility was preserved. A small junction area between the graphene layers relative to the graphene electrodes was defined by electron-beam lithography, resulting in asymmetric I – V characteristics due to geometric effects [48]. DC measurements under AM1.5G illumination using a solar simulator were carried out to evaluate the photoresponse of the devices.

2. Materials and Methods

2.1. Device Fabrication

Figure 1 shows the schematics of the top and cross-sectional views of the GI^2G tunnel diode. The cross-sectional schematic shows stacked tunnel dielectrics between graphene electrodes. Because the tunneling current depends exponentially on the insulator thickness,

the tunnel barrier was formed using atomic layer deposition (ALD), which enables nanometer-scale thickness control. Samples with two different tunnel dielectric structures were prepared to investigate the transport mechanism in the diodes (Table 1). A stacked barrier composed of $\text{Al}_2\text{O}_3/\text{SiO}_2$ was used to achieve asymmetric I – V characteristics. In the GI^2G structure, the stacked dielectric barrier introduces step tunneling under positive bias due to differences in the electron affinities and band gaps of the two dielectrics (Figure S1). This band alignment results in a polarity-dependent tunnel barrier, where the effective barrier height and tunneling width depend on the polarity of the applied bias. As a result, step tunneling enhances I – V asymmetry even when symmetric graphene electrodes are used.

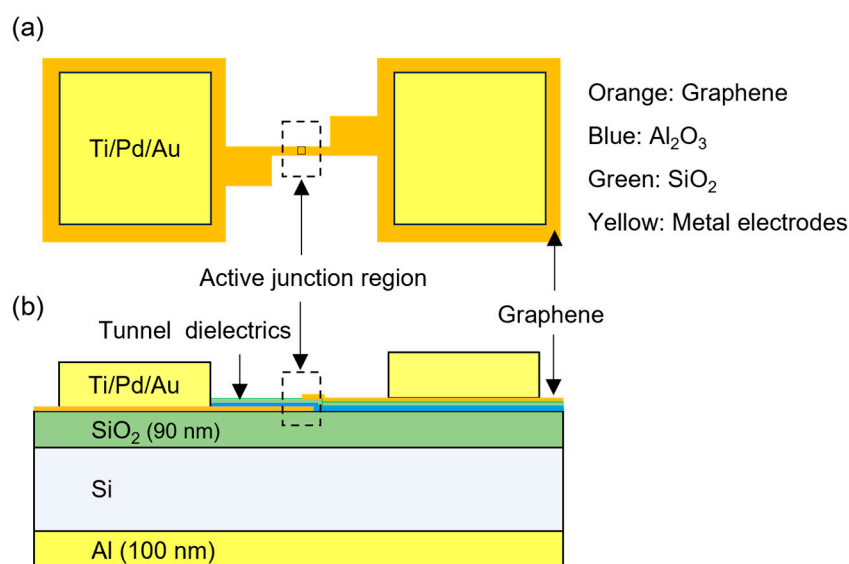


Figure 1. Schematic illustration of the GI^2G device. (a) Top view of the device (not to scale). (b) Corresponding cross-sectional structure (not to scale). The dashed region indicates the active junction area, where the graphene electrodes are separated by tunnel dielectric layers.

Table 1. Structural parameters of the fabricated samples.

Sample	Device Structure	Dielectrics I_1/I_2
Sample 1	p-Si/ I_1 / I_2 /Al	Al_2O_3 (3 nm)/ SiO_2 (3 nm)
Sample 2	p-Si/ I_1 / I_2 /Al	Al_2O_3 (3 nm)/ SiO_2 (6 nm)
Sample 3	Graphene/ I_1 / I_2 /Graphene	Al_2O_3 (2 + 3 nm)/ SiO_2 (3 nm)
Sample 4	Graphene/ I_1 / I_2 /Graphene	Al_2O_3 (2 + 3 nm)/ SiO_2 (6 nm)

To evaluate the effect of the tunnel region configuration on the I – V characteristics, multiple devices with different tunnel region designs were fabricated using the following process. Monolayer graphene grown by chemical vapor deposition on a Cu foil (Graphenea, San Sebastian, Spain) was transferred onto a Si/ SiO_2 substrate using a method similar to that reported by Shiga et al. [17]. A polymethyl methacrylate (PMMA) support layer was formed on the top surface of the Cu foil. To remove graphene grown on the back of the Cu foil, a 10% polyvinyl alcohol (PVA) solution was spin-coated on the back surface. The PVA layer, together with the unwanted graphene, was first removed using an iron nitrate solution, after which the Cu foil was etched in the same solution. The remaining graphene/PMMA stack was scooped up with a Si/ SiO_2 substrate and rinsed twice in pure water. The substrate was left overnight and subsequently annealed in air at 80 °C for 8 h using a drying oven to remove residual water trapped between the graphene and the substrate. Finally, the PMMA layer was removed by immersion in hot acetone. To improve the adhesion at the SiO_2 /graphene interface, the sample was annealed at 350 °C for 5 h in

Ar (500 sccm). A hydrogen silsesquioxane (HSQ) resist was spin-coated, and a fine pattern was defined by electron-beam lithography (JBX-9300SA, JEOL, Tokyo, Japan), followed by patterning of the first graphene layer using O₂ reactive ion etching (RIE-10NR, Samco, Kyoto, Japan) at 100 W for 30 s. After patterning, openings in the HSQ layer were defined by photolithography, and the exposed HSQ was removed using buffered oxide etchant (BOE). Ti/Pd/Au (0.5/20/70 nm) layers were deposited by electron-beam evaporation (TU-8, Asahi Shokai Sendai, Sendai, Japan) and lift-off to form electrodes on the graphene. The entire substrate was coated with a 1.5 nm-thick Al layer by electron-beam evaporation and naturally oxidized to form a thin Al₂O₃ passivation layer. Based on the Pilling–Bedworth relationship [49] and assuming a γ -Al₂O₃ density of 3.70 g/cm³, the 1.5 nm-thick Al layer formed an Al₂O₃ layer with an estimated thickness of 2.0 nm [50]. The naturally oxidized Al₂O₃ layer was used to passivate the graphene surface and to provide a uniform nucleation layer for subsequent ALD. Additional tunnel dielectrics consisting of 3 nm-thick Al₂O₃ and 3- or 6 nm-thick SiO₂ layers were then deposited by ALD (AD-230LP, Samco, Kyoto, Japan). The Al₂O₃ layer was grown by thermal ALD at 200 °C using trimethylaluminum (TMA) and H₂O as the precursor and oxidant, respectively. The SiO₂ layer was deposited by plasma-assisted ALD at 200 °C using bis(diethylamino)silane (BDEAS) as the precursor and O₂ plasma as the oxidant. ALD enables precise control of dielectric thickness and is widely used in Si processing, providing stable and reproducible interfaces with Si and metal electrodes. A second graphene layer was then transferred onto the tunnel dielectrics. To increase adhesion between graphene and ALD-SiO₂, the sample was again annealed at 350 °C for 4 h in Ar (500 sccm). The second graphene layer was coated with HSQ, and a fine pattern was defined by electron-beam lithography followed by O₂ reactive-ion etching at 100 W for 30 s. Contact openings were defined by photolithography, and the exposed HSQ within the openings was removed by using BOE. Ti/Pd/Au (0.5/20/70 nm) layers were deposited on the top graphene layer by a separate electron-beam evaporation (ADS-E810, R-DEC, Tsukuba, Japan), and electrodes were formed by lift-off. Because the tunnel dielectrics covered the bottom electrode, additional photolithography and etching steps were required to form contact windows to the bottom graphene layer. Finally, 100 nm-thick Al was deposited on the backside of the Si substrate to form the electrode. We also fabricated metal–double-insulator–Si (MI²S) tunnel diodes with a device area of 5.2 mm² using the same Al₂O₃/SiO₂ tunnel barrier to evaluate the asymmetry of the *I*–*V* characteristics. Al electrodes with a thickness of 100 nm were formed on the dielectric layers and on the backside of the Si substrate.

2.2. Electrical and Optical Measurements

The *I*–*V* characteristics of the fabricated devices were measured using a manual probe station (MPS150, Cascade Microtech, Beaverton, OR, USA) combined with a semiconductor parameter analyzer (4155C, Keysight Technologies, Santa Rosa, CA, USA). The capacitance–voltage (*C*–*V*) characteristics of the MI²S diodes were measured using a precision LCR meter (4284A, Keysight Technologies) at 1 MHz, with the voltage sweep covering the accumulation and inversion regions. Photocurrent measurements were performed using a standard solar simulator (HAL-320, Asahi Spectra Inc., Tokyo, Japan) providing AM 1.5G illumination, which was positioned to expose the devices uniformly during measurements. The illumination intensity was calibrated to 1-sun conditions over the wavelength range of 350–1100 nm. We evaluated more than 100 devices per sample, and each device was measured multiple times to confirm reproducibility. A field-emission scanning electron microscope (SU8000, Hitachi, Tokyo, Japan) was used to analyze the device structure. Raman measurements were performed using a Raman microscope (InVia, Renishaw, Wotton-under-

Edge, UK), and the spectra were recorded with a 50 $\times$ objective at an excitation wavelength of 532 nm and a laser power of 0.5 mW.

3. Results and Discussion

We initially performed Raman measurements on graphene transferred onto thermally oxidized SiO₂ substrates. The Raman spectra showed that the transferred graphene was a monolayer with a low defect density (Figure S2). Figure 2 shows field emission scanning electron microscope images of representative GI²G devices. The active junction region, defined by the graphene overlap area, is highlighted by dashed squares. The device shown in Figure 2a has a small antenna with an overlap area of 125 $\times$ 50 nm, whereas the device in Figure 2b features a large antenna with an overlap area of 6 $\times$ 0.2 μ m. Electron-beam lithography enabled precise pattern alignment and the fabrication of features with a minimum dimension of around 50 nm, allowing systematic evaluation of junction geometry and antenna size effects.

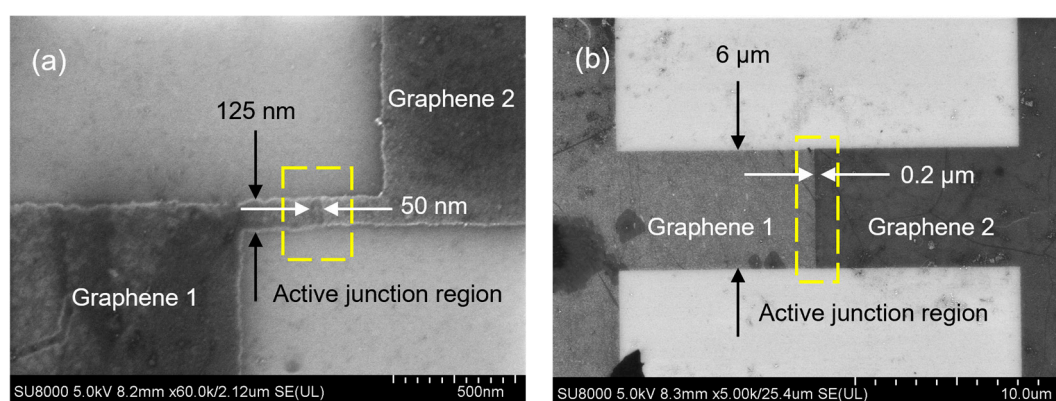


Figure 2. SEM images of GI²G devices. The active junction region is highlighted by dashed squares. (a) Device with a small antenna and an overlap area of 125 $\times$ 50 nm. (b) Device with a large antenna and an overlap area of 6 $\times$ 0.2 μ m.

Figure 3 shows representative *I*–*V* characteristics of the MI²S diodes for the two structures summarized in Table 1. Asymmetric *I*–*V* characteristics were observed because of the asymmetric tunnel barrier profile of the Al₂O₃/SiO₂ stack, resulting in reduced tunneling current in the reverse-bias region. Sample 1 exhibited a higher current than Sample 2 because of the thinner stacked dielectric layers.

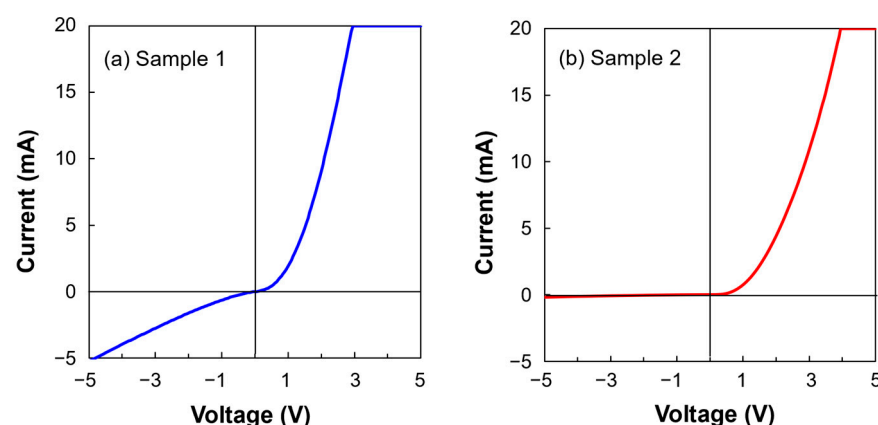


Figure 3. Comparison of the *I*–*V* characteristics of Samples (a) 1 and (b) 2 with an area of 5.2 mm², demonstrating different nonlinear behavior related to the dielectric structures.

Figure 4 shows representative C - V characteristics of the MI²S diodes for the two device structures. The devices exhibited typical p-type substrate behavior, showing an accumulation region under reverse bias and a decrease in capacitance under forward bias. Compared with Sample 1, Sample 2 exhibited lower capacitance because of the thicker SiO₂ layer. The relative dielectric constant of the ALD-Al₂O₃ layer was extracted from the accumulation capacitance at 1 MHz and found to be 9.0, consistent with previously reported values [51].

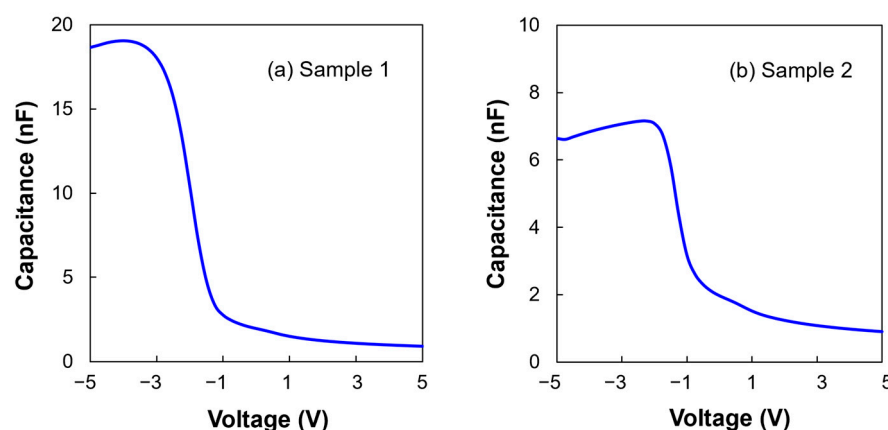


Figure 4. C - V characteristics of the MI²S diodes with an area of 5.2 mm² for Samples (a) 1 and (b) 2.

Figure 5 shows I - V characteristics and the junction area dependence of the asymmetry. The overall device yield was approximately 52%. The junction areas were defined by electron-beam lithography, which provides high alignment accuracy and ensures good uniformity of the designed junction dimensions. The device-to-device variation is shown in Figure 5c, which summarizes the performance metrics measured across multiple devices.

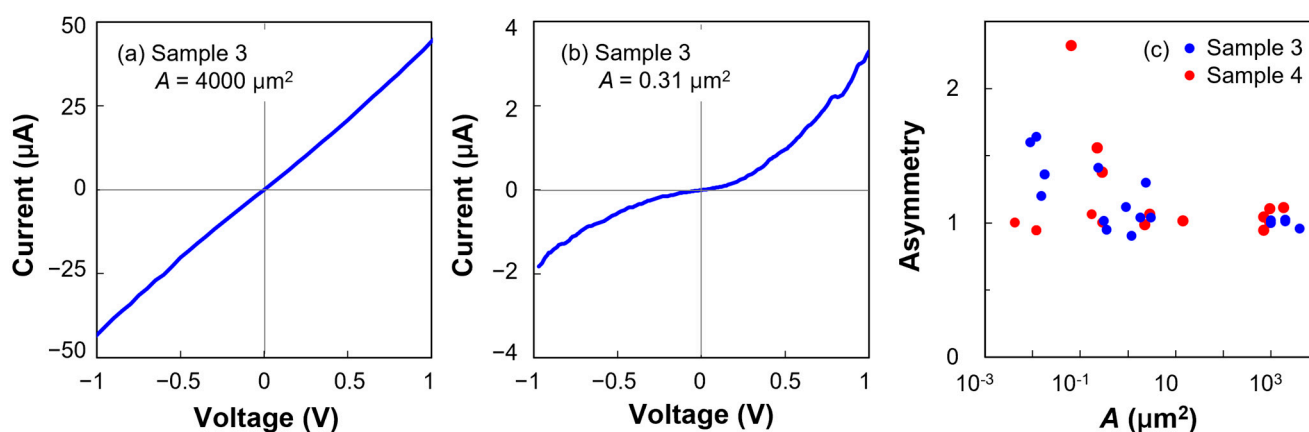


Figure 5. I - V characteristics of Sample 3 with different junction areas (A) of (a) 4000 and (b) 0.31 μm². (c) Dependence of the extracted asymmetry on A , showing increased asymmetry for smaller devices (Samples 3 and 4).

A large-area device with an active junction area of 4000 μm² exhibited nearly symmetric I - V behavior, whereas a nanoscale device with an active junction area of 0.31 μm² showed pronounced nonlinearity and asymmetry. The extracted asymmetry, defined as the ratio of current at V of ± 1 V, increased systematically with decreasing junction area, as summarized for multiple devices in Figure 5c. Diode characteristics were observed for Samples 3 and 4 when the junction area was sufficiently small, and increased nonlinearity was obtained in devices with miniaturized antenna structures [48]. The nonlinear and asymmetric I - V characteristics were mainly associated with the formation of small

graphene overlap regions defined by electron-beam lithography. These results suggest that geometric effects can induce I - V asymmetry more effectively than stacking dielectric layers with different band gaps and electron affinities. The electric-field concentration and edge-dominated transport in the small overlap region likely amplified the nonlinear I - V characteristics of the tunnel junction. Developing a quantitative framework that incorporates geometry-dependent electric fields and transport physics will be important for future analysis.

Although the stacked $\text{Al}_2\text{O}_3/\text{SiO}_2$ dielectrics formed an asymmetric tunnel barrier, large-area GI^2G devices exhibited nearly linear I - V characteristics because tunneling current was area-averaged between symmetric graphene electrodes. Owing to their thinner tunnel dielectrics, Sample 3 devices exhibited currents 10^2 – 10^3 times larger than those of Sample 4 devices. In contrast, Sample 4 devices showed greater nonlinearity, which was attributed to the thicker SiO_2 layer suppressing the tunneling current.

The photoresponse characteristics of Sample 3 devices were evaluated (Figure 6). When the device was illuminated with simulated solar light, an increase in current attributed to the photoconductive effect occurred, indicating the generation of charge carriers in graphene. Photoresponse behavior was observed for Samples 3 and 4 devices. In particular, Sample 3 devices showed a larger modulation current and higher photoresponsivity compared with Sample 4 devices. Furthermore, the photoresponse was measured under zero bias conditions, and a measurable current was observed without an applied bias voltage (Figure 6b). The apparent power conversion efficiency (APCE) increased with decreasing graphene overlap area, reaching approximately 0.01% (Figure 6c). Sample 3 devices exhibited a slightly higher APCE compared with Sample 4 devices, suggesting that asymmetric and nonlinear diode characteristics might play an important role in the observed photoresponse. Although the definitions of efficiency and measurement conditions differ across studies, our result is comparable to graphene geometric diodes [47] and higher than several reported CNT-based diodes [44,45], point-contact MIM diodes [40], and MI^2M diodes [43], which typically exhibit efficiencies in the range of $10^{-3}\%$ or less. Reported efficiencies in these devices were often limited by low optical absorption, series resistance, and impedance mismatch between the antenna and diode. The graphene-based tunnel diodes may help mitigate some of these limitations. It should be noted that the APCE represents the apparent device-level power conversion efficiency and may include contributions from both high-frequency rectification and thermal effects arising from illumination. Further wavelength-resolved analysis will be necessary to clarify the underlying mechanism.

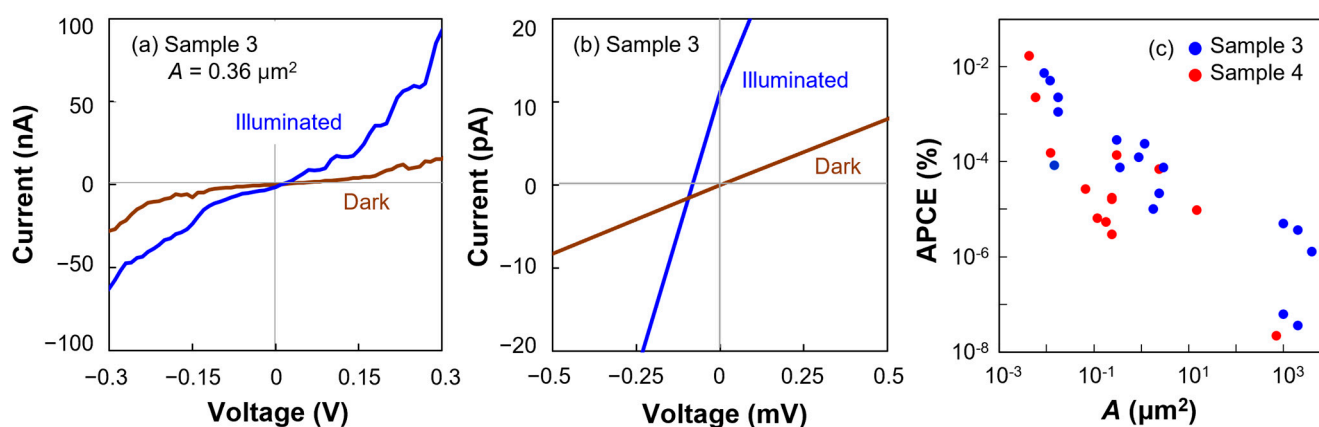


Figure 6. (a) I - V characteristics of Sample 3 with a junction area (A) of $0.36 \mu\text{m}^2$, measured in the dark (brown) and under illumination (blue). (b) Photoresponse characteristics of Sample 3 under dark and illuminated conditions near zero bias. (c) Dependence of the apparent power conversion efficiency (APCE) on A (Samples 3 and 4).

4. Conclusions

We fabricated graphene-based vertical tunnel diodes with $\text{Al}_2\text{O}_3/\text{SiO}_2$ dielectrics of different band gaps and electron affinities, sandwiched between graphene layers. The diodes exhibited asymmetric I – V characteristics, with a small overlap region defined by electron-beam lithography. Geometric asymmetry introduced by reducing the graphene overlap area was key to increasing diode nonlinearity, surpassing the effect of the dielectric structure alone.

Photoresponse measurements under AM1.5G illumination revealed a clear photocurrent, suggesting a possible rectification-related response. The photoresponse increased with decreasing junction area, which is consistent with the observed asymmetric behavior. These results suggest that electric-field concentration and edge-dominated transport in nanoscale junctions may improve rectification behavior.

Although the optical absorption efficiency of the device was not quantitatively evaluated in this study, integrating this device into plasmonic nanostructures may increase optical absorption via localized surface plasmon excitation [52]. The present findings highlight the potential of GI^2G tunnel diodes for next-generation energy harvesting and optical sensing applications.

Supplementary Materials: The following supporting information can be downloaded at: <https://www.mdpi.com/article/10.3390/c12010018/s1>. Figure S1: Schematic energy band diagrams of the GI^2G structure and Figure S2: Raman spectrum of graphene on a Si/SiO_2 substrate.

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Conflicts of Interest: The authors have no conflicts to disclose.

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