Review
An Overview of State-of-the-Art D-Band Radar System Components

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Abstract: In this article, a literature study has been conducted including 398 radar circuit elements from 311 recent publications (mostly between 2010 and 2022) that have been reported mainly in the F-, D- and G-Band (80–200 GHz). This study is intended to give a state-of-the-art comparison on the performance of the different technologies—RFCMOS, SiGe/BiCMOS and III–V semiconductor composites—regarding the most crucial circuit parameters of Voltage-Controlled Oscillators (VCO), Power Amplifiers (PA), Phase Shifters (PS), Low-Noise Amplifiers (LNA) and Mixers. The most common topologies of each circuit element as well as the differences between the technologies will further be laid out while reasoning their benefits. Since not all devices were derived solely from single device publications, necessary steps to yield as fairly a comparison as possible were taken. Results include the area and power efficiency in RFCMOS, superior noise and power performance in III–V semiconductors and a continuous compromise between efficiency and performance in SiGe. The most rarely published devices, being Mixers and PSs, in the given frequency range have also been identified to give incentive for further developments.

Keywords: III–V semiconductor; D-Band; F-Band; G-Band; Low-Noise Amplifier; Mixer; Phase Shifter; Power Amplifier; radar circuits; RFCMOS; SiGe

1. Introduction

A lot of scientific interest has been invested in the D-Band in the last few years due to its relatively low atmospheric attenuation [1] at high frequencies. This is exploited by novel D-Band systems in the unregulated ISM-Band (122–123 GHz) [2], the potential automotive-band (134–141 GHz) [3] and various, recently FCC, Ofcom as well as CEPT/ETSI-approved industrial frequency bands above 100 GHz [4]. Especially radar systems have grown in significance, as they have been used in different applications such as imaging, near-field communications, wireless personal area networks or distance/velocity measurements [5–8]. This increased demand facilitated not only continuous scaling of technologies such as RFCMOS, SiGe HBT or III–V semiconductor composites (e.g., InP or GaAs) but also led to higher transit (ct. Figure 1) and oscillation frequencies.

Furthermore, these technologies are supported by new advances in packaging such as Wafer-Level Packaging (WLP) [9], allowing for more reliability whilst increasing the performance not only for single- but also multi-technology systems compared to wire-bond techniques.

To oversee new progress in the multitude of different devices published each year, surveys such as [10,11] have been conducted. They, however, only focus on single device publications for a specific circuit element, leaving out its performance in radar systems. As a result, this overview is meant to present the current state-of-the-art performance of all devices that are crucial for a radar system in the mentioned technologies around 140 GHz.
2. Radar Circuit Elements

Universally, radar systems are composed of a signal source and at least one transmit (Tx) and one receive path (Rx). A Voltage-Controlled Oscillator (VCO) generally locked in a Phase-Locked Loop (PLL) constitutes the signal source. The frequency-stabilized signal has either a static frequency as is the case for Continuous Wave (CW) or will be modulated for Frequency-Modulated Continuous Wave (FMCW) applications. Depending on the frequency of the VCO and the amount of Tx/Rx channels, frequency multiplication and distribution networks are required. Both have been omitted from this study, because their shortcomings can be compensated by buffer stages and the data can be adjusted theoretically.

A Tx primarily focuses on delivering as much power as possible to antennas in order to increase the Link Budget (LB) of the system as stated by the radar equation [12]:

$$LB = \frac{P_{Rx}(r)}{S_i},$$

$$P_{Rx}(r) = \frac{P_{Tx}G_{Tx}G_{Rx}\lambda^2\sigma_{Antenna}}{(4\pi)^3r^4}. \quad (1)$$

For this reason, a Power Amplifier (PA), divided into different stages, and/or multiple PAs combined in parallel (power combining) are used. The succeeding antennas might have to be driven with different phases in Multiple Input Multiple Output (MIMO) radars to enlarge the virtual array size or achieve beamsteering capabilities. This can be completed by applying phase shifters (PSs).

Owing to a typically low signal level caused by the free space loss (Equation (1)), the received signal ought to be amplified. A Low-Noise Amplifier (LNA) is usually employed for this purpose to retain a high Signal to Noise Ratio, which is the result of the LNA’s low noise contribution and the reduced noise impact of all following elements. Lastly, the frequency of the amplified signal is downconverted to a lower-frequency range for digital signal processing typically by utilizing the VCO signal at a Mixers Local Oscillator input.

All previously mentioned circuit elements will be separately investigated in the following sections.
2.1. Voltage-Controlled Oscillator (VCO)

A VCO is a circuit element that changes its output frequency depending on the applied tuning voltage. Unlike the other circuit elements in this overview, it is not necessarily employed at D-Band frequencies but rather at lower frequencies to decrease the VCOs complexity and ensure correct operation with improved performance. The subsequent lower frequency signal is then upconverted by frequency multipliers such as doubler or tripler architectures. A radar operating frequencies therefore depends on the frequency multiplied carrier frequency $f_c$ and the Frequency Tuning Range (FTR) [12]:

$$FTR = \frac{f_{\text{max}} - f_{\text{min}}}{f_c} \cdot 100\%$$  \hspace{1cm} (2)

of the VCO. As FTR stays constant regardless of the operating frequency, it can be used to compare the tunability of VCOs in the D-Band. Figure 2 displays the FTR for all gathered VCOs where each unique shape represents a different topology according to given legend. Exemplary VCOs were collected outside the F-, D- or G-Band to give an estimation of VCOs at lower frequencies. A decreasing trend of FTR with $f_c$ can be determined. Additionally, the technologies are primarily distributed in specific frequency bands such as the K-/E-Band for RFCMOS, the U-/W-Band for III–V semiconductors or the Ka-/D-Band for SiGe. Based on the lack of SiGe in the W-Band, this is likely a statistical artifact emerging from publications not being sought out excessively below the F-Band.

![Figure 2. VCO: Frequency Tuning Range as function of the Center Frequency in the frequency range of 13.895–208.55 GHz.](image)

The most dominant characteristic to assess a VCO on is the Phase Noise (PN). It describes the intensity of undesired frequency components in relation to $f_c$ and is therefore measured in $\text{dBc}/\text{Hz}$ [12]. These undesired frequency components might be downconverted or emitted, worsening the detectability of radar targets. Due to the exponential drop in PN starting from the $f_c$, it is imperative to use equal Offset Frequencies and Measurement Bandwidths when comparing VCOs. Offset Frequencies of 1 MHz and Measurement Bandwidths of 1 Hz were collected whenever possible. When the PN of all collected VCOs in Figure 3 is inspected, a distinct frequency dependency is visible. The higher the frequency, the more PN is generally introduced into the system. As a result, one might assume that frequency multiplied low frequency oscillations perform better than higher frequency signals. That assumption, however, does not take the added phase noise due to frequency multiplication into account. If a Frequency Multiplication Factor $N$ were to be defined as:

$$N = \frac{f_\text{target}}{f_c},$$  \hspace{1cm} (3)

the according PN addition to reach the desired frequency $f_{\text{target}}$ can be derived to be [13]:

$$\Delta L(N\omega_0) = \Delta L(\omega_0) + 20 \cdot \log_{10}(N).$$  \hspace{1cm} (4)
Figure 3. VCO: Phase Noise as a function of the Center Frequency. Dashed lines mark the $\pm 2\sigma$ interval in accordance with Leeson’s equation.

To put it into perspective, 6 dBc/Hz of PN is added per doubler and 9.5 dBc/Hz is added per tripler stage. It should be pointed out here that SiGe and RFCMOS publications readily make use of push–push doublers to achieve higher operating frequencies while attenuating the fundamental $f_c/2$ as well as odd harmonics $(2n + 1) \cdot f_c/2, \forall n = N$. Since the doublers’ non-ideal contribution cannot be removed, nor the losses estimated, they will not be accounted for rather but seen as a part of a higher frequency VCO. A more comprehensible illustration of the corrected PN alongside the mean PN of the specific technologies is given in Figure 4 for a $f_{\text{target}}$ of 140 GHz. From it, an increase in Phase Noise of about 3 dB is present on average between SiGe ($-89.46$ dBc/Hz), RFCMOS ($-86.56$ dBc/Hz) and III–V semiconductor composites ($-83.32$ dBc/Hz). By examining the value spread, one can determine the consistency of the PN performance. SiGe has a larger span, whereas RFCMOS and III–V semiconductors display more reliable values.

Figure 4. VCO: Phase Noise adjusted by the required multiplication stages to reach 140 GHz. Horizontal lines represent mean values.

Another important trait of VCOs is the Output Power $P_{\text{Out}}$ that is shown alongside the DC-Power Consumption $P_{\text{DC}}$ in Figure 5. High $P_{\text{Out}}$ allows for less/no buffer stages to be used to compensate potential losses. These buffer stages would also generate noise, which can be largely disregarded as it is Amplitude Noise and not Phase Noise [14]. It has to be noted that the presence of buffer stages, that could not be de-embedded, might result in the data instead reflecting on the performance of those buffers. Nonetheless, a linear relation between $P_{\text{Out}}$ and $P_{\text{DC}}$ is apparent. Higher $P_{\text{Out}}$ thus necessitates a higher $P_{\text{DC}}$. Moreover, the technologies evidently differ in DC-Power. The lower spectrum of Figure 5 is almost entirely made up of RFCMOS devices, whereas higher $P_{\text{DC}}$ are seen first in SiGe and then in III–V semiconductors.
Figure 5. VCO: Output Power as a function of the DC-Power Consumption in the frequency range of 13.895–208.55 GHz. Dashed lines mark the ±2σ interval.

A consideration of the topology leads to a vastly dissimilar circuit structure between VCOs from different technologies. Whereas RFCMOS heavily favors a cross-coupled structure as a result of an easy start-up with lower power consumption (cf. Figure 5), SiGe uses its higher transconductance $g_m$ to drive colpitts/hartley VCOs that usually have better noise and power performance (Figures 3–5) [15,16]. Considering that a decent number of III–V semiconductor VCOs could only be gathered prior to 2010 (see Figure 1), a lot of miscellaneous (Misc) circuit concepts were found alongside the prevalent cross-coupled and colpitts structure. Of additional note in this case are Resonate Tunneling Diode (RTD)-based VCOs that allow for extremely low-power oscillations (cf. Figure 5) when a low voltage is applied [17]. Another interesting detail is exposed when the varactor of the technologies is inspected. While the respective transistor type is used in RFCMOS (MOS-varactor) and III–V semiconductors (HBT/HEMT-varactor), SiGe HBT VCOs are commonly seen using MOS-varactors. This is mainly due to MOS-varactors having a comparable Q-factor as well as no imminent danger to forward bias pn-junctions at low Tuning Voltages [18].

2.2. Power Amplifier (PA)

PAs are typically driven in saturation, if no amplitude modulation is required, to generate a constant high Output Power $P_{sat}$. $P_{sat}$ is generated by an average of 3.07/3.46/3.65 PA stages in SiGe/RFCMOS/III–V semiconductors, which are divided into multiple buffer/gain stages and an output stage. Generally, both stage types are of a similar kind of topology, which is why buffer/gain stages will not be touched on further.

A commonly used circuit modification to increase the Output Power is to connect multiple PAs in parallel (power combining). Power combining takes the form of either transmission line- or transformer-based combining, depending on the technology that is used. Resulting from the relatively low Q-factor of passive structures in RFCMOS, transformers are not only used to connect the different PA stages but also to link parallel PAs. This has the added benefit of a spatially low power increase. Two different transformer combining variants can be distinguished, being voltage- and current combining. Voltage combining uses one coil to enclose both load coils of the parallel PAs, whereas current combining employs a coil for each load coil with one terminal shorted to ground. The low output impedance provided by voltage combining is favored at lower frequencies in contrast to the lower parasitic influence of current combining at higher frequencies [19]. Moreover, different turn ratios allow for offsetting the restrictions of current combining, resulting in no voltage combiner being used in the whole dataset. For the other technologies, transmission-line based combining such as Wilkinson dividers/combiners were almost exclusively used. This has likely to do with the high area consumption of transformers.
In terms of the added Output Power, power combining does not reflect on the employed technology, instead adding $3 \text{ dB} \cdot \log_2(N)$ assuming N lossless, parallel and saturated stages. Its ideal contribution has consequently been removed in Figure 6, which also displays the mean $P_{\text{sat}}$ of each technology ($P_{\text{sat, SiGe}} = 11.82 \text{ dBm}$, $P_{\text{sat, RFCMOS}} = 8.67 \text{ dBm}$, $P_{\text{sat, III–V}} = 15.16 \text{ dBm}$). III–V semiconductor components deliver a higher output power than its two competitors. Its data points are also moderately grouped up, ensuring usually high $P_{\text{sat}}$ in these devices. Likely by virtue of parity issues in III–V semiconductors, single-ended structures make up the majority its publications. Benefits of differential techniques such as the increased Common-Mode-Rejection Ratio (CMRR) are therefore not present in III–V semiconductor PAs. A low variation and thus reliable values are also seen in RFCMOS alongside modest $P_{\text{sat}}$. This comparatively low $P_{\text{sat}}$ can largely be attributed to low breakdown voltages, which necessitate lower gain and deep-well processes for cascode structures [20–23]. Thus, the Miller effect is canceled, and the stability is increased through neutralization capacitance in common source/emitter (CS) circuits instead [24]. In contrast, mainly cascode stages to suppress the Miller effect and leverage the high $g_m$ of SiGe let it compete with both technologies as a result of larger deviations from its mean [25–28].

![Figure 6. PA: $P_{\text{sat}}$ per power combining stage in the frequency range of 90–190 GHz. Horizontal lines represent mean values.](image)

A high $P_{\text{sat}}$ in a PA can only be considered a merit if it is accompanied by a sufficiently high enough amplification factor (Gain). It is mostly reported as the Small Signal Gain, i.e., the Gain in the linear region. Although not specifically noted here, the Gain-Bandwidth Product is also commonly used to express the Gain of a PA. Since the bandwidth could not be estimated with enough certainty, it was left out of this study. Nevertheless, distributed amplifiers can be highlighted as having the highest recorded bandwidths. When the Gain is set into relation with the DC Power Consumption (Figure 7), it is customarily compiled into a different criterion called the Power-Added Efficiency PAE [29]:

$$\text{PAE} = \frac{P_{\text{in}} \cdot (\text{Gain} - 1)}{P_{\text{DC}}} \cdot 100\% = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC}}} \cdot 100\%$$  \hspace{1cm} (5)

to estimate the efficiency of PAs. From Figure 8, RFCMOS devices can be deduced as having the highest PAE in their respective $P_{\text{sat}}$ region. The next highest efficiency is displayed in SiGe. Yet, to achieve the highest $P_{\text{sat}}$, III–V semiconductor composites become indispensible. From a closer inspection of Figure 8, common base/gate (CB) stages emerge as one of the best topologies for high $P_{\text{sat}}$. The reason behind this, as is explained in [30], is that CB stages grow more efficient than common emitter stages as the Operating Frequency approaches $f_T$. $f_T$ conversely is strongly dependant on the current density $j_C$ and thus $P_{\text{sat}}$ by prospect of the linear relation between $P_{\text{sat}}$ and $P_{\text{DC}}$. The improved efficiency added to a non-class A operation facilitates low power consumption, thus yielding high PAE.
In cases where modulation (e.g., in communication systems) of the emitted signal is relevant, linearity becomes one of the focal points of PAs. A heavily used criterion is the First-Order Compression Point (P1dB), which can be further divided into an Output Referred (OP1dB) or an Input Referred Compression Point (IP1dB). It references a 1 dB variation between the course of the output power and the extrapolation of the linear region. Albeit the OP1dB is typically of higher interest for PAs, both compression points are given in Figure 9. An analysis of the technologies yields increased linearity in III–V semiconductors compared to SiGe and SiGe compared to RFCMOS. In terms of topology, the highest linearity is seen in single-ended devices.

Figure 7. PA: Gain as a function of the DC Power Consumption in the frequency range of 90–190 GHz.

Figure 8. PA: PAE as a function of Psat in the frequency range of 90–190GHz.

Figure 9. PA: Linearity shown in OP1dB vs. IP1dB from 90–190 GHz.
2.3. Phase Shifter (PS)

The phase of a signal can be adjusted by applying either a passive, reflective or vector modulated (VM) PS. The different architectures mainly differ in terms of Resolution, Gain and linearity. Active VM-PSs generally have a higher Resolution and Gain [31], whereas the linearity in the passive architectures is higher [32]. Since the Resolution is intrinsically linked to the utilized bitwidth of PSs, Figure 10 only shows the Gain of the reported PSs.

The bulk of the data, especially for RFCMOS, was accumulated in the lower F- and higher W-Band on the account that only a few PS were reported in the D-Band. The scarcity of the data allows for no conclusive performance statements. Only passive phase shifters, divided into Reflection-Type Phase Shifters (RTPS) and switched passive elements, were reported for III–V semiconductors, whereas a greater number of active devices are present for the other technologies. These active components can largely be divided into two subcategories: Switched-Quad (the sole VM-PS in RFCMOS) and Vector-Sum (exclusively present in SiGe). They differ from each other simply by their polarity/phase selection. While the digital select signals are directly applied at the Gate/Base of the switching Quads (akin to setting VDD to a Gilber–Cell transistor quad), vector summing involves numerous selections by SPDT-Switches and phase shifts by a multitude of couplers. Additionally, multiple Vector-Gain Amplifiers (VGA) to sufficiently cover the coupler losses as well as provide adequate resolutions are required. The Resolution and Gain of switching quads depend on the number of quads or pre-amplifiers used, which will not be covered in this study. As for the differences between RFCMOS and SiGe, a similar average Gain in the examined frequency bands is exhibited. For the same frequency range, however, SiGe outperforms RFCMOS.

In order to assess the phase and amplitude imbalances in each PS state, Root Mean Square (RMS) errors are most commonly used. Both the RMS Gain as well as the RMS Phase Errors are depicted in Figure 11. Disproportionally higher Phase Errors in RFCMOS and Gain errors in SiGe were reported when comparing the technologies. These devices almost exclusively belong to the vector-sum/switched-quad PSs for SiGe/RFCMOS. Thus, it can be estimated that the complexity in those devices is at fault for their poor RMS errors. The other devices and especially the passive devices in III–V composite devices, with its only poor performing device being an outlier, accomplished low RMS errors.

![Figure 10. PS: Gain as a function of the frequency.](image-url)
2.4. Low-Noise Amplifier (LNA)

As the first active element in the receiver chain, the LNA’s noise contribution $F_1$ has the strongest impact on a system’s Noise Figure (NF) in accordance with Friis’ formula [12]:

$$\text{NF}_{\text{receiver}} = 10 \cdot \log_{10} \left( F_1 + \sum_{i=2}^{n} \frac{F_i - 1}{\prod_{j=1}^{i-1} \text{Gain}_j} \right).$$ (6)

This noise contribution differs noticeably between III–V semiconductors and both SiGe and RFCMOS as is evident from Figure 12. On average, the lowest Noise Figure can be achieved in III–V semiconductors ($\text{NF}_{\text{III–V}} = 3.67 \text{ dB}$). In contrast to the other two technologies, only single-ended amplifiers were used because they exhibit better noise performance than differential ones. RFCMOS and SiGe devices in comparison show an almost equal NF with the former having a higher discrepancy and thus yielding slightly worse average values ($\text{NF}_{\text{RFCMOS}} = 7.77 \text{ dB}$) compared to latter ($\text{NF}_{\text{SiGe}} = 7.48 \text{ dB}$). Another important NF contributor is the interconnects in each technology. While low loss/noise Grounded-Coplanar Wave Guides (GCPW) are commonly used in III–V semiconductors, transformer and transmission line losses in RFCMOS and SiGe, respectively, may increase their NF.

While $F_1$ does not become reduced by any other circuit element, an LNA decreases the noise contribution $F_i$ of all following elements by its Conversion Gain (CG) as stated in Equation (6). Usually, a compromise between the LNAs NF and the Gain, as Figure 13 illustrated, has to be carried out. This compromise also appears in the choice of topology wherein the increased Gain of a cascode stage worsens the NF due to the contribution of the common base/gate stage when contrasted with common source/emitter (CS) stages [33–35]. To offset the Gain difference, more stages are usually employed in CS LNAs [36]. This leads to the least amount of Gain stages (1–4 stages) being used in SiGe devices with 2.74 stages on average, even though among the highest Gains were demonstrated. In stark contrast, RFCMOS has the largest span with 1–8 stages and a mean stage amount of 3.96, while the overall lowest CG was repeatedly reported. Lastly, III–V semiconductors can be highlighted as having the best mean Gain whilst averaging 3.71 stages within a range of 2–4 stages.

Linearity is also of prime concern for LNAs because the systems dynamic range may be restricted as a result of intermodulation distortion (e.g., blocking or cross-modulation) [13]. Nevertheless, a lack of available data is apparent from Figure 14. This scarcity might be explained by low signal levels emerging from the free space loss (ct. Equation (1)) and the corresponding rarely arising need to measure it. EM-crosstalk resulting from a PA in close proximity, however, could occur, increasing the input power past the IP1dB. From the limited data, III–V semiconductors seem to be the least affected by those effects. Whether
SiGe or RFCMOS devices possess better linearity, however, is not decisive due to the data shortage. Another statistical uncertainty is the higher linearity in differential devices in contrast to their single-ended equivalents.

Figure 12. LNA: Noise Figure in the frequency range of 78.5–195 GHz. Horizontal lines represent mean values.

Figure 13. LNA: Conversion Gain over DC power consumption in the frequency range of 78.5–200 GHz.

Figure 14. LNA: Linearity shown in OP1dB and IP1dB for a frequency range of 95–190 GHz.

2.5. Mixer

Frequency conversion is a method to decrease (downconvert) or increase (upconvert) the frequency of a signal by either transistor switching as is the case for gilbert cells or by using the transconductance of a nonlinear element such as diodes or transistors. Since only downconverters are conventionally employed in radar receive paths, they have been exclusively analyzed in this study. In downconverters, the received signal is
applied to the RF-Port, the (frequency multiplied) VCO signal is connected to the LO-Port and the generally baseband frequency output is generated at the IF-Port. Yet, in the investigated publications, Mixers have been operated with varying IF-Frequencies, spanning from 1 MHz to 31 GHz (IF = 3.71 GHz). This prevents a definitive comparison from being conducted as a consequence of the differing intensity of frequency dependent effects such as the 1/f-Noise. The results should thus be regarded with caution. As an element in the receiver chain, one of the most important characteristics of a mixer is its NF. The lowest average noise contribution, discerned from Figure 15, is $\overline{\text{NF}} = 10.43$ dB in III–V semiconductors. The different III–V semiconductor devices also achieve values in close proximity to each other, exemplifying the feasibility of this NF. Having competitive values with III–V semiconductors, SiGe has a high data spread that results in a worse mean NF with a value of 13.6 dB. Further investigations are required to give a conclusive statement about RFCMOS’s noise performance. Disregarding the outlier with the worst Noise Figure, values similar to the other two technologies are attained. In this case, RFCMOS performs the best on average out of the three investigated technologies. With the outliers, however, the worst average NF is reported (14.91 dB).

Since the lack of data is also present in other categories such as the DC power consumption, the CG of the gathered mixers is separately shown in Figure 16. A comparable CG range is accomplished in all three technologies. The value distribution, however, distinguishes III–V semiconductor mixers as having the worst ($\overline{\text{CG}}_{\text{III–V}} = -6.12$ dB) and SiGe as having the best ($\overline{\text{CG}}_{\text{SiGe}} = 7.46$ dB) mean CG. RFCMOS, meanwhile, has a uniform dispersal of CGs ($\overline{\text{CG}}_{\text{RFCMOS}} = -3.4$ dB). This distribution might be connected to the utilization of buffer stages, in which case the CG would reflect on the performance of those buffer stages instead of the mixers.

![Figure 15. Mixer: Noise Figure in the frequency range of 90–200 GHz. Horizontal lines represent mean values.](image)

![Figure 16. Mixer: Conversion Gain in the frequency range of 90–200 GHz. Horizontal lines represent mean values.](image)
High LO-Powers typically facilitate an improved mixer operation. Depending on the LO-RF Isolation of the mixer, a significant amount of this power might be forwarded to the RF-Port, causing interference, disturbance or emission in the Rx. If an LNA is present, this effect can largely be neglected due to the LNA’s high reverse isolation. However, without an LNA, the LO-RF Isolation becomes an important, rarely reported mixer parameter that can only be compared indecisively as Figure 17 demonstrates. The limited data show that the isolation is consistently high in RFCMOS, lower with a higher spread in SiGe, and it has a broad range with both low and high values in III–V semiconductors.

In regard to the mixer topologies, the most widespread architecture depends on the respective technology. Because of the modest 1/f noise performance in RFCMOS and III–V composites, the least amount of transistors should carry out the frequency conversion. Hence, resistive mixers and single-device transconductance mixers have become common. They additionally benefit from an increase in linearity, which is confirmed in the gathered data, with no discernable effect on the NF. Contrastingly, Gilbert cells or cascode transconductance mixers are usually seen in SiGe publications. While Gilbert mixers are known to typically demonstrate the highest Gains (cf. Figure 16), no improved Isolation in comparison to the other architectures could be verified [37,38].

![Figure 17. Mixer: LO-RF Isolation in the frequency range of 90–180 GHz. Horizontal lines represent mean values.](image)

3. Conclusions

The three most commonly used technologies—RFCMOS, SiGe HBT and III–V semiconductor composites—have been investigated by means of a literature study. Insight was given into the most crucial radar circuit parameters, and the technologies were compared based upon them. Particularly, the low cost connected with the efficiency both in area and power consumption (cf. Figures 18 and 19) alongside the ease of baseband interfacing are favorable traits in RFCMOS. Additionally, no substantial noise variation between RFCMOS and SiGe was determined. Yet, its high-frequency struggle with rather poor output power hampers its practicality. In stark contrast, III–V semiconductor devices excel at attaining the highest possible performance in single devices, but they are held back by high production costs, high area and power consumption as well as fewer fabrication facilities. Lastly, the usage of the widely established SiGe HBTs leads to a compromise between efficiency and performance, which is why it is the most common technology for D-Band radar systems.
Figure 18. Average Area Consumption of all circuit elements.

Figure 19. Average DC Power Consumption of all circuit elements.

4. Disclaimer

The authors are not liable for any inaccuracy or falsities connected with assuming, calculating and/or estimating values from the publications based on the given diagrams and data. The data were taken from the provided measurement plots whenever possible, and data non-conforming to the principles and comparison methods used in this study were adjusted accordingly. The authors are not accountable for any future use of this study.
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**References**


22. Li, S.; Rebeiz, G.M. High Efficiency D-Band Multiway Power Combined Amplifiers with 17.5–19-dBm Psat and 14.2–12.1% Peak PAE in 45-nm CMOS RFSOI. IEEE J. Solid-State Circuits 2022, 57, 1332–1343. [CrossRef]


25. Kucharski, M.; Borngräber, J.; Wang, D.; Kissinger, D.; Ng, H.J. A 109–137 GHz power amplifier in SiGe BiCMOS with 16.5 dBm peak output power and 12.8% PAE. In Proceedings of the 2017 47th European Microwave Conference (EuMC), Nuremberg, Germany, 10–12 October 2017; pp. 1021–1024. [CrossRef]


34. Weber, R.; Massler, H.; Leuther, A. D-band low-noise amplifier MMIC with 50% bandwidth and 3.0 dB noise figure in 45-nm mHEMT technology. In Proceeding of the 2017 IEEE MTT-S International Microwave Symposium (IMS), Honolulu, HI, USA, 4–9 June 2017; pp. 756–759. [CrossRef]


37. Deng, X.-D.; Li, Y.; Wu, W.; Xiong, Y.-Z. D-band down conversion chipset with I-Q outputs using 0.13µm SiGe BiCMOS technology. In Proceeding of the 2015 IEEE 11th International Conference on ASIC (ASICON), Chengdu, China, 3–6 November 2015; pp. 1–4. [CrossRef]


63. Khamaisi, B.; Socher, E. A 159–169 GHz frequency source with 1.26 mW peak output power in 65 nm CMOS. In Proceedings of the 2013 European Microwave Conference, Nuremberg, Germany, 6–10 October 2013; pp. 1507–1510. [CrossRef]
64. Volkerts, W.; Steyaert, M.; Reynaert, P. 118 GHz fundamental VCO with 7.8% tuning range in 65 nm CMOS. In Proceedings of the 2011 IEEE Radio Frequency Integrated Circuits Symposium, Baltimore, MD, USA, 5–7 June 2011; pp. 1–4. [CrossRef]
77. Yin, J.; Luong, H.C. A 57.5–90.1 GHz Magnetically Tuned Multimode CMOS VCO. IEEE J. Solid-State Circuits 2013, 48, 1851–1861. [CrossRef]
81. Akhter, N.; Amin, M.T.; Faruque, O. A High Figure of Merit Low Power LC VCO for D Band Applications. In Proceedings of the 2019 22nd International Conference on Computer and Information Technology (ICCIT), Dhaka, Bangladesh, 18–20 December 2019; pp. 1–6. [CrossRef]


112. Toupé, R.; Deval, Y.; Bégueret, J. A 125GHz LC-VCO in a SiGe:C Technology dedicated to mmW applications. In Proceedings of the 2010 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Austin, TX, USA, 4–6 October 2010; pp. 1–4. [CrossRef]


114. Kakani, V.; Jin, Y.; Dai, F.F. A 25 GHz wide-tuning VCO RFIC implemented in 0.13 um SiGe BiCMOS technology. In Proceedings of the 2010 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Austin, TX, USA, 4–6 October 2010; pp. 5–8. [CrossRef]


121. Jamal, F.I.; Wessel, J.; Kissinger, D. A low-power K-band Colpitts VCO with 30% tuning range in a 130 nm SiGe BiCMOS Technology. In Proceedings of the 2010 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Austin, TX, USA, 4–6 October 2010; pp. 1–4. [CrossRef]


123. Ali, U.; Fischer, G.; Thiede, A. Low power fundamental VCO design in D-band using 0.13 µm SiGe BiCMOS technology. In Proceedings of the 2015 German Microwave Conference, Nuremberg, Germany, 16–18 March 2015; pp. 359–362. [CrossRef]


198. Furqan, M.; Ahmed, F.; Auffinger, K.; Stelzer, A. A D-band fully-differential quadrature FMCW radar transceiver with 11 dBm output power and a 3-dB 30-GHz bandwidth in SiGe BiCMOS. In Proceedings of the 2017 IEEE MTT-S International Microwave Symposium (IMS), Honolulu, HI, USA, 4–9 June 2017; pp. 1404–1407. [CrossRef]


219. Pepe, D.; Zito, D. A 78.8–92.8 GHz 4-bit 0–360° active phase shifter in 28nm FDSOI CMOS with 2.3 dB average peak gain. In Proceedings of the ESSCIRC Conference 2015—41st European Solid-State Circuits Conference (ESSCIRC), Graz, Austria, 14–18 September 2015; pp. 64–67. [CrossRef]


222. de Wit, M.; Reynaert, P. An F-band active phase shifter in 28nm CMOS. In Proceedings of the 2017 IEEE MTTS International Microwave Symposium (IMS), Honolulu, HI, USA, 4–9 June 2017; pp. 965–968. [CrossRef]


224. Sayginer, M.; Rebeiz, G.M. A 94–96 GHz phased-array receive front-end with 5-bit phase control and 5 dB noise figure receive in 32 nm CMOS SOI. In Proceedings of the 2017 IEEE MTTS-S International Microwave Symposium (IMS), Honolulu, HI, USA, 4–9 June 2017; pp. 768–770. [CrossRef]


234. Sayginer, M.; Rebeiz, G.M. A 94–96 GHz phased-array receive front-end with 5-bit phase control and 5 dB noise figure receive in 32 nm CMOS SOI. In Proceedings of the 2017 IEEE MTTS-S International Microwave Symposium (IMS), Honolulu, HI, USA, 4–9 June 2017; pp. 768–770. [CrossRef]

235. Pepe, D.; Zito, D. A 78.8–92.8 GHz 4-bit 0–360° active phase shifter in 28nm FDSOI CMOS with 2.3 dB average peak gain. In Proceedings of the ESSCIRC Conference 2015—41st European Solid-State Circuits Conference (ESSCIRC), Graz, Austria, 14–18 September 2015; pp. 64–67. [CrossRef]


240. Testa, P.V.; Carta, C.; Ellinger, F. A 140–210 GHz Low-Power Vector-Modulator Phase Shifter in 130nm SiGe BiCMOS Technology. In Proceeding of the 2018 Asia-Pacific Microwave Conference (APMC), Kyoto, Japan, 6–9 November 2018; pp. 530–532. [CrossRef]


253. Elkhouly, M.; Glicic, S.; Ellinger, F.; Scheytt, J.C. 120 GHz phased-array circuits in 0.25 µm SiGe BiCMOS technology. In Proceeding of the 2012 The 7th German Microwave Conference, Ilmenau, Germany, 12–14 March 2012; pp. 1–4. [CrossRef]


Chips 2022, 1


Shumakher, E.; Elad, D. Towards a 120 GHz SiGe LNA for millimeter-wave imaging. In Proceeding of the 2011 IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems (COMCAS 2011), Tel Aviv, Israel, 7–9 November 2011; pp. 1–4. [CrossRef]


Liu, G.; Schumacher, H. 47–77 GHz and 70–155 GHz LNAs in SiGe BiCMOS technologies. In Proceeding of the 2012 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Portland, OR, USA, 30 September–3 October 2012; pp. 1–4. [CrossRef]


Aguilar, E.; Issakov, V.; Weigel, R. Highly-Integrated <0.14mm2 D-Band Receiver Front-Ends for Radar and Imaging Applications in a 130 nm SiGe BiCMOS Technology. In Proceeding of the 2019 IEEE 19th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), Orlando, FL, USA, 20–23 January 2019; pp. 1–4. [CrossRef]


Testa, P.V.; Riess, V.; Carta, C.; Ellinger, F. A 130 nm-SiGe-BiCMOS Low-Power Receiver Based on Distributed Amplifier Techniques for Broadband Applications From 140 GHz to 200 GHz. IEEE Open J. Circuits Syst. 2021, 2, 508–519. [CrossRef]

Stärke, P.; Seidel, A.; Carta, C.; Ellinger, F. Direct-Conversion Receiver Front-End for 180 GHz with 80 GHz Bandwidth in 130nm SiGe. In Proceeding of the 2017 12th European Microwave Integrated Circuits Conference (EuMIC), Nuremberg, Germany, 8–10 October 2017; pp. 5–8. [CrossRef]


Stärke, P.; Fritsche, D.; Carta, C.; Ellinger, F. A 24.7 dB low noise amplifier with variable gain and tunable matching in 130 nm SiGe at 200 GHz. In Proceeding of the 2017 12th European Microwave Integrated Circuits Conference (EuMIC), Nuremberg, Germany, 8–10 October 2017; pp. 5–8. [CrossRef]


Kanar, T.; Rebeiz, G.M. A low-power SiGe D-band total power radiometer with NEPmin of 1.4 fW/Hz½ and NETD of 0.25K. In Proceeding of the 2016 IEEE MTT-S International Microwave Symposium (IMS), San Francisco, CA, USA, 22–27 May 2016; pp. 1–4. [CrossRef]


310. Liu, Y.; Wen, J.; Wang, L. A D-Band Down-Conversion Mixer Based on 65 nm CMOS Technology. In Proceedings of the 2018 International Applied Computational Electromagnetics Society Symposium-China (ACES), Beijing, China, 29 July–1 August 2018; pp. 1–2. [CrossRef]


