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A Smart, Sensor-Augmented Probe Card for Wafer-Level Photonic Testing of Co-Packaged Optics Devices

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Abstract

The transition from electrical to optical interconnects, enabled by the adoption of co-packaged optics (CPO) in advanced processors, is accelerating the scale-up to high volumes and redefining wafer-level test requirements. As optical interfaces migrate closer to the compute die, an increasing share of functional characterization must occur at the probe, where stringent sub-micron alignment, the mechanical stability necessary to preserve optical coupling against dynamic disturbances, and opto-electrical co-validation introduce new technical challenges. Ensuring repeatable and precise fiber-array-unit (FAU) engagement at the wafer level is therefore essential to enable scalable manufacturing of photonic-enabled processors. This paper introduces the EclipsePhotonic probe card, which embeds the Eclipse Dynamic piezoelectric positioning mechanism into a standard vertical-needle probe head as a route toward six-degree-of-freedom FAU manipulation with nanometric positioning accuracy. This architecture is designed to support repeatable coupling to on-wafer photonic structures without requiring specialized probe-head designs, thereby reducing integration complexity and addressing alignment-related yield risks. The platform is also intended to support multi-site electrical and optical probing, providing a path toward parallel test execution once the corresponding layout, optical-routing, and validation constraints are satisfied. A core innovation of the platform is its embedded sensor network, which integrates low- and higher-frequency displacement sensors, relative displacement sensors, and temperature sensors around a microcontroller-based supervisor. The vibration sensor fulfills a dual operational role: it detects environmental and test-cell disturbances that may have influenced optical coupling, providing essential context for binning decisions or targeted retest, and it contributes to probe card lifecycle monitoring by ensuring that the mechanical signature of the probe card remains within a validated operational “swim lane” throughout its service life. Recently published characterization of the underlying Eclipse Dynamic alignment engine shows that, in the production-optimized high-speed regime with effective hysteresis compensation, the Fixed Gradient routine provides the best normalized trade-off among the evaluated routines, with a normalized alignment cost of 1.44 a.u., 95.8% convergence reliability, and 99.4% of the global maximum optical coupling. These values should be interpreted as inherited algorithmic benchmarking results rather than as absolute wall-clock performance of the fully integrated sensor-augmented platform.



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1. Introduction

The relentless growth of bandwidth requirements in data centers, high-performance computing and artificial-intelligence accelerators has driven the adoption of photonic integrated circuits (PICs) and is accelerating the high-volume scale-up of co-packaged optics (CPO) architectures in which optical input/output (I/O) is integrated next to the compute die [1,2]. This transition reshapes the wafer-level test requirements that have historically been tailored to electrical wafer sort (EWS): photonic devices introduce the critical requirement to establish a stable and repeatable optical interface between the device under test (DUT) and a fiber-array unit (FAU), alongside the conventional electrical contact challenge [3,4]. Because optical coupling efficiency degrades sharply with even sub-micron lateral (X-Y), vertical (Z), and angular misalignment, this interface must be established and maintained with nanometric precision while still being compatible with high-volume probing infrastructure.

Recent silicon-photonics and CPO roadmaps emphasize that this test challenge is intensifying as optical links move from board-level or pluggable modules toward package-proximal and package-integrated architectures [5–9]. Reviews on the adoption of photonics solutions in data centers further show that bandwidth scaling, energy efficiency and packaging density increasingly depend on the co-design of photonic devices, electronic drivers and high-throughput test infrastructure [10]. In this setting, wafer-level optical test is not only a screening operation; it becomes a manufacturing enabler that determines whether photonic-enabled compute packages can be reliably binned as Known Good Die (KGD) before expensive assembly, optical attach and package-level integration.

To help the reader navigate the current landscape of wafer-level photonic test solutions before the detailed review that follows, Table 1 summarizes the three architecture families discussed below alongside the proposed EclipsePhotonic platform.

Table 1. Summary of state-of-the-art wafer-level photonic test architectures compared with the proposed EclipsePhotonic platform.

Architecture Family	Alignment Approach	Key Limitation	Integration Profile
Dedicated photonics stations [3]	External precision motion systems with vision-assisted fiber positioning, mounted separately from the probe card	Effective for challenging edge-coupler geometries but difficult to integrate into a high-throughput wafer-sort flow	High mechatronic footprint; optical and electrical alignment handled by separate subsystems
Prober-adapted external-FAU systems [11]	External FAUs routed through prober cut-outs or peripherals, aligned via external stages	Reduces some setup burden relative to stand-alone stations, but preserves a substantial integration penalty	Reduced footprint versus dedicated stations; optical alignment remains external to the probe head
Embedded optical probe cards [12]	Optical hardware integrated directly into the probe card, in some cases using beam-expanding structures to relax alignment sensitivity	Reduced sensitivity to misalignment is typically obtained at the expense of insertion loss and optical budget	Compact, probe-card-centric, but without integrated sensing or self-awareness of mechanical state
EclipsePhotonic (this work)	FAU embedded in a standard vertical-needle probe head, actuated via an integrated six-degree-of-freedom piezoelectric flexure with optical-power feedback	Requires co-design of DUT layout for multi-site parallelism (see Section 6)	Probe-card-centric; tester-agnostic; embeds real-time structural health monitoring alongside optical alignment

Conventional industrial and research solutions for wafer-level photonic test rely on external positioning systems, vision assistance, hexapods, or dedicated photonics stations [3,11,12]. Although flexible, these solutions add mechanical complexity, footprint and cycle-time overhead, and they couple the optical alignment problem to a long mechatronic chain whose compliance, backlash and thermal drift accumulate at every joint. A more recent direction is to embed the optical interface directly into the probe card. In the Eclipse Dynamic concept introduced by Technoprobe, the FAU is integrated within the probe head, mounted inside a mechanical flexure, and actuated by an array of piezoelectric elements that drive translation and tilt of the FAU as a rigid block [13,14]. This architecture eliminates external fiber-positioning equipment during wafer-level photonic test, supports nanometric alignment behavior through optical-power feedback, and is structurally more compatible with multi-site parallelism than peripheral fiber stages. Following the initial feasibility demonstration of this concept, a comprehensive study systematically evaluated seven alignment algorithms on the Eclipse Dynamic hardware, demonstrating that under high-speed actuation with effective hysteresis compensation, the alignment engine achieves favorable normalized alignment performance using open-loop control hardware [15].

In parallel, recent work on probe card structural health monitoring (SHM) has shown that embedded sensor networks can support real-time monitoring, anomaly detection, failure forecasting and predictive maintenance in EWS applications. A recently developed artificial-intelligence-assisted framework for real-time monitoring and management of probe cards in EWS prioritizes the dominant failure modes from eight months of historical data, instrumenting the card with low- and higher-frequency displacement sensors, temperature sensors, and overtravel sensors networked through a microcontroller [16]. Subsequent contributions extended this framework with self-attention-based imputation of corrupted sensor streams [17], digital-twin-assisted optimal sensor placement [18] and a Transformer-based classifier capable of distinguishing baseline, loose-screw and crack health states from frequency-response data with very high accuracy [19]. Taken together, these results indicate that a probe card can plausibly monitor and dynamically assess its own mechanical state during test, translating that assessment into actionable production decisions.

The combination of these two trajectories defines a new class of wafer-level photonic test hardware: a probe card that not only aligns an FAU inside the probe head with sub-micron precision, but also continuously observes its own mechanical state and the test-cell environment. The present paper develops this concept under the name EclipsePhotonic. To clarify the nomenclature, Eclipse Dynamic refers specifically to the underlying piezoelectric positioning hardware integrated within the probe head, whereas EclipsePhotonic designates the complete, sensor-augmented probe card system and its various operational options. The architecture extends the integrated FAU to a six-degree-of-freedom positioning concept with nanometric target accuracy, retains compatibility with standard vertical-needle probe heads and standard probers, and adds an embedded sensor network for relative displacement sensing for measuring overtravel, dynamic displacement sensing for structural monitoring, and thermal monitoring. The contributions of this paper are threefold. First, we consolidate the system architecture of the EclipsePhotonic platform, including the integrated FAU motion stage, the sensor network and the management framework that connects them. Second, we summarize the demonstrated alignment performance of the underlying Eclipse Dynamic engine in the production-optimized high-speed, hysteresis-compensated regime, drawing on the recent algorithmic study [15] to establish what the optical alignment subsystem actually delivers. Third, we describe how the sensor-augmentation layer, derived from the AI-assisted EWS monitoring framework [16] and its data-integrity [17] and sensor-placement [18,19] extensions, transforms the probe card into a self-aware production asset suited to CPO-class wafer sort.

The remainder of the paper is organized as follows. Section 2 reviews the state of the art in wafer-level photonic testing and probe card monitoring, and identifies the technical gap addressed by the proposed EclipsePhotonic platform. Section 3 introduces the platform concept, including the integrated FAU positioning architecture, its compatibility with standard vertical-needle probe heads, and the rationale for extending the underlying Eclipse Dynamic concept toward six-degree-of-freedom alignment. Section 4 summarizes the demonstrated performance of the alignment engine in the production-oriented high-speed regime with effective hysteresis compensation (HS-NH), and discusses the data-profile analysis that motivates the selection of the Fixed Gradient routine as the baseline optical-power optimization method. Section 5 presents the embedded sensor network and management framework, with emphasis on distance and overtravel sensing, vibration-based test-context awareness, thermal monitoring, data-integrity support, and lifecycle diagnostics. Sections 6 and 7 describe the proposed wafer-level photonic test flow and discuss its expected implications for throughput, yield protection, and probe card reliability. Section 8 discusses the remaining validation steps required to qualify the EclipsePhotonic concept under production-like conditions, and Section 9 concludes the paper.

2. State of the Art and Technical Gap

2.1. Wafer-Level Photonic Test Approaches

State-of-the-art wafer-level photonic test can be grouped into three broad families. The first uses dedicated photonics stations in which fibers are positioned by precision motion systems mounted externally to the probe card (typically on separate manipulator arms) with vision assistance; this approach remains effective, especially for challenging edge-coupler geometries, but is difficult to integrate into the automated, high-throughput environment of a standard wafer-sort shop floor [3]. The second adapts conventional wafer probers by routing external FAUs through cut-outs or peripherals of the prober while relying on external stages for alignment, which reduces some setup burden but still preserves a substantial integration penalty [11]. The third embeds optical hardware more directly into the probe card itself, sometimes using beam-expanding optical structures to relax sensitivity to alignment, albeit at the expense of insertion loss and optical budget [12].

Recent wafer-level photonic-test literature also shows that the coupling interface itself remains a major design variable. Edge-coupling probes have been demonstrated for robust wafer-level optical testing, including automated edge-coupling measurement systems and butt-coupling probe-card concepts with polarization control [20–22]. High-throughput approaches based on dense edge coupling and micro-interposer-mounted lensed fibers address the parallelism required for 300 mm silicon-photonics wafers [23,24]. At the device-interface level, the choice between grating couplers, edge couplers and other coupling strategies determines the tolerance budget seen by the probe card [25,26], while recent intelligent optomechanical systems such as the Automated Optomechanical Intelligent Coupling System (AtOMICS) illustrate the role of automation and learning in reducing alignment burden [27].

The Eclipse Dynamic architecture sits at the most integrated end of this spectrum. According to the published feasibility study and the patented mechanical concept, the FAU is mounted inside the probe head, at the same level as the electrical probes, within a flexure assembly actuated by three piezoelectric elements [13,14]. This design reduces dependence on specialized external positioning systems and opens a path toward smaller optical/electrical pad separation, a reduced overall PIC footprint and multi-site capability. The proposed open-loop piezoelectric actuation, however, exhibits measurable hysteresis, meaning the actuator position is path-dependent and prone to alignment errors, the Y motion is not perfectly orthogonal to X, and the achieved alignment time depends strongly

on the search routine used to maximize optical power. These observations motivated a dedicated benchmarking study [15] that systematically compared seven alignment algorithms across four operating regimes, demonstrating that an integrated probe head architecture can achieve strong normalized alignment performance provided that the search algorithm is explicitly matched to the hysteresis compensation method to ensure stable convergence and prevent path-dependent positioning errors. They also indicate that future generations of integrated photonic probe cards must combine actuation with richer state awareness in order to translate algorithmic performance into reliable manufacturing outcomes.

2.2. Probe Card Monitoring and Digital-Twin Methods

Recent SHM research for probe cards offers the missing instrumentation ingredients. The AI-assisted framework introduced by Bejani et al. [16] is built on an analysis of eight months of historical data from Technoprobe field operations, which are organized into needle-related, mechanical and electrical failure modes and prioritized by frequency and repair time. The dominant production-relevant failures, namely needle contamination, programmed overtravel (POT) and actual overtravel (AOT) discrepancies, thermal misalignment between wafer and probe card, cracks in ceramic plates and loosening of probe-head screws, are then mapped onto a sensor network composed of accelerometers, microphones, temperature sensors and overtravel sensors connected through a central microcontroller and a low-power safety supervisor.

The broader SHM and predictive-maintenance literature supports this direction. A recent work on semiconductor probe-card proactive maintenance shows that field data can be converted into maintenance decisions using graph-based self-supervised learning [28]. Reviews of optimal sensor placement for SHM emphasize that sensor count, location and information content must be accurately selected to optimize signal-to-noise ratio considering space and I/O resource constraints [29,30], and acoustic-emission/deep-transfer-learning studies on bolted joints show that loosened mechanical interfaces can be monitored through vibration and acoustic signatures [31]. These results reinforce the need to treat the photonic probe card as a monitored mechanical structure rather than as a passive carrier for probes and fibers.

Each sensor type addresses a specific failure mechanism. Low-frequency displacement sensors track touchdown counts and lifetime indicators that drive predictive maintenance scheduling. Higher frequency displacement sensors capture acoustic and structural vibration changes associated with cracks in plates or with screw loosening, both of which alter the frequency response function (FRF) of the probe head. Temperature sensors detect thermal mismatches between the wafer and different regions of the probe card, helping to interpret thermal-expansion-induced misalignment and the open/short electrical failures that follow. Overtravel sensors quantify the difference between programmed and actual overtravel (POT and AOT), which governs probe compression and contact resistance. This taxonomy provides a directly transferable foundation for the photonic probe card case considered in the present paper, where the same failure modes coexist with the additional sensitivity of the optical alignment subsystem.

A complementary line of work addresses the need for the monitoring pipelines to remain robust to incomplete data. Using signals from higher- and low-frequency displacement sensors sampled at 1 kHz, a self-attention-based imputation model recovered corrupted sensor signals with materially improved fidelity over standard baselines [17]. Specifically, the model achieved an average mean absolute error (MAE) improvement of 66% compared to traditional statistical methods (such as linear interpolation and k-nearest neighbors), while training more than twenty times faster per full dataset cycle than state-of-the-art recurrent architectures (such as standard LSTM networks). In par-

allel, digital-twin-assisted and Transformer-based studies have shown that data-driven sensor-placement strategies can identify the most informative monitoring points on a probe card and classify health states such as baseline, loose screws and cracks with classification accuracy of 99.83% and crack-detection recall of 99.73% [18,19]. These results suggest that sensor placement on a photonic probe card should not be ad hoc but jointly optimized with the mechanics of the probe head and the failure modes of interest.

2.3. Gap Addressed in This Work

The technical gap is therefore not simply “how to move a FAU” or “how to monitor a probe card” independently. It is how to build a probe card that does both simultaneously for wafer-level optical test of CPO-class devices. A production-worthy platform must align the FAU with sub-micron repeatability across the relevant translational and angular degrees of freedom, coexist with dense vertical electrical probing and the associated radio-frequency or high-speed digital channels, determine in real time whether environmental vibrations or local mechanical disturbances are affecting the validity of the optical measurement, preserve monitoring continuity even in case of sensor data loss, and support lifecycle management so that drift in the probe card itself does not silently degrade yield. The EclipsePhotonic platform developed in the subsequent sections is explicitly positioned as a unified response to this combined requirement, integrating the previously described positioning engine with the aforementioned sensor-network and management framework.

3. EclipsePhotonic Platform Concept

3.1. System-Level Architecture

Figure 1 summarizes the proposed system architecture. The platform combines three tightly coupled subsystems: a conventional vertical-needle electrical probe head for wafer contact, an integrated FAU carriage derived from the Eclipse Dynamic concept that provides embedded optical alignment within the probe head, and a sensor and control layer that observes the probe card state, the FAU-to-wafer separation and the vibration environment during test. The tester drives an electrical test program, consisting of an automated sequence of instrument configurations, test vectors, and parametric measurements, through the probe needles, and executes an equivalent optical test program via an optical modulator and photoelectric converter that close the optical alignment loop with the FAU, while a piezo power supply and voltage boost stage drive the integrated piezoelectric actuators. Sensor channels for distance, vibration and temperature run in parallel to the test signal paths and are exposed to the automated test equipment (ATE) through a dedicated on-line communication interface.

The mechanical core is inherited from the foundational Eclipse Dynamic prototype [13,14]. To establish optical coupling, the embedded alignment algorithm utilizes real-time feedback on the actual position—derived as a function of the integrated sensors and the optical power meter—and drives multiple piezoelectric actuators to iteratively tune the FAU to the optimum position. This continuous opto-electronic optimization abstracts the underlying mechanical kinematics, allowing the system to achieve nanometric precision without relying on perfectly rigid, open-loop mechanics. The FAU itself is a configurable interface whose number of fibers and pitch are selected to match the layout of the PIC under test, while the electrical needle field is implemented with conventional Technoprobe vertical-needle technology. Figure 2 illustrates the internal mechanism of this foundational design. The macroscopic vertical approach (Z-axis) is handled by the prober chuck strictly to establish global electrical contact. At this stage, it is critical to distinguish between POT and AOT. While the chuck executes the POT, the inherent mechanical compliance of the assembled probe head causes the needles to experience the marginally lower AOT.

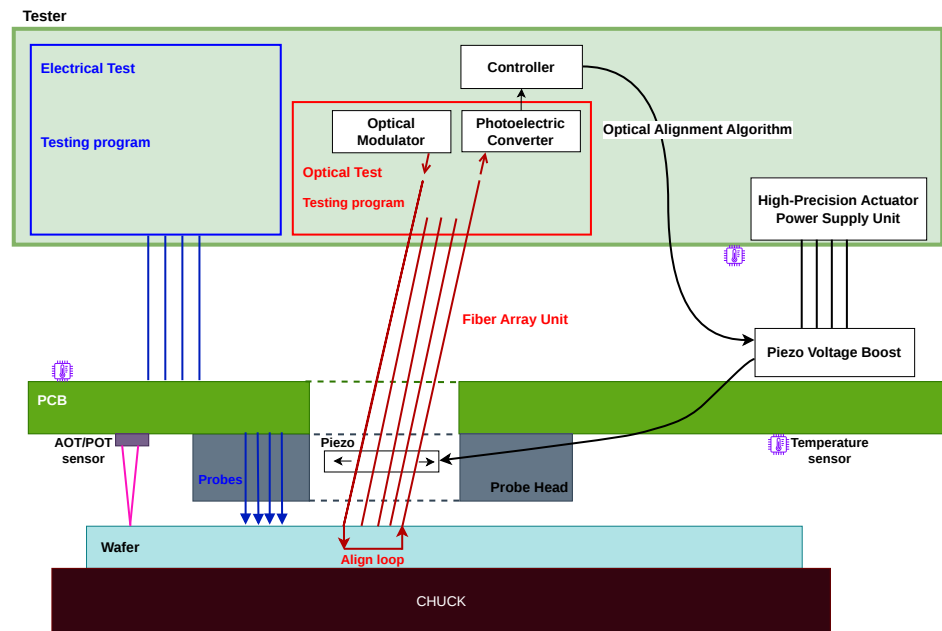


Figure 1. Conceptual system-level architecture of the proposed EclipsePhotonic platform. The probe head integrates electrical needles and an FAU actuated by piezoelectric elements; the tester executes both an electrical and an optical test program, closing the optical alignment loop through a controller and a piezo voltage-boost stage; an embedded distance/overtravel sensor and temperature sensors are shown next to the probe card PCB [15].

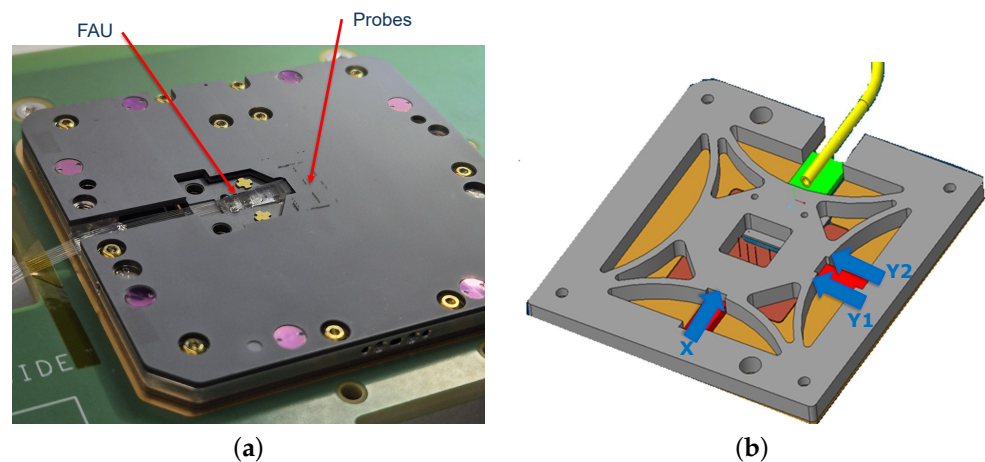


Figure 2. The foundational 3-DOF Eclipse Dynamic XY probe-head architecture, which serves as the mechanical baseline for the EclipsePhotonic platform. (a) Complete probe head assembly showing electrical probes and FAU integration. (b) Internal flexure mechanism of the legacy XY generation, showing the three planar piezoelectric actuators (X, Y1, Y2) marked in blue [15]. The new Eclipse Dynamic XYZ prototype expands this exact flexure arrangement with additional vertical actuators to achieve true six-degree-of-freedom manipulation.

While the foundational algorithmic study [15] characterized the Eclipse Dynamic XY architecture—which provided 3 degrees of freedom—the proposed architecture evolves into the Eclipse Dynamic XYZ positioning system. This advanced prototype achieves true six-degree-of-freedom (6-DOF) manipulation, independently controlling translation (X, Y, Z) and angular orientation (RX, RY, RZ) with nanometric precision. Crucially, this XYZ prototype incorporates the necessary piezoelectric drive electronics directly on the printed circuit board. By migrating the power and control electronics out of the automated test

equipment and onto the board itself, the EclipsePhotonic probe card becomes completely tester- and prober-agnostic, drastically reducing integration complexity on the shop floor.

3.2. Rationale for Six-Degree-of-Freedom Alignment

As optical I/O moves closer to the compute die in CPO devices, the tolerance stack for test alignment tightens drastically depending on the coupling interface. The previous Eclipse Dynamic XY generation was primarily designed for grating couplers, where 3-DOF alignment is often sufficient to achieve maximum optical power. However, state-of-the-art CPO devices increasingly rely on high-density edge couplers. Edge coupling imposes a significantly stricter spatial envelope: lateral offsets in the X-Y plane reduce mode overlap, vertical (Z) offsets modify focus, and angular errors (RX, RY, RZ) change incidence conditions to the point of total signal loss. The transition to the Eclipse Dynamic XYZ architecture is therefore a strict requirement for edge-coupled devices, ensuring that all spatial and angular deviations are compensated before the test is executed.

The core design principle is to keep the optical alignment function inside the probe card rather than external to it. Doing so minimizes the number of separate coordinate systems that must be registered at test time and reduces the accumulation of compliance, backlash or thermal drift across a larger mechatronic chain. It also preserves compatibility with standard probers and testers, which was already identified as a central advantage of the integrated Eclipse Dynamic approach [13] and which is a prerequisite for the high-volume CPO-class workloads addressed by the present paper.

4. Demonstrated Alignment Performance in the Production-Optimized Regime

Before presenting these results, it is important to delineate their origin precisely. The alignment metrics reported throughout this section, namely the average number of measurement steps, the normalized alignment times, the achieved coupling percentages and the convergence reliabilities of the seven search routines, are not new experimental results generated for the present paper. They are inherited directly from the dedicated algorithmic benchmarking study of the open-loop Eclipse Dynamic positioning hardware reported in [15], which characterized these routines in isolation from any sensor-augmentation layer. The contribution of the present paper is not the alignment engine itself, but the architectural integration of that engine into the sensor-augmented, six-degree-of-freedom EclipsePhotonic probe card described in Sections 3 and 5, together with the operational and management framework presented in Sections 6 and 7 that surrounds it. The remainder of this section summarizes the inherited performance baseline that motivates the selection of Fix-Grad as the reference alignment routine for the platform.

The mechanical and electrical core of the EclipsePhotonic platform inherits the alignment engine of the foundational positioning architecture, whose computational performance has been characterized in detail in a recent algorithmic study [15]. That study evaluates seven alignment routines, namely Reference Coarse Scan (Ref-Coarse), Reference Coarse+Fine Scan (Ref-Coarse+Fine), Cross Scan (Cross), Local Bayesian Optimization (Local BO), Global Bayesian Optimization (Global BO), Variable Gradient Ascent (Var-Grad) and Fixed Gradient Ascent (Fix-Grad), whose distinct search behaviors and mechanical characteristics are detailed in Section 4.1. These routines were evaluated across four operating regimes obtained by combining high-speed (HS) or low-speed (LS) actuation with active hysteresis compensation (NH) or uncompensated hysteresis (H). Because the production-optimized configuration for practical manufacturing corresponds to high-speed actuation with effective feedforward hysteresis compensation, the present paper focuses

on the HS-NH regime as the reference performance point for the alignment engine of the platform.

The emphasis on hysteresis compensation follows the established piezoelectric-actuator literature. Modified and generalized Prandtl–Ishlinskii models, which are mathematical frameworks used to predict and invert the nonlinear and path-dependent hysteresis of smart materials, along with their rate-dependent extensions, have become standard tools for feedforward compensation of piezoelectric micropositioners [32–36]. Recent asymmetric and survey treatments confirm that residual hysteresis, rate dependence and local nonlinearities remain critical limitations in high-speed precision positioning [37,38]. For an integrated photonic probe card, this literature justifies the architectural separation between the mechanical ability to move the FAU and the control-layer requirement to linearize the actuation path, yielding a proportional input-to-displacement response, as well as to precompensate or otherwise manage the piezoelectric response before optical-power optimization is executed.

4.1. Algorithm Behavior on the Coupling Landscape

Figure 3 compares the seven alignment algorithms on a representative simulated coupling landscape generated from experimental scans applying the standardized evaluation approach established in [15], which systematically tests search algorithms across different operating speeds and hysteresis conditions. The exhaustive raster scans of Ref-Coarse and Ref-Coarse+Fine sample the full $120\text{ V} \times 120\text{ V}$ actuation space on regular grids and therefore visit hundreds of points. The Cross routine collapses the search to two orthogonal one-dimensional sweeps before refining the peak. The two Bayesian variants build a Gaussian-Process surrogate of the coupling landscape: Local BO confines the search to a neighborhood identified by an initial cross-scan, while Global BO explores the entire actuation space from the outset using Latin-hypercube initialization. The two gradient routines, Var-Grad and Fix-Grad, climb the landscape using finite-difference gradient estimates: Var-Grad uses an adaptive learning rate that scales inversely with the measured power, while Fix-Grad halves a fixed step size whenever no improvement is found in any cardinal direction.

The Bayesian routines are motivated by the broader Bayesian-optimization literature, in which Gaussian-Process surrogates and acquisition functions are used to minimize the number of expensive measurements needed to locate an optimum [39]. Local trust-region Bayesian optimization addresses scalability and nonstationarity by restricting the model to promising subregions [40]. Autonomous beamline and accelerator-tuning demonstrations provide close analogues to photonic alignment, because both classes of instrument maximize a measured signal through a small number of sequential, hardware-limited adjustments [41–43]. In the present platform, this analogy explains why BO is an attractive reference method even when the final production choice favors deterministic Fix-Grad behavior.

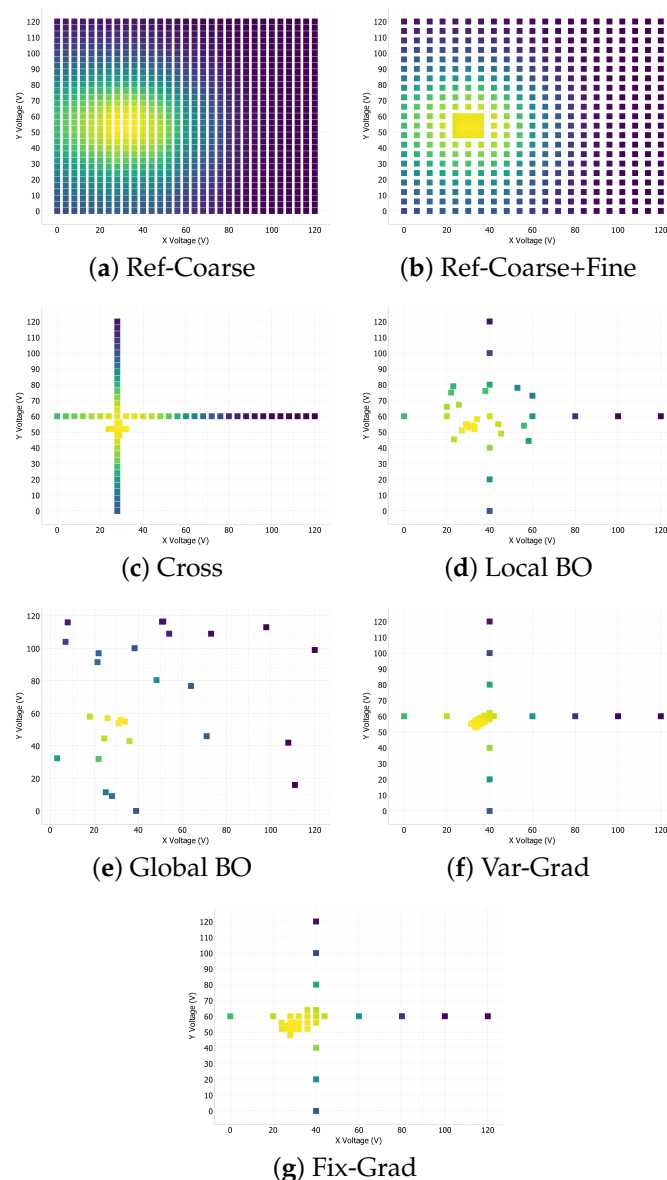


Figure 3. Comparison of the seven alignment algorithms on the same simulated mock-scan scenario derived from Eclipse Dynamic experimental data [15]. Each panel shows the search path of the algorithm overlaid as discrete colored measurement points, where the color intensity represents the measured optical power (from dark purple for low power to bright yellow for the highest power): (a,b) exhaustive raster scanning, (c) dimensional reduction, (d,e) Bayesian optimization with intelligent sampling, (f,g) gradient-based hill climbing.

4.2. HS-NH Performance and Algorithm Selection

Table 2 consolidates the simulation outcomes of [15] for the production-optimized HS-NH regime, evaluated across 72 test scenarios. This specific sample size was established to comprehensively represent the matrix of expected initial physical misalignments by combining 8 experimental coupling landscapes with 9 systematic spatial offsets per landscape. Throughout the table, alignment time is expressed in arbitrary units (a.u.), normalized so that the baseline execution time of the Local BO method in the LS-H configuration corresponds to 100.0 a.u. To strictly differentiate between performance metrics, accuracy represents the final achieved coupling power as a percentage of the absolute peak, while convergence reliability represents the success rate of the algorithm. A problem is considered solved when the algorithm reaches at least 95% of the global maximum optical power, and the reliability column reports the percentage of all evaluated trials that meet this criterion.

Table 2. Per-die alignment performance of the seven evaluated algorithms in the production-optimized HS-NH regime, summarized from the simulation study of [15] across the evaluated test scenarios. The columns report the average number of measurement steps (independent of the operating regime, reflecting only algorithmic logic), the average total alignment time including movement and settling delays (expressed in arbitrary units, a.u.), the average final coupling power as a percentage of the global maximum, and the convergence reliability defined as the percentage of trials reaching at least 95% of the global maximum power.

Algorithm	Avg. Steps	Avg. Time (a.u.)	Avg. Coupling (%)	Reliability (%)
Ref-Coarse	961.0	30.64	99.9	100.0
Ref-Coarse+Fine	539.6	18.10	100.0	100.0
Cross Scan	75.6	2.44	98.2	94.4
Local BO	31.3	1.54	98.3	94.4
Global BO	24.7	2.24	98.0	90.3
Var-Grad	26.1	1.18	98.0	90.3
Fix-Grad	34.4	1.44	99.4	95.8

The HS-NH numbers in Table 2 establish a clear performance hierarchy. The exhaustive Ref-Coarse and Ref-Coarse+Fine routines achieve perfect reliability at the cost of 30.64 a.u. and 18.10 a.u. per die, respectively, with several hundred measurement steps; they are useful as ground-truth baselines but are not viable for high-volume production. The Cross routine reduces alignment time to 2.44 a.u. but plateaus at 94.4% reliability because it is sensitive to the specific landscape shape. The two Bayesian variants offer the best sample efficiency, with Global BO converging in only 24.7 measurement steps on average; however, the Gaussian-Process update overhead inflates Global BO total time to 2.24 a.u. and reliability is limited to 90.3% in HS-NH because purely probabilistic exploration occasionally fails to localize the optimum within the iteration budget. Local BO is more reliable (94.4%) and faster (1.54 a.u.) thanks to its cross-scan initialization, and is the strongest Bayesian option in this regime.

The two gradient methods occupy the speed-versus-reliability frontier of the HS-NH operating point. Var-Grad provides the absolute fastest alignment at 1.18 a.u., but its adaptive step heuristics make it more susceptible to entrapment in local maxima, which limits its reliability to 90.3%. Fix-Grad, by contrast, combines a deterministic step-halving rule with cross-scan initialization to deliver 95.8% reliability at 1.44 a.u. per die, while also achieving the highest final optical coupling power among the non-exhaustive routines (99.4% of the global maximum). For a production environment in which manual intervention on a failed alignment is significantly more expensive than a marginal speed loss, this profile makes Fix-Grad the recommended baseline algorithm of the EclipsePhotonic alignment engine.

Figure 4 reports the data profile [44,45] obtained for the production-optimized HS-NH regime. To correctly interpret this benchmarking graph, the horizontal axis represents the normalized execution time, while the vertical axis displays the cumulative fraction of alignment cases successfully solved. Consequently, a superior algorithm produces a curve that rises steeply toward the upper-left, indicating rapid and reliable convergence. Specifically, the graph plots the fraction of the evaluated test scenarios solved as a function of total alignment time on a logarithmic scale. The data profile reveals convergence behaviors that simple averages would obscure. Var-Grad shows the steepest initial trajectory and is the fastest method on benign landscapes, but plateaus near 90% solved problems, exposing a residual fraction of cases in which it never converges within tolerance. Fix-Grad has a slightly later but steeper rise and reaches a higher and more consistent plateau at 95.8%. The Bayesian methods rise more gradually because of their Gaussian-Process overhead, with Local BO outperforming Global BO at every time budget. The reference scans are

visible as the rightmost staircases that only become competitive once orders of magnitude more time is allowed.

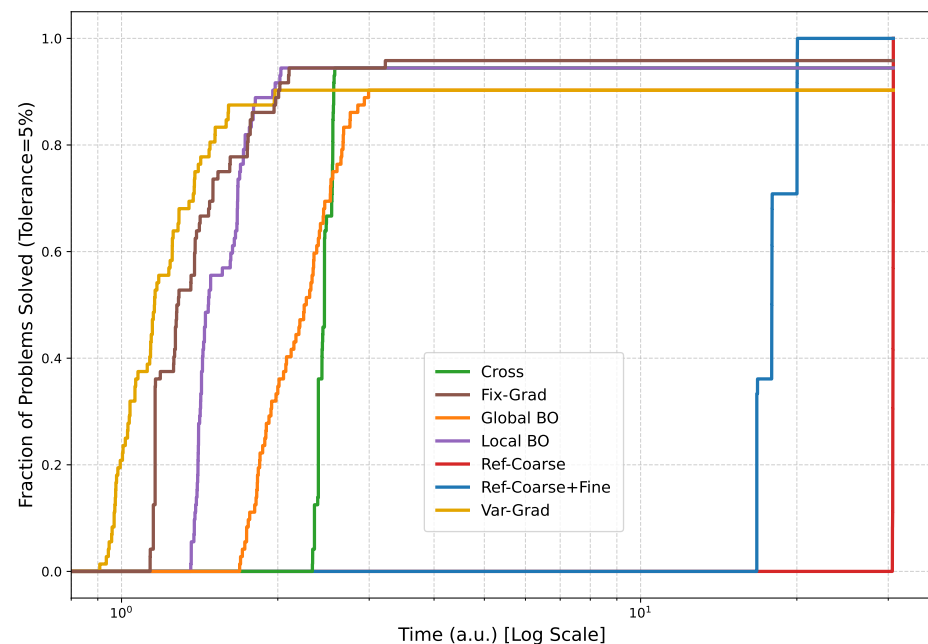


Figure 4. Data profile [44,45] of the alignment algorithms in the production-optimized HS-NH regime, showing the fraction of all simulated test cases solved (within 5% tolerance of the global coupling maximum) as a function of total alignment time on a logarithmic scale. Curves reconstructed from the published HS-NH performance of [15]. Fix-Grad combines high reliability (95.8%) with rapid convergence; Var-Grad is the absolute fastest at the price of a residual 9.7% failure rate; Bayesian methods rise more gradually because of their Gaussian-Process overhead.

The HS-NH operating regime is therefore the design point at which the alignment engine of the EclipsePhotonic platform is intended to operate in production. From a system perspective, this point is reached only when high-speed piezoelectric drive electronics are paired with effective feedforward hysteresis compensation. The recent algorithmic study [15] demonstrates that, in this regime, the open-loop architecture of the Eclipse Dynamic probe head achieves the most favorable normalized speed–reliability trade-off among the evaluated search routines, while preserving the integrated, parallel-test-friendly nature of the probe-card-centric approach. What remains, and what motivates the rest of this paper, is to surround that alignment engine with the sensing and management layer that turns it into a self-aware, production-ready platform.

The addition of sensor input to the alignment algorithm is expected to improve coupling repeatability primarily by suppressing the contribution of transient, non-representative measurements, rather than by altering the intrinsic mechanical repeatability of the FAU stage itself. In the absence of context-awareness, a vibration event coincident with the optical acquisition window is, in the raw optical power trace, indistinguishable from a genuine reduction in coupling efficiency, and is included in repeatability statistics as if it were a valid measurement. By flagging and excluding such mechanically corrupted acquisitions, or triggering a local retest as described in Section 6, the sensor-augmented alignment loop is expected to bring the measured coupling repeatability closer to the intrinsic mechanical repeatability of the open-loop actuation stage reported in [15], rather than the wider, environment-dependent spread that would otherwise be observed on a production floor with uncontrolled vibration sources. A precise quantification of this improvement, together with the associated absolute insertion-loss noise floor under realistic

test-cell conditions, is an explicit objective of the second validation stage discussed in Section 8, since it requires dedicated experiments that isolate the effect of induced vibration from that of intentional angular and lateral offsets on the assembled hardware.

5. Embedded Sensor Network and Management Framework

5.1. Failure Modes and Sensor Roles

The sensor-augmentation layer of the EclipsePhotonic platform extends the recently proposed AI-assisted EWS monitoring framework [16] to the photonic probe card case. That framework utilizes the previously detailed sensor network to directly target these dominant operational issues. The same sensor types are directly relevant to a photonic probe card, and each one acquires an additional photonic-test interpretation in the EclipsePhotonic context, as summarized in Table 3.

Table 3. Sensor functions in the EclipsePhotonic platform, mapped from the AI-assisted EWS monitoring framework of [16] to the photonic probe card context.

Sensor Type	Primary Role in EclipsePhotonic	Manufacturing Value	Required Specifications
Relative displacement sensors (AOT-POT)	Measure FAU-to-wafer separation and the difference between programmed and actual overtravel near the optical interface	Reduce collision risk, improve Z control, expose contextual data for alignment repeatability and wafer-topography compensation, and support reliable electrical contact ^a	Resolution: micrometric to nanometric precision. Range: calibrated to standard probe tip compression distances.
Low frequency displacement sensors	Detect touchdown events, wear indicators, and ambient or test-cell disturbances; measure dynamic behavior of the probe head and FAU carriage	Tag optical measurements acquired under unstable conditions, support binning and retest decisions, and feed lifecycle monitoring [16]	Bandwidth: wideband shock detection. Dynamic range: sufficient to capture macroscopic chuck impact forces without clipping.
Higher frequency displacement sensors	Observe FRF changes related to cracks in ceramic plates and loosened screws in the probe-head assembly	Enable SHM and predictive maintenance, complementing low-frequency event detection [16,19]	Bandwidth: 400–4000 Hz (structural resonances). Sensitivity: high SNR capable of resolving localised amplitude shifts.
Temperature sensors	Monitor thermal gradients between the wafer and different probe card regions	Help interpret thermally induced misalignment, transient electrical/optical contact issues, and warm-up behaviour [16]	Range: 25 °C to 250 °C. Accuracy: ± 0.5 °C to detect minute spatial thermal gradients.

^a Overtravel and distance sensing are central to the EWS monitoring framework [16]. In the EclipsePhotonic platform, they are implemented as PCB-integrated relative displacement sensors with active shielding, protecting the FAU during approach and feeding the optical alignment routine [46–48].

Low-frequency displacement sensors track touchdown counts, wear and lifetime, and they capture dynamic events on the probe card assembly that may coincide with the optical acquisition window. Higher frequency displacement sensors capture acoustic emissions specifically within the 400–4000 Hz band, a targeted frequency window that encompasses the dominant mechanical resonances characteristic of the probe card assembly. The FRF within this band varies measurably in the presence of cracks in the ceramic plates or loosened screws in the probe-head housing, both of which were demonstrated through finite-element studies and confirmed experimentally in [16,19]. Temperature sensors monitor the thermal mismatch between the wafer and different regions of the probe card; in a photonic platform, this gradient also drives differential expansion of the FAU mount, which directly affects optical alignment stability. Distance and overtravel sensors quantify the relative position between the FAU and the wafer surface and the difference

between programmed and actual overtravel; in the photonic case, they additionally protect the FAU during approach and provide contextual information about wafer topography that can be fed to the alignment engine.

5.2. Sensor Network Architecture

The sensor network architecture, illustrated in Figure 5, centers on a primary microcontroller unit (MCU) responsible for aggregating and processing data from the low-frequency, higher-frequency, and relative displacement sensors, alongside the thermal monitors. To support the buffered data acquisition and lifecycle telemetry layers, the central MCU is coupled with an integrated data storage module. A smart interface provides general-purpose communication capabilities for comprehensive monitoring, controlling, and managing of the overall probe card state. In parallel to this management layer, a dedicated ATE on-line signaling protocol translates critical internal network data to expose synchronized diagnostic flags directly to the test cell. This topology is similar to the network architecture validated for EWS applications in [16], but is here transposed to the integrated photonic probe card case.

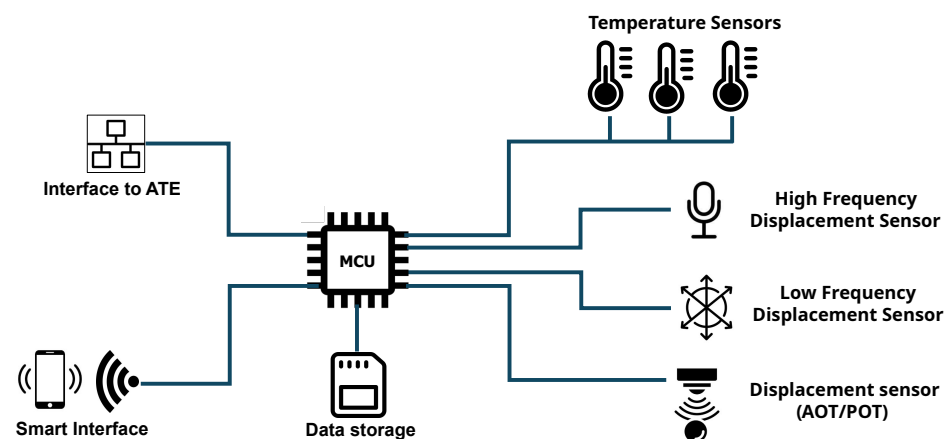


Figure 5. Block diagram of the embedded sensor network of the EclipsePhotonic platform, adapting the topology validated in the EWS monitoring framework of [16]. Low- and higher-frequency displacement, relative displacement, and temperature sensors feed a central MCU equipped with local data storage for lifecycle telemetry. A smart interface provides general communication capabilities for system monitoring, control, and management, while a dedicated ATE on-line signaling path exposes synthesized diagnostic flags to the test cell.

The AOT/POT distance channel is implemented via non-contact relative displacement sensing rather than as a mechanically intrusive contact sensor. In this configuration, the probe-side PCB carries the sensing elements and active-shield layers directly in the probe-side stack-up, while the DUT acts as the target. The measured displacement is converted into FAU-to-wafer gap or actual-overtravel information, so the same channel supports safe approach, collision prevention, and verification of the difference between POT and AOT. Active shielding is important because it drives the shield at nearly the same potential as the sensing node, reducing environmental interference from surrounding conductors and improving signal stability in precision non-contact measurement geometries [46,49]. Guarded and active-shielded layouts are also consistent with historical guard-electrode concepts and with established layered, non-contact relative displacement architectures [50–52].

This topology is well suited to a photonic probe card because the probe side can contain only passive copper electrodes and shield layers, while the capacitance-to-digital or analog front-end IC is placed on the tester side. Keeping the front-end electronics away from the DUT and chuck region prevents direct exposure to DUT temperature, simplifies

thermal design and leaves the fragile probe-side area mechanically thin. Remote capacitive sensing with driven shields and modern readout circuits provides the circuit precedent for separating the electrode from the electronics [48,53–56]. The remaining design variables are the electrode diameter, guard-ring spacing, shield-layer geometry, stand-off distance and calibration model; these are known to control slope error, nonlinearity, range and nanometer-scale resolution in capacitive displacement sensors [47,57,58].

The sensor network supports three operational layers. The first layer is real-time signaling, in which the MCU exposes synchronous flags such as “vibration above threshold”, “thermal gradient out of range” or “AOT/POT mismatch” to the ATE through the on-line signaling interface. The second layer is buffered data acquisition, in which raw low- and higher-frequency displacement, relative displacement, and temperature streams are acquired in short windows around relevant test events. Crucially, this buffered data feeds the anomaly detection module, which is explicitly trained to classify the instantaneous structural health of the probe card into three distinct operational states: a healthy Baseline, a critical Crack in the ceramic plates, or a Loose Screw within the probe-head assembly, directly building upon the classification framework established in [19]. The third layer is lifecycle telemetry, in which long-horizon aggregates—such as touchdown counts used to classify needle contamination levels, FRF baselines, and thermal-cycle histories—are persisted as a slowly evolving signature of the probe card. These three layers correspond to the primary monitoring objectives identified in the EWS framework [16] and provide the explicit diagnostic classes required for the management functions described next.

5.3. Dual Role of Vibration Monitoring

The vibration sensing subsystem performs two operational roles; both are central to the value proposition of the EclipsePhotonic platform. The first role is test-context awareness. Optical coupling can fluctuate not only because the DUT is marginal, but also because the local mechanical environment has temporarily degraded the optical coupling between the FAU and the device under test. A vibration event recorded during a power measurement can therefore explain unexpected optical loss or increased variability. Instead of treating such outliers as purely device-driven, the test system can use the vibration trace to flag the result, reclassify the confidence level or trigger a targeted retest, which is especially relevant when pass/fail margins are narrow. The second role is probe card lifecycle monitoring. The monitoring framework [16] explicitly targets cracks in plates, loose screws, contamination and other degradation modes, all of which alter the dynamic signature of the assembly. By tracking whether the dynamic signature of the card remains within a validated operational “swim lane”, the platform can identify cards whose mechanics are drifting before they create widespread test escapes or yield loss. In a photonic probe card, this is particularly valuable because a gradual change in mechanical response can silently erode optical alignment stability without producing an immediate catastrophic failure.

5.4. Data Integrity and Missing-Data Recovery

A practical monitoring layer must survive imperfect data collection. Modern time-series imputation methods based on self-attention, probabilistic diffusion and cross-dimensional attention provide the broader methodological context for reconstructing multivariate sensor streams with missing or corrupted intervals [59–61]. As previously discussed, recent work on self-attention-based imputation [17] shows that probe card sensor streams are vulnerable to missing values, and that deep-learning imputation can reliably reconstruct these corrupted signals faster and more accurately than baseline methods. For EclipsePhotonic, this implies that missing samples from vibration or auxiliary sensors need not invalidate the entire monitoring layer. A deployable pipeline can segment

sensor signals into short windows, reconstruct corrupted intervals and pass the completed streams into downstream anomaly-detection or event-tagging modules. This resilience is important because probe card monitoring should enhance production robustness, not create a new single point of failure.

5.5. Sensor Placement and Health Classification

The position of the sensors on the probe card is itself a design variable, consistent with the SHM sensor-placement literature in which observability, cost and damage sensitivity are optimized together [29,30]. The digital-twin-assisted study [18] demonstrates that model-based optimization of sensor placement on a probe card can substantially reduce the number of required sensors while maintaining the quality of the monitoring stream, and the Transformer-based approach of [19] reports a hybrid CNN–Transformer model trained on FRF data from simulated failure scenarios that achieved 99.83% classification accuracy and 99.73% crack-detection recall, with attention weights also highlighting the most informative sensor locations. For the EclipsePhotonic platform, these results provide both a method and a validated performance benchmark for selecting the placement of the displacement and temperature sensors on the photonic probe card, and they motivate sensor-placement co-optimization with the mechanical layout of the FAU flexure.

6. Proposed Wafer-Level Photonic Test Flow

The proposed operating flow for the EclipsePhotonic platform is structured to preserve compatibility with standard wafer sort while inserting optical alignment and monitoring as tightly integrated subroutines. After the wafer chuck steps to a new die or group of dies, the electrical needles and FAU are brought into their nominal probing configuration. Distance sensing acts as a protective and informative layer in this phase: it confirms safe approach, detects unexpected Z offsets, and helps normalize alignment behavior across local wafer topography and chuck flatness variations. Once the interface is within the controlled approach window, optical-power-based alignment begins. The alignment routine generalizes a previously established two-stage scheme [13], where a first stage performs a coarse cross-scan to localize the optical signal across the actuation window, and a second stage performs a local optimization around the condition of maximum optical coupling between the FAU and the wafer. In the production-optimized HS-NH regime characterized in Section 4, this second stage is realized by the Fix-Grad routine, which delivers 95.8% reliability and 99.4% of the global maximum optical coupling in approximately 1.44 a.u. per die [15]. Because the actual optimum is determined functionally rather than geometrically, absolute actuator path perfection is less important than repeatable convergence to the best optical-power state.

A primary architectural strength of this integrated approach is that electrical and optical interfaces can be established in the same mechanical frame. The same touchdown can therefore support both traditional wafer-sort checks and photonic characterization, which is particularly important in CPO-oriented devices where the production-relevant question is whether the combined opto-electronic function works under a realistic package-adjacent interface condition. Furthermore, the architecture supports multi-site electrical and optical probing; once the optical interface is embedded rather than externally staged, the platform becomes structurally compatible with parallelism. Multi-site implementation still requires careful management of optical path routing, thermal interactions, and tester resources, but the probe card-centric architecture is directionally aligned with that goal and inherits the configurable-FAU geometry described in the underlying patent [14]. To enable this multi-site capability, the platform relies on independently actuated flexure elements integrated within a single multi-site probe head assembly. By construction, devices on a

wafer already possess a regular, patterned repetition from die to die. Consequently, the solution is not a universal, layout-independent multi-site head; rather, the probe card architecture must be configured for the die topology under the assumption that probe card feasibility constraints are respected within each individual die. The specific layout effort required from chip designers is to carefully account for Design for Manufacturing (DFM) recommendations constraining the minimum physical distance between the electrical pads and the optical I/Os. This ensures that the electrical needles and the optical FAU can be simultaneously and safely housed within the localized footprint of each test site. Beyond multi-site capabilities, a distinctive contribution of the platform is that it allows test results to be interpreted together with the mechanical context of the probe card. If a vibration event occurs during optical acquisition, the test software can record not only the optical power value but also the dynamic condition under which it was obtained. This enables richer decision-making, including assigning a lower confidence score to measurements obtained during abnormal vibration, repeating only the affected optical subtest instead of retesting the entire DUT, separating likely DUT failures from likely infrastructure-induced anomalies, and correlating recurring disturbances with specific prober, handler, or cell conditions. This event-aware approach is consistent with the emphasis on real-time anomaly detection and predictive maintenance for probe cards found in recent monitoring literature [16], and it directly leverages the on-line signaling layer of the sensor network described in Section 5.

7. Design Implications for Throughput, Yield and Reliability

Throughput gains in the EclipsePhotonic platform are expected to arise from the combination of an integrated alignment engine and a self-aware management layer. With the FAU embedded in the probe head, there is less need for setup-intensive external motion hardware, fewer coordinate transformations, and a shorter mechatronic chain to settle after each movement. In the production-optimized HS-NH regime, the Fix-Grad alignment routine achieves a normalized alignment cost of 1.44 a.u. in the inherited algorithmic benchmark [15]. This value is useful for comparing search routines under the same experimental protocol, but it should not be interpreted as an absolute per-die cycle time or directly extrapolated to a full-wafer throughput figure without the ATE communication, probing, measurement, retest, and hardware-integration overheads of a specific production cell.

It is crucial to emphasize that these normalized values, expressed in arbitrary units (a.u.), represent the fundamental algorithmic efficiency of the search routines rather than absolute system performance. Absolute wall-clock alignment times are therefore not reported here, because actual test duration depends strongly on ATE communication overheads, probing sequence design, optical measurement settings, retest policy, and commercial hardware integration details that are outside the scope of the present architecture-level study. Consequently, the core objective of the EclipsePhotonic platform is not strictly to define the absolute speed limit of photonic testing, but rather to demonstrate how a specific set of embedded sensors boosts the performance and reliability of a probe card designed for this task. For instance, while previous studies utilized accelerometers and microphones primarily to monitor mechanical aging [16], in the photonic testing context, we leverage them to observe specific vibration spectra that may dynamically impair or corrupt delicate optical measurements. Furthermore, embedded relative distance sensors are utilized explicitly to enhance FAU operational safety during high-speed wafer approaches. By combining optimal algorithmic efficiency with these targeted sensor safeguards, the platform ensures that theoretical throughput gains are not negated by environmental disturbances, collisions, or unnecessary retesting on the production floor.

Consequently, this self-awareness directly supports yield protection, which depends on avoiding both false rejects and false passes driven by mechanical instability, specifically test-cell vibrations disrupting optical coupling or structural drift degrading electrical contact. A transient disturbance may make a good device appear optically weak, while a drifting probe card may produce inconsistent results that mask a true device issue. The quantitative benefit of the sensor layer can be framed directly in terms of first-pass yield: on a conventional, unaugmented probe card, a transient mechanical disturbance coincident with the optical acquisition window is recorded as a device-level insertion-loss failure, contributing to the false-reject rate in proportion to the frequency of such events on a given production floor. The embedded sensor network continuously monitors vibration and displacement channels that have already been shown to be informative for probe-card health classification; for example, the underlying frequency-response classification task reported a crack-detection recall of 99.73% [19]. This result supports the feasibility of using these sensing channels for structural-health awareness, but it does not by itself quantify real-time vibration-event detection during optical acquisition. In the proposed EclipsePhotonic flow, such event-level detection is therefore treated as a validation target: the management framework is architecturally positioned to flag potentially infrastructure-compromised measurement windows and trigger a localized retest of only the affected die, but the quantitative false-reject reduction must be measured in the dedicated validation stage. Quantifying the resulting false-reject reduction, and the associated retest time overhead relative to the total wafer-sort budget, requires production-floor disturbance statistics specific to a given fab and test-cell configuration that are not yet available for the EclipsePhotonic platform; obtaining them is an explicit goal of the third validation stage described in Section 8, in which controlled disturbances are injected to confirm detection performance and quantify the resulting yield-protection benefit under representative conditions. This distinction is likely to grow in importance as optical margins tighten in advanced CPO designs.

Preserving this metrological self-awareness requires ongoing condition tracking rather than periodic manual inspection alone. An extensive failure modes analysis of EWS probe cards has already been reported in [16]. Extending that logic to a photonic probe card is compelling because the optical function introduces additional sensitivity to micro-motion and structural drift; minor mechanical anomalies that might remain electrically benign can cause sub-micron misalignment of the FAU and severely degrade optical coupling between the probe head and the device under test. A maintenance strategy informed by embedded sensing, missing-data recovery [17], and digital-twin-supported sensor placement [19] can reduce unplanned downtime while preserving alignment repeatability over the lifetime of the probe card, providing a rational basis for replacing fixed maintenance intervals with condition-based interventions.

8. Discussion and Validation Roadmap

The EclipsePhotonic platform consolidates three propositions that are individually supported by the recent literature. First, an FAU can be integrated and actuated inside a probe head for wafer-level photonic coupling [13,14], and the alignment engine can be operated in the production-optimized HS-NH regime with the normalized speed–reliability profile reported in Section 4. Second, probe cards can host embedded sensor networks that target the most frequent EWS failure modes, with sensor types and topology validated on historical field data [16]. Third, modern machine-learning methods can both recover degraded sensor streams [17] and identify informative sensing locations and health states for reliable SHM [18,19]. The contribution of the present paper is to combine these three propositions into a cohesive hardware architecture for CPO-class wafer sort, iden-

tifying the operating regime, the recommended alignment routine, and the supporting management functions that turn the integrated probe card into a smart, sensor-augmented production asset.

Some EclipsePhotonic-specific claims, in particular the explicit six-degree-of-freedom manipulation, the nanometric positioning target across all degrees of freedom, and production-grade multi-site optical probing, should be interpreted as platform objectives to be validated rather than as fully documented results. The HS-NH alignment performance summarized in Section 4 is drawn directly from [15], in which the alignment engine of the underlying positioning hardware was characterized across the full suite of simulated test scenarios and on eight experimental coupling campaigns. These results provide a quantitative baseline against which the additional value of the sensor-augmentation layer must be measured. To clarify the scope of the current manuscript, this work is positioned as a system-architecture design blueprint rather than a report of a fully validated integrated platform. It bridges, formalizes, and integrates two engineering domains that have each been independently validated in isolation: the open-loop, high-speed piezoelectric alignment hardware [15] and the microcontroller-driven probe-card structural health monitoring network [16–19]. By establishing the explicit data routing, active-shielding topologies, and cycle-time modeling framework necessary to combine these layers, this paper provides a design blueprint intended to guide next-generation hardware implementations. A complete engineering validation of the fully assembled physical platform will proceed in four stages.

The first stage extends previous static and dynamic alignment characterizations [13,15] to all six claimed degrees of freedom, expanding beyond planar motion to rigorously evaluate independent vertical, pitch, roll, and yaw manipulation. This stage verifies translational and angular positioning resolution, repeatability, and cross-axis coupling under realistic probing loads and representative thermal and contact conditions. The second stage quantifies optical coupling robustness, measuring insertion loss, re-alignment time, and optical coupling repeatability across multiple wafers, die locations, and photonic structures, with separate experiments designed to isolate the effects of wafer topography, probe card vibrations, and intentional angular offsets, such as programmed pitch and roll deviations introduced to test the recovery limits of the alignment algorithm.

The third stage validates the sensor framework as a production aid rather than as a demonstration feature. Controlled disturbances can be injected to test whether vibration events are correctly detected, whether self-attention-based imputation [17] preserves actionable features, and whether result-tagging improves downstream binning or retest decisions. Furthermore, probe card faults such as artificially loosened screws, seeded cracks in non-critical coupons, or known contamination conditions can be used to confirm that the monitoring layer distinguishes the relevant health states. The fourth stage focuses on production-readiness, explicitly defining the commercial sensor specifications, including the necessary bandwidth, sensitivity, and footprint, required to transition from prototype components to a deployable configuration. This final stage addresses multi-site repeatability, cycle time, maintenance intervals, and the stability of the mechanical “swim lane” over the lifetime of the probe card, representing the phase where digital-twin and Transformer-based sensor-placement methodologies [18,19] become most useful in selecting a cost-effective, high-volume sensor network.

9. Conclusions

Wafer-level test for photonic-enabled processors is moving toward a regime in which optical coupling accuracy and speed, the mechanical stability required to sustain this alignment against test-cell vibrations and structural drift, and test-context awareness must be engineered together. This paper has introduced EclipsePhotonic, a smart, sensor-

augmented evolution of the underlying positioning hardware that combines an embedded FAU, six-degree-of-freedom alignment intent with nanometric target accuracy, and a monitoring layer for relative displacement (AOT-POT) sensing, vibration, acoustic, and thermal awareness. The alignment engine of the platform inherits the demonstrated algorithmic performance of Eclipse Dynamic: in the production-optimized HS-NH regime, the Fix-Grad search algorithm, selected for its stable convergence to peak optical power, reaches 95.8% reliability and 99.4% of the global maximum optical coupling at a normalized alignment cost of approximately 1.44 a.u. per die [15]. These values define the inherited algorithmic baseline for the architecture, while absolute wafer-sort cycle time remains a target for future integrated validation. Around this engine, the embedded sensor network derived from the AI-assisted EWS monitoring framework [16] provides low frequency displacement tracking for touchdowns and disturbances, higher frequency displacement monitoring for FRF evaluation for cracks and screw loosening, relative displacement (AOT-POT) sensing for safe approach and electrical-contact validation, and temperature monitoring for thermally induced misalignment, all collected through a microcontroller-based supervisor with on-line ATE signaling. Self-attention-based imputation [17] preserves monitoring continuity when data are incomplete, while digital-twin and Transformer-based sensor-placement methods [18,19] provide a route to efficient and cost-effective SHM deployment.

The immediate next step is the physical integration of the specified commercial sensors into a complete prototype, followed by comprehensive validation of the platform under production-like conditions. This validation will particularly focus on multi-site operation, long-term lifecycle stability, and the integration of context-aware result interpretation into downstream binning and retest decisions. If these validations are successful, this sensor-augmented architecture can become a practical enabler for high-volume wafer sort of the next generation of CPO-based processor technologies.

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