electronics

MDPI

Article

Analytical Design Solution for Optimal Matching of Hybrid Continuous Mode Power Amplifiers Suitable for a High-Efficiency Envelope Tracking Operation

Tao Cao [1,*], Youjiang Liu [1], Wenhua Chen [2], Chun Yang [1] and Jie Zhou [1]

[1] Institute of Electronic Engineering, China Academy of Engineering Physics, Mianyang 621900, China; liuyj04@163.com (Y.L.); ychun507@163.com (C.Y.); 13198663594@163.com (J.Z.)
[2] Department of Electronic Engineering, Tsinghua University, Beijing 100084, China; chenwh@tsinghua.edu.cn
* Correspondence: caotaog@gmail.com; Tel.: +86-0816-248-9152

Received: 27 April 2019; Accepted: 29 May 2019; Published: 1 June 2019

Abstract: An analytical method to design a power amplifier (PA) with an optimized power added efficiency (PAE) trajectory for envelope tracking (ET) architecture is proposed. To obtain feasible matching solutions for high-efficiency performance of the PA in the dynamic supply operation, hybrid continuous modes (HCM) architecture is introduced. The design space for load impedances of the HCM PAs with nonlinear capacitance is deduced mathematically using the device's embedding transfer network, without the necessity of using load-pull. The proposed design strategy is verified with the implementation of a GaN PA operating over the frequency range of 1.9 GHz to 2.2 GHz with PAE between 67.8% and 72.4% in the 6.7 dB back-off power region of the ET mode. The ET experimental system was set up to evaluate the application of the PA circuit. Measurement results show that the ET PA at 2.1 GHz reaches the efficiency of 61%, 54%, 44% and an error vector magnitude (EVM) of 0.32%, 0.60%, 0.67% at an average output power of 34.4 dBm, 34.2 dBm, 34.1 dBm for 6.7 dB peak-to-average power ratios (PAPR) signals with 5 MHz, 10 MHz, and 20 MHz bandwidths, respectively. Additionally, tested by a 20 MHz bandwidth 16 quadrature amplitude modulation (QAM) signal, 41.8% to 49.2% efficiency of ET PA is achieved at an average output power of 33.5 dBm to 35.1 dBm from 1.9 GHz to 2.2 GHz.

Keywords: envelope tracking (ET); power amplifier (PA); continuous modes; digital pre-distortion (DPD); high efficiency

1. Introduction

The current wireless communication schemes employ spectrally efficient complex modulation techniques to address the high data throughput demand. The dynamic wideband envelope and high peak-to-average power ratios (PAPRs) of 4G/5G waveforms challenge the RF power amplifier (PA) linearity–efficiency trade-off. Therefore, several architectures to improve the efficiency of RF PA have been investigated, e.g., Doherty, linear amplification with nonlinear components (LINC), envelope elimination and restoration (EER), and envelope tracking (ET) [1–4]. Unfortunately, architectures such as Doherty and LINC have bandwidth restrictions inherently. As for EER, the linearity of the signal is strongly dependent on the supply modulator and dependent on time-alignment between the RF phase signal and the amplitude envelope signal at the output of the PA [5]. However, these issues can be alleviated in envelope tracking (ET) architecture, which utilizes an envelope amplifier (EA) to instantly adjust the PA power supply voltage in synchronism with the envelope of the RF signal to ensure PA is always working at peak efficiencies for different output power levels. Since the EA is independent of the carrier frequency, the ET architecture has demonstrated considerable flexibility in multimode and multiband (MMMB) application scenarios. Moreover, the amplitude information is contained in the RF input under ET mode, and consequently,

the envelope supply waveform can be de-troughed to prevent gain collapse and reduce the bandwidth of the envelope waveform [6], which is an advantage over EER.

The overall efficiency of the ET architecture is given by the product of the PA efficiency and EA efficiency. The state-of-the-art wideband EA circuits in the literature demonstrate average efficiency of 70% to 85%, depending on the signal bandwidth and the load impedance [7–11]. Therefore, to achieve more than 50% overall efficiency by considering the statistical probability distribution function (PDF) of the modulated signal, the power added efficiency (PAE) of the RF PA at the power back-off region should necessarily surpass 70%. This is a challenging task, since the change in drain-to-source capacitance (C_{ds}) in the dynamic supply operation would result in a shift of the optimal load impedances to achieve high efficiency mode. Different modes, such as class-AB/B, class-J, and class-F Pas, have been investigated to overcome this limitation, whereas the art of ET's RF PA design is still immature as the RF PA's PAE at the power back-off region, i.e., the low drain supply voltage condition (corresponding to the average drain voltage of ET mode), is seldom above 70% at S-band [12–15].

This paper investigates, for the first time, the feasibility of utilizing hybrid continuous modes (HCM) PAs, which combine all the continuous modes between continuous Class-B/J and continuous Class-F [16], to optimize PAE trajectory for ET architecture. The design space for load impedances of the HCM PAs with nonlinear C_{ds} is deduced mathematically using the embedding transfer network. Using the optimal impedance solutions at the package plane, a GaN high electron mobility transistor (HEMT)-based PA is designed and the simulated fundamental impedances in load–pull are in good conformity with the predicted ones based on the proposed method. The ET experimental system was set up to evaluate the application of the PA circuit. Measurement results show that the proposed ET PA exhibits competitive overall efficiency and linearity.

2. Feasible Design Space for ET Operation

2.1. Nonlinear Capacitance and Parasitic Model

The variation of C_{ds} with the drain voltage (v_{ds}) is the main reason why conventional PA cannot be fully optimized over the full range of DC drain supplies (e.g., 3.5–30 V) under ET operation. It is therefore necessary to obtain a nonlinear capacitance model and embedding transfer network. The nonlinear C_{ds} profile given by Equation (1) and the parasitic model extracted in [17] are used in this work, as shown in Figure 1. This network offers an approximated large-signal model for the Cree commercial GaN HEMT device CGH40010F (Cree Inc., Durham, NC, USA).

$$C_{ds}(v_{\mathrm{ds}}) = 0.95 + 1192.4 \times [1 + \tanh(-0.0594714 \times v_{\mathrm{ds}} - 2.94696)]\ [\mathrm{pF}]. \quad (1)$$

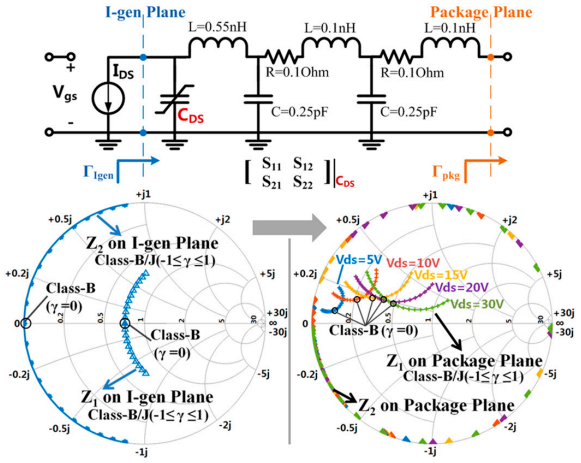


Figure 1. Nonlinear embedding model and continuous class-B/J power amplifier (PA) loads.

For simplicity, it is feasible to use average drain voltage V_{ds} to calculate C_{ds}, and then S-parameters ($\mathbf{S}^{(\mathrm{P})}$) of the embedding transfer network at different supply voltage can be computed conveniently utilizing the ABCD parameter matrix, as shown in Equation (2). Subsequently, the optimal impedances Z_{Igen} at the current generation plane can transform to Z_{pkg} at the package plane.

$$\mathbf{S}^{(\mathrm{P})} = \begin{bmatrix} \mathrm{S}_{11}^{(\mathrm{P})} & \mathrm{S}_{12}^{(\mathrm{P})} \\ \mathrm{S}_{21}^{(\mathrm{P})} & \mathrm{S}_{22}^{(\mathrm{P})} \end{bmatrix} = \begin{bmatrix} \frac{A+B/Z_0-CZ_0-D}{A+B/Z_0+CZ_0+D} & \frac{2(AD-BC)}{A+B/Z_0+CZ_0+D} \\ \frac{2}{A+B/Z_0+CZ_0+D} & \frac{-A+B/Z_0-CZ_0+D}{A+B/Z_0+CZ_0+D} \end{bmatrix} \tag{2}$$

Under different drain supply conditions, the multiple fundamental and harmonic impedance solutions of continuous class-B/J PA at both the current generation plane and package plane are calculated and shown in Figure 1. Evidently, the trajectory of the required impedances varies with drain supply voltage, which means that it would be inappropriate to select a fixed Z_{Igen} at different supply voltages. Another observation is that there is a possibility of achieving a fixed Z_{pkg} when Z_{Igen} at different supply voltages are appropriately selected, which is beneficial to design matching circuits for ET's RF PA.

2.2. Dynamic Envelope Supply Voltage

The PAE of the PA should be optimized at the drain bias corresponding to the maximum PDF of the supply envelope signal to achieve the maximum average efficiency under ET operation. In this work, a set of 16 QAM signals with 6.7 dB PAPRs are used to generate the dynamic envelope supply voltage signals. To avoid gain collapse at low drain voltages for the PA, the envelope signals are de-troughed using an exponential function proposed in [18].

The waveform of the de-troughed envelope signal and correspondent envelope amplitude PDF is illustrated in Figure 2. The de-troughed envelope voltage varies from 3.5 V to 30 V, and there is the highest probability that envelope amplitude voltage is close to 15 V. Considering the value range of nonlinear C_{ds}, it is appropriate that the drain bias of 15 V, 20 V, and 30 V are selected when the optimal impedance of the PA is targeted.

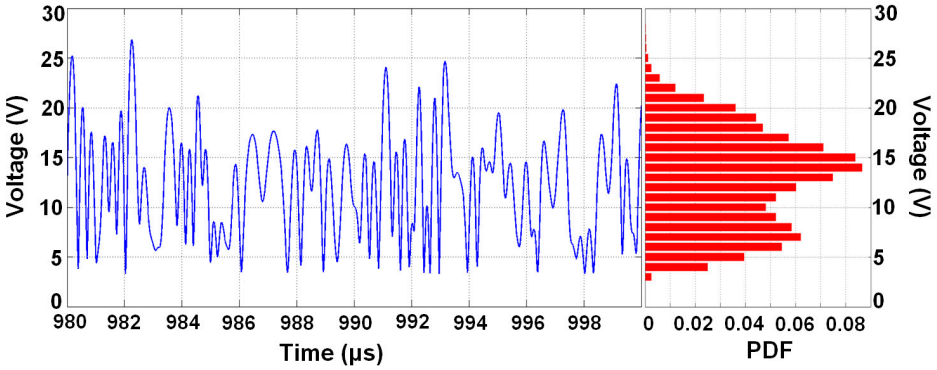


Figure 2. The waveform of the de-troughed envelope signal and correspondent envelope amplitude probability distribution function (PDF).

2.3. HCM PAs Design Space for PAE Trajectory Optimization

The HCM PAs illustrated in Equation (3) combine continuous Class-B/J ($\alpha = 1$, $\beta = 0$) and continuous Class-F ($\alpha = 2/\sqrt{3}$, $\beta = 1/3\sqrt{3}$), and the different values of α and β correspond to different continuous modes [16].

$$v_{ds}(t) = (1 - \alpha\cos(\omega t) + \beta\cos(3\omega t)) \times (1 - \gamma\sin(\omega t)) \qquad -1 \le \gamma \le 1 \tag{3}$$

It is shown in [19] that for obtaining high efficiency in the Class-J and Class-F case, the nonlinear device output capacitance can reduce the sensitivity to the second and third harmonic impedance terminations. So it is reasonable that the design of this work focuses more on the fundamental match.

HCM PAs obviously expand design space for realizing high-efficiency performance and can maintain the output power and efficiency above classical Class-B. Figure 3 shows the multiple fundamental impedance solutions of HCM PAs at the package plane. There exists a common area of impedance solutions when the drain supply voltage is above 15 V, which gives more design freedom for realizing ET PA. To explain the design methodology of this work in detail, a mathematical analysis process is presented as follows.

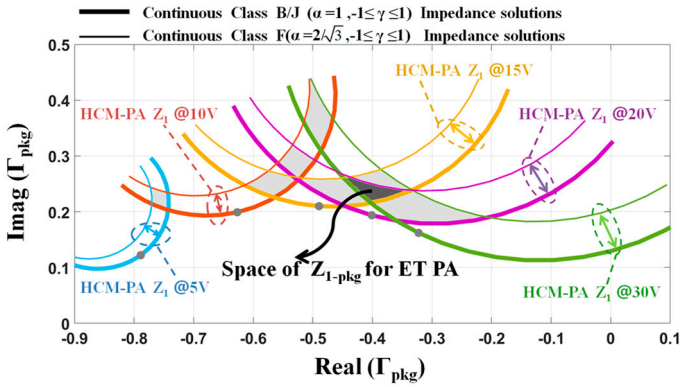


Figure 3. Fundamental impedance solutions of hybrid continuous modes power amplifiers (hybrid continuous modes (HCM) PAs) at the package plane.

Drain supply voltages are set to 15 V, 20 V and 30 V, respectively, as mentioned above, then $\mathbf{S}^{(\mathrm{P})}$ can be extracted from the embedding transfer network and be described as

$$\mathbf{S}^{(P_i)} = \begin{bmatrix} \mathrm{S}_{11}^{(P_i)} & \mathrm{S}_{12}^{(P_i)} \\ \mathrm{S}_{21}^{(P_i)} & \mathrm{S}_{22}^{(P_i)} \end{bmatrix} \qquad i \in [1,2,3]. \tag{4}$$

The fundamental impedance at the current generation plane with different supply voltages is represented by

$$Z_{1\_Igen}(\alpha_i, \gamma_i) = R_{opt}(\alpha_i + j\gamma_i) \qquad i \in [1,2,3], \tag{5}$$

where $R_{opt} = 2(\mathrm{V}_{DC} - \mathrm{V}_{Knee})/\mathrm{I}_{Max}$, and $R_{opt} = 36\,\Omega$ is chosen for CGH40010F in this work. Then reflectance at the current generation plane and package plane can be described as

$$\Gamma_{1\_Igen}(\alpha_i, \gamma_i) = \frac{Z_{1\_Igen}(\alpha_i, \gamma_i) - \mathrm{Z}_0}{Z_{1\_Igen}(\alpha_i, \gamma_i) + \mathrm{Z}_0}, \tag{6}$$

$$\Gamma_{1\_pkg}^{(P_i)} = \frac{\Gamma_{1\_Igen}(\alpha_i, \gamma_i) - \mathrm{S}_{11}^{(P_i)}}{\mathrm{S}_{21}^{(P_i)}\mathrm{S}_{12}^{(P_i)} - \mathrm{S}_{11}^{(P_i)}\mathrm{S}_{22}^{(P_i)} + \mathrm{S}_{22}^{(P_i)}\Gamma_{1\_Igen}(\alpha_i, \gamma_i)}. \tag{7}$$

To evaluate the distance between impedance solutions at the package plane under different drain supply conditions, parameter $\boldsymbol{L}$ is defined as

$$\boldsymbol{L} = \left|\Gamma_{1_{pkg}}^{(P_1)} - \Gamma_{1_{pkg}}^{(P_2)}\right| + \left|\Gamma_{1_{pkg}}^{(P_1)} - \Gamma_{1_{pkg}}^{(P_3)}\right| + \left|\Gamma_{1\_pkg}^{(P_2)} - \Gamma_{1\_pkg}^{(P_3)}\right|. \tag{8}$$

The minimum of $\boldsymbol{L}$ can be found for different modes of PA. For HCM PAs the problem can be expressed as

$$\begin{array}{ll} min & \boldsymbol{L}(\alpha_1, \alpha_2, \alpha_3, \gamma_1, \gamma_2, \gamma_3) \\ \text{s.t.} & 1 \le \alpha_1 \le 2/\sqrt{3} \\ & -1 \le \gamma_1 \le 1 \qquad i \in [1,2,3] \end{array} \tag{9}$$

Table 1 summaries the calculated results of PA design parameters utilizing numeric analysis. Obviously, HCM PAs can provide design space for achieving a fixed Z_{1_pkg} to realize impedance matching optimization at different supply voltages. Theoretically, there is a large number of solutions for Equation (9), and the result in Table 1 is one suitable for practical realization. The normalized drain voltage and current waveforms of HCM PAs presented in Table 1 have little overlap, as shown in Figure 4, which indicates that the proposed solution has very low power dissipation over a wide range of drain supply.

Table 1. Calculated results of power amplifier (PA) design parameters.

PA Mode	Design Parameter				
	V_{ds}	Z_{1_Igen}	Z_{1_pkg}	Ideal η	L_{min}
Class-B	15 V	36	15.8 + 9.3j	78.5%	0.35
Class-B	20 V	36	20.0 + 9.7j	78.5%	0.35
Class-B	30 V	36	24.5 + 9.1j	78.5%	0.35
Class-B/J	15 V	36 − 8.2j	19.7 + 10.7j	78.5%	0.04
Class-B/J	20 V	36 + 0.7j	19.6 + 9.7j	78.5%	0.04
Class-B/J	30 V	36 + 8.3j	19.7 + 10.7j	78.5%	0.04
Hybrid continuous modes (HCM)	15 V	41.6 − 4.9j	16.9 + 12.3j	89.9%	0
HCM	20 V	41.2 + 6.5j	16.9 + 12.3j	89.5%	0
HCM	30 V	36.6 + 14.4j	16.9 + 12.3j	79.7%	0

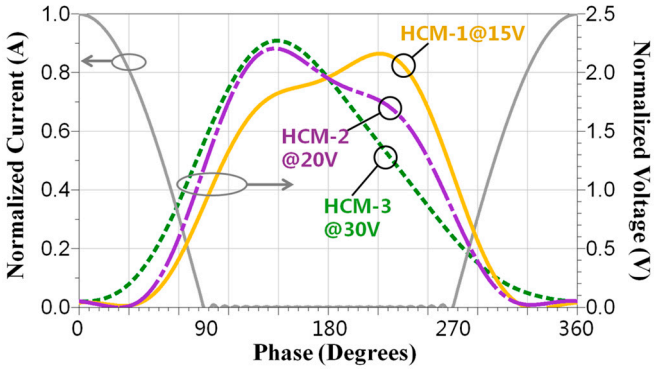


Figure 4. Normalized drain voltage and current waveforms of HCM PAs.

2.4. PA Implementation and Test

To verify optimum fundamental load impedance proposed above, the load–pull simulation was carried out, and the PA circuit was fabricated. In the simulation, the optimum fundamental load impedance is determined by analyzing output power and PAE contours at different drain supply. Figure 5 shows that there is a feasible solution space to provide high PAE (79.5%) and proper output power at both 15 V and 30 V drain bias, which is of benefit to ET operation.

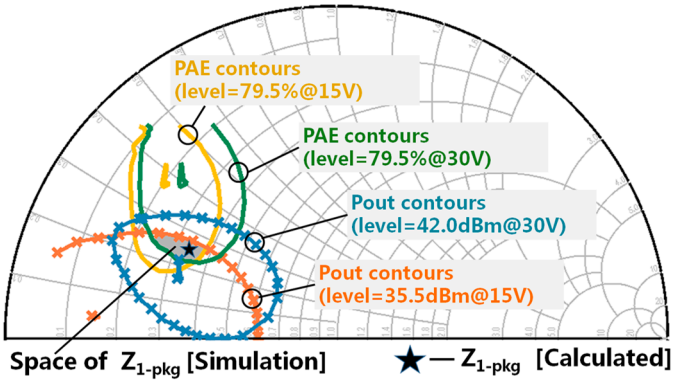
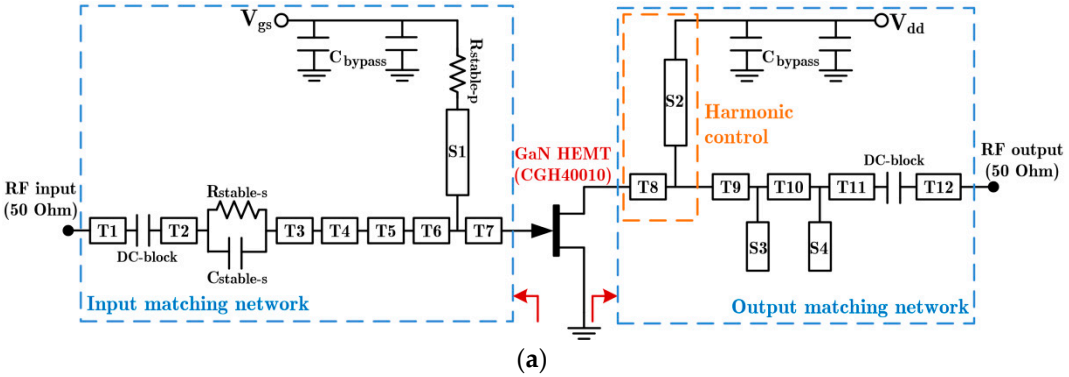


Figure 5. Simulated fundamental load–pull contours of the output power and power added efficiency (PAE) under different drain biases.

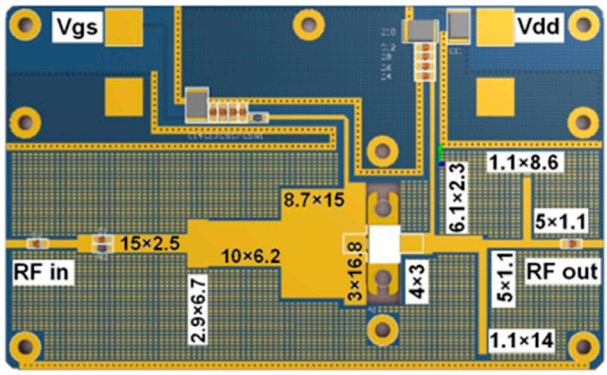
The calculated Z_{1_pkg} in Section 2.3 is also presented in Figure 5, as a comparison with the simulated results, which proves the validity of the proposed design strategy in this work. Additionally, the harmonic load impedance in this work is chosen to the edge of the Smith chart with the constraints of high efficiency and high power regions, and optimum fundamental source impedance is picked out with resorting to source pull simulation.

The input and output matching network schematic of the proposed PA circuit is shown in Figure 6a. The input fundamental matching network, considering the stability by adding a serial resistor-capacitor and parallel resistor, is matched to optimum fundamental source impedance. For the purpose of designing a broadband matching network conveniently, conventional multiple sections of transmission line topology are used in the input matching circuit. In addition, the optimum load impedance Z_{1_pkg} at fundamental frequency can be matched by using the output matching network. To optimize efficiency and output power of the proposed PA, the second harmonic control circuit, which is constituted of the quarter wave transmission line S2 and matching transmission line T8, is adopted to restrict the second harmonic impedance roll-off to the edge of the Smith chart. The matching networks are implemented on substrate RO4350B from Rogers Inc. (Chandler, AZ, USA), with a dielectric constant of 3.66 and thickness of 0.508 mm. The matching network layout of the proposed PA circuit is illustrated in Figure 6b.



(**a**)

Figure 6. *Cont.*



(**b**)

Figure 6. (**a**) Input and output matching network schematic of the proposed PA circuit; (**b**) Matching network layout of the proposed PA circuit.

The measured gain and PAE at various supply voltages as a function of output power together with the statistical PDF of the modulated signal are shown in Figure 7. The blue dots on the gain and PAE curves represent the gain trajectory and PAE trajectory of the ET operation. The maximum drain supply is set to 27.5 V, and the corresponding output power is about 42 dBm. The minimum drain supply is set to 5 V, and the corresponding peak output power is about 24 dBm. Note that the peak PAE exceeds 70% when drain supply is set from 12.5 V to 27.5 V. That means the proposed PA provides high PAE over a wide range of output powers. This behavior ensures high overall efficiency for the ET architecture. The performances of the demonstrated PA are listed in Table 2, in comparison with the state-of-the-art ET PAs in the literature.

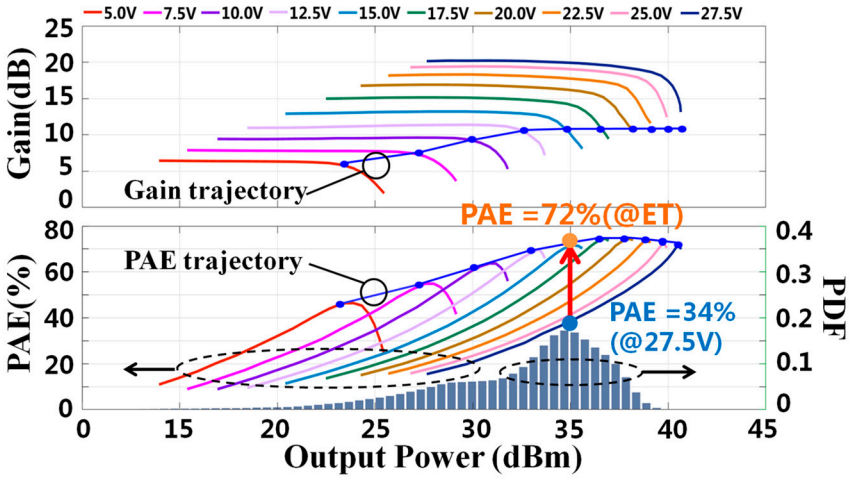


Figure 7. Measured results of the fabricated PA at various drain biases (from 5 V to 27.5 V with 2.5 V step).

Table 2. Summary and comparison of the RF PA performances (under low supply voltage condition) used in envelope tracking (ET) architecture.

Ref.	Freq. (GHz)	Back Off (dB)	Pout (dBm) @ Low Supply	Power Added Efficiency (PAE) (%) @ Low Supply	Gain (dB) @ Low Supply
[12]	2.68	7.0	34.5	50.1	10.2
[13]	1.85	7.5	22.5	46.0	9.5
[14]	3.6	6.5	32.5	68.5	12.3
[15]	1.8–2.7	8.0	35.0–36.3	59.0–65.0	8.0–11.0
This work	1.9–2.2	6.7	35.1–36.0	67.8–72.4	10.5–12.1

3. Envelope Tracking Transmitter Experimental System

3.1. High Efficiency and Wideband Hybrid Envelope Amplifier

To evaluate the application of the PA circuit, the overall ET transmitter experimental system was set up for testing. Since the overall efficiency of the ET system is roughly the product of efficiencies of the EA circuit and the RF PA circuit, a high efficiency and wideband EA circuit is another key part of the ET transmitter. The designed EA circuit in this work has a hybrid structure, which is composed of a linear stage, a sensing stage, and a buck switcher stage [20,21], as shown in Figure 8a. The reason for using the hybrid architecture relies on the characteristics of the input envelope signal [22].

The designed EA is tested with a 7.5 Ω resistive load for efficiency and accuracy verification. A group of 6.7 dB PAPR 16 QAM signals with 20 MHz, 40 MHz, and 60 MHz modulation bandwidths are employed to generate the envelope signals. The efficiency of the EA modulator is measured and shown in Figure 8b. Using 40 MHz 6.7 dB PAPR signal, it achieves an efficiency of 82% at the average output power of 18.3 W and over 70% efficiency when the output power is larger than 5 W. In addition, the small signal 3 dB bandwidth of the EA circuit is 209 MHz, which implies that it can support wide bandwidth envelope inputs.

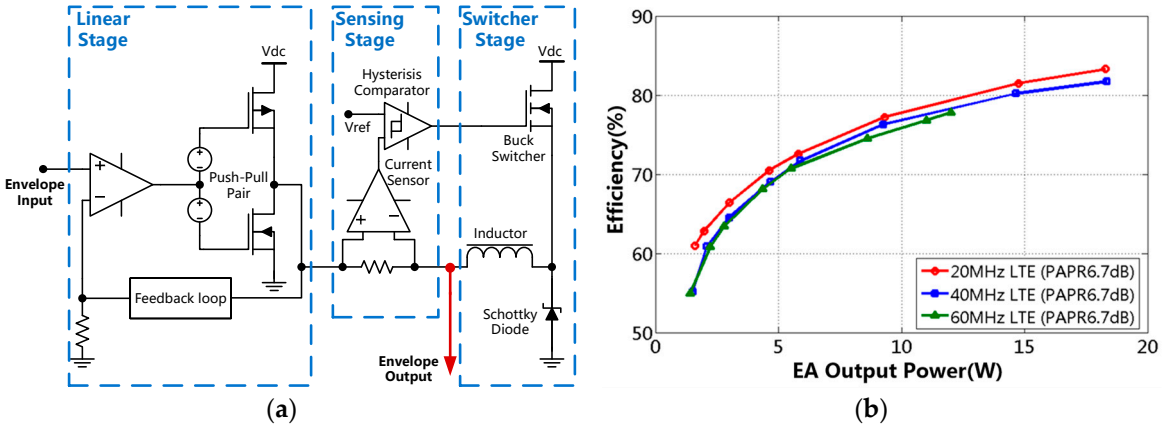


Figure 8. (**a**) Simplified hybrid envelope amplifier (EA) block diagram; (**b**) EA efficiency versus output power of the envelope signals.

3.2. Measurement Setup

Figure 9 presents the ET experimental system diagram. The testing signals are 5 MHz, 10 MHz, and 20 MHz bandwidths 16 QAM long term evolution (LTE) signals with 6.7 dB PAPR at 2.1 GHz. The baseband modulated signals and envelope signals were generated and pre-processed in MATLAB in PC, and they were streamed to the R&S SMJ100A (R&S Inc., Munich, Bayern, Germany) and Tektronix AWG7122C (Tektronix Inc., Beaverton, OR, USA), respectively.

The ET system includes an RF signal path and an envelope path. In the RF path, the up-converted RF signals from VSG are amplified by the driver, and then the output of the driver is provided to the input of the PA. The PA output comes into the spectrum analyzer R&S FSW50 (R&S Inc., Munich, Bayern, Germany), which can capture and record the baseband data of the transmitter system. In the envelope path, the wideband and high-efficiency EA amplifies the generated envelop signals from the AWG, and modulates the drain supply of the PA. To minimize the distortion caused by the time misalignment between the envelope path and the RF path, synchronization needs to be performed. The EA output envelope and the down-converted RF signal are monitored by a high speed oscilloscope Tektronix MSO5104B (Tektronix Inc., Beaverton, OR, USA). In the digital signal processing, an envelope-enhanced memory polynomial DPD model [7] is extracted by using the time-aligned input and output data of the ET system. Finally, the pre-distorted input is downloaded again to rectify the nonlinearity of the ET transmitter.

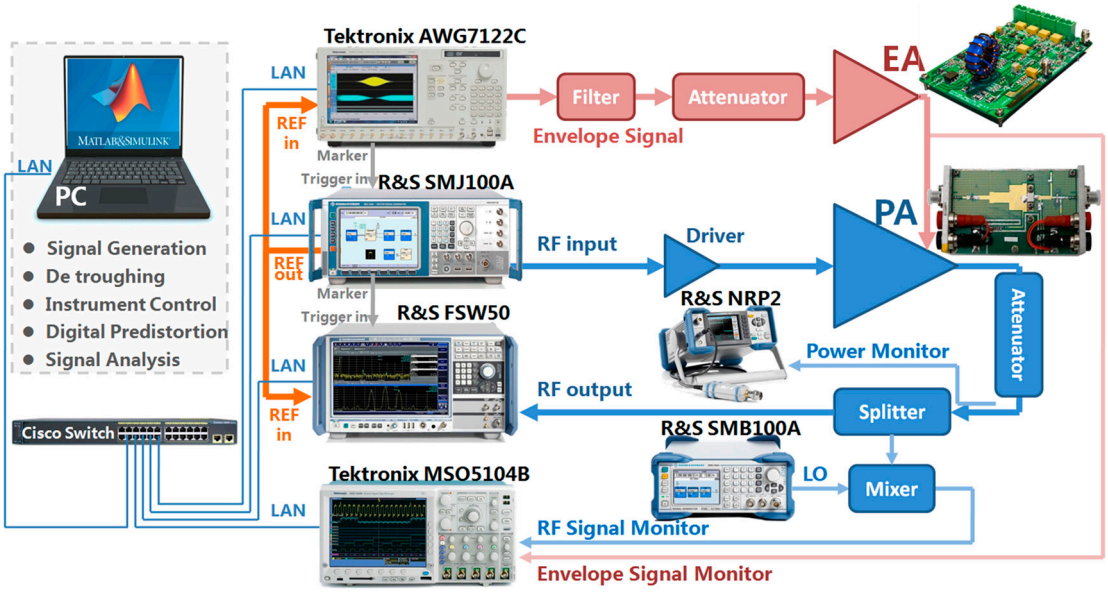


Figure 9. Measurement setup of the envelope tracking (ET) experimental system diagram.

4. Measurement Results

Table 3 summaries the measurement results which demonstrate the ET system performance. The ET transmitter obtains the measured efficiency of 60.8%, 53.7%, 44.1% and error vector magnitude (EVM) of 0.32%, 0.60%, 0.67% at an average output power of 34.4 dBm, 34.2 dBm, 34.1 dBm for 6.7 dB PAPR 16 QAM LTE signals with 5 MHz, 10 MHz, and 20 MHz bandwidths, respectively. Figure 10 shows the representative measured waveforms (20 MHz bandwidth (BW) LTE at 2.1 GHz) for RF output, drain voltage, and switching state in the ET experimental system. The drain supply voltage closely tracks the RF PA output envelope, which indicates that the proposed PA is working at high-efficiency ET mode.

The digital pre-distortion (DPD) technique can compensate the nonlinear distortion well enough to ensure high signal quality of the transmitter. Measured ET transmitter output spectra (20 MHz BW LTE at 2.1 GHz) before and after DPD are presented in Figure 11. It is apparent that the output spectrum shows less spectral re-growth and a 20 dB reduction in adjacent channel power ratio (ACPR) can be achieved after using the DPD technique.

Table 3. Summary of measurement results of the ET system performance.

Bandwidth (BW) (MHz)	Digital Pre-Distortion (DPD)	Pout (dBm)	Gain (dB)	Eff. (%)	ACLR1 (dBc)	Error Vector Magnitude (EVM) (%)
5	W/O	34.4	11.0	61.3	−26.7	7.50
5	With	34.4	11.0	60.8	−49.7	0.32
10	W/O	34.6	11.1	56.7	−26.8	8.10
10	With	34.2	10.7	53.7	−46.3	0.60
20	W/O	34.3	11.3	46.4	−26.4	8.90
20	With	34.1	11.1	44.1	−46.0	0.67

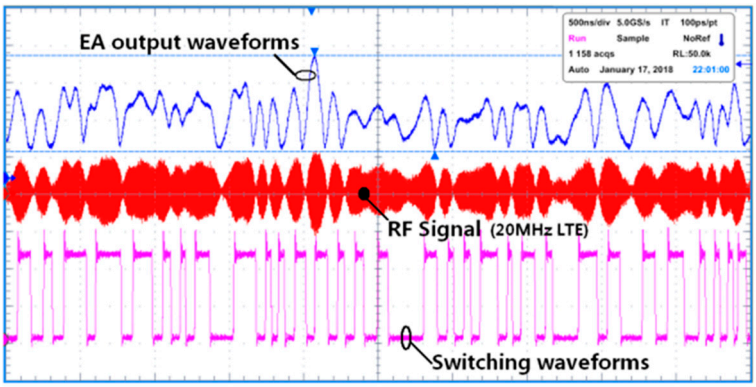


Figure 10. Representative waveforms of the ET experimental system.

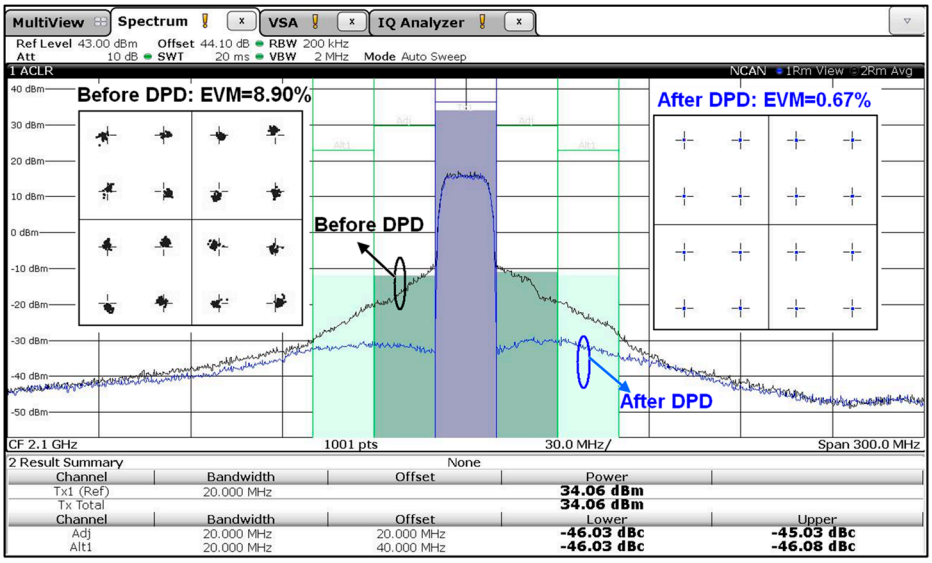


Figure 11. Measured ET PA output spectra before and after digital pre-distortion (DPD).

In addition, without DPD, ET PA shows significant AM-AM and AM-PM distortion with memory effects. Figure 12 shows the detailed AM-AM and AM-PM characteristics of the ET PA, before and after DPD. Obviously, the linearity of the ET PA in this work can be improved with the DPD technique.

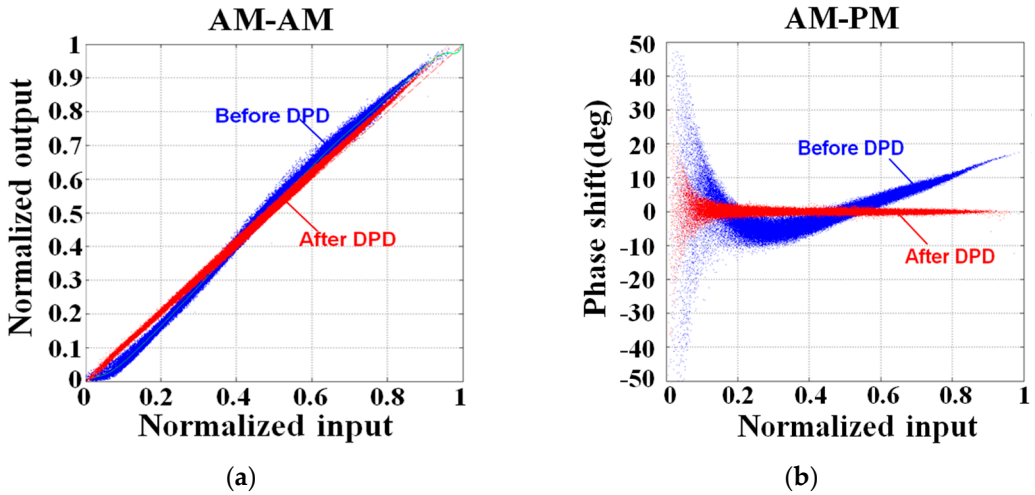


Figure 12. (**a**) AM-AM characteristics of ET PA before and after DPD; (**b**) AM-PM characteristics of ET PA before and after DPD.

ET PA can support multi-band operation since the EA circuit is independent of the carrier frequency. To show the broadband performances of ET PA, experiments were also performed at different frequencies. Tested by 20 MHz BW, 6.7 dB PAPR 16 QAM signal, 41.8% to 49.2% overall efficiency of ET PA is achieved at an average output power of 33.5 dBm to 35.1 dBm from 1.9 GHz to 2.2 GHz, as shown in Figure 13. Evidently, the proposed PA is quite suitable for a high-efficiency ET mode, and it has great potential for upgrading the broadband characteristics in a dynamic supply operation.

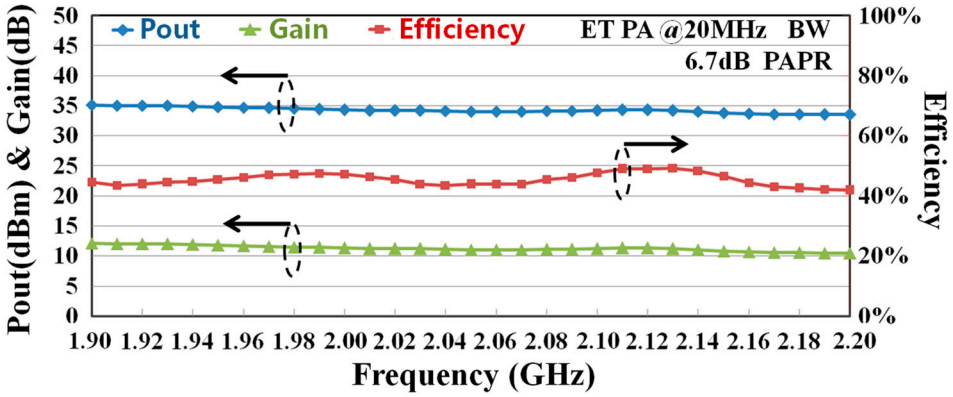


Figure 13. Measured output power, gain, and efficiency of ET PA from 1.9 GHz to 2.2 GHz with 20 MHz BW, 6.7 dB peak-to-average power ratios (PAPR) signals.

5. Conclusions

The feasibility of utilizing HCM PAs to optimize PAE trajectory for ET architecture is investigated for the first time. The design space for load impedances of the HCM PAs with nonlinear capacitance is deduced mathematically using the device's embedding transfer network. The proposed design methodology has been verified by extensive experiments. Measurement results show that ET architecture with the proposed PA circuit exhibits competitive overall efficiency and linearity for high PAPR modulation signals in a wide RF frequency range.

Author Contributions: T.C. conceived the methodology, performed the experiments, and wrote the initial draft. Y.L. and W.C. provided significant comments and technical feedback throughout the research. C.Y. reviewed and revised the final draft. J.Z. financially supported this work.

Funding: This research was funded by the National Natural Science Foundation of China, grant number 61601425, and the Presidential Foundation of China Academy of Engineering Physics, grant number YZJJLX2017006.

Acknowledgments: The authors would like to thank the Keylink Microwave Technology Company Limited of China for providing technical support in circuits fabrication.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. McKnight, K.; Darwish, A.; Zaghloul, M. A Compact Output Power Combiner for Broadband Doherty Power Amplifiers. *Electronics* **2019**, *8*, 275. [CrossRef]
2. Ramella, C.; Piacibello, A.; Quaglia, R.; Camarchia, V.; Pirola, M. High Efficiency Power Amplifiers for Modern Mobile Communications: The Load-Modulation Approach. *Electronics* **2017**, *6*, 96. [CrossRef]
3. Tena-Ramos, D.; Patino-Gomez, M.; Ortega-Gonzalez, F.J. Hybrid Envelope Elimination and Restoration Technique for Enhancing the Linearity of Switchmode Envelope Amplifiers. *IEEE Microw. Wirel. Components Lett.* **2017**, *27*, 186–188. [CrossRef]
4. Asbeck, P.; Popovic, Z. ET Comes of Age: Envelope Tracking for Higher-Efficiency Power Amplifiers. *IEEE Microw. Mag.* **2016**, *17*, 16–25. [CrossRef]
5. Jeong, J.; Chaudhary, G.; Jeong, Y. Time Mismatch Effect in Linearity of Hybrid Envelope Tracking Power Amplifier. *IEEE Microw. Wirel. Components Lett.* **2015**, *25*, 1. [CrossRef]

6. Kimball, D.F.; Nakatani, T.; Yan, J.; Mukai, K. Analog & Digital Envelope Tracking Power Amplifier Reduced Bandwidth Techniques for 5G NR. In Proceedings of the Asia-Pacific Microwave Conference (APMC), Kyoto, Japan, 6–9 November 2018; pp. 55–57.
7. Liu, Y.J.; Yoo, C.S.; Fairbanks, J.; Yan, J.; Kimball, D.; Asbeck, P. A 53% PAE Envelope Tracking GaN Power Amplifier for 20MHz Bandwidth LTE Signals at 880MHz. In Proceedings of the IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR), Austin, TX, USA, 24–27 January 2016; pp. 30–32.
8. Wang, Y.; Jin, Q.; Ruan, X. Optimized Design of the Multilevel Converter in Series-Form Switch-Linear Hybrid Envelope-Tracking Power Supply. *IEEE Trans. Ind. Electron.* **2016**, *63*, 5451–5460. [CrossRef]
9. Jin, Q.; Ruan, X.; Ren, X.; Wang, Y.; Leng, Y. Step-Wave Switched Capacitor Converter for Compact Design of Envelope Tracking Power Supply. *IEEE Trans. Ind. Electron.* **2017**, *64*, 9587–9591. [CrossRef]
10. Jing, Y.; Bakkaloglu, B. A High Slew-Rate Adaptive Biasing Hybrid Envelope Tracking Supply Modulator for LTE Applications. *IEEE Trans. Microwave Theory Tech.* **2017**, *65*, 1–12. [CrossRef]
11. Xi, H.; Cao, J.; Liu, N.; Ruan, X.B.; Fang, Z.; Ji, B.J. High Bandwidth Envelope Tracking Power Supply with Pulse Edge Independent Distribution Method. *IEEE Trans. Ind. Electron.* **2019**, *66*, 5907–5917. [CrossRef]
12. Huang, F.; Chen, W.; Zhang, Q.; Li, J.; Lv, G.; Feng, Z. A design methodology of envelope tracking power amplifier based on harmonic impedance tuning. *Microw. Opt. Technol. Lett.* **2018**, *60*, 639–642. [CrossRef]
13. Moon, J.; Kim, J.; Kim, B. Investigation of A Class-J Power Amplifier with A Nonlinear Cout for Optimized Operation. *IEEE Trans. Microwave Theory Tech.* **2010**, *58*, 2800–2811. [CrossRef]
14. Komatsuzaki, Y.; Lanfranco, S.; Kolmonen, T.; Piirainen, O.; Tanskanen, J.K.; Sakata, S.; Ma, R.; Shinjo, R.; Yamanaka, K.; Asbeck, P. A High Efficiency 3.6-4.0 GHz Envelope-Tracking Power Amplifier Using GaN Soft-Switching Buck-Converter. In Proceedings of the IEEE/MTT-S International Microwave Symposium (IMS), Philadelphia, PA, USA, 10–15 June 2018; pp. 465–468.
15. Carrubba, V.; Ture, E.; Quay, R.; Raay, F.; Musser, M.; Ambacher, O. Analysis and Performance of Drain Bias "In-dependent" Class-J Power Amplifier. In Proceedings of the Asia-Pacific Microwave Conference (APMC), Sendai, Japan, 4–7 November 2014; pp. 998–1000.
16. Chen, J.; He, S.; You, F.; Tong, R.; Peng, R. Design of Broadband High-Efficiency Power Amplifiers Based on a Series of Continuous Modes. *IEEE Microw. Wirel. Components Lett.* **2014**, *24*, 631–633. [CrossRef]
17. Tasker, P.; Benedikt, J. Waveform Inspired Models and the Harmonic Balance Emulator. *IEEE Microw. Mag.* **2011**, *12*, 38–54. [CrossRef]
18. Jeong, J.; Kimball, D.; Kwak, M.; Hsia, C.; Draxler, P.; Asbeck, P. Modeling and Design of RF Amplifiers for Envelope Tracking WCDMA Base-Station Applications. *IEEE Trans. Microwave Theory Tech.* **2009**, *57*, 2148–2159. [CrossRef]
19. Tuffy, N.; Guan, L.; Zhu, A.; Brazil, T.J. A Simplified Broadband Design Methodology for Linearized High-Efficiency Continuous Class-F Power Amplifiers. *IEEE Trans. Microwave Theory Tech.* **2012**, *60*, 1952–1963. [CrossRef]
20. Kimball, D.; Jeong, J.; Hsia, C.; Draxler, P.; Lanfranco, S.; Nagy, W.; Linthicum, K.; Larson, L.; Asbeck, P. High-Efficiency Envelope-Tracking W-CDMA Base-Station Amplifier Using GaN HFETs. *IEEE Trans. Microwave Theory Tech.* **2006**, *54*, 3848–3856. [CrossRef]
21. Cao, T.; Huang, F.; Zhang, Q.; Liu, Y.J. High Efficiency and Wideband Hybrid Envelope Amplifier for Envelope Tracking Operation of Wireless Transmitter. In Proceedings of the IEEE/MTT-S International Wireless Symposium (IWS), Chengdu, China, 6–10 May 2018; pp. 1–4.
22. Kim, D.; Kang, D.; Choi, J.; Kim, J.; Cho, Y.; Kim, B. Optimization for Envelope Shaped Operation of Envelope Tracking Power Amplifier. *IEEE Trans. Microwave Theory Tech.* **2011**, *59*, 1787–1795. [CrossRef]