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Review

A Review of Modern CMOS Transimpedance Amplifiers for OTDR Applications

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Abstract: The work presents a review of modern CMOS transimpedance amplifiers (TIAs) in the context of their application for low-cost optical time-domain reflectometry (OTDR). After introducing the basic principles behind the OTDR, the requirements for a suitable CMOS TIA are presented and discussed. A concise review of several basic TIA topologies is provided with a brief overview of their main properties. A detailed discussion is given on a representative set of approaches reported in the literature and the figure of merit (FOM) is introduced as a unified basis for performance comparison. Limitations of a single FOM as a basis for comparison are pointed out. Based on the provided discussion, some suggestions are made on the suitability of the TIA topologies for OTDR applications.

Keywords: capacitive-feedback amplifier; CMOS integrated circuits; low-noise and high-gain amplifier; optical time-domain reflectometer; performance metrics; shunt-shunt feedback amplifier; transimpedance amplifier

1. Introduction

The transimpedance amplifier (TIA) is defined as a sensitive and fast current measurement device which converts typically weak input current signal to the output voltage of considerable magnitude. Although the term TIA usually evokes an image of a resistive shunt-feedback (SFB) resistor approach [1], this architecture has been the gold standard by providing a fair trade-off for the most important TIA parameters. Although, as is the trend for all microelectronics, the classical SFB TIA benefits from the continuous improvement in the technological processes, novel TIA topologies and circuit-level modifications have been constantly reported. Almost each newly reported work provides a novel or refined perspective on design with respect to the target trade-off between different performance measures while addressing some of the system's or related technological constraints.

Although historically TIAs have been mostly developed for the front-ends of the optical receivers [2], (e.g., the families of 2.5, 10, 40, ... GB/s), their usage is definitely not limited to optical-only applications, although those have been for longer the major driving force beyond the development towards both lower noise and higher speeds. Nevertheless, in recent decades advanced TIA designs are becoming increasingly popular for a variety of applications such as particle physics and radiation detectors, miniaturized magnetic resonance spectroscopy [3], vision and biological sensors as well as inertial sensors such as Microelectromechanical Systems (MEMS) accelerometers and gyroscopes. As different applications usually have their own requirements for the main parameters of the TIA, the varying scenarios triggered an active search for improved and customized TIA designs. For example, high-speed optical communication circuits have pushed the bandwidth of TIAs in

multiple GHz range, while the biological or inertial sensors benefit from the novel designs with lower power consumption, reduced chip area and minimized noise while operating at significantly lower frequencies. A different set of constraints must be considered while evaluating how to design the TIA for a particular application. The specifics of the domain often play a crucial role on the final decision on selecting a suitable topology for product implementation.

The context of a typical TIA application is presented in Figure 1. Here the TIA can be considered to be the first block (the other two are the filter and the main amplifier—MA) of a so-called linear channel for the input current processing. The linear channel is modeled as a complex frequency response which relates the amplitude and the phase of the output voltage to that of the input current. The modeling of the linear channel as a product of three responses is shown in Figure 1. This is shown for depiction purposes and in practice the filter stage or the MA can be omitted or integrated into the TIA. As an input to the linear channel, a current i_{PD} from the photodiode (PD) is shown with its noise current $i_{n,PD}$. Clearly, any element providing a current input can be used in the given context. Here the noise characteristics of the linear channel are modeled as a single equivalent noise current generator $i_{n,TIA}$ at the channel's input (see Figure 1). Although this noise current source is not white, it can be considered to be stationary and its amplitude distribution can be often well approximated as a Gaussian one. This is quite opposite for the statistics of a simple PD, which is typically approximated to have white, but non-stationary and non-Gaussian noise.

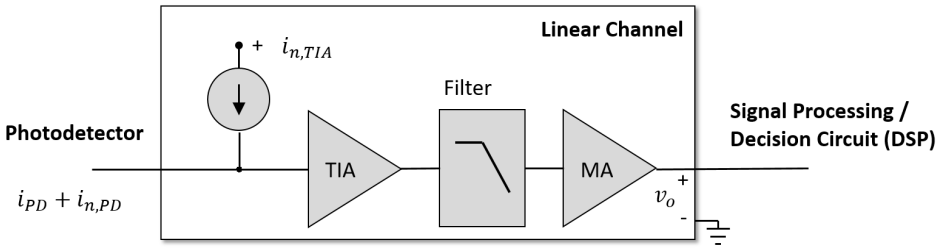

Figure 1. The context and the structure of the linear channel for a typical TIA.

Obviously, the front-end TIA is the most critical component of the channel affecting both the noise-sensitivity and the speed of the overall system [2]. At the output of the linear channel the voltage is provided which can be later used by either the signal processing or the decision circuits. Please note that here one assumes that the PD's performance is not the limiting factor for the front-end and thus, the focus of the paper is put on the improvements of the TIA design. Still, one has to be aware that different detectors or current sensing elements may have varying primary noise mechanisms which need to be considered while performing the circuit-level simulations and when assessing the feasibility of the candidate TIA design for a very particular application. For example, although the shot noise is believed to be a major noise source for PIN type detectors, avalanche noise with the excess noise factor must be considered if an Avalanche Photodetector (APD) is utilized. Furthermore, it is also assumed that the PD is sufficiently linear so that the signal distortions are minimized.

Until recently, the higher performance TIAs were often implemented in GaAs, HEMT, HBT and SiGe BiCMOS technologies due to their speed, noise, bandwidth and gain advantages [4]. Here the decision has been made to employ a conventional low-cost deep-submicron CMOS due to its low-cost and high integration characteristics—the so-called "holy grail" for system-on-chip (SoC) solutions [4]. In fact, the submicrometer CMOS technologies have provided sufficient performance for radio-frequency applications in 1–2 GHz since back in 2000 and, therefore, the performance of modern CMOS processes is more than sufficient for the intended 1 GHz Optical Time-Domain Reflectometry (OTDR) application. Although a discussion on performance of CMOS against III-V technologies probably deserves its own paper similar to that on CMOS for RF power amplifiers [5], some brief discussion may still benefit this review work. Definitely, for the high-volume production, the costs of the standard CMOS are relatively low and are continuously decreasing over the past several decades.

There is also a large production capacity available at the foundries and one does not need to own a custom line to keep up with the trends in the market [5]. Furthermore, from the system perspective the non-TIA components such as the processing logic etc. can be easily integrated with the TIA if desired while achieving almost any level of integration [6]. Of course, when having the data processing and the interface chips with different technologies, the packaging costs may increase while the overall system performance may decrease due to interconnecting bond-wires and pads [7]. Here the availability of millions of cheap transistors allows easy addition of the performance-enhancing functionality including complex bias circuits and advanced Electrostatic Discharge (ESD) design procedures—something which may be not easily available for III-V technologies. Although this work concentrates on CMOS TIA design, one shall not eliminate III-V technologies from the consideration. These technologies are continuously becoming feature-rich and with the addition of field-effect transistors to most of HBT processes designers now have higher flexibility in implementing circuits for more advanced and specific applications [5].

For cost-saving purposes CMOS technology presents an excellent candidate to design a truly low-cost and low-power TIA; however there are significant technical challenges which make the development path more than non-trivial. These technical challenges are mainly related to the contradicting requirements of a typical TIA such as high-gain, large bandwidth and, at the same time, low input noise [8]. Here increasing the gain usually increases chances of instability, while the requirement for lower noise performance often translates into higher power consumption. Furthermore, typical CMOS technological challenges have to be also addressed such as severe parasitic capacitances [9], supply voltage limitations, relatively low transimpedance and noise performance as well the inherent bandwidth limitations caused by large PD capacitance, where the latter is often responsible for the dominant pole in TIA and leads to the corresponding bandwidth constraints [7,10,11]. Finally, even though the reduction of the channel width does not shrink the size of analog circuits in the same way it does for digital ICs [12], such scaling may significantly increase the costs. Therefore, the specific technology shall be carefully selected as a trade-off for both the performance and the costs.

As a relatively large number of the design solutions for CMOS TIAs have been reported in the literature with each approach targeting an application-specific trade-off of the main circuit parameters, a basis for the performance comparison needs to be selected as a unified and a clear measure for relative positioning of the numerous designs reported in recent years. For example, while optical communications do not consider the linearity of the TIA as a crucial performance measure, this may become important for non-optical applications such as magnetic resonance imaging [3]. Even though a tabulated report on the major circuit characteristics is almost always needed for the completeness of the discussion or to convince the reader that a proposed design is definitely better than all those published before, the selection of the competitors is usually rather limited with up to 8 or 10 alternative solutions for comparison. Moreover, a tabulated specification of the main TIA parameters often results in a mixed or an unclear impression on the superiority of the proposed scheme based on one or a few key parameters from the set. Unfortunately, some of the parameters important for OTDR applications may not be reported in the most cited works on CMOS TIA for optical communications as these parameters may have a lower priority when compared to the gain and bandwidth for mainstream applications such as receivers for optical communication systems [13]. As with some of the previous works, we try to address a problem of a unified performance metric by introducing a so-called Figure of Merit (FOM), which can be used, at least till some extent, as a single criterion for the TIA's performance assessment. Clearly, the main requirement for this performance measure is that it should provide a fair balance for the most common TIA measures such as the amplifier's bandwidth, transimpedance gain, noise, the power consumption, etc. Although several approaches have been suggested in the literature [7,9,11], they have their own limitations. For example, some works [7,9] do not include the PD's capacitance and the noise level with the latter often considered to be a critically important design criterion for higher performance TIAs. On the other hand, the complex FOM as suggested in other

works may include a penalty due to the number inductances used in the design. However, counting inductances results in implicitly penalizing the area of the design similarly to FOM proposed in [7] which we would like to avoid due to several reasons. First, not all works explicitly report the design area or make a clear separation between the TIA front-end and the rest of the circuit. Secondly, the area may be not a good criterion as not all research works try to minimize the area of the final circuit as often the major objective is to improve the other circuit parameters.

Although the pursuit for a higher TIA performance has a much broader scope than the original application of the circuits for optical communications, we believe that a fair comparison and even an analysis of the unified performance metrics for TIA shall, nevertheless, consider an intended application domain of the circuits. The provided review is done within the context of developing a custom TIA for a front-end of higher performance, but nevertheless, lower-cost OTDR. Untill recent, the TIAs as used in commercial OTDR instruments were often implemented using discrete components [14]. Thus, due to their large parasitic capacitances, the bandwidth of typical circuits was limited to between 50 and 70 MHz significantly limiting the performance of available instruments [12]. Furthermore, the discrete solutions are more vulnerable to noise leading to significant limitations when trying to achieve higher dynamic range and signal-to-noise ratio [14]. A TIA implemented as a complete integrated circuit would result in lower parasitic capacitances and, due to significantly increased bandwidth, would lead to a dramatic decrease in the dead zone when compared to existing discrete solutions. For the OTDR instrument, similarly to other applications, the TIA appears to be the most critical part of the optical receiver (see the classical discussion in [2]) and its performance has a dramatic impact on the overall characteristics of the instrument [15,16]. Obviously, the specifics of OTDR instrumentation may mandate significant circuit innovations when compared to typical TIAs designed for optical communication networks. We believe that a CMOS TIA for a higher performance albeit low-cost OTDR instrument may heavily rely on circuit design techniques to overcome the technology shortcomings. The presented work tries to provide a systematic overview of the design methodologies and a fair comparison of the reported CMOS TIAs topologies as well as circuit-level solutions in the context of the envisioned OTDR application. Within the review, we will try to discuss and point out the issues which may be relevant for the OTDR applications according to the summary of the requirements and specifics of the application domain as presented in Section 2 below.

The rest of the paper is organized as follows: Section 2 presents a concise overview of the working principles behind OTDR, while Section 3 provides a general discussion on several classical TIA designs. Section 4 presents a detailed discussion on a set of recently reported CMOS TIAs with an in-depth discussion on the trade-off of each approach. Based on these findings, Section 5 provides a discussion on the suitability of some of the reported topologies for an intended OTDR application with Section 6 summarizing the contribution of the paper and providing the outlook for the future TIA implementation.

2. Optical Time-Domain Reflectometry

The OTDR is a well-established tool for investigating the attenuation characteristics of optical fibers [17]. Usually, OTDR is employed to characterize the faults, loss and damage along the optical fiber link, where the precise location of the faults can be resolved along with the nature of the problem. OTDR can be also used to evaluate the fluctuations of the fiber's parameters and is extremely useful for the case of optical transmission lines composed of several optical fiber cables. Moreover, OTDR is also often used for estimating the capacity and real-time performance of Passive Optical Networks (PON) [18]. The methods of OTDR employ the measurements of the time-delayed version of the Rayleigh Backscattering (RBS) signal or the Fresnel reflections from the incident optical power (e.g., injected optical pulse) along the fiber to provide a complete figure on the fiber's loss characteristics as a function of its length. The method allows the splice and the connector losses to be evaluated and delivers an estimate for the location of any faults in the optical link under test. During the OTDR operation, relatively narrow optical pulses are injected into the splitter and then propagate down the

fiber. As the signal comes across the discontinuities along the fiber, a fraction of the light is rejected and routed back through the splitter to the receiver. Based on the timing and the amplitude of the rejected pulse, the location and type of the fault in the fiber can be determined. Moreover, even in the fiber without a fault, some rejections do occur due to Rayleigh scattering which is caused by variations in the density or composition of the fiber material. This scattering mechanism is a dominant loss mechanism in the state-of-the-art fibers for typical operating wavelengths.

In OTDR applications the relationship between the frequencies of the incident and scattered light determine the effect of the light scattering in the fiber. In the case of elastic scattering, the frequency of the incident and scattered photons are equal. RBS is an example of such a mechanism, where the scattering occurs due to the linear transfer of the energy between the modes. RBS is caused by the density and the structure of the fiber material [19]. By contrast, in inelastic scattering the frequencies of the incident and scattered photons are not equal. Spontaneous Raman Scattering (SRS) is a good example of this inelastic process. Here the incident optical signal stimulates the molecular vibration of the silica material and final energy of Raman Stokes scattering is higher than that of the initial state, while the final energy state of anti-Stokes Raman scattering is lower than that of the initial energy state. The frequency of the scattered photons shifts to a particular value which is equal to the characteristic vibration frequencies of the molecules determined by the Raman spectrum of the fiber material. Please note that in Raman OTDR one must ensure the incident power to be larger than the threshold value for SRS to take place.

When a peak power of the injected optical pulse is limited, there is a trade-off between the width of the pulse and the spatial resolution [17], where a broad optical pulse increases the dynamic range by sacrificing the spatial resolution of the instrument. The effect can be mitigated by so-called correlation OTDR, where a pseudo-random bit sequence is used to modulate the optical pulse and the correlation between the backscattered light and the delayed bit sequence is obtained by the cross-correlator.

A typical OTDR instrument may contain several parts or modules which provide the required functions. These modules may include the waveform generator (one or more laser diodes), a detector, a signal processing unit and a display. The instrument should also provide capability to connect to the fiber under test using, for example, a directional coupler. The block functions of a typical OTDR instrument are shown in Figure 2.

The key characteristics of the technique are the attenuation dead zone (ADZ) and the dynamic range (DR), where both depend on the laser's pulse width and the bandwidth, and where the DR also depends on the laser's power and receiver's SNR. An ideal OTDR shall have a zero ADZ and infinite DR. However, such an ideal configuration can be only achieved for the case of a noiseless optical receiver with infinite bandwidth and delta-function type laser pulses [12]. In practice, the laser power is limited to approximately 1W by the nonlinear Kerr effect and the pulse width must be increased to deliver more energy into the fiber [12].

Several parameters of the OTDR usually have an impact on the performance of the instruments. First, the width of the injected optical pulse controls the amount of light provided to the fiber. A short pulse width enables high resolution and short dead zones, but results in a small dynamic range of the instrument. On the other hand, a longer pulse width enables high dynamic range but leads to reduced resolution and larger dead zones. Furthermore, the acquisition time is defined as the time during which the OTDR instrument acquires and averages the data points. By increasing the acquisition time one can improve the dynamic range without affecting the resolution and the dead zones. Finally, the time-domain measurements as obtained by the OTDR are mapped to distance along the fiber using the available index of refraction. The obtained characteristic (called the *trace of OTDR*) provides a visual interpretation of the measurements and can be effectively mapped to the length measurements of the fiber (Figure 2).

The availability of high-speed and high-density Application-Specific Integrated Circuit (ASIC) technology has made it possible to integrate the functions required to create the OTDR measurements on a single chip [14] and even use the OTDR capability directly in the optical transceiver modules [20].

Several interesting works have been recently reported which have adressed a problem of minimizing complete OTDR modules via a higher integration level. For example, a single chip integration OTDR ASIC developed by Ultra Communications Inc. for higher resolution OTDR applications was recently announced [20]. The system provides the necessary clocking, timing/pattern generation (arbitrary 20-bit pattern), receiving and sampling functions needed to implement an OTDR within a compact transceiver module and physical layer components while being only 4.0 mm × 1.655 mm. The programmable timing circuits can operate up to 10 GHz with current-mode output logic output and a four-channel receiver/sampling circuit. The presented ASIC can generate pulse widths of 100 ps and sample at 100 ps resolution, which is approximately equal to the round-trip time for an optical pulse to travel 1 cm in fiber. Moreover, within the architecture, the pulse width can be easily adjusted by setting a different bit pattern while enabling both flexible and low-cost implementation of OTDR within physical layer components. According to the authors, both the offset and the gain of TIA and associated post-amplifiers could be tuned appropriately for detecting small and large signals.

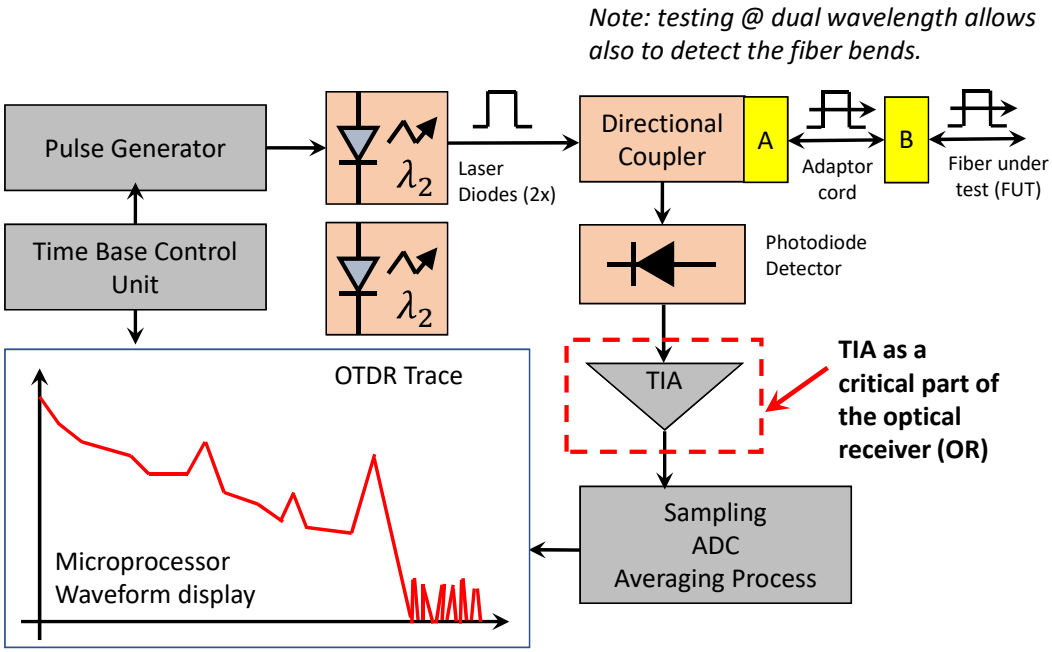

Figure 2. Block functions of a typical OTDR instrument.

A System-on-Chip (SoC) solution for OTDR had been also demonstrated in [18]. The developed circuit could be configured into several modes including high-performance mode (external modulator, expensive off-chip laser and PD) as well as low-cost mode (low power/gain with inexpensive laser and PD). The developed circuit achieved a maximum detectable fiber length of 25 km with the spatial resolution of 2.5 m, 4 m and 10 m depending on the configuration. When compared to the current discrete solutions (year 2016) on the market, the integrated system was expected to reduce the cost by factor 100×, area by factor 5× and power consumption by 4×. As the received signals due to Rayleigh backscattering were below the noise level of the system, only the measurements of Fresnel reflections could have been demonstrated.

Recently, yet another ASIC implementation of the OTDR module had been demonstrated in [14]. The OTDR ASIC was implemented using 350 nm CMOS process and occupied the area of 5 mm by 4 mm while operating from 3.3 V power supply.

Unfortunately, almost no TIA designs have been reported specifically for OTDR applications. Although no details on TIA architecture or its performance characterization have been reported in the original publication of [20], the detection scheme as proposed by the authors was designed to measure only the reflective events in the optical pathways and not the RBS, which is, probably, an indicator

that no special requirements for the TIA performance have been set and a classical resistive SFB TIA may have been used. The authors in [18] employed a two-stage TIA with common-mode feedback and corresponding amplification stages of 20 dB and 10 dB respectively. The TIA is followed by a second-order low-pass filter with biquad architecture and 20–40 dB tunable gain (step size of 10 dB). Furthermore, an inverse Thomas-Tow biquad technique and DC offset cancelation are employed for low-noise and offset compensation. Finally, the authors have placed a programmable gain amplifier between the filter and the output buffer to provide a final amplification for an output scale of 30 dB with a 1 dB step.

The newest work [14] employed a classical resistive feedback TIA, where additionally a feedback capacitance was added in parallel with the feedback resistor. While the transimpedance gain of the TIA was mainly determined by the feedback resistor R_F, the feedback capacitance C_F helps to improve the stability of the TIA. The resistor mux was designed for adjustable transimpedance gain. The core voltage amplifier was designed as a 2-stage OP-Amp due to simultaneous requirements on high bandwidth and wide output swing. The authors also implemented a sample and hold amplifier to decouple the TIA from a Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) as the ADC may load down the TIA affecting the overall performance of the system.

A unique work on addressing specifically TIA design for OTDR is [12], where a variable gain fully differential SFB TIA was proposed. The variable gain was implemented with feedback resistors connected in series using the single-pole double throw (SPDT) switches to reduce input parasitic capacitances with five resistor pairs used to achieve the desired range of the gains. A self-biased topology was chosen, and a start-up circuit was added to avoid an unwanted bias state. Unfortunately, the author does not go beyond a classical SFB TIA and exact noise figures are not provided to facilitate a juxtaposition to the other reported TIAs. Therefore, the comparison of the reported CMOS TIA designs as presented in this work is done without an explicit application domain constraint and the TIAs are selected from similar (mainly optical) applications.

The sensitivity of an optical receiver can be limited by various noise sources, both in the detector and in the following amplifier. Originally, two options may have been considered for developing a low-noise input stage for OTDR either by using a high-impedance or a TIA. Nevertheless, the latter type is preferred for amplification of the backscattered signals due to its superior dynamic range. However, the noise performance of both approaches is similar (the feedback resistor of TIA becomes the load resistor in high-impedance approach). As the TIA-based strategy may be considered to be a well-established technique for the design of high-performance optical receivers, it had been selected for OTDR application.

To evaluate properly the suitability of the reported TIA topologies for the intended application, a preliminary specification for the CMOS TIA shown in Table 1. The bandwidth of the TIA must be adequate to reproduce the shortest pulse length and, thus, the degradation of the range resolution in a final OTDR system can be avoided. Out of these preliminary requirements, one should point out two which make the design rather non-trivial: the relatively low noise requirement (<5 pA$/\sqrt{\text{Hz}}$) for the given bandwidth and the flatness of the frequency response (0.1 dB). These two requirements eliminate most of the standard high-speed architectures and could need special handling including revision of an approach which is typically used for OTDR application—i.e., classical resistive shunt-feedback TIA. The requirement on the flatness of the frequency response may also challenge widely adopted techniques of inductive broad-banding or those might be applied with greater care. As the work addresses the design of a single-channel TIA, no special consideration for crosstalk performance is, probably, required, while particular treatment expected to ensure the specification conformance for a broader range of transimpedance gains. Finally, no constraints are given in terms of the chip area, although, naturally, one should seek for area minimization when targeting commercial low-cost applications. Please note that the design of TIA as an integrated circuit leads to an increased flexibility in circuit tuning and noise optimization via the device geometry adjustment, when compared to the design with discrete components [21]. Here special design optimization techniques can be used to find

optimal values for the geometry of separate elements. This becomes an important feature which is simply not possible when designing the TIA from discrete components.

Table 1. Preliminary CMOS TIA specification for OTDR application.

Parameter	Value
3dB bandwidth	0.1–500 MHz @ min. gain of 10 kΩ 0.1–1 GHz @ min. gain of 5 kΩ
Noise power spectral density	<5 pA/$\sqrt{Hz}$ @ 500 MHz
Gain	Variable: 5 (10), 25, 100, 500 kΩ
Frequency response flatness	0.1 dB
Input capacitance	0.5 pF
Photodetector capacitance	0.5 pF
Quiescent power	$<$50 mA
Output common-mode voltage	0.7…1.7 V
Linear output signal swing	$\pm$1 V
Saturated overshoot recovery to 0.1 dB	$<$5 ns
Technology	CMOS (TSMC 0.18–0.13 µm)
Operating temperature range	Industrial ($-$40…+85 °C)
Power supply voltage	1.8 V

Please note that the TIA shall be designed to operate with the C_D as large as 500 fF and input capacitance (ESD, etc.) of additional 500 fF. The need to support such large capacitances arises due to PD being external to the chip with correspondingly large bondpad capacitances. A lower input capacitance would permit a higher input impedance and allow smaller devices to be used in TIA resulting in substantial power savings, while retaining the same bandwidth and improved sensitivity or increased bandwidth with the same sensitivity.

A special challenge of the proposed CMOS TIA is the requirement of the variable gain. Although the original work on OTDR-specific TIA [12] reported a variable gain SFB TIA, a practical implementation may be non-trivial if the rest of the constraints need to be fulfilled with a single global TIA structure. Furthermore, depending on the topology finally selected for the TIA, it may be non-trivial to implement a variable gain while changing only one parameter of the circuit (i.e., such as implemented with feedback resistor in [12] or [14]) and advanced design methodologies may be needed. Please note that the specification does not have an explicit requirement for the phase linearity and the group delay variation for the TIA as well as no constraints on the die size are presented.

The specification, as shown above, corresponds to high-resolution integrated OTDR based on RBS and Fresnel reflections. On the other hand, the methods of OTDR are often used in combination with SRS to implement distributed temperature sensing [19] as the anti-Stokes components of SRS are strongly sensitive to temperature. This nonlinear effect allows the optical fiber to act as a distributed sensor which can replace many point sensors [22] with the detector placed at the beginning of the fiber cable. The technique is capable of providing many sensing points over a wide area and has been successfully used in spectroscopy and different monitoring applications. Please note that the optical fiber acts as a combination of the transmission medium and the sensor, where the monitoring of backscattered optical Stokes and anti-Stokes components takes place. An interesting idea on combining both RSB and SRS was proposed in [23] to support an integrated background correction function as the change in background transmission properties of the fibers (e.g., due to ageing effects) can be distinguished from pure thermal effects.

Unfortunately, conversely from classical OTDR, where recently several ASIC have been reported (see [14,18]) and special OTDR-specific TIAs have been considered [12], no similar works are known to the authors for Raman OTDR applications. Typically, for Raman OTDR applications a laboratory equipment with APD and data acquisition cards are employed (see [19,24]). As no details on the built-in APD or external TIA are provided, very little information can be extracted on Raman OTDR requirements for TIAs. The major difference is that as high spatial resolution for distributed

temperature sensing is typically not required, the TIA for Raman OTDR application may need significantly lower bandwidth (on the order of several to tens of MHz) when compared to the specification in Table 1. The work [24] reported on the amplifier bandwidth of 50 MHz, while a TIA with only 3 MHz bandwidth was employed in [25].

3. Design Strategies

The study on recent advances on CMOS TIA will definitely start from the recent book [1]. The work provides a gentle introduction to the area of optical communications and covers all the major TIA topologies and practical circuit implementations for optical receivers, although the discussion on TIA is general enough and in most cases can be used for other application areas. Although Chapter 9 of [1] summarizes a set of representative high-speed TIA designs, no attempt is made to quantify the performance of the designs in a form of a unified performance metric. Furthermore, as the author concentrates on optical receivers, a priority in the discussion is given to the modern circuits for high-speed applications, while recent works on lower-speed and low-noise application circuits seem to be of minor interest. Finally, due to a broader scope of the monograph, the author in [1] provides only a general information on the designs without in-depth discussion of the implementation details. The author concentrates on the basic properties of the selected topologies and many details on the circuit-level innovations needed to make the circuits operating in practice are left unaddressed.

Below, a basic introduction to classical TIA design strategies is presented. A general overview of a set of selected topologies is provided along with concise comments on their pros and cons, while the details regarding the performance of the selected circuits based on some of these classical designs are discussed in Section 4.

Before we proceed with more advanced design, let us consider a so-called *passive TIA* which is a single resistor which is placed in parallel with PD's capacitance C_D [26]. While the transimpedance of such a circuit is equal to R, from the bandwidth relationship:

$$BW_{-3\text{dB}} = \frac{1}{2\pi R_{IN} C_D}, \tag{1}$$

it becomes clear that the possible values of C_D are bounded by the constraint above. For example, for the bandwidth and gain requirements as specified in Table 1, the upper bound on the C_D which can be used with such passive TIA is approximately 32 fF. Although CMOS compatible PDs with small capacitances have been reported, the requirements for OTDR instrument are 0.5 pF for the C_D as well as an additional input capacitance up to 0.5 pF which would not fit this simplistic passive TIA architecture. Please note that the integrated input-referred noise would have been a yet another constraint, although not critical in this case.

Within the discussion below we do not consider the simplest designs such as low- and high-impedance front-ends due to their poor noise or bandwidth performance [1], although those have been the first ones to consider in early years of the optical communication systems (e.g., see the original discussion in [2]).

3.1. Inverter TIA

The inverter TIA with resistive feedback is, probably among the simplest feasible TIA configurations and is shown in Figure 3. The push-pull inverter is used to maximize the transconductance and is configured as a digital inverter with the operating point selected to have both transistors in the saturation region resulting in the inverter in its high-gain region. Please note that in this case and all the cases described below, the detector is represented by the current source in parallel with the detector's capacitance C_D. The current source is responsible for the generation of the carriers which are separated across the detection junction capacitance C_D [2] with the series resistance neglected in this circuit.

Some straightforward modifications of this simple design are also possible. For example, the feedback resistor can be replaced with the MOSFET device [27,28] or additional NMOS added in parallel with M_1 to minimize the Miller effect [28]. A single-stage inverter amplifier can be replaced with multiple cascaded stages if one needs an increased gain (e.g., 5x in [29]). The bandwidth of this basic design can be improved by adding the inductor in the feedback path and while the transfer function of the system adds one zero and one pole compared to a pure resistive approach, the input-referred noise gets also improved [8]. Although the inverter configuration of the TIA was among the earliest employed in CMOS TIA, due to its simplicity it is still often used with minor modifications such as inductive peaking [30].

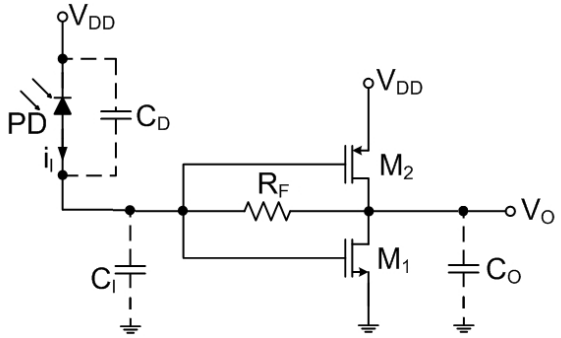

Figure 3. Push-pull inverter TIA with resistive feedback.

3.2. Shunt-Feedback Resistor TIA

Any discussion on designs for TIA shall include a classical SFB TIA as shown in Figure 4. This is a well-accepted feedback topology for the TIA circuits and is often a default choice due to its low input impedance as desired for a current input block and, at the same time, low output impedance, as needed for voltage-output amplifier [31]. The feedback network also ensures almost constant transimpedance gain in the bandwidth of interest while decreasing the sensitivity to process and measurement variations [32]. The design provides a reasonable balance between all the key parameters of the TIA such as relatively large gain-bandwidth product and acceptable (often, but not always) noise [29].

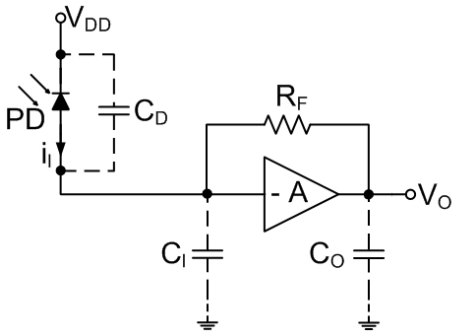

Figure 4. Basic configuration of the shunt-feedback TIA.

In general, there is a certain flexibility in the design of the voltage amplifier. Usually, challenged by the requirements of the noise performance, a simpler voltage amplifier with fewer active components is opted [32] leading to a smaller input current noise. A basic TIA design can use a single-stage voltage amplifier under an assumption that sufficient gain is achieved. The choice of the topology for the input voltage amplifier is mainly dictated by the noise requirements as well as those of bandwidth.

In the basic version of this TIA topology, the mid-band transimpedance gain R_T becomes equal:

$$R_T = \frac{A}{A+1} R_F, \tag{2}$$

which for sufficiently large values of the open-loop gain $A >> 1$ (which typically the case for a properly designed core voltage amplifier), becomes approximately equal to R_F. The 3-dB bandwidth of the design becomes correspondingly:

$$BW_{-3\text{dB}} = \frac{1}{2\pi R_{IN} C_T}, \tag{3}$$

where R_{IN} is the input resistance of the circuit and C_T is the total input capacitance. As the following holds:

$$R_{IN} = \frac{R_F}{A+1}, \tag{4}$$

and $C_T = C_D + C_I$, one easily obtains:

$$BW_{-3\text{dB}} = \frac{A+1}{2\pi R_F \left(C_D + C_I\right)}, \tag{5}$$

where C_I is the input (including gate) capacitance and C_D is the sum of all capacitances of the active area of the PD as well as the associated parasitic capacitances such as those arising from the bond-pads, ESD circuits, etc. [15]. These input parasitic capacitances limit the bandwidth and the noise performance of this simple TIA topology [32], where the choice of the PD allows increase of the bandwidth if its capacitance is low. The expression above sets the maximum bandwidth which can be achieved by the regular feedback TIA, where the product $R_{IN}C_T$ defines the dominant pole of the circuit.

The low-frequency input-referred noise current for the SFB TIA is given by:

$$\overline{i^2_{n,TIA}} = \overline{i^2_{n,R_F}} + \overline{i^2_{n,amp}} = \overline{i^2_{n,R_F}} + \frac{\overline{v^2_{n,amp}}}{R_F^2} = \frac{4kT}{R_F} + \frac{4kT\gamma}{g_m R_F^2}, \tag{6}$$

where k is the Boltzmann's constant, T is the absolute temperature and γ stands for the noise excess factor of the transistors and g_m is the transconductance of the transistor in CS core voltage amplifier configuration. The input-referred amplifier noise is passed to the input while scaling it with R_F^2 and the overall input-referred noise current is approximately equal to the one of a simple impedance front-end. From this basic design above it becomes clear that this TIA benefits from the low noise of a large R_F without the drawback of a slow response as it may be the case for a trivial impedance TIA [1]. Please note that the R_F does not carry a large bias current and hence its value can be maximized.

If one limits the analysis to the TIA designs which are free of the amplitude peaking (e.g., Butterworth, Bessel and critically damped designs), one can arrive to the following inequality which is known as the *transimpedance limit* for the second-order system:

$$R_T \leq \frac{A f_O}{2\pi C_T BW^2_{-3\text{dB}}}, \tag{7}$$

where Af_O stands for the gain-bandwidth product of the single-pole voltage amplifier and which is roughly constant for the given technology. The transimpedance limit predicts a rapid noise increase for wider bandwidth making the classical SFB TIA far less attractive for high-speed applications. Furthermore, in advanced CMOS technologies the lower V_{DD} can further limit the attainable gain A with one stage voltage amplifier. Clearly, cascading more gain stages, though boosting the amplifier

gain, makes it difficult to ensure a sufficient phase margin and, therefore, often a single-stage core amplifier is employed for these designs.

From the discussion above it becomes clear that the significant noise reduction for a typical SFB TIA can be only achieved at a price of reducing the bandwidth, resulting in significant design challenges in the form of trade-offs between input noise current and speed as well as gain, power dissipation and the requirements for the supply voltage [33]. Therefore, for typical speed, voltage headroom and power constraints the core amplifier transistor may contribute as much input noise as the feedback resistor itself. Numerous works have been reported in an attempt to design higher performance TIAs while relaxing the influence of large input parasitic capacitances using conventional CMOS. The discussion below provides only a summary of some representative works which the authors consider relevant within the context of the OTDR application.

3.3. Common-Gate TIA

A classical SFB TIA, as described above, can also have stability issues when designed to work with a large PDs of different capacitances and the capacitance C_D also significantly limits the bandwidth of the circuit as well as its noise performance [15,34]. Although the feedback capacitance C_F (in parallel with R_F) can also reduce the TIA's sensitivity to varying values of C_D (Exactly this behavior was employed in [14] while designing the OTDR ASIC), it also reduces the maximum achievable transimpedance R_T and, therefore, may not always be the best option. An alternative topology to remedy these issues is to use a so-called *feedforward* Common-Gate (CG) TIA as shown in Figure 5. Here the PD capacitance is isolated from the bandwidth determination by reduction of the input impedance of the amplifier which is roughly equal to $1/g_{m,M_1}$. Thus, if the output pole does not limit the bandwidth, one gets:

$$BW_{-3\text{dB}} = \frac{1}{2\pi R_{IN} C_T} = \frac{g_{m,M_1}}{2\pi C_T}. \tag{8}$$

Therefore, even with a big C_T either a wider bandwidth or a larger transimpedance gain can be easily achieved. As all the signal current flows into the load resistor R_D, the transimpedance can be found to be $R_T = R_D$. A clear advantage of this architecture is that the input impedance and the transimpedance are decoupled and can be individually adjusted, while in SFB TIA the transimpedance gain and the input impedance are dependent on each other resulting in the bandwidth and gain being inversely proportional [7]. The thermal noise current from bias M_2 and the load resistor R_D are directly referred to the input resulting in:

$$\overline{i^2_{n,TIA}} = \overline{i^2_{n,R_D}} + \overline{i^2_{n,M_2}} = \frac{4kT}{R_D} + 4kT\gamma g_{m,M_2}. \tag{9}$$

This architecture has typically low power consumption, broadband and no stability issues while relaxing the effect of the input parasitic capacitance. Still, a straightforward implementation of the CG TIA has several fundamental disadvantages such as relatively high noise [33] as the noise currents due to R_D and M_2 are directly referred to the input. However, what is maybe even more important, the design provides fewer degrees of freedom for noise optimization when compared to the classical SFB TIA design described above. As the voltage drop across R_D must be maximized to minimize its noise current and to achieve a high gain, the allowable headroom for M_2 is limited, resulting in significant noise contribution. One could also mention that for large transistors and/or large C_D, the noise contribution due to M_1 also rises at high frequencies. Finally, with the same technology and bandwidth, the feedforward TIA will always have lower transimpedance when compared to the feedback approach.

Please note that although often the CG TIA is only used as an input stage for the complete TIA followed by a voltage-gain stage, the poor noise performance of the input stage makes the topology less suitable for very low-noise applications. Even though the CG TIA seemed to be an interesting

candidate due to its reduced sensitivity to input parasitic capacitances, its high noise contribution will make the design less suitable for the intended low-noise OTDR application.

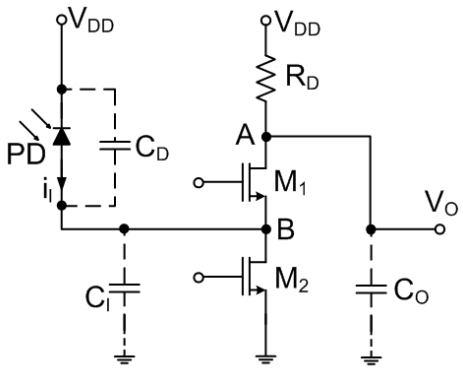

Figure 5. Common-gate TIA.

3.4. Regulated Cascode TIA

The regulated cascode (RGC) TIA (see Figure 6), previously also known as a common-gate TIA with active feedback [26], is yet another approach to get a very small input impedance which can support a very high bandwidth at very low power consumption [6]. Still, similarly to the case of CG TIA, the noise performance is worse than that of the CS-based SFB TIA and although the RGC configuration can also isolate the capacitance effect, it may be difficult to implement the topology at very low supply voltages.

In RGC TIA the input is applied to the source of the common-gate amplifier M_1 which is a low input resistance node and is suitable for the input current. The voltage amplifier creates feedback which connects the source and the gate of M_1 together, where the former gets a small portion of the input and creates a voltage signal at the gate of M_1 [16]. This signal is again inverted and amplified by M_1 and is added to the output signal from M_1 in CG configuration. The feedback also increases the transconductance of M_1 which itself helps to reduce the input resistance and isolate the parasitic capacitances at the input, thus resembling the inductive characteristic. The mid-band transimpedance gain R_T becomes:

$$R_T = R_D, \tag{10}$$

and is limited by R_D which often cannot be increased too much due to the limited voltage supply in low-power applications. However, the input impedance:

$$R_{IN} = \frac{1}{g_{m,M_1}(1+A)}. \tag{11}$$

and is factor $1 + A$ smaller compared to CG TIA. In its simplest case, the bias stage of RGC is implemented as a single-stage CS voltage amplifier, although more advanced configurations are clearly possible. Finally, the input noise current becomes smaller than that of the CG input current configuration which makes RGC configuration often preferred over CG under the same conditions.

A simulation-based comparison of SFB, CG and RGC TIA is provided in [26], where minimum design current was reported depending on the PD's capacitance. Although the devices were optimized for a particular application of the authors in [26], the simulation clearly demonstrates that the CS-based RGC TIA has the worst scaling with increasing C_D for high-frequency applications, while RGC TIA seems to have the lowest minimum device current from all three reference architectures.

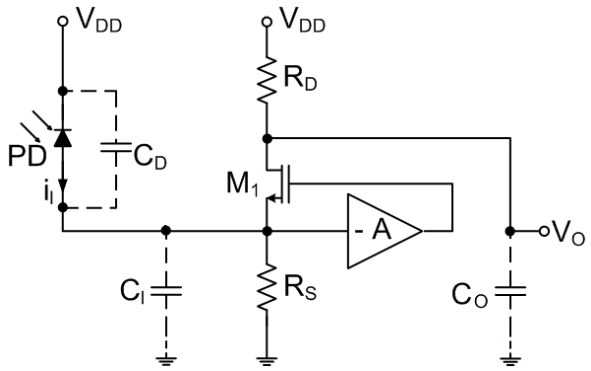

Figure 6. Regulated cascode TIA.

3.5. Inductor Peaking TIA

Even though the inductors have been historically associated with narrow-band circuits, they appeared to be useful in broad-circuits as well [4]. Monolithic inductors have opened up new possibilities for wideband circuit design and had been intensively employed in developing modern CMOS TIA circuits. The inductor can tune out the capacitance to boost both the transimpedance and the bandwidth of the TIA circuit.

The TIAs with inductor peaking mainly differ in the way the inductors are mounted to expand the bandwidth of the circuit. Several approaches are known such as feedback peaking inductor [8,16], shunt peaking [4,35], single or multiple inductive-series peaking [29,30], π-type inductor peaking (PIP) [9,36] or different combinations of the aforementioned [26,37]. For example, by using an inductive shunt peaking at the output of TIA one is able to improve the bandwidth by adding a zero to the transfer function, while an addition of the inductor to the gate of the output transistor in RGC configuration (see [26]) implements an inductive peaking by adding a pair of complex conjugate poles. Depending on the type of the inductive peaking, one may theoretically achieve a bandwidth enhancement as high as factor 3.46, although the discrepancies in the real circuit and the assumptions on the parasitic capacitances may degrade the expected circuit bandwidth (see results in [36]). A clear advantage of the inductor peaking TIA is that the bandwidth increase often comes with no additional power dissipation [4,35], while the flatness of the frequency response is typically (but not necessarily) sacrificed.

One of the most interesting approaches is the PIP method detailed on a series of works of Jun-De Jin et al. [9,36] which was proposed to break the bandwidth limitation by resonating with the intrinsic capacitances of the devices. Composed of three inductors, PIP can enhance progressively the bandwidth of the CS- stage by the factor of 3.31 without disturbing the low-frequency gain and permitting the gain flatness of around 2 dB. The PIP inductors can create two zeros and two pairs of complex conjugate poles in the transfer function resulting in significantly enhanced bandwidth [36]. Please note that PIP topology only alters the frequency response whereas the DC power consumption remains unchanged compared to the basic amplifier without the PIP inductors.

On-chip inductors are typically realized either by using the bond-wires or on-chip spirals. As the bond-wires may exhibit much higher quality factors when compared to the spiral inductors, their usage may be constrained by the limited range of the realized inductances and large production fluctuations [4]. Furthermore, the bondpad capacitance may also degrade the performance of such inductor. According to [4], differential implementation of such amplifiers may experience a degradation in power supply rejection ratio (PSRR) due to possible mismatch between the two bond-wires. The spiral on-chip inductors usually exhibit good matching and have been more suitable for envisioned differential architectures of the OTDR TIA. Although these inductances also allow a larger range of values to be realized, they may possess lower quality factors and have been historically harder to model as is elaborated in [4]. In practice, the inductor design problem often boils down to choosing

the geometrical parameters of the spiral such as the desired inductance is obtained while the parasitic capacitance is minimized.

Nevertheless, using inductors to increase the bandwidth of the amplifier has several important drawbacks. First, the usage of inductors with a standard CMOS dramatically increases the chip size and, therefore, make associated hardware costs very high especially when one addresses cheap devices. This argument, however, may be not as critical anymore as the optimized shunt peaking on-chip inductors may consume only a fraction (e.g., 15%) of the total chip area [4]. On the other hand, a large inductor not only occupies a large area, but can also cause difficulties to maintain an inductive characteristic up to the circuit bandwidth [38]. Furthermore, the substrate coupling typically increases through the inductors resulting in higher cross-talks when compared to inductor-less designs (Low substrate coupling is extremely important in multi-channel solutions where crosstalk between several parallel channels have to be minimized). Finally, large group delay fluctuations can become also problematic [39] and the TIA with inductor peaking may also degrade in digital process with thin metals and lossy passive components [10].

3.6. Capacitive-Feedback TIA

As we have seen above, one of the main drawbacks of the SFB TIA is due to its relatively poor noise performance. The current noise of the resistor is directly added to the input-referred current noise of the TIA which dramatically degrades its noise performance. Hence, one of the solutions to reduce the noise of the circuit is to replace the noisy feedback resistor with a noise-free circuit such as a capacitor. Such a circuit would eliminate the disadvantages of typical resistive feedback while maintaining the advantages due to the circuit's feedback structure.

An attempt to address the typical problems of CG and SFB TIA by designing a so-called capacitive-feedback (CF) TIA have been first reported in the seminal work of Razavi [33]. Later, in a series of works Shahdoost elaborated the concept of the capacitive feedback [21,31,32,40]. The general circuit topology of a TIA with a capacitive-feedback network is shown in Figure 7. Here the capacitance C_1 senses the voltage across C_2 and returns a proportional current to the input. If $A >> 1$, then the current gain is approximately:

$$\frac{I_{out}}{I_{in}} \approx 1 + \frac{C_2}{C_1}. \tag{12}$$

and this suggests that the circuit can operate as a current amplifier [33]. With the resistor R_D connected to the drain of the output transistor, the low-frequency gain becomes:

$$R_T = \left(1 + \frac{C_2}{C_1}\right) R_D, \tag{13}$$

with the bandwidth equal to:

$$BW_{-3dB} = \frac{(1+A)\, g_{m,M2}}{2\pi C_2}. \tag{14}$$

In the case of the CS input stage (transistor M_1 and resistor R_1), the noise calculations can be shown [40] to result in:

$$\overline{i^2_{n,TIA}} = \frac{4kT\gamma}{g_{m,M1}} \left(1 + \frac{1}{g_{m,M1} R_1}\right) \left[\left(\frac{C_2}{1 + C_2/C_1} + C_T\right) s\right]^2. \tag{15}$$

As the resistor R_1 is usually increased to improve the noise performance and considering the headroom limitations, the term $\frac{1}{g_{m,M1} R_1}$ may be neglected resulting in:

$$\overline{i^2_{n,TIA}} = \frac{4kT\gamma}{g_{m,M1}} \left[\left(\frac{C_2}{1 + C_2/C_1} + C_T\right) s\right]^2. \tag{16}$$

The topology as shown in Figure 7 has three major advantages over classical TIA designs [33]. First, the gain definition network consisting of capacitances C_1 and C_2 contributes no noise. Furthermore, the capacitance as seen at the input node to ground lowers the DC loop gain rather than degrades the stability. Finally, the total noise current contributed by the first stage is significantly lower than the one in classical SFB TIA for the frequencies of interest. Moreover, the system's gain is due to the ratio of two main capacitors which makes the overall design less vulnerable to the process variations when compared to the case when the absolute value of the resistance is used. Still, several significant circuit-level adjustments, such as DC current elimination, need to be also implemented to produce a functioning design.

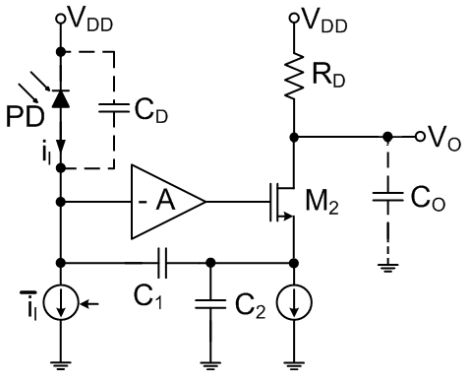

Figure 7. TIA with a capacitive-feedback network.

Although the noise of M_2 and the current source is also of a concern, with proper design the contribution of M_2 can be made negligible. This can be achieved by representing the output stage as a voltage source in series with the gate, which allows this noise to be divided by the gain A and, therefore, simply treated as part of the noise of A [33]. One can also show that the noise of the aforementioned current source directly adds to the noise current of R_D—behavior similar to the CG stage discussed before. When compared to the CG TIA, the design also has clear advantages: while in CG TIA both the R_D and M_2 directly contribute the noise, in the CF scheme the noise currents of R_D and the current source are divided by $(1 + C_2/C_1)$. Moreover, although in CG TIA the transimpedance gain is equal to R_D, in capacitive-feedback approach it is increased by the same factor $(1 + C_2/C_1)$.

4. Reported Results and Performance Evaluation

As we have discussed in the introduction, the CMOS TIA performance comparison may benefit from adopting a unified performance measure in the form of FOM. For the presented overview we suggest adopting the following FOM:

$$FOM_1 = \frac{\sqrt{BW\,[\mathrm{GHz}]}R_T\,[\Omega]\,C_T\,[\mathrm{pF}]}{Noise\left[\mathrm{pA}/\sqrt{\mathrm{Hz}}\right]\,P\,[\mathrm{mW}]}. \tag{17}$$

where BW is the bandwidth in GHz, R_T is the transimpedance gain in Ω, C_T is the combined PD and parasitic capacitance, P is the power in mW and the $Noise$ is the input noise current density. Please note that differently from the work of Atef [6], an input current noise density is used instead of an equivalent input noise and this is exactly the reason a square-root of the bandwidth is taken in the numerator of the expression above. Alternatively, the FOM metric of Atef [39] can be also used:

$$FOM_2 = \frac{BW\,[\mathrm{GHz}]R_T\,[\Omega]\,C_T\,[\mathrm{pF}]}{Noise\,[\mu\mathrm{A}]\,P\,[\mathrm{mW}]}. \tag{18}$$

It is interesting to notice that both metrics show the best results for the same design and in general may be considered to be equivalent. If the works do not specify the value of C_D, a default value of 0.5 pF is used for the FOM calculations. We consider this to be a reasonable assumption as the values in practice are between 0.2 pF and 0.6 pF for external photodiodes. For most of the works it may be unclear whether the reported P_D is a true PD capacitance, or a combined value including the parasitic capacitance such as the one due to ESD protection diode and pad (The parasitics due to ESD protection and pad may be as high as 0.5 pF as reported in [15]). Simpler FOM metrics have been also used historically. For example, in their series of works on PIP TIA Jun-De Jin et al. [9] have used the gain-bandwidth product per DC power as some FOM approximation:

$$FOM_1 = \frac{\sqrt{BW\,[\mathrm{GHz}]}R_T\,[\Omega]}{P\,[\mathrm{mW}]}. \tag{19}$$

Even though this FOM may work fairly well for benchmarking the TIA's for high-speed optical communications (e.g., 40-Gb/s addressed in [9]), the metric does not penalize the designs with large noises and does not consider the value P_D which may have a detrimental effect on the achievable bandwidth of the amplifier. Usage of such FOM may benefit simpler and faster TIAs with significant noise and can unjustly penalize the topologies targeting low-noise applications.

Clearly, if a particular design does not report on some of the other critical performance measures such as power consumption, no FOM value could be calculated. In this case, the design will be still described in the summary parameter table below and only FOM numbers may be missing. As is clear from the expression above, we have also chosen the strategy not to penalize, explicitly or implicitly (e.g., via counting the inductances) the area of the proposed design. There are several reasons for this decision. First, numerous works do not report the total chip area especially is the results are reported for simulation only and no post-layout simulation had been performed. Furthermore, some works report the area only for the front-end TIA while considering the rest of the auxiliary circuits of minor importance, while still the others include the total design area with the buffer. Thus, the inclusion of the area for this design may significantly bias the ranking. Finally, as a lot of designs have been reported by academic research groups, it becomes unclear on how much effort has been really invested on minimizing the final chip area especially when this is often not the key requirement in research projects.

The summary of the performance of the selected TIA as reported in the original works is shown in Table 2. When a total input noise current is specified by the authors, the noise density is calculated using the provided bandwidth values. The FOM is calculated using the first approach described above. Please note that in some cases the authors either do not specify the value of the C_D or specify together with the rest of the input parasitics. Moreover, in some cases, the power consumption cannot be clearly separated between the TIA front-end and the rest of the circuit. Bearing all this in mind the FOM shall be only considered to be a rough indicator and as an approximation of ever evading unified performance metric. The works are sorted in the order of publication to avoid biasing in terms of one performance indicator.

Table 2. Performance measures of several CMOS TIA.

Work/Year	Technology	TIA Gain (dBΩ)	BW_{-3dB} (GHz)	Power/Supply (mW)	Avg. in.-Ref. Noise (pA/$\sqrt{\text{Hz}}$)	FOM	Topology
Park [34] [2], 1998	0.6 µm	61	3.5	135	4.2	1.18	RGC with voltage follower and feedback resistor
Mohan [4] [3], 2000	0.5 µm	58.1 / 64.1	1.2	225 @ 3.3V	17.3	0.14/0.27	differential, with CG input stage and inductive shunt-peaking
Razavi [33], 2000	0.6 µm	78.8	0.55	30 @ 3.0V	4.5	23.92	capacitive feedback
Oh [35], 2004	0.35 µm	68	1.73	50 @ 3.3V	3.3	12	broadband cascode with active inductor peaking
Wu [30], 2005	0.18 µm	61	7.2	70.2 @ 1.8V	8.2	1.3	multiple inductive-series peaking, inverter TIA with M-derived matching
Jun-De Jin [9], 2006	0.18 µm	51.0	30.5	60.1 @ 1.8V	34.3	0.048	4 cascaded CS-stages with PIP
Park, Oh [15] [1], 2007	0.18 µm	64	2.1	50 @ 1.8V	33.2	2.76	differential, CG input stage, CS voltage-gain stage, DC-balanced output buffer
Oh, Park [41] [1], 2007	0.18 µm	96	4.7	72 @ 1.8V	25	76	differential, advanced CG input-stage, TIA gain stage with R_F, DC cancelation stage of f_T doubler type
Wang [37], 2007	0.18 µm	59	8.6	18 @ 1.8V	25	0.87	2-staged with combined series/shunt inductive peaking
Jun-De Jin [36], 2008	0.18 µm	75.0	7.2	91.8 @ 1.8V			6 cascaded CS-stages with PIP
Aflatouni [26], 2009	0.13 µm	57	8	1.8/10.9 @ 1.2V	30	13.7	differential RGC with combined shunt/gate inductor peaking and stacked inductor modeling
Ngo [42], 2010	0.13 µm	50	7.5	4.1	102	0.62	RGC with broadband matching network
Hammoudi [28] [1], 2010	0.35 µm	54.5	2.75	53.5 @ 3.3V	12.76	0.51	3x cascaded stages push-pull inverter with PMOS in feedback
Bashiri [16], 2010	0.065 µm	46.7	21.6	39.9 @ 1.2V	30	0.18	RGC TIA with Cherry-Hooper, inductive feedback/series peaking
Momeni [10], 2010	0.13 µm	62	6.0	98 @ 2.0V	20	0.4	2x parallel identical SFB TIA
Han [43] [1], 2010	0.18 µm	61.2	5.12	18.4 @ 1.8V	11.4	6.2	RGC input stage. CS with capacitive degeneration/active inductor peaking
Atef [44] [1], 2012	0.13 µm	79.5	1.5	4.5/15 @ 1.1V	9	85.6	differential, NC-TIA with 3-stage inverter
Atef [6], 2012	0.04 µm	47	8.0	2 @ 1.1V	22	6.2	inverter with active CD feedback, with single-ended to differential
Liu [45], 2012	0.5 µm	57.6	1.04	73.4 @ 3.3V	18.33	0.28	RGC with resistive feedback from voltage-gain stage, STDC
Escid [29], 2013	0.18 µm	53	9.28		36.12		5x stages inverter TIA with series inductor peaking and resistive feedback
Shahdoost [40], 2014	0.18 µm	75.5	1.62	26.3 @ 2.2V	3.18	42.79	capacitive-feedback, DC current elimination
Atef [11] [1], 2014	0.13 µm	76.8	1.6	47.3 @ 1.8V	26.5	14	SFB CS-based with active inductive peaking
Szilagyi [7] [1,2], 2014	0.028 µm	43	22	2.0/4.2 @ 1.0V	53		RGC with 2-stage feedback amplifier (CG + CS), active inductor, Cherry-Hooper feedback resistor
Shahdoost [21], 2016	0.13 µm	76	1.76	13.7 @ 1.5V	2.67	114.42	capacitive-feedback, DC current elimination
Salhi [8] [2], 2017	0.18 µm	50.8	7.9	7.2 @ 1.8V	7.7	8.79	push-pull inverter with inductive peaking and NMOS in feedback

[1]—simulation or post-layout simulation; [2]—simulated, exact value of C_T is unknown; [3]—single-ended vs. differential.

The discussion shall be, probably, started from the series of works of Toumazou and Park dating back to 90s. In their first works [46,47] (not shown in Table 2) the authors developed a CG TIA with an additional feedback resistor from the output to the drain of the input-stage transistor which gives an additional tuning knob to control the dominant pole of this feedback amplifier. In their later work [34] the authors addressed a problem of TIA's bandwidth and noise performance constraints by using an RGC input stage with the subsequent voltage follower and again the feedback resistor to the drain of M_1. The authors demonstrated the RGC TIA to outperform the equivalent CG solution both in terms of the power consumption, gain and noise. Unfortunately, the original work [34] does not specify the value of the input parasitic capacitance for which the simulation was performed and for the FOM calculation a default value of 0.32 pF was assumed from the previous work of the authors [47]. Furthermore, relatively large overall power consumption along with the moderate gain did not allow this design to achieve high FOM values.

Relatively simple push-pull single stage [8], three [28] or five cascaded stages [29] TIA have been also proposed. In all the cases either NMOS or PMOS devices biased in the triode regions were employed to optimize the noise when replacing a default resistor in the feedback path. The [8] also suggested to use an additional inductor in the feedback path to extend the bandwidth, while the work [29] suggested to use a series inductive peaking before the last inverter stages. Although the nominal performance of these simple designs seems to be good (especially [8]), the simulation results are only presented, and no measurements are provided to confirm the final performance. Furthermore, the inductances introduced significant peaking in the passband which may be not acceptable for OTDR applications and the work does not detail on the PD capacitance used for simulation [8] or even no power consumption and PD capacitance given in [29].

The seminal work of [33] and the subsequent works of Shahdoost employed a CF approach with a CS input stage and a current-divider configuration, where the CS input stage was selected due to superior noise performance as elaborated in [31]. Several practical modifications should have been done compared to a reference design shown in Figure 7. For example, a PMOS current source was applied to the drain of the CS input-stage transistor and biased at the maximum possible gate-source voltage to minimize the thermal current noise. Furthermore, a cascode input stage was designed to improve the noise performance and to compensate for the Miller effect (The cascode eliminates the bandwidth degradation due to the Miller effect of the CS stage's gate-drain capacitance. This degradation is particularly significant in CMOS circuits where the gate-drain capacitance can be as high as one third of the gate-source capacitance. The cascode also enhances the overall gain by increasing the stage's output impedance [4]). While an output buffer with on-chip inductor was added to extend the bandwidth and minimize possible phase distortions in [33], the work [31] employed an inductor-less approach with a source follower. Finally, a specially designed input bias networks have been added to limit the lower end of the amplifier's bandwidth.

Although the approach does not contain an explicit integrator, the voltage amplifier output still follows the integral of the input current. Clearly, such design may be susceptible to instability and saturation problems and may suffer from the intolerance to DC input currents. All this necessitates a DC input current control circuit as was already reported in the original work of Razavi [33] and further elaborated by Shahdoost. Although the results as reported by Shahdoost look extremely promising and have been mostly confirmed by experimental circuits using two different technologies, there may be certain issues that could impede a direct implementation of that circuit for low-power CMOS. Here the major concern is related to the problem of a voltage headroom which can manifest itself for circuits designed to run with lower than 2.2 V supply voltage reported in his most recent work. Furthermore, none of the works of Shahdoost including the most detailed one [21] specified the value of the input and/or PD's capacitance used for simulation and measurement characterization which makes it harder to position the design within the results of competing works as the results reported may be over-optimistic and the circuit performance with actual input capacitances may be significantly worse.

Both works of Razavi and Shahdoost addressed the problem of designing the TIA for optical communications. Different perspectives have been taken in [3], where the authors used the CF TIA to design a low-noise and highly linear TIA for miniaturized magnetic resonance imaging. The authors proposed a modification of the CF TIA where a push-pull buffer stage (see Figure 8) is introduced when compared to vanilla CF TIA [1]. The new approach eliminates the R_D as the current passing through C_1 may be sensed by a low input impedance stage as the current-mode mixer or the V_o can be used for voltage mode operation. According to [3], as the feedback also reduces the output impedance of the circuit, the noise currents of M_1 and M_2 are believed not to have significant contributions to the total noise figures. The push-pull architecture allows larger voltage swings which also help to reduce the input noise current as a smaller capacitance can be implemented for the given maximum value of the input current. According to [3], the push-pull output stage can be also biased with a current smaller than the peak current delivered to the load, resulting in a lower power dissipation without affecting the linearity of the design. On the other hand, this buffer stage increases the capacitive loading of the voltage amplifier. Although this capacitive loading may be still acceptable for lower-frequency operations (generally below 150 MHz) such as MRI in [3], this may be undesirable for higher-frequency applications close to 1 GHz range such as the envisioned OTDR.

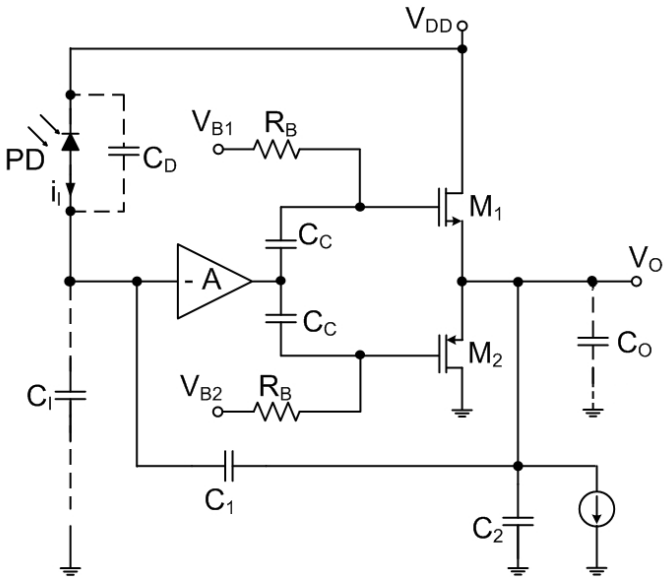

Figure 8. Capacitive-feedback TIA with push-pull buffer stage.

Considering all the trade-offs in CF TIA design, [3] suggested to employ the voltage amplifier with the steering topology as shown in Figure 9. Here the higher voltage gain is achieved by using M_4 to provide 90% of the bias current needed for M_1 allowing implementation of a large R_L, where the noise contribution of M_4 is minimized by biasing it with a large overdrive voltage. The biasing voltage for M_4 is generated by a current mirror while the biasing voltage for M_3 is simply set to the lowest value that keeps the M_3 in the saturation region during the operation. A careful examination reveals that this current steering topology with an additional M_4 device is identical to the solution in the series of works of Shahdoost [21]. Although the approach with push-pull buffer stage demonstrates a promising improvement in the linearity of the TIA, the transimpedance is inversely proportional to the frequency and, therefore, can be hardly used in the proposed form for wideband application such as OTDR.

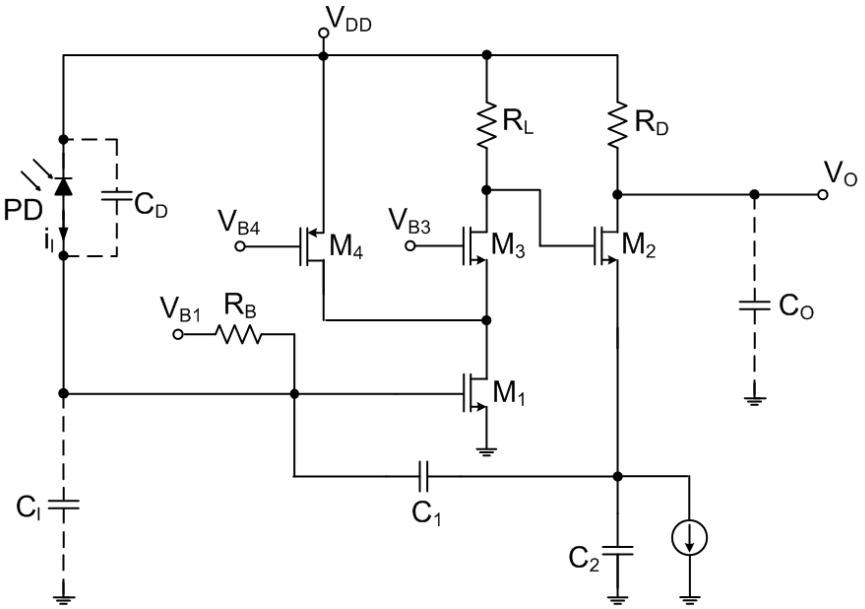

Figure 9. Capacitive-feedback TIA with current steering topology.

Another promising approach was suggested in [44], where a three-stage inverting amplifier TIA was proposed based on a noise-canceling concept (NC-TIA) (see Figure 10). According to the authors, such NC-TIA shows approximately 15% reduction in the integrated input noise current when compared to the traditional three-stage inverter amplifier. Such a limited reduction is caused by the fact that the noise cancelation methods may only cancel the thermal noise and the flicker noise of the input MOSFET but cannot cancel the noise due to feedback resistor R_F. The authors managed to achieve an extremely good sensitivity with the FOM just slightly worse to that reported by Shahdoost.

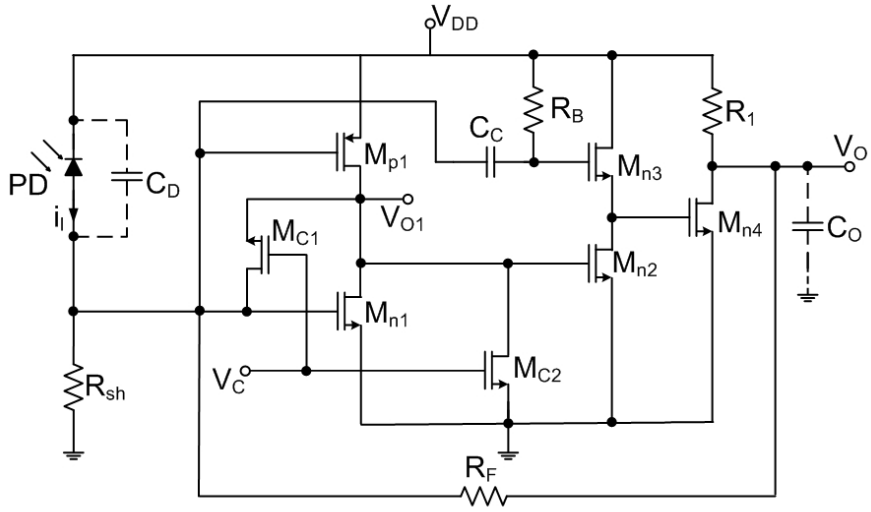

Figure 10. Three-stage inverter TIA with noise cancelation technique.

The work [15] provides one of the early examples of CMOS TIA design, where the CG input stage was selected to relax the trade-off between the bandwidth and the large PD capacitance (2.0 pF for the total input parasitic capacitance including ESD protection pad, etc. for DVI/HDMI applications). The authors have chosen the differential design to eliminate the common-mode noises with the subsequent two-cascaded voltage-gain stages designed as conventional CS differential amplifiers with active PMOS loads. Although the authors did not specifically target low-noise design, relatively poor noise performance of the circuit may again be attributed to the CG input stage. The presented

results are obtained from the post-layout simulation and real circuit performance may have been slightly worse.

Around the same time, the same team also reported on a differential 12-Channel 60-Gb/s transimpedance amplifier array for optical printed circuit boards (OPCB) [41]. The authors exploited again a CG input stage and applied an active feedback technique with negative capacitance compensation to obtain something which is currently known at RGC TIA, where the R_S was replaced by the MOSFET in triode mode. Although a classical CG input stage already has relatively small input impedance, according to the authors in [41] this is insufficient to totally isolate the input capacitance due to poor device characteristics of conventional CMOS. The reported design showed extremely good results in terms of the FOM with the improved mainly achieved due to both increased gain and bandwidth, while the absolute noise figures remained rather poor. As with the design reported in [15], this may be again attributes to relatively week noise performance of the input RGC stage.

Similar RGC TIA was used as a basis in [16], where the Cherry-Hooper technique was used to increase the bandwidth of the amplifier. Such modified RGC with local feedback is claimed to improve the regular RGC design. The authors introduced a feedback circuit (resistor in series with an inductor, see Figure 11) which connects the gate to the drain of M_1 in classical RGC. The modification not only improves the bandwidth of the amplifier, but also partially addresses a problem of the voltage headroom and decreases the input-referred noise. Moreover, a series inductor L_1 had been also added for further bandwidth improvement and noise reduction. The implemented TIA is followed by a three-stage CS buffer with shunt peaking inductors used to enhance their bandwidth and a matching network. Interestingly, the amplifier itself draws only 8.2 mW out of the total power consumption reported for the circuit, while the rest 31.5 mW being consumed by the buffers. According to [16], another important advantage of the approach is an improved biasing of the transistors. In the proposed modified RGC TIA the feedback resistor creates yet another path for the bias current of M_1 through R_B, so that the voltage drop across R_D can be controlled by adjusting the current that flows through R_D. Thus, R_D can be increased to reduce even further the input-referred noise while sufficient DC current is provided to M_1 by this additional path.

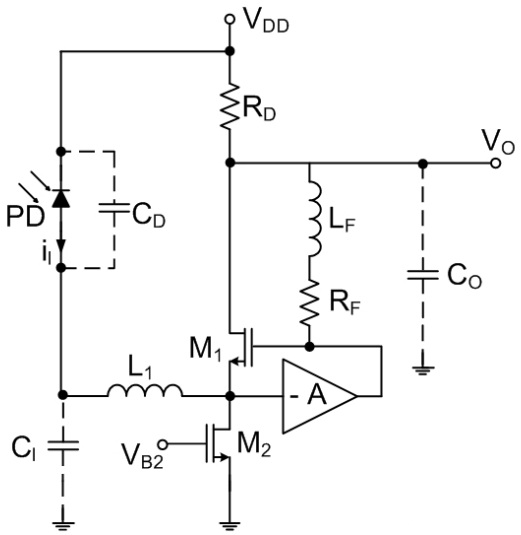

Figure 11. Modified RGC TIA with local inductive feedback (Cherry-Loop technique).

An interesting modification of a classical RGC TIA has been suggested in [6,39], where a low-power TIA (2 mW with a total power consumption including single-ended differential, pre-driver and driver circuits of 16 mW) was designed using an inverter with active common-drain feedback (ICDF) as shown in Figure 12. A new design can be obtained from classical CS-based RGC TIA by replacing both resistors in CG main amplifier and CS local feedback with corresponding PMOS transistors. This inductor-less design allows achieving a large bandwidth of 8 GHz with approximately

28% reduction in current compared to the original RGC design. The impedance of the circuit is significantly lower compared to the standard RGC TIA as the inverter stage, in general, has larger gain than the CS amplifier stage from the conventional approach. The difference between the RGC and ICDF is that RGC outputs from the drain of the CG amplifier with the CS amplifier functioning as a local feedback stage, while the ICDF design takes the output from the inverter amplifier where the input stage operates as a local feedback stage. Hence, the transimpedance gain of the ICDF-TIA is larger than that of the classical RGC TIA designed for the same technology and similar performance constraints such as the same input impedance (see [39] for details). The authors employed low-threshold transistors available in the 40nm CMOS process with the multi-threshold approach simultaneously enabling higher gain and adequate voltage headroom.

On the other hand, the conventional inverter-based TIA can have lower noise than the ICDF-TIA proposed in [39] at the price of smaller bandwidth as the noise contribution due to active local feedback in ICDF-TIA is higher than the noise of the resistive feedback. The authors also show that the ICDF-TIA is also less sensitive to the supply noise when compared to classical RGC TIA. Still, the noise performance seems to remain a major drawback of the proposed design, as it is for classical RGC TIA circuits.

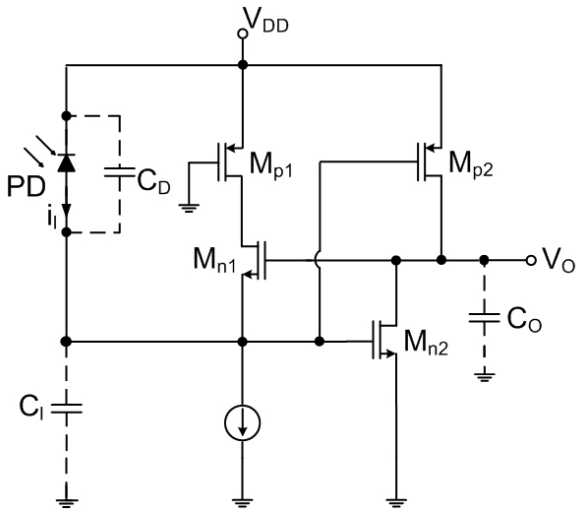

Figure 12. An inverter with active common-drain feedback (ICDF) TIA.

Similar good noise performance was also achieved with a multiple inductive-series technique in [30], where the proposed wideband architecture consisted of the inverter gain stages as shown in Figure 3 with on-chip inductors deployed between them. Here the deployed inductors with the parasitic capacitances resemble a third-order LC-ladder filter to perform an impedance transformation network. Obviously, the technique also allows absorption of the PD's capacitance as a part of the impedance transformation network. The authors also claimed that the series approach manifests larger bandwidth enhancement and less sensitivity to an on-chip inductor quality factor when compared to more classical shunt-peaking techniques [30].

A wideband CMOS TIA based on a combined series/shunt inductive peaking was reported in [37]. The solution consisted of two stages, where the first pre-amplifier stage is a typical SFB TIA based on CS cascode. Here the source follower was used for the unilateral feedback with the post-amplifier composed of the cascode amplifier and the source follower. The shunt inductive peaking was applied to both the pre- and the post-amplifier with the inter-stage inductor inserted to split the capacitance from the transistors.

Further attempts to push the bandwidth of the TIA with inductive peaking have been reported in [9,36,38], where limitations of the classical CS stages have been addressed with the PIP approach (see Figure 13). The works [9,38] reported a TIA for 40 Gb/s applications composed of four cascaded CS stages with identical resistances for drain biasing resistors employed in each stage, while the

input and output impedances are matched through the dedicated matching resistors R_M. It is worth mentioning that the P_D which is also one of the main limitations of the bandwidth in TIA, can also be effectively resonated by the proposed PIP configuration. Although this design provides an excellent gain-bandwidth product and good power consumption, the reported measured results on transimpedance showed significant non-flatness far bigger than 3 dB claimed by the authors. It is interesting to note here that although the design supports extremely large bandwidth of >30 GHz, the computed FOM is rather small. This is caused by relatively small P_D supported by design (50 fF for this high-speed application), moderate gain and relatively high noise. In 2008 a design for 10 Gb/s was reported by the same authors containing six CS stages with PIP. Although the latter design demonstrated an improvement in flatness and operated with P_D of 450 fF, no clear statement on the noise figures was provided.

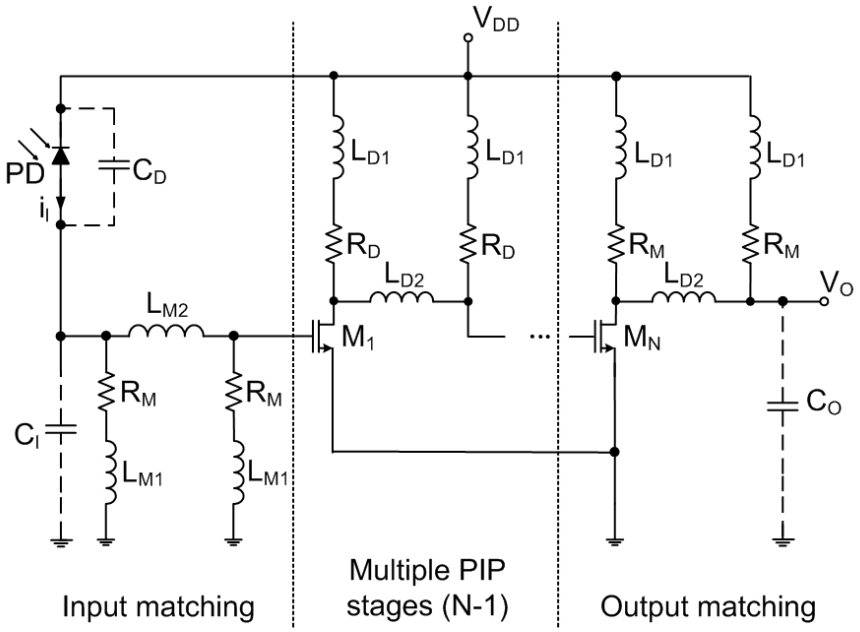

Figure 13. Six cascaded CS stages TIA with PIP.

An interesting design idea had been reported by [26], where a classical RGC TIA was modified to have both the inductive shunt peaking and inductive gate peaking. The vertically stacked coupled inductors have been introduced by the author to enhance the bandwidth via the creation of complex poles. As the stacked inductors allow reduction of the area, the method introduces a relatively large coupling between both inductors and this coupling needs to be considered in the design. The author in [26] also paid additional attention to the stability conditions in such advanced TIA. Unfortunately, even such an optimized architecture resulted in significant chip size compared to inductor-less designs (100 µm × 100 µm), while the noise numbers are also relatively high due to properties of the RGC stage as discussed before. The latter can be partially explained by the increased noise contribution of the M_1 due to the presence of the gate inductor. An advantage of the approach is that the design is relatively insensitive to the quality factor of both added inductors and very thin traces were used to produce high inductance per area to further reduce the chip size.

An attempt to use a broadband matching with classical RGC had been reported in [42], where the matching network included the C_D, the inductance of the bond wire, the parasitic capacitance at the source of M_1 and an additional inductance. Although here again the RGC was responsible for relatively large noise, the work provides a good practical example on how the bonding wire can be exploited as an element of the matching network. Please note that a precise value of the bonding inductance cannot be guaranteed due to the process variations (typically between 0.7 and 2 nH) and

one may need to choose the additional inductance optimally for wider bandwidth with negligible gain peaking.

Even though the inductor peaking results in significant bandwidth improvement for high-speed CMOS TIAs, many works reported on attempts in improving the bandwidth using inductor-less TIA configurations. For example, the work [10] suggested to use N identical TIAs in a parallel configuration to boost the bandwidth while keeping the transimpedance gain constant. Clearly, the same PD and the same capacitance C_D are used to drive this parallel TIA. According to the authors, the assumption of an ideal adder would not significantly affect the results as it can be realized using common-source buffers at the output of each SFB TIA and by adding their currents through a single resistive load. Here the buffers need to have a gain of 1 and, therefore, they can have the bandwidth much higher than the TIA itself. As the number of the parallel TIA increases, the effective damping factor of a combined TIA decreases translating to more ringing in the step response of the amplifier. This overshoot in the time domain corresponds to the peaking in the frequency domain and resembles the effects from the inductive peaking technique as the bandwidth enhancement comes at the expense of an acceptable ringing of the step response. The difference is that while in inductive peaking the bandwidth improvement comes at a price of an extra chip area used for the inductors, in the configuration proposed the power consumption is sacrificed [10]. A clear advantage of the proposed scheme is that it can be used for any TIA topology and the bandwidth enhancement can be achieved for any type of the core TIA. Unfortunately, a higher number of the core TIAs also results in higher input-referred noise so that in lieu of the noise, ringing and the power consumption performance one shall not use more than two or three amplifiers connected in parallel.

If the amplifier is designed for relatively low-frequency applications (e.g., 1–2 GHz) such as OTDR shown in Table 1, not all inductive peaking configurations for bandwidth extension can be useful in practice. For example, if one tries to adopt a simple inductive shunt peaking, the required inductance can be very large unless the load resistor and the parasitic load capacitance are unrealistically small. In conventional shunt peaked (e.g., CS cascode) amplifier with a resistive load the maximum value of the output resistor is limited by the voltage drop across the resistor and the strategy as proposed in [35] allows achievement of a higher gain when using a current source with inductive degeneration (see Figure 14). As a result, a much smaller sized inductor is required when compared to a conventional shunt peaked approach. His approach achieves extremely good noise performance and the noise current density seems to be relatively flat over the frequency as detailed in [35]. Several works have attempted to extend the bandwidth of the classical TIA topologies using the method of so-called active inductor peaking without inductance as shown in Figure 14. A classical RGC TIA with resistive feedback as suggested by earlier works of [34] was used by [45] for designing a 1 GHz CMOS pre-amplifier with active inductor peaking to alleviate possible bandwidth degradation, while the work of [11] instead employed a classical SFB TIA with resistive feedback, where the R_D of the CS stage was replaced by an identical active inductor configuration. Interestingly, the CS-based approach with active inductor load did not show a significant noise improvement when compared to RGC topology. The work [45] also did not report on C_D value used for the measurements and both works employed a single-to-differential converter. It is worth mentioning that the work [11] also adopted rather big C_T of 2 pF to model both the PD with large area suitable for lower-cost plastic optical fibers and significant input parasitic capacitance. According to [11], the configuration not only allowed increase of the bandwidth but also resulted in approximately 15% decrease in noise when compared to classical SFB TIA with CS stage.

A similar active inductive peaking technique in combination with the capacitive degeneration was reported in [43]. The authors employed an input RGC to reduce the input impedance, where an active inductive peaking and capacitive degeneration were used for the CS stage. Here, differently from [11], the authors attempted to reduce the area and the parasitic capacitance of the resistor (see Figure 14 (left)) by replacing the resistor R with a MOSFET. The capacitive degeneration was applied to the source resistor of the CS stage to enhance the bandwidth via generating a zero to compensate the lowest pole.

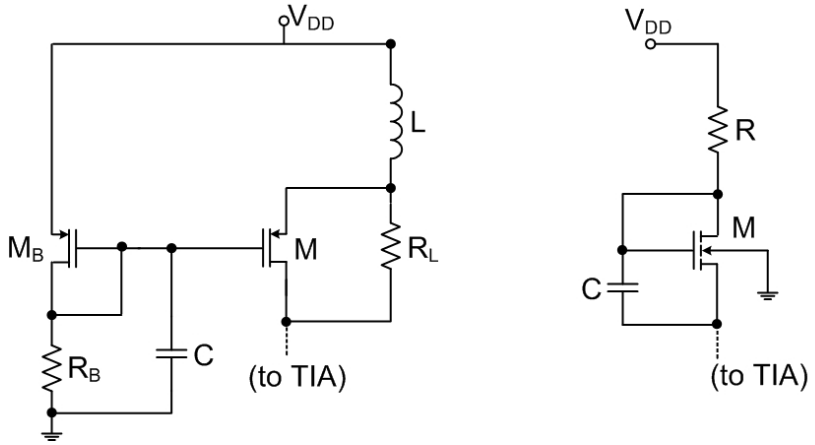

Figure 14. The bandwidth extension with inductive degeneration (left) and an active inductor approach (right).

A combination of several techniques had been suggested in [7] to implement a TIA for 30 Gb/s communication link in 28 nm 1 V CMOS process. The authors addressed the problem by modifying the RGC TIA to have a 2-stage feedback amplifier, where the first CG stage shifts the voltage level at the input of the TIA closer to the supply voltage, while the second high-gain CS stage increases the gain in the loop. As with the previously discussed work [16], here the authors also employed the Cherry-Hooper configuration to reduce the effect of the parasitic capacitance in M_1. Finally, an active inductor is used for bandwidth enhancement. This paper provides an excellent example that several circuit-level modifications of the reference TIA topologies may be needed to achieve the requirement performance with standard CMOS. Unfortunately, the results [7] are provided without including P_D and no FOM may be computed (We cannot assume unknown value and use 0.5 pF as the author explicitly states that the P_D was not included).

The FOM-based performance of the reported CMOS TIA is shown in Figure 15 in the form of dependency on the year the original publication. As expected, the CF TIA from Shahdoost has the highest FOM among the presented works. Please note that the logarithm of the FOM measure is provided and the second-best TIA from Oh [41] is actually 1.5× worse in terms of FOM.

A complementary view on the evolution of the CMOS TIA in terms of suggested FOM is shown in Figure 16, where the reported works are plotted depending on the technology node. A careful inspection of both works reveals that the work of Razavi [33] can be considered to be an outlier in the sense that it seemed to perform better than one would expect from the year and technology. However, this will not be as surprising when one recalls that this was exactly the work which introduced the CF TIA.

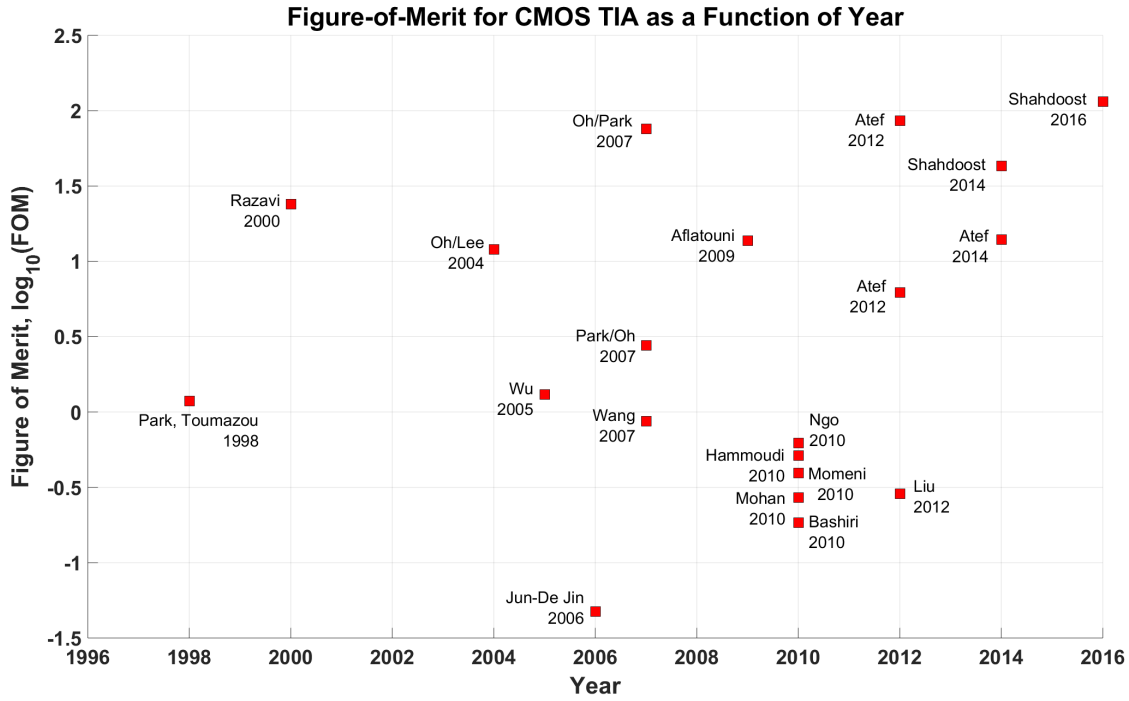

Figure 15. The FOM-based performance of the reported CMOS TIA depending on the year of publication.

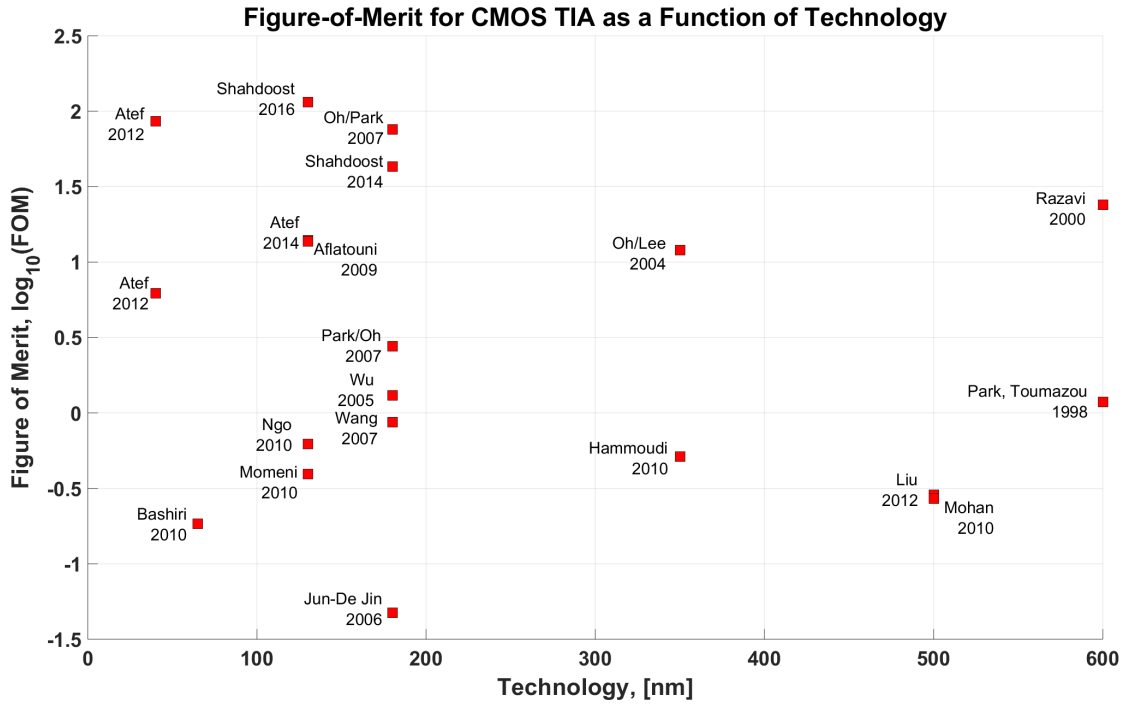

Figure 16. The FOM-based performance of the reported CMOS TIA depending on the technology.

5. Discussion

Obviously, a bigger market of classical optical communication TIAs when compared to very specific OTDR market, resulted in numerous design strategies proposed in last decades for optical communication systems. Although the TIA targeting the OTDR application has rather specific requirements such as low noise and higher linearity, while the TIAs for optical communications are typically optimized for their speed, some of the topologies originally proposed for optical receivers

seem to be applicable to OTDR TIA with modest modifications. Here it becomes clear that it may make less sense to squeeze maximum from classical SFB TIA [12,14] when designing TIA for OTDR, where newer strategies deliver better trade-offs with less design efforts.

Several comments are also necessary regarding an attempt to compare the TIA designs using the presented FOM metric. As has been mentioned before, not all promising publications are detailed enough to separate between the power consumption of the TIA stage and the power consumption of the complete circuit including the voltage followers, output buffer, etc. The same holds for the specification of the C_D which is not always clearly stated or separated from the rest of the input parasitic capacitance (or the latter is completely ignored). In this case, the FOM metric cannot be calculated or, when a default C_D of 0.5 pF is assumed, it may result in the wrong position of the design in terms of FOM metric due missing or insufficiently detailed information. Finally, none of the proposed FOM seems to consider such a parameter as a nonlinearity or the non-flatness of the passband leaving these important parameters beyond relevant performance indicators. Although the FOM metric as defined above seems to work reasonably well for optical receivers in GHz range, its applicability for non-optical applications shall be questioned especially when the FOM is computed for low-frequency application such as MEMS inertial sensors. Please note that while calculating the FOM we are also not separating between single-ended and the differential designs. There are several reasons for this. First, due to the limited number of designs discussed the global view may have been less representative when considering both architectures separately. Secondly, for some of the designs the differential implementations have not been reported.

Despite the limitations of the FOM metrics, some conclusions can be drawn on the general suitability of the reported designs for the intended OTDR application. From the results presented in the previous section is becomes clear that in the context of the OTDR problem the capacitive-feedback approach of Razavi/Shahdoost seems to be one of the most promising candidates for the TIA circuit. Interesting that in the presented capacitive-feedback design it is the ratio of the capacitors which defines the feedback gain and, therefore, they can be implemented also with poly capacitors to be more area efficient and less vulnerable to process variation compared to the absolute value of the RF as used in classical SFB TIA. However, several issues must be addressed for the circuit to fit the specifications. For example, in his early works [31,40] the author did not consider the flatness within the passband (reported peaking in the frequency response less around 1.0–1.5 dB) which may still lead to unacceptable signal distortion in OTDR applications. Furthermore, the series of works of Shahdoost did not report on the input parasitic capacitance nor the value of C_D. Thus, in practice the performance of such as capacitive-feedback approach may be somehow worse if realistic parasitic capacitances are taken into account as this capacitance strongly affect the bandwidth of the amplifier. The voltage headroom problem may also appear to be a challenge for the envisioned TIA design operating at the target 1.8 V.

Similarly, Raman OTDR as used in distributed temperature sensing may also benefit from the flexibility and the advantages of proposed CF TIA design. As the bandwidth requirements for OTDR are relatively low (i.e., below 50 MHz [25]), the designer may benefit from either higher gain or lower noise when compared to the specification discussed in Table 1. Although high gain can be achieved in this case by classical SFB TIA as well, the low-noise property of capacitive feedback may be extremely beneficial for low-cost and low-power integrated solutions where high accuracy in temperature measurements is needed. The complementary requirements of classical and Raman OTDR in terms of the bandwidth may prohibit an effective usage of a single TIA for combined sensing with background compensation as suggested in [23] except very low-cost or lower performance systems.

Some of the promising approaches are not considered due to pure technological reasons. For example, relatively high FOM have been also achieved while using an active inductor as shown [35], where an augmentation of classical broadband cascode topology with an active inductor load allowed achievement of extremely good performance at a price of increased size due to inductor presence. An attractive feature of inductor peaking is that the bandwidth extension may be achieved with no or

minor increase in power consumption, although this may be not as critical for OTDR applications as it is for low-power implantable devices or sensors.

A significant challenge for the OTDR design may be a requirement to implement a variable gain amplifier using the selected architecture when compared to vanilla SFB TIA with resistance feedback network. An interesting observation is that the low-noise capacitive-feedback design from above does not result in extremely low power when compared to advanced RGC strategy or CG TIAs.

Despite an overwhelmingly large number of works reported on CMOS TIA design, relatively few works discuss the effect of process variation on the performance of the designed TIA. A rather exception is the work [11] where a Monte Carlo simulation was performed to model the transimpedance gain and bandwidth. While the standard deviation of the gain was shown to be below 1.5 dbΩ for the input-stage TIA, the standard deviation of the bandwidth was close to 160 MHz which is close to 10% of the nominal bandwidth. Unfortunately, similar information for other topologies is usually missing which does not permit us to evaluate the effect of the process variations on the performance of the design.

6. Conclusions

The TIA front-end is, probably, the most important block in sensor readout or optical communication systems and usually it is the TIA's performance which limits the bandwidth, gain and the signal-to-noise ratio characteristics of the final system. Although due to the cost and integration constraints it becomes more important to implement lower-cost TIAs with CMOS, significant challenges must be addressed in terms of the design to overcome the relevant technological constraints associated with standard CMOS. The report introduces the scope of OTDR application and discusses the application and the requirements of the CMOS TIA for lower-cost integrated OTDR. Here the flexibility of the integrated design allows obtaining of the TIA with desired characteristics overcoming the limitations of the OTDR TIAs built out of discrete components and using classical resistive SFB topology. The work provides a general discussion on the typical topologies used for CMOS TIA and details on a representative set of the recent works reporting advancement in CMOS TIA design. The proposed schemes are compared using a FOM metric and details are provided regarding the circuit implementations and design decisions made by the authors.

A comparative study on these works revealed that the TIA with capacitive feedback can be seen as the most promising candidate for implementation of low-noise CMOS TIA when considering the constraints imposed by the OTDR instrument. The reported results confirm that the topology ensures a sufficient performance to fulfill all the major requirements of the OTDR application such as gain, bandwidth and noise. The circuit avoids usage of on-chip inductors which not only simplifies the design but also makes it possible to fit the chip size constraints imposed by low-cost applications. Furthermore, the sufficient performance margin of the main TIA parameters can be extremely helpful in fulfilling the secondary requirements such as flatness of the response or the linearity. Finally, this architecture is easily amenable to modifications towards reducing the final power consumption.

Still, several challenges must be addressed to implement the TIA for OTDR. First, a requirement of the variable gain imposes a development of a clear methodology for gain adaptation in CF TIA under the rest of the performance constraints. Furthermore, the differential design which is needed for the final circuit may exhibit worse noise performance when compared to the single-ended architecture and further changes may be needed to get the CF differential TIA to fit the OTDR requirements. Even though the original OTDR front-end specification does not impose any constraints on the group delay, the final design may still need to consider those in practice. Finally, some circuit-level innovations may be needed to address a potential problem of the voltage headroom while operating with 1.8 V voltage supply. Clearly, at the end, it is only the actual circuit performance as measured under realistic application condition including all the parasitics is the one which can guarantee that the proposed design fits the intended application.

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Abbreviations

The following abbreviations are used in this manuscript:

ADC	Analog-to-Digital Converter
ADZ	Attenuation Dead Zone
APD	Avalanche Photodiode
ASIC	Application-Specific Integrated Circuits
CD	Common-Drain
CF	Capacitive Feedback
CG	Common-Gate
CS	Common-Source
CMOS	Complementary Metal-Oxide-Semiconductor
DR	Dynamic Range
ESD	Electrostatic Discharge
FOM	Figure Of Merit
MA	Main Amplifier
MEMS	Microelectromechanical Systems
OTDR	Optical Time-Domain Reflectometer
PD	Photodetector
PON	Passive Optical Networks
PSRR	Power Supply Rejection Ratio
RBS	Rayleigh Backscattering
RGC	Regulated Cascode
SAR	Successive Approximation Register
SFB	Shunt feedback
SoC	System-on-Chip
SRS	Spontaneous Raman Scattering
SPDT	Single-Pole Double Throw
TIA	Transimpedance Amplifier

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