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Simplified Modal-Cancellation Approach for Substrate-Integrated-Waveguide Narrow-Band Filter Design

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Abstract: Current substrate-integrated-waveguide (SIW) filter design methodologies can be extremely computational and time-inefficient when a narrow-band filter is required. A new approach to designing compact, highly selective narrow-band filters based on smartly positioned obstacles is thus presented here. The proposed modal-cancellation approach is achieved by translating or eliminating undesired modes within the frequency of interest. This is performed by introducing smartly located obstacles in the maxima and nulls of the modes of interest. This approach is different from the traditional inverter technique, where a periodic number of inductive irises are coupled in a ladder configuration to implement the desired response of an nth-order filter, and significantly reduces the complexity of the resulting filter structure. Indeed, the proposed method may be used to design different filters for several frequency bands and various applications. The methodology was experimentally verified through fabricated prototypes.

Keywords: cavities; communications; filters; substrate integrated waveguide; wave propagation

1. Introduction

The increasing need for higher bandwidth in communication networks calls for systems that can support many frequency bands [1]. For example, modern smartphone networks have continued adding frequency bands to the point where 30 bands are not uncommon [2]. Such networks/systems use filters operating at radio-frequency (RF), microwaves and millimeter-wave parts of the spectrum to select or reject various frequency channels [1]. Rectangular cavities are often used as filters in satellite communication, where low insertion loss and high-power handling capability are required [3,4]. However, filters that rely on rectangular waveguides are large and heavy, which has limited their widespread use in other communication networks. As an alternative, substrate-integrated waveguides (SIWs) have gained popularity due to their high quality, compact size, and power efficiency. Their planar structure allows for easy integration that may lead to full on-chip RF–complementary-metaoxide-semiconductor (CMOS) systems, reducing the amount of material and space needed for electronics. An SIW consists of metal via holes embedded in a planar dielectric structure between two metal layers. Such a structure can be manufactured using standard fabrication processes such as printed-circuit-board (PCB) manufacturing, low-temperature cofired ceramics (LTCC), and nanofabrication processes in the case of a silicon substrate [5–7]. The resulting device can be easily

connected to planar circuits such as microstrip lines and coplanar waveguides (CPW) [8], allowing for the straightforward integration on active circuits.

Traditional filter-design methods, under the assumption of periodicity in the structure, exploit the mapping between network elements and the structure's unit-cell parameters [9,10]. Among these design methods, the K-inverter scheme has dominated the way in which SIW bandpass filters are designed [7,11–13]. For a bandpass K-inverter filter, ladder-configuration metallic irises are used as the LC components of the desired nth-order filter. Once the normalized impedances of the inverters are found, the physical dimensions of the corresponding iris are obtained. Multiple attempts were previously made to simplify the filter-design process, with space mapping being preferred due to its computational and theoretical approaches [14].

Sensing applications, modulation schemes, and a full electromagnetic spectrum require narrow-band filters. Most filter-design methodologies operate conveniently when a broadband filter is required; however, they can result in a complex process for the design of a highly selective filter. In this work, we propose a fast and simple method that intelligently selects transverse-electric (TE) modes to efficiently obtain a narrow-filter response at any desired frequency. Each mode has a set of nulls and maxima inside the SIW. The nulls and maxima for the TE electric modes can be effectively disturbed by the presence of obstacles that can tailor electromagnetic behavior into a desired application [15]. By introducing a limited number of metallic-via holes at the maximal-electric-field locations of the undesired modes and in the nulls of the desired ones, a highly selective narrow-band behavior can be obtained. Using a full-wave simulator, the SIW is discretized into square cells that tell the information of the electric field at the frequency of interest. As the electric modes for each frequency of interest are simulated and extracted, the obstacles can be precisely collocated to give extremely high selectivity. Once an obstacle is added, the SIW is again discretized to define the optimal positions for future obstacles if needed. This approach is fast and efficient if a low-complexity high-quality factor and low-order filters are required.

The remainder of the paper is organized as follows. Section 2 refers to the mode-cancellation technique using smartly placed optimized obstacles. Section 3.1 shows different examples of SIW filters, while Section 3.2 illustrates the experiment results of a primary filter made in FR4 epoxy with an inductive obstacle at its center. Lastly, Section 4 provides some concluding remarks.

2. Materials and Methods

This section describes the implementation model of the proposed narrow-band SIW filter-design methodology.

2.1. Mode Selection

The SIW structure is shown in Figure 1. It consists of top and bottom metal plates with a dielectric substrate in-between. Two parallel rows of metal vias that shortcut both metal layers are located at the edges of the structure. The vias must be shorted to both metal plates to provide vertical current paths. The frequencies of the waveguide modes are given by [16]

$$f_c = \frac{c}{2\pi \sqrt{\epsilon_r}} \sqrt{\left(\frac{m\pi}{L}\right)^2 + \left(\frac{n\pi}{W}\right)^2},$$

(1)

where the effective parameters are assumed (these are air-filled rectangular waveguide width W, length L, thickness H, and dielectric permittivity ϵ_r effectively reduced to a dielectric-filled SIW). Additionally, two conditions are required for the distance between the centers of the vias (pitch) and their diameter to allow wave propagation (higher dimensions result in high power leakage) [17]:

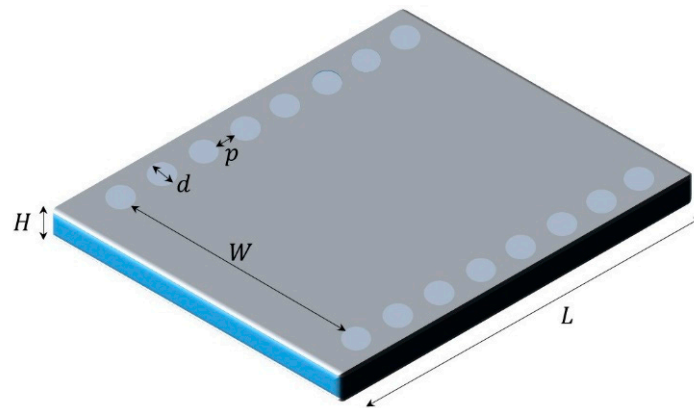$$d < \frac{\lambda_g}{5}, \text{ and } p < 2d.$$

(2)

Figure 1. Schematic showing diameter and pitch of substrate-integrated-waveguide (SIW) metallic vias.

An optimization process is performed several times to match the fence-via radius with the obstacle-via radius. If a microstrip-to-SIW transition is required, one can refer to Appendix A (propagating frequencies may be shifted by the transition introduction).

Since the vertical metal walls of the rectangular waveguides are replaced by rows of vias or via fences for the SIW structures, the modes of both structures are close to each other. Since the fence vias resemble a metallic wall, transverse-magnetic (TM) modes do not propagate. On the basis of multiple-mode response, one can smartly locate obstacles that attenuate all modes except for a desired one. The SIW smart-dimension selection starts with substrate selection (having characteristics ϵ_r and δ). Afterwards, the thickness of the substrate is carefully chosen; an extremely thin structure has high conduction losses and low power capabilities [18]. Mode $TE_{m,n}$ is selected to propagate at f_c with fixed width W and length L that controls the frequency of operation.

Mode $TE_{1,0}$ is usually avoided due to its easy cancellation by any obstacle. Operating under a second mode, $TE_{2,0}$, is usually preferred due to the simplicity of canceling the first- and higher-order modes by locating an obstacle in the center of the SIW. The quality factor of the filter can be enhanced using modal recombination; for this, immediately higher-order mode TE_{m^+,n^+} (m^+ and n^+ are the values of m and n for this mode) is chosen to propagate closely to f_c at f_{c+} (immediately lower-order mode TE_{m^-,n^-} can be used as well). In this case, after fixing W, L must simultaneously solve the previous equation and

$$\frac{c}{2\pi \sqrt{\epsilon_r}} \sqrt{\left(\frac{m^+\pi}{L}\right) + \left(\frac{n^+\pi}{W}\right)^2} - f_c^+ = 0. \tag{3}$$

If a wider band is required, the location can be slightly upshifted. For efficient miniaturization, the diameter of the vias is selected as $d = \lambda_g/40$ and pitch distance as $p = 2d/8$; this guarantees a compact metallic-via fence.

2.2. Mode Cancellation Using Inductive Obstacles

Equivalent wavelength formulations that apply for an inductive obstacle inside a dielectric-filled SIW (value of a is equal to W from Figure 1 when vias are centered) are

$$\lambda = \frac{c}{\sqrt{\epsilon_r} f_c}, \tag{4}$$

$$\lambda_g = \frac{\lambda}{\sqrt{1 - \left(\frac{\lambda}{2a}\right)^2}}. \tag{5}$$

Metallic-via obstacles of a circular cross-section (Figure 2) with an axis parallel to the electric field are modeled as four-terminal resonant (LC) impedance blocks, as stated in [19]

$$\frac{X_a}{Z_0} - \frac{X_b}{2Z_0} = \frac{a}{2\lambda_g}\csc^2\left(\frac{\pi x}{a}\right)\left[S_0 - \left(\frac{\pi d}{2\lambda}\right)^2 - \left(\frac{\pi d}{2a}\right)^2\left(S_0\cot\left(\frac{\pi x}{a}\right) - S_1\right)^2\right], \tag{6}$$

$$\frac{X_b}{Z_0} \approx \frac{a}{\lambda_g}\frac{\left(\frac{\pi d}{a}\right)^2}{1 + \frac{11}{24}\left(\frac{\pi d}{a}\right)^2}, \tag{7}$$

where $-jX_b$ is the reactance for the capacitors, and jX_a is the equivalent reactance of the inductance. These reactances are conditioned to

$$S_0 = \ln\left(\frac{4a}{\pi d}\right) - 2 + 2\sum_{n=3,5}^{\infty}\left[\frac{1}{\sqrt{n^2 - \left(\frac{2a}{\lambda}\right)^2}} - \frac{1}{n}\right], \tag{8}$$

$$S_2 = \ln\left(\frac{4a}{\pi d}\right) - \frac{5}{2} + \frac{11}{3}\left(\frac{\lambda}{a}\right)^2 - \left(\frac{\lambda}{a}\right)^2\sum_{n=3,5}^{\infty}\left[\sqrt{n^2 - \left(\frac{2a}{\lambda}\right)^2} - n + \frac{2}{n}\left(\frac{a}{\lambda}\right)^2\right]. \tag{9}$$

There are two variables of control for the introduced equivalent impedance, radius and position. To simplify filter fabrication, the radius can be fixed to the same one used for the metallic fences. Capacitance $-jX_b$ is fixed, leaving x as the only variable of control for inductance jX_a. After defining the obstacle and evaluating the dimensions for the desired *TE* modes, SIW discretization may start. The SIW is then discretized into square cells $C_{i,j}$ with a side of $d + p$, as shown in Figure 3a.
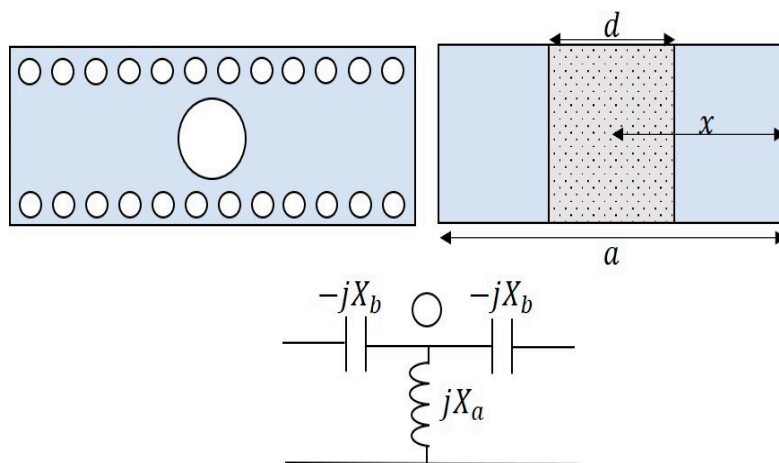

Figure 2. Inductive obstacles: SIW model, cross-section, and circuit equivalent for inductive metal post.

Algorithm 1 Defining frequency-selective obstacles.

Result: Narrow-band filter for desired f_c frequency
1. Select substrate to be used according to ϵ_r and δ.
2. Identify desired mode $TE_{m,n} > TE_{1,0}$ with which to operate.
3. Define diameter of vias and pitch between them for metallic fences.
4. Fix value of width W, and find L for having the desired electric mode.
5. Discretize SIW into $C_{i,j}$ cells.
6. Simulate using Ansys HFSS.
7. Identify CN and CA cells for TE, TE^+, and TE^-.
8. Identify the possible locations of obstacles $C_{i,j}$.
    a. Select maximal number of metallic-via obstacles.
    b. Define diameter for an obstacle, and locate it in a centered C cell.
    c. Validate possible circuit equivalent for the system.
    d. Define a search domain.
    e. Simulate using Ansys HFSS.
        If $CA_{i,j}^+ \neq 0 \vee CA_{i,j}^- \neq 0$, then, to minimize,

                           repeat Steps 6 and 7. If $C_{i,j}$ are limited, then
                           increase the radius of the obstacle(s), or else
                           add new vias in $C_{i,j}'$
                             end
                      else
                             Stop if response is appropriate.
                     end
                        end

         end

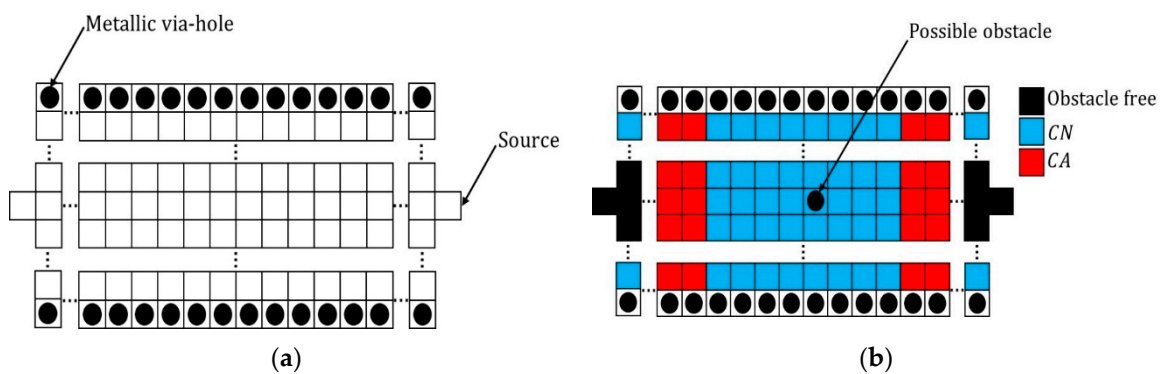9. Optional: design optimized SIW–microstrip transition (Appendix A).

Figure 3. Obstacle location inside SIW. (**a**) SIW discretized into $C_{i,j}$ square cells; (**b**) division of cells inside SIW.

For the desired $TE_{m,n}$, the electric field is obtained for each $C_{i,j}$ cell; each of them is identified in a binary way as

$$C_{i,j} = \begin{cases} CA \text{ electric mode,} \\ CN \text{ electric field null.} \end{cases} \tag{10}$$

In Figure 3b, a third kind of cell is highlighted in black as obstacle-free regions; this is due to the high impedance so close to the source, and that may easily forbid propagation. The role of the obstacles is to act as resonators that couple the energy of only the selected frequencies. A frequency

sweep between $f_c - f_c/4 \leq f \leq f_c + f_c/4$ is then realized after modeling the empty SIW in Ansys HFSS; afterwards, the electric-mode peak frequencies are identified. Frequencies for the neighbor modes of $TE_{m,n}$ are then used as solving frequencies in the simulator. The electric fields inside the SIW are then exported, discretized, and classified as *CA* and *CN*. Assuming that TE^+ is the immediate-neighbor higher mode and TE^- the immediate-neighbor lower mode for TE, common $C_{i,j}$ cells are compared to obtain $C'_{i,j}$ cells that might include obstacle

$$C'_{i,j} = \begin{cases} 1 \ if \ CA^+_{i,j} = CA^-_{i,j} = CN_{i,j}, \\ 0 \ if \ CA^+_{i,j} = CA^-_{i,j} = CA_{i,j}. \end{cases} \tag{11}$$

Subsequently, maximal number of vias $\max(v)$ is selected as the maximal number of obstacles. The obstacles are positioned as individual metallic vias or as compound windows. Because the search area can be extensively high compared to $\max(v)$, we reduced the search domain into the closest nulls near the maxima of interests. The introduced impedance was validated using the LC models for the vias and their position inside the SIW; the distance between components was modeled as transmission lines. Depending on the obstacle array, cavity resonators can be introduced to the SIW. The vias were modeled in Ansys HFSS, and modal cancellation was verified; if the requirements were not satisfied, the number of vias could be increased, or the radius of the existing ones could be altered. Optimetric, a tool from HFSS, can simplify this optimization process. The extraction of the electric field inside the SIW is not straightforward using Ansys HFSS. After a solution is obtained, a nonmodel object must be created; in this case, polylines that represented the desired cells. Each cell was made up of four intersections, each of them giving an electric field; the average electric field was calculated. It was not necessary to discretize the whole design, but just the main areas of interest (nulls and maxima). The summary of the design procedure is stated in Algorithm 1.

3. Results

This section describes the implementation of the previously described algorithms in filter designs for different frequency bands. It finalizes with a fabricated proof of concept in which the dimensions of the filter were correctly optimized.

3.1. Narrow-Band Filter Design

Transmission and reflection parameters S_{21} and S_{11} were used to evaluate the performance of different filters at different frequency bands. The main advantage of this technique is its easy adaptability to any frequency band. The dimensions, structure, and operation of filters for various frequencies were studied according to the following objectives:

1. Multiple transverse electromagnetic modes should be tested.
2. Verify the effect of the microstrip–SIW transition for different modes. For the sake of simplicity, the first filter was modeled as a no tapered SIW–microstrip transition.
3. Different materials were tested using the proposed methodology. Complementary-metal-oxide-semiconductor (CMOS) integration requires the use of silicon (undoped silicon with $\epsilon_r = 11.9$) as the substrate of the SIW devices, while traditional radio-frequency (RF) circuitry uses common FR4 and Rogers substrates.
4. Devices with minimal sizes are always desired; for this, varying thicknesses of silicon were tested for different frequency ranges.

Several filters were designed according to the previous objectives. Three different frequency bands are proposed for validating the methodology through simulations: 28, 5.8, and 3.2 GHz. Silicon, traditional Rogers duroid®, and FR4 were used. Ansys HFSS was used with a PC setup with two processors, Intel Xeon Gold 6130 CPU @2.10 GHz and 128 GB of RAM. Each iteration consisted of running a simulation in Ansys in HFSS and then introducing its results into MATLAB, where the

set of algorithms was executed. Each full-wave simulation took approximately 25 min to complete, while MATLAB identification could take a maximum of five minutes, thus adding to a total of 30 min per iteration. Each design could take approximately eight iterations to complete, leading to a total of 240 min of computational time per design. The lower-frequency filter was optimized to be fabricated in a simple manner by an LPKF s103 PCB maker.

3.1.1. 28 GHz Filter Based on Smart Modal Selection

Millimeter-wave communication is a promising technological direction, as the spectrum is less crowded and higher bandwidth is available. The band around 28 GHz is expected to be massively used under 5G and 6G standards; it is of utmost necessity to design miniaturized filters for this range of frequencies using as few components as possible. A filter operating in the $TE_{4,1}$ mode was analyzed. Rogers 5880 duroid® with $\epsilon_r = 2.2$, $\delta = 0.0004$, and 1.575 mm of thickness with two 18 μm layers of copper is used as the substrate. The filter consisted of a rectangular SIW ($W = 4.54$ mm and $L = 27.55$ mm) with 0.16 mm vias in diameter and a pitch of 0.14 mm. Our mode of interest had its two closest neighbors at 26.24 GHz and 30.05 GHz. The SIW was discretized, as shown in Figure 4, for the three frequencies of interest. The C_N cells of 0.3 mm size were exported from Ansys HFSS. Due to the electric-field configuration of the electric mode, seven inductive obstacles were selected as max(v). After obtaining the null cells, we selected the geometric center of the SIW as the starting point. One obstacle with a diameter of 0.16 mm was positioned in the geometric. The immediate lower-order mode had a strong coupling inside the waveguide; as can be seen after the first obstacle introduction (Figure 5a), modal recombination was preferable.
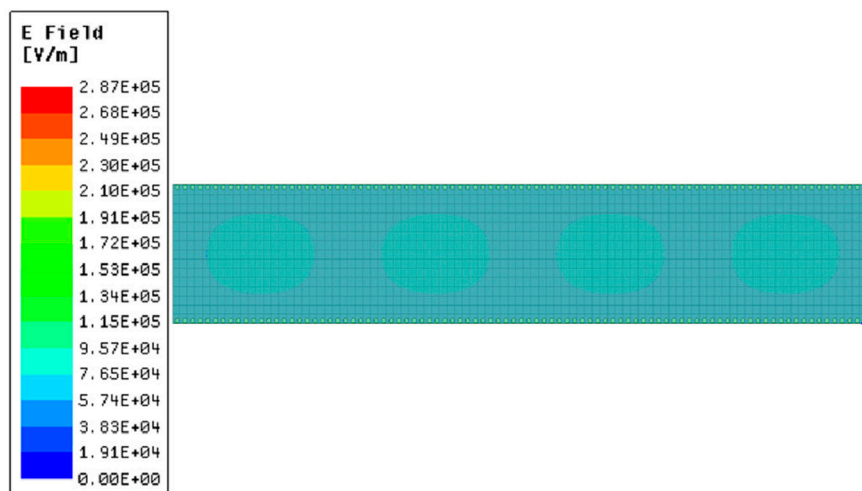

Figure 4. Discretized SIW operating under mode $TE_{4,1}$. Electric field discretized for 28 GHz using nonmodel object cells of 0.3 mm side in Ansys HFSS.

The number of obstacles was increased, and the modal recombination can be seen in Figure 5. Lastly, seven equal vias 0.16 mm in diameter were located symmetrically inside the structure (equivalent impedance shown in Figure 6a). Three vias were located in the center null, while the four others were positioned vertically on the sides. Utilizing the circuit equations (Section 2.2), the MATLAB solver, and Optimetrics from HFSS, the filter was designed to have a narrow-band response with low insertion loss. To obtain the desired behavior, only seven iterations were needed to have a narrow response, that being much faster to converge than other computer-aided techniques [20,21]. The implementation of Algorithm 1 for this 28 GHz narrow-band filter is shown in Algorithm 2. Lastly, the geometry of Figure 6b was selected. The corresponding frequency response performed by HFSS is shown in Figure 6c. The filter had 20 dB matching in the frequency band of 27.90–28.04 GHz with a mean insertion loss of 0.4643 dB. The amount of copper used for the metal layers, and the metallization of the silver used to fill the vias strongly influenced the quality factor of the filter.
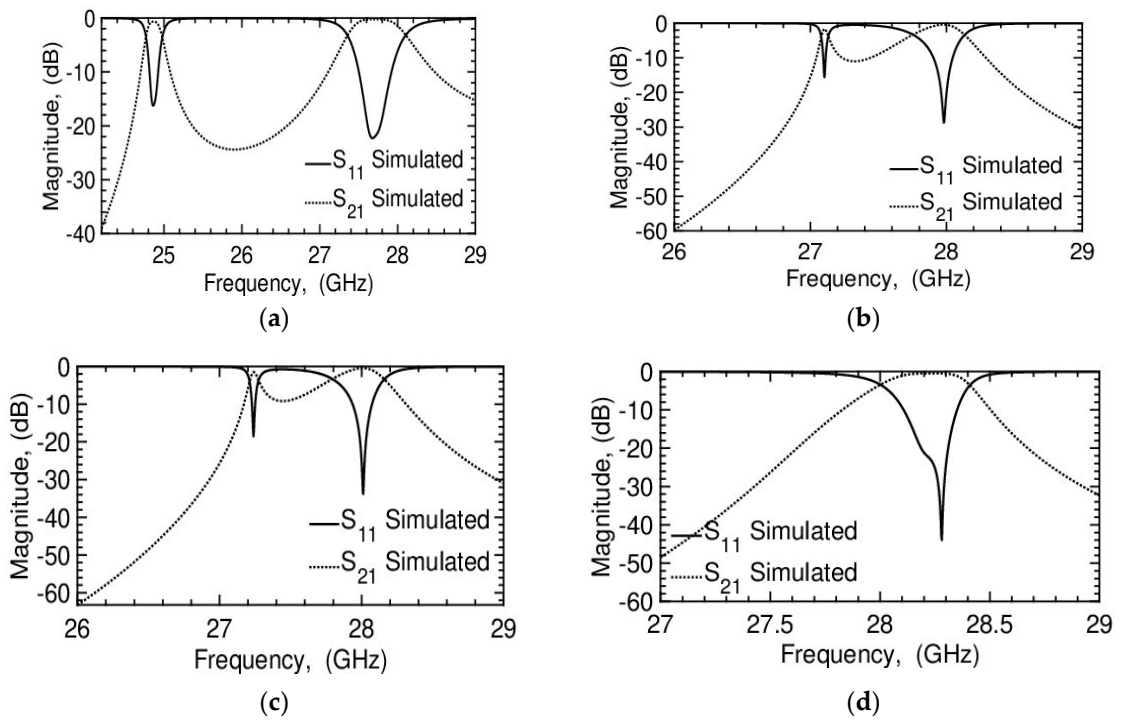
Figure 5. Increasing obstacles for simulated 28 GHz band Rogers 5880 filter: (**a**) one, (**b**) three, (**c**) five, and (**d**) seven obstacle(s).
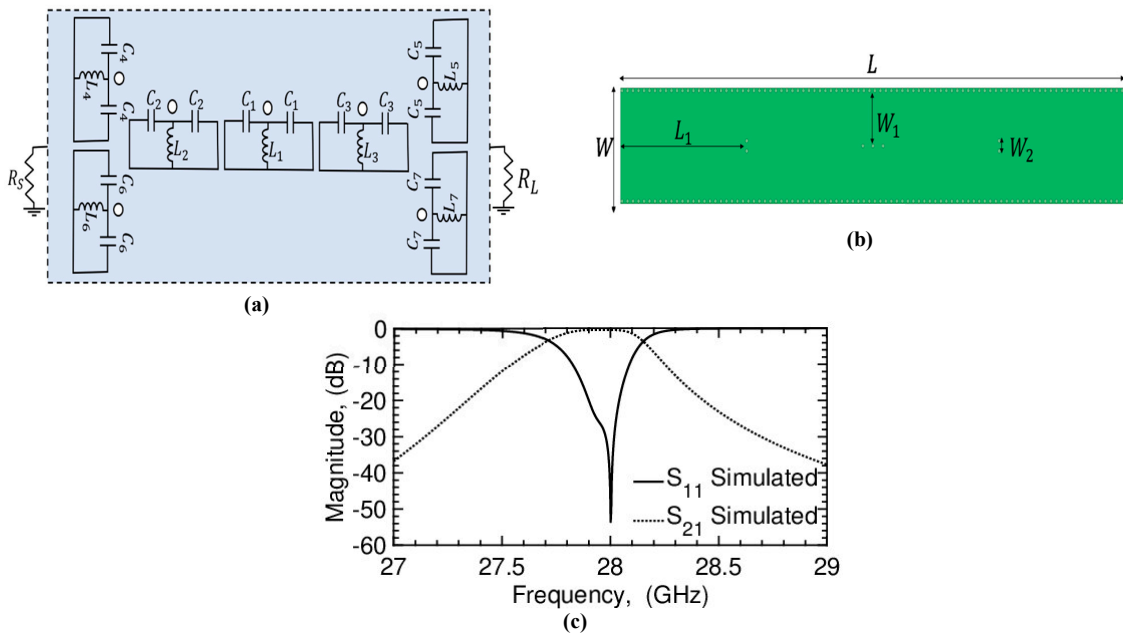

Figure 6. Simulated 28 GHz band Rogers 5880 filter. (**a**) Equivalent circuit for 28 GHz filter. Each via corresponds to an LC four-terminal element. R_S and R_L, equivalent resistance of source and load. (**b**) Schematic of proposed filter: $W = 4.54$ mm, $W_1 = 2.19$ mm, $W_2 = 0.24$ mm, $L = 27.55$ mm, and $L_1 = 6.8875$ mm. (**c**) Simulated S-parameters.

Algorithm 2: Application of Algorithm 1 on the design of 28 GHz narrow-band filter.

Result: Narrow-band filter for desired f_c frequency
    1. Rogers duroid® 5880 with $\epsilon_r = 2.2$, $\delta = 0.0004$, and 1.575 mm of thickness.
    2. Mode TE_{41} selected to resonate at 28 GHz.
    3. Diameters and pitches for vias defined to be 0.16 and 0.14 mm, respectively.
    4. W fixed to 4.54 mm, and L then obtained using Equation (1) and optimized using Ansys HFSS.
    5. Nonmodal polylines added to discretize the filter into a 0.3 mm square mesh.
    6. Simulate using Ansys HFSS.
    7. The four electric maximal centers are located at XY for the mode of interest: [2, 3 mm], [2, 10 mm], [2, 17 mm], and [2, 24 mm]. We define this area as CA.
    8. Variable $\max(v) = 7$; the diameter of the obstacles forced to be 0.16 mm to match the fences.
    9. Start locating vias in the nulls of the mode of interest. The search domain is restricted to the space between each pair of maxima, being the center of these nulls: [6.5 mm, 3 mm], [2 mm, 13.5 mm], and [2 mm, 20.5 mm].
    10. Locate CA^+ and CA^- at 26.24 GHz and 30.05 GHz, respectively, for the search domain.
    f. Validate the circuit equivalent for the system.
    g. Simulate using Ansys HFSS, and obtain the fields for the reduced domain of interest:
If $CA_{i,j}^+ \neq 0 \lor CA_{i,j}^- \neq 0$, then, to minimize,

                repeat Steps 6 and 7. If $C_{i,j}$ are limited, then
                increase the radius of the obstacle(s), or else
                add new vias in $C_{i,j}'$
                  end
              else
                Stop if the response is appropriate.
              end
                end

        end

3.1.2. 5.8 GHz Filter Based on Smart Modal Selection

The sub-6 GHz band is currently one of the most relevant 5G frequency bands; miniaturized SIW topologies are required. Silicon is the primary substrate in existing electronics; having high dielectric permittivity, easier miniaturization is possible in contrast to low-permittivity duroid®. A silicon SIW filter based on $TE_{3,1}$ mode is proposed. The filter includes a tapered transition between the microstrip line and waveguide for smooth field matching. Typical thickness for silicon wafers (400 µm) with $\epsilon_r = 11.9$ is used as the substrate. Thinner silicon wafers would not allow propagation due to high conductivity losses [18]. The bottom and top metallic layers were assumed to be 1 µm thick. The diameter of the vias of the metal fence was 0.271 mm, with a pitch of 0.0678 mm between each. The layout of the proposed filter after discretization is shown in Figure 7 with the tapered transition.

The mode of interest had its closest neighbors at 4.19 GHz and 7.42 GHz. Again, $\max(v)$ was equal to 7. The electric-field configuration for the empty filter at 5.8 GHz showed maxima in the tapered transition. For 4.19 GHz, the maximum appeared in the center of the SIW; however, the electric mode around 7.42 GHz shared different maxima with 5.8 GHz. Modal recombination was mandatory. The only null area where vias could be embedded was in the center of the SIW; any other would attenuate the mode of interest. Eight iterations are necessary to reach proper modal recombination. The obstacles' dimensions and positions were obtained using the equivalent impedance expressions

with MATLAB, and then optimized using HFSS tool Optimetrics. Initially, a wide via of 0.542 mm radius was added at the center of the SIW, thus canceling the lower modes. Including two more vias, the higher mode was downshifted. Lastly, including two vias of 0.1355 mm radius and two of 0.271 mm radius allowed for appropriate modal recombination. The final filter had the equivalent filter in Figure 8a, and its dimensions are shown in Figure 8b. The structure consisted of an SIW–microstrip tapered transition with two cavity resonators constructed by the smart-obstacle position methodology. The filter had a 20 dB matching band of 5.76–5.84 GHz (Figure 8c) with a mean insertion loss of 0.02 dB.
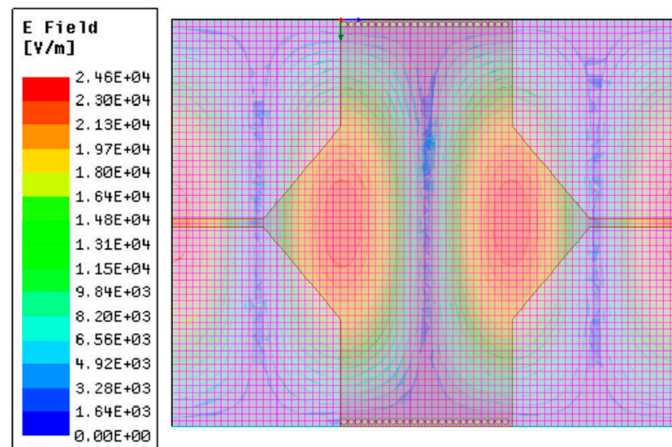
Figure 7. Discretized SIW with SIW–microstrip transition operating under mode $TE_{3,1}$. Electric field discretized for 5.8 GHz using nonmodel object cells of size 0.34 mm in Ansys HFSS.
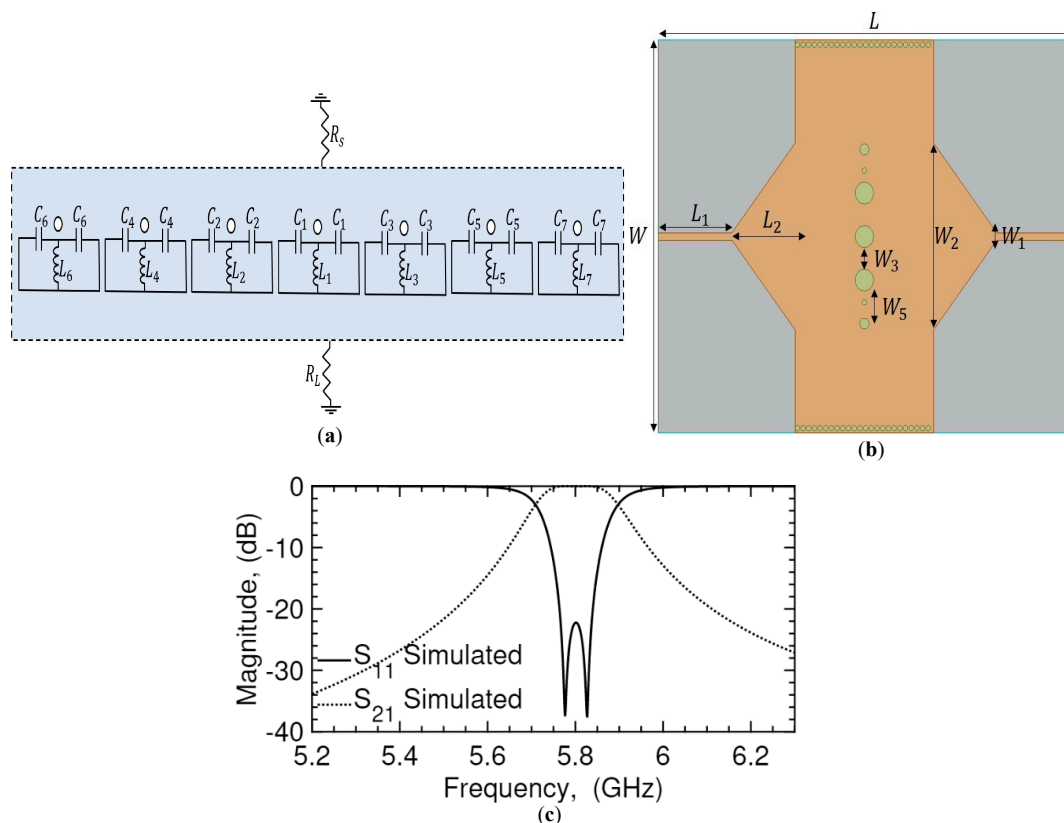

Figure 8. Simulated 5.8 GHz band silicon filter. (**a**) Equivalent circuit for 5.8 GHz filter. Each via corresponded to LC four-terminal element. R_S and R_L are equivalent resistance of source and load. (**b**) Schematic of proposed filter: $W = 19.571$ mm, $W_1 = 0.4$ mm, $W_2 = 9.3$ mm, $W_3 = 1.1$ mm, $W_4 = 1.355$ mm, L = 24.6 mm, $L_1 = 4.4515$ mm, and $L_2 = 3.8$ mm. (**c**) Simulated S-parameters.

3.2. Fabrication and Proof of Concept for 3.2 GHz Filter

A low-frequency 3.2 GHz FR4 filter (having a copper layer of 18 μm and a loss tangent of $\delta = 0.002$) was used to prove the efficiency of a smart selection of the obstacle and its position in the waveguide using the presented methodology. Vias were designed to have a diameter of 1.1 mm and a pitch of 0.61 mm between each of them following the restrictions given by the used LPKF s103. The minimal number of obstacles to be used was selected to show the effectiveness of the methodology after fabrication; a straightforward center-inductive post was optimized using an EM simulator to filter the lower order and higher orders. The dimensions of the tapered transition and the SIW waveguide were optimized to avoid parasitic modes in the band of interest, reducing design complexity (Figure 9a). After PCB fabrication, a silver paste was used to fill the holes. A polishing process was completed to give a smooth and homogeneous finish (Figure 9b). The simulated and measured results of the filter are reported in Figure 9c. Vector network analyzer Agilent N5225A, calibrated using a through-open-short-match (TOSM) method with an output power level of −10 dBm was used for the measurements. The filter exhibited a measured insertion loss of 2.2 dB (compared to 0.2 dB from the simulation) and an S_{11} peak of 57.97 dB (compared to 59.42 dB from the simulation). The −10 dB return loss bandwidth was measured to be between 3.17 GHz and 3.515 GHz, wider in comparison to the simulated bandwidth 3.223–3.402 GHz.
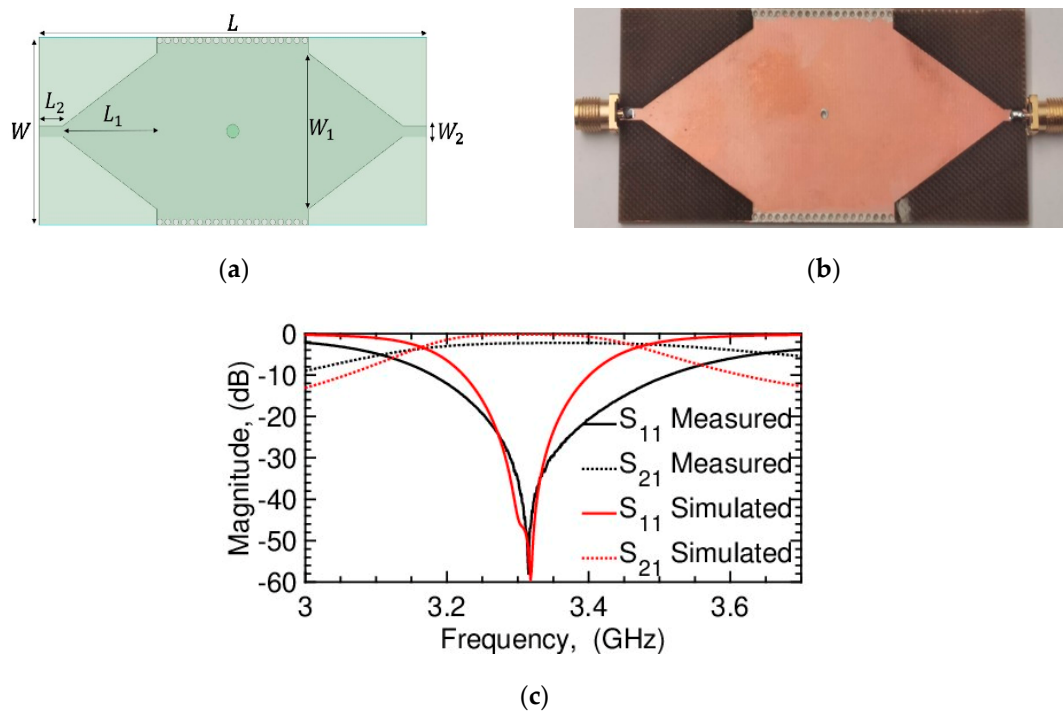

(**a**)   (**b**)

(**c**)

Figure 9. Fabricated filter on FR4 using second-mode TE_{11} approach. (**a**) Schematic of 3.2 GHz FR4 simple narrow-band filter; $W = 36.1$ mm, $W_1 = 30$ mm, $W_2 = 2$ mm, $L = 32.15$ mm, $L_1 = 25$ mm, and $L_2 = 1$ mm. (**b**) Photograph of fabricated filter. (**c**) Simulated and measured S-parameters of proposed filter.

Both the simulation and the experiment verification adequately matched. The small discrepancy in the transmission level could be attributed to the more significant δ loss tangent that the substrate might have, in addition to losses in the connectors (approximately 0.4 dB) and the mismatch introduced by the soldering. Implementing the filter using low-loss RF substrates, such as the Rogers duroid® series, and low-loss connectors could reduce the effect of the insertion losses.

The system showed how a simple structure with a center post made of silver paste is capable of attenuating higher- and lower-order modes without affecting the frequency of interest if it is well-optimized, proving how robust this methodology can be.

4. Discussion

K-inverters have been the traditional approach for SIW filter design. They consist of a set of normalized K-inverter model equations, as shown in Appendix B, where the physical dimensions of a real filter are obtained depending on the chosen order and ripple decay. High-order filters result in complex topologies with a great density of inner vias [22]. Due to the need for designing compact structures, multiple studies have gone beyond this into coupling techniques, space mapping, and composite right–left-handed (CRLH) technology, to mention the most popular.

The performance of several reported filters is summarized and compared in Table 1. Their center frequency wavelength normalizes the physical sizes of the reported filters (λ_0). The filters designed in this work resulted in compact-size filters for cases of 3.2 GHz and 5.8 GHz. The large dimensions obtained for the 28 GHz filter were due to the higher-order mode chosen for its design. All of our filter topologies are simple and straightforward compared to reported designs. We obtained the reported design variables for different frequency structures and compared them with ones used for the designed filters in this work; these variables include any length, diameter, width, pitch, or gap needed to design a device. Using a technique that focuses its operation on the cancellation or translation of undesired electric modes at specific frequency bands has proven to be efficient in the design of low-complexity filters. Filters like the one reported in [23–27] require a high number of internal topologies, increasing the probability of mismatch after fabrication.

Table 1. Comparison of SIW filters. CRLH, composite right–left-handed.

Ref.	Center Frequency	Bandwidth	Topology SIW	Number of Reported Variables	Size ($\lambda_0 \times \lambda_0$)
28 GHz filter using smartly positioned obstacles	28 GHz	0.27 GHz	Single layer—seven inner vias	7	2.57 × 0.42
5.8 GHz filter using smartly positioned obstacles	5.8 GHz	0.2 GHz	Single layer—seven inner vias	11	0.37 × 0.47
3.2 GHz filter using smartly positioned obstacles	3.2 GHz	0.28 GHz	Single layer—one inner via	8	0.12 × 0.14
[23]	3.35 GHz	0.2 GHz	Two sawtooth CRLH	>10	0.12 × 0.09
[24]	5 GHz	0.7 GHz	Modified CRLH	>10	0.37 × 0.25
[25]	6.8 GHz	0.2 GHz	CRLH	>10	0.23 × 0.14
[26]	8.25 GHz	0.33 GHz	Single layer—multiple cavities	>10	1.27 × 1.27
[27]	34.5 GHz	0.86 GHz	Multilayered—multiple slots	>15	0.46 × 0.44

5. Conclusions

The paper described a methodology for the realization of substrate-integrated-waveguide filters at different frequency bands for different types of dielectric substrates. In this study, 3D filters for multiple purposes and requirements were designed, demonstrating the vast possibilities of using simple embedded obstacles inside the substrate to control the propagation modes of the SIW, as first stated for metallic waveguides. The modes were smartly canceled or relocated according to application needs, simplifying the design process while reducing the topology of the filter when a highly selective narrow-band filter is required.

Appendix A

A transition between substrate-integrated waveguide (SIW) and planar circuitry must be included to enable their integration, allowing, for example, a microstrip port to excite the planar waveguide. Multiple SIW-microstrip coupling transitions were proposed [3]. The tapered-microstrip transition is primarily used because it proved to be efficient on a single-layer substrate [6,7]. Compared to a coplanar waveguide (CPW)/SIW transition, this excitation through a microstrip port is simpler to implement. The tapered transition can be optimized to cancel or translate undesired modes. On a thick substrate, such transition might generate radiation loss, which may lead to strong coupling with neighboring integrated circuits. Simultaneous field and impedance matching are essential for the design. The value of taper-width expression W_1 of the Figure A1 schematic, showing an example of an SIW with tapered transition, can be found in [28]. Tapered length L_2 is given by $L_2 = n\lambda_g/4$, $n = 1, 2, 3, 4 \ldots$, and $\lambda_g = c/(f\sqrt{\epsilon_r})$. Length of transition L_1 was optimized, being at least less than $\lambda_g/3$ to avoid any major changes in the dominant mode and to reduce return losses.
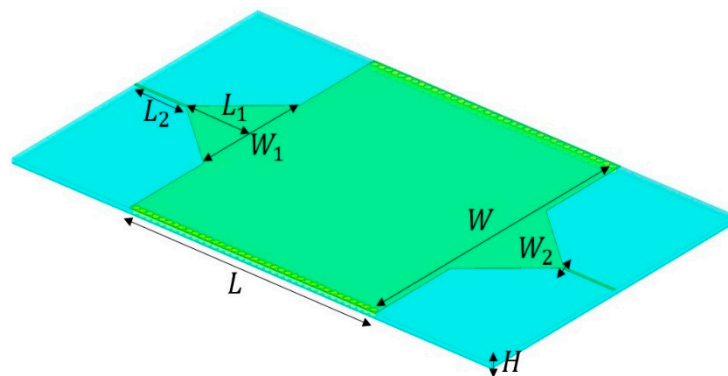

Figure A1. SIW example with tapered transition.

Appendix B

The normalized equations based on the K-inverter technique are [9]

$$\lambda_{g0} = \frac{\lambda_{g1} + \lambda_{g2}}{2}, \tag{A1}$$

$$\omega_\lambda = \frac{\lambda_{g1} - \lambda_{g2}}{\lambda_{g0}}, \tag{A2}$$

$$\frac{K_{0,1}}{Z_0} = \sqrt{\frac{\pi}{2} \frac{\omega_\lambda}{g_0 g_1 \omega_1}}, \tag{A3}$$

$$\frac{K_{i,i+1}}{Z_0} = \frac{\pi \omega_\lambda}{2\omega_1} \frac{1}{\sqrt{g_i g_{i+1}}}, i = 1 : n-1, \tag{A4}$$

$$\frac{K_{n,n+1}}{Z_0} = \sqrt{\frac{\pi}{2} \frac{\omega_\lambda}{g_n g_{n+1} \omega_1}},$$

$$\frac{X_{i,i+1}}{Z_0} = \frac{\frac{K_{i,i+1}}{Z_0}}{1 - \left(\frac{K_{i,i+1}}{Z_0}\right)^2}, \tag{A5}$$

where n is the filter order; λ_{g0}, λ_{g1}, and λ_{g2} are the guided wavelengths at the center frequency and the upper and lower limits; ω_λ is the fractional bandwidth; and g_i is the Chebyshev low-pass coefficient. Using the relationships in [19], normalized inductance jX/Z_0 can be represented into a window iris geometry made by vias. Each iris geometry divides the SIW into cavities with physical lengths:

$$\phi_i = -\tan^{-1}\left(\frac{2X_{i,i+1}}{Z_0}\right), \ i = 0 : n, \tag{A6}$$

$$L_{i+1} = \frac{\lambda_{g0}}{2\pi}\left(\pi + \frac{1}{2}(\phi_i + \phi_{i+1})\right), \ i = 0 : n-1. \tag{A7}$$

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