


Article

High-Speed Rail-to-Rail Class-AB Buffer Amplifier with Compact, Adaptive Biasing for FPD Applications

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Abstract: A high-slew-rate, low-power, CMOS, rail-to-rail buffer amplifier for large flat-panel-display (FPD) applications is proposed. The major circuit of the output buffer is a rail-to-rail, folded-cascode, class-AB amplifier which can control the tail current source using a compact, novel, adaptive biasing scheme. The proposed output buffer amplifier enhances the slew rate throughout the entire rail-to-rail input signal range. To obtain a high slew rate and low power consumption without increasing the static current, the tail current source of the adaptive biasing generates extra current during the transition time of the output buffer amplifier. A column driver IC incorporating the proposed buffer amplifier was fabricated in a 1.6- μm 18-V CMOS technology, whose evaluation results indicated that the static current was reduced by up to 39.2% when providing an identical settling time. The proposed amplifier also achieved up to 49.1% (90% falling) and 19.9% (99.9% falling) improvements in terms of settling time for almost the same static current drawn and active area occupied.

Keywords: buffer amplifier; output buffer; adaptive biasing; FPD application; high slew rate; low power; rail-to-rail; signal range; class-AB; column driver

1. Introduction

The demand for large, high-resolution flat-panel-display (FPD) panels has strong requirements for low-power, high-slew-rate operation for thin-film transistor liquid-crystal display (TFT-LCD) column (data or source) drivers. As display panels need to be larger and have higher resolution, the column drivers of an LCD driving system are becoming important to drive more efficiently large resistive and capacitive loads with low-power dissipation, small area and fast settling time. A column driver of a FPD panel generally includes shift registers, input registers, data latches, level shifters, digital-to-analog converters (DACs) and output buffers with output switches [1–10]. FPD driving systems generally use analog [11–19] or digital driving methods [20,21]. As the display resolution increases, the resistance and capacitance loads of the output buffer increase, whereas the required settling time decreases. The target settling time of the output buffer for the LCD column drivers should be shorter than the horizontal scanning time of the panel [11,12,14–19]. Rail-to-rail class-A, AB or B amplifiers described in [11–19] have been generally used as buffer amplifiers of FPD column drivers. The output buffer amplifier in [11] is used a rail-to-rail input stage and a dual-path push-pull output stage with both class-B and class-AB output sections combined together to improve slew rate. Based on the traditional design in [13], the buffer amplifier in [16] uses several rail-to-rail input stages for 4-bit or 3-bit voltage interpolation with g_m -modulation. When used as an output buffer amplifier, its operation is the

same as that of the buffer amplifier in [13] because several input stages collectively operate as one. The output buffer amplifier in [17] has the same structure as the buffer amplifier in [13], except that explicit output-polarity multiplexer switches are incorporated to improve settling time, and a single differential pair is used as the input stage of the buffer. The output buffer amplifier in [15] was adopted to implement an area-efficient 10-bit DAC by a buffer-reusing method when a large transient driving capability, small static current and compact layout area were required. These buffer amplifiers have their output slew rate proportional to the input bias current. Therefore, the static power consumption increases as the bias current is increased to provide a high-slew-rate performance. To enhance the slew rate without a large static bias current, rail-to-rail, folded-cascode, class-AB buffer amplifiers with dynamic biasing have been proposed [18,19]. However, they have some drawbacks. In [18], the dynamic biasing circuit uses a P-type slew detector for increasing the tail current of the N-type input differential pair of the core amplifier, and uses an N-type slew detector for increasing the tail current of the P-type input differential pair. Consequently, the slew rate can be enhanced, but power and area overheads also become higher. Moreover, since an opposite type of slew detector is used for each input differential pair, the buffer amplifier cannot be fully functional for the entire rail-to-rail input signal range. To address this problem, a modified class-AB output amplifier shown in Figure 1 was proposed [19]. In this buffer amplifier, the dynamic biasing circuit has been modified to allow the same types of slew detectors as the input differential pairs to be used for dynamically adjusting the bias current, resulting in a full slew rate enhancement throughout the entire rail-to-rail signal range. However, unfortunately, the resulting dynamic biasing circuit requires many transistors (as much as 26 transistors). Thus, like [18], it still causes substantially increased power and area overheads. Consequently, a high-slew-rate output buffer amplifier with low-power consumption and a small area is indispensable for the design of TFT-LCD column drivers.

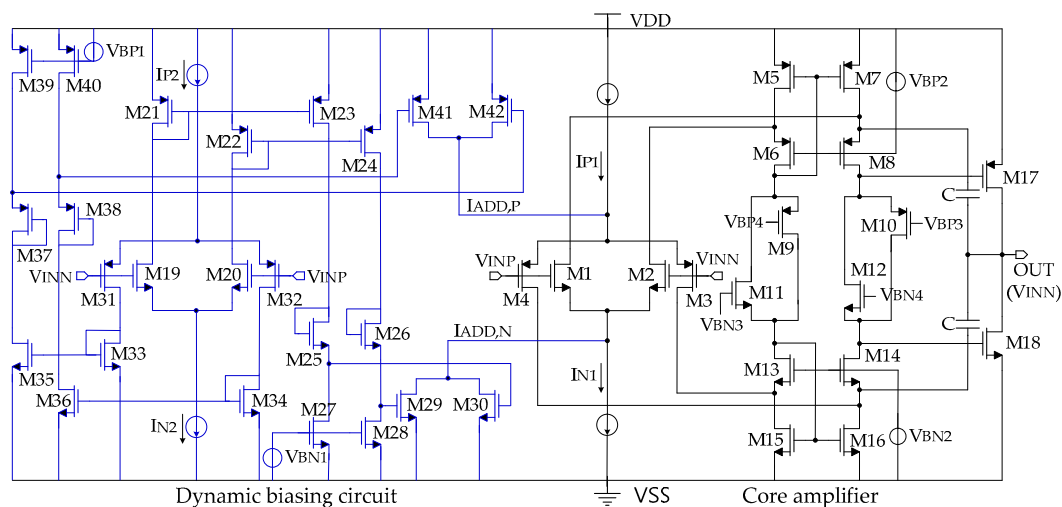


Figure 1. Conventional buffer amplifier with slew rate enhancement for an entire rail-to-rail input and output signal range [19].

To address these issues, a high-slew-rate, low-power, rail-to-rail, folded-cascode, class-AB output buffer amplifier with compact adaptive biasing is proposed in this paper. We present a newly developed output buffer amplifier that requires substantially smaller overheads in terms of power and area to provide an increased slew rate capability. The rest of the paper is arranged as follows. In Section 2, the structure and operation of the proposed buffer amplifier is described with discussion on the advantages of the proposed circuit. In Section 3, evaluation and comparison results are presented based on experimental data measured from a column driver IC incorporating the proposed buffer amplifier. Finally, conclusions are given in Section 4.

2. Proposed Buffer Amplifier

The circuit schematic of the proposed buffer amplifier is shown in Figure 2. It is configured as a complementary differential input stage followed by a floating current source stage for providing a rail-to-rail input common-mode range with class-AB operation as conventional buffer amplifiers do. However, unlike the conventional buffer amplifiers, the proposed buffer amplifier does not use a bulky dynamic biasing circuit having auxiliary differential pairs and multiple current mirrors for slew rate enhancement. Instead, it incorporates just two additional transistors, MP3A and MN3A, as tail current sources of the common source amplifier in the complementary input stage, which are driven by signals, Pu and Pd, driving output driver transistors, MP8 and MN8, respectively. Transistors MP9, MN9, MN10 and MN11 (MN12, MP10, MP11 and MP12) for the current mirror operation of MP3A (MN3A) are used for full slew rate enhancement throughout entire rail-to-rail signal range. MN9 (MN10) is used to reduce the static current by lowering the drain and gate voltage of the current mirror transistors, MN10 and MN11 (MP11 and MP12), and the static current of the common source amplifiers, while MP9 and MN12 act as additional tail current sources. Subsequently, the proposed buffer amplifier combines main tail current sources (MP3 and MN3) and auxiliary tail current sources (MP3A and MN3A) in the input stage for fast transient operation. These auxiliary transistors are sized to be about 40 times smaller than output drivers MP8 and MN8. Moreover, due to the narrow width effect [20], in which the threshold voltage of a MOS transistor is increasing as the transistor width becomes narrower, the threshold voltages of MP3A and MN3A become higher than those of MP8 and MN8 in the steady state. These effects are combined to let the bias currents in MP3A and MN3A be much smaller than those of MP8 and MN8. For example, in our design ($DC\ 8.5\ V = V_{DD}/2 @ V_{DD} = 17\ V$), the sizes of MP3A and MN3A are such that the threshold voltages are made to be 937 and 964 mV, whereas the sizes of MP8 and MN8 are such that the threshold voltages are made to be 808 and 831 mV, respectively, resulting in about 130 mV higher threshold voltages for MP3A and MN3A than those of MP8 and MN8. Now, the bias voltages at Pu and Pd are set at VDD 888 and 910 mV, respectively, so that they are larger than the threshold voltages of MP8 and MN8 and less than those of MP3A and MN3A. This leads to a bias current of about 5 nA for MP3A and MN3A, which is negligible as compared to the bias currents of MP3/MN3 (1.6 μ A), MP5/MN5 (2.1 μ A), MP7/MN7 (2.1 μ A) and MP8/MN8 (5.6 μ A), resulting in almost no increase on overall bias current of the amplifier in the steady state.

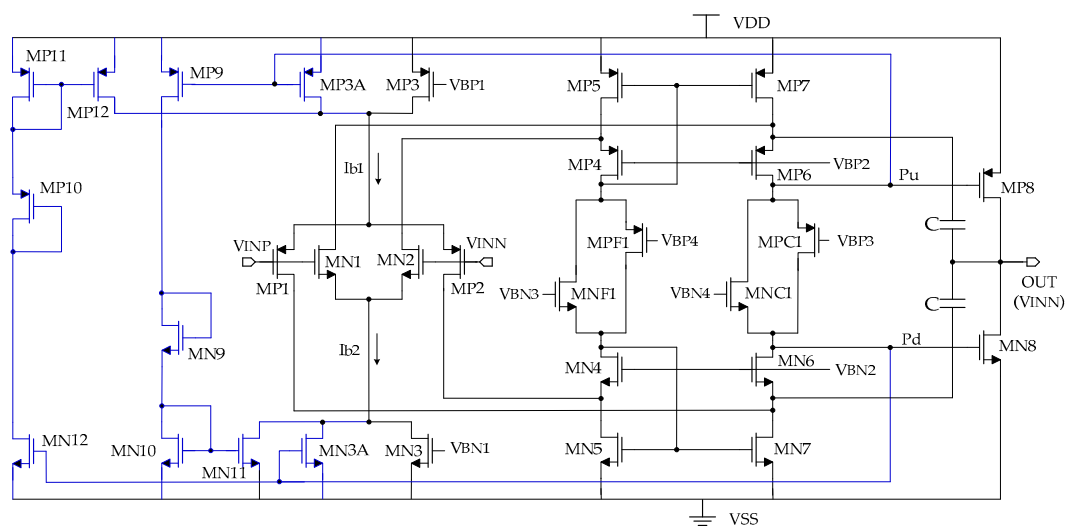


Figure 2. Proposed buffer amplifier with area- and power-efficient slew rate enhancement throughout entire rail-to-rail signal range.

As for the operation principle, when the input has some voltage swing, the voltages at Pu and Pd go up or down depending on input polarity, so the gate-to-source voltages (V_{GS}) of MP3A and

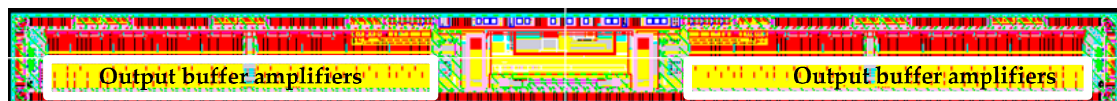
MN3A increase or decrease accordingly. For a very large input voltage difference, the voltage of Pu (Pd) can change from its nominal value to near ground (VDD). Then, the amount of current flowing through MP3A (MN3A) increases substantially, resulting in a larger bias current in the input stage for slew rate enhancement only during the rising and falling transitions of the output buffer amplifier. When the input swing (V_{INP}) is small, Pu and Pd have small voltage changes, so MP3A and MN3A have low current. In addition, when the input voltage swing becomes larger, Pu and Pd have large voltage excursions, so MP3A and MN3A draw a higher current, resulting in a faster transient response. The auxiliary adaptive tail current increases to obtain a faster transient response when the voltage of node Pu is low in the rising transition of the input (output) voltage swing, and the voltage of node Pd is high in the falling transition. The voltage of node Pu offers lower levels and the voltage of node Pd offers higher levels with the larger capacitive load and the voltage swing of the larger input transient. Therefore, the output buffer amplifier has a good driving capability when the capacitive load is larger and the voltage swing of the input transient response is higher.

The proposed buffer amplifier can provide a substantial slew rate enhancement during a full-swing transition for high voltage, as conventional buffer amplifiers do. However, as compared to the conventional high-slew-rate amplifiers in [18,19], the proposed buffer amplifier uses a significantly smaller number of transistors for embodying the slew rate enhancement and is fully functional for the entire rail-to-rail input signal range. Actually, the buffer amplifier in [18] requires 12 transistors to embody slew rate enhancement and is not fully functional for the entire input range. The buffer amplifier in [19] overcomes the input voltage range problem, but requires as much as 26 transistors to achieve high-slew-rate operation. Meanwhile, in the proposed buffer amplifier, just two additional transistors in the complementary differential input stage, which act as extra tail current sources, and eight transistors for configuring current mirrors, are used to provide high-slew-rate operation, resulting in a significant reduction in terms of silicon area and power consumption.

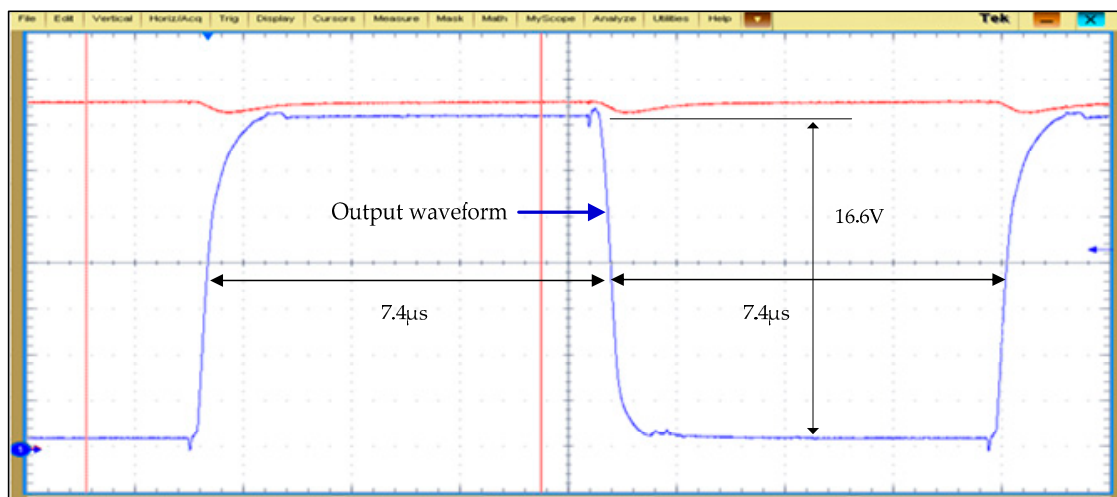
3. Experimental Results

A column driver IC incorporating the proposed buffer amplifier for a large-sized flat-panel-display (FPD) was designed and fabricated using a 1.6 μm 18 V CMOS technology. The layout picture of the column driver IC is depicted in Figure 3a, where the active area occupies $12,685 \mu\text{m}^2 \times 1010 \mu\text{m}^2$. Figure 3b shows that the measured output waveforms for the white pattern (full-swing) in the dot inversion prove a fast transient response of the proposed output buffer circuit. The simulated output waveforms of the conventional buffer amplifiers published in [13,19] and of the proposed buffer amplifier are shown in Figure 4, where the settling behavior can be compared. The conditions for the simulation were that the buffer amplifiers were identically driving a resistance of 8.5 K Ω and a capacitance of 300 pF as the column-line load of a 55-inch TFT-LCD panel at a voltage swing from 0.2 V to 16.8 V. As recognized by the Figure 4, the settling time for rising and falling transitions of the proposed output buffer is much faster than that of [13], and similar to that of [19]. Note that, for achieving this high performance, the proposed buffer amplifier uses far less static current than the conventional buffer amplifier in [19], as seen below (Tables 1 and 2). The performance matrix such as the static current, dynamic current, settling times and active area of the proposed buffer amplifier are summarized and compared with those of conventional buffer amplifiers based on experimental measurement results in Table 1. For some representative ones, the performance comparison in the same process technology is also shown in Table 2, where the simulated and measured data of the proposed buffer amplifier are well matched to each other. As indicated in Table 2, the static current of the proposed buffer amplifier in the 2- g_m region of the input stage where the dc quiescent current consumes the most is reduced from 18.86 μA to 11.44 μA (39.3% reduction) as compared to [19] for providing a similar settling performance. As shown in Tables 1 and 2, the output buffer in [11] has a slower 99.9% slew rate than the proposed buffer amplifier, although the capacitive load is large but the RC load is much smaller. The output buffer in [16] requires a driving voltage higher by 1 V (6%) but has a slower settling time than the proposed buffer amplifier, even though the resistive load is 3.5 K Ω

(41.2%) smaller. The output buffer in [15] has a slower 99.9% settling time than the proposed buffer amplifier, although the RC load is much smaller and the driving voltage is lower. The output buffer in [17] has the same structure as the buffer amplifier in [13], except using output-polarity multiplexer switches and a single differential pair input stage. The buffer has a slower 90% settling time than the proposed buffer amplifier, although the RC load is smaller. As compared to [19], which has an adaptive biasing structure, the active area of the proposed buffer amplifier is reduced from 8401 to 4960 μm^2 (40.9% reduction). As compared to [13], the proposed amplifier achieves up to 49.1% (90% falling) and 19.9% (99.9% falling) improvements in terms of settling time for almost the same static current drawn and active area occupied. The robustness of the proposed scheme against process and temperature variations is summarized in Table 3 using corner simulations at NN 25 °C, FF -30 °C and SS 125 °C. The improved performance of the proposed buffer amplifier comes from the fact that the buffer can achieve the slew rate enhancement much more efficiently using a smaller number of transistors, resulting in a higher area efficiency, lower power consumption and faster settling. The experimental evaluation results presented above imply that the proposed buffer amplifier is applicable to amplifiers with high-slew-rate operations and well suited as a column driver for large, high-definition FPDs.



(a)



(b)

Figure 3. A column driver IC using the proposed output buffer amplifier. (a) Layout picture and (b) measured output waveform of the white pattern ($V_{SS2} +0.2\text{ V}$ (0.2 V)— $V_{DD} -0.2\text{ V}$ (16.8 V)) in the dot inversion.

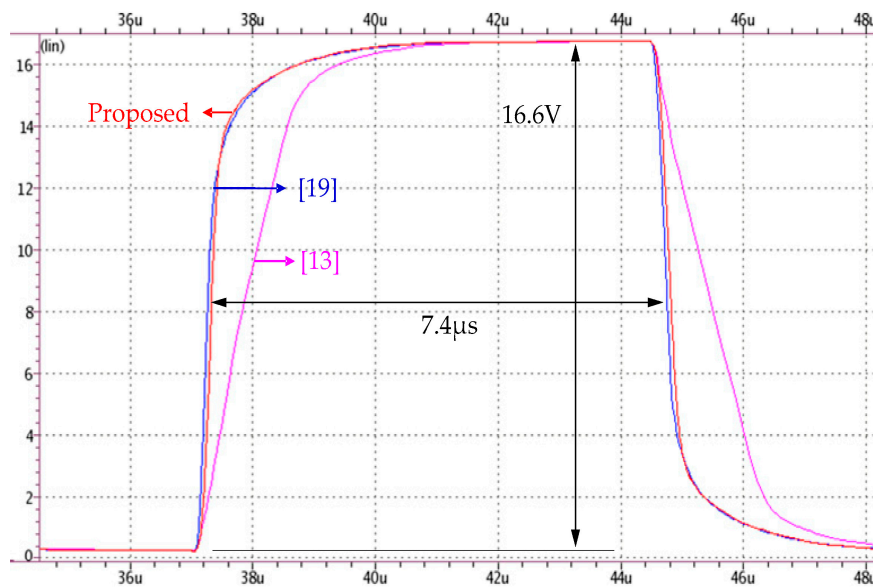


Figure 4. Simulated output waveforms of buffer amplifiers.

Table 1. Performance comparison of buffer amplifiers.

Parameter	[11]	[13]	[15]	[16]	[17]	[19]	This Work
	Measured	Measured	Measured	Measured	Measured	Measured	Measured
CMOS Technology (μm)	0.35	-	0.35 (2P3M)	0.18 (1P4M)	0.18 (1P3M)	0.35	0.18 (1P3M)
Power supply (V)	3	2.5–6	3.3/5	1.8/9/18	1.8/7/13.5	3.3	1.8/9/18
Gray Scale (bits)	-	-	10	10	8	-	8
Static current (μA)	1.63 ¹	180	-	7 ¹	-	5.8	11.40
Driving voltage (V)	3	3.3	5	9/18 ²	10.36	3.3	DC 8.5 @17
Dynamic current (μA)	-	-	-	-	247	-	371
Settling time (μs , 90% rising)	-	-	-	-	1.47	-	0.91
Settling time (μs , 90% falling)	-	-	-	-	1.38	-	0.95
Settling time (μs , 99.9% rising)	1.20 ³	-	5.6	5.6 ⁴	2.61 ³	-	3.11
Settling time (μs , 99.9% falling)	1.02 ³	-	-	-	2.53 ³	-	3.04
Active area (μm^2)	5562	4000	-	23 × 510	-	-	31 × 160
Loads	C = 1000 pF	R = 10 K Ω , C = 10 pF	R = 1.5 K Ω , C = 100 pF	R = 5 K Ω ⁵ , C = 300 pF ⁵	R = 3.29 K Ω , C = 364 pF	C = 200 pF	R = 8.5 K Ω , C = 300 pF
Conditions	VDD = 3 V	VDD = 3.3 V, Ta = 27 °C	VDD = 5 V, 0–4.995 V	VDD = 18 V, 0.2–17.8 V	VDD = 10.36 V, Ta = 25 °C, Period = 7.4 μs , 0.2–10.16 V	VDD = 3.3 V	VDD = 17 V, Ta = 25 °C, Period = 7.4 μs , 0.2–16.8 V

¹ Simulated data. ² 9 V (0–9 V), 18 V (9–18 V). ³ 1.20 μs , 1.02 μs , 2.61 μs , 2.53 μs at 99% rising and falling settling time. ⁴ Target voltage—10 mV (0.2–17.8 V@VDD = 18 V) at the near point of the five-order RC distributed network. ⁵ R and C loads on a five-order RC distributed network.

Table 2. Performance comparison of buffer amplifiers with the same technology.

Parameter	[13]	[19]	This Work	
	Simulated	Simulated	Simulated	Measured
CMOS Technology (μm)		0.18 (1P3M)		
Power supply (V)		1.8/9/18		
Gray Scale (bits)		8		
Static current (μA)	11.42	18.86	11.45	11.40
Driving voltage (V)		DC 8.5 (VDD/2) @17		
Dynamic current (μA)	376.4	415	389.4	371
Settling time (μs , 90% rising)	1.817	1.031	0.989	0.91
Settling time (μs , 90% falling)	1.947	1.022	0.991	0.95
Settling time (μs , 99.9% rising)	3.943	3.416	3.404	3.11
Settling time (μs , 99.9% falling)	4.131	3.377	3.305	3.04
Slew-rate (V/ μs , 90% rising)	8.222	14.490	15.106	16.417
Slew-rate (V/ μs , 90% falling)	7.673	14.618	15.075	15.726
Slew-rate (V/ μs , 99.9% rising)	4.209	4.859	4.876	5.401
Slew-rate (V/ μs , 99.9% falling)	4.018	4.921	5.022	5.526
Active area (μm^2)	31×130	31×271	31×160	31×160
Loads		R = 8.5 K Ω ¹ , C = 300 pF ¹		R = 8.5 K Ω , C = 300 pF
Conditions	VDD = 17 V, Ta = 25 °C, Period = 7.4 μs , 0.2 V–16.8 V			

¹ R and C loads on a five-order RC distributed network.

Table 3. Corner simulation results for the proposed buffer amplifier (8.5 V @VDD = 17 V).

Conditions	Process Parameter	NN	FF	SS
		Temperature (°C)	25	−30
	Compensation cap. (pF)		0.15	
	Loads/Voltage swing/Period	R = 8.5 K Ω , C = 300 pF, 0.2 V–16.8 V, Period = 7.4 μs		
	Open-Loop Gain (dB)	90.22	89.88	83.85
	Phase Margin (degrees)	59.86	63.01	70.89
	Static current (μA)	11.45	14.32	10.78
	Dynamic current (μA)	389.4	525.6	354.8

4. Conclusions

A high-speed, low-power, rail-to-rail, folded-cascode, class-AB output buffer amplifier with an adaptive biasing circuit is proposed. The proposed buffer amplifier uses a compact, novel, adaptive biasing scheme for a slew rate enhancement. To obtain a faster transient response, the proposed adaptive biasing scheme requires just two transistors of the additional tail current sources and eight transistors for current mirrors. These additional transistors can provide a significant amount of extra bias current to the core amplifier during the slewing period while consuming a negligible amount of current during the steady-state period. The proposed adaptive biasing method can be applicable to amplifiers for high-slew-rate operation, and is well suitable for column drivers in large, high-definition FPDs.

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Conflicts of Interest: The authors declare no conflict of interest.

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