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Switched Capacitor Compensation of Supply Distortion in Class-D Amplifiers

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Abstract: This paper presents a switched capacitor technique for bus-pumping compensation in a half-bridge class-D amplifier. The proposed approach, in addition to the almost complete reduction of the bus-pumping effect, allows the half-bridge class-D amplifier to preserve maximum energy efficiency. The studied hardware implementation of the proposed technique demonstrates its advantages of high efficiency, simple circuit, and low cost. The principal design and operating principles are analyzed and described. The experimental static characteristics and time-domain waveforms for the proposed technique are shown to verify its feasibility.

Keywords: class-D; half-bridge; bus-pumping; switched-capacitor

1. Introduction

A class-D output stage in half-bridge (HB) configuration is one of the most used output stages in general-purpose power conversion, especially when the load is in single-ended form. Apart to audio amplifiers [1–7], it can be found in many other applications, including power electronic converters [7–11], power amplifier in grid testing equipment [12,13], as a compensation amplifier in feedback systems [14–17], etc. As a power amplifier, class-D HB is a simple, portable, and space and energy-efficient replacement for a linear class-AB amplifier.

As a configuration, class-D HB has long been matured. In the case of audio amplifiers, all important issues are investigated, and many solutions are proposed. However, for the case of applications in other engineering fields, some problems are still worthy of attention.

One of the problems in HB is known as a bus-pumping (BP) effect [1,7,8,15], which, in audio applications, increases distortion and noise and degrades the sound quality. It arises when the HB stage is supplied with a unilateral power source and when the amount of BP disturbance generated at power supply busses is equal to [1]:

$$\Delta V_{BB} = V_{BB}/(8\pi \cdot f_a \cdot C_a \cdot R_a). \quad (1)$$

In Equation (1), V_{BB} is power supply voltage, R_a is load resistance, C_a is power supply blocking capacitance, and f_a is the frequency of an audio signal.

An alternative to HB output stage is a full-bridge (FB) output stage, which is structurally immune to BP effect. However, for a class-D amplifier supplied by front-end switching power supply, HB is still more used, due to simple circuit architecture, especially for multi-channel amplification [9,10,12,13,18,19]. Additionally, FB is limited to applications in which the load can be differentially driven [1,16].

The most commonly used solutions to this issue are not to eliminate the cause of the problem but to treat the consequences. This kind of solutions perform active techniques, based on feedback and feed-forward compensation, thus achieving noticeable results in the elimination of acoustic noise [5,20–23]. In power electronics applications, as well as in some high power audio applications, hardware methods that directly reduce BP are applied [7,8,24–26].

In some sensor applications, where HB class-D is used as a compensation amplifier, quantities f_a, or R_a approaches to zero [14,15,17]. As a consequence, voltage disturbance on power supplies can be large enough to disable regular operation of the system, or even to damage power stage and other related electronics. Since f_a can be zero, blocking capacitors of any reasonable size are ineffective. Existing hardware solutions are applicable, but they are too complex for portable sensor devices where simplicity and cost efficiency are required.

This paper treats the possibilities of eliminating BP primarily on DC, as well as at low frequencies where the efficiency of blocking capacitors is insufficient. A dissipative solution of BP compensation is analyzed in details as a foundation for non-dissipative switched-capacitor (SC) bus-pumping suppression solution. Based on that analysis, an SC circuit was designed for which it was experimentally determined to possess ability to greatly reduce BP and to preserve energy efficiency of ideal HB class-D amplifier.

2. Power Efficiency of an Ideal Class-D HB Amplifier and the Root of the BP Problem

For the case of AC operation, various analysis of the BP effect can be found in literature. However, it is difficult to find analysis of the DC transfer dependence of supply currents against PWM duty ratio (D). Therefore, simplified derivation of this dependence is performed, which serves as a foundation for rest of discussion.

For that purpose a HB output stage from Figure 1 is considered. DC power supply PS is ideal (bilateral) with output currents i_{SS} and i_{DD}. Gate drive logic is managed with clock CLK of switching period T. It controls ideal MOS switches, turning on M_1 for $D{\cdot}T$ seconds during first part of the switching period, and turning on M_2 for $(1{-}D)T$ seconds during second part of the switching period, where D is PWM duty ratio. Output stage load is represented as a serial connection of large inductance L and small serial resistance R. For simplicity, it is assumed that the time constant of the load $\tau = L/R$ is sufficiently large; therefore, $i_l(t) \to 0$ and $i_L(t) \approx I_L$. As a function on D, load current I_L is equal to:

$$I_L = I_{D2} - I_{D1} = ((1-D)V_{SS} - DV_{DD})/R. \quad (2)$$

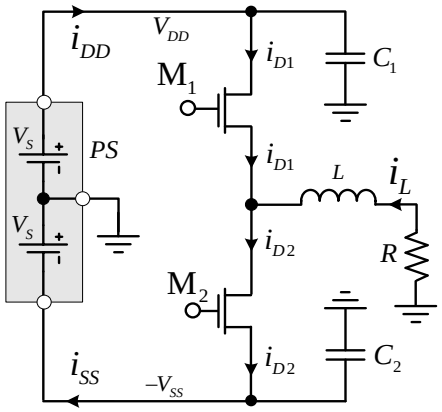

Figure 1. Basic configuration of class-D half-bridge (HB) amplifier without control circuitry. Amplifier output stage is powered by symmetrical supply with voltages $V_{DD} = V_S$ and $-V_{SS} = -V_S$.

By inverting Equation (2), duty factor D can be evaluated as:

$$D = (V_{SS} - RI_L)/(V_{SS} + V_{DD}). \tag{3}$$

For $D = 1$ or $D = 0$, load current reaches maximal possible amplitude:

$$I_{LM} = V_S/R. \tag{4}$$

Using Equation (4), Equations (2) and (3) can be written in more suitable form:

$$D = 0.5 - RI_L/(2V_S) = 0.5 - I_L/(2I_{LM}), \tag{5}$$

and

$$I_L = I_{LM}(1 - 2D). \tag{6}$$

Using Equation (5) and Equation (6), currents I_{D1}, I_{D2} and their sum can be represented as:

$$\begin{array}{l} I_{D1} = -DI_L = -I_{LM}D(1-2D); \\ I_{D2} = (1-D)I_L = I_{LM}(1-D)(1-2D) \\ I_{D1} + I_{D2} = I_{LM}(1-2D)^2 \end{array} . \tag{7}$$

Normalized values I_{D1}/I_{LM} and I_{D2}/I_{LM}, in respect to D, are displayed in Figure 2. It can be seen that current I_{D1} reaches minimum of $-I_{LM}/8$ for $D = 1/4$, whereas current I_{D2} reaches the same minimum for $D = 3/4$.

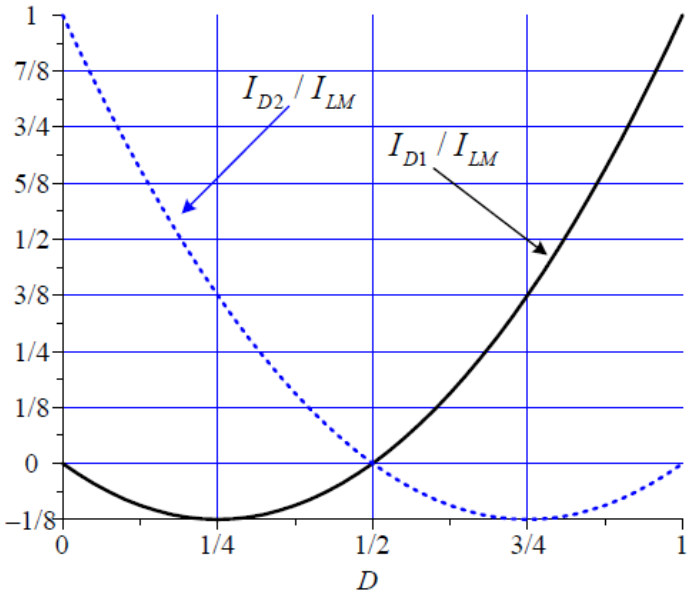

Figure 2. Normalized values I_{D1}/I_{LM} and I_{D2}/I_{LM} with respect to D.

Since $I_{DD} = I_{D1}$ and $I_{SS} = I_{D2}$, precisely one of the supply currents (I_{DD} or I_{SS}) is negative regardless of D. That means that part of the energy, deposited in L during the first part of a switching period, is recuperated during rest of the period. Using Equations (4), (5), and (7), total power consumption P_{tot}, as a function of D is in a form:

$$\begin{array}{l} P_{tot} = V_{DD} \cdot I_{DD} + V_{SS} \cdot I_{SS} = V_S(I_{D1} + I_{D2}) = \\ V_S I_{LM}(1-2D)^2 = RI_{LM}^2(1-2D)^2 = RI_L^2. \end{array} \tag{8}$$

According to Equation (8), the total power delivered by the supply is dissipated only on the load resistance R, so the class-D amplifiers' theoretical power efficiency is optimal.

As a comparison, power consumption of an ideal class-AB power amplifier, with the same supply, and fictive parameter D, is equal to:

$$P_{lin} = |V_S I_L| = R I_{LM}^2 |1 - 2D|. \tag{9}$$

Normalized power consumption as a function of D for previous two cases is depicted in Figure 3.

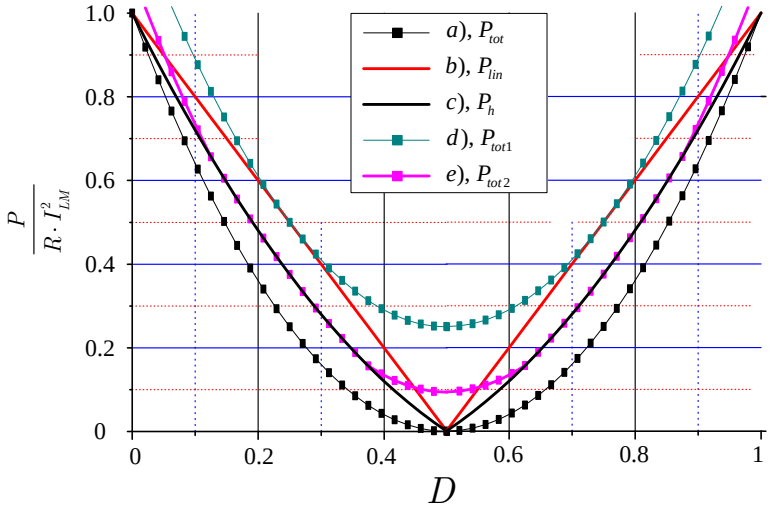

Figure 3. Normalized power consumption as a function of D, for several amplifier realizations: (**a**) HB with bilateral power supply, Equation (8); (**b**) Class-AB power amplifier, Equation (9); (**c**) HB with unilateral power supply and ideal absorption of negative supply currents, Equation (10); (**d**) P_{tot1} Equation (19); (**e**) P_{tot2} Equation (20).

In typical applications, the power supply is usually unidirectional, which can be modeled with ideal diodes D_1 and D_2, Figure 4. Consequently, currents I_{DD} and I_{SS} cannot be negative. For example, if I_{D1} is negative, then I_{DD} is zero, and blocking capacitor C_1 has been charging much over V_S, causing BP effect on V_{DD} bus [15]. A similar effect occurs for negative I_{D2}. Therefore, some countermeasures should be taken in order to prevent such behavior.

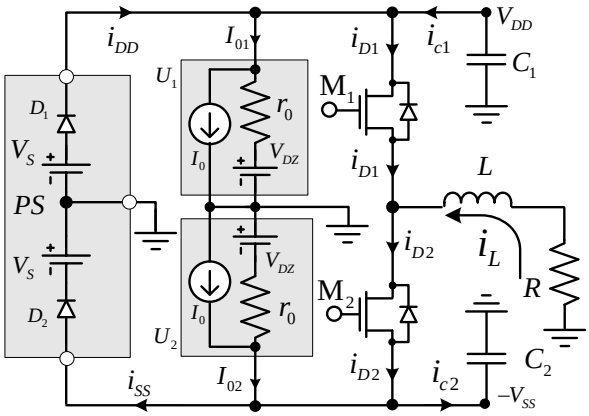

Figure 4. Principal schematic of class-D HB amplifier without control circuitry. An amplifier is powered with unidirectional power supply and augmented with pus-pumping suppression electronics. Capacitors C_1 and C_2 are large enough so that voltages on supply busses can be considered as ripple-free.

If the negative current I_{DD} (or I_{SS}) is entirely dissipated [15], then BP is fully stopped. In that case, only positive current I_{SS} (or I_{DD}) contribute to power consumption, which is described as:

$$P_h = \begin{cases} V_S I_{D2} = R I_{LM}^2 (1-D)(1-2D), & D < 0.5 \\ V_S I_{D1} = -R_0 I_{LM}^2 D(1-2D), & D > 0.5 \end{cases}. \quad (10)$$

Normalized power consumption P_h is depicted in Figure 3. Power consumption for the case (c), Equation (10), is positioned approximately in the middle between ideal case (a) and the power efficiency of class-AB amplifier, case (b).

3. Analysis of a Passive BP Suppression and Impact on Power Consumption

Principal schematic of class-D HB amplifier without control circuitry, powered with unidirectional power supply, and augmented with bus-pumping suppression circuitry, is presented in Figure 4.

Apart to dissipation on R, there is, in reality, an additional dissipation caused by power demands of used electronic components. This dissipation, modeled as current sources I_0 in Figure 4, is usually small and negligibly affects the compensation of negative I_{D1} or I_{D2} [15,16].

With the help of additional passive circuit, modeled by r_0 and V_{DZ}, it is possible to significantly absorb negative I_{D1} or I_{D2} and perform partial or full compensation of the BP effect. For the simplicity, combination of I_0, r_0 and V_{DZ}, inside subcircuits U_1 and U_2, can be replaced by a serial connection of r_0 and voltage source V_0, Figure 5:

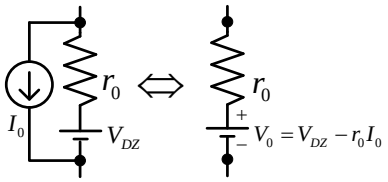

Figure 5. Equivalent representation of subcircuits U_1 and U_2. Typically, voltage source V_{DZ} is made of Zener diode with breakdown voltage V_{DZ}. Subcircuits U_1 and U_2 consume energy and, therefore, are thermodynamically passive.

Without loss of generality, from now on, analysis is limited to $D < 0.5$. For $D > 0.5$, conclusions are equivalent due to symmetry.

Let us assume that size of r_0 is sufficient so that $V_0 + r_0 \cdot I_{01}$ is greater than V_S for some values of D. Then, the V_{DD} portion of the power supply is blocked, $I_{DD} = 0$, and $I_{01} = -I_{D1}$. The voltage on V_{DD} bus is:

$$V_{DD} = \max\{V_S,\ V_0 - I_{D1} r_0\}, \quad (11)$$

while the voltage on $-V_{SS}$ bus is equal to $-V_{SS} = -V_S$. According to Equation (2), current I_L is equal to

$$I_L = ((1-D)V_0 - DV_{DD})/R, \quad (12)$$

and, for the case of $V_{DD} > V_S$, it is satisfied that:

$$V_{DD} = V_0 + DI_L r_0 = V_0 + r_0 D \frac{(1-D)V_S - DV_{DD}}{R}. \quad (13)$$

That means:

$$V_{DD} = \frac{RV_0 + r_0 D(1-D)V_S}{R + r_0 D^2}. \quad (14)$$

For complete interval $0 < D < 0.5$, V_{DD} portion of power supply is equal to:

$$\begin{aligned} V_{DD} &= \max\left\{V_S,\ \frac{RV_0+r_0D(1-D)V_S}{R+r_0D^2}\right\} = \max\left\{V_S,\ V_S\frac{V_0/V_S+(r_0/R)D(1-D)}{1+(r_0/R)D^2}\right\} = \\ &= \max\left\{V_S,\ V_S\frac{\alpha+\beta\cdot D(1-D)}{1+\beta\cdot D^2}\right\} = \max\{V_S,\ V_S\cdot g(\alpha,\beta,D)\}, \end{aligned} \tag{15}$$

where $\alpha = V_0/V_S$, and $\beta = r_0/R$, and $g(\alpha,\beta,D) = (\alpha+\beta\cdot D(1-D))/\left(1+\beta\cdot D^2\right)$.

Since $D(1-D) > D^2$ for $0 < D < 0.5$, if $\alpha > 1$, then $g(\alpha, \beta, D)$ is always greater than 1. Therefore, in order to prevent BP, a necessary condition is that $V_0 < V_S$. Due to symmetry, the conclusion is also valid for U_2.

3.1. Maximal Efficiency–Ideal Dissipative Method

A theoretically "ideal" case arises when $r_0 \to 0$, and $\alpha = 1 + \varepsilon$, $\varepsilon \to 0$. Then, $I_{DD} = 0$ for all values of D in the range $0 < D < 0.5$. Only $-V_{SS}$ portion of power supply delivers energy to the load, which corresponds to Equation (10), and dependence marked as case (c) in Figure 3. In reality, both V_{DZ} and V_S can be decently stable. But, V_S can be intentionally variable, and V_{DZ} is not precise in a simple implementation. So, if it happened that $V_S > V_{DZ}$, then excessive dissipation would occur.

For that reason, simple passive realizations, for example, Zener diode for V_{DZ}, are hardly usable. For performance described by Equation (10), active clamp circuit can be applied, which performs active tracking between V_S and V_{DZ} [15].

3.2. Maximal Simplicity

For a low cost, low supply, or space critical designs, an active clamp circuit proposed in Reference [15] can be inappropriate. Furthermore, due to the negative feedback configuration, in some circumstances, it can face stability issues. Thus, with some lower performance regarding power efficiency, and proper selection of component parameters, the passive alternative from Figure 5 may be used.

For some combinations of β and $\alpha < 1$, and some values of $D < 0.5$, it is satisfied that

$$g(\alpha,\beta,D) = \frac{\alpha+\beta\cdot D(1-D)}{1+\beta\cdot D^2} < 1. \tag{16}$$

Therefore, $I_{DD} = I_{D1}+I_{01}$, and, consequently, $I_{SS} = I_{D2} + I_{02}$. For that case, total power consumption is greater than consumption derived in Equation (10), and, according to Equations (3)–(7), it is equal to:

$$\begin{aligned} P_{tot} &= V_S(I_{D1}+I_{01}+I_{D2}+I_{02}) = V_S(-DI_L+(1-D)I_L+I_{01}+I_{02}) = \\ &= RI_{LM}^2(1-2D)^2 + V_S(I_{01}+I_{02}) = RI_{LM}^2(1-2D)^2 + 2(V_S-V_0)/r_0. \end{aligned} \tag{17}$$

Parameters $\alpha < 1$, and β can be selected for complete suppression of BP effect. In that case, Equation (16) should be satisfied for all values of D, including extreme condition, i.e., for $D = 1/4$:

$$\frac{\alpha+3\beta/16}{1+\beta/16} \le 1 \Rightarrow \beta \le 8(1-\alpha). \tag{18}$$

Minimal consumption is achieved for the equality sign in the previous equation. Then, using $V_0 = \alpha V_S$, and $r_0 = 8(1-\alpha)R$ and Equation (17), total power consumption in respect to D is equal:

$$\begin{aligned} P_{tot1} &= RI_{LM}^2(1-2D)^2 + 2(V_S-V_0)/r_0 = RI_{LM}^2(1-2D)^2 + 2V_S\frac{V_S-\alpha V_S}{8(1-\alpha)R} = \\ &= RI_{LM}^2(1-2D)^2 + RI_{LM}^2/4. \end{aligned} \tag{19}$$

Since $(1-2D)^2 + 1/4 > |1-2D|$ for any value of D, P_{tot1} in Equation (19) is worse than P_{lin} in Equation (9), as in Figure 3. Therefore, regarding power efficiency, the simple passive realization that guarantees BP-free operation is worse than a class-AB case; see Figure 3.

On the other hand, if some BP is allowed, power consumption can be positioned between P_{lin} and P_h:

$$P_{tot2} = \max\{V_S I_{D2}, P_{tot1}\}. \tag{20}$$

For example, if it is allowed that V_{DD} and V_{SS} could race up to $1.1V_S$, then, for $\alpha = 0.53$ and $\beta = 5$, expression $g(0.53, 5, D)$ is greater than 1 in a range of $1/8 < D < 3/8$. In that range, $I_{DD} = 0$, only $-V_{SS}$ portion of power supply delivers energy to the load, and power dissipation complies expression from Equation (10). For $D < 1/8$ or $D > 3/8$, current $I_{DD} > 0$, and power dissipation complies expression from Equation (17). Graphical representation of P_{tot2} for the whole range of D is depicted in Figure 3.

If the application requirements are such that factor D is limited to a narrower range, i.e., $0 < D_{LO} < D < D_{HI} < 1$, and if a particular deviation of V_{DD} from V_S is tolerated, i.e., a small overshoot is allowed, then such a realization is quite competitive to active clamp solution proposed in Reference [15].

However, regarding power efficiency, passive suppression of BP effect cannot provide the full potential of HB topology.

4. SC Compensation of BP Effect

SC techniques have long been routinely migrated from mixed-signal processing to power converter electronics [27–32]. With a simple rearrangement of switches, or by manipulation of frequency and phase of clock signals, SC counterparts of continuous circuits can easily acquire new features that are difficult to achieve in the continuous domain. One of the features is a flexible energy transfer from one part of the circuit to another, which is regularly used in power electronics designs [29–32].

Let us consider circuit from Figure 6, with a BP SC suppression subcircuit. The analysis is performed for $0 < D < 0.5$, while the conclusions for $0.5 < D < 1$ are symmetric and can be deduced from analogy. The SC subcircuit consists of capacitor $C_3 << C_1, C_2$, MOS switches P_1, P_2, P_3, and P_4, and gate-drive logic (not shown on the picture). The gate-drive logic of P_1, P_2, P_3, and P_4 is clocked with a two-phase clock scheme CLK_1 with nonoverlapping phases having duty factor of 0.5. The CLK_1 with frequency $f_1 = 1/T_1$ is physically distinct to CLK. Clock phase φ_1, which is active during the first half of switching period T_1, turns on P_1 and P_2, while P_3 and P_4 are in the blocked state. During the second part of the switching period, clock phase φ_2 is active, and it turns on P_3 and P_4, while P_1 and P_2 are in a blocked state. Therefore, during the first half of the period T_1, capacitor C_3 is connected in parallel with capacitor C_1, while, during the rest of the period, it is connected in parallel with C_2.

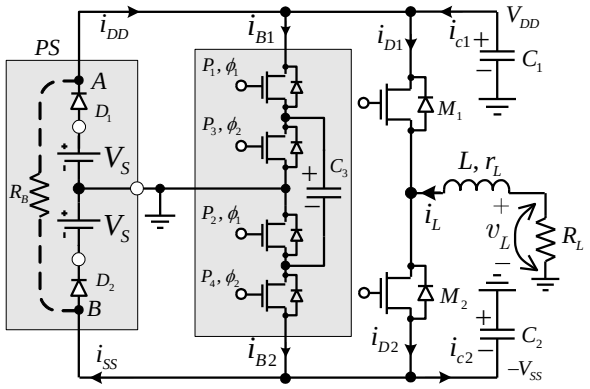

Figure 6. Principal schematic of class-D HB amplifier without control circuitry. The amplifier is powered with unidirectional power supply and augmented with bus-pumping (BP) switched-capacitor (SC) suppression circuit. Resistor R_B is disconnected during regular operation of the amplifier. The total resistance R is the sum of the coil resistance r_L and the load resistance R_L: $R = R_L + r_L$.

4.1. Power Efficiency Analysis

For values of D, which makes V_{DD} greater than V_S, a simplified version of the circuit, from Figure 6, is presented in Figure 7a,b. The current i_{DD} is equal to zero, the V_{DD} portion of the power supply is blocked, and, therefore, it is not shown. On the other hand, $i_{SS} > 0$, maintaining negative supply active, and $-V_{SS} = -V_S$. Since capacitor C_2 is at constant voltage V_S, then $i_{c2} = 0$. Thus, C_2 does not affect circuit operation, so it is not included in Figure 7.

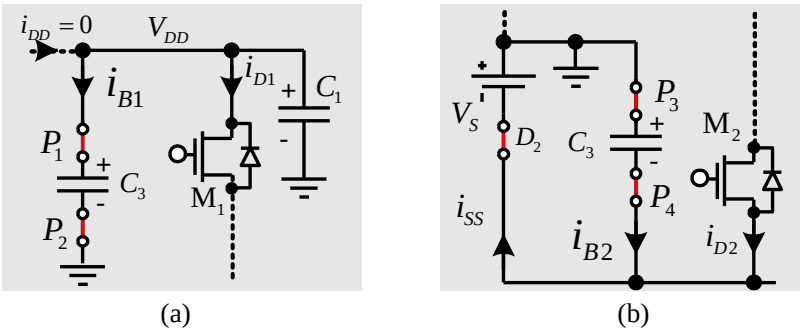

Figure 7. The active part of the BP suppression SC circuit: (**a**) during the first half of switching period T_1; (**b**) during the second half of the switching period T_1.

Figure 7a describes the active part of the BP suppression SC circuit during the first half of the switching period T_1. Switches P_1 and P_2, are closed, and C_3 is connected in parallel with C_1. C_1 is large enough so that voltage V_{DD} can be considered constant over several periods of T_1. Since $C_3 << C_1$, capacitor C_3 is charged to voltage V_{DD}.

Figure 7b describes the active part of the BP suppression SC circuit during the second half of the switching period T_1. Switches P_3 and P_4 are closed; capacitor C_3 is connected to PS and charged to voltage V_S.

Voltage change ΔV_{C3} (1) on capacitor C_3, at the beginning of first half of the period T_1, is equal to $\Delta V_{C3}(1) = V_{DD} - V_S$, thus having the charge flowing through C_3 equal to $\Delta Q(1) = \Delta V_{C3}(1) \cdot C_3$. Consequently, the average value of current i_{B1} during single switching period T_1 is equal to

$$I_{B1} = \Delta Q(1)/T_1 = C_3(V_{DD} - V_S)/T_1. \quad (21)$$

Voltage change ΔV_{C3} (2) on capacitor C_3, at the beginning of second half of the period T_1, is equal to $\Delta V_{C3}(2) = V_S - V_{DD} = -\Delta V_{C3}(1)$. Therefore, the charge flowing through C_3 is equal to $\Delta Q(2) = -\Delta Q(1)$, and the average value of current i_{B2} during single switching period T_1 is equal to $-I_{B1}$. According to Figure 7a, it is fulfilled that $-I_{B1} = I_{D1}$, from which it follows that $I_{B2} = I_{D1}$. Since $I_{SS} = I_{B2} + I_{D2}$, it follows that $I_{SS} = I_{D1} + I_{D2}$, and total power consumption is equal to $P_{tot} = V_S(I_{D1} + I_{D2})$. The obtained result confirms that P_{tot} is the same as in the ideal case and that applied SC circuit provides maximum consumption efficiency of the class-D amplifier.

4.2. BP Analysis

Based on Figure 7 and Equation (21), it can be seen that the SC circuit behaves as the circuit from Figure 5, where V_{DD} bus is connected via SC equivalent resistor $r_0 = T_1/C_3$ to the generator $V_{DZ} = V_S$ and that $I_{B1} \Leftrightarrow I_{01}$

$$I_{B1} = \frac{V_{DD} - V_S}{T_1/C_3} = \frac{V_{DD} - V_S}{r_0} = I_{01}. \quad (22)$$

Therefore, for BP analysis, circuits from Figures 4 and 5, together with corresponding Equations, can be used.

If we neglect I_0, then $V_0 = V_{DZ} = V_S$, α =1, and BP effect occurs for full range 0 <D < 0.5:

$$V_{DD} = V_S \frac{1 + \beta \cdot D(1-D)}{1 + \beta \cdot D^2} > V_S. \quad (23)$$

Contrary to dissipative BP suppression, SC equivalent resistor r_0 can be arbitrarily small. Therefore, BP effect can be made negligible. For example, if β = 0.5, maximum voltage on V_{DD} bus is achieved approximately at D = 1/4 and is equal to:

$$V_{DD} = V_S \frac{1 + 0.5 \cdot 3/16}{1 + 0.5 \cdot 1/16} = 1.06 V_S. \quad (24)$$

In practical realizations, there is always a small current I_0, which causes the current I_{DD} to be greater than zero during a small part of the period T. Still, this fact does not change the essence of the conducted analysis.

4.3. Dynamical Behavior

Due to the existence of the zero-order hold effect, SC circuits are well equivalent to their continual counterparts up to ≈1/10 of the sampling frequency [27,28]. From that side, proposed SC compensation of BP effect is useful to at least 1/10 of $f_1 = 1/T_1$. With the current state of technology, sampling frequencies can routinely go over 50 kHz, so that blocking capacitors solve the BP problem easily at f_1/10. As an illustration, we may consider the following "worst-case" example. Let us assume that the sampling frequency of the SC BP suppression circuit is f_1 = 10 kHz. Thus, we can pessimistically consider that over f_1/10 = 1 kHz SC circuit is ineffective regarding BP suppression. Furthermore, let us assume that class-D amplifier has the following parameters: R_a =1 Ω, and C_a = 4.7 mF. At $f_1/10 = f_a$ = 1 KHz, according to Equation (1), $\Delta V_{BB}/V_{BB}$ = 1/(4.7·8π) = 0.0085, which is below 1%. Therefore, if usual switching frequencies are used, modeling performed in the paper is sufficient for accurate prediction of the dynamical behavior of the proposed SC BP suppression method.

When frequencies below f_1/10 are observed, the transient behavior of the voltages v_{DD} and v_{SS} is defined by the time constants $\tau_{DD} = r_0 \cdot C_1$ and $\tau_{SS} = r_0 \cdot C_2$. For the case of positive supply bus, when diode D_1 is blocked, and R_B is disconnected, as in Figure 6, Unit-step response of the voltage v_{DD} is in the form

$$S_{DD}(t) = 1\ [\mathrm{A}]\ \cdot r_0(1 - e^{-t/\tau_{DD}}) \cdot \mathrm{u}(t), \quad (25)$$

where u(t) is Unit-step function, and assumed excitation is current i_{D1}. The same equation is valid for a negative supply bus. It can be seen that the worst case is on DC and that the purpose of the dynamic behavior analysis can only be to optimize the values of the blocking capacitors C_1 and C_2.

4.4. Experimental Verification

Previous derivations regarding power consumption and suppression of BP effect are verified using experimental setup based on Figure 6. Power source PS is configured as ±12 V desktop power supply modified with diodes D_1 and D_2 (MUR1045), which gives final output voltage as $\pm V_S \approx \pm 11.5$ V at 0.5 A load and load regulation of 0.6 V/A. When needed, the bilateral power supply is simulated by adding a blinder resistor R_B = 215 Ω between nodes A and B, as in Figure 6, so that currents I_{DD} and I_{SS} could flow in both directions. The current through R_B has a negligible effect on the load regulation; it does not affect I_{DD} or I_{SS} and is not covered by the measurements. Measured electrical quantities are I_{DD}, I_{SS}, V_{DD}, V_{SS}, and I_L in a range of 0.05 < D < 0.95. For each pair of MOS transistors, and an accompanying gate driving logic, one-half of each of the three different L6202 is used. Capacitors C_1 and C_2 have values of 1000 μF. Quiescent supply current for D = 0.5 is $I_0 \approx 20$ mA, giving power consumption at rest as

$$P_0 = 2V_S \cdot I_0 = 460\ \mathrm{mW}. \quad (26)$$

Used load is made of coil with L = 50 mH, r_L = 5.3 Ω, and resistor R_L = 10 Ω, which gives $R = R_L + r_L$ = 15.3 Ω. Switching periods are $T_1 = T$ = 100 μs. For a set of different C_3 values, the calculated characteristic quantities, used in paper equations, are given in Table 1. V_{DD} supply bus voltage is calculated for D = 1/4, which is near the extreme value for both V_{DD} and V_{SS}.

Table 1. Characteristic quantities r_0, V_0, α, β, and extreme values for V_{DD} and V_{SS}.

C_3 [μF]	$r_0 = T_1/C_3$ [Ω]	$V_0 = V_S - I_0 \cdot r_0$ [V]	α	β	Max{V_{DD}} at D = 1/4, Equation (15) Max{V_{SS}} at D = 3/4 [V]	Time Constant $C_1 \cdot r_0$ [ms]
2.07	48.3	10.53	0.916	3.157	14.48	τ_1 = 48.3
5.16	19.4	11.11	0.966	1.267	12.83	τ_2 = 19.4
10.3	9.7	11.31	0.983	0.635	12.19	τ_3 = 9.7
24.3	4.1	11.42	0.993	0.269	11.80	τ_4 = 4.1

Measured supply voltages V_{DD} and V_{SS} for the selected set of C_3 values, as well as calculated supply voltages based on Table 1, are given in Figure 8. Measured voltages are presented as line charts, whereas calculated voltages are presented as symbol + line charts. The picture shows a good agreement between experiment and theory.

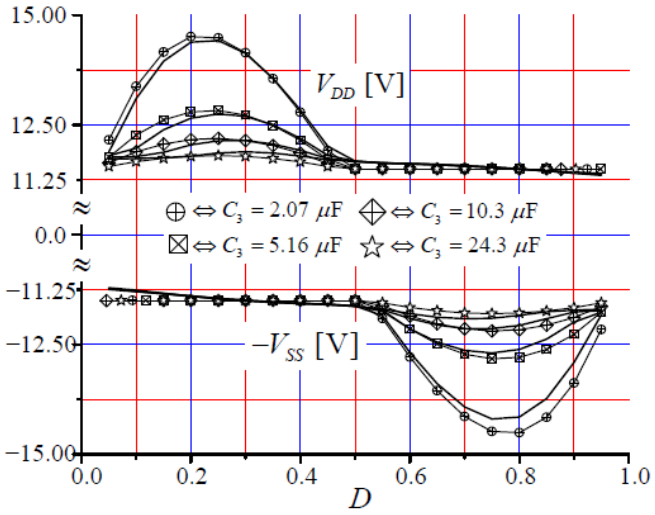

Figure 8. Measured and calculated supply voltages V_{DD} and V_{SS} for the selected set of C_3 values. Measured voltages are presented as line charts, whereas calculated voltages are presented as symbol + line charts.

Measured supply currents I_{DD} and I_{SS} against D, are presented in Figure 9. For cases (b) and (c), supply currents are greater than or equal to zero for a complete range of D, whereas sum $I_{DD} + I_{SS}$ is the same for all 3 cases, which corroborates theoretical predictions.

Power consumption, for several measured or theoretically calculated cases, is presented in Figure 10. For cases (b) and (c), power supply is unidirectional, and the SC circuit is fully active. For the case (a) in which power supply is bilateral, capacitor C_3 is removed (C_3 = 0) so that SC circuit contributes to quiescent consumption, but it does not engage in BP suppression.

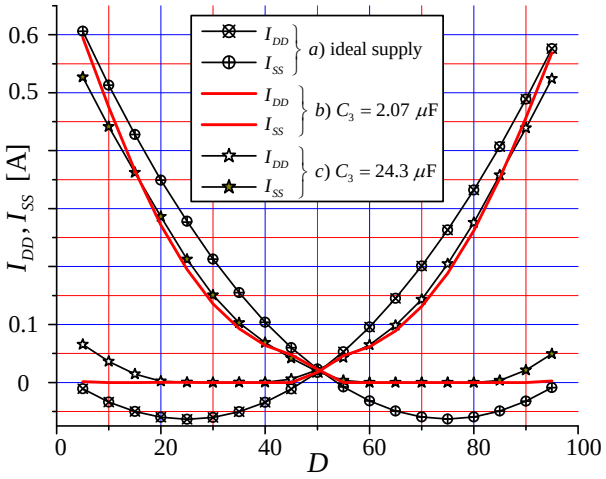

Figure 9. Measured supply currents: (**a**) ideal (bilateral) power supply; (**b**) unilateral power supply and C_3 = 2.07 µF; (**c**) unidirectional power supply and C_3 = 24.3 µF.

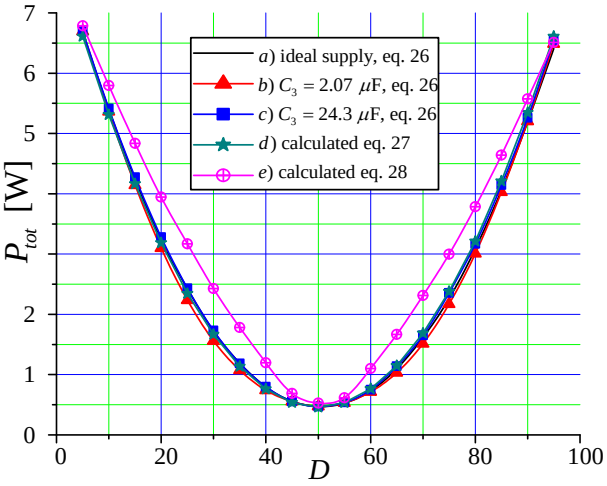

Figure 10. Measured and calculated power consumption: (**a**) measured, bilateral power supply; (**b**) measured, unidirectional supply and C_3 = 2.07 µF; (**c**) measured, unidirectional supply and C_3 = 24.3 µF; (**d**) calculated, ideal case augmented with quiescent consumption P_0 (**e**) calculated, unilateral power supply and perfect absorption of negative supply currents, raised with quiescent consumption P_0 (ideal dissipative method).

When power consumption is measured, for cases (a), (b), and (c), it is done indirectly as

$$P_{tot} = V_{DD} \cdot I_{DD} + V_{SS} \cdot I_{SS}. \tag{27}$$

For the case (d) and (e), power consumption is calculated on the basis of Equation (8) and Equation (10), augmented with quiescent consumption P_0:

$$P_{tot} = P_o + RI_{LM}^2(1-2D)^2, \tag{28}$$

for bilateral power supply, and

$$P_{tot} = \begin{cases} P_0 + RI_{LM}^2(1-D)(1-2D), \ D < 0.5 \\ P_0 + -R_0 I_{LM}^2 D(1-2D), \ D > 0.5 \end{cases}, \tag{29}$$

for unilateral power supply.

It can be observed that the use of proposed SC circuit preserves energy efficiency, as in the case of ideal power supply.

The waveforms for illustrating dynamic behavior of the positive and negative supply voltages when the duty factor alternately changes from 0.5 to 0.25, and vice versa, with intervals of 50 ms, are shown in Figure 11. Responses are captured in a following way: for the case of bilateral supply, case (a); for the case of unilateral power supply and two different values of capacitor C_3, cases (b), (c). Voltage v_L, a seen in Figure 6, is displayed on channel CH 1, voltage $+v_{DD}$ is displayed on channels CH 5–CH 7, and voltage $-v_{SS}$ is displayed on channels CH 2–CH 4.

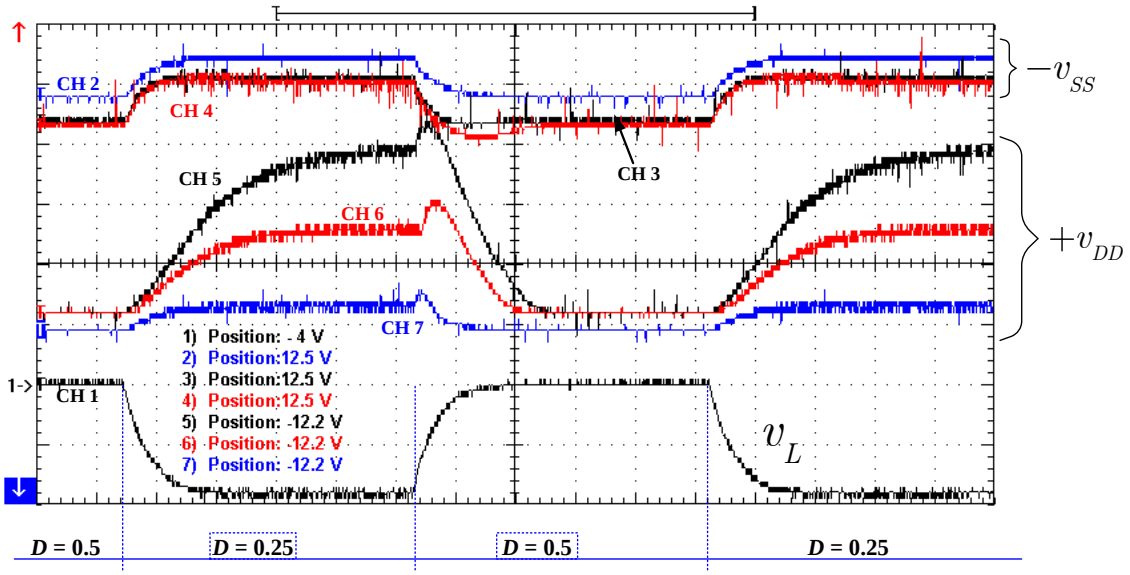

Figure 11. Vertical scale CH 1: 2 V/div, zero position −4 V. Vertical scale CH 2–CH 4: 200 mV/div, zero position 12.5 V. Vertical scale CH 5–CH 7: 200 mV/div, zero position −12.2 V. Horizontal scale: 10 ms/div. Channels: (a) CH 2 and CH 7, transients on supply busses, bidirectional power supply; (b) CH 6 and CH 3, transients on supply busses, unidirectional power supply, C_3 = 24.3 µF; (c) CH 6 and CH 3, transients on supply busses, unidirectional power supply, C_3 = 24.3 µF. (d) CH 5 and CH 4, transients on supply busses, unidirectional power supply, C_3 = 10.3 µF.

For the case (a), there is no bus-pumping, and power supply voltages $+v_{DD}$ and $-v_{SS}$ suffer from voltage drops caused by load regulation. Transient response of supply voltages follows the transient response of the load, with time constant $\tau_L = L/R$ = 3.3 ms.

For the cases (b) and (c), only positive portion of the power supply is blocked during time periods when D = 0.25, and $+v_{DD}$ bus experiences BP. Transient response of $+v_{DD}$ is slowed down due to time constants τ_3 and τ_4, Table 1. On the other hand, the negative portion of the power supply is active, and transient response of the voltage $-v_{SS}$ follows transient response of the load, according to time constant τ_L.

5. Conclusions

For the case of standard unilateral power supplies, described dissipative methods for BP suppression in class-D amplifiers can be extremely simple and cost-effective. Still, they cannot provide the full potential of HB topology regarding power efficiency. As an alternative, a high-efficiency SC technique for BP reduction in HB class-D amplifiers is proposed in this paper. It is shown that the proposed SC technique can reduce BP significantly and preserve energy efficiency of ideal HB class-D amplifier, with advantages of high efficiency, simple implementation possibility, and low cost. Analytical results are given to verify the operation principles. Hardware implementation of the proposed technique and its operation considerations were analyzed and described. A laboratory

prototype was implemented and tested to show its performance, regarding BP suppression, power efficiency, and dynamical characteristics.

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Nomenclature

DC and average quantities are represented by uppercase symbols with uppercase subscripts, for example, I_{D1}. AC quantities are represented by lowercase symbols with lowercase subscripts, for example, i_{d1}. Total quantities AC+DC are characterized by lowercase symbols with uppercase subscripts, for example, $i_{D1} = i_{d1} + I_{D1}$. Any quantity is considered negative if it is less than zero; for example, negative i_{D1} means that $i_{D1} < 0$.

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