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Interleaved High Step-Up Current Sharing Converter with Coupled Inductors

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Abstract: An interleaved high-step-up current sharing DC–DC converter with coupled inductors is proposed in this paper. The operation principle and property of this converter are analyzed. The ripple of the input current in the proposed converter is decreased significantly by using the two-phase parallel interleaved input. The voltage gain is extended and the switch voltage stress is reduced by the coupled inductors. The leakage inductance of the coupled inductors reduces the reverse-recovery problem of the output diode, resulting in the reduction of reverse-recovery losses. As there are two interleaved phases in the proposed converter, the third winding of each coupled inductor is embedded in another phase. With this design, when the leakage inductance or duty cycle is asymmetrical, the current sharing performance is still positive. Consequently, the new topology is very suitable for applications to occasions with low voltage input and high voltage output, such as the fuel cell power system. Finally, the performance of this topological circuit is verified by a prototype with 500 W output.

Keywords: current sharing; interleaved boost converter; high step-up; coupled inductors

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1. Introduction

Due to the public awareness of climate change and strict emission regulations issued by governments, automobile companies are trying to develop low emission or zero emission vehicles [1]. In recent years, technological progress in the field of alternative power supply and switching power supply has promoted the development of electric vehicles (EVs). Battery electric vehicles (BEVs), fuel cell hybrid electric vehicles (FCHEVs) and plug-in hybrid electric vehicles (PHEVs) are being widely studied and developed [2–5]. In the electric vehicle system with low voltage and high current battery, in order to control the DC side voltage, a DC–DC converter is required to boost the battery voltage. This converter must have large voltage gain, low switch stress and input current ripple and high conversion efficiency.

Traditional boost converters have many disadvantages, including large ripples of input current and high switch voltage stress. It is necessary to apply ultimate duty cycle to get a high voltage gain. This may increase loss of the converter because the existence of parasitic parameters of the converter blocks access to high voltage gains even by using ultimate duty cycle [6]. Many coupled-inductor converters with high set-up and high efficiency have been developed to overcome defects of traditional converters [7–12]. Voltage gain is increased significantly by a multiplier unit composed of coupled inductor and capacitance and the main switch voltage stress is decreased greatly since the coupled inductor has the functions of transformer. Energies of leakage inductance are absorbed by clamping circuit and the rate of current reduction of the output diode is limited by leakage inductance, thus alleviating the reverse-recovery problem of the output diode. Thanks to single-phase operation, converters have a relatively low power level and relatively large ripples of input current. Ripples of current of different phases are offset mutually through the

interleaved parallel connection [13,14]. Although this decreases ripples of input current and increases power level significantly, the switch voltage stress is relatively large and the gain is relatively low.

The interleaved parallel DC–DC converter with high set-up is characteristic of high gains, low switch voltage stress, small ripples of input current and high power level under the same duty cycle [15–19]. This kind of converter has several issues. First, additional active clamp switches accompanied with floating gate-drive signals are required which increase both the complexity of the circuit and the cost. Second, a high conduction loss results from the high current through the active clamp switch. Thus, the efficiency is limited. Moreover, if the output is of an uninterleaved structure, the output voltage ripple will be large [20,21]. Third, the current autobalance between the two interleaved branches is not achieved, which leads to a high burden for one branch and a large input current ripple at asymmetry condition [22]. Fourth, it still fails to solve the output diode reverse-recovery problem.

To address the above defects of DC–DC converters, a novel interleaved high-step-up current sharing DC–DC converter with coupled inductors was proposed in the present study. With interleaved input, this converter has high power level, small ripples of input current, high voltage gains and small main switch voltage stress. The switches achieve zero current switching (ZCS) turn-on. The reverse-recovery loss of the output diode is small due to the leakage inductance of coupled inductor. Due to interleaved coupling of third coils in the coupled inductor, the circuit is equipped with current sharing performance. In other words, the input current and output current can be balanced automatically under an asymmetrical duty cycle.

2. Working Principle

The topology of an interleaved high-step-up current sharing DC-DC converter with coupled conductors is shown in Figure 1. The traditional interleaved boost converter (low-voltage side) is shown in the left dotted framework, which uses two-phase parallel input to decrease ripples of input current and increase power level. The circuit has two coupled inductors and each one has three coils. The number of turns of the three coils in each coupled inductor are n_1, n_2 and n_3, respectively. The dotted terminals of coupled inductors are marked by "○" and "•". The third coil is inserted into another phase to realize current sharing performance. C_{C1} and C_{C2} are clamp capacitors which can absorb energy of leakage inductance (L_{LK}) and reduce switch voltage stress. C_{f1} and C_{f2} are series capacitors. D_{C1} and D_{C2} are clamping diodes. D_{o1} and D_{o2} are output diodes, respectively.

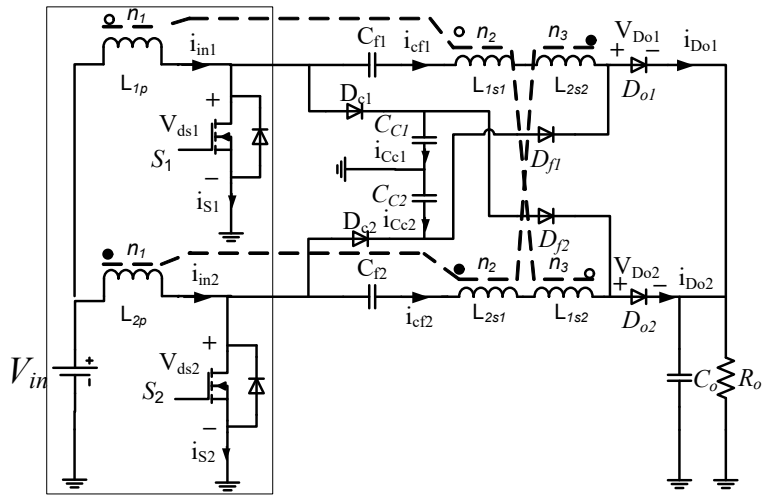

Figure 1. Interleaved high step-up current sharing converter with coupled conductors.

The equivalent circuit of the interleaved high step-up current sharing converter is shown in Figure 2. L_{m1} and L_{m2} are excitation inductances. L_{LKa} and L_{LKb} are leakage inductances of primary coil of the corresponding coupled inductor. L_{LKc} is the sum of leakage inductances in the secondary coil 2 of coupled inductor 1 and the secondary coil 3 of coupled inductor 2. L_{LKd} is the sum of leakage inductances in the secondary coil 2 of coupled inductor 2 and the secondary coil 3 of coupled inductor 1. S_1 and S_2 are power switches. V_{in} and V_{out} are input voltage and output voltage. Let n_2 be equal to n_3 and the turns ratio (N) is determined n_2/n_1.

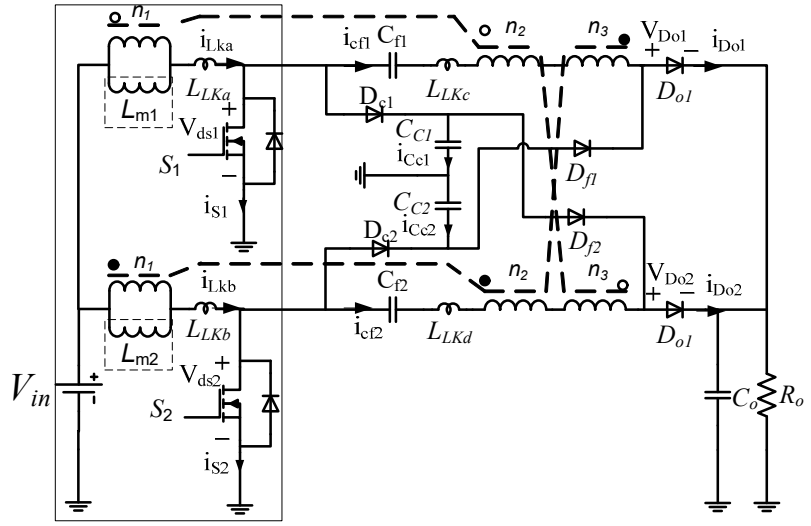

Figure 2. Equivalent circuit of the interleaved high step-up current sharing converter.

Key waveforms of the proposed converter under stable state are presented in Figure 3. There are 12 operation stages in each period. Considering the symmetrical structure of the circuit topology, only six operation stages are chosen in the following analysis.

Stage 1 (t_0-t_1): As shown in Figure 4a, switches S_1 and S_2 are turned on, and diodes D_{o1}, D_{o2}, D_{c1}, D_{c2}, D_{f1} and D_{f2} all adopt reverse bias. The power supply is used for charging of excitation inductors (L_{m1} and L_{m2}) and leakage inductances (L_{k1} and L_{k2}). The rate of current rise of leakage inductance is:

$$\frac{di_{LKa}}{dt} = \frac{V_{in}}{L_{LKa} + L_{m1}} \tag{1}$$

$$\frac{di_{LKb}}{dt} = \frac{V_{in}}{L_{LKb} + L_{m2}} \tag{2}$$

Stage 2 (t_1–t_2): As shown in Figure 4b, switch s_1 is turned off and the excitation inductor charges the drain-source parasitic capacitor C_{s1}. When the drain-source voltage is increased, the inverse voltage on diode D_{c1} is decreased (Equation (3)). This operation stage is very short since the parasitic capacitance is very small.

$$v_{ds1}(t) = \frac{I_{Lm1}(t - t_1)}{C_{s1}} \tag{3}$$

Stage 3 (t_2–t_3): As shown in Figure 4c, voltage of V_{ds1} at t_2 increased to power on the clamping diode D_{C1} and the excitation inductor L_{m1} charges the clamp capacitor C_{C1}. The drain-source voltage V_{ds1} is clamped by the clamp capacitor C_{C2}. Energies on excitation inductor begin to be transmitted onto the clamp capacitor:

$$u_{ds1}(t) = V_{ds1}(t2) + \frac{I_{Lm1}(t2)}{C_{c2}}(t - t_2) \tag{4}$$

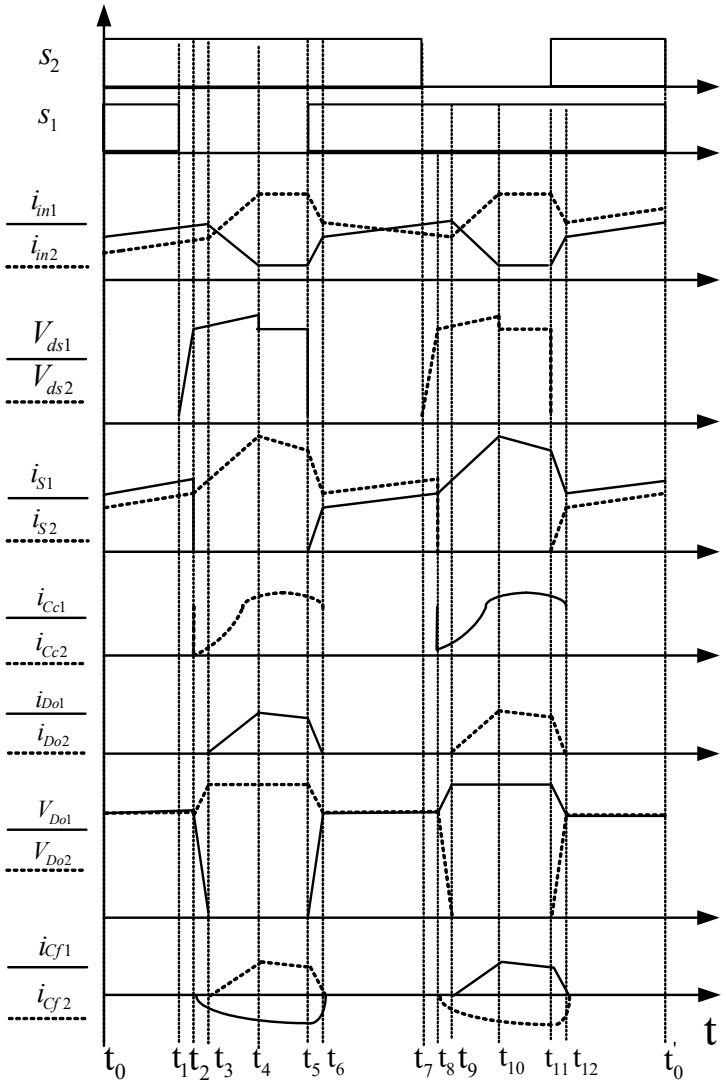

Figure 3. Key waveforms of the interleaved high step-up current sharing converter.

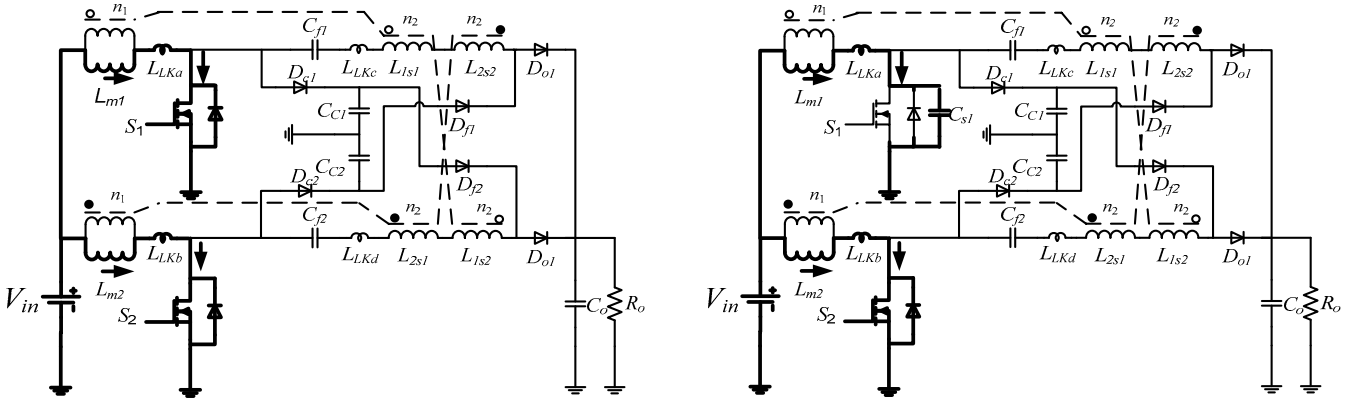

Figure 4. *Cont.*

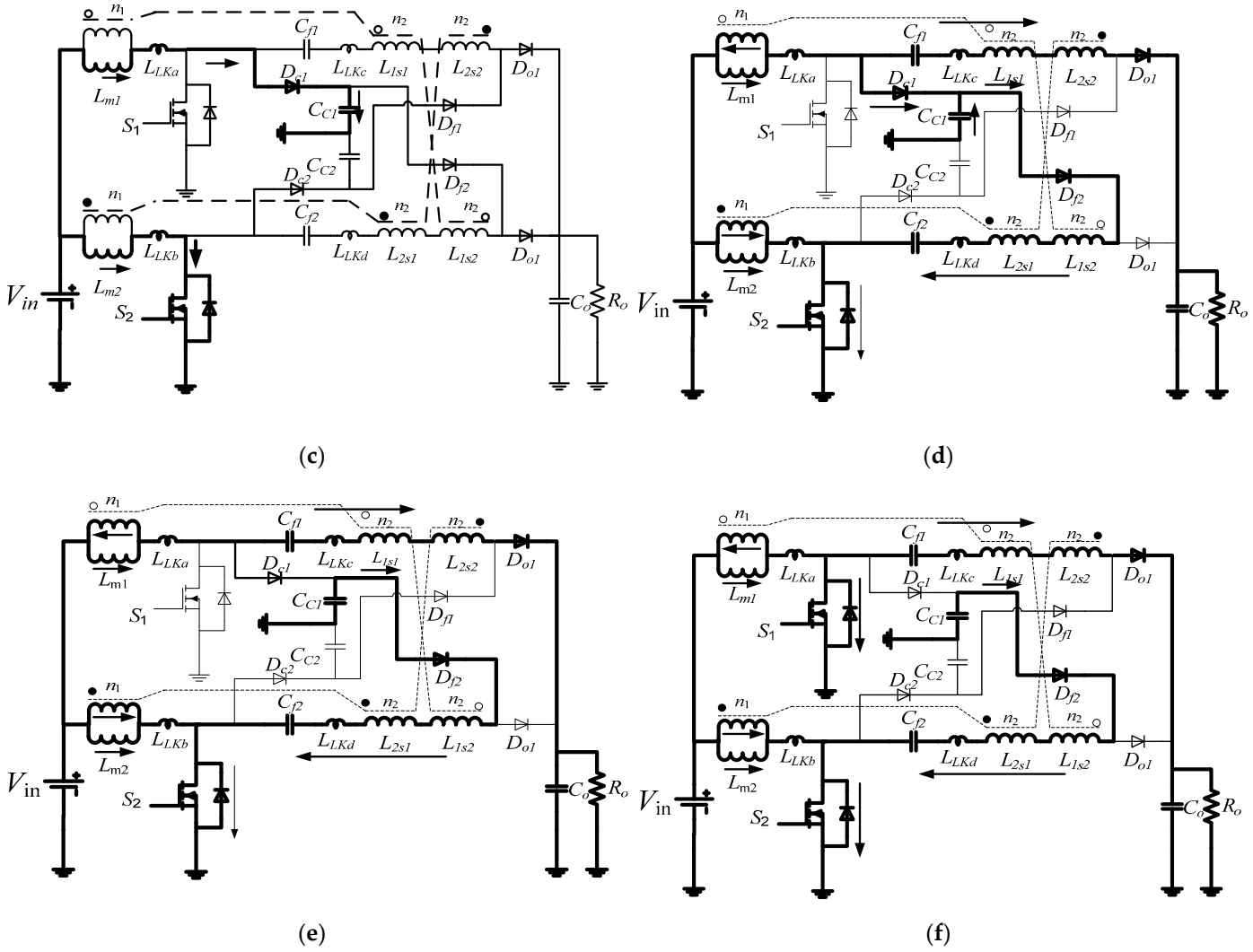

Figure 4. Operation stages of the interleaved high step-up current sharing converter. (**a**) Stage 1. (**b**) Stage 2. (**c**) Stage 3. (**d**) Stage 4. (**e**) Stage 5. (**f**) Stage 6.

Stage 4 (t_3–t_4): As shown in Figure 4d, since the inverse voltage of output diode D_{o1} at t_3 decreased to zero and it is turned on, the rate of rise of the diode current is controlled by the leakage inductance L_{Kc}. The current of D_{c1} declines when the current of D_{o1} increases. The series connection of series capacitor C_{f1}, the secondary coil 1 of the coupled inductor 1 and the secondary coil 2 of the coupled inductor 2 is used as the power source to get high voltage gain for the output. Meanwhile, the diode D_{f2} is turned on and energies which are stored on the clamping diode C_{c1} are transmitted to the series capacitance C_{f2} through diode D_{f2}, secondary coil 1 of the coupled inductor 2, secondary coil 2 of the coupled inductor 1 and the switch s_2. The current of diode D_{f2} is controlled by the leakage inductance L_{Kd}. The current relationship is as follows:

$$i_{D_{c1}}(t) = i_{L_{m1}}(t) - (N+1)i_{D_{o1}}(t) - Ni_{D_{f2}}(t) \tag{5}$$

Stage 5 (t_4-t_5): As shown in Figure 4e, current which flows through the clamping diode D_{C1} decreases to zero and the clamping diode D_{C1} is shut off. Since the rate of current reduction is controlled by leakage inductance, there is no reverse-recovery problem. Energies which are stored on the series capacitor C_{f1} are transmitted onto the load. Currents which flow through D_{o1} are controlled by L_{Ka} and L_{kc} together.

Stage 6 (t_5–t_6): As shown in Figure 4f, the switch s_1 is powered on at t_5 and it realizes zero current turn-on since there's leakage inductance (L_{Ka}). The rate of current reductions in the diode D_{o1} and the diode D_{Cf2} are controlled by leakage inductances L_{LKc} and L_{LKd}, respectively. Therefore, there is no diode reverse-recovery problem.

$$i_{L_{LKa}} = i_{D_{c1}} + i_{D_{o1}} \tag{6}$$

$$i_{S2} = i_{Lm2}(t) + Ni_{D_{o1}}(t) + (N+1)i_{i_{D_{f2}}}(t) \tag{7}$$

$$i_{D_{f2}} = i_{D_{f2}}(t_5) - \frac{V_{Cf2} - V_{C_{C2}}}{L_{LKd}}(t - t_5) \tag{8}$$

$$i_{D_{o1}}(t) = I_{D_{o1}}(t_5) - \frac{V_o - V_{Cf1}}{L_{LKc}}(t - t_5) \tag{9}$$

3. Steady-State Working Performance Analysis

3.1. Voltage Gains

The duty cycle of signals is controlled within 0 < D < 0.5. Due to the symmetry of the circuit, there are $L_{m1} = L_{m2}$, $C_{C1} = C_{C2}$ and $C_{f1} = C_{f2}$.

To simplify the analysis, voltages of the clamp capacitor (C_C and series capacitor (C_f) are assumed to be stable. Hence, the voltage on the clamp capacitor is:

$$V_{c_c} = \frac{V_{in}}{1 - D} \tag{10}$$

The voltage on V_{cf} can be gained from Stage 4:

$$V_{cf} = \frac{1 + N}{1 - D}V_{in} \tag{11}$$

The output voltage can be gained from Stage 4:

$$V_o = V_{cc2} + V_{C_{f1}} - V_{L_{1S1}} + V_{L_{2S2}} \tag{12}$$

$$V_{L_{1S1}} = V_{in} - V_{cc1} \tag{13}$$

$$V_{L_{2S2}} = V_{in} \tag{14}$$

The output voltage gain can be obtained from Equations (10)–(14):

$$M = \frac{2(1 + N)}{1 - D} \tag{15}$$

where N is the turns ratio of the coupled inductor, D is the duty cycle of switch control signals and M is the output voltage gain.

It can be seen from Equation (15) that the voltage gain of the proposed converter M is determined by duty cycle D and the turns ratio of the coupled inductor N. The relations between these two factors and voltage gain are shown in Figure 5. M is increased with the increase of D and N. In this way, it can avoid the traditional use of ultimate duty cycle in application occasions with high gains, thus decreasing the ripple of current and switching loss.

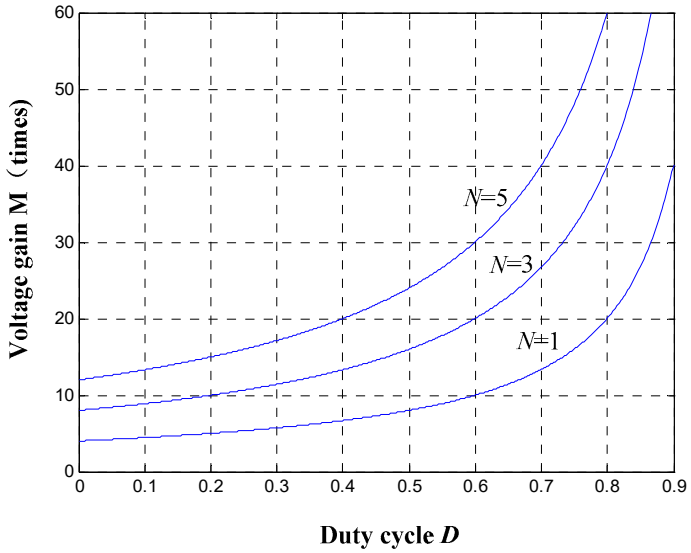

Figure 5. Relation curves of voltage gain with turns ratio and duty cycle.

3.2. Switch Voltage Stress

Voltages on the switch S and the clamping diode D_C are equal to voltage of the clamp capacitor:

$$V_s = V_D = \frac{V_{in}}{1-D} = \frac{V_{out}}{2(1+N)} \tag{16}$$

It can be seen from Equation (16) that when the output voltage is fixed, the voltage stress of the power switch is determined by the turns ratio of the coupled inductor. Relation curve between voltage stress and turns ratio is shown in Figure 6. The maximum voltage stress ratio is 0.5 and it declines gradually with the increase of the turns ratio. Hence, Mosfet with low rated voltage can be used in application occasions which require high gains. The lower the rated voltage is, the smaller the on-resistance is, and thus the smaller the conduction loss is.

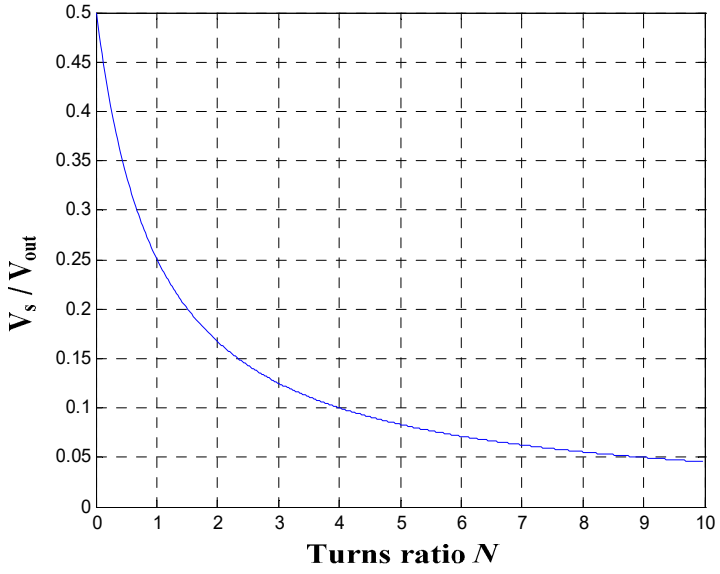

Figure 6. Relation curve between turns ratio and normalized switch voltage stress ratio.

The voltage of the series capacitor C_f is:

$$V_{cf} = \frac{1+N}{1-D} V_{in} = \frac{V_{out}}{2} \tag{17}$$

The voltage stress of output diode D_o is:

$$V_{Do} = V_{out} - V_{c_c} = \frac{1+2N}{1-D} V_{in} = \frac{1+2N}{2(1+N)} V_o \tag{18}$$

The relationship between output diode voltage stress and turns ratio is shown in Figure 7. The minimum output diode voltage stress ratio is 0.5. With the increase of turns ratio, the voltage stress increases. However, it always remains lower than the output voltage.

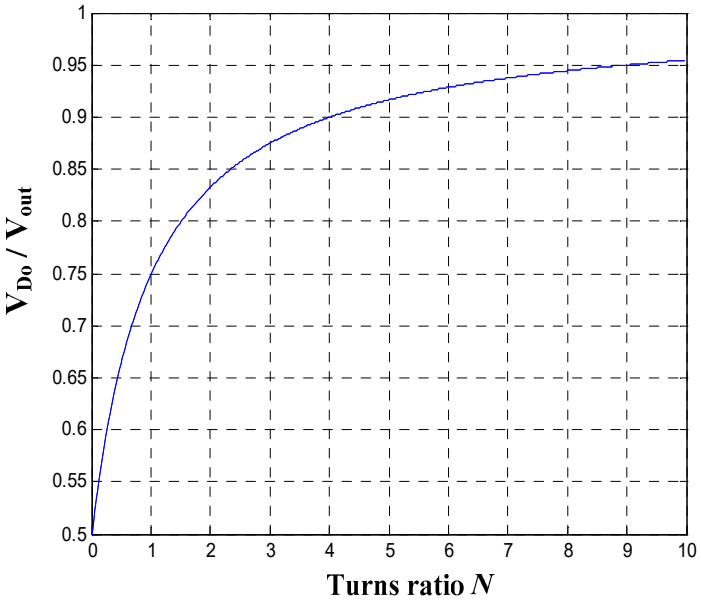

Figure 7. Relation curves between turns ratio and normalized output diode voltage stress ratio.

The voltage stress of the diode D_f is:

$$V_{Df} = V_{out} - V_{c_c} = \frac{1+2N}{1-D} V_{in} = \frac{1+2N}{2(1+N)} V_o \tag{19}$$

This is same with the output diode voltage stress.

3.3. Realization of Soft Switching

When the switches S_1 and S_2 are turned on, they can realize zero-current turn on due to the effects of leakage inductances (L_{LKa} and L_{LKb}) of the coupled inductors. The conduction loss of switches is low. When S_1 and S_2 are turned off, energies which are stored in the leakage inductor are transmitted to the clamp capacitor through the clamping diode, thus significantly decreasing stress on switches and turn-off losses of the switches. Influenced by leakage inductance of the coupled inductor, the current of the clamping diode is controlled by leakage inductance and there is no reverse-recovery problem. The rate of current reduction of the output diode is controlled by L_{LKc} and L_{LKd}, which avoids reverse-recovery problem and decreases diode losses.

3.4. Current Sharing

Since the third coil of the coupled inductor is inserted into another phase, two-phase current sharing can be achieved when the duty cycle is asymmetric. Simulation results of input current unbalance factor $(I_{in1} - I_{in2})/I_{in2}$ when the converter power is 1000 W, the duty ratio of S_1 is 0.7 and the duty ratio of s_2 increases from 0.65 to 0.75 are shown in Figure 8. I_{in1} and I_{in2} are primary currents of two coupled inductors. It can be seen from Figure 8 that the input current unbalance factor is very small when the duty cycle of S_2 changes. When the duty cycles of S_1 and S_2 are 0.7 and 0.75, the input current unbalance factor is only 0.2. Simulation results of the output current unbalance factor $(I_{o1} - I_{o2})/I_{o2}$ under the same conditions are shown in Figure 9. I_{o1} and I_{o2} are currents of two output diodes. The unbalance factor is basically zero with changes of duty ratio of S_2. This circuit has very strong current sharing performances.

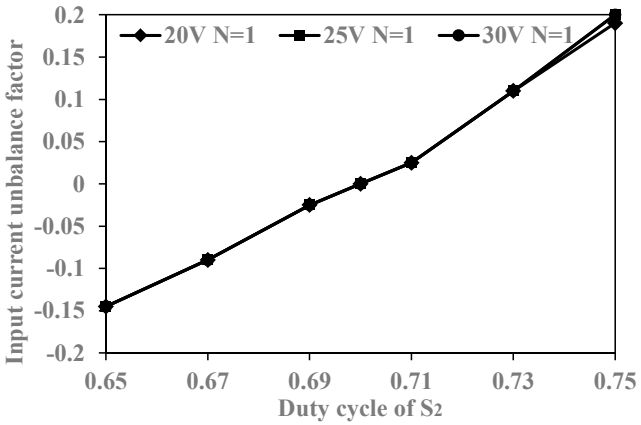

Figure 8. Input current auto-balance performance under asymmetrical duty cycle.

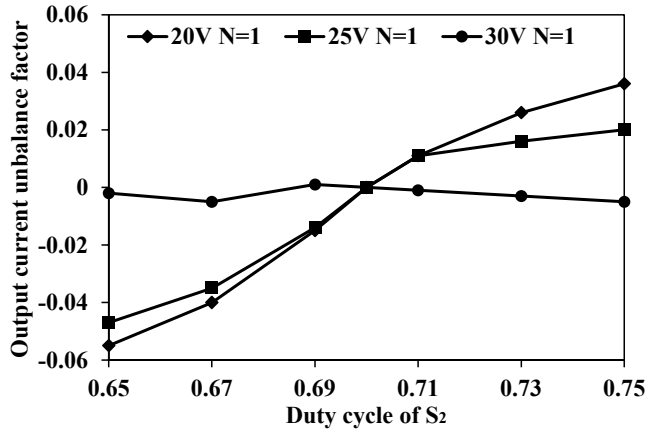

Figure 9. Output current auto-balance performance with asymmetrical duty cycle.

4. Experimental Verification

To verify the accuracy of the theoretical analysis, a 500 W prototype was used in the experimental verification. Experimental parameters of converter are introduced as follows: V_{in} = 20–30 V; P_{out} = 500 W; f_s = 50 kH; n_2/n_1 = 16/16; L_m = 100 µH; C_o = 100 µF; C_{c1} and C_{c2}: 4.7 µF; C_{f1} and C_{f2}: 4.7 µF; S_1 and S_2: IRF34158; D_{c1} and D_{c2}: MUR1560T; D_{f1} and D_{f2}: MUR1560T; D_{o1} and D_{o2}: MUR1560T; duty cycle of control signals D = 0.7. Figure 10 shows the experimental setup.

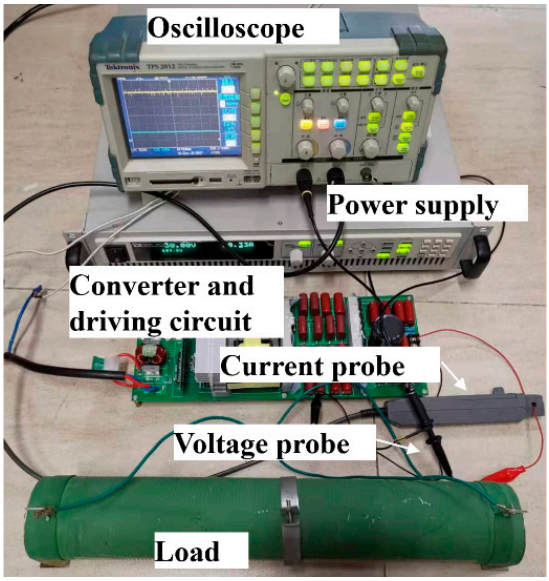

Figure 10. Experimental setup.

The voltage stress waveform and the driving signal waveform of S_1 are shown in Figure 11a (S_2 is similar to S_1). Drain-source voltage of S_1 is about 80 V and it is only about 1/3 of output voltage. Voltage stresses of S_1 and S_2 are equal. The voltage waveform of S_1 and the voltage waveform of clamp capacitor C_1 are shown in Figure 11b. The average voltage of C_1 is about 80 V. The voltage waveform of S_1 and the current waveform of leakage inductance i_{LKa} are shown in Figure 11c. The input current waveform of the converter and current waveforms of two leakage inductances i_{LKa} and i_{Lkb} are presented in Figure 11d. The proposed converter uses interleaved two-phase input, which decreases ripples of its input current significantly. Voltage waveform of S_1 and voltage waveform of C_{f1} are shown in Figure 11e. Voltage waveforms of D_{c1} and D_{f2} are shown in Figure 11f. Voltage and current waveforms of D_{o1} are shown in Figure 11g, which present no reverse-recovery problem of the output diode.

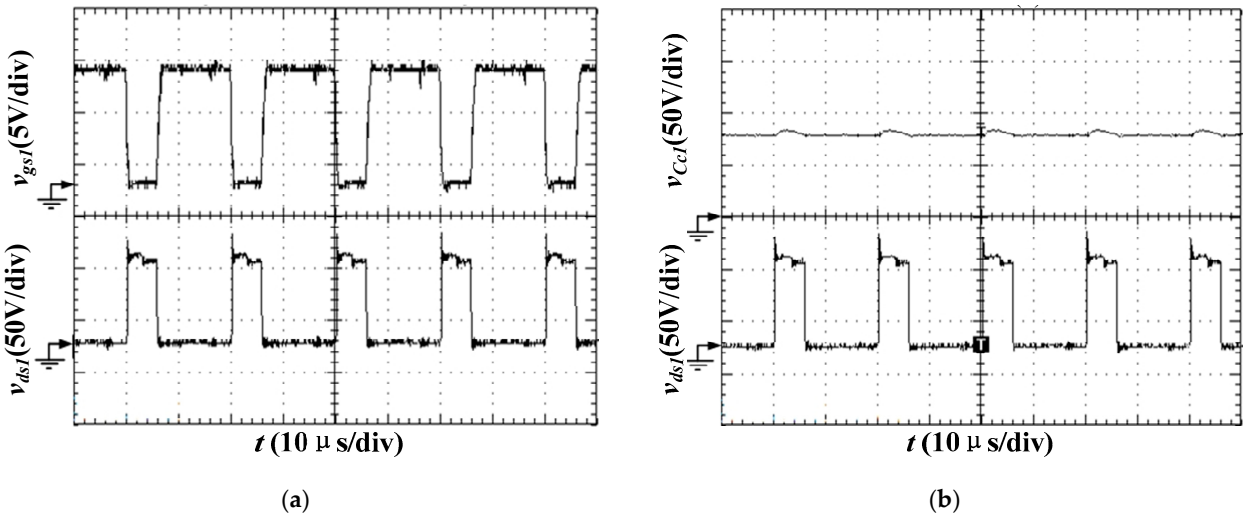

Figure 11. *Cont.*

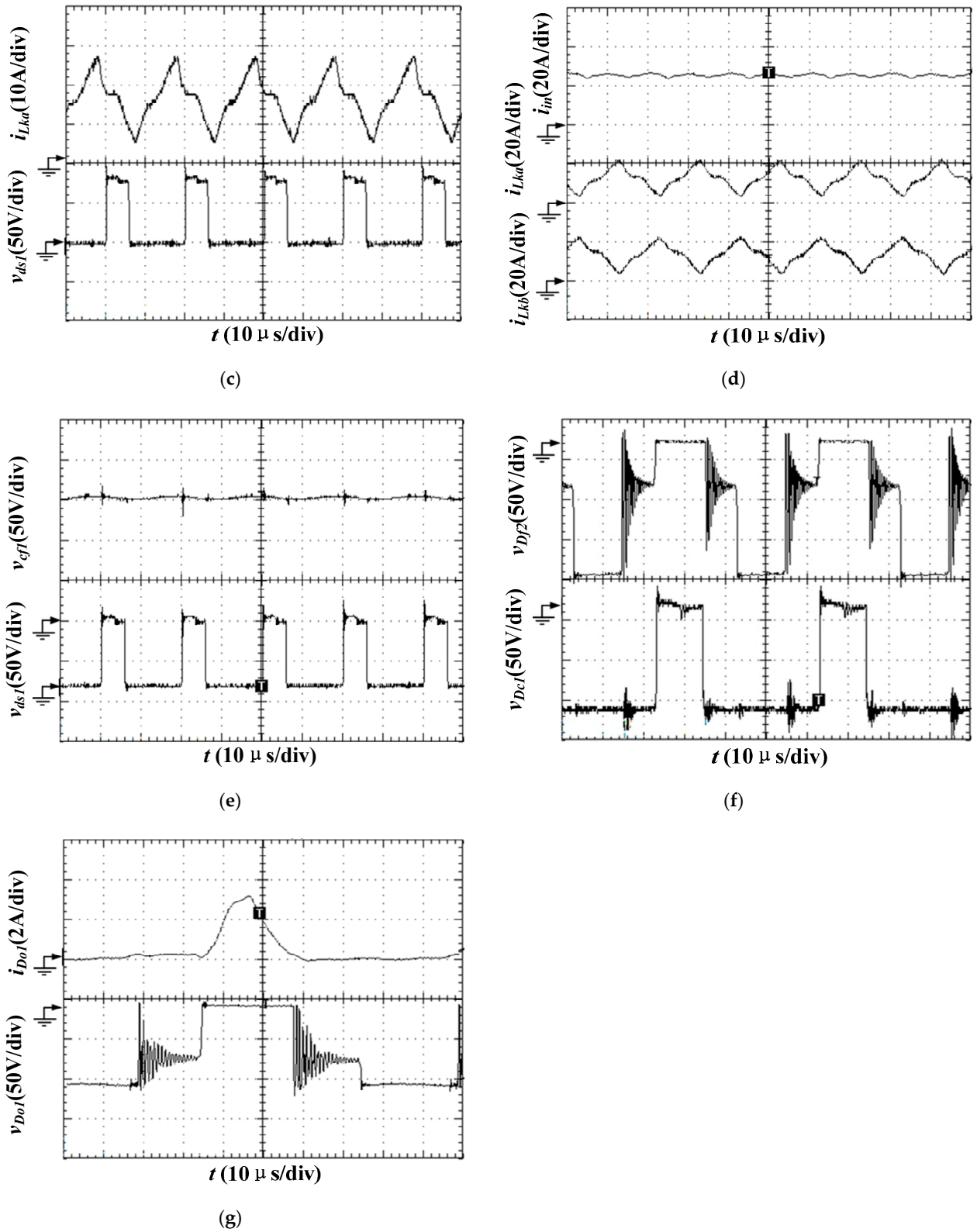

Figure 11. Experimental waveforms. (**a**) Voltage stress waveform and the driving signal waveform of S_1. (**b**) Voltage waveform of S_1 and the voltage waveform of clamp capacitor C_1. (**c**) Voltage waveform of S_1 and the current waveform of leakage inductance. (**d**) Input current waveform of the converter and current waveforms of two leakage inductances. (**e**) Voltage waveform of S_1 and voltage waveform of C_{f1}. (**f**) Voltage waveforms of D_{c1} and D_{f2}. (**g**) Voltage and current waveforms of D_{o1}.

The relation between the input voltage and efficiency under a closed-loop control when the output power is 500 W and the output load is constant is exhibited in Figure 12. Clearly, efficiency is positively related to the increase of input voltage. The efficiency is about 94% when the input voltage is 30 V.

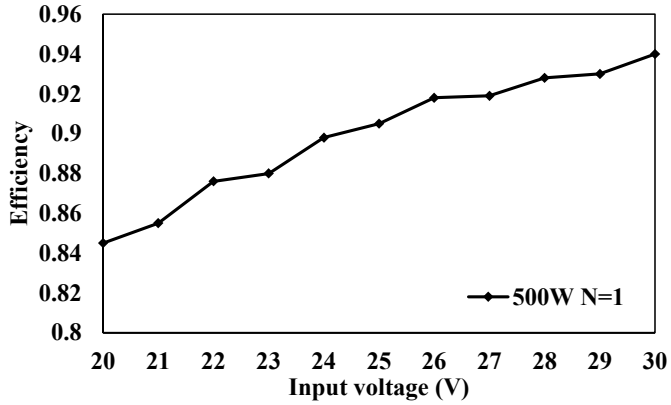

Figure 12. Measured conversion efficiency under different input voltages at 500 W.

The relation between efficiency and output power when duty cycle is 0.75 and input voltages are 20 V, 25 V and 30 V is shown in Figure 13. When the output power is fixed, efficiency is positively related with input voltage. When the input voltage is fixed, efficiency is negatively correlated with output power.

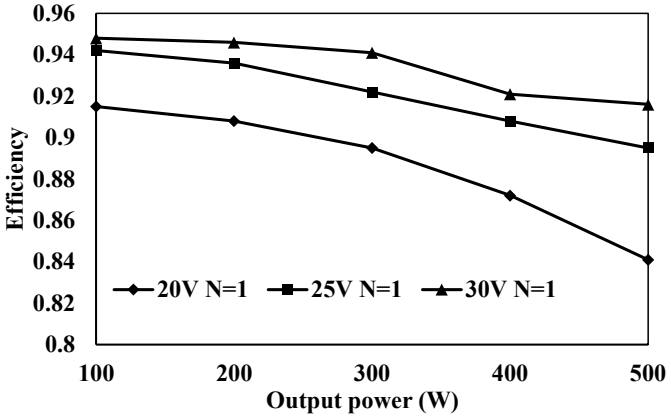

Figure 13. Measured efficiencies at different loads.

5. Conclusions

An interleaved high step-up current sharing DC–DC converter with coupled conductors is proposed in this paper. Table 1 gives a performance comparison among the conventional transformer-included boost converter, the conventional interleaved boost converter, the improved interleaved boost converter described in [22] and the proposed converter. Compared to a conventional transformer-included boost converter and conventional interleaved boost converter, the proposed interleaved high step-up current sharing DC–DC converter has higher voltage gains by using the coupled inductors and voltage multiplier. Therefore, it avoids the use of ultimate duty cycle to increase voltage gain. Influenced by clamping diode and clamp capacitor, energies which are stored in leakage inductor can be recovered to the clamp capacitor, thus decreasing switch voltage stress. The proposed converter decreases ripples of input current significantly by using the parallel interleaving mode. Switches S_1 and S_2 realize ZCS turn on. Due to existences of leakage inductance, the reverse-recovery problem of output diode is alleviated; thus, the switching

loss and electromagnetic interferences are decreased. Compared to the converter in [22], the proposed converter realized current autobalance. In addition, its clamp circuit is simpler.

Table 1. Converter performance comparison.

	Conventional Transformer Included Boost Converter	Conventional Interleaved Boost Converter	Converter in [22]	Proposed Converter
Voltage gain	$\frac{N}{2\cdot(1-D)}$	$\frac{1}{1-D}$	$\frac{2+2N}{1-D}$	$\frac{2+2N}{1-D}$
Main switch voltage stress	$\frac{2\cdot V_o}{N}$	V_o	$\frac{V_o}{2+2N}$	$\frac{V_o}{2+2N}$
Output diode voltage stress	V_o	V_o	V_o	Less than 2/3 V_o
Input current ripple	Large	Large	Small	small (in total)
Soft switching	ZCS or ZVS	Hard switching	ZVS	ZCS
Reverse recovery	Large	Large	Small	Small
Output voltage ripple	Large	Large	Small	Small
Current autobalance	No	No	No	Yes
Clamp circuit	Natural voltage clamping	Additional circuit	Two MOSFETS two capacitors	Two diodes Two capacitors

There are two issues that need to be addressed in the future work. First, the switches S_1 and S_2 only achieve zero current turn-on. The future work is to realize zero voltage turn-off to further reduce switching loss and improve the conversion efficiency. Second, the loss of the output diode is large. The voltage stress of the output diode approaches the output voltage when the turn ratio of the coupled inductor increases. Therefore, another future work is to reduce the voltage stress of the output diode to further improve the efficiency and boost the capability of the converter.

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