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Evaluation of V_{TH} and R_{ON} Drifts during Switch-Mode Operation in Packaged SiC MOSFETs

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Abstract: In this paper, we investigate the evolution of threshold voltage (V_{TH}) and on-resistance (R_{ON}) drifts in the silicon carbide (SiC) power metal-oxide-semiconductor field-effect transistors (MOSFETs) during the switch-mode operation. A novel measurement setup for performing the required on-the-fly characterization is presented and the experimental results, obtained on commercially available TO-247 packaged SiC devices, are reported. Measurements were performed for 1000 s, during which negative V_{TH} shifts (i.e., V_{TH} decrease) and negative R_{ON} drifts (i.e., R_{ON} decrease) were observed. To better understand the origin of these parameter drifts and their possible correlation, measurements were performed for different (i) gate-driving voltage (V_{GH}) and (ii) off-state drain voltage (V_{PH}). We found that V_{TH} reduction leads to a current increase, thus yielding R_{ON} to decrease. This correlation was explained by the R_{ON} dependence on the overdrive voltage (V_{GS}–V_{TH}). We also found that gate-related effects dominate the parameter drifts at low V_{PH} with no observable recovery, due to the repeated switching of the gate signal required for the parameter monitoring. Conversely, the drain-induced instabilities caused by high V_{PH} are completely recoverable within 1000 s from the V_{PH} removal. These results show that the measurement setup is able to discern the gate/drain contributions, clarifying the origin of the observed V_{TH} and R_{ON} drifts.

Keywords: silicon carbide; V_{TH} instability; R_{ON} drift; on-the-fly characterization

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1. Introduction

Silicon carbide (SiC) is a common technology option for replacing silicon (Si) in power-switching applications that require low switching and conduction losses [1]. Unfortunately, the degradation of key electrical parameters in SiC power devices under repetitive switching stress reduces both device performance and reliability well below specifications [2]. In this scenario, stability issues like threshold voltage (V_{TH}) and dynamic on-resistance (R_{ON}) drifts are often encountered [3], severely impacting device lifetime and performance. For instance, a positive R_{ON} drift (i.e., increase) affects the conduction losses within power-switching converters, yielding a considerable efficiency reduction. Similarly, a positive V_{TH} shift results in a lower current level for a given driving gate voltage (V_{GS}) [4,5], whereas negative V_{TH} variations could impede fully turning off the device, causing unwanted conduction at a large drain bias [6].

Generally, Bias Temperature Instability (BTI) experiments are employed to reveal the mechanisms underlying these issues in SiC technology [7–9]. However, BTI tests can only be used to investigate the effects related to gate bias, neglecting the effects related to the drain bias. To get a more complete picture of the detrimental effects produced by repetitive switching stress [2,10], it is necessary to evaluate the V_{TH} and R_{ON} evolution when the

device is driven in realistic operating conditions, i.e., with both gate and drain potential repeatedly switched on and off. To this end, test circuits should be designed to mimic conventional switching conditions in terms of frequency, voltage, and current level. At the same time, these circuits should also extract the parameters of interest (e.g., V_{TH} and R_{ON}) without affecting device operation. Accordingly, a fast stress measurement approach is needed, in order to cope with switching frequencies in the kHz range [11] and also to limit the delay between the stress and readout [12–14] phases, thus avoiding ambiguous parameter drifts and/or wrong data interpretation. Nevertheless, achieving these goals is challenging for conventional parameter analyzers, especially when characterizing packaged devices with large parasitic capacitances [15]. The development of custom, ad-hoc systems is thus essential to investigate the stability and performance of commercially available state-of-the-art devices.

In this work, we present a novel measurement setup that allows the simultaneous monitoring of both V_{TH} and R_{ON} during the conventional switch-mode operation for packaged SiC metal-oxide-semiconductor field-effect transistors (MOSFETs). The measurement is carried out by means of double-pulsed on-the-fly (OTF) characterization, in which the Device Under Test (DUT) is repeatedly switched between a high voltage off-state condition and a low voltage on-state one in the kHz frequency range. To this end, soft-switching conditions are considered (i.e., turn ON and turn OFF transitions are performed at zero current). During OTF measurements, the device V_{TH} and R_{ON} are evaluated in order to monitor their drifts over time with a digital sampling oscilloscope (DSO). Since the parameter instabilities could manifest either after a few or several operating cycles [16], it is important to monitor the parameters of interest over several time decades to capture the whole dynamics. Accordingly, the DSO acquisition was triggered at logarithmically spaced time instants in order to avoid memory saturation and loss of accuracy [17]. By applying the proposed measurement method on commercially available devices (i.e., TO–247 vertical SiC MOSFETs), it was possible to test the effectiveness of the setup and to provide a qualitative interpretation of the physical mechanisms leading to the observed V_{TH} and R_{ON} drifts. Particularly, negative drifts (i.e., decrease) were observed for both V_{TH} and R_{ON}, that can be ascribed to the presence of traps at the SiC/SiO_2 interface [18–20].

The paper is organized as follows. Section 2 describes the custom measurement setup and the adopted design strategies to improve the measurement accuracy. In Section 3, the data collected for tested SiC MOSFETs are presented, highlighting the drift effects on the devices' trans-characteristics. Particularly, we investigated the effect of the bias conditions on the observed drifts, emphasizing the effect of the gate-driving voltage applied in on-state (V_{GH}) and of the drain voltage applied during off-state stress (V_{PH}). Finally, Section 4 draws the conclusions of the paper.

2. Measurement Setup

The simplified schematic of the custom measurement setup is shown in Figure 1. The system was developed starting from the design first presented in [17], with several important modifications as discussed in the following.

The gate driver circuit is responsible for repeatedly switching the DUT ON and OFF and is devoted to the generation of the ramp signal required for the extraction of the V_{TH} and R_{ON} values. For performing on-wafer measurements, the usage of a simple waveform generator would be sufficient, thanks to the small parasitic capacitances of the DUTs. However, this solution is not viable for characterizing packaged devices due to the gate-to-source capacitances (C_{GS}) in the order of few nF [15]. For this reason, a custom gate driver circuit is required to prevent any distortion of the ramp signal, thus ensuring a fast and accurate V_{TH} extraction [14].

In off-state conditions, the DUT is stressed with a large drain voltage (V_{PH}), provided by a DC power supply, inducing both lateral and vertical trapping [21], while the on-state drain bias voltage (V_{PL}) is provided through an isolated DC/DC converter. The drain voltage is pulsed by means of a couple of NMOS (M_{PH} and M_{PL} in Figure 1) arranged in a

push–pull configuration, with an additional NMOS device (M_{PLL}) inserted for reducing the series resistance during DUT turn-on. A 0.1 Ω resistor (R_{SENSE}) is connected to the DUT's source terminal in order to extract the drain current (I_{DS}) while a clamping circuit (M_1, R_1, D_1) is connected to the drain terminal of the DUT for improving the measurement accuracy at low voltages. An additional NMOS (M_{DSC}) was placed between the DUT's drain terminal and GND in order to force the drain voltage to 0 V. This condition is required for monitoring the parameter recovery after the V_{PH} removal. The whole setup is controlled by a MicroController Unit (MCU) used for triggering the DSO acquisition with logarithmically spaced time steps [17] and for generating the necessary synchronization signals. Figure 2 illustrates a typical bias scheme for the circuit. Figure 3 shows the time sequence of the trigger signal used to activate the DSO acquisition.

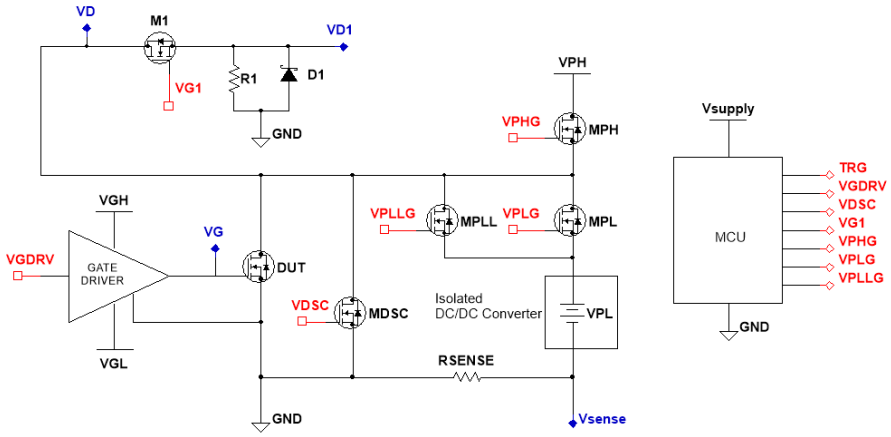
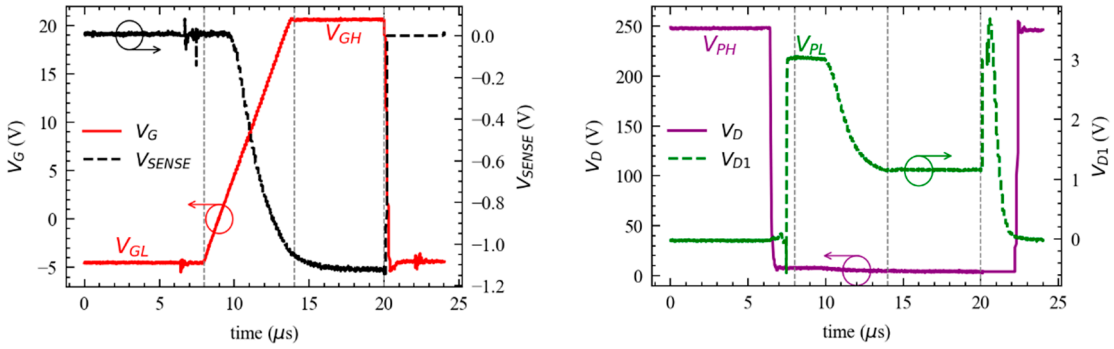


Figure 1. Setup schematic. The whole setup is controlled by an MCU used for triggering the DSO acquisition with logarithmic time steps and generating the necessary synchronization signals.



(**a**) (**b**)

Figure 2. (**a**) Gate voltage (V_G) is swept for extracting V_{TH} and a stable 20 V level is held at the end of the ramp to ensure a stable current and voltage level for a correct R_{ON} extraction. (**b**) V_D is monitored during the off-state stress phase, while V_{D1} is the signal provided by the clamping circuit (M_1, R_1, D_1).

The DSO used in this work was a four-channel PicoScope 5000 Series with 14-bit resolution and a 200 MHz maximum bandwidth. In this study, the rapid block mode was used for data acquisition in order to allow the log-like sampling required for monitoring the drifts over a large time interval.

Measurements were carried out with a 120 µs switching period and 10% Duty Cycle, i.e., by applying a gate bias rising from −5 V to 20 V in 6 µs, and staying at 20 V for the further 6 µs during the low-(drain)-voltage on-state time interval (see Figure 2a). In off-state conditions, a V_{PH} stress voltage is applied to the DUT, whereas in the on-state V_{PL} it is set to 3 V (see Figure 2b). V_{GL} is typically set to −5 V in order to prevent a false

turn-on and ensure the safe operation against voltage spikes on the gate [6]. During the 6 µs rising ramp, the I_{DS}–V_{GS} characteristic is reconstructed, allowing the extraction of the device V_{TH} using the extrapolation in the linear regime method [7,22]. To perform a correct R_{ON} extraction, at the end of the gate ramp, a stable V_{GH} level is held for 6 µs to compute R_{ON} as the ratio between the measured V_{D1} and I_{DS} averaged over the 6 µs range.

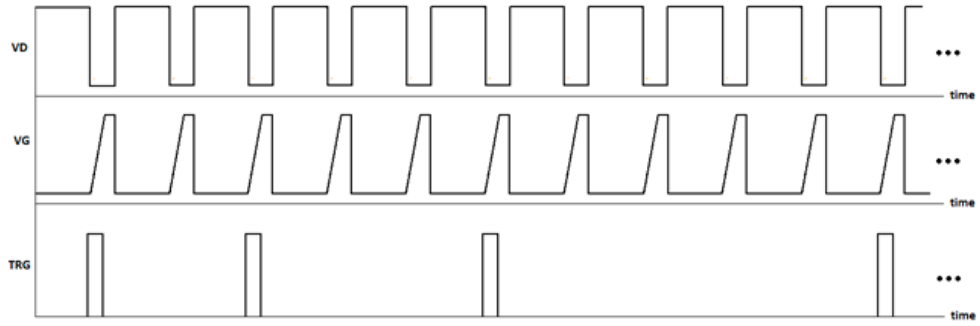


Figure 3. Typical measurement sequence: The Device Under Test (DUT) is repeatedly switched ON and OFF at each cycle, but the trigger signal (TRG) is generated only for some predefined periods logarithmically spaced in time. This avoids the DSO's memory saturation, preserving time accuracy.

The chosen I_{DS}–V_{GS} sweep rate represents the best compromise between speed and accuracy, since the short time required for the V_{TH} and R_{ON} measurement minimizes the fast recovery between stress phases but still provides enough samples for a correct I_{DS}–V_{GS} acquisition.

The DUTs were commercially available TO−247 packaged SiC MOSFETs based on a vertical structure for which a good measurement repeatability was found. Accordingly, we discuss the results obtained on a single device without loss of generality. The fresh I_{DS}-V_{GS} characteristic acquired with the custom setup is shown in Figure 4.

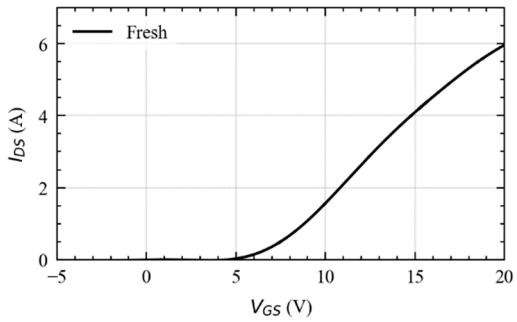


Figure 4. Fresh I_{DS}-V_{GS} characteristics for tested silicon carbide (SiC) MOSFET obtained with (V_{GL}; V_{GH}) = (−5 V; 20 V) and V_{PL} = 3 V.

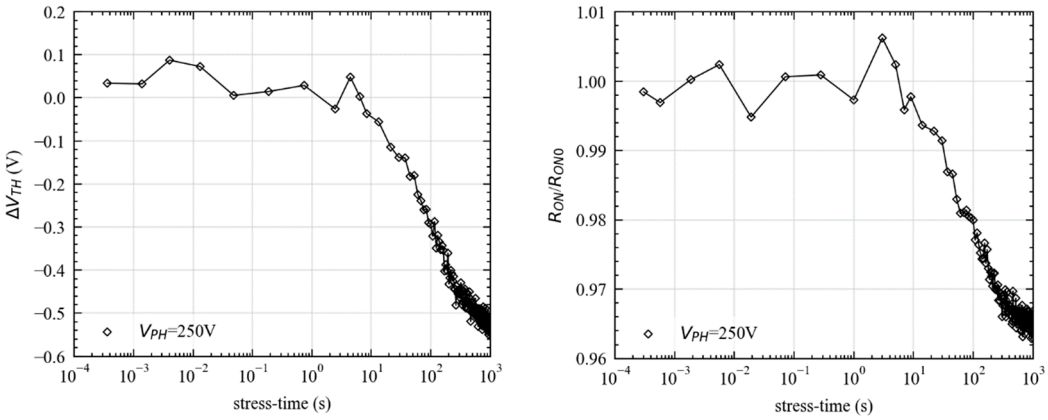
3. Results

In this section, we discuss the results obtained with the OTF characterization system presented in Section 2. The results are shown in terms of V_{TH} and R_{ON} drifts.

A sequence of no-stress acquisitions (i.e., V_{PH} = 0 V) is performed on fresh devices at the beginning of each characterization and the corresponding I_{DS}–V_{DS} curves were acquired to set a reference value (V_{TH0} and R_{ON0}) from which the relative drifts are evaluated. Then, the parameter evolution is monitored for 1000 s. ΔV_{TH} is simply calculated as (V_{TH}–V_{TH0}), whereas the acquired R_{ON} values are normalized with respect to the fresh value (R_{ON0}).

3.1. V_{TH} and R_{ON} Drifts

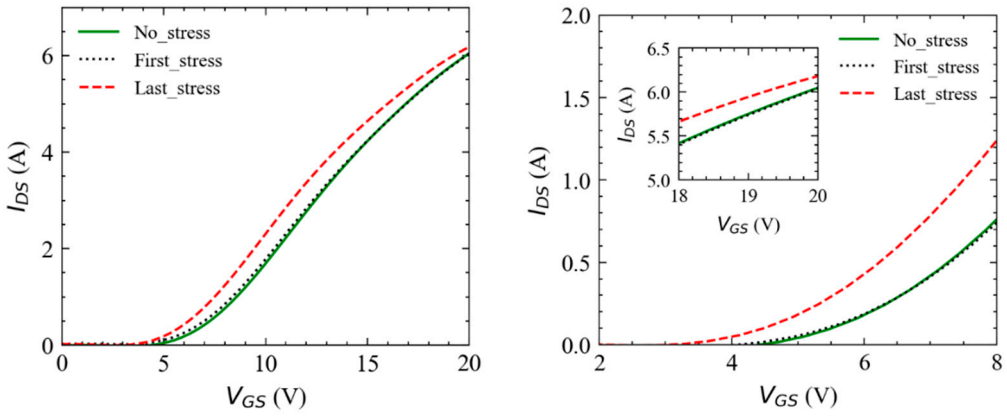
The data obtained during the OTF characterization are shown in Figure 5. As we can see in Figure 5a, a significant negative V_{TH} drift was observed only after several stress cycles (e.g., −0.55 V at 1000 s). The R_{ON} parameter evolution is shown in Figure 5b, in which a small benign negative shift of ≈−3.5% was observed after 1000 s stress.



(**a**) (**b**)

Figure 5. Results obtained with (V_{GL}; V_{GH}) = (−5 V; 20 V) and (V_{PL}; V_{PH}) = (3 V; 250 V). (**a**) ΔV_{TH} (i.e., V_{TH}–V_{TH0}). (**b**) Normalized R_{ON} variation (i.e., R_{ON}/R_{ON0}).

To gain further insights on the origin of these behaviors, we investigated the trans-characteristics (I_{DS}–V_{GS}) evolution during stress. Accordingly, in Figure 6, we report three transfer curves measured at some relevant time instants. That is, the green solid curves, referring to the fresh devices, are used as reference, while the black dotted and red dashed curves correspond to the first (≈110 µs) and to the last (1000 s) stress period, respectively.



(**a**) (**b**)

Figure 6. (**a**) I_{DS}–V_{GS} characteristics from which R_{ON} and V_{TH} were extracted. Reported curves were collected for 250 V off-state drain voltage in three different conditions: before stress (green solid lines), after the first stress period of ≈110 µs (black dotted curves), and after 1000 s stress (red dashed curves). (**b**) Detail of parameters drifts: V_{TH} moves towards the left after 1000 s of operation. The current increase observed in the triode region (see figure inset) is a signature of decreased R_{ON}.

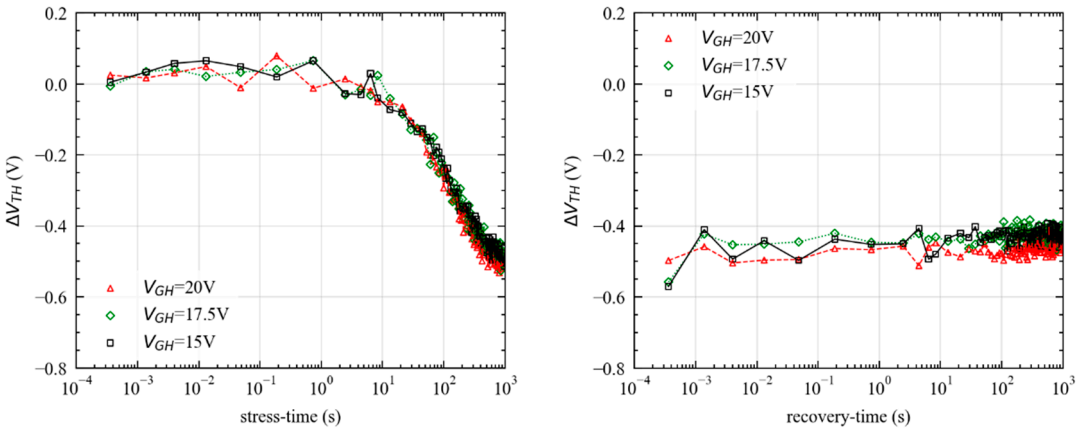
The parameter drifts shown in Figure 5 find consistent correspondence with the trans-characteristics drifts of Figure 6. No appreciable drifts were observed after the first stress period on both V_{TH} and R_{ON}, whereas non-negligible variations appeared after 1000 s of stress. A considerable triode-current variation (i.e., R_{ON} drift) is present in correspondence with the last stress cycle, in which a slight I_{DS} increase (see inset of Figure 6b) is a signature

of decreased R_{ON}. The negative V_{TH} shift observed in Figure 5a is consistent with the I_{DS} curve shift in Figure 6b after 1000 s. These negative drifts could be potentially explained by the presence of traps at the SiC/SiO_2 interface [18–20] and the long transients observed could be a signature of charge emission dynamics.

3.2. Effects of Measurement Conditions on the Parameter Drifts

In order to better understand the mechanism involved in the observed drifts, it is important to know the influence of the measurement conditions on the parameter drifts. To this end, the effects associated to (i) the gate-driving voltage provided in on-state (V_{GH}) and (ii) off-state drain voltage (V_{PH}) were investigated. With the aim of pursuing a deeper investigation, after 1000 s stress, an additional 1000 s measurement phase was inserted for monitoring the parameter recovery after the V_{PH} removal. During this additional phase, the V_{PH} bias is no longer applied to the DUT and the drain voltage in the off-state condition is set to 0 V. On the other hand, the same gate ramp (V_{GL}; V_{GH}) and low drain voltage (V_{PL}) are provided to the DUT for extracting V_{TH} and measuring R_{ON} in the triode region.

To highlight the V_{GH} effect on the observed drifts, the characterization was performed by ramping the gate voltage from −5 V to three different V_{GH} levels (15 V, 17.5 V, and 20 V), whereas the V_{PH} voltage was fixed to 100 V. The results obtained for the V_{TH} and R_{ON} parameters are shown in Figures 7 and 8, respectively.



(**a**) (**b**)

Figure 7. (**a**) Effect of gate voltage level (V_{GH}) on the V_{TH} drift during the stress with V_{PH} = 100 V. (**b**) Monitored V_{TH} recovery at different V_{GH} levels (15 V, 17.5 V, and 20 V) with V_{PH} = 100 V.

The transients observed for both V_{TH} and R_{ON} during the stress phase present similar time constants, suggesting a possible correlation between the two phenomena. Particularly, the observed negative V_{TH} drift should lead to an increase in device conductivity (at a fixed driving V_{GH}), thus yielding a R_{ON} reduction. The observed R_{ON} transient (Figure 8a) could thus be a directly correlated to the V_{TH} ones (Figure 7a), indicating the presence of a single underlying mechanism.

However, a different V_{GH} effect was observed for V_{TH} and R_{ON} transients during the stress phase. As shown in Figure 7a, the V_{TH} transients are not affected by the applied V_{GH}, while a reduction in the R_{ON} drift is observed for higher V_{GH}. This can actually be ascribed to the fact that at higher V_{GH}, the device transconductance (g_m) degrades [23], yielding a negligible impact on the overdrive voltage (i.e., V_{GS}–V_{TH}) variations on the device current and, consequently, on R_{ON}. On the other hand, at lower V_{GH}, variations in the V_{TH} affect the device current (i.e., R_{ON}), due to a less degraded g_m [23]. Accordingly, the R_{ON} variation increases with decreasing V_{GH} from 20 V to 15 V (see Figure 8a), even though the associated V_{TH} transients present negligible differences (i.e., the V_{TH} drift is the same). Concerning the recovery phase (see Figures 7b and 8b), both V_{TH} and R_{ON} drifts are unrecoverable in the considered time interval (i.e., 1000 s), independently on

the applied V_{GH} level. This observation can be explained in two ways. (i) The recovery transients could present time constants longer than 1000 s, thus making the employed time window insufficient for observing them; (ii) the applied V_{PH} stress (i.e., 100 V) does not affect the parameter drifts, and the observed instabilities can be totally ascribed to the gate switching applied during the OTF measurement. In fact, monitoring the device parameters in the recovery phase requires the gate voltage to be repeatedly switched from negative to positive and vice versa. As a consequence, the corresponding stress cannot be removed, making the second hypothesis more likely. To prove this point, the drain bias should be completely removed from the stress phase (V_{PH} = 0 V), thus monitoring the DUT behavior when just the V_{GS} stress is applied. Clearly, the results obtained with V_{PH} = 0 V do not mimic a real operative condition but are nonetheless useful to clarify the origin of the observed drifts.

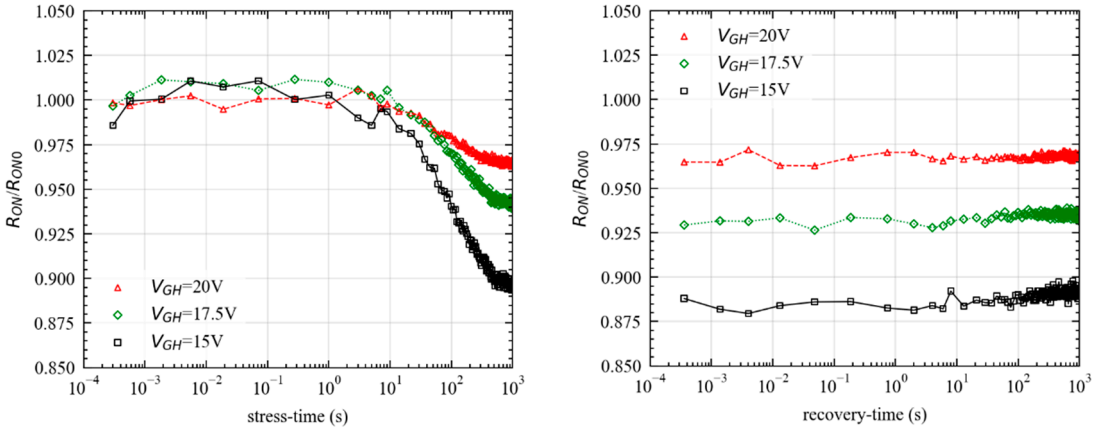


Figure 8. (**a**) Effect of gate voltage level (V_{GH}) on the R_{ON} drift during stress with V_{PH} = 100 V. At an increasing V_{GH}, the R_{ON} transient amplitude decreases. (**b**) Monitored R_{ON} recovery at different V_{GH} levels (15 V, 17.5 V, and 20 V) with V_{PH} = 100 V.

The results obtained with V_{PH} = 0 V are shown in Figure 9, in which the transients measured during the stress phase are compared with those obtained for V_{PH} = 100 V.

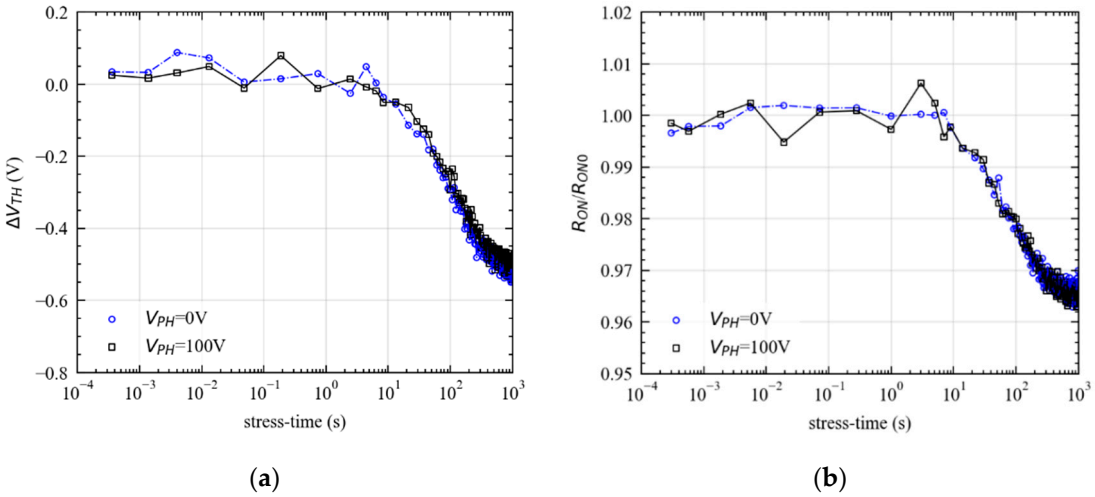


Figure 9. Comparison between (**a**) V_{TH} and (**b**) R_{ON} drift obtained with V_{PH} = 0 V and V_{PH} = 100 V.

The results shown in Figure 9 confirm our hypothesis, since no appreciable variation between the drifts measured with V_{PH} = 0 V and V_{PH} = 100 V was found, yielding nicely

overlapped transients. Accordingly, the observed drifts can be totally ascribed to the driving V_{GS}, at least for relatively low V_{PH} (i.e., 100 V). This result is consistent with the vertical structure presented by tested devices. In fact, the influence of the drain voltage on interface states is limited by the physical distance between the oxide and the drain contact, while the gate bias plays a major role on the V_{TH} stability [7–9]. However, thanks to the large breakdown voltage of SiC devices, the drain voltage applied in the off-state could be significantly higher than 100 V during a typical switching operation; thus, the complete absence of drain-induced instabilities cannot be ruled out. Accordingly, the V_{PH} role has to be studied for sufficiently high stress voltages to observe the corresponding effect.

We now investigate the V_{TH} and R_{ON} drifts at higher stress voltages (V_{PH}). To this end, it is important to keep the driving V_{GL} and V_{GH} constant in order to discern the gate/drain contributions. Accordingly, a gate voltage between −5 V and 20 V was applied to the DUT, consistently with the waveforms reported in Figure 2, while three different V_{PH} levels were considered (100 V, 250 V, and 500 V). A non-negligible V_{PH} effect is observed on the V_{TH} transients (Figure 10), whereas the corresponding R_{ON} drifts present a weak dependence on the applied V_{PH} (see Figure 11).

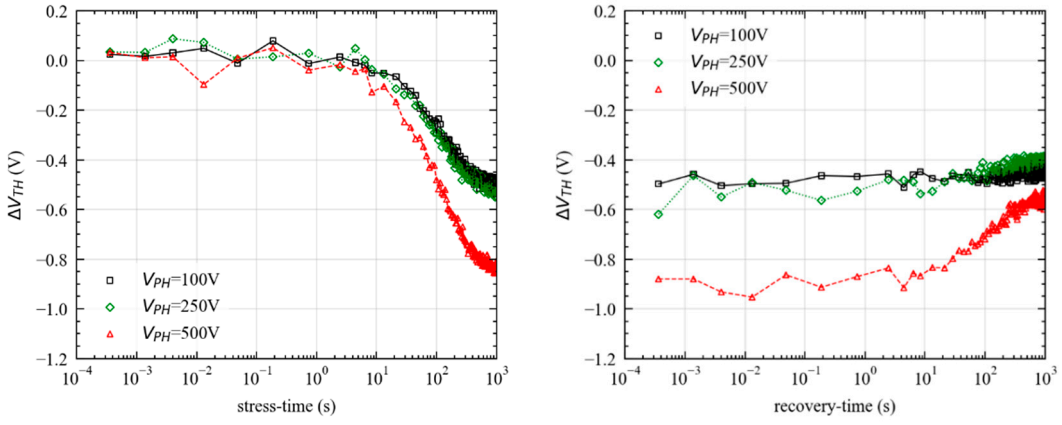


Figure 10. (**a**) Effect of drain off-state stress voltage (100 V, 250 V, and 500 V) on the V_{TH} drift with V_{GH} = 20 V. (**b**) Monitored V_{TH} recovery after V_{PH} removal (V_{GH} = 20 V).

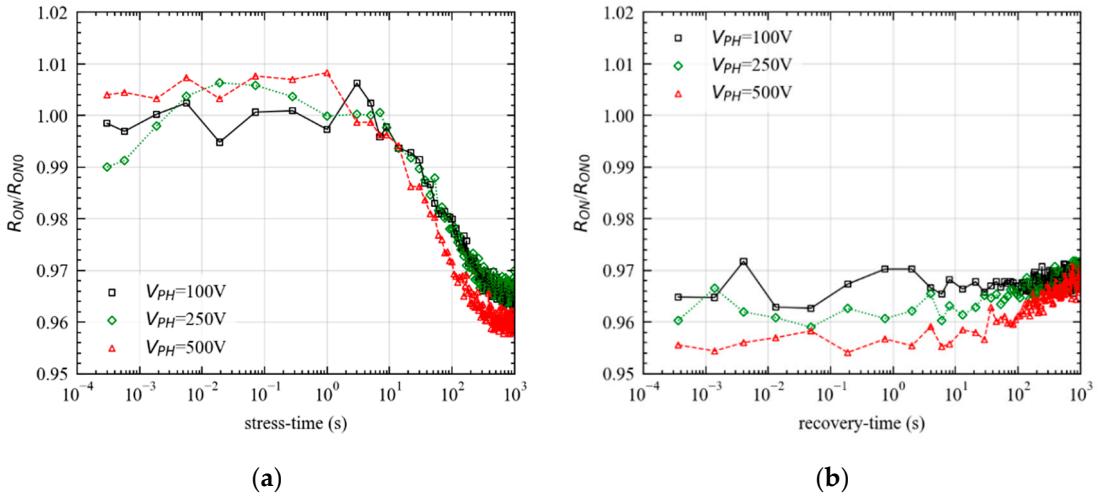
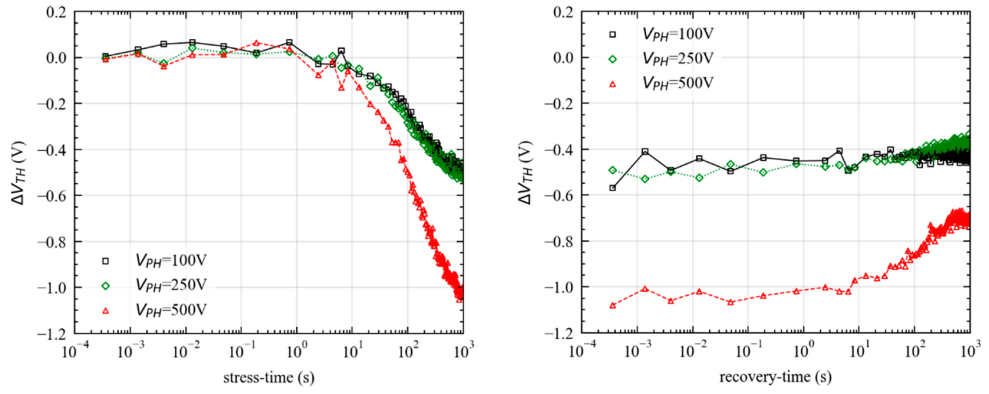


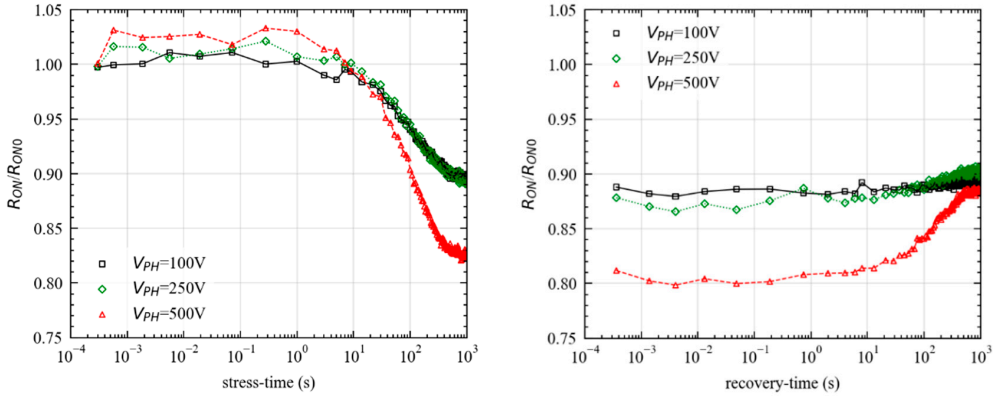
Figure 11. (**a**) Effect of drain off-state stress voltage (100 V, 250 V, and 500 V) on the R_{ON} drift during the stress with V_{GH} = 20 V. At an increasing stress voltage, the R_{ON} drift retained after 1000 s does not change significantly. (**b**) Monitored R_{ON} recovery for different drain stress voltages.

Negligible differences were observed on the V_{TH} transients measured at 100 V and 250 V, whereas the negative V_{TH} shift is more pronounced at V_{PH} = 500 V (Figure 10a), indicating that the off-state stress voltage plays a role to some extent. Interestingly, this additional drift is recoverable within 1000 s from the V_{PH} removal (see Figure 10b), indicating that negative BTI (NBTI) effects are non-permanent and are enhanced by high V_{PH} values. The fact that stress and recovery transients have similar time constants suggests that both mechanisms are governed by two similar and opposite slow processes. Moreover, no recovery was observed for V_{PH} = 100 V and V_{PH} = 250 V, confirming that lower off-state stress voltages do not produce any additional instability with respect to that induced by the gate potential. On the other hand, as shown in Figure 11, the slow R_{ON} transients observed in the range between 1 s and 1000 s present negligible V_{PH} dependence and just a weak recovery appears at V_{PH} = 500 V (at least within 1000 s from the stress removal, as discussed in Section 3.1). This result is consistent with the V_{GH} dependence previously investigated, indicating that the large gate bias applied in this phase (i.e., V_{GH} = 20 V) makes the device current less sensitive to the V_{TH} variations. In fact, the maximum R_{ON} dynamics was observed at V_{GH} = 15 V (see Figure 7a), indicating that this condition is optimal to highlight the V_{PH} effect even on the R_{ON} parameter. Accordingly, a new set of measurements was taken for a gate voltage ranging between V_{GL} = −5 V and V_{GH} = 15 V, exploring the same V_{PH} levels used previously (100 V, 250 V, and 500 V). The corresponding V_{TH} and R_{ON} drifts are reported in Figures 12 and 13, respectively.



(**a**) (**b**)

Figure 12. (**a**) Effect of drain off-state stress voltage (100 V, 250 V, and 500 V) on the V_{TH} drift during the stress with V_{GH} = 15 V. At V_{PH} = 500 V, the negative V_{TH} drift retained after 1000 s increases. (**b**) Monitored V_{TH} recovery at different drain stress voltages.



(**a**) (**b**)

Figure 13. (**a**) Effect of drain off-state stress voltage on the R_{ON} drift during the stress with V_{GH} = 15 V. The R_{ON} drift retained after 1000 s increases for V_{PH} = 500 V. (**b**) Monitored R_{ON} recovery at different drain stress voltages (100 V, 250 V, and 500 V) with V_{GH} = 15 V.

Once again, the negative V_{TH} shift observed at V_{PH} = 500 V is stronger with respect to that measured at lower V_{PH} (Figure 12a). At the same time, the R_{ON} drift clearly changes from −10% to −17% while passing from 250 V to 500 V, showing the same V_{PH} dependence observed on V_{TH} (compare Figures 12a and 13a). The fact that similar trends were observed on both V_{TH} and R_{ON} degradation confirms that the observed instabilities share the same origin. Particularly, the R_{ON} drift is a direct consequence of the V_{TH} one, since at V_{GH} = 15 V, the less degraded g_m [23] makes the device current (i.e., R_{ON}) highly sensitive on the overdrive voltage (i.e., V_{GH}–V_{TH}). Accordingly, the significant impact of the drain stress voltage observed on V_{TH} yields an additional R_{ON} drift at V_{PH} = 500 V, whereas a negligible effect is observed at 100 V and 250 V.

Further evidence of the V_{PH} role is given by the partial recovery observed after 500 V stress. Almost no recovery was observed after the stress performed at 100 V and 250 V, whereas the recovery transients appear for both R_{ON} and V_{TH} at 500 V. In fact, after the V_{PH} removal, the drain-induced instabilities can be recovered, whereas the gate-induced ones are still present, yielding a residual drift in V_{TH} and $R_{ON.}$ Accordingly, the recovery monitoring can be used to isolate the drain-induced instabilities from the gate-related ones, whereas the effect of the gate-driving voltage can be observed by reducing (or by possibly removing) $V_{PH.}$

4. Conclusions and Recommendations

The developed measurement technique is able to highlight V_{TH} and R_{ON} drifts in packaged SiC power devices. The observed slow negative V_{TH} shift was associated with the presence of traps at the SiC–SiO_2 interface. A direct correlation between V_{TH} and R_{ON} drifts was first speculated and then verified. To this end, the impacts of the gate-driving voltage (V_{GH}) and of the off-state stress drain voltage (V_{PH}) were separately investigated. At a relatively low V_{PH} (i.e., 100 V), the drifts can be totally ascribed to the repeated switching of the gate signal, whereas the V_{PH} influence could be observed only at 500 V. This result is consistent with the vertical structure of tested devices, for which the gate potential is expected to mainly affect the dynamics of traps at the oxide–semiconductor interface. In order to observe drain-related effects in vertical devices, it is thus recommended to apply a large off-state stress voltage (V_{PH}), which was limited to 500 V in this study. The outcomes obtained with the developed system are instrumental to reveal the mechanisms limiting device stability and performance, by discerning the gate/drain contribution on the parameter degradation. To get a better insight into gate-related effects, in future works, we will investigate other bias combinations, and we will study the effect of the negative gate voltage applied in the off-state (V_{GL}). Moreover, the capabilities of the designed setup will be further enhanced by including hard-switching characterization, which will be used to highlight the effect of the transitions when SiC devices are driven in more severe switching conditions.

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References

1. Kimoto, T.; Cooper, J.A. *Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications*; Wiley: Singapore, 2014.
2. Ouaida, R.; Berthou, M.; Leon, J.; Perpina, X.; Oge, S.; Brosselard, P.; Joubert, C. Gate oxide degradation of SiC MOSFET in switching conditions. *IEEE Electron. Device Lett.* **2014**, *35*, 1284–1286. [CrossRef]
3. Wei, J.; Liu, S.; Lou, R.; Tang, L.; Ye, R.; Zhang, L.; Zhang, X.; Sun, W.; Bai, S. Investigation on the Degradation Mechanism for SiC Power MOSFETs under Repetitive Switching Stress. *IEEE J. Emerg. Sel. Top. Power Electron.* **2019**, 1. [CrossRef]
4. Yang, S.; Lu, T.; Liu, S.; Wang, H.; Liu, C.; Chen, K.J. Impact of Vth shift on Ron in E/D-mode GaN-on-Si power transistors: Role of dynamic stress and gate overdrive. In Proceedings of the 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Prague, Czech Republic, 12–16 June 1016; pp. 263–266.
5. Guevara, E.; Herrera-Pérez, V.; Rocha, C.; Guerrero, K. Threshold voltage degradation for n-channel 4H-SiC power MOSFETs'. *JLPEA* **2020**, *10*, 3. [CrossRef]
6. Hua, M.; Wei, J.; Bao, Q.; Zhang, Z.; Zheng, Z.; Chen, K.J. Dependence of VTH stability on gate-bias under reverse-bias stress in E-mode GaN MIS-FET. *IEEE Electron Device Lett.* **2018**, *39*, 413–416. [CrossRef]
7. Gurfinkel, M.; Suehle, J.; Bernstein, J.; Shapira, Y.; Lelis, A.; Habersat, D.B.; Goldsman, N. Ultra-fast measurements of VTH instability in SiC MOSFETs due to positive and negative constant bias stress. In Proceedings of the 2006 IEEE International Integrated Reliability Workshop Final Report, South Lake Tahoe, CA, USA, 16–19 October 2006; pp. 49–53.
8. Lelis, A.J.; Green, R.; Habersat, D.B.; Goldsman, N. Effect of threshold-voltage instability on SiC DMOSFET reliability. In Proceedings of the 2008 IEEE International Integrated Reliability Workshop Final Report, South lake Tahoe, CA, USA, 12–16 October 2008; pp. 72–76.
9. Ghosh, A.; Hao, J.; Cook, M.; Kendrick, C.; Suliman, S.A.; Hall, G.D. Studies of bias temperature instabilities in 4H-SiC DMOSFETs. In Proceedings of the 2020 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 28 April 2020; pp. 1–4.
10. Schrock, J.A.; Pushpakaran, B.N.; Bilbao, A.V.; Ray, W.B.; Hirsch, E.A.; Kelley, M.D.; Holt, S.L.; Bayne, S.B. Failure analysis of 1200-V/150-A SiC MOSFET under repetitive pulsed overcurrent conditions. *IEEE Trans. Power Electron.* **2016**, *31*, 1816–1821. [CrossRef]
11. Calderon-Lopez, G.; Forsyth, A. High power density DC-DC converter with SiC MOSFETs for electric vehicles. In Proceedings of the 7th IET International Conference on Power Electronics, Machines and Drives (PEMD 2014); Institution of Engineering and Technology, Manchester, UK, 8–10 April 2014; p. 1.
12. Habersat, D.B.; Lelis, A.J.; Green, R. Measurement considerations for evaluating BTI effects in SiC MOSFETs. *Microelectron. Reliab.* **2018**, *81*, 121–126. [CrossRef]
13. Berens, J.; Weger, M.; Pobegen, G.; Aichinger, T.; Rescher, G.; Schleich, C.; Grasser, T. Similarities and differences of BTI in SiC and Si power MOSFETs. In Proceedings of the 2020 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 28 April 2020; pp. 1–7.
14. Lelis, A.J.; Habersat, D.; Green, R.; Ogunniyi, A.; Gurfinkel, M.; Suehle, J.; Goldsman, N. Time dependence of bias-stress-induced SiC MOSFET threshold-voltage instability measurements. *IEEE Trans. Electron Devices* **2008**, *55*, 1835–1840. [CrossRef]
15. Sheng, H.; Chen, Z.; Wang, F.; Millner, A.R. Investigation of 1.2 kV SiC MOSFET for high frequency high power applications. In Proceedings of the 2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Palm Springs, CA, USA, 21–25 February 2010; pp. 1572–1577.
16. Mori, Y.; Hisamoto, D.; Tega, N.; Matsumura, M.; Yoshimoto, H.; Shima, A.; Shimamoto, Y. Effects of interface properties in SiC MOSFETs on reliability. In Proceedings of the 2015 IEEE 22nd International Symposium on the Physical and Failure Analysis of Integrated Circuits, Hsinchu, Taiwan, 29 June–2 July 2015; pp. 68–71.
17. Chini, A.; Iucolano, F. Evolution of on-resistance (RON) and threshold voltage (VTH) in GaN HEMTs during switch-mode operation. *Mater. Sci. Semicond. Process.* **2018**, *78*, 127–131. [CrossRef]
18. Kwietniewski, N.; Piotrowski, T.; Gutt, T.; Piotrowska, A.; Gołaszewska, K.; Rzodkiewicz, W.; Sochacki, M.; Szmidt, J. Oxidation process of SiC by RTP technique. *Mater. Sci. Forum* **2009**, *615–617*, 529–532. [CrossRef]
19. Lelis, A.J.; Green, R.; Habersat, D.B.; El, M. Basic mechanisms of threshold-voltage instability and implications for reliability testing of SiC MOSFETs. *IEEE Trans. Electron. Devices* **2015**, *62*, 316–323. [CrossRef]
20. Lelis, A.J.; Green, R.; Habersat, D.B. SiC MOSFET threshold-stability issues. *Mater. Sci. Semicond. Process.* **2018**, *78*, 32–37. [CrossRef]
21. Meneghini, M.; Vanmeerbeek, P.; Silvestri, R.; Dalcanale, S.; Banerjee, A.; Bisi, D.; Zanoni, G.; Meneghesso, G.; Moens, P. Temperature-dependent dynamic RON in GaN-bMIS-HEMTs: Role of surface traps and buffer leakage. *IEEE Trans. Electron. Devices* **2015**, *62*, 782–787. [CrossRef]
22. Ortiz-Conde, A.; Sánchez, F.G.; Liou, J.; Cerdeira, A.; Estrada, M.; Yue, Y. A review of recent MOSFET threshold voltage extraction methods. *Microelectron. Reliab.* **2002**, *42*, 583–596. [CrossRef]
23. Islam, M.S.; Akanda, R.K.; Anwar, S.; Shahriar, A. Analysis of resistances and transconductance of SiC MESFET considering fabrication parameters and mobility as a function of temperature. In Proceedings of the International Conference on Electrical & Computer Engineering (ICECE 2010), Dhaka, Bangladesh, 18–20 December 2010; pp. 5–8.