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Unity-Gain Zero-Offset CMOS Buffer with Improved Feedforward Path

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Abstract: A voltage unity-gain zero-offset CMOS amplifier with reduced gain error and increased PSRR (power supply rejection ratio) is proposed. The amplifier uses two feed mechanisms, negative feedback and supporting positive feedforward, to achieve low deviation from unit gain over the entire input range. The circuit, designed in a standard 180-nanometer 1.8-voltage CMOS process, is compared with two known buffers of similar topology, also designed in the same process. Simulations show that, with the same supply (1.8 V), power (1.2 mW), load (12 pF), bandwidth (50 MHz), and similar area (600 μm^2), the proposed buffer achieves the lowest gain error (0.3%) and the highest PSRR (72 dB).

Keywords: CMOS analogue circuits; buffer amplifier; unity-gain voltage amplifier; CMOS integrated circuits

1. Introduction

A unity-gain buffer is an analogue amplifier with a voltage gain equal to 1 V/V. Among these amplifiers there are unity-gain zero-offset buffers characterized by zero offset between input and output voltages [1–8]. Unity-gain zero-offset buffers have found application in the testing of analogue chips [8], in analogue filtering [9–11], oscillators [12], voltage regulators [13,14], and in LCD panels [15,16]. Most of these buffer solutions use the classic approach based on a high-gain differential amplifier and a negative feedback to obtain unity gain and zero offset. A representative example of the classic approach is the Miller opamp (operational amplifier) with an output connected to an inverting input (Figure 1a). The advantages of this buffer solution are its relatively simple design, wide input voltage range, and its full compatibility with standard CMOS technologies. Furthermore, since the Miller OpAmp has a high open-loop gain for differential-mode signals, a buffer gain can be very close to 1 V/V. To further reduce the gain error, it was proposed in [1] to use also a common-mode signal. In this case, a common-mode signal component is forwarded from the input to the output along an additional path. Such a feedforward path for a common-mode signal can be relatively simple to implement by using only one n-channel transistor (M_6 in Figure 1b). A limitation of such a solution is the need for using an n-channel transistor without the body effect, which is not available in standard CMOS processes. In this paper, an improvement of the solution of [1] is proposed (Figure 1c), which gives substantially reduced gain error, improved PSRR, and full applicability in standard CMOS technologies.

The circuits in Figure 1a–c are studied and the impact on circuit performance from introducing a common-mode feedforward path is examined. To make this study meaning-ful, key parameters, such as power consumption, load capacitance, bandwidth, and layout area, are assumed to be similar in all three circuits. The results of theoretical analyses and simulations, followed by discussion assuming the circuits realization in 180-nm 1.8-V process of austriamicrosystems AG (ams AG), are presented in the following sections.
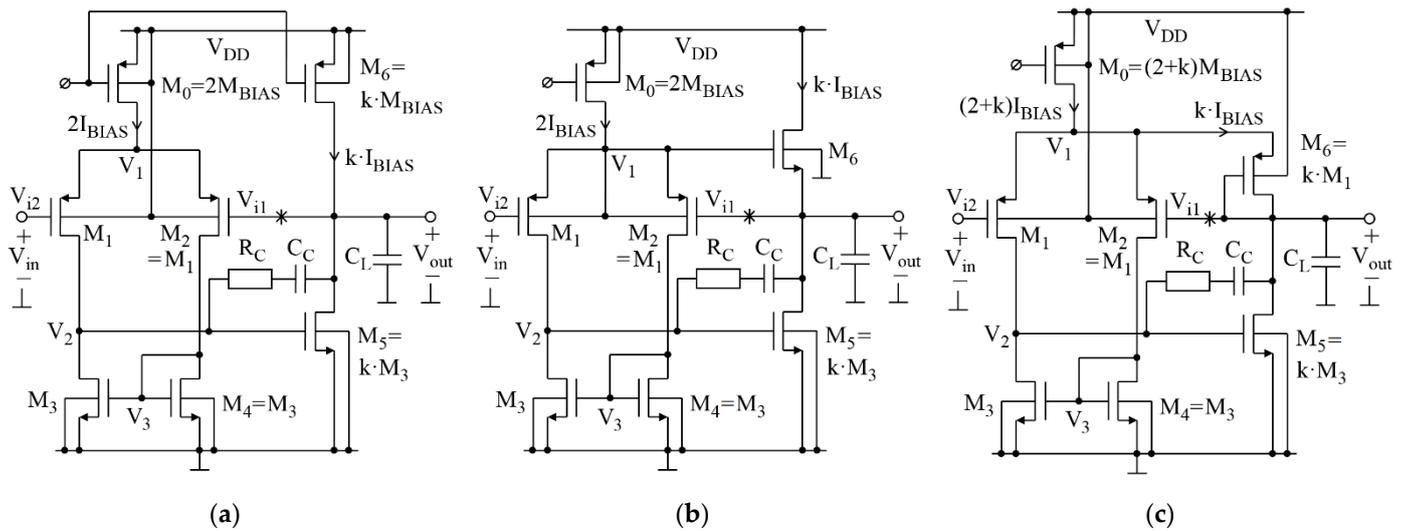
Figure 1. Unity-gain zero-offset buffers: (**a**) classic; (**b**) based on [1]; (**c**) proposed.

2. Theoretical Analysis

The circuits in Figure 1a–c are closed-loop differential amplifiers with two stages. The first stage is exactly the same in all cases and is composed of the transistors M_1-M_4. The second stage in Figure 1a,b consists of M_5 loaded by M_6. In Figure 1c, the second stage can be identified as M_5 loaded by the series connection of M_6 and M_1-M_2. The transistors are sized so that the first and second stages are biased at $2I_{BIAS}$ and kI_{BIAS}, respectively.

Each circuit has a traditional negative feedback loop (the loop breaking point is marked by the symbol *) operating on a differential-mode component of the input signal $(V_{i1} - V_{i2})$. The circuits in Figure 1b,c also have a positive feedforward loop operating with the common-mode component, $(V_{i1} + V_{i2})/2$. The common-mode component is generated at node V_1 by the differential pair and is transferred to the output by M_6.

In the following analysis, the common-mode signal at node V_2 is omitted because it is suppressed by the first stage due to its symmetry (owing to CMRR).

When the negative feedback loop is opened (broken in the point *), the output small-signal voltage can be determined using the superposition principle [1]

$$V_{out} = A_D \cdot (V_{i1} - V_{i2}) + A_C \cdot \frac{V_{i1} + V_{i2}}{2} \tag{1}$$

where A_D and A_C are the small-signal gains for the differential- and common-mode components, respectively.

$$A_D = \left. \frac{V_{out}}{V_{i1} - V_{i2}} \right|_{V_{i1}+V_{i2}=0} \tag{2}$$

$$A_C = \left. \frac{V_{out}}{(V_{i1} + V_{i2})/2} \right|_{V_{i1}-V_{i2}=0} \tag{3}$$

After closing the loop ($V_{i1} = V_{out}$, $V_{i2} = V_{in}$) the voltage gain becomes

$$\frac{V_{out}}{V_{in}} = 1 - \frac{1 - A_C}{1 - A_D - A_C/2} \cong 1 - \frac{1 - A_C}{-A_D} \tag{4}$$

Equation (4) indicates that, as A_C is close to 1, the gain error is significantly reduced even though A_D is reduced.

The result of applying the superposition principle (1) to each of the circuits in Figure 1a–c is shown in the corresponding diagrams in Figure 2a–c.
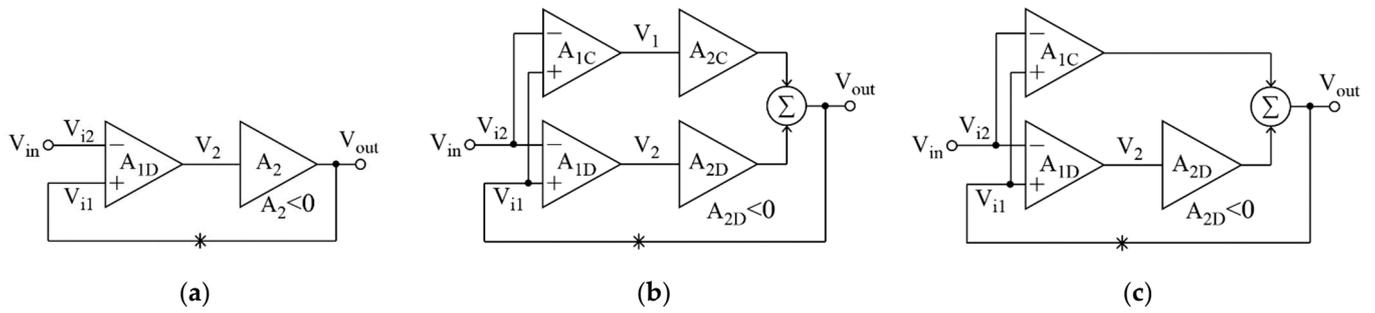
Figure 2. Block diagrams of circuits: (**a**) in Figure 1a; (**b**) in Figure 1b; (**c**) in Figure 1c.

2.1. Gain Error in the Classic Buffer

The circuit in Figure 1a processes only the differential-mode component due to the CMRR effect, as mentioned earlier. This means that $A_C = 0$ and $A_D = A_{1D} \cdot A_2$, where A_{1D} and A_2 are the gains of the first and the second stage, respectively,

$$A_{1D} = \left. \frac{V_2}{V_{i1} - V_{i2}} \right|_{V_{i1} + V_{i2} = 0} = \frac{g_{m1,2}}{g_{ds1,2} + g_{ds3,4}} \tag{5}$$

where $g_{m1,2} = g_{m1} = g_{m2}$, $g_{ds1,2} = g_{ds1} = g_{ds2}$, $g_{ds3,4} = g_{ds3} = g_{ds4}$, and

$$A_2 = \frac{V_{out}}{V_2} = -\frac{g_{m5}}{g_{ds5} + g_{ds6}} \tag{6}$$

Thus

$$\frac{V_{out}}{V_{in}} = 1 - \frac{1}{-A_{1D}A_2} = 1 - \frac{g_{ds5} + g_{ds6}}{A_{1D}g_{m5}} \tag{7}$$

The gain error in (7) can be relatively small because the product $|A_{1D} \cdot A_2|$ ranges from 10^2 to 10^3, depending on I_{BIAS} and transistor sizes.

2.2. Gain Error in the Buffer of Figure 1b

The circuit in Figure 1b processes differential- and common-mode components, as shown in Figure 2b. The differential signal path (A_{1D} followed by A_{2D}) is the same as in the classic circuit, but the gain of the second stage (A_{2D}) is lower and is close to -1.

$$A_{2D} = \left. \frac{V_{out}}{V_2} \right|_{V_{i1} + V_{i2} = 0} = -\frac{g_{m5}}{g_{m6} + g_{mb6} + g_{ds6} + g_{ds5}} \underset{\substack{g_m \gg g_{ds} \\ g_{mb} \gg g_{ds}}}{\cong} -\frac{g_{m5}}{g_{m6} + g_{mb6}} \tag{8}$$

The common-mode signal passes, firstly, through the differential pair to node V_1 and, next, through the source follower M_6 to the buffer output. The particular gains of the common-mode feedforward path are

$$A_{1C} = \left. \frac{V_1}{(V_{i1} + V_{i2})/2} \right|_{V_{i1} - V_{i2} = 0} = \frac{g_{m1,2}}{g_{m1,2} + g_{ds1,2} + g_{ds0}} \underset{g_m \gg g_{ds}}{\cong} 1 \tag{9}$$

and

$$A_{2C} = \left. \frac{V_{out}}{V_1} \right|_{V_{i1} - V_{i2} = 0} = \frac{g_{m6}}{g_{m6} + g_{mb6} + g_{ds6} + g_{ds5}} \underset{\substack{g_m \gg g_{ds} \\ g_{mb} \gg g_{ds}}}{\cong} \frac{g_{m6}}{g_{m6} + g_{mb6}} \cong 0.8 \tag{10}$$

where A_{2C} is the gain of the follower M_6. Note that in a typical CMOS process, A_{2C} is about 0.8 V/V, because the transconductance ratio in M_6 (g_{mb6}/g_{m6}) is close to 0.2. Therefore,

the common-mode signal is forwarded to the buffer output with a gain less than 1 ($A_C = A_{1C} \cdot A_{2C} < 1$).

Hence, the buffer gain is

$$\frac{V_{out}}{V_{in}} = 1 - \frac{1 - A_{1C}A_{2C}}{-A_{1D}A_{2D}} = 1 - \frac{g_{mb6}}{A_{1D}g_{m5}} \tag{11}$$

As A_{1D} and g_{m5} in (11) are the same as in (7), the gain error is larger than in the classic solution because of the body effect of M_6 (because g_{mb6} is larger than $g_{ds6} + g_{ds5}$).

2.3. Gain Error in the Proposed Buffer

In the proposed buffer (Figure 1c), the NMOS source follower (M_6) is replaced by a PMOS voltage shifter, i.e., the diode-connected PMOS FET. Thus, the body effect of M_1-M_2 and M_6 cancels each other out, and the common-mode component is transferred to the output with a gain theoretically equal to 1,

$$A_{1C} = \left.\frac{V_{out}}{(V_{i1} + V_{i2})/2}\right|_{V_{i1}-V_{i2}=0} \underset{\substack{g_m \gg g_{ds} \\ g_{mb} \gg g_{ds}}}{\cong} \frac{1 + g_{mb6}/g_{m6}}{1 + g_{mb1,2}/g_{m1,2}} = \frac{1 + (k \cdot g_{mb1,2})/(k \cdot g_{m1,2})}{1 + g_{mb1,2}/g_{m1,2}} = 1 \tag{12}$$

Furthermore, the gain of the differential path is higher than that of the circuit in Figure 1b, as M_5 is loaded by a higher resistance resulting from the series connection of M_6 and M_1-M_2.

$$A_{2D} \underset{\substack{g_m \gg g_{ds} \\ g_{mb} \gg g_{ds}}}{\cong} -\frac{g_{m5}}{g_{m6}}\left(1 + \frac{g_{m6} + g_{mb6}}{g_{m1,2} + g_{mb1,2}}\right) = -\frac{g_{m5}}{g_{m6}}(1 + k) \tag{13}$$

Thus

$$\frac{V_{out}}{V_{in}} = 1 - \frac{1 - A_{1C}}{-A_{1D}A_{2D}} = 1 - \frac{\frac{g_{m6}}{1+k}}{A_{1D}g_{m5}}(1 - A_{1C}) = 1 \tag{14}$$

Comparing (14) and (7), it can be seen that the gain error of the proposed solution can be lower than the classic one due to the fact that A_{1C} is 1.

2.4. Output Resistance

The output resistances (R_{out}) of the considered buffers are practically the same as it is determined mainly by g_{m5} and A_{1D}. In detail, the output resistance of the classic buffer is

$$R_{out} = \frac{1}{g_{ds5} + g_{ds6}} \cdot \frac{1}{1 - A_{1D}A_2} = \frac{1}{g_{m5}A_{1D} + g_{ds5} + g_{ds6}} \cong \frac{1}{g_{m5}A_{1D}} \tag{15}$$

For the buffer of [1] it is

$$R_{out} \cong \frac{1}{g_{m5}A_{1D} + (g_{m6} + g_{mb6})/2} \cong \frac{1}{g_{m5}A_{1D}} \tag{16}$$

And, for the proposed one the output resistance is

$$R_{out} \cong \frac{1}{g_{m5}A_{1D} + g_x/2} \cong \frac{1}{g_{m5}A_{1D}} \tag{17}$$

where $1/g_x \cong 1/(g_{m6} + g_{mb6}) + 0.5/(g_{m1,2} + g_{mb1,2})$.

2.5. Power Supply Rejection Ratio

Supply interference paths, from V_{DD} to V_{out}, are different in each of the buffers. In the buffer in Figure 1a, V_{DD} interference passes to V_{out} in three ways: through M_0 (g_{ds0}), $M_{1,2}$ (bulk), and M_6 (g_{ds6}). The output conductance of M_6 (g_{ds6}) together with R_{out}

form a resistive divider. Since $1/g_{ds6} >> R_{out}$, interference passing through g_{ds6} to V_{out} is suppressed. V_{DD} interference passing through M_0 and $M_{1,2}$ is attenuated in the first stage, owing to CMRR.

In the circuit in Figure 1b, as $M_{1,2}$ bulk is not connected to V_{DD}, the supply interference passes in two ways: through M_0 (g_{ds0}) and M_6 (g_{ds6}). Interference that passes through g_{ds6} is suppressed, similar to Figure 1a. Nevertheless, the interference that passes through g_{ds0} is not suppressed at all because the follower M_6 transfers it from node V_1 directly to V_{out}. Since V_1 interference is at a comparable level to that in the circuit of Figure 1a, the feedforward path formed by M_6 causes PSRR degradation.

In the buffer in Figure 1c, V_{DD} interference goes in one way only, through g_{ds0}, because transfer through $M_{1,2}$ and M_6 bulks is suppressed due to the body effect compensation, as mentioned earlier. Interference from V_{DD} passes through g_{ds0} to V_1 and, next, this interference is transferred by the shifter M_6 directly to V_{out}. However, in opposite to Figure 1b, M_6 is a diode-connected transistor and, thereby, its conductance (g_{m6}), together with $g_{ds0}, g_{m1,2}$ and R_{out}, compose a divider that substantially attenuates V_1 interference. As a result, the level of V_1 interference in the circuit in Figure 1c is much lower than in Figure 1a. Since there is no another path of interference, a higher PSRR than in the circuit in Figure 1a can be obtained. Above conclusions are confirmed by simulation results in the next section where detailed values of PSRR of each of the buffers are presented in a performance summary.

3. Simulations

The example designs of the buffers in Figure 1a–c were made for testing analogue chips (for buffering and monitoring internal analogue nodes). Therefore, a C_L of 12 pF is assumed as it is a capacitance of a typical oscilloscope probe (also such value of C_L was used in [1]). The transistor scaling factor k is set to five due to Miller compensation requirements. In a practical two-stage opamp, proper compensation is possible when the transconductance of a second stage is at least five times larger than in a first stage. I_{BIAS} is set to 100 µA, which results from limiting the power supply to 1 mW at a supply voltage of 1.8 V. The sizes of the transistors are given in Table 1. The 1.8-voltage standard-V_{TH} transistors with $V_{THP} \approx -0.4$ V and $V_{THN} \approx 0.45$ V were used.

Table 1. Transistors sizes (W/L in µm/µm) and values of R_C and C_C.

	Figure 1a	Figure 1b	Figure 1c
M_0	$2 \times 20/0.25$	$2 \times 20/0.25$	$(5+2) \times 20/0.25$
M_1, M_2	$10/0.25$	$10/0.25$	$10/0.25$
M_3, M_4	$10/0.25$	$10/0.25$	$10/0.25$
M_5	$5 \times 10/0.25$	$5 \times 10/0.25$	$5 \times 10/0.25$
M_6	$5 \times 20/0.25$	$5 \times 10/0.25$	$5 \times 10/0.25$
$R_C/C_C/C_L$	2.8 kΩ/2.5 pF/12 pF	2.4 kΩ/1.4 pF/12 pF	2.6 kΩ/1.9 pF/12 pF

The buffers were compensated to obtain similar -3-dB frequencies in small-signal characteristics (Figure 3a) as well as minimal overshoots under pulse excitation (Figure 3b). The applied values of the compensating elements, R_C and C_C, are given in Table 1. Some small overshoot still exists in the classical buffer impulse response, and of course this can be suppressed, but then the -3-dB frequency will be lower. The circuit of [1] features the best positive slew rate (SR+), but it results from the fact that the increase in gain error causes an increase in I_{DS6} (the larger the difference in $V_{in} - V_{out}$, the larger V_{GS6} becomes).

The detailed characteristic of the gain error can be determined directly from a derivative of the static responses in Figure 4a. The gain error is the deviation of the derivative from 1, i.e., *gain error* = $\mathrm{d}V_{out}/\mathrm{d}V_{in} - 1$. The plots of derivatives presented in Figure 4b show that, for low V_{in}, the classic solution has the smallest gain error. However, the gain error integrated across the entire available input range is the smallest in the proposed circuit (the available ranges are marked in Figure 4b and are determined by the boundaries

beyond which the derivatives sharply change their value). The integrated gain errors are 1.2%, 2.3%, and 0.3% for the classic, from [1], and proposed circuits, respectively.
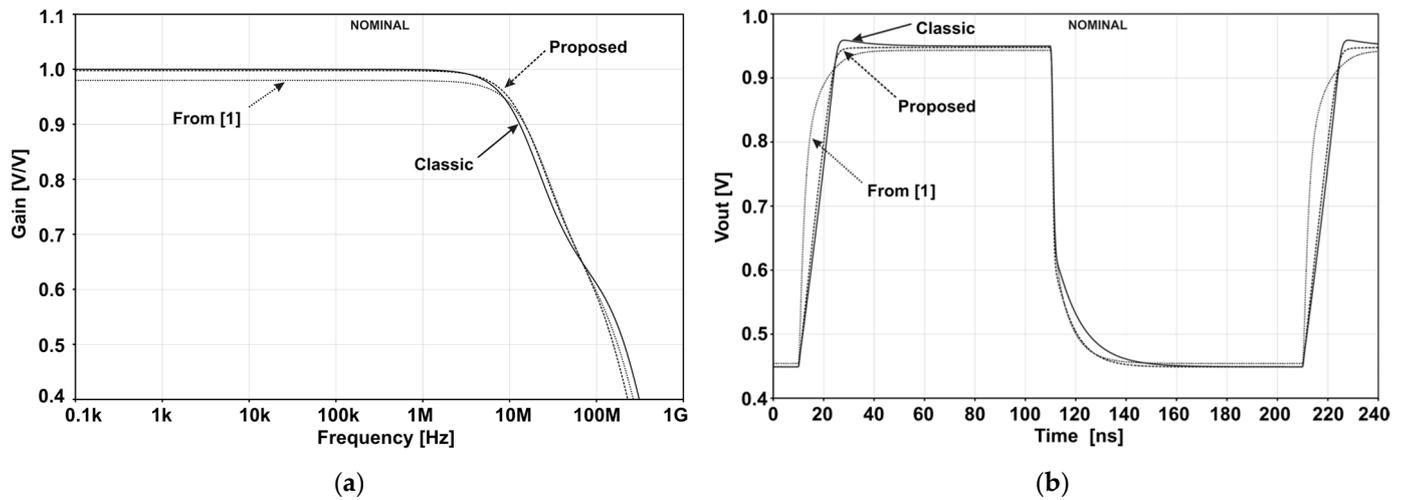
Figure 3. Simulated dynamic characteristics: (**a**) the small-signal gain characteristic; (**b**) the large-signal pulse response. Nominal (corner) models of transistors are used.
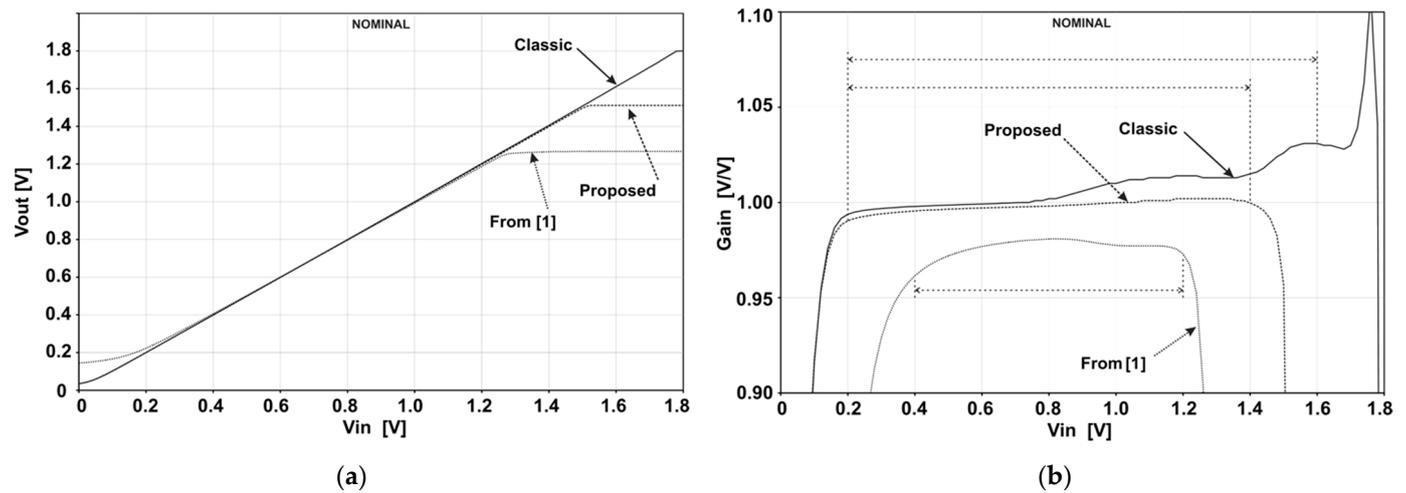
Figure 4. Simulated static characteristics: (**a**) V_{out} vs. V_{in}; (**b**) $Gain = dV_{out}/dV_{in}$. Nominal (corner) models of transistors are used.

The influence of the process spread and mismatch on the gain is depicted in Figure 5a,b, respectively. All the buffers show a relatively small sensitivity to process spread. However, the mismatch increases the gain error near the upper boundaries of the input ranges.

The process spread and the mismatch also cause an offset between V_{out} and V_{in}. Figure 6a,b show the difference ($V_{out} - V_{in}$) under conditions of process spread and mismatch, respectively. Note that ($V_{out} - V_{in}$) contains both the offset and gain errors. However, ($V_{out} - V_{in}$) is dominated by the offset error. The process-induced offset (Figure 6a) is the highest in the topology of [1] because M_1-M_2 and M_6 are opposite-type. On the other side, the mismatch-induced offset (Figure 6b) is similar in all of the topologies because it is determined mainly by the matching of transistors in the first stage. An aggregated (process + mismatch induced) offset is comparable in all the topologies, and is 6.58 mV, 6.29 mV, and 6.48 mV (1 sigma) for the circuits in Figure 1a–c, respectively.
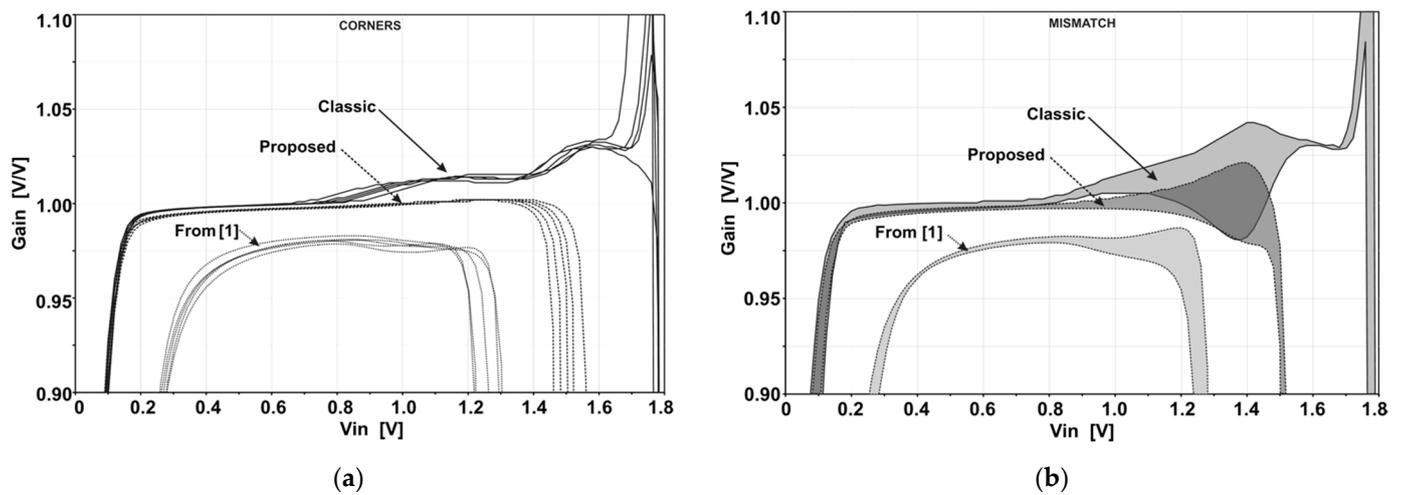
Figure 5. Simulated sensitivity of gain to: (**a**) process corners (nominal and four corners: wz, wo, ws, wp); (**b**) mismatch (500 monte carlo runs).
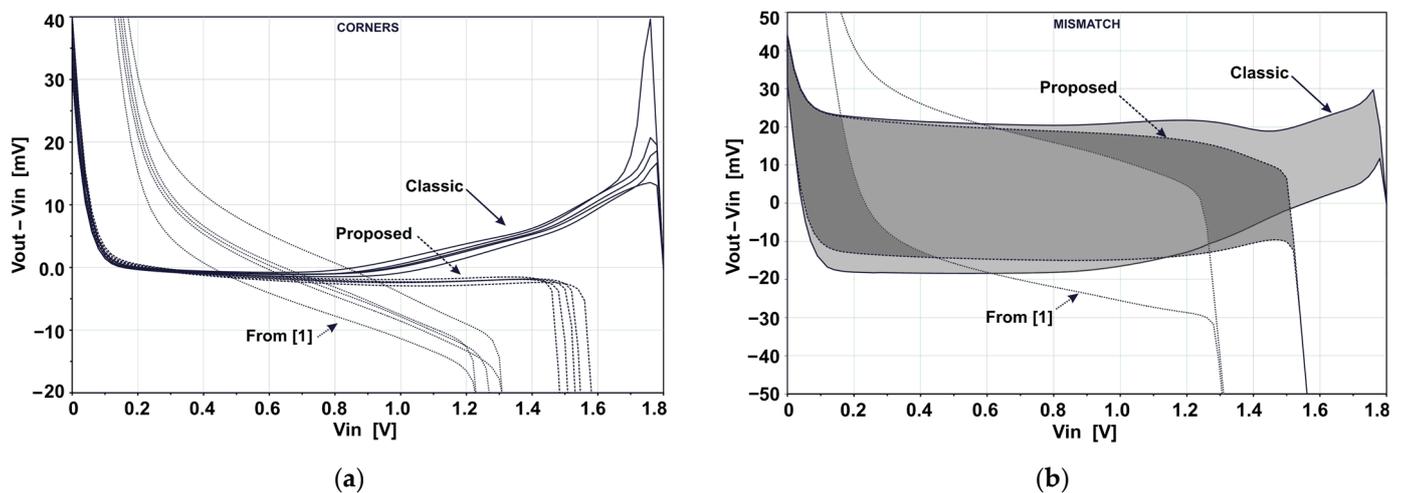
Figure 6. Simulated offset induced by: (**a**) process corners (nominal and four corners: wz, wo, ws, wp); (**b**) mismatch (500 monte carlo runs).

The buffers parameters are summarized in Table 2. In accordance with the design goal, similar power consumption, bandwidth, and occupied area were achieved. Furthermore, the output resistance and noise are practically the same. In these conditions, the classic buffer has the widest DC input range (0.2–1.6 V) and a moderate gain error (1.2%). The proposed solution features an input range (0.2–1.4 V) that is narrower by 200 mV, but the gain error (0.3%) is four times smaller. Moreover, the PSRR (72 dB) is about 20 dB better.

Table 2. Simulated buffer performance [1] using 180-nm CMOS process of *ams AG*.

	Classic (Figure 1a)	Based on [1] (Figure 1b)	Proposed (Figure 1c)
Supply (V_{DD})	1.8 V	1.8 V	1.8 V
Power	1.25 mW	1.19 mW	1.18 mW
−3-dB small-signal bandwidth	45.2 MHz	51.5 MHz	49.8 MHz
Area (active and passive devices)	763 μm^2	506 μm^2	611 μm^2
DC input range [2]	0.2–1.6 V	0.4–1.2 V	0.2–1.4 V
Gain error [3]	1.2%	2.3%	0.3%
1-sigma offset [4] (mismatch+process)	6.58 mV	6.29 mV	6.48 mV
Input sine [5] amplitude @ THD_{out} = 1%	462 mV	290 mV	370 mV

Table 2. *Cont.*

	Classic (Figure 1a)	Based on [1] (Figure 1b)	Proposed (Figure 1c)
SR+/SR− (for 10–90% transition)	32.7/32.9 V/µs	42.8/51.7 V/µs	33.8/46.8 V/µs
Settling time (for 1% accuracy)	36 ns	25 ns	19 ns
Overshoot	3.76%	0.06%	0.63%
Output resistance (R_{out})	13.13 Ω	13.12 Ω	13.94 Ω
Input noise (for 100 Hz–50 MHz)	176 µV$_{RMS}$	165 µV$_{RMS}$	171 µV$_{RMS}$
PSRR (in band)	57 dB	51 dB	72 dB

[1] At $T = 25\,°C$, $C_L = 12$ pF, $I_{BIAS} = 100$ µA, $k = 5$. [2] Determined in Figure 4b. [3] RMS error integrated over the DC input range. [4] At DC $V_{in} = 0.7$ V. [5] Frequency 5 MHz, DC component 0.7 V.

4. Discussion (Circuit Design Principle and Trade-Off)

In this paper, an improved version of a unity-gain zero-offset buffer, which uses an additional feedforward path for a common-mode signal component, is proposed. This modification results in an improvement of some parameters while maintaining circuit complexity similar to the classic Miller OpAmp. The principles of optimization of power consumption, bandwidth, and stability are still the same as in the classical solution. This fact greatly facilitates design of the proposed circuit. Selection of circuit component parameters, depending on design requirements, is carried out in the traditional way. For example, in order to achieve a small offset between V_{out} and V_{in}, it is necessary to reduce mismatch of threshold voltages in the input differential-pair transistors $M_{1,2}$ (due to the fact that $V_{out} = V_{in} + V_{sg1} - V_{sg2}$). Reduction in offset involves using large transistors in the differential pair. Noise optimization requires the reduction in noise from dominant sources, i.e., from the current mirror ($M_{3,4}$) and from $M_{1,2}$. In all three buffers designed in this work, contributions from $M_{3,4}$ and $M_{1,2}$ to the total buffer noise are 80% and 10%, respectively. The contribution from the current mirror is highest because gates of $M_{3,4}$ (i.e., noise sources at $M_{3,4}$ gates) are at a node (V_3) of highest gain to V_{out} (i.e., V_{out}/V_3 is higher than V_{out}/V_2, V_{out}/V_1, and V_{out}/V_{in}).

The proposed common-mode feedforward, when applied to the classic buffer, reduces its input voltage range, but improves its gain error and PSRR. Thus, the choice of an appropriate buffer variant depends on the trade-off between input range, gain error, and PSRR. From the point of view of speed performance (slew rate, settling time, overshoot, etc.), it is worth considering the solution from Figure 1b. In this circuit, the n-channel output stage gives a higher slew rate than achievable using the mixed p-n-channel stages in the classic and proposed buffers. Note that the solution in Figure 1b would also allow for low gain error if implemented in a triple-well or silicon-on-insulator process, where there is no body effect in the n-channel M_6 transistor. On the other hand, stage arrangements in the classic and proposed buffers are less sensitive to process variations because the first and second stages are better matched, as $M_{1,2}$ and M_6, and $M_{3,4}$ and M_5, have the same channel type.

5. Conclusions

The proposed improved feedforward common-mode path ensures full compatibility with standard CMOS processes, lower gain error, and higher PSRR. Improvement in PSRR makes the proposed buffer solution particularly useful in biomedical sensors and filters, since immunity to power interference is one of the key requirements in biomedical applications.

Conflicts of Interest: The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

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