

Article

# A BIST Scheme for Bootstrapped Switches

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**Abstract:** This paper proposes a built-in self-test (BIST) scheme for detecting catastrophic faults in bootstrapped switches. The clock signal and the gate voltage of the sampling MOS transistor are taken as the observation signals in the proposed BIST scheme. Usually, the gate voltage of the sampling MOS transistor is greater than or equal to the supply voltage when the switch is turn on, and such a voltage is not suitable for observation. To solve this problem, a low power supply voltage is provided for the bootstrapped switch to obtain a suitable observation voltage. The proposed BIST scheme and the circuit under test (CUT) are realized with transistor level. The proposed BIST scheme was simulated by HSPICE. The simulated fault coverage is approximately 87.9% with 66 test circuits.

**Keywords:** built-in self-test; fault diagnosis; bootstrapped switches



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## 1. Introduction

Fault diagnosis is an important element in the design and test of integrated circuits. Especially with the development of CMOS circuits, it is more and more difficult to detect faults only with limited input and output ports. BIST is a viable approach that has been used by many researchers [1–9].

For data converter fault diagnosis schemes, there are schemes based on Differential Non-Linearity (DNL) test data [1], based on code-width [2], based on a resistance matching [3], and so on. For amplifier fault diagnosis schemes, there is a scheme by using an RF peak detector and two comparators [4], a scheme by checking the stable output of transient response [5], a scheme based on chaotic oscillation [6], and so on. For sample and hold circuit fault diagnosis schemes, there is a scheme by online balance self-checking [7], a scheme by measuring performance parameters [8], a scheme by monitoring the same output with common-mode input [9], and so on.

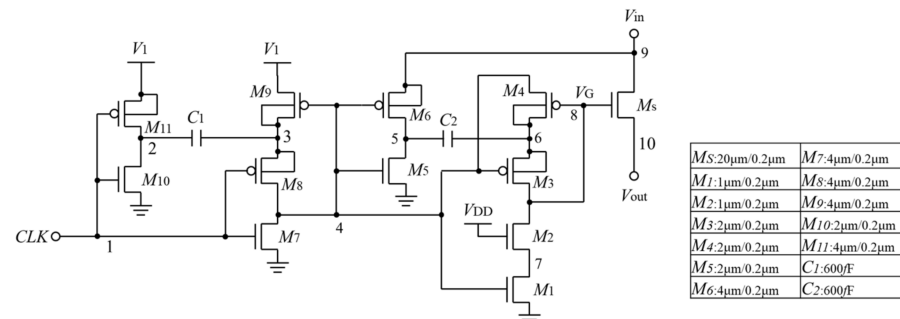
Bootstrapped switches are widely used in many mixed-signal circuits [10–13]. For example, they are used in sample and hold circuits to achieve rail-to-rail switching functions [10,11], used in charge pump circuits to improve energy harvesting by node pre-charging [12,13], and so on. There are also reports on improving the performance of bootstrap switches [14–16]. For example, the body effect compensation technology is used to improve the linearity of the bootstrapped switch [14,15], the dual-channel sampling switch technology is used to improve the accuracy and linearity of the bootstrapped switch [16], and so on. However, there are few reports on the fault diagnosis schemes for bootstrapped switches.

Consequently, this paper proposes a BIST scheme for detecting catastrophic faults in bootstrapped switches. Section 2 previews the bootstrapped switch under testing. Section 3 presents the model of fault diagnosis. Section 4 presents the BIST implementation. Section 5 sets the simulation result by HSPICE. Section 6 discusses the results. Section 7 sets the conclusion.

## 2. The Bootstrapped Switch under Test

In this study, the bootstrapped switch in [17] was used as the circuit under test. The circuit and the designed size of elements are shown in Figure 1. CLK is the clock

signal, which controls the “ON” phase and “OFF” phase of the bootstrapped switch.  $V_{in}$  is the input signal.  $V_{out}$  is the output signal.  $V_G$  is the gate voltage of the sampling MOS transistor.



**Figure 1.** The bootstrapped switch in [17] and the designed size of elements.

When the bootstrapped switch is in the “ON” phase, the CLK is “1”. Then, the voltage of Node 4 is pulled down to GND via  $M_7$  and the voltage of Node 2 is pulled down to GND via  $M_{10}$ . Then, the voltage of Node 3 is pulled up to  $V_{DD}$  via  $M_9$ , the voltage of Node 5 follows the voltage of  $V_{in}$  via  $M_6$  and the voltage of Node 8 follows the voltage of Node 6 via  $M_3$ . The voltage of Node 5 is transmitted to Node 6 via  $C_2$ , so the voltage of Node 6 is the voltage of  $V_{in}$  plus the voltage previously-stored at node 6.

When the bootstrapped switch is in the “OFF” phase, the CLK is “0”. Then, the voltage of Node 2 is pulled up to  $V_{DD}$  via  $M_{11}$  and the voltage of Node 4 follows the voltage of Node 3 via  $M_8$ . Then, the voltage of Node 3 is pulled up to  $2V_{DD}$  via  $C_1$ , so the voltage of Node 4 is  $2V_{DD}$ . Then, the voltage of Node 8 is pulled down to GND via  $M_2$  and  $M_1$ . Then, the voltage of Node 6 follows the voltage of Node 4 via  $M_4$ .

So, the voltage of Node 6 is  $2V_{DD}$  in the “OFF” phase and  $2V_{DD}$  plus the voltage of  $V_{in}$  in the “ON” phase.

The Bootstrapped technique improves linearity by increasing the voltage at the node to lower and stabilize the on-resistance of the sampling switch. In this study, the transmission voltage reached  $2V_{DD}$ , which was difficult to set up the test circuit.

### 3. The Proposed BIST Scheme

When the bootstrapped switch is in the “ON” phase, the gate voltage of the sampling MOS transistor has a stable voltage. When the bootstrapped switch in the “OFF” phase, the gate voltage of the sampling MOS transistor is GND. According to this characteristic, the gate voltage of sampling MOS transistor and CLK signal are used as observation signals.

Due to the bootstrapped switch in this study, in the “ON” phase, the gate voltage of the sampling MOS transistor is  $2V_{DD}$ . If the power supply voltage is 1.8 V, then the gate voltage of the sample MOS transistor is 3.6 V. Such a high voltage is not suitable for observation.

To solve this problem, a low power supply voltage is provided to the bootstrapped switch. As a result, an appropriate voltage can be obtained on the sampling MOS transistor during the “ON” phase.

The testing strategy is if the response analysis module meets the following conditions, output “F = 0”, it indicates that the circuit is fault-free; otherwise output “F = 1”, indicates that the circuit has faults.

1. When “CLK = 1”, the gate voltage of the sampling MOS is a constant value. In this study, the value is determined by a window comparator.

2. When “CLK = 0”, the gate voltage of the sample MOS is GND. In this study, the GND is determined by a phase inverter.

The proposed BIST schematic is shown in Figure 2. The CLK signal of the bootstrapped switch and the gate voltage of the sampling MOS ( $V_G$ ) are connected to the response analysis module as the input. The response analysis module analyzes the two-observation

signal to determine whether the circuit has a fault. The  $EN$  is an enabling signal that controls whether the analysis module works. The power supply voltage of the bootstrapped switch is  $V_{DD1}$ . The power supply voltage of the response analysis is  $V_{DD2}$ .

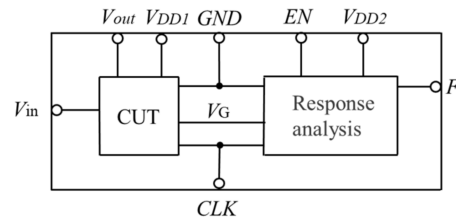


Figure 2. The proposed BIST schematic.

The schematic of the response analysis module is shown in Figure 3. When “ $EN = 0$ ”, the response analysis module is not working. The  $CLK$  signal and  $V_G$  signal do not affect the response analysis module. The output  $F$  is “1”. When “ $EN = 1$ ”, the analysis module works. If the output is “1”, it indicates that the circuit is fault-free. If the output is “0”, it indicates that the circuit has faults. Because the bootstrapped switch is sensitive to the changes of  $V_G$  signal, a source follower is used to collect the  $V_G$  signal.

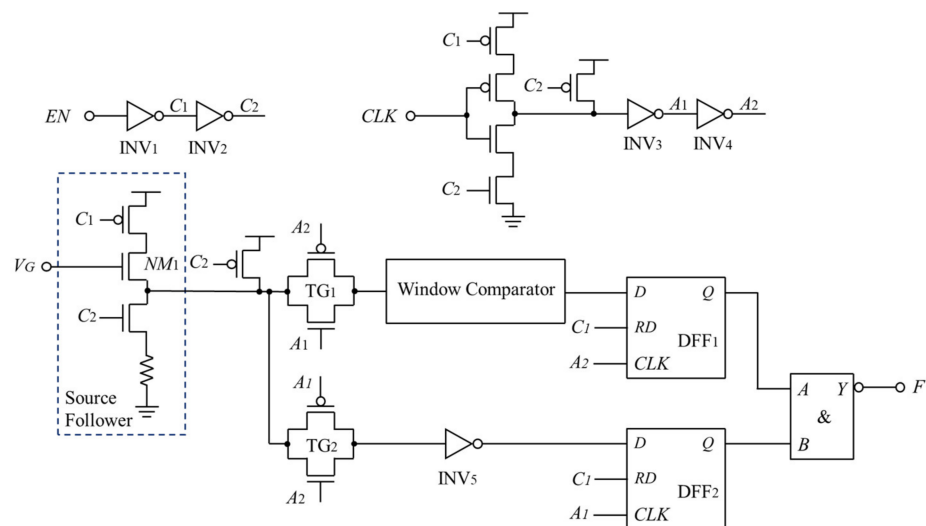


Figure 3. The schematic of the response analysis module.

The schematic of the window comparator in [5] is shown in Figure 4. The window comparator outputs a high potential within the designed input range. The input range can be adjusted by adjusting the  $W/L$  of the four inverters.

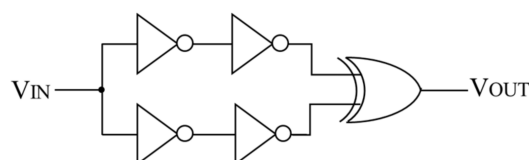
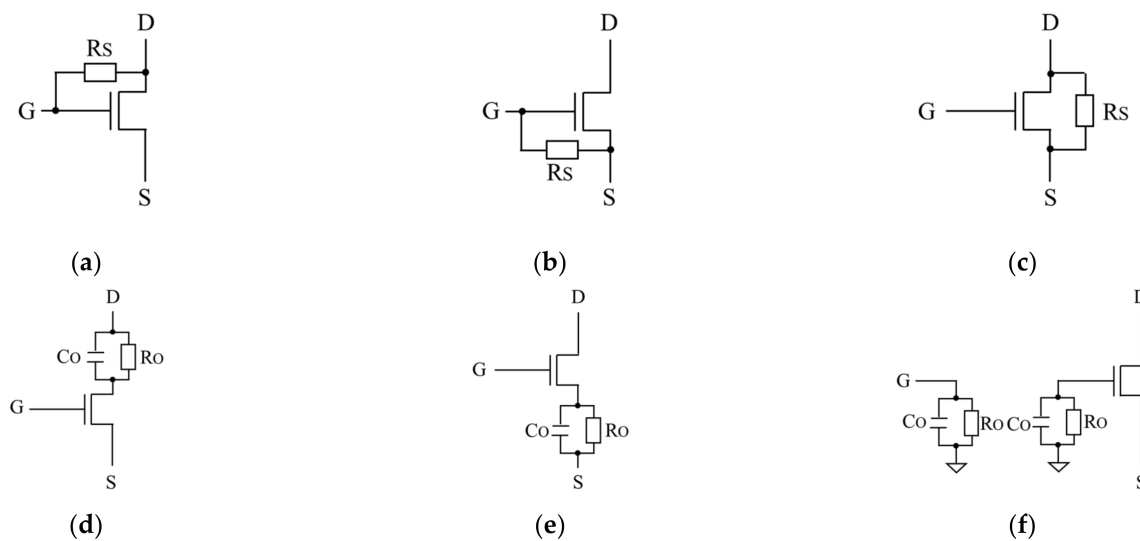


Figure 4. The schematic of the window comparator.

#### 4. Fault Modeling

To evaluate the proposed test strategy, six fault models were added to the circuit under testing. The fault models considered in this paper are shown in Figure 5.

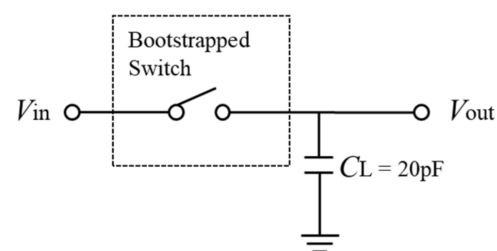


**Figure 5.** The six fault models in this paper (a) gate-drain short (GDS); (b) gate-source short (GSS); (c) drain-source short (DSS); (d) drain open (DO); (e) source open (SO); (f) gate open (GO).

The short fault of MOS transistor is simulated by a  $10\Omega$  resistor between two ports connected. The specific ones are Figure 5a gate-drain short (GDS), Figure 5b gate-source short (GSS), and Figure 5c drain-source short (DSS), respectively. The open fault of MOS transistor is simulated by inserting a  $100\text{fF}$  capacitor and a  $10\text{M}\Omega$  resistor in parallel at the port. The specific ones are Figure 5d drain open (DO), Figure 5e source open (SO), and Figure 5f gate open (GO), respectively.

## 5. Simulation Results

To obtain the influence information of BIST on the bootstrapped switch, the performance simulation of the bootstrapped switch with and without the test circuit was carried out. As shown in Figure 6, the bootstrapped switch and a  $20\text{pF}$  capacitor are combined into a track and hold circuit. The CUT schematic is shown in Figure 1. The schematic of CUT with BIST is shown in Figure 2.



**Figure 6.** The performance simulation schematic for bootstrapped switch.

The  $CLK$  signal is a  $10\text{MHz}$  square wave and the input signal is a sine wave with an amplitude of  $1.8\text{V}$  and a frequency of  $4.96\text{MHz}$ . After the spectrum analysis of the circuit, the performance parameters in Table 1 were obtained. The simulation results show that the BIST scheme has no obvious burden on the CUT. Note a slight decrease in SNR, which is due to the additional noise provided by  $NM_1$ . The  $V_{GS}$  of the  $M_S$  with BIST scheme is higher than that of the  $M_S$  without the BIST scheme, which results in the on-resistance of the  $M_S$  with the BIST scheme being lower than that of the  $M_S$  without the BIST scheme. Therefore, the parameters except SNR are slightly improved.



**Table 1.** Parameters comparison with and without BIST circuit.

Parameter	CUT	CUT with BIST
ENOB (bits)	9.45	9.46
SINAD (dB)	58.69	58.73
SNR (dB)	83.35	83.23
SFDR (dBc)	58.94	58.98
THD (dB)	−58.70	−58.74

To evaluate the proposed BIST scheme, a fault attachment script was used to add the six faults to the MOS transistor of the bootstrapped switch except for the  $M_5$ . The fault of DSS, DO and SO of  $M_5$  does not cause voltage changes at the gate voltage of  $M_5$  which as observation voltage. Therefore, this BIST scheme cannot detect the fault of DSS, DO and SO of  $M_5$ . However, the  $M_5$  connects the input and output signals, a fault in the  $M_5$  can be easily detected by other methods. Therefore, the  $M_5$  is not used as a test object. The total number of fault circuits is 66.

The  $V_{DD1}$  and the input signal are set to 0.6 V, thus the  $V_G$  is approximately 1.56 V during the “ON” phase. Therefore, the output voltage of the source follower is carefully designed to be approximately 0.7 V, when the input voltage of the source follower is approximately 1.56 V. To cope with the possible deviation of the circuit manufacturing, the window voltage of the window comparator is designed to be 0.5 V to 0.9 V.

Figure 7 shows the output signal by transient simulation. Figure 7a shows the result of fault-free. When BIST is off, the output is “ $F = 1$ ”; when BIST is on, the output is “ $F = 0$ ” which indicates that the circuit is fault-free. Figure 7b shows the result of a fault with gate-source short with the  $M_1$ . When BIST is off, the output is “ $F = 1$ ”; when BIST is on, the output is “ $F = 1$ ” which indicates that the circuit has faults.

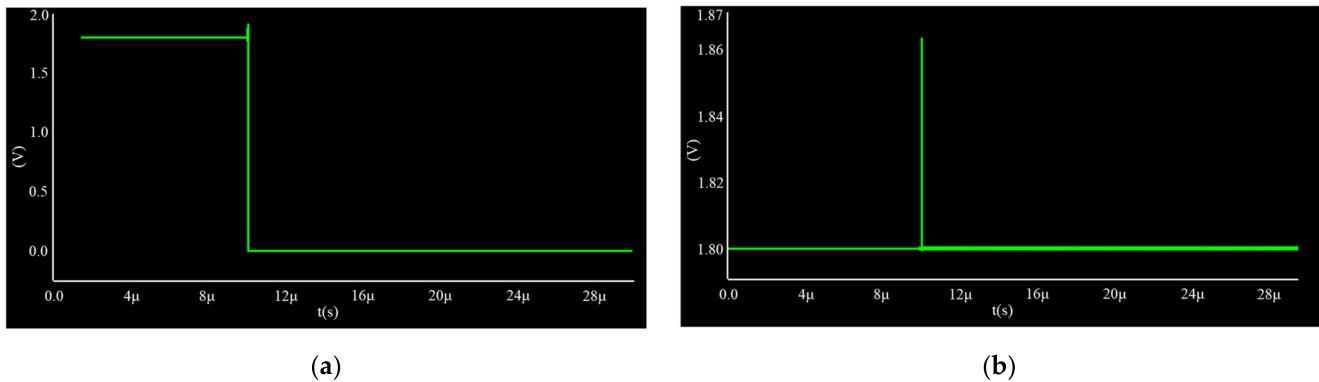
**Figure 7.** The output signal by transient simulation (a) fault-free; (b) fault with gate-source short with the  $M_1$ .

Table 2 shows the simulation results with 66 test circuits. The fault coverage of the BIST scheme is approximately 87.9%. The 200 times Monte-Carlo simulation results show that the BIST scheme works well. Extreme process simulation results show that the fault coverage of the BIST scheme is approximately 75.8%, 78.8%, 89.4% and 84.8% at FF, FS, SS and SF corner, respectively.

**Table 2.** Simulation results of injected and defected fault.

Fault Types	Injected Faults	Detected Faults
GDS	11	11
GSS	11	11
DSS <sup>1</sup>	11	10
GO <sup>2</sup>	11	4
DO	11	11
SO	11	11

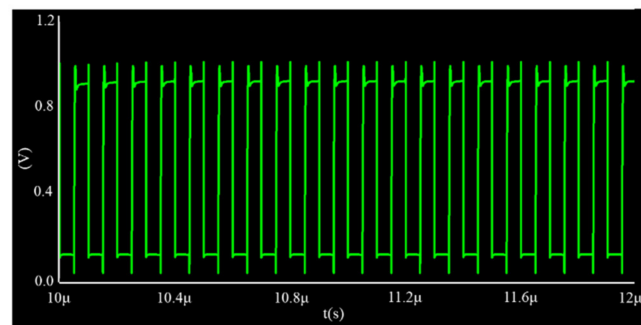
<sup>1</sup> The undetected MOS transistors is  $M_2$ . <sup>2</sup> The undetected MOS transistors are  $M_1, M_2, M_3, M_4, M_5, M_9$  and  $M_{10}$ .

## 6. Discuss

The function of  $M_2$  is to relieve the pressure of  $M_1$ , that is, to prevent the drain-source voltage of  $M_1$  from being greater than  $V_{DD}$ .  $M_2$  can be equivalent to resistance. Therefore, the BIST scheme cannot be detected to the fault of DSS of  $M_2$ .

Note that the BIST scheme has low fault coverage for the gate open of the MOS transistor. This issue is discussed with the fault of GO of  $M_1$ .

Figure 8 shows the transient simulation of the gate voltage of  $M_1$  with the fault of GO with  $M_1$ . Although the gate of  $M_1$  is open, the gate voltage of  $M_1$  is still high and low at the right time sequence due to the presence of parasitic capacitance. Therefore,  $M_1$  can be turned on and off at the correct timing with the gate open. This indicates that the effect of this type of fault on the circuit is not catastrophic. However, this fault may still affect the circuit performance, and subsequent research will be carried out to address this issue.



**Figure 8.** The gate voltage of  $M_1$  with the fault of GO of  $M_1$ .

## 7. Conclusions

Bootstrapped switches are an indispensable type in analog circuits, but there are few fault diagnosis schemes for them. Thus, this paper proposed a bootstrapped switch BIST scheme for detecting catastrophic faults. According to the characteristics of the bootstrap switch, the clock signal and the gate voltage of the sampling MOS transistor are used as the observation signals. However, the gate voltage of the sampling MOS transistor reaches  $2V_{DD}$  during sampling, which is not conducive to observation. In this paper, the method of low power supply voltage is adopted to solve this problem. The proposed BIST scheme was designed and simulated in  $0.18 \mu\text{m}$  CMOS technology. The HSPICE simulation results show that the fault coverage is approximately 87.9% with 66 test circuits. However, in the real circuit, the test result of this BIST scheme may be lower than the simulation results due to noise, technology, or any uncertainty. Therefore, we plan to test and evaluate the prototype chip after it is delivered in the future.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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