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A 0.18-ns Response Time Digital LDO Regulator with Adaptive PI Controller in 180-nm CMOS

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Abstract: Digital low drop-out regulator (D-LDO) with fast settling time and superior transient response is gaining increasing attention to make up for the deficiency of analog LDO. However, as the traditional digital LDOs regulate the output voltage code at a rate of 1 bit per clock cycle, the transient response speed is limited. In this paper, a multi-bit conversion technique is proposed to improve the transient response speed. The multi-bit conversion technique is achieved by an error detector with adaptive regulation of proportion and integration parameters in the digital controller before pass devices. Besides, a voltage sensor and a time-to-digital converter are employed to convert the output voltage to digital codes. Implemented in a 180-nm CMOS process, the proposed D-LDO features under 36/33 mV of undershoot/overshoot at V_{OUT} = 0.95 V as the load current steps up with 40 mA/1 ns on a 0.5 nF load capacitor. The simulated response time is 0.18-ns, the figure-of-merit of speed FOM1 is 0.65 ps and FOM2 achieves 0.068 pF.

Keywords: low drop-out regulator; adaptive control; fast response; embedded power management

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1. Introduction

Digital low drop-out regulator (D-LDO), enjoying a wide range of applications in the Internet of Things (IoT) technology, has recently become one of the main topics of much research in the field of wireless communications. LDOs normally use power from the battery or the energy harvest. In such conditions, LDOs are desired to improve battery life and improve user experiences with immediate transition. In particular, the application of the IoT makes that the battery or the energy harvest provide supply voltage lower than ever. Hence, the stability is harder to control because the decrease of dynamic range and bandwidth of integrated circuits.

Conventional LDOs have been designed with analog circuits and employed an error amplifier and a driver amplifier to provide voltage regulation with negative feedback. They exhibit high efficiency, fast response time and high power supply rejection (PSR) [1–3]. However, it is difficult for analog LDOs to operating at low supply voltage, which has prompted the digital implementations of LDOs [4].

Comparing with analog LDOs, the digital low-dropout regulator (D-LDO) is more suitable for low-supply-voltage operation, and the input-voltage range of D-LDOs is unlimited without error amplifiers. In addition, D-LDO has better scalability and portability exploiting the benefit of digital-logic characteristics. Employing a large number of shift-register, conventional D-LDO has a slower transient response than the analog LDO [5]. Fast load regulation is important in digital circuits with rapidly changing supply current. In [6–8], D-LDOs with an improved triggered comparator have been proposed to improve the transient response, but the performances of the D-LDOs are limited by the analog-to-digital interface, i.e., the comparator. Ref. [9] has categorized all the existing LDO

designs by their control methods. Itpresents the hybrid LDO is a good low-voltage solution with fast transient response and also certain power supply rejection. In [10], D-LDO with transient enhanced PI controller which forms control deviation according to the given value and the actual output value achieves fast transient settling by adjusting the gain of PI controller, and the load current variation can be improved as well. D-LDO in [11] boosts loop-gain dynamically during load transients by a load transient detector without compromising the stability of the D-LDO at steady-state operation, but there may be a deviation in the regulation because of the analog-to-digital converter (ADC).

In this paper, a D-LDO with fast settling time and low undershoot/overshoot is proposed. To improve the load transient response, a time-to-digital converter (TDC) based converter and a PI controller are adopted to achieve a multi-bit regulation. By combining the benefits of both analog and digital control loops with PI controller can be a good low-voltage solution with fast response. The settling time is reduced by five times to 26 ns. In addition, an error detector is proposed to adjust the coefficient of the PI controller adaptively and reduce undershoot/overshoot voltage to 36/33 mV with 40 mA/ns.

The remainder of this paper is organized as follows: In Section 2, the architecture of the D-LDO is proposed. Section 3 presents the details of the circuit implementation of the proposed structure. The simulation results, discussions, and comparisons are illustrated in Section 4. Finally, the conclusion of this paper is given in Section 5.

2. Architecture of the Proposed D-LDO

2.1. Topology

Figure 1 shows the circuit diagram for the baseline D-LDO and the proposed D-LDO. The baseline D-LDO employs a comparator and a barrel shifter, whose output code switches 1 bit in a clock cycle. In order to speed up the response, a TDC-Based Converter and an adaptive PI controller are used. The first component is the TDC-based Converter, which provides a digital code of the output voltage V_{OUT} . In the TDC-based converter, a voltage sensor firstly converts the output voltage (V_{OUT}) to a time signal by capturing the charging time of a capacitor. The TDC includes the buffers and D-Flip-Flops, converting the time signal to a 63-bit width thermometer code furtherly. Then, the second component is the Digital Controller which consists of a subtractor, an error detector and a PI controller. The subtractor in the digital controller outputs the error between the thermometer code V_{OUT} and the reference voltage V_{REF}. The error is transmitted to the PI controller and the error detector. Together with a *State* code calculated by the error detector, the PI controller determined the number of turned-on transistors in the following PMOS array which contains 63 identical PMOS devices controlled by the digital code supplied currents. The proportion and integral coefficients of the PI controller are selected adaptively according to fuzzy rules based on the error and the integral of the error. In this way, the PI controller produces 63-bit width thermometer codes to control the gate of the power transistors in the PMOS array, so that the right amount of current is supplied to the load. The major building blocks of the proposed architecture above will be illustrated in Section 3.

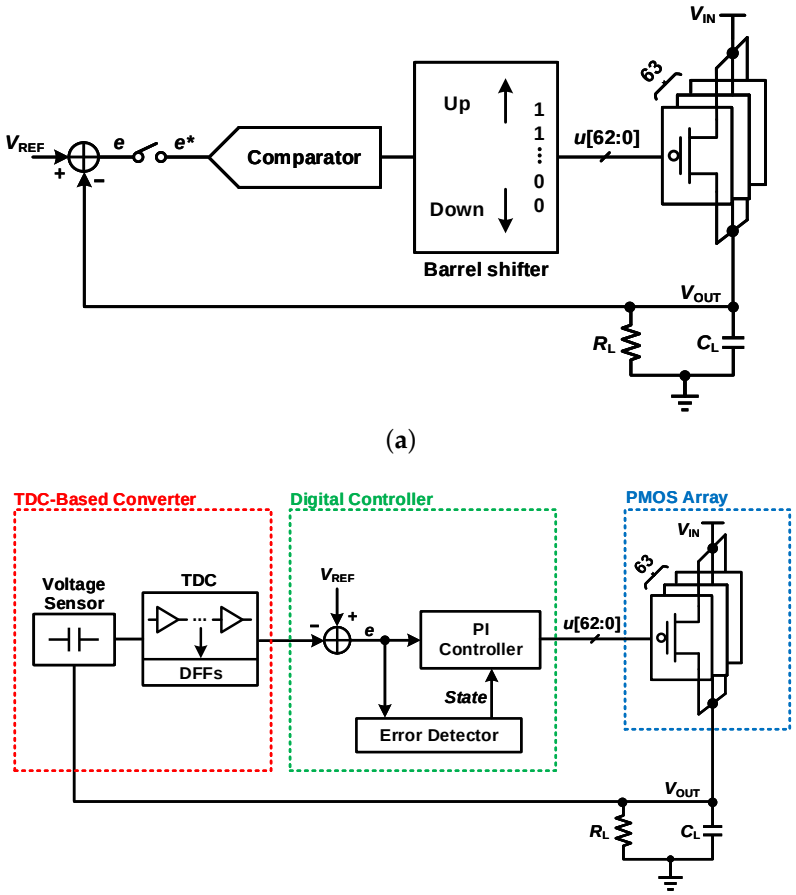

Figure 1. The circuit architecture of (**a**) the baseline D-LDO and (**b**) the proposed D-LDO.

2.2. Transfer Function of the Control Loop

Figure 2 shows the hybrid model for the proposed D-LDO. The relationship between input and output of the TDC-based converter is modeled as a gain K_{TDC} and a zero order holder (ZOH) as interface between continue signal and discrete signal. The z-domain transfer function of the digital controller is derived by taking the traditional z-transfer of the PI controller and is given as

$$\mathrm{G_{PI}}(z) = (K_{\mathrm{p}} + K_{\mathrm{Adjust}}) + (K_{\mathrm{i}} + K_{\mathrm{Adjust}})\frac{z^{-1}}{1 - z^{-1}} \tag{1}$$

where K_{Adjust} is the adaptive coefficient. The output stage and load can be approximated as an RC circuit, and the z-domain model of load and PMOS array is

$$\mathrm{G_{LP}}(z) = \frac{F_{\mathrm{LOAD}} z}{z - e^{-F_{\mathrm{LOAD}}/F_{\mathrm{S}}}} \tag{2}$$

where $F_{\mathrm{LOAD}} = 1/(2\pi \cdot R_{\mathrm{LOAD}} \cdot C_{\mathrm{LOAD}})$, F_{S} is sampling frequency. The K_{P} and K_{i} with K_{Adjust} can be represented as K'_{P} and K'_{i}. V_{REF} is considered as AC ground so the closed-loop transfer function of the D-LDO in z-domain is derived as

$$G(z) = \frac{\left[K'_{\mathrm{p}} z - \left(K'_{\mathrm{p}} - K'_{\mathrm{i}}\right)\right]\left[(1 + F_{\mathrm{LOAD}})z - 1\right]}{\left[1 + K_{\mathrm{TDC}} K'_{\mathrm{p}}(1 + F_{\mathrm{LOAD}})\right]z^2 - \left[2 + K_{\mathrm{TDC}} K'_{\mathrm{p}} + K_{\mathrm{TDC}}\left(K'_{\mathrm{p}} - K'_{\mathrm{i}}\right)(1 + F_{\mathrm{LOAD}})\right]z - \left(K'_{\mathrm{p}} - K'_{\mathrm{i}}\right)K_{\mathrm{TDC}} + 1} \tag{3}$$

Consider that K_p and K_i are adjusted with *error*, the stability of the proposed D-LDO is changed in each period. If there is a large *error*, the stability is traded off to obtain a faster transient response. In contrast, K'_p and K'_i are changed to achieve a more stable regulation when the *error* is small.

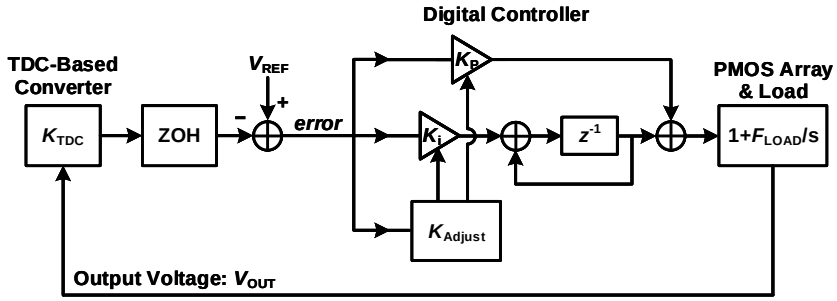

Figure 2. The system hybrid model for the proposed D-LDO.

Figure 3 shows the poles of the proposed system under variable integration gain. As illustrated in Figure 3, a higher integration gain of the PI controller leads loss of stability. According to the traditonal PI theory, large K_p leads to qucik adjustment and large K_i leads to high accuracy. In adaptive process, a large K'_p is selected when *error* in wide region to approach V_{REF} quickly. In addition, if *error* in narrow region, a large K'_i is chosen for eliminating errors.

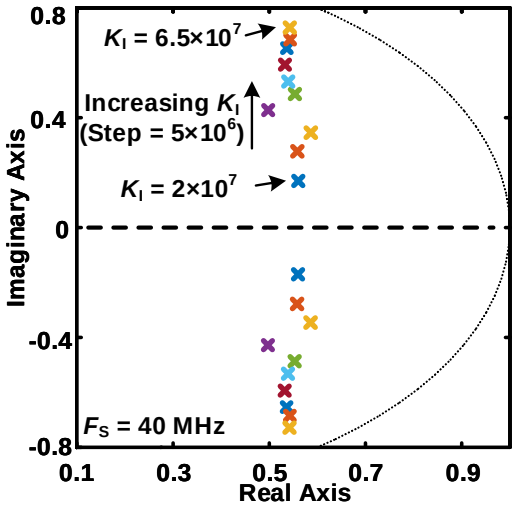

Figure 3. The pole plot of the proposed system under variable integration gain (x shown in Figure 3).

3. Circuit Implementation

3.1. Time-to-Digital Based Converter

The transformation of the V_{OUT} from analog to digital is based on a voltage sensor and a TDC.

Figure 4 shows the schematics of the voltage sensor which converts the analog signals to time signals. The operation process of voltage sensor consists of two parts. Firstly, when *clk* is low level, the switches M0, M1, M5, and M6 are turned on. The capacitor C_C is pre-charged with V_{OUT} and V_{IL} which is the trigger voltage of the DFFs which is an information storage device with memory function and two stable states behind. During the charge stage, the quantity of electric charge in C_C can be expressed as $Q_{pre} = C_C \cdot (V_{OUT} - V_{IL})$. Secondly when *clk* is high level, M3, M4, and M6 are turned on, the two

plates of C_C are connected with GND and current source I_C. Because the current loss of C_C does not occur suddenly, the charge variation in C_C is given as follow

$$\Delta Q = C_C \cdot [V_{IL} - (V_{IL} - V_{OUT})] = I_C \cdot \Delta t \tag{4}$$

where Δt is the time from the beginning of charging to the DFFs are triggered. Hence, the voltage sensor converts V_{OUT} to a time signal Δt.

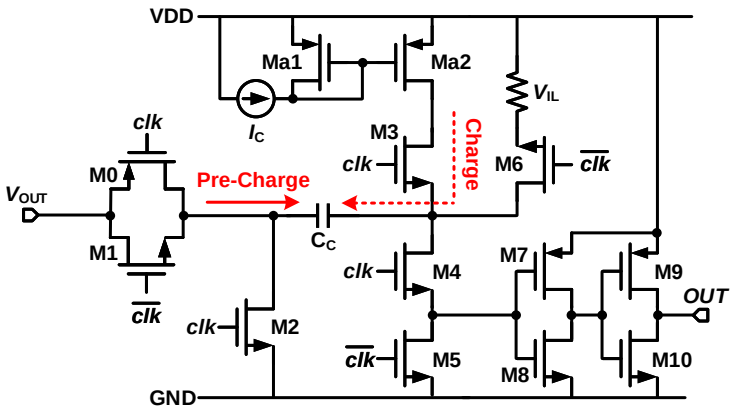

Figure 4. Schematics of the Voltage Sensor.

Figure 5 shows the schematics of the TDC. During the time of Δt, the input signal "1" is transmitted in the delay line. When the pin OUT generates a positive edge, in other words, the time Δt is consumed, the DFFs are triggered. The number of DFFs output signal "1" is expressed as $N = [\Delta t / t_d]$, where t_d is the delay time of a buffer. The buffers and DFFs showed in Figure 5 are suitable for standard cell-based logic synthesis.

From the discuss above, an analog signal of V_{OUT} is converted to a signal about time through the operation of voltage sensor when clk in low level. After clk is switched to high level, the time signal is transmitted to the TDC for generating digital codes. At the end of a cycle, 63-bit digital thermometer code is obtained. Figure 6 shows the linearity of the proposed TDC-based converter. The test points are fitted into a quadratic function. The different value of V_{OUT} is converted to digital code and the a quantization interval of the TDC-based converter is about 25 mV.

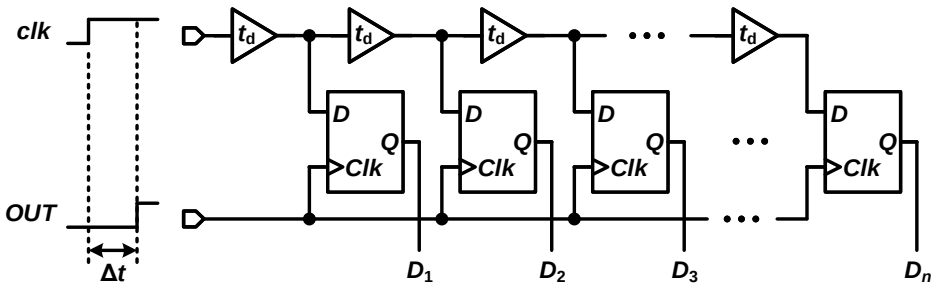

Figure 5. Schematics of the Time-to-Digital Converter.

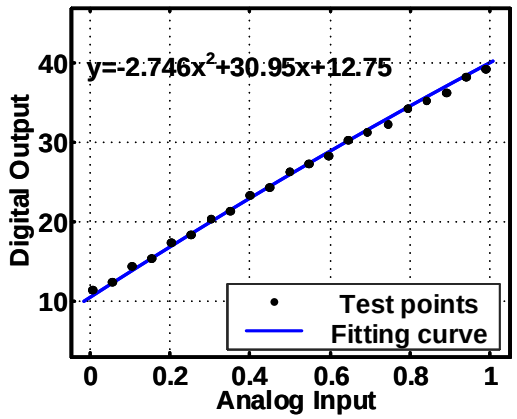

Figure 6. The linearity of proposed TDC-Based converter.

3.2. Error Detector

The adaptive operation in the proposed D-LDO adjusts the coefficients of P and I which is ducted by the error detector as shown in Figure 7. In this mode, the *error* between V_{OUT} and V_{REF} is divided into four ranges. The four ranges correspond to four groups of coefficients for the PI controller. Therefore, using the PI digital controller with an error detector, the proposed D-LDO achieves a faster response time and lower overshoot/undershoot voltage.

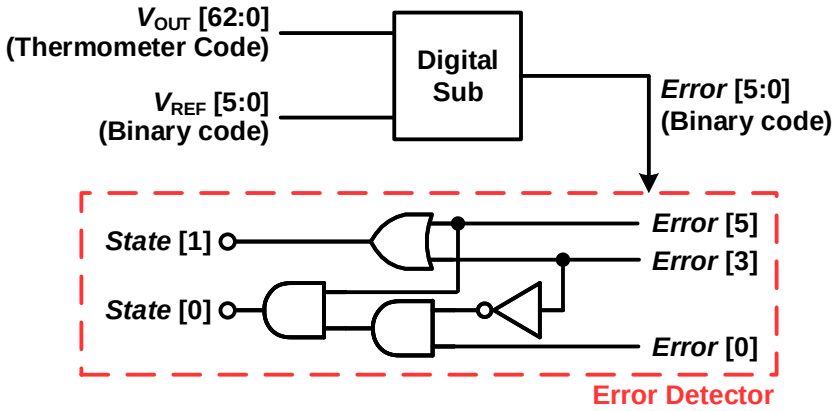

Figure 7. Schematics of the Error Detector

A digital sub is introduced to generate the error between the V_{OUT} and V_{REF}. Because the output of the TDC-based converter is thermometer code and the reference voltage is binary, the digital sub contains a encoder to convert the output of the TDC-based converter to binary codes. The entire digital sub is implemented by Verilog and logical synthesis.

Four levels for error are shown in Table 1: $Error \geq 32$, $Error \geq 8$, $Error \geq 1$, $Error = 0$, where the digital code is equivalent to the thermometer code from the TDC-based converter output N. And $\Delta N = 1$ is equivalent to the 25 mV of voltage values. Therefore, the $State$[1:0] becomes "11" when $Error \geq 0.9$ V, and becomes "10" when $Error \geq 0.4$ V, and becomes "01" when $Error < 0.4$ V and becomes "00" when achieve stabilivolt. Depending on $Error$[5], $Error$[3], $Error$[0], the PI controller operates in three groups of coefficient as shown in Table 2.

Table 1. State table. 1 means high voltage, 0 means low voltage, X means any voltage.

Error Levels	**Input**			**Output**	
	Error[5]	Error[3]	Error[0]	State[1]	State[0]
Error ≥ 32	1	X	X	1	1
Error ≥ 8	0	1	X	1	0
Error ≥ 1	0	0	1	0	1
Error $= 0$	0	0	0	0	0

Table 2. Cofficient.

Input		**Output**	
State[1]	State[0]	P	I
0	0	Hold on	Hold on
0	1	0.8	4
1	0	1	0.7
1	1	1.2	0.1

The determination of coefficients is based on the fuzzy algorithm [12,13]. For example, if the *error* is "large" then $K_P = a_1 x + b_1$, here the a_1 and b_1 are the premise parameter in membership functions of the fuzzy sets "large" in the premises. Therefore, we define the relative range of error as $[-3, -2, -1, 0, 1, 2, 3]$ corresponding to [Negative large, Negative mid, Negative small, Zero, Positive small, Positive mid, Positive large]. To confirm the parameter, we divide the spaces into some fuzzy subspaces where the performance index is minimized.

As mentioned in Section 2, the large K_i leads instability. In order to speed up the rate of regulation, a large K_p is chosen. Hence, we expect K_i will not generate overshoot when the system is regulated quickly. Hence, we select the value of K_i is less than 1 when the error is large. On the contrary, when the V_{OUT} close to reference, a large K_i and a small K_p are needed to eliminate the error and avoid the underdamping. That's the fuzzy principle to design the value of K_p and K_i. Through the simulation and the experience of the control system, the final parameters are obtained to calculate the coefficients in Table 2.

4. Simulation Results and Discussion

The proposed adaptive D-LDO is realized in 180-nm SMIC technology as shown in Figure 8 and the area is 235 µm × 312 µm. In the circuit, the charing capacitor C_C is 450 fF and the charging current I_C is 100 µA. The delay of each buffers t_d is 0.145 ns. The D-LDO operates within an input voltage range of 1–1.2 V and an output voltage of 0.95 V. The D-LDO supplies a maximum current of 100 mA with a load capacitance of 500 pF, while operating at a 40 MHz clock rate with a quiescent current of 34.68 µA. Simulated current efficiency is 99.64% at 10 Ω load resistor.

In order to describe the transient response speed of the proposed circuit, the settling time T_S with variable load was simulated. The settling time is defined as the time that the output voltage recovers to 90% of the droop voltage. As shown in Figures 9 and 10, the proposed D-LDO reduces the settling time under each condition. The settling time is decreased to only 17.6% of the baseline design of D-LDO (from 147.8 ns to 26.1 ns) on average in corner tt which means typical corner . In other words, the proposed circuit improves the response speed by about 5 times.

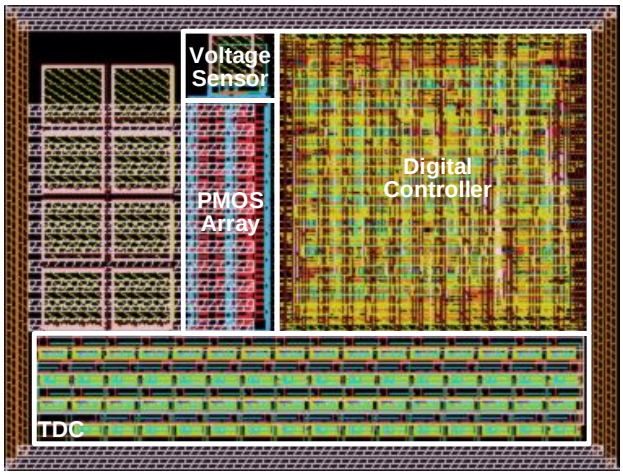

Figure 8. The layout of the proposed D-LDO.

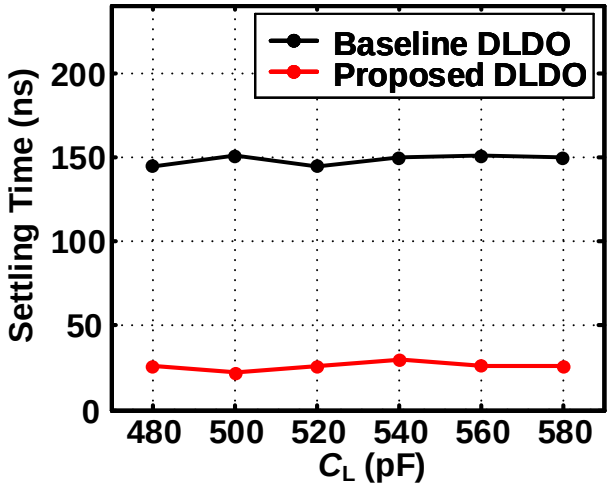

Figure 9. The settling time with load capacitance change.

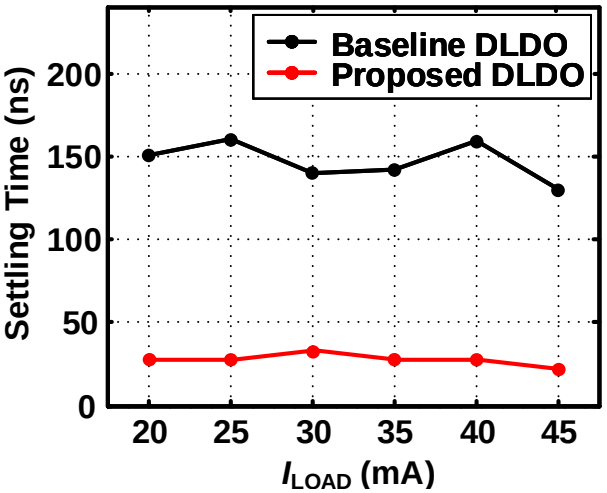

Figure 10. The settling time with I_{LOAD} change.

As shown in Figures 11 and 12, the output voltage with a load current range from 20 to 100 mA and a line voltage range from 1 to 1.2 V are simulated. The effect of the load current and the line voltage on the output voltage is not slight, a load regulation of 0.3 mV/mA and a line regulation of 0.1 mV/mV are achieved. Due to the quantization interval of the TDC-based converter is about 25 mV, the output voltage error in variations of simulation environment is acceptable.

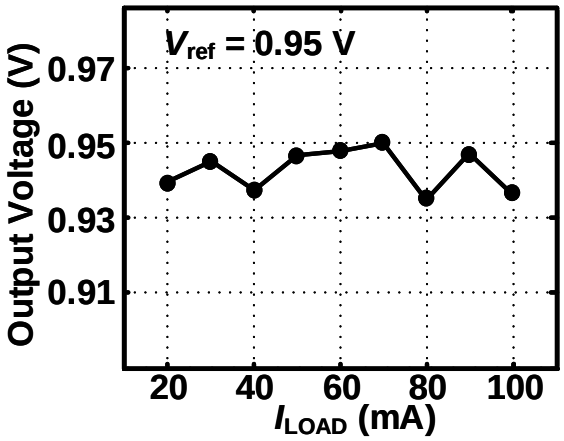

Figure 11. The output voltage under the variations of load current.

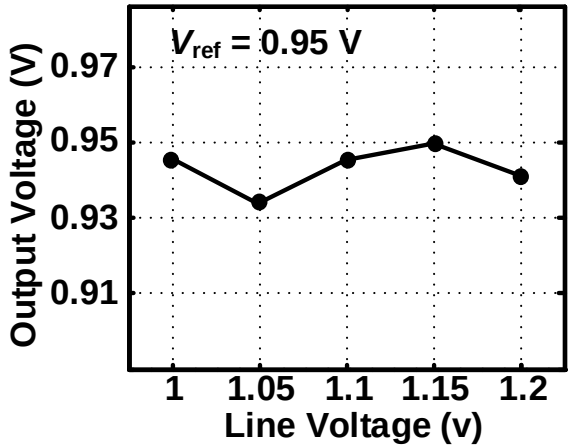

Figure 12. The output voltage under the variations of line voltage.

Figure 13 shows the simulated settling time in various corners. With V_{IN} = 1 V and V_{OUT} = 0.95 V, corner tt achieves 26.1 ns, corner ff and ss which means fast or slow corner achieve 42 ns and 44 ns, respectively. It shows the proposed D-LDO has consistency in different conditions.

The simulated output transient response for the load current change with 40 mA in 1 ns in Figure 14. With V_{in} = 1 V, V_{OUT} = 0.95 V (both step up and down), f_S= 40 MHz, C_L = 0.5 nF, R_L = 10 Ω, the simulated output undershoot is 36 mV and the overshoot is 33 mV. Recovery time achieves 143/186 ns within undershoot/overshoot. Compared with the published LDO designs with PI controller, the proposed D-LDO exhibits a significantly faster settling time.

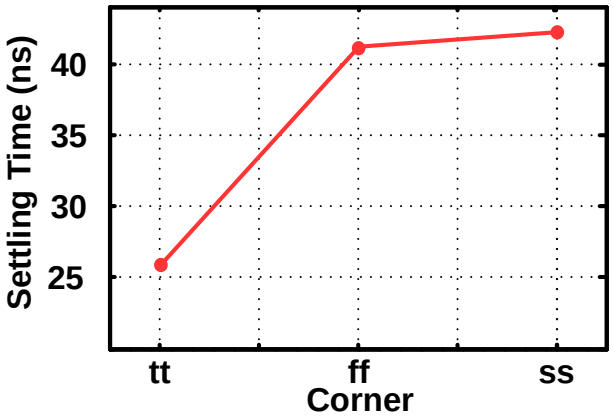

Figure 13. The settling time with corner change.

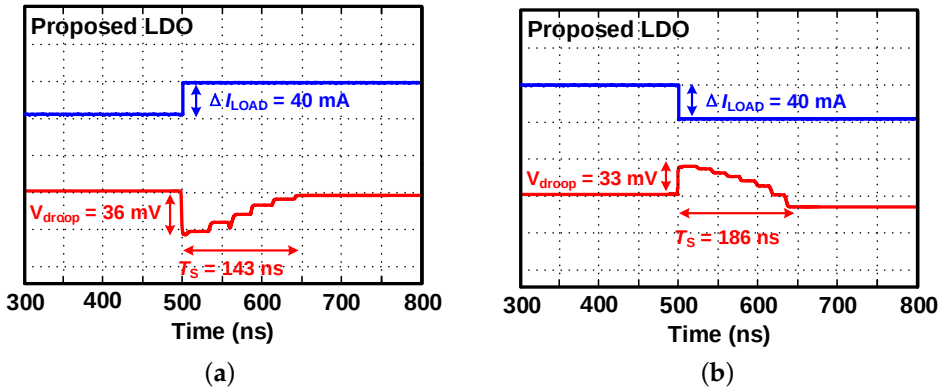

Figure 14. The transient responses of V_{OUT} when I_{LOAD} change of (**a**) step up and (**b**) step down.

The response time T_R of the D-LDO is proposed in [14] is given as

$$T_R = \frac{C_L \Delta V_{OUT}}{I_{MAX}} \tag{5}$$

where C_L is the load capacitance, ΔV_{OUT} is the undershoot/overshoot voltage, I_{MAX} is the maximum load current. Commonly used figure-of-merits FOM1 and FOM2 [14] for LDO performance is

$$\text{FOM1} = \frac{C_L \Delta V_{OUT}}{I_{MAX}} \cdot \frac{I_Q}{I_{MAX}} \tag{6}$$

$$\text{FOM2} = \frac{\Delta V_{OUT}}{V_{OUT}} \cdot \frac{I_Q}{I_{MAX}} \cdot C_L \tag{7}$$

where I_Q is the quiescent current. The smaller FOM indicates the better LDO performance.

The comparison with published D-LDOs are listed in Table 3. In comparison to those prior designs, the proposed D-LDO achieves FOM1 of 0.65 ps, FOM2 of 0.068 pF, and T_R of 0.18-ns. In contrast to these prior D-LDOs, this paper achieves faster response time, lower undershoot/overshoot voltage, and more outstanding performance on the figure-of-merit FOM1 and FOM2. Meanwhile, the proposed D-LDO exhibits decent competitive current efficiency.

Table 3. Comparison with published D-LDO designs.

Design	Yuan [15], EDSSC'19	Yuan [16], TCSII'20	Chen [17], TPEL'21	This Work
Process	180- nm	180-nm	110-nm	**180-nm**
V_{IN} (V)	1	0.8–1.1	0.8–1.2	**1–1.2**
V_{OUT} (V)	0.9	0.7–1.0	0.7–1.1	**0.95**
Load Regulation (mV/mA)	0.053	0.11	0.422	**0.3**
Current Consumption (µA)	500	500	188.8–197.9	**34.68**
Total C_L	Not available	390 pF	40 pF	**0.5 nF**
ΔV_{OUT}@ΔI_{LOAD}	420 mV @216 mA	267 mV @160 mA	360 mV @47.5 mA	**36 mV @40 mA**
Load Transient Edge Time (ns)	NA	65	<1	**1**
Recovery Under/Over-shoot Time (ns)	80/80	80/80	67/250	**143/186**
Peak Current Efficiency (%)	99.78	99.71	92.98–99.61	**99.64**
Response Time T_R (ns)	0.95	0.52	0.2	**0.18**
FOM1 (ps)	2.1	2.03	1.26	**0.65**
FOM2 (pF)	Not available	0.362	0.0706	**0.068**

5. Conclusions

A fully integrated D-LDO with fast transient response is proposed. The D-LDO is designed and simulated in 180-nm technology. With an error detector, the proposed D-LDO achieves an undershoot of 36 mV , overshoot of 33 mV , and transient response time of 143/186 ns for a load change with a 40 mA/ns slew rate. The multi-bit conversion technique decreases the settling time in corner tt, ff, ss to 17.6%, 27.3%, and 28.6% of the baseline D-LDO respectively. The current consumption is 34.68 µA and the peak current efficiency is 99.64%. The proposed D-LDO achieves FOM1 of 0.65 ps and FOM2 of 0.068 pF, which are comparable with the state-of-the-art designs.

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Data Availability Statement: The data presented in this study are available on request from the corresponding author.

Conflicts of Interest: The authors declare no conflict of interest.

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