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Design and Analysis of a Novel High-Gain DC-DC Boost Converter with Low Component Count

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Abstract: In this paper, a novel high-gain DC-DC boost converter with reduced component count is proposed. The converter that is proposed in this paper provides high DC voltage gain, while keeping the overall component count significantly lower in comparison to some similar high voltage gain DC-DC converters presented recently. The proposed converter uses only one power switch, two inductors, two capacitors, and three diodes to achieve high-voltage gain, without a significant compromise on the efficiency. In addition, the proposed design uses small passive component sizes compared to other similar designs of the same power rating. Due to the reduced component count, and hence the small physical size, the proposed converter will find applications in several practical domains, ranging from industrial control embedded systems to the DC transmission bus bars in fully electrical vehicles and renewable energy distribution grids. A 250 Watts prototype of this newly proposed DC-DC boost converter was implemented and simulated using the PSIM simulation tool. The promising simulation results proved the reliable performance of the proposed DC-DC boost converter design.

Keywords: DC-DC converters; voltage boosting techniques; DC transmission; PV systems; switch-mode

1. Introduction

In recent years, the evolution of power conversion has developed significantly, owing to the long-life batteries that supply energy to embedded systems and many similar gadgets. In response to the need for efficient, compact, and cost-effective high-voltage gain, switch-mode DC-DC power converters have flourished over the recent years, to meet the standards of both the domestic and industry sectors. Several new topologies have been proposed in recent years that are intended to cope with this challenge of obtaining high DC voltage gain, while keeping the overall design economical [1]. Nowadays, renewable energy sources are becoming an important subject of research in the field of electrical engineering [2]. It has been estimated that in the near future, the requirement for renewable energy will increase threefold, hence the need for increasingly improved topologies of DC-DC boost converters has become the focus of researchers. In order to meet this need, several universities around the world have introduced undergraduate and graduate level courses on this subject, to disperse the outcomes of related research. In recent years, photovoltaic (PV) panels have achieved commercial success as a reasonable and economical substitute for conventional electricity. Generally, the DC voltage levels provided by PV panels are not high enough to drive domestic lighting [3]. In such lighting equipment, several ultra-bright LEDs are connected in series to obtain high luminescence. These strings of LEDs generally require voltage levels up to 80 V to 100 V, backed by switch-mode boost converters. In such...
applications, multilevel converters are widely used for their simple structure and higher voltage gain [4]. Another popular scheme that has been adopted to meet the requirements of high-voltage gain in hybrid vehicles and smart homes is a switched-capacitor based converter topology, as presented in [5].

The transportation sector is another noteworthy domain that has gained substantial importance in modern society, both on a social and economic basis [6,7]. Electric motors that drive modern fully electric vehicles (FEV) are powered by storage batteries or fuel cells that are stacked over each other and produce DC voltage around 100 V, while the DC bus bar in FEVs runs at 400 V DC [8,9]. Therefore, a high-gain DC boost converter is required to transform the low DC voltage of storage batteries into the high DC voltage for the DC bus bar.

The DC-DC boost converter proposed in this paper is a potential solution to such problems; where high-voltage gain is required along with a small physical size of equipment. The proposed converter constitutes one power switch in the form of a power MOSFET, three diodes, two inductors, and two capacitors, hence making the total component count significantly lower than some recently proposed high-voltage gain DC-DC converter designs [9–11]. The design presented in [9] exploits a cascade topology to achieve high DC voltage gain. The converter in [9] utilizes a quadratic boost converter that is followed by a Cuk converter to achieve significantly higher voltage gain. This approach is adaptable where very high-voltage gain is the prime objective, such as the DC bus bar in fuel-cell vehicles. However, high-voltage gain comes at the cost of considerably larger component count. Although, the converter in [9] uses a single power switch, three inductors, four diodes, and four capacitors make the design implementation larger, hence limiting the scope of applications. In Reference [10], a new boost converter topology is introduced that allows for a wide input voltage range and achieves high-voltage gain at a moderate duty-cycle. In addition, this design uses a larger component count than the design presented in [9]. Moreover, the design presented in [10] is limited in its application to fuel-cell bus bars, where fluctuations in input voltage levels are relatively high. Alzahrani et al. [11] proposed a new design of high-voltage gain converters that uses an interleaved converter integrated with Dickson bifold multiplier cells. This scheme allows achieving a very high-voltage gain, by adding many more bifold cells. The topology that is proposed in [11] uses two power switches, six diodes, two inductors, and six capacitors. The voltage gain of the design proposed in [11] is given as $2N$, where $N$ is the number of Dickson bifold multiplier cells integrated with the basic interleaved converter. Investigating the topologies proposed in [9–11], it can be seen that the high-voltage gain is obtained with a relatively large component count that renders these designs unsuitable for compact areas, such as robotics and embedded systems.

The converter presented in this paper proposes a solution to this problem by introducing a new topology, to achieve high-voltage gain with a reduced component count, and without significant reductions in efficiency.

2. Operation and the Switching Modes

The DC-DC boost converter proposed in this paper has one power switch, which is a power MOSFET, three diodes, two inductors, and two capacitors. The topology of this converter is presented in Figure 1. Due to the existence of only one switch, the converter operates in two switching modes: Mode 0 (M0) and Mode 1 (M1). Proposed converter operates in a continuous conduction mode (CCM) and is capable of driving a wide range of resistive loads.
2.1. During M0

The MOSFET S1 is turned on, and diode D1 is forward biased and hence starts conducting. This causes the linear flow of current $I_{L1}$ through the inductor L1, and hence the energy is stored in it. This condition is represented in Figure 2. After passing the short-lived transient phase, inductor L2 is also magnetized by the current $I_{L2}$. The directions of $I_{L1}$ and $I_{L2}$ are shown in Figure 2. Power diodes D2 and D3 are off, due to the reverse voltage polarity across them and hence do not conduct. The reason that capacitor C1 is in series with the inductor L2, is that the current $I_{L2}$ also charges C1 with the voltage polarity, as shown in Figure 2. The current that flows through S1 is the algebraic sum of $I_{L1}$ and $I_{L2}$.

![Figure 1. Topology of the proposed DC-DC boost converter.](image1)

![Figure 2. Voltage polarities and current directions in Mode 0.](image2)

The voltage across the inductor L1, $V_{L1,ON}$, is only equal to the input DC voltage $V_{in}$, as shown in Figure 2.

$$V_{L1,ON} = V_{in} \quad (1)$$

The voltage across L2, $V_{L2,ON}$, is the same as the voltage across C1, $V_{C1}$. Hence,

$$V_{L2,ON} = V_{C1} \quad (2)$$

2.2. During M1

The switch S1 is turned off and the polarity across both L1 and L2 is reversed to maintain the current flow in the same direction as in M0. In this mode, diode D1 is off, due to the reverse bias polarity across it, and diodes D2 and D3 are on, as has been shown in Figure 3.
The energy that was stored in L1 and L2 is now released and transferred to the capacitors C1 and Co. Capacitor Co starts charging by developing the voltage V_{Co} across it according to the polarity shown in Figure 3. During M1, the voltage V_{L1,OFF} across L1 is the difference of the input DC voltage V_{in} and the voltage V_{C1} across C1. Additionally, the voltage V_{L2,OFF} across L2 is the difference between V_{C1} and V_{Co}.

These relationships are represented as,

\[ V_{L1,OFF} = V_{in} - V_{C1} \]  \( \text{(3)} \)
\[ V_{L2,OFF} = V_{C1} - V_{out} \]  \( \text{(4)} \)

From (1),

\[ V_{in} = L_1 \cdot \frac{di_{L1}}{dt} \]

During M0, the time differential dt is equal to the D \cdot T, where D is the duty-cycle and T is the switching period of the S1.

Hence,

\[ V_{in} = L_1 \cdot \frac{di_{L1}}{D \cdot T} \]  \( \text{(5)} \)

Moreover, from (3),

\[ V_{in} - V_{C1} = -L_1 \cdot \frac{di_{L1}}{(1 - D) \cdot T} \]  \( \text{(6)} \)

3. Steady-State Analysis

The proposed converter operates in the CCM mode of operation even when heavily loaded. Assuming that the proposed converter operates in CCM mode and all the components used in the implementation are ideal, the analysis of the steady-state voltage gain, voltage stresses across the MOSFET, and all the diodes, as well as the efficiency is presented in the subsequent text.

3.1. DC Voltage Gain

Applying volt-second balance on (5) and (6) for L1 gives,

\[ V_{in} \cdot D \cdot T = -(V_{in} - V_{C1}) \cdot (1 - D) \cdot T \]

or,

\[ V_{in} \cdot D = -V_{in} + V_{C1} \cdot (1 - D) \]  \( \text{(7)} \)

From (2),

\[ V_{C1} = L_2 \cdot \frac{di_{L2}}{D \cdot T} \]  \( \text{(8)} \)
and from (4),
\[ V_{C1} - V_{Co} = -L_2 \frac{di_{L2}}{(1 - D) \cdot T} \]  \hspace{1cm} (9)

Applying the volt-second balance on (8) and (9) for L2 gives,
\[ V_{C1} \cdot D \cdot T = (V_{Co} - V_{C1}) \cdot (1 - D) \cdot T \]

From Figure 3, it is obvious that the voltage \( V_{Co} \) across the output capacitor Co and the output voltage \( V_{out} \) across the load is the same quantity; therefore, the output voltage \( V_{Co} \) can be replaced with \( V_{out} \). This leads to the following equation.
\[ V_{C1} \cdot D = (V_{out} - V_{C1}) \cdot (1 - D) \]  \hspace{1cm} (10)

Using (7), the voltage across C1 can be calculated from the above equation, in terms of the duty-cycle D and the input voltage \( V_{in} \), as given below.
\[ V_{C1} = V_{in} \cdot \left( \frac{1}{1 - D} \right) \]  \hspace{1cm} (11)

Putting the value of \( V_{C1} \) from (11) into (10), the steady-state DC voltage gain, \( G \), of the proposed converter can then be derived, and is given by
\[ G = \frac{V_{out}}{V_{in}} = \frac{1}{(1 - D)^2} \]  \hspace{1cm} (12)

The steady-state DC voltage gain transfer function of the proposed high-gain DC-DC boost converter given in (12), reveals that the output voltage is inversely proportional to the square of duty-cycle. Hence, increasing the duty-cycle value in (12) increases the output voltage quadratically, which validates the voltage boosting operation of the proposed DC voltage boost converter.

### 3.2. Voltage Stresses

When S1 is off in M1, the diode D2 becomes on and the S1 becomes parallel to the load. Therefore, the voltage across S1 is the same as \( V_{out} \).
\[ V_{S1,OFF} = V_{out} = \frac{V_{in}}{(1 - D)^2} \]  \hspace{1cm} (13)

When D1 is off, the voltage stress across D1, \( V_{D1,OFF} \), can be calculated by applying the KVL around the loop, consisting of D3, \( V_{in} \), and L1. This gives
\[ V_{D1,OFF} = V_{out} \cdot \left( 2D - D^2 \right) + V_{L1} \]  \hspace{1cm} (14)

The voltage stress across D2 can be calculated by the condition when D2 is off in M0. It can be observed from Figure 2 that
\[ V_{D2,OFF} = V_{L2,ON} = L_2 \cdot \frac{\Delta I_{L2}}{D \cdot T} \]
\[ V_{D2,OFF} = L_2 \cdot \frac{\Delta I_{L2}}{D} \cdot f_s \]  \hspace{1cm} (15)

The voltage stress, \( V_{D3,OFF} \), can be calculated by applying the KVL around the loop consisting of D3, S1, and Co during M0. As S1 is on, the voltage across D3 during its off state is the voltage across Co, the \( V_{out} \). Hence,
\[ V_{D3,OFF} = \frac{V_{in}}{(1 - D)^2} \]  \hspace{1cm} (16)
3.3. Efficiency Analysis

The total power loss in the MOSFET is the sum of the static loss and the dynamic loss. Static power loss occurs in the MOSFET due to the channel resistance when the device is on; whereas dynamic power loss occurs due to the switching of the device. The static power loss in the MOSFET can be calculated as

$$P_{S,\text{static}} = r_{DS(on)} \cdot I_{S(rms)}^2$$  \hspace{1cm} (17)

In (17), $r_{DS(on)}$ is the on-state resistance of the transistor and $I_{S(rms)}$ is the rms current flowing through it. Dynamic loss for one switching period is given as

$$P_{S,\text{dynamic}} = \frac{V_{in} \cdot I_{out}}{3}$$  \hspace{1cm} (18)

Hence the total power loss in the switch is given as

$$P_S = r_{DS(on)} \cdot I_{S(rms)}^2 + \frac{V_{in} \cdot I_{out}}{3}$$ \hspace{1cm} (19)

The power loss in a diode is the sum of the power loss due to the forward voltage drop and due to the on-state resistance under forward bias. The power loss in a diode can then be given as

$$P_D = V_F \cdot I_{D(avg)} + r_D \cdot I_{D(rms)}^2$$  \hspace{1cm} (20)

In (20), $V_F$ is the forward voltage drop of the diode, $r_D$ is the forward junction resistance, and $I_{D(avg)}$ is the average current flowing through the diode under the on state. Power loss in a capacitor $P_C$ can be calculated as

$$P_C = \text{ESR} \cdot I_{C(rms)}^2$$ \hspace{1cm} (21)

In (21), ESR is the “equivalent series resistance” and $I_{C(rms)}$ is the rms value of capacitor current. Identically, the power loss, $P_L$, in an inductor can be calculated as

$$P_L = r_{\text{series}} \cdot I_{L(rms)}^2$$ \hspace{1cm} (22)

In (22), the $r_{\text{series}}$ is the series resistance of the material the inductor is made form, and $I_{L(rms)}$ is the rms value of the current flowing through it. Hence, the total power loss in the proposed converter design will then be

$$P_{\text{loss(total)}} = P_S + 3P_D + P_{C1} + P_{C0} + P_{L1} + P_{L2}$$ \hspace{1cm} (23)

The efficiency can be given as

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss(total)}}}$$ \hspace{1cm} (24)

4. Designing of the Passive Components

Selection of the values of the energy storing component is a critical factor in the behavior and performance of DC-DC converters, no matter which topology is used. The tolerance level in the ripple current of inductors and the ripple voltage of capacitors affects the smoothness and regulation in the output DC voltage levels. As a rule of thumb, the allowable maximum ripple in the inductor current should be no more than 10% of the maximum current that would flow through the inductor. Similarly, the maximum tolerable ripple in the voltage across a capacitor should be no more than 10% of the maximum voltage that will develop across the capacitor.

These assumptions set a fair principle for calculating the size of inductors and capacitors for a stable design that produces a smooth level of voltage across the load and
provides a constant current. This principle is reflected in the calculations of the inductors and capacitor values used in this proposed boost converter.

4.1. Design of Inductor L1

The voltage developed across an inductor can be calculated using

\[ V_{\text{in}} = L \frac{dI_{L1}}{dt} \]  (25)

Hence, the current through the inductor L1 is given as

\[ \Delta I_{L1} = \frac{V_{\text{in}} \cdot D \cdot T}{L_1} \]  (26)

Similarly, the current through inductor L2 is given as

\[ \Delta I_{L2} = \frac{V_{C1} \cdot D \cdot T}{L_2} \]  (27)

The voltage across capacitor C1 is given by

\[ V_{C1} = V_{\text{in}} \left( \frac{1}{1-D} \right) \]

or

\[ V_{C1} \cdot D = V_{\text{in}} \left( \frac{D}{1-D} \right) \]

or

\[ V_{C1} \cdot D \cdot \frac{1}{L_2 \cdot f_s} = V_{\text{in}} \left( \frac{D}{1-D} \right) \cdot \frac{1}{L_2 \cdot f_s} \]  (28)

From (27),

\[ \Delta I_{L2} = V_{C1} \cdot D \cdot \frac{1}{L_2 \cdot f_s} \]  (29)

Comparing (28) and (29) gives

\[ \Delta I_{L2} = V_{\text{in}} \cdot \frac{D}{1-D} \cdot \frac{1}{L_2 \cdot f_s} \]  (30)

Rewriting (26) for L1

\[ L_1 = \frac{V_{\text{in}} \cdot D \cdot T}{\Delta I_{L1}} \]  (31)

and in terms of \( V_{\text{out}} \) and \( f_s \)

\[ L_1 = \frac{V_{\text{out}} (1-D)^2 \cdot D}{\Delta I_{L1} f_s} \]  (32)

The relation given in (32) gives the minimum value for L1 inductor that could be used. The \( \Delta I_{L1} \) is the ripple in the L1 inductor current, \( f_s \) is the switching frequency of the power switch, \( V_{\text{out}} \) is the output DC voltage of the converter, and \( D \) is the duty-cycle.

4.2. Design of Inductor L2

From (30),

\[ \Delta I_{L2} \cdot (1-D) f_s = \frac{V_{\text{in}} \cdot D}{L_2} \]  (33)

or

\[ L_2 = \frac{V_{\text{in}} \cdot D}{\Delta I_{L2} \cdot (1-D) \cdot f_s} \]  (34)
and in terms of $V_{out}$,

$$L_2 = \frac{V_{out}(1-D)^2 \cdot D}{\Delta I_{L2} \cdot (1-D) \cdot f_s} \quad (35)$$

(34) and (35) give the minimum $L_2$ inductor value that is required in terms of $V_{in}$ and $V_{out}$, respectively, with $\Delta I_{L2}$ being the ripple level in $L_2$ current.

### 4.3. Design of Capacitor $C_1$

During Mode 0, the $L_2$ and $C_1$ are in series and the current through this branch is given as,

$$I_{C1} = C_1 \cdot \frac{\Delta V_{C1}}{\Delta t}$$

During Mode 0, the above equation takes the form

$$C_1 = \frac{I_o \cdot D \cdot T}{\Delta V_{in}} \quad (36)$$

Using the relation $V_{C1} = V_{in} \cdot \left(\frac{1}{1-D}\right)$,

$$\frac{\Delta V_{C1}}{\Delta V_{in}} = \frac{1}{1-D}$$

Hence (36) becomes

$$C_1 = \frac{I_o \cdot D \cdot T}{\Delta V_{C1} \cdot (1-D)} \quad (37)$$

or

$$C_1 = \frac{I_o \cdot D}{\Delta V_{C1} \cdot (1-D) \cdot f_s} \quad (38)$$

The relationship given in (38) gives the minimum value of $C_1$ that can be used with $\Delta V_{C1}$ ripples in the voltage across $C_1$.

### 4.4. Design of Capacitor $C_0$

The current through the capacitor $C_2$ is given by

$$I_{C0} = C_0 \cdot \frac{dV_{out}}{dt}$$

During Mode 0

$$C_0 = I_{C0} \cdot \frac{D}{\Delta V_{out} \cdot f_s} \quad (39)$$

The relationship presented in (39) gives the minimum output capacitor value with $\Delta V_{out}$ ripples in the output voltage. If switching frequency, the output voltage ripple and output capacitor current are kept constant, then the upper limit of the output capacitor is set by the duty-cycle of the converter. This leads to designing the output capacitor by operating the converter at the maximum permissible duty-cycle.

### 5. Results

This section describes the results and outcomes of the proposed boost converter. A PSIM simulation diagram and various relationships among the different parameters are presented in the form of graphs and tables to substantiate the proposed objectives of this research.

The proposed converter was simulated using PSIM to verify the relationships derived in Section 3 and presented in (12)–(16) and (24). All the components used in the implementation of the proposed design were assumed ideal.

Figure 4 shows the PSIM implementation of the proposed high-gain DC-DC boost converter, along with different virtual instruments which were used to measure the circuit
parameters during the simulation. All the component values displayed in the schematic diagram are in standard units.

![Schematic Diagram](image)

**Figure 4.** PSIM implementation schematic of the proposed converter.

The values of the energy storage elements were set as: $L_1 = 400 \, \mu\text{H}$, $L_2 = 100 \, \mu\text{H}$, $C_1 = 100 \, \mu\text{F}$, and $C_0 = 2200 \, \mu\text{F}$. The switching frequency of the power switch was set at 50 KHz. Simulation results were obtained with different input DC voltages, ranging from 5 V to 50 V and with different values of load resistance, ranging from 0.1 $\Omega$ to 50 $\Omega$.

5.1. **Operating Modes of the Proposed Converter**

The proposed converter is intended to be used in a wide array of applications that range from PV grids to hybrid vehicles. Such applications demand that the converter operates in a continuous-conduction mode (CCM).

The proposed boost converter operates promisingly in CCM, even when it is loaded heavily ($R_{\text{Load}} = 5 \, \Omega$) to maintain the smooth flow of power to the load. Therefore, all the relationships derived in Section 3 are validated. The current waveforms through the inductors $L_1$ and $L_2$ are shown in Figure 5.

![Current Waveform](image)

**Figure 5.** Cont.
Currents through both the inductors, L1 and L2, do not completely cease during a switching cycle and hence prevent the converter from entering discontinuous-conduction mode (DCM).

### 5.2. Output DC Voltage

Simulation response of the voltage gain, shown in Figure 6, demonstrates that the converter remained in the transient state for less than 0.2 s and enters quickly into the steady-state phase.

![Figure 6. Output voltage simulation waveform for D = 0.75.](image)

The simulation results revealed that the proposed converter follows the steady-state voltage gain relationship, \( \frac{1}{(1-D)^2} \) for the duty-cycle range of \( D \leq 0.75 \).

### 5.3. DC Voltage Stress

The simulation results promisingly satisfied the relationships derived in (13)–(16) over the effective range of the duty-cycle. Table 1 shows a mutual comparison of the theoretical results with the PSIM simulation results for semiconductor devices S1, D1, D2, and D3.

### 5.4. DC Voltage Gain vs. Duty-Cycle Response

Figure 7 shows a graph of the steady-state DC voltage gain response of the proposed converter against the duty-cycle ranging from 0.1 to 0.95.
The simulation results revealed that the proposed converter follows the steady-state voltage gain vs. duty-cycle response.

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</table>

Figure 7. Steady-state voltage gain vs. duty-cycle response.

A 250 Watts prototype of the proposed boost converter with a 50 kHz switching frequency was configured for the most practical parasitic values of the components used in the modeling. These values are given as: the $R_{DS,ON}$ of the MOSFET was set to 0.02 $\Omega$, the forward voltage drop for each diode was set to 0.6 $V$, ESR for each capacitor was set to 0.001 $\Omega$, and the series resistance for each inductor coil was set to 0.1 $\Omega$.

5.5. Efficiency vs. Duty-Cycle Response

The efficiency versus duty-cycle relationship over the effective range of duty-cycle ($D \leq 0.75$) for the 250 Watts prototype is shown in Figure 8. The graph shown in Figure 7 highlights that the proposed converter performed with more than 90% efficiency over a wide range of duty-cycles ($D \leq 0.6$). Moreover, the proposed converter design can perform at a higher efficiency in comparison with the design presented in [9], when operated for high output. This feature marks its significance as a high-gain voltage boost structure for use in hybrid vehicles.

5.6. Efficiency vs. Output Power Response

Figure 9 presents the efficiency vs output power response of the proposed converter by simulating it in PSIM. The duty-cycle for the whole data set was set to 50%. The response shown in Figure 9 revealed that the converter performs efficiently, even under an overloaded condition.
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Figure 8. Efficiency versus duty-cycle plot of the 250 Watts prototype.

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Figure 9. Efficiency versus output power plot of the proposed converter.

5.7. Efficiency Comparison with Cascaded-Boost Converter

A cascaded DC-DC boost converter is merely an integration of two conventional DC-DC boost converters, such that the output of the first converter is directly fed to the second converter. This topology has been obligated by the fact that the total gain of two cascaded systems is the product of the individual gains.

An efficiency comparison of the 250 Watts prototype of the proposed converter and a cascaded boost converter is presented in Figure 10.

Figure 10. Efficiency comparison of the proposed and cascaded boost converter. These prototypes were simulated using PSIM. The comparison presented in Figure 10 shows that the proposed converter is no less efficient than the cascaded converter, even...
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![Figure 10](image)

**Figure 10.** Efficiency comparison of the proposed and a cascaded boost converter.

These prototypes were simulated using PSIM. The comparison presented in Figure 10 shows that the proposed converter is no less efficient than the cascaded converter, even for high duty-cycles. The use of a single power switch makes the proposed converter more efficient while operated at a lower duty-cycle. Operating the converter at a lower duty-cycle allows the switch to remain off for most of the time during its switching period, and hence the average on-state voltage drop across the switch is reduced. Moreover, diodes that do not conduct during the ON state of the power switch do not dissipate any noticeable power. Therefore, power dissipation in the form of heat is reduced considerably, and, ultimately, the efficiency of the converter increases. In this proposed converter, the efficiency is higher than the cascaded converter for lower duty-cycles, without compromising the DC voltage gain, as evident from Figure 10.

The efficiency curve of the proposed converter also implies that this new design can be integrated in cascade with its replica to achieve even higher DC voltage gain. This approach will be helpful when both the cascaded converters are operated at a relatively low duty-cycle.

6. Discussion

The DC-DC voltage boost converters presented in [9–11] have many widespread advantages for modern switch-mode converter application domains, such as fuel cells and renewable energy. It was concluded from this research that the high-voltage gain is achieved by the integration of different voltage lifting techniques in these and other recently proposed boost converter designs.

A relative comparison based on the component count and the steady-state gain among the designs proposed in [9–11], the cascaded boost, and the design proposed in this research is presented in Table 2. Data presented in Table 2 show that the new high-voltage gain DC-DC boost converter proposed in this paper has a significantly lower component count.
compared to the other similar designs, without a considerable compromise in the DC voltage gain.

Table 2. Component count and steady-state gain comparison among different topologies.

<table>
<thead>
<tr>
<th>Converter Design</th>
<th>Component Count</th>
<th>Steady-State Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Switches</td>
<td>Diodes</td>
</tr>
<tr>
<td>Proposed in [9]</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td></td>
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<td></td>
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<tr>
<td>Proposed in [10]</td>
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<td>5</td>
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<tr>
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<td></td>
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<tr>
<td>Cascaded boost</td>
<td>2</td>
<td>2</td>
</tr>
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<td></td>
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<tr>
<td>Proposed in this paper</td>
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<td>3</td>
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</tbody>
</table>

7. Conclusions

In this paper a new DC-DC boost converter is presented that utilizes a low component count in comparison to some recently proposed high DC voltage gain boost converters. The proposed boost converter was simulated for the DC voltage gain, voltage stresses, and efficiency. The simulation results proved the validity of the proposed design.

A 250 Watts prototype model was designed and simulated, and the results were compared with very recently published designs of boost converters, based on component count and component sizing. The comparison clearly revealed that the proposed design promisingly met the objective of achieving high-voltage gain, while keeping the component count low.

Author Contributions: Author contributions: The conceptualization and idea of the converter were generated by U.R. and A.F.M., H.A.S. provided the formal analysis and confirmation of mathematical modeling. D.G. provided help in reviewing the overall concept, its conceptual validation, and handling, plus submission of manuscript to the journal. All authors have read and agreed to the published version of the manuscript.

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