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Miller Plateau Corrected with Displacement Currents and Its Use in Analyzing the Switching Process and Switching Loss

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Abstract: This paper reveals the relationship between the Miller plateau voltage and the displacement currents through the gate–drain capacitance (C_{GD}) and the drain–source capacitance (C_{DS}) in the switching process of a power transistor. The corrected turn-on Miller plateau voltage and turn-off Miller plateau voltage are different even with a constant current load. Using the proposed new Miller plateau, the turn-on and turn-off sequences can be more accurately analyzed, and the switching power loss can be more accurately predicted accordingly. Switching loss models based on the new Miller plateau have also been proposed. The experimental test result of the power MOSFET (NCE2030K) verified the relationship between the Miller plateau voltage and the displacement currents through C_{GD} and C_{DS}. A carefully designed verification test bench featuring a power MOSFET written in Verilog-A proved the prediction accuracy of the switching waveform and switching loss with the new proposed Miller plateau. The average relative error of the loss model using the new plateau is reduced to 1/2∼1/4 of the average relative error of the loss model using the old plateau; the proposed loss model using the new plateau, which also takes the gate current's variation into account, further reduces the error to around 5%.

Keywords: Miller effect; Miller plateau; displacement current; switching loss; switching process

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1. Introduction

Integrated power management and conversion circuitry is a fundamental block in many emerging applications such as Internet of Things (IoT) systems [1,2] and wearable healthcare devices, which are usually powered by batteries and energy harvesters [3,4]. The power consumption of these devices needs to be minimized to prolong the battery lifetime and improve the usability in inaccessible environments, requiring highly efficient DC-DC converters. In recent years, the operating frequency of the converter has been continuously increasing [5–8] to achieve higher power efficiency, faster speed, and higher power density. In addition to the consideration of topologies and control strategies [9–12], the switching process and the switching loss of the power switches are playing more important roles in a high-frequency DC-DC converter. The transient behavior of a power transistor can cause power dissipation and overvoltage, overcurrent, or even ringing [13–17], which are related to the system efficiency, maximum voltage or current ratings of the power transistor, and the electromagnetic interference (EMI) property of the system. Therefore, in-depth analysis of the switching process and more accurate switching loss models are necessary to ensure better performance and maintain the high efficiency of the switching mode power supply (SMPS) working at a higher and higher switching frequency.

Obviously, the switching behavior can be reproduced accurately with simulators such as Spectre and HSpice, but the simulation-based approach fails to provide intuitive

understanding [18,19], which is helpful in circuit design. On the other hand, an analytical model with reasonable simplifications provides closed-form mathematical equations, which show the relationship between the device loss and key parameters. These equations can be further used to optimize the power transistors. The conventional piecewise-linear model [20–22] is simple and effective in a capacitance-limited case, but not suitable for the latest generation of low-voltage power MOSFETs where the parasitic inductance limits the switching process. Many new analytical models [18,23–28] with different tradeoffs between accuracy and complexity have been proposed to analyze the switching process and switching loss. These analytical models are more application-specific and may even include the nonlinearity of the capacitors of the devices. Reference [27] aimed at super-junction MOSFETs and demanded the unusual extraction of electrical characteristics from regular datasheets. Reference [28] only analyzed output capacitance-related losses in wide-bandgap transistors and did not include other kinds of switching losses. Effective figures of merit (FOMs) [29,30] of the power transistors have also been proposed to measure the device performance and help to select the right design parameters of power transistors. Nevertheless, providing an analytical model of the power transistor's switching process and switching power loss with high accuracy is still very challenging. With the least added complexity, loss models developed directly from the classical piecewise-linear model that can still provide accurate prediction are especially attractive.

One major reason for the limited accuracy of the analytical switching loss models is that the so-called Miller plateau is difficult to predict. The Miller effect has long been a well-known phenomenon, and the Miller plateau observed in the switching process of a power transistor is related to this effect. In the conventional or the newly proposed analytical models [20,24,27,30], the Miller plateau voltage V_{pl} has proven to be useful in analyzing the switching process and calculating switching loss. In existing analytical models, the value of V_{pl} is defined as the gate–source voltage V_{GS} when the channel current I_{ch} equals the load current. However, as revealed in this paper, the Miller plateau voltage also relates to the gate driving voltage V_{dr} and the displacement currents through C_{GD} and C_{DS}. A more precise Miller plateau voltage will improve the accuracy of the calculated switching loss.

In this paper, we analyze the Miller effect in the switching operation of power MOSFETs thoroughly and provide a more accurate Miller plateau including the displacement currents through the parasitic capacitances. As a result, the switching process and the switching loss can be analyzed more accurately: the average relative error of the loss model using the new Miller plateau is reduced to $1/2 \sim 1/4$ of the one obtained by the traditional Miller plateau. The rest of the paper is structured as follows: the new model for accurate Miller plateau estimation is proposed in Section 2. Based on the corrected Miller plateau voltage, the switching process and the switching power loss are analyzed in Section 3. Experimental and simulation results are provided in Section 4, verifying the proposed analysis method using the new Miller plateau. Finally, the conclusion is given in Section 5.

2. Miller Plateau Corrected with Displacement Currents

Figure 1a shows a traditional boost converter, which is a widely used step-up DC-DC converter. Since the duration of the turn-on time T_r or turn-off time T_f is much smaller than the switching period T_s, the inductance L may be considered to be a constant current source and the output capacitance C a constant voltage source during the switching transitions. With these assumptions and a simple rearrangement of the circuit elements, the equivalent circuit shown in Figure 1b is obtained, which is used to analyze the switching process in this paper. It has been proven that this equivalent circuit can also be utilized to analyze the switching process of other SMPS topologies [18,31,32].

As was clarified in [32] that the basic transistor action is fast enough, which makes solving the physical equations governing the device behavior simultaneously with the circuit equations unnecessary, and we can safely rely on the fact that what decides the switching process is the time required to establish voltage changes across the parasitic capacitances and current changes in the parasitic inductances. The parasitic capacitances

mainly comprise the three interelectrode capacitances, namely C_{GS}, C_{GD}, and C_{DS}. The parasitic inductances of the drain and source leads, L_D and L_S, must also be considered in high-frequency SMPS. These parasitic capacitances and inductances are also indicated in Figure 1b. Although the capacitances of the devices manifest great nonlinearity, methods as shown in [24] can be adopted to estimate the effective value of each capacitance. To simplify the discussion, we here use the effective values of C_{GS}, C_{GD}, and C_{DS} and omit their nonlinearity.

In Figure 1b, the transistor SN used as a power switch is a MOSFET. In a monolithic low-voltage DC-DC converter, those integrated power switches are no more than standard CMOS MOSFETs, only that there are thousands of elementary cells in parallel with each other and usually bearing at least 1 A current in the ON state [33]. Figure 1b also gives the equivalent circuit of the MOSFET and its three states.

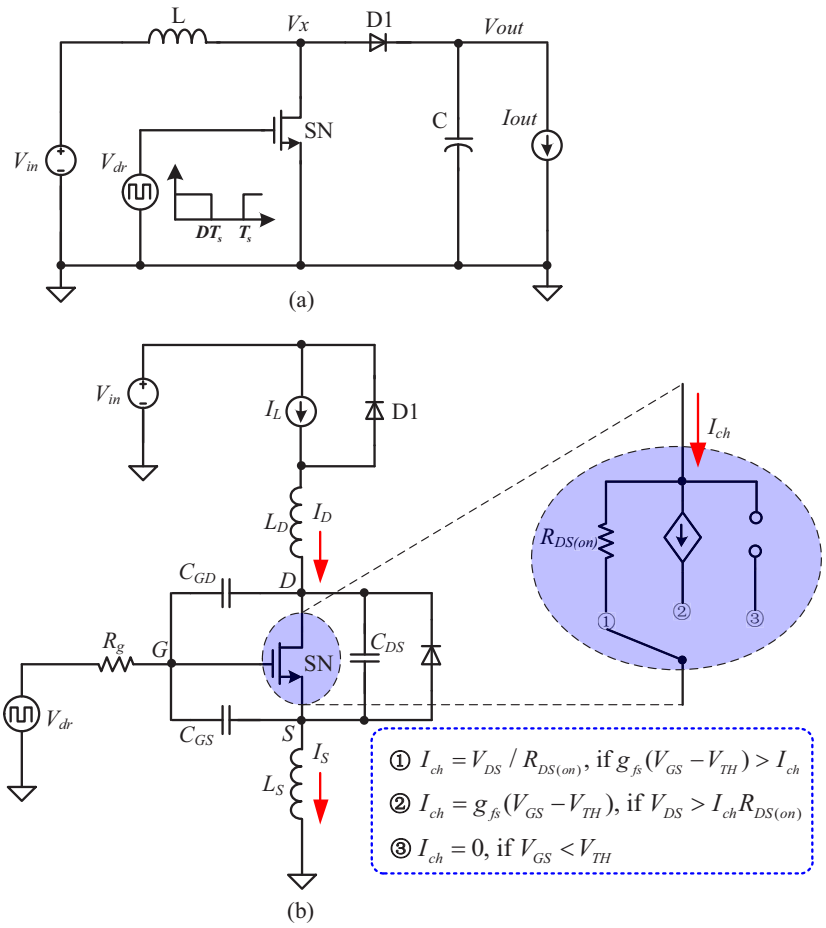


Figure 1. (**a**) Boost converter with practical realization using a MOSFET and diode; (**b**) MOSFET switch with a partially clamped current load (three states of the MOSFET: ① → ON, ② → ACTIVE, ③ → OFF).

Both the source inductor L_S and the gate–drain capacitor C_{GD} form negative feedbacks from the drain circuit to the gate circuit. The former slows down the gate circuit, creating more switching loss, while the latter causes the Miller effect [34–36]. The Miller effect shows that the equivalent input capacitance related to C_{GD} is multiplied by $1 + A$, where A denotes the voltage gain from V_G to V_D. The observed Miller plateau in the switching process of a power transistor is a result of the Miller effect. When the load current of the power transistor is I_L, the Miller plateau of V_{GS} is traditionally [20–22,24] defined as:

$$V_{pl} = V_{TH} + \frac{I_L}{g_{fs}} \tag{1}$$

where g_{fs} is the MOSFET's transconductance and V_{TH} is its typical threshold voltage.

According to (1), the turn-on Miller plateau voltage and turn-off Miller plateau voltage are the same with a constant current load, and few papers have mentioned the impact of the displacement currents through C_{GD} and C_{DS} on the Miller plateau. Reference [27] defined a current I_p that correlates with the displacement current, but its value was calculated empirically by observing I_p patterns in the simulated waveforms, and only the displacement current through C_{DS} was considered.

During the switching process, the current flowing through the transistor is not equal to the load current, namely $I_{ch} \neq I_L$. As shown in Figure 1b, the displacement currents flowing through C_{GD} and C_{DS} must also be included. According to Kirchhoff's current law (KCL) for node D in Figure 1b, it is derived that:

$$I_{ch} = I_L + C_{GD}\frac{dV_{GD}}{dt} - C_{DS}\frac{dV_{DS}}{dt} \tag{2}$$

With an ideal current source load, the voltage gain $A = g_m R_{out} \to \infty$, and this equals an infinite capacitance according to the Miller effect. When V_{GS} reaches the Miller plateau V_{pl_on} during the turn-on process, all the gate current $(V_{dr} - V_{pl\_on})/R_g$ flows into C_{GD}, but there is no voltage increase of V_{GS}. As a result, the voltages of the gate node G and the source node S are both constant, and their rate of change is zero. Therefore, $dV_{GD} = dV_G - dV_D = -dV_D$, and $dV_{DS} = dV_D - dV_S = dV_D$. Then,

$$\frac{dV_{GD}}{dt} = -\frac{dV_{DS}}{dt} \tag{3}$$

The current flowing into C_{GD} is now $(V_{dr} - V_{pl\_on})/R_g$, and the current flowing out of C_{DS} and C_{GD} in parallel is now $(I_{ch} - I_L)$. Substituting $I_{ch} = g_{fs}(V_{pl\_on} - V_{TH})$ and the capacitor's current–voltage relationship $I = CdV/dt$ into (3), it is deduced that:

$$\frac{V_{dr} - V_{pl\_on}}{R_g C_{GD}} = \frac{g_{fs}(V_{pl\_on} - V_{TH}) - I_L}{C_{GD} + C_{DS}} \tag{4}$$

This equation reveals the relationship between the turn-on Miller plateau and the two displacement currents through C_{GD} and C_{DS}.

Similarly, when V_{GS} reaches the Miller plateau V_{pl_off} during the turn-off process, the current flowing out of C_{GD} is V_{pl_off}/R_g and the current flowing into C_{DS} and C_{GD} in parallel is $(I_L - I_{ch})$. Substituting $I_{ch} = g_{fs}(V_{pl\_off} - V_{TH})$ and the capacitor's current–voltage relationship $I = CdV/dt$ into (3), it is deduced that:

$$\frac{V_{pl\_off}}{R_g C_{GD}} = \frac{I_L - g_{fs}(V_{pl\_off} - V_{TH})}{C_{GD} + C_{DS}} \tag{5}$$

This equation reveals the relationship between the turn-off Miller plateau and the two displacement currents through C_{GD} and C_{DS}.

From (4) and (5), the Miller plateau voltages of the turn-on process and turn-off process are derived as:

$$\begin{cases} V_{pl\_on} = \dfrac{V_{TH} g_{fs} R_g C_{GD} + I_L R_g C_{GD} + V_{dr}(C_{GD} + C_{DS})}{(1 + g_{fs} R_g) C_{GD} + C_{DS}} \\ V_{pl\_off} = \dfrac{V_{TH} g_{fs} R_g C_{GD} + I_L R_g C_{GD}}{(1 + g_{fs} R_g) C_{GD} + C_{DS}} \end{cases} \tag{6}$$

This equation shows that the two Miller plateau voltages of the turn-on and turn-off processes are different even with a constant current load. This can be better explained by realizing that a Miller plateau voltage of V_{GS} also means a Miller plateau current of I_{ch}. Since the MOSFET is in the ACTIVE state during the Miller time, the turn-on Miller plateau current I_{pl_on} and turn-off Miller plateau current I_{pl_off} are:

$$\begin{cases} I_{pl\_on} = g_{fs}(V_{pl\_on} - V_{TH}) \\ I_{pl\_off} = g_{fs}(V_{pl\_off} - V_{TH}) \end{cases} \quad (7)$$

With the capacitances being considered, the channel current I_{ch} must be larger than the load current I_L during the turn-on process and smaller than the load current I_L during the turn-off process to provide the extra displacement currents through C_{GD} and C_{DS}. The traditional value of V_{pl} in (1) does not take the displacement currents into account and assumes that $I_{ch} = I_L$ when V_{GS} reaches the Miller plateau V_{pl} during the switching process; thus, the Miller plateau is the same in both the turn-on and turn-off process. As will be shown in the following sections, using the new assessment of the Miller plateau voltage, the switching process and switching power loss can be more accurately analyzed, especially for the low-voltage, high-frequency SMPS.

3. Analyzing the Switching Process and Switching Loss with the New Miller Plateau

The new Miller plateau voltage shown in (6) can be easily applied to the conventional piecewise-linear model or other analytical models. In the turn-on process, the traditional Miller plateau voltage V_{pl} should be replaced by V_{pl_on}; in the turn-off process, V_{pl} should be replaced by V_{pl_off}.

3.1. Switching Waveform Analysis Using the New Miller Plateau

The turn-on or turn-off transition of a power transistor follows several distinct intervals [18,20,32]. Figure 2 illustrates the switching waveforms of a power MOSFET with a clamped current load. Both the turn-on and the turn-off switching processes are divided into five intervals. In Figure 2, each interval of the turn-on sequence is marked by T_{*r}, and each interval of the turn-off sequence is marked by T_{*f}. On the top of the figure, the corresponding state of the MOSFET in each interval is also indicated with the same mark (three states of the MOSFET: ① → ON, ② → ACTIVE, ③ → OFF) in Figure 1b.

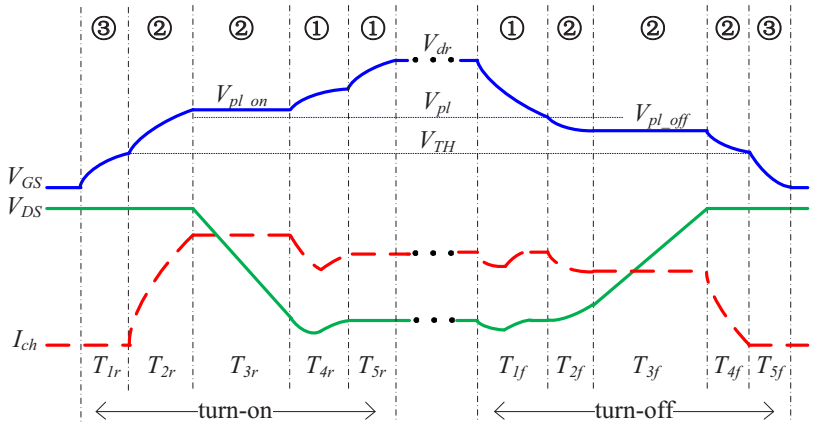


Figure 2. The turn-on sequence and turn-off sequence of a power MOSFET with a clamped current load.

In the turn-on sequence, the first interval is the delay time T_{1r}, during which V_{GS} ramps up to V_{TH}. Next comes the current increase phase, during which V_{GS} continues ramping up to the Miller voltage V_{pl_on}. The channel current I_{ch} also reaches its Miller plateau, a value larger than the load current I_L. T_{3r} is the Miller time, and V_{DS} falls from V_{in} to zero with a constant rate $K_r = (V_{dr} - V_{pl\_on})/(R_g C_{GD})$. Entering T_{4r}, the MOSFET has already gone into the ON state. This is the time I_{ch} needs to change from its Miller value to its final state. The time constant τ in this interval is $R_{DS(on)}C_{DS}$. The final interval sees V_{GS} complete its rise toward V_{dr}.

In the turn-off sequence, the first interval is the delay time T_{1f}, during which V_{GS} ramps down to V_{pl}. Next comes the interval during which V_{GS} continues ramping down to

the Miller voltage V_{pl_off}. The channel current I_{ch} also reaches its Miller plateau, a value smaller than the load current I_L. T_{3f} is the Miller time, and V_{DS} rises from zero to V_{in} with a constant rate $K_f = V_{pl\_off}/(R_g C_{GD})$. Entering T_{4f}, the MOSFET is still in the ACTIVE state. This is the time I_{ch} needs to change from its Miller value to zero. The final interval sees V_{GS} complete its fall toward zero.

According to the above analysis, the equivalent circuit of each interval is first-order, whose solution can be easily obtained. For example, during the delay time T_{1r}, the gate–source voltage V_{GS} rises exponentially towards V_{dr} with a time constant given by $R_g C_{iss}$ ($C_{iss} = C_{GS} + C_{GD}$), that is,

$$V_{GS} = V_{dr}(1 - e^{-\frac{t}{R_g C_{iss}}}) \tag{8}$$

The delay time T_{1r} lasts until $V_{GS} = V_{TH}$. Thus, T_{1r} is derived as follows:

$$T_{1r} = R_g C_{iss} \ln \frac{V_{dr}}{V_{dr} - V_{TH}} \tag{9}$$

Table 1 gives the duration of each interval of the switching process. As T_{5r} and T_{5f} indicate, when V_{GS} is larger than $0.99V_{dr}$, the turn-on sequence is believed to be over; when V_{GS} is smaller than $0.01V_{TH}$, the turn-off sequence is believed to be over.

Table 1. Duration of each interval of the switching process of a power MOSFET with a clamped current load.

Turn-On		**Turn-Off**	
T_{1r}	$R_g C_{iss} \ln \frac{V_{dr}}{V_{dr} - V_{TH}}$ *	T_{1f}	$R_g C_{iss} \ln \frac{V_{dr}}{V_{pl}}$
T_{2r}	$R_g C_{iss} \ln \frac{V_{dr} - V_{TH}}{V_{dr} - V_{pl\_on}}$	T_{2f}	$R_g C_{iss} \ln \frac{V_{pl}}{V_{pl\_off}}$
T_{3r}	V_{in}/K_r	T_{3f}	$V_{in}/K_f - T_{2f}$
T_{4r}	$5R_{DS(on)} C_{DS}$	T_{4f}	$R_g C_{iss} \ln \frac{V_{pl\_off}}{V_{TH}}$
T_{5r}	$R_g C_{iss} \ln \frac{V_{dr} - V_{pl\_on}}{(1-0.99)V_{dr}} - T_{4r}$	T_{5f}	$R_g C_{iss} \ln \frac{V_{TH}}{0.01 V_{TH}}$

*$C_{iss} = C_{GS} + C_{GD}$.

Figure 2 and Table 1 analyze the switching process of the capacitance-limited (the parasitic L_D and L_S are small enough to be neglected) case with a clamped current load. However, the proposed new Miller plateau can be used to analyze the switching process under other conditions only if some revisions are made.

For example, with a resistive load R_L, T_{1r} remains unchanged. However, the duration of the following intervals must be changed since the load current now varies during the switching process. T_{2r} can be calculated with the same equation in Table 1 with a new value of V_{pl_on1} @ $I_L = 0$. The value of V_{pl_on2} @ $I_L = V_{in}/R_L$, together with V_{pl_on1}, can be used to calculate T_{3r}:

$$T_{3r} = R_g[C_{GS} + (1 + g_{fs}R_L)C_{GD}] \ln \frac{V_{dr} - V_{pl\_on1}}{V_{dr} - V_{pl\_on2}} \tag{10}$$

If L_D cannot be ignored, the time constant of T_{1r} is $R_g(C_{GS} + C_{GD}//C_{DS})$ instead of $R_g(C_{GS} + C_{GD})$ since L_D acts as a current source during this interval. Reference [32] showed that, in the turn-on sequence, depending on which, the gate circuit and drain circuit, is faster, the drain voltage will collapse before there is any appreciable rise in current, or the current will reach its Miller value before the drain voltage collapses. This actually equals whether there is a Miller plateau in the turn-on sequence or not. If L_D is small, there will be a Miller plateau in the turn-on sequence and the channel current will finish its rise earlier. From the analysis of [32], V_{GS} varies according to a quadratic function during the

main transition interval. Then, the rate of the V_{GS} rise will accelerate, and this means an abrupt change when it enters its Miller plateau. With the new value of V_{pl_on}, we can make it rise smoothly since V_{GS} still needs to change from V_{pl} to V_{pl_on} during T_{2r} in Figure 2.

There will always be a Miller plateau in the turn-off process even in the inductance-limited case (the drain voltage collapses before the channel current finishes its rise in the turn-on process). However, during T_{4f}, V_{DS} must rise above V_{in} to discharge L_D. Using the same method as in [32] with the new Miller plateau V_{pl_off} of the turn-off process to analyze the switching action during T_{4f},

$$V_{GS} = V_{pl\_off}(1 - \frac{t^2}{\tau_m \tau_{G'}}) \tag{11}$$

where $\tau_m = g_{fs} L_D$ and $\tau_{G'} = R_G C_{GD}$. Thus:

$$T_{4f} = \sqrt{\tau_m \tau_{G'} \frac{V_{pl\_off} - V_{TH}}{V_{pl\_off}}} \tag{12}$$

In all, using the new Miller plateau voltages V_{pl_on} and V_{pl_off}, the switching waveforms can be analyzed under various load conditions. Parasitic inductances can also be included. No detail is missed; each interval has its own physical meaning, and the duration thereof can be easily calculated, which greatly helps to comprehend the switching process of the power MOSFET.

3.2. Switching Loss Analysis Using the New Miller Plateau

The above analysis shows that it is rather easy to use the new Miller plateau voltages V_{pl_on} and V_{pl_off} to analyze the switching process of a power transistor. With the switching waveforms being known, it is straightforward to calculate the corresponding turn-on and turn-off losses by calculating the integral of $V_{DS} \times I_{ch}$ over the switching time. Since the analyzed switching waveforms are accurate, the calculated switching losses will be accurate as well.

To simplify the discussion and make a better comparison, we here directly cite the closed-form loss model of [30]:

$$\begin{cases} P_{on} = \dfrac{V_{in} I_L f_{sw}}{2} \dfrac{C_{iss}(V_{pl} - V_{TH}) + C_{GD} V_{in}}{(V_{dr} - V_{pl})/R_g} \\ P_{off} = \dfrac{V_{in} I_L f_{sw}}{2} \dfrac{C_{iss}(V_{pl} - V_{TH}) + C_{GD} V_{in}}{V_{pl}/R_g} \end{cases} \tag{13}$$

where $C_{iss} = C_{GS} + C_{GD}$; P_{on} and P_{off} represent turn-on switching loss and turn-off switching loss, respectively, and f_{sw} is the switching frequency. This equation differs a little from its original expression in [30]. In [30], the gate charge was used instead of the capacitance. Although the capacitances of a power transistor manifest great nonlinearity, methods as shown in [24] can be adopted to estimate the effective value of each capacitance. After the new Miller plateau is calculated with the capacitance's effective value, the gate charge can still be used. To simplify the discussion, we here use the effective values of C_{GS}, C_{GD}, and C_{DS} and omit their nonlinearity.

Based on (13), the new V_{pl_on} and V_{pl_off} in (6) are used instead of the conventional V_{pl}, and the corresponding I_{pl_on} and I_{pl_off} in (7) are also used to replace the load current I_L. Then,

$$\begin{cases} P_{on} = \dfrac{V_{in} I_{pl\_on} f_{sw}}{2} \dfrac{C_{iss}(V_{pl\_on} - V_{TH}) + C_{GD} V_{in}}{(V_{dr} - V_{pl\_on})/R_g} \\ P_{off} = \dfrac{V_{in} I_{pl\_off} f_{sw}}{2} \dfrac{C_{iss}(V_{pl\_off} - V_{TH}) + C_{GD} V_{in}}{V_{pl\_off}/R_g} \end{cases} \tag{14}$$

In (13) and (14), the gate current was assumed to be constant during the switching process, namely $(V_{dr} - V_{pl\_on})/R_g$ in the turn-on process and V_{pl_off}/R_g in the turn-off process. However, this makes sense only during the Miller time of the switching process. When V_{GS} changes from V_{TH} to V_{pl_on} in the turn-on process or from V_{pl_off} to V_{TH} in the turn-off process, the gate current varies greatly. It is necessary to make a more accurate assessment of the gate current during this time to further improve the prediction accuracy of the switching power loss, especially for the low-voltage, high-frequency SMPS.

Using the average gate current when V_{GS} changes from V_{TH} to V_{pl_on} in the turn-on process or from V_{pl_off} to V_{TH} in the turn-off process, (14) can be further written as:

$$\begin{cases} P_{on} = \dfrac{V_{in} I_{pl\_on} f_{sw}}{2} \left[\dfrac{C_{iss}(V_{pl\_on} - V_{TH})}{I_{avg\_on}} + \dfrac{C_{GD} V_{in}}{(V_{dr} - V_{pl\_on})/R_g} \right] \\ P_{off} = \dfrac{V_{in} I_{pl\_off} f_{sw}}{2} \left[\dfrac{C_{GD} V_{in}}{V_{pl\_off}/R_g} + \dfrac{C_{iss}(V_{pl\_off} - V_{TH})}{I_{avg\_off}} \right] \end{cases} \tag{15}$$

in which I_{avg_on} and I_{avg_off} are the average gate current when V_{GS} changes from V_{TH} to V_{pl_on} in the turn-on process and the average gate current when V_{GS} changes from V_{pl_off} to V_{TH} in the turn-off process, respectively. Their values are approximated as:

$$\begin{cases} I_{avg\_on} = [V_{dr} - \dfrac{1}{2}(V_{TH} + V_{pl\_on})]/R_g \\ I_{avg\_off} = \dfrac{1}{2}(V_{TH} + V_{pl\_off})/R_g \end{cases} \tag{16}$$

which is a simple linear approximation.

Simply replacing the traditional Miller plateau with the proposed new Miller plateau will improve the prediction accuracy of the existing loss models. In addition, unlike previous works, we here directly analyzed I_{ch} instead of I_D. In this way, it is clear that the widely accepted output capacitance loss term is redundant [25]. If the capacitance's effect on the switching duration has already been included, there is no need to further add the output capacitance loss to the final calculation of the switching loss.

4. Experimental and Simulation Verification

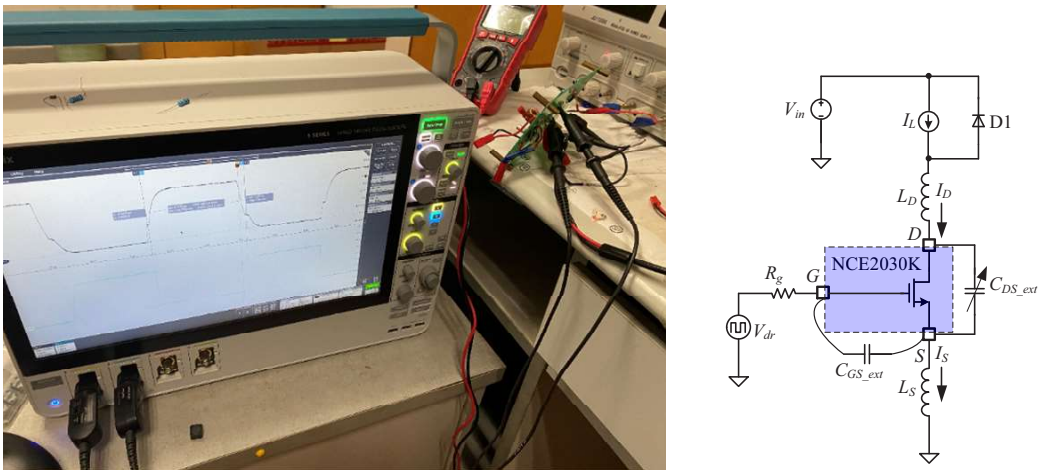
4.1. Experimental Test Result of the Miller Plateau

Shown in Figure 3, the experimental validation of the newly calculated Miller plateau was carried out by testing NCE2030K [37] with an equivalent load current $I_L = 0.1$ A. The input voltage V_{in} was 10 V, and the gate driving voltage V_{dr} was 3 V. The nominal values of NCE2030K's key parameters were: $g_{fs} = 10$ S, $V_{TH} = 0.7$ V, $C_{iss} = 900$ pF (@ $V_{ds} = 10$ V), $C_{oss} = 162$ pF (@ $V_{ds} = 10$ V), $C_{rss} = 105$ pF (@ $V_{ds} = 10$ V).

The circuit was driven directly by the signal generator whose 50 Ω output impedance served as R_g. The driving signal was 100 kHz with a 50% duty cycle. An external 2 nF capacitance C_{GS_ext} was also connected in parallel with the power MOSFET.

The relatively low-frequency operation and the added capacitors made the gate circuit slow and reduced the effect of parasitic inductances, which ensured that the Miller plateau voltages could be accurately measured.

The measured switching waveforms of V_{GS} and V_{DS} are shown in Figure 4, where the Miller plateau of V_{GS} can be readily identified from its waveform. As shown in this figure, the turn-on Miller plateau voltage V_{pl_on} and the turn-off Miller plateau voltage V_{pl_off} are different, which cannot be explained by the existing calculation method of the Miller plateau in (1). In contrast, the proposed calculation method of the Miller plateau in (6) shows that the two Miller plateau voltages of the turn-on and turn-off processes are different even with a constant current load. (6) also reveals that the Miller plateau correlates with the relevant capacitances.



(**a**) (**b**)

Figure 3. (**a**) Experimental validation of the newly calculated Miller plateau by testing NCE2030K; (**b**) testing setup of NCE2030K.

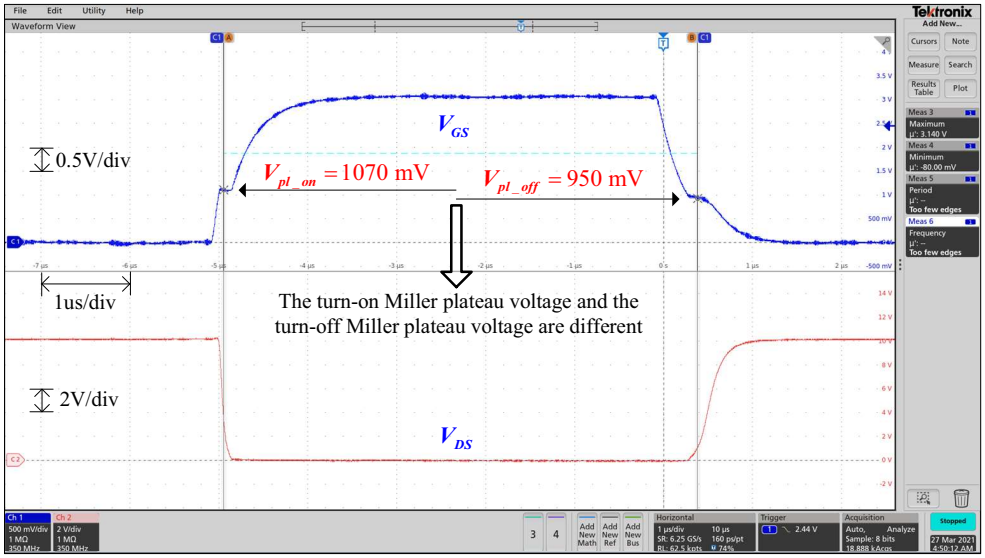


Figure 4. Measured switching waveforms of V_{GS} and V_{DS} for NCE2030K when $V_{dr} = 3$ V, $I_L = 0.1$ A, and $C_{DS\_ext} = 1$ nF.

Table 2 shows the measured (Meas.) Miller plateau, the predicted Miller plateau by the existing (Exist.) method, and the predicted Miller plateau by the proposed (Prop.) method when the relevant capacitance changes. Substituting the above circuit parameters into (1), the predicted Miller plateau V_{pl} by the existing method is 710 mV in both the turn-on and turn-off switching processes and has no relationship with the relevant capacitances. Substituting the above circuit parameters into (6), the predicted Miller plateau voltages are: $V_{pl\_on} = 760$ mV and $V_{pl\_off} = 695$ mV when $C_{DS\_ext} = 1$ nF; $V_{pl\_on} = 922$ mV and $V_{pl\_off} = 644$ mV when $C_{DS\_ext} = 5$ nF. Apart from the measurement errors, as (6) indicates, the values of V_{pl_on} and V_{pl_off} greatly depend on V_{TH} whose real value may be larger than the nominal one given in [37]. This explains why the difference between the measured Miller plateau and the predicted Miller plateau is quite large.

However, as Table 3 shows, the measured voltage difference of V_{pl_on} (@ $C_{DS\_ext} = 1$ nF) and V_{pl_on} (@ $C_{DS\_ext} = 5$ nF) is 160 mV and the calculated voltage difference by the proposed method is 162 mV; the measured voltage difference of V_{pl_off} (@ $C_{DS\_ext} = 1$ nF) and V_{pl_off} (@ $C_{DS\_ext} = 5$ nF) is 41 mV and the calculated voltage difference by the proposed method is 51 mV. The calculated variation trend of plateau voltage as C_{DS} changes agrees

well with the measurement result, which verifies the correctness of (6) in revealing the relationship of the Miller plateau and the relevant capacitance. In contrast, the existing calculation method of the Miller plateau in (1) fails to predict the relationship of the Miller plateau and the relevant capacitance.

Table 2. The measured (Meas.) Miller plateau, the predicted Miller plateau by the existing (Exist.) method, and the predicted Miller plateau by the proposed (Prop.) method when the relevant capacitance changes.

	When $C_{DS\_ext} = 1$ nF			**When $C_{DS\_ext} = 5$ nF**		
	Meas.	**Exist.**	**Prop.**	**Meas.**	**Exist.**	**Prop.**
V_{pl_on}	1070 mV	710 mV	760 mV	1230 mV	710 mV	922 mV
V_{pl_off}	950 mV	710 mV	695 mV	909 mV	710 mV	644 mV

Table 3. Variation of the Miller plateau when C_{DS_ext} changes from 1 nF to 5 nF.

	Measured	**Existing**	**Proposed**
ΔV_{pl_on}	160 mV	0 mV	162 mV
ΔV_{pl_off}	41 mV	0 mV	51 mV

4.2. Verification of Analyzing the Switching Waveform

The SPICE model of a MOSFET always includes the corresponding capacitors, which makes it impossible to separate I_{ch} from I_D, and it is difficult to measure the actual switching loss and make a loss breakdown analysis of an experimental prototype. As a result, an ideal MOSFET with the equivalent circuit in Figure 1b was written in Verilog-A. The key source code is as in Algorithm 1:

Algorithm 1

```
if (vov < 0) begin
  mosfet_state = ‘OFF;
end
else if(gfs * vov < V(vd, vs)/ron) begin
  mosfet_state = ‘ACTIVE;
end
else begin
  mosfet_state = ‘ON;
end

if (mosfet_state == ‘OFF) begin
  I(vd,vs) <+ 0.0;
end
else if (mosfet_state == ‘ACTIVE) begin
  I(vd,vs) <+ gfs * vov;
end
else begin
  I(vd,vs) <+ V(vd, vs)/ron;
end
```

The relevant parasitic capacitances and parasitic inductances can then be added to this ideal power MOSFET.

Based on this ideal power MOSFET, several test benches were set up to verify the effectiveness of the proposed analysis method using the new Miller plateau voltages V_{pl_on} and V_{pl_off}. The parameters of the power MOSFET were: $V_{TH} = 1$ V, $g_{fs} = 10$ S, and

$R_{DS(on)} = 0.02\ \Omega$. The parasitic capacitors of the power MOSFET were: $C_{GS} = 0.6$ nF, $C_{GD} = 0.1$ nF, and $C_{DS} = 0.2$ nF. The gate driver was a voltage source driver with $V_{dr} = 5$ V and $R_g = 2\ \Omega$. The switching frequency was 10 MHz.

Substituting the above circuit parameters into (1) and (6), V_{pl}, V_{pl_on}, and V_{pl_off} were calculated to be 2 V, 2.39 V, and 1.74 V, respectively, when $I_L = 10$ A and $V_{in} = 10$ V. In the turn-on process, the new Miller plateau was larger than the traditional value; in the turn-off process, the new Miller plateau was smaller than the traditional value.

The simulated switching waveforms of V_{GS}, I_{ch}, and V_{DS} in a capacitance-limited (the parasitic L_D and L_S were small enough to be neglected) case are shown in Figure 5. The simulated turn-on Miller plateau voltage (2.391 V) and turn-off Miller plateau voltage (1.746 V) were different, and they accorded with the predicted values from (6) very well.

The calculation (Cal.) and simulation (Sim.) results of the duration of each switching interval are shown in Table 4, in which the calculation result is based on the equations in Table 1.

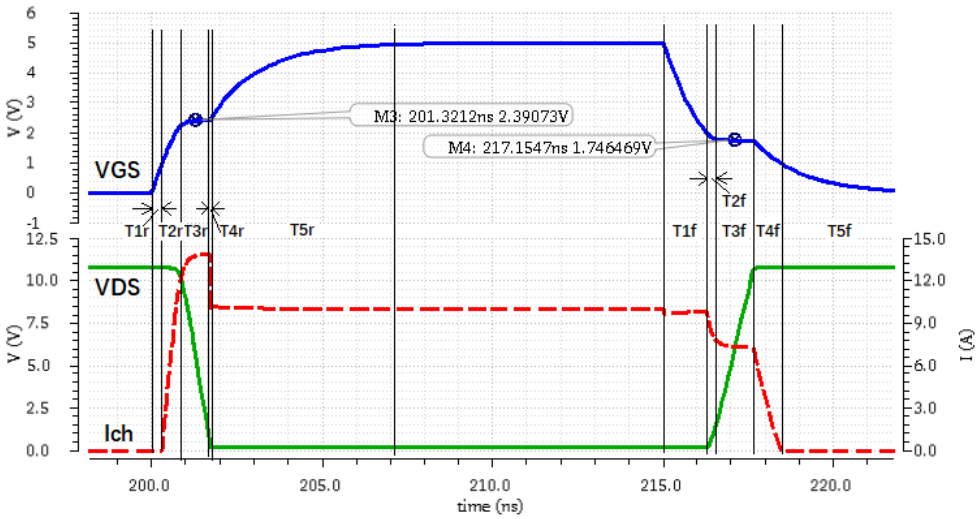


Figure 5. Simulated switching waveforms of V_{GS}, I_{ch}, and V_{DS} in a capacitance-limited case.

Table 4. Calculation and simulation results of switching interval duration.

Turn-On				Turn-Off			
On	**Cal.**	**Sim.**	**Error**	**Off**	**Cal.**	**Sim.**	**Error**
T_{1r}	312 ps	313 ps	0.31%	T_{1f}	1.28 ns	1.29 ns	0.77%
T_{2r}	598 ps	577 ps	3.6%	T_{2f}	195 ps	240 ps	18%
T_{3r}	767 ps	772 ps	0.65%	T_{3f}	954 ps	1.05 ns	9.1%
T_{4r}	20.0 ps	22 ps	9.0%	T_{4f}	775 ps	785 ps	1.3%
T_{5r}	5.52 ns	5.50 ns	0.36%	T_{5f}	6.44 ns	6.45 ns	0.15%

The solution of Table 1 and the calculation result of Table 4 are accurate to the first-order. Compared with the simulation result, the accuracy of the calculation result of each interval in Table 4 is generally satisfactory with the exceptions of T_{4r}, T_{2f}, and T_{3f}. The duration of T_{4r} is particularly small compared with other intervals. The time constant of this interval is $R_{DS(on)}C_{DS}$ since the MOSFET is now in the ON state. The MOSFET is also in the ON state during T_{1f}, but the ending of T_{1f} is marked by when V_{GS} falls to V_{pl_off}. Moreover, I_{ch} goes through a substantial change in T_{4r}, but both I_{ch} and V_{DS} only change a little in T_{1f}. The errors of T_{2f} and T_{3f} come from the first-order linear approximation. During T_{2f}, V_{DS} and I_{ch} vary simultaneously. It is better to use a quadratic function for the approximation [32].

Figure 6 shows the switching waveform of V_{GS}, I_{ch}, and V_{DS} with a partially clamped current load ($L_D = 1$ nH). Now, the drain voltage changes faster than the drain current, and there is no Miller voltage in the turn-on process, which also means that this is an inductance-limited case. Instead, we can use $I_D = 0$ to obtain an approximate V_{pl_on} (1.52 V) to calculate T_{2r} and T_{3r}, which were 195 ps and 575 ps, respectively. Compared with the simulated data (203 ps and 687 ps, respectively) in Figure 6, the relatively larger error of T_{3r} also comes from the first-order linear approximation. As was analyzed earlier, during T_{4f} of the turn-off sequence, V_{DS} must rise above V_{in} to discharge L_D. Using (12), the calculated T_{4f} was 1.30 nS, which is also an accurate value according to the simulated result in Figure 6.

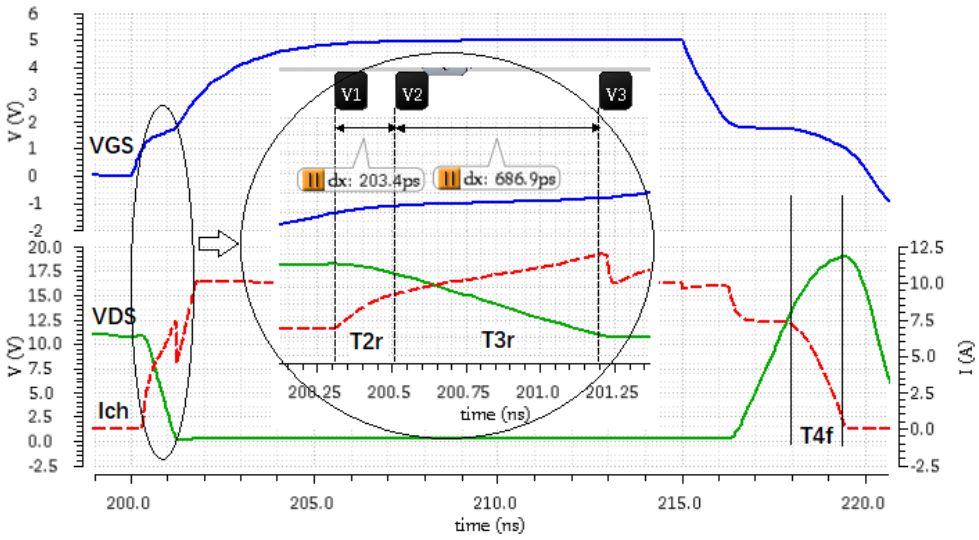


Figure 6. Simulated switching waveforms of V_{GS}, I_{ch}, and V_{DS} in an inductance-limited case.

4.3. Verification of Analyzing Switching Loss

In this part, the simulation result of the switching loss was still based on the power MOSFET written in Verilog-A, and the circuit parameters were the same as in the preceding subsection. The simulated turn-on and turn-off switching losses were calculated by integrating $V_{DS} \times I_{ch}$ over the switching time directly.

Using the above circuit parameters, the loss model in (13), which uses the traditional Miller plateau, the loss model in (14), which uses the proposed new Miller plateau (denoted by Proposed Model 1), and the loss model in (15), which uses the proposed new Miller plateau and further takes the gate current's variation into account (denoted by Proposed Model 2), were calculated and compared. These three models were based on the loss calculation method in [30]. The Proposed Model 1 and Proposed Model 2 here do not indicate specific loss models, and they can be developed by other loss calculation methods only if the traditional Miller plateau is replaced by the proposed new Miller plateau, and the effect of the gate current's variation was further included for the Proposed Model 2. For example, the corresponding Proposed Model 1 and Proposed Model 2 using the loss calculation method in [20] were also calculated and compared to the original piecewise-linear model in [20]. The aim was to verify the improvement of the prediction accuracy by replacing the traditional Miller plateau with the proposed new Miller plateau.

Figure 7a,b shows the curves of the turn-on and turn-off switching losses as a function of the load current for the Verilog-A simulation, the original Model in [20], the Proposed Model 1, and the Proposed Model 2, respectively. Based on the loss calculation method in [20], the Proposed Model 1 uses the new Miller plateau, while the original Model in [20] uses the conventional Miller plateau. As Table 5 shows, replacing the conventional Miller plateau by the new Miller plateau can improve the prediction accuracy of the switching loss: the average relative error of the Proposed Model 1 was almost reduced to 1/3 of the

average relative error of the original Model in [20]. The Proposed Model 2, which further takes the gate current's variation into account, had the smallest prediction error.

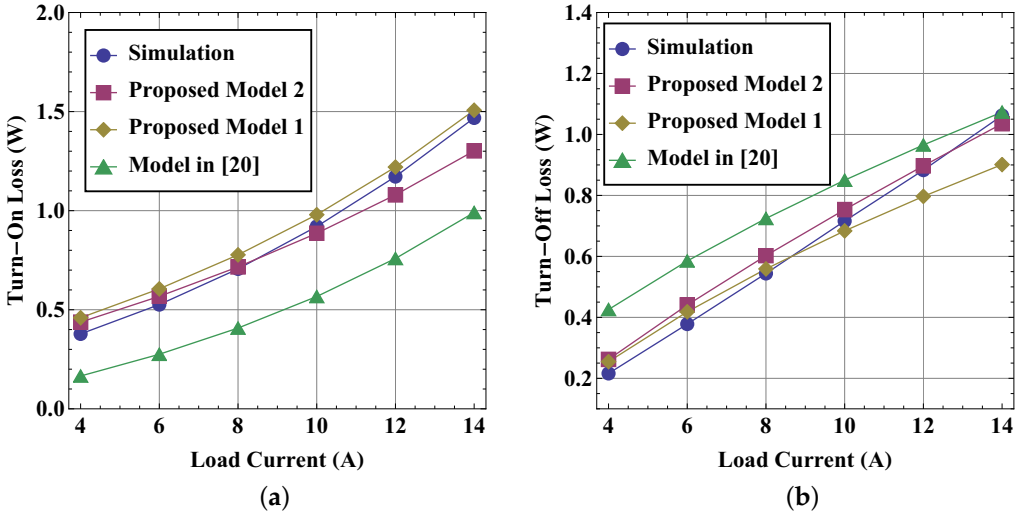


Figure 7. Switching loss of the models based on [20] at 10 MHz, 10 V input voltage, and 5 V gate driving voltage: (**a**) turn-on loss as a function of load current; (**b**) turn-off loss as a function of load current.

Figure 8a,b shows the curves of the turn-on and turn-off switching losses as a function of the gate driving voltage for the Verilog-A simulation, the original Model in [20], the Proposed Model 1, and the Proposed Model 2, respectively. As Table 6 shows, compared with the loss model based on conventional Miller plateau, the loss model based on new Miller plateau again better followed the trend of the simulation result: the average relative error of the Proposed Model 1 was almost reduced to 1/4 of the average relative error of the original Model in [20]; the Proposed Model 2, which further takes the gate current's variation into account, had the smallest prediction error.

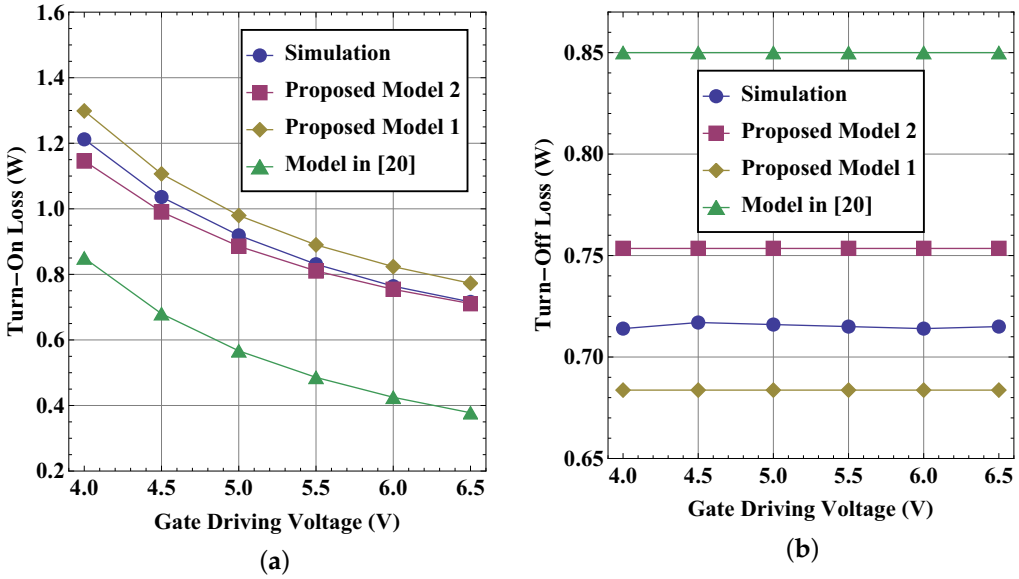


Figure 8. Switching loss of the models based on [20] at 10 MHz, 10 V input voltage, and 10 A load current: (**a**) turn-on loss as a function of gate driving voltage; (**b**) turn-off loss as a function of gate driving voltage.

Figure 9a,b shows the curves of the turn-on and turn-off switching losses as a function of the load current for the Verilog-A simulation, the original Model in [30], the Proposed

Model 1, and the Proposed Model 2, respectively. Based on the loss calculation method in [30], the Proposed Model 1 uses the new Miller plateau, while the original Model in [30] uses the conventional Miller plateau. As Table 5 shows, replacing the conventional Miller plateau by the new Miller plateau can improve the prediction accuracy of the switching loss: the average relative error of the Proposed Model 1 was almost reduced to 1/3 of the average relative error of the original Model in [30]. The Proposed Model 2, which further takes the gate current's variation into account, had the smallest prediction error: the average relative error is within 5.5%.

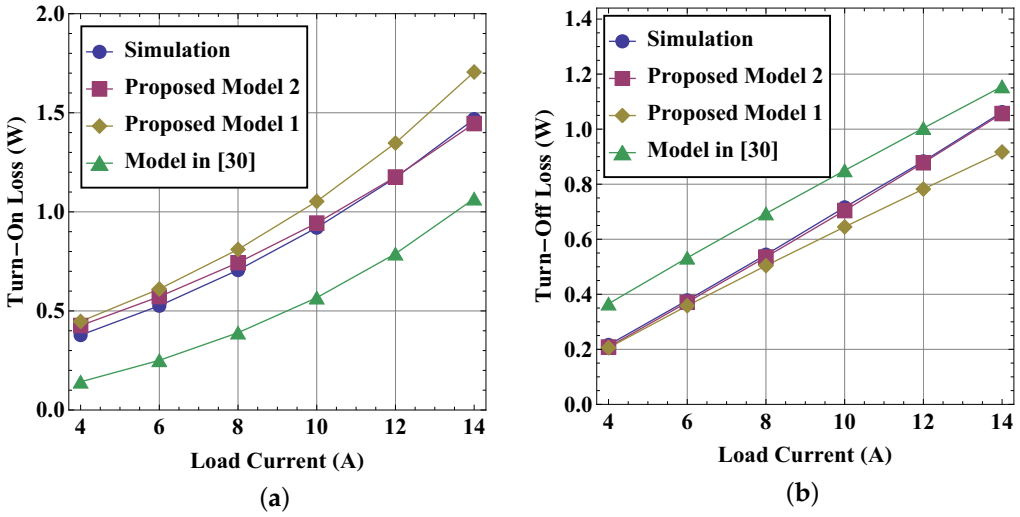


Figure 9. Switching loss of the models based on [30] at 10 MHz, 10 V input voltage, and 5 V gate driving voltage: (**a**) turn-on loss as a function of load current; (**b**) turn-off loss as a function of load current.

Figure 10a,b shows the curves of the turn-on and turn-off switching losses as a function of the gate driving voltage for the Verilog-A simulation, the original Model in [30], the Proposed Model 1, and the Proposed Model 2, respectively. As Table 6 shows, compared with the loss model based on conventional Miller plateau, the loss model based on new Miller plateau again better followed the trend of the simulation result: the average relative error of the Proposed Model 1 was almost reduced to 1/2 of the average relative error of the original Model in [30]; the Proposed Model 2, which further takes the gate current's variation into account, had the smallest prediction error and its average relative error is within 4.5%.

Table 5. The average relative error of different loss models based on two calculation methods when the load current I_L changes from 4.0 A to 14 A at 10 MHz, 10 V input voltage, and 5 V gate driving voltage.

	The Loss Calculation Method in [20]			**The Loss Calculation Method in [30]**		
	Original Model in [20]	**Proposed Model 1**	**Proposed Model 2**	**Original Model in [30]**	**Proposed Model 1**	**Proposed Model 2**
P_{on}	42.1%	9.9%	8.0%	43.0%	15.8%	5.2%
P_{off}	35.7%	10.1%	9.7%	29.8%	8.7%	1.6%

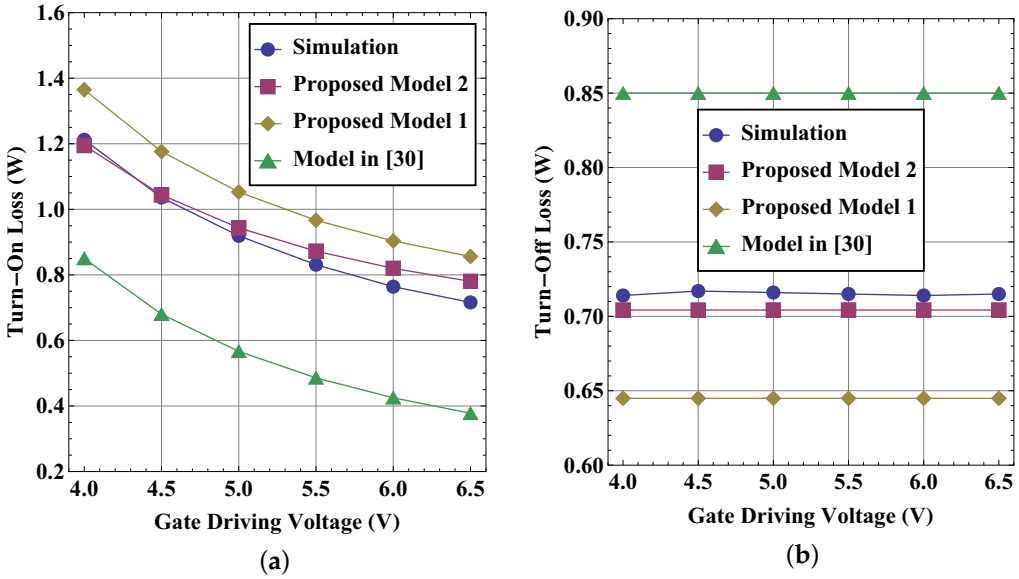


Figure 10. Switching loss of the models based on [30] at 10 MHz, 10 V input voltage, and 10 A load current: (**a**) turn-on loss as a function of gate driving voltage; (**b**) turn-off loss as a function of gate driving voltage.

Table 6. The average relative error of different loss models based on two calculation methods when the gate driving voltage V_{dr} changes from 4.0 V to 6.5 V at 10 MHz, 10 V input voltage, and 10 A load current.

	The Loss Calculation Method in [20]			The Loss Calculation Method in [30]		
	Original Model in [20]	Proposed Model 1	Proposed Model 2	Original Model in [30]	Proposed Model 1	Proposed Model 2
P_{on}	39.3%	7.2%	2.9%	39.3%	15.8%	4.3%
P_{off}	18.8%	4.4%	5.3%	18.9%	9.8%	1.5%

5. Conclusions

In order to estimate the switching loss of SMPS accurately, the relationship between the Miller plateau voltage and the displacement currents through parasitic capacitance of a power MOSFET was analyzed and a quantitative model was derived in this paper. Based on the proposed model, the Miller plateau should have different voltage levels during turn-on/-off, and it also changes according to different load conditions. Using the new Miller plateau, the switching waveform and switching loss can be analyzed and calculated more accurately. Experiment and simulation were performed to verify the proposed new Miller plateau and its use in analyzing switching process. For switching loss prediction, the benchmarking table shows that the achieved average relative error of the proposed Miller plateau-based loss model (Model 1) can be reduced to well below 10%, which is a 50∼75% reduction of the one obtained by the traditional Miller plateau-based model. Moreover, the error can be further reduced to around 5%, the lowest among these loss models, by using the proposed Miller plateau-based model (Model 2), taking into consideration the gate current's variation. The proposed new Miller plateau can be further used to measure the device performance and to help to select the right device and gate driver for designing a high-frequency SMPS.

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Abbreviations

The following abbreviations are used in this manuscript:

CMOS	Complementary metal-oxide semiconductor
DC	Direct current
EMI	Electromagnetic interference
FOM	Figures of merit
KCL	Kirchhoff's current law
IoT	Internet of Things
MOSFET	Metal-oxide-semiconductor field-effect transistor
SMPS	Switching mode power supply
SPICE	Simulation Program with Integrated Circuit Emphasis

Nomenclature

C_{GS}, C_{GD}, C_{DS}	Parasitic interelectrode (gate, drain, and source) capacitances
C_{GS_ext}	External capacitance connected between the gate and source electrodes
C_{DS_ext}	External capacitance connected between the drain and source electrodes
C_{iss}	Input capacitance. Equals $C_{GS} + C_{GD}$
C_{rss}	Reverse transfer capacitance. Equals C_{GD}
C_{oss}	Output capacitance. Equals $C_{DS} + C_{GD}$
f_{sw}	Switching frequency of an SMPS
g_{fs}	Power MOSFET's transconductance in the ACTIVE state
I_{ch}, I_D, I_L	Channel current, drain current, and load current
I_{pl_on}, I_{pl_off}	Miller plateau currents in the turn-on and turn-off processes
I_{avg_on}	Average gate current when V_{GS} changes from V_{TH} to V_{pl_on} during turn-on
I_{avg_off}	Average gate current when V_{GS} changes from V_{pl_off} to V_{TH} during turn-off
K_r	The constant rate when V_{DS} falls linearly from V_{in} to zero during turn-on
K_f	The constant rate when V_{DS} rises linearly from zero to V_{in} during turn-off
L_D, L_S	Parasitic inductances of the drain and source leads
P_{on}, P_{off}	Turn-on and turn-off switching power losses
$R_{DS(on)}$	Drain–source on-state resistance
R_g	Gate resistance
T_S	Switching period of an SMPS
T_f, T_r	Turn-off time and turn-on time
T_{1f} to T_{5f}	Each interval of the turn-off sequence
T_{1r} to T_{5r}	Each interval of the turn-on sequence
τ_m	The time constant related to g_{fs} and L_D
$\tau_{G'}$	The time constant related to R_g and C_{GD}
V_{GS}, V_{GD}, V_{DS}	Gate–source voltage, gate–drain voltage, and drain–source voltage
V_{dr}	Gate driving voltage
V_{pl}	Traditional Miller plateau voltage
V_{pl_on}, V_{pl_off}	Miller plateau voltages in the turn-on and turn-off processes
V_{TH}	Power MOSFET's threshold voltage

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