electronics

MDPI

Article

A Novel Self-Biased Phase-Locked Loop Scheme for WLAN Applications

Peng Li [1,2,*], Tian Tian [1,2], Bin Wu [1] and Tianchun Ye [1,2]

[1] The Intelligent Manufacturing Electronics R&D Center, Institute of Microelectronics of Chinese Academy of Sciences, Beijing 100029, China; tiantian@ime.ac.cn (T.T.); wubin@ime.ac.cn (B.W.); tcye@ime.ac.cn (T.Y.)
[2] School of Electronic, Electrical and Communication Engineering, University of Chinese Academy of Sciences, Beijing 100049, China
* Correspondence: lipeng@ime.ac.cn

Abstract: This article presents a novel self-biased phase-locked loop (PLL) scheme for wireless local area network (WLAN) applications. A novel self-biased circuit that contains a current mirror circuit and a variable resistor circuit related to the frequency division ratio are proposed. The proposed self-biased PLL scheme achieves a fixed damping factor. Moreover, the self-biased technology allows the PLL loop bandwidth to track the input reference frequency and division ratio. The proposed start-up circuit speeds up the locking of the PLL. In addition, the proposed differential-to-single-ended (DTS) converter can guarantee a 50% duty cycle without operating the PLL at twice the chip operating frequency. The proposed self-biased PLL is implemented in a Semiconductor Manufacturing International Corporation (SMIC) 55 nm CMOS process. The measured root-mean-square jitter (RMS-jitter) integrated of PLL is 2.4 ps with a dissipation of 8.6 mW, and the resulting figure-of-merit is −223.05 dBc/Hz.

Keywords: WLAN; self-biased PLL; start-up circuit; DTS converter

Citation: Li, P.; Tian, T.; Wu, B.; Ye, T. A Novel Self-Biased Phase-Locked Loop Scheme for WLAN Applications. *Electronics* **2021**, *10*, 2077. https://doi.org/10.3390/electronics10172077

Academic Editor: Paul Leroux

Received: 22 July 2021
Accepted: 24 August 2021
Published: 27 August 2021

1. Introduction

In recent years, the rapid development of WLANs has played an increasingly important role in communication systems. The PLL is one of the most critical building blocks in wireless transceivers [1–4]. The constantly updated WLAN technology introduces higher requirements on frequency synthesizers. A PLL that multiplies low-frequency reference clocks to generate high-frequency clocks is usually designed with a ring voltage-controlled oscillator (ring-VCO) or an LC VCO. However, an LC VCO shows high sensitivity to magnetic coupling and occupies a large silicon area. Hence, the ring-VCO-based PLL is preferable in many applications. Its main advantages are a very small die area, which reduces the integrated circuit (IC) cost and helps minimize the substrate noise and spur coupling, and a wide tuning range.

PLL is a closed-loop feedback system [5–7]. The loop bandwidth and damping factor of the PLL will affect the PLL loop characteristics, such as the stability and locking time [8–10]. Usually, the PLL output frequency is variable, and there is an output range, especially for wideband PLL. We usually adjust the PLL output frequency by changing the reference frequency and the division ratio of the divider. However, the loop bandwidth of the traditional PLL cannot track the reference input frequency and the loop frequency division ratio, resulting in a narrow operating frequency range. Moreover, the loop bandwidth is set to be small for stability, resulting in a long locking time and poor jitter performance. The loop damping factor is affected by the frequency division ratio and the process, voltage, temperature (PVT). It is not a fixed value, which leads to the deterioration of the stability of the PLL. The problems mentioned above pose a higher challenge for the design of high-performance PLLs.

The PLL based on self-biased techniques is attractive for solving these problems [11–15]. The self-biased PLL has the following advantages:

- It is completely self-biased and does not require additional voltage and current bias circuits, so it has a smaller area.
- The loop bandwidth follows the input reference frequency. The loop bandwidth can be set to be relatively large, so that the lock time of the PLL is relatively short, and the anti-jitter ability is relatively strong.
- The self-biased phase-locked loop has a fixed damping factor, and the stability of the loop is not affected by the input reference frequency, frequency division ratio, etc., so the stability of the self-biased phase-locked loop is very good.
- The damping factor and the ratio of loop bandwidth to input reference frequency are completely determined by the ratio of capacitance and have nothing to do with the PVT and other factors.
- The self-biased PLL can automatically adjust the operating point of the bias circuit to the optimum according to the working environment (the oscillation frequency of the VCO), thereby achieving self-adaptation.
- The self-biased PLL can adapt to different input reference frequencies and frequency division ratios, and can adapt well to different application requirements.

However, many self-biased PLLs [11–13] whose loop bandwidth cannot track the division ratio have removed the division ratio effect, and the bandwidth is unchanged when the reference clock is stable. The low-pass filter (LPF) is a key module in PLL. It converts the charge/discharge current of the charge-pump (CP) into VCO tuning voltage, filters the ripple on VCO tuning voltage, reduces the fluctuation of VCO tuning voltage, and improves the jitter performance of PLL. Although PLLs use self-biased technology in reference [11,12], all those mentioned above use first-order LPF. The first-order LPF cannot effectively filter the ripple of VCO tuning voltage and also makes PLL unable to achieve low phase noise and jitter performance. Therefore, second-order or third-order LPF is required to obtain low jitter PLL. The bias generation circuits in [13] occupy a large area. Although a self-biased PLL without any bias circuit [14] was proposed, the operational amplifier (OPA) in the voltage-to-current (VI) converter consumes considerable power, especially when the loop bandwidth is large. Moreover, because the charge/discharge current of the self-biased PLL is a monotonically increasing function of the VCO frequency, it is extremely low when the VCO begins oscillating after a power-up. Therefore, the classical self-biased PLL always exhibits a very long power-up latency to approach locking at a required frequency. To speed up the locking process of the PLL, an initialization circuit is added to the PLL [15]. The function of this initialization circuit is to set the current of the charge-pump to the maximum value and discharge the tuning voltage of the VCO close to the ground level when the PLL is powered on. At this time, the VCO oscillates at the highest frequency. If the target frequency is high, the locking time of the PLL will be reduced. However, if the target frequency is low, the locking time will still be very long.

Based on the problem mentioned above, this paper presents a novel self-biased PLL scheme. The main contributions of this paper are listed below:

- The novel self-biased scheme is very simple to implement and has the characteristics of small area and low power consumption.
- Regardless of whether the target frequency is high or low, the proposed start-up circuit is very effective and can accelerate the locking of the PLL.
- A differential-to-single-ended (DTS) converter is presented to reduce the operating frequency and obtain a single-ended output with a 50% duty cycle.

In this paper, a novel self-biased circuit that contains a current mirror circuit and a variable resistor circuit related to the frequency division ratio is proposed. The variable resistor is used in the LPF. The second-order LPF is used in the proposed PLL, which is a third-order PLL, to obtain better phase noise and jitter performance. Moreover, the bias current of the charge-pump and VCO is provided by the self-biased circuit, which

limits power consumption and area. With the self-biased circuit, both the current of the VCO delay cells and the charge/discharge (I_{CP}) current of the charge-pump change with the VCO tuning voltage of (V_{CTRL}) by quadratic functions. Therefore, a start-up circuit is needed to speed up the PLL locking. The proposed start-up circuit can increase the VCO tuning voltage to 600 mV in a very short time. Moreover, when the VCO tuning voltage is pulled to 600 mV, the start-up circuit is automatically closed without affecting the normal operation and locking of the PLL. In addition, a DTS converter is presented to reduce the operating frequency and obtain a single-ended output with a 50% duty cycle.

2. The Traditional PLL

A traditional PLL is shown in Figure 1. It consists of a phase/frequency detector (PFD), a charge-pump, an LPF, a VCO, and a divide-by-N frequency divider. When PLL is locked, there is no phase error between the reference clock and the divider output clock for the charge-pump PLL.

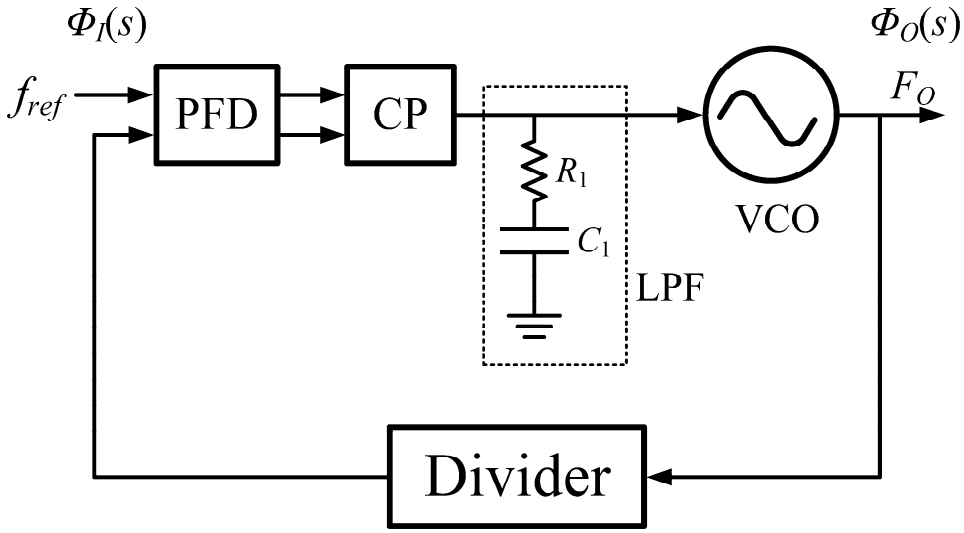


Figure 1. Traditional PLL block diagram.

The closed-loop response of the traditional PLL can be easily obtained as Equation (1).

$$\frac{\Phi_O(s)}{\Phi_I(s)} = \frac{N \times (1 + s \cdot C_1 \cdot R_1)}{1 + s \cdot C_1 \cdot R_1 + s^2 \cdot N \cdot C_1 \cdot 2\pi/(K_{VCO} \cdot I_{CP})} \tag{1}$$

where $\Phi_I(s)$ is the input phase, $\Phi_O(s)$ is the output phase, R_1 is the loop filter resistor, C_1 is the loop filter capacitance, I_{CP} is the charge pump current, N is the divider division ratio, and K_{VCO} is the VCO gain.

We prefer, from control theory, to express the denominator in the form $s^2 + 2\zeta\omega_n s + {\omega_n}^2$. Thus,

$$\frac{\Phi_O(s)}{\Phi_I(s)} = N \cdot \frac{1 + 2 \cdot \zeta \cdot (s/\omega_n)}{1 + 2 \cdot \zeta \cdot (s/\omega_n) + (s/\omega_n)^2} \tag{2}$$

The expressions of the damping factor ζ and the loop bandwidth ω_n are as follows:

$$\zeta = \frac{R_1}{2} \cdot \sqrt{\frac{I_{CP} \cdot K_{VCO} \cdot C_1}{2\pi N}} \tag{3}$$

$$\omega_n = \frac{2 \cdot \zeta}{R \cdot C_1} \tag{4}$$

The loop bandwidth and damping factor describe the closed-loop response characteristics of PLL and are important system parameters to be considered when designing PLL. The damping factor ζ has an important influence on the dynamic performance of

the PLL. For a critically-damped response, $\zeta=\sqrt{2}/2$, we typically choose ζ in the range of $\sqrt{2}/2$ and 1. The loop bandwidth ω_n must be a decade below the reference frequency for stability. In addition, ω_n should be positioned as close as possible to ω_{ref} to minimize the total phase error. For a typical PLL, the charge-pump current I_{CP}, VCO gain K_{VCO}, loop filter capacitance C_1, and loop filter resistance R_1 are changed because of variations in the PVT. Moreover, the division ratio N varies with the PLL output frequency. Therefore, ζ and ω_n are changed because of the variation in these parameters. Thus, the loop characteristics of PLL are changeable.

3. The Proposed Self-Biased PLL

In a typical PLL, ω_n and ζ vary with division ratio N and PVT. In this paper, we propose a novel self-biased PLL scheme to solve the above problems. The proposed self-biased PLL shown in Figure 2 is a part of the Wi-Fi chip we designed, and this Wi-Fi chip supports the 802.11ac protocol. The self-biased circuit provides bias voltage and current for the charge-pump, VCO, and LPF. The resistor in LPF is a variable resistor. The VCO is followed by the DTS converter. The start-up circuit is designed to speed up PLL locking by giving the VCO tuning voltage (V_{ctrl}) an initial value when the PLL starts to work. The PLL has four outputs, among which F_{VCO} is directly generated by VCO. The VCO is followed by three dividers, which generate F_{O1}, F_{O2}, and F_{O3}. The operating frequency of the VCO in the proposed PLL is 960 MHz. The oscillating signal of the VCO passes through two frequency dividers with a frequency division ratio of 6 to generate two clock signals with a frequency of 160 MHz for the analog-to-digital converter (ADC) and baseband, and a frequency divider with a frequency division ratio of 80 to produce a clock signal with a frequency of 12 MHz for the universal serial bus (USB).

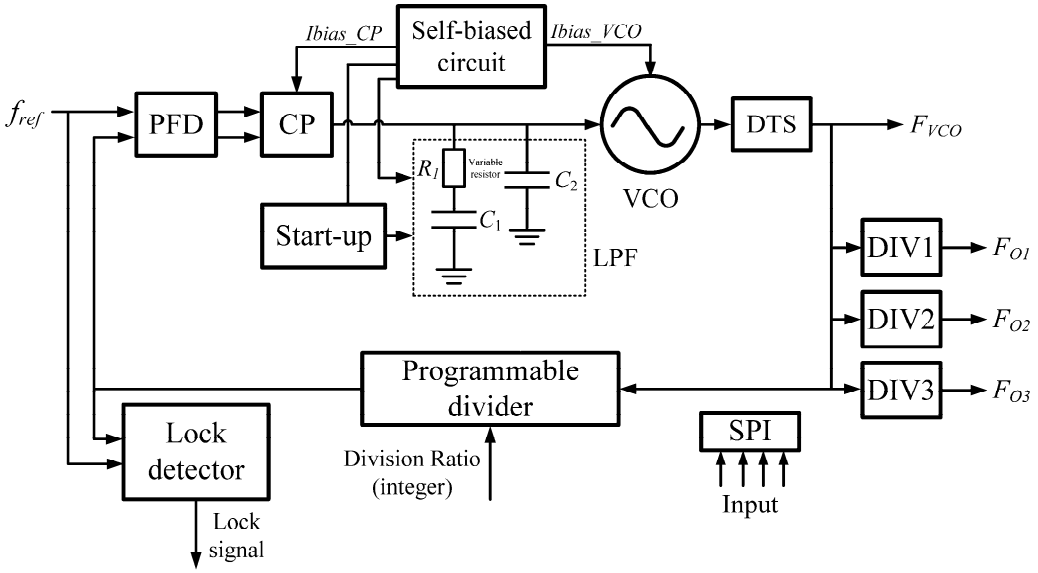


Figure 2. The proposed self-biased PLL.

3.1. The Self-Biased Circuit

The proposed self-biased circuit is shown in Figure 3. N[0], N[1], N[2], N[3], N[4], N[5], N[6], and N[7] are the corresponding bits of the 8-bit programmable frequency divider.

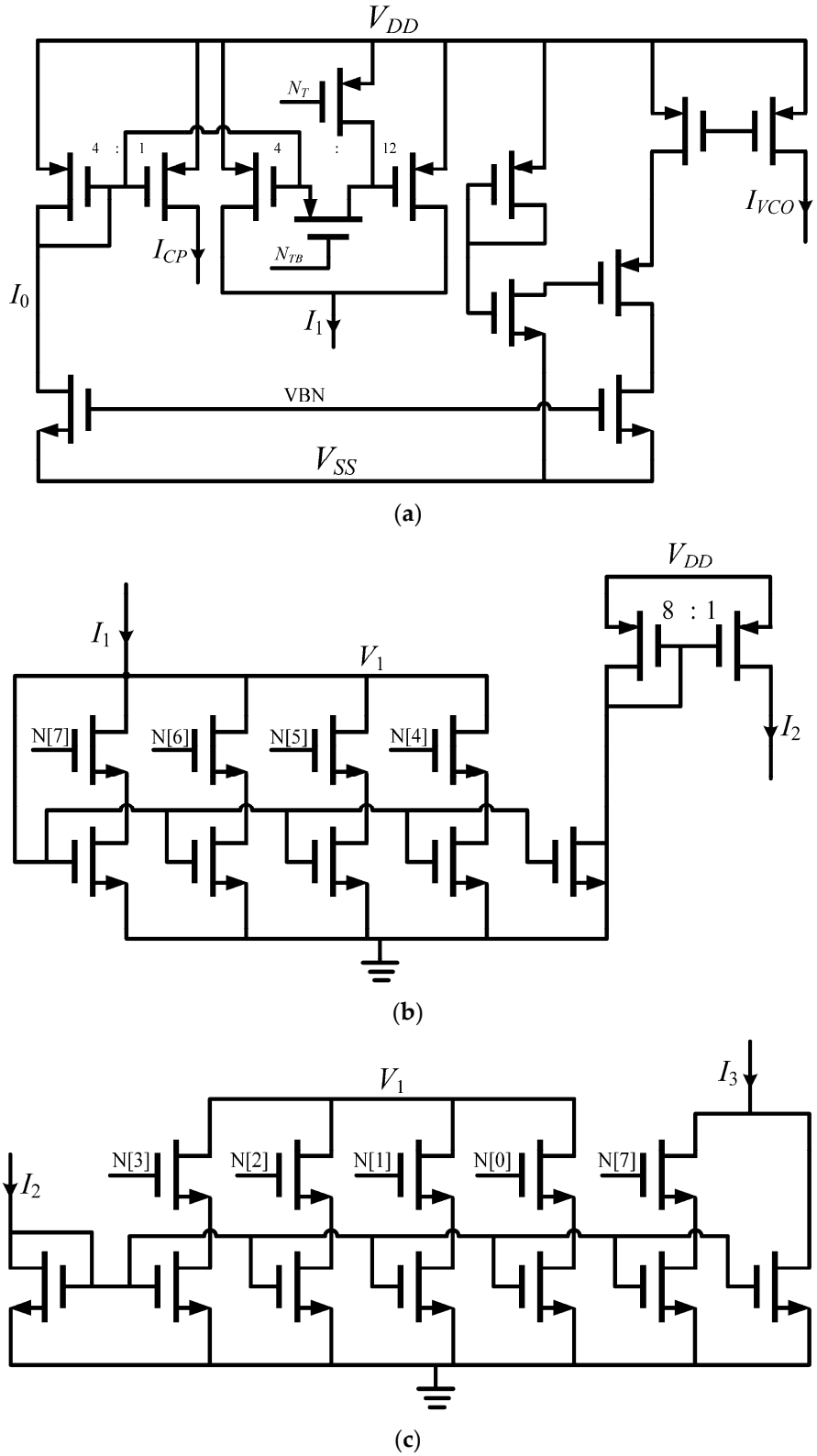


Figure 3. The proposed self-biased circuit: (**a**) The current of the circuit is related to the tuning voltage of the VCO; (**b**) The current of the circuit is related to the upper four bits of the control word of the frequency divider; (**c**) The current of the circuit is related to the lower four bits of the control word of the frequency divider.

The current I_1 is related to I_0 by

$$I_1 = (N_T \times 3 + 1) \times I_0 \tag{5}$$

where N_T is the OR logic of the 5th, 6th, and 7th bits of the divider. That is, N_T is given by

$$N_T = N[5] + N[6] + N[7] \tag{6}$$

N_{TB} is the inverse of the N_T.

The current I_{CP} is related to I_0 by

$$I_0 = 4 \times I_{CP} \tag{7}$$

The current I_2 is related to I_1 by

$$I_2 = \frac{2 \times I_1}{N} \tag{8}$$

where N is the division ratio of the divider.

The current I_3 is related to I_2 by

$$I_3 = (N[7] \times 1 + 1) \times I_2 \tag{9}$$

The current I_3 is related to I_1 by

$$I_3 = (N[7] \times 1 + 1) \times \frac{2 \times I_1}{N} \tag{10}$$

The current I_3 is related to I_0 by

$$I_3 = \frac{2 \times (N_T \times 3 + 1) \cdot (N[7] \times 1 + 1)}{N} \cdot I_0 = Y \cdot I_0 \tag{11}$$

where Y is given by

$$Y = \frac{2 \times (N_T \times 3 + 1) \cdot (N[7] \times 1 + 1)}{N} \tag{12}$$

3.2. The LPF with a Variable Resistor

The proposed variable resistor is shown in Figure 4. The variable resistor is composed of three branches. N7B is the inverse of the $N[7]$. The transistor size ratio of each branch is 1:6:2. β_P, $\beta_P = \mu_P \cdot C_{ox} \cdot W/L$, represents the transistor parameters of the smallest size branch, and X represents the relationship between the total size of the transistor of the variable resistor and the smallest size branch.

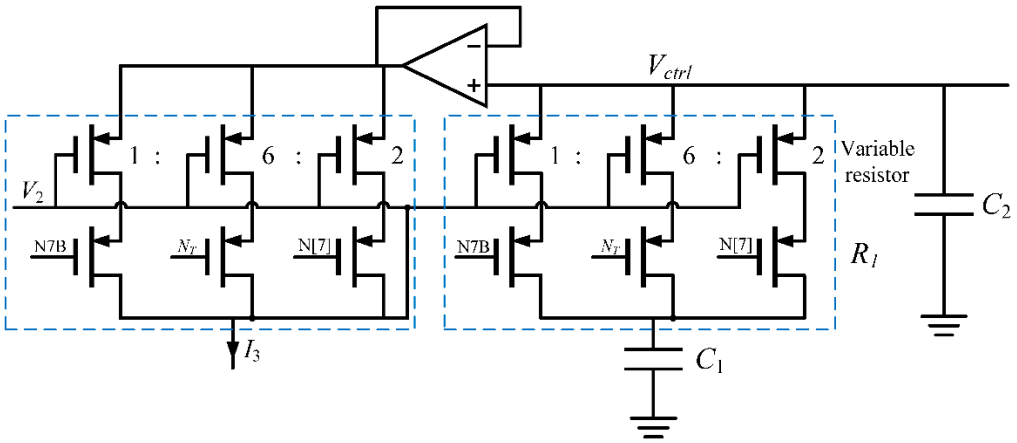


Figure 4. The LPF with a variable resistor.

X is then given by

$$X = \frac{8}{(N_T \times 3 + 1) \times (N[7] + 1)} \tag{13}$$

The product of X and Y is given by

$$X \cdot Y = \frac{8}{(N_T \times 3 + 1) \times (N[7] + 1)} \cdot \frac{2 \times (N_T \times 3 + 1) \cdot (N[7] \times 1 + 1)}{N} = \frac{16}{N} \tag{14}$$

Then, the resistance of the variable resistor is given by

$$R_1 = \frac{1}{g_{totalm}} = \frac{1}{\sqrt{2 \cdot \beta_P \cdot X \cdot I_3}} = \frac{1}{8} \cdot \sqrt{\frac{N}{2 \cdot \beta_P \cdot I_{CP}}} \tag{15}$$

3.3. The Proposed Ring-VCO

The requirements of ADC, baseband, and USB for clock jitter performance are not very high. For example, the ADC that we designed requires that the clock jitter is less than 5 Ps. Therefore, considering the phase noise, jitter performance, complexity, area, power consumption, and other factors, we chose the ring oscillator. A ring-VCO consists of many gain stages in a loop. The total number of inversions in the loop must be odd so that the circuit does not latch up. In contrast, the differential implementation can utilize an even number of stages by simply configuring one stage such that it does not invert [16,17]. This flexibility demonstrates another advantage of differential circuits over their single-ended counterparts. The number of stages in a ring-VCO is determined by various requirements, including speed, power dissipation, and noise immunity. In most applications, three to five stages provide optimum performance (for differential implementations).

The top architecture of the proposed ring-VCO with three-stage delay cells is illustrated in Figure 5a. Since each delay cell contributes noise, the three-stage structure can achieve lower phase noise as compared to four- or more-stage designs. The ring-VCO delay cells are the differential buffer delay stages with symmetric loads. Figure 5b presents the buffer stage which includes a source coupled pair with resistive load elements, called symmetric loads [9]. Because the effective resistance of the load elements changes with V_{BN}, the buffer delay also changes with V_{BN}. In addition, the cross-coupled transistors M1 and M2 in Figure 5b increase the charge and discharge current of the delay cell, which improves the flip speed of the output level.

The three-stage VCO oscillation frequency is:

$$f_{VCO} = \frac{1}{2 \cdot 3 \cdot t} = \frac{\sqrt{2 \cdot k \cdot I_D}}{C_T} \tag{16}$$

where C_T is the total VCO capacitance, $k = \mu_n \cdot C_{ox} \cdot W/L$, and I_D is the drain current for one of the diode-connected NMOS devices biased at VBN. Thus, the VCO gain K_{VCO} is as follows:

$$K_{VCO} = \left| \frac{df_{VCO}}{dV_{ctrl}} \right| = \frac{k}{C_T} \tag{17}$$

Then, the damping factor ζ is given by

$$\begin{aligned} \zeta &= \tfrac{R_1}{2} \cdot \sqrt{\tfrac{I_{CP} \cdot K_{VCO} \cdot C_1}{2\pi N}} \\ &= \tfrac{1}{2} \cdot \tfrac{1}{8} \cdot \sqrt{\tfrac{N}{2 \cdot \beta_P \cdot I_{CP}}} \cdot \sqrt{\tfrac{I_{CP} \cdot K_{VCO} \cdot C_1}{2\pi N}} \\ &= \tfrac{1}{32} \cdot \sqrt{\tfrac{k}{\pi \cdot \beta_P}} \cdot \sqrt{\tfrac{C_1}{C_T}} \end{aligned} \tag{18}$$

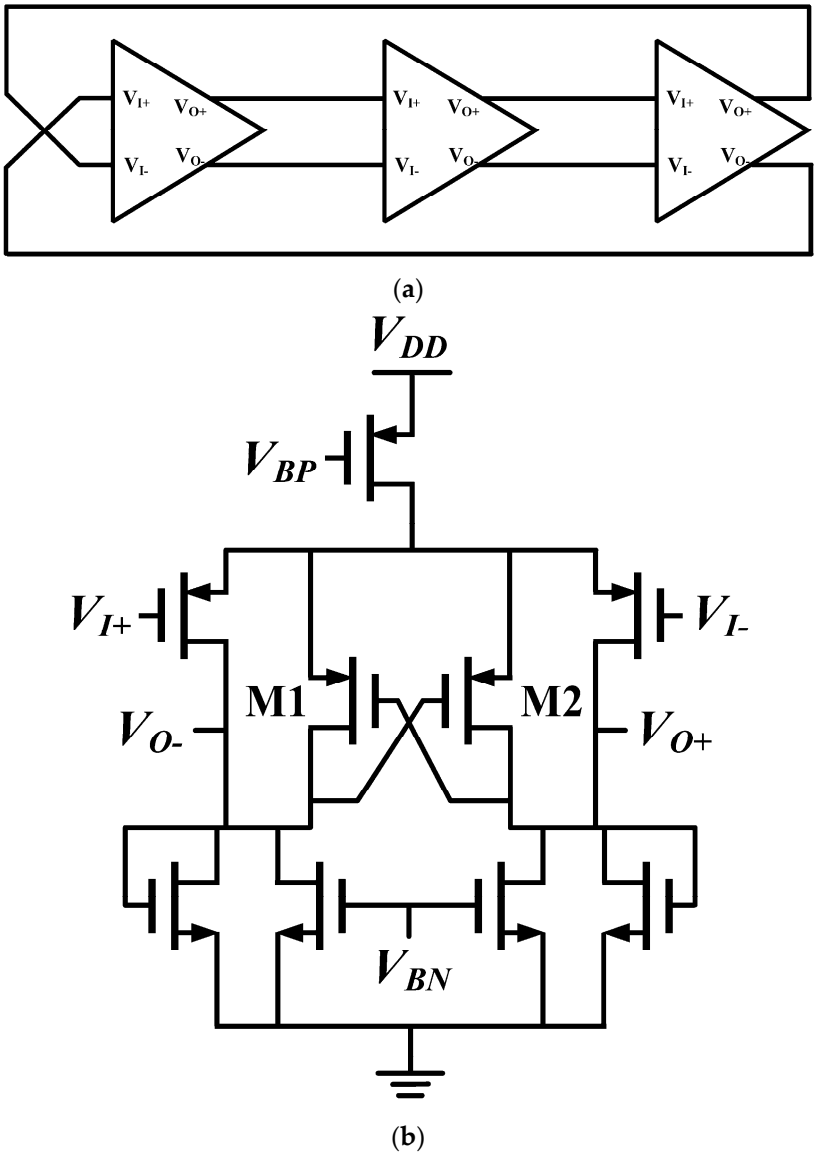


Figure 5. Three-stage ring-VCO: (**a**) top-level; (**b**) the delay cell.

The loop bandwidth ω_n to operating frequency ratio is:

$$\begin{aligned} \frac{\omega_n}{\omega_{ref}} &= \frac{2\cdot\zeta}{R_1\cdot C_1}\cdot\frac{N}{2\pi f_{VCO}} \\ &= \sqrt{\frac{I_{CP}\cdot K_{VCO}\cdot C_1}{2\pi N}}\cdot\frac{1}{C_1}\cdot\frac{N\cdot C_T}{2\pi\sqrt{2\cdot k\cdot I_D}} \\ &= \frac{\sqrt{N}}{8\pi\sqrt{2\pi}}\cdot\sqrt{\frac{C_T}{C_1}} \end{aligned} \tag{19}$$

Equations (18) and (19) show that the damping ζ and the loop bandwidth ω_n to operating frequency ratio are constant, and are determined by the capacitance ratio. Equation (19) shows that, with a given N, the bandwidth is proportional to the input reference clock. When N is increased, the bandwidth increases to suppress more VCO noise to achieve better jitter performance. This means that the PLL will be more robust and stable.

3.4. Start-Up Circuit

Self-biased topology avoids the necessity of external biasing. However, the nonlinear capture behavior of a self-biased PLL results in very long power-up latency, which is unacceptable for most applications. With the bias generator, both the VCO delay cells

currents and the charge-pump discharge/charge (I_{CP}) currents change with V_{CTRL} by quadratic functions [18,19]. Therefore, a start-up circuit is needed to speed up PLL locking.

The proposed start-up circuit is shown in Figure 6. When the PLL is powered on, SWB and PR are low. TE is also low. Transistor M3 mirrors the current to transistor M4, and transistor M2 mirrors the current to transistor M5. SWB turns on transistor M6, charging V_{C1} to 600 mV. When the voltage of V_{C1} is 600 mV, the transistor M10 is turned on, then the SWB becomes high, and transistor M6 is turned off. At this time, the start-up circuit is closed and the PLL starts to work normally. The SWB and V_{C1} levels with time are shown in Figure 7. Figure 7 shows that the V_{C1} level is pulled up to 600 mV at approximately 4.3 µs, and the SWB level changes from low to high. The SWB level changes from low to high, which turns off transistor M6, and the start-up circuit no longer works. The PLL lock signal is presented in Figure 8. Figure 8 shows that the lock signal becomes high at approximately 27 µs, which indicates that the proposed PLL has been locked. The lock time fully meets the usage requirements.

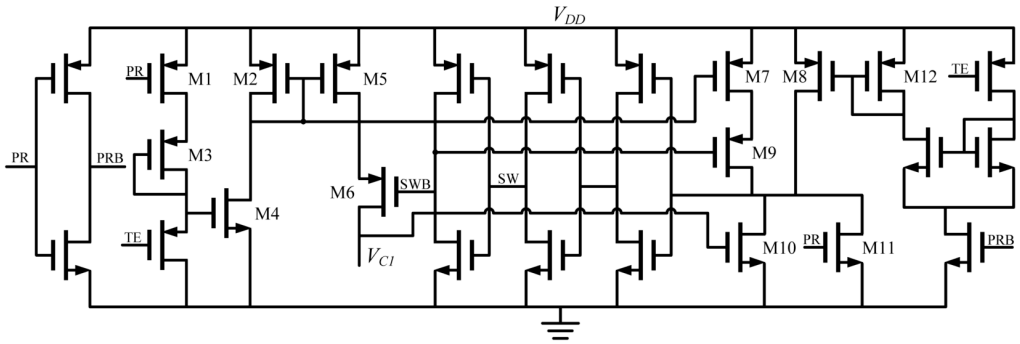


Figure 6. The start-up circuit.

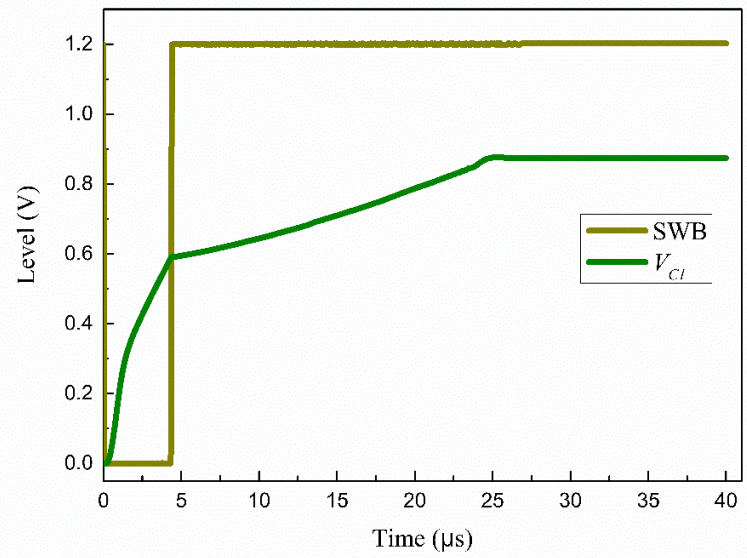


Figure 7. The SWB and V_{C1} levels with time.

3.5. Differential-to-Single-Ended Converter

Generally, the PLL output should be 50% duty cycle [20,21]. We usually use a divider which is divided by 2 to get a 50% duty cycle. Figure 9 shows the proposed DTS converter scheme. The circuit can generate the needed output clock with a 50% duty cycle. It is made up of two PMOS differential amplifiers driving two CMOS inverters and connected by the cross-coupled transistors M1 and M2 that increase the flip speed of the output level. The two PMOS differential amplifiers use the same current source bias voltage, V_{BP}, as the VCO delay cells. The role of the two PMOS differential amplifiers is to provide signal

amplification. The CMOS inverters provide additional signal amplification and conversion to a single-ended output whose range extends from rail to rail. However, if we use a divider to generate a 50% duty cycle output, the VCOs are designed to operate at twice the chip operating frequency. When the output signal frequency is high with a 50% duty cycle, the designed VCO works at a higher frequency. Therefore, to generate a 50% duty cycle output, this circuit's design constraints can be relaxed [9].

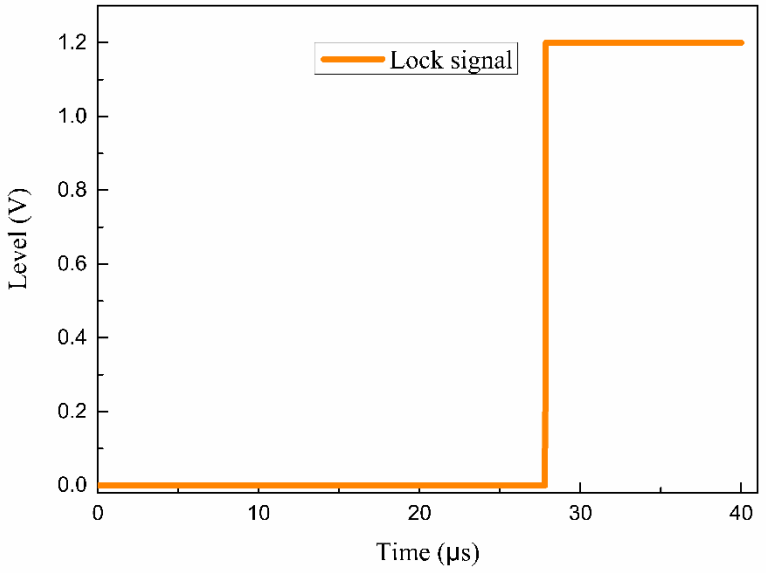


Figure 8. The lock signal with time.

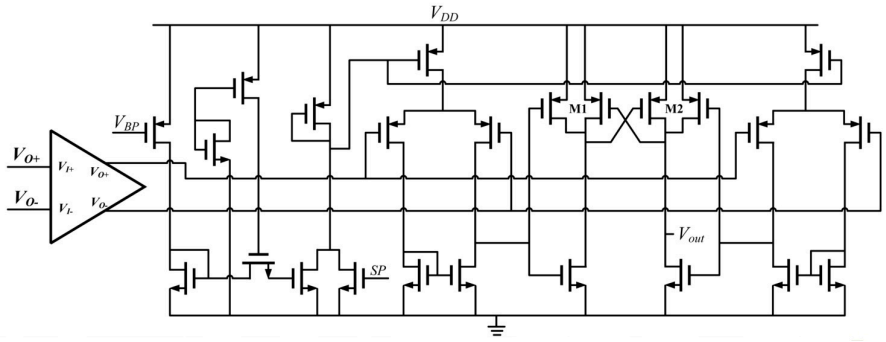
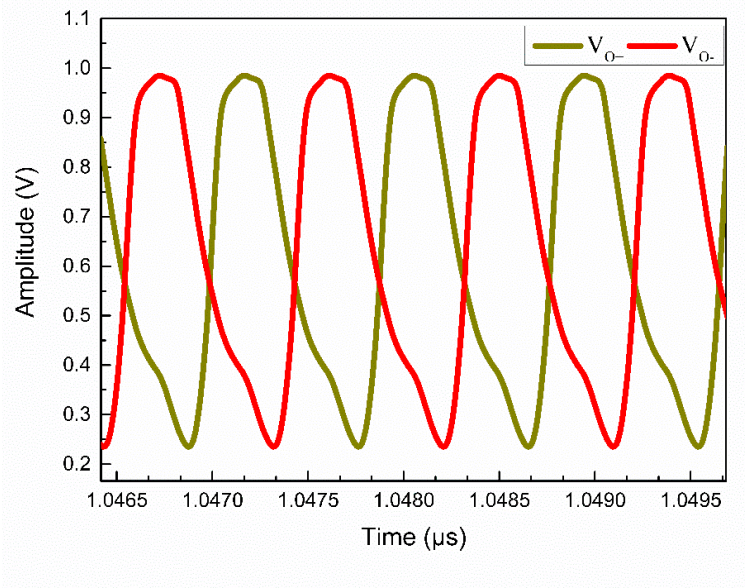
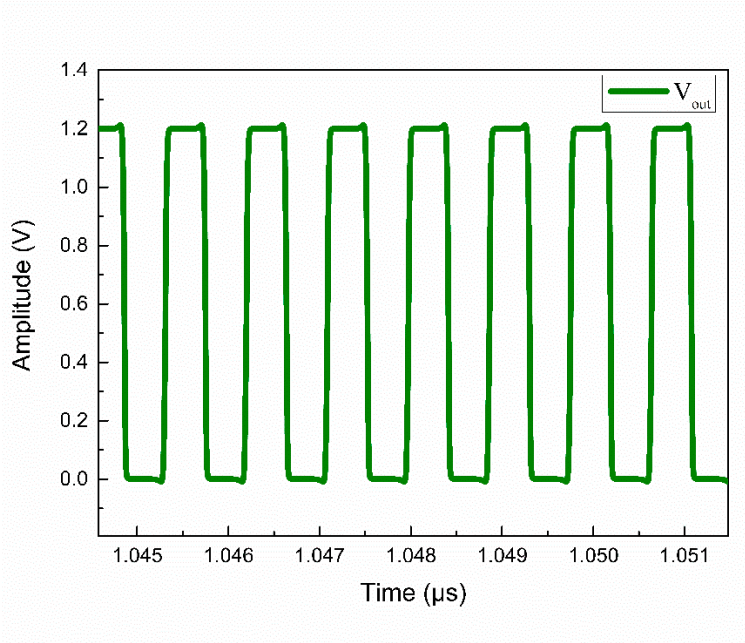


Figure 9. Scheme of the differential-to-single-ended converter.

Figure 10 illustrates the waveform of the input and output clock of the DTS converter. Figure 10a shows the output clock of the ring-VCO, which is the input clock of the DTS converter. As shown in Figure 10a, because of the voltage limitation, the ring-VCO amplitude is not so large that it may not be used directly in digital circuits. Moreover, when the working frequency of the ring-VCO is low, the ring-VCO amplitude will be close to the threshold voltage. The output clock of the DTS converter is shown in Figure 10b, and its output range extends from rail to rail. In addition, the duty cycle of the output clock is 50%. In this case, the output clock can be directly used in digital circuits.



(**a**)



(**b**)

Figure 10. The waveforms of the input and output clocks of the DTS converter: (**a**) input clock; (**b**) output clock.

4. Measurement Results

A micrograph of the proposed PLL fabricated using the SMIC 55 nm CMOS process is shown in Figure 11, and the chip occupies 253 μm × 349 μm, excluding the I/O pads. The PLL utilizes a reference clock of 40 MHz, which is a crystal oscillator that occupies 290 μm × 136 μm and is integrated into the PLL chip. The proposed crystal oscillator scheme is shown in Figure 12. It is a parallel crystal oscillator based on the Colpitts structure. The crystal oscillator in the chip photo, which includes resistors, capacitor arrays, inverters, and buffers, is the rest of the circuit except the crystal (the dashed box in Figure 12). The crystal is soldered on the printed circuit board (PCB) and directly connected to the chip. The chip measurement setup is shown in Figure 13. The output level of the lock detector is shown in Figure 14. Figure 14a shows the output level of the lock detector

when the PLL is not locked. Figure 14b shows the output level of the lock detector when the PLL is locked. As shown in Figure 14b, the proposed PLL can be locked normally. When the output frequency of VCO is 960 MHz, the output clock frequency of the VCO signal passing through the three-way frequency divider is 160 MHz, 160 MHz, and 12 MHz. Figure 15 shows the waveform and spectrum of 160 MHz output.

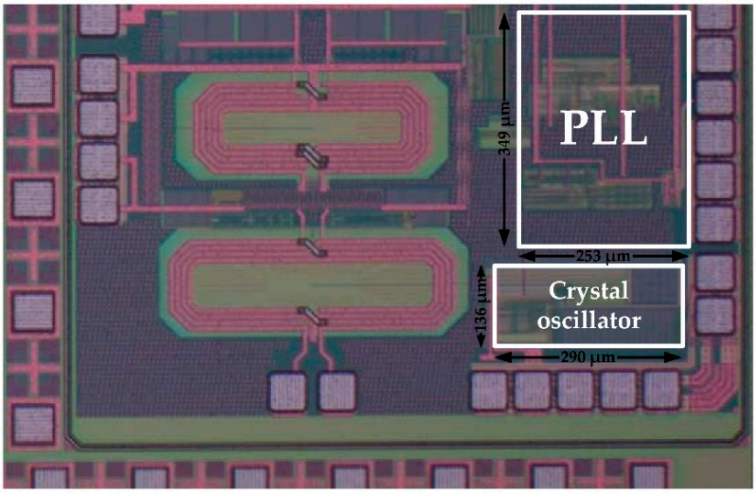


Figure 11. Chip micrograph of the proposed PLL.

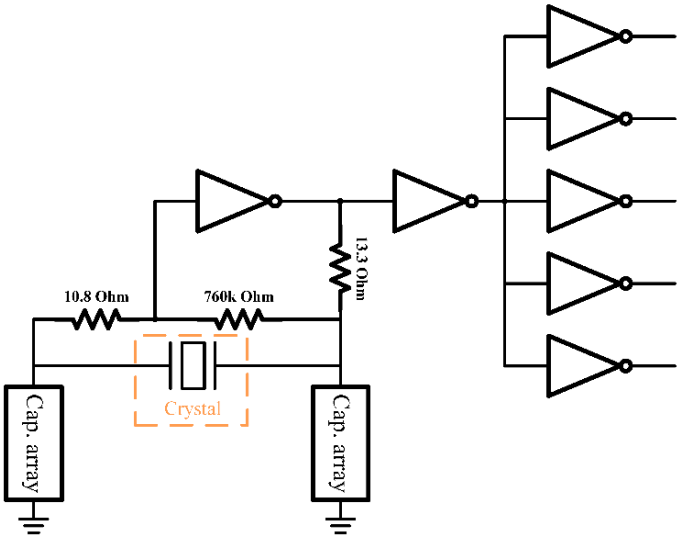


Figure 12. The proposed crystal oscillator scheme.

A Rohde & Schwarz FSW50 signal and spectrum analyzer was used to test the phase noise of the PLL. Figure 16 shows the phase noise of the proposed PLL at a carrier frequency of 960 MHz. The phase noise of the designed PLL is –104.8 dBc/Hz at a 1 MHz frequency offset. The RMS jitter integrated from 10 kHz to 10 MHz is 2.4 ps. There is a spike shown in Figure 16 at a frequency offset of 40 MHz. The spike, called the reference spur in the spectrum, comes from a reference clock with a frequency of 40 MHz generated by the crystal oscillator. The reference spur is caused by the mismatch of the charge and discharge currents of the charge-pump, which will generate periodic ripples on the tuning voltage of the VCO. A summary of the measured results and performance comparison is given in Table 1. Table 1 shows that the figure-of-merit (FoM) is also better than most of the works listed in Table 1.

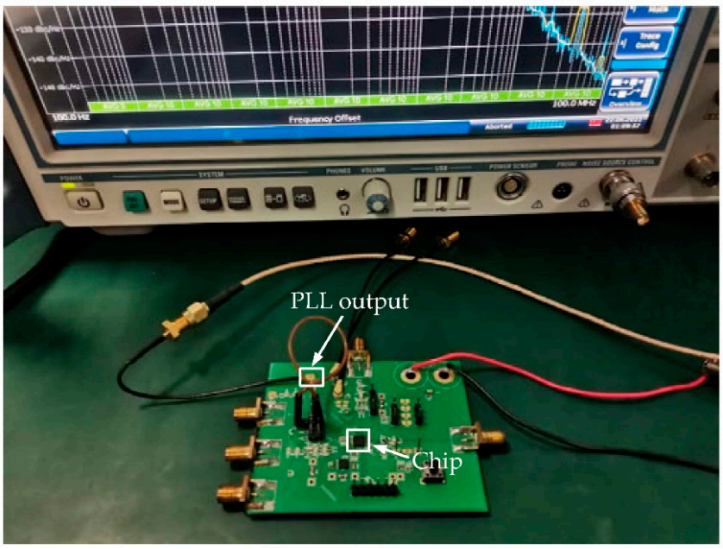
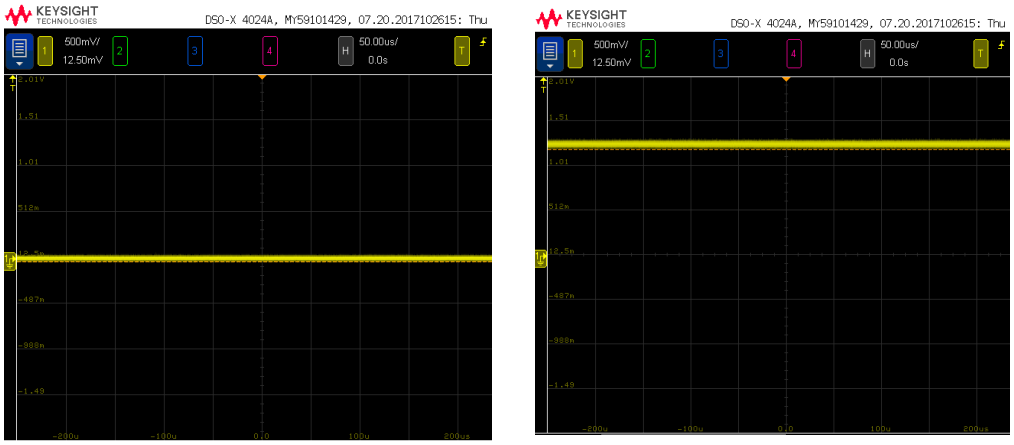
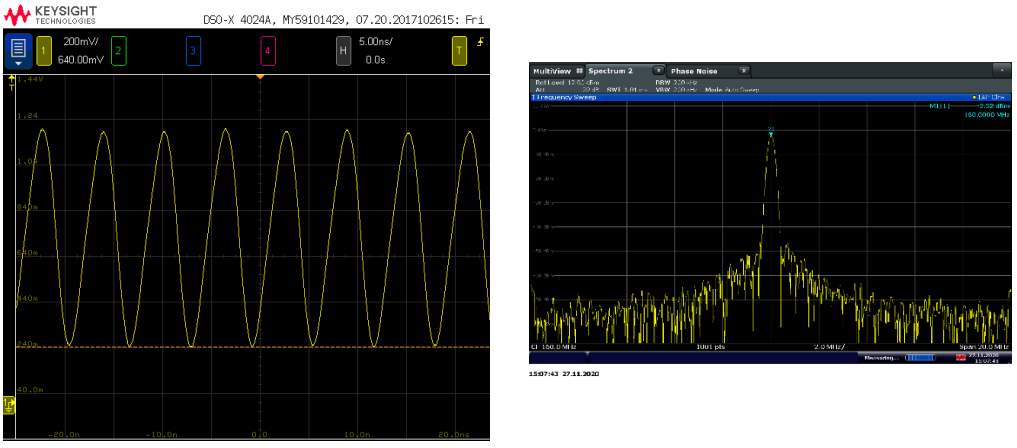


Figure 13. Measurement setup.



(**a**) (**b**)

Figure 14. The output level of the lock detector. (**a**) The PLL is not locked; (**b**) the PLL is locked.



(**a**) (**b**)

Figure 15. The output waveform and spectrum of 160 MHz. (**a**) The waveform; (**b**) the spectrum.

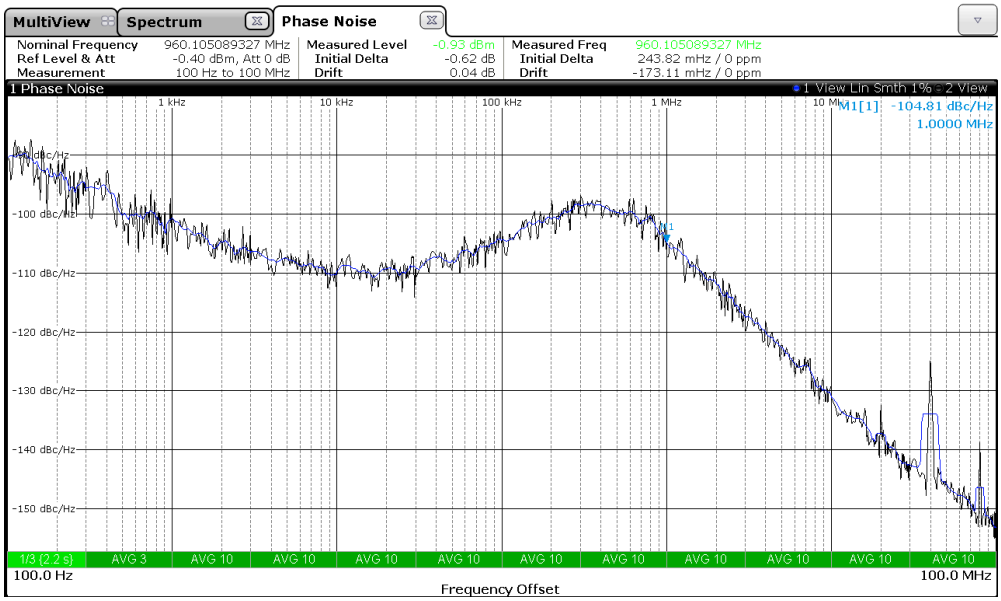


Figure 16. Measured phase noise of the proposed PLL.

Table 1. Performance summary and comparison.

	Tech. (nm)	Osci. Topo.	Freq. Range (GHz)	Freq. (GHz)	Phase Noise (dBc/Hz)	RMS jitter (ps)	Power (mW)	FoM * (dBc/Hz)
This work	55	Ring-VCO	0.51–1.45	0.96	–104.8 @ 1 MHz	2.4	8.6	–223.05
5	180	Ring-VCO	0.06–1.92	0.48	–112 @1 MHz	2.61	17.4	–219.25
11	65	Ring-VCO	1.25–6.25	6.25	–110 @1 MHz	0.78	3.1	–237.2
14	65	Ring-VCO	1.25–3.125	3.125	-	1.65	28.8	–221.1
16	180	Ring-VCO	0.5–2.5	1	-	3.11	25	–218.6
17	130	Ring-VCO	2.35–2.55	2.4	–96.01 @1 MHz	-	10.7	-

* FoM = 20 log(J_{RMS}/1 s) + 10 log(P_{DC}/1 mW)

5. Conclusions

This paper demonstrated a novel self-biased PLL scheme. The proposed self-biased PLL scheme achieves a fixed damping factor and allows the PLL loop bandwidth to track the input reference frequency and division ratio. The proposed start-up circuit can raise the VCO tuning voltage to 600 mV in a very short time. Moreover, when the VCO tuning voltage is pulled to 600 mV, the start-up circuit is automatically closed. The DTS converter is presented to reduce the operating frequency and obtain a single-ended output with a 50% duty cycle. The RMS jitter integrated from 10 kHz to 10 MHz is 2.4 ps at a carrier frequency of 960 MHz.

Author Contributions: Conceptualization, P.L.; methodology, P.L.; software, P.L. and T.T.; validation, P.L. and T.T.; formal analysis, P.L.; investigation, P.L.; resources, P.L.; data curation, P.L.; writing—original draft preparation, P.L.; writing—review and editing, P.L.; visualization, P.L.; supervision, B.W.; project administration, B.W. and T.Y.; funding acquisition, B.W. and T.Y. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the National Major Science and Technology Program of China grant number 2013ZX03004007.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Tsai, T.-H.; Sheen, R.-B.; Chang, C.-H.; Hsieh, K.C.-H.; Staszewski, R.B. A Hybrid-PLL (ADPLL/Charge-Pump PLL) Using Phase Realignment with 0.6-us Settling, 0.619-ps Integrated Jitter, and −240.5-dB FoM in 7-nm FinFET. *IEEE Solid State Circuits Lett.* **2020**, *3*, 174–177. [CrossRef]
2. Seol, J.-H.; Choo, K.; Blaauw, D.; Sylvester, D.; Jang, T. A 67-fsrms Jitter, −130 dBc/Hz In-Band Phase Noise, −256-dB FoM Reference Oversampling Digital PLL with Proportional Path Timing Control. *IEEE Solid State Circuits Lett.* **2020**, *3*, 430–433. [CrossRef]
3. Tao, J.; Heng, C.-H. ΔΣ Fractional-N PLL With Hybrid IIR Noise Filtering. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2020**, *67*, 1004–1008. [CrossRef]
4. Fu, J.S.; Teo, T.H.; Tan, E.L. Fully integrated frequency synthesizer design for wireless network application with digital programmability. *Microw. Opt. Technol. Lett.* **2007**, *49*, 2579–2582. [CrossRef]
5. Zou, W.; Ren, D.; Zou, X. A wideband low-jitter PLL with an optimized Ring-VCO. *IEICE Electron. Exp.* **2020**, *17*, 20190703. [CrossRef]
6. Hu, A.; Liu, D.; Zhang, K. A 0.03- to 3.6-GHz Frequency Synthesizer with Self-Biased VCO and Quadrature-Input Quadrature-Output Frequency Divider. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2019**, *66*, 1997–2001. [CrossRef]
7. Li, Z.; Cheng, G.; Han, T.; Li, Z.; Tian, M. A 23–36.8-GHz Low-Noise Frequency Synthesizer with a Fundamental Colpitts VCO Array in SiGe BiCMOS for 5G Applications. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **2020**, *28*, 2243–2256. [CrossRef]
8. Gardner, F. Charge-Pump Phase-Lock Loops. *IEEE Trans. Comm.* **1980**, *28*, 1849–1858. [CrossRef]
9. Maneatis, J.G. Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques. *IEEE J. Solid State Circuits* **1996**, *31*, 1723–1732. [CrossRef]
10. Kuo, Y.-F.; Yang, M.-H.; Chiang, Y.-C. A 5-GHz Adjustable Loop Bandwidth Frequency Synthesizer with an On-Chip Loop Filter Array. *IEEE Microw. Wirel. Compon. Lett.* **2021**, *31*, 72–75. [CrossRef]
11. Yuan, B.; Liu, H. A generalized low power and lower jitter charge pump PLL. In Proceedings of the 2013 International Workshop on Microwave and Millimeter Wave Circuits and System Technology, Emeishan, China, 24–25 October 2013; p. 471.
12. Maneatis, J.G.; Kim, J.; McClatchie, I.; Maxey, J.; Shankaradas, M. Self-biased high-bandwidth low-jitter 1-to-4096 multiplier clock generator PLL. *IEEE J. Solid State Circuits* **2003**, *38*, 1795–1803. [CrossRef]
13. Shen, K.-Y.; Farooq, S.F.S.; Fan, Y.; Nguyen, K.M.; Wang, Q.; Elshazly, A.; Kurd, N. A 0.17-to-3.5 mW 0.15-to-5 GHz SoC PLL with 15 dB built-in supply noise rejection and self-bandwidth control in 14 nm CMOS. In Proceedings of the 2016 IEEE International Solid State Circuits Conference, San Francisco, CA, USA, 1–4 February 2016; pp. 330–331.
14. Jung, W.J.; Choi, H.C.; Jeong, C.; Kim, K.; Kim, W.; Jeon, H.; Koo, G.; Kim, J.; Seo, J.; Ko, M.; et al. A 1.2 mW 0.02 mm^2 2 GHz Current-Controlled PLL Based on a Self-Biased Voltage-to-Current Converter. In Proceedings of the 2007 IEEE International Solid State Circuits Conference, San Francisco, CA, USA, 11–15 February 2007; pp. 310–605.
15. Zhang, H.; Du, X.; Zhang, Y.; Gong, L.; Cheng, J. A low-jitter third-order self-biased PLL with adaptive fast-locking scheme for SerDes interfaces. *Analog Integr. Circ. Sig. Process* **2015**, *85*, 311–321. [CrossRef]
16. Broenlee, M.; Hanumolu, P.K.; Mayaram, K.; Moon, U.-K. A 0.5-GHz to 2.5-GHz PLL With Fully Differential Supply Regulated Tuning. *IEEE J. Solid State Circuits* **2006**, *41*, 2720–2728. [CrossRef]
17. Caram, J.P.; Galloway, J.; Kenney, J.S. Voltage-Controlled Ring Oscillator with FOM Improvement by Inductive Loading. *IEEE Microw. Wirel. Compon. Lett.* **2019**, *29*, 122–124. [CrossRef]
18. Zhao, Z.; Liu, L.; Feng, P.; Liu, J.; Wu, N. Compact 0.3-to-1.125 GHz self-biased phase-locked loop for system-on-chip clock generation in 0.18 um CMOS. *Jpn. J. Appl. Phys.* **2016**, *55*, 04EF05.
19. Jia, H.L.; Chen, X.M.; Liu, Q.; Feng, G.T. A self-biased PLL with low power and compact area. *J. Semicond.* **2015**, *36*, 132–136. [CrossRef]
20. Young, I.A.; Greason, J.K.; Wong, K.L. A PLL clock generator with 5 to 110 MHz of lock range for microprocessors. *IEEE J. Solid State Circuits* **1992**, *27*, 1599–1607. [CrossRef]
21. Boerstler, D.W. A low-jitter PLL clock generator for microprocessors with lock range of 340–612 MHz. *IEEE J. Solid State Circuits* **1999**, *34*, 513–519. [CrossRef]