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High-Performance Double-Node-Upset-Tolerant and Triple-Node-Upset-Tolerant Latch Designs

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Abstract: To avoid soft errors in integrated circuits, this paper presents two high-performance latch designs, namely LOCDNUTRL and LOCTNUTRL, protecting against double-node upset (DNU) and triple-node upset (TNU) in the harsh radiation environment. First, the LOCDNUTRL latch consists of two single-node upset (SNU) self-recovery modules and uses a C-element at the output. Next, based on the LOCDNUTRL latch, the LOCTNUTRL latch is proposed, which uses five extra inverters to fully tolerate TNU. Unlike the LOCDNUTRL latch, which uses an output level C-element as a voter, LOCTNUTRL is insensitive to the high-impedance state (HIS), making it more reliable for aerospace applications. The HSPICE simulation results, using a predictive technology model, show that the LOCTNUTRL latch saves 57.74% delay, 7.7% power consumption, 11.74% area cost, and 63.59% power delay production (PDP) on average compared with the state-of-the-art hardened latches. The process, voltage, and temperature variation analysis show that the proposed two latches are less sensitive to changes.

Keywords: soft errors; triple-node upsets; self-recoverable; c-element; clock gating; fast path

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1. Introduction

Voltage scaling in the integrated circuits (ICs) leads to improved IC energy efficiency [1]. With the reduction in the process size, the supply voltage and node capacitance of ICs decreased in some applications, such as biomedicine, sensors, and aerospace devices. Therefore, the energy efficiency of the circuit has improved [2]. However, when high-energy particles hit sensitive nodes in a circuit, the circuit is vulnerable to soft errors, since the amount of charge required for node turnover is small [3,4]. Terrestrial soft errors in electronic circuits are caused by either alpha particles originated from packaging or neutron particles from cosmic rays. On the other hand, heavy ions, protons, and electrons mainly cause soft error in space. When a high-energy particle strikes a sensitive region of a transistor and creates an electron–hole pair (EHP), a soft error occurs [5]. Recently, based on the radiation-hardening technology, many circuit structures for SNU [6,7] and DNU [8–10] hardening have been proposed. These design methods use interlocked holding nodes and spatial redundancy to block the wrong logic value to the output. In a harsh radiation environment, multi-node upset, especially a triple-node upset (TNU), induced by multi-node charge sharing is becoming more and more prominent, resulting in an increasing soft error rate [11,12]. However, these existing latches still have the following issues. Most of the hardened latches still suffer from a large silicon area and power consumption, and few of them can be effectively hardened to TNUs. What is more serious is that when some latches tolerate soft errors, the output generates an HIS. Therefore, the existing latches do not have enough radiation-hardening capability and can hardly be applied to high-reliability circuit systems in aerospace.

Based on the radiation hardening by design (RHBD) approach, this paper firstly proposed a LOw-Cost DNU ToleRant Latch (LOCDNUTRL). The latch is composed of two SNU self-recovery modules to tolerate a DNU from the wrong logic value caused by high-energy particle impact in the circuit. In order to reduce the delay of the LOCDNUTRL and improve its robustness, a LOw-Cost TNU-ToleRant Latch (LOCTNUTRL) is proposed. The proposed LOCTNUTRL latch is more suitable for the low power consumption characteristics of special environmental requirements. Compared with the previously proposed latches, the LOCTNUTRL proposed in this paper reduces the delay by 57.74%, the power consumption is reduced by 7.7%, the area overhead is reduced by 11.74%, and the PDP is reduced by 63.59%. In addition, process, voltage, and temperature (PVT) variation analysis shows that our LOCTNUTRL latch is more stable than other latches.

The rest of the paper is organized as follows. Section 2 reviews previous hardened latch structures. Section 3 describes the implementation, normal working principles, and fault toleration verifications for the proposed latch design. Section 4 provides the comparison and evaluation results of overhead and presents a comparison between the latches proposed in this article and the previously hardened latches under PVT variations. Section 5 concludes the paper.

2. Previous Hardened Structures

The circuit structure of the C-element is shown in Figure 1. Figure 1a shows the traditional two-input C-element circuit structure. The logic values of the two inputs are the same, and the logic values of the output are the opposite. The C-element consists of two p-type MOS (PMOS) transistors denoted as P1 and P2, and two n-type MOS (NMOS) transistors denoted as N1 and N2. By adding two clock-controlled transistors to the structure presented in Figure 1a, the C-element's power consumption and transmission delay can be greatly reduced, as shown in Figure 1b.

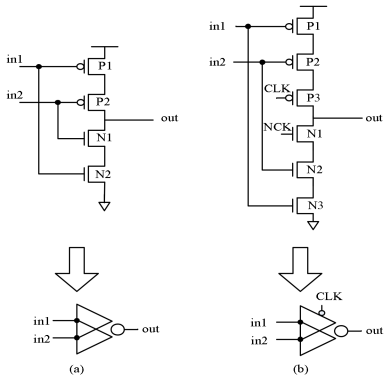

Figure 1. The circuit structure of the C-element: (**a**) traditional two-input C-element; (**b**) clock-controlled two-input C-element.

2.1. SNU-Tolerant Latches

The FERST latch [13] is shown in Figure 2a, and it consists of four transmission gates, two inverters, three two-input C-elements, and a weak keeper. The FERST latch uses an inverter and a C-element to construct a robust feedback loop to store data. At the same time, the FERST can tolerate an SNU regardless of which node is impacted by energetic particles. However, the latch cannot tolerate DNU because if the data that remain in the two feedback loops are flipped, the latch will propagate incorrect logical values.

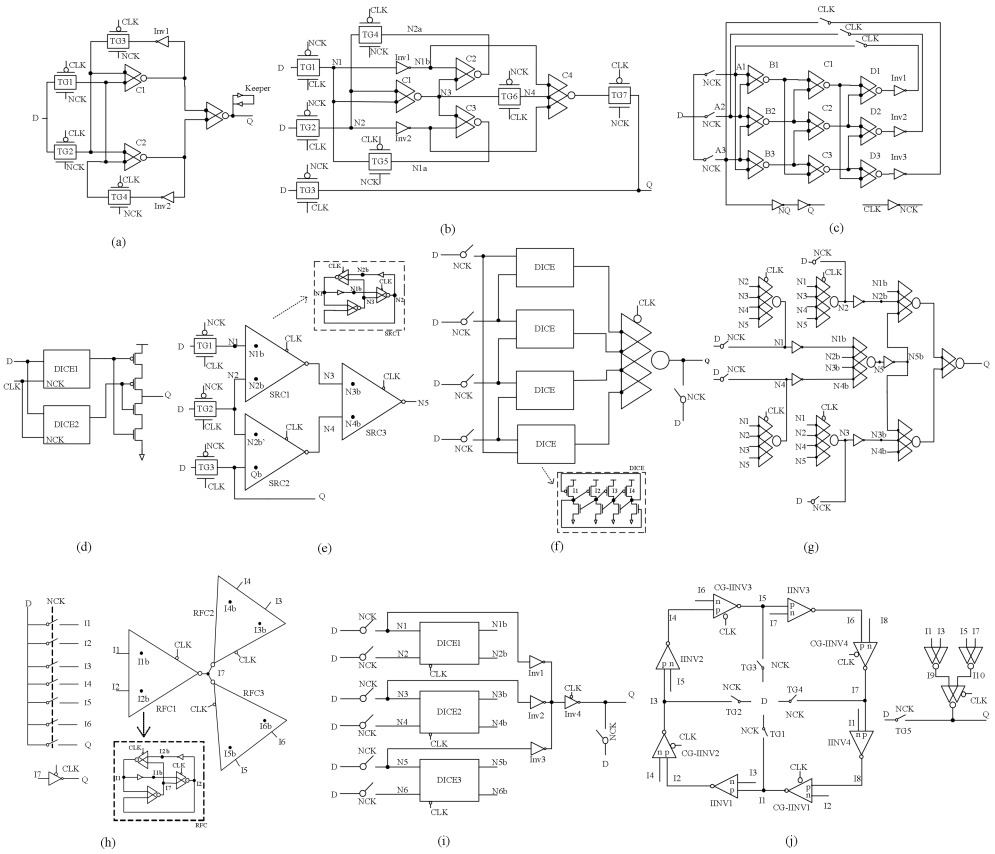

Figure 2. The existing hardened structure designs: (**a**) FERST [13]; (**b**) HLDTL [14]; (**c**) NTHLTCH [15]; (**d**) DNCS-SEU [16]; (**e**) DNURL [17]; (**f**) DICE4TNU [18]; (**g**) TNUHL [19]; (**h**) SMNUT [20]; (**i**) TMHIMNT [21]; (**j**) LCTNUT [22].

The HLDTL latch [14] is shown in Figure 2b. This latch consists of an SNU self-recovery cell and a three-input C-element. The SNU self-recovery cell consists of three two-input C-elements and two inverters. However, this latch does not fully tolerate DNUs.

2.2. DNU-Tolerant Latches

The NTHLTCH latch [15] is shown in Figure 2c, where it can be seen that it uses nine C-elements, three transmission gates, and three inverters to construct a triple-interlocked feedback loop. The NTHLTCH tolerates not only SNUs but also DNUs. Since the latch consists of multiple C-elements, transmission gates, and inverters, reliable data retention can be ensured, but large latency and area overhead can be caused.

The DNCS-SEU latch [16] is composed of two clock-controlled DICE units and a two-input C-element, as shown in Figure 2d. The DICE unit can provide a single-node upset self-recovery ability, and the latch can tolerate DNU. However, the latch may produce an HIS when fault-tolerant, so the DNCS-SEU involves a higher delay, and the latch cannot tolerate the TNU.

The DNURL latch [17] consists of three transmission gates and three interlocked single-node upset self-recovery units, as shown in Figure 2e. Each single-node upset self-recovery unit consists of two clocked two-input C-elements, one two-input C-element, and two inverters. Single-node upset self-recovery units are connected to achieve DNU tolerance, but DNURL cannot tolerate TNU.

2.3. TNU-Tolerant Latches

The DICE4TNU [18] latch includes four interlocked DICE units and uses a four-input clock-controlled C-element to tolerate the TNU, as shown in Figure 2f. In the worst case, the

DICE unit cannot recover itself from the DNU, which will cause the input of the C-element to be different; i.e., the output will further result in an HIS. The area overhead of the latch is too large, the delay and power consumption are relatively high, and this latch is not economical.

The TNUHL latch [19] uses five interlocked four-input C-elements to create feedback loops to preserve values, as shown in Figure 2g. This latch is based on multimode redundancy and double-level error interception (DLEI) to tolerate TNU. However, this latch has high latency and large area overhead. The SMNUT latch [20] consists of three SNU self-recovery cells (SRCs), each of which consists of three mutual-feedback two-input C-elements, as shown in Figure 2h. The C-elements have a common convergent output node that feeds back a signal to the output of the latch, enabling the latch to tolerate TNUs. However, this structure has a large area overhead.

The TMHIMNT latch [21] consists of three clock-controlled DICE units, seven transmission gates, three inverters, and one clock-controlled inverter, as shown in Figure 2i. At the output end, the current competition is used to avoid the HIS generated when the C-element is used to tolerate fault. The number of TMHIMNT transistors is relatively large, so the delay and power consumption of the latch are relatively high.

The LCTNUT latch [22] is composed of four input-split inverters and four input-split clocked inverters. Three two-input C-elements are added to the output to prevent the propagation of soft errors, as shown in Figure 2j. Although the delay and power consumption of the latch is relatively low, an HIS may generate when the latch tolerates fault at the output end.

3. Proposed Hardened Htructure

3.1. Circuit Structure and Behavior

The structure of the proposed LOCDNUTRL latch is presented in Figure 3. The proposed latch consists of two SNU self-recovery cells denoted as SRC1 and SRC2, an inverter denoted as Inv1, two transmission gates (TG1 and TG2), and a three-input C-element. In Figure 3, CLK and NCK represent the system clock and negative system clock, respectively. The self-recovery cells have the pull-up and pull-down capabilities due to MOS transistors, so they can tolerate the wrong logical values caused by particle bombardment and can recover themselves quickly.

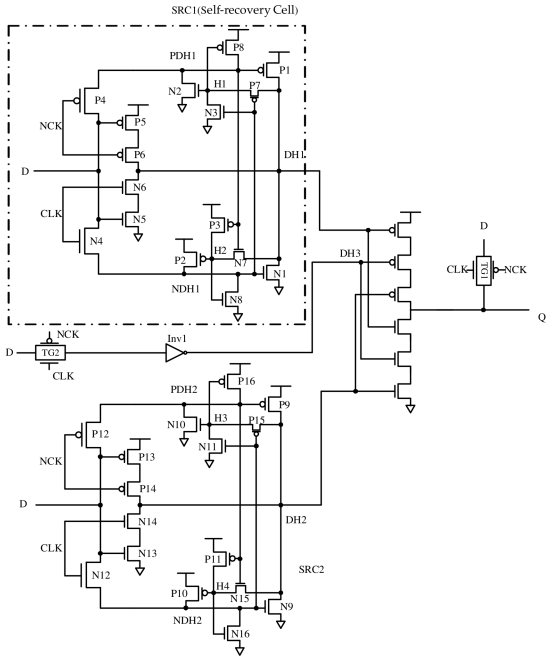

Figure 3. Proposed LOCDNUTRL structure design.

In SRC1 of Figure 3, PDH1, NDH1, and DH1 denote sensitive nodes. Depending on the logical values stored in PDH1 and NDH1, nodes in the input D-driven storage module have the same logical values as the input when the clock CLK is high and NCK is low, while DH1 has the opposite logic value. In contrast, when the clock CLK is low and NCK is high, the LOCDNUTRL is in the latch mode. Assuming that input D is zero, PDH1 (PDH2) and NDH1 (NDH2) are also zero, and DH1 (DH2) is one. Take the SRC1 unit as an example; it is known that when PDH1 is zero, P3 opens, and H2 is pulled up to one; then, N8 is opened and grounded, and the NDH1 value is maintained. Similarly, NDH1 is zero, P7 is passed through, and DH1 is one. Thus, N2 is always grounded when turned on, the logical value of PDH1 is maintained to zero, and P1 is always turned on to pull up DH1. To ensure better application to the system-on-chips (SoCs), a single-sided hybrid PMOS and NMOS reinforcement unit design is adopted, which reduces the time of SNU self-recovery and stores logical values for a longer time [23], thus increasing the fast path from input D to output Q and greatly reducing the transmission delay of the circuit. The simulation results for the normal working principle of the LOCDNUTRL latch are presented in Figure 4, where it can be seen that the latch can operate correctly.

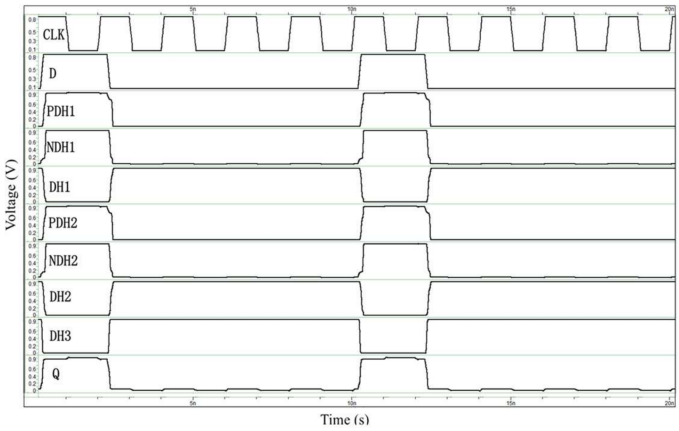

Figure 4. Simulation results for the normal operation of the LOCDNUTRL latch.

3.2. SNU-Tolerance Feature

Due to the symmetry of the proposed structure, only SRC1 elements will be described in detail. Assuming that the latch stores logical values of zero; then, PDH1 and NDH1 store zeros, and DH1 stores a logical value of one. When NDH1 is flipped from zero to one by particle bombardment, DH1 becomes unstable due to the switching on of transistor N1, but at this point, DH1 is still maintained by parasitic capacitance, and transistor N8 is conductive, so N8 lowers NDH1 to a low level, and NDH1 restores the correct logical value. When PDH1 is bombarded by particles from zero to one, DH1 becomes unstable due to the closing of P1. Since DH1 is still maintained by parasitic capacitance, transistor N2 turns on and lowers PDH1 to the low level, so PDH1 can restore the correct logic value. When DH1 is flipped from the logical value of one to zero, PDH1 and NDH1 are still at the value of zero, and PDH1 will float due to the closure of transistor N2, but PDH1 remains the value of zero by the parasitic capacitance, and P1 remains ON for a certain period. As a result, DH1 is pulled up to a high level, transistor N2 is turned on again, and the reinforcement unit is restored to the correct logical value. For sensitive node DH3, since the three-input C-element is used at the output to block the propagation of soft errors, the logic value of output Q is not affected.

3.3. DNU-Tolerance Feature

When a pair of sensitive nodes are bombarded by particle (s), there are three possible situations in the LOCDNUTRL. CASE D1: nodes bombarded by particles exist in different SRC modules; CASE D2: nodes bombarded by particles exist in SRC modules and DH3

modules; CASE D3: nodes bombarded by particles exist in one SRC module. These three cases are explained in the following in detail.

CASE D1: As mentioned above, the SRC module in the hardened circuit has the SNU self-recovery characteristic, so when a DNU occurs in the SRC1 and SRC2 modules, it can be considered as an SNU, so the output Q will not be affected.

CASE D2: When the DNU occurs in the SRC and DH3 modules simultaneously, due to the SNU SRC self-recovery feature, the incorrect logical value will be corrected quickly, and the output will not be affected due to the blocking effect of the three-input C-element on the output.

CASE D3: This is the worst case, in which the LOCDNUTRL latch is bombarded by particles. The SRC module cannot fully tolerate DNUs when sensitive node pairs (PDH1 and NDH1) are bombarded by particles. Assuming that SRC1 stores the logical value of zero; then, PDH1 and NDH1 are flipped from zero to one, P1 is turned off, N7 is turned on, and N1 is turned on, but DH1 can still be maintained due to parasitic capacitance, so the N8 conductor keeps pulling down NDH1, making NDH1 restore to zero, P7 open, and N2 turn on. By further pulling down, PDH1 restores to zero, and finally, conductor P1 pulls up DH1. When a particle bombards a sensitive node pair (PDH1, DH1) or (NDH1, DH1) of SRC1, the logical values in the node will flip regardless of the logical value the latch stores, and the output will not be affected. Thus, the LOCDNUTRL latch is completely tolerant of DNUs.

3.4. TNU-Tolerance Feature

Due to the symmetry of the structure, there are three following situations. CASE T1: node flipping occurs in two different SRC modules; CASE T2: node flipping occurs at the output end; CASE T3: node flipping occurs in one SRC module.

CASE T1: Based on the previous discussion, the proposed hardened latch is completely tolerant to DNU, so regardless of sensitive nodes where a three-node pair flip occurs, it can be transformed into an SNU plus a DNU problem, so output Q will not be affected.

CASE T2: When the three-node pair (DH1, DH2, DH3) flip occurs at the output, DH1 and DH2 can be recovered by SRC1 and SRC2, and DH3 will not be affected by the blocking effect of the C-element.

CASE T3: When a three-node pair occurs in an SRC module, the logical values of the sensitive nodes in SRC1 will be reversed, but the logical values of SRC2 and DH3 are still correct, so the output will remain the correct logical values. Therefore, the latch can tolerate TNU with the exception only of (PDH, DH, Q) and (NDH, DH, Q) when a large high-energy radiation particle bombards, since the invalid input and output of the three-input C-element are retained. In a word, the LOCDNUTRL latch is completely tolerant to DNU and also has a reinforcement effect for TNU.

In order to fully tolerate TNU and avoid HIS caused by error propagation, the LOCTNUTRL latch is proposed. Compared with the LOCDNUTRL latch, the LOCTNUTRL latch has lower transmission latency and power consumption, and although it increases the area overhead relatively, it is more robust against soft errors. The structure of the LOCTNUTRL is shown in Figure 5.

Five inverters (Inv2, Inv3, Inv4, Inv5, and Inv6) are added to make the logic values of the two SRC cells converge to M and prevent the propagation of soft errors through current competition. It abandons the use of the C-element at the output, improves the ability of the latch to tolerate soft errors at the output Q, avoids the high-impedance state caused by the difference between the two inputs of the C-element, reduces the power consumption and transmission delay, and also has relatively low area overhead that provides economic benefits.

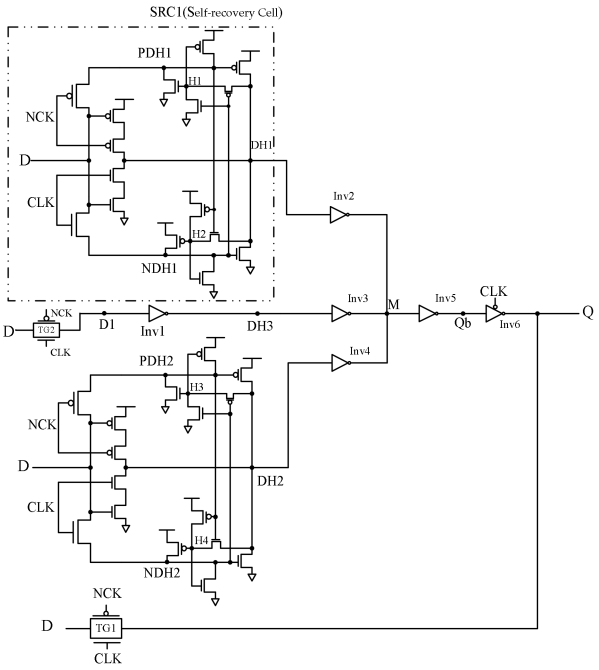

Figure 5. Proposed LOCTNUTRL structure design.

3.5. Simulation Results

The proposed structures were verified by simulations. In the simulations, the 32 nm predictive technology model (PTM) [24] was adopted, and the HSPICE simulation tool was used for the fault injection experiment. The power supply voltage was 0.9 V, the temperature was 27 °C, and the clock frequency was 500 MHz. In LOCDNUTRL, we set the aspect ratios to (W/L) p = 4 and (W/L) n = 2 for the C-element, and (W/L) p = 2 and (W/L) n = 1 for other PMOS and NMOS transistors. A flexible double-exponential current source model was used to perform all fault injections [25]. The equation of the model is shown in (1):

$$I_{inj}(t) = \frac{Q_{inj}}{\tau_1 - \tau_2}\left(e^{\frac{-t}{\tau_1}} - e^{\frac{-t}{\tau_2}}\right) \quad (1)$$

Q_{inj} denoted the amounts of induced charge at time t. τ_1 and τ_2 are the material-dependent time constants. In our simulations, the current source injection is 0.685 mA, and the duration is 1 ps.

As shown in Figure 6, soft error waveforms were injected into the following sensitive node pairs: (PDH1, PDH2), (NDH1, NDH2), (DH1, DH2), (PDH1, DH3), (NDH1, DH3), and (DH1, DH3). The tolerance of the proposed latch to the DNU was analyzed. As can be seen from the diagram in Figure 6, after particles had bombarded the sensitive node, the wrong logical values did not continue to propagate downward and could recover themselves quickly.

Figure 7 shows the results that were obtained when the soft errors were injected into sensitive node pairs (PDH1, NDH1), (PDH1, DH1), and (NDH1, DH1), when zero and one were stored in the latch, respectively. This is the case in which the latch tolerates two-node flipping presented in the section "DNU-TOLERANCE FEATURE". As shown in Figure 7, a sensitive node pair (PDH1, NDH1) stored the logical value of zero or one in the latch, and the fast self-recovery of the wrong logical value would not continue. However, pairs (PDH1, DH1) and (NDH1, DH1) in the SRC1 module stored incorrect logical values after the storage of zero or one was bombarded by particles. Still, due to the blocking effect of the output C-element, the Q point was not affected, and the logical values in the SRC module would resume in the next clock cycle. Then, the soft errors were injected into sensitive node pairs (PDH1, NDH1, DH2), (PDH2, NDH2, DH1), (DH1, DH2, DH3), and (PDH1, NDH1, DH1), and the obtained results are presented in Figure 8. It can be seen from Figure 8 that

the output Q can still maintain the correct logical value in the worst case, that is, when three sensitive nodes in one SRC1 are flipped at the same time, so the LOCDNUTRL presented in this paper is entirely tolerant to DNU but partially tolerant to TNU.

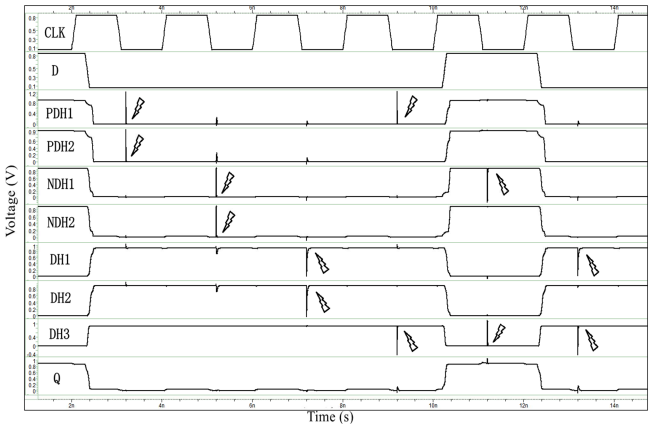

Figure 6. Simulation waveforms of the LOCDNUTRL when a particle strikes a node pair in terms of CASE D1 and CASE D2.

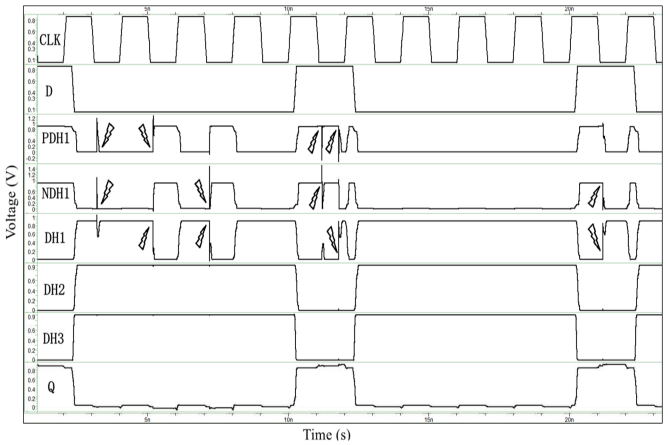

Figure 7. Simulation waveforms of the LOCDNUTRL when a particle strikes a node pair in terms of CASE D3.

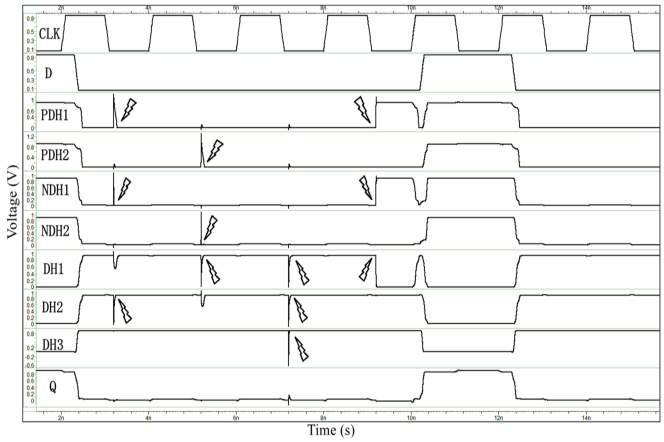

Figure 8. Simulation waveforms of the LOCDNUTRL considering particle impact on three node pairs.

Therefore, this paper improves the LOCDNUTRL and puts forward the LOCTNUTRL latch. During the LOCTNUTRL latching period, soft errors are injected into sensitive node pairs (DH2, PDH2, Q), (DH1, PDH1, Q), (DH1, PDH1, DH2), (DH2, PDH2, DH1), (DH1,

PDH1, NDH1), (DH1, DH2, DH3), (D1, Q), (D1, DH1, Q), and (D1, DH2, Q). Especially for node pairs (DH2, PDH2, Q) and (DH1, PDH1, Q), which are not fully hardened in LOCDNUTRL, it can be seen from Figure 9 that the logic values of output errors are corrected quickly and do not continue to propagate. In addition, a double-node upset was injected at nodes (D1, Q) and two triple-node upsets were injected at nodes (DH1, D1, Q) and (DH2, D1, Q) in the simulation in hold mode for the LOCTNUTRL; the output Q can be recovered quickly.

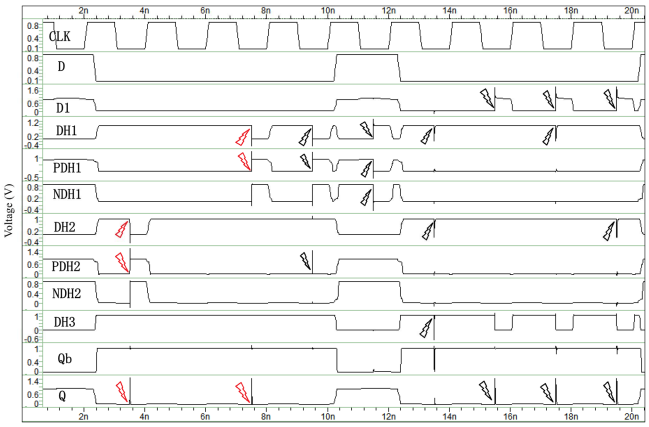

Figure 9. Simulation waveforms of the LOCTNUTRL considering particle impact on sensitive nodes.

4. Comparison and Evaluation Results

4.1. Performance Evaluation

The comparison of the reinforcement ability of different latches is presented in Table 1. The quantitative comparison of the delay, power consumption, transistor number, and PDP is also provided. The simulation was carried out under 32 nm PTM. In Table 1, the delay represents the transmission delay from D to Q, that is, the average value of the rising delay and falling delay from D to Q. The power denotes the average power consumption [26]. In this study, unit size transistors (USTs) [27] were used to measure the area overhead. The PDP in Table 1 was calculated as (2):

$$\text{PDP} = \text{Power} \times \text{Delay}. \tag{2}$$

Table 1. Comparison of parameters between the proposed latch and the existing latches.

Latch	Delay/ps	Power/μW	Area (UST)	$10^{-18} \times$ PDP
FERST [13]	86.54	0.25	26	21.63
HLDTL [14]	16.83	0.72	36	12.11
NTHLTCH [15]	65.06	5.81	54	377.99
DNURL [17]	23.97	0.42	66	10.07
DICE4TNU [18]	25.76	5.62	54	144.77
TNUHL [19]	117.2	1.83	78	214.48
SMNUT [20]	40.92	1.46	71	59.74
TMHIMNT [21]	32.41	3.11	53	100.79
LCTNUT [22]	24.27	0.49	53	11.89
LOCDNUTRL	29.3	1.23	44	36.03
LOCTNUTRL	14.23	1.21	50	17.22

As shown in Table 1, the first two latches could tolerate only the SNU but could not tolerate the DNU, which led to the incompatibility between the first two designs. In addition, although the DNU could be fully tolerated by the structures [15] and [17], the TNU could not be tolerated compared with the latch proposed in this paper, and the structures had a large delay and power consumption overhead. As shown in Table 1, the LOCTNUTRL latch has a larger transistor number but a lower delay than the LOCDNUTRL

latch. Since the LOCDNUTRL latch uses the C-element as the voter, there is a current competition at the output. However, the LOCTNUTRL latch uses the clock-controlled inverter, Inv6, at the output. Hence, during the transparent period, Inv6 is closed, and the signal is directly transmitted from D to Q through the transmission gate TG1 without current competition, which significantly reduces the transmission delay. Compared with the other structures regarding the TNU-tolerance ability, the LOCTNUTRL latch had less delay and power consumption, the lowest area cost, and a smaller PDP.

The reduction in the percentage of the LOCTNUTRL latch in comparison to the other TNU-tolerant latches regarding the parameters given in Table 1 was calculated by (3), and the numerical values are presented in Table 2 where "Δ" is the factor used for showing the percentage change.

Table 2. The percentage reduction of the LOCTNUTRL latch cost compared with other latches.

Latch	ΔDelay (%)	ΔPower (%)	ΔArea (%)	ΔPDP (%)
DICE4TNU [18]	−44.76	−78.46	−7.4	−88.10
TNUHL [19]	−87.58	−33.88	−35.89	−91.97
SMNUT [20]	−65.22	−17.12	−29.58	−71.18
TMHIMNT [21]	−6.09	−61.09	−5.6	−82.91
LCTNUT [22]	−41.37	145.93	−5.6	44.82
LOCDNUTRL	−51.43	−1.62	13.63	−52.21
Average	−57.74	−7.7	−11.74	−63.59

As shown in Table 2, the LOCTNUTRL latch achieved significant decreases in the delay, power consumption, and PDP, simulated under 32 nm PTM, compared to the other latches. Compared with the recently proposed TNU-tolerant latches, the LOCTNUTRL latch reduced delay by 57.74%, power consumption by 7.7%, area overhead by 11.74%, and PDP by 63.59% on average. The small delay of LOCTNUTRL means this latch is of high performance. The results prove that the proposed latch has great economic benefits compared to the existing TNU-tolerant latches.

$$\Delta = (\text{Proposed Latch} - \text{Compared Latch}) \ / \ \text{Compared Latch} \quad (3)$$

4.2. PVT Variation Analysis

With the continuous reduction in the process size, the influence of PVT variations on the reliability of nano-integrated circuits has become more severe. In order to ensure that the circuit can operate correctly within a certain PVT variation range, it is necessary to analyze and evaluate the circuit structure under the PVT. In this work, the changes in power consumption and delay of eight different latches and the proposed latches were evaluated under the influence of PVT variations. The HSPICE simulation tool was used to analyze the influence of the PVT variation on each latch in detail. The 32 nm PTM model was used in the simulation. For better visibility, we use the sample standard deviation as (4) to compare the power consumption and delay changes of several TNU-tolerant latches under PVT variations.

$$s = \sqrt{\frac{\sum_{i=1}^{n}(x_i - \overline{x})^2}{n - 1}} \quad (4)$$

where s is the sample standard deviation, x_i is the ith observation in the sample, $\overline{x}$ is the sample mean, and n is the number of observations in the sample.

There are five corners: FF (Fast NMOS Fast PMOS), FS (Fast NMOS Slow PMOS), TT (Typical NMOS Typical PMOS), SF (Slow NMOS Fast PMOS), and SS (Slow NMOS Slow PMOS) [24].

As shown in Figure 10a,b, the power change of the DICE4TNU was the largest for process variations. The sensitivity orders are (only aiming at TNU-tolerant latches): DICE4TNU > TNUHL > Proposed LOCTNUTRL > SMNUT > TMHIMNT > LCTNUT. As shown in Figure 10c,d, the delay of TMHIMNT is most sensitive to process variations.

The sensitivity orders are (only aiming at TNU-tolerant latches): TMHIMNT > LCTNUT > TNUHL > Proposed LOCTNUTRL > DICE4TNU > SMNUT. So, regarding process variations, our proposed latch is a little bit sensitive.

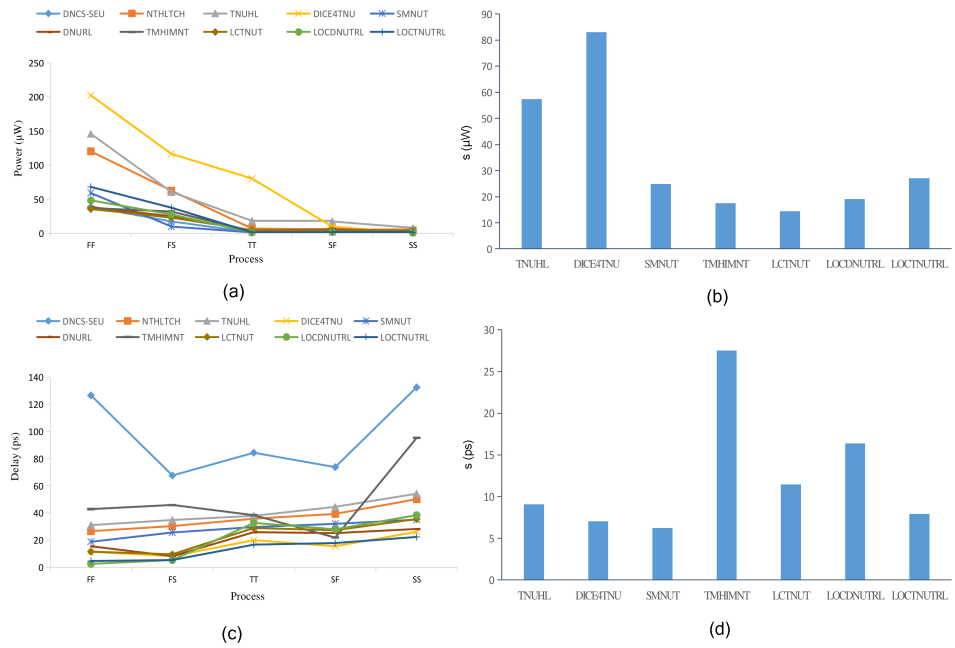

Figure 10. (**a**) Changes of power consumption of different latches under process variation; (**b**) sample standard deviation of (**a**) for TNU-tolerant latches; (**c**) changes of delay of different latches under process variation; (**d**) sample standard deviation of (**c**) for TNU-tolerant latches.

As shown in Figure 11a,b, the supply voltage is varied from 0.8 to 1.25 V. Under different operating voltages, compared with the same type latches, the power consumption of the proposed latch has less sensitivity to supply voltage, but it is worse than that of LCTNUT. The sensitivity orders are (only aiming at TNU-tolerant latches): DICE-4TNU > TMHIMNT > TNUHL > SMNUT > Proposed LOCTNUTRL > LCTNUT. As shown in Figure 11c,d, the delay reduces along with the supply voltage decreasing. The delay of the proposed latch has less sensitivity to supply voltage variation. The sensitivity orders are (only aiming at TNU-tolerant latches): TNUHL > TMHIMNT > SMNUT > LCTNUT > DICE4TNU > Proposed LOCTNUTRL. The power and delay of the LOCTNUTRL latch was less sensitive under the variation of the supply voltage.

As shown in Figure 12a,b, the temperature is varied from −25 to 65 °C. The LOCTNUTRL latch has a smaller power change compared with the other latches at different temperatures. The sensitivity orders are (only aiming at TNU-tolerant latches): DICE-4TNU > TNUHL > TMHIMNT > SMNUT > Proposed LOCTNUTRL > LCTNUT.

In terms of delay, we can see that the delay increases along with the rise of temperature. As shown in Figure 12c,d, when the temperature rises from 25 to 65 °C, the delay change of the TNUHL was the largest. The sensitivity orders are (only aiming at TNU-tolerant latches): TNUHL > SMNUT > LCTNUT > TMHIMNT > DICE4TNU > Proposed LOCTNUTRL. Based on the obtained results, the LOCTNUTRL latch maintained relatively stable delay and power consumption under temperature variations.

In summary, the proposed LOCTNUTRL latch is less sensitive to process, voltage, and temperature variations.

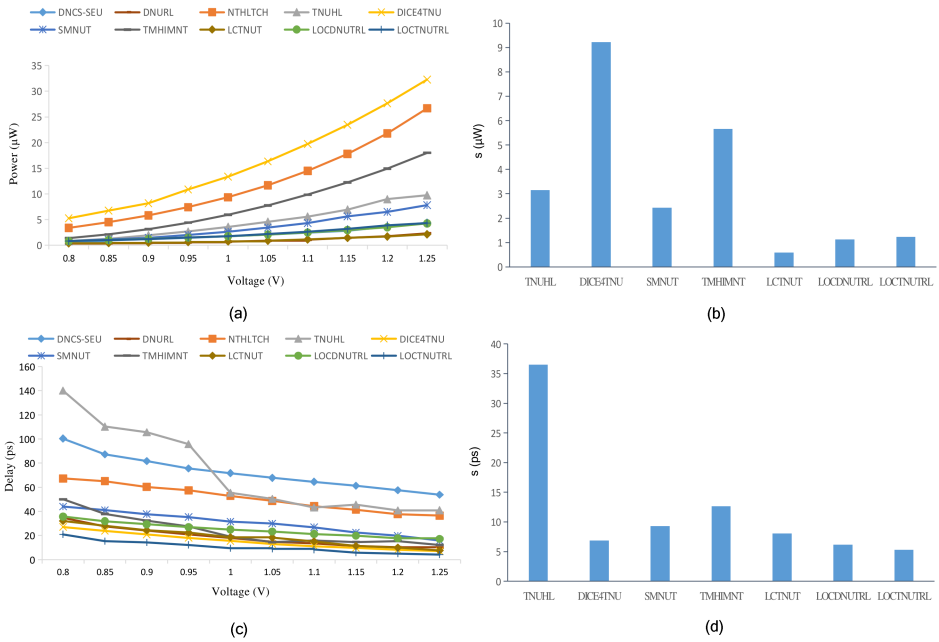

Figure 11. (**a**) Changes of power consumption of different latches under voltage variation; (**b**) sample standard deviation of (**a**) for TNU-tolerant latches; (**c**) changes of delay of different latches under voltage variation; (**d**) sample standard deviation of (**c**) for TNU-tolerant latches.

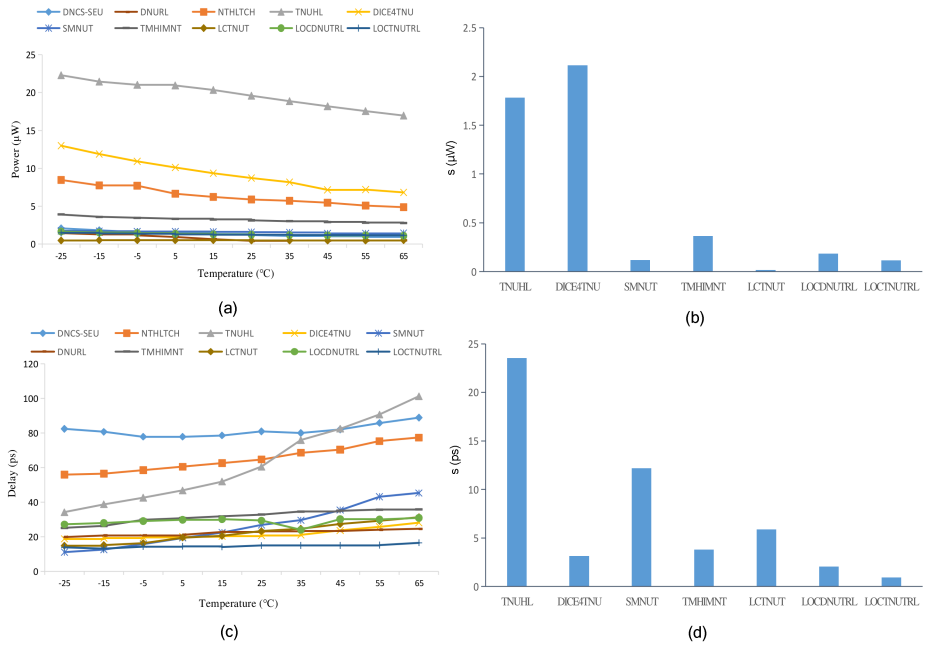

Figure 12. (**a**) Changes of power consumption of different latches under temperature variation; (**b**) sample standard deviation of (**a**) for TNU-tolerant latches; (**c**) changes of delay of different latches under temperature variation; (**d**) sample standard deviation of (**c**) for TNU-tolerant latches.

5. Conclusions

With the continuous size reduction in the CMOS technology, traditional sequential circuits have become more vulnerable to soft errors. Soft errors in sequential circuits are caused by the decreasing supply voltage and critical charge. In this paper, initially, a DNU-tolerant LOCDNUTRL latch with high reliability and low power consumption is proposed. The LOCDNUTRL latch is composed of two SNU self-recovery cells, which are composed of one-sided mixed PMOS and NMOS. The three-input C-element is added to block the soft

error at the output. Based on the LOCDNUTRL latch, the LOCTNUTRL latch is proposed. The LOCTNUTRL latch has lower power consumption and delay, because no C-element is used at the output, avoiding HIS. The analysis shows that these two latches are insensitive to the process, voltage, and temperature variations. The proposed latches can be effectively applied for safety-critical real-time applications, such as aerospace, nuclear plants, and biomedicine devices, where high reliability and performance is required.

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References

1. Markovic, D.; Wang, C.C.; Alarcon, L.P.; Liu, T.; Rabaey, J.M. Ultralow-Power Design in Near-Threshold Region. *Proc. IEEE* **2010**, *98*, 237–252. [CrossRef]
2. Kaul, H.; Anders, M.A.; Mathew, S.K.; Hsu, S.K.; Agarwal, A.; Krishnamurthy, R.K.; Borkar, S. A 320 mV 56 μW 411 GOPS/Watt Ultra-Low Voltage Motion Estimation Accelerator in 65 nm CMOS. *IEEE J. Solid-State Circuits* **2009**, *44*, 107–114. [CrossRef]
3. Anjan, S.; Baghini, M.S. Robust Soft Error Tolerant CMOS Latch Configurations. *IEEE Trans. Comput.* **2016**, *65*, 2820–2834. [CrossRef]
4. Baumann, R. Soft errors in advanced computer systems. *IEEE Des. Test. Comput.* **2005**, *22*, 258–266. [CrossRef]
5. Ferlet-Cavrois, V.; Massengill, L.W.; Gouker, P. Single Event Transients in Digital CMOS—A Review. *IEEE Trans. Nucl. Sci.* **2013**, *60*, 1767–1790. [CrossRef]
6. Xu, H.; Zhu, J.; Lu, X.; Li, J. An advanced SEU tolerant latch based on error detection. *J. Semicond.* **2018**, *39*, 055003. [CrossRef]
7. Kumar, C.I.; Bulusu, A. High performance energy efficient radiation hardened latch for low voltage applications. *Integration* **2019**, *66*, 119–127. [CrossRef]
8. Li, H.; Xiao, L.; Li, J.; Qi, C. High robust and cost effective double node upset tolerant latch design for nanoscale CMOS technology. *Microelectron. Reliab.* **2019**, *93*, 89–97. [CrossRef]
9. Yamamoto, Y.; Namba, K. Complete Double Node Upset Tolerant Latch Using C-Element. *IEICE Trans. Inf. Syst.* **2020**, *103*, 2125–2132. [CrossRef]
10. Xu, H.; Liu, X.; Yu, G.; Liang, H.; Huang, Z. LIHL: Design of a Novel Loop Interlocked Hardened Latch. *Electronics* **2021**, *10*, 2090. [CrossRef]
11. Alessio, M.D.; Ottavi, M.; Lombardi, F. Design of a Nanometric CMOS Memory Cell for Hardening to a Single Event with a Multiple-Node Upset. *IEEE Trans. Device Mater. Reliab.* **2014**, *14*, 127–132. [CrossRef]
12. Black, J.D.; Dodd, P.E.; Warren, K.M. Physics of Multiple-Node Charge Collection and Impacts on Single-Event Characterization and Soft Error Rate Prediction. *IEEE Trans. Nucl. Sci.* **2013**, *60*, 1836–1851. [CrossRef]
13. Fazeli, M.; Patooghy, A.; Miremadi, S.G.; Ejlali, A. Feedback Redundancy: A Power Efficient SEU-Tolerant Latch Design for Deep Sub-Micron Technologies. In Proceedings of the 37th Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN'07), Edinburgh, UK, 25–28 June 2007; pp. 276–285. [CrossRef]
14. Yan, A.; Huang, Z.; Yi, M.; Cui, J.; Liang, H. HLDTL: High-performance, low-cost, and double node upset tolerant latch design. In Proceedings of the 2017 IEEE 35th VLSI Test Symposium (VTS), Las Vegas, NA, USA, 9–12 April 2017; pp. 1–6. [CrossRef]
15. Li, Y.; Wang, H.; Yao, S.; Yan, X.; Gao, Z.; Xu, J. Double Node Upsets Hardened Latch Circuits. *J. Electron. Test.* **2015**, *31*, 537–548. [CrossRef]
16. Katsarou, K.; Tsiatouhas, Y. Double node charge sharing SEU tolerant latch design. In Proceedings of the 2014 IEEE 20th International On-Line Testing Symposium (IOLTS), Girona, Spain, 7–9 July 2014; pp. 122–127. [CrossRef]
17. Yan, A.; Huang, Z.; Yi, M.; Xu, X.; Ouyang, Y.; Liang, H. Double-Node-Upset-Resilient Latch Design for Nanoscale CMOS Technology. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2017**, *25*, 1978–1982. [CrossRef]
18. Lin, D.; Xu, Y.; Li, X.; Xie, X.; Jiang, J.; Ren, J.; Zhu, H.; Zhang, Z.; Zou, S. A novel self-recoverable and triple nodes upset resilience DICE latch. *IEICE Electron. Express* **2018**, *15*, 20180753. [CrossRef]
19. Watkins, A.; Tragoudas, S. Radiation Hardened Latch Designs for Double and Triple Node Upsets. *IEEE Trans. Emergy Top. Comput.* **2020**, *8*, 616–626. [CrossRef]
20. Song, Z.; Yan, A.; Cui, J.; Chen, Z.; Li, X.; Wen, X.; Lai, C.; Huang, Z.; Liang, H. A Novel Triple-Node-Upset-Tolerant CMOS Latch Design using Single-Node-Upset-Resilient Cells. In Proceedings of the 2019 IEEE International Test Conference in Asia (ITC-Asia), Tokyo, Japan, 3–5 September 2019; pp. 139–144. [CrossRef]

21. Yan, A.; Xu, Z.; Yang, K.; Cui, J.; Huang, Z.; Girard, P.; Wen, X. A Novel Low-Cost TMR-Without-Voter Based HIS-Insensitive and MNU-Tolerant Latch Design for Aerospace Applications. *IEEE Trans. Aerosp. Electron. Syst.* **2020**, *56*, 2666–2676. [CrossRef]
22. Yan, A.; Lai, C.; Zhang, Y.; Cui, J.; Huang, Z.; Song, J.; Guo, J.; Wen, X. Novel Low Cost, Double-and-Triple-Node-Upset-Tolerant Latch Designs for Nano-scale CMOS. *IEEE Trans. Emerg. Top. Comput.* **2021**, *9*, 520–533. [CrossRef]
23. Komatsu, Y.; Arima, Y.; Fujimoto, T.; Yamashita, T.; Ishibashi, K. A soft-error hardened latch scheme for SoC in a 90 nm technology and beyond. In Proceedings of the IEEE 2004 Custom Integrated Circuits Conference (IEEE Cat. No.04CH37571), Orlando, FL, USA, 6 October 2004; pp. 329–332. [CrossRef]
24. Predictive Technology Model (PTM) for SPICE. Available online: http://ptm.asu.edu/ (accessed on 14 October 2021).
25. Baumann, R.C. Radiation-induced soft errors in advanced semiconductor technologies. *IEEE Trans. Dev. Mater. Reliab.* **2005**, *5*, 305–316. [CrossRef]
26. Weste, N.H.E.; Harris, D.M. *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed.; Addison-Wesley: Boston, MA, USA, 2011.
27. Watkins, A.; Tragouodas, S. A Highly Robust Double Node Upset Tolerant latch. In Proceedings of the 2016 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), Storrs, CT, USA, 19–20 September 2016; pp. 15–20. [CrossRef]