

Article

A SPICE Model for IGBTs and Power MOSFETs Focusing on EMI/EMC in High-Voltage Systems

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Abstract: We describe two models of Power Transistors (IGBT, MOSFET); both were successfully used for the analysis of electromagnetic interference (EMI) and electromagnetic compatibility (EMC) while modeling high-voltage systems (PFC, DC/DC, inverter, etc.). The first semi-mathematical-behavioral insulated-gate bipolar transistor (IGBT) model introduces nonlinear negative feedback generated in the semiconductor's p+ and n+ layers, which are located near the metal contact of the IGBT emitter, to better describe the dynamic characteristics of the transistor. A simplified model of the metal-oxide-semiconductor field-effect transistor (MOSFET) in the IGBT is used to simplify this IGBT model. The second simpler behavioral model could be used to model both IGBTs and MOSFETs. Model parameters are obtained from datasheets and then adjusted using results from a single measurement test. Modeling results are compared with measured turn-on and turn-off waveforms for different types of IGBTs. To check the validation of the models, a brushless DC electric motor test setup with an inverter was created. Despite the simplicity of the presented models, a comparison of model predictions with hardware measurements revealed that the model accurately forecasted switch transients and aided EMI-EMC investigations.

Keywords: electric/hybrid vehicle; EMC simulations; IGBT; MOSFET SPICE models



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1. Introduction

Power transistors are the main source of electromagnetic interference (EMI) and electromagnetic compatibility (EMC) problems in power devices. In the modern metal-oxide-semiconductor field-effect transistor (MOSFET) and insulated-gate bipolar transistor (IGBT), switching times range from 30 to 200 ns, and switching currents may exceed 2000 A with high voltage (>4500 V). To simulate power devices from an EMI-EMC standpoint, focus should be on the noise generation mechanisms inside transistors.

Much research has been devoted to power transistor modeling. For example, “A Review of IGBT Models” [1] reviews transistor models in the literature before the year 2000, analyzing, comparing, and classifying them by type of mathematics, objectives, complexity, accuracy, and speed. We focus on IGBT models consisting of MOSFET and PNP transistors. Physics-based analytical models are represented in articles by A.R. Hefner [2–5], D.S. Kuo [6,7], R.J. McDonald [8] (whose works provided the fundamentals for the IGBT basic model in Simulation Program with Integrated Circuit Emphasis (SPICE) simulators), B.J. Baliga [9], G.M. Strollo [10], F. Mihalic [11], Han-Soo Kim [12], Ying-Yu Tzou [13], Z. Shen [14], J.T. Hsu [15], S. Musumeci [16], J.L. Tichenor [17], A. Tone [18], and Jinlei Meng [19]. In reviewing the models, we found that those based on the ambipolar diffusion equation [2–10] are characterized by high accuracy and that convergence problems are seldom revealed after model refinement. Parameters required to build a model are difficult to obtain [10,11,14], and even if all parameters are present, substantial time and qualified personnel are required to assemble the model.

Factory SPICE models are mainly based on the above method. However, due to their complex modeling systems, when several models of transistors are required simultaneously, the modeling time increases when factory models are used, which can lead to frequent convergence problems [10,14]. In reviewing the simpler models, which mainly use the behavioral modeling principle based on semiconductor devices physics [11–19], we found that the most of these models are optimized for certain situations. It remains unclear how to get these models and optimize their parameters.

In this paper, we present a methodology for the generation and usage of EMI–EMC applications in two variants of power transistor models optimized for simulations of power devices:

- (1) A model accurately describing the operation of an IGBT that is as simple and universal as possible; and
- (2) A simple model illustrating only the basic parameters of transistors but capable of modeling EMC–EMI problems.

An important requirement is that the models do not create or complicate convergence problems during calculations. The first model is a combination of semi-mathematical and behavioral models based on the physics of semiconductor devices. While working on the model, we observed that impedance of the p+ and n+ layers located near the emitter influenced the transistor parameters. A novelty of this model is the addition of nonlinear, current-dependent resistance near the emitter, which increases the accuracy of the model in static and dynamic modes. The creation of this model requires complicated procedures. The first model is useful for capturing the fine effects caused by the interaction of the transistor's nonlinear parasitic capacities with the outer circle.

The second model is a behavioral model requiring only seven parameters for proper operation. These parameters are obtained from the transistor datasheet. As practical experience has shown, the second model is sufficient in most EMI/EMC applications and gives good results.

The rest of the paper is structured as follows. The methodology underlying the first complex modeling of an IGBT is presented in Section 2. Section 3 describes the measurement procedure required for model validation. Section 4 discusses the creation of simple IGBT and MOSFET models. Section 5 reviews the calculations times. In Section 6, we present an experimental setup of a brushless DC motor with an inverter and modeling of this setup. Section 7 concludes.

2. Methodology

Our methodology consists of the following steps:

- Construction of a simulation model for an IGBT for SPICE using the initial parameter values obtained from datasheets;
- Construction of a test bench for the IGBT;
- Measurements of input and output voltages;
- Construction of a simulation model of the test bench;
- Simulation of input and output voltages and adjustment of the IGBT parameters to fit the measurement results;
- Testing of the IGBT models for different levels of controlling signals;
- Testing of the IGBT models in the presence of different loads.

2.1. Equivalent Circuit Model of an IGBT

General circuit models of IGBTs consist of a combination of MOS and PNP bipolar junction transistors (Figure 1a). The nonlinear input capacity and feedback capacity of the MOSFET are modeled with three capacitors, C1, C2, and C3 (Figure 1b).

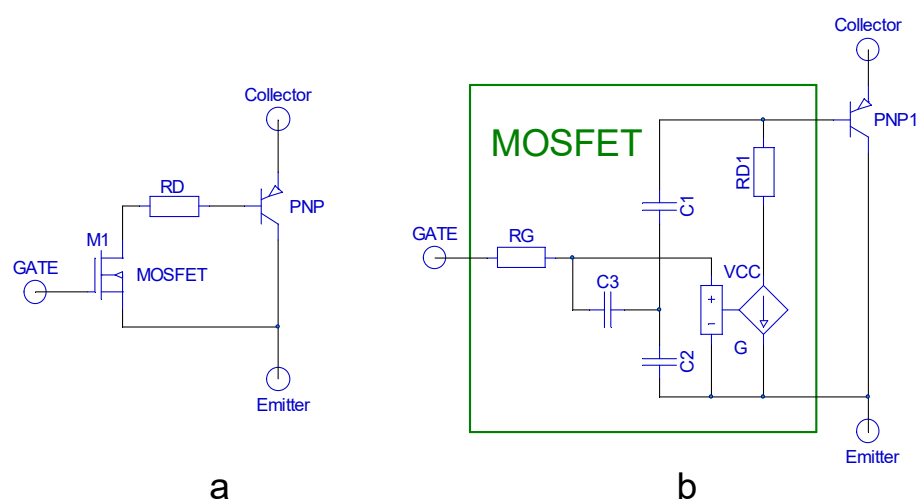


Figure 1. General circuit models of the IGBT showing the (a) MOS (metal–oxide–semiconductor) and PNP bipolar junction transistor and (b) three capacitors, C1, C2, and C3.

In the first model, we used three diodes (D1, D2, and D3) to describe them (Figure 2). For the MOS transistor M1, which is included in the IGBT (Figure 1) circuit, we replaced the voltage-controlled current source G1 (Figure 2). The formulas used in our model accurately describe the law of change in the capacity of the p–n junction, according to the voltage across the p–n junction.

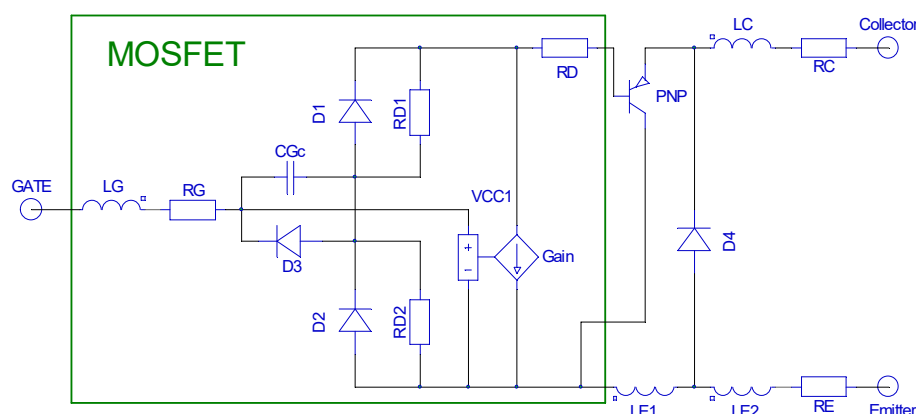


Figure 2. Equivalent circuit model of the IGBT (Insulated Gate Bipolar Transistor).

Diodes D1 and D2 describe the current change directly in the p–n junctions, and diode D3 describes the change in capacitance caused by a change in the excitation of the adjacent semiconductor layers of the gate. Since the gate is placed in a SiO₂ (dielectric) environment, its magnitude should not change. However, as shown in Figure 3, where the topological structure of the IGBT transistor is given, the total gate capacitance consists of a constant component (gate capacitance to the emitter metal CGc Figure 2) and a variable part (D3 describes this capacitance) that is created when the gate interacts with a semiconductor structure (n+, p–, n–, p–, n+). The conductivity of these layers varies from almost fully insulated to fully conductive.

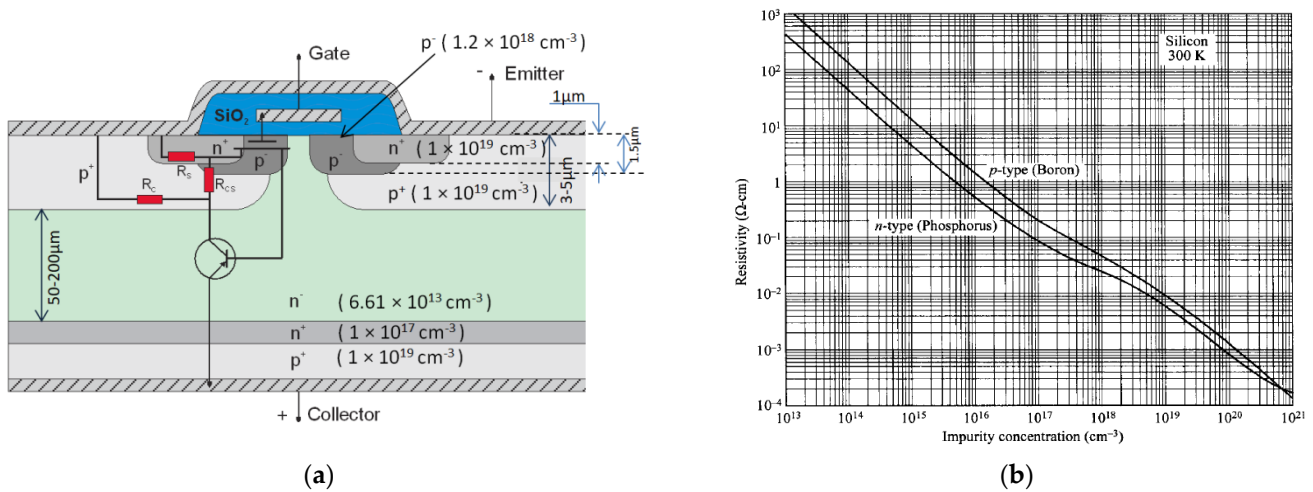


Figure 3. Diagram of IGBT cell (a) and resistivity vs. impurity concentration at 300 K for silicon (b) from [20].

It is likely that the law of change of such additional capacity differs from the law of change of the capacity of the diode, although our results show that such an assumption gives a fairly accurate result. Note that in all variants of SPICE, the diode is described in the same way. Thus, if we enter $IBV = 0$, $IBVL = 0$, $IS = 0$, and $ISR = 0$ in the model, the power goes out and only capacity works, according to the PSpice reference guide [21].

$$C_j = \begin{cases} C_{j0} \cdot \left(1 - \frac{V}{V_j}\right)^{-M}; & V \leq F_c \cdot V_j \\ C_{j0} \cdot (1 - F_c)^{-(1+M)} \times \left(1 - F_c \cdot (1 + M) + M \frac{V}{V_j}\right); & V > F_c \cdot V_j. \end{cases} \quad (1)$$

Here, V_j is the threshold potential; V is the voltage across the p–n junction; and C_{j0} is the threshold capacity when $V = 0$. M and F_c define the nonlinearity parameters.

Diodes D3 and D2 are respectively connected in parallel with resistors RD3 and RD2. These resistors create an additional initial constant bias voltage, which is necessary for the correct starting values of the diode capacities and to maintain a non-zero value of the current in the external circuit to improve convergence. The values of these resistors should be selected so that they do not affect the basic parameters of the transistor. The gain coefficients of voltage-controlled voltage sources are calculated as follows:

$$Gain = \begin{cases} \alpha \cdot (V_G - V_{th}) \cdot \left(\beta - \exp\left(\gamma - \frac{V_{ds}}{V_G}\right)\right), & V_G > V_{th} \\ 0, & V_G \leq V_{th} \end{cases} \quad (2)$$

where V_G is the driving voltage, V_{th} is the threshold voltage, and α , β , and γ are coefficients. LG and RG indicate the connecting wire inductance and total resistance of the gate, respectively. Parasitic inductances and resistances of the emitter and collector are modeled by LE1, LE2, Lc, and RE. The p–n–p transistor model is taken from the SPICE standard table (MODEL QSUB PNP).

Our investigations demonstrated that the equivalent scheme presented in Figure 2 describes the cut-off and saturation states of the IGBT but is not accurate enough to describe the active linear states (see Section 3 for a detailed discussion on this issue). In our opinion, the reason for this is the nonlinear negative feedback generated by the volumetric resistances in the n+, p+, and n– layers near the emitter contact (Figure 3a).

The magnitudes of resistors Rs, Rc, and Rcs (Figures 3a and 4a) depend on the emitter current. As shown in Figure 4, they form a negative feedback loop. The value of these resistors can range from 0.01 to 1 Ohm when the transistor is locked (i.e., $V_G \leq V_{tr}$) and within 0.1 and 10 mOhms when the transistor is in active mode (i.e., $V_G \geq V_{tr}$) [20,22,23]. This is due to the high doping level of the emitter's n+ and p+ layers (Figure 3b) and therefore their low impedance of 1–10 mOhm/sm [20].

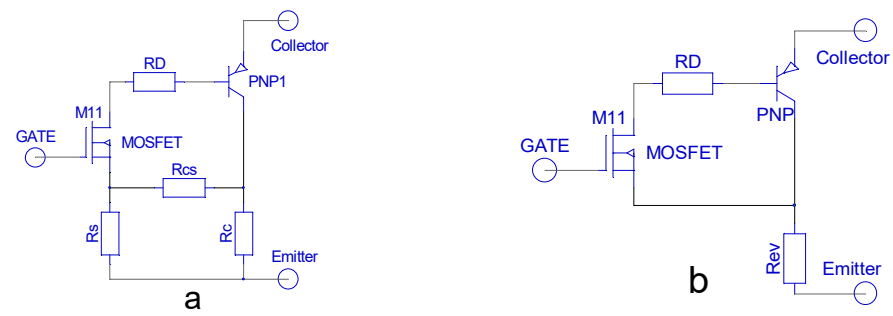


Figure 4. Updated general circuit of the IGBT negative feedback resistor connection schematic in the IGBT (a,b) simple versions of this connection.

Since they vary by one law according to the current (i.e., a good approximation can be described for a single resistor), it is possible to replace them with an equivalent single resistor (Figure 4b).

We can model this nonlinear impedance using a voltage-controlled current source G_r , as in Figure 5, with a transmission coefficient G_r as follows:

$$G_r = \frac{V_{R_2}}{[k + \exp(0.195/mV_{R_1})]} \quad (3)$$

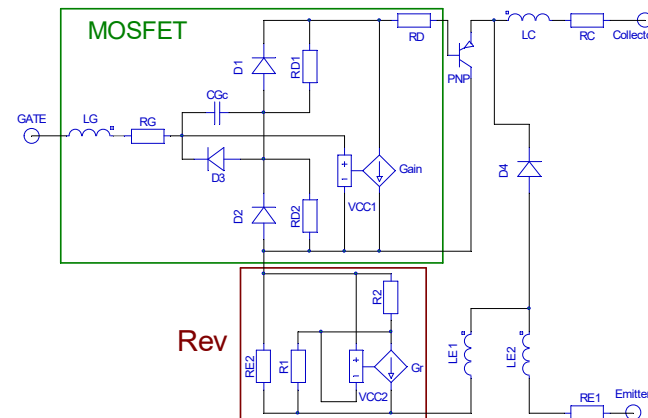


Figure 5. Equivalent circuit model of the IGBT.

The concentration of current carriers (electrons and holes) and current increase exponentially; hence, the volumetric impedance of the layers of the semiconductor structure of the transistor decreases by the same exponential law. The law of change of the Rev resistor (Figure 4b) also is exponential, as shown in Equation (3). RE2 determines the initial value of the nonlinear impedance; R1 and R2 comprise the current sensors (Figure 5).

Their values are specified in the modeling process by correlating them with the measurement results. The initial value can be selected according to the concentration of dopants in the IGBT emitter layers [20,22,23]. Their values range from R1 = 0.1–1 mΩ, R2 = 0.1–1 mΩ, and RE2 = 0.1–1 Ω. The new scheme in Figure 5 is more accurate than the one represented in Figure 2, as shown in Figures 10–12 in Section 3.

2.2. Procedure to Generate Parameters of the Equivalent Circuit Model of the IGBT

Our procedure for adjusting the parameter values is based on measurements. Test bench (Figure 6) and measurement procedure of IGBT characteristics is applicable to all transistor modules tested. The schematic of the test printed circuit board shown on Figure 7a. However, the design of each printed circuit board (Figures 7b and 11) depends on the transistor packaging and configuration of power and control terminals. The PCB layout is designed to reduce its influence on measured quantities as much as possible. The

two-layer PCB bottom is completely grounded. Copper bus bars in the bottom and top layers reduce ground resistance, which in turn reduces the voltage drop across the ground electrode and improves the measurement results.

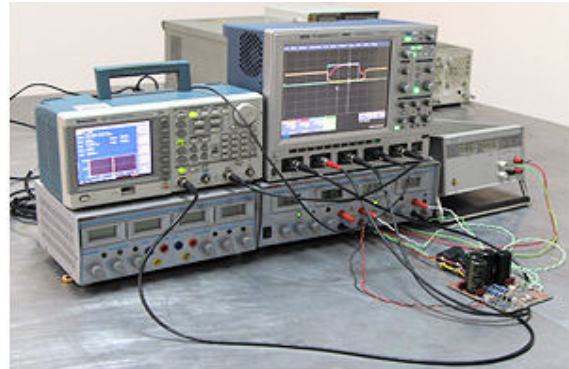
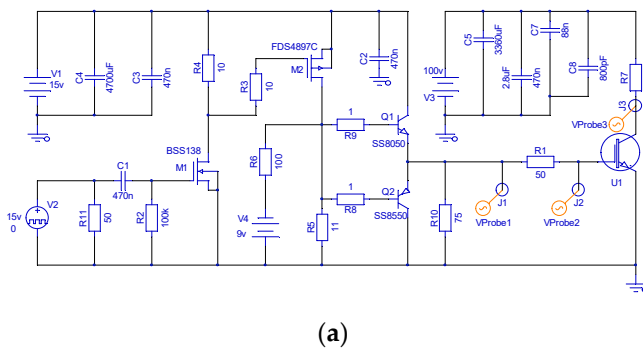
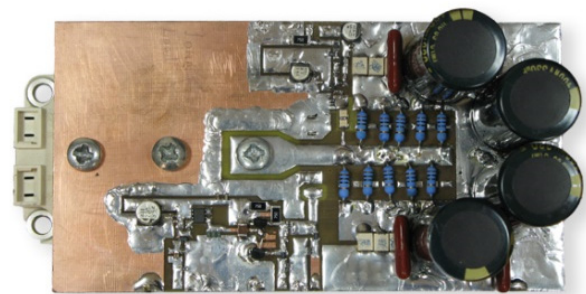


Figure 6. Measurement test-bench setup.



(a)



(b)

Figure 7. (a) Schematic of PCB for measuring IGBT characteristics, (b) test-bench PCB designed for SEMIKRON module SKM200GB123D.

Using a test bench (Figure 6), we measured voltage waveforms using an oscilloscope (Lecroy WaveRunner 04Xi 2 GHz 10 GS/s) at the collector (Figure 7a, Probe 3) and at the gate (Figure 7a, Probe 2) of the IGBT for different levels of pulse input voltage (Figure 7a, Probe 1). Parameter adjustment was considered complete when the equivalent circuit could describe the behavior of the IGBT module with minimum errors in all working modes that were measured.

To generate the required input voltage, we used a pulse amplifier based on M1, M2, Q1, and Q2 transistors (Figure 7a). The pulse voltage at the output of the amplifier was regulated by the voltage of the DC source V1. Elements R11, C1, and R2 matched the high-resistance input of the M1 (BSS138) transistor, with 50 Ohm input impedance of the signal generator V2 (Tektronix AFG3252 240 MHz 2 GS/s). Transistor M2 (FDS4897C) had low drain-source impedance ($R_{DS(on)} = 63 \text{ m}\Omega$), which reduced the influence of the input port on the charging and discharging processes of the input capacitances in transistors Q1 (SS8050) and Q2 (SS8550). These transistors formed the output stage of the amplifier and had minimal output impedance and thus minimal influence on the measured quantities. In this case, the charging and discharging processes of the input capacitance of transistor U1 depended completely on resistor R1. Thus, we used high-resistance probes connected to resistor R1 (see Figure 7a).

The IGBT under investigation had an R7 load on the collector, which comprised 18 Ω 2W low-inductive resistors connected in parallel. To decouple the power supply line from the test-bench PCB, several capacitors (C2–C8) of different types were used. Section 3 describes the test-bench examples and results.

3. Model Verification

Several transistors of different types were examined. In this section, we present the results for the two IGBT modules.

3.1. Modeling of SEMIKRON Module SKM200GB123D

IGBT module SKM200GB123D is from SEMIKRON and based on a non-punch-through-type IGBT with an integrated diode. Using this transistor model, we present a comparison of the basic (Figure 8a) and improved (Figure 8b) models in Figure 8.

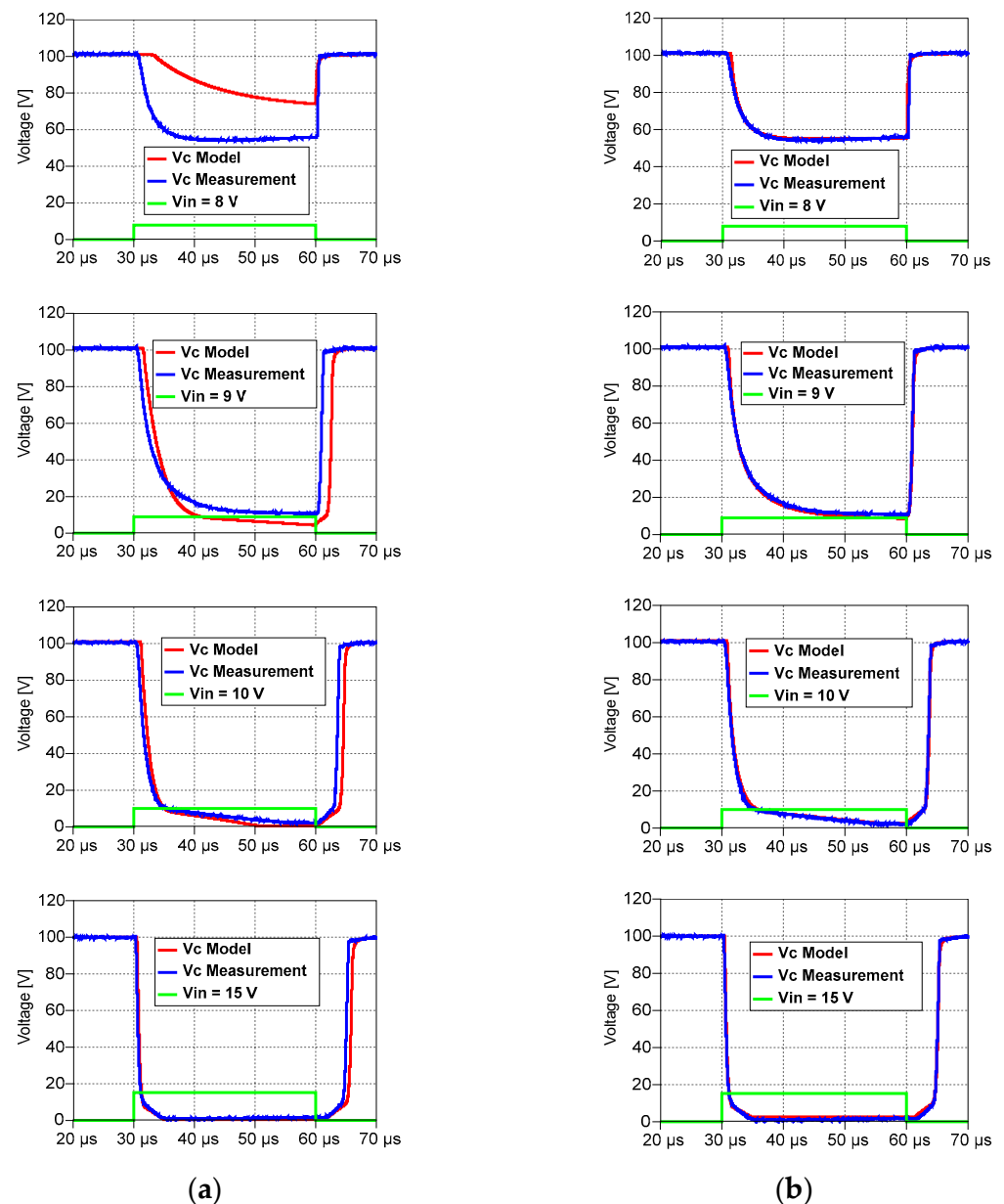


Figure 8. Comparison of collector voltage between basic and improved models. (a) First model (Figure 2); (b) Improved model (Figure 5).

An advantage of the improved model is that it is more accurate when the input voltage level is close to the threshold voltage. Figure 9 shows the collector voltage fall and Rise diagram when the pulse voltage at the gate is 15 v.

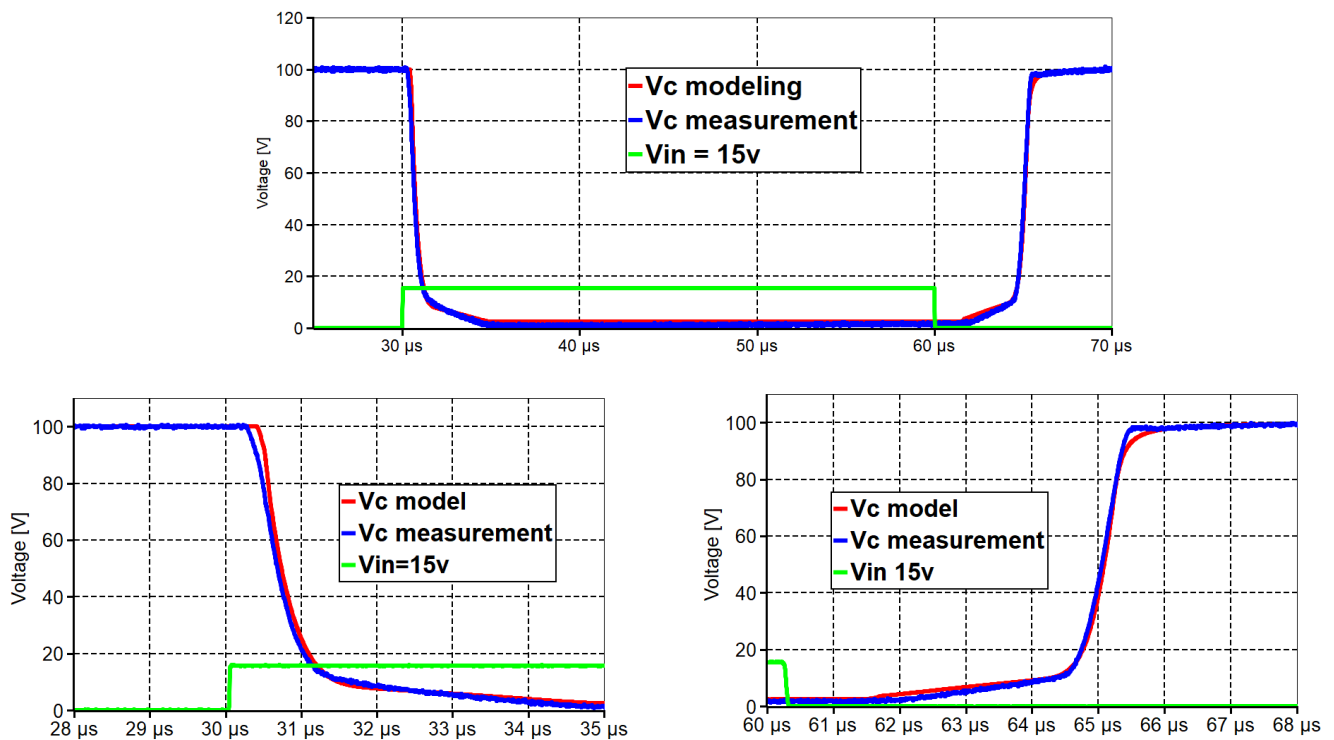


Figure 9. Collector voltage for 15 V input pulse.

Figure 10 represents the modeled and the measured voltages at gate for 15 V of input. The graphs in Figures 8–10 are for $R_1 = 50 \text{ Ohm}$ (Figure 7a). When the value of R_1 decreases, the switching time decreases to the minimum time of the transistor being tested.

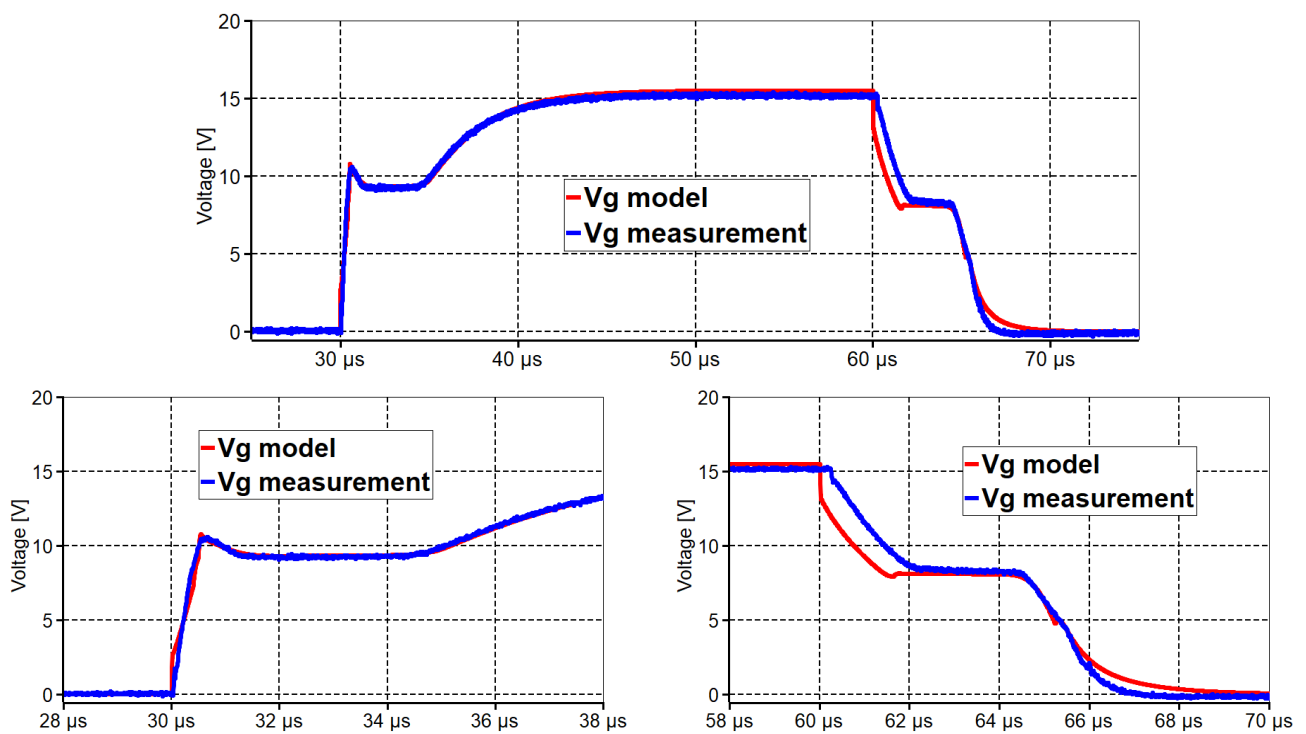


Figure 10. Gate voltage for 15 V input pulse.

3.2. Modeling of Mitsubishi Electric Model CM450DX-24S

Figure 11 shows the test-bench PCB (Printed Circuit Board) designed for Mitsubishi Electric IGBT, Model CM450DX-24S.

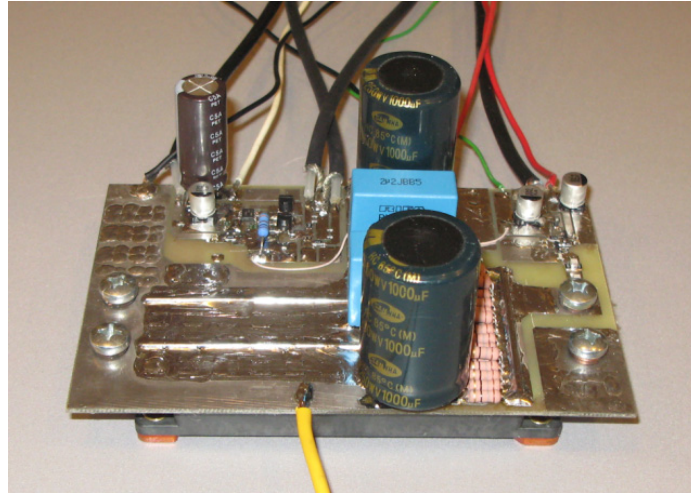


Figure 11. Test-bench PCB with attachment for Mitsubishi Electric CM450DX-24S module.

Figures 12 and 13 represent the results for 15 V of input. Once again, the new model demonstrated high accuracy in comparison with measurements.

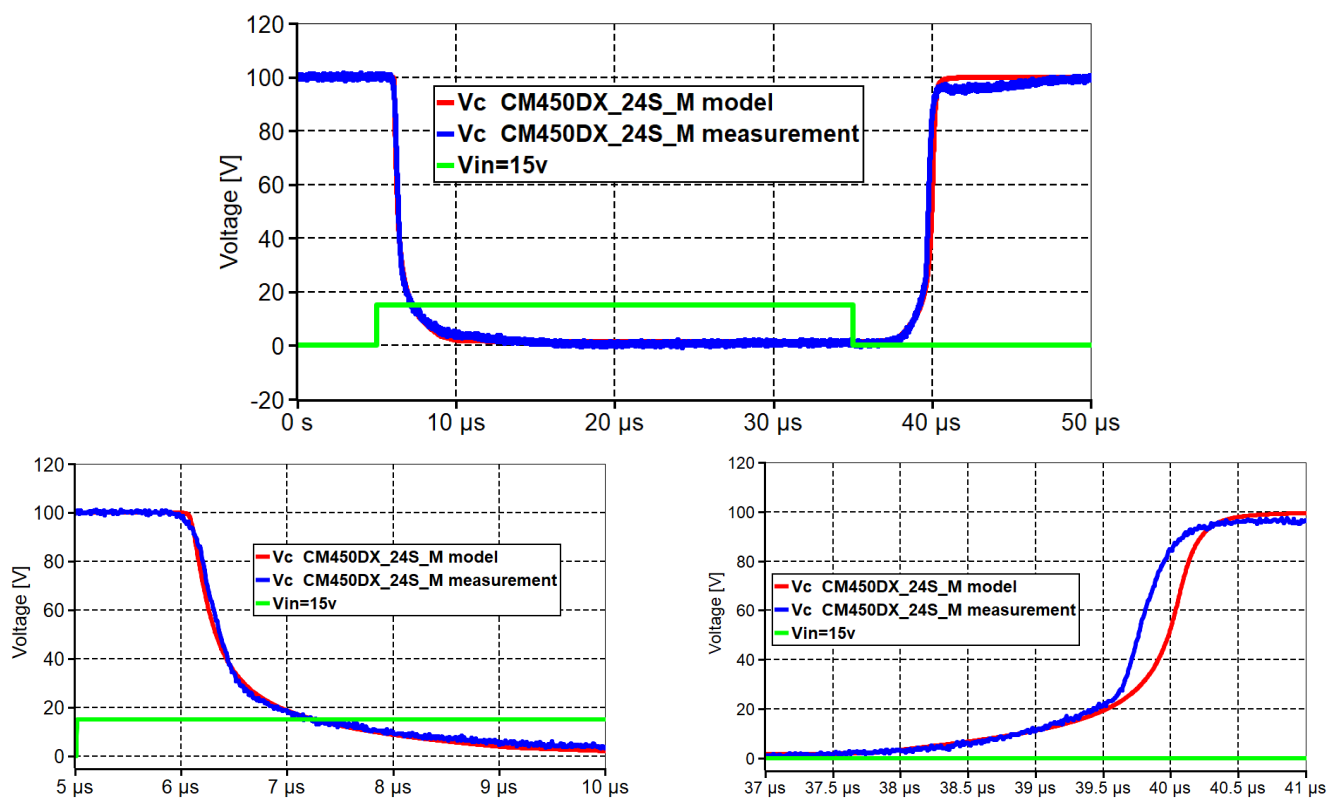


Figure 12. Simulated and measured collector voltages for the Mitsubishi Electric CM450DX-24S module.

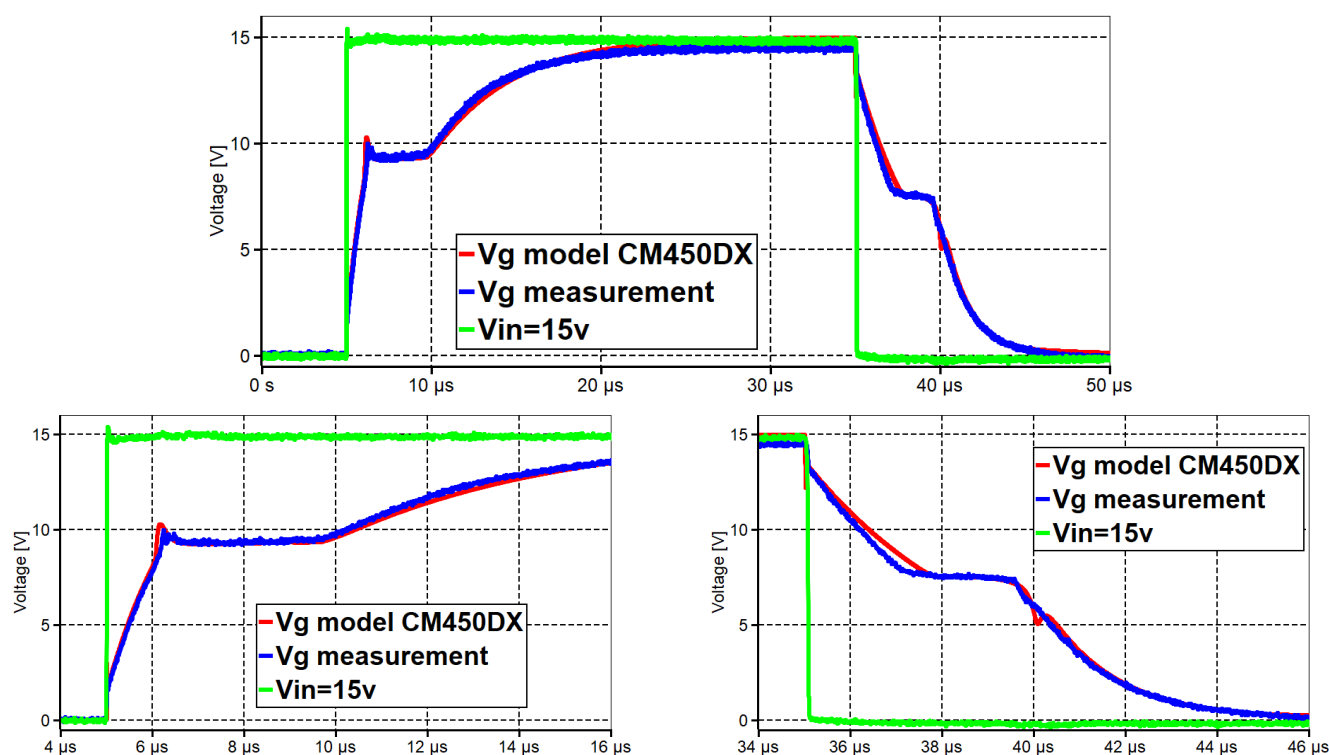


Figure 13. Simulated and measured gate voltages for the Mitsubishi Electric CM450DX-24S module.

Figures 9, 10, 12, and 13 present the good matching of measurement and modeling results. Figure 9 (SKM200GB123D) and Figure 12 (CM450DX-24S) show the change in collector voltage of the IGBT transistor when a 15 V amplitude pulse signal is supplied to the GATE; as it can be seen from the figure, the shapes of the Fall and Rise signals are almost identical in the measured and modeled graphs. The IGBT transistor is supplied with a signal at GATE through 50 Ohm resistors. This allowed us to better understand the current processes at the GATE, which are the complex result of the process of charging and discharging the parasitic capacities of the transistor. Figure 10 (SKM200GB123D) and Figure 13 (CM450DX-24S) show the voltage change pattern on the GATE in the event of 50 Ohms. Here, it should be noted that the signal forms match each other quite well. Small time differences do not have a significant impact on the device modeling results.

4. EMC-Oriented Model of IGBTs and MOSFETS

In this section, we describe an even simpler model of power transistors that can be used to model both IGBTs and MOSFETs. This simple model requires a much smaller number of parameters than the improved model we described above (Figure 5). Thus, it is recommended for preliminary analysis of electronic systems because it reduces design time and computing resources by accelerating calculations by up to 10 times. The parameters used in the model are as follows:

- Ron: drain-source on-state resistance;
- Roff: drain-source off-state resistance;
- Vdr: input drawing pulse signal amplitude;
- Vtr: gate threshold voltage;
- Ciss: input capacitance;
- Coss: output capacitance;
- Crss: reverse capacitance.

All these parameters can be found in the transistor datasheet. For example, Figure 14 shows the transistor diagram and SUBCKT file. We conventionally call it RMOS0101D.

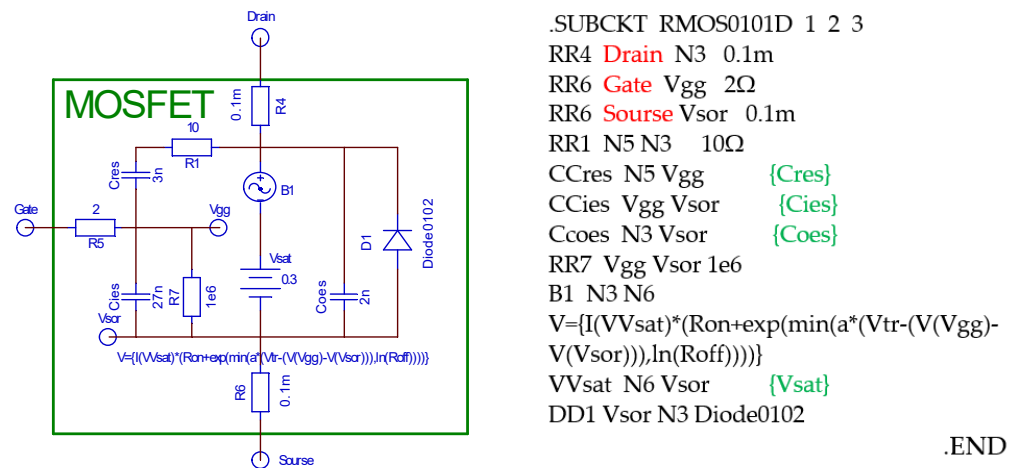


Figure 14. The transistor diagram and SUBCKT file.

Resistance is changed by exponential law:

$$R = R_{on} + e^{\min(a \times (V_{tr} - (V(Vg) - V(Vso))), \ln(R_{off}))} \quad (4)$$

where $a = 2 \times (\ln(R_{on}/R_{off})) / (V_{tr} - V_{dr})$. The minimum and maximum values of resistance, R_{on} and R_{off} , respectively, are bounded (limited) by the “min” function. The rate of change of R from R_{on} to R_{off} depends on coefficient “a.” In general, the selection of the value of “a” should be done with the help of an optimization program. (The given formula is its empirically selected best option.) In Figure 15, the simulation design for RMOS0101D is represented with resistive and inductance loads. Figures 16 and 17 show the results of the modeling.

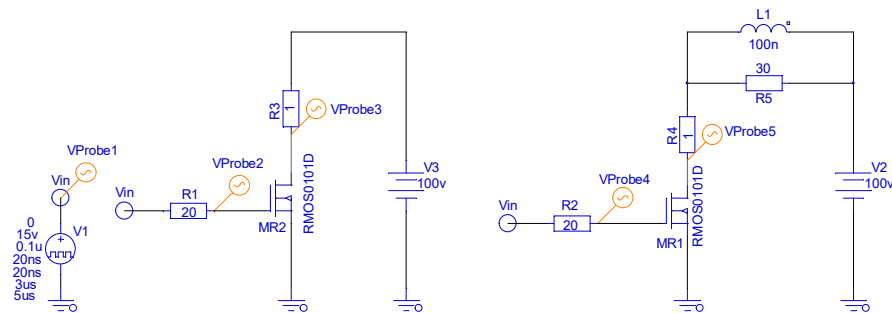


Figure 15. Simulation design for RMOS0101D with resistive and inductance loads.

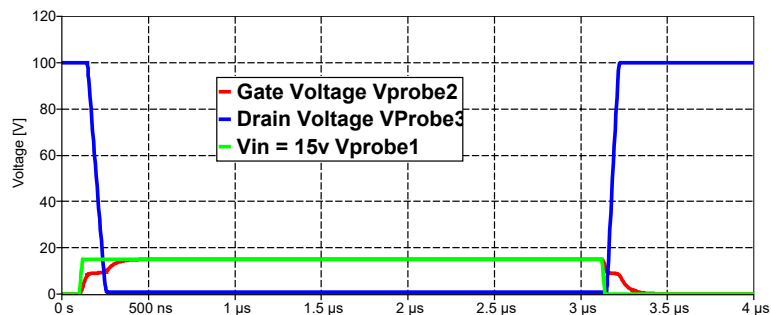


Figure 16. RMOS0101D with resistive load (Figure 15).

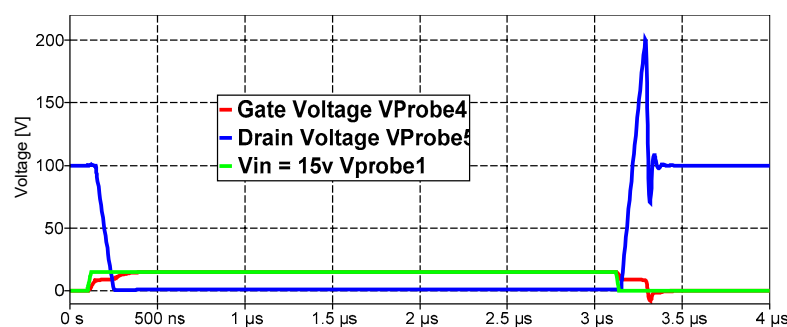


Figure 17. RMOS0101D with inductive-resistive load (Figure 15).

We compared the accuracy model (Figure 5) for the Mitsubishi Electric CM450DX-24S1 module and the simple model for transistor RMOSCM450DM (Figures 18 and 19) with measurement data. Figure 18 shows the transistor diagram and SUBCKT file.

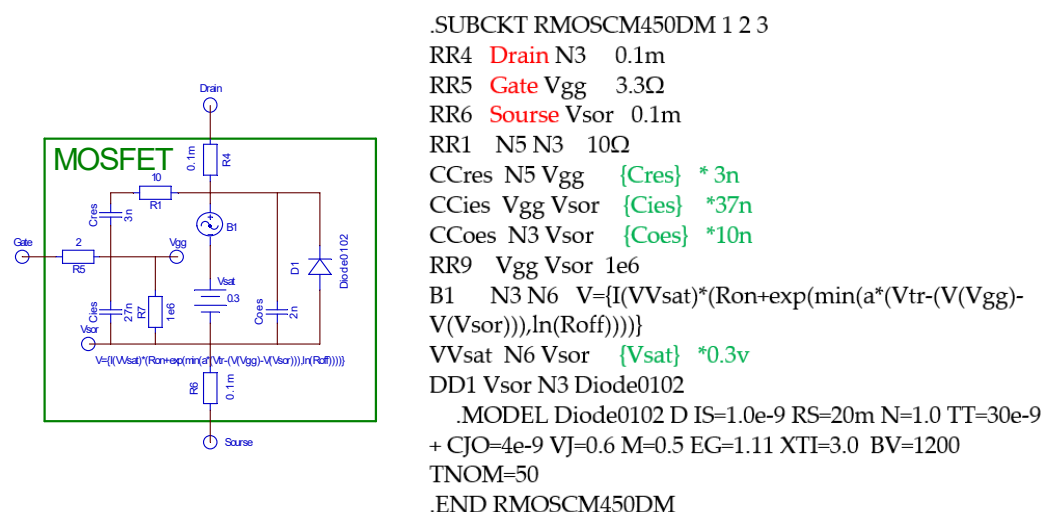


Figure 18. Model of CM450DX-24S1.

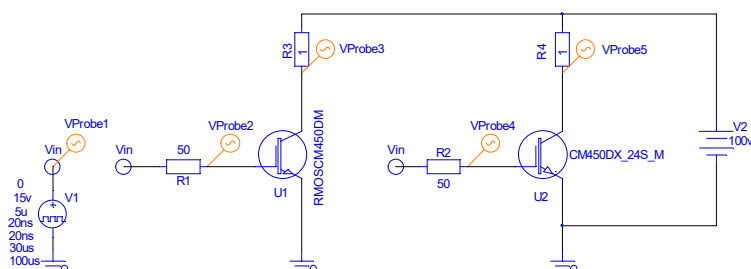


Figure 19. CM450DX-24S modeling test schematic.

This model uses the same exponential function of impedance change as in the previous simple model.

Figure 19 shows the schematic for comparison of models shown in Figures 5 and 18. Figures 20–22 show the comparison of measurements and modeling results.

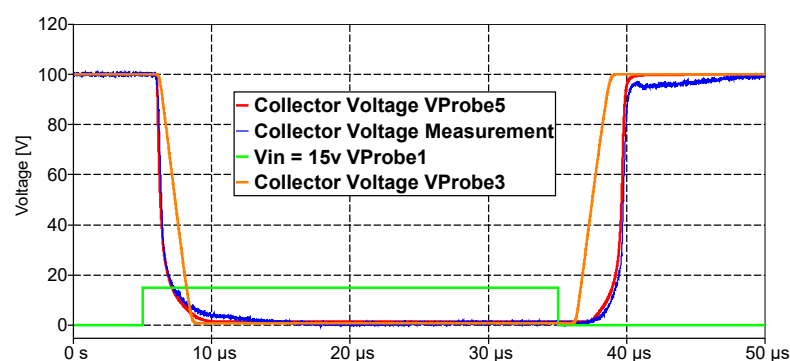


Figure 20. Collector and gate voltages with $R1 = R2 = 50 \text{ Ohm}$ (Figure 19).

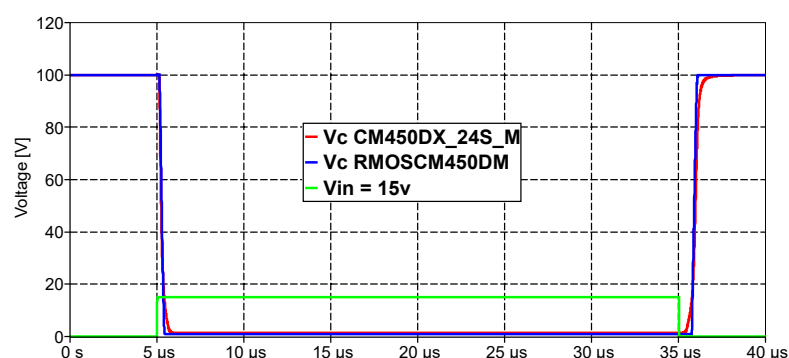


Figure 21. Rise and Fall time with $R1 = R2 = 1 \text{ Ohm}$ (Figure 19).

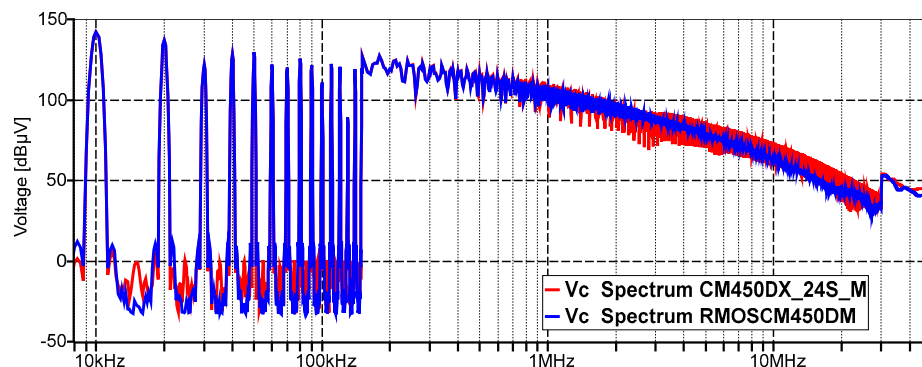


Figure 22. Collector voltages spectrum with $R4 = R3 = 1$ (Figure 19).

If for solving the problem, we need an accurate description of the transient characteristics of the transistor, a simple model is insufficient for this level of simulation (Figure 20). As shown in Figure 21, if only the fast-switching mode of the transistor is needed, then to determine how the currents generated in the circuit are distributed and quickly detect unwanted resonances of filters and wires (EMC problems), a simple model offers a stable and fast solution. Figure 21 shows that the fall and release times, which determine the amplitude and bandwidth of the spectrum, are fairly well described (Figure 22).

We tested the transistors by modeling different types of circuits, such as an inverter, DC–DC converter, power factor corrector, charger, filter, and joint operation. Along with the cables of the listed devices, the modeling was successful. In all cases, the calculations were stable. The signals obtained during modeling and the shape of their spectra matched the measurement results (Figures 26 and 27). The accuracy also was sufficient to detect parasitic resonances in complex harnesses and to determine the causes of their occurrence. The acceleration of the calculation allows engineers to conduct more modeling experiments and solve the problem in a short time.

5. Calculation Times

To compare the calculation times for different transistor models, we used a relatively simple inverter model using space vector pulse width modulation with a filter and a simple motor (Figure 23).

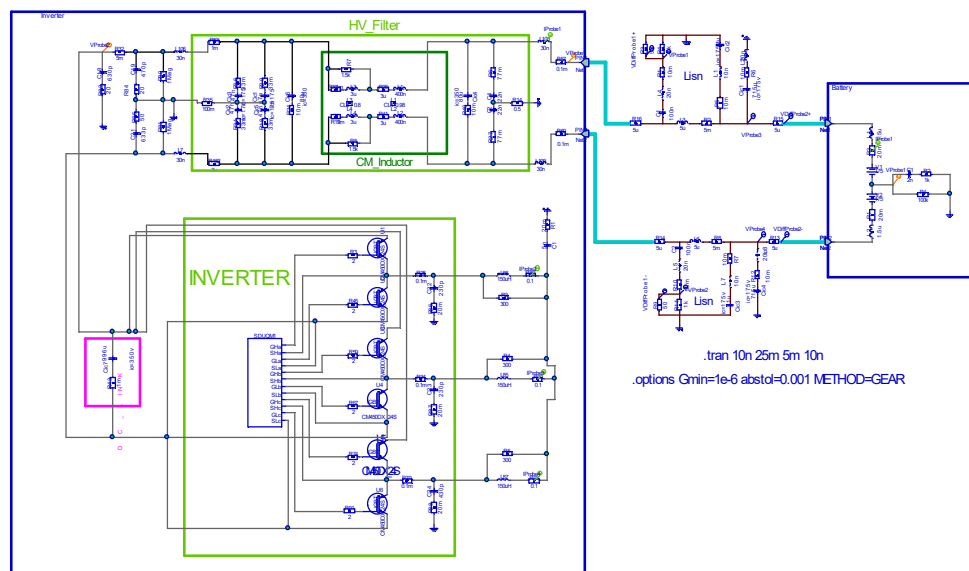


Figure 23. Simple inverter setup.

The results of the calculation times are shown in Table 1.

Table 1. Results of calculation time.

Model	SIMetrix	LTspice
	Calculation Time	Calculation Time
RMOS450DX	3 min 36 s	3 min 58 s
CM450DX-24S	10 min 12 s	19 min 20 s
RGTVM6TS65D (Rohm model)	8 min 57 s	Convergence problem

6. EMC-Oriented Model of IGBT and MOSFET

We assembled an operating stand for the UQM Powerphase 100 (Figure 24).

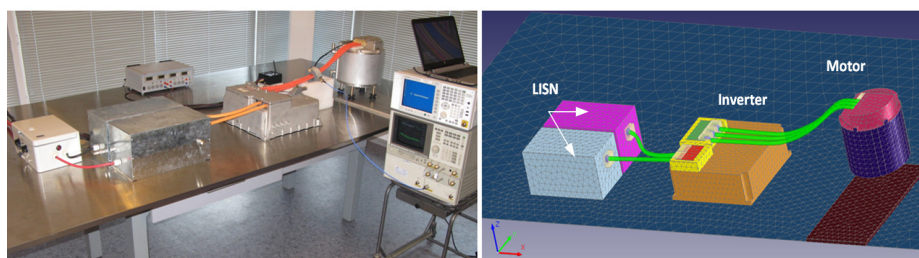


Figure 24. Photo and 3D model of UQM Powerphase 100 setup.

A complete model of this stand was created, including the inverter with space vector pulse width modulation, DC link capacitor, high-voltage filter, line impedance stabilization networks, simplified battery model, and motor and cable models. Modeling was performed in stages. First, we measured the S parameters of the filter and then determined the internal structure of the CM coil using X-ray computed tomography. Based on this information,

we created a CM inductance model. Then, the complete filter model was created. Using the same method, the DC link capacitor and motor models were developed, along with an inverter model with SVPWM modulation. The modeling was done using EMCoS Studio, which allowed the creation of high-voltage cable models to assemble and calculate the complete power train system model. Figure 25 shows the full model of the stand.

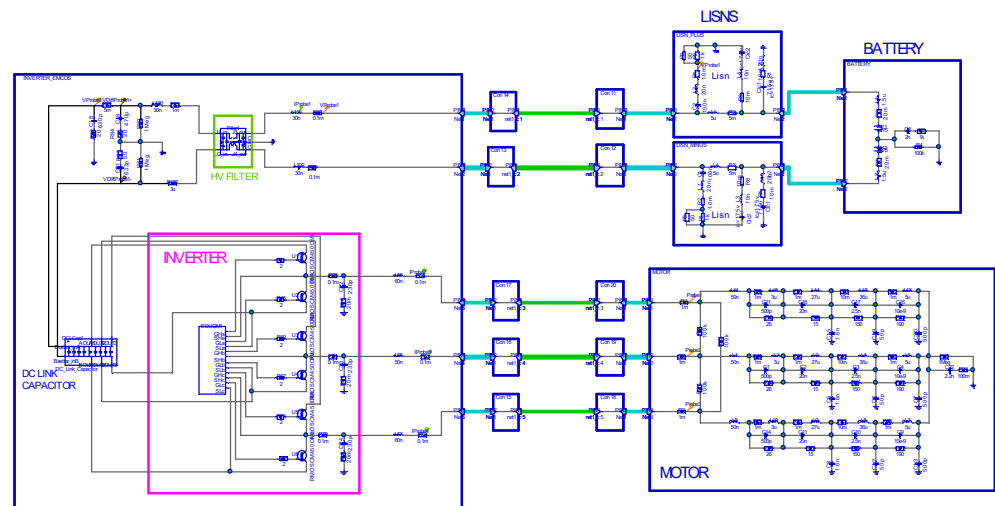


Figure 25. UQM Powerphase 100 setup model.

The model is large and requires optimized transistor models. Thus, we used both a complex IGBT model (CM450DX; Figure 5) and a simple model (RMOS450DX; Figure 21), the parameters of which we took directly from the transistor datasheet.

Figures 26 and 27 show the modeling results. The simple transistor model did not differ much in the calculations, compared to the complex model. Therefore, we concluded that during the EMC pre-analysis of complex systems (e.g., the electrical wiring of a car, ship, aircraft, or other equipment), when it is necessary to detect and prevent parasitic resonances, it is sufficient to use the proposed simple model to save time.

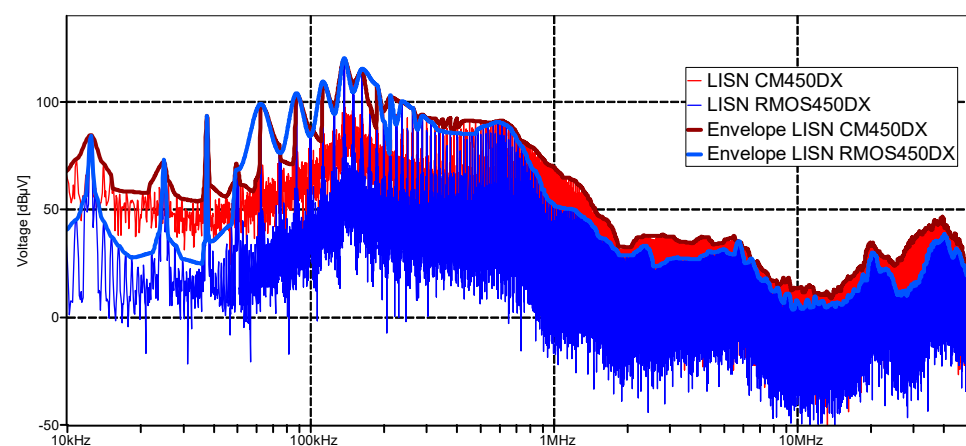


Figure 26. Modeling comparison for CM450DX and RMOS450DX models showing spectra of the LISN.

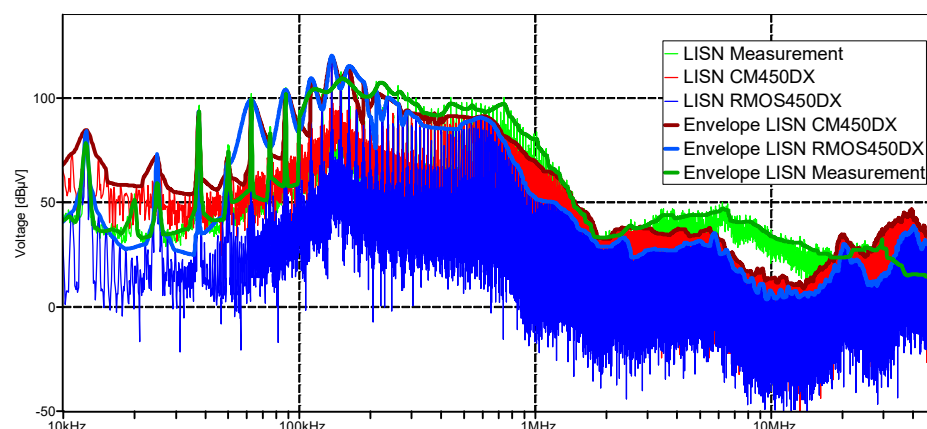


Figure 27. Measurement and modeling comparison.

7. Conclusions

In our paper, we present IGBT modeling that describes transistor characteristics for use in both EMI–EMC and circuit analyses. Two transistor models were developed, both of which account for the physical processes in the semiconductor layers and near the emitter. We introduced nonlinear feedback into the overall circuit model of the IGBT, which significantly improved the simulation of the dynamic characteristics of IGBTs. Moreover, the developed model is relatively simple and robust, which provides advantages in EMI–EMC simulations of complex power devices.

The parameter extraction methodology is based on the values obtained from the IGBT datasheet. Further adjustments were made by comparing simulations and measurements using a single test panel. The second model is an approximate model of the transistor, which can be used only to analyze pulse switching circuits. Nevertheless, it has the advantage of simplicity of setup and stable operation, and it can be used to replace both IGBTs and MOSFETs. Test set modeling with a brushless DC electric motor and inverter demonstrated the applicability of the developed models.

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