electronics

MDPI

Article

Development of a Digitally Controlled Inductive Power Transfer System with Post-Regulation for Variable Load Demand

Kateryna Stoyka [1,*], Antonio Vitale [1], Massimo Costarella [1], Alfonso Avella [1], Mario Pucciarelli [1] and Paolo Visconti [2]

[1] Medinok S.p.A., Via Palazziello, 79, 80040 Volla, Italy; a.vitale@medinok.com (A.V.); m.costarella@medinok.com (M.C.); a.avella@medinok.com (A.A.); m.pucciarelli@medinok.com (M.P.)
[2] Department of Innovation Engineering, University of Salento, Street for Monteroni, 73100 Lecce, Italy; paolo.visconti@unisalento.it
* Correspondence: k.stoyka@medinok.com; Tel.: +39-3206242635

Abstract: Inductive Power Transfer (IPT) is an emerging technology enabling a contactless charging process in manifold applications such as electric vehicles, wearable and portable devices, or biomedical applications. Such technology can be profitably used to develop enhanced electronic solutions in the framework of smart cities, homes and smart workplaces. This paper presents the development and realization of a series–series compensated IPT System (IPTS) followed by a post-regulator implemented by means of a DC–DC converter. Such a system is modeled through a first harmonic approximation method, and a sensitivity analysis of the IPTS performance is carried out with respect to the variations of the primary inverter switching frequency and phase-shift angle. As an element of novelty of this work, the bias points are determined which allow the efficiency maximization while ensuring system controllability. An enhanced dynamic modeling of the system is then performed by means of a coupled mode theory, including the inverter phase-shift modulation and extending its validity to whatever operating frequency. A digital control of the post-regulator is implemented by means of a commercial low-cost microcontroller enabling the output voltage regulation under both fixed and variable load conditions through a voltage mode control technique. An IPTS prototype is eventually realized, which is able to correctly perform the output voltage regulation at the desired nominal value of 12 V for static resistive loads in the range [5, 24] Ω, yielding the output power in the range [6, 28.8] W and the experimental efficiencies going from 72.1% (for 24 Ω) to 91.7% (for 5 Ω). The developed system can also be effectively used to deliver up to 35 W output power to variable loads, as demonstrated during the battery charging test. Finally, an excellent output voltage regulation is ascertained for load transients between 5 Ω and 24 Ω, with limited over- and undershoot amplitudes (less than 3% of the nominal output voltage), thus enabling the use of the proposed system for both fixed and variable loads in the framework of smart homes and workplaces applications.

Keywords: DC–DC converters; digital control; inductive power transfer systems; modeling; pot cores; switch-mode power supplies; wireless power transfer

Citation: Stoyka, K.; Vitale, A.; Costarella, M.; Avella, A.; Pucciarelli, M.; Visconti, P. Development of a Digitally Controlled Inductive Power Transfer System with Post-Regulation for Variable Load Demand. *Electronics* **2022**, *11*, 58. https://doi.org/10.3390/electronics11010058

Academic Editor: Nikolay Hinov

Received: 24 November 2021
Accepted: 21 December 2021
Published: 25 December 2021

1. Introduction

The wireless charging of electric and electronic devices and systems has become increasingly popular in everyday life since it allows for a contactless power transfer between a stationary primary source and one or more stationary or movable secondary loads. In this framework, Inductive Power Transfer (IPT) allows for a safe, reliable and cost-effective charging process over relatively large air-gaps via magnetic coupling between the primary transmitting and the secondary receiving coil, by exploiting the same operation principle as that of transformers and coupled inductors but with weaker coupling. Today, IPT Systems (IPTSs) are used in manifold applications such as charging electric vehicles [1], as

extensively discussed in [2], mobile [3] and portable [4] devices, biomedical applications [5], etc. Such technology can be profitably used to develop enhanced electronic solutions in the framework of smart cities [6], homes [7] and smart workplaces [8].

Resonant circuits are normally employed in the primary and/or secondary IPTS side to increase the power transfer capability while minimizing the required voltage and current ratings of the power supply [9]. Different compensation topologies can be adopted in this regard, depending on the resonant circuit configuration. The simplest and most used topology is a Series–Series (S–S) compensation, which employs a resonant capacitor in series with each coupling coil. One of the advantages of the S–S topology is that there is no reflected reactance if the IPTS is operated at the secondary resonant frequency. Thus, the primary inductance can be compensated independently of either the magnetic coupling or the load by a series-connected capacitance in the primary network. Hence, the S–S compensation has been adopted for the IPTS presented in this paper. As regards the IPT coil configuration, different commercial off-the-shelf parts are available from manufacturers such as Würth Elektronik [10], TDK [11] and Abracon [12], satisfying the given constraints of the size, of the self and mutual inductance, as well as of the DC winding resistance and rated current values. However, as the available coupling area becomes smaller, only commercial products with rather high DC winding resistance values are available for a certain inductance target, since small winding cross-section areas are usually adopted to meet the dimensional requirements. Consequently, rather high power losses are expected to occur in the coil windings as the application currents increase, leading to lower overall system efficiencies. Hence, custom coils should be realized for the applications requiring relatively small coupling areas and relatively high currents.

Generally, the main requirements which need to be satisfied by the IPTSs concern the output voltage/current regulation and the system efficiency maximization. The first one depends on the load specifications (battery, resistive load, etc.) and is usually the primary design objective which has to be fulfilled. In recent years, different IPTS architectures and control techniques have been proposed to reach the above requirements. These include the IPT systems with passive [13] and active [14] rectification on the receiving side, as well as the IPTS with regulating rectifiers [15]. More complex solutions include the pre-regulated and the post-regulated IPTSs using the DC/DC converters on the transmitting and the receiving side, respectively [16]. A detailed overview of different IPTS architectures and control techniques is provided hereinafter, and the relative advantages and drawbacks are highlighted.

In this paper, we present a digitally controlled IPT system with a synchronous rectification and a step-down DC/DC converter used as a post-regulator. The output voltage regulation for variable loads is accomplished by means of the digital voltage mode control of the DC/DC converter, while the maximum efficiency is achieved by modulating the switching frequency and the phase-shift angle of the full-bridge inverter located at the transmitting IPTS side. A static system-level modeling of the proposed IPTS has been performed through a First Harmonic Approximation (FHA) method, since the resonant coil currents are nearly sinusoidal, and only the first harmonics of the primary and the secondary voltages and currents contribute to the power transfer.

As a first element of novelty of this work, we have developed the FHA-based static model of the post-regulated S–S IPTS, and carried out a sensitivity analysis of the system performances with respect to the variations of the main operating parameters and component values. In particular, we have adopted such a model with a two-fold purpose: (i) to determine the optimal values of the compensation capacitances for given IPT coils; (ii) to perform the mapping of the system performances with respect to several IPTS operating parameters (namely the inverter switching frequency and phase-shift angle), so as to determine the maximum overall efficiency.

As a second element of novelty, we have investigated the controllability issues of the buck post-regulator cascaded to the IPTS using the developed FHA static model. In this regard, we have shown that the buck output voltage can present a non-monotonic behavior

with respect to the duty-cycle, which may lead to system instability for certain parameters and component values. Hence, feasible operating regions have been determined wherein the system controllability is ascertained.

As a third element of novelty, we have performed the dynamic modeling of the post-regulated IPTS by means of Coupled Mode Theory (CMT). In this regard, we have enhanced the original CMT modeling procedure by including the inverter phase-shift modulation and by extending its validity to whatever operating frequency. As a result, the control-to-output transfer function of the post-regulator has been obtained, enabling the digital controller design needed for the output voltage regulation.

An experimental prototype of the IPTS has been eventually developed to be able to deliver up to 35 W output power at the maximum efficiency of 91.7%. The article is arranged as follows: in the next sub-section, an overview of different IPTS architectures and control techniques is provided; in Section 2, the static system-level modeling of the presented IPTS is discussed, followed by the dynamic modeling and digital controller design presented in Section 3. The experimental prototype of the proposed IPTS is described in Section 4, and the measurements results are provided and discussed. Eventually, the conclusions are drawn in Section 5.

1.1. Overview of IPTS Architectures and Control Techniques

Figure 1 depicts one of the most commonly used architectures of the IPT systems based on the S–S compensation topology and using a full-bridge inverter on the transmitting (TX) side and a passive diode-bridge rectifier on the receiving (RX) side. The primary inverter converts the DC voltage and current waveforms of the source into the AC waveforms applied to the primary resonant tank, which is composed of a primary IPT coil and the respective resonant capacitor. The power is wirelessly transferred between the primary and the secondary coil by means of mutual coupling, and the resulting AC voltage and current waveforms of the secondary resonant tank are rectified by the diode-bridge and delivered to the load. For such IPTS topology, it is not possible to realize the output voltage regulation entirely on the RX side, since the diodes are automatically turned on and off depending on the secondary coil current direction. The research presented in [13] proposed a control scheme to regulate the output voltage of the S–S IPTS with passive rectification by controlling the switching frequency or the phase-shift angle of the full-bridge inverter. A detailed dynamic analysis based on the extended describing function technique was presented and the small-signal model of the system derived including both the frequency and the phase-shift control. However, such a control strategy requires the presence of a communication link between the TX and RX sides, which introduces a delay in the control loop and thus limits the dynamic performances of the proposed control scheme.

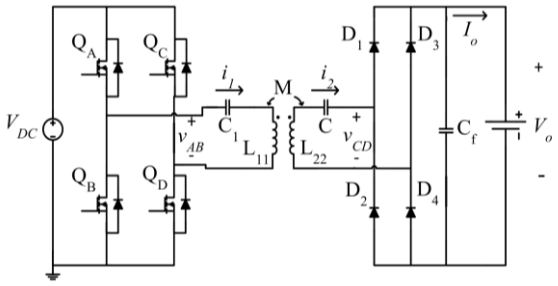


Figure 1. S–S IPTS with passive rectification [13].

An active rectification scheme replaces rectifier diodes with power MOSFETs, thus allowing to control their switching process and directly regulate the output voltage on the RX side, without using any communication link with the TX side. In [14], a fixed-frequency phase-shift control strategy was proposed for dual active IPTS including full-bridge inverter and rectifier. In such a scheme, the secondary phase-shift angle is controlled to regulate the system output voltage, while the primary phase-shift angle is adjusted to achieve the

minimum duty-cycle needed for zero-voltage switching (ZVS). The complication of the proposed scheme is that the current phase detection circuits are required on both the TX and RX sides to realize the proposed control strategy.

A similar bidirectional S–S IPTS with a double active bridge configuration was presented in [17], with the difference that two cascaded contactless transformers have been adopted for energy charging between electric vehicles. Two control strategies were implemented: the Primary Phase-Locked Loop (P-PLL) and Pulse-Width Modulation (PWM) control (P-PLL&PWM) and the Primary Constant Frequency plus Secondary PWM control (P-CF+S-PWM). In the P-PLL&PWM control scheme depicted in Figure 2, the PWM controller regulates the pulse width of the primary full-bridge inverter to regulate the output voltage, and the PLL control strategy regulates the frequency of the inverter to the achieve the ZVS of power devices on the primary side, while the active bridge rectifier on the RX side works as a conventional rectifier circuit. In the P-CF+S-PWM scheme shown in Figure 3, the primary inverter provides a full square-wave voltage having a constant switching frequency, while the output voltage regulation is realized entirely on the RX side by controlling the rectifier pulse-width duration. Hence, the second approach does not require a communication link between the TX and RX side. The experimental results suggest that the P-CF+S-PWM control has higher efficiency. However, such a strategy does not consider the efficiency maximization and can therefore be improved.

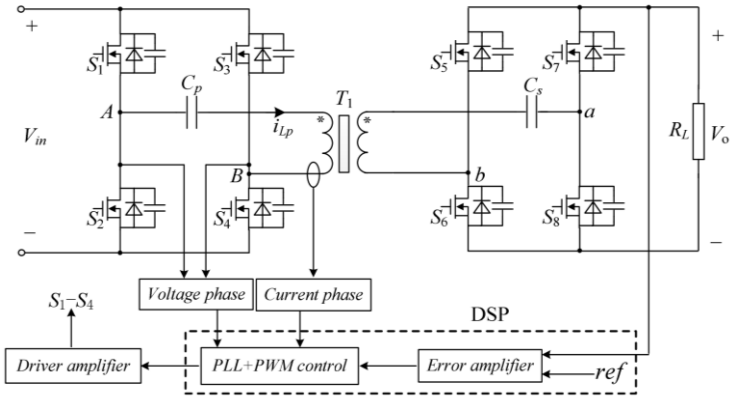


Figure 2. Dual active S–S IPTS with P-PLL&PWM control strategy [17].

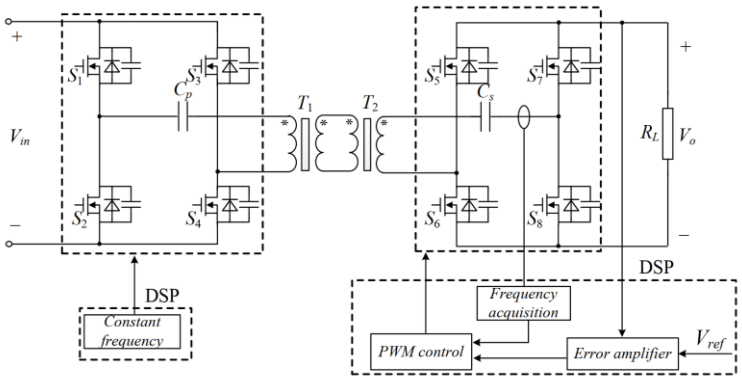


Figure 3. Dual active S–S IPTS with P-CF+S-PWM control strategy [17].

A more complex IPTS scheme with active rectification and a post-regulator on the RX side depicted in Figure 4 was proposed in [18] with the scope to maximize the efficiency as well as increase the amount of extractable power while operating in non-resonant conditions. The proposed method is based on actively modifying the equivalent secondary-side load impedance Z_L seen at the rectifier input, by controlling the phase-shift φ of the active rectifier and its output voltage level V_r. This parameter can be controlled by either

adjusting the duty-cycle D of the post-regulator or by varying the duty-cycle δ of the active rectifier, as shown in Figure 5. The phase-shift φ between the secondary voltage V_L and current I_L is realized by inserting a time delay between the primary and secondary side control signals, which is achieved by using a communication link between the primary and secondary side controllers. The proposed scheme considers a constant battery voltage at the IPTS output and does not perform the output voltage regulation, which could be a drawback for different types of load.

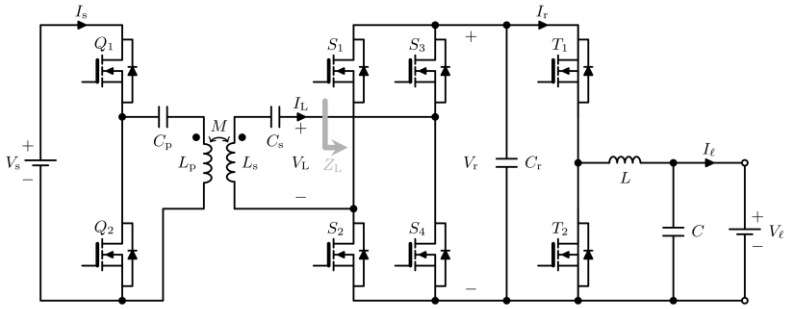
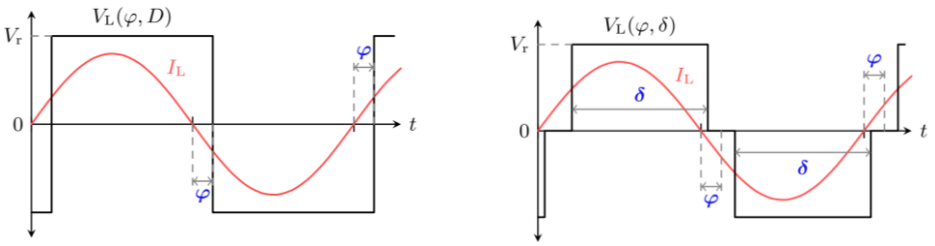


Figure 4. S–S IPTS with active rectifier and buck post-regulator [18].



(**a**) (**b**)

Figure 5. Graphs of voltage V_L and current I_L delayed by the phase shift φ obtained by varying: (**a**) the buck duty-cycle D and (**b**) the active rectifier duty-cycle δ, where V_r is the resulting rectified voltage [18].

To enhance regulation capabilities of the IPTS schemes with passive rectification such as the one depicted in Figure 1, pre- or post-regulators can be adopted. Some of the papers introducing IPTSs with post-regulating DC/DC converters have used the perturb-and-observe (P&O) techniques to achieve maximum system efficiency. The research presented in [19] proposed the S–S IPTS using a passive diode-bridge rectifier followed by a cascaded boost-buck converter. A P&O technique was adopted which searches for the optimal post-regulator duty-cycle value maximizing the overall system efficiency obtained at the IPT resonant frequency. Similarly to the work presented in [18], no regulation of the output voltage was included in the above control scheme. In [20], a method for automatic maximum efficiency point tracking of the IPTS followed by a buck–boost converter was proposed. The presented algorithm searches for the minimum input power operating point for a given output power by varying the phase-shift of the inverter, while the PI controller of the buck–boost adjusts the output voltage. Because the searching process is carried out on the TX side, the proposal does not require any feedback from the RX side. The research in [21] proposes some improvements with respect to [20], by adopting a Discrete Sliding Mode Control (DSMC) scheme for the buck–boost post-regulator. The TX side of the adopted IPTS comprises a phase-shift full-bridge inverter, which incorporates the hill-climbing-search-based phase angle control for achieving minimum input current injection from its DC source, thereby attaining minimum the input power operation. The buck–boost converter realizes the output voltage regulation by means of the proposed DSMC scheme, which outperforms classical PI controller-based schemes in terms of better dynamic performances.

The S–S IPTS with a passive rectifier and a Single-Ended Primary Inductor Converter (SEPIC) depicted in Figure 6 was proposed in [22]. The SEPIC topology offers several benefits in switching power supplies thanks to its non-inverting step-up/step-down conversion ratio, to the possibility of reducing the size of magnetic components by using coupled inductors and to its loss-less resistor behavior in power factor pre-regulation applications [23]. A phase-shift control of the primary inverter was designed to regulate the primary coil current at a given reference value, in order to optimize the equivalent load resistance seen at the post-regulator input for maximum energy efficiency. A peak-current-control of the SEPIC was configured to guarantee the output voltage regulation under different load conditions. A disadvantage of the proposed approach consists of utilizing a refence value for the primary current (to achieve the optimal load conditions) which is very sensitive to the coupling coefficient and system component variations.

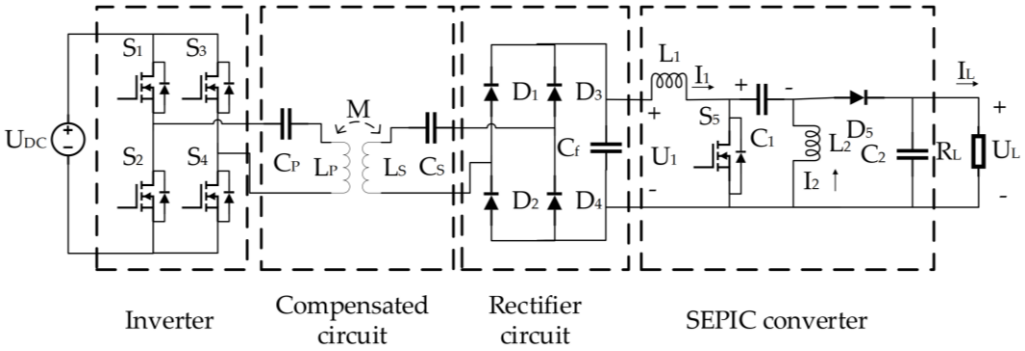


Figure 6. S–S IPTS with passive rectifier and SEPIC post-regulator [22].

A more complicated control scheme for the IPTS with a passive rectification and a buck–boost post-regulator was proposed in [24] with the aim of maximizing the overall system efficiency while maintaining a constant output power level. In such a scheme, a primary-to-secondary voltage ratio is regulated through the buck–boost duty-cycle control to reach the maximum efficiency under resonance conditions, while the IPTS input voltage is adjusted to yield the target output power to the load. Such a control scheme requires a pre-regulator (e.g., a boost converter) to change the IPTS input voltage, which ends up being complicated for practical implementations; moreover, the proposed voltage ratio control criterion is only valid under given resonance conditions. Finally, the output voltage regulation is not included in the above control scheme.

The authors in [25] presented a Maximum Efficiency Point (MEP) tracking method for IPTSs whose RX side contains either a passive rectifier with post-regulator or a regulating rectifier. This last rectification topology uses two additional MOSFETs at the input of the diode bridge which are periodically turned on and off to regulate the IPTS output voltage. It is proven that, under resonance conditions, at the MEP, the derivative of post-regulator duty-cycle D with respect to the inverter DC input voltage V_{in} is equal to or smaller than a constant β determined by the system parameters, namely $\mathrm{d}D/\mathrm{d}V_{in} \leq \beta$. It is also shown that increasing V_{in} allows to reach the MEP as soon as $\mathrm{d}D/\mathrm{d}V_{in}$ becomes equal to or lower than β. Thus, the MEP can be tracked without a power or current sensor.

Four different IPTS schemes and relative control techniques were analyzed and compared in [16], with the scope to achieve the output voltage regulation: Lower-side Frequency Control (LFC), Higher-side Frequency Control (HFC), pre-regulation, and post-regulation. The first two techniques are based on the behavior of an open-loop IPTS which presents two peaks near the split frequencies in the "over coupled" region, as depicted in Figure 7. In particular, LFC (HFC) controls the inverter switching frequency on the left (right) side of the low (high) split frequency to regulate the IPTS output voltage. Conversely, the pre- (post-) regulation scheme adopts a DC/DC converter on the primary (secondary) IPT side to regulate the output voltage by fixing the switching frequency and controlling the converter duty-cycle. A Maximum Efficiency Point Tracking (MEPT) control scheme was proposed

based on the use of a both pre- and post-regulating DC/DC converter (see Figure 8), where the output voltage regulation is accomplished by the post-regulator controller, while the maximum efficiency is achieved by the pre-regulator controller.

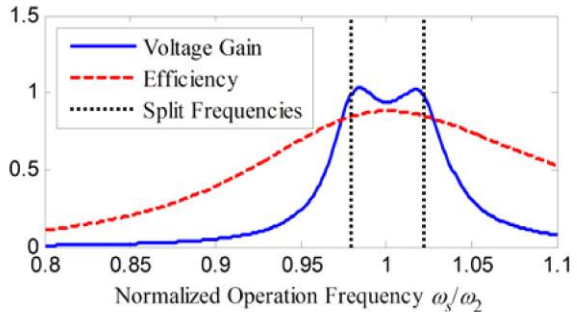


Figure 7. Illustration of the IPTS voltage gain and efficiency including split frequencies [16].

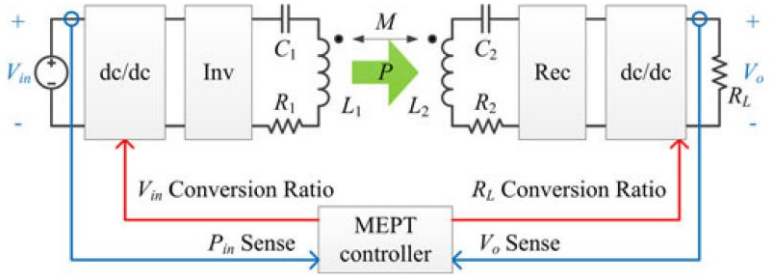


Figure 8. Closed-loop system structure of the MEPT control scheme proposed in [16].

Eventually, Ref. [26] presented an MEPT algorithm for the post-regulated IPTS to match the load impedance to that of the source impedance. The proposed algorithm varies both the switching frequency and the phase-shift of the inverter to minimize the input power, whereas the output power is kept constant by a buck converter, which is used to regulate the battery voltage and current. The drawback of the proposed study is that, during the buck controller design, the influence of the IPTS on the duty-to-output transfer function of the buck converter is not taken into account.

In this paper, we overcome such a limitation by correctly modeling the post-regulator dynamics accounting for the IPTS connected to its input. To this end, we exploit the findings of [27] which used Coupled-Mode Theory (CMT) to deal with the dynamic modeling of the IPTS pre-regulated by a buck converter. Such an approach uses slowly varying amplitudes and phases of coupled modes, rather than resonant currents and voltages, to model the coupled resonances of the IPT stage. It also includes the non-linearities of the inverter and rectifier stages operating at a full square-wave voltage under IPTS resonant conditions. A continuation of [27] can be found in [28], where the steady-state and dynamic characteristics of an open-loop IPTS post-regulated by a buck–boost converter are investigated by means of the CMT. It is shown that, for certain operating conditions and system component values, the steady-state control-to-output curve of the post-regulator can be non-monotonic, since its static and dynamic characteristics are tightly coupled to the IPT stage. In particular, when the control-to-output curve changes its slope and starts decreasing, the system runs into positive feedback and goes out of control. In this paper, we enhance the modeling procedure proposed in [27,28] by including the inverter phase-shift modulation and by extending its validity to whatever operating frequency. Such an enhanced procedure is herein formulated for the buck post-regulator, but its findings are general and can also be applied to other basic converter topologies (e.g., boost, buck–boost, etc.).

A comparison between the main IPTS solutions discussed previously and the system developed in this work is subsequently provided in the Section 4.4, highlighting their relevant features and specifications.

2. Static Modeling of Post-Regulated IPTS

2.1. Post-Regulated IPTS (PR-IPTS)

Figure 9 shows a schematic of a Post-Regulated IPTS (PR-IPTS) using a series–series compensation topology. The coupling coils, represented by the self-inductances L_1 and L_2, are compensated with the series capacitors C_1 and C_2. The magnetic coupling between the coils is represented by their mutual inductance M. The TX coil is connected to the source through a MOSFET full-bridge inverter implementing a phase-shift and frequency modulation, with the objective of maximizing the overall system efficiency. The phase-shift modulation consists of modulating the phase angle α between the complementary square-wave gate signal pairs used to control the MOSFETs of the two inverter legs, as depicted in Figure 10. As a result, a modified square-wave voltage $v_1(t)$ is obtained at the inverter output (indicated by the green waveform in Figure 10). The resistor R_1 includes the equivalent resistances of L_1, C_1 and of the two inverter MOSFETs conducting simultaneously.

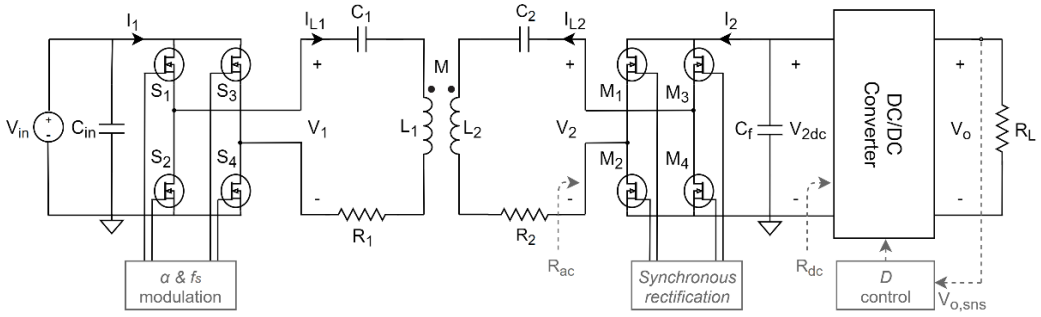


Figure 9. Series–series post-regulated IPTS schematic.

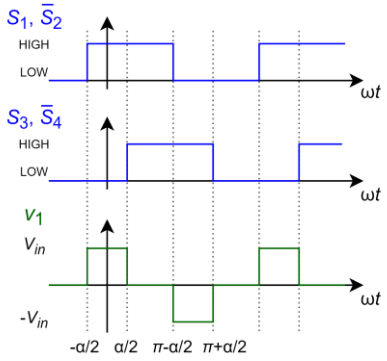


Figure 10. Waveforms example of the phase-shift modulation: MOSFET gate signals (blue) and inverter output voltage (green).

The RX coil is connected to the resistive load R_L through a MOSFET full-bridge rectifier followed by a buck DC/DC converter implementing a duty-cycle D control at a fixed switching frequency f_{Buck}. Such control aims to regulate the system output voltage V_o at a desired nominal value $V_{o,nom}$, under both static and dynamic load conditions. As a result of the presence of the buck converter, the equivalent DC resistance seen at the rectifier output is given by (1):

$$R_{dc} = R_L / M(D)^2 \quad (1)$$

where $M(D) = V_o / V_{2dc} = D$ represents the buck conversion ratio while V_{2dc} is the intermediate bus voltage between the rectifier and the buck. The resistor R_2 includes the equivalent resistances of L_2, C_2 and of the two rectifier MOSFETs conducting simultaneously. A synchronous rectification scheme has been herein adopted for the full-bridge rectifier, in which each MOSFET is turned on after a short conduction of the relative body-diode (as soon as its drain–source voltage decreases below a given negative threshold), and is turned off

when its drain–source voltage exceeds the threshold [29]. Thus, the conduction losses can be reduced as compared to the passive diode bridge configuration [30].

2.2. Static Modeling of PR-IPTS

The above PR-IPTS has been modeled using an FHA method, since the primary and the secondary coil currents are nearly sinusoidal, and only the first harmonics of the voltages ($v_1(t)$, $v_2(t)$) and currents ($i_{L1}(t)$, $i_{L2}(t)$) contribute to the power transfer. Such FHA quantities can be represented through their respective phasors $\overline{V}_1 = V_1 e^{j\phi V_1}$, $\overline{V}_2 = V_2 e^{j\phi V_2}$, $\overline{I}_{L1} = I_{L1} e^{j\phi_{L1}}$, $\overline{I}_{L2} = I_{L2} e^{j\phi_{L2}}$.

As a result of the phase-shift modulation, the peak amplitude of the primary voltage phasor is given by (2):

$$V_1 = \frac{4}{\pi} V_{in} \sin\left(\frac{\alpha}{2}\right) \tag{2}$$

The FHA allows to model the power electronics connected to the RX side with an equivalent AC resistance R_{ac}, expressed as the ratio between the amplitudes of the first harmonics of voltage and current at the input of the rectifier bridge [1]:

$$R_{ac} = \frac{V_2}{I_{L2}} = \frac{8}{\pi^2} R_{dc} \tag{3}$$

Under FHA assumption, the analyzed IPTS can be described with the following phasor equation system (4):

$$\begin{cases} \overline{V}_1 = \left(j\omega_s L_1 + \frac{1}{j\omega_s C_1} + R_1\right)\overline{I}_{L1} + j\omega_s M \overline{I}_{L2} \\ \overline{V}_2 = j\omega_s M \overline{I}_{L1} + \left(j\omega_s L_2 + \frac{1}{j\omega_s C_2} + R_2\right)\overline{I}_{L2} = -R_{ac}\overline{I}_{L2} \end{cases} \tag{4}$$

where $\omega_s = 2\pi f_s$ represents the angular switching frequency of the inverter. For a certain value of the intermediate bus voltage V_{2dc}, the equivalent resistance R_{ac}, seen by the IPT secondary side, can be evaluated using (1) and (3), while the peak amplitude of the secondary voltage first harmonic is given by (5):

$$V_2 = \frac{4}{\pi} V_{2dc} \tag{5}$$

If the phase ϕ_{V2} is taken as a zero reference for the phase angles, the phasor $\overline{V}_2 = V_2$ is known, and the equation system (4) can be solved to obtain the remaining phasors, as given in (6):

$$\begin{gathered} \overline{I}_{L2} = -\frac{\overline{V}_2}{R_{ac}}, \qquad \overline{I}_{L1} = \frac{\left(j\omega_s L_2 + \frac{1}{j\omega_s C_2} + R_2 + R_{ac}\right)}{j\omega_s M} \frac{\overline{V}_2}{R_{ac}} \\ \overline{V}_1 = \frac{\left[\left(j\omega_s L_1 + \frac{1}{j\omega_s C_1} + R_1\right)\left(j\omega_s L_2 + \frac{1}{j\omega_s C_2} + R_2 + R_{ac}\right) + \omega_s^2 M^2\right]}{j\omega_s M} \frac{\overline{V}_2}{R_{ac}} \end{gathered} \tag{6}$$

Starting from (6), it is possible to evaluate the peak amplitude of the primary voltage first harmonic V_1, and estimate the resulting phase-shift α by inverting (2):

$$\alpha = 2\arcsin\left(\frac{\pi}{4}\frac{V_1}{V_{in}}\right) \tag{7}$$

If the resulting α value is real and included in the range $[0, \pi]$, the analyzed operating condition (relative to the considered V_{2dc} value) is feasible, and the primary and secondary IPT average powers P_1 and P_2 can be evaluated according to (8):

$$\begin{aligned} P_1 &= 1/2\ Re\left\{\overline{V}_1 \overline{I}_{L1}^*\right\} \\ P_2 &= 1/2\ Re\left\{\overline{V}_2 \overline{I}_{L2}^*\right\} \end{aligned} \tag{8}$$

Note that such average powers do not take into account the inverter switching losses, the coils ferrite core losses and the post-regulator losses, since simplified FHA modeling do not allow for including such loss contributions. However, the above approach does enable the evaluation of the overall system behavior under different operating conditions of f_s and V_{2dc}, which are the two main parameters used herein to optimize the IPTS efficiency $\eta = P_2/P_1$.

2.3. Compensation Capacitors Selection

For a given TX and RX coil set, the IPTS power and efficiency levels depend on the selected values of the compensation capacitors C_1 and C_2, as highlighted by the IPTS modeling solution (5)–(8). Given the IPTS operating parameters and component values listed in Table 1, Equations (5)–(8) have been evaluated for V_{2dc} = 17 V, C_1 = {100, 200} nF and C_2 = {50, 100, 150, 200} nF. The IPT coil design resulting in the coil parameters of Table 1 will be subsequently described. Note that the analyzed IPTS has been herein designed to deliver an average output power of approximately 20 W at a regulated output voltage of 12 V to a resistive load of 7 Ω, but different output power levels are also feasible and will be tested in the experimental section of this paper. Figure 11 depicts the simulated IPTS efficiency η (Figure 11a), the primary coil rms current $I_{L1\text{rms}} = I_{L1}/\sqrt{2}$ (Figure 11b), and the normalized phase-shift $d = \alpha/\pi$ (Figure 11c,d)), for C_1 = 100 nF (solid lines) and C_1 = 200 nF (dashed lines). Note that only the TX coil rms current is shown in Figure 11b, since the RX coil current does not depend on the C_1, C_2 and f_s values. The plots of Figure 11c,d highlight the fact that the phase-shift changes with both C_1 and C_2, since it is dependent on the $\overline{V}_1$ solution in (6). The points with $d = 0$ represent unfeasible operating conditions for which the output voltage regulation cannot be achieved. The plots of Figure 11a,b show that η and $I_{1\text{rms}}$ levels only depend on C_2, while C_1 determines the operating ranges wherein the IPTS modeling solution is feasible ($\alpha \in [0, \pi]$ or $d \in [0, 1]$). The capacitor values C_1 = 100 nF and C_2 = 50 nF enable achieving the highest simulated efficiency (red solid curve in Figure 11a) at high frequencies, where the converters switching losses and the coils ferrite losses are likely to become high. For this reason, the optimal choice is C_2 = 100 nF (green curve) allowing to maximize the efficiency at ~120 kHz, with both C_1 = 100 nF and 200 nF.

Table 1. IPTS operating parameters and component values.

V_{in} (V)	V_o (V)	R_L (Ω)	L_1 (μH)	R_1 (mΩ)	L_2 (μH)	R_2 (mΩ)	M (μH)
24	12	7	23	67	23	64	12.2

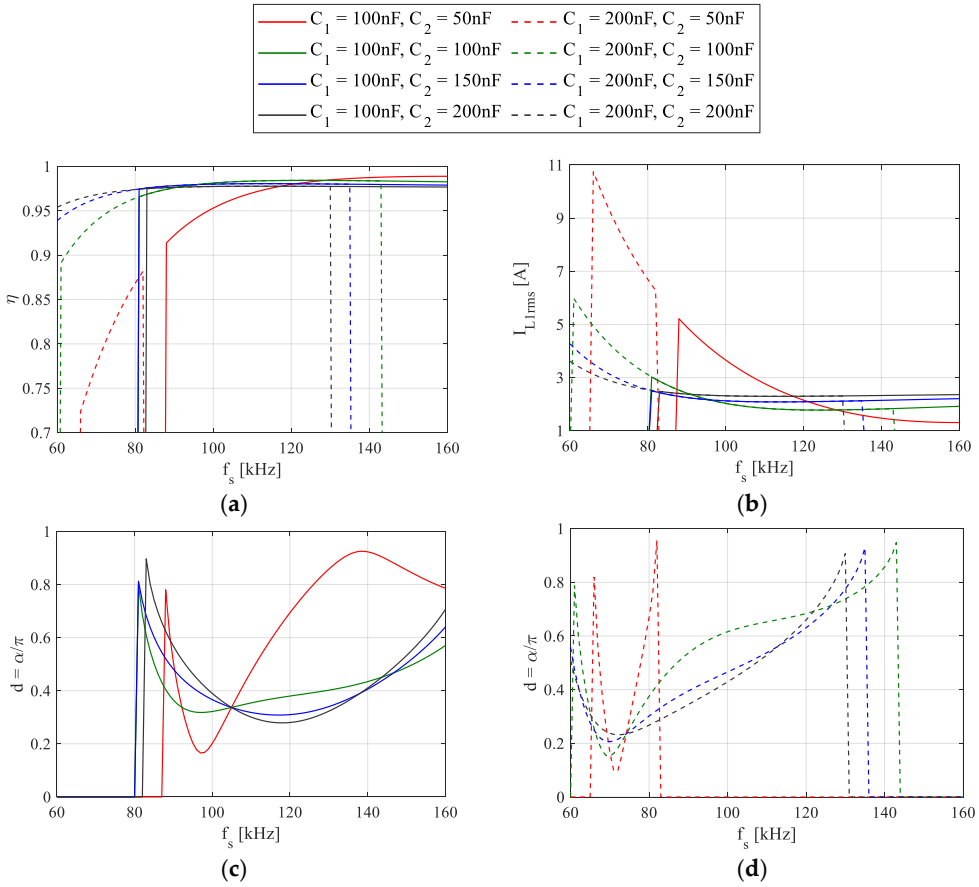


Figure 11. Predictions of IPTS modeling solution (5)–(8) vs. f_s, for different values of C_1 and C_2: (**a**) IPTS efficiency η; (**b**) primary coil rms current $I_{L1\text{rms}}$; (**c**) normalized phase-shift d for C_1 = 100 nF; (**d**) normalized phase-shift d for C_1 = 200 nF.

2.4. Static Modeling Results

Once the optimal compensation capacitor values have been selected, the IPTS modeling solution (5)–(8) has been evaluated over the ranges V_{2dc} = [14, 20] V and f_s = [60, 160] kHz, in order to determine the optimal parameter values maximizing the overall IPTS efficiency. Note that, in practice, a certain value of V_{2dc} can be achieved through the inverter phase-shift modulation (for a given value of f_s), either in an open-loop fashion or through the closed-loop feedback control. However, the latter would require a communication link between the IPT primary and secondary side; therefore, the open-loop strategy has been adopted herein.

Two different capacitor set-ups, identified as the optimal ones in the previous subsection, have been analyzed and compared: {C_1 = 100 nF, C_2 = 100 nF} and {C_1 = 200 nF, C_2 = 100 nF}. Figure 12 depicts the simulated IPTS efficiency η (Figure 12a), the rms currents $I_{L1\text{rms}}$ (solid lines) and $I_{L2\text{rms}}$ (dashed lines) of the TX and RX coil, respectively (Figure 12b), the IPT stage voltage gain V_2/V_1 (Figure 12c) and the normalized phase-shift d (Figure 12d), for the first capacitor set-up {C_1 = 100 nF, C_2 = 100 nF}. The plot of Figure 12a highlights that, for different frequencies, the simulated efficiency can be maximized at different levels of V_{2dc} (different line colors in the plots). For this set-up, the maximum value η_{max} = 0.9845 has been obtained at V_{2dc} = 15 V and f_s = 115 kHz. Figure 12b shows that the secondary coil rms current level (dashed lines) does not depend on the frequency, since it only depends on

V_{2dc} and R_{ac} values, as described by (6). Figure 12c highlights the fact that the IPTS voltage gain is independent of V_{2dc} (and hence of R_{ac}) at two split frequencies [28]:

$$f_L = \frac{1}{2\pi\sqrt{1-k^2}}\sqrt{\frac{\omega_1^2+\omega_2^2}{2} - \sqrt{\left(\frac{\omega_1^2-\omega_2^2}{2}\right)^2 + \omega_1^2\omega_2^2k^2}}$$
$$f_R = \frac{1}{2\pi\sqrt{1-k^2}}\sqrt{\frac{\omega_1^2+\omega_2^2}{2} + \sqrt{\left(\frac{\omega_1^2-\omega_2^2}{2}\right)^2 + \omega_1^2\omega_2^2k^2}} \quad (9)$$

where $\omega_1 = 2\pi f_1 = 1/\sqrt{L_1C_1}$ and $\omega_2 = 2\pi f_2 = 1/\sqrt{L_2C_2}$ are the primary and the secondary side angular resonant frequencies. For the capacitor set-up of Figure 12, the split frequencies are located in f_L = 85 kHz and f_R = 153 kHz. As will be explained in the next section, operating at the right-side split frequency f_R can be beneficial in terms of better controllability of the post-regulated IPTS, while maintaining high efficiency due to the ZVS inverter operation [31]. Finally, the blue rectangle in Figure 12d highlights a frequency region (from approximately 95 kHz to approximately 125 kHz) wherein the V_{2dc} voltage decreases as the normalized phase-shift d increases. This behavior could determine an instable operation region for the buck controller wherein the regulation of the buck output voltage could be lost, as will be explained hereafter. Hence, it could be impossible to exploit the maximum efficiency over such a frequency range, while operating the IPTS at higher frequencies could lead to decreased efficiency due to the increasing switching and ferrite losses.

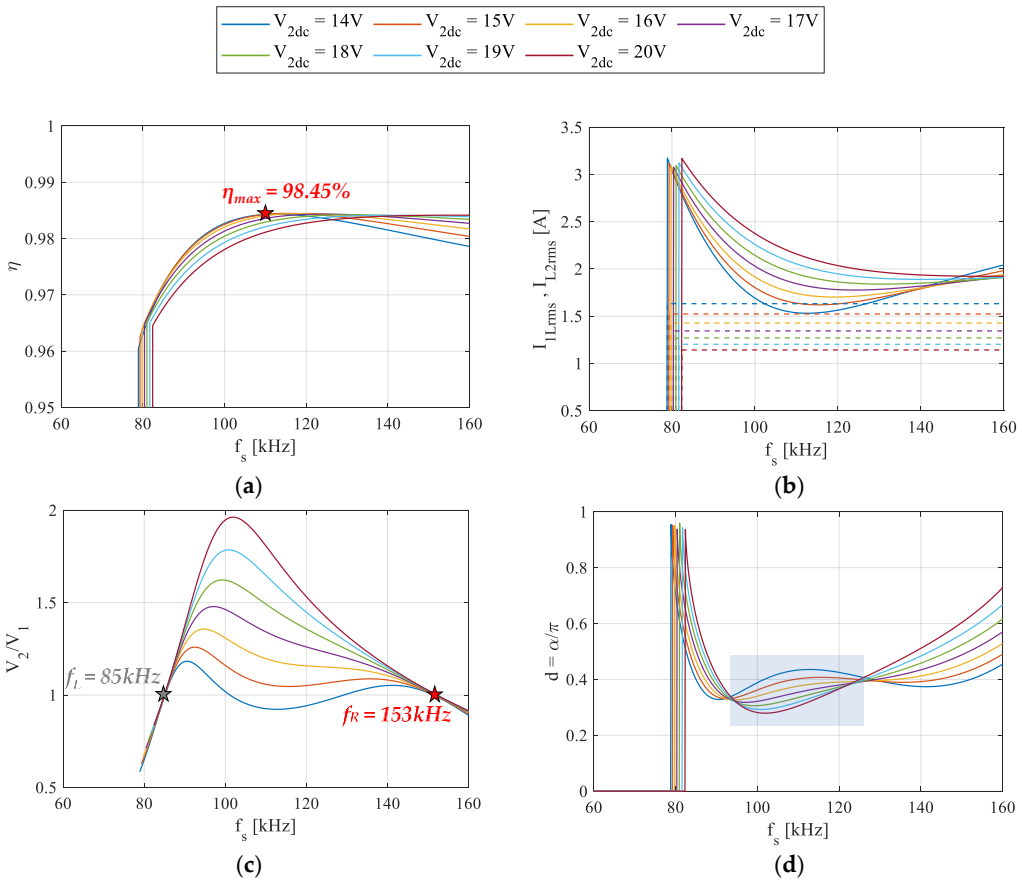


Figure 12. Predictions of IPTS modeling solution (5)–(8) vs. f_s for different values of V_{2dc}, for the capacitor set-up {C_1 = 100 nF, C_2 = 100 nF}: (**a**) IPTS efficiency η; (**b**) TX and RX coil rms currents $I_{L1\text{rms}}$ (solid), $I_{L2\text{rms}}$ (dashed); (**c**) IPTS RX-to-TX voltage gain V_2/V_1; and (**d**) normalized phase-shift d.

Figure 13 depicts the simulated IPTS efficiency η (Figure 13a), the rms currents $I_{L1\text{rms}}$ (solid lines) and the $I_{L2\text{rms}}$ (dashed lines) of the TX and RX coils, respectively (Figure 13b), the IPTS voltage gain V_2/V_1 (Figure 13c) and the normalized phase-shift d (Figure 13d), for the second capacitor set-up {C_1 = 200 nF, C_2 = 100 nF}. Also for this configuration, the maximum value η_{max} = 0.9845 has been obtained at V_{2dc} = 15 V and f_s = 115 kHz, since C_1 does not influence the maximum efficiency but the feasible frequency range over which such efficiency can be obtained. The split frequencies, for which the IPTS voltage gain is independent of the load, are now located in f_L = 68 kHz and f_R = 135 kHz. Again, the blue rectangle in Figure 13d highlights a frequency region (from approximately 70 kHz to approximately 100 kHz), wherein the V_{2dc} voltage decreases as the normalized phase-shift d increases, over which the buck controller could lose the capability of regulating the output voltage, as explained in the following section. However, compared to the capacitor set-up of Figure 12, now such a critical frequency region is shifted to the left, thus allowing to exploit the maximum efficiency operating conditions around the f_s = 115 kHz point. Hence, the optimal compensation capacitor set-up selected herein is {C_1 = 200 nF, C_2 = 100 nF}, resulting in the following values of the primary and secondary resonant frequencies f_1 = 74 kHz and f_2 = 105 kHz.

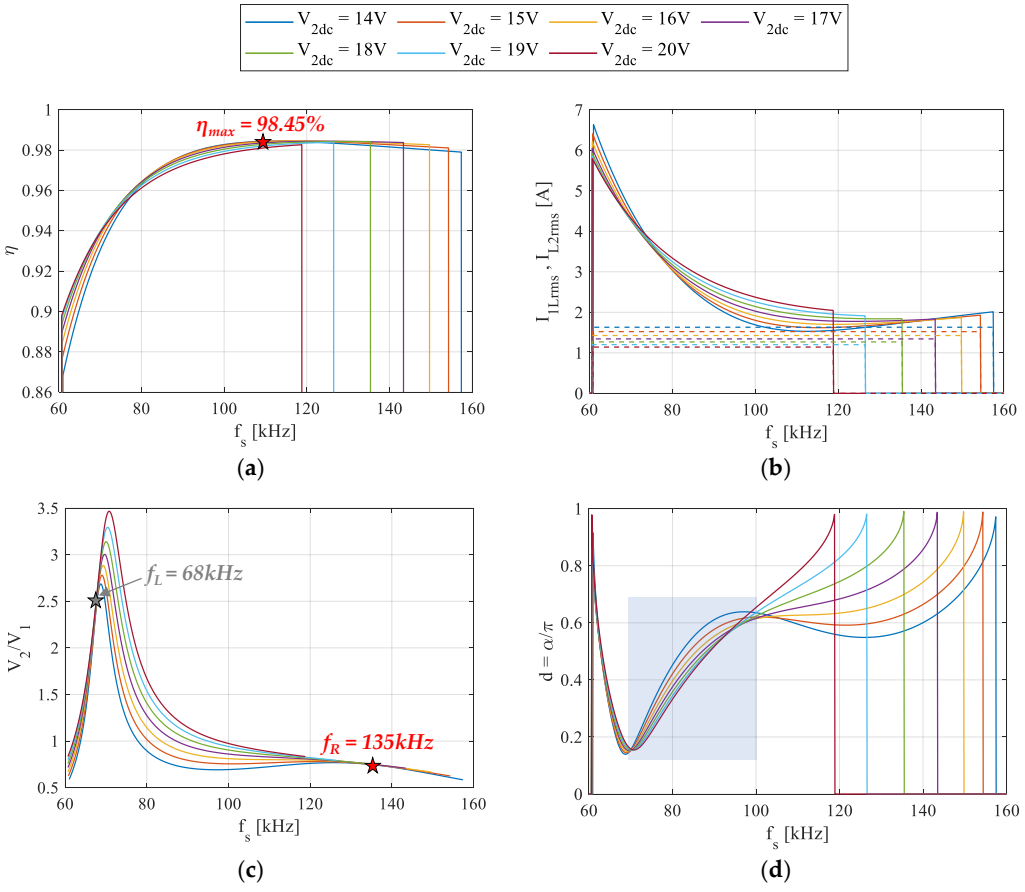


Figure 13. Predictions of IPTS modeling solution (5)–(8) vs. f_s for different values of V_{2dc}, for the capacitor set-up {C_1 = 200 nF, C_2 = 100 nF}: (**a**) IPTS efficiency η; (**b**) TX and RX coil rms currents $I_{L1\text{rms}}$ (solid), $I_{L2\text{rms}}$ (dashed); (**c**) IPTS RX-to-TX voltage gain V_2/V_1; and (**d**) normalized phase-shift d.

2.5. PR-IPTS Controllability Assessment

The modeling results presented in the previous section are based on the assumption that the buck converter correctly regulates its output voltage for all the analyzed conditions of the inverter switching frequency f_s and the intermediate bus voltage V_{2dc}. However, the control characteristics of a post-regulator cascaded to an IPTS are quite different from

a standalone DC/DC converter [28]. This is due to the fact that, as the post-regulator duty-cycle D increases, the equivalent resistance R_{ac} seen by the IPT stage decreases, and the intermediate bus voltage V_{2dc} can either increase or decrease in function of the IPTS response to the equivalent load variation. Hence, the converter output voltage $V_o = V_{2dc} \cdot M(D)$ can increase or decrease with the duty-cycle, in function of the amount of V_{2dc}· and $M(D)$ variation with D. Under certain operating conditions, the output voltage can become non-monotonic with respect to the duty-cycle, which means that the resulting Bode diagram varies significantly with the operating point. This may lead to difficulties in closed-loop control. In this section, we solve the PR-IPTS equations with the buck converter operating in open-loop and show that the non-monotonic behavior of the output voltage with duty-cycle occurs within the operating regions highlighted with blue rectangles in Figures 12d and 13d.

Let us assume that the PR-IPTS is operating in open loop with the buck duty-cycle varying in the range D = [0.1, 0.9]. The system equation (4) is still valid, but the output voltage V_o is no more regulated at its nominal value. The equivalent AC resistance R_{ac} seen at the rectifier input changes with the duty-cycle according to (1) and (3), thus varying the IPTS operating point. Let us also assume that the inverter normalized phase-shift d is varied in the range d = [0.1, 1]. For each value of d, the primary voltage peak V_1 is given by (2) and, if the phase ϕ_{V1} is taken as a zero reference for the phase angles, the phasor $\overline{V}_1 = V_1$ is known, and the equation system (4) can be solved to obtain the remaining phasors, as given in (10):

$$\begin{aligned} \overline{I}_{L1} &= \frac{\left(j\omega_s L_2 + \frac{1}{j\omega_s C_2} + R_2 + R_{ac}\right)}{\left(j\omega_s L_1 + \frac{1}{j\omega_s C_1} + R_1\right)\left(j\omega_s L_2 + \frac{1}{j\omega_s C_2} + R_2 + R_{ac}\right) + \omega_s^2 M^2} \overline{V}_1 \\ \overline{I}_{L2} &= -\frac{j\omega M}{\left(j\omega_s L_1 + \frac{1}{j\omega_s C_1} + R_1\right)\left(j\omega_s L_2 + \frac{1}{j\omega_s C_2} + R_2 + R_{ac}\right) + \omega_s^2 M^2} \overline{V}_1 \\ \overline{V}_2 &= \frac{j\omega M R_{ac}}{\left(j\omega_s L_1 + \frac{1}{j\omega_s C_1} + R_1\right)\left(j\omega_s L_2 + \frac{1}{j\omega_s C_2} + R_2 + R_{ac}\right) + \omega_s^2 M^2} \overline{V}_1 \end{aligned} \tag{10}$$

Starting from the result of (10), the voltage V_{2dc} can be estimated by inverting (5), and the resulting output voltage can be obtained for each analyzed value of D as $V_o = V_{2dc} \cdot D$. Figure 14 shows the values of V_o and V_{2dc} for the capacitor set-up {C_1 = 200 nF, C_2 = 100 nF}, obtained over the given ranges of D and d for f_s values in the interval [70, 135] kHz. It can be observed that at f_s = 70 kHz (Figure 14a), V_o is non-monotonic with respect to D, while V_{2dc} reaches very high levels for low duty-cycle values (high R_{ac}). Such a condition could result in an unstable controller behavior within the positive feedback region located at the right-hand-side of the V_o vs. D curve peak. In this region, an increase in D would result in a decrease in V_o, and the controller would try to further increase D until saturating its value at the maximum allowed limit. Hence, the output voltage regulation would be lost. Similarly, a decrease in D would cause an increase in V_o, and the controller would try to further decrease the duty-cycle, until reaching the V_o vs. D curve peak and going to the negative feedback region. In principle, in such a region the controller could be able to guarantee the output voltage regulation, but V_{2dc} may increase to very high levels, causing possible component failures (such as capacitors, buck converter MOSFETs and relative gate drivers, etc.). Hence, the system operation under conditions resulting in a non-monotonic control-to-output characteristic should be avoided. At f_s = 90 kHz (Figure 14b), V_o is still non-monotonic with respect to D but V_{2dc} assumes lower values, while at f_s = 110 kHz (Figure 14c), V_o becomes monotonic resulting in a correct controller behavior. These findings are in agreement with the results of Figure 13d, where the IPTS operation in the range [70, 100] kHz is not recommended because of the inversion of the V_{2dc} vs. d trend. Eventually, the plots of Figure 14d depict V_o and V_{2dc} for f_s = 135 kHz (corresponding to the right-hand-side split frequency f_R), highlighting that V_{2dc} (and consequently, the IPTS gain V_2/V_1) is independent of the duty-cycle D (or, equivalently, of R_{ac}), which is in agreement with the results of Figure 13c. Hence, operating IPTS at f_R can be convenient if the load variations occur, but the overall system efficiency may decrease somewhat (as can be seen

in Figure 13a). To maximize the efficiency, IPTS should be operated at f_s = 115 kHz, which is still a feasible condition located in the stable frequency region, as previously shown in Figure 13d.

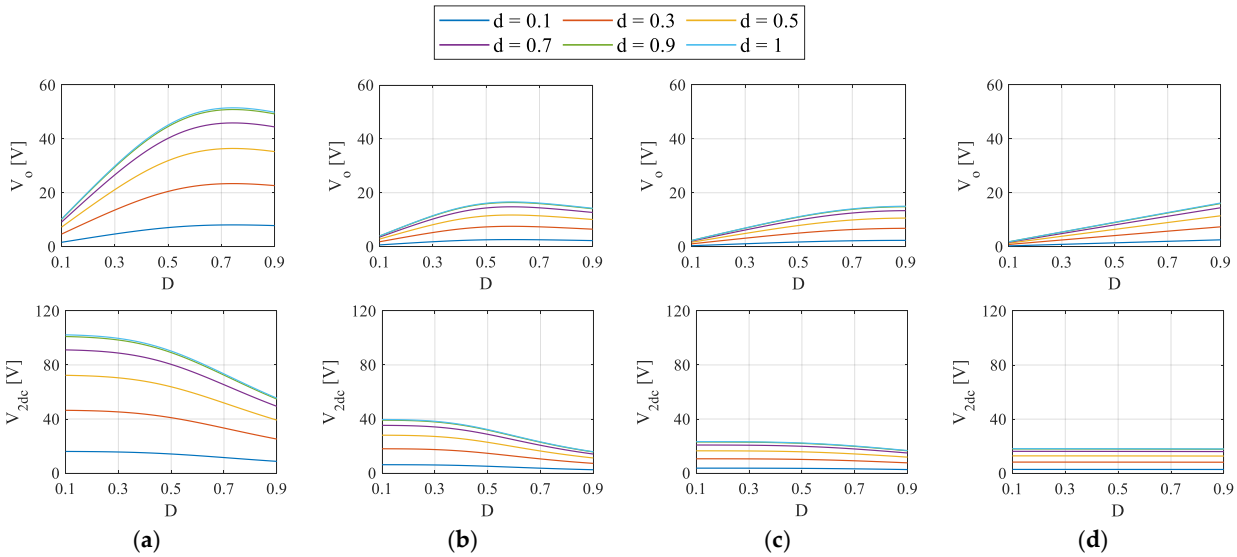


Figure 14. PR-IPTS output voltage V_o (top) and intermediate bus voltage V_{2dc} (bottom) vs. buck duty-cycle D for different values of normalized phase-shift d at: (**a**) f_s = 70 kHz; (**b**) f_s = 90 kHz; (**c**) f_s = 110 kHz; and (**d**) f_s = 135 kHz.

3. Dynamic Modeling and Control of PR-IPTS

In this section, we describe the dynamic modeling of the PR-IPTS based on CMT, similarly to the research developed in [27]. In contrast to the findings of [27], which are valid for a full square-wave inverter operation under resonance conditions, we propose the modified modeling including the inverter phase-shift modulation which is valid for whatever switching frequency. As one of the modeling outputs, we obtained the duty-to-output transfer function of the post-regulator, necessary for the design of the digital controller as discussed hereafter.

3.1. Dynamic Modeling of IPT Stage

Figure 15 shows the AC equivalent circuit of the IPT stage of Figure 9, where v_1 and v_2 are considered to be the exciting source and sink, respectively. The dynamics of such an equivalent circuit can be described by the equation system (11):

$$\begin{cases} L_1\frac{di_{L1}}{dt} + M\frac{di_{L2}}{dt} + R_1 i_{L1} + v_{C1} = v_1 \\ L_2\frac{di_{L2}}{dt} + M\frac{di_{L1}}{dt} + R_2 i_{L2} + v_{C2} = v_2 \\ C_1\frac{dv_{C1}}{dt} = i_{L1} \\ C_2\frac{dv_{C2}}{dt} = i_{L2} \end{cases} \tag{11}$$

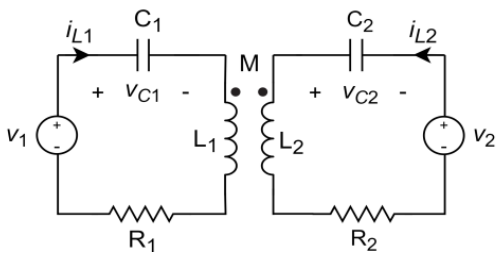


Figure 15. AC equivalent circuit of the IPT stage.

As a result of the phase-shift modulation (see Figure 10), the inverter output voltage $v_1(t)$ can be described by (12):

$$v_1(t) = \begin{cases} v_{in}\,, & -\frac{\alpha}{2} \le \omega_s t < \frac{\alpha}{2} \\ 0, & \frac{\alpha}{2} \le \omega_s t < \pi - \frac{\alpha}{2} \\ -v_{in}, & \pi - \frac{\alpha}{2} \le \omega_s t < \pi + \frac{\alpha}{2} \end{cases} \tag{12}$$

The rectifier input voltage $v_2(t)$ is determined by the secondary coil current direction:

$$v_2(t) = -sgn(i_{L2}(t))v_{2dc} \tag{13}$$

According to the CMT, the IPT coil currents $i_{Ln}(t)$ and the compensation capacitor voltages $v_{Cn}(t)$ (n = 1, 2) can be represented as given in (14):

$$\begin{cases} i_{Ln}(t) = \sqrt{\frac{2}{L_n}} a_n \cos(\omega_s t + \theta_n) & (14a) \\ v_{Cn}(t) = \frac{1}{\omega_s C_n}\sqrt{\frac{2}{L_n}} a_n \sin(\omega_s t + \theta_n) & (14b) \end{cases}$$

where a_n and θ_n are the amplitudes and phases of the coupled modes representing the state of the primary and secondary resonators. Such variables are assumed to vary slowly with time. Let us note that (14b) has been modified compared to the formulation given in [27], so as to extend its validity to whatever operating frequency. Using (14), the derivatives of the resonant voltages and currents become:

$$\begin{cases} \frac{di_{Ln}}{dt} = \sqrt{\frac{2}{L_n}}\left[\frac{da_n}{dt}\cos(\omega_s t + \theta_n) - a_n\left(\omega_s + \frac{d\theta_n}{dt}\right) sin(\omega_s t + \theta_n)\right] \\ \frac{dv_{Cn}}{dt} = \sqrt{\frac{2}{C_n}}\left[\frac{da_n}{dt}\sin(\omega_s t + \theta_n) + a_n\left(\omega_s + \frac{d\theta_n}{dt}\right) cos(\omega_s t + \theta_n)\right] \end{cases} \tag{15}$$

By substituting (15) into (11), it is possible to derive the dynamic equations of the amplitudes and phases of the coupled modes:

$$\begin{aligned} \frac{da_1}{dt} = {} & \omega_1 a_1 sin(\omega_s t + \theta_1) cos(\omega_s t + \theta_1) + \\ & + \frac{\sqrt{L_1/2}}{(L_1L_2 - M^2)} \cos(\omega_s t + \theta_1)\left[-\frac{L_2}{\omega_s C_1}\sqrt{\frac{2}{L_1}} a_1 sin(\omega_s t + \theta_1) + \right. \\ & - L_2 R_1 \sqrt{\frac{2}{L_1}} a_1 cos(\omega_s t + \theta_1) + L_2 v_1(t) - M v_2(t) + \\ & \left. + MR_2\sqrt{\frac{2}{L_2}} a_2 cos(\omega_s t + \theta_2) + \frac{M}{\omega_s C_2}\sqrt{\frac{2}{L_2}} a_2 sin(\omega_s t + \theta_2)\right] \end{aligned} \tag{16a}$$

$$\begin{aligned} \frac{d\theta_1}{dt} = {} & -\omega_s + \omega_1 - \omega_1 \sin^2(\omega_s t + \theta_1) + \\ & - \frac{\sqrt{L_1/2}}{(L_1L_2 - M^2)} \frac{sin(\omega_s t + \theta_1)}{a_1}\left[-\frac{L_2}{\omega_s C_1}\sqrt{\frac{2}{L_1}} a_1 sin(\omega_s t + \theta_1) + \right. \\ & - L_2 R_1 \sqrt{\frac{2}{L_1}} a_1 cos(\omega_s t + \theta_1) + L_2 v_1(t) - M v_2(t) + \\ & \left. + MR_2\sqrt{\frac{2}{L_2}} a_2 cos(\omega_s t + \theta_2) + \frac{M}{\omega_s C_2}\sqrt{\frac{2}{L_2}} a_2 sin(\omega_s t + \theta_2)\right] \end{aligned} \tag{16b}$$

$$\begin{aligned} \frac{da_2}{dt} = {} & \omega_2 a_2 sin(\omega_s t + \theta_2) cos(\omega_s t + \theta_2) + \\ & + \frac{\sqrt{L_2/2}}{(L_1L_2 - M^2)} \cos(\omega_s t + \theta_2)\left[-\frac{L_1}{\omega_s C_2}\sqrt{\frac{2}{L_2}} a_2 sin(\omega_s t + \theta_2) + \right. \\ & + L_1 v_2(t) - M v_1(t) + \\ & \left. + MR_1\sqrt{\frac{2}{L_1}} a_1 cos(\omega_s t + \theta_1) + \frac{M}{\omega_s C_1}\sqrt{\frac{2}{L_1}} a_1 sin(\omega_s t + \theta_1)\right] \end{aligned} \tag{16c}$$

$$\begin{aligned} \frac{d\theta_2}{dt} = {} & -\omega_s + \omega_2 - \omega_2 \sin^2(\omega_s t + \theta_2) + \\ & - \frac{\sqrt{L_2/2}}{(L_1L_2 - M^2)} \frac{\sin(\omega_s t + \theta_2)}{a_2}\left[-\frac{L_1}{\omega_s C_2}\sqrt{\frac{2}{L_2}} a_2 sin(\omega_s t + \theta_2) + \right. \\ & - L_1 R_2 \sqrt{\frac{2}{L_2}} a_2 cos(\omega_s t + \theta_2) + L_1 v_2(t) - M v_1(t) + \\ & \left. + MR_1\sqrt{\frac{2}{L_1}} a_1 cos(\omega_s t + \theta_1) + \frac{M}{\omega_s C_1}\sqrt{\frac{2}{L_1}} a_1 sin(\omega_s t + \theta_1)\right] \end{aligned} \tag{16d}$$

Note that (12) and (13) should be used in (16) to describe $v_1(t)$ and $v_2(t)$, respectively. Assuming that the slowly varying variables in (16)—a_n and θ_n (n = 1, 2)—are constant during a buck switching period $T_{Buck} = 1/f_{Buck}$, the time-invariant averaged model can be obtained by taking the average values of both sides of (16) over T_{Buck}:

$$\left\langle \frac{da_1}{dt} \right\rangle = \frac{\sqrt{L_1/2}}{(L_1L_2-M^2)}\left[-\frac{L_2R_1}{\sqrt{2L_1}}a_1 - \frac{M}{\omega_s C_2\sqrt{2L_2}}a_2 sin(\theta_1-\theta_2) + \right. \\ \left. + \frac{MR_2}{\sqrt{2L_2}}a_2 cos(\theta_1-\theta_2) + \frac{2L_2v_{in}}{\pi}\cos(\theta_1)\sin\left(\frac{\alpha}{2}\right) + \frac{2M}{\pi}v_{2dc}\cos(\theta_1-\theta_2)\right] \tag{17a}$$

$$\left\langle \frac{d\theta_1}{dt} \right\rangle = -\omega_s + \frac{\omega_1}{2} - \frac{\sqrt{L_1/2}}{(L_1L_2-M^2)a_1}\left[-\frac{L_2}{\omega_s C_1\sqrt{2L_1}}a_1 + \frac{M}{\omega_s C_2\sqrt{2L_2}}a_2\cos(\theta_1-\theta_2) + \right. \\ \left. + \frac{MR_2}{\sqrt{2L_2}}a_2\sin(\theta_1-\theta_2) + \frac{2L_2v_{in}}{\pi}\sin(\theta_1)\sin\left(\frac{\alpha}{2}\right) + \frac{2M}{\pi}v_{2dc}\sin(\theta_1-\theta_2)\right] \tag{17b}$$

$$\left\langle \frac{da_2}{dt} \right\rangle = \frac{\sqrt{L_2/2}}{(L_1L_2-M^2)}\left[-\frac{L_1R_2}{\sqrt{2L_2}}a_2 + \frac{M}{\omega_s C_1\sqrt{2L_1}}a_1 sin(\theta_1-\theta_2) + \right. \\ \left. + \frac{MR_1}{\sqrt{2L_1}}a_1 cos(\theta_1-\theta_2) - \frac{2L_1v_{2dc}}{\pi} - \frac{2Mv_{in}}{\pi}\cos(\theta_2)\sin\left(\frac{\alpha}{2}\right)\right] \tag{17c}$$

$$\left\langle \frac{d\theta_2}{dt} \right\rangle = -\omega_s + \frac{\omega_2}{2} - \frac{\sqrt{L_2/2}}{(L_1L_2-M^2)a_2}\left[-\frac{L_1}{\omega_s C_2\sqrt{2L_2}}a_2 + \frac{M}{\omega_s C_1\sqrt{2L_1}}a_1\cos(\theta_1-\theta_2) + \right. \\ \left. - \frac{MR_1}{\sqrt{2L_1}}a_1\sin(\theta_1-\theta_2) - \frac{2Mv_{in}}{\pi}\sin(\theta_2)\sin\left(\frac{\alpha}{2}\right)\right] \tag{17d}$$

while the "$\langle\cdot\rangle$" operator denotes the averaged values of the relevant quantities over T_{Buck}. The averaged model (17) can be represented in a more compact form (18):

$$\frac{d\boldsymbol{x}}{dt} = \boldsymbol{f}(x, v_{in}, v_{2dc}) \tag{18}$$

where:

$$\boldsymbol{x} = [a_1 \;\; \theta_1 \;\; a_2 \;\; \theta_2]^T, \quad \boldsymbol{f} = [f_1 \;\; f_2 \;\; f_3 \;\; f_4]^T \tag{19}$$

and f_n (n = 1, . . . , 4) is the right-hand-side expression of the n-th equation in (17). The averaged value over T_{Buck} of the current at the diode bridge output is given by (20):

$$\langle i_2 \rangle = g_2(\boldsymbol{x}) = -\frac{1}{\pi}\sqrt{\frac{2}{L_2}}a_2 \tag{20}$$

Denoting the small-signal variations of the state variables and of the IPT input and output voltages as $\hat{a}_n$, $\hat{\theta}_n$ and $\hat{v}_n$ (n = 1, 2), the linearized small-signal model of the IPT stage can be described by (21):

$$\frac{d\hat{\boldsymbol{x}}}{dt} = \boldsymbol{F_x}\hat{\boldsymbol{x}} + \begin{bmatrix} \dfrac{\partial \boldsymbol{f}}{\partial v_{in}} & \dfrac{\partial \boldsymbol{f}}{\partial v_{2dc}} \end{bmatrix}\begin{bmatrix} \hat{v}_{in} \\ \hat{v}_{2dc} \end{bmatrix} \tag{21}$$

where:

$$\hat{\boldsymbol{x}} = \begin{bmatrix} \hat{a}_1 \\ \hat{\theta}_1 \\ \hat{a}_2 \\ \hat{\theta}_2 \end{bmatrix}, \; \boldsymbol{F_x} = \begin{bmatrix} \frac{\partial f_1}{\partial a_1} & \frac{\partial f_1}{\partial \theta_1} & \frac{\partial f_1}{\partial a_2} & \frac{\partial f_1}{\partial \theta_2} \\ \frac{\partial f_2}{\partial a_1} & \frac{\partial f_2}{\partial \theta_1} & \frac{\partial f_2}{\partial a_2} & \frac{\partial f_2}{\partial \theta_2} \\ \frac{\partial f_3}{\partial a_1} & \frac{\partial f_3}{\partial \theta_1} & \frac{\partial f_3}{\partial a_2} & \frac{\partial f_3}{\partial \theta_2} \\ \frac{\partial f_4}{\partial a_1} & \frac{\partial f_4}{\partial \theta_1} & \frac{\partial f_4}{\partial a_2} & \frac{\partial f_4}{\partial \theta_2} \end{bmatrix} \tag{22}$$

According to (20), the small signal variation of the IPT stage output current is:

$$\hat{i}_2 = \nabla g_2 \hat{x}, \quad \nabla g_2 = \begin{bmatrix} \dfrac{\partial g_2}{\partial a_1} & \dfrac{\partial g_2}{\partial \theta_1} & \dfrac{\partial g_2}{\partial a_2} & \dfrac{\partial g_2}{\partial \theta_2} \end{bmatrix} \tag{23}$$

3.2. Small-Signal Modeling of PR-IPTS

Using the IPTS dynamic model presented thus far, it is possible to develop a system-level PR-IPTS model by combining Equations (18)–(23) with the differential equations of the post-regulator. Figure 16 depicts an averaged small-signal equivalent circuit of the

buck converter, where the PWM switching cell is replaced with an equivalent two-port AC model described by (24):

$$\hat{i}_x = D \cdot \hat{i}_L + I_L \cdot \hat{d} \tag{24a}$$

$$\hat{v}_y = D \cdot \hat{v}_{2dc} + V_{2dc} \cdot \hat{d} \tag{24b}$$

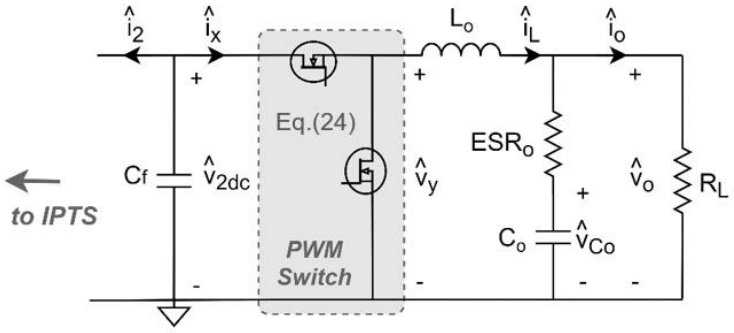


Figure 16. Averaged small-signal equivalent circuit of the buck converter.

The "^" operator in (24) denotes the small-signal variations of the considered quantities (note that the duty-cycle variation $\hat{d}$ is different from the normalized phase-shift d used previously).

The small-signal variation of the buck output voltage can be described by (25):

$$\hat{v}_o = ESR_o \left(\hat{i}_L - \frac{\hat{v}_o}{R_L} \right) + \hat{v}_{Co} \tag{25}$$

which yields (26):

$$\hat{v}_o = \frac{R_L ESR_o}{R_L + ESR_o} \hat{i}_L + \frac{R_L}{R_L + ESR_o} \hat{v}_{Co} \tag{26}$$

Using (23) and (24a), the dynamic equation of the intermediate bus capacitor C_f can be expressed as given in (27):

$$\frac{d\hat{v}_{2dc}}{dt} = -\frac{1}{C_f} \left(\hat{i}_2 + \hat{i}_x \right) = -\frac{\nabla g_2}{C_f} \hat{\mathbf{x}} - \frac{D}{C_f} \hat{i}_L - \frac{I_L}{C_f} \hat{d} \tag{27}$$

Using (26), the dynamic equation of the buck output capacitor C_o can be expressed as given in (28):

$$\frac{d\hat{v}_{Co}}{dt} = \frac{1}{C_o} \left(\hat{i}_L - \frac{\hat{v}_o}{R_L} \right) = \frac{R_L}{(R_L + ESR_o) C_o} \hat{i}_L - \frac{1}{(R_L + ESR_o) C_o} \hat{v}_{Co} \tag{28}$$

Using (24b) and (27), the dynamic equation of the buck inductor L_o can be obtained:

$$\frac{d\hat{i}_L}{dt} = \frac{1}{L_o} \left(\hat{v}_y - \hat{v}_o \right) = \frac{D}{L_o} \hat{v}_{2dc} + \frac{V_{2dc}}{L_o} \hat{d} - \frac{R_L ESR_o}{(R_L + ESR_o) L_o} \hat{i}_L - \frac{R_L}{(R_L + ESR_o) L_o} \hat{v}_{Co} \tag{29}$$

By combining the IPTS dynamic model (21) with Equations (26)–(29), the seventh-order small-signal model of the PR-IPTS is developed:

$$\underbrace{\frac{d}{dt}\begin{bmatrix}\hat{x}\\ \hat{v}_{2dc}\\ \hat{i}_L\\ \hat{v}_{Co}\end{bmatrix}}_{\dot{\hat{X}}}=\underbrace{\begin{bmatrix}\boldsymbol{F_x} & \frac{\partial f}{\partial v_{2dc}} & \mathbf{0} & \mathbf{0}\\ -\frac{\nabla g_2}{C_f} & 0 & -\frac{D}{C_f} & 0\\ \mathbf{0} & \frac{D}{L} & k_1 & k_2\\ \mathbf{0} & 0 & k_3 & k_4\end{bmatrix}}_{\boldsymbol{A}}\begin{bmatrix}\hat{x}\\ \hat{v}_{2dc}\\ \hat{i}_L\\ \hat{v}_{Co}\end{bmatrix}+\underbrace{\begin{bmatrix}\mathbf{0}\\ -\frac{I_L}{C_f}\\ \frac{V_{2dc}}{L}\\ 0\end{bmatrix}}_{\boldsymbol{B}}\hat{d}$$
$$\hat{v}_o=\underbrace{\begin{bmatrix}\mathbf{0} & 0 & k_5 & k_6\end{bmatrix}}_{\boldsymbol{C}}\begin{bmatrix}\hat{x}\\ \hat{v}_{2dc}\\ \hat{i}_L\\ \hat{v}_{Co}\end{bmatrix} \tag{30}$$

where:

$$\begin{gathered}k_1=-\frac{R_L ESR_o}{(R_L+ESR_o)L_o},\quad k_2=-\frac{R_L}{(R_L+ESR_o)L_o},\quad k_3=\frac{R_L}{(R_L+ESR_o)C_o},\\ k_4=-\frac{1}{(R_L+ESR_o)C_o},\quad k_5=\frac{R_L ESR_o}{R_L+ESR_o},\quad k_6=\frac{R_L}{R_L+ESR_o}\end{gathered} \tag{31}$$

Note that in (30), the IPTS input voltage is considered constant with time ($\hat{v}_{in}=0$). From (30), the state-space solution of the system can be obtained as

$$\hat{\boldsymbol{X}}=(s\boldsymbol{I}-\boldsymbol{A})^{-1}\boldsymbol{B}\hat{d} \tag{32a}$$

$$\hat{v}_o=\boldsymbol{C}(s\boldsymbol{I}-\boldsymbol{A})^{-1}\boldsymbol{B}\hat{d} \tag{32b}$$

The steady-state operating point of the IPT stage, needed to evaluate (32), can be obtained from the FHA modeling solution (6) presented in the previous section, according to (33):

$$a_1=I_{L1}\sqrt{\frac{L_1}{2}},\quad a_2=I_{L2}\sqrt{\frac{L_2}{2}},\quad \theta_1=\phi_{IL1}-\phi_{V1},\quad \theta_2=\phi_{IL2}-\phi_{V1} \tag{33}$$

where I_{L1}, I_{L2}, ϕ_{IL1} and ϕ_{IL2} are the amplitudes and phases of the primary and secondary current phasors $\overline{I}_{L1}$ and $\overline{I}_{L2}$ in (6). Let us note that, to evaluate the phase angles θ_1 and θ_2, all the phase angles obtained from (6) should be decremented by ϕ_{V1} (i.e., the phase of the primary voltage phasor $\overline{V}_1$), since in the CMT formulation such ϕ_{V1} term is considered null. Equation (32b) allows to evaluate the duty-to-output transfer function of the buck converter connected to the IPTS:

$$G_{vd}(s)=\frac{\hat{v}_o}{\hat{d}}=\boldsymbol{C}(s\boldsymbol{I}-\boldsymbol{A})^{-1}\boldsymbol{B} \tag{34}$$

As previously discussed, under certain operating conditions, the buck output voltage can become non-monotonic with respect to the duty-cycle, leading to difficulties in the closed-loop control. Figure 17 depicts the Bode plot of $G_{vd}(s)$ for the operating point {f_s = 70 kHz, V_{2dc} = 14 V} located in the unstable region highlighted in Figure 13d, for the buck parameters listed in Table 2. Indeed, the resulting phase of $G_{vd}(s)$ is close to $-180°$ at low frequencies, because of the negative static gain G_{vd0}. This means that the increase in the duty-cycle will lead to the decrease in the output voltage, which is in agreement with the plot of Figure 14a highlighting a non-monotonic V_o vs. D static characteristic. Figure 18 depicts the Bode plot of $G_{vd}(s)$ for the operating point {f_s = 110 kHz, V_{2dc} = 14 V} located in the stable region of Figure 13d. Under such conditions, the static gain G_{vd0} is positive, and the V_o vs. D static characteristic is monotonic (see Figure 14c). Hence, this last operating point is feasible for the practical controller design discussed hereafter.

Table 2. Buck converter parameters.

V_{2dc} (V)	V_o (V)	f_{Buck} (kHz)	R_L (Ω)	L_o (μH)	C_o (μF)	ESR_o (mΩ)	C_f (μF)
14	12	100	7	22	440	5	2068

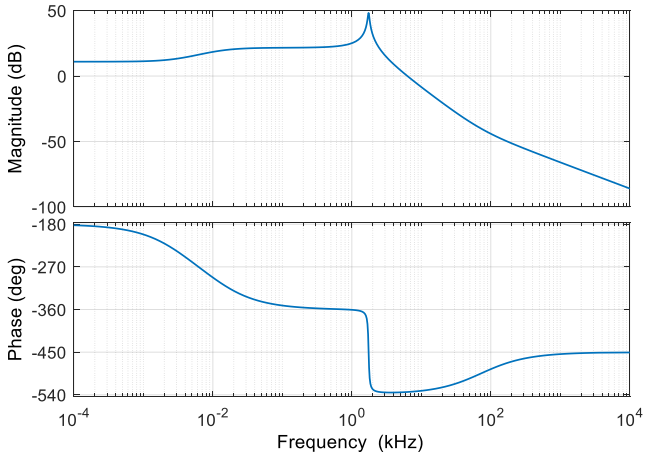


Figure 17. Bode plots of $G_{vd}(s)$ for $\{f_s = 70$ kHz, $V_{2dc} = 14$ V$\}$.

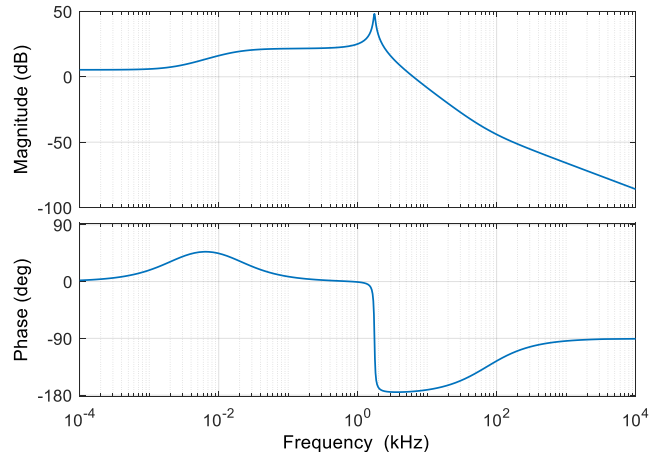


Figure 18. Bode plots of $G_{vd}(s)$ for $\{f_s = 110$ kHz, $V_{2dc} = 14$ V$\}$.

3.3. Digital Voltage Mode Control Design of Post-Regulator

To achieve the buck output voltage regulation, a Digital Voltage Mode Control (DVMC) has been adopted, whose functional schematic is shown in Figure 19. The output voltage $v_o(t)$ is scaled down by means of the resistive sensor H_V and sampled by the ADC, yielding the feedback voltage $v_{fb}[n]$ in the n-th sampling instant. Such a voltage value is then compared with the digital reference V_{ref}, and the resulting error $e[n]$ is sent to the digital controller which calculates the desired control voltage value $v_c[n]$. The output of the controller is delivered to the Digital Pulse Width Modulator (DPWM) which generates the two complementary driving signals for the buck converter MOSFETs.

To properly design the DVMC, the analog version of the controller has been first developed and subsequently transformed into its digital version. The block diagram representation of the analog VMC is shown in Figure 20, which utilizes a single feedback loop to regulate the output voltage at the desired reference value. The blue box represents the dynamic model of the buck converter including its main transfer functions. The control-to-output transfer function $G_{vd}(s)$ is provided in (34), while the transfer functions $G_{vi}(s)$ and $Z_o(s)$ can be obtained through the same modeling procedure. The block $G_{pwm} = 1/V_{pp}$

represents the PWM gain, where V_{pp} is the peak-to-peak amplitude of the PWM sawtooth signal (herein, V_{pp} = 1 V has been used).

The analog controller $G_{va}(s)$ has been designed by the K-factor method [32], to obtain a given phase margin of the compensated loop transfer function $T_c(s) = G_{va}(s) \cdot G_{pwm} \cdot G_{vd}(s)$ at the desired crossover frequency, ensuring the closed-loop system stability.

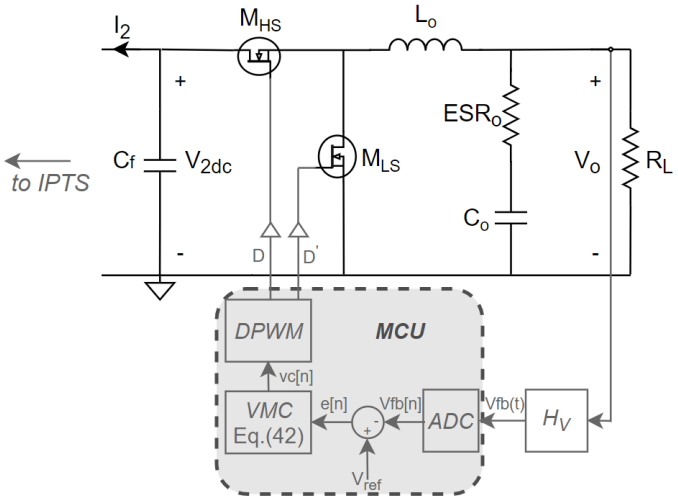


Figure 19. DVMC of the buck converter.

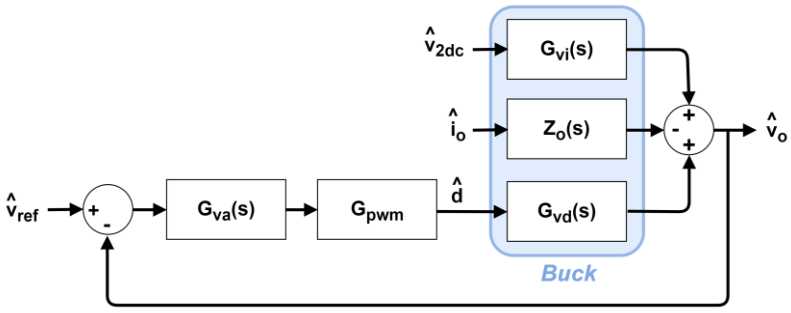


Figure 20. Analog VMC block diagram.

Referring to the duty-to-output transfer function of Figure 18, a crossover frequency of $f_{Buck}/20$ = 5 kHz and a phase margin of 52° have been set, yielding the third-order controller (35) whose coefficients are listed in Table 3:

$$G_{va}(s) = \frac{\omega_{p1}}{s} \frac{(1 + s/\omega_{z1})^2}{(1 + s/\omega_{p2})^2} \tag{35}$$

Table 3. Analog controller coefficients.

ω_{z1} (rad/s)	ω_{p1} (rad/s)	ω_{p2} (rad/s)
5.99×10^3	683.86	1.65×10^5

To obtain the digital version of such a controller, the Tustin transform (36) has been adopted:

$$s = 2 f_{samp} \frac{(1 - z^{-1})}{(1 + z^{-1})} \tag{36}$$

where the sampling frequency f_{samp} has been set equal to the buck switching frequency f_{Buck}, so as to synchronize the sampling process with respect to the switching of the converter.

Substituting (36) into (35) provides the digital controller transfer function $G_{va}(z)$ given in (37), whose coefficients are listed in Table 4:

$$G_{va}(z) = K_p \frac{b_0 + b_1 z^{-1} + b_2 z^{-2} + b_3 z^{-3}}{1 - a_1 z^{-1} - a_2 z^{-2} - a_3 z^{-3}} \tag{37}$$

where K_p is a scaling factor allowing to adapt the ADC resolution res_{ADC} to the DPWM resolution res_{DPWM} [33]:

$$K_p = \frac{res_{ADC}}{H_V} \frac{1}{res_{DPWM}} \tag{38}$$

Table 4. Digital controller coefficients.

a_1	a_2	a_3	
1.193312123257	−0.202654517506	0.009342394250	
b_0	b_1	b_2	b_3
0.824716092259	−0.728775227352	−0.821925844304	0.731565475307

The ADC resolution is determined by the ADC full-scale value V_{FS} and by the number of bits used for the quantization N_{bit}:

$$res_{ADC} = \frac{V_{FS}}{2^{N_{bit}} - 1} \tag{39}$$

The DPWM resolution is determined by the number of discrete DPWM levels N_{DPWM}:

$$res_{DPWM} = \frac{1}{N_{DPWM}} \tag{40}$$

where N_{DPWM} is determined by a fixed time resolution t_{res} of the DPWM peripheral and by the desired buck switching frequency f_{Buck} according to (41):

$$N_{DPWM} = \frac{1}{f_{Buck} t_{res}} - 1 \tag{41}$$

where an edge-aligned mode of the DPWM peripheral has been adopted, which allows realizing a desired PWM period by counting from zero up to the N_{DPWM} level and then starting a new period.

Applying the inverse Z-transform to (37) yields the digital control law (42):

$$\begin{aligned} v_c[n] = {} & a_1 v_c[n-1] + a_2 v_c[n-2] + a_3 v_c[n-3] + K_p b_0 e[n] \\ & + K_p b_1 e[n-1] + K_p b_2 e[n-2] + K_p b_3 e[n-3] \end{aligned} \tag{42}$$

Due to the sampling process, the sampled output voltage shows an additive delay, equal to half the sampling period, as compared to the original signal, which may lead to the phase margin erosion of the compensated loop gain $T_c(s)$ that can affect the system stability. Figure 21 shows the impact of the sampling delay on the Bode plots of $T_c(s)$, highlighting that the desired phase margin $Pm = 52°$ of $T_c(s)$ (blue curves) is decreased to $Pm = 43°$ in the delayed version of $T_c(s)$ (red curves). Nevertheless, the closed-loop system stability is still ensured with the acceptable values of both gain and phase margins.

Eventually, the absence of the limit cycle phenomenon has been verified for the proposed DPWM scheme. Limit cycles refer to the steady-state oscillations of $v_o(t)$ and other system variables at frequencies lower than the converter switching frequency, which may result from the presence of signal amplitude quantizers such as the ADC and DPWM modules in the feedback loop [34]. Referring to Figure 19, for a given duty-to-output DC gain G_{vd0}, the duty-to-feedback voltage DC gain is $G_{vd0}\, H_V$. To prevent limit cycles, the change of the feedback voltage $\Delta V_{fb}(t)$ determined by the minimum duty-cycle change

ΔD_{min} (corresponding to the DPWM resolution res_{DPWM}) has to be smaller than ADC resolution res_{ADC}:

$$\Delta D_{min} G_{vd0} H_V < res_{ADC} \tag{43}$$

The static gain G_{vd0} has been estimated by substituting $s = 0$ in (34). For the presented controller design, the aforementioned parameter values are listed in Table 5. Substituting such values into (43), the absence of the limit cycle has been ascertained. It is worth mentioning that the presence of the IPTS connected to the buck input has caused the static gain reduction as compared to the stand-alone buck regulator for which G_{vd0} is equal to the converter input voltage (herein V_{in} = 14 V). This helped prevent the limit cycle onset which otherwise could occur in the digitally controlled buck converter.

Table 5. Digital control loop parameters used in Equations (38)–(41).

G_{vd0}	H_V	V_{FS} (V)	N_{bit}	res_{ADC} (V)	N_{DPWM}	t_{res} (ps)	res_{DPWM}	K_P
1.8474	0.1522	3.3	12	8.059×10^{-4}	204,800	48.828	4.883×10^{-6}	1084.1

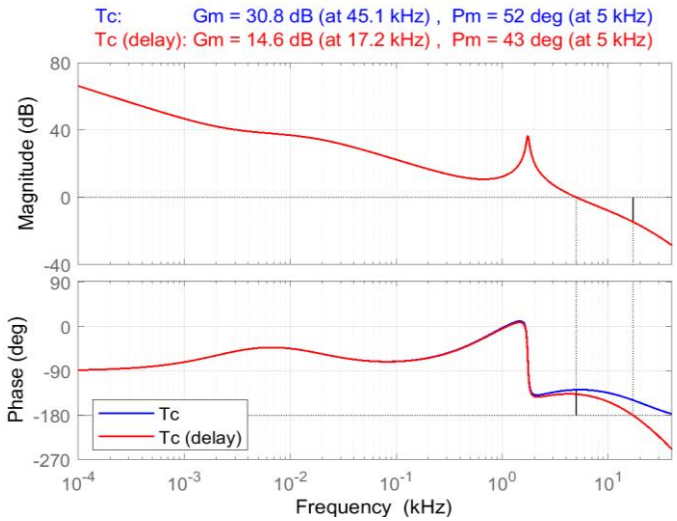


Figure 21. Bode plots of the compensated loop gain $T_c(s)$ including the sampling delay effect.

4. Experimental Prototype

4.1. IPT Coil Realization

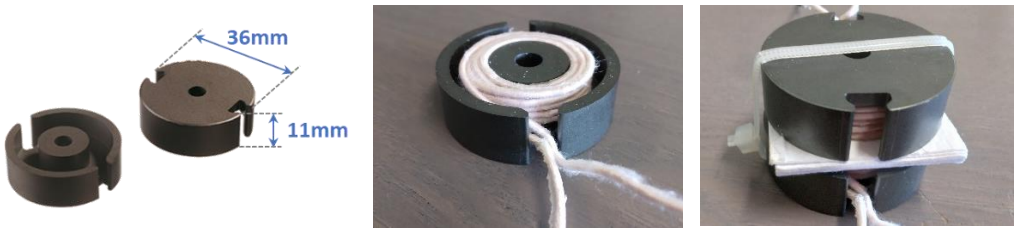
To optimize the overall system performances while maintaining the limited coupling area, custom IPT coils have been herein realized by adopting ferrite pot cores and suitable litz-wires. These latter allow to reduce high-frequency skin and proximity effects in the windings, which could lead to an increase in the resulting AC resistance and power losses [35]. In particular, the Ferroxcube P36/22–3C91 pot cores made of 3C91 ferrite material have been adopted [36] and are depicted in Figure 22a. To realize the windings, litz-wire 170/40 has been used, which is composed of 170 strands of AWG #40 wire, recommended for the operating frequency range [100, 200] kHz. At 200 kHz, the resulting skin depth δ_{skin} in the copper wire is higher than the litz-wire diameter $d_{AWG\#40}$, thus allowing to reduce the skin effect:

$$\delta_{skin} = \sqrt{\frac{\rho_{Cu}}{\pi \mu_{Cu} f_s}} = 0.146 \text{ mm} > d_{AWG\#40} = 0.08 \text{ mm} \tag{44}$$

where ρ_{Cu} = 1.68 × 10^{-8} Ω·m and μ_{Cu} = 1.256629 × 10^{-6} are the copper resistivity and magnetic permeability, respectively. The number of strands (N_{str} = 170) allows for the rms current handling capability of the litz-wire given by (45):

$$I_{rms} = N_{str}\left(\frac{\pi d_{AWG\#40}^2}{4}\right)J_{rms} = 5.13\ \text{A} \tag{45}$$

where J_{rms} = 6 A/mm^2 represents the maximum allowable rms current density of the copper wire. Thus, the resulting I_{rms} is sufficiently higher than the expected rms current levels in the coils depicted in Figure 13b (see the feasible frequency range from approximately 100 kHz to approximately 150 kHz).



(**a**) (**b**) (**c**)

Figure 22. Custom IPT coils realized with Ferroxcube P36/22–3C91 pot cores and litz-wire 170/40: (**a**) P36/22–3C91 cores; (**b**) single custom coil; and (**c**) TX and RX coil set with 3 mm air-gap.

Fifteen turns of the litz-wire 170/40 have been realized on each pot core, and the resulting self-inductances L_1, L_2 and the DC winding resistances R_{L1}, R_{L2} have been measured by means of the Extech Instruments LCR200 Passive Component LCR Meter [37]. Such measurement data are listed in Table 6, together with the coupling coefficient values $k = \sqrt{M/(L_1L_2)}$ obtained between the two identical coils for three different air-gap lengths, namely l_g = {1.5, 3, 6} mm. The air-gap l_g = 3 mm has been herein selected for the final TX and RX coil set depicted in Figure 22c, since such a value yields sufficiently high self-inductances of the coils $L_1 = L_2$ = 23 µH and a coupling coefficient k = 0.53, which is a good trade-off solution for the considered application.

Table 6. Custom IPT coils measurement data.

l_g (mm)	L_1, L_2 (µH)	R_{L1}, R_{L2} (mΩ)	k
1.5	35	50	0.75
3	23	50	0.53
6	20	50	0.34

4.2. PR-IPTS Boards

An experimental prototype of the proposed PR-IPTS has been assembled using the components listed in Table 7 (refer to Figures 12 and 22 for the IPTS and buck components, respectively). The realized custom Printed Circuit Boards (PCBs) of the IPT TX and RX stages are depicted in Figure 23, with the dimensions of 95 mm × 70 mm × 18 mm and 106 mm × 70 mm × 18 mm, respectively.

Table 7. PR-IPTS components.

Circuit Components	Values
Inverter MOSFETs S_1–S_4	IPD50N04S4–10: R_{ds} = 9.3 mΩ, Qg = 14 nC
Rectifier MOSFETs M_1–M_4	BSZ070N08LS5: Rds = 7 mΩ, Qg = 14 nC
Buck half bridge MOSFETs M_{HS}-M_{LS}	BSC0993ND: Rds_{HS} = 4.2 mΩ, Qg_{HS} = 13 nC Rds_{LS} = 5.6 mΩ, Qg_{LS} = 6.7 nC
TX and RX coils L_1, L_2	$L_1 = L_2$ = 23 µH, $R_{L1} = R_{L2}$ = 50 mΩ
Buck output inductor L_o	L_o = 22 µH, R_{Lo} = 23 mΩ
TX and RX compensation capacitors C_1, C_2	C_1 = 200 nF, C_2 = 100 nF
IPTS input capacitor C_{in}	C_{in} = 2440 µF
Intermediate bus capacitor C_f	C_f = 2068 µF
Buck output capacitor C_o	C_o = 440 µF, ESR_o = 5 mΩ

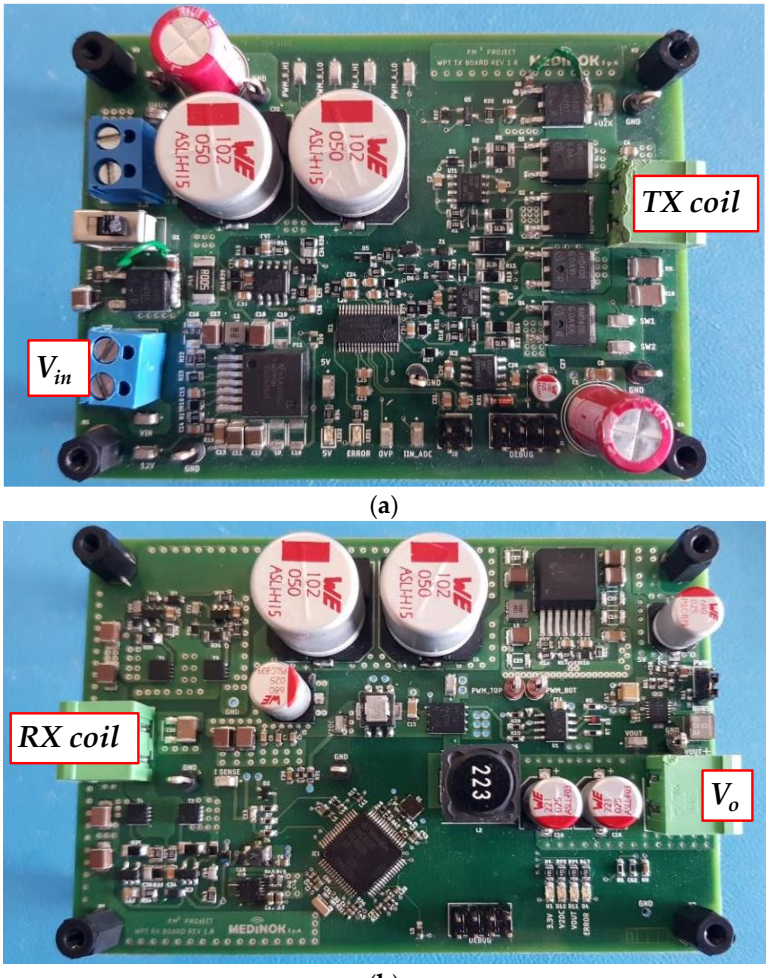


Figure 23. PCBs of the experimental prototype: (**a**) TX board; and (**b**) RX board.

On the TX board, the switching frequency and phase-shift modulation of the full-bridge inverter has been digitally implemented through the Infineon 32-bit XMC1302-T038X0064AB microcontroller with ARM® Cortex®-M0 [38], which allows to properly configure the peripherals using the proprietary Integrated Development Environment (IDE) Dave Infineon® [39]. Thus, two PWM signal pairs synchronized at the same switching frequency have been generated from two different DPWM peripherals of the Micro Controller Unit (MCU) and subsequently delivered to the IRS2106SPBF drivers of the two inverter legs [40]. Each PWM signal pair includes two complementary square-wave signals used to drive the high- and low-side MOSFETs of the respective leg, and a 100 ns dead-time

has been introduced to prevent a cross-conduction of the switches. To realize a desired phase-shift angle, a delay has been added to the second PWM signal pair with respect to the first one. Both DPWM peripherals have a fixed time resolution t_{res} = 15.625 ns, resulting in a number of discrete digital levels N_{DPWM} which depends on the desired inverter switching frequency f_s, according to (46):

$$N_{DPWM} = \lceil 0.5\left(\frac{1}{f_s t_{res}} - 1\right)\rceil \quad (46)$$

where a center-aligned mode of the DPWM peripherals has been set, which allows to realize a desired PWM period by first counting up from zero to the N_{DPWM} level and then down to zero [38]. For the switching frequency f_s = 100 kHz, (46) yields N_{DPWM} = 320, while for f_s = 200 kHz, it provides N_{DPWM} = 160. The delay between the two DPWM peripherals, needed to implement a normalized phase-shift angle in the range d = [0, 1], can then be realized with discrete DPWM steps in the range [0, N_{DPWM}], resulting in the normalized phase-shift resolution Δd_{min} given by (47):

$$\Delta d_{min} = 1/N_{DPWM} \quad (47)$$

For f_s = 100 kHz, (47) yields Δd_{min} = 0.003125, while for f_s = 200 kHz, it provides Δd_{min} = 0.00625. Hence, the phase-shift resolution is lower than 1% for the switching frequency range of interest f_s = [100, 200] kHz.

On the RX board, the DVMC of the buck converter has been realized through the Infineon 32-bit XMC4200-F64X256 microcontroller with the ARM® Cortex®-M4 [41]. Its main peripheral parameters of interest are provided in Table 5, where a high-resolution DPWM peripheral of the XMC4200 MCU has been adopted. The generated complementary DPWM signals are used to drive the buck MOSFETs M_{HS}-M_{LS} through the IRS2011SPBF gate driver [42]. Each of the rectifier MOSFETs M_1–M_4 is switched by the respective IR1161LPBF controller [29], according to the synchronous rectification scheme previously described in Section 2.1.

4.3. Experimental Results

4.3.1. Efficiency Assessment with Electronic Load

The developed PR-IPTS prototype has been tested under different load conditions to assess its power and efficiency performances and output voltage regulating capabilities for variable load demands. Figure 24 shows a complete experimental set-up used during the tests, including the TX and RX boards with the coupling coils, a BK Precision 9111 180 W Multi Range 60 V/8 A DC Power Supply connected to the IPTS input, an HP Agilent Keysight 6060B 300 W 60 A/60 V DC Electronic Load connected to the system output, and a Teledyne LeCroy HDO9404 Digital Oscilloscope.

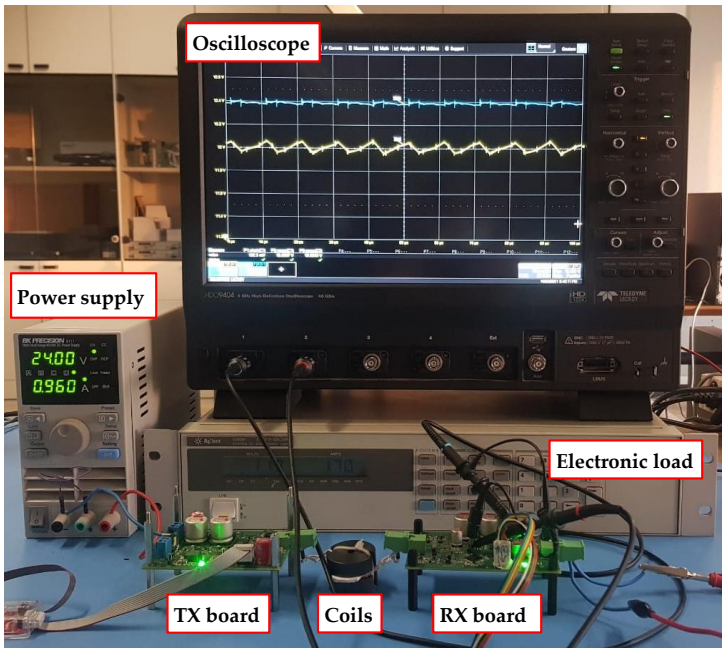


Figure 24. Experimental set-up used to test the developed PR-IPTS prototype.

The overall PR-IPTS efficiency has been measured under four different load conditions R_L = {5, 7, 14, 24} Ω (emulated by means of the electronic load configured in the constant resistance mode), which, respectively, correspond to the load power values P_o = {28.8, 20.6, 10.3, 6} W. The inverter switching frequency has been varied in the range f_s = [105, 140] kHz: for frequencies lower than approximately 100 kHz, the system enters an instable region (blue rectangle in Figure 13d) wherein the buck controller may loose the capability of regulating the output voltage because of the non-monotonic control-to-output characteristic (see Figure 14a,b). On the other hand, for frequencies higher than 140 kHz, the overall high-frequency losses increase yielding the lower experimental efficiency. The intermediate bus voltage V_{2dc} has been varied in the range [14, 17] V while ensuring the output voltage regulation at 12 V: the V_{2dc} values lower than 14 V cannot be realized by the buck converter due to the respective duty-cycle saturation, while the V_{2dc} values higher than 17 V cannot be achieved over the frequency range of interest f_s = [105, 140] kHz due to the phase-shift saturation, as previously highlighted in Figure 13a. Figure 25 depicts the resulting experimental efficiencies obtained over the considered ranges of f_s and V_{2dc} for four analyzed load conditions. It can be noted that for the heavy loads R_L = 5 Ω (Figure 25a) and R_L = 7 Ω (Figure 25b), η decreases with f_s, for the light load R_L = 24 Ω (Figure 25d), η increases with f_s, while for the intermediate load R_L = 14 Ω (Figure 25c), the efficiency decreases with f_s at low V_{2dc} values and increases with f_s at high V_{2dc} levels. Figure 25b–d highlight that the efficiency is maximized at V_{2dc} = 14 V for loads R_L = {7, 14, 24} Ω, while V_{2dc} = 15 V maximizes η for R_L = 5 Ω (Figure 25a). The resulting maximum efficiency points are listed in Table 8 for the analyzed load conditions. Eventually, Figure 26 shows the mean values of the experimental efficiency (red circles, obtained by averaging the measurement data of Figure 25) vs. the output power P_o, together with the respective error bars indicating the minimum and the maximum experimental efficiency points. The graph highlights that the average efficiency increases from approximately 71% at P_o = 6 W to approximately 91% at P_o = 28.8 W.

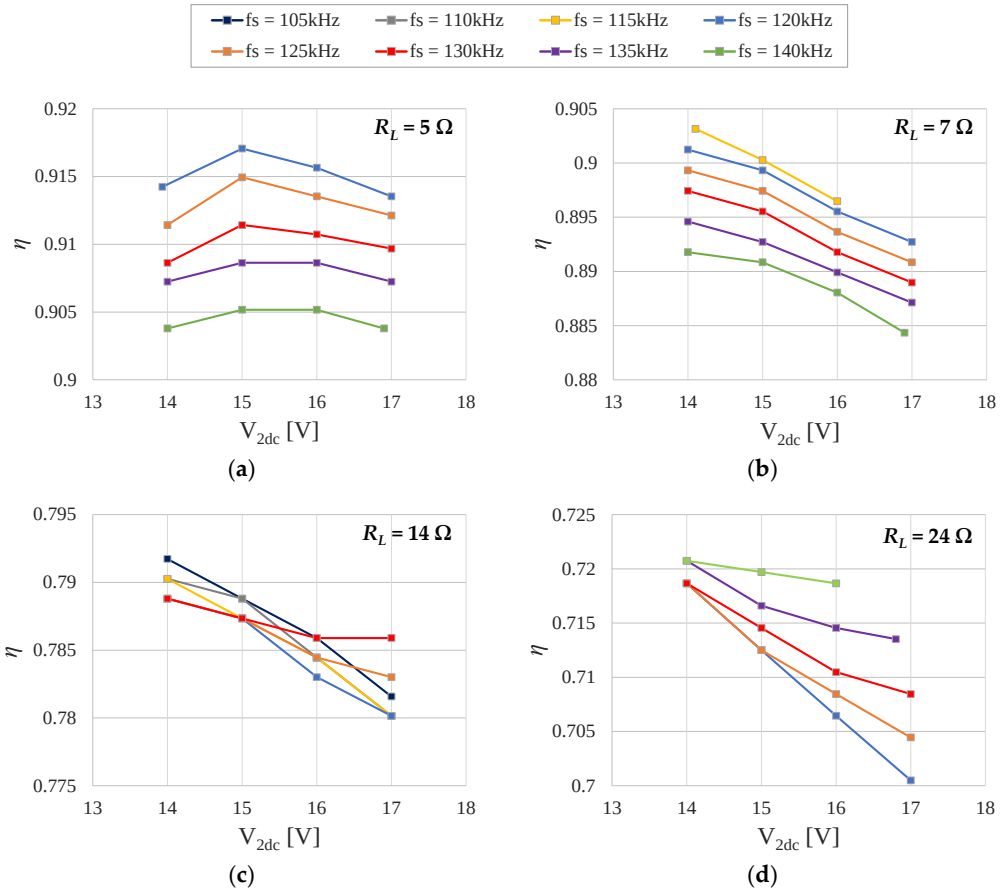


Figure 25. Experimental PR-IPTS efficiency vs. intermediate bus voltage V_{2dc} and inverter switching frequency f_s for different load conditions: (**a**) R_L = 5 Ω; (**b**) R_L = 7 Ω; (**c**) R_L = 14 Ω; and (**d**) R_L = 24 Ω.

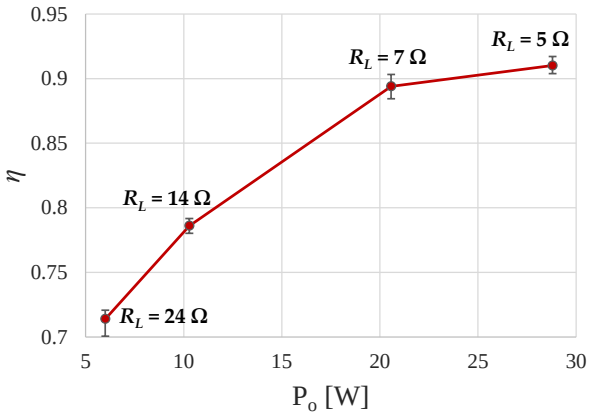


Figure 26. Average experimental efficiency vs. output power P_o (red circles) with error bars indicating the minimum and the maximum efficiency points.

Table 8. Maximum efficiency points achieved for the analyzed load conditions.

R_L (Ω)	P_o (W)	f_s (kHz)	V_{2dc} (V)	η_{max}
5	28.8	120	15.0	0.917
7	20.6	115	14.1	0.903
14	10.3	105	14.0	0.792
24	6.0	140	14.0	0.721

4.3.2. Output Voltage Regulation under Variable Load Conditions

To assess the output voltage regulation capabilities, the IPTS has been tested under both static and dynamic load conditions. Figure 27 shows steady-state experimental waveforms of the output voltage $v_o(t)$ and intermediate bus voltage $v_{2dc}(t)$ measured under static load conditions, obtained for the load values R_L = {5, 7, 14, 24} Ω at f_s = 120 kHz and V_{2dc} = 15 V. The plots highlight that for all the analyzed load levels, the output voltage is correctly regulated at the desired nominal value $V_{o,nom}$ = 12 V (with an accuracy lower than 20 mV ≈ 0.17% $V_{o,nom}$), while the amplitude of the peak-to-peak voltage ripple is limited to 110 mV ≈ 0.92% $V_{o,nom}$. Finally, Figure 28 shows experimental waveforms of $v_o(t)$ and $v_{2dc}(t)$ measured under dynamic conditions, where the electronic load has been configured to emulate a square-wave variation of the load resistance between 7 Ω and 14 Ω (Figure 28a) and between 5 Ω and 24 Ω (Figure 28b) at a frequency f_{LT} = 5 Hz. Note that such results have been obtained for the inverter switching frequency f_s = 120 kHz, while the phase-shift has been adjusted during each test to achieve the intermediate bus voltage V_{2dc} = 15 V at the lower load resistance (i.e., d = 0.621 for R_L = 7 Ω in Figure 28a and d = 0.717 for R_L = 5 Ω in Figure 28b). From Figure 28a, it can be observed that $v_{2dc}(t)$ presents a step variation between 15 V and 15.7 V as the load resistance changes from 7 Ω to 14 Ω (and *vice versa*), since the equivalent DC resistance R_{dc} seen at the buck input also changes, and the IPT stage evolves towards a new bias point. As a result, $v_o(t)$ presents over- and undershoots with amplitudes of 123 mV (1.03% $V_{o,nom}$) and 148 mV (1.23% $V_{o,nom}$), respectively. From Figure 28b it can be observed that $v_{2dc}(t)$ presents a step variation between approximately 14.8 V and 17.6 V as the load resistance changes from 5 Ω to 24 Ω, resulting in the output voltage overshoot and undershoot amplitudes of 240 mV (2% $V_{o,nom}$) and 282 mV (2.35% $V_{o,nom}$), respectively. It is worth observing that such amplitudes are contained within the typical ranges conventionally adopted for switching regulators (e.g., 5% $\Delta V_{o,nom}$), while the DVMC controller ensures a correct output voltage regulation under load transient conditions.

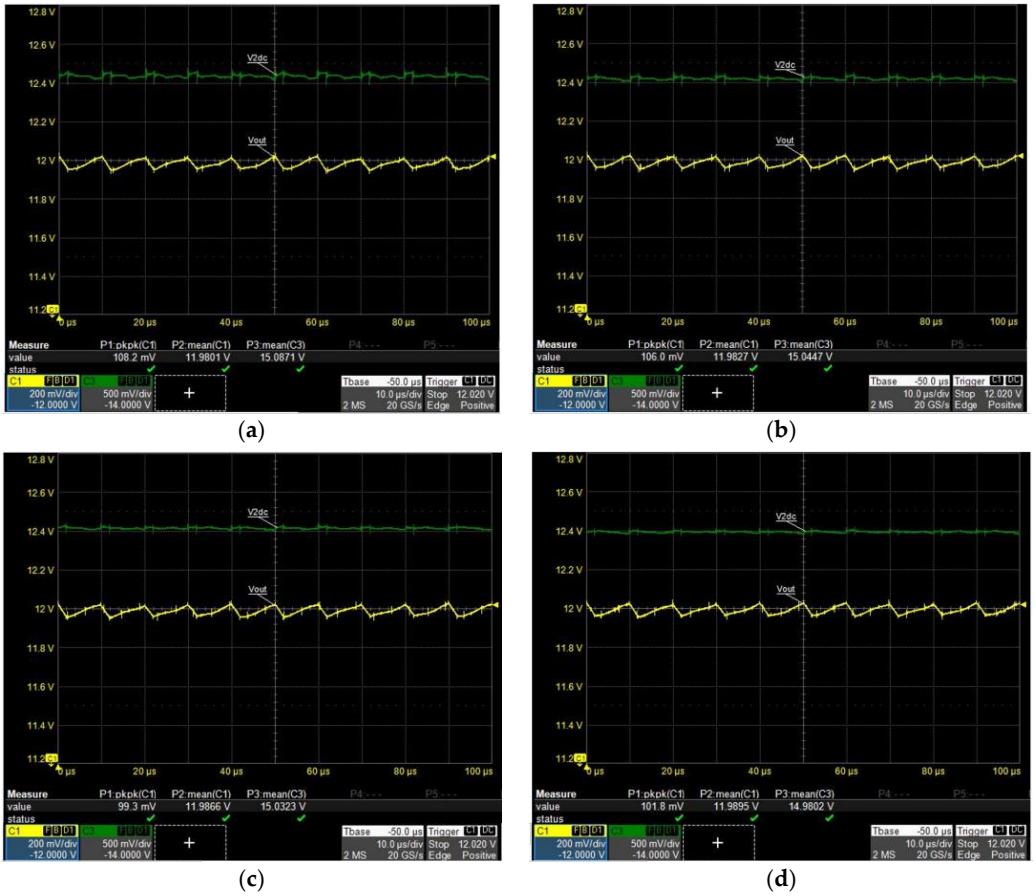


Figure 27. Steady-state experimental waveforms of $v_o(t)$ (yellow) and $v_{2dc}(t)$ (green) at f_s = 120 kHz and V_{2dc} = 15 V for different load conditions: (**a**) R_L = 5 Ω; (**b**) R_L = 7 Ω; (**c**) R_L = 14 Ω; and (**d**) R_L = 24 Ω.

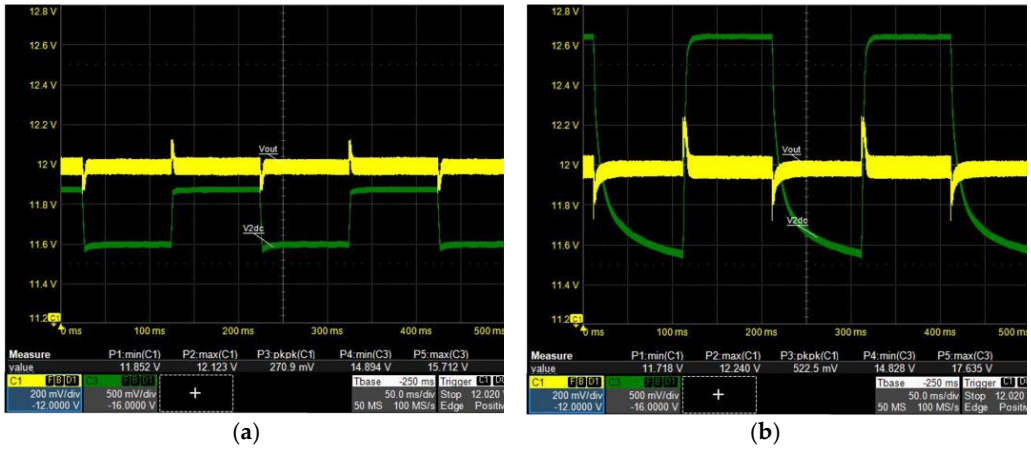


Figure 28. Experimental waveforms of $v_o(t)$ (yellow) and $v_{2dc}(t)$ (green) at f_s = 120 kHz and f_{LT} = 5 Hz for different load transient conditions: (**a**) R_L = {7–14} Ω; and (**b**) R_L = {5–24} Ω.

4.3.3. Battery Charging Test

Eventually, the developed PR-IPTS prototype has been used to charge the Aftertech EB-162442275573 Lithium battery with a nominal voltage of 12 V, a capacity of 10 Ah and a maximum recharge current of 3 A [43]. The charging process has been performed in a constant voltage mode by imposing the 12 V regulated output voltage of the PR-IPTS to the battery. Since the equivalent static resistance of the battery, defined as the ratio

between the slowly varying voltage and the current, increases during the charging, the tests have been carried out by setting the inverter switching frequency equal to 130 kHz and gradually adjusting the inverter phase-shift to achieve the intermediate bus voltage V_{2dc} = 15 V. During the test, the battery static resistance R_{batt} increased from approximately 4 Ω to approximately 24 Ω, as shown in Figure 29a, while the battery current decreased from 3 A to 0.5 A, and the average output power delivered to the battery varied from approximately 35 W to approximately 6 W. The resulting PR-IPTS efficiency is depicted in Figure 29b, confirming that the developed IPT system yields experimental efficiencies higher than 85% over a wide output power range [15, 35] W.

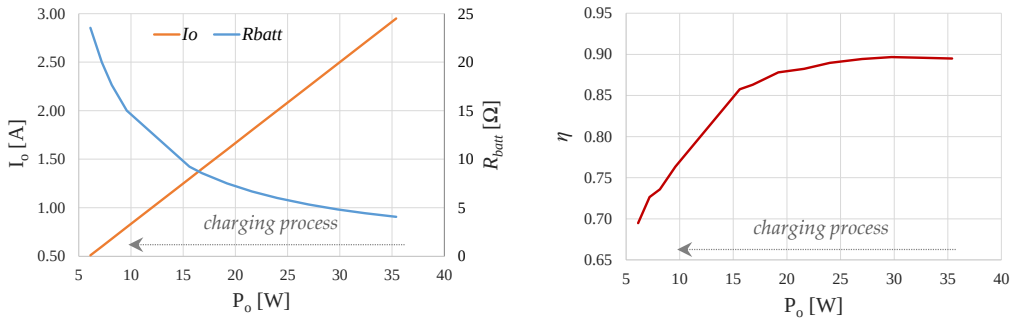


Figure 29. Experimental measurements obtained during the battery charging test: (**a**) PR-IPTS output current I_o (orange) and battery static resistance R_{batt} (blue) and (**b**) efficiency (red), vs. average output power P_o.

4.4. Results Discussion

The experimental tests presented in the previous section have showed that the developed IPTS is able to correctly perform the output voltage regulation at the desired nominal value of 12 V for static resistive loads in the range R_L = [5, 24] Ω, yielding the output power in the range P_o = [6, 28.8] W. The experimental efficiencies have been measured over the operating ranges f_s = [105, 140] kHz and V_{2dc} = [14, 17] V, highlighting that, for different loads, the efficiency is maximized in different operating points of f_s and V_{2dc} as previously reported in Table 8. The achieved maximum efficiencies are of 72.1% for R_L = 24 Ω (6 W) and of 91.7% for R_L = 5 Ω (28.8 W).

The output voltage regulation capabilities of the presented IPTS have been assessed under different static and dynamic load conditions. For the former, the V_o accuracy lower than 20 mV (0.17% $V_{o,nom}$) has been obtained, with a peak-to-peak voltage ripple amplitude limited to 110 mV (0.92% $V_{o,nom}$). For the latter, the IPTS behavior has been tested in the presence of load transients, confirming the excellent output voltage regulation capabilities with limited over- and undershoot amplitudes (less than 3% for the worst-case load transient R_L = [5–24] Ω).

The system performances have also been assessed during a battery charging test, performed on a commercial lithium battery with a 12 V nominal voltage. It has been shown that the PR-IPTS is able to correctly charge the battery with efficiency levels higher than 85% over the output power range P_o = [15, 35] W, while an experimental efficiency of approximately 70% has been obtained for the battery power level of 6 W toward the end of the charging process. These results, obtained for the slowly varying battery static resistance in the range R_{batt} = [4, 24] Ω, are consistent with the tests performed for the fixed resistive loads. Thus, the developed system can be effectively adopted to charge both fixed and variable loads.

Eventually, Tables 9 and 10 provide a comparison between the main IPTS solutions discussed in Section 1.1 and the system developed in this work, highlighting their relevant specifications (Table 9) and functionalities (Table 10).

Table 9. IPTS specification comparison.

Reference	TX/RX Coil Size	Air Gap	Frequency	Power	Efficiency
This work	36/36 mm	3 mm	100–160 kHz	6–35 W	72–92%
[13]	N/A	70 mm	165–180 kHz	2.5–3.7 kW	N/A
[14]	N/A	N/A	95.6 kHz	9–90 W	74–90%
[16]	270/270 mm	250 mm	515 kHz	25–100 W	74–79%
[17]	100 × 58/100 × 58 mm	5 mm	50 kHz	300–1800W	60–77%
[18]	43/28 mm	3 mm	140 kHz	1–11 W	69–78%
[19]	320/320 mm	70 mm	13.56 MHz	40 W	70%
[20]	27/27 mm	N/A	97.56 kHz	4.5 W	65%
[21]	310/310 mm	N/A	100 kHz	5.6 W	60%
[22]	53 × 53/53 × 53 mm	12 mm	100 kHz	1–10 W	34–70%
[24]	500 × 500/500 × 500 mm	100 mm	85 kHz	3 kW	95%
[25]	43/43 mm	23.5 mm	592 kHz	0.25–5 W	73%
[26]	N/A	N/A	92–110 kHz	100–600 W	65–78%

Table 10. IPTS functionality comparison.

Reference	Rectification Type	Pre/Post-Regulation	TX–RX Communication	Output Voltage Regulation	Efficiency Maximization Control
This work	Synchronous	Post	No	Yes	No
[13]	Passive	No	Yes	Yes	No
[14]	Active	No	No	Yes	No
[16]	Passive	Pre and post	Yes	Yes	Yes
[17]	Active	No	No	Yes	No
[18]	Active	Post	Yes	No	No
[19]	Passive	Post	Yes	No	Yes
[20]	Passive	Post	No	Yes	Yes
[21]	Passive	Post	No	Yes	Yes
[22]	Passive	Post	No	Yes	Yes
[24]	Passive	Pre and post	Yes	No	Yes
[25]	Regulating	No	No	Yes	Yes
[26]	Passive	Post	No	Yes	Yes

It can be observed that the system proposed in this work ranks among the best IPTS solutions in terms of efficiency (92%), together with the systems developed in [14,24] having the maximum efficiencies of 90% and 95%, respectively. As regards the IPTS solution presented in [14], it provides a wider output power range (up to 90 W) but a slightly lower maximum efficiency (90%) as compared to our system (92%, 35 W). Both systems are able to guarantee the output voltage regulation, while with respect to the efficiency maximization, the solution of [14] only considers the ZVS achievement yielding a minimization of the inverter switching losses, but does not optimize the overall system efficiency. A complication of the proposed scheme lies in the need for current phase detection circuits on both the TX and RX sides to realize the proposed control strategy.

The solution presented in [24] outperforms our system in terms of efficiency (95%) and is conceived for higher output power levels (3 kW). In comparison, our system presents a limited architectural complexity, since it does not require a pre-regulation and a bidirectional communication link between the TX and RX sides. Even if the latter has a limited implementation cost, the system complexity is significantly increased. Moreover, the solution of [24] does not implement the output voltage regulation which could be a drawback for the loads requiring a stable supply voltage. Such a scheme is mainly focused on the maximum efficiency achievement performed under resonance conditions, but is not valid at different operating frequencies.

Even though our solution does not implement the maximum efficiency tracking scheme, it enables the efficiency mapping with respect to both the inverter switching

frequency and the phase-shift. Conversely, previous works [20,21] proposed IPTSs with similar architectural complexities implementing the efficiency maximization by controlling the phase-shift parameter only, but did not consider the inverter frequency optimization. In this regard, our approach provides a more complete and extended characterization of the developed system and addresses the post-regulator controllability issues which instead are not taken into account in the above references. The implementation of control algorithms for maximum efficiency point tracking will be the subject of future works.

5. Conclusions

In this paper, a Post-Regulated Inductive Power Transfer System (PR-IPTS) has been developed, which is based on a series–series capacitive compensation scheme and a DC/DC buck converter used as a post-regulator. Digital control techniques have been implemented by means of low-cost commercial microcontrollers with the objective of ensuring the system efficiency maximization and the output voltage regulation. In this regard, the former objective has been reached through the primary inverter phase-shift modulation performed under different switching frequency and intermediate bus voltage conditions to determine the maximum efficiency points for different loads, while the latter objective has been achieved through the Digital Voltage Mode Control (DVMC) of the duty-cycle of the buck post-regulator. The experimental results performed on a laboratory prototype showed that the developed PR-IPTS yields excellent output voltage regulation capabilities for both fixed and variable loads (including both resistive and battery loads) and is able to deliver up to 35 W output power with a maximum efficiency of 91.7%. The proposed PR-IPTS solution can be profitably used to develop enhanced electronic solutions in the framework of smart homes and workplaces applications.

Author Contributions: Conceptualization, K.S., A.V. and M.C.; methodology, K.S. and A.V.; software, A.V., K.S. and A.A.; validation, K.S., A.V. and M.C.; data curation, A.A. and M.P.; writing—original draft preparation, K.S., A.V., P.V.; writing—review and editing, K.S., A.V. and P.V.; supervision, A.V., M.C., A.A., M.P. and P.V. All authors have read and agreed to the published version of the manuscript.

Funding: This research was carried out as a deep extension of studies into the Project "PM3-Modular Multi-Mission Platform, CUP: B66G18000740005", Italian Ministry of Education, University and Research call n. 1735/2017, PON Research & Innovation 2014–2020 and FSC.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data of our study are available upon request.

Conflicts of Interest: The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

References

1. Ruffo, R.; Cirimele, V.; Diana, M.; Khalilian, M.; La Ganga, A.; Guglielmi, P. Sensorless control of the charging process of a dynamic inductive power transfer system with an interleaved nine-phase boost converter. *IEEE Trans. Ind. Electron.* **2018**, *65*, 7630–7639. [CrossRef]
2. Cirimele, V.; Diana, M.; Freschi, F.; Mitolo, M. Inductive power transfer for automotive applications state-of-the-art and future trends. *IEEE Trans. Ind. Appl.* **2018**, *54*, 4069–4079. [CrossRef]
3. Yeo, T.-D.; Kwon, D.; Khang, S.-T.; Yu, J.-W. Design of Maximum Efficiency Tracking Control Scheme for Closed-Loop Wireless Power Charging System Employing Series Resonant Tank. *IEEE Trans. Power Electron.* **2017**, *32*, 471–478. [CrossRef]
4. Al-Attar, A.; Attia, S.A.; Al-Bialy, A.; Abdelatif, E.N.; Al-Gazar, A.S.; Salem, A.; Badr, B.M. Wireless Power Transfer for Toys and Portable Devices. In Proceedings of the IEEE Conference on Power Electronics and Renewable Energy (CPERE), Aswan, Egypt, 23–25 October 2019; pp. 479–484. [CrossRef]
5. Haerinia, M.; Shadid, R. Wireless Power Transfer Approaches for Medical Implants: A Review. *Signals* **2020**, *1*, 12. [CrossRef]
6. Mao, Z.; Han, H.; Zhu, Q.; Su, M.; Peng, T. New concept of wireless power grid for industrial and home application. In Proceedings of the 2018 IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES), Hamilton, New Zealand, 31 January–2 February 2018. [CrossRef]

7. Fadhil, H.A.; Abdulqader, S.G.; Aljunid, S.A. Implementation of wireless power transfer system for Smart Home applications. In Proceedings of the IEEE 8th GCC Conference & Exhibition, Muscat, Oman, 1–4 February 2015. [CrossRef]
8. Mano, M.; Sankar, R. Wireless Charger Networking for Mobile Devices using Bluetooth Technologies. *Int. J. Linguist. Comput. Appl. (IJLCA)* **2018**, *5*, 1–3.
9. Wang, C.-S.; Stielau, O.H.; Covic, G.A. Design Considerations for a Contactless Electric Vehicle Battery Charger. *IEEE Trans. Ind. Electron.* **2005**, *52*, 1308–1314. [CrossRef]
10. Würth Elektronik, REDEXPERT. Available online: https://redexpert.we-online.com/redexpert/#/ (accessed on 1 September 2021).
11. TDK, Wireless Power Transfer. Available online: https://product.tdk.com/en/products/wireless-charge/index.html (accessed on 26 August 2021).
12. Abracon, Wireless Charging. Available online: https://abracon.com/parametric/wirelesscharging (accessed on 27 August 2021).
13. Zahid, Z.U.; Dalala, Z.M.; Zheng, C.; Chen, R.; Faraci, W.E.; Lai, J.-S.; Lisi, G.; Anderson, D. Modeling and Control of Series–Series Compensated Inductive Power Transfer System. *IEEE J. Emerg. Sel. Top. Power Electron.* **2013**, *3*, 111–123. [CrossRef]
14. Liu, F.; Lei, W.; Wang, T.; Nie, C.; Wang, Y. A phase-shift soft-switching control strategy for dual active wireless power transfer system. In Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, USA, 1–5 October 2017. [CrossRef]
15. Ahn, D.; Kim, S.; Moon, J.; Cho, I.-K. Wireless Power Transfer with Automatic Feedback Control of Load Resistance Transformation. *IEEE Trans. Power Electron.* **2016**, *31*, 7876–7886. [CrossRef]
16. Li, H.; Li, J.; Wang, K.; Chen, W.; Yang, X. A Maximum Efficiency Point Tracking Control Scheme for Wireless Power Transfer Systems Using Magnetic Resonant Coupling. *IEEE Trans. Power Electron.* **2015**, *30*, 3998–4008. [CrossRef]
17. Chen, Q.; Jiang, L.; Hou, J.; Ren, X.; Ruan, X. Research on bidirectional contactless resonant converter for energy charging between EVs. In Proceedings of the 39th Annual Conference of the IEEE Industrial Electronics Society (IECON), Vienna, Austria, 10–13 November 2013. [CrossRef]
18. Berger, A.; Agostinelli, M.; Vesti, S.; Oliver, J.A.; Cobos, J.A.; Huemer, M. A Wireless Charging System Applying Phase-Shift and Amplitude Control to Maximize Efficiency and Extractable Power. *IEEE Trans. Power Electron.* **2015**, *30*, 6338–6348. [CrossRef]
19. Fu, M.; Yin, H.; Zhu, X.; Ma, C. Analysis and Tracking of Optimal Load in Wireless Power Transfer Systems. *IEEE Trans. Power Electron.* **2015**, *30*, 3952–3963. [CrossRef]
20. Zhong, W.X.; Hui, S.Y.R. Maximum Energy Efficiency Tracking for Wireless Power Transfer Systems. *IEEE Trans. Power Electron.* **2015**, *30*, 4025–4034. [CrossRef]
21. Yang, Y.; Zhong, W.; Kiratipongvoot, S.; Tan, S.-C.; Hui, S.Y.R. Dynamic Improvement of Series–Series Compensated Wireless Power Transfer Systems Using Discrete Sliding Mode Control. *IEEE Trans. Power Electron.* **2018**, *33*, 6351–6360. [CrossRef]
22. Li, T.; Wang, X.; Zheng, S.; Liu, C. An Efficient Topology for Wireless Power Transfer over a Wide Range of Loading Conditions. *Energies* **2018**, *11*, 141. [CrossRef]
23. Di Capua, G.; Femia, N. A Critical Investigation of Coupled Inductors SEPIC Design Issues. *IEEE Trans. Ind. Electron.* **2014**, *61*, 2724–2734. [CrossRef]
24. Ishihara, H.; Moritsuka, F.; Kudo, H.; Obayashi, S.; Itakura, T.; Matsushita, A.; Mochikawa, H.; Otaka, S. A voltage ratio-based efficiency control method for 3 kW wireless power transmission. In Proceedings of the 2014 IEEE Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX, USA, 16–20 March 2014. [CrossRef]
25. Tang, X.; Zeng, J.; Pun, K.P.; Mai, S.; Zhang, C.; Wang, Z. Low-Cost Maximum Efficiency Tracking Method for Wireless Power Transfer Systems. *IEEE Trans. Power Electron.* **2018**, *33*, 5317–5329. [CrossRef]
26. Patil, D.; Sirico, M.; Gu, L.; Fahimi, B. Maximum efficiency tracking in wireless power transfer for battery charger: Phase shift and frequency control. In Proceedings of the 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 18–22 September 2016. [CrossRef]
27. Li, H.; Wang, K.; Huang, L.; Chen, W.; Yang, X. Dynamic Modeling Based on Coupled Modes for Wireless Power Transfer Systems. *IEEE Trans. Power Electron.* **2015**, *30*, 6245–6253. [CrossRef]
28. Li, H.; Tang, Y.; Wang, K.; Yang, X. Analysis and control of post regulation of wireless power transfer systems. In Proceedings of the 2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC), Auckland, New Zealand, 5–8 December 2016; pp. 1–5. [CrossRef]
29. Infineon Technologies, SmartRectifier IR1161LPbF Datasheet. 2016. Available online: https://www.infineon.com/dgdl/ir1161lpbf.pdf?fileId=5546d462533600a4015355c439a5164d (accessed on 28 June 2021).
30. Hurtuk, P.; Radvan, R.; Frivaldský, M. Full bridge converter with synchronous rectifiers for low output voltage application. In Proceedings of the 2011 International Conference on Applied Electronics, Pilsen, Czech Republic, 7–8 September 2011.
31. Zhang, W.; Wong, S.; Tse, C.K.; Chen, Q. Design for Efficiency Optimization and Voltage Controllability of Series–Series Compensated Inductive Power Transfer Systems. *IEEE Trans. Power Electron.* **2014**, *29*, 191–200. [CrossRef]
32. Venable, H.D. The K Factor: A New Mathematical Tool for Stability Analysis. In Proceedings of the 10th International Solid-State Power Electronics Conference (Powercon 10), San Diego, CA, USA, 22–24 March 1983.
33. Biricha Digital Power Ltd., Digital PSU Plant Measurement 2017. Available online: https://www.biricha.com/uploads/8/9/8/0/89803127/digital_plant_measurement_reviewed.pdf (accessed on 21 June 2021).

34. Peterchev, A.V.; Sanders, S.R. Quantization resolution and limit cycling in digitally controlled PWM converters. *IEEE Trans. Power Electron.* **2003**, *18*, 301–308. [CrossRef]
35. Cho, J.; Sun, J.; Kim, H.; Fan, J.; Lu, Y.; Pan, S. Coil design for 100 KHz and 6.78 MHz WPT system: Litz and solid wires and winding methods. In Proceedings of the 2017 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI), Washington, DC, USA, 7–11 August 2017. [CrossRef]
36. Ferroxcube, P36/22 P Cores and Accessories. 2008. Available online: http://ferroxcube.home.pl/prod/assets/p3622.pdf (accessed on 5 July 2021).
37. Extech Instruments LCR200 Passive Components LCR Meter. Available online: http://www.extech.com/products/LCR200 (accessed on 6 July 2021).
38. Infineon Technologies, XMC1300 AB-Step Reference Manual, V1.3 2016-08. Available online: https://www.infineon.com/dgdl/Infineon-xmc1300-AB_rm-UM-v01_03-EN.pdf?fileId=5546d46249cd1014014a0a8436965e28 (accessed on 6 July 2021).
39. Infineon Technologies, DAVE™—Professional Development Platform for XMC™ Microcontrollers. Available online: https://infineoncommunity.com/dave-download_id645 (accessed on 13 July 2021).
40. Infineon Technologies, IRS2106/IRS21064(S)PbF Datasheet, No. PD60246. Available online: https://www.infineon.com/dgdl/Infineon-IRS2106-DataSheet-v01_00-EN.pdf?fileId=5546d462533600a4015356763aa527a3 (accessed on 15 July 2021).
41. Infineon Technologies, XMC4100/XMC4200 Reference Manual, V1.6 2016-07. Available online: https://www.infineon.com/dgdl/Infineon-xmc4100_xmc4200_rm_v1.6_2016-UM-v01_06-EN.pdf?fileId=db3a30433afc7e3e013b3c44ccd35c20 (accessed on 16 July 2021).
42. Infineon Technologies, IRS2011(S)PBF Datasheet. 2015. Available online: https://www.infineon.com/dgdl/Infineon-IRS2011-DataSheet-v01_00-EN.pdf?fileId=5546d462533600a401535675c19f2784 (accessed on 12 July 2021).
43. Battery pack 12 V 10 Ah Rechargeable High Quality Lithium F2D5. Available online: https://www.aftertech.eu/pacco-batteria-12-volt-10000mah-10ah-12v-ricaricabile-alta-qualita-litio-f2d5-p-16292.html (accessed on 15 July 2021).