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Review

CMOS Low-Dropout Voltage Regulator Design Trends: An Overview

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Abstract: Systems-on-Chip's (SoC) design complexity demands a high-performance linear regulator architecture to maintain a stable operation for the efficient power management of today's devices. Over the decades, the low-dropout (LDO) voltage regulator design has gained attention due to its design scalability with better performance in various application domains. Industry professionals as well as academia have put forward their innovations such as event-driven explicit time-coding, exponential-ratio array, switched RC bandgap reference circuit, etc., to make a trade-off between several performance parameters such as die area, ripple rejection, supply voltage range, and current efficiency. However, current LDO architectures in micro and nanometer complementary metal–oxide–semiconductor (CMOS) technology face some challenges, such as short channel effects, gate leakage, fabrication difficulty, and sensitivity to process variations at nanoscale. This review presents the LDO architectures, optimization techniques, and performance comparisons in different LDO design domains such as digital, analog, and hybrid. In this review, various state-of-the-art circuit topologies, deployed for the betterment of LDO performance and focusing on the specific parameter up-gradation to the overall improvement of the functionality, are framed, which will serve as a comparative study and reference for researchers.

Keywords: linear regulator; CMOS; low-dropout (LDO); figure of merit (FOM)

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1. Introduction

The level of integration of modern electronic circuitries has increased in the last few years, because of the advancement of complementary metal–oxide–semiconductor (CMOS) technology, resulting in compact as well as low-cost electronic appliances [1,2]. The rapid growth of CMOS technology enables lower power supply operation, which helps to attain reduced power dissipation in the circuit and a minimalized fabrication cost because of the compact chip size. CMOS offers the prospect of integrating radio frequency (RF), digital, and analog functions on a single chip in a low-cost manner by eliminating the need for different external components [3,4]. Along with the advantages, the CMOS has also brought up some inevitable challenges for the designers, which include short channel effects, gate leakage, fabrication difficulty, sensitivity to process variations at nanoscale, etc. [5,6]. With the adaptation of the internet of things (IoT), battery-powered devices such as mobile phones, personal digital assistants (PDAs), and smartwatches are nowadays gaining much popularity around the world. Power management has become a more significant issue to improve a device's battery run-time, which necessitates efforts from the

radio frequency integrated circuits' (RFIC) designers for efficient power management for the battery-operated electronic devices [7–10].

Voltage regulators are the integral parts of the power delivery systems of all modern electronic devices and systems. A linear regulator circuit is used to regulate an output voltage, which includes a first current path to conduct a first current, a feedback path to provide feedback and maintain a constant output voltage, and a transistor positioned in the first current path to afford the output voltage [11]. While large power transistors are charged and discharged by the driver, switching losses can incur. A linear regulator has low drain efficiency, which indicates that the output power dissipated as heat in amplifiers due to the average DC current is minimum. Therefore, the load network and DC biasing has little impact on device performance that elongates the linear regulator's effectiveness. A linear regulator can provide high-speed variations in the output signal and can generate a faster load transient response. Moreover, it causes poor performance in current efficiency when the low drop output is large [12–17].

Linear regulators can yield regulated low noise and precise supply voltage, which makes them a crucial power management module, as shown in Figure 1. The functionality of an LDO becomes noteworthy when there is a low voltage difference between the input and output. The drawback of linear regulators is that they primarily reduce the power efficiency that can be measured by the regulation FET's dropout voltage [18]. Several conditions such as external compensation of the regulators, output capacitance, and parasitic capacitance of the output capacitor affect the response of the regulators to a load transient [19].

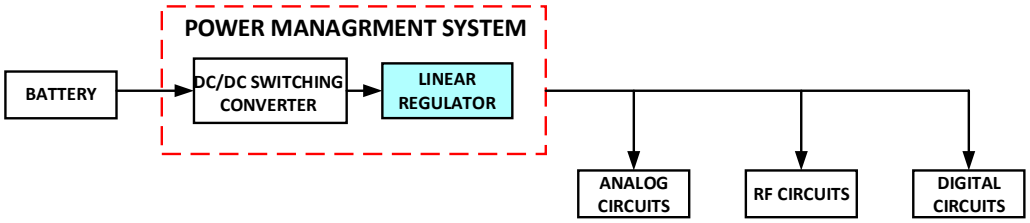


Figure 1. Voltage Regulator in a Power Management System.

There are various parameters for the gross evaluation of a linear regulator, namely, dropout performance, quiescent current, line regulation, load regulation, transient response, power supply rejection ration, die area, and power consumption. Moreover, researchers integrating significant parameters of their design to specify a compact effect of their design propose several mathematical approaches. This review presents an overview of the design strategies reported in the literature to build high-performance linear regulators, especially low-dropout (LDO), that are proven as convenient for versatile applications. Several types of LDO designs are discussed, both from the circuit implementation and the performance parameter perspective.

2. Background

2.1. Overview of Different Categories of Voltage Regulators

A voltage regulator is an integral part of the power management system (PMS) of all electronic devices and it has been the focal point of research over the past few years. The basic block-level architecture of a voltage regulator is shown in Figure 2, which consists of a reference voltage, a feedback network, and a comparator circuit. Figure 2 represents a general block diagram of a voltage regulator.

The voltage sensed at the output terminal is redirected to the comparator circuit through a feedback network that is matched with the reference value set at the comparator. Whenever the comparator circuit discerns any voltage variation, it instantaneously drives the control element to a suitable operating point so as to ensure regulated output voltage. Then, the comparator sends the error signal to the controller, which produces the corrected and regulated output.

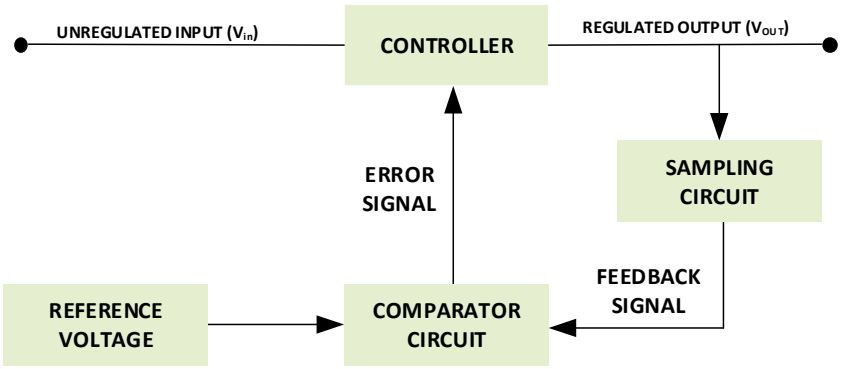


Figure 2. The Block Diagram of a Voltage Regulator.

Voltage regulators can be divided into two categories, as depicted in Figure 3, in terms of their principle of operation: (1) linear voltage regulator and (2) switching voltage regulator. The main difference between these two categories arises from their pass transistor's region of operation. The pass element of a linear regulator varies according to the desired level of dropout voltage. When BJT is used as a pass element, the pass element requires high differential value between the input and output. However, when the difference is very low, the pass transistor needs to be operated in an active region to maintain a regulated output. Voltage-controlled FET devices are required to operate in the linear region when large load variation is involved as gate voltage varies according to the load current. On the other hand, FET devices need to set in the saturation region in case the load swing requirement is small. The linear regulator can also be divided into many classes such as a positive adjustable regulator, negative adjustable regulator, floating regulator, and low-dropout (LDO) regulator. However, LDO has become incredibly popular because of its potential and advantages, especially for applications in emerging technologies such as SoC, IoT, and wireless communication. The challenges of LDO designs have pushed researchers to employ novel circuit architectures in different domains such as analog, digital, and hybrid designs to obtain the desired performance trade-off.

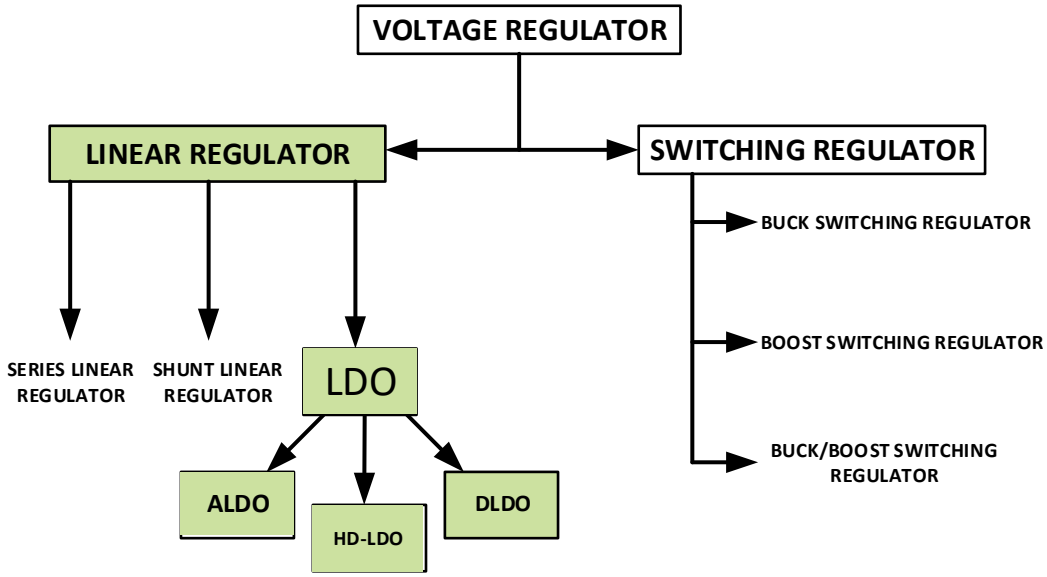


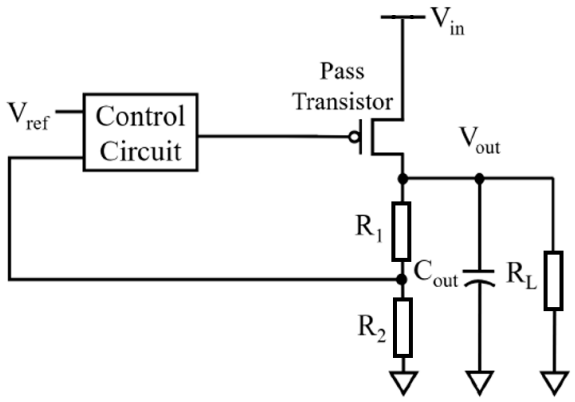
Figure 3. Classification of Voltage Regulator.

Continuous scaling with the inherent benefits of low-cost integration enables the CMOS-based approach to be a competitive platform to implement high-performance electronic devices. Hence, the trend of merging the linear regulator concept with CMOS

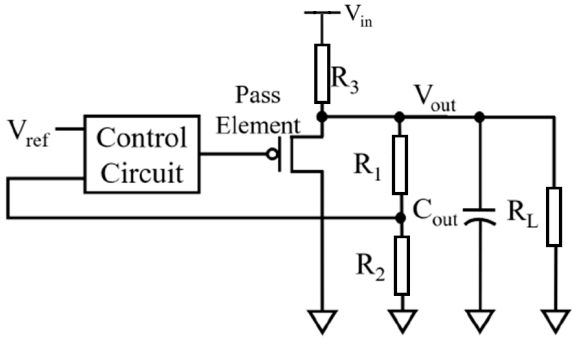
technology has been apparent over the past few years, considering the wide acceptability of CMOS technology and its superior functioning prospects.

2.2. Linear Regulator Scheme

When the pass transistor of a voltage regulator is operated in the ohmic or linear region, the regulator architecture is known as a linear voltage regulator. The active pass element (such as BJT or MOSFET) of the regulator exploits the linear or saturation region's characteristics to regulate the output voltage, as shown in Figure 4. Whenever the output diverges from the reference voltage, the current through the pass transistor is varied to obtain the desired output voltage. As a result, the difference between the input and output voltage is dropped in the active pass component, thus, wasting the power through heat dissipation. This type of regulator does not need an extra storage element for transferring energy. This model consumes a smaller area and is free from switching noise. However, it is less efficient than its switching regulator counterpart. Over the decades, the design trends of the linear regulator have evolved from simple series (Figure 4a) or (Figure 4b) shunt structures to several advanced architectures based on its novel topologies such as folded compensation cascode, buffer impedance attenuation, current steering, supercapacitor-assisted, and fast-response adaptive-phase, etc., for different application-specific applications [20–65].



(**a**)



(**b**)

Figure 4. Block Diagram of (**a**) Series Linear Regulator (**b**) Shunt Linear Regulator.

2.3. Low-Dropout (LDO) Voltage Regulator

As a significant amount of power is dropped in the transistor's pass element, which reduces the transistor's voltage drop, this has become a vital issue when designing a linear regulator. The continuous effort of minimizing dropout voltage has developed a new class of linear regulators called low-dropout (LDO) voltage regulators. Generally, when the transistor's dropout voltage is low, it is considered an efficient LDO voltage regulator in terms of power dissipation. As power dissipation is the product of dropout voltage and load current, the higher dropout voltage indicates that more power will be dissipated

as heat. The simple block diagram of LDO, as shown in Figure 5, consists of three main components: the error amplifier, pass transistor, and feedback network. Over the years, different potential techniques have been deployed in each component to meet the desired specification challenges. Several state-of-the-art topologies of LDO design in analog, digital, or hybrid domains are described, respectively, in the following sections.

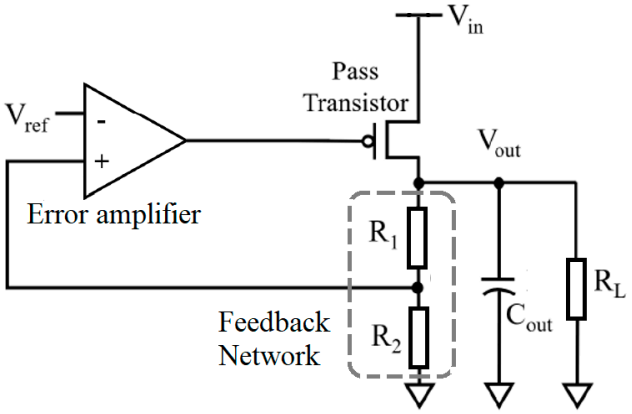


Figure 5. Basic Block Diagram of LDO Voltage Regulator.

2.4. LDO Design Parameters

LDO is one of the most fitting linear regulators that is widely accepted in power supply management due to its simplicity, as well as better performance. Following are the most common design parameters of LDO.

Dropout Voltage: Dropout performance is an important parameter when designing a low-dropout linear regulator. The effects of system parameters, dropout performance, and device parameters are interconnected. System parameters have an impact on the LDO's dropout performance that influences other device parameters. Generally, the summation of the voltage drop across the pass transistor and the output voltage are approximately equal to the input voltage, where the voltage drop is a function of the minimum dropout resistance, RDS, which is the function of the size of the pass element. The error amplifier ensures the desired operating point of the pass transistor so that the output can be maintained at an appropriate level.

Dropout voltage ($V_{DROPOUT}$) can be defined as the voltage deviation of the output voltage from the input voltage. At dropout voltage, the LDO cannot tune voltage anymore with a further reduction in the input voltage. Mathematically, it can be expressed as the multiplication of load current (I_{LOAD}) and drain-to-source resistance (R_{DS}).

$$V_{DROPOUT} = I_{LOAD} \times R_{DS} \tag{1}$$

Quiescent Current: Quiescent or ground current (I_Q) is the differential current between input and output. It is the minimum current necessary to operate the LDO's internal circuitry, such as bandgap reference, error amplifier, and output voltage divider when there is no external load current. Several factors such as temperature and topology can affect this value. It can be expressed as

$$I_Q = I_{INPUT} - I_{OUTPUT} \tag{2}$$

Line Regulation: The unit line regulation defines the LDO's aptness to conserve a specific output voltage (ΔV_{OUT}) against varying input voltage (ΔV_{IN}). It is defined as

$$LINE\ REGULATION = \Delta V_{OUT} / \Delta V_{IN} \tag{3}$$

Load Regulation: Load regulation is a standard used to define the LDO's capacity to sustain a particular output voltage upon a range of output currents (ΔI_{OUT}) for diverse load conditions. Load regulation is defined as

$$LOAD\ REGULATION = \Delta V_{OUT}/\Delta I_{OUT} \tag{4}$$

Transient Response: The transient response is a measure used to record output voltage variation for a step-change in load current. It depends on several metrics such as slew rate, equivalent series resistance (ESR), and output capacitor

Power Supply Rejection Ratio: Power supply rejection suggests the LDO's ability to block the swing of the regulated output voltage. PSRR is a dimensionless quantity, whereas PSR is expressed in dB. PSR can be written as

$$\text{PSRR(dB)} = 20\log(\Delta\text{VIN} = \Delta\text{VOUT}) \tag{5}$$

$$\text{PSR(V = V)} = \Delta\text{V OUT} = \Delta\text{V IN} \tag{6}$$

Figure of Merit (FOM): The calculation of figure of merit (FOM) is widely adopted by researchers and acts as a collective measure of all other performance parameters. The most established equation for calculating FOM is included in Equation (7), which is adopted by many researchers [19–23,45,47,48,51–58,60,62]. Moreover, several methods of evaluating FOM is presented by authors to signify their design performances, which are added in Equation (8) [25], Equation (9) [44], Equation (10) [58], Equation (11) [59], Equation (12) [51], and Equation (13) [48].

The FOM of capless LDO can also be calculated [62] using Equation (7) where total capacitance is equal to output load capacitance and on-chip capacitance is zero. Moreover, researchers have proposed the FOM equation for comprehending the minimum channel length [48] and output power at which ripple is present [25] to reflect the power consumption and active area performance, while others mentioned those parameters separately. In this review, Equation (7) is considered standard as many researchers utilize it repeatedly. Considering the existing FOM equations, it is apparent that FOM cannot demonstrate the overall performance of LDO in a single quantity; rather, other parameters have to be taken into consideration to fully indicate the performance of an LDO. However, a new computational concept may be proposed integrating other key parameters of LDO design such as fabricated area, power dissipation, and dropout performance that can provide a holistic assessment of the performance of the circuit in a compact form.

$$FOM\ (s) = C_{TOTAL} \times \Delta V_{OUT} \times {}^{I_Q}/_{{I_{Lmax}}^2} \tag{7}$$

Here, C_{TOTAL} is the equivalent capacitance of on-chip capacitance and output load capacitance. ΔV_{OUT} is the differential between voltage measured at minimum load current (I_{Lmin}) and voltage measured at maximum load current (I_{Lmax}). I_{Lmax} is the maximum load current. I_Q is quiescent current.

$$FOM_{ripple}(\text{F/A}) = \frac{V_{ripple} \times C_T}{P_{max}} \tag{8}$$

Here, V_{ripple} is the output ripple voltage. C_T is the total capacitance. P_{max} is the output power at which ripple is measured.

$$FOM\ (V) = R_R \times R_E \times \frac{\Delta V_{OUT} \times I_Q}{\Delta I_{OUT}} \tag{9}$$

Here, R_R is the settling time ratio, R_E is the edge time ratio, ΔI_{OUT} is the difference between the largest and the smallest output current.

$$FOM\ (s) = \frac{Droop\ Recovery\ Time}{Load\ Step} \tag{10}$$

$$FOM\ (Hz) = Power\ Supply\ Rejection \times Peak\ Power\ Efficiency \tag{11}$$

$$FOM\ (F) = C_{TOTAL} \times \frac{\Delta V_{OUT}}{V_{OUT}} \times {}^{I_Q}/_{\Delta I_{LOAD}} \tag{12}$$

Here, V_{OUT} is the output LDO voltage.

$$FOM\ (V.s) = T_{Edge} \times \Delta V_{OUT} \times {}^{I_Q}/_{\Delta I_{LOAD}} \tag{13}$$

Here, T_{Edge} is the transition time of I_{LOAD}.

Efficiency: The efficiency of an LDO is roughly the ratio of the output voltage to the input voltage (considering negligible I_Q) and can be expressed as

$$EFFICIENCY = I_{OUT}/(I_{OUT} + I_Q) \times V_{OUT}/V_{IN} \times 100\% \tag{14}$$

3. LDO Design Topologies

With the progress of CMOS technology and application-specific metrics' requirements, the LDO design approach has transfigured significantly over the past few years. This enthralling design scenario has intrigued researchers to improvise their circuit architecture with novel topologies in different domains. A conventional analog LDO (ALDO) with an external capacitor provides good power supply rejection ratio (PSRR) and a transient response. However, it occupies a large area, which usually lessens the system's reliability. With this pitfall, the designers have approached the capacitorless or "Capless" LDO voltage regulator scheme, which significantly deteriorates the PSSR and transient response performance. Moreover, technology scaling has intrigued researchers to shift their research focus towards the digital domain, which gives rise to a new branch of LDO design called digital LDO (DLDO). However, the switching nature of DLDO produces ripples in output voltage that, in turn, influence PSRR value. Hence, to address the issues mentioned earlier, the designers tried to exploit both ALDO and DLDO together and propose a new hybrid or mixed-mode structured design. Detailed specifications of different performance parameters of reported ALDO, DLDO, and HD-LDO with their respective circuit topologies are appended in Tables 1–3, respectively. Although it is hard to compare different types of LDOs, the categorization of discrete LDO architectures can aid researchers for both application-specific and parameter-specific researches on LDO architecture. Figure 6 gives the general classifications of LDO architecture with their offered advantages and disadvantages. In general, it is observed that the ALDO exhibits less ripple in output voltage and offers comparatively better PSSR compared to its DLDO counterpart. On the other hand, the DLDO, mainly, can work with smaller power transistors, has less load dependency, and is more reliable in nature. The HD-LDO (mixed-mode) has the flexibility to adopt the advantages from ALDO and DLDO based on the specifications and requirements of the device.

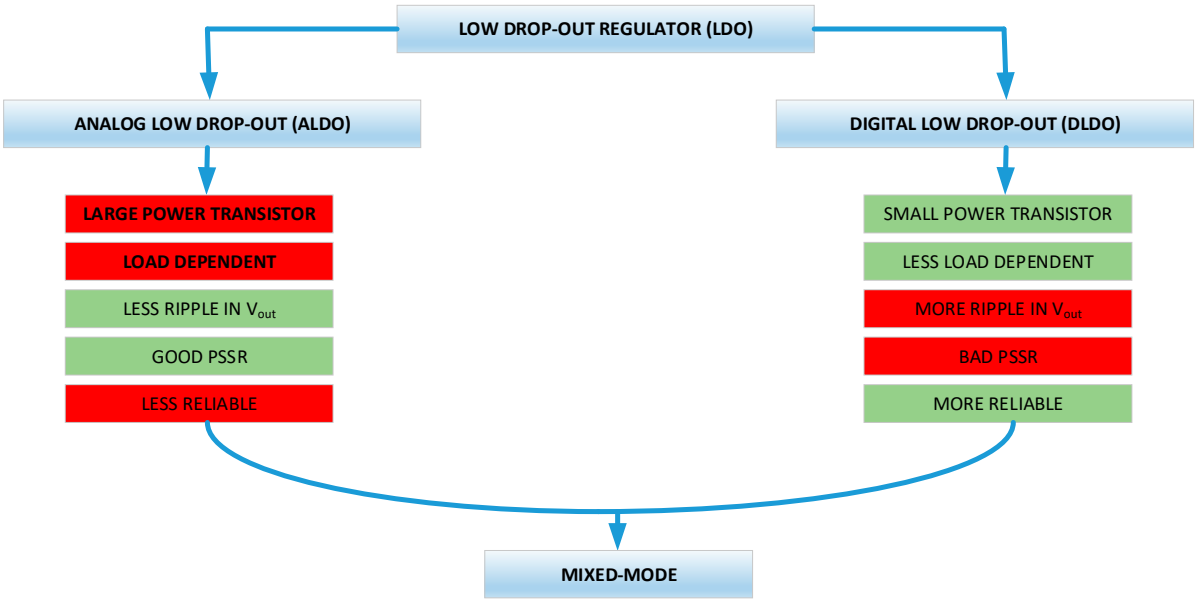


Figure 6. Characteristics of different types of LDOs.

3.1. ALDO Design Topologies

The fundamental architecture of an ALDO, as illustrated in Figure 7, incorporates a voltage reference, an error amplifier, a feedback network, and a pass transistor. An ALDO has a closed-loop architecture, hence, an efficient feedback design is necessary to maintain stability. Therefore, one of the designer's goals is to achieve a low quiescent current so that the feedback can operate steadily with high current efficiency. Another design challenge of ALDO is to attain high PSSR with the fast transient response; hence, an additional load capacitor is appended. However, this extra component consumes a large area, which has convinced researchers to model "Capless" ALDO. Moreover, several circuit techniques are amalgamated in other ALDO blocks according to application specifications to improve ALDO's overall performance, as illustrated below.

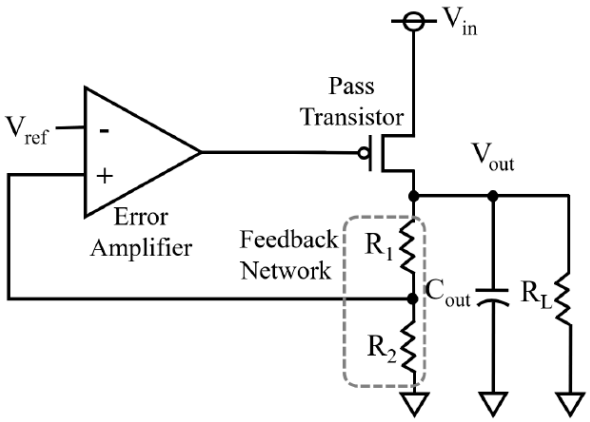


Figure 7. The basic structure of a conventional ALDO [40].

3.1.1. Folded Compensation Cascode Topology

A conventional ALDO is demonstrated by Lin et al. (2008) in Figure 8, which implements an active-frequency compensation scheme in order to solve the LDO stability problem [21]. A pseudo-differential technique has been adopted in the frequency compensation circuit with a boosted effective current multiplication factor that generates two similar DC voltages VA and VB, which causes a reduction in the voltage difference at the VA node. An on-chip capacitor, a cascode current-mirror, and a cascode bias current source

are employed to reduce the offset current, which, in turn, stabilizes the LDO output voltage. In the proposed design, the supply voltage requirement is minimized by applying folded cascode topology.

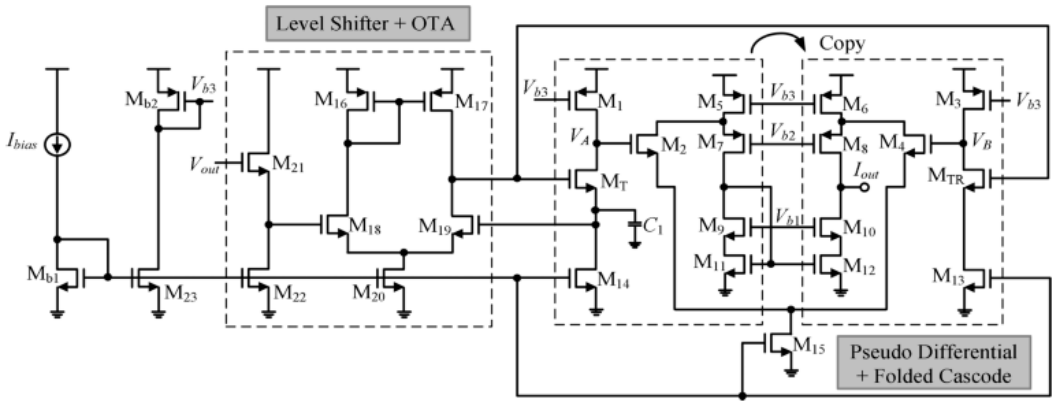


Figure 8. The basic structure of a conventional ALDO [40].

3.1.2. Buffer Impedance Attenuation Topology

M. Al-Shyoukh et al. (2007) proposed a buffer impedance attenuation (BIA) method that drives the pMOS pass device to improve the performance of LDO [22]. Here, dynamically biased shunt feedback causes a reduced output resistance in the buffer, which, in turn, pushes the poles at the gate over the unity gain. Therefore, this process dissipates low-level quiescent current. Figure 9 shows the structure of the LDO implementing the current buffer compensation scheme. The LDO is combined with a bandgap voltage reference of 1V, provided at the error amplifier input. The simple active load connected with the diode generates lower output resistance in comparison with the cascade load that causes the compensation capacitor to lower its value and reach a specific phase margin. Their proposed LDO keeps the error amplifier gain higher than 50dB [22].

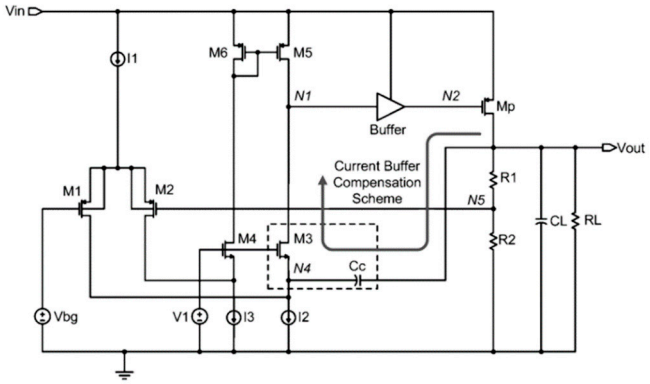


Figure 9. Structure of the LDO using the current buffer compensation scheme [22].

3.1.3. Current Steering—Fast Transient LDO

An LDO with a fast transient response is reported by Saberkari et. al. (2013), which utilizes the current steering approach as shown in Figure 10 [23]. A current feedback amplifier (CFA) basically constitutes the control mechanism in the pass transistor. The CFA combines an inverting output buffer and one open-loop voltage follower. The output signal is fed to the CFA along with the feedback network. Therefore, it is contrasted with a reference voltage, and the result is amplified, which controls the pass transistor gate. Fast transient response is obtained through the low impedance at the input of CFA [23].

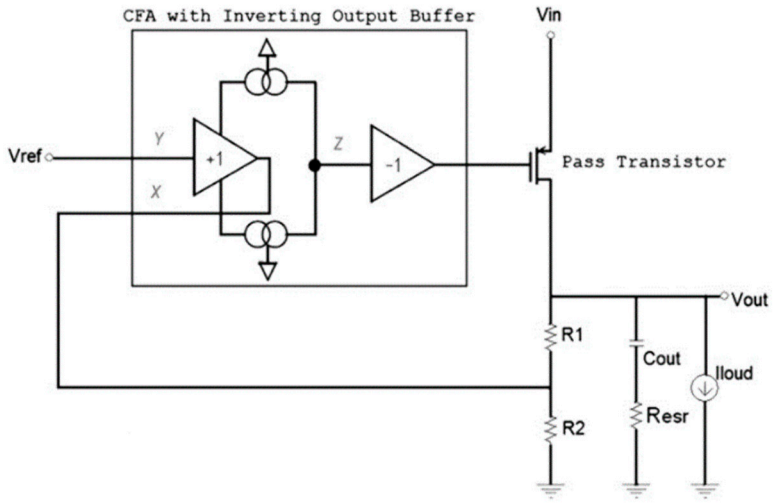


Figure 10. LDO architecture based on CFA [23].

3.1.4. Current-Mode Feedback Buffer Amplifier-Based LDO

A current-mode feedback buffer amplifier is designed in CMOS 0.25 µm technology to overcome the LDO linear regulator's common drawbacks, as visualized in Figure 11 [19]. A dual feedback design is implemented where a precise steady-state operation is obtained through global voltage-mode feedback, and fast transient response is received using a current feedback amplifier (CFA) [41]. The design comprises a voltage feedback amplifier (VFA) based on an operational transconductance amplifier (OTA), a second stage CFA, a regulation FET, and a feedback network. The second stage CFA helps in minimizing the settling time of output and reducing the slew rate. On the other hand, accuracy is obtained in a steady-state by the global voltage-mode feedback.

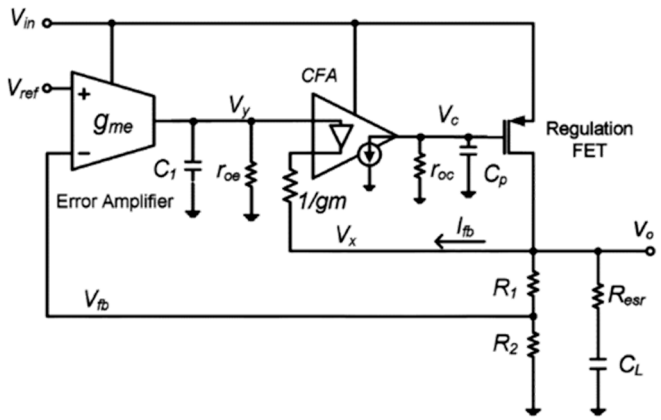


Figure 11. LDO architecture using CFA-based buffer amplifier [19].

3.1.5. High-Speed Compact Output Driver-Based LDO

A novel architecture of a capacitor-CMOS LDO reported by Saberkari et al. (2013), as shown in Figure 12, used a compact NMOS output driver. The output driver cell generates a low voltage ripple and achieves a fast transient response under large load steps within a minimum chip size [23]. The LDO can generate output voltage as a function of VDD for two different load currents (100 µA and 14 mA). The developed LDO required a 1.8 V of VDD and the LDO's output voltage follows the input voltage power supply.

The operation of the LDO under dynamic load conditions was simulated using an SoC load model [42]. The power routing digital core of a microcontroller was back-annotated into a schematic view, resulting in an equivalent circuit with a total capacitance of 2.25 nF and 125,000 gates. The load was modeled by using 40% of these gates toggled simultaneously in each clock cycle. The worst-case scenario concerning the microcontroller unit

(MCU) operation modes occurs when the MCU is taken from an ultra-low power mode to an active mode when the CPU and all peripheral modules are active [23]. Thus, to simulate the developed LDO under these dynamic conditions, the clock frequency is initially f_{ck} = 250 kHz (typical of a low-power mode operation). After 14 µs, the clock frequency is increased to f_{ck} = 16 MHz (representing an MCU running in a high-power mode).

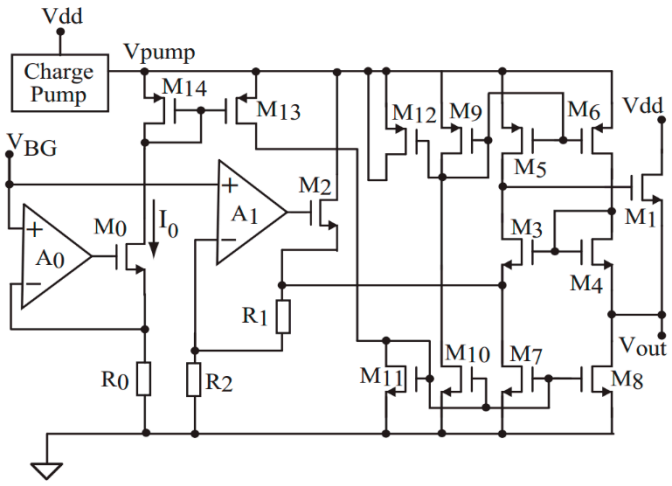


Figure 12. The LDO with compact output driver [23].

3.1.6. Supercapacitor Assisted LDO

Recent developments have led to a wide variety of supercapacitors ranging from fractions of farads to several thousand farads. Simultaneously, the equivalent series resistance (ESR) can vary up to several hundreds of milliohms. Voltage ratings of supercapacitor modules can exceed 100V, whereas the single-cell devices reach about 4.0 V [24]. Applications include memory backups, surge absorption, wind energy, and portable devices [13,24].

A simple variation of the supercapacitor topology [24] is shown in Figure 13. Figure 13a demonstrates the first phase where the input voltage of the LDO drops to the lowest value $V_{in(min)}$ during the charging period of the supercapacitor. In the next step, the supercapacitor and input of LDO are connected in parallel to losing the stored energy, displayed in Figure 13b.

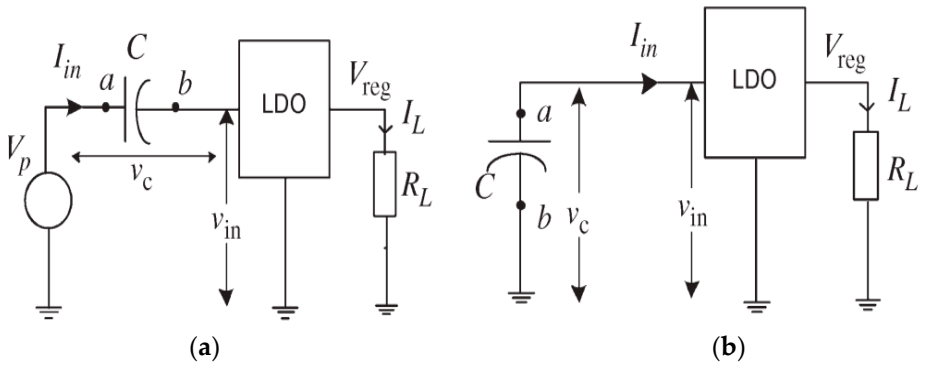


Figure 13. Concept of supercapacitor energy recovery: (**a**) minimizing the series element dissipation; (**b**) reuse of stored energy in the supercapacitor [24].

3.1.7. Fast-Response Adaptive-Phase LDO

The 65nm CMOS technology was used to design an improved DC–DC converter with a fast-response adaptive-phase (fast-RAP) digital controller [25]. Compared to cascaded linear regulators, fast-RAP controllers have a quicker response rate, and, thus, these controllers will maintain a good transient response. This design is capable of enhancing line

and load regulations of the charge pump and can develop efficient standalone linear regulators. Without the need for further step-ups, this method can lower dropout voltage, as displayed in Figure 14. In the presence of a high load transient, all the phases are activated simultaneously. A clock tripler is also required to maintain the transient response while assisting in the implementation of an adaptive-phase scheme [25].

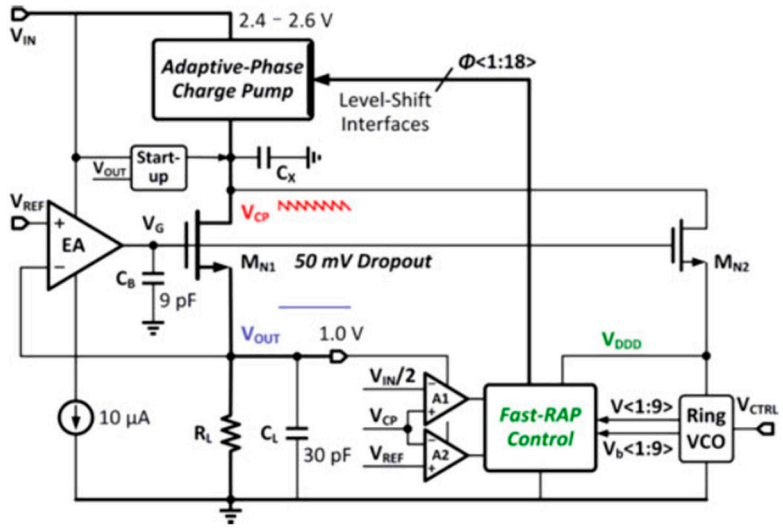


Figure 14. Block diagram of the fully integrated regulated switched capacitor dc–dc converter with fast-RAP control [25].

3.1.8. Feedforward Compensated High-Voltage Linear Regulator LDO

A unique framework of the linear regulator with high current sinking potential targeting the capacitive micromachined ultrasonic transducer (CMUT) technology [43]. The regulator embodies a high voltage NMOS pass transistor, feedback network, an error amplifier, and a biasing resistor, depicted in Figure 15. The feedback network consists of two high voltage N-doped poly resistors utilized to intuit any anomaly in output voltage. Furthermore, the transistor's channel length and width are adjusted in such a way that provides minimal resistivity to subside gate capacitance.

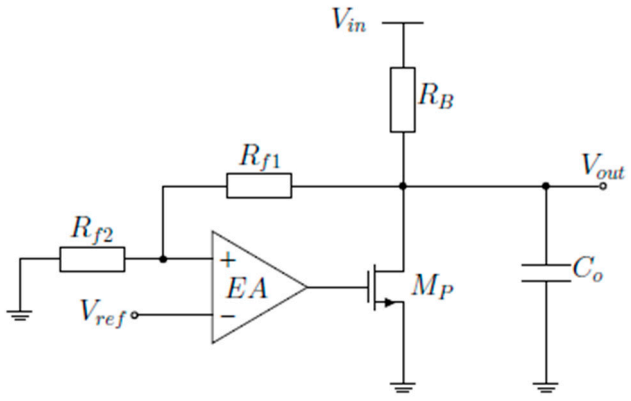


Figure 15. Feedforward Compensated High-Voltage Linear Regulator [43].

3.1.9. High Power Supply Rejection Linear Regulator LDO

A design proposed by Chen et al. (2020) provides several appealing features, including high power supply rejection (PSR), wideband ripple filtering, and fast transient response [44], as shown in Figure 16. The linear voltage regulator of the design incorporates four blocks: (1) an N-type pass transistor, (2) output-supplied voltage reference circuit, (3) charge pump, and (4) dual feedback system. Bypassing the usage of a voluminous decoupling capacitor is considered one of the fascinating aspects of this design, while the

shortfall of decoupling capacitance is tackled by a two-stage feedback structure comprised of a high-gain and a wide-bandwidth path. Additionally, a deep N-well NMOS is employed to cope with the fluctuating output voltage, which escalates the breakdown voltage to 2.8V from 1.8V and neutralizes the body effect.

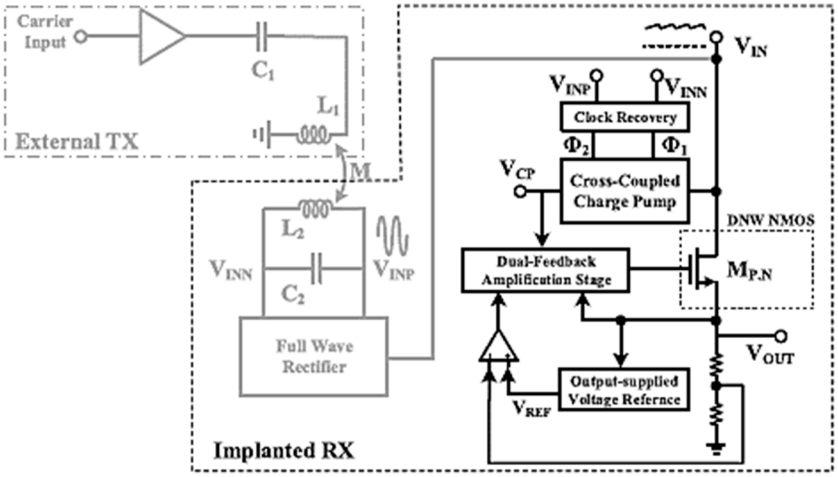


Figure 16. High PSR linear regulator [44].

3.1.10. Concurrent Bulk Modulation and Forward Body Bias

An innovative structure for a low-dropout (LDO) regulator suitable for the sub-1-V supply [45] is demonstrated in Figure 17. The primary blocks of this design are a common-source-configured PMOS, rail-to-rail error amplifier (EA), buffer (BUF), and load current generator (LCG). The adaptive biasing technique, efficient forward body biasing (FBB), modified driving concept, and novel concurrent bulk modulation approach enables this design to accomplish the desired characteristics. In this design, the buffer is engineered based on a differential flipped voltage follower (FVF) that demonstrates approximately zero voltage shifting from input to output. Additionally, LCG provides the required bias current to maintain the loop stability when the load current is zero.

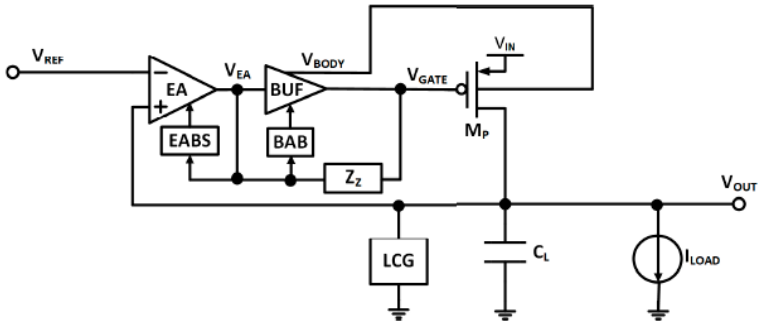


Figure 17. Concurrent Bulk Modulation and FBB-Based ALDO [45].

3.1.11. Current-Mode Feedforward Ripple Canceller

A linear low-dropout regulator, as illustrated in Figure 18, is reported by Joshi et al. (2020) adopting a current-mode feedforward ripple canceller (CFFRC) in order to facilitate high power supply rejection (PSR), fast load transient response, and low quiescent current, simultaneously [46]. The LDO architecture integrates the PMOS power FET, power FET driver buffer, folded cascade error amplifier (EA), CFFRC amplifier, and compensation network. The benefits of both the feedforward and the current-mode technique are optimized in a single circuit. The feedforward approach is convenient to maintain low quiescent power consumption and reduce noise by adjusting the impedance ratio. The current-mode

is chosen over the voltage-mode due to its inherent ability to improve PSR without the cost of padding extra circuit elements.

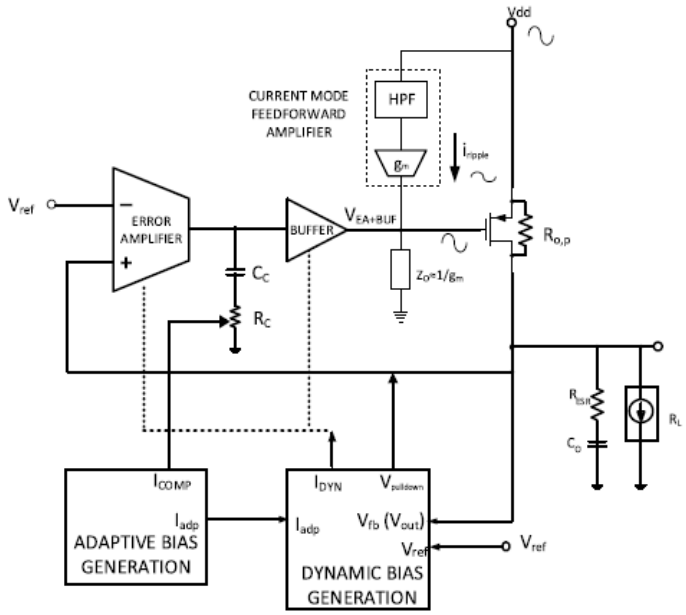


Figure 18. Current-mode FFRC-based ALDO [46].

3.1.12. Negative Charge Pump-Enhanced (NCPE) LDO

The analog LDO depicted in Figure 19 was implemented especially for low-voltage applications [47], ensuring a balance between the power supply and the efficiency. The amplification is performed in two distinct stages: the error amplifier (EA) stage and the gain stage. The negative charge pump's output is linked with the ground terminal of both amplifiers. The power transistor is powered by the outcome of the gain stage amplifier, which increases load regulation. As the NCP is not connected directly with the power transistor, it cancels the possibility of adding ripples.

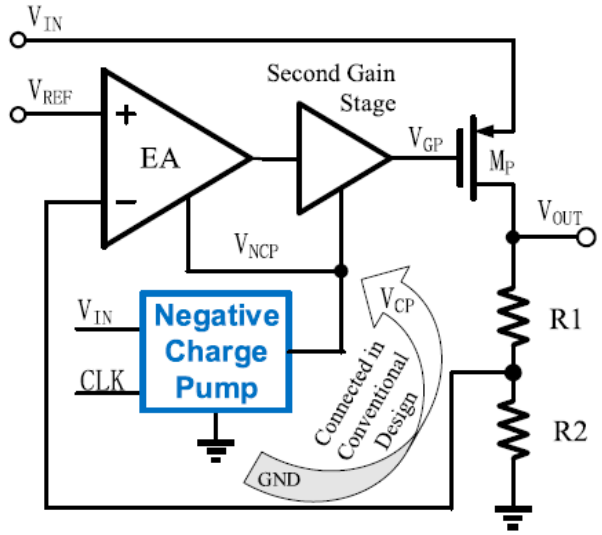


Figure 19. Negative Charge Pump-Enhanced ALDO [47].

3.1.13. Low-VDD Inverting Buffer with Efficient Feedforward Path

An LDO design by Park et al. (2020), as illustrated in Figure 20, uses a low-VDD inverting buffer and an efficient feedforward path to produce a high-performance inverting buffer with additional transistors and capacitors [48]. Though it consumes extra area

compared to the traditional buffer circuits, it eliminates the pole-effect, hence upgrading the PSSR performance of LDO. Moreover, the feedforward path is engineered as such by replacing constant current sources with dynamic current sources. This approach allows the output signal to bypass the high impedance node, thus improving stability.

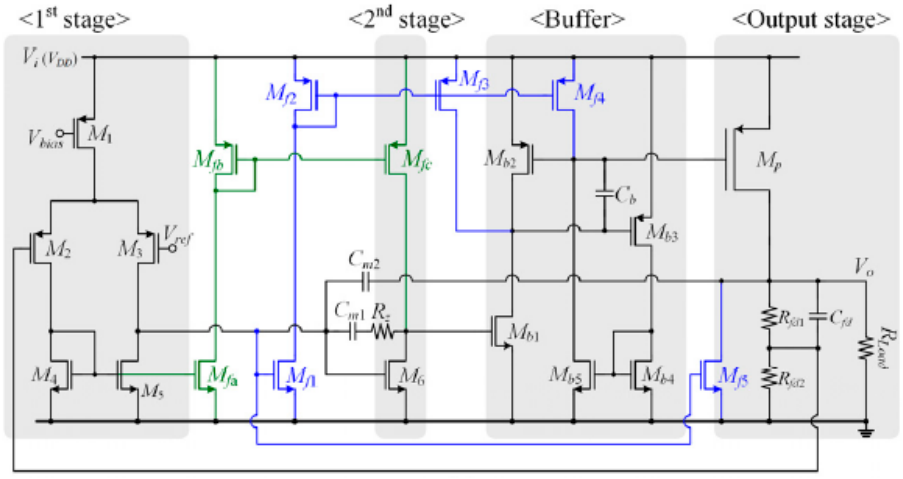


Figure 20. Low-VDD Inverting Buffer-based ALDO [48].

3.1.14. Multistage Error Amplifier and PRDTRA-Based LDO

An LDO design especially for low-power SoC applications has been demonstrated by Huang et al. (2020), as shown in Figure 21 [49]. The idiosyncrasies of this architecture are a multistage error amplifier (EA) accompanied by the transient acceleration pulse generator (TAPG) and a feedback network optimized by a programmable recursively divide by two resistor array (PRDTRA). The error amplifier contains three successive stages: the main gain stage, the gain-boosting stage, and the output stage. The common-mode rejection ratio (CMRR) of the output stage cancels the power noises transmitted through the previous two steps. A TAPG also follows the output stage to provide an additional route to enlarge the transient response. Moreover, the circuit optimizes the PRDTRA algorithm to achieve the scaling of the output voltage.

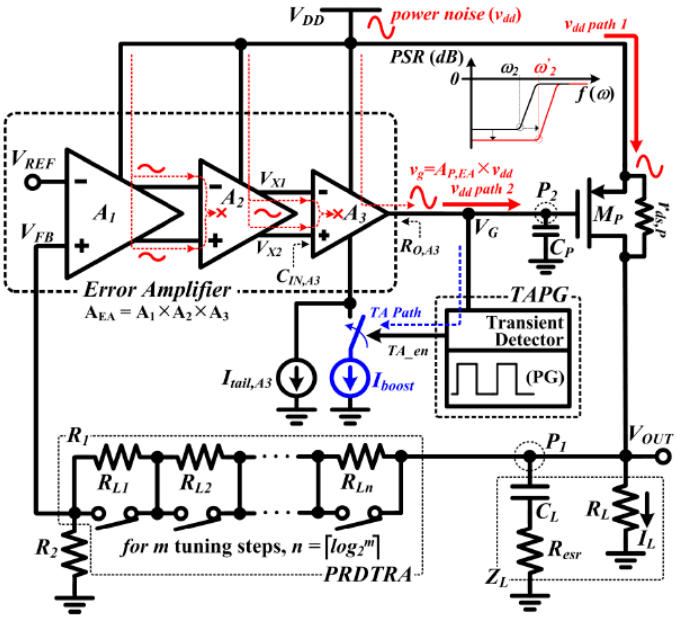


Figure 21. Multistage EA and PRDTRA-Based LDO [49].

3.1.15. Switched RC Bandgap Reference LDO

A low-noise LDO circuit implemented for noise-sensitive mixed-signal applications is shown in Figure 22 [50]. The LDO circuit is vulnerable to various noises such as thermal noise, shot noise, flicker noise, etc. A sample and hold switched RC filter eliminates the noises produced by the bandgap reference circuit and scaling amplifier before entering the error amplifier. The flicker noise generated by the two-stage error amplifier is filtered using the drain-side modulated current-mode chopping technique. The ripples created at the EA are suppressed by a switched capacitor (SC) notch filter. Furthermore, a first-order passive RC filter is also introduced to cancel the noise in the bias circuit.

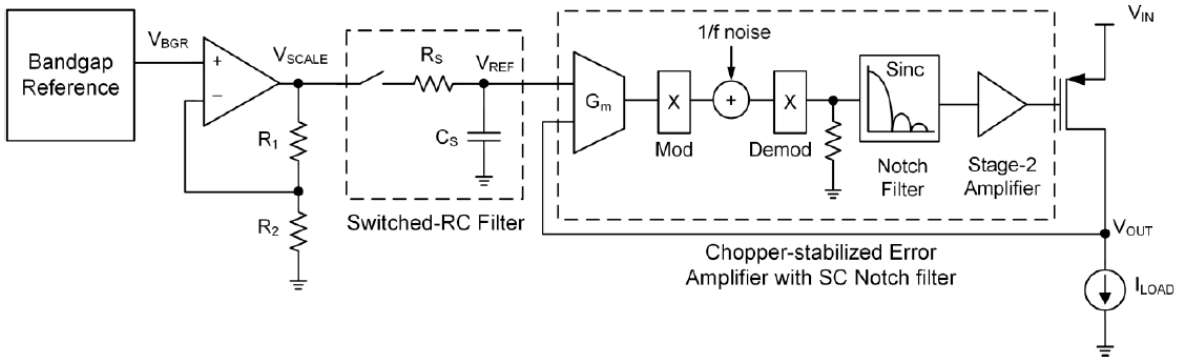


Figure 22. Switched RC Bandgap Reference ALDO [50].

3.1.16. Voltage Difference to Time Converter with Direct Output Feedback

A low-dropout regulator scheme modeled based on a voltage difference to time converter (VDTC) was reported by Shin et al. (2020), as given in Figure 23 [51]. Extracting attributes from both digital and analog LDOs, the design yields a ripple-free output and small quiescent current over a broad range of operating voltage. The structure contains a VDTC, a power transistor, a charge pump, and a coupling capacitor. The VDTC performs the role of sensing the difference between the reference and the output voltage, and the result is updated in every clock cycle. Moreover, the load current can be adjusted quickly during rapid transition through an optimized direct output feedback loop.

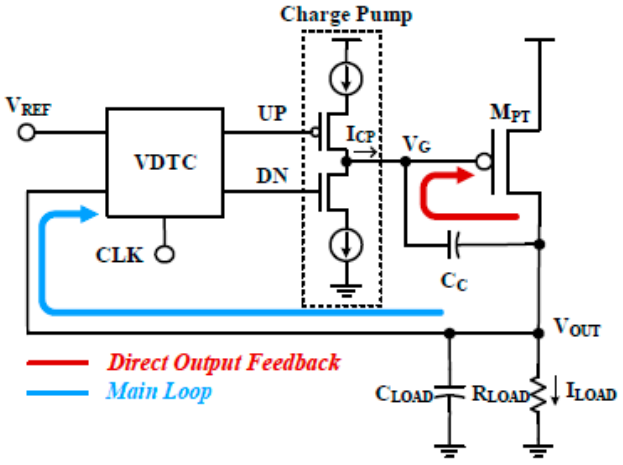


Figure 23. VDTC-Based ALDO [51].

3.1.17. Performance Comparison of ALDO

Table 1 reflects the comparative analysis of several ALDO architectures with respect to their performance metrics. The data listed in the table signify the design flexibility of ALDO according to the application-specific considerations. Among several designs, the best LDO performance in terms of maximum allowable current conveyed is 600 mA [48],

which is a significant improvement as it allows a current value almost three times larger than the second-best I_{max} value reported [22]. Recent advances in ALDO design prefer capless architecture because of its acceptability in fully on-chip implementation as well as economical considerations. In the aforementioned table, some designs offer capacitorless architecture [48,50], whereas one design has the lowest output capacitor requirement (0.05 µF) [19] compared to others. Quiescent current is another important parameter of LDO design as it expresses the minimum current requirement of the internal circuitry of LDO. Therefore, the smaller the quiescent current, the better the LDO design. The necessary quiescent current is the minimum value, which is only 0.016 µA [45]. One design offers the minimum low-dropout voltage along with the maximum current efficiency [51]. There are a few other parameters such as dropout voltage and current efficiency that define the overall performance of LDO.

Table 1 also indicates the various kinds of circuit topology with respect to various designs where the important parameters of the specific circuit structures can be identified. The design in [48] supports the maximum load current and incorporates the concept of a low-VDD inverting buffer with the cost of an additional transistor and replacing the constant current source with a dynamic current source. Thus, it allows the output signal to avoid a high impedance path and improves the current value. Both the capacitorless architecture and architecture with capacitors have their advantages and disadvantages. Because of the off-chip capacitor, there remains a dominant pole at the output that ensures a good load and line regulation with better stability. However, the capacitor performance may degrade at a high frequency because of effective series inductance (ESR) and effective series resistance (ESR). On the other hand, capless architecture, a tempting choice for SoC applications, lessens the number of external pins and metal bonds, sacrificing the stable output pole. Design [50] achieves a capless architecture by improvising a low-pole passive RC filtering circuit in the bandgap reference (BGR) circuit to eliminate the noises created by the BGR circuit. The other capless design [48], introduces an efficient buffer circuit that alleviates the pole-up effect at a higher frequency, thus relaxing the necessity for an off-chip capacitor. Design [45] presents an optimized rail-to-rail buffer utilizing a differential flipped voltage follower (DFVF), which cancels out the use of an auxiliary amplifier for bulk modulation, thus limiting the quiescent current. In addition, there are several circuit techniques such as the current feedback amplifier, buffer impedance attenuation, folded cascode topology, dual feedback structure with charge pump, and multistage error amplifier with TAPG that are prominent in ALDO design. The objective of design [47] is to establish an LDO architecture that can be operated in a low voltage domain to enhance battery life. Therefore, the designer introduced a negative charge pump in the controller section to extend the voltage range of the error amplifier. Similarly, the design in [51] achieved a target of low voltage operation by using a different technique of a voltage to time converter with direct output feedback. On the other hand, the focus of design [49] was to achieve clean power by suppressing ripples, which is accomplished by adapting the concept of the multistage error amplifier. The linear regulator proposed in reference [43] is designed for a capacitive micromachined ultrasonic transducer (CMUT), where the driver circuit should switch between two discrete high-level voltages. The linear regulator designed in [43] is suitable for this kind of application, which reduces the additional circuit requirement similar to a level-shifter. Moreover, the input and output voltages of LDO proposed in reference [23] are 3–5 V and 2.8 V. Thus, the calculated dropout voltage is 200–2200 mV, which is capable of regulating a large voltage range. The LDO designs presented in [23,43] are for special applications only and are rarely considered as references for ALDO design.

Table 1. Summary of the ALDO performance comparison.

References	Process (μm)	I_{max} (mA)	V_{in} (V)	V_{out} (V)	C_{out} (μF)	I_Q (μA)	ΔV_{OUT} (mV)	V_{DROP} (mV)	Load reg. (mV/mA)	Line reg. (mV/V)	Current Efficiency (%)	Active Area (mm^2)	PSR (dB)	Topology	FOM # (ps)
[19]	0.25	50	2–2.5	1.5–1.97	0.05	100	0.47	530	0.08	N/A	99.8	0.23	43 @ 30 KHz	Current Feedback Amplifier	940
[22]	0.35	200	2.0	1.8	1.0	20	0.2	200	34	2	99.8	0.264	340 @ ILM	Buffer Impedance Attenuation	100
[21]	0.35	150	2.0	1.8	1.0	27	0.2	200	10	0	60	0.409	40 @ 20 KHz	Folded Cascade Topology	0.01
[23]	0.35	100	3–5	2.8	1	59–189	3	2200	0.025	13.5	99.8	N/A	>56 (0 Hz–100 Hz)	Current Steering Approach	17.7
[25]	0.65	30	2.5	1	39	10	195	50	0.2	0	80.3	0.154	2.8 @ 100 mHz	Adaptive Phase Scheme	0.085 and 0.08 n *
[50]	0.25	100	N/A	1–3.3	Capless	40	N/A	230	N/A	N/A	N/A	0.21	50 @ 10 KHz	Sample and Hold Switched RC Filter	N/A
[47]	0.065	45	0.6	0.5	10^{-4}	21	44	100	0.047	1	99.95	0.045	N/A	Negative Charge Pump	0.1037
[44]	0.18	11	1.3	1.09	N/A	276	45	210	0.015	0.6	N/A	0.105	−54 @ 10 MHz	Dual Feedback Structure with Charge Pump	10.49 and 0.677 mV **
[43]	0.18	0	70	66	0.066	288	0.17	4000	1.7	90	99.71	0.15	N/A	Feedforward Compensated Method	0.03
[45]	0.055	10	0.8	0.6	1	0.016	70	200	1.05	0.5	N/A	0.042	42.7 @ 50 KHz	Differential Flipped Voltage Follower	11.4
[49]	0.04	100	1.1–1.9	0.2–1.1	1	56	28	900	0.176	0.857	99.94	0.375	−60 @ 1 MHz	Multistage Error Amplifier with TAPG	157
[48]	0.5	600	1.5–5.0	1.3–4.8	5.1×10^{-6}	16.5	514	200	0.011	0.156	99.95	0.082	−26.7 @ 1 MHz	Low-VDD Inverting Buffer	0.00012 and 1.42 ns.mV ***
[51]	0.65	60	0.6–1.2	0.5–1.15	10^{-5}	0.1–10	111	100	N/A	N/A	99.99	0.086	N/A	Voltage Difference to Time Converter	0.000202 and 0.182 fF ****

All FOM values are calculated using Equation (7). * FOM is calculated using Equation (8). ** FOM is calculated using Equation (9). *** FOM is calculated using Equation (13). **** FOM is calculated using Equation (12).

3.2. DLDO Design Topologies

With the expansion of System-on-Chip (SoC) applications, the power management system requires LDO suitable for low-voltage operation. This scenario has drawn scholars to attempt to devise LDO in the digital domain. The basic model of DLDO contains a voltage reference, comparator, a digital controller, and an array of pass transistors. The switching nature of the DLDO transistor generates a significant amount of output ripple, thus degrading PSSR characteristics. Therefore, the primary concern of the DLDO design is to minimize the ripples. Furthermore, several approaches are employed in the controller part to avoid unnecessary operations to accomplish a fast response. Figure 24 illustrates the basic architecture of a conventional DLDO [52].

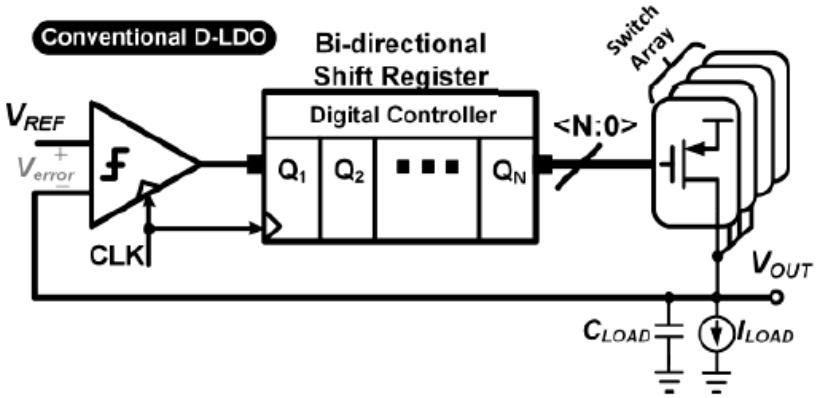


Figure 24. Basic Structure of Conventional DLDO [52].

3.2.1. Proportional Derivative (PD) Compensation and Sub-LSB Duty Control

An unprecedented design approach for a recursive digital low-dropout regulator (RDLDO), shown in Figure 25, demonstrates the potential for an optimal response time and improved load regulation range compared with the previous design [53]. This design utilizes a successive approximation (SAR) algorithm, Sub-LSB pulse width modulation (PWM) duty control technique, and proportional derivative (PD) compensation scheme to ensure a befitting substitution of analog LDOs. An efficient PD compensation configuration swiftly discerns the output voltage, which stamps out the overshoots and undershoots during SAR transformation and maintains stability. Sub-LSB PWM control brings forth gate voltage information that alleviates the DC accuracy limitation and output voltage peak-to-peak ripple limitation.

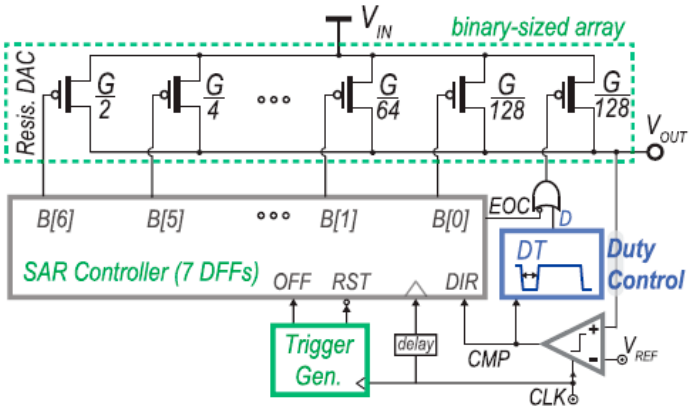


Figure 25. The architecture of PD Compensation and Sub-LSB Duty Control DLDO [53].

3.2.2. Fully Standard Cell-Based Digital LDO

With the evolution of CMOS technology, digital low-dropout (DLDO) regulators are continuously becoming popular among researchers because of their near-threshold voltage operation potentials. A standard cell-based DLDO regulator offers a small quiescent current and fast load transient response, as depicted in Figure 26 [52]. This design's fundamental components are a logic threshold-triggered comparator (LTTC), multi-mode detector, multi-loop switchable controller, and 12-bit binary-segmented MOS. The CMOS inverter-based LTTC keeps track of the difference between the reference and output voltage. The multi-mode controller section consists of three sub-sections: fixed-gain accumulator (FG-ACC), variable-gain accumulator (VG-ACC), and successive approximation register (SAR). Finally, the circuit achieves 99.97% current efficiency, which is the prime concern of a conventional DLDO design.

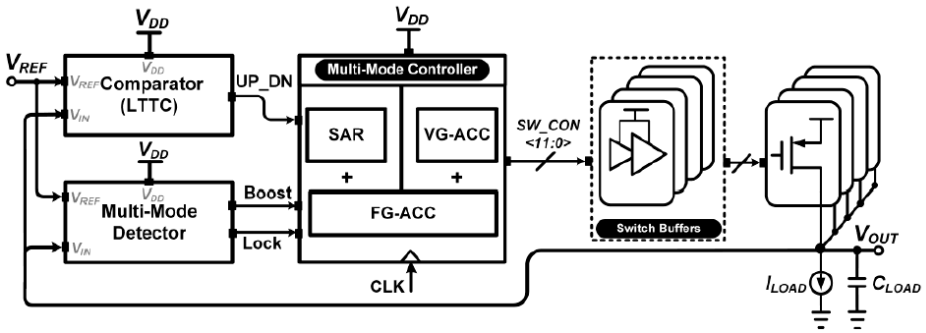


Figure 26. Fully Standard Cell-Based DLDO [52].

3.2.3. Coarse–Fine Dual Loop Digital LDO

Figure 27 shows a digital low-dropout (LDO) regulator suitable for mobile application processors (MAP). The two loops, such as a coarse loop and fine loop are used to control the output voltage [54]. Both loops have certain aspects in terms of performance parameters. For instance, the coarse loop utilizes a speedy current-mirror flash analog to digital converter (ADC), which provides a large output current and improves transient performance. The fine loop minimizes the ripples in voltage while supplying a low-level output current.

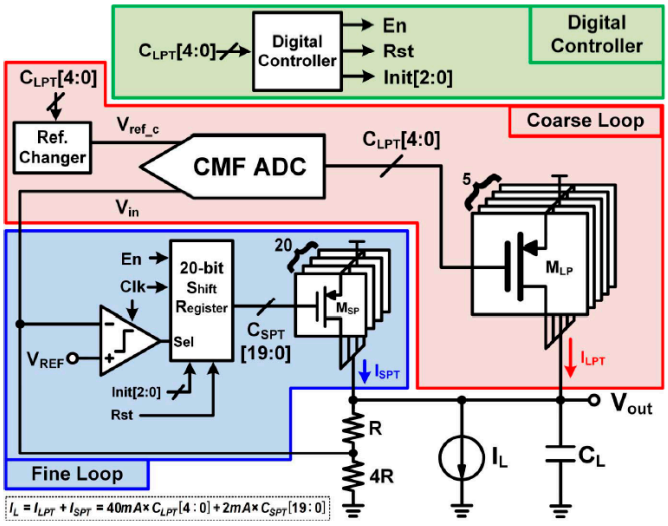


Figure 27. Coarse–Fine Dual Loop-Based DLDO [54].

3.2.4. Event-Driven Explicit Time-Coding Architecture-Based DLDO

Load current handling is a prime concern when designing a low-dropout voltage regulator. To manipulate the rapid fluctuation of the load current, a traditional DLDO

optimizes a high-frequency clock; however, this impacts the power efficiency and the transient response of the LDO. An event-driven strategy is utilized to address this issue in the design, as illustrated in Figure 28 [55], which avoids irrelevant operations by responding to a new event. The proposed architecture contains four primary blocks: a 3-bit continuous-time ADC, trigger generator, proportional-integral (PI) controller, and power transistor. Whenever a deviation from the seven pre-defined reference voltages is spotted, the trigger generator immediately delivers a signal to the PI controller. The PI controller's response decides the operation of the power transistor, thus controlling the required quantity of current to the load.

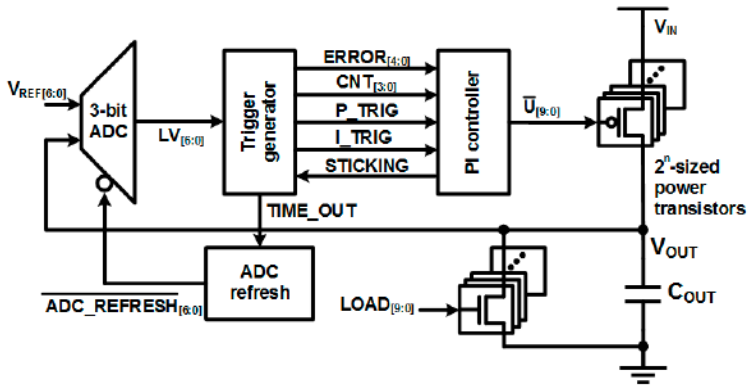


Figure 28. Event-Driven Explicit Time-Coding DLDO [55].

3.2.5. Beat-Frequency Quantizer and VCO-Based DLDO

A digital LDO using a beat-frequency (BF) quantizer, as shown in Figure 29, was introduced instead of a classic voltage quantizer [56]. The overall architecture of the DLDO comprises four components: a voltage-controlled oscillator, time quantizer, digital controller, and pass transistor. The proposed BF time quantizer is designed efficiently to adjust the sampling frequency according to the change in the operation mode (steady-state, overshoot). Adaptive voltage positioning (AVP) is exploited to cope with the voltage change and ensure good regulation and transient response performance.

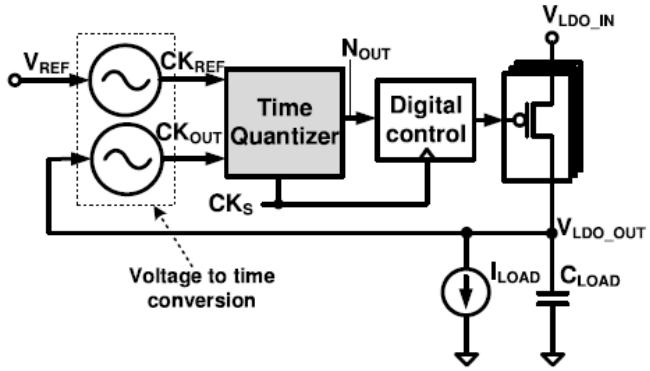


Figure 29. Beat-Frequency Quantizer and VCO-Based DLDO [56].

3.2.6. Time-to-Digital Converter (TDC)-Based DLDO

A time-to-digital converter (TDC)-based DLDO was implemented to upgrade the transient response, as shown in Figure 30 [57]. The proposed DLDO comprises three primary blocks: a TDC-based signal converter, digital controller, and PMOS array. Here, the time-to-digital converter (TDC) is preceded by a voltage sensor, which records the capacitor's charging time, thus achieving high linearity. Furthermore, this model's controller section is engineered using a digital PI controller rather than a conventional shift register, which allows for multi-bit operation in a single clock cycle; hence, it improves the transient response.

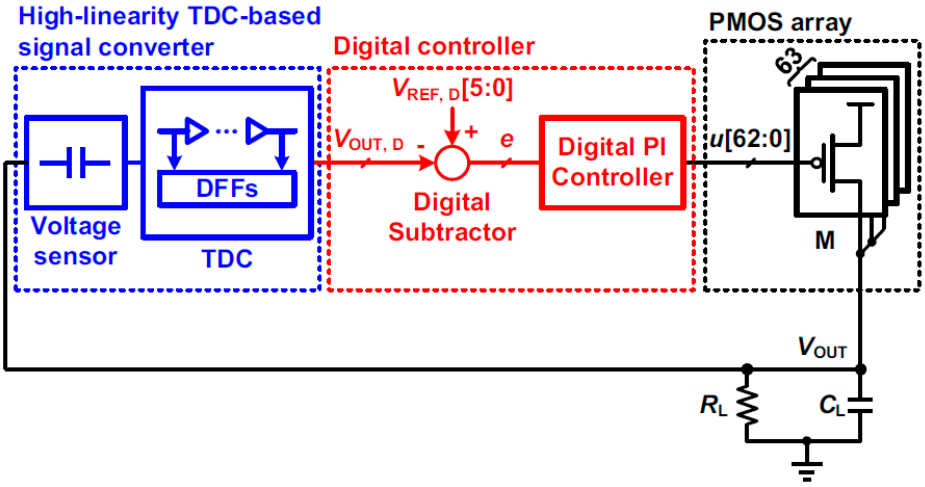


Figure 30. Time-to-Digital Converter (TDC)-based DLDO [57].

3.2.7. Performance Comparison of DLDO

Table 2 indicates the performance summary for the DLDO design parameters of the linear regulator schemes from previous researchers. FOM is a key criterion in evaluating the performance of CMOS linear regulators. The lower the FOM, the better the design. Packaging parasitic inductances, gate driving loss, and switching loss are some of the critical factors playing a role in regulating the FOM. Therefore, when the device is operating at a comparatively low frequency, FOM is good for evaluating materials and acts as a performance parameter in optimization. The lowest FOM of 1.11 ps was achieved by the design in [55] in the year 2017. The performance of FOM increases by the quiescent current over the maximum load current due to the time response of the processor. A lower FOM ensures an improved transient response. In this design, the researchers accomplished superior performance of the overall DLDO design by integrating several efficient modules such as a 3-bit continuous-time ADC, trigger generator, PI controller, and power transistor. The design in [53] shows the best result in terms of area consumption, occupying only 0.0023 mm^2. Again, design [52] shows the best output in terms of low quiescent current and maximum current efficiency. Here, the designer maneuvered a logic threshold-triggered comparator instead of a conventional comparator triggered by the clock frequency. Thus, the design reduces the current consumption and maximizes the current efficiency. Among several tabulated designs, the top architecture in terms of the off-chip capacitor is proposed by [56], requiring only 40 pF. In this design, the sampling frequency of the bit frequency quantizer responds with the voltage droop, hence, the successive clock edge comes faster. Due to this adaptive sampling technique, instead of fixed sampling, the circuit needs a low load capacitor. The maximum load current is achieved by design [54] as the flash analog to digital converter of this design consumes only static current. In addition, the prime concern of design [57] was to improve the transient response by replacing the traditional single-bit conversion technique with a multi-bit conversion technique. For this, the designer proposed a voltage sensor-based time-to-digital converter (TDC), which removes the reliance on the buffer gate's delay time to operate the TDC.

Table 2. Summary of the DLDO performance comparison.

References	[54]	[52]	[55]	[56]	[53]	[57]
Technology (nm)	28	65	65	65	65	65
V_{IN} (V)	1.1	0.7–1.2	0.5–1	0.6–1.2	0.5–1	0.7–1.1
V_{OUT} (V)	0.9	0.6–1.1	0.45–0.95	0.4–1.1	0.3–0.45	0.65–1.05

Table 2. *Cont.*

References	[54]	[52]	[55]	[56]	[53]	[57]
V_{OUT} (mV) @ I_{LOAD} (mA)	120@180	200@23.5	40@0.5VIN	108@50	40@1.06	371@80
$I_{LOAD,MAX}$ (mA)	200	25	0.0072–3.511	100	2	120
I_Q (mA)	0.2	0.006	0.012–0.216	0.1–1.07	0.014	0.495
Current Peak Efficiency (%)	99.94	99.97	96.3	99.5	99.8	99.6
C_{LOAD} (nF)	23.5	1	0.4	0.04	0.4	0.5
Load Regulation (mV/mA)	N/A	0.04	N/A	0.638	<5.6	0.6
Line Regulation (mV/V)	N/A	0.78	N/A	N/A	2.3	0.5
PSRR (dB)	N/A	N/A	N/A	–38@1MHz	N/A	N/A
Active Area (mm^2)	0.021	0.014	0.029	0.0374	0.0023	0.017
Response Time, T_R (ns)	N/A	N/A	N/A	N/A	15.1	2.1
FOM #	7.75 (ps)	2.17 (ps)	1.11 (ps)	1.38 (ps)	199 (ps)	8.7 (ps)
Circuit Topology	Current-mirror flash analog to digital converter (ADC)	Logic-Threshold Triggered Comparator	Event-Driven Explicit Time-Coding	Beat-Frequency Quantizer and VCO	PD Compensation and Sub-LSB Duty Control	Time-to-Digital Converter (TDC)

All FOM values are calculated using Equation (7).

3.3. HD-LDO Design Topologies

The prime drawbacks of ALDOs are their ability to control large transient currents, though they display better performance in terms of small signal regulation. Contrastingly, DLDOs exhibit accurate large signal performance, however, their overall performance degrades due to clocking and dynamic power consumption. Considering the amalgamation of both analog and digital loads and the necessity of discrete operating ranges in the same platform, designers have been required to merge the features of both ALDO and DLDO. Therefore, the mixed-mode LDO could employ the advantages of multiple power rails in the chip, and split the high-efficiency power conversion task through a low-dropout digital voltage rail, and achieve a satisfactory noise rejection capability through a high-dropout voltage rail. The basic architecture of the hybrid LDO is shown in Figure 31, which has an ALDO in parallel with a DLDO [58]. The DLDO branch undertakes the 80–90% majority of the LDO current with a coarse granularity power train. The quantization error of the coarse granularity is absorbed by the ALDO branch. Selected recent state-of-the-art works of the hybrid LDO design are described in the following section.

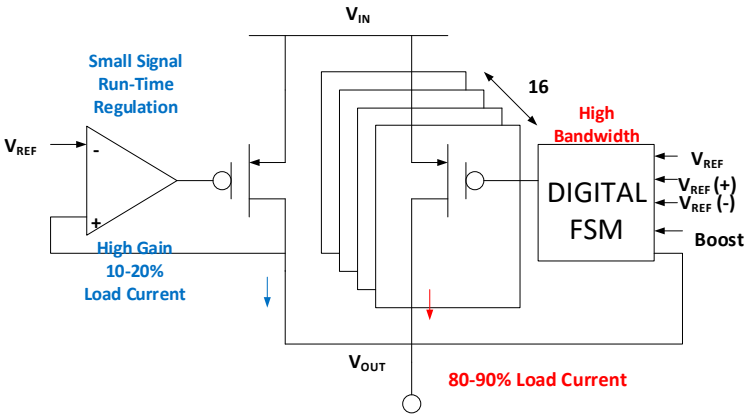


Figure 31. Basic Architecture of HD-LDO [58].

3.3.1. Scan Reconfigurable Hybrid LDO

A hybrid low-dropout (LDO) voltage regulator [59] operates in four distinct modes, as illustrated in Figure 32. The design exploits both analog and digital LDO with discrete current sources that allow the flexibility to select desired power efficiency and power supply noise rejection (PSR) standards upon choosing a specific operation mode. For example, mode-1 exhibits high power efficiency with low PSR, whereas mode-3 displays high PSR with low power efficiency.

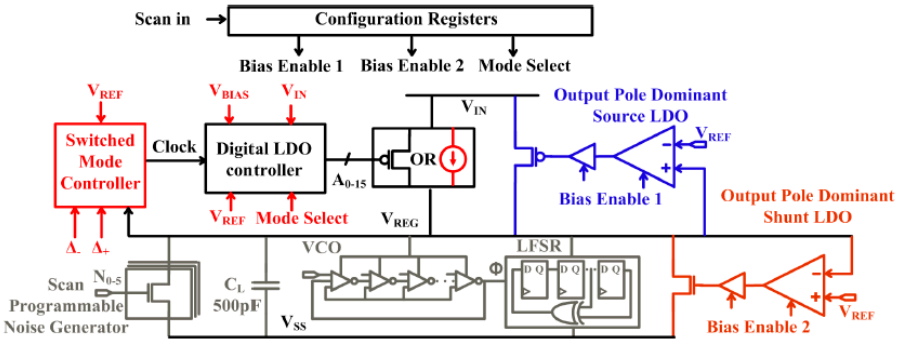


Figure 32. The architecture of Scan Reconfigurable Hybrid LDO [59].

3.3.2. Bandgap Reference-Based Hybrid LDO

Power supply rejection (PSR) performance is a crucial design parameter of LDO due to its ability to smoothen output voltage by suppressing ripples [60]. The bandgap-based LDO, as depicted in Figure 33, offers several benefits such as high power supply rejection (PSR), variable frequency range, finite ripple rejection, low design intricacy, low power consumption, swift transient response, and high stability. The multiplexer decides that either the input or output voltage will be linked with the bandgap reference supply-rail (BGR). As this architecture utilizes the output voltage rather than the noisy input voltage to the PSR of BGR, it ensures excellent PSR of LDO even if the ripple rejection of BGR is not commendable.

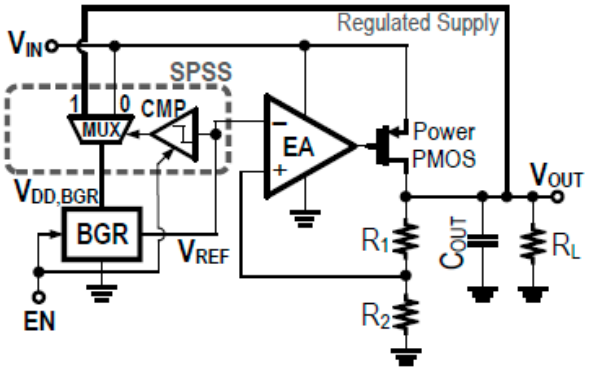


Figure 33. Bandgap Reference-Based Hybrid LDO [60].

3.3.3. Active Ripple Suppression-Based HD-LDO

A hybrid LDO structure combining a DLDO and an analog ripple cancellation amplifier (RCA) [61] is illustrated in Figure 34. A DLDO and RCA are operated in parallel to ensure swift and stable operation, mitigating voltage ripples. A DLDO is prone to quantization error due to its switching nature; therefore, the RCA is operated along with the DLDO to counterbalance this error. The DLDO structure is also efficiently devised, incorporating analog to digital converter (ADC) feedback, a PID controller, and a current-mode digital to analog converter (DAC).

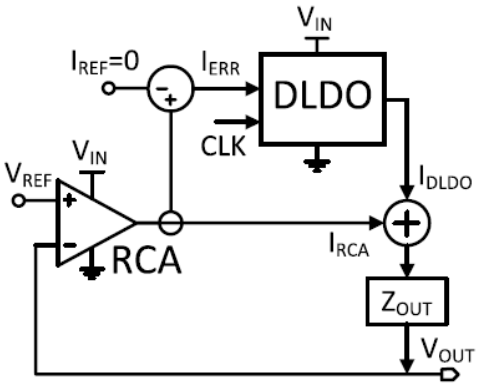


Figure 34. Active Ripple Suppression-based HD-LDO [61].

3.3.4. Switched-Mode-Control-Based Hybrid LDO

A hybrid LDO design based on switched-mode-control (SMC), shown in Figure 35, is made suitable for less power-consuming applications [58]. The design combines an all-digital LDO with an output pole dominant analog LDO to extract advantages from both domains. To perform instant switching, SMC is proposed, which comprises a large signal (LS) and a small signal (SS) controller. A voltage-based error signal decides which controller will be used. Thus, this design achieves fine-grain power management, a fast response, and an efficient regulation scheme.

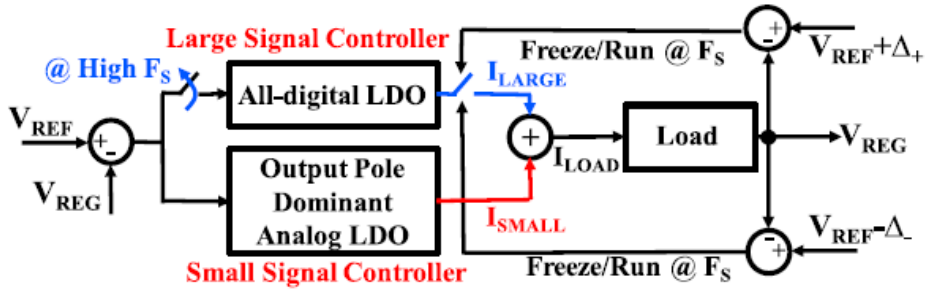


Figure 35. Switched-Mode-Control-based HD-LDO [58].

3.3.5. Exponential-Ratio Array (ERA)-Based Hybrid LDO

A capacitorless hybrid LDO incorporating a thermometer-coded exponential-ratio array (ERA) [63] produced a weak-gain ALDO, depicted in Figure 36. The analog and the digital loop of the HLDO work in parallel to ensure stability, eliminating the necessity of an extra capacitor. The ERA lessens the required number of bits and PMOS transistors, thus widening the load current range and allowing a fast transient response. Moreover, an augmented linear proportional controller (ALPC) improves the linearity of digital loop tracking.

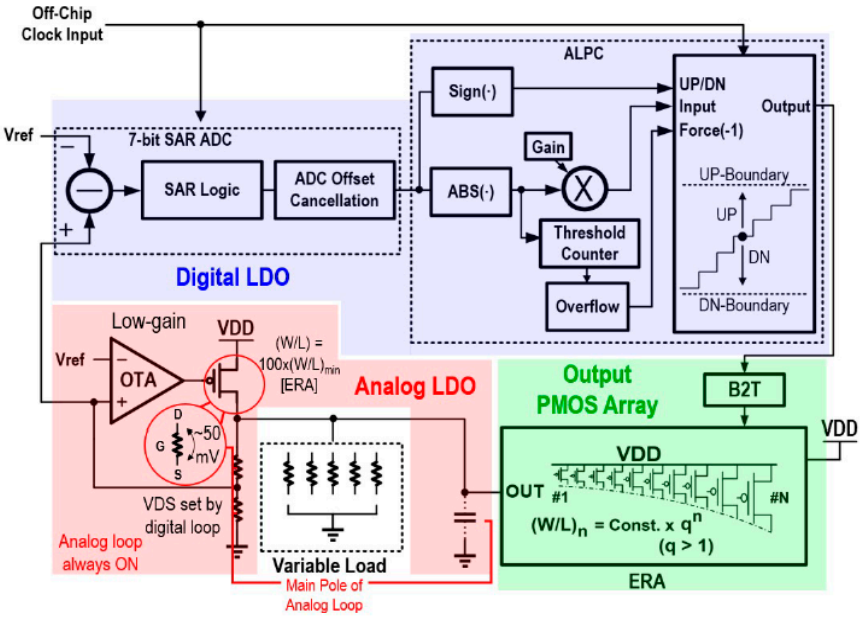


Figure 36. Exponential-Ratio Array (ERA)-based HD-LDO [62].

3.3.6. Performance Comparison of HD-LDO

DLDO architectures are highly desirable because of the increasing number of digital loads and decent large signal transient performance, etc. Nevertheless, DLDO suffers from output ripple, whereas ALDO performs better small signal regulation with suppressed ripple. In face of the above consideration, researchers are intrigued by the idea of using the hybrid LDO strategy of the linear voltage regulator as it extracts features from both the digital and the analog domains of LDOs. The HD-LDO is the most attractive design due to its multi-domain conglomerate design availability according to application specifications. However, in search of achieving the desired performance, HD-LDO requires additional and complex circuitry. The performances of several parameters of different types of LDOs are tabulated in Table 3. Among several designs, [63] presents the superior peak current efficiency with 99.7% performance along with low quiescent current and capless architecture. It also shows better performance in terms of FOM compared to other designs' available data. The designer utilized a 255-bit thermometer-coded exceptional-ratio array (ERA), which reduces the tracking time and suppresses the voltage drop, thus improving the current efficiency. The loop stability is generated by digital logic as the system clock is operated at a much slower speed than settling time. Moreover, the output PMOS in the digital loop can produce an output dominant pole, therefore, moving towards a capless architecture. Furthermore, another unique feature of design [62] is its wide load current range. Again, the maximum load current is achieved in design [60], which is almost thrice the relevant best possible data [61]. Design [60] shows a good power supply rejection ratio (PSRR), which is not tabulated in Table 3. The novelty of this design lies in the implementation of additional feedforward ripple cancellation techniques and a modified gate buffer. Both the capacitorless design [61,63] and design with output capacitors [58,59] are observed in the HD-LDO design. Moreover, the focus of design [59] is to achieve a broad range of PSSR to

generate clean power. Some other parameters are also enlisted in the table, but they are not compared due to the lack of available data.

Table 3. Summary of the HD-LDO performance comparison.

References	[61]	[58]	[59]	[63]	[60]
Technology (nm)	180	130	130	65	500
Input Voltage, V_{IN} (V)	1.43–2.0	0.6, 1.1–1.2	N/A	0.8–1.0	2.2–5
Output Voltage, V_{OUT} (V)	1.0–1.57	0.5–0.55, 0.8–1.1	N/A	0.75–0.95	2–4.85
V_{DROP} (mV)	N/A	N/A	N/A	50	120 (P-type)
Maximum I_{LOAD} (mA)	100	12	5	0.01–40	300
Quiescent Current, IQ (mA)	1	N/A	0.057	0.12	0.050
Current Peak Efficiency (%)	99.11	98.5 (R), 98.64 (L)	98.86	99.7	N/A
C_{OUT}(nF)	Cap-Free	0.5	0.5	Cap-Free	1
Load Regulation (mV/mA)	0.01	<2.67	N/A	N/A	0.003
Line Regulation (mV/V)	1	N/A	N/A	N/A	0.28
PSR (dB)	N/A	N/A	−9 to −34 @ 100 MHz	N/A	80 @0.1 MHz
Active Area (mm^2)	0.679	0.0818	N/A	0.175	N/A
FOM (ps) #	N/A	166(R), 244.8 (Linear) and 0.58 (R), 1.747(Linear) ns/mA ##	28.06 and 28.06 @ 100 MHz ###	0.0188	11

All FOM values are calculated using Equation (7). ## FOM values are calculated using Equation (10). ### FOM values are calculated using Equation (11).

4. Conclusions

This article reviewed the linear regulators in CMOS technology developed by previous researchers. There are many aspects used to identify the performance of the circuit such as the dropout performance, FOM, percentage of current efficiency, power consumption, die area, etc. The study aimed to provide some ideas of possible method modifications to increase the current efficiency and performance of linear regulators. The current efficiency greatly impacts the stability of the circuit in low load current conditions. Dropout voltage affects PSRR, power consumption, and noise performance. FOM signifies the combined impacts of various parameters such as on-chip capacitance, maximum load, output voltage swings, etc. Researches discussed in this paper put significant effort into improving the LDO performance, ranging from application-specific feature development to the trade-off between several specifications. This documentation, as a handy framework, can benefit upcoming researches regarding LDO architectures. The illustrative designs and detailed comparisons presented in this paper can assist researchers to have a better understanding of current developments and promote further improvements in linear regulator circuit designs.

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