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An N/M-Ratio All-Digital Clock Generator with a Pseudo-NMOS Comparator-Based Programmable Divider

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Abstract: A multiplying delay-locked loop (MDLL)-based all-digital clock generator with a programmable N/M-ratio frequency multiplication capability for digital SoC is presented. The proposed digital MDLL provides programmable N/M-ratio frequency multiplication using a new high-speed Pseudo-NMOS comparator-based programmable divider with small area and low power consumption. The proposed MDLL clock generator can also provide a de-skew function by eliminating the phase offset problem caused by the propagation delay of the front divider in conventional N/M MDLL architectures. Fabricated in a 0.13-µm 1.2-V CMOS process, the proposed digital MDLL clock generates fully de-skewed output clock frequencies from 0.3 to 1.137 GHz with programmable N/M ratios of N = 1~32 and M = 1~16. It achieves a measured effective peak-to-peak jitter of 12 ps at 1.0 GHz when N/M = 8/1. It occupies an active area of only 0.034 mm^2 and consumes a power of 10.3 mW at 1.0 GHz.

Keywords: clock generator; multiplying delay-locked loop; MDLL; frequency divider; SoC

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1. Introduction

The high-frequency on-chip clock generators used in modern digital system-on-chips (SoCs) require the ability to provide dynamic frequency scaling (DFS), which generates the output frequency by multiplying the frequency of the input clock (=f_{ref}) by various integer or fractional values. In these on-chip clock frequency generation and multiplication for digital SoCs using scaled CMOS technologies, integer-N phase-locked loops (PLLs) [1–3] based on ring oscillators have generally been widely used to achieve an N/M-ratio frequency multiplication with small chip area and low power consumption, where N and M are integers.

Figure 1 illustrates a simplified block diagram of a general integer-N PLL, which comprises a phase frequency detector (PFD), a loop filter (LF), a ring oscillator (RO)-based voltage-controlled oscillator (VCO), and two frequency dividers (front M & feedback N). However, classical RO-based PLLs generally exhibit poor jitter or phase noise performance. Also, the trade-off between the PLL's loop bandwidth and stability makes it challenging to generate wide-range output clock frequencies in a single integer-N PLL.

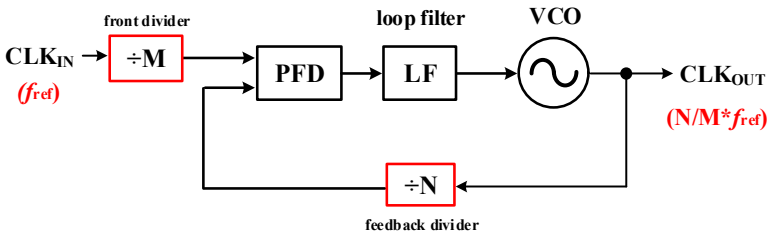
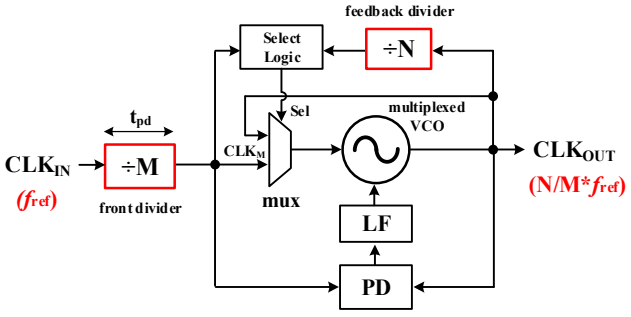


Figure 1. Block diagram of a general integer-N PLL.

Among various on-chip clock generators, multiplying delay-locked loops (MDLLs) can be considered as a way to implement the N/M-ratio frequency multiplication while improving the jitter performance with reduced loop bandwidth issues [4–16].

Figure 2a shows a block diagram of a general MDLL with a front divider M and a feedback divider N to provide the fractional-ratio (=N/M) output clock frequency $f_{out} = N/M \times f_{ref}$. It includes a 2-to-1 multiplexer (MUX), a phase detector (PD), a loop filter (LF), a multiplexed VCO, a select logic, and two dividers (M, N). The locking process of this MDLL when N/M = 4/1 is shown in Figure 2b, assuming the propagation delay (t_{pd}) of the front divider M is zero for simplicity. Here, the t_{pd} means the clock-to-Q delay of the edge-triggered flip-flop constituting the divider. In practice, this t_{pd} is the time it takes for the output of the divider to be in a stable state after an input clock edge occurs, which can be variable by the structure of the divider and the change in the divisor value N or M. At the beginning of the operation, the VCO starts with the maximum frequency, and the delay of the VCO is gradually increased until the N + 1th rising edge of CLK_{OUT} reaches the 2nd rising edge of CLK_{IN}. After locking, the N + 1th rising edge of CLK_{OUT} is phase aligned with the 2nd rising edge of CLK_{IN} without timing skew, and the output clock frequency becomes $f_{out} = N/M \times f_{ref} = 4 \times f_{ref}$ in this example. In addition, whenever the reference CLK_{IN} is injected, the jitter accumulated in the VCO is removed, and the jitter and phase noise characteristics of the MDLL are improved.



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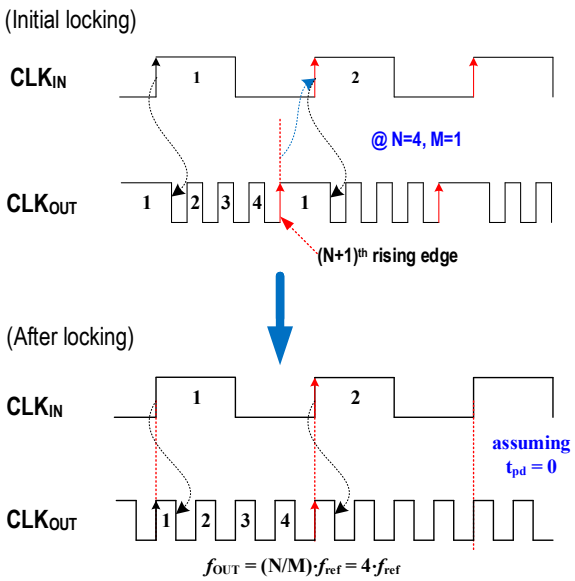
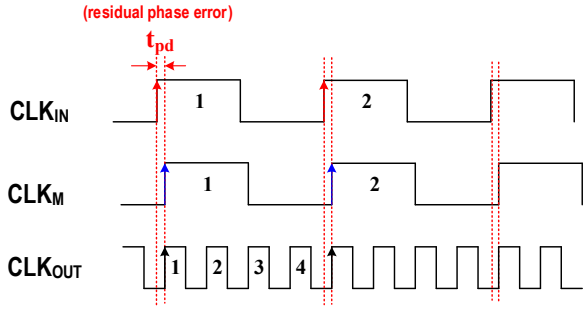


(**b**)

Figure 2. *Cont.*



(**c**)

Figure 2. (**a**) Block diagram of a general MDLL with a front divider M and a feedback divider N to generate N/M times output frequency. (**b**) Locking process when N/M = 4/1 (assuming t_{pd} = 0). (**c**) Residual phase error (or offset) problem when $t_{pd} \neq 0$.

However, in a practical MDLL, the t_{pd} of the front divider M is not zero, so a static phase offset or timing skew occurs between CLK_{OUT} and CLK_{IN}, which adversely affects the performance of the MDLL. Figure 2c shows this residual phase error or phase offset problem more in detail. In an actual situation where the t_{pd} is not zero, a timing skew problem occurs: CLK_{OUT} is locked to CLK_M instead of CLK_{IN}, and an internal phase offset of t_{pd} remains between the CLK_{OUT} and CLK_{IN} signals even after locking. In applications where the front division ratio M is fixed, this timing skew can be eliminated by adding a predetermined fixed delay to the feedback path. However, in the wide-frequency range operation where the M value changes, the t_{pd} value continues to change, so this residual phase error problem still exists and deteriorates the performance of the MDLL [8,10]. Another example of the effect of this residual phase error is the clock distribution network or IO interface of a synchronous system. The output clock of a clock distribution network must be accurately synchronized without skew to the input reference clock. If there is a timing skew caused by the t_{pd} of the front divider M, the timing margin of a high-speed I/O system may be seriously reduced.

To solve the residual phase error problem caused by the front divider's propagation delay of the conventional MDLL structure, an improved de-skewed N/M-ratio MDLL was presented in [10], its architecture is shown in Figure 3a. It includes a 3-to-1 MUX, a PD, a digital LF, a multiplexed digitally controlled oscillator (DCO), a 3-to-1 select logic, and two dividers (M, N). This structure can generate fully de-skewed N/M-ratio frequency multiplication using a 3-to-1 MUX and a new phase detecting structure that directly receives CLK_{IN} and CLK_{OUT} as inputs of the PD. Figure 3b shows the locking process when N/M = 5/2 as an example. At the beginning of the operation, it can be seen that an initial phase error exists between the N + 1th rising edge of CLK_{OUT} and the M + 1th rising edge of CLK_{IN}. After that, as the delay of the DCO gradually increases, the MDLL enters the lock state. At this time, the residual phase error becomes zero, and the output frequency has a fractional ratio value multiplied by N/M = 5/2. For this de-skewed MDLL to generate various N/M-ratio output frequencies in a wide frequency range, it is essential to use a programmable divider that can change the divisor value N or M to different values during operation. However, [10] has a problem in that the N/M-ratio programmability is limited because it uses simple flip-flop-based counter dividers with large area and power consumption.

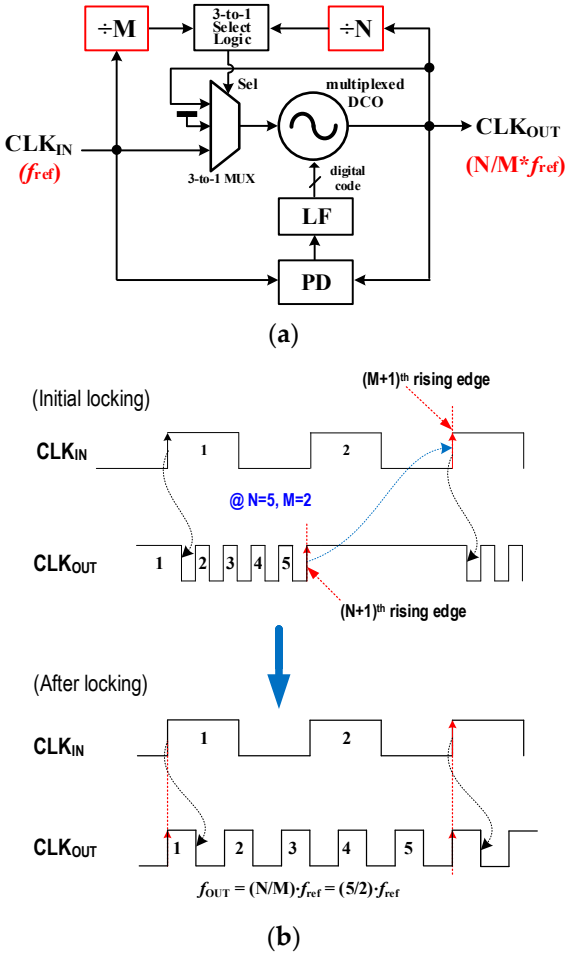


Figure 3. (**a**) Block diagram of a de-skewed N/M-ratio MDLL architecture [10]. (**b**) Locking process when N/M = 5/2.

This paper introduces a new wide-range N/M-ratio MDLL clock generator using a new Pseudo-NMOS comparator-based programmable divide-by-N divider [16]. The proposed divide-by-N divider has the advantages of small area, low power, and high-speed operation, while providing wide programmable division ratios. The proposed MDLL clock generator is optimized for digital SoCs and memories requiring programmable multiplied on-chip clock frequencies. The key contributions of this work are: (a) a silicon-proven N/M-ratio frequency multiplication scheme for de-skewed digital on-chip clock generators, and (b) a new area-efficient and high-speed programmable divide-by-N frequency divider architecture for PLL/MDLL-based clock multipliers. To describe these techniques, this paper is organized as follows: Section 2 presents the architecture and circuit design of the proposed all-digital N/M-ratio MDLL clock generator, Section 3 shows the measurement results, and Section 4 presents the conclusion.

2. Proposed All-Digital N/M-Ratio Clock Generator

2.1. Proposed Digital MDLL Architecture

Figure 4a shows the proposed N/M-ratio digital MDLL clock generator architecture with a new programmable divider, which consists of a 3-to-1 MUX, a multiplexed DCO, a 3-to-1 select logic, a PD, a 10-bit digital loop filter (DLF), a 4-to-16 thermometer decoder, and two programmable frequency dividers (N = 1~32 and M = 1~16). The DCO consists of a coarse delay line (CDL) and a fine delay line (FDL). The CDL consists of sixteen digital delay elements (DEs) connected in series. When the MDLL is enabled, the PD generates the Comp signal by comparing the N + 1th rising edge of CLK_{OUT} and the M + 1th rising

edge of CLK_{IN} as shown in Figure 3b. The 10-bit DLF then generates the Q [9:0] signal needed to control the DCO delay. The 4-to-16 thermometer decoder receives the 4-bit most significant bits (MSBs) of the DLF, Q [9:6], and outputs the thermometer codes T [15:0] for CDL control.

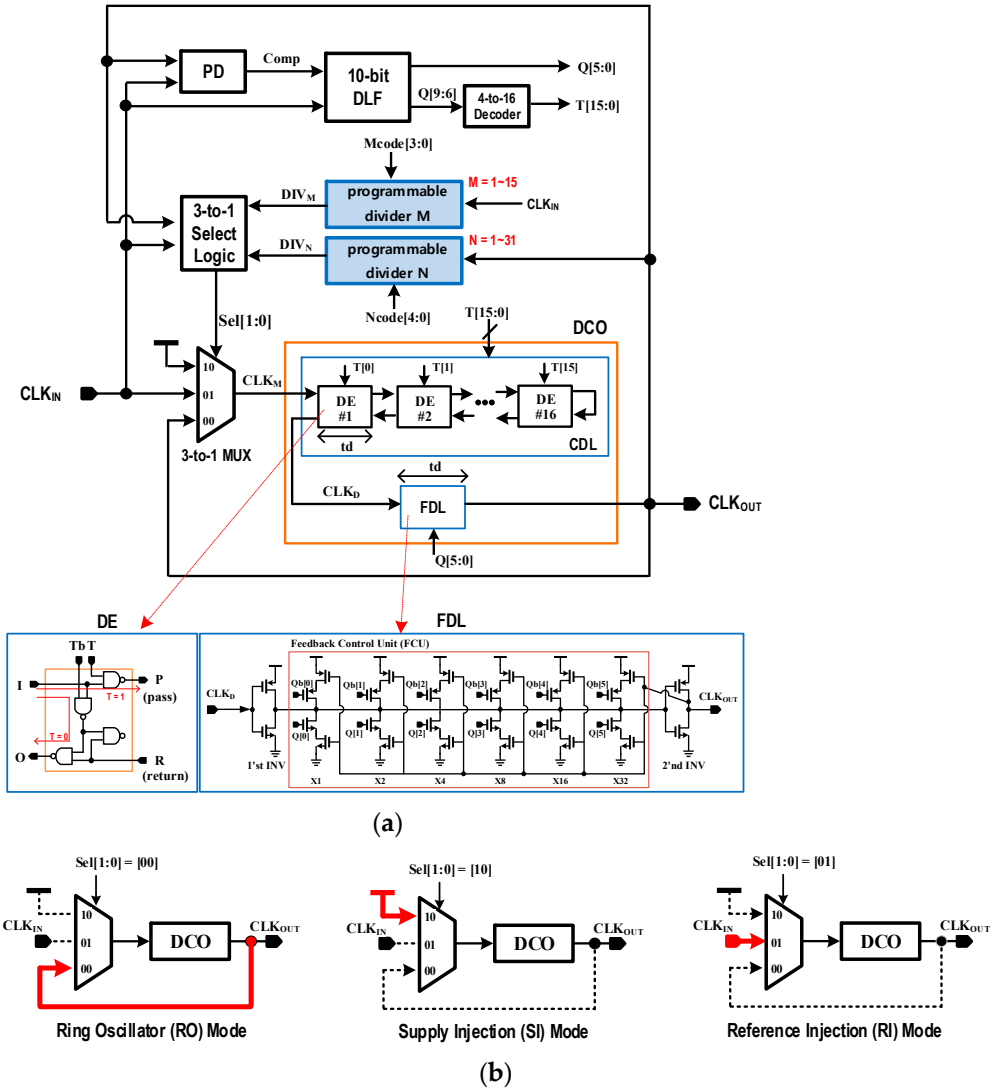


Figure 4. (**a**) Proposed N/M-ratio digital MDLL clock generator architecture with a new programmable divider (N & M). (**b**) Three operation modes: RO, SI, and RI.

As shown in Figure 4a, the NAND-gate-based digital DE has a propagation delay of t_d. The CDL consisting of sixteen serial DEs can have a maximum variable propagation delay of up to 16 × t_d. At the beginning of the MDLL operation, it starts with a value of Q [9:0] = [0], and all of the thermometer codes T [15:0] for CDL control have a value of logic zero. So, the CDL has only two NAND-gate delays as the minimum value. Since the FDL also starts at the minimum delay, the MDLL operates at the maximum frequency at the initial operation. The FDL uses a feedback delay element (FDE) [10], and the delay adjustment of the FDL is controlled by Q [5:0], the least-significant bits (LSBs) of the 10-bit DLF. In addition, the FDL has a programmable variable propagation delay of t_d, where the delay resolution is $t_d/64$. As the value of the DLF increases according to the output signal (Comp) of the PD, the delay of the DCO gradually increases, and phase and frequency lock operation start.

Since the proposed MDLL sequentially performs phase tracking, it has the advantage of fundamentally eliminating the harmonic lock problem. Figure 4b shows the

three operation modes of the proposed MDLL: ring oscillator (RO), supply injection (SI), and reference injection (RI) mode. When the MDLL is turned on, a phase locking process of sequentially repeating the RO, SI, and RI modes is performed at the beginning of the operation. After locking, only the RO and RI modes are repeated to generate a phase-aligned N/M-ratio output frequency.

2.2. Proposed Divide-by-N Divider Architecture

As shown in Figure 5, a clock frequency divider is a circuit that divides the frequency of the input clock (f_{IN}) by a specific divisor value N, producing an output frequency f_{OUT} (=f_{IN}/N) that is lower than the input. The clock frequency divider can generally be classified into three categories: flip-flop-based cascaded divide-by-2 counter, dual-modulus prescalar, and divide-by-N counter [17–20]. The cascaded divide-by-2 counter type clock divider is limited in its use as it can only divide the output frequency by 2^M, where M is the number of cascaded flip-flop stages. Dual-modulus prescalar based dividers are mainly suitable for RF applications that generate high frequency resolution in a narrow frequency range. Among the three types mentioned, when it is necessary to freely program the division ratio N to an arbitrary integer value in a wide frequency range during operation, it is necessary to select a divide-by-N counter type [17–19]. However, there is a problem in the conventional divide-by-N counter dividers using a reloading scheme. The maximum operating frequency is not high due to the propagation delay of the count detector with a multi-stage gate delay. Therefore, to obtain a faster operating speed in the programmable divide-by-N divider, it is necessary to improve the counter detector structure.

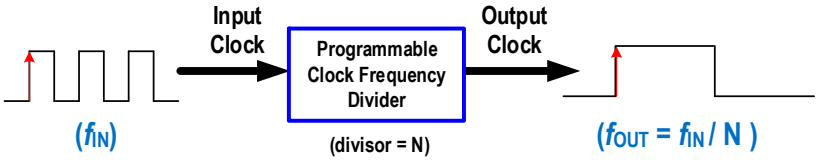


Figure 5. Operation of a general programmable clock frequency divider.

Figure 6 shows a block diagram of the proposed Pseudo-NMOS comparator-based programmable divide-by-N clock frequency divider, which comprises a new count detector, an inverter, and a control block. The control block includes a 5-bit synchronous UP counter and a reset logic. This clock divider receives a periodic CLK signal with a frequency of f_{CLK} and generates the output DIV_N signal with a frequency of f_{CLK}/N. If 5-bit is used as the program code (=Ncode [4:0]), the range of the programmable divisor N value is from 1 to 32 (=2^5). The divider can be reprogrammed by changing a new Ncode [4:0] value. A bypass circuit is built into the divider so that when the Ncode [4:0] is [0], the input CLK signal is passed directly to the output of the divider. The count detector comprises a new 5-bit Pseudo-NMOS comparator and has the advantages of small area and high-speed operation. If a programmable divisor N value extension is required, it is solved by just adding a comparator unit in parallel. When using an 8-bit Pseudo-NMOS comparator, the maximum division ratio N can be increased to 2^8 = 256 with minimal area and power overhead. The divider's speed is limited by the count detector delay, the propagation delay of the synchronous UP counter, and the reset logic delay. Among them, the delay component of the count detector occupies the most significant portion, which was remarkably improved by using the proposed Pseudo-NMOS comparator structure. The worst-case occurs when Ncode [4:0] = [11111] (i.e., N = 32), and even in this case, the proposed divider can operate at 10 GHz in a 0.13-μm process. The power consumption of the proposed divider is only 0.92 mW at 1 GHz with N = 32. The 5-bit divider occupies an active area of only 0.008 mm^2.

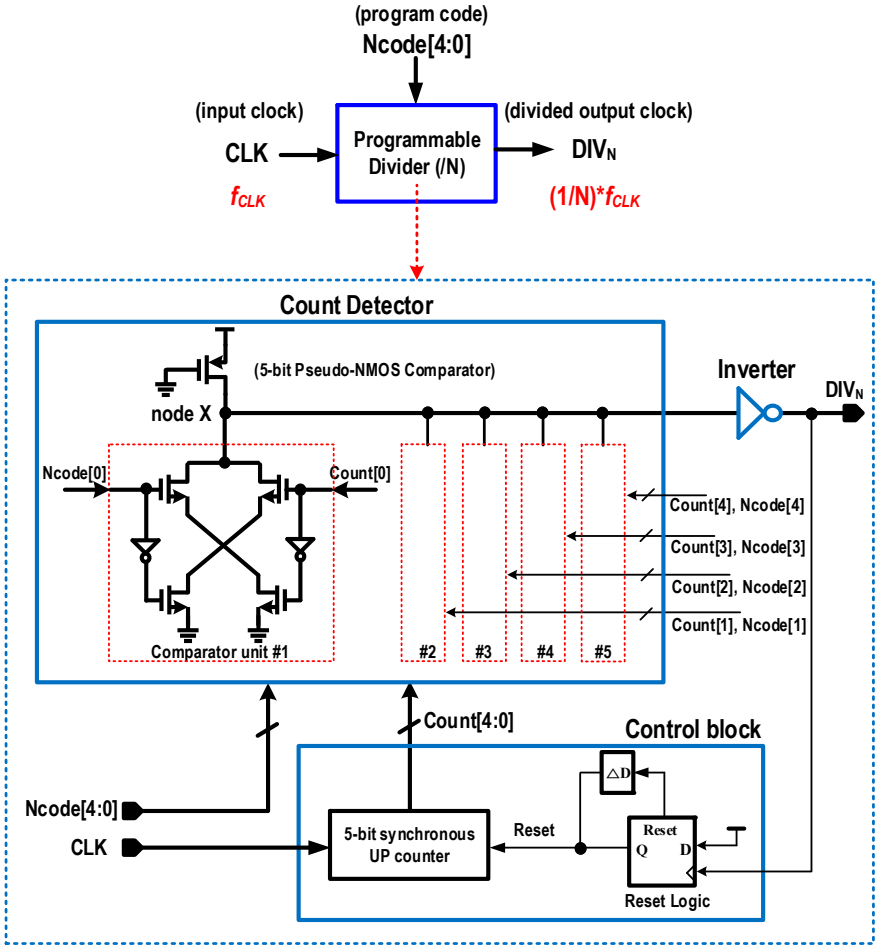


Figure 6. Proposed Pseudo-NMOS comparator-based programmable divide-by-N divider.

Figure 7 illustrates the operation of the proposed Pseudo-NMOS comparator-based programmable divider when the divisor value N = 4 (Ncode [4:0] = [11]) as an example. When the divider is enabled, the output signal Count [4:0] of the 5-bit UP counter increases by one from the initial value (=[0]) to the trigger value (=N) every CLK cycle. Here, the trigger value means the divisor value N, and it can be programmed using Ncode [4:0]. In this example, Count [4:0] starts from [0] and becomes [11] at the rising edge of the 4th CLK, and it becomes equal to Ncode [4:0]. At this moment, the node X (shown in Figure 6) of the count detector changes the state and goes logic high, and then the divider's output signal DIV_N goes logic low with a propagation delay of Δt_{d1}. Then, as Count [4:0] changes, the node X goes logic low, and DIV_N returns to logic high in the next CLK cycle with a propagation delay of Δt_{d2}. For high-frequency operation over several GHz, both Δt_{d1} and Δt_{d2} delays must be minimized. The proposed Pseudo-NMOS comparator-based count detector has a unique structure that minimizes the Δt_{d1} and Δt_{d2} delays and thus enables high-speed operation. Since this detecting operation is repeated every N (=4) cycle, the divider's output (DIV_N) frequency is exactly 1/N (=1/4) of the input CLK frequency (f_{CLK}). The output duty-cycle ratio of the proposed divider is not 50%. However, since the proposed MDLL and most PLLs use a single-edge triggered PD (or PFD), there is no problem in operation.

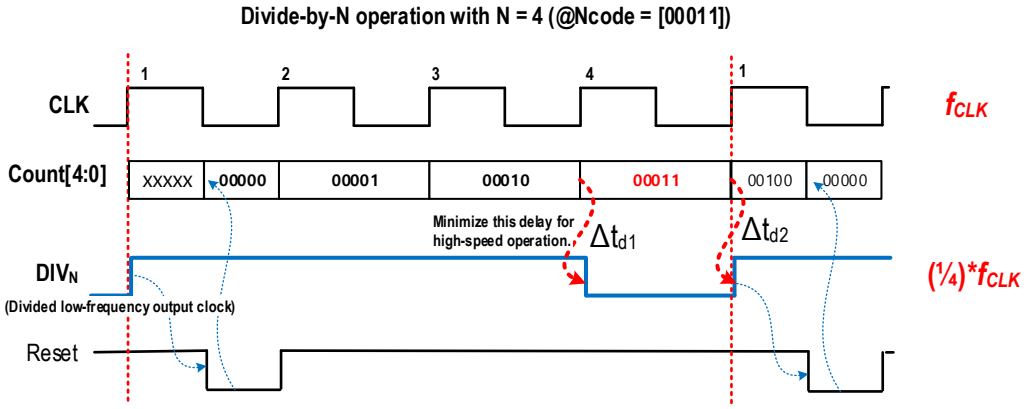
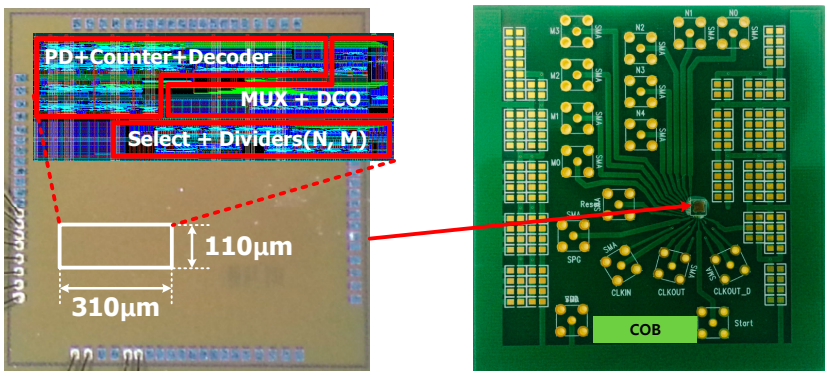


Figure 7. Operation of the proposed programmable divide-by-N divider when N = 4 (Ncode [4:0] = [11]).

3. Measurement Results

The proposed all-digital N/M-ratio MDLL clock generator was fabricated in a 0.13-µm CMOS process and tested with various N/M-ratio multiplication factors. The Tektronix DSA71604 is used to measure the peak-to-peak (p–p) and root-mean-square (RMS) jitter characteristics. The Anritsu MP1763C pulse pattern generator is used to provide various input reference clock frequencies. Figure 8a shows the silicon chip/layout and test chip-on-board (CoB) of the proposed MDLL clock generator, where the active core area is only 310 µm × 110 µm = 0.034 mm^2. Figure 8b shows the measurement setup.



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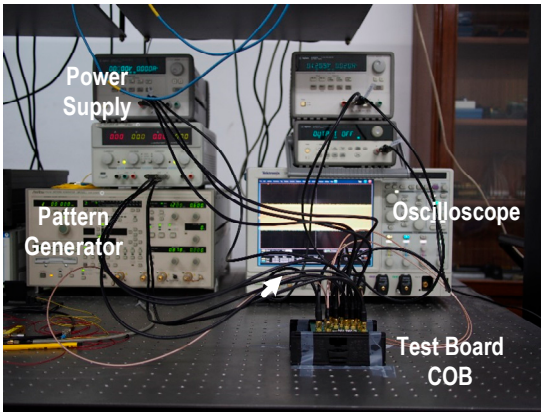


(**b**)

Figure 8. (**a**) Fabricated silicon Chip/Layout and test COB of the proposed N/M-ratio MDLL clock generator. (**b**) Measurement setup.

The proposed digital MDLL can generate output clock frequencies from 0.3 to 1.137 GHz with various programmable N/M multiplication ratios of N = 1~32 and M = 1~16. Figure 9 shows the measured locking process of the proposed MDLL with N/M = 17/4 and f_CLK_{IN} = 150 MHz. This measurement result is precisely consistent with the description of the locking process shown in Figure 3b. The left shows that the RO, SI, and RI modes described in Figure 4b are repeatedly performed at the beginning of the operation. On the right, it can be seen that the input and output clocks are accurately phase-aligned after locking and that the output frequency is multiplied by N/M (=17/4).

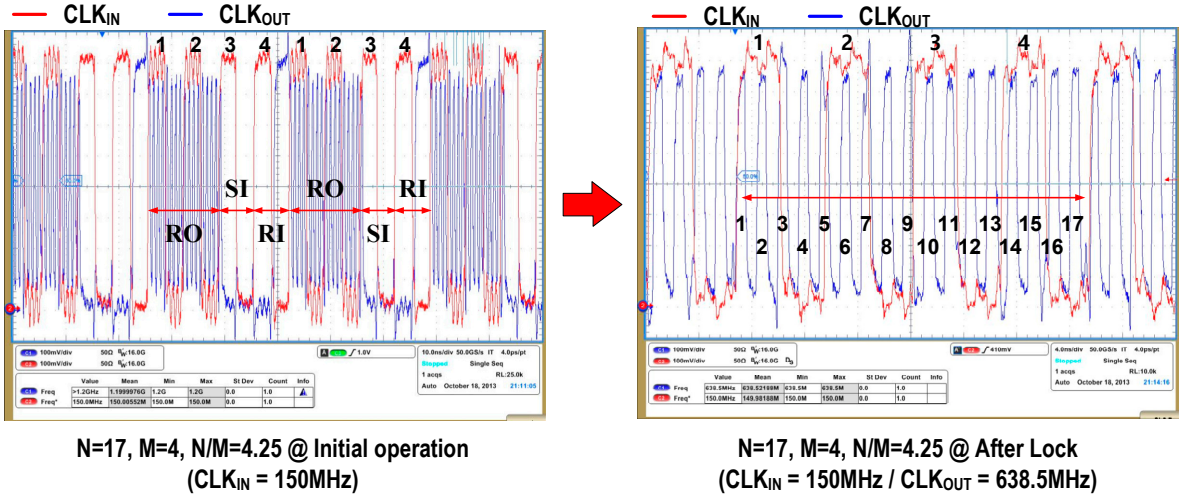
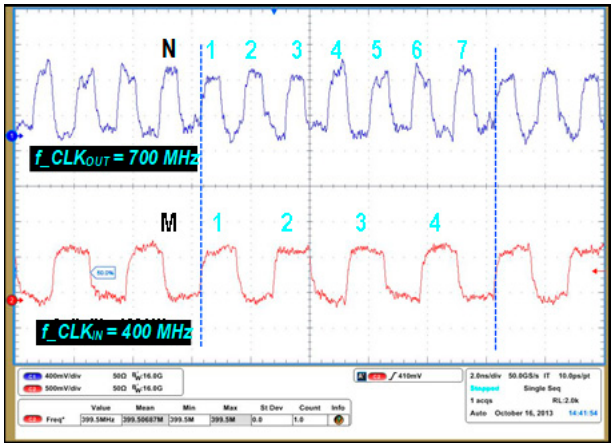


Figure 9. Measured locking process of the proposed N/M-ratio digital MDLL @ N/M = 17/4 = 4.25 and f_CLK_{IN} = 150 MHz. Before lock (Initial Operation, **left**) and after lock (**right**).

Figure 10a illustrates the measured input and output clock waveforms of the proposed N/M-ratio MDLL when the frequency multiplication factor N/M = 7/4. With an input clock frequency f_CLK_{IN} = 400 MHz, the proposed MDLL generates an accurately phase-aligned 700 MHz (=400 × 7/4) output clock f_CLK_{OUT}. Figure 10b shows the measured result when N/M = 31/3, f_CLK_{IN} = 110 MHz, and f_CLK_{OUT} = 1136.67 MHz. Figure 10c shows another phase aligned measurement result when N/M = 31/4 and f_CLK_{IN} = 100 MHz.



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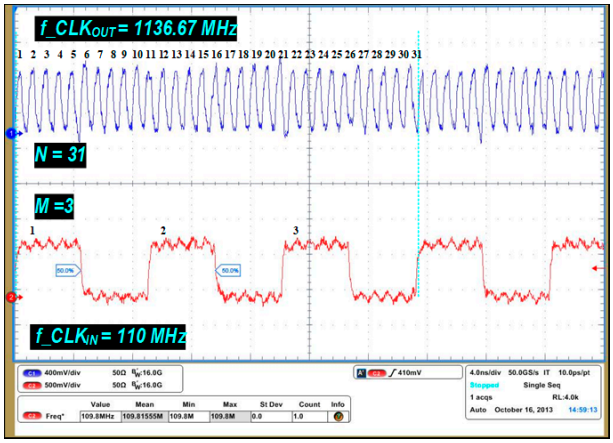

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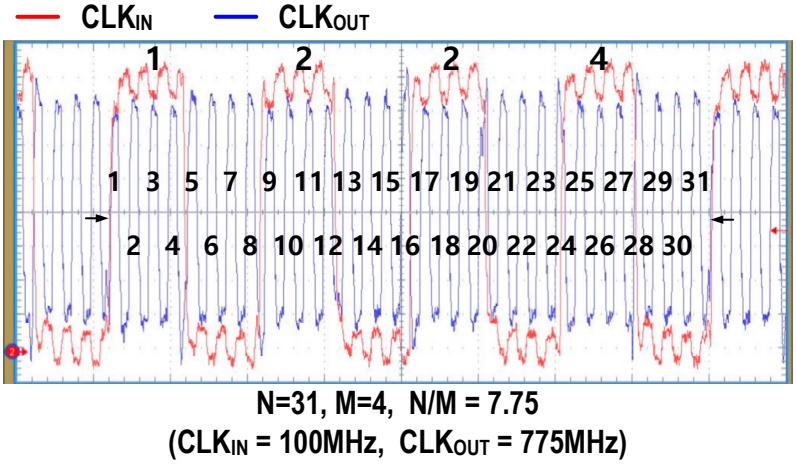

(**c**)

Figure 10. Measured input and output clock waveforms of the proposed N/M-ratio digital MDLL (**a**) f_CLK$_{OUT}$ = 700 MHz, f_CLK$_{IN}$ = 400 MHz, and N/M = 7/4; (**b**) f_CLK$_{OUT}$ = 1136.67 MHz, f_CLK$_{IN}$ = 110 MHz, and N/M = 31/3; and (**c**) f_CLK$_{OUT}$ = 775 MHz, f_CLK$_{IN}$ = 100 MHz, and N/M = 31/4.

The measured p–p jitter and RMS jitter of the proposed MDLL for the multiplication ratio of N/M = 8/1 are shown in Figure 11. Here, the left represents the input clock, and the right represents the output clock. The jitter characteristics of the input clock were measured by connecting the MP1763C's output to the DSA71604 with a 30-cm subminiature version A (SMA) cable. With an input clock frequency of 125 MHz (from the Anritsu MP1763C), the measured effective output p–p jitter of the MDLL is approximately 12 ps at 1.0 GHz when N/M = 8/1, which is the output clock jitter value minus the input clock jitter value (32 ps − 20 ps = 12 ps). It consumes a power of 10.3 mW from a 1.2 V supply at 1.0 GHz. The performance summary and comparisons with the previously reported digital MDLLs [7,10,21,22] with a programmable frequency multiplication capability (with variable N or N/M) are listed in Table 1. Compared with the MDLLs in Table 1, the proposed digital N/M-ratio MDLL achieves the widest range of variable and programmable N/M frequency multiplication factors while adding the unique feature of de-skewing capability without harmonic lock problems. The key advantages, such as ultra-small size, low power consumption, and N/M-ratio frequency programmability, make it ideal for use in digital SoCs and memories requiring a dynamic frequency scaling capability.

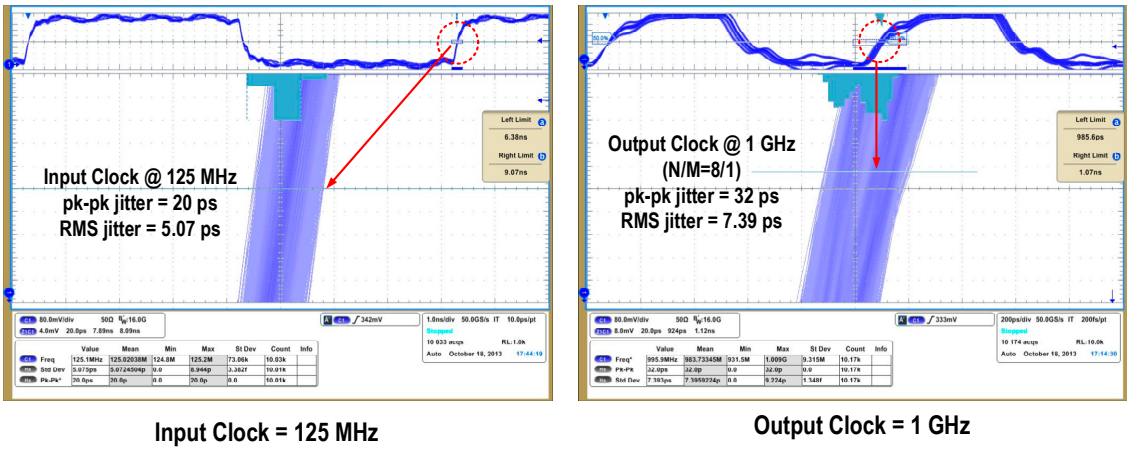

Figure 11. Measured input and output clock's p-p/RMS jitter characteristics of the proposed digital MDLL (@ 1 GHz, N/M = 8/1).

Table 1. Digital MDLL performance summary and comparisons.

Reference	[7] JSSC 06	[10] TCAS-II 18	[21] ISSCC 18	[22] TCAS-I 18	This Work
Process & Supply	0.35 µm/3.3 V	65 nm/1.1 V	28 nm/0.8 V	40 nm/1.8 V	0.13 µm/1.2 V
Output Freq. range [GHz]	0.12–1.8	0.7–2.0	1.6–3.2	0.1536–0.5184	0.3–1.137
Fractional-ratio (N/M) multiplication capability	No	Yes	No	No	Yes
Multiplication factor (N only or N/M)	N = 1~8 (N only)	N = 1, 4, 5, 8, 10 M = 1, 2, 3	N = 8~16 (N only)	N = 8~27 (N only)	N = 1~32 M = 1~16
p–p/RMS jitter [ps]	6.6/1.8 @ 1.3 GHz, N = 4	22/2.86 @ 2 GHz, N/M = 8/2	NA/0.292 ** @ 3 GHz, N = 15	NA/1.28 ** @ 0.5184 GHz, N = 27	12.0/2.32 @ 1 GHz, N/M = 8/1
Power [mW]	86.6 @ 1.6 GHz	3.31 @ 1 GHz	1.45 @ 3.0 GHz	2.6 @ 0.518 GHz	10.3 @ 1 GHz
Active area [mm^2]	0.07	0.019	0.0056	0.047	0.034
FOM *	−215.52	−225.67	−249.1	−233.7	−222.56

* FOM = 10 × $\log_{10}$[(RMS jitter/1 s)^2 × (Power/1 mW)]; ** Integrated RMS jitter.

4. Conclusions

In this paper, a new MDLL-based programmable N/M-ratio clock generator that features a new programmable divider is presented. The proposed all-digital MDLL utilizes a new Pseudo-NMOS comparator-based programmable divide-by-N divider to provide various and wide-range N/M frequency multiplication ratios. Compared with the conventional programmable divider design, the new count detector circuit achieves a minimal area and low power consumption while significantly improving speed. Also, the proposed digital MDLL clock generator achieves a fully de-skewed N/M multiplication function by eliminating the phase offset problem caused by the propagation delay of the front divider in a conventional N/M MDLL structure. The proposed N/M-ratio all-digital MDLL clock generator is fabricated in a 0.13-µm 1.2-V CMOS process operates in a frequency range from 0.3 to 1.137 GHz, with a power consumption of 10.3 mW at 1.0 GHz. The measured effective p–p jitter is only 12 ps at 1.0 GHz when N/M = 8/1. Thus, the proposed programmable N/M-ratio MDLL clock generator is suitable for low-power memory and SoC design requiring de-skewed and wide-range dynamic frequency scaling.

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