

# High-Density Solid-State Memory Devices and Technologies

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## 1. Introduction

The relevance of solid-state memories in the world of electronics is on the constant rise. On one hand, the continuous increase in the integration density of semiconductor technologies has been making solid-state storage the dominant storage solution of the 21st century, thanks to a successful trade-off against cost, performance and reliability. On the other hand, new memory-centric computing scenarios based on solid-state memories are appearing on the horizon to overcome the limitations of the mainstream von Neumann computing architecture. The 3D NAND Flash memory technology, the NOR Flash memory technology, the phase-change memory (PCM) technology, the resistive random-access memory (ReRAM) technology, the magnetoresistive random-access memory (MRAM) technology, and the ferroelectric memory technology are the most important players at the heart of the ongoing memory revolution, along with the dynamic random-access memory (DRAM) technology and the static random-access memory (SRAM) technology.

In this context, this Special Issue aims to examine high-density solid-state memory devices and technologies from various standpoints, in the attempt to foster their continuous success in the future. Considering that the broadening of the range of applications will likely offer different types of solid-state memories the chance to come to the spotlight, the Special Issue is not focused on a specific storage solution, but it embraces all the most relevant solid-state memory devices and technologies currently on stage. Even the subjects dealt with in the Special Issue are widespread, going from process and design issues/innovations to the experimental and theoretical analysis of the operation, the performance and the reliability of memory devices and arrays and to the exploitation of solid-state memories to pursue new computing paradigms.

## 2. Overview of the Papers in the Special Issue

This Special Issue includes six review papers and three original research papers focused on the most important solid-state memory devices and technologies.

The first review paper in the Special Issue is by Pedretti and Ielmini [1] and summarizes the current status of analog in-memory computing with RRAM devices, representing a promising non-von Neumann computing approach. In the paper, the fundamentals of RRAM devices and of the new computing concept are first reviewed, highlighting the importance of achieving a tight control over the analog conductance of the resistive memory elements. The constraints to that control are then discussed, considering programming variations, conductance drifts/time-dependent fluctuations and array-level issues. The options for coding the computational coefficients in the RRAM array are also presented, discussing the trade-off between precision and memory area, and examples of circuit primitives for analog in-memory computing are provided. Finally, the prospects and challenges of the new computing approach are debated, pointing out that RRAM represents the most mature and promising technology to pursue it.



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The second review paper in the Special Issue is by Watanabe and Lin [2] and presents an overview of the reliability issues arising from traps in the dielectric layers of solid-state memory cells. Trap-related phenomena are discussed in the time and frequency domain, pointing out the intrinsic discreteness involved in them. The possibility to get some relevant information about traps in dielectrics through ad hoc experimental analyses and theoretical investigations is demonstrated, paving the way to possible technology and process optimizations.

The third review paper in the Special Issue is by Teramoto [3] and discusses low-frequency noise in metal-oxide-semiconductor field-effect transistors (MOSFETs), representing the building blocks of the memory cells of the most important solid-state storage technologies. Due to the relevant role played by the phenomenon on the reliability of deeply scaled devices, emphasis is on random telegraph noise (RTN) and on its statistical experimental characterization and theoretical analysis. In the paper, the amplitude of RTN fluctuations is first addressed, considering its dependence on device parameters and operating conditions and taking into account both two-state and multi-state waveforms. The time constants of the process are then analyzed not only for stationary but also for switched biasing conditions. Finally, RTN in advanced device structures, such as buried-channel and asymmetric source-drain MOSFETs, is debated, pointing out possible solutions to mitigate the phenomenon in future technology nodes.

The fourth review paper in the Special Issue is by Chiu and Shirota [4] and summarizes a method to investigate the endurance of NAND Flash memories starting from cell transconductance. Nowadays, NAND Flash memories represent the dominant nonvolatile storage solution, and techniques allowing us to get some information about the microscopic mechanisms constraining its endurance are of utmost importance for the development of next-generation technology nodes. In the paper, first, a mix of experimental and theoretical analyses is adopted to come to the build-up of charge in the cell tunnel-oxide as a result of the program/erase cycles performed on the memory array. Then, the charge build-up is studied as a function of the cycling conditions of the array, e.g., the cycling temperature and the idle time in-between cycles. Finally, a physical picture for the generation of oxide charge is proposed, allowing us to deepen the understanding of NAND Flash reliability.

The fifth review paper in the Special Issue is by Goda [5] and comprehensively examines the evolution of the 3D NAND Flash technology. In the paper, the historical trend of the storage density of NAND Flash memory chips is first discussed, showing how 3D technologies achieved the extraordinary figures that are revolutionizing the nonvolatile storage scenario. The role played by the growth of the number of memory layers vertically stacked in the array, the miniaturization of cell dimensions and the increase in the stored bits per cell is then discussed, along with innovative integration schemes such as the CMOS-under array solution. Finally, the future challenges and opportunities of the technology are highlighted.

The sixth review paper in the Special Issue is by Ohba et al. [6] and summarizes the state-of-the-art of the Bumpless Build Cube (BBCube) using a Wafer-on-Wafer (WOW) and a Chip-on-Wafer (COW) approach, representing a new process solution for Tera-Scale Three-Dimensional Integration (3DI). In the paper, the BBCube architecture is explicitly considered for memory applications, considering BBCube DRAM and BBCube NAND Flash solutions. The challenges and prospects of the new integration approach are clearly highlighted, unveiling the promise of a next big step in the semiconductor roadmap.

The first research paper in the Special Issue is by Zambelli et al. [7] and investigates the benefits and shortcomings of program suspend operations in 3D NAND Flash Solid-State Drives. Through experimental analyses and system-level simulations, the impact of including program suspend in the command set of the storage device on its speed, reliability and power consumption is clarified.

The second research paper in the Special Issue is by Rao et al. [8] and demonstrates the benefits of alloying conventional free-layer materials such as CoFeB in STT-MRAM cells

with nonmagnetic metals (such as W). The solution is presented as an alternative approach to achieve write performance improvements in STT-MRAM technologies.

The third research paper in the Special Issue is by Malavena et al. [9] and proposes the adoption of a pulse-width modulation scheme to implement hardware artificial neural networks based on NOR Flash memory arrays. The new operating scheme is shown to be highly immune to noise and temperature variations, paving the way to the development of highly reliable, noise-resilient neuromorphic systems.

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