

## Article

# A Control Strategy to Smooth Power Ripple of a Single-Stage Bidirectional and Isolated AC-DC Converter for Electric Vehicles Chargers

Leonardo A. Ramos , Rafael F. Van Kan , Marcello Mezaroba \*  and Alessandro L. Batschauer 

Department of Electrical Engineering, Santa Catarina State University, Joinville 89219-710, Brazil; leonardoadrianoramos@hotmail.com (L.A.R.); rafaelvankan@gmail.com (R.F.V.K.); alessandro.batschauer@udesc.br (A.L.B.)

\* Correspondence: marcello.mezaroba@udesc.br

**Abstract:** This paper proposes a single-stage AC-DC rectifier with power factor correction (PFC), high-frequency isolation and bidirectional power conversion capability for on-board battery charger (OBC) applications. The proposed converter is based on the interleaving technique and the Dual Active Bridge (DAB) operation, applying the phase-shift control to regulate the power flow. In addition to topology, this article presents a control strategy for reducing low-frequency power ripples transferred to the secondary side without any additional component and hence maintaining overall size and cost. The single-phase OBC can interchange active power with the grid to charge batteries while performing grid-to-vehicle (G2V) functionality or transferring energy back to the grid via vehicle-to-grid (V2G) mode. The theoretical analysis of the converter including modulation strategy and feedback control scheme are presented. The proposed topology and control strategy have been verified by experimental results of a 650 W SiC-based prototype.

**Keywords:** electric vehicles; vehicle-to-grid (V2G); power factor correction (PFC); high-frequency isolation; Dual Active Bridge; power decoupling



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## 1. Introduction

The electrification of transportation is a major technological approach for decreasing air pollution in heavily populated places and a promising alternative to contribute to energy diversification and greenhouse gas (GHG) emission reduction. Automotive market reports show that electric vehicles (EVs) will account for about 30% of the market by 2030 [1]. In this context, new challenges and opportunities are emerging in terms of the on-board chargers (OBCs) for electric vehicles mainly related to power density, efficiency, reliability, safety and lifetime [2–4].

EV battery chargers can be broadly classified according to installation as off-board (level 3) and on-board (levels 1 and 2) and power flow capability (unidirectional or bidirectional) [5]. Multifunctional OBCs will incorporate smart features to the grid. Moreover, bidirectional OBCs will enable vehicle-to-grid (V2G) functionalities, such as peak shaving, reactive power compensation, frequency regulation and spinning reserve [6–8]. Expanding V2G technologies will change the dynamics by turning EVs from a consumer of electricity into a power provider [1].

The conventional approach for OBCs is based on the two-stage structure, which consists of a front-end single-phase AC-DC converter for power factor correction (PFC) and an isolated DC-DC converter for output voltage regulation [9–11]. The main drawbacks of the two-stage charger are increased part count, cost, size and weight. Single-stage AC-DC topologies reduce complexity, hardware, weight and cost while improving the efficiency of the system [12]. Various single-stage topologies are presented in [13–15]. In single-phase OBCs, there is an inherent power ripple component that pulses at twice the grid frequency [16]. Conventional techniques usually employ bulky electrolytic capacitors to reduce this low-frequency ripple,

compromising the reliability of the converter because the life of electrolytic capacitors is very short and also increases cost and volume.

In recent years, great efforts have been made to avoid the use of electrolytic capacitors on single-phase typologies [17,18]. In order to increase power density, OBCs with sinusoidal charging were proposed in [19]. With this method, low-frequency power pulsation flows into the battery; thus, DC-link capacitance can be significantly reduced. Previous studies show that the low-frequency ripple current affects the lifetime of the battery due to internal heating [20] and also increases the number of charge/discharge cycles and, hence, capacity degradation [21].

Many methods of active power decoupling circuits have been proposed to minimize the ripple power at the DC-link [22,23]. Active power filters (APFs) can be classified depending on the location of whether the APF is on the DC-link side or AC-link side [24,25]. This approach utilizes auxiliary circuits to absorb low-frequency ripple power, which results in increased system complexity, cost and additional losses.

Compact charging technologies are particularly important in the automotive industry, as OBC has to meet strict dimensional requirements to fit inside EV [5]. In addition, galvanic isolation is a prerequisite in most OBCs to ensure safety and voltage level adaptation between the grid and the DC side [26,27]. Moreover, high-frequency (HF) transformers should be employed to achieve a compact size and weight reduction [28]. OBCs with V2G capability are in early adoption phases, and its potential depends on the availability of vehicles to participate in such services at suitable times, consumer acceptance and other technical constraints related to impacts on battery lifetime [29]. Many electric vehicle manufacturers are interested on developing bidirectional OBCs, but currently there are few EVs capable of operating with V2G. From this perspective, the proposed topology is one solution that can contribute to V2G growth.

This paper proposes a novel isolated bidirectional charger with V2G capability that aims for a high degree of integration and, thus, integrates the functionalities of PFC and HF transformer. The topology combines the characteristics of an interleaved PFC rectifier and a Dual Active Bridge (DAB) converter and provides three ports: the AC grid, the primary DC-link without isolation and an isolated secondary DC-link. Power flow between the grid and batteries is controlled by the phase-shift angle between the primary and secondary sides. Furthermore, it smooths low-frequency voltage ripples without any additional components, hence maintaining the overall size and cost. The initial idea of the proposed converter with simulation results has been presented in [30], but detailed analyses and experimental results are shown in this paper to verify the converter operation and to test the proposed control strategy.

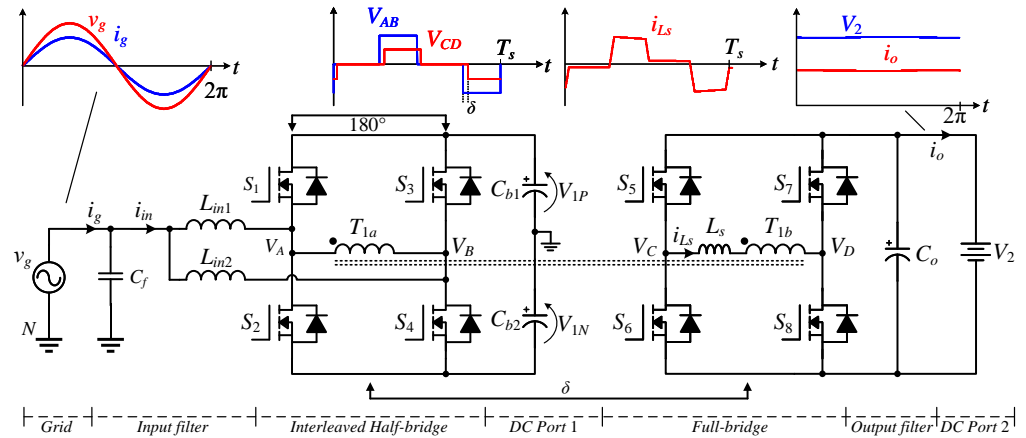
The proposed topology features reduced complexity compared to state-of-the-art solutions and is mainly addressed towards a reduced number of semiconductors, V2G mode, HF isolation and reduced low-frequency voltage ripple. The paper is organized as follows: Section 2 presents a comprehensive description of the proposed converter system and discusses its operation principle. This section also analyzes the control strategy applied to smooth the power ripple. Section 3 describes the prototype and presents the discussion of experimental results. Finally, Section 4 presents general conclusions obtained from the study.

## 2. Materials and Methods

### 2.1. Circuit Description

The proposed topology results from the integration of two converters widely studied in the literature, as shown in Figure 1. The interleaved half-bridge boost rectifier (IHBR) is responsible for regulating the primary DC-link voltage and for achieving low AC current total harmonic distortion (THD). On the DC side, the Dual Active Bridge (DAB) is integrated and shares primary switching legs with IHBR, thus providing galvanic isolation between the primary and secondary sides.

The interleaving operation on the grid side allows the insertion of the HF transformer by connecting it to the full-bridge on the DC side. This galvanic isolation provides high voltage ratio conversion and user protection when handling the vehicle charging plug. The primary-side IHBR boosts the grid voltage to the nominal DC voltage  $V_1 = V_{1P} + V_{1N}$  and ensures a sinusoidal current  $i_g$  that is in-phase with the grid voltage  $v_g$  to achieve unity power factors.



**Figure 1.** Circuit schematic of the proposed single-stage AC/DC converter.

The primary and secondary switches of the converter operate with the same duty cycles. Thus, the gate signals of the transistors on the secondary side are subjected to a common phase-shift  $\delta$  to control output power at the secondary DC-link voltage. Power flow control is performed by using the phase-shift (PS) technique, i.e., controlling the angle between primary and secondary sides through an HF transformer, with turn ratios set to  $n = 2 = V_1/V_2$  to achieve efficient operation of the DAB converter.  $L_s$  is the equivalent series inductance that represents an external series inductance added to the leakage inductance of the transformer. In addition, the phase-shift control adds power decoupling on the DC side of the converter, which minimizes the ripple power transferred to the secondary side to charge the batteries and also reduces DC-link capacitance at the converter output.

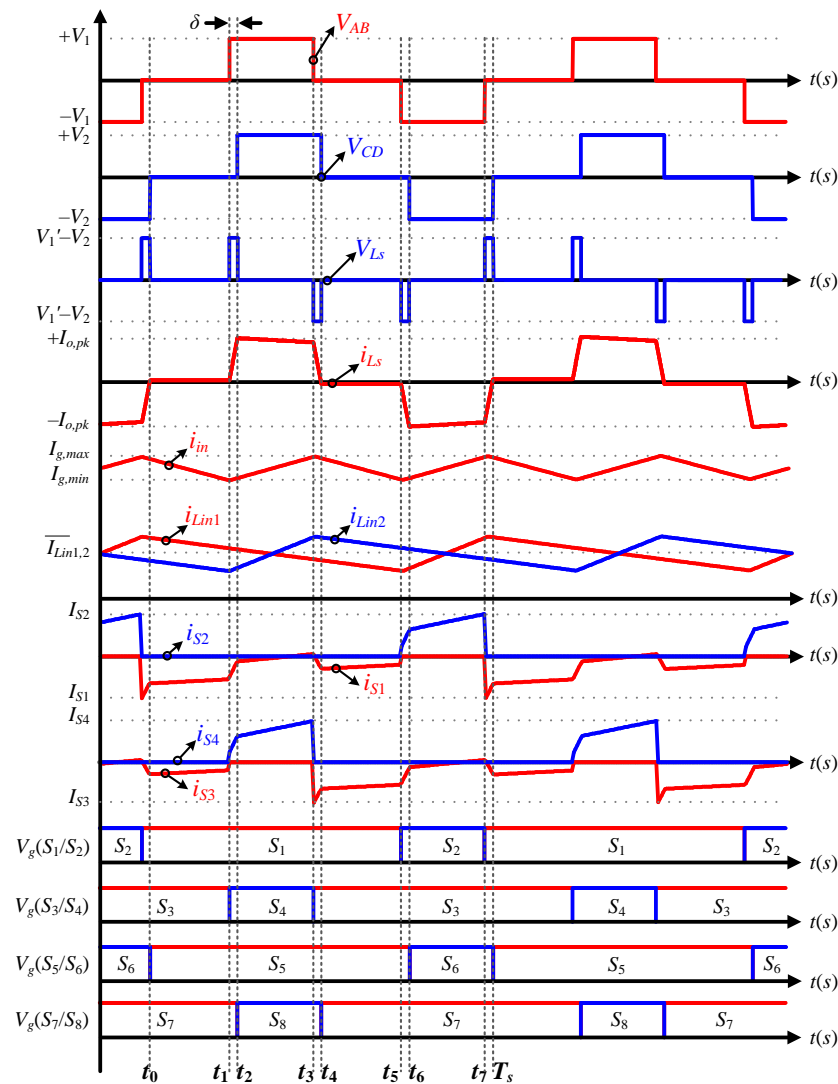
### 2.2. Operation Analysis of the Proposed OBC

In order to analyze the operating stages of the single-stage OBC depicted in Figure 1, the following assumptions are made to simplify analysis: All components are lossless; the AC-voltage source is purely sinusoidal and constant during one switching period ( $T_s$ ) and the DC-link voltage is constant. The operation during a switching period can be described by using eight stages with the corresponding key waveforms in Figure 2.

In addition, the gate signals of the pair of switches  $(S_1/S_2)$ ,  $(S_3/S_4)$ ,  $(S_5/S_6)$  and  $(S_7/S_8)$  are complementary to each other;  $i_{Lin1}$  and  $i_{Lin2}$  are the currents through the interleaved inductors;  $i_{in}$  is the input current ( $i_{Lin1} + i_{Lin2}$ );  $V_{AB}$  and  $V_{CD}$  are the voltages across primary ( $T_{1a}$ ) and secondary ( $T_{1b}$ ) windings of the transformer, respectively;  $i_{Ls}$  is the current through the power transfer inductance  $L_s$ ; and  $\delta$  represents the phase-shift angle between  $V_{AB}$  and  $V_{CD}$ :

1. Stage 1 ( $t_0, t_1$ ): The switches  $S_1, S_3, S_5$  and  $S_7$  are ON. During this interval, the voltages across the transformer  $V_{AB}$  and  $V_{CD}$  are null. Thus, the energy stored on the capacitor  $C_o$  is transferred to the battery.
2. Stage 2 ( $t_1, t_2$ ): Initially, the switch  $S_4$  is switched ON and  $S_3$  is switched OFF so that the primary voltage is  $V_{AB} = +V_1$ . In the secondary side, the condition remains the same as stage 1, whereas current  $i_{Ls}$  increases linearly since its voltage is equal to  $+V_1/n$ , i.e., the difference between  $V_{AB}$  and  $V_{CD}$ .

3. Stage 3 ( $t_2, t_3$ ): In the primary side, the state remains the same as stage 2. For the secondary side,  $S_7$  is switched OFF and  $S_8$  is switched ON; thus, the voltage at the secondary is  $V_{CD} = +V_2$ . The voltage across the inductance  $L_s$  is null, and current  $i_{L_s}$  remains constant at its peak value.
4. Stage 4 ( $t_3, t_4$ ): Switch  $S_3$  is switched ON; thus, the voltages across the transformer are  $V_{AB} = 0$  and  $V_{CD} = +V_2$ . Furthermore, the voltage applied on the inductance  $L_s$  is  $-V_2$  and the current  $i_{L_s}$  starts to decrease linearly until it reaches zero.



**Figure 2.** Main waveforms for the proposed single-phase converter during a switching period and positive cycle  $v_g$ .

The operating stages are symmetric and are explained only for the positive half-cycle of the input current. The behavior of  $V_{AB}$ ,  $V_{CD}$  and  $i_{L_s}$  is analogous for the other half-switching period, assuming negative values during the interval ( $t_4, T_s$ ).

As observed in Figure 2, the waveforms of the currents through all switches located in the primary side are identical, as well as the current flowing through all secondary switches. Therefore, the currents through the primary and secondary-side semiconductors can be derived as follows.

$$i_{S_{1,2,3,4}}(t) = i_{in}(t)/2 - i_{L_s}(t)/n \tag{1}$$

$$i_{S_{5,6,7,8}}(t) = -i_{L_s}(t) \tag{2}$$

### 2.3. Modulation Strategy

The bidirectional charger presented in this study uses a sinusoidal pulse width modulation plus phase-shift control to achieve high-frequency operation. The interleaved legs at the primary side of the converter are driven by two triangular carriers ( $crr_{1,p}$  and  $crr_{2,p}$ ) fixed and displaced  $180^\circ$  from each other. The two carriers of the secondary side switches ( $crr_{1,s}$  and  $crr_{2,s}$ ) are phase-shifted by an angle  $\delta$  from  $crr_{1,p}$  and  $crr_{2,p}$ , which enables active power flow control.

The modulators of the secondary side use the same control signals as those of the primary side ( $m_{a,1}$  and  $m_{a,2}$ ) in order to avoid low-frequency current flowing through the HF transformer and to minimize reactive power flow that would degrade converter efficiency. Thus, the voltage waveform across the transformer ( $V_{AB}$  and  $V_{CD}$ ) corresponds to a three-level rectangular voltage displaced of  $\delta$ , as shown in Figure 3. From the adopted modulation strategy, it is possible to identify 16 operating regions depending on phase-shift angle  $\delta$  and the sinusoidal variation of the duty-cycle, where each region has eight operating stages (see Section 2.2).

We define a purely sinusoidal grid voltage  $v_g$  and input current  $i_g$  in-phase with  $v_g$ :

$$v_g(t) = V_{pk} \cdot \sin(\omega_g t) \tag{3}$$

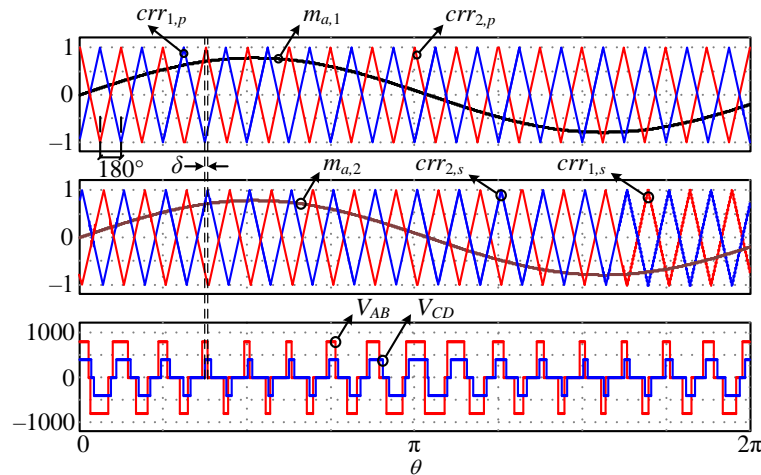
$$i_g(t) = I_{pk} \cdot \sin(\omega_g t) \tag{4}$$

where  $V_{pk}$  and  $I_{pk}$  are, respectively, the peak values of the AC source voltage and current, and  $\omega_g = 2\pi f_g$  is the grid's angular frequency.

Considering PFC operation and neglecting voltage drop across the boost inductors, the duty-cycle  $d(t)$  generated by the converter control system is defined as follows:

$$d(t) = \frac{1}{2} - M \sin(\omega_g t) \tag{5}$$

where  $M = V_{pk} / V_1$  is the modulation index.

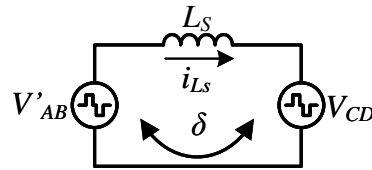


**Figure 3.** Sinusoidal PWM modulation plus phase-shift control.

### 2.4. Equivalent Circuit and Power Flow Analysis

For the discussion of power flow control, a simplified lossless, secondary-referred equivalent circuit is shown in Figure 4, where the converter can be seen as one inductor  $L_s$  (leakage inductance + external inductor) connected between two controlled quasi-square wave voltage sources. The equivalent series inductor  $L_s$  represents the energy transfer element, which is the main parameter for defining maximum output power. The primary voltage referred to the secondary is  $V'_{AB}$ , and  $V_{CD}$  is the secondary voltage. The phase-

shift between the voltages applied on the primary and secondary side of the transformer determines the direction and amplitude of the power flow.



**Figure 4.** Fundamental model where the input and output switches are replaced by equivalent voltage sources  $V'_{AB}$  and  $V_{CD}$ , referred to the transformer’s secondary-side.

The fundamental model has been extensively discussed in the literature with a satisfactory correlation compared to the real model [31]. The three-level rectangular voltage applied on both sides of the transformer (with the sinusoidal behavior of the duty cycle, as shown in (5)) can be replaced by its respective fundamental component. The *rms* value of the fundamental component is obtained by applying a Fourier Series to the quasi-square wave voltage sources given by the following:

$$V'_{AB,rms} = \frac{2\sqrt{2}}{\pi} \cdot \frac{V_1}{n} \cdot \sin(\pi d_{AB}) \tag{6}$$

$$V_{CD,rms} = \frac{2\sqrt{2}}{\pi} \cdot V_2 \cdot \sin(\pi d_{CD}) \tag{7}$$

where  $d_{AB}$  and  $d_{CD}$  are, respectively, the duty-cycle for each voltage,  $V_1$  and  $V_2$  are the primary and secondary DC-link voltages and  $n$  is the turns ratio.

In order to determine the required power transfer inductor for a given power and phase-shift angle, the steady-state current phasor through inductor  $L_s$  is given as follows.

$$\vec{I}_{L_s}(\delta, d) = \frac{V'_{AB,rms} \cdot e^{j0^\circ} - V_{CD,rms} \cdot e^{-j\delta}}{jX_{L_s}} \tag{8}$$

The apparent power is obtained by multiplying the complex conjugate of the equivalent series inductor current  $I_{L_s}^*$  and the voltage  $V'_{AB}$ , as provided in (9).

$$\vec{S}_o(\delta, d) = V'_{AB,rms} \cdot \vec{I}_{L_s}^*(\delta, d) = P_o + jQ_o \tag{9}$$

From (8) and (9), the active power processed by the transformer is determined by the following:

$$P_o(\delta, d) = \Re(\vec{S}_o) = \frac{8V_1V_2}{n\pi^2\omega_sL_s} \cdot \sin(\delta) \cdot \cos^2[M\pi\sin(\theta)] \tag{10}$$

where  $d_{AB} = d_{CD} = d(t)$  and  $\theta = \omega_s t$ .

According to (10), for a fixed switching frequency, the power is related to the phase-shift angle, the sinusoidal duty-cycle and power transfer inductance. Figure 5 illustrates normalized active power flow  $P_{o_{pu}}$  as a function of the phase-shift angle and duty-cycle (operating with a modulation index  $M = 0.444$ ). The power transferred is maximum when  $d(t) = 0.5$  and  $|\delta| = \pi/2$ . All results are normalized according to the following.

$$P_{base} = \frac{8V_1V_2}{n\pi^2\omega_sL_s} \tag{11}$$

$$P_{o_{pu}} = \sin(\delta) \cdot \cos^2[M\pi\sin(\theta)] \tag{12}$$

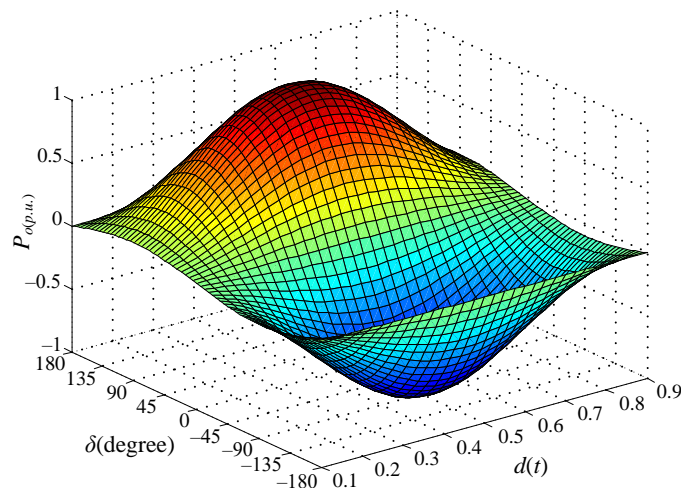


Figure 5. Power flow according to the phase-shift angle and duty-cycle.

The average power transferred by the converter over one grid period ( $f_g$ ) is obtained from the integration of (10), resulting in the following.

$$P_{o,avg}(\delta) = \frac{1}{2\pi} \int_0^{2\pi} P_o(\delta, \theta) d\theta \tag{13}$$

The single-phase PFC rectifier produces a sinusoidal input current in phase with the grid voltage; thus, multiplying (3) and (4) allows calculating instantaneous input power according to (14). Input power  $p_g(t)$  is formed by active power  $P_g$  and ripple power  $\tilde{P}_g$ , which are oscillating at twice the grid frequency, and they are stored in primary DC-link capacitors ( $C_{b1}$  and  $C_{b2}$ ).

$$p_g(t) = v_g(t) \cdot i_g(t) = \underbrace{\frac{V_{pk}I_{pk}}{2}}_{P_g} - \underbrace{\frac{V_{pk}I_{pk}}{2} \cdot \cos(2\omega_g t)}_{\tilde{P}_g} \tag{14}$$

It can be observed from (10) that the power flowing through the HF transformer contains a large AC ripple at the double line frequency, as shown in Figure 6. This behavior comes from sinusoidal modulation applied on the primary side switches and mirrored to the secondary side switches. In order to overcome this intrinsic characteristic of the proposed single-stage converter and minimize low-frequency ripple power, we propose to invert and isolate the phase-shift variable  $\delta(P_o)$  from the Equation (10), resulting in the following.

$$\delta(P_o) = \sin \left[ \frac{n\pi^2 \omega_s L_s}{8V_1 V_2 \cos^2(M\pi \sin\theta)} \right]^{-1} \tag{15}$$

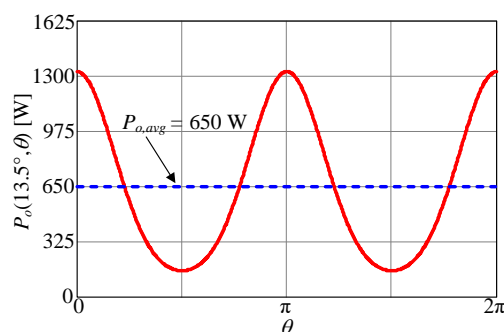


Figure 6. Active power for  $\delta = 13.5^\circ$  over one grid period and the average output power  $P_{o,avg}(13.5^\circ)$  delivered to the battery.

Thus, by solving (15) and respecting converter specifications, it is possible to obtain a constant steady-state output power while achieving power decoupling from primary and secondary sides. The phase-shift angle is generated by the converter control system as presented in Figure 7, mitigating low-frequency ripple. The average phase-shift angle ( $\delta_{avg}$ ) corresponds to the same value of the active power waveform shown in Figure 6, indicating that angle variation is able to compensate the ripple power.

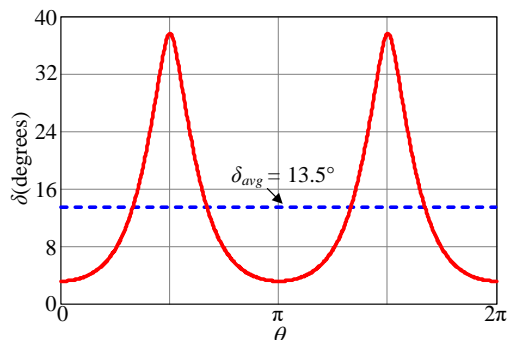


Figure 7. Phase-shift angle behavior to maintain a quasi-constant output power over one grid period.

2.5. Control Strategy

A feedback control scheme able to regulate primary and secondary DC-link voltages ( $V_1$  and  $V_2$ ) of the proposed converter and shape the instantaneous value of the AC-side current is presented in Figure 8. In order to obtain near unity power factor, the input current must be sinusoidal and synchronized with the grid’s fundamental voltage. Therefore, a single-phase phase-locked loop (PLL) is implemented to track the phase angle of the grid’s voltage.

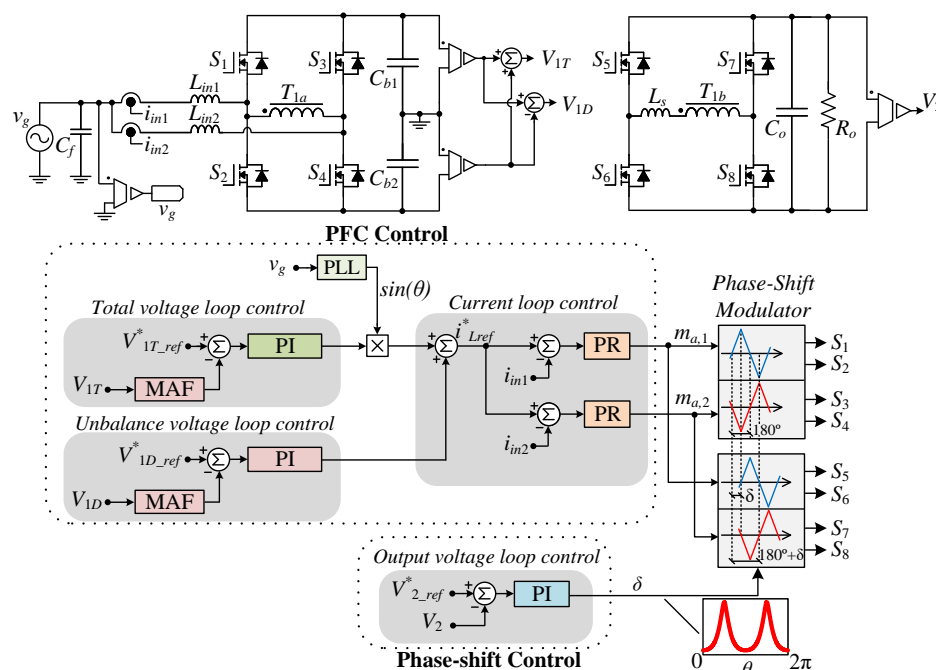


Figure 8. Feedback control scheme and phase-shift modulator circuit.

The primary DC-link voltage is regulated by two outer control loops that control DC-link total voltage  $C_{vt}$  and unbalance voltage control  $C_{vun}$ , which maintains the voltage across the balanced DC-link capacitors ( $C_{b1}/C_{b2}$ ). The bandwidth of the voltage control loops should be significantly lower than the grid frequency to maintain low input current distortion. In order to overcome this effect, a digital moving average filter (MAF) is used to reject low-frequency components that are integer multiples of the grid frequency [32].



Thus, this enables a closed loop that provides both high bandwidth and low input current total harmonic distortion (THD).

The combination of outer voltage loops outputs multiplied by the sinusoidal reference of the PLL generates reference signal  $i_{Lref}^*$  for the fast inner current control loop  $C_i$ . A proportional-resonant (PR) controller is designed to improve reference tracking and disturbance rejection. Finally, the gate commands for  $S_1/S_2$  and  $S_3/S_4$  are generated by comparing modulating signals  $m_{a,1}$  and  $m_{a,2}$  with the two interleaved triangular carriers  $crr_{1,p}$  and  $crr_{2,p}$ , respectively.

Power flow control is performed by the phase-shift  $\delta$  between the primary and secondary side carriers and, therefore, the voltages across primary and secondary windings. The modulators of the secondary side uses the same control signals as those of the primary side ( $m_{a,1}$  and  $m_{a,2}$ ) to minimize reactive power flow through the HF transformer. The voltage loop  $C_{vo}$  regulates the secondary DC-link voltage. For this application, a high bandwidth PI control strategy is used to obtain a high instantaneous power balance between the grid and the load and compensates low-frequency ripple power. Thus, the gate signals of the primary and secondary side switches are generated by the same modulating signals but are phase-shifted by angle  $\delta$  resulting from the triangular carriers displacement.

### 2.6. Comparative Analysis

A comparative analysis between the proposed converter (A) and other existing bidirectional isolated AC-DC converters is given in Table 1. One is a well-known two-stage topology (B), which is composed of a front-end AC-DC bidirectional full-bridge PFC converter associated with a DC-DC Dual Active Bridge (DAB) converter [33]. The other topology (C) comprises a single-stage front-end rectifier operating at line frequency and a DAB converter, eliminating the bulky electrolytic capacitors between the two converters [34]. The voltage and current stresses of the semiconductors are generically quantified as low, medium and high. The proposed topology has the lowest number of semiconductors among the analyzed converters, which results in a more reliable and simpler solution. In addition, the current stresses on power semiconductor switches for A are higher than B and C because of the integration of two converters. Moreover, the voltage stresses on primary side semiconductors are higher because the front-end half-bridge converter needs a higher DC-link voltage when compared to full-bridge converters. These two conditions lower the efficiency of the proposed topology.

**Table 1.** Comparison of the proposed topology with other existing isolated topologies.

Topology Parameter	A: Proposed Converter	B: Two-Stage Full-bridge PFC [33] and Dual Active Bridge	C: Single-Stage Dual Active Bridge with Line Rectifier [34]
No. of switches	8	12	12
Output current ripple	Lowest	Low	High
Current stress	High	Medium	Medium
Voltage stress	High	Medium	Medium
No. of magnetic components	1 × transformer with 2 windings 1 × external inductor 2 × PFC inductors	1 × transformer with 2 windings 1 × external inductor 1 × PFC inductor	1 × transformer with 2 windings 1 × PFC inductor
Control variables	Duty-cycle regulation for PFC and single phase-shift	Duty-cycle regulation for PFC and single phase-shift	Dual phase-shift and triple phase-shift
Soft switching	No	Yes	Yes
Full load efficiency	90%@650 W	92%@2 kW	81%@1 kW

## 3. Results and Discussion

A 650 W prototype was designed and built according to Table 2. A picture of the hardware prototype is shown in Figure 9, with outer dimensions of 295 mm × 150 mm × 202 mm. The digital control algorithms and modulation schemes have been implemented within a DSC TMS320F28335 from Texas Instruments. The converter parameters are designed following the equations presented in the paper and using analytic equations published in [30,35,36]. A list of the passive components and semiconductor devices employed in the lab prototype is provided in Table 3.

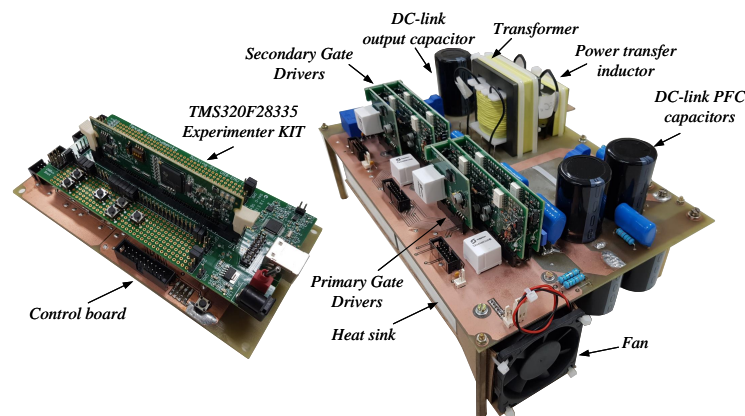
The design of the prototype is based on efficiency, volume and available financial resources. SiC MOSFETs were used on the primary and secondary sides in order to take advantage of their reduced switching and conduction losses. Sendust toroidal PFC inductors were used because of its reduced losses at high frequencies when compared to iron powder cores. Finally, N87 magnetic cores from TDK were used to reduce the size of the transformer and power transfer inductor, since it has high flux density and low losses at 50 kHz (switching frequency).

**Table 2.** Parameters of the OBC prototype.

Parameter	Symbol	Value
Grid voltage/frequency	$v_g / f_g$	220 V / 60 Hz
Primary DC-link voltage	$V_{dc1}$	700 V
Secondary DC-link voltage	$V_{dc2}$	350 V
Rated output power	$P_o$	650 W
Switching frequency	$f_s$	50 kHz
Nominal phase-shift angle	$\delta$	13.45°
Primary DC-link capacitance	$C_b$	470 $\mu$ F
Secondary DC-link capacitance	$C_o$	220 $\mu$ F
Interlaving inductance	$L_{in1} / L_{in2}$	1.6 mH
Transformer turns ratio	$n$	2
Power transfer inductance	$L_s$	47 $\mu$ H

**Table 3.** Main devices employed in the lab prototype.

Component	Main Specification
$S_1, S_2, S_3, S_4$	C2M0160120D Cree (1200 V / 19 A)
$S_5, S_6, S_7, S_8$	SCT3120 Rohm (650 V / 21 A)
$C_{b1}, C_{b2}$	B43503-S5477-M91 Epcos (470 $\mu$ F / 450 V)
$C_o$	B43303-A0687-M90 Epcos (220 $\mu$ F / 400 V)
$L_{in1}, L_{in2}$	MMTS60T5715 core (77 turns, 1 $\times$ 20 AWG)
$L_s$	E42/21/15 TDK (21 turns, 9 $\times$ 26 AWG, air gap = 1.644 mm)
$T_{1ab}$	E65/32/27 TDK (75 turns, 10 $\times$ 29 AWG 38 turns, 10 $\times$ 26 AWG)
Gate drivers	Supplier DRO100D25A
Current sensor	LEM LTSR 15-NP (15 A)
Voltage sensor	LEM LV 20-P (500 V)
Heat sink	KM2-250 mm
DSC	Texas Instruments TMS320F28335



**Figure 9.** A 650 W hardware prototype of the proposed OBC and the control board.

The inner current PR controller designed in harmonic components {1, 3, 5, 7, 9} has a gain margin of  $GM_i = 9.1$  dB at 7.1 kHz and a phase margin of  $PM_i = 48.7^\circ$  at 2.5 kHz. The proportional controller is adjusted for the Bode Diagram zero cross frequency to be around 2.5 kHz, which is twenty-times lower than the control law calculation frequency. In this loop, sampling frequency is set to 50 kHz.

The total voltage controller  $C_{vt}$  and the unbalanced voltage controller  $C_{vun}$  are proportional in addition to integral controllers. The primary DC-link total voltage controller is tuned to have a phase margin of  $PM_{vt} = 60^\circ$  at 8 Hz, while the unbalanced voltage controller is tuned to have a phase margin of  $PM_{vun} = 70^\circ$  at 4 Hz. The outer loop sampling frequency is adjusted to be one-tenth of the current inner loop.

A proportional-integral controller  $C_{vo}$  is used in the output voltage control loop. To evaluate the proposed control strategy, the controller is designed three times using different zero-crossing frequencies {36 Hz, 1200 Hz, 3600 Hz} and with the same phase margin of  $PM_{vo} = 60^\circ$  for all three cases.

The experimental tests are performed at different power and voltage levels. The operation of the power factor correction control can be observed in Figure 10. The waveform of the current drawn from the grid is regulated to be sinusoidal and in phase with the grid voltage, and the measured THD of the input current was 2.76% for full-load with a power factor higher than 0.99. As a comparative analysis, the input current THD without the moving average filter was 5.37%. The primary DC-link voltage unbalance control maintains voltages  $V_{1P}/V_{1N}$  as well balanced. Finally, Figure 11 shows the harmonic spectrum of the grid current  $i_g$  and IEC 61000-3-2 class D limits [37]. The PR controller is responsible for reducing the odd harmonic components of the grid current and for ensuring that the converter complies with the standard.

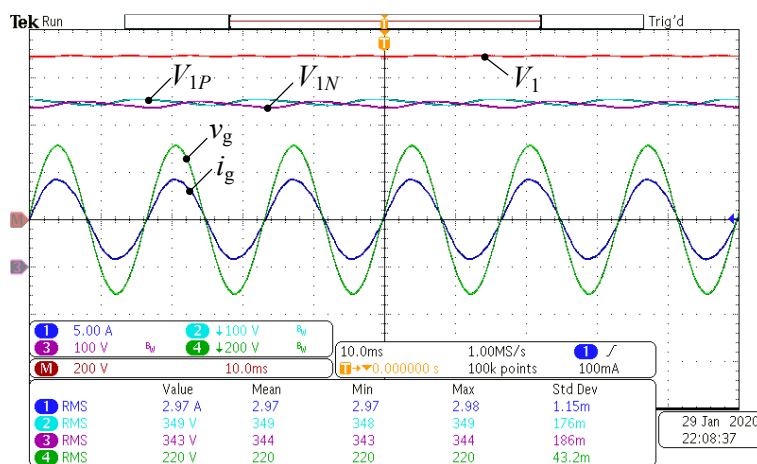


Figure 10. Experimental results: grid voltage  $v_g$ , input current  $i_g$  and primary DC-link voltage  $V_{1P} + V_{1N} = V_1$ . The converter presents low-current total harmonic distortion THD = 2.76% and high power factor PF > 0.99.

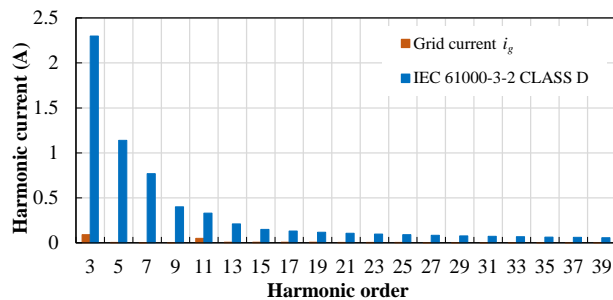
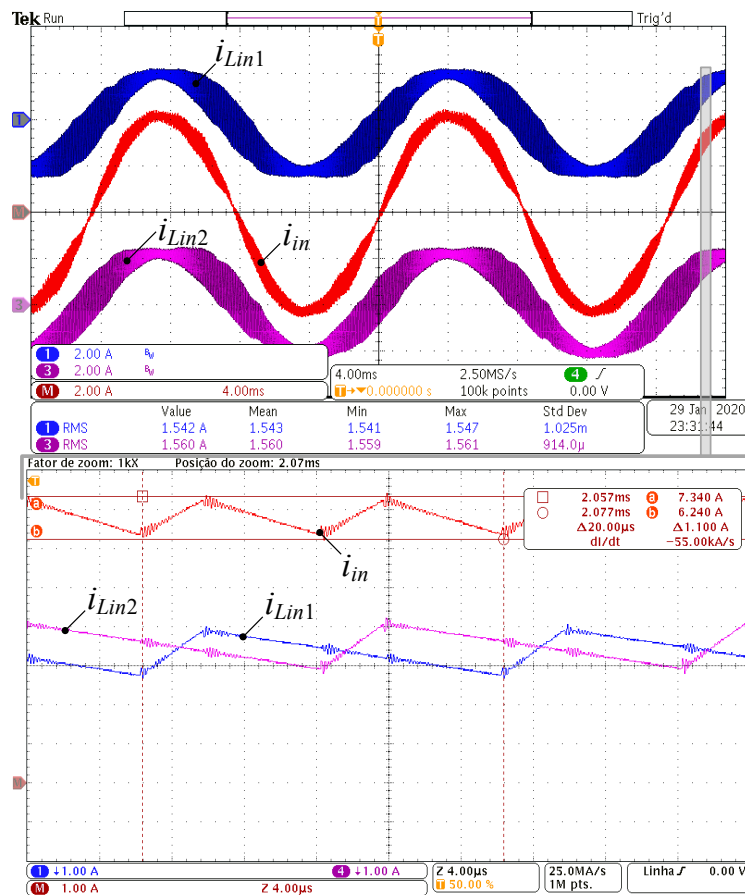


Figure 11. Harmonic components of grid current  $i_g$  and IEC 61000-3-2 class D limits for the converter operating at rated output power.

Figure 12 shows that leg currents  $i_{Lin1}$  and  $i_{Lin2}$  are interleaved and the resulting current  $i_{in}$  has twice the converter’s switching frequency. It is observed tolerances and non-idealities in passive and active components (mainly the inductors  $L_{in1}/L_{in1}$  and semi-conductors) cause differences in high-frequency current ripples among the interleaved legs. The existing differences are negligible and does not compromise OBC PFC operation.



**Figure 12.** Experimental results: interleaved leg currents  $i_{Lin1}/i_{Lin2}$  and the resulting current  $i_{in}$ . The bottom figure shows a zoomed-in view of a switching period interval, where the total input current has twice the switching frequency  $f_s$ .

The main waveforms of the grid-connected operation of the proposed charger are shown in Figure 13. On the AC side, power factor correction is achieved, and output voltage is regulated by PS control on the DC side. The obtained efficiency is higher than 90% in both operation modes (rectifier and inverter modes) at full load. The measured THD of the input current is less than 5% from half to full load.

The measured transformer voltages  $V_{AB}$  and  $V_{CD}$  and the corresponding current series inductance  $I_{Ls}$  are shown in Figure 14 for two different grid voltage phase angles  $w_g t$ . Voltage waveform across the transformer’s primary and secondary windings corresponds to a three-level rectangular voltage shifted by  $\delta$  similar to the DAB converter operation.

Figure 15 presents the dynamic performance of the proposed control for two resistive load steps: from 400 W to 200 W and from 200 W to 400 W. The converter presents low overshoot and fast response, and in both cases the input current exhibits smooth behavior during transient events. In order to demonstrate phase-shift control, a low-bandwidth PI control for output voltage control was used. Thus, the  $\delta$  waveform is constant and varies during load steps.

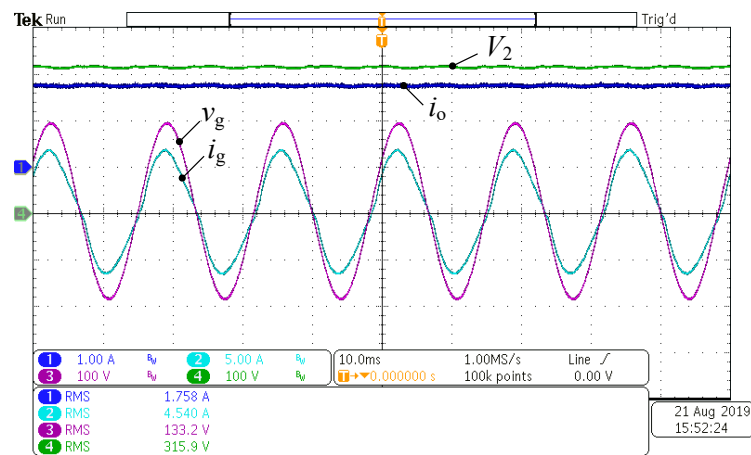


Figure 13. Experimental results: grid voltage  $v_g$  and input current  $i_g$  on the AC-side of the converter. On the DC-side, the output voltage  $V_2$  and current  $i_o$  are shown.

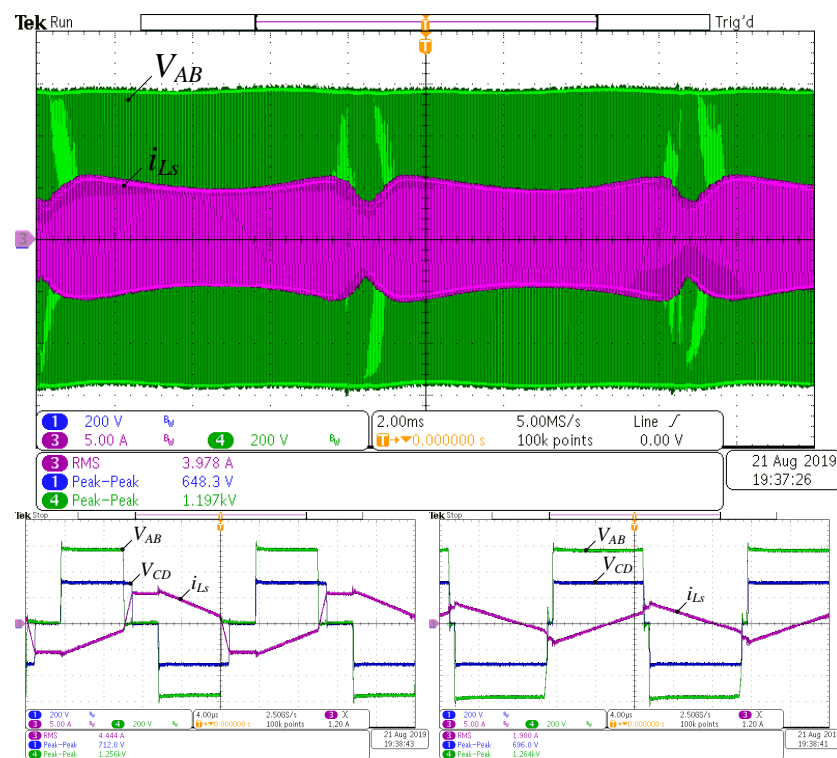


Figure 14. Experimental results: transformer voltages  $V_{AB}$ ,  $V_{CD}$  and secondary current  $I_{Ls}$  for nominal operation and different grid phase angles  $w_g t$ .

For the validation of the bidirectional power flow control, a step from 150 W to  $-150$  W was made, as shown in Figure 16. The transition from grid-to-vehicle to vehicle-to-grid mode occurs smoothly; thus, the phase between grid voltage and input current is shifted by  $180^\circ$ . The secondary DC-link voltage  $V_2$  demonstrates good dynamic response (settling time of 0.4 s), with a voltage overshoot of less than 8% of the nominal voltage. Figure 17 shows the dynamic response of the converter when using the output voltage controller with a high-bandwidth (3.6 kHz). It can be observed that the settling time of 0.04 s is sufficiently high for battery charging applications.

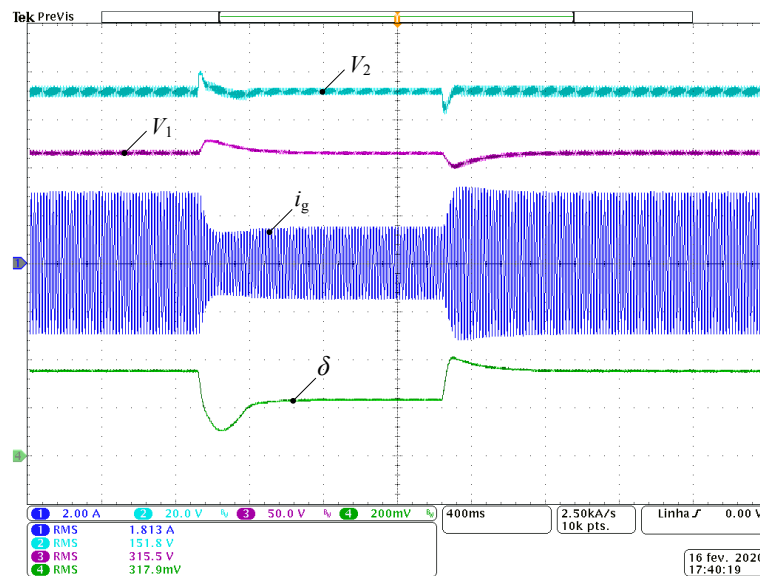


Figure 15. Experimental results: measurements for a load transient (400 W → 200 W → 400 W). Input current  $i_g$ , primary  $V_1$  and secondary  $V_2$  DC-link voltage and phase-shift angle  $\delta$ .

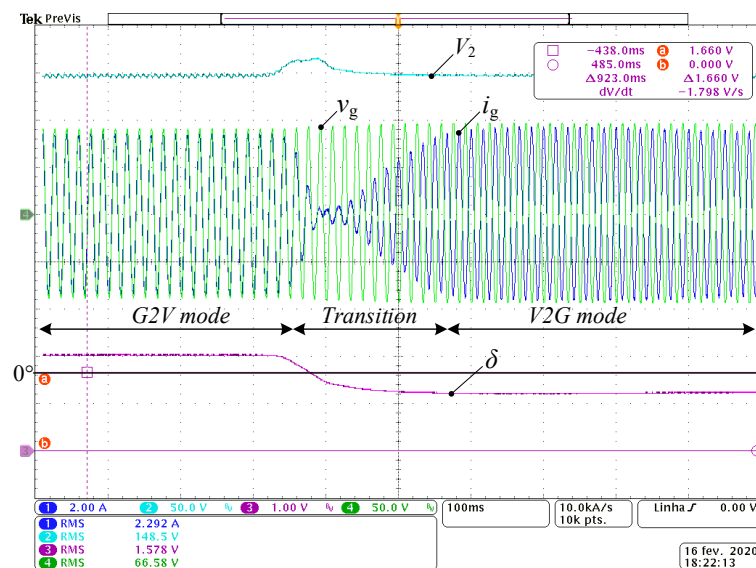


Figure 16. Experimental results: grid voltage, input current and phase-shift angle  $\delta$  for a load step from 150 W to -150 W representing bidirectional power flow (G2V → V2G).

As analyzed in Section 2.4, the low-frequency ripple power can be compensated by the variation of phase-shift angles. PS is generated by the output of the secondary voltage controller; thus, for this application, it was proposed as a control strategy with a high bandwidth in order to obtain high instantaneous power balance between the grid and the load. Figure 18 shows that the waveforms of the  $\delta$  angle starts as a constant value and, for a higher frequency (3.6 kHz), it has the same shape of Figure 7, validating the analytical equations presented. Increasing the zero cross frequency  $f_c$  of the controller  $C_{v0}$  from 36 Hz up to 3.6 kHz reduces voltage ripple for about 80% from the initial frequency design, as shown in Figure 19. Moreover, using a fast controller improved load transient responses.

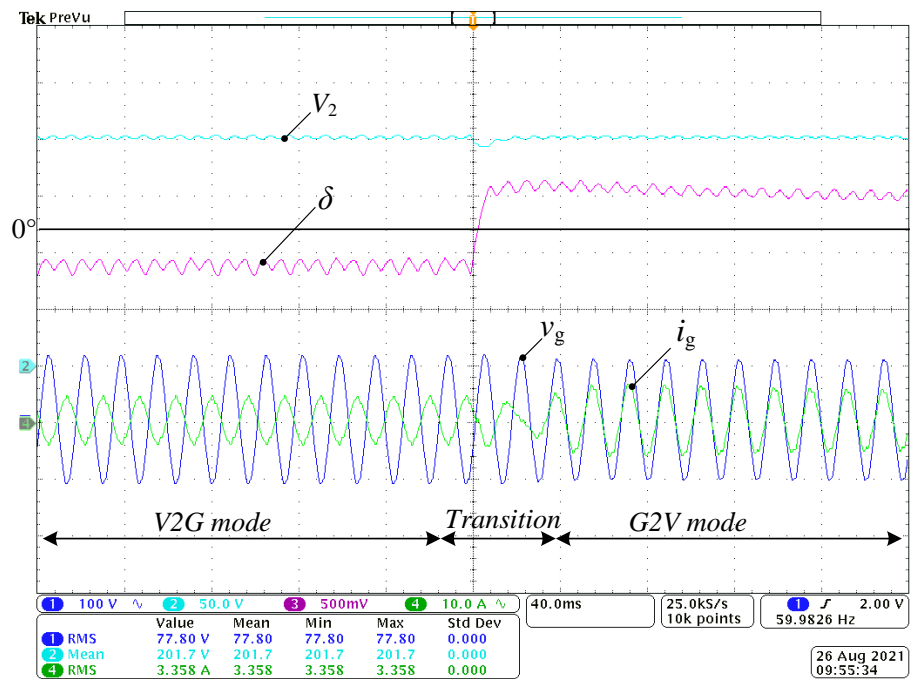


Figure 17. Experimental results: grid voltage, input current and phase-shift angle  $\delta$  for a load step from  $-275$  W to  $330$  W representing bidirectional power flow ( $V2G \rightarrow G2V$ ).

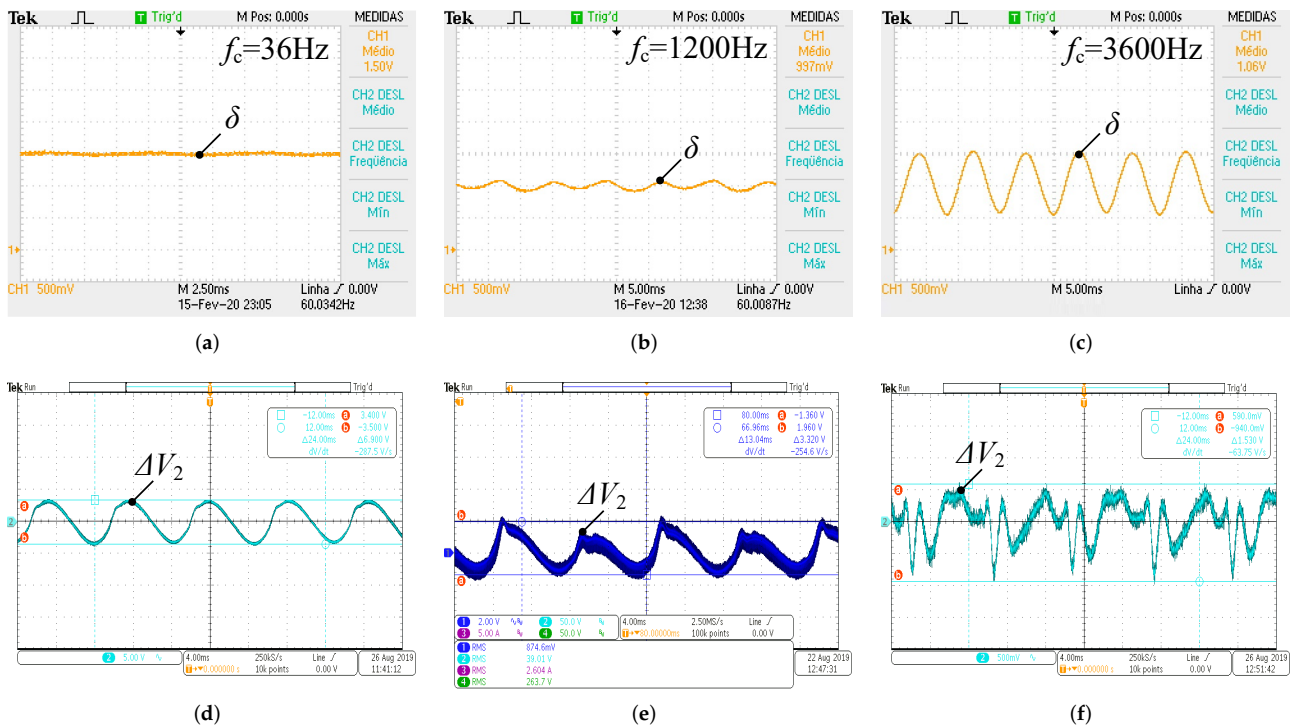
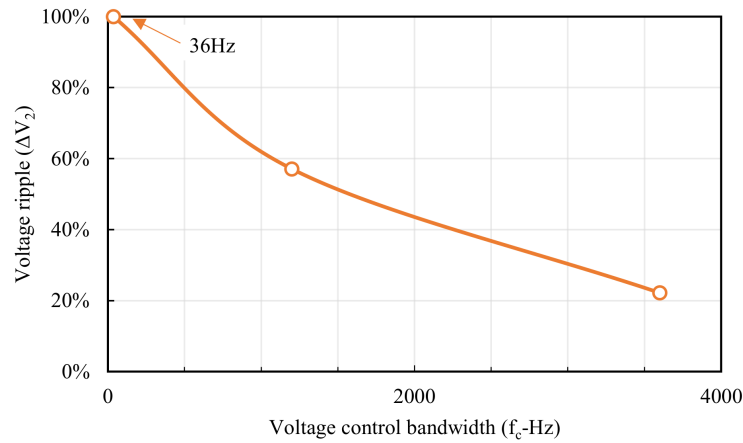
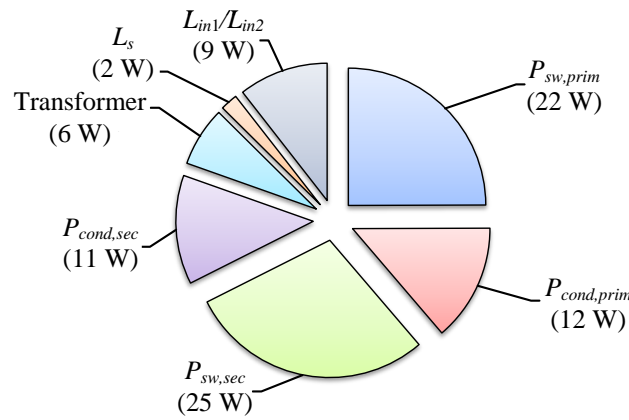


Figure 18. Experimental results: Phase-shift angle  $\delta$  and secondary DC-link voltage ripple  $\Delta V_2$  at different zero cross frequencies of the secondary voltage controller  $C_{vo}$ . (a)  $\delta$  variation with  $f_c = 36$  Hz. (b)  $\delta$  variation with  $f_c = 1200$  Hz. (c)  $\delta$  variation with  $f_c = 3600$  Hz. (d) Secondary DC-link voltage ripple with  $f_c = 36$  Hz. (e) Secondary DC-link voltage ripple with  $f_c = 1200$  Hz. (f) secondary DC-link voltage ripple with  $f_c = 3600$  Hz.

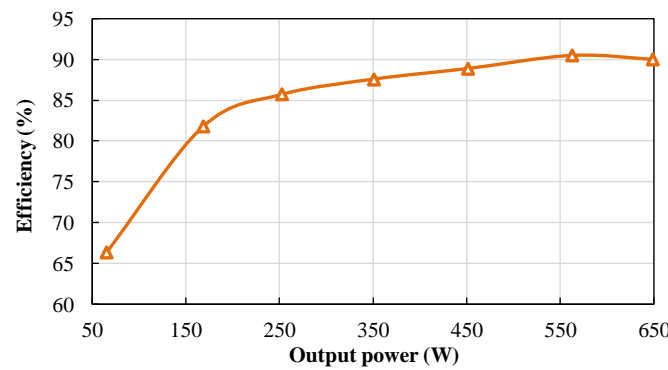
The breakdown losses among the main components of the proposed topology are shown in Figure 20a. According to loss distribution, more than 70% of the total losses account for semiconductors losses (conduction + switching). Magnetic components represent one-fifth of the losses and mostly occur in the windings of the HF transformer. Figure 20b shows measured converter efficiency with the rated parameters of Table 2. The measurement has not considered the auxiliary power supply for the gate drivers, fan and control board. Efficiency is over 90% for output powers higher than 500 W.



**Figure 19.** Secondary DC-link voltage ripple  $\Delta V_2$  at different zero cross frequencies of secondary voltage controller. Increasing controller bandwidth produces an output  $\delta$  capable of low-frequency ripple reduction.



(a)



(b)

**Figure 20.** Experimental results: (a) component losses; (b) measured efficiency of the proposed converter.



#### 4. Conclusions

In this paper, a novel single-stage single-phase AC/DC converter was proposed and analyzed, which features high-frequency galvanic isolation, bidirectional power conversion capability and a high degree of component integration. The main design expressions, modulation scheme and control strategy have been presented. Power flow control is performed by using the phase-shift (PS) technique, i.e., controlling the angle between primary and secondary sides through an HF transformer, while the sinusoidal variation of the duty-cycle allows power factor correction. Compared to state-of-the-art solutions, this converter operates as a single-stage topology and with independent control loops between the primary and secondary sides. The main advantages of the proposed topology is that it uses unidirectional switches and requires fewer semiconductors than other existing bidirectional isolated AC/DC converters, thus reducing circuit complexity. The main difficulties of the proposed topology include the design of power transfer inductance, since its value is directly related to the phase-shift angle and, consequently, power flow.

The proposed control strategy, based on a simple and widely known proportional-integral controller, allows achieving power decoupling on the DC side of the converter without any additional components, minimizes secondary voltage ripples by 80% when compared to traditional solutions and also reduces DC-link capacitance at the secondary side. Finally, in order to validate the converter operation, a 650 W SiC-based hardware prototype has been built and tested. At nominal operating conditions, a power efficiency of 90.3% and an input current THD of 2.76% have been measured, which is within the regulatory restrictions for PFC rectifiers (IEC 61000-3-2 standard). The experimental results show that the topology is well suited for bidirectional OBCs enabling V2G functionalities. The reduced-scale prototype was built to validate the concept, but this topology can be used as level 1 or 2 OBCs and operate with a wide range of input–output voltage to meet the grid and battery requirements. Further research will focus on the investigation of efficiency and power density improvements that can be achieved based on alternative control schemes and modifications of topology structure.

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