Article

Evolution Trends and Paradigms of Low Noise Frequency Synthesis and Signal Conversion Using Silicon Technologies

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Abstract: Silicon technologies for HF applications have been proven for more than two decades, and technologies have greatly evolved. Whether CMOS or BiCMOS technologies, the unique combination of radio frequency, baseband, and digital functions allow a very high level of integration. While it is possible to achieve fully integrated transceivers, the major advantages of these silicon technologies lie mainly in their unparalleled performance in the field of frequency synthesis and frequency conversion. We propose in this paper a review of the major results obtained on these RF components since the beginning of the 2000s, also considering the impact of the technology node. The back-end of line (BEOL) process on which depends the quality of microwave monolithic integrated circuits (MMICs) is briefly presented in the introductory part. If circuit performances are tightly bound to the active devices (i.e., the heterojunction bipolar transistor SiGe HBT or CMOS transistor), passive elements (i.e., quality factor of inductors and varactors, losses of transmission, or interconnection lines) as well as the definition of the substrate also play a major role. The core of the article is oriented toward the noise of synthesized signals and frequency conversion. Frequency synthesis is presented through the analog design of a voltage-controlled oscillator (VCO) or through the direct digital frequency synthesis (DDFS), for which respective figures of merit are presented and discussed in a second section. The spectral purity of the oscillators being decisive in the definition of the throughput of a link is approached through the comparison of different figures of merit (FoM) for a set of circuits achievements over the selected period. If the realization of free oscillators is closely bound to the phase-locked loop (PLL)-type control loop for VCOs, the DDFS solution provides more direct and more flexible alternative at first sight. Therefore, these two solutions are analyzed collectively. Finally, the oscillator integrated in the transmitter or receiver supplies the needed LO (local oscillator) power to the frequency mixer in the frequency conversion module: henceforth, the third part of this study focuses on high-frequency mixer realizations. We thus consider this LO power in some advanced figure of merit mentioned in the second section. The design trade-off of the mixer is presented in an approach combining LO (conversion gain, channel isolation, and phase noise) and RF (HF noise figure and channel isolation) constraints. The final section provides a summary of the results and trends mentioned in the paper.

Keywords: MMIC; CMOS; SiGe HBT; low phase noise; spurious signals; VCO; DDFS; DDS; mixer; frequency conversion

1. Introduction

The integration of electronic functions has been one of the motivations for technological developments. Since the first MMIC developed in 1975 by R. Pengelly and J. Turner [1], it was possible to develop both active and passive devices on the same substrate. If the first MMICs were developed at the border between X-band and Ku-band [2], then the first low-noise amplifiers (LNA) and power amplifiers (PA) demonstrators were developed in S-band for multifunction electronically scanned adaptive radar (MESAR) purposes under a joint program between Plessey Central Research Laboratories and Roke Manor Research Limited. There has been a lot of progress since the first achievement to the commercialization of

MMIC circuits, first developed on GaAs substrates in the 1980s, then on silicon substrates at the end of the 1990s for BiCMOS technologies such as initiated by IBM [3] followed by many telecommunication companies. From this latter technology, it was possible to combine CMOS transistors for digital functions with SiGe HBTs for high-frequency analog applications, although the Si substrate has higher loss than the GaAs substrate. The active device fabrication process optimization is crucial as it defines the maximum operating frequency (transition frequency f_t or maximum oscillation frequency $f_{\max}$) and the available power of a technology. If the trade-off between power and frequency defines a technology's roadmap, noise performance is also required on additive noise sources (noise floor for the low noise amplifier LNA on the receiver side) and on excess noise sources (to be considered with additive linear noise sources for frequency synthesis). At the beginning, the CMOS process was envisaged for low-frequency digital applications while III-V GaAs or InP devices were dedicated to high-frequency analog applications. The introduction of Germanium in the base of silicon heterojunction bipolar transistors (SiGe HBT) has opened the way for high-frequency applications due to the good electron mobility together with the reduction of the base resistivity. Then, the association of SiGe:C HBT (the addition of carbon to reduce the exodiffusion of Boron and to allow steep doping profiles) and CMOS made possible BiCMOS processes for a low-cost high integration level with digitally controlled functions. The evolution trend of f_t and $f_{\max}$ as proposed in the BiCMOS survey in [4], is linked to the shrinking in the dimension of the transistors and to the mastery of their process. Advanced European projects such as DOTSEVEN [5], or the TARANTO project [6], paved the way to the increase in f_t and $f_{\max}$ (such as the T-Music project under DARPA control [7]). For HBT, the development of double-polysilicon self-aligned (DPSA) process, have considerably improved the operating frequency [8], with $f_{\max}$ up to 400 GHz [9]. Reducing the gate length also targets the same trends for denser CMOS nodes. While the CMOS frequency limit has improved significantly with the reduction in gate length (shrinking of the technology node) to compete with SiGe BiCMOS, the latter still offers the best frequency/noise/power performance. It should be pointed out that the HBT roadmap for BiCMOS technologies is not linked to the law of shrinkage of CMOS node (Moore's law), but the decisive reduction in the CMOS gate length reduces the gap between HBT and CMOS when these bipolar devices are not technologically upgraded (improved) and do not offer a significant advantage on their performances over the downscaled CMOS devices. For standalone RF functions, the area of the chip is dominated by inductors and pads, and BiCMOS technology can represent a lower-cost solution than CMOS, even considering its more complex process (estimated at around +20% for BiCMOS) It should be noted that the size of these passive elements does not change significantly from one process to another one (including III-V technologies). However, the reduction of the CMOS node becomes a major argument when the digital functions balance favorably with the analog functions, thanks to the scaling of the chip with the lithographic dimension.

This article focuses on (SiGe Bi)CMOS silicon circuits operating at frequencies below 100 GHz (and above 2.5 GHz) where most of the high-frequency applications are proposed. If demonstrators of fully integrated transceivers have been proposed in the literature [10,11] even above 100 GHz [12], BiCMOS technologies can hardly compete with GaAs (or InP and also GaN) technologies for high-power or low-level amplification. However, the benefit of mixed-signal makes this technology a first choice for frequency conversion, by considering a fully integrated chip with local oscillator (PLL or DDFS) with the mixer, even to the baseband signal module (Figure 1, depicts an architecture of a zero-IF demodulation).
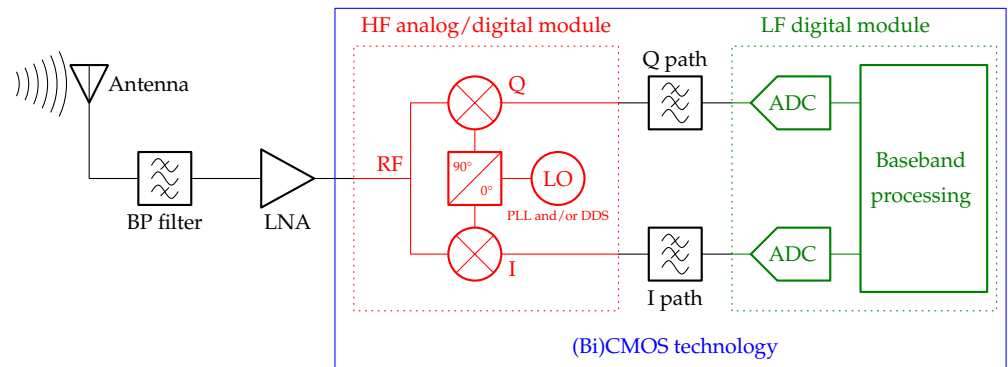
Figure 1. Zero-IF receiver architecture, comprising the analog and digital part which can be integrated on the same (Bi)CMOS chip for high purity frequency signal (down)conversion.

This article provides an overview of the frequency synthesis (VCO used for PLL or DDFS) and of the frequency mixer developed over the past two decades on CMOS and BiCMOS silicon technologies. The objective is to identify some effective design topologies, or trends, for each HF function and to propose a discussion on the articulation between the frequency synthesis of the local oscillator and the frequency mixer (Figure 1, red box). In fully integrated MMIC transceivers (TxRx), either transmit (power amplifier, PA) or receive (low noise amplifier, LNA) amplifiers can be designed on the same (Bi)CMOS chip. However, if these circuits can be processed with silicon HF technologies according to the needs of a specific radio-link budget, the best performances in power or in noise factor (respectively, in transmission or reception) are achieved with III-N or III-V technologies.

From selecting a technological development to designing specific high-frequency functions, there is a gap that is not easily bridged. The choice of a technology depends on the quality of its active and passive devices in a complete BEOL vision. Each device is usually assessed by specific figures of merit (FoMs). These FoM are diverse and change when considering the device alone (active or passive device) or when it comes to integrating it into different circuits or systems. These FoM must be representative or relevant to the targeted applications, at the device level as well as at the circuit level.

On the one hand, $f_{\max}$ or f_t are always useful at first to assess the ability of a transistor to operate in a given frequency band, while the compression point or the noise figure are, respectively, more relevant to select the transistor for designing amplifiers, respectively, at the transmitter or receiver side. On the other hand, passive devices such as transmission lines, capacitors (varactors), and inductors are essentially characterized by their losses or quality factors. In the end, it is quite difficult to anticipate the figure of merit of a circuit, but this FoM must be sufficiently revealing of the aptitudes of the circuit under concern to fulfill its mission, and thus help users in their technological selection. Here, the circuits under concern are the VCO, the DDFS, and the mixer: all these circuits can be efficiently embedded together on the same MMIC chip, as the design of such complex analog and mixed-signal circuits is possible in a (Bi)CMOS technology for VLSI products. An example of a 20 GHz PLL and mixer is given in Figure 2, realized with BiCMOS7RF process from ST microelectronics.
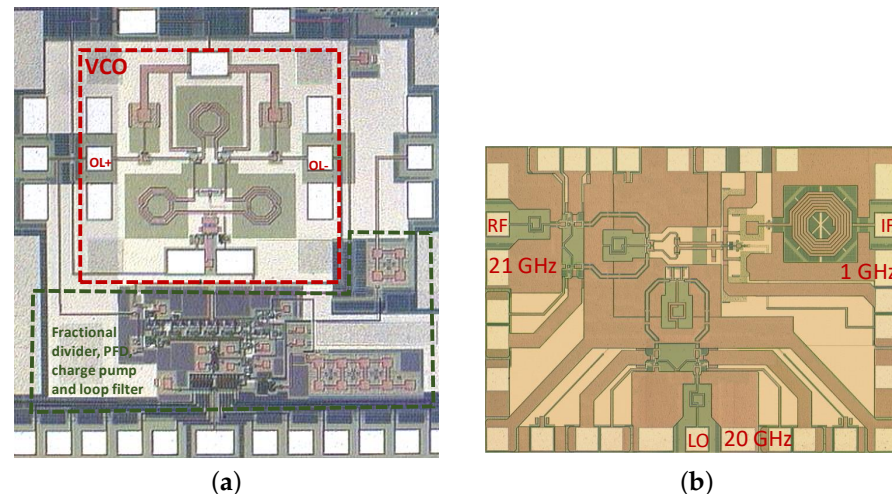
Figure 2. Microphotographs of: (**a**) a 20 GHz PLL (LO) based on a push-push differential VCO and using a fractional digital divider, and (**b**) a 21 GHz (RF) to 1 GHz (IF) mixer. These circuits have been designed by the authors from LAAS-CNRS and developed with BiCMOS technologies from ST-Microelectronics (BiCMOS 7RF), 2003.

Interfacing between the VCO and the PLL is a common view for the engineering of a frequency source, while association of the VCO with the mixer is less usual (Figure 3). However, from an RF design perspective, there are various parameters to optimize between the LO access of the mixer and the dynamic output access of the VCO. Indeed, the VCO output power sets the conversion gain of the mixer, while the mixer load sets the pulling of the VCO as well as part of its phase noise (depending on the chosen topology). Then, using a buffer amplifier cascaded with the VCO can help addressing roughly these trade-offs. Few of the VCO publications consider the output power to be a major factor of merit, as is discussed in the section on frequency sources. The design of the VCO with the PLL is not the only way, and an optimization of the VCO together with the mixer in an analog-oriented design as depicted in Figure 3 has been found to be very efficient by previous works from the authors (not published) and is largely used for the design of monolithic transceivers. Thus, if the recent topology mixers also embed image rejection filters, and if the VCO is generally balanced with two 90° phase-shifted outputs connected to the I-Q mixers (a simplified structure is presented in Figure 1), the PLL is still designed aside with the VCO in a first intention. A fully integrated frequency converter, i.e., the frequency synthesizer and the mixer, in a (Bi)CMOS technology (DDFS digital solution or the VCO with the phase/frequency detector, charge pump and loop filter, frequency divider on the same die with the mixer) stands as an attractive solution in terms of performance/cost as far as VCOs offer state-of-the-art phase noise performances. In Figure 3, the green parts represent the digital functions, and the red parts depict the analog circuits. The second section of this article presents a study on the analog and digital solutions that can be used for frequency synthesis using VCO and DDFS, respectively. For the sake of simplicity, the discussion does not include the whole PLL circuit. In the third section, an overview on mixers is also performed. Then, the last section aims to bridge the frequency synthesis with the mixer for an efficient design of a frequency converter in (Bi)CMOS technologies. To make a simple but fair comparison between designs of the same family of circuits which can be optimized for different purposes, it is common practice to use a figure of merit (FoM). Within this paper, various FoMs are presented and discussed. The purpose of such FoMs is to objectively translate the impact of the main performance parameters of an electronic function through a single figure. An efficient FoM must include most of the characteristics of the circuit: one has to keep in mind that a trade off between some of these parameters is usually mandatory in order to optimize the targeted parameter at the expense of another one. Then, an appropriate FoM should remain unchanged if a simultaneous

modification of two dependent parameters occurs in the same proportion compared to that of their dependence.
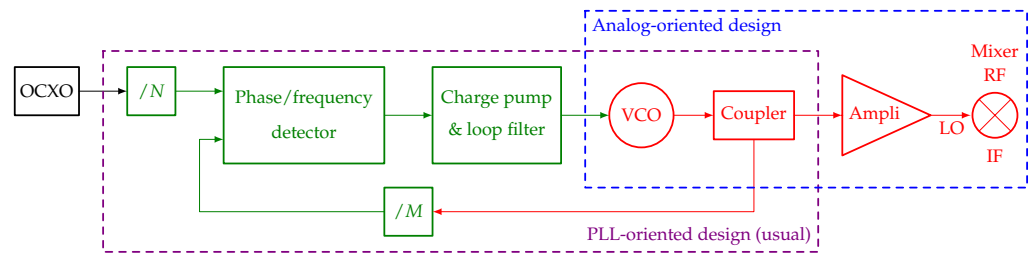
Figure 3. Two approaches for the design of a frequency converter. PLL oriented (purple box) starts with PLL integration and then with adding the modules for interfacing with the mixer. Analog-oriented design (blue box) considers the mixer's performances together with the VCO design (impact of the coupler topology, of the LO access load of the mixer, output power of the VCO for the gain conversion optimization) and then combines with the PLL modules. The need for a buffer amplifier, and its impact on the DC consumption and phase noise must be included in both approaches.

2. Analog and Digital Frequency Synthesis

The frequency synthesis of microwave and millimeter wave sources can be developed by analog or digital circuit design, using a phase-locked loop (PLL) or direct digital frequency synthesis (DDFS) design, or even both. One crucial requirement for the frequency source generation concerns the lowering of its phase noise that enables the modulation scheme with large symbol constellations. The next section presents a review over up to two decades, related to (Bi)CMOS VCOs and DDFS.

2.1. Voltage Controlled Oscillator

The conception of tunable oscillators allowing very high performances of phase-noise to reach a high data rate is still a challenge for the designers. Different topologies of VCOs are available to fulfill the specific requirements of such equipment, as expected in its final context. FoMs have been developed and improved to better match with the intrinsic quality of these circuits. The introduction of an essential FoM still today (related to the phase noise electrical parameters) was proposed by Leeson [13]. When an oscillator's phase noise is optimized in the $-20\,\mathrm{dB/dec}$ region (i.e., neglecting the $1/f$ noise sources), then the corner frequency delimiting the RF noise floor and the $1/f$ excess noise source f_c is set to zero. Leeson's formula can be expressed as:

$$\mathscr{L}(f_m) = 10 \log \left[\left(\frac{f_0}{f_m} \right)^2 \frac{R_L}{Q_L^2} \frac{F\,k\,T}{V_0^2} \right] \tag{1}$$

where f_0 is the output frequency, f_m is the offset from the output frequency, Q_L is the loaded quality factor of the resonating tank, R_L is the equivalent parallel load resistance of the resonator at f_0, F is the oscillator excess noise factor, k is Boltzmann's constant, T is the absolute temperature in K, and V_0 is the amplitude of the oscillation, sometimes expressed as output power, and in general tends to be close to the saturated output power condition. The advantage of HBT over ultrascaled CMOS concerns their elevated oscillation amplitude (and possibly better $f_t/f_{\max}$), their lower $1/f$ noise contribution as well as the improved Q-factor for passive devices (high-quality substrate and thick metals, using small inductors), that represent keystone parameters for the design of low phase noise VCOs, as suggested by Equation (1). When the $1/f$ flicker noise source is preponderant on the thermal noise contribution, leading to a $1/f^3$ instead of a $1/f$ frequency regression around the carrier, other FoMs should be used, based on Leeson's empirical formula as found in [13], also considering the DC power consumption as proposed in [14] which leads to the formulation of $\mathrm{FoM}_{1/f}$ proposed by D. Ponton in [15].

If the designers first used this FoM from Equation (1) as a major parameter, most of them remained pragmatic and considered the VCO in its final integration with other modules (i.e., mixers). Then, new FoM started to add parametric to Leeson's formula to better account for the final integration with other analog circuits. Thus, the performance of an oscillator is largely evaluated by normalizing the FoM by frequency and DC power, as shown in Equation (2) where P_{DC} is referenced relative to 1 mW and usually designated by FoM_1.

$$\mathrm{FoM}_1 = \mathscr{L}(f_m) - 10\log\left[\left(\frac{f_0}{f_m}\right)^2 \frac{1}{P_{DC}}\right] = -10\log\left[\frac{R_L}{Q_L^2}\frac{F\,k\,T}{V_0^2}P_{DC}\right] \tag{2}$$

In the expression of FoM_1, the oscillator frequency f_0 is compensated; therefore, the excess noise factor F related to the active device and to the topology of the oscillator becomes a first-order parameter, as well as the loaded quality factor Q_L of the resonating tank and the output power related to the amplitude of the oscillation V_0. If the set of FoMs proposed in this article are negative, we can also find in the literature a positive representation of Equation (2) and of Equation (5). Here, the lower the FoM, the better the performances in the same logic as for Leeson's expression. Some authors consider that P_{DC} from FoM_1 can be associated with the dynamic power of the oscillator $V_0^2/(2\,R_L)$ as a power conversion efficiency factor. However, then the dynamic output power (also related to the oscillator's DC to AC power conversion) is not considered as an independent nor major parameter. A similar analogy could be made between the linear gain of an amplifier and its compression point to reveal the power level at the output of the amplifier. Nevertheless, in Equation (2), the SSB rejected noise is already normalized by the output power in $\mathscr{L}(f_m)$. These considerations have been used to augment Equation (2) into $FoM_{P_{RF}}$ by formally considering such a signal swing (then dynamic power P_{out}) in Equation (3) [16], as it decides whether or not a buffer amplifier is needed when connecting the VCO to the mixer.

$$\mathrm{FoM}_{P_{RF}} = \mathscr{L}(f_m) - 10\log\left[\left(\frac{f_0}{f_m}\right)^2 \frac{P_{out}}{P_{DC}}\right] \tag{3}$$

In addition, since this is evaluating tunable oscillators, Equation (4) adds the tuning range in the previous equations, expressed in percentage through TR% in $FoM_{P_{RF}\&T}$, with a small adjustment from the expression first proposed in [16] and also used in other works, some of them being referenced in the dedicated figure later in this article.

$$\mathrm{FoM}_{P_{RF}\&T} = \mathscr{L}(f_m) - 10\log\left[\left(\frac{f_0}{f_m}\right)^2 \left(\frac{\mathrm{TR}\,\%}{10}\right)^2 \frac{P_{out}}{P_{DC}}\right] \tag{4}$$

The same consideration is already applied through the widely used FoM_T, as expressed by Equation (5) derived from Equation (2).

$$\mathrm{FoM}_T = \mathscr{L}(f_m) - 10\log\left[\left(\frac{f_0}{f_m}\right)^2 \left(\frac{\mathrm{TR}\,\%}{10}\right)^2 \frac{1}{P_{DC}}\right] \tag{5}$$

Lastly, some designers also consider the area of the chip (normalized to 1 mm^2) in some FoM_A [17], but we do not discuss this FoM within this article. Figure 4 depicts the number of publications on VCOs over the selected period starting with the first BiCMOS articles.
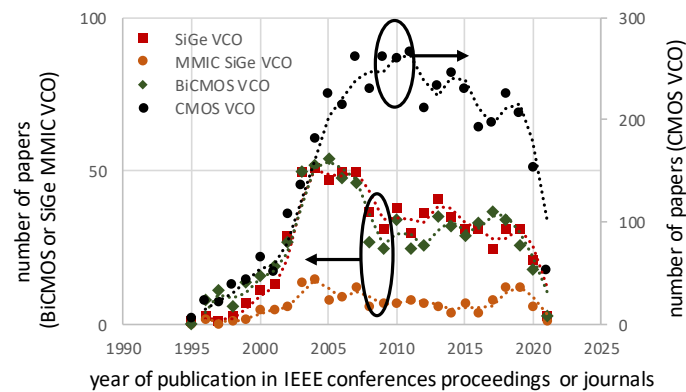
Figure 4. Publication trend between 1995 and 2020. Selection was made by keywords as proposed in the upper-left area.

CMOS-related works are up to six times that of BiCMOS studies, regardless of frequency. "SiGe VCO" and "BiCMOS VCO" follow the same trend as they are more or less related to the same articles. From these thousands of published articles, the references that were selected for the bibliography of this work relates to specific topologies or state-of-the-art performances or widely cited papers. Some of the references used for the discussion in this paper are represented in Figures 5–11 [16–32], along with some other nonreferenced pertinent publications and commercial products [33–40].

An interesting point is the evolution of the publication timeline selected by technological node (Figure 5): the trend clearly indicates the effort to shrink the gate length of CMOS transistors (starting at 0.35 µm in the middle of the 1990s and decreasing down to 40 or 28 nm in the 2010s) with the objective of increasing the maximum oscillating frequency f_{max}. If VCOs based on CMOS on silicon and more recently CMOS on SOI technologies always take advantage of the latest researches, it is not clear how this size reduction of the gate length really improves the Leeson's factor or other FoM from Equations (1)–(5), as the dynamic power also decreases and the low-frequency noise (LFN) increases when reducing the area of the active device (also losses or Q-factors of passives degrade with frequency). It must also be noticed that HBT devices are less impacted by the technological node, as the frequency dependence of these vertical devices dimensions mainly depend on the base thickness. This explains why the HBT are confined to a CMOS technological node between 0.13 µm and 0.35 µm in Figure 5. This evolution trend of technologies concerns both the transistors via their maximum oscillating frequency, their gain, their power and their electrical noise, and the passive devices aiming high-quality factors for transmission lines, capacitors, and inductors (using thick metal layers or 3D-multilayers facilities). Many strategies have been developed for this purpose, as clearly summarized by [41–43]. Compared to CMOS, SiGe HBT feature lower $1/f$ noise, higher voltage capability, and higher output resistance for a given frequency, which represents an advantage for VCO design.
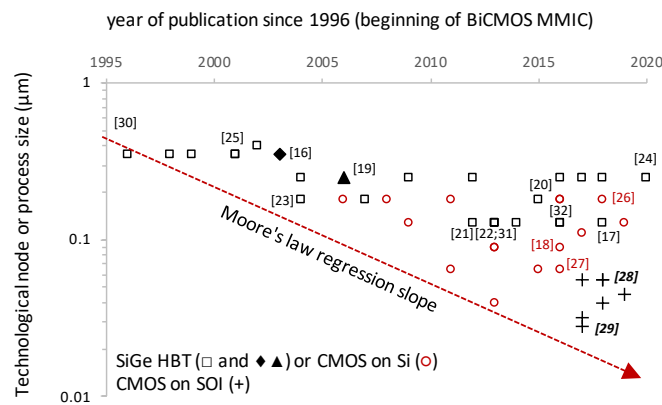
Figure 5. MMIC VCOs technological trends: the technological node used is plot versus the year of publication. BiCMOS HBT-based VCOs (□ and also authors' personal work ♦▲) and CMOS-based VCOs on Si (○) and SOI (+). The regression line illustrates Moore's law. Some references used in the paper are noted close to the associated symbol [16–40].

A special focus is given for frequencies above 5 GHz, even if few papers reported lower frequencies, using 65 nm CMOS technologies [27] or 0.25 μm BiCMOS technology [24]. This timeline starts with the first X-band MMIC BiCMOS VCO in 1996 [30]. Obviously, CMOS on Si nodes are well reported, also with the onset of CMOS on SOI from 2017. In Figure 6, the oscillation frequency of the selected (Bi)CMOS MMIC VCOs works is reported over the past two decades, where the same trend as in Figure 5 can be sensed through the increase in the synthesized frequencies.

An interesting way to represent the evolution trends is also to plot the oscillation frequency (a) and the Leeson's factor (b) versus the technological node as proposed in Figure 7. It could be expected to obtain degraded FoM when using a short gate length at low oscillation frequency for CMOS VCOs, as the low-frequency noise (LFN) source on the gate of CMOS transistors increases with the reduction of the gate pad (notice: PMOS features better phase noise than NMOS). But in [27] where a 65 nm technological node is used to design a 2.46 GHz CMOS VCO, both the Leeson's phase noise taken at 1 MHz distance of the oscillation frequency (Figure 7b), FoM_T (Figure 10a,b), and $\text{FoM}_{P_{RF}\&T}$ (Figure 11a,b) are positioned more or less at the state of the art of academic papers. It can be appreciated from Figure 8b that the Leeson's factor $\mathcal{L}(f_m)$, $\mathcal{L}(1\,\text{MHz})$ for this work is almost proportional to the oscillation frequency, at least in its best case of trend. FoM_T and $\text{FoM}_{P_{RF}\&T}$ are by their mathematical construction, independent from the frequency of oscillation; this makes the comparison easier between the selected articles as proposed in what follows.
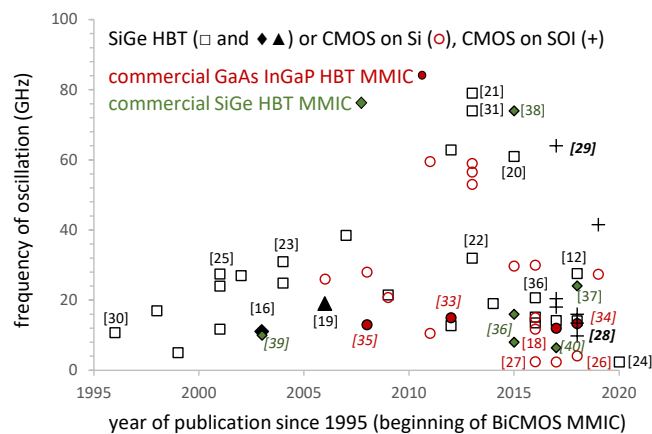
Figure 6. Evolution of oscillating frequencies for MMIC (Bi)CMOS VCOs from 1995 to 2020. Some references used in the paper are noted close to the associated symbol [16–40].

From Figure 7a, the best performance for CMOS VCOs on silicon, regarding Leeson's equation, is obtained for frequencies of oscillation below 10 GHz [26,27] while this figure of merit degrades by 20 dB or more for frequencies above 30 GHz. The same differentiation can be conducted on BiCMOS VCOs below 30 GHz [16,19,23,25] and above 40 GHz [20,21,31]. It is worth noticing that the performances of the VCO regarding the size of the active device or the quality factor of passive elements strongly depend on the frequency: the *Q*-factor of inductors degrades as the losses increase with frequency, whereas LFN sources degrade as the transistor size is reduced to reach higher frequencies (and to cop with the parasitic effects on the gain of the transistor). This is clearly illustrated in Figure 8b with the parameter $\mathscr{L}(f_m)$ plotted versus the oscillation frequency. It is interesting noticing the improvement of $\mathscr{L}(f_m)$ over the proposed period in Figure 8a. This can be attributed to an improvement of the gain of active devices with a better process mastering of the passive elements and of the noise sources in the active transistors. Still some realizations offer variable $\mathscr{L}(f_m)$ performances when used for higher-frequency bands. At first glance, the technological node does not appear as a first-order differentiating parameter for the quality of the oscillators: it just broadens the frequency range to synthesize RF signals.
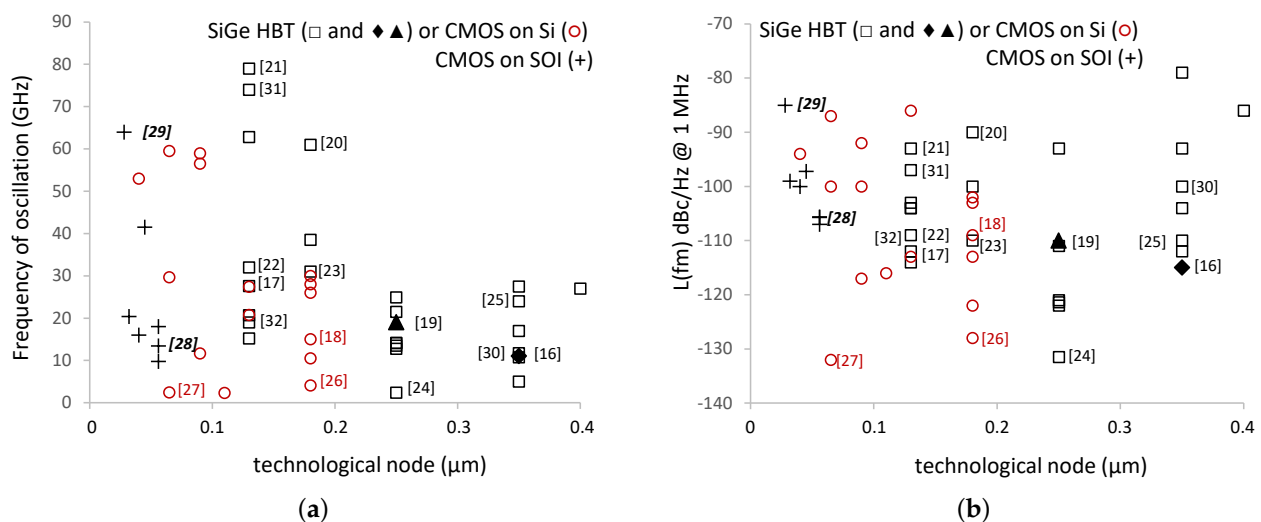
**Figure 7.** Evolution of the MMICs VCO oscillation frequencies (**a**) and Leeson's factor (**b**) versus the technological node. Some references used in the paper are noted close to the associated symbol [16–40].

From Figure 8 and on the next figures related to FoMs, the performances of commercial MMIC VCOs are plotted for SiGe HBT and III-V HBT (narrow bandgap) technologies [33–40]. The best results for commercial circuits, compared with R&D works, can be explained by the high technology readiness level (TRL9) associated with such circuits, thus by a better mastering of defects (LFN sources) or electrical performances of active devices, as well as the losses of passive elements. GaAs or InGaP HBT-based VCOs take advantage of the high-quality passive elements and low LFN transistors allowing high voltage swings as required by Leeson's formula. In addition, it should be considered that these commercial solutions are available in the lower-frequency band of the study, for which the mastery of the technology has been more effectively exploited both at the front- and back-end of line levels. Then, the technological node is not really a marker of improved or degraded figures of merit. However, the targeted oscillation frequency makes it more or less easy to simultaneously obtain a high gain (or low losses for the passive) and low-frequency noise reduction of the transistor, due to the size reduction of the active device linked to the rise in frequency.

(a)

(b)
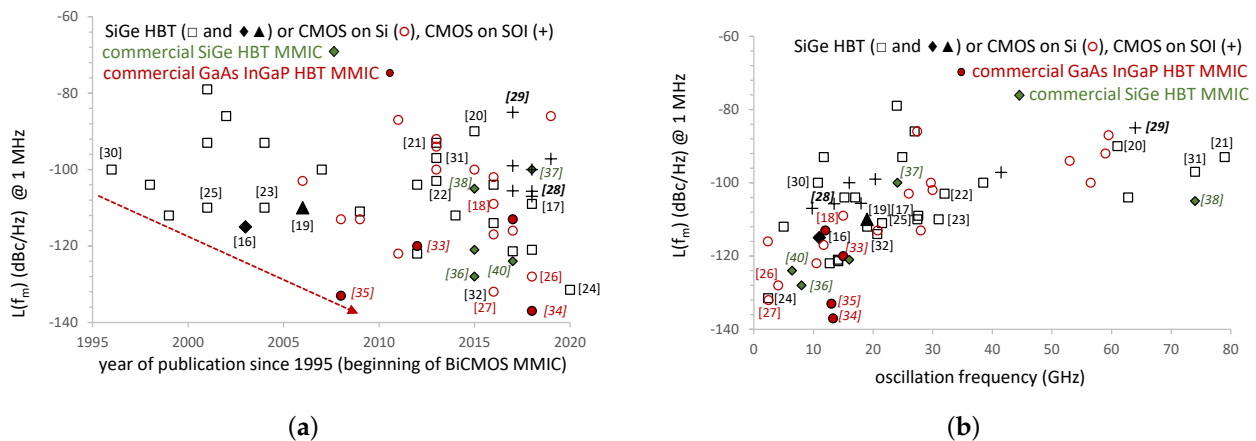
Figure 8. Evolution of Leeson's figure of merit (**a**) versus the year of publication (timeline) and (**b**) versus the oscillation frequency. Some references used in the paper are noted close to the associated symbol [16–40].

Thus, the topology of the circuit must be considered as a differentiating element: more precisely, the passive inductance-capacitance structure of the resonant tank must be considered in conjunction with the optimization of the conversion of the LFN sources in the active device (and with its biasing mode). Among the very large number of architectures (some of the main architectures being summarized in a simplified form in Figure 9), we can mention the classical Clapp or Colpitts simple structure, push-push cross-coupled, quadrature VCO, tail capacitive feedback, biasing class B/C/D topologies, which are often upgraded or merged according to the strategy for improving the phase noise, the power efficiency, or the tuning range (TR). Some topologies can reduce the LFN contribution as for Clapp or Colpitts structures where the noise source at the input of the transistor flows back to the resonating tank.

A reflective topology (negative resistance) has proven to give better results than transmission topology in X-band [16] once the input LFN source is lowered thanks to an appropriate biasing. However, a trade-off must be performed between the phase noise, the dynamic output power, and the power consumption. As seen in Figure 10a,b, the performances of these first MMIC BiCMOS VCOs between 10 and 30 GHz based on different topologies [16,19,23,25] are still competing with the state of the art two decades later. Moreover, a Clapp or Colpitts topology generates a small amplitude of oscillation, and it is usually designed with a Cascode amplifier to meet the RF power level requirements. Most designs using CMOS or SiGe HBT technology are based on a crosscoupled Colpitts structure [21,28,29,32], where the core oscillator frequency is only half of the output frequency. However, this crosscoupled schematic introduces a delay between the symmetrized transistors, usually at the price of a frequency reduction. In addition, the delay time introduced by the structure symmetry necessitates higher f_{max}/f_t (smaller) devices, at the cost of degraded LFN and P_{RF} if the targeted oscillation frequency is well below f_{max}. To alleviate the impact of the delay time, Colpitts push-push topology [19] is prone to improve the phase noise by adjusting the series feedback inductors on the emitters or sources together with the resonating tank structure and also to broaden the negative resistance over the desired TR. In addition, a 3 dB improvement on P_{RF} can be achieved with these differential topologies. However, if this topology allows a fundamental at $f_0/2$ with consequent advantage for parasitic reduction and for improved Q of the varactor, push-push structure makes it difficult to achieve a good isolation between the resonating tank and the negative resistance. Phase noise performances $\mathscr{L}(f_m)$, FoM_T or also $FoM_{P_{RF}\&T}$, can significantly vary with almost 50 dB variation for these FoMs, resulting in degraded FoM_T and $FoM_{P_{RF}\&T}$ as seen in Figures 10 and 11. Considering almost the same frequency of oscillation, the metrics from [16] published in 2003 (using a 0.35 μm BiCMOS) and from [28] published in 2017 (using a 56 nm CMOS on SOI) propose 3 decades lower FoM_T than that for the

first published X-band VCO to the authors knowledge [30] (developed with a 0.35 μm BiCMOS). By contrast, VCOs from [27] (CMOS on Si) and [29] (CMOS on SOI) present a similar FoM_T (Figure 10a,b) for almost identical technological node and for the same period of publication, but for frequencies, respectively, at 2.46 and 64 GHz. Of course, the mastery of all design optimization positions, the quality of the electrical and noise models, and the improvement of the technological processes with time largely explain such differences as illustrated in Figures 10 and 11. Therefore, commercial products clearly propose the best FoM_T and $FoM_{P_{RF}\&T}$ but usually at moderate frequencies (X-band) and with quite recent designs (after 2007 for the best InGaP HBT MMIC VCO [35] and 2015 for SiGe BiCMOS VCO [36]). In Figure 10, the increase in FoM_T for the higher frequencies above 40 GHz is also clear, as justified earlier by the difficulty to achieve low losses passive devices for the resonating tank together with high gain-power and low-noise active devices when frequency increases. However, some articles present adjustments such as a fine optimization of the Q-factor of the varactor [41], the introduction of noise filtering techniques [24], or also the use of a g_m-boosted topology [32], which helps to keep these FoMs at the state of the art of R&D results [20,21,29,31].
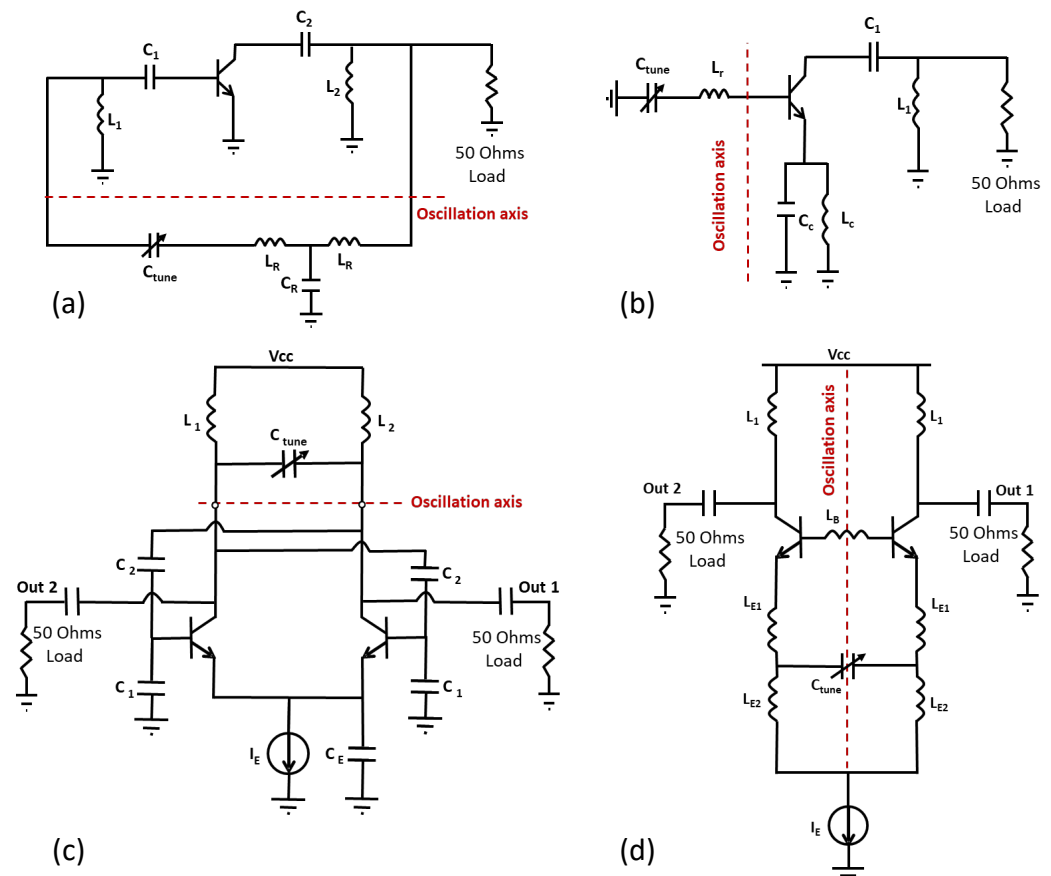
Figure 9. Main simplified topologies of HF oscillators with (**a**) parallel, (**b**) reflection, (**c**) crosscoupled, and (**d**) balanced push-push architectures.

Beyond the transistor configuration (negative resistance), the resonating tank must enable a large tuning range with effective high-Q as formulated in Equation (1) for which the reduction of the losses is crucial, as accounted for in Equations (4) and (5) for FoM_T and $FoM_{P_{RF}\&T}$, respectively, depicted in Figures 10 and 11. However, varactors generally feature poor Q at elevated frequencies, as inductors do in spite of optimized small inductors (and thick metal lines). The design of the tank inductor is constrained by both the Q-factor and the oscillation amplitude. To minimize the phase noise, according to Leeson's formula, the resonant tank must work with high capacitance and low inductance. The inductance value is determined according to the varactor size that meets the specification of TR. If some

articles make use of high-*Q* active capacitors to compensate the loss of the passives [20], the topology of the tank is closely bound to the noisy active device, and this represents the main optimization axis if the LFN sources are accurately represented and positioned in the transistor electrical model. Lastly, the biasing of the active device can boost the power efficiency as needed in FoMs from Equations (2) to (5). Class-C can improve by 3 dB the phase noise that can be achieved using the Class-B biasing mode. On the other hand, (P)MOS transistors could unfortunately be biased in the triode region when biased in class C, resulting in losses in the active device and thus phase noise degradation. The saturation of the transistor must be avoided at all costs, using limiting or automatic gain control techniques. However, if these techniques have been proved to be efficient to avoid a phase noise degradation, they do not necessarily improve it, and the related FoMs do not necessarily stand out on the trends from Figures 10 and 11 by comparison with conventional topologies.
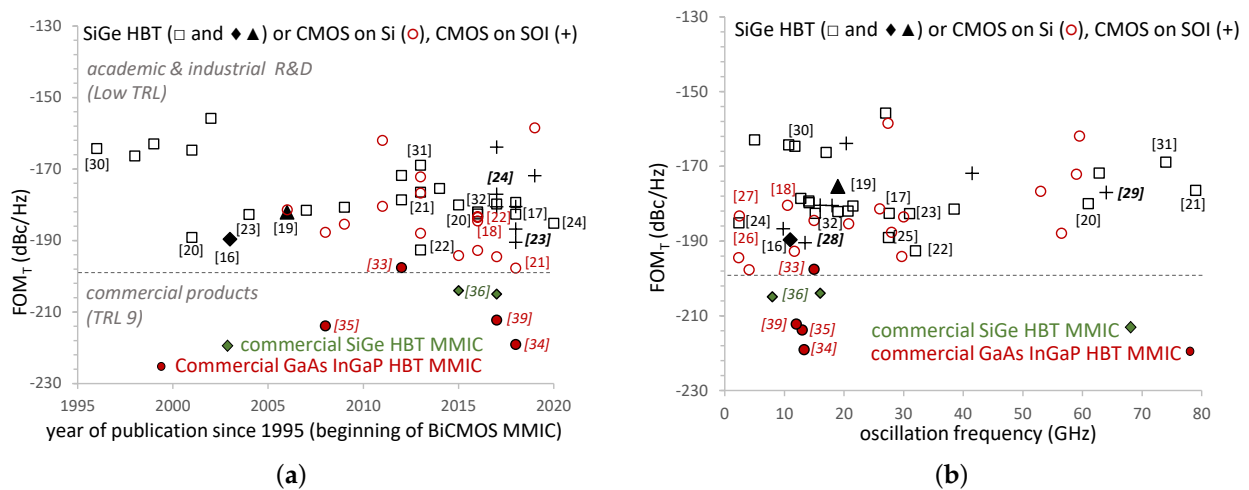
Figure 10. Evolution of the FoM$_T$ metric (Equation (5)) (**a**) with the year of publication (**b**) versus the oscillation frequency. Some references used in the paper are noted close to the associated symbol [16–40].

Lastly, from a raw comparison between Figures 10 and 11, it can be observed that there is no big gap on FoM$_T$ between commercial and R&D oscillators in Figure 10, whereas this distinction is clearer on FoM$_{P_{RF}\&T}$ in Figure 11. As FoM$_{P_{RF}\&T}$ is not widely distributed and used in the literature, this means that P_{RF} dynamic output power is not strongly considered as a major parameter by some R&D designers, but it is obviously a representative parameter for manufacturers. Thus, [16,18,23,25,31] based on HBT BiCMOS process provide high-performance FoM$_T$ and FoM$_{P_{RF}\&T}$, while [20] deviates from the best trend for FoM$_{P_{RF}\&T}$ in Figure 11b. It can be noted the advantage of HBT devices used in these selected articles, over their CMOS counterparts regarding the FoM$_{P_{RF}\&T}$ metric, thanks to higher output voltages. Obviously, P_{RF} is related to the complexity of the architecture of the VCO (and to its P_{DC} consumption if designers aim to optimize FoM$_T$). However, it also determines the power budget between the output of the oscillator and the LO input of the mixer (the necessity to use or not use a buffer amplifier). The low number of articles specifying the P_{RF} parameter should be noted in Figure 11 compared to Figure 10.
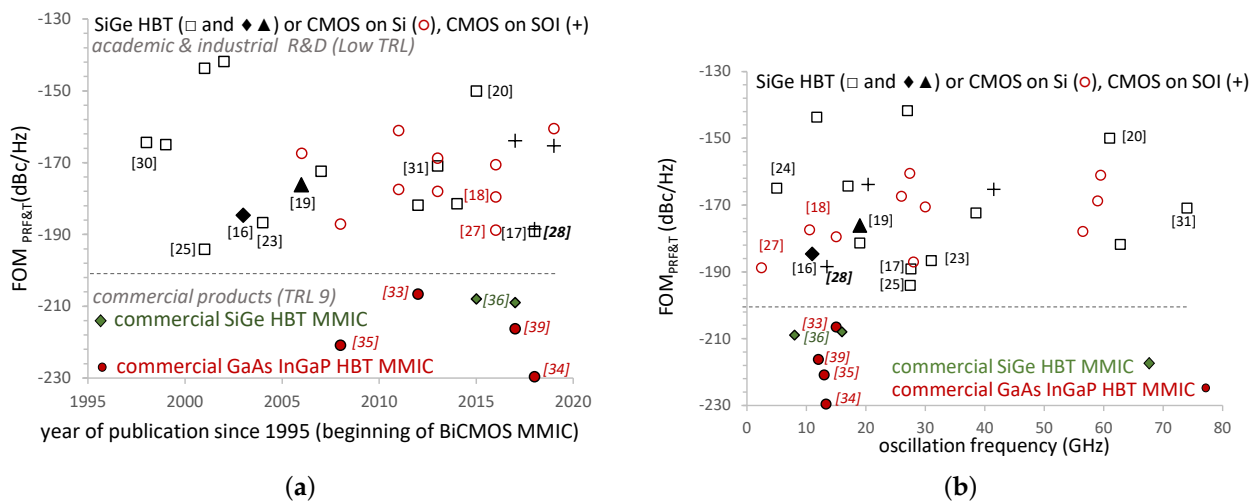
Figure 11. Evolution of the $\text{FoM}_{P_{RF}\&T}$ metric (Equation (4)) (**a**) with the year of publication (**b**) versus the oscillation frequency. Some references used in the paper are noted close to the associated symbol [16–40].

2.2. Direct Digital (Frequency) Synthesis (DDFS or DDS)

For programmable frequency generation above gigahertz, PLLs have long been the only usable technique. Despite DDFS being known since the 1970s [44] and actively developed since the 1980s, it has been mostly used to generate arbitrary waveforms (AWG) at low frequencies (<1 GHz). Indeed, in its initial form, the DDS is made with a phase accumulator (Pacc), a phase-to-amplitude converter (PAC) implemented with a memory (RAM or ROM), a digital-to-analog converter (DAC), and takes a frequency control word FCW at the input to control the output frequency, as shown in Figure 12. The fundamental equation of the DDFS calculates the output frequency f_{out}, from a fixed clock frequency f_{clk}, the number of bits n of the Pacc, and the FCW:

$$f_{\text{out}} = \frac{f_{\text{clk}}}{2^n} \text{FCW} \tag{6}$$
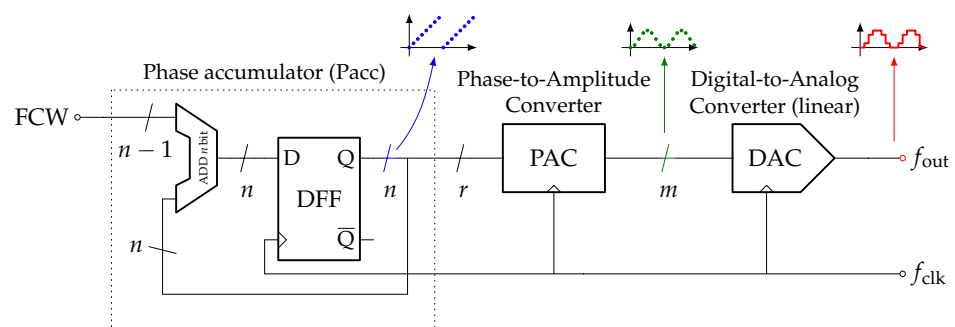
Figure 12. DDFS basic structure (DFF: D-flip-flop).

The ROM/RAM PAC allows storing samples from any waveform, providing the AWG behavior of the DDFS, but at the same time is the design bottleneck of the whole DDFS: high area, high consumption, frequency limitation. Moreover, when a PLL generates output frequencies from a lower-frequency reference (a few tens or hundreds of megahertz), the DDFS generates output frequencies from a higher-frequency reference (f_{clk}) and is limited by the Nyquist–Shannon theorem. For example, for an identical 10 GHz synthesized output frequency, only some subcomponents are needed to work at 10 GHz in the PLL (VCO and frequency divider) while the others work at lower frequencies (phase/frequency detector, charge pump and filter), whereas all the DDFS components are needed to work at least

at 25 GHz to satisfy the Nyquist–Shannon theorem. Then, DDFS are less suited than PLL when generating high frequencies. Regardless, some DDFSs have been shown to work up to 32 GHz but in InP DHBT technologies and with a very high power consumption of 9.45 W [45].

Nevertheless, the DDFS features many advantages over PLL that make them advantageous at high frequencies, such as fast frequency switching, subhertz resolution, or intrinsic fractional frequency behavior. With (Bi)CMOS technologies working at even higher frequencies over the years, various evolutions of the basic structure have appeared to reach a reasonable power consumption without losing much performance at high frequencies. Considering the bottleneck of the DDS, the PAC as a RAM or ROM, many compression techniques have been utilized to reduce the size of these memories and overcome some of their limitations regarding frequency and consumption. The easiest one is to take only the most significant *r* bit out of the total *n* bit of the Pacc: these *r* bit phase have less precision than the internal Pacc *n* bit phase and, when converted to a signal amplitude, create further spectrum noise/spurious contributions to the quantification noise of the output DAC. Keeping *n* bit in the Pacc ensure maximum precision on the phase (important for having subhertz resolution). As well, other PAC families allowing RAM/ROM replacement have also been studied in the literature, such as algorithms which calculate the next sample step by step. However, they do not solve the frequency limitation problems: they cannot run at a sufficiently high frequency nor under low consumption. A comprehensive review of all these techniques around the classical DDFS (i.e., with a digital PAC) can be found in [46]: angular decomposition, angular rotation based methods, sine amplitude compression, and polynomial approximations.

2.2.1. Radio Frequency DDFSs

When increasing the clock signal f_{clk}, all PAC in the pure digital domain start consuming excessive power or simply cannot run, mainly because reading the samples or calculating them is too slow. Therefore, it is necessary to remove the PAC module out of the purely digital world and replace it somewhere else to allow high-frequency operation (>1 GHz) together with a moderate consumption (<1 W).

In this paper, we focus on such RF-aware DDFS (RF-DDFS) techniques under a moderate consumption, which are most of the time qualified as "ROM-less" in reference to the initial basic structure where the PAC is a power-hungry ROM in the digital part: "Digital-PAC-less" should be more appropriate, because all PAC in the digital domain whatever their implementation (memory or hardware calculation logic) are generally both frequency limited and power-hungry, with only a few exceptions.

After removing the digital PAC, giving the waveform its final shape requires an adequate nonlinearity somewhere else, in the DAC or after, so that the reshaping is, at least for a part, in the analog world. The digital ramp at the Pacc output is then simply decoded by an EXOR between $(n-1)$ bits and the MSB so that the DAC receives a digital triangle waveform at its input. In this case, we can write that the number of bits at the output of the Pacc is equal to the number of bits at the input of the DAC ($m = r$). Two major techniques are then used to implement the nonlinearity:

1. Inside the DAC which becomes nonlinear (NL-DAC) and shapes the output waveform at the same time it converts it to analog (Figure 13);
2. After the DAC which remains linear and outputs an analog triangle waveform to a final analog stage which reshapes it in the analog world. We call it an analog sine PAC (AS-PAC) (Figure 14).

All these RF-DDFSs come with a drawback: by removing either the storing in a memory or the digital calculation of the waveform samples (i.e., removing the PAC, whatever its technique from the digital part), the RF-DDFS is no longer able to generate arbitrary waveforms anymore. It generates only a few waveforms, particularly the most needed one, the sine. At the extreme, by keeping only the most significant bit (MSB) from the Pacc, a simple squared waveform at frequency $\frac{f_{\mathrm{clk}}}{2^{n-1}}$ FCW can be obtained: the *m* bit DAC is

no longer required and can be replaced by a simple output buffer: it is the "pulse output DDFS"). The MSB is not the only bit of phase that can be used in such a way: it is possible to use any of them, with a doubling of the frequency each time you decrease the weight of the retained bit by one.
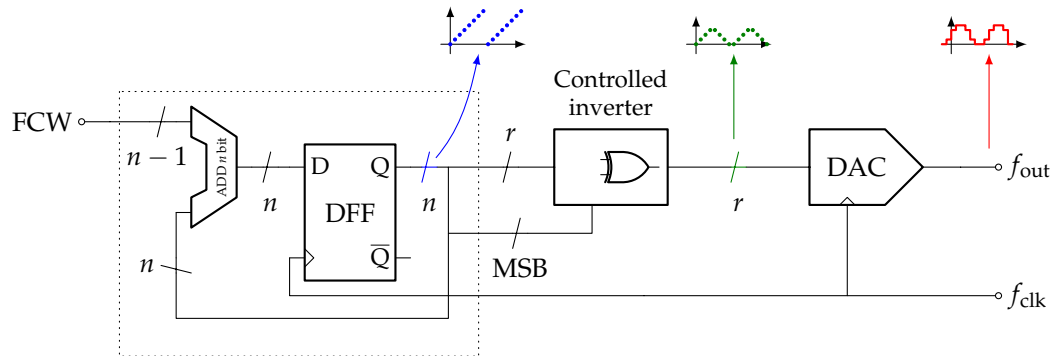
Figure 13. RF-DDFS with a nonlinear DAC (NL-DAC).
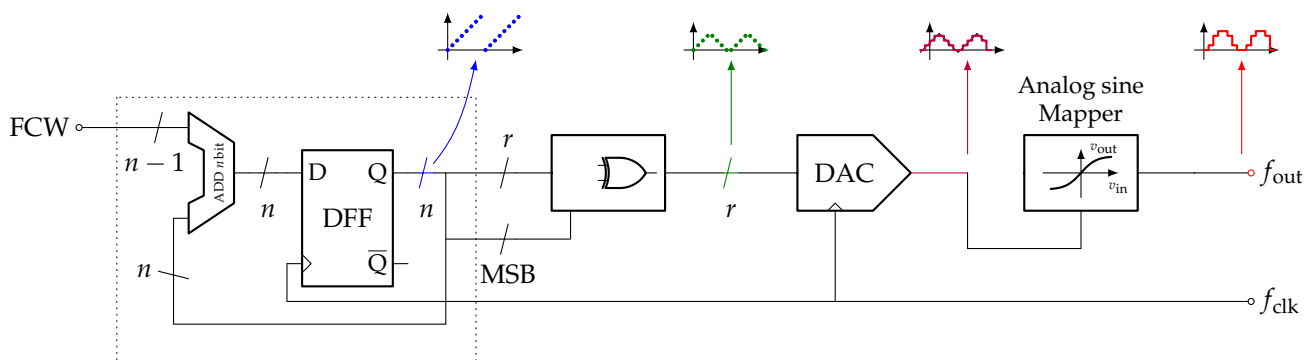
Figure 14. RF-DDFS with an analog sine mapping.

In this paper, we focus our attention on silicon technologies (CMOS and BiCMOS SiGe), but we also add GaAs and InP realizations we have found in the literature when it does not impact too much the scale of the graphs. Not much fully characterized RF-DDFSs have been published over the years as shown in Figure 15, for CMOS, SiGe, InP, and GaAs technologies.
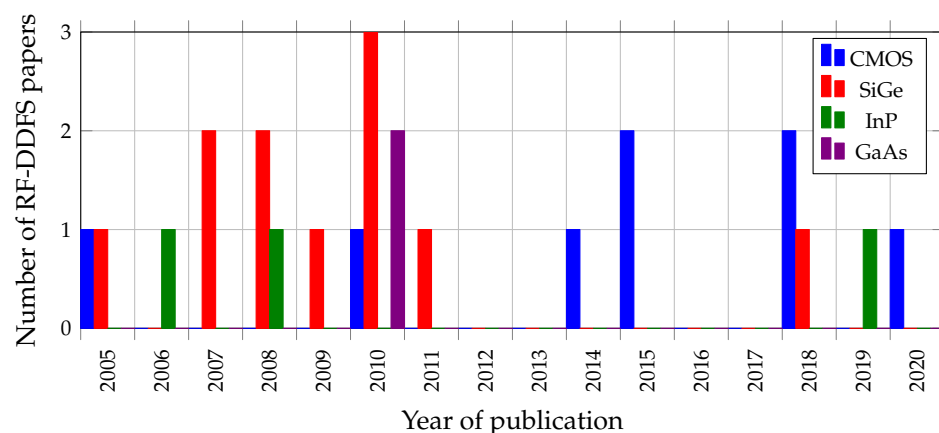
Figure 15. Number of fully characterized published RF-DDFS versus year of publication.

Only published RF-DDFS with measurements at a f_{clk} greater than 1 GHz were considered in this paper. In particular, DDFS "chip-set" exhibiting high output frequencies greater than 1 GHz thanks to an analog internal up-conversion stage are not considered (if $f_{clk} < 1$ GHz) as in [47]. All published standalone functions of DDFS (Pacc, PAC or DAC), even when claimed to be relevant to DDFS were also pushed aside at the profit of fully functional DDFSs. We also kept only the final journal reference for DDFSs published multiples times in conferences first. We found a total of 24 references.

RF-DDFSs of the first previously mentioned technique (with NL-DAC) were proposed, to the author's knowledge, by [48]. It was introduced to lower the consumption, with still a constraint in the clock frequency up to only 230 MHz. A number of other successful implementations have come after [49–63]. Figure 16 shows the maximum clock frequency versus consumption for different RF-DDFSs based on NL-DAC topologies for SiGe and GaAs technologies. CMOS RF-DDFSs are plotted as well, whatever their technique. We can also cite two other RF-DDFS in InP technology: [64] for a DDFS of the same nonlinear DAC type at 24 GHz under 19.8 W and [45] for a DDFS of the initial topology (ROM-PAC) at 32 GHz under 9.45 W. Because of both their high frequency of operation and high consumption, they are not included in the graphs to keep full scale for all other references. CMOS technologies are clearly not suited for high-frequency operations compared to other technologies but obtain an honorable frequency of operation of 3.5 GHz in [65] with a quite low consumption of 601 mW. It is to be noted that this reference surprisingly still uses a digital PAC, created by an automated logic synthesizer software. This 3.5 GHz can be compared to the frequency at which today's most microprocessors are running. Unfortunately, microprocessors maximum frequency have been almost stuck for many years now, and CMOS RF-DDFS based on synthesized logic will probably follow this tendency and will not be able to significantly increase their frequency of operation soon. Reference [66] is also a CMOS RF-DDFS working at 2.5 GHz, based on an optimized hardware implementation of the CORDIC algorithm.

Reference [67] is another example of an RF-DDFS still based on a digital PAC, working over 1 GHz, at 1.7 GHz, in a 0.35 µm SiGe technology. Its PAC, while digital is all the same simplified to convert to sine-only waveform, and the power dissipation is high as expected for a digital PAC (even simplified), at 3 W.

The second method to design RF-DDFSs (based on AS-PAC) has been proposed by McEwan et al. in [68] through behavioral simulations. The initial purpose was also to lower the consumption. The first successful measured implementation of an AS-PAC on a BiCMOS SiGe:C 0.25 µm technology was first conducted by Thuries et al. (author's papers) in [69] for the standalone AS-PAC, and [70] for a full DDFS at 6 GHz. Between the two, McEwan et al. also published a complete DDFS in CMOS 0.35 µm but with a very limited frequency of 10 MHz [71]. After that, many other contributors implemented the same idea in more recent SiGe technologies [72–75] and obtained both high-frequency and moderate consumption DDFS. Figure 16 also shows RF-DDFSs with an AS-PAC (only SiGe at these frequencies). It is clear that this second family (AS-PAC) gives better performances in terms of both the maximum frequency and the consumption than the first (NL-DAC).
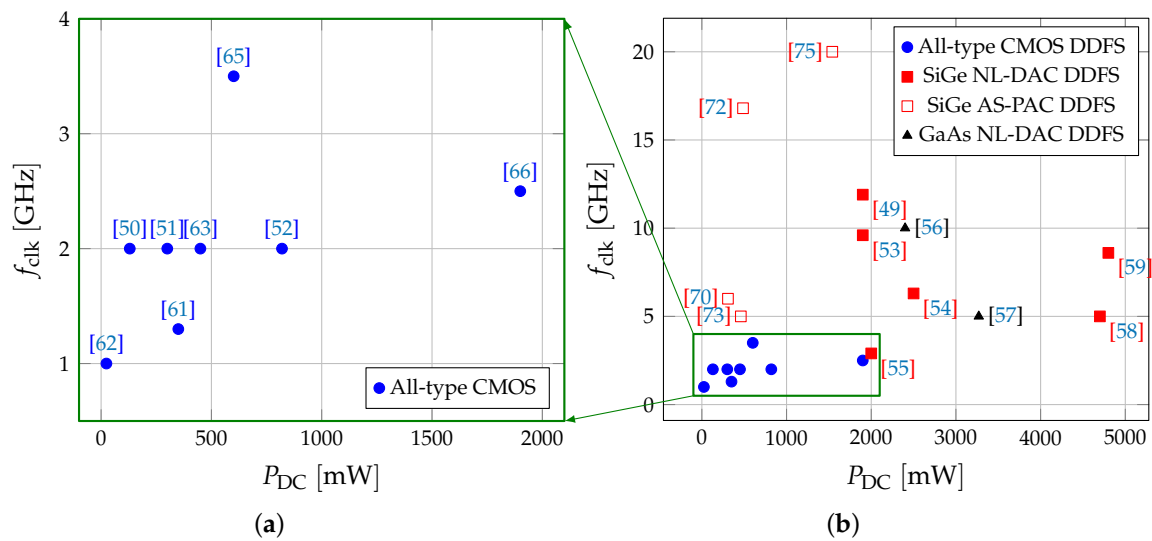
Figure 16. f_{clk} versus consumption P_{DC} for DDFSs in (**a**) All-type CMOS (full scale) and (**b**) All-type CMOS, an NL-DAC or AS-PAC SiGe and GaAs technologies [49–59,61–63,65,66,70,72,73,75].

2.2.2. DDFS Figures of Merit

The f_{clk} and P_{DC} cannot be the only important parameters in a DDFS. To make the comparison meaningful, the technological node, the spurious free dynamic range (SFDR which define the power ratio of the fundamental signal to the strongest spurious signal in the output), the phase noise, the output power, the sizes of the accumulator (*n*) and the DAC (*m*), and the topologies (NL-DAC or AS-PAC), the frequency control word (FCW) at which measurements are conducted should also been considered. Unfortunately, all these parameters are not always given in published papers (such as output power, phase noise, integration area of the core, and not the whole chip with PADs).

As previously introduced, FoMs are largely employed to make more or less fair comparisons between the designed circuits. In the case of DDFS, there are a few FoMs in the literature. The first one is the most widely used and considers only $f_{clk_{max}}$ and P_{DC} as we have shown in Section 2.2.1 until now:

$$\text{FoM}_1 = \frac{f_{clk_{max}}[\text{GHz}]}{P_{DC}[\text{mW}]} \tag{7}$$

It gives the best score to DDFS which work at the highest frequency with the lowest consumption, no matter what the other parameters are, which is not very fair.

A second one, found in [56], which is less used, is:

$$\text{FoM}_2 = \frac{f_{clk_{max}}[\text{Hz}]}{f_t[\text{Hz}]} \times 100\,\% \tag{8}$$

and is all about frequencies (f_t is the cut-off frequency of the employed devices) which is no more informative, even less than FoM$_1$ of Equation (7). Actually, it can be given in parallel to FoM$_1$, but giving multiple FoMs for the same function is against the all-in-one philosophy of FoM, and the real initial parameters should be preferred to multiple FoMs.

The spectral purity is one the main drawbacks of the DDFS, because it generates periodic waveforms on the basis of *n* bit integer counting in the Pacc, with overflows, resulting in a mathematical period generally different to the wanted (apparent) one: it is the case each time 2^n is not exactly divided by FCW.

For example, with $2^n = 8$ and FCW= 3, the counting on each period of the clock (T_{clk}) is 0, 3, 6, 1, 4, 7, 2, 5, back to 0 with two overflows. The apparent period is $\frac{8\,T_{clk}}{3}$ but the true (mathematical) period is $8\,T_{clk}$. The fundamental frequency at the output is then $\frac{f_{clk}}{8}$, and

the main apparent output frequency is only its third harmonic: all other harmonics are also there and more or less pollute the whole spectrum, with a strong dependency to FCW.

More generally, the apparent output frequency is given by Equation (6), but the true fundamental frequency is:

$$f_{\text{out}_{\text{fund}}} = \frac{f_{\text{clk}}}{2^n} \, \text{GCD}(2^n, \text{FCW}) \tag{9}$$

with GCD the greatest common divisor, and the apparent f_{out} is its $\left\lceil \frac{\text{FCW}}{\text{GCD}(2^n, \text{FCW})} \right\rceil^{\text{th}}$ harmonic.

To these unavoidable spurious from the Pacc counting with 2^n values, one should add those due to the truncation of bits at the output of the Pacc [76]. Indeed, in an RF-DDFS, the DAC input keeps only the r most significant bits from the n (after the controlled inverter of Figure 13 or 14). These spurious are also added to the quantization noise of the DAC. This signal-to-noise ratio (SNR), in the case of a sine that we want to generate, is linked to the DAC resolution r by the well-known equation:

$$\text{SNR [dB]} = 6.02 \, r + 1.76 \tag{10}$$

Taking the spurious into account is performed through the SFDR and can be given in a narrow band (Nyquist-Shannon band) or in the whole spectrum. Keeping the band narrow ensures the exclusion of frequency replica around each multiple of the clock frequency, which is a legitimate behavior shared by all sampled waveforms.

The following other FoMs have been found in publications [56,59,65,73,77]:

$$\text{FoM}_3 = \frac{f_{\text{clk}_{\text{max}}}[\text{GHz}] \cdot n[\text{bit}] \cdot \text{SFDR}[\text{dBc}]}{P_{\text{DC}}[\text{W}]} \tag{11}$$

$$\text{FoM}_4 = \frac{f_{\text{clk}_{\text{max}}}[\text{GHz}] \cdot n[\text{bit}] \cdot r[\text{bit}] \cdot \text{SFDR}[\text{dBc}]}{P_{\text{DC}}[\text{W}] \cdot f_t[\text{GHz}]} \tag{12}$$

$$\text{FoM}_5 = \frac{f_{\text{clk}_{\text{max}}}[\text{GHz}] \cdot n[\text{bit}] \cdot r[\text{bit}] \cdot \text{SFDR}[\text{dBc}]}{P_{\text{DC}}[\text{W}] \cdot \text{Area}_{\text{norm}}} \tag{13}$$

$$\text{FoM}_6 = \frac{2^{\frac{\text{SFDR[dBc]}}{6}} \cdot f_{\text{clk}_{\text{max}}}[\text{GHz}]}{P_{\text{DC}}[\text{W}]} \tag{14}$$

A good FoM for a complex circuit such as the DDFS is not simple, because the Pacc, the DAC, and the PAC do not behave identically regarding power consumption, frequency of operation, and number of bits and do not contribute to the final SFDR the same way. We choose here the following definition, inspired by the previous ones in Equations (7), (13), and (14):

$$\text{FoM} = \frac{f_{\text{clk}_{\text{max}}}[\text{GHz}] \cdot n[\text{bit}] \cdot r[\text{bit}] \cdot 2^{\frac{\text{SFDR[dBc]}}{6}}}{P_{\text{DC}}[\text{W}] \cdot \text{Area}_{\text{norm}}} \tag{15}$$

with the following justifications:

- The size n of the Pacc is used to weight the consumption: by doubling the number of bits n in the accumulator, its consumption is also roughly doubling, as well as its area.
- The size r of the DAC, in addition to being tied to its SNR as seen before (Equation (10)), is also tied to its consumption: as a power of two for the static part, and proportionally for the dynamic part [78], as well as its area.
- In an RF-DDFS with mainly a Pacc and a DAC, doubling the number of bits in the Pacc as well as in the DAC should roughly double the area and double the dynamic power, such that the area and dynamic power are both proportional to $\sqrt{n\,r}$ and their product to $n\,r$.
- Comparing the integration area is important, but preferably in a "normalized" way which is defined as the area divided by the technological node squared [79]. For example, switching from a 0.35 µm to a 0.25 µm technology gives a potential reduction

of the integration area equal to $1 - \frac{0.25}{0.35} = 28.6\,\%$. This shrinking coefficient is often more exact for CMOS devices than for their bipolar counterpart but still goes in the right way inside an FoM. Publications which give only the full area with no information on the core area are a bit penalized.

- The transition frequency f_t is not always given in the publications; therefore, while being a parameter of interest, we do not use it.
- The FCW word is also of importance, because if it perfectly divides (null remainder) 2^n (e.g., for 8 bit: $2^8 = 256$), the output period is exactly the fundamental period, and the corresponding spurious disappear. However, of course, this is one of all the n (e.g., 8) best cases for FCW: with all the other $2^n - n$ (e.g., 248) integer values of FCW, the remainder is again different from zero, and the spurious are there again. The FoM should reflect those numerous $(2^n - n)$ FCW worst cases that occur during real running conditions and not the few n best ones. Unfortunately, this information is not always given and is not taken into account.

The main problem with an FoM is that it completely hides the range value of each parameter. By looking at Figure 17 which shows the evolution of the chosen FoM with the year and month of publication through all technologies, it is clear that CMOS RF-DDFSs are the most interesting from a pure FoM point of view. However, it should not hide that the CMOS technologies are far behind the others one from the frequency of operation point of view. Moreover, they use CMOS transistors for which the integration area is optimized, as well as the ease with which designers can increase the value of n, often with the automized help of CAD sofwares such as in [65]. As a consequence, the smaller $f_{\text{clk}_{\max}}$ is largely compensated in the FoM by the n and the Area$_{\text{norm}}$.

For these reasons, while keeping the curve on the same graph, we should avoid an "FoM-only" comparison between CMOS RF-DDFSs FoM (in blue) with RF-DDFSs from the others technologies. Giving the $f_{\text{clk}_{\max}}$ a greater proportion than the Area$_{\text{norm}}$ and/or n in Equation (15) could also help.
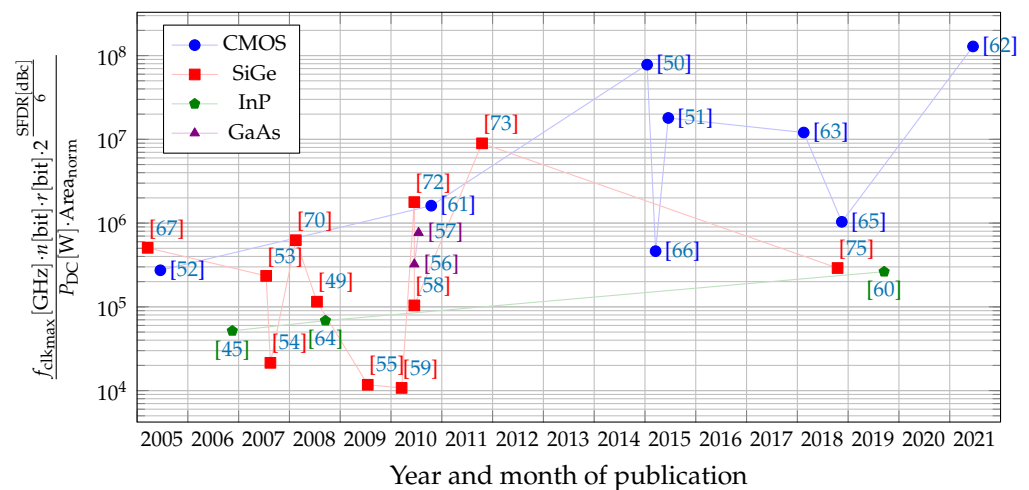
Figure 17. Retained FoM (Equation (15)) versus year and month of publication [45,49–67,70,72,73,75].

CMOS are the main technologies used for the last published DDFSs with the highest available FoMs. Unfortunately, at the same time, they are still now far behind regarding the $f_{\text{clk}_{\max}}$ (Figure 16). Previously, SiGe technologies have shown the best results for designing RF-DDFSs since 2005, but have been less used in the last decade. Nevertheless, they keep undeniable advantages on all performances while sharing with pure CMOS technologies the CAD approach on their CMOS components, which should help in designing some critical digital parts (such as optimized Pacc with parallel/pipelined approaches). Moreover, they offer access to high-performance HBT transistors to make RF-aware topologies such as AS-PAC able to work at very high frequency together with offering better SFDR performances.

3. Mixers

The mixer performs frequency translation by multiplying baseband, IF or RF signal with LO as illustrated in Figure 1 in receiving configuration. As the ideal multiplication operator is difficult to achieve in practice, a nonlinearity or a switch driven by LO signal is employed to bring it out. From the point of view of the RF-IF signal path, the circuit should be as linear as possible to avoid corrupting the frequency-translated information. Hence, a mixer is characterized by a conversion gain and by a noise figure (NF) at a given LO power or voltage. Its level of linearity is evaluated through input/output 1 dB compression point (I/OCP) and 3rd order input/output intercept point (I/OIP3). Because switching or driving nonlinearity adds a lot of undesired tones at circuit ends, balanced architectures are preferred, when possible, to clean up the signals and improve port-to-port isolation.

During the 1990s, when this survey starts, the only silicon-based mixers exceeding 10 GHz employ SiGe transistors [80,81]. Bipolar mixers remain under 5 GHz [82] while CMOS ones catch up to GHz [83,84]. The original vertical Gilbert cell is employed to demonstrate BJT and SiGe HBT frequency capabilities, while CMOS counterparts are integrated in current switching passive or sampling mixers. In what follows, the discussion focuses on the evolution over time of the comparative performances of the two families of mixers that are the Gilbert cell and its derivatives, as well as the passive mixers, which also incorporates several variants (voltage or current conveyors and sampling mixers). Unlike the previous circuits, the use of FoM is not very widespread in the case of mixers. Indeed, the complexity of the circuit makes it more difficult to characterize, and all the necessary information is not always available to compare the solutions with respect to each other.

Figures 18 and 19 plot publication timeline regarding technological nodes, circuits architectures, and active devices, as well as RF operating frequencies. The most significant references featuring RF frequencies mainly comprised between 10 and 100 GHz have been selected from the literature, i.e., those which introduce new ideas, report state-of-the-art performances, and provide sufficient detail to allow meaningful comparisons with other works.

Figure 18. Mixers technological trends: technological node versus year of publication [81–110].

These figures show to what extent applications are driving technological developments with local multipoint distribution service (LMDS) or multipoint video distribution system (MVDS) between 10 and 40 GHz in the 2000s, then the 24 GHz band initially planned for automotive radar systems until 2010 before moving to the 77 GHz band, high-data rate wireless communications (WPAN and outdoor point-to-point links) operating at 60 GHz from 2007, and more recently the 24–40 GHz and even higher bands targeting 5G. Unsurprisingly, SiGe BiCMOS technologies drove the trend until process size reduction

allowed CMOS devices to compete with SiGe, at least in frequency, starting in the mid-2000s. CMOS technologies have gradually established themselves at all frequencies up to 100 GHz. The performance offered is sufficient for the majority of applications. However, SiGe remains relevant in some applications, i.e., when high output power is required, such as in up-converters targeting mm-wave 5G transmitters [85–87].
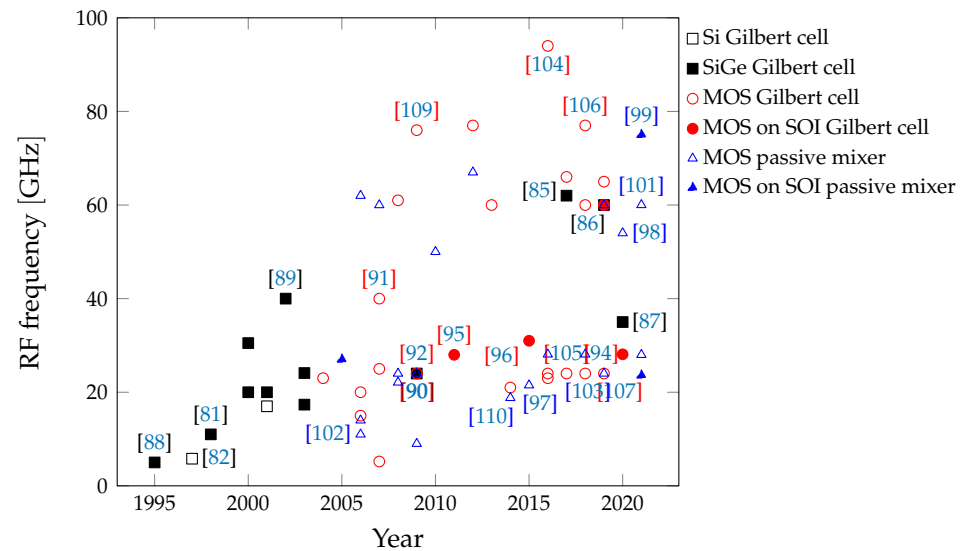
**Figure 19.** Mixers technological trends: technological node versus RF operating frequency [81–110].

Regarding linearity, passive mixers are also well known for their excellent behavior which brings some welcome degrees of freedom in the design of LNA-mixer front-ends. Their conversion losses allow IIP3 and ICP to reach much higher values than with Gilbert mixers. However, to compare the true potential of one or the other of these solutions, output-referenced data are more relevant as they do not depend on conversion gain. OCP is chosen as an indicator of linearity in the following discussion as too few papers present linearity in terms of IP3. The next figure reports OCP of various mixers plotted against technological node (Figure 20a) and frequency (Figure 20b). Only mixers without output amplifier are considered to avoid unfair comparisons or mixers employing unity-gain buffer, assuming that the latter does not influence mixer's OCP.

The best OCPs are achieved by Gilbert mixers and particularly SiGe-based ones [86,88,89]. High-voltage supplies allow SiGe mixers to deliver more output power than CMOS. They also outperform CMOS mixers in most performance metrics thanks to the better high-frequency gain and the lower noise of the HBT but at the cost of increased power consumption [90]. For CMOS Gilbert mixers, there is more to say. The Gilbert Mixer is an all-in-one vertically integrated circuit embedding mixing switches inside an amplifier, allowing the circuit to provide conversion gain. Two factors restrict its linearity: the transconductance amplifier saturation when input voltage exceeds a few U_T, and the output voltage swing limitation due to voltage headroom of tail current, differential amplifier and mixing stages. When CMOS versions do not deviate much from Gilbert's original design, OCP values seem to stay well behind SiGe [87,88]. However, improvements allowing CMOS to come closer to SiGe are possible by combining several linearization techniques. Among them, the current bleeding technique helps in reducing the current flowing through the mixing quad and load resistors [91]. References [92,93] use this technique and replace the original input differential amplifier by more linear single-ended (SE) amplifiers. Folded architecture is also used to allow separate tuning of bias currents and to increase output voltage swing [94]. Another approach called multiple gated transistor adds transistors around the main transconductance amplifier to cancel out IM3 tones [95,96].

Figure 20b shows no clear trend of OCPs as a function of frequency or technological node. Except for some low values resulting from an assumed trade-off in a very low

power context [97,98], passive mixers appear to offer comparable OCPs to Gilbert mixers when one would have thought to see them above. However, the best achievements do not necessarily appear in this survey. Virtually all of the standalone passive mixers shown are pumped by an external RF source that delivers a sinusoidal signal, which clearly does not optimize linearity. Moreover, passive mixers are more often embedded in much larger works with the recent technological nodes [99,100]. A passive mixer comes in different forms depending on whether a power, voltage, or current transfer is desired. Standalone passive mixers designed to reach low impedance matching (typ. 50 Ω) provide most of the available data, but they may not reach the best linearity due to large mixing devices v_{DS} swing. Voltage and current switching mixers (i.e., driven by an LO square voltage) intend to solve this problem but are typically integrated into front-ends that provide the required set of impedances to the RF and IF ends of the mixer as well as a square voltage to the LO end. It is then difficult to retrieve the performance of the mixer alone [99–101]. However, the best OCPs shown in Figure 20 among passive mixers (−2 and −3 dBm) are attributed to two voltage passive mixers [102,103] loaded by high input impedance unity-gain source followers.

The LO power (P_{LO}) driving different classes of mixers is plotted in Figure 21 against technological node, and it tends to decrease with channel length shrinking and frequency (not shown). Circuits with LO buffer have been excluded from these plots. Half of the remaining papers include a passive balun on the LO access which generates an average increase of 0.5 dB on P_{LO}. The larger LO drive usually required for passive mixers compared to Gilbert mixers does not stand out clearly. However, it becomes a bit more obvious in Figure 22 when OCP is plotted versus P_{LO}. If we exclude the ultra low power mixers from [97,98], the excess power required by a passive mixer is 5–10 dB more than Gilbert mixers for comparable OCPs. This difference, visible for technological nodes larger than 0.13 µm in Figure 21, vanishes with the latest CMOS technologies where lower gate-source voltage and therefore lower P_{LO} is needed to reach similar r_{ON}. On these nodes, P_{LO} ranges become similar for passive and Gilbert mixers for OCPs around 0 dBm [103].

(a)

(b)
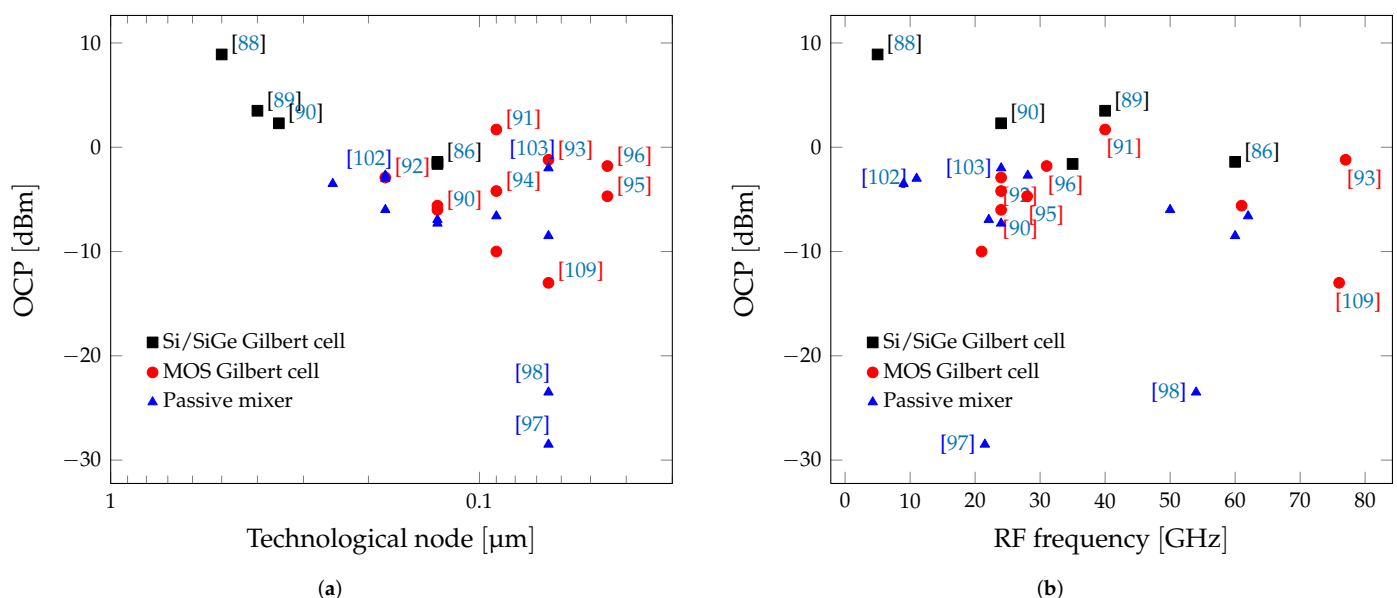
Figure 20. OCP of Gilbert and passive mixers including their respective derivative any technology combined: (**a**) OCP versus technological node and (**b**) OCP versus RF operating frequency.

Figure 21. P_{LO} plotted versus technological node for Gilbert and passive mixers.

Figure 22. OCP versus P_{LO}.

The LO feedthrough is another widely shared data, allowing comparison of LO-to-RF isolation between mixers. Published data in the 10–140 GHz range are reported in Figure 23. Single-balanced (SB) papers are separated from double-balanced (DB) ones and from Gilbert cell derivatives using special feedthrough reduction techniques [104–107]. Such techniques often involve inductors to resonate with parasitic capacitors at mixing pairs common nodes. They also tend to improve noise and linearity but at the expense of a reduced bandwidth. Apart from these particular circuits, no noticeable difference exists between passive and active mixers. Taking care of the layout symmetry is enough to lead to LO-to-RF isolation in the 30–40 dB range. Passive SB mixers [108] can also bring isolation levels on the same order as their DB counterparts [102,103], which can lead to interesting design simplifications in some specific cases, e.g., in I/Q direct conversion receivers.
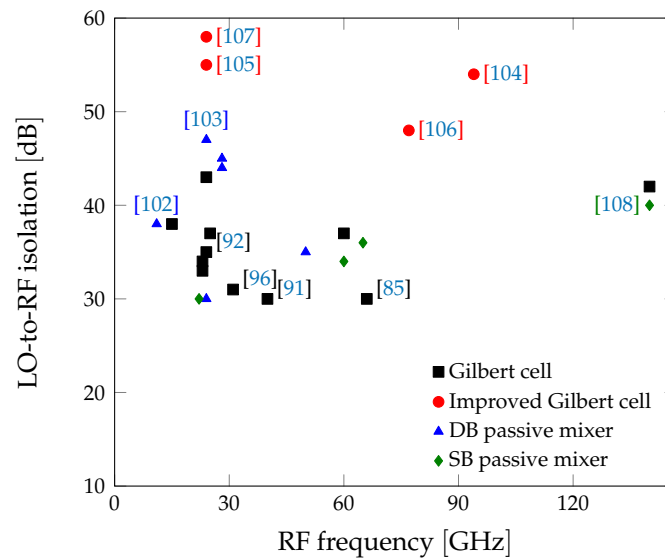
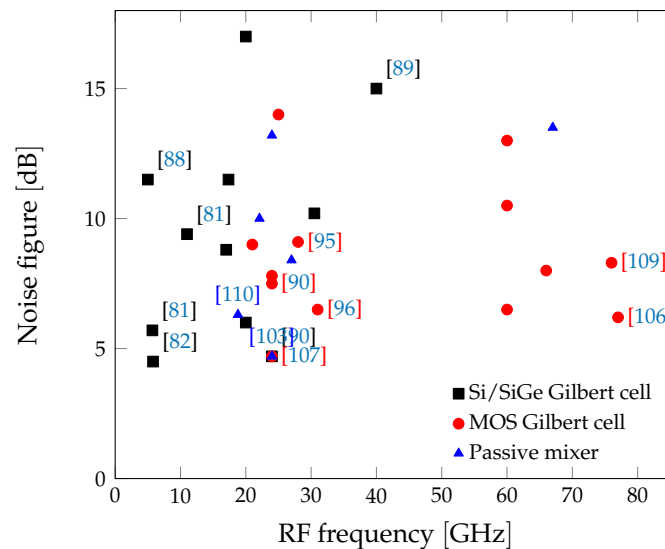**Figure 23.** LO-to-RF isolation versus frequency.

Figure 24. Double-sideband (DSB) NF plotted versus frequency for main type of mixers.

The DSB noise figure (NF) is shown in Figure 24 versus frequency. As might be expected, Gilbert mixers and their variants are more suited to provide low NF than power-matched passive mixers, knowing that conversion losses convert into noise. A better noise performance is however possible using voltage or current switching mixer when LO voltage duty cycle is lower than 50% to reduce conversion losses. This approach, widely used for applications located in the low end of the RF spectrum [111–113], is reaching millimeter-wave frequencies [103,110]. In [110] (author's paper), an NF of 6.3 dB is obtained at 19 GHz by a voltage sampling mixer. This result contains the noise contributions of switching devices but also of the baseband amplifier, including baseband amplifier contribution.

4. Discussion and Conclusions

From the previous sections, a large review is proposed for the frequency synthesis of RF signal and frequency conversion. For each of these functions, FoMs or main electrical parameters were presented and discussed to fairly compare the designs over the last two decades (i.e., from the first RF circuit designs). Concerning the RF signal generation, first, it can be noticed that the frequency synthesis based on the VCO (embedded in the final PLL)

and on the DDFS appear to be definitively complementary and not really in competition with each other. Their main advantages do not really conflict with each other, and high frequency is achieved with RF VCOs while a high level of integration (small area) and reconfigurability is to the advantage of DDFS. Then, the initial choice strongly depends on the targeted first order constraint.

For its part, DDFS provides wide frequency range but only up to a few GHz above 10 GHz when using SiGe technologies, these former ones gaining access to higher-frequency ranges (with f_t and $f_{\max}$ of the latest technologies close to the THz!). On their side, DDFS based on CMOS are frequency limited, even when considering smaller CMOS nodes as the transition frequency f_t collapses for gate length below 28 nm [114]. As a consequence of the frequency limitation, the HF circuit performance scaling with technological node also peaks at 28 nm for VCOs phase noise, as evoked in [115]. Another strong advantage of the DDFS structure is that it enables simple and direct frequency/phase/amplitude modulations without the use of any mixer needed in an analog structure (PLL+mixer). Then, the architecture of a digital structure is, in theory, more flexible and reconfigurable.

By presenting itself as the only possible alternative for the synthesis of a sine-type signal at very high frequency (the silicon DDFS remaining below 20 GHz at the time of publication), the VCO results from a set of compromises. From all the presented VCO structures, it is evidenced that the lowest phase noise does not necessarily coincide with the best FoM as one might legitimately believe when it comes to frequency synthesis at high spectral purity. Achieving a large tuning range of high purity VCO is at the expense of multiple VCOs high Q-factor design (and then larger dice area). Other different parameters are weighted in these FoM, one of them concerning the dynamic power that is used to feed the mixer LO access.

Thus, the mixer design is closely bound to the PLL (VCO outputs), and the collective design of the VCO with the mixer should be considered as early as possible in the design process. First, because several phases (typ. 0°, 90°, 180°, and 270°) of the same signal are required for the proper operation of the receiver's frequency translation and image rejection and because differential LO signals help to reject LO residuals on the RF and IF ports. Secondly, the LO voltage waveform must be tailored to the chosen mixer topology to optimize its performance. A square signal with sharp transitions is for example desirable, mainly to avoid noise issues in Gilbert mixers and linearity issues in passive mixers. As this approach is hardly applicable to millimeter-wave frequencies, one solution to reduce the switching transition times is by increasing the amplitude of a nearly sinusoidal LO signal. However, in the case of a CMOS Gilbert mixer, LO voltage amplitude must remain sufficiently low to prevent the mixing transistors from entering the triode region and thus degrading the linearity. For switching passive mixers, a rail-to-rail voltage swing optimizes the conversion losses and noise figure. Very recently, a nearly square wave signal of $1.2V_{\text{p-p}}$ has been demonstrated up to 35 GHz by cascading several fast inverters in [100] and using a 28 nm CMOS node. As a low duty cycle LO waveform is too difficult to achieve at these frequencies, it is possible to mimic a low duty cycle switch by using a cascade of two MOS switches driven by two time-shifted square wave signals. This approach has been successfully implemented by the authors at 26 GHz using a 28 nm FD-SOI CMOS process to build a subharmonic sampling mixer operating at an RF frequency of 77 GHz [116].

At last, it is obvious that silicon technologies offer a variety of unparalleled functions and performances, with a very strong potential for integrating analog and digital functions. Many investigations are still going on to improve both the technology and the circuit topology. A decade before, the use or FBAR opened the way to very low phase noise at fixed frequencies [117,118], and it could be considered as an efficient alternative to low Q-factor 2D inductors to design VCOs if associated with high Q-factor varactor. Beyond the functions mentioned in this article, we can also evoke the derivative functions used in chips dedicated to active antennas (AESA) for telecommunications and Radar, such as multifunction chips (corechip) [119], and many are the fully integrated TxRx realizations which demonstrate the potential of these technologies [10]. The applications are numer-

ous for low-cost applications markets such as automotive, industrial, or consumer IoT, 5G [120,121] or Radar applications [122,123]. The strength of silicon-based technologies is that they meet the coexisting design parameters concerning the electrical performances, the miniaturization and the cost of a technological process which are essential for large market production as well as highly integrated modules dedicated to high-frequency applications (bricks and tiles for RF modules). However, it should be noted that the increase in frequency (reduction in size) is obtained at the expense of the cost of the chip linked to the complexity of the technological process.

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