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A Calibration-Free, 16-Channel, 50-MS/s, 14-Bit, Pipelined-SAR ADC with Reference/Op-Amp Sharing and Optimized Stage Resolution Distribution

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Abstract: This paper presents a calibration-free, 16-channel, 14-bit, 50-MS/s, pipelined successive approximation register (pipelined-SAR) analog-to-digital converter (ADC) for ultrasound imaging systems. A reference sharing scheme with reduced buffers is proposed to improve area-and-power efficiency, which is essential for multi-channel systems. Based on this, a three-stage, pipelined-SAR ADC architecture with reference/op-amp sharing and optimized stage resolution distribution is proposed. The prototype ADC is designed in a 0.18-µm process with peripheral circuits integrated, including low-voltage differential signaling (LVDS), bandgap, etc. It achieves a robust and calibration-free performance with 68.25-dB signal to noise and distortion ratio (SNDR) and 82.19-dB spurious-free dynamic range (SFDR), translating into a competitive figure of merit (FoM) of 0.47 pJ/conversion-step among other high-resolution ADCs used in ultrasound applications.

Keywords: ultrasound imaging system; ADC; pipelined-SAR; reference sharing; op-amp sharing; stage resolution distribution

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1. Introduction

1.1. Ultrasound Imaging System

Ultrasound imaging is widely used in non-destructive testing and medical examination because it is simple, cheap, and non-invasive [1–3]. With the development of phased array and synthetic aperture technology, the number of receiving (RX) and transmitting (TX) channels in ultrasound imaging systems is increasing to obtain a larger scan range and higher resolution [4,5]. Figure 1 illustrates a typical ultrasound imaging system.

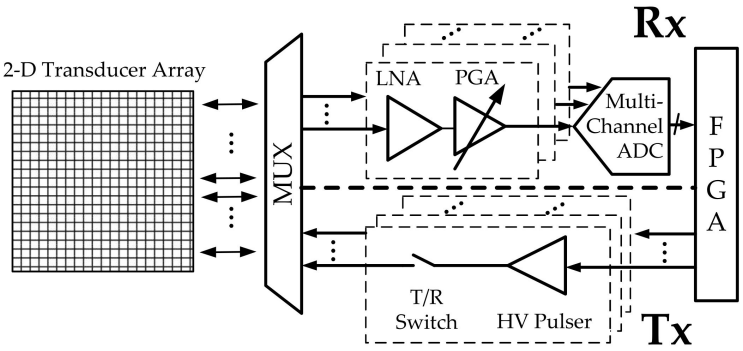

Figure 1. System diagram of an ultrasound imaging system. The arrows indicate the electronic signal flow in both Tx and Rx channels. Components surrounded by a dashed box are usually integrated into a single chip. A multi-channel ADC quantifies signals from multiple chips and sends them to FPGA.

During the TX phase, the high-voltage (HV) pulsers emit pulses that go through the transmit-and-receive (T/R) switches and the multiplexer (MUX), exciting transducers, generating ultrasonic waves. After being reflected by the target to be measured, the echo signal is converted into an electrical signal by the transducer. The electrical signal is first amplified by the low noise amplifiers (LNA), then by the programmable gain amplifiers (PGA) according to the attenuation during propagation. After being quantized by a multi-channel ADC, it is sent to a field programmable gate array (FPGA) for imaging.

The ADC often becomes the bottleneck of the whole system [6]. It not only determines the final signal-to-noise ratio (SNR) of the images but also significantly affects the complexity of the entire circuit system. The more channels integrated into a single chip, the more compact the system can be.

Therefore, the trend of ADCs for high-end ultrasound imaging systems is to increase the number of channels while maintaining high resolution [7–9]. The resolution of the ADCs is 12-bit or more. Thanks to the limited bandwidth of ultrasound signal, which is usually less than 10 MHz, the requirement for ADC sampling rate is eased. The pipelined-SAR architecture that achieves high area-and-power efficiency becomes an attractive option in such multi-channel, high-precision, medium-speed scenarios.

1.2. Pipelined-SAR ADC

Figure 2 illustrates the architecture of a pipelined-SAR ADC. Compared with the traditional pipeline architecture, SAR rather than flash ADC is adopted as the sub-ADC of each pipeline stage, achieving a good balance between conversion speed and power consumption. Each pipeline stage consists of a residue amplifier (RA) that is usually a high precision operational amplifier (op-amp) and a k_i-bit SAR ADC that includes a capacitive DAC (C-DAC), comparator, and SAR logic. Correspondingly, the operating cycle of a pipeline stage is divided into three phases: Sampling (S), SAR conversion (SAR), and Amplification (A).

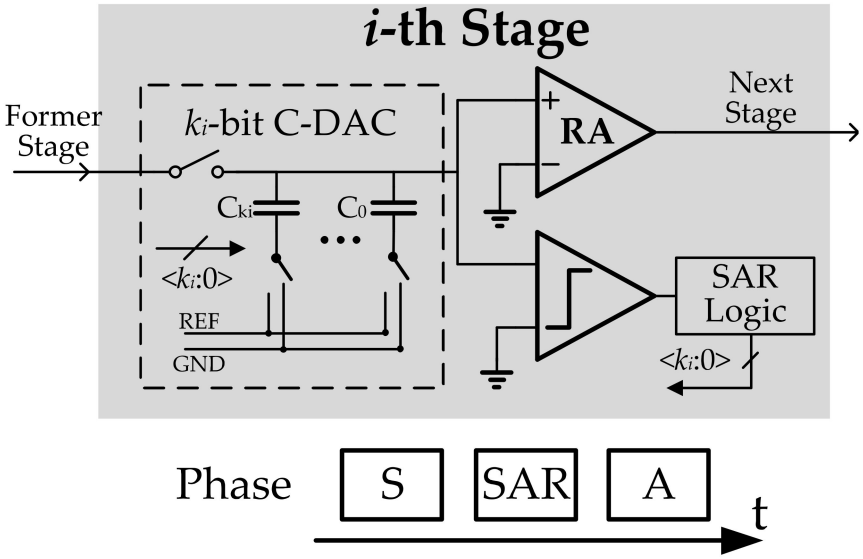

Figure 2. Block diagram of a pipelined-SAR ADC. The area marked with grey represents the critical blocks in the *i*-th stage. The detailed structure of the C-DAC, including capacitor array and sampling switch, is in the dashed box. A simplified timing diagram is drawn below.

Several efforts have been made to improve the area-and-power efficiency of pipelined-SAR ADCs, which is critical in a multi-channel application. A popular and effective improvement is to replace the power-hungry op-amps with amplifiers without DC power consumption, such as ringamp [10,11], dynamic amplifiers [12,13], or to use open-loop amplifiers [14,15]. Though these designs significantly reduce the power consumption of RA, they suffer from PVT fluctuations and often rely on complex background calibration.

Since the performance uniformity between channels is also essential in ultrasound imaging systems, traditional op-amps with a robust closed-loop structure are preferred. Another method is to use the half-gain technique, which halves the gain of the RA, reducing the signal swing and easing the requirement of RA [16,17]. However, this method requires that the reference voltages of the post-stages are also halved, increasing the complexity of the reference circuit. Op-amp sharing technique, which is popular in pipeline ADCs and can also save in power consumption of the op-amps, is seldom used in pipelined-SAR architecture because it takes extra time to eliminate memory effect, degrading the sampling rate. While for medium-speed applications, it remains effective and will be further introduced in the following sections.

In addition, many of the optimization techniques applied to SAR ADCs can also be applied to multi-stage pipeline-SAR ADCs, such as efficient switching schemes [18–20], redundant trails in SAR conversion, which alleviate the requirements for comparator offset and MSB settlement [21]. Finally, as digital circuits benefit more from process development, more designs tend to use digital calibration methods to compensate for analog circuits, such as split-channel-based architectures that can calibrate both capacitor arrays and amplifiers [22].

However, little attention is paid to another power-hungry but essential circuit block, reference, which is explained in detail in the following section. Besides, ADCs in ultrasound applications usually need to be integrated with analog frontends (AFE) and sometimes HV circuits to realize higher system integration. It leads to the necessity to use mature processes with high supply voltage to guarantee a large dynamic range, making a significant overhead of digital calibration. Thus, aggressive circuit simplification based on digital calibration is not favored.

1.3. Reference Considerations in Pipelined-SAR ADCs

In a pipelined-SAR ADC, each pipeline stage needs a pair (positive and negative) of stable references to finish the SAR conversion and to hold the residual voltage left on the top plate of the C-DAC during amplification. Figure 3 illustrates the transient waveforms of residual voltages and the output (V_{ref}) of a positive reference buffer (RB) during SAR and Amplification phase. A decreasing droop is generated on the reference during the SAR phases. Suppose the ripple does not disappear before the next trial starts; a decision error may occur, which cannot be corrected if there is no sufficient redundancy in the capacitor array. When in the Amplification phase, the ripple on the reference will cause fluctuation on the residual voltage, and a noise-like gain error may be introduced and degrades the SNR.

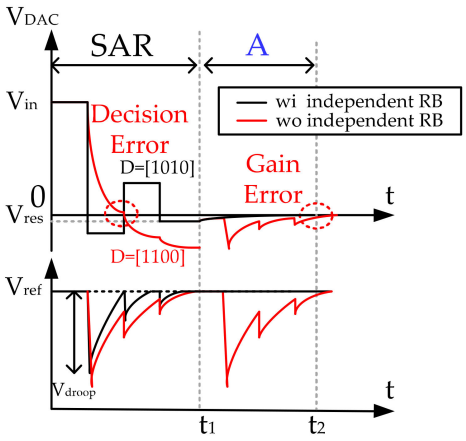

Figure 3. Transient waveforms of the residual voltage and the output of the reference buffer in one stage of a pipelined-SAR ADC. The red line indicates the situation with no independent RB, which has a larger droop in the SAR phase and unwanted function during amplification, causing possible decision error and gain error, respectively.

To reduce the ripple in the SAR phase, it is necessary to use either larger decoupling capacitors [23,24] which occupy more area, or reduce the output resistance of reference buffers [25,26], making them more power-hungry. To avoid the gain error, the reference connected to the C-DAC should be idle during the Amplification phase. Thus, allocating an independent reference buffer for each stage becomes an optimal solution [27], where significant area and power can be saved if the number of buffers needed is reduced.

According to the discussion above, a reference sharing scheme is proposed with one-third of reference buffers reduced and no performance tradeoff. The scheme is a generic method applicable to all pipelined-SAR ADCs with three or more stages, effectively improving the area-and-power efficiency.

Based on the reference sharing scheme, a calibration-free, 16-channel, 50-MS/s, 14-bit ADC for ultrasound imaging systems is designed and measured. The area-and-power efficiency of the ADC is further improved by the op-amp sharing technique and optimization of the stage resolution distribution. The proposed ADC is fabricated in a 0.18-µm process. The measurement results show that it achieves a robust and competitive performance without calibration, and can be easily further integrated with AFEs.

This paper is organized as follows. Section 2 explains the proposed reference sharing scheme used in multi-stage pipelined-SAR ADCs. Section 3 analyzes the impact on the area and power consumption caused by stage resolution distribution, proposing an optimized architecture for a 14-bit resolution ADC. Sections 4 and 5 show the structure and circuit implementation of the proposed ADC. Measurement results are shown in Section 6. Section 7 concludes this paper.

2. Reference and Op-Amp Sharing in Pipelined-SAR ADCs

2.1. Proposed Reference Sharing Scheme

Figure 4 shows the connections and the operating phases of the proposed reference sharing scheme between three adjacent pipeline stages (S_{i-1}, S_i, and S_{i+1}). One-third of reference buffers are reduced with only a little extra cost of switches and no loss on performance. It is also compatible with the op-amp sharing technique similar to [28], which further improves the area-and-power efficiency. For simplicity, only single-ended circuits are drawn. RB1 and RB2 represent two independent reference buffers. The Sampling, SAR, and Amplification phases are designed to each take one-third of the operating cycle, which is easy to realize in medium-speed scenarios.

In phase (a), S_{i-1} is in the sampling phase, connected to input common-mode voltage (not drawn in the figure). And S_i performs SAR conversion, drawing charge from RB2. S_{i+1} is connected to RB1 to hold the residual voltage. In the next phase (b), S_{i-1} is connected to RB1 for SAR conversion, and S_i is connected to the idle RB2. The shared residual amplifier is connected between S_i and S_{i+1}. S_{i+1} is in the sampling phase. In the last phase (c), the residue voltage held by RB2 in S_{i-1} is amplified. S_i samples while RB1 charges S_{i+1}.

With this reference sharing scheme, only two pairs of references are alternately connected to any three adjacent pipeline stages. A reference buffer serves only one stage in SAR conversion, and an idle reference is always connected to the stage in the Amplification phase. Hence, the risk of decision error and gain error are eliminated.

Figure 5 compares the described scheme in (a) and an alternative implementation in (b). In Figure 5b, each stage connects to both reference buffers, thus fully mitigating the offset caused by mismatches between the references. Compared with (b), the connection of references in Figure 5a is much simpler, and the offset in S_{i-1} which is more critical, is also eased. In addition, in this scheme, RB2 is only used for S_i charging, whose capacitance load is smaller than S_{i-1}, as a result the power consumption of RB2 can be further reduced.

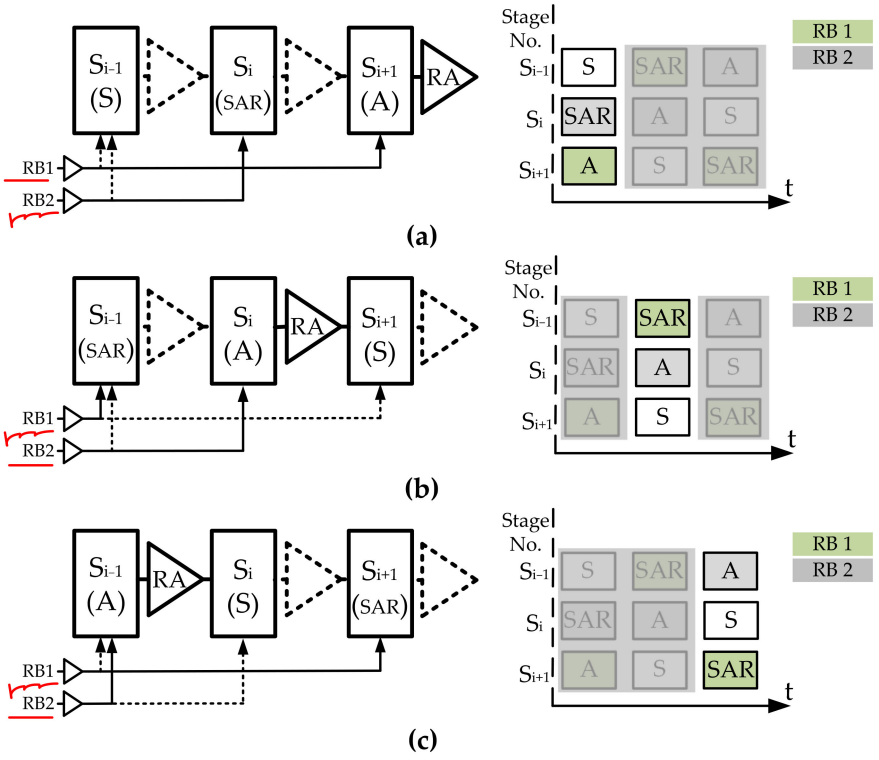

Figure 4. The phases and the connection of the reference sharing scheme along with op-amp sharing. Two reference buffers are connected to three adjacent stages (**left**). The solid and dotted lines represent the alternately connected paths. The current phase is highlighted in the timing diagram of each stage (**right**). The connected buffers are marked with green and grey. (**a**) RB1 idle, RB2 charging Si; (**b**) RB1 charging S_{i-1}, RB2 idle; (**c**) RB1 charging S_{i+1}, RB2 idle.

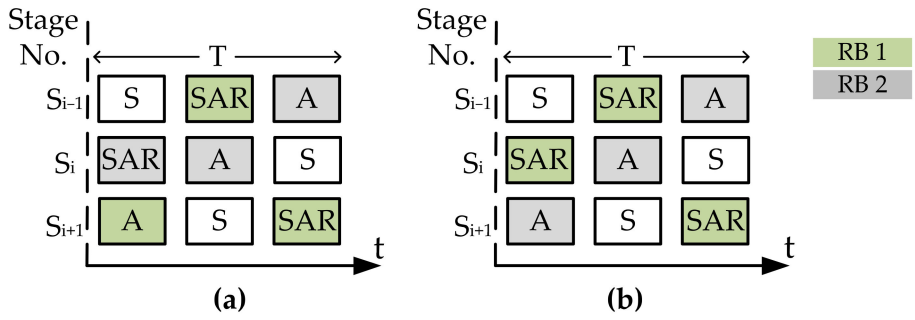

Figure 5. Two possible implements of the reference sharing scheme. The connection differs in the S_i and S_{i+1} where (**a**) references not exchanged and (**b**) references exchanged with each other.

2.2. Op-Amp Sharing in the Proposed Scheme

In conventional pipelined ADCs, the primary concern of op-amp sharing is the memory effects that will degrade settlement accuracy and sampling rate. This problem worsens in pipelined-SAR ADCs because SAR conversion takes up extra time, resulting in less time available for the op-amp to reset. When applying the proposed scheme, this dilemma is alleviated because the settlement requirement of S_i is less than that of S_{i-1}, a part of the settlement time is saved and a reset phase can be inserted after phase (b). Besides, after phase (c) there is a long idle time (phase (a)) to completely eliminate the residual charge.

The op-amp can also be biased differently in phase (b) and (c) to reduce power consumption. The detailed timing diagram and circuit implementation are shown in Sections 4 and 5.

3. Architecture Optimization Based on Reference/Op-Amp Sharing

As explained in Section 1, the area-and-power efficiency rather than sampling rate is more essential in the multi-channel ultrasound imaging system. Based on the reference/op-amp sharing scheme, the efficiency can be further improved by optimizing the number of stages and the stage resolution distribution. In this section, the effectiveness of sharing is first compared in different architectures. In order to better measure the design cost of these architectures, a unit capacitance-based analysis method which eliminates the impact introduced by the process and circuit design is explained. And finally, an optimized architecture is proposed for the 14-bit design target. Its superiority is demonstrated by comparison with other possible implementations.

3.1. Reference and Op-Amp Sharing in Different Architectures

Figure 6 presents the timing diagram of three pipelined-SAR ADCs with a different number of stages. The application of sharing scheme is also illustrated. A two-stage pipelined-SAR ADC in (a) cannot share op-amp and reference. A four-stage pipelined-SAR ADC in (c) needs only a single op-amp, but three references are required, even with reference sharing. For a three-stage architecture in (b), the sharing scheme maximizes the efficiency with one op-amp and only two references are shared between stages. A detailed comparison of area and power consumption [29,30] of these pipelined-SAR ADCs is made in the following sections.

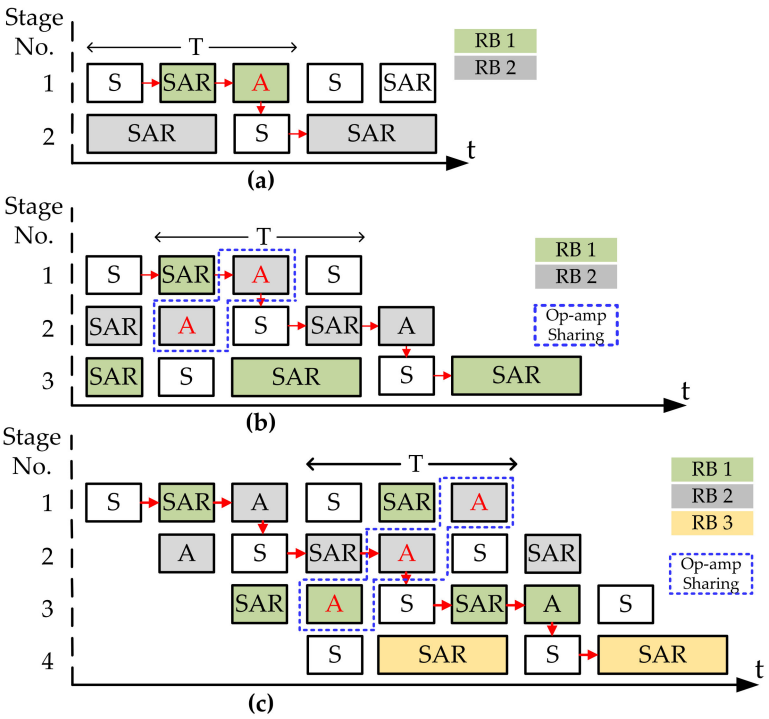

Figure 6. The timing diagram of pipelined-SAR ADCs with (**a**) two stages, (**b**) three stages, and (**c**) four stages. In each timing diagram, the signal flow is represented with red arrows. The blue dashed box means that the amplification in different phases is finished with a shared op-amp. The needed reference buffer is marked with different colors.

3.2. Principle of Area and Power Consumption Analysis

To focus on the optimization of architectures, it is necessary to exclude the offset brought by the process and circuit design, and then a fair comparison can be made. It is achieved by normalizing the design cost of area and power to the unit capacitor provided by each process. The principle is detailed presented as follows.

3.2.1. Area Analysis

The area of a pipelined-SAR ADC can be expressed as:

$$A_{total} = \sum_{i=1}^{M} A_{stage,i} + N_{op} \times A_{op} + N_{ref} \times A_{ref} \quad (1)$$

where A_{total}, $A_{stage,i}$, A_{op}, and A_{ref} represent the area of an M-stage ADC, the i-th stage, the op-amp, and the reference (including decoupling capacitors), respectively. The number of amplifiers (N_{op}) and reference (N_{ref}) can be reduced by reference/op-amp sharing.

$A_{stage,i}$ is composed of several unit capacitors ($A_{ucap,i}$) and active parts ($A_{active,i}$) in this stage, including comparators, SAR logic, and switches. The number of unit capacitors is exponentially related to the stage resolution (k_i) and is modified by different switching schemes (usually 2^{k_i} capacitors are needed). The unit capacitor in each stage may also scale down according to the linearity and noise requirement. And since the active parts drive the capacitors (ignoring the relatively small comparators), it is reasonable to assume that $A_{active,i}$ is proportional to the capacitance.

In Equation (2), the area of one stage is normalized to the unit capacitor (A_{unit}) provided by the process. α is the proportional coefficient between the size of capacitors and active parts, x is the scaling "taper factor" that is mostly around $\sqrt{2}$ [31], and γ is the ratio between unit capacitor used in the first stage and the unit capacitor provided by the process ($A_{ucap,1}/A_{unit}$).

$$A_{stage,i}(k_i) = 2^{k_i} A_{ucap,i} + A_{active,i} = (1+\alpha)2^{k_i} A_{ucap,i} = (1+\alpha)x^{1-i}2^{k_i}\gamma A_{unit} \quad (2)$$

Bringing Equation (2) into (1), Equation (3) shows that the overall area is determined by the stage resolution distribution (k_i) and the number of op-amps (N_{op}) and references (N_{ref}). The coefficients (α, x, γ) reflect the impact caused by the process and circuit design.

$$A_{total} = \sum_{i=1}^{M} \left[(1+\alpha)x^{1-i}2^{k_i}\gamma A_{unit} \right] + N_{op} \times A_{op} + N_{ref} \times A_{ref} \quad (3)$$

3.2.2. Power Consumption Analysis

The total power consumption (P_{total}) of an M-stage pipelined-SAR ADC is made up of switching power of capacitors in each stage ($P_{stage,i}$), power of residue amplifiers (P_{op}), and references (P_{ref}), as listed in Equation (3).

$$P_{total} = \sum_{i=1}^{M} P_{stage,i} + N_{op} \times P_{op} + N_{ref} \times P_{ref} \quad (4)$$

For simplicity, the difference between the residue amplifier and the reference buffer of each stage due to scaling down is neglected.

Because the power consumption of each stage ($P_{stage,i}$) under a given sampling rate is also determined by unit capacitors and corresponding active parts, the expression is similar to the analysis of the area in Equation (2). Replacing A_{unit} with the switching power of a unit capacitor (P_{unit}), the normalized $P_{stage,i}$ is represented in Equation (5). And β is the proportional coefficient of active parts to the capacitors in each stage.

$$P_{stage,i}(k_i) = (1+\beta)x^{1-i}2^{k_i}\gamma P_{unit} \quad (5)$$

Combing Equations (4) and (5), the overall power consumption is also determined by k_i, N_{op} and N_{ref}, as shown in Equation (6).

$$P_{total} = \sum_{i=1}^{M} \left[(1+\beta) x^{1-i} 2^{k_i} \gamma P_{unit} \right] + N_{op} \times P_{op} + N_{ref} \times P_{ref} \quad (6)$$

3.3. Proposed Area-and-Power Efficient Three-Stage Architecture for a 14-Bit ADC

According to the discussion of the sharing effectiveness in Section 3.1, a three-stage architecture can maximally utilize the shared reference and op-amp (in other words, N_{op} and N_{ref} are reduced). Thus, an area-and-power efficient three-stage architecture with optimized stage resolution distribution (k_i) is proposed for ADCs with 14-bit resolution and medium sampling rate. The resolution of each stage is 5-bit, 5-bit, and 6-bit, respectively, with a 1-bit inter-stage redundancy.

Table 1 lists other designs that also achieve 14-bit resolution and a similar sampling rate with different stage resolution distributions. They also have a 1-bit inter-stage redundancy. For three- and four-stage architectures, the resolution of pipeline stages is set to be the same to reduce the complexity of timing. Each design's area and power consumption are normalized to the unit capacitor in each process according to Equations (3) and (6). The area and power consumption of a single op-amp and reference (including the buffer and the decoupling capacitor) compared to the unit capacitor are listed in Table 2. It is based on the measurement results of these reference designs and statistical results in [23].

Table 1. Comparison between architectures.

Architecture	Resolution Distribution (k_i) *	Case No.	Number of Op-Amp (N_{op})		Number of References (N_{ref})	
			Original	With Op-amp Sharing	Original	With Reference Sharing
2-stage PPL-SAR	6b + 9b [32]	i	1	1	2	2
	7b + 8b [21]	ii	1	1	2	2
3-stage PPL-SAR	4b + 4b + 8b	iii	2	1	3	2
	5b + 5b + 6b (this work)	iv	2	1	3	2
4-stage PPL-SAR	4b × 3 + 5b [33]	v	3	1	4	3

* The circuit-design and process-related coefficients (α, β, x, γ) will change the absolute values of area and power consumption, but not the relative relationships in the comparison. They are set based on the used 0.18-µm process as follows: α is 0.5, β is 0.2, x is 1.4. γ is mainly determined by the linearity of capacitors and is set to 2.

Table 2. Ranges of the area and power normalized to the unit capacitor.

Circuit Block	Range of Area (A/A_{unit})	Range of Power (P/P_{unit})
Residue Amplifier *	100–400	10–200
Reference *	200–400	100–500

* For simplicity, the median of the range is used, and the result is not changed by the value chosen.

As shown in Figure 7, the superiority of the proposed architecture is demonstrated, achieving both the least normalized area and power. For all architectures, the area and power consumption of capacitors decrease with the increase of the number of stages. If with three or more stages, the op-amp and reference rather than capacitors dominate the design cost. Because of op-amp sharing, only a single op-amp is used in all of these architectures. The number of references becomes the key that distinguishes the three-stage from the four-stage architecture, where the three-stage architecture requires one less reference, saving significantly more area and power.

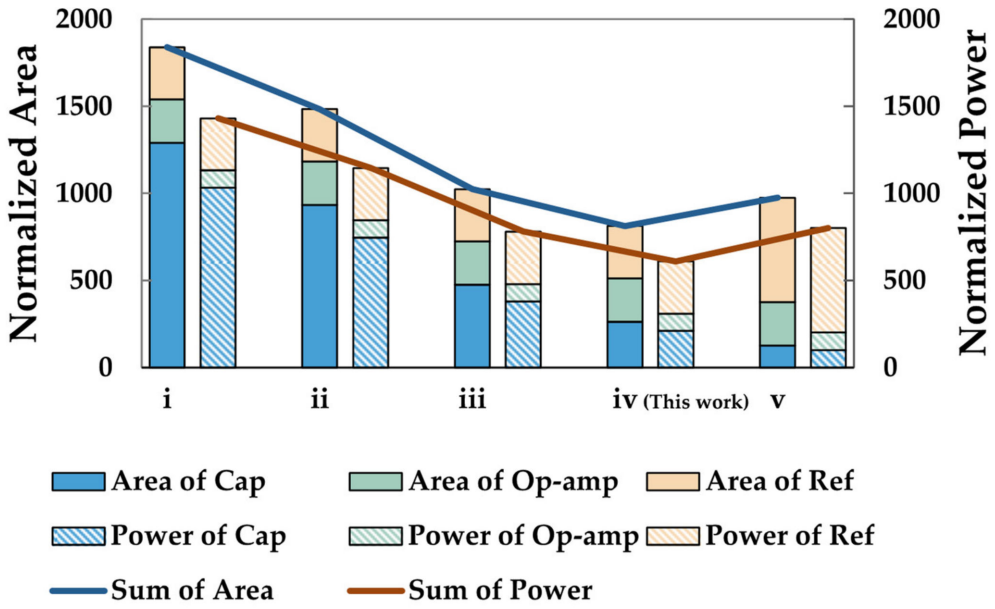

Figure 7. Comparison of area and power between different architectures. Each component in the stacked bar is marked with different colors and grains, as illustrated below. The normalized area and power are compared in left and right, respectively. The trend lines of the sum area (blue) and power (brown) indicate that the architecture in this work achieves the best efficiency.

Between the two three-stage architectures, the proposed "5-5-6-bit" architecture balances the capacitance of each stage better, hence achieving better area-and-power efficiency than the other.

3.4. Summary of This Section

In this section, the effectiveness of reference/op-amp sharing is compared and a generic analysis method for the area and power consumption of pipelined-SAR ADCs is presented. Combing these two, a three-stage architecture with a "5-5-6-bit" stage resolution distribution is proposed. Its area-and-power efficiency is the best in comparison with other architectures, thus it is adopted in the targeted 14-bit 50 MS/s ADC design.

4. Proposed Three-Stage Pipelined-SAR ADC

4.1. Overall Structure

Figure 8 shows the overall structure of the proposed ADC. It consists of 16 independent sub-channel ADCs and peripheral circuits, including LVDS, serial peripheral interface (SPI), bandgap, phase-locked loop (PLL). Each sub-channel ADC realizes a 14-bit resolution with a 50 MS/s sampling rate, and the quantization results are converted into serial output by LVDS. A 50-MHz frame clock (FCO) and a 700-MHz data clock (DCO) are also outputted.

The main part of each sub-channel ADC is a three-stage pipelined-SAR ADC with a "5-5-6-bit" resolution distribution. There is 1-bit redundancy between each stage to eliminate the risk of an overflow caused by comparators' offset, and a taper factor of 1.4 is applied in the unit capacitance. The sub-ADCs of the first two stages are asynchronous. The residual voltage of each stage is amplified 16 times through a shared op-amp. The third stage uses synchronous timing SAR logic to finish the left 6-bit quantization. The outputs of three stages are added in ADDer, where the least significant bit (LSB) of the former stage overlaps with the most significant bit (MSB) of the latter stage, generating the final 14 bits output. Each sub-channel ADC has its own reference, guaranteeing it is not affected by adjacent channels.

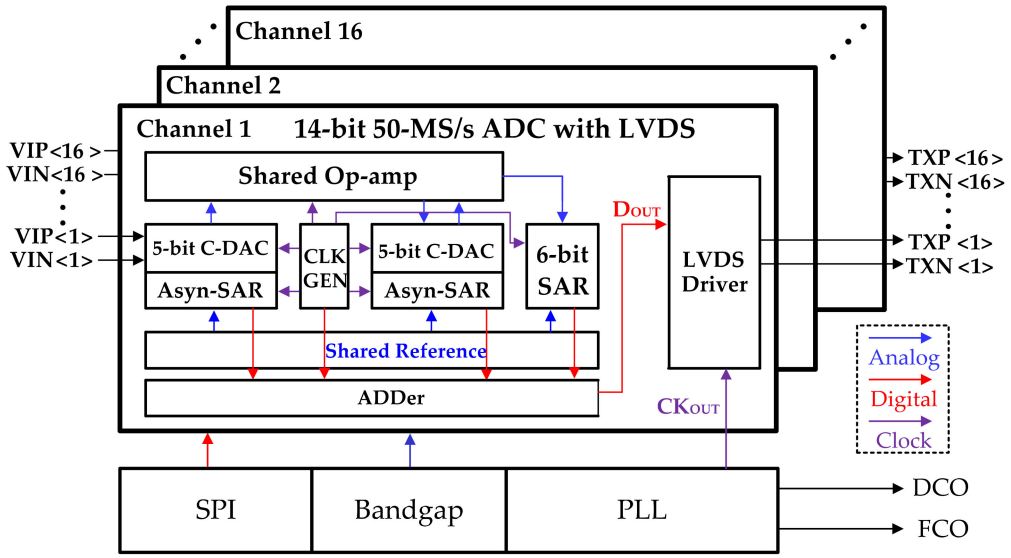

Figure 8. The overall structure of the proposed ADC. The ADC has 16 channels and each channel is drawn in the solid line box, including three sub-stages, the shared reference/op-amp and LVDS. The peripheral circuits shared by all channels are drawn below. As illustrated right, different signal flows are marked with arrows with different colors.

4.2. Timing Diagram

The detailed timing diagram of the proposed ADC is shown in Figure 9. In the first and second stage, each Sampling, SAR, and Amplification phase takes roughly one-third of the cycle. After sampling, the asynchronous SAR ADC finishes five trials, and then the shared op-amp starts to work in the two adjacent phases ($\varphi_{AMP,1}$ and $\varphi_{AMP,2}$). Due to the relaxed settlement requirement, $\varphi_{AMP,2}$ is a little shorter than $\varphi_{AMP,1}$, and a quick reset phase (0.6 ns) is inserted between them. The third stage has a longer time for SAR conversion. Therefore, a simple and robust synchronous timing logic is adopted, generating the last six bits.

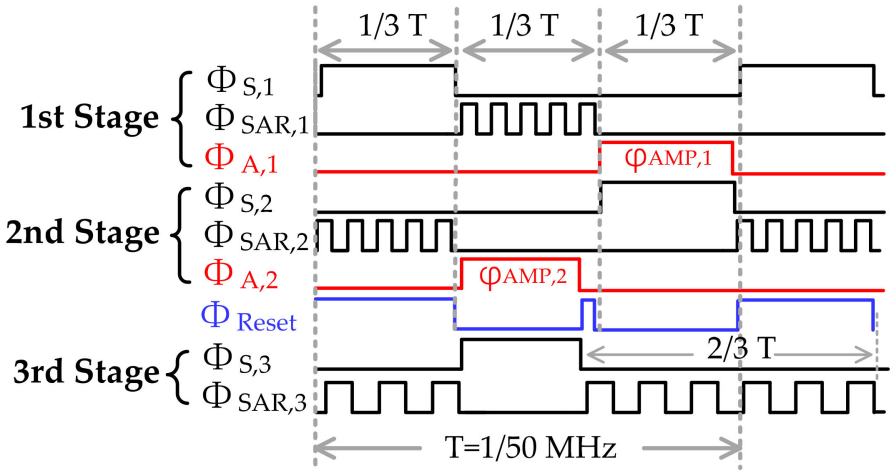

Figure 9. The timing diagram of the proposed ADC. The detailed phase clock of each stage is grouped. The shared op-amp has two operating phases (red line), and the Reset phase (blue line) is inserted between them. The Sampling, SAR, and Amplification phases each take one-third of the period.

5. Circuit Implementation

5.1. Shared Reference

The shared reference in this design is shown in Figure 10. Figure 10a shows the circuit implementation, where a master-slave architecture is adopted, consisting of a feedback loop and two open-loop buffer branches. The common-mode voltage (V_{cm}) is also generated by a similar branch and is neglected for simplicity. All of the source followers are composed of NMOS transistors, which are more efficient in converting current to transconductance (gm/I_D) than PMOS transistors, thus reducing power consumption and parasitic introduced by the transistors [34].

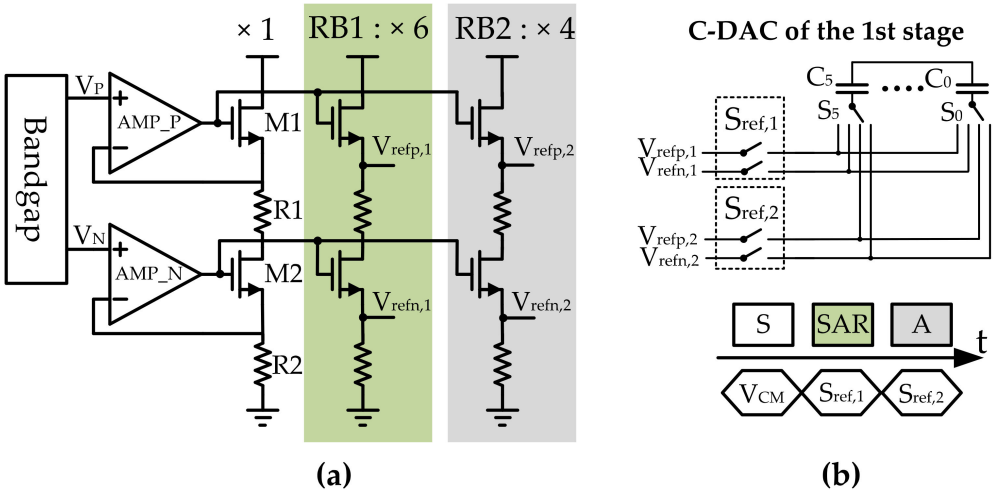

Figure 10. (**a**) The circuit implementation of the shared reference. The feedback loop with error amplifiers is on the left. Two references are marked with different colors. The number of branches is also annotated. (**b**) Implementation of the reference sharing in the 1st stage. The two pairs of switches for sharing are in the dashed box. The corresponding timing diagram is also drawn below, where $S_{ref,1}$ is connected in the SAR phase and $S_{ref,2}$ in the Amplification phase.

In the feedback loop, the two error amplifiers with different input pairs are biased in the subthreshold region to save power. M1, M2, and R1, R2 determine the operation point of the buffer branches.

The driving capability of the branches is designed differently according to the discussion in Section 2.2. The settlement requirement of RB2 is eased since it only needs to charge the second stage. The number of branches is reduced accordingly.

Figure 10b shows the circuit implementation and the operation phases of reference sharing in the C-DAC of the first stage. Each capacitor connects to both references through two pairs of switches ($S_{ref,1}$ and $S_{ref,2}$). During the SAR phase, $S_{ref,1}$ is close with $S_{ref,2}$ open and RB1 charges the C-DAC. Then in the Amplification phase, $S_{ref,1}$ is open with $S_{ref,2}$ close, and RB2 provides the idle reference to hold the residue voltage.

5.2. Shared Op-Amp

In this design, the shared op-amp adopts a two-stage Miller-compensated architecture with high PVT robustness (Figure 11). The output stage uses a push–pull architecture with switched-capacitor common-mode feedback (SC-CMFB), whose details are omitted in the figure for simplicity. The amplifier achieves a gain-bandwidth product (GBW) of 2.8 Giga with 118.7-dB dc gain and 65° phase margin when operating for the first stage.

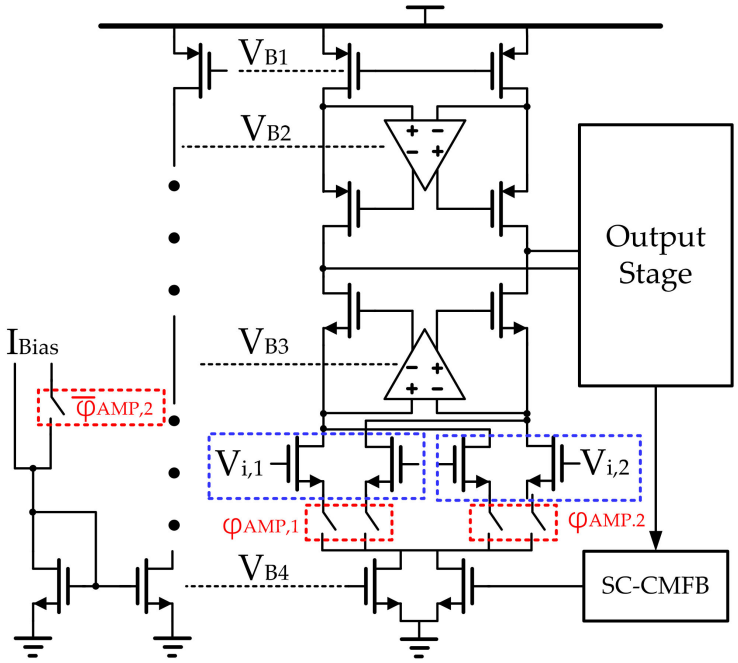

Figure 11. The shared op-amp with adjustable bias. The two input pairs for different inputs are in the blue dashed box, along with their control switches in the red box. When operating for the 2nd stage, the switch on I_{Bias} (**left**) is open, reducing the overall bias current and saving power.

To reduce the memory effect, the amplifier uses two independent input pairs ($V_{i,1}$ and $V_{i,2}$) for the first and second Amplification phase ($\varphi_{AMP,1}$ and $\varphi_{AMP,2}$). During the reset phase described in Section 4.2, both pairs of input transistors are connected to the input common-mode voltage to eliminate the residual charge.

To further reduce power consumption, the op-amp uses an adjustable bias. Since the load capacitance is smaller and the settlement requirement is eased in the second Amplification phase, the quiescent operating current of the op-amp can be reduced. It is realized by reducing the bias current inputted to the bias network, thus changing the DC operating points in the op-amp. In this way, 25% of the power consumption is reduced, and the GBW is reduced to 2 Giga with 72° phase margin.

5.3. Layout Considerations

Since it is necessary to integrate 16 channels of the proposed ADC in a single die, the overall floorplan needs to be fully considered during the top-level design. Considering the high design and testing cost of the ball grid array (BGA) package, a quad flat package (QFP) package is adopted with its pins laid around the package. Accordingly, each channel of the ADC is designed as a slim rectangle to place the input/output pins on the left and right sides of the package, and the 16 channels are lined up in a row. Due to the elongated shape, the distance between each stage is stretched. Especially when the reference sharing scheme is applied, RB1 needs to connect both the first and third stages, running through the entire chip. Therefore, the parasitic capacitance and resistance introduced by wiring are carefully simulated to minimize the RC time constant and to prevent settlement errors. In addition, the LVDS of all channels share the same clock, so the clock distribution network of the PLL is also balanced to ensure a consistent clock phase. Finally, the supply network is simulated and verified by electromigration analysis.

6. Measurement Results

Figure 12a shows the photograph of the proposed single-channel ADC, where each circuit block is designed as a long skinny rectangle. The shared op-amp and reference are beside the three stages. The area of the single-channel ADC is 2 mm × 0.25 mm. Figure 12b

shows the photograph of the whole chip. SPI, bandgap, and PLL locate between the top and bottom eight channels. Figure 12c is the packaged chip and the socket test board for batch testing.

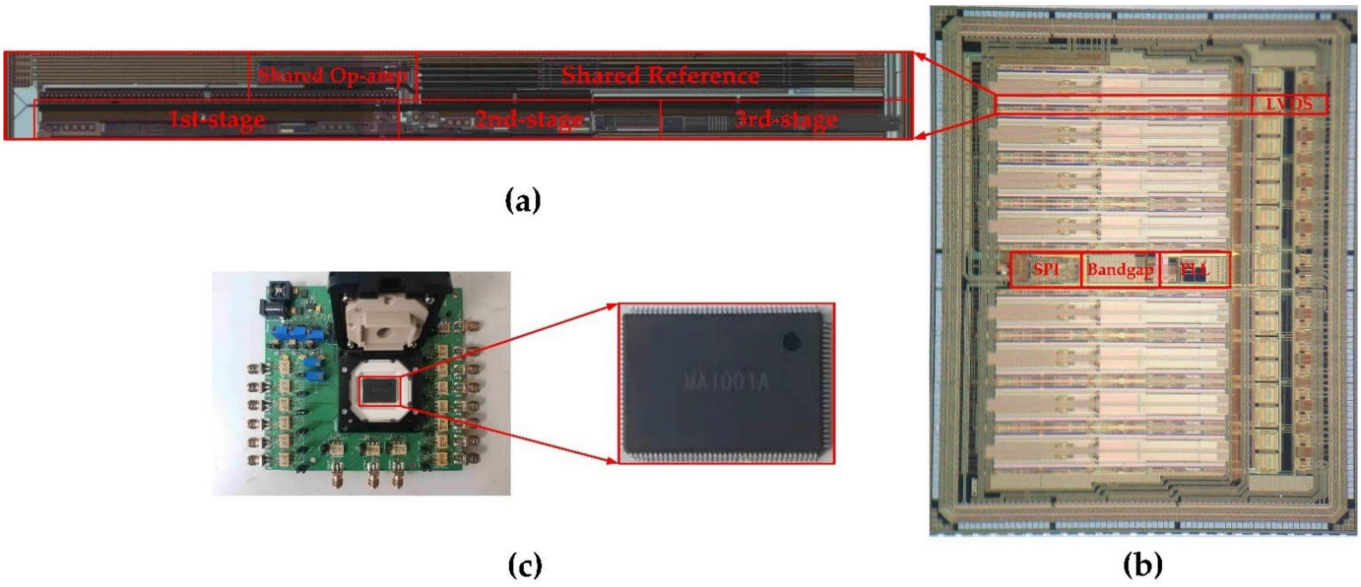

Figure 12. Photograph of (**a**) single-channel ADC, with main blocks marked in the red box; (**b**) 16-channel ADC with peripheral circuits integrated, which are also annotated; and (**c**) package and the batch test board with a socket.

Figure 13 shows the measured static performance. The test is done with a 2.4-MHz sinusoidal input signal and 50-MHz sampling frequency under a 1.8-V supply. The measurement result is analyzed by code density, and the calculated differential nonlinearity (DNL) error and integral nonlinearity (INL) error is −0.46/0.6 LSB and −2.53/1.32 LSB, respectively.

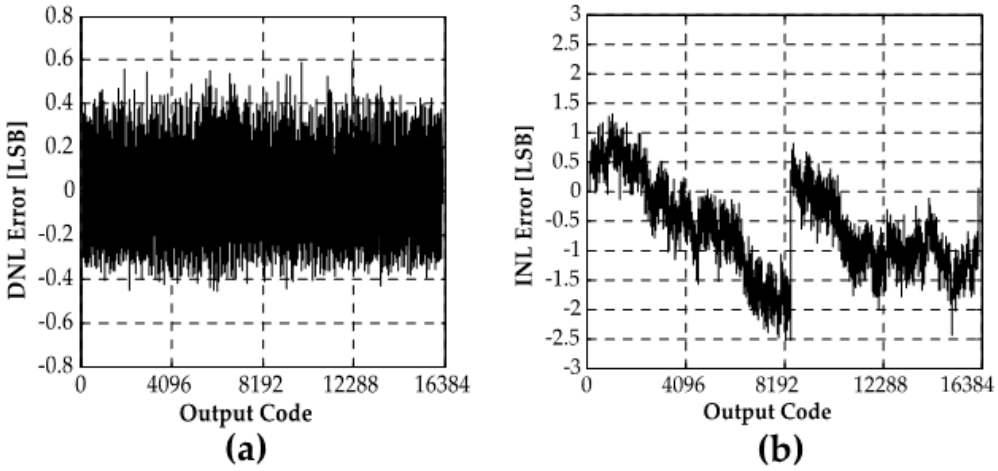

Figure 13. Measured (**a**) DNL error and (**b**) INL error. The DNL error and INL error is −0.46/0.6 LSB and −2.53/1.32 LSB, respectively. They are calculated from a histogram test with full-swing input and 16,384 sampling points.

Figure 14a. shows a typical dynamic performance of the ADC, achieving an SFDR of 82.19 dB, and an SNDR of 68.25 dB at 2.4-MHz input. Figure 14b shows the measured dynamic performance versus input frequency up to 70 MHz. This ADC maintains stable SFDR and SNDR performance in the second Nyquist zone, making it suitable for second harmonic ultrasound imaging. And the performance is uniform for different channels with

a 1.9 dB standard deviation of SNDR among more than 50 test chips. It is also tested from −30 to 80 °C with only slight performance loss.

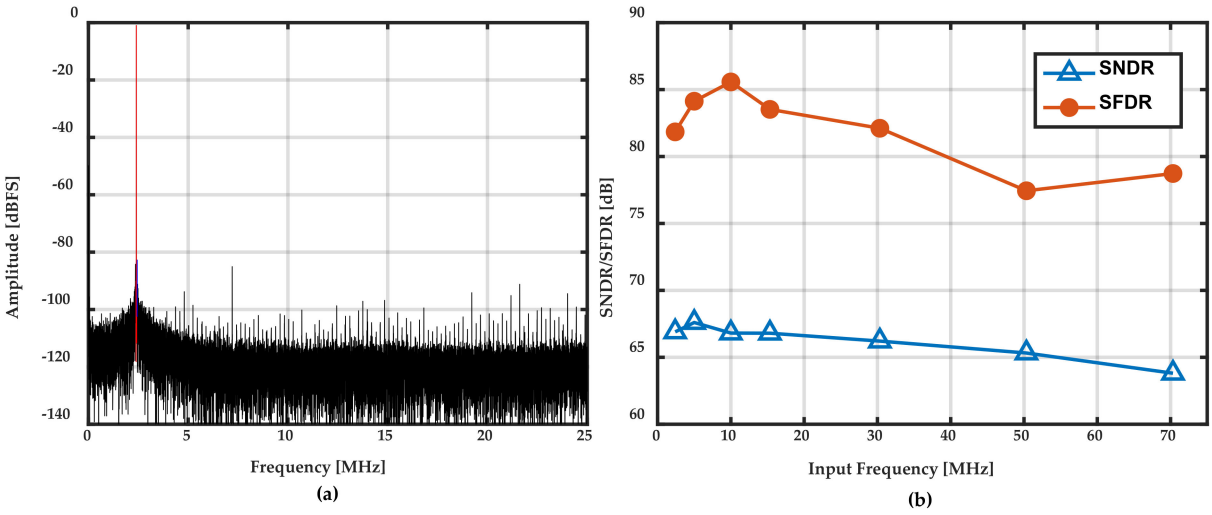

Figure 14. (**a**) Measured output amplitude in the spectrum with 2.4-MHz input, achieving an SFDR of 82.19 dB, and an SNDR of 68.25 dB; (**b**) dynamic performance versus input frequency. The SNDR is drawn in blue and SFDR in red. Used test frequencies are also marked with points and triangles.

When integrating the 16 channels, each channel is surrounded by guard rings. Sensitive signals are also protected by shield wires. The measured crosstalk coefficient between two adjacent channels is −65 dB and slightly changed under different input frequencies, which are mainly introduced by bonding wires and the testing board.

The power breakthrough of a single channel is shown in Figure 15. All other peripheral circuits consume 12 mW/channel on average. The core consumes 49.5 mW (references not included), translating into an FoM of 0.47 pJ/conversion-step. Though limited by the process which leads to high total power consumption, the effectiveness of reference sharing is verified with 15% power saved. The three-stage pipelined-SAR architecture combing both reference and op-amp sharing scheme achieves an estimated 30% power reduction, showing great potential in further applications.

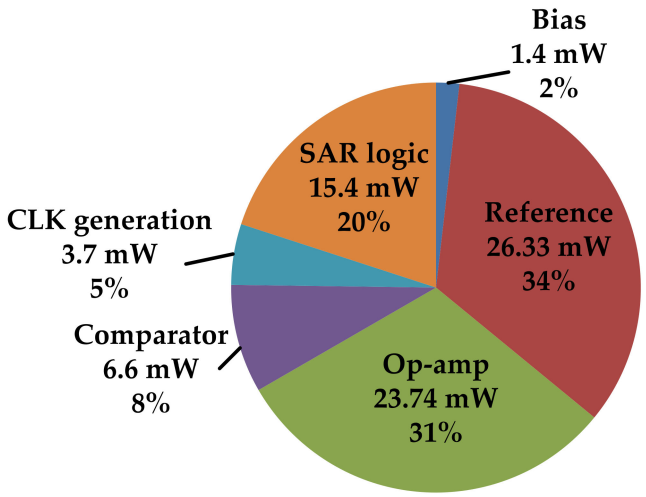

Figure 15. Power breakthrough of the proposed ADC. The power consumption of each block is annotated with its percentage. With the reference/op-amp sharing, 30% power is saved from the reference and op-amp, which are the most power-hungry blocks.

Table 3 summarizes the performance and compares it with other ADCs. Compared with ADCs with 14-bit resolution and similar sampling rate [32,35,36], the proposed ADC integrates more channels in a single chip and achieves a comparable SNDR performance without any calibration. The area efficiency is demonstrated especially compared to [36], which is also designed in a 0.18-µm process. And compared with the ADCs reported for ultrasound imaging systems [37,38], the proposed ADC achieves higher resolution and a competitive FoM.

Table 3. Performance summary and comparison.

	[32]	[35]	[36]	[37]	[38]	**This Work**
Technology	65 nm	65 nm	180 nm	180 nm	130 nm	180 nm
Architecture	Pipelined-SAR	Split-Pipeline	Pipeline	SAR	Sigma-Delta	Pipelined-SAR
Number of Channels	1	1	1	8	128	16
Sampling Rate (MS/s)	75	100	60	20	20	50
Resolution (bit)	14	14	14	12	12	14
SNDR (dB)	77.8	68.5	76.9	58.2	65	68.25
SFDR (dB)	92.1	84.4	91.2	N/A	58	82.19
Power/channel [a] (mW)	24.9	32	67.8	2.6	17	49.5
Area/channel (mm^2)	0.342 [b]	0.38	1.43	0.26	N/A	0.625 [b]
FoM [c] (pJ/conv-step)	0.052	0.147	0.198	0.196	0.585	0.469
Calibration	Background	Background	Background LMS	Beam-forming	Background	Not required

[a] Core power consumption. [b] With on-chip reference buffer. [c] Walden FoM = Power/($2^{ENOB} \times$ Fs).

7. Conclusions

In this paper, a reference sharing scheme that is suitable for medium-speed, high-resolution, pipelined-SAR ADC is proposed. Based on this, a three-stage architecture with reference/op-amp sharing and optimized stage resolution distribution is proposed and verified. A prototype 16-channel ADC is designed and measured in a 0.18-µm process with 14-bit resolution and a 50-MS/s sampling rate. The measurement results show that the proposed architecture can save up to 30% power with no cost to performance, achieving high area-and-power efficiency, which is suitable for ultrasound imaging systems.

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